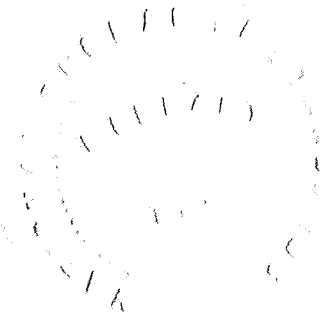
UNITED STATES DEPARTMENT OF COMMERCE • Sinclair Weeks, *Secretary*
NATIONAL BUREAU OF STANDARDS • A. V. Astin, *Director*

Computer Development (SEAC and DYSEAC) at the National Bureau of Standards Washington, D. C.



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Foreword

Since 1946 the National Bureau of Standards has been active in the general field of electronic digital computers, largely for other agencies of the Government. The Bureau's computer program has been conducted jointly by the Electronics Division and the Applied Mathematics Division. The work of the Electronics Division in Washington has included the development and construction of two computers (SEAC and DYSEAC), components research and development, and various technical and advisory services. The work of the Applied Mathematics Division has included research in numerical analysis of importance in the solution of problems by computers and the design and construction of a computer (SWAC) at the Bureau's Institute for Numerical Analysis in Los Angeles.

This volume presents reports on various aspects of the computer program through 1953, based largely on the work and experience relating to SEAC and DYSEAC. Such topics as systems development, engineering development, design, construction, and maintenance of computer equipment are covered. The introduction summarizes the history of this program in the Electronic Computers Laboratory of the Electronics Division.

A. V. Astin, *Director.*

Contents

Introduction

S. N. Alexander

The development of electronic digital computing machinery at the National Bureau of Standards started in 1946 because of the interest of the Bureau of the Census in the possible use of electronic digital techniques for tabulating purposes. In particular, the Bureau of the Census hoped to attain trial use of an electronic installation in connection with the 1950 decennial census, and the National Bureau of Standards was asked to provide technical guidance and developmental support to this long-range program. Concurrently, NBS was seeking to obtain an electronic digital computer as a scientific instrument for its own use. Immediately following the establishment of these two tasks, a 2-year program for the development of improved components for digital computers was established under the sponsorship of the Office of the Chief of Ordnance, Department of the Army.

The relatively short time schedule desired for the delivery of the two complete machine installations, together with suitable auxiliaries and operational supplies, made it advisable from the outset to seek commercial sources for such equipment. In this way, it seemed possible to compress the research, development, and construction of such equipment into an integrated effort and thereby meet the time schedules. This decision was buttressed by further requirements from the Office of Air Comptroller, Department of the Air Force, and the Army Map Service for similar equipment with comparably short time schedules. NBS agreed to serve as technical agent in monitoring the design, construction, and installation of these machines from two commercial suppliers, while its own laboratories were fully occupied with the component development program.

Because of an unanticipated sequence of technological and contractual difficulties, it became evident early in 1948 that the delivery of complete machine installations would be delayed considerably beyond the target dates. The unexpected difficulties associated with the developmental phases of all such programs, both commercial and university, emphasized the uncertainty of availability of electronic digital computing facilities of any sort. This motivated a request for a "stopgap" installation to serve some of the urgent needs of both the Air Comptroller and NBS during the interim period until full-scale equipment could be obtained from commercial sources within a more realistic time schedule. During the summer of 1948, NBS explored the possibilities of designing and constructing an interim machine that would have sufficient power for general use and yet be simple enough to be constructed in a short time. The feasibility of this program was based on the preceding 2 years of active experience in component development and the availability of the best technology that had been reported by other computer groups, particularly those in the universities.

The original modest objectives for an interim machine were reconsidered toward the end of 1949, when it became evident that the proposed SEAC computer would be the only equipment available to NBS and collaborating Government agencies for at least 2 years. To cope with this altered situation, the plan for the machine was adjusted so that a full-scale installation could be attained by subsequent expansion of an initial nucleus. However, the prime objective was still to have the initial nucleus in operation at the earliest possible date. The resulting machine began useful operation in May 1950, less than 2 years after the start of the program, and SEAC completed nearly a year of scheduled operation for NBS and its collaborators before any other installation was available to them. Furthermore, SEAC was the one installation that was readily available to serve the intermittent computational needs of many other Government agencies, and for over 2 years was used on a round-the-clock basis for the full 7-day week. Even now, after 3 years of regularly scheduled operation, the SEAC is still employed for an extended work week in the solution of problems.

The task of designing a large-scale digital computer such as SEAC from original conception to final realization was, of course, the effort of many minds and the work of many hands. The team chosen for this task encompassed a wide spectrum of talents and skills. The successful completion of SEAC at a time when the availability of such a facility was of urgent importance to the Government was recognized by the Award for Exceptional Service from the Department of Commerce to the

SEAC staff as a group. In addition to this group-citation to the 33 scientists and technicians who contributed to the SEAC accomplishment, particular mention was made of the individual contributions by S. N. Alexander, W. W. Davis, R. D. Elbourn, S. Greenwald, R. C. Haueter, A. L. Leiner, S. Lubkin, C. H. Page, J. L. Pike, R. J. Slutz, and J. R. Sorrells. The early contributions of H. Senf and W. Martin also deserve recognition, even though they did not remain to participate in the completion of SEAC.

As soon as the central nucleus of SEAC was functioning reliably enough to warrant regularly scheduled operations, the program of expansion and additions began. Indeed, the machine became a proving ground for the evolution of advances in computer components, design techniques, and maintenance procedures. The expansion and testing were carried out in the midst of a regular work load of important computing that was tightly scheduled because of priorities. Thus it was necessary to plan carefully in order to meet the requirements for scheduled computation and also include the necessary development work. The fact that these two conflicting objectives were meshed in an effective manner is a compliment to the fine cooperation and management between the scientists and engineers who designed SEAC and the mathematicians who used it.

During this period of expansion, over 90 percent of the time available in a full 168-hour week was effectively scheduled and used for either problem solution, development work, or preventive maintenance. During this period, 83 hours a week were scheduled for problem solution, of which 65 percent was logged as productive time, and 52 hours a week were scheduled for development work. Only 20 percent of the time scheduled for either development work or problem solution was recorded as being ineffective because of machine malfunctions. This is considered a gratifying performance for a pioneering installation, particularly when the difficult tasks of operating and expanding the machine were under way at the same time.

The initial program for expansion was directed primarily at the task of improving the input-output facilities, which resulted in the addition of magnetic wire and magnetic tape units to increase the speed of computation on problems that could not readily be kept within the confines of the 512 words available in the high-speed memory. As more of these magnetic units became available, an external selector panel was added to the machine to permit automatic selection of the desired input-output unit under programmed control of the computer as well as by manual operation of the console switches. This, in turn, made it necessary to design and construct both an inscriber and an outscriber to facilitate the transition between the documents containing the coded problem and the typed sheets giving the results of the computation by the machine. In addition, arrangements were made to permit transfers to and from punched cards which were either the source for data or the final form desired for the solution. Most of the effort in this area was planned and directed by R. J. Slutz, with the able collaboration of S. Greenwald, R. C. Haueter, E. F. Ainsworth, J. L. Pike, L. Cahn, P. R. Westlake, W. H. Bridge, and P. D. Shupe, Jr.

While the input-output system of SEAC was being augmented, steady planning and construction by a group under the leadership of W. W. Davis were also under way for the addition of an experimental electrostatic memory, primarily for trial and evaluation but with the eventual goal of regular service as an additional 512-word high-speed memory. This equipment also served as an exacting evaluation of experimental cathode-ray tubes specifically designed for storage purposes and of testing procedures that were being developed for selecting tubes suitable for operation in the memory.

The central control of the machine also underwent considerable revision and expansion. Some of these changes related to the inclusion of additional machine operations, but the more significant changes related to the inclusion of an automonitor function and a three-address control system, which is described in detail in one of the following papers. These revisions and expansions resulted from suggestions arising out of operational experience and the desire to make the machine more versatile. The detailed planning of these changes was the work of A. L. Leiner, who had been responsible for most of the final system plans for the SEAC nucleus. The physical realization and installation of these new features are a tribute to a combination of careful engineering and patience on the part of R. C. Haueter, S. Greenwald, and P. D. Shupe.

Sporadic performance of the experimental electrostatic memory directed specific attention to the development of an improved cathode-ray tube for storage purposes. By this time, the Bureau had begun the planning of a far more powerful machine than SEAC to be used in the SCOOP program of the

Office of Air Comptroller. This machine definitely required a rapid-access memory, and for this reason the development of both cathode-ray tubes and improved electrostatic storage techniques was pursued vigorously, under A. W. Holt and D. C. Friedman. Meanwhile, other approaches to rapid-access storage were being explored, one of which resulted in the Diode-Capacitor memory system suggested by A. W. Holt and reported in a companion paper.

During the expansion of SEAC and the evaluation of components aimed toward the creation of a SCOOP machine, it became evident that the dynamic circuitry devised for SEAC was susceptible to considerable electronic standardization. In turn, this became the basis for a repetitive physical configuration out of which the high-level pulse circuitry could be assembled. The advantages and possibilities of a standardized package design were realized by R. J. Slutz, and its detailed design and execution were the results of combined efforts of R. P. Witt and R. D. Elbourn.

The computer group at the U. S. Air Force Missile Test Center, Patrick Air Force Base, Cocoa, Florida, collaborated in the mechanical design of the first satisfactory packages, and these were successfully employed in the outscriber that was constructed for SEAC. This packaged design, with some refinements, was used in two computing machines that have recently been completed, one at the Air Force Missile Test Center and the other at the Willow Run Research Center of the University of Michigan. The Bureau revised this package design to incorporate etched circuit techniques. These are the packages that were used in the construction of DYSEAC, a new machine sponsored by the Research and Development Board for the evaluation of a number of organizational and engineering innovations. All three of these machines are based on the circuit techniques and some of the organizational features of SEAC, but they are distinguished one from the other by variations on the SEAC organization that were included to meet specific application requirements.

In order to cover adequately the 5 years of development that stemmed from the SEAC program, the component improvement program, and the subsequent DYSEAC program, the senior personnel of this laboratory have shared the responsibility for reporting on the achievements of the entire group. The authors of any of these particular papers are not necessarily, therefore, the only major contributors to the solution of problems discussed; and many of these authors, with others, have made important contributions to other programs as well as to those on which they are now reporting. Here again, it is important to recognize the team nature of the developmental activity that is being carried on at NBS.

While the detailed planning of the SCOOP computer was deferred in order to identify more clearly its operating characteristics and to have at hand a proved rapid-access memory, the design and construtions of DYSEAC, which was to result in a complete machine that would serve certain specialized needs and also provide a thorough evaluation of the packaging techniques, was undertaken. Although DYSEAC employs an acoustic memory and a serial arithmetic unit, the basic organization is considerably more sophisticated than that of SEAC, for it contains some of the system features that had been planned for the SCOOP machine. In addition, special features have been incorporated to permit the machine to serve as a tool for experimentation on the handling of large masses of business-type data and for experimentation in using digital equipment in a control system.

The task of planning the organization of DYSEAC and its detailed execution through the preparation of wiring tables was carried out under the direction of A. L. Leiner, with the able collaboration of W. A. Notz, J. L. Smith, A. Weinberger, and W. H. Bridge. The physical realization of the machine involved many original design problems related to the use of packages and a modular type of construction for the chassis. The decision to install DYSEAC in a pair of vans was made after the program was well under way. This added many new mechanical and electrical considerations. The formidable task of constructing DYSEAC was accomplished in approximately 18 months by a team of about 25 people directed by R. P. Witt, ably supported by R. W. Smith, H. P. Belcher, and R. Hand.

One of the major purposes in the SEAC program was to evaluate the reliability and serviceability of techniques that appeared highly promising but were at that time still unproved. Subsequent operating experience has established the soundness of many of the engineering choices that were significant departures from the techniques then current. Operating experience established another important feature: the significant benefits that accrued from using an operating machine as a proving ground for new component and operating techniques. SEAC has served as a valuable focal point that prompted the exchange of ideas among the components researcher, the machine designer, the maintenance engineer, and the user. The DYSEAC holds promise of becoming a comparable source of ideas for further machine development.

1. SEAC

S. Greenwald, S. N. Alexander, and Ruth C. Haueter

1. INTRODUCTION

The first major contribution of the National Bureau of Standards to the development of electronic computing machinery occurred with the completion of the SEAC (Standards Eastern Automatic Computer) in May 1950. This digital machine was the culmination of almost 2 years of intensive design and construction work which was sponsored by the Office of Air Comptroller, Department of the Air Force. The initial objective set during the summer of 1948 was to provide at the earliest possible date a machine of limited computing power that would meet the immediate computational needs of the National Bureau of Standards. This installation would serve as a "stopgap" for the interim period during which full-scale equipment from a commercial source was being completed for delivery to the Government. Toward the end of 1949 this point of view was gradually abandoned, as it became evident that there would be no other equipment available for 2 years or possibly longer. As a result, the ultimate objective was altered so that a full-scale machine could be attained by expansion of the initial nucleus without delaying its completion.

Still another aspect of building an expandable machine was the ability to use it as a proving ground for experimental equipment.

At the present time, after more than 3 years of regularly scheduled operation, SEAC is still actively employed in the solution of problems for both NBS and many Government agencies. What is perhaps more important is that for the initial 2 years of its operation it was the most powerful computer installation readily available to the Government, and consequently was scheduled around-the-clock for a full 7-day week.

Since the machine was first put into operation, a significant fraction of the total time available has been devoted to the engineering work associated with the expansion of SEAC. The magnitude of this effort can be estimated from the fact that the number of vacuum tubes in the system was increased from approximately 750 to 1,300 and the number of germanium diodes from approximately 10,500 to 16,000. This expansion and testing program was carried out in the midst of a regular work load of important computation that was tightly scheduled because of priorities.

A number of circuit and equipment innovations were included in the SEAC program in order to evaluate the reliability and serviceability of techniques that were highly promising but unproved. One example in this area is the extensive use of diode switching. Another is the achieving of a-c coupling by using pulse transformers for highly variable duty factor service. Success with these techniques made practical the use of vacuum tubes as a means of power amplification rather than as gating devices.

At the present, two machines based on a packaged version of the SEAC "transformer-coupled dynamic circuitry" have been completed. One is located at the Air Force Missile Test Center in Florida and the other at the Willow Run Research Center of the University of Michigan. A still further extension of these techniques was employed at the National Bureau of Standards in the construction of the DYSEAC, which is described in a companion paper.

2. OPERATING CHARACTERISTICS

The SEAC is an automatic high-speed digital computer that operates at a 1-Mc pulse repetition rate. The machine is predominately serial in nature and uses the binary number representation. Both instruction words and number words consist of 45 binary digits, which are equivalent to approximately 13 decimal digits. When the machine was first put into operation in May 1950, 11 different types

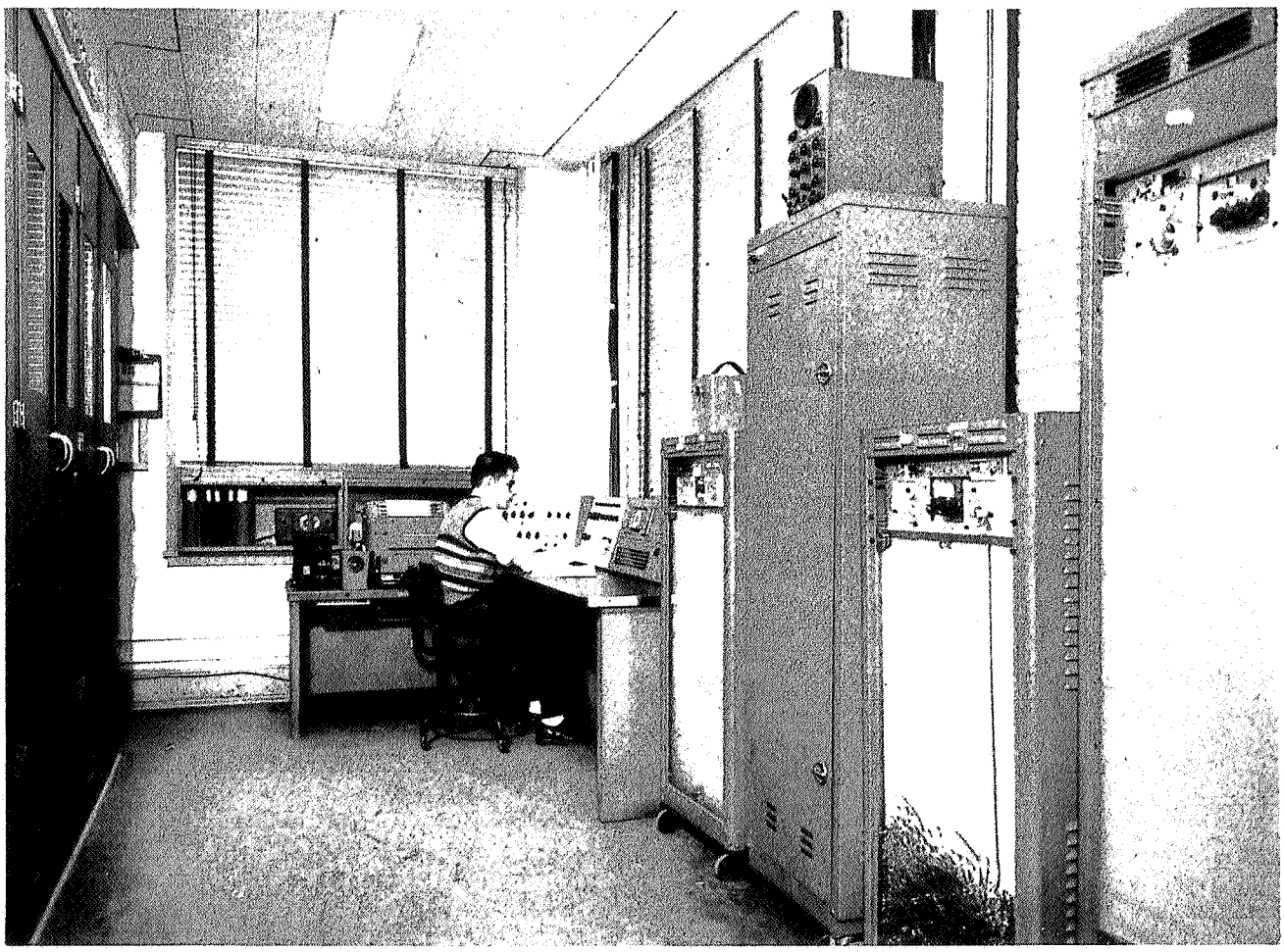

FIGURE 1.1. *SEAC from control console side.*

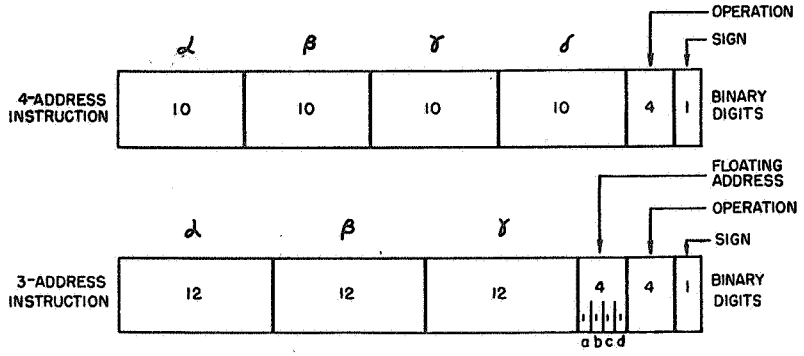

FIGURE 1.2. *Component parts of a SEAC instruction.*

of operations were performed by it: (1) addition, (2) subtraction, (3) multiplication, major part, unrounded, (4) multiplication, major part, rounded, (5) multiplication, minor part, (6) division, (7) comparison, algebraic value, (8) comparison, absolute value, (9) logical transfer, (10) read in, and (11) print out. The instruction words expressed these operations in the four-address mode. The original high-speed memory consisted of 512 words of acoustic delay-line storage, and all of the input-output devices were modified Teletype equipment. The input was from either a tape reader or keyboard, and the output was to either a printer or tape punch.

During the 3 years the machine has been operating, it has been expanded into a far more powerful and convenient tool than its original conception. For example, five additional operations have been incorporated: (1) reverse tape or wire, (2) logical multiplication, (3) base, (4) file counter information, and (5) clear memory cell, bringing to a total of 16 the types of operations available. An experimental Williams type of electrostatic memory has also been added. This stores 512 words in 45 cathode-ray tubes, with parallel access to a complete word in 12 μsec. An alternative instruction system, using the three-address mode of operation has also been installed. By simply setting several switches inside the machine, the computer is set for operation in either the three-address or four-address system.

Magnetic wire and magnetic tape units were added to increase the speed of the computer on problems which require considerable input-output or auxiliary memory capacity. In particular, the magnetic wire handling equipments greatly speed up initial input and final output. Magnetic tape units, both single-and multiple-channel, provide external memory. Figure 1.1, which is a view of the computer from the console side, shows several of these units. Either automatic or manual selection of input-output units is available. Still another feature that has been added by modification of the circuitry is the ability to automatically monitor the operations being performed. When called into use by setting a switch on the console, this feature causes the machine to print out the program-sequence counter information, the instruction being performed, and the result of the operation. This facility is a great convenience, and will be discussed in more detail later.

The component parts of an instruction word in both the four-address and three-address systems are shown in figure 1.2. In the four-address system, the addresses are denoted by the symbols α, β, γ, and δ. Normally, α is the address of the first operand, β the address of the second operand, γ the address of the result of the operation, and δ the address of the next instruction. The instruction also contains a code specifying the type of operation to be performed and a conditional halt control digit in the sign position. An address comprises 10 binary digits, so it can designate one out of 2^{10}, or 1,024, memory cells. This is sufficient for the two SEAC memories. Four binary digits specify the operation to be performed. The 16 different operation codes thus available are now all used. The single binary digit in the sign position indicates whether or not the computer is to halt after performing the operation. In the course of executing one instruction, the control of the computer cycles through four phases, one for each reference to the memory. In a typical operation, address β is referred to in phase 2, α in phase 3, γ in phase 4, and δ in phase 1.

A typical three-address instruction word contains the addresses α and β of the operands and the address γ of the result. The remainder of the word contains floating-address information, the code specifying the type of operation to be performed, and the conditional halt digit. Twelve binary digits are used to specify an address, providing the basis for selection among 4,096 memory cells; four binary digits are used to provide information for the floating address feature. The operation code for the 16 instructions is the same as in the four-address system.

The main difference between the three-and four-address systems is in the designation of the next instruction to be performed. In the four-address system, the instruction contains an explicit statement (δ) designating where the next instruction is located in the memory. In the three-address system, however, there is no such explicit statement. Instead, instructions in this system are automatically sequenced in accordance with a convention, successive instructions being normally located in consecutively numbered memory positions. An exception to this convention is available through the comparison (conditional transfer) operation, whenever the first operand (α) is less than the second operand (β). In this case the result of the comparison leads to what is called a "jump" operation in which the next instruction for both the three-address and four-address systems is chosen from address γ.

The floating address feature allows the programmer to designate any address as either absolute or relative. An absolute address is interpreted in the usual sense, merely as a number identifying a specific memory location. A relative address, however, identifies a position in the memory by specifying its displacement relative to that position from which the instruction word itself was taken. To illustrate, suppose that an instruction located in memory position m specifies that the address of the first operand is number 17 relative. Then the control will take the word in memory location $(m+17)$ and use it as the first operand. If location $(m-17)$ is desired, the complement of 17 is used as the address.

It is possible to use any combination of absolute or relative addresses in an instruction word. Of the four binary digits that supply floating address information, the first three digits, a, b, and c, indicate whether α, β, and γ, respectively, are absolute or relative. The fourth binary digit d tells which of two control counters is to be used during operation in the three-address mode. Counter 0 is normally the operating counter. However, starting with any desired address, counter 1 can be put into operation by a "jump" comparison in which γ is the desired address and binary digit d specifies counter 1. Counter 1 will be the operating counter only so long as d in each following instruction indicates counter 1. As soon as an instruction is reached in which d indicates counter 0, the control automatically returns to counter 0 after performing the instruction.

A typical use of this feature is to code subroutines for counter 1 with floating addresses. The use of floating addresses allows the subroutine to be placed anywhere in the memory automatically. By coding a subroutine for counter 1, a "jump" comparison sends the control to counter 1 at the desired address, and after finishing the subroutine it returns the control automatically to counter 0 at the point in the main program where it left off.

The basic operations of SEAC and their functions are summarized in table 1.

TABLE 1

Name of operation	Description of instruction
Addition	Form the sum of the word in α and the word in β, and write the result in address γ in the memory.
Subtraction	Form the difference α minus β, and write the result in address γ in the memory.
Multiplication, major, unrounded.	Form the product of the word in α and the word in β, and write the major part (unrounded) in address γ in the memory.
Multiplication, major, rounded.	Form the product of the word in α and the word in β, and write the major part (rounded off) in address γ in the memory.
Multiplication, minor	Form the product of the word in α and the word in β, and write the minor part in address γ in the memory.
Division	Form the quotient of the word in β divided by the word in α, and write it in address γ in the memory.
Logical transfer	Write in address γ in the memory those digits of the word in α which correspond to one-digits of the word in β. Leave the word in γ unchanged in those digit positions which correspond to zero-digits in the word in β.
Comparison, algebraic	If the word in α is algebraically greater than or equal to the word in β, take the next instruction from the normal next-instruction address position. (In the four-address system, this is address δ in the memory; in the three-address system, this is the next consecutively numbered address position.) If, however, the word in α is less than the word in β, take the next instruction from address γ in the memory.
Comparison, absolute	Perform algebraic comparison except treat both words as positive.
Read in	If the address number β is odd, read in one word from the selected external unit designated by address number α, and write the data in address γ in the memory; if the address number β is even, read in eight words, and write in the eight addresses beginning with address γ.
Print out	Print out the word in address γ in the memory if the address number β is odd (or the block of eight words beginning with address γ if β is even) onto the selected external unit designated by address number α.

TABLE 1—Continued

Name of operation	Description of instruction
Reverse	Reverse through one word if the address number β is odd (or through eight words if the address number β is even) on the selected external unit designated by address number α.
Logical multiplication	Write the digit-by-digit product of the words in addresses α and β into address γ in the memory.
Base (primarily for four-address system).	If address number α is greater than or equal to address number β, put the number β into the special base-number counter-register and take the next instruction from address δ in the memory. In subsequent instructions, all references to odd-numbered addresses will now be interpreted relative to this constant number β. If address number α is less than address number β, the counter-register is cleared and the next instruction is taken from address γ in the memory.
File	Write the contents of special counter-registers into memory address γ.
Clear	Clear memory address γ.

3. MACHINE ORGANS

An over-all block diagram of SEAC is shown in figure 1.3, in which information paths are shown as solid lines and control paths as dashed lines. Interchanges of information between the Shift Register, the Arithmetic Unit, the Control, and the Mercury Memory are made through the unit called the Bus. The Bus not only provides correct routing of information but correct timing as well. During an input operation, instructions and numbers are read into the Shift Register from one of the input-output units via the Selection Circuits. From the Shift Register there are two possible paths. The digits are transferred either in parallel into the Electrostatic Memory or serially into the Mercury Memory via the Bus. For an output operation, the procedure is the same but the path is reversed. For internal operations, instructions are routed from the Memory to the Control Unit, and numbers are routed between the Memory and the Arithmetic Unit. Transfers are made to and from the Mercury Memory directly through the Bus. Whenever the Electrostatic Memory is used, an additional transfer through the Shift Register is required.

The Arithmetic Unit in SEAC is involved in almost every operation that the computer performs, with the exception of several such as File and Base. Figure 1.4 is a block diagram of the Arithmetic Unit. In the process by which two numbers are added, the first number enters the Arithmetic Unit in phase 2 of the cycle through which the computer sequentially progresses. If the number is positive, it goes through the Input Complementer and Adder into the Accumulator Register. If the number is negative, the Sign Sensing Unit activates the Input Complementer, and the complement of the number is sent to the Accumulator Register. During phase 3, the second number is sent to the Arithmetic Unit. Again it is complemented or not, depending on whether it is negative or positive. The second number is then added to the first number, which has been circulating in the Accumulator Register and is available at the second input to the Adder. In phase 4, the result of the addition is sent via the Output Complementer through the Bus connection to the Memory. If the result is negative, the Sign Determining Unit inserts a binary 1 in the sign position of the number and also activates the Output Complementer.

The process of subtraction is almost identical, the difference being that the effect of the sign of the number from β on the Sign Sensing Unit is reversed. The process for a comparison is similar to that for subtraction. However, no result is transferred to the memory; instead a signal is sent to the Control Unit when α is less than β.

Multiplication is performed in SEAC by repetitive additions, which involve the use of two other registers, the Multiplier and the Multiplicand Registers. In phase 2, β enters the Multiplier Register, and in phase 3, α enters the Multiplicand Register. Multiplication is accomplished by successive additions of the multiplicand to the partial product in the Accumulator Register under the control of the digits of the multiplier. The shifting is accomplished in the Accumulator Register by shortening it one pulse time. Division is also a repetitive process using all three registers,

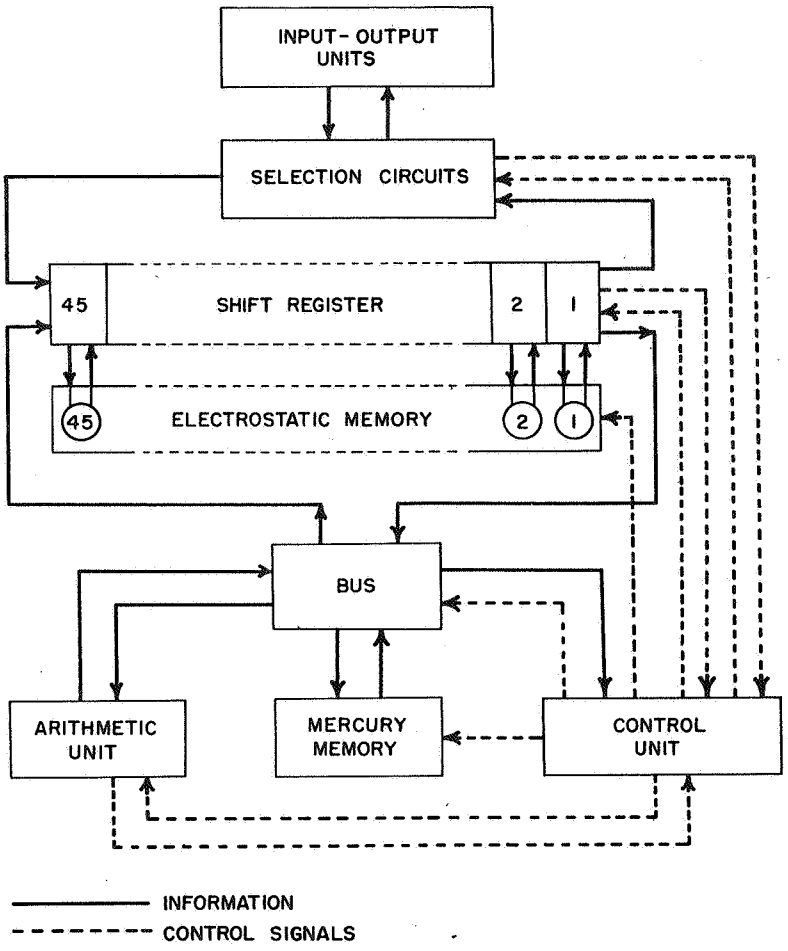

FIGURE 1.3. *Block diagram of SEAC.*

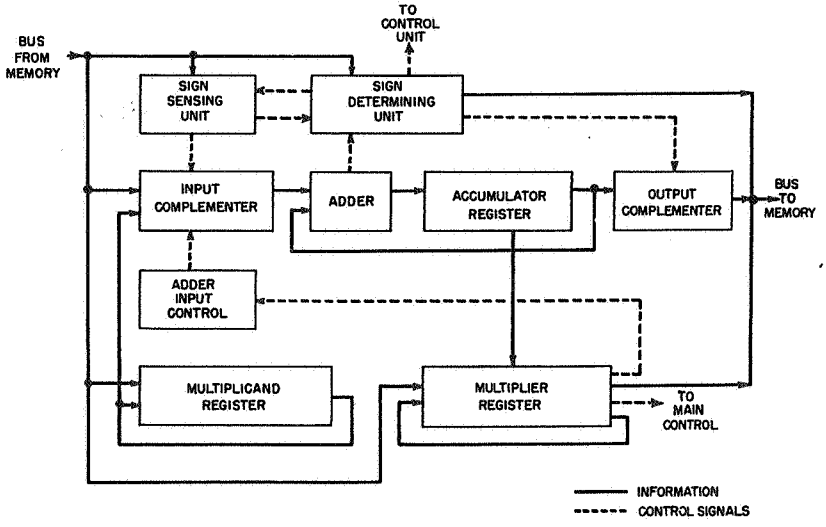

FIGURE 1.4. *Block diagram of Arithmetic Unit.*

with the quotient formed in the Multiplier Register. The nonrestoring method of division is used and consists of successive subtractions or additions of the divisor, according to the sign of the remainder. Physically, the entire Arithmetic Unit occupies only 1 1/4 relay racks. It is interesting to note that this early design for a binary adder, which is used in all computations, employs only three single-cathode vacuum tubes.

The Control Unit is the most complex part of the computer, as may be seen in the simplified block diagram of the control in figure 1.5. This has resulted partially from the experimental nature of the machine and from the continuous expansion it has undergone. One of the major functions of the Control Unit is to decode the instruction to determine (1) the type of operation to be performed, (2) the location of the numbers involved in the operation, and (3) the location of the instruction to be performed next. After the instruction is received from the memory, it circulates in the Instruction Register. The digits representing the operation are decoded in the Staticizer and Decoder, and the appropriate operation lines are activated.

The addresses are selected one at a time in what is called the Address Selector. If the location called for is in the Mercury Memory, the address information is sent to the Mercury Comparator. When the output of the Minor Cycle Counter agrees with the temporal selection portion of the address, the Mercury Comparator sends a signal to the Execute Generator that the desired word is in position to be read out. The Phase Counter is then advanced and the transfer is made. On the other hand, if the location called for is within the 512 words of the Electrostatic Memory, the address is routed into the Electrostatic Control. This Control then determines when the Execute Generator will advance the Phase Counter and when transfer between the Electrostatic Memory and the Shift Register will be made. In three-address operation the information from the selected counter is sent to the Address Selector where it is used to select relative addresses and the location of the next instruction.

The Shift Register Control serves mainly to direct the transfer of information in and out of the Shift Register at the rate acceptable to the Input-Output device in use. The Automonitor Control automatically cycles the computer through the necessary print-outs for each instruction being monitored. The Multiplication Counter counts off the 44 minor cycles (word times) necessary for a multiplication or division and prevents the phase counter from advancing until this portion of the operation is completed. Finally, the Manual Control permits the computer to be started or stopped, or its operation to be modified, by means of switches located on the console.

The Mercury Memory for SEAC is housed in a separate cabinet, which contains the 64 mercury-filled acoustic lines, their associated amplifiers and gating circuits, the selection matrix, and other miscellaneous circuitry. Figure 1.6 shows one side of the cabinet with 32 of the recirculation amplifiers and half of the selection circuitry. As the nominal delay through the lines is 384 μsec, 8 words of 48 digits each are stored in each mercury line. Thus the total capacity of the memory is 512 words.

Because the delay of a mercury line varies somewhat with temperature and yet the whole memory must be kept in step with the crystal-controlled computer clock, it is necessary to maintain all lines at the same constant temperature. A system of aluminum plates and extrusions bonds the 64 mercury-filled glass tubes into a nearly isothermal unit, which is insulated from the outside and is electrically heated and thermostated to 50 $\pm$0.25° C.

Pulses are stored in each line as packets of an 8-Mc carrier. For every binary one there is an associated radio-frequency pulse packet, and for every zero there is a gap. The acoustic output of the line activates a quartz crystal whose electrical output is then transformer-coupled to the input of the recirculation amplifier. The first three tubes serve as a radio-frequency amplifier and detector, with an over-all gain of 50 to 55 db and a center frequency of 8 Mc. The fourth tube in the chain has the function of switching information into or out of the line, as well as that of synchronizing and reshaping. The fifth tube develops the 8-Mc packet of 200-v peak-to-peak amplitude, which is transformer-coupled to the input crystal of the mercury line.

Figure 1.7 shows the general organization of the mercury cabinet. Digital information denoting the mercury line to be selected comes from the Mercury Comparator located in the control section of the machine. An electrical delay line brings these time sequential pulses into positions from which

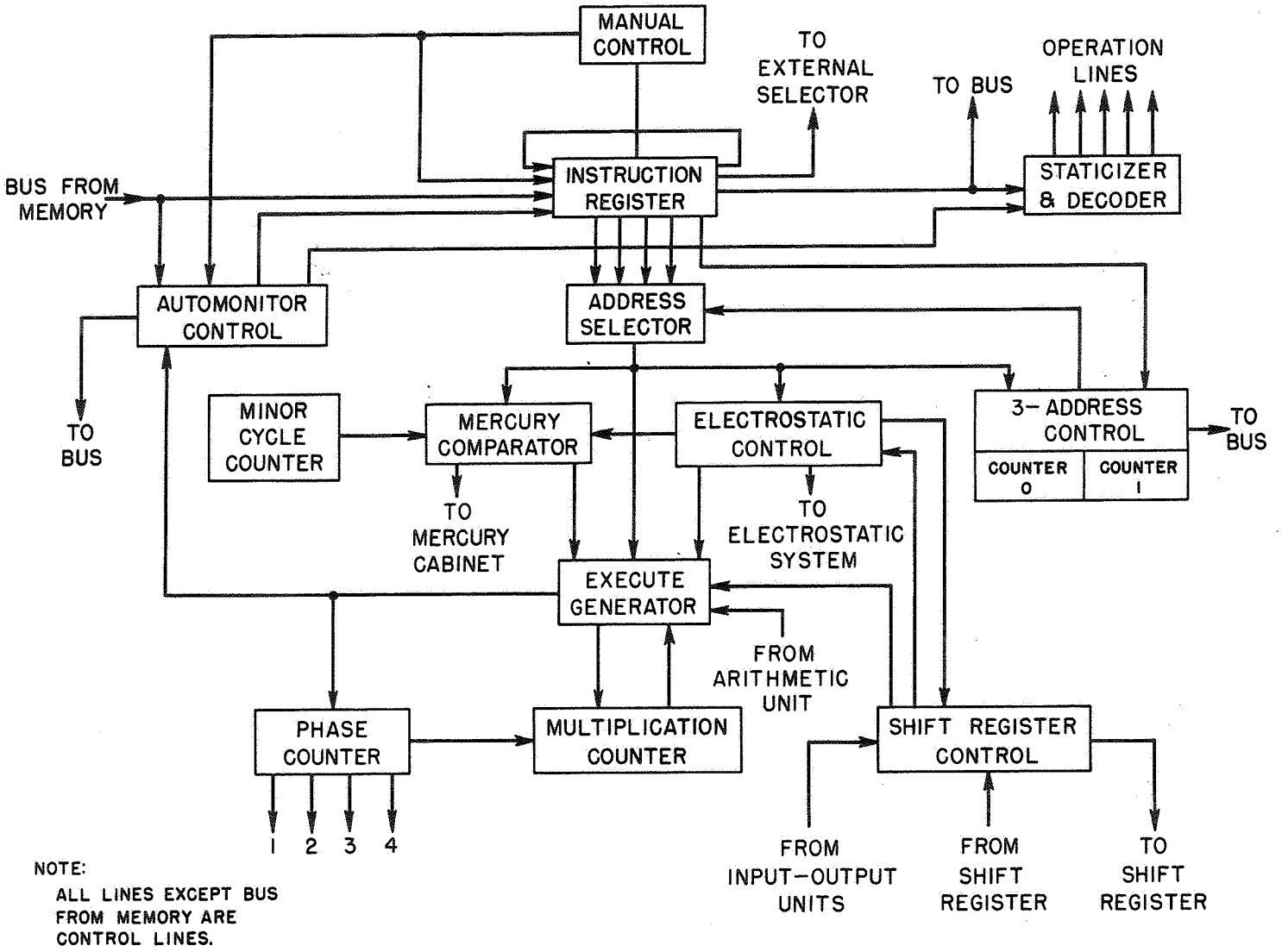

FIGURE 1.5. *Block diagram of Control Unit.*

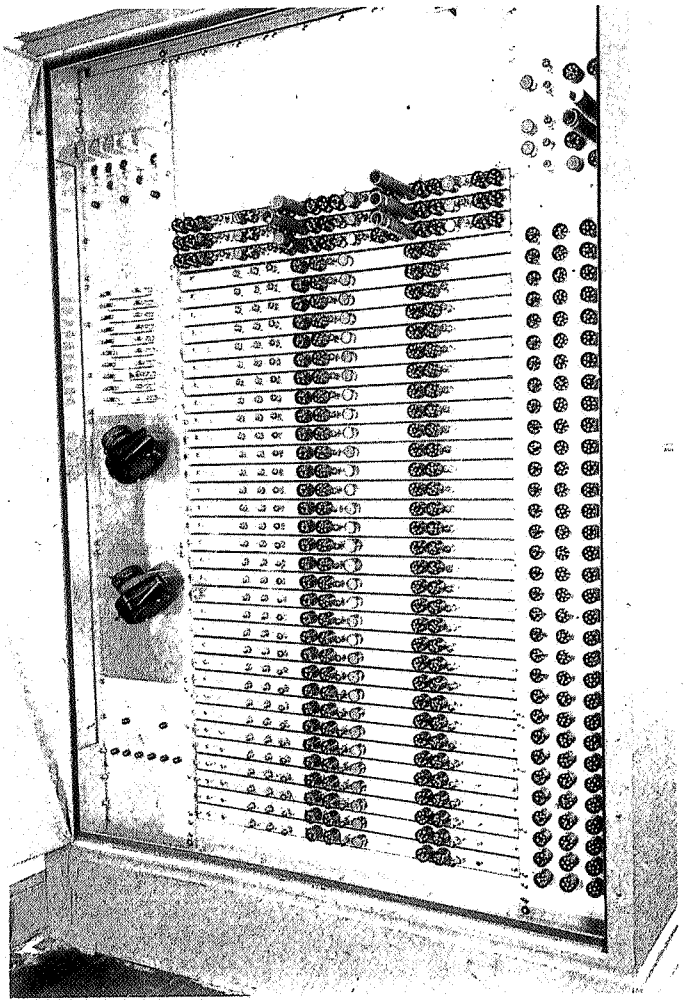

FIGURE 1.6. *Side view of Mercury Memory cabinet.*

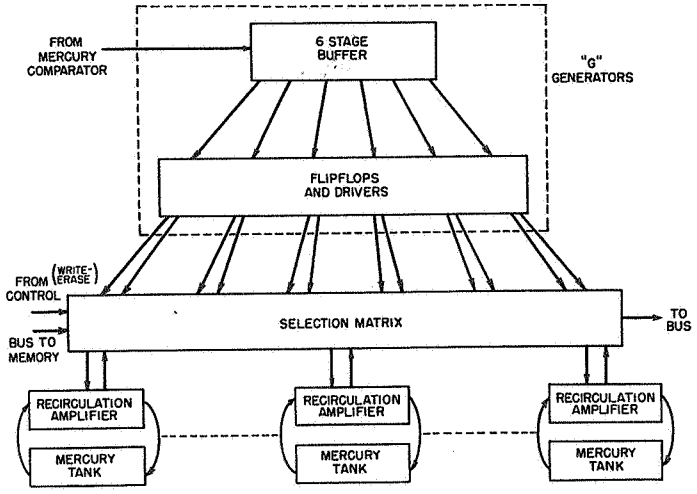

FIGURE 1.7. *Block diagram of the Mercury Memory.*

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they can be simultaneously gated into six flip-flops with associated drivers. This portion of the circuitry is called access gating or, more popularly, "G" Generators. The varied combination of six positive and six negative pulse lines from the "G" Generators selects one of the 64 mercury lines that connect with the matrix. When writing into the memory, which is done in phase 4, information appears on the Bus to Memory, from which it is routed to the selected memory line, the old information being simultaneously deleted. In phases 1, 2, and 3, information from the selected address is transmitted via the output mixer of the matrix to the Bus. Information is erased by interrupting the recirculation path only when new information is written in.

As previously mentioned, in addition to the acoustic memory, SEAC also includes a full-scale experimental electrostatic memory. This provides an additional 512 words of storage, effectively increasing the capacity of the machine to 1,024 words. As this memory is arranged to operate in the parallel mode, the access time is considerably decreased, which thereby increases the speed of the machine over that which is possible with the mercury memory. The type of electrostatic storage is that originated by Williams and Kilburn, in which the phosphor surface of a conventional cathode-ray tube is charged to store digital information.

This memory occupies approximately six standard relay racks. Four racks hold the cathode-ray tubes (CRT) plus their associated regeneration amplifiers and gating circuitry. The remaining two racks contain the deflection generators, the counter, and other control circuitry. There are actually 48 CRT positions, but only 45 are employed at any one time. The other three positions are available as spares. Two types of cathode-ray tubes are used for storage, the 5UP1 and the 3KP1. The well-known dot-slide technique is used, in which a dot signifies a binary zero and a dash a binary one.

Figure 1.8 is a block diagram of the electrostatic memory for SEAC, showing the flow of information and the method of control. Numbers or instructions are transferred to the memory along parallel lines from the Shift Register, and this information is stored for as long as it is needed by a continuous process of regeneration, which takes place with the aid of the regeneration amplifiers. At any given time the location of the electron beam in the CRT is determined by the digital information in the Staticizer, which can be loaded from either the Address Register or the Regeneration Counter. The Staticizer sends out pulses of about 7-μsec duration. These pulses are sent to the Deflection Generators where they are decoded and converted to CRT deflection signals having very accurately derived voltage levels. All 48 CRT's are deflected in parallel, and the actions of turning the beam on and strobing the output signal of the amplifier are also performed simultaneously for all CRT positions.

The Operations Generator provides the proper "turn-on" signals to the CRT grids for both dot and dash conditions. It also provides a strobe pulse to the amplifier and a "twitch" signal to the Deflection Generators. The Synchronizer dispatches signals to the other units to insure that the correct sequence of pulses takes place and, furthermore, that these actions are synchronous with the rest of the machine.

When the electrostatic memory is being used, a read or write action can take place as frequently as every 48 microseconds. Of this time, only 12 μsec is actually required for the action, so the remaining time is always used to accomplish three regenerations.

The Shift Register and its Control comprise two full racks of equipment, which are shown in figure 1.9. Its size and complexity are due to its many functions. First, it acts as an intermediary, or buffer, storage between the input-output equipment and the serial acoustic memory. In connection with input-output operations, it also has the functions of digit counting, word counting, and word inversion. Further, the Shift Register acts as a register for the electrostatic memory, which operates in the parallel mode, and serves to provide the transfer to and from the serial representation in the rest of SEAC. In connection with the electrostatic memory, it also helps perform the logical transfer operation.

Figure 1.10 is a simplified diagram of the Shift Register showing how it connects to both memories. It will be noted that the register consists of 48 flip-flops arranged in a closed loop. Shifting may be done only to the right, as indicated by the arrows. During an input operation, the highest order of the number comes in first and is sent to stage 46. This digit then undergoes a

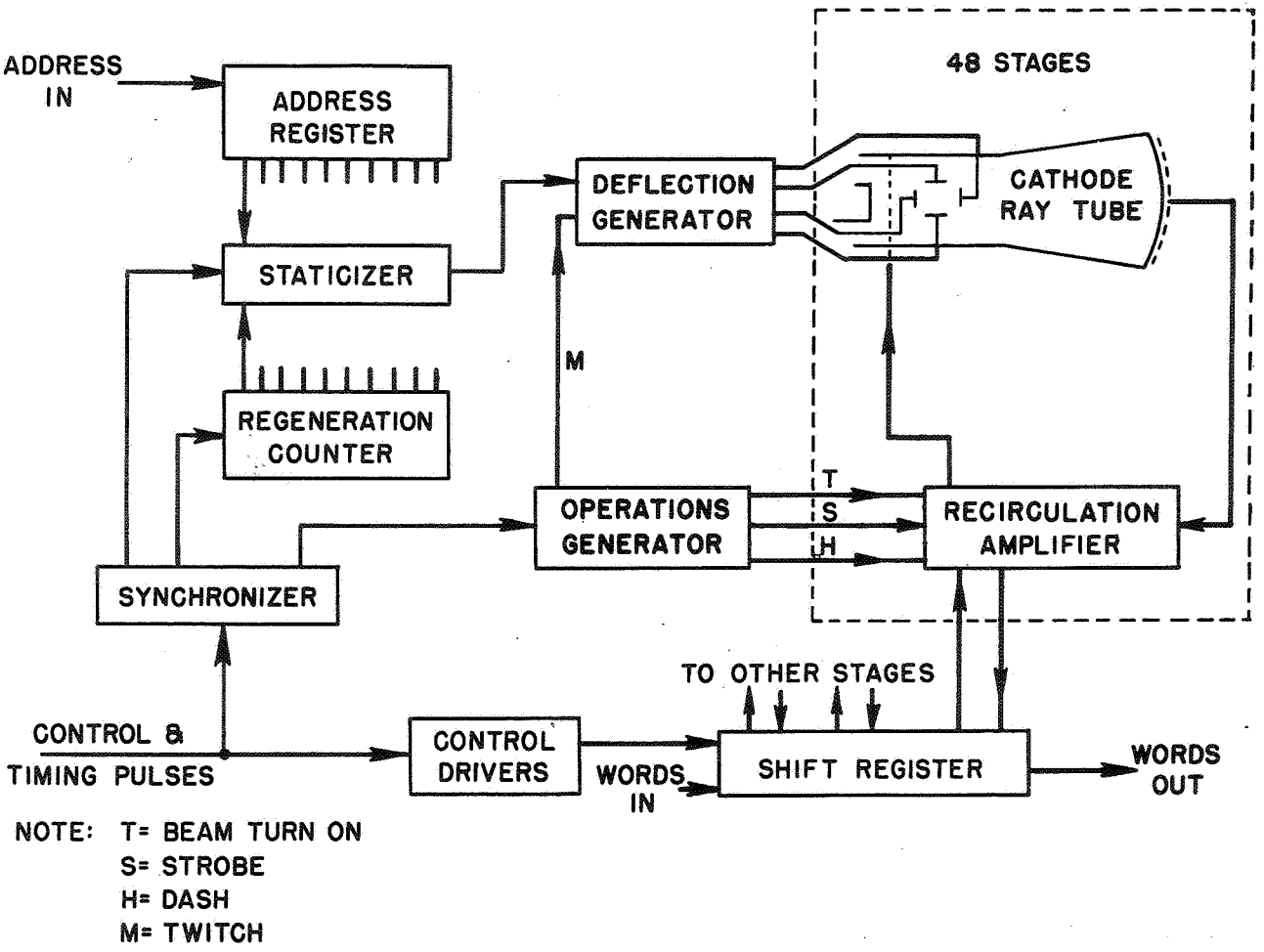

FIGURE 1.8. *Block diagram of the Electrostatic Memory.*

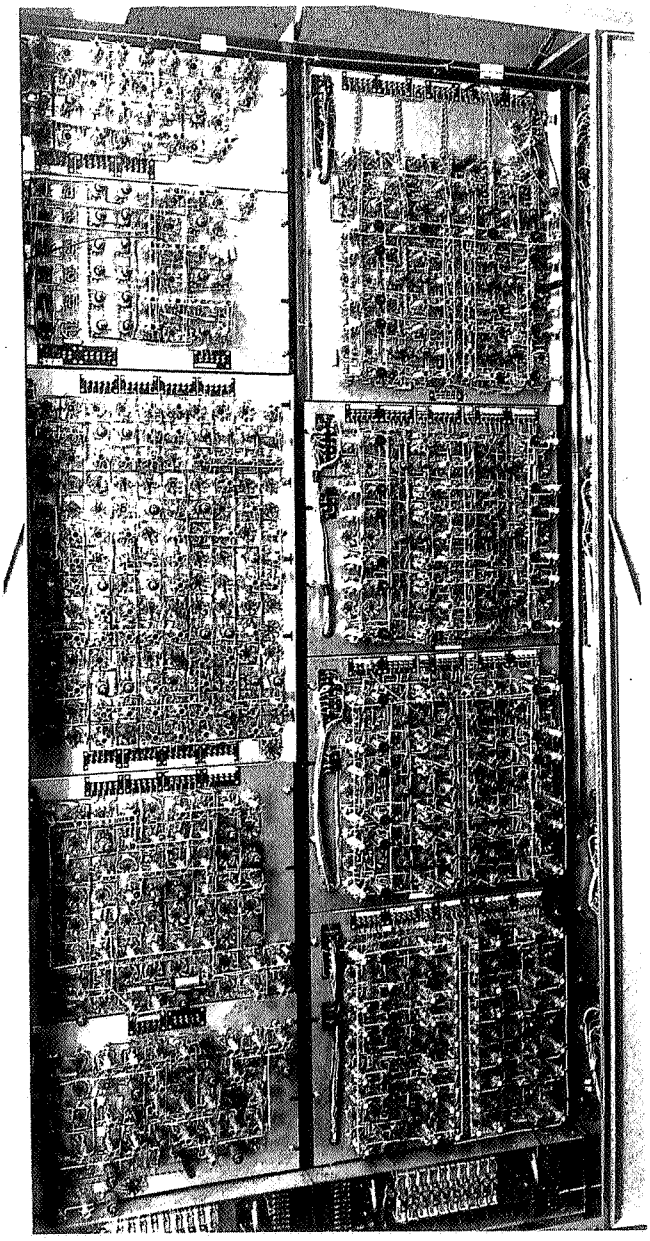

FIGURE 1.9. *Shift Register and Shift Register Control.*

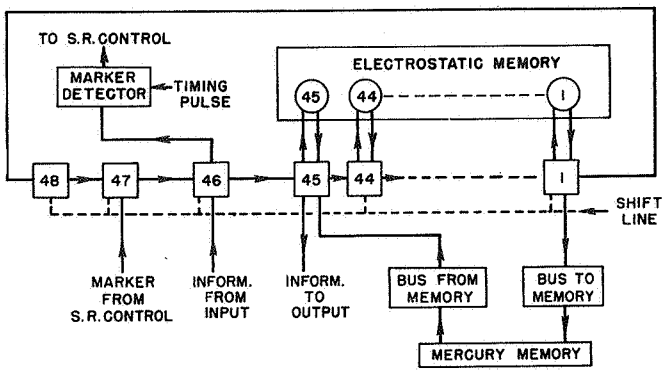

FIGURE 1.10. *Block diagram of Shift Register.*

series of right shifts, until it ends up in stage 47. Then the second highest order digit is inserted in stage 46, and again a series of right shifts takes place. This process continues until the entire number has entered the Shift Register. When the number is in position, a marker pulse signals the end of operation. At this time the number is shifted serially from stage 1 of the Shift Register into the memory at a one-megacycle rate.

During an output operation, the reverse process takes place. The number is shifted rapidly into the register through stage 45. Then, one digit at a time is sent to the appropriate tape, wire, or teletype unit via stage 45. The end of operation is again signalled by the marker pulse.

The Input-Output equipment used in SEAC is fully covered in a separate article. However, some salient facts pertaining to each type of equipment may be of general interest. The Teletype equipment operates at six characters per second, where each character represents four binary digits. This gives an equivalent speed of two seconds per word. Because of this low speed, Teletype is used primarily for manual operations, for which it is a very convenient means for printing out or inserting information in any memory location. The wire units, which employ cartridge loading, are used mainly for initial input and final output from the computer. The time required to fill the mercury memory from the wire input is about 12 sec, including the time for manual manipulations. The tape units developed at NBS for external storage use no reels and are single channel only. These units will hold up to 24,000 words on a 1,200-ft tape. Recently a multichannel tape unit was added to SEAC. Both types of tape units have extremely rapid acceleration, starting and stopping in less than 5 msec. This characteristic makes them especially valuable for external storage.

The Input-Output Selector (upper half of fig. 1.11) consists of the manual switches and the circuitry that are necessary to select one or more units for an input or an output operation. The system permits selection from among 10 different units. A unit may be selected automatically by inserting the proper information in the input or output instruction. The five binary digits that contain the necessary coding enter the Selection Register, as indicated in figure 1.12. The outputs of the register energize at least one selector relay (shown at the top of the diagram) by means of the Selection Gates and Automatic Selection Switches. These multicontact relays switch the necessary signals to control reading and writing on the unit. An input or an output instruction, of course, contains a code to designate a particular input-output unit; however, by means of manual switches on the Input-Output Selector one can establish any correspondence desired between the codes and the actual devices. This feature is especially useful when a new code is being checked or when one of the units happens to be inoperable.

The function of the Comparator is to determine when the input-output unit called for is different from the one previously chosen. Only in this situation is the computer halted momentarily while the necessary relays are energized. Automatic selection can be overridden by any of the manual selection switches. There are three of these switches, one for manual input operations, one for manual output operations, and one for direct selection during computation.

There are a number of auxiliary units physically separate from SEAC that allow the slow work of preparing input programs and data and that of printing the output results to be accomplished without losing valuable computing time. Teletype keypunches and reperforators are used to prepare the initial punched paper tape. An inscriber transfers the information from the punched tape onto magnetic wire for rapid computer input and automatically inserts the proper spacing between blocks of information. An outscriber takes the output data printed onto wire by the computer and produces a punched paper tape. This unit takes its information from a continuously moving wire, performs the necessary operations of counting and recognizing each binary digit, punches the paper tape, and checks for errors in the transcription to the wire as well as errors in its own operation. Additional equipment produces printed copy and/or punched cards from the tape punched by the outscriber.

Besides the fundamental requirements of starting and stopping the machine, the SEAC control console has many facilities that enable the operator to follow the course of the problem, print out any desired information, and make any changes that might be required. Only a few steps are required to put a new problem into the computer. These are clearing the control and memory, selecting the desired input unit, and pressing the start button. To perform a manual print out, the machine must first be halted by throwing the Run-Halt switch. The Computer then halts after performing the present instruction. The Print-Out switch is then positioned to allow the operator to print out either

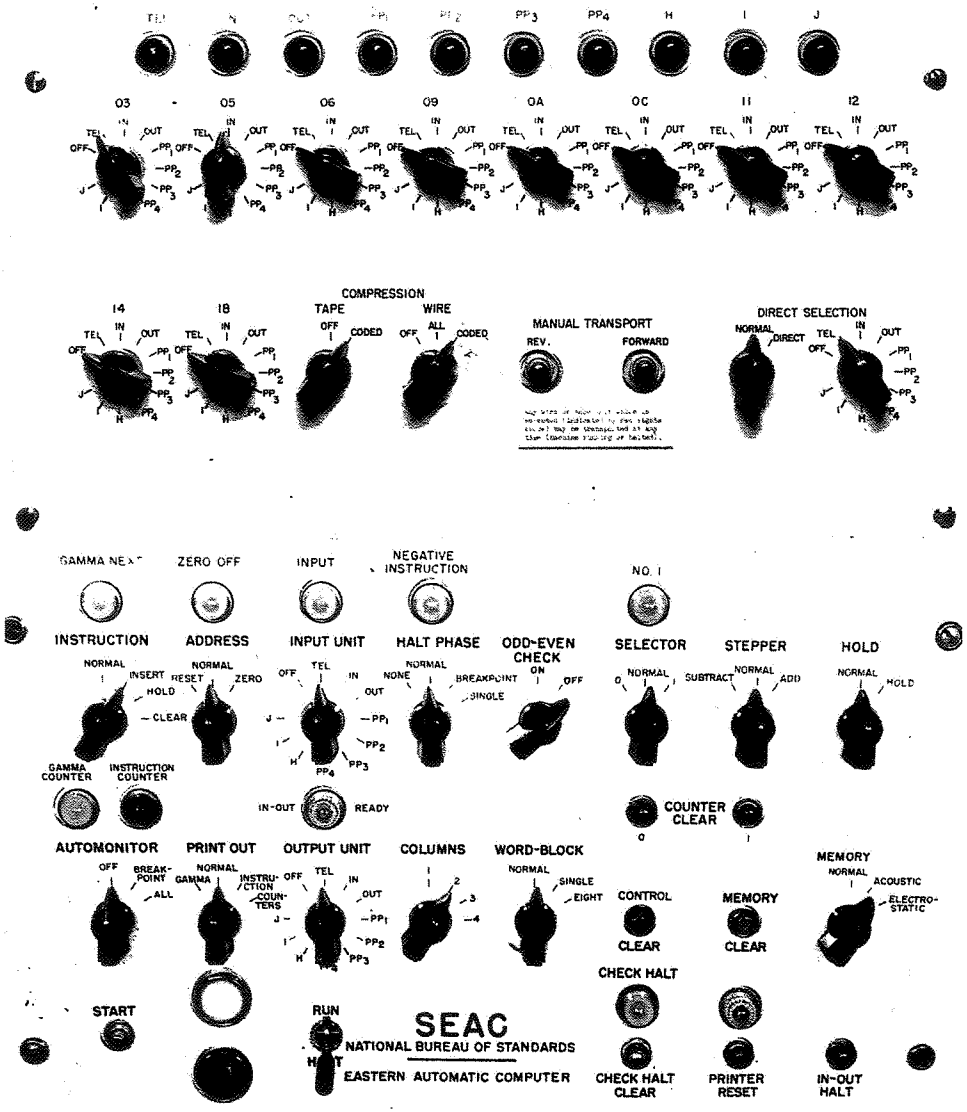

FIGURE 1.11. *Input-Output Selector panel and Manual Control Panel (bottom).*

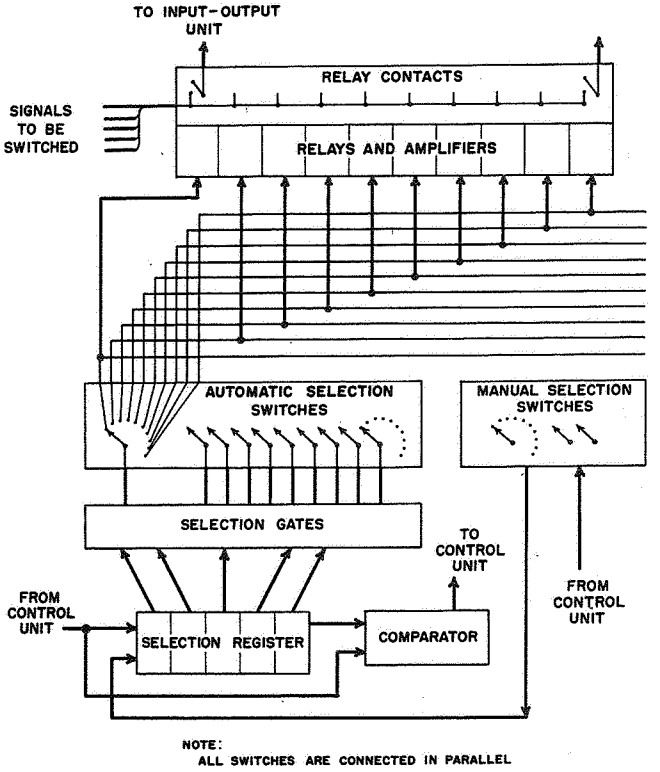

FIGURE 1.12. *Block diagram of Input-Output Selector.*

the instruction just performed, the result of the instruction, or the counter contents. The manual output selector switch allows the operator to select any unit, but the one usually chosen is Teletype.

To insert a word into any specified memory location, first the machine must be halted and the Instruction switch thrown to INSERT. When the Start button is pushed, an input instruction in which γ is the specified location is read into the first cell of the memory from the unit selected by the Input Selector Switch. Again the unit selected is usually Teletype. The Instruction switch is now set back to normal, the Start button pushed once more, and the operation completed. The memory Selector switch permits computation to be carried out in either the Electrostatic or Mercury Memory without a change in coding. In the Normal position of the switch, both memories are in use. The preceding discussion is by no means an exhaustive treatment of the switches and manual control operations available, but mentions briefly those most frequently used.

4. CIRCUITRY AND SYMBOLS

The circuitry of SEAC follows a rather uniform pattern throughout most of the central computer, with the exception, of course, of recirculation amplifiers, magnetic tape amplifiers, and the like. This pattern consists of diodes and resistors for gating, a beam power tube for amplification, and a transformer for coupling to subsequent stages. By intensive engineering of a single type of circuit, a high degree of reliability was achieved and subsequent design, testing, and maintenance were simplified.

Figure 1.13 shows a typical gating stage, of which there are numerous variations. Certain facts about the gating should be pointed out. The diode structure is three gates deep, or-and-or. Up to five inputs are allowed to each gate before the resistor values must be changed; however, this condition occurs in very few locations. The resistors are computed to allow a minimum rise of 100 v/μsec during any part of the pulse excursion. The diodes drawn in a horizontal direction carry pulse information; those drawn in a vertical direction are the clampers. It will be noticed that the gate output, which connects to the grid of the amplifier, is connected to a -5-v clamping diode. As the middle of the gate employs a -8-v clamping diode, a 3-v disconnect is obtained across the final or-gate. This is important in preventing noise from producing spurious signals. An additional disconnect of 2 v is achieved by connecting the positive output of the transformer to -10 v. Negative inputs to and-gates that are used for inhibition omit the initial or-gate, and the position of the -8-v clamping diodes is shifted to prevent them from drawing excessive current.

The single vacuum tube in the stage, tube type 6AN5, has no gating function. Its purpose is power amplification only. The 6AN5 is a miniature beam power tube with some excellent characteristics for this kind of computer service. Its pertinent characteristics are enumerated as follows:

Input capacitance	9.0 $\mu\mu$f.
Output capacitance	4.8 $\mu\mu$f.
Transconductance	8000 μmhos.
Filament rating	0.45 amp at 6.3 v.

The cathode material is passive nickel, which apparently prevents the formation of interface. In the unpulsed condition the tube stands by with a current of at least 1 ma. The clamping diode to +2 v and a small resistor in the cathode circuit help keep the dissipations of the control and screen grids within ratings.

The transformer used for coupling has several advantages. It provides impedance matching between tube and load, it enables a single stage to transmit either positive or negative pulses, and it avoids the difficulties involved in dc coupling. A step-down ratio of either 5 to 1 or 7 to 1 is used in most SEAC circuits. In any case, the equivalent load presented to the tube is such as to cause the tube to bottom, i.e., to operate below the knee of the $e_p - i_p$ curve. This kind of operation results in almost uniform voltage output even though tubes with 2 to 1 variation in current capabilities are plugged into the same circuit. The cores of the pulse transformers in SEAC are grain-oriented silicon iron in 0.001-inch thick laminations.

As SEAC is a synchronous machine, it requires precise timing pulses to all its circuits to keep the various parts of the machine in step. This is accomplished by the use of a 1-Mc master clock

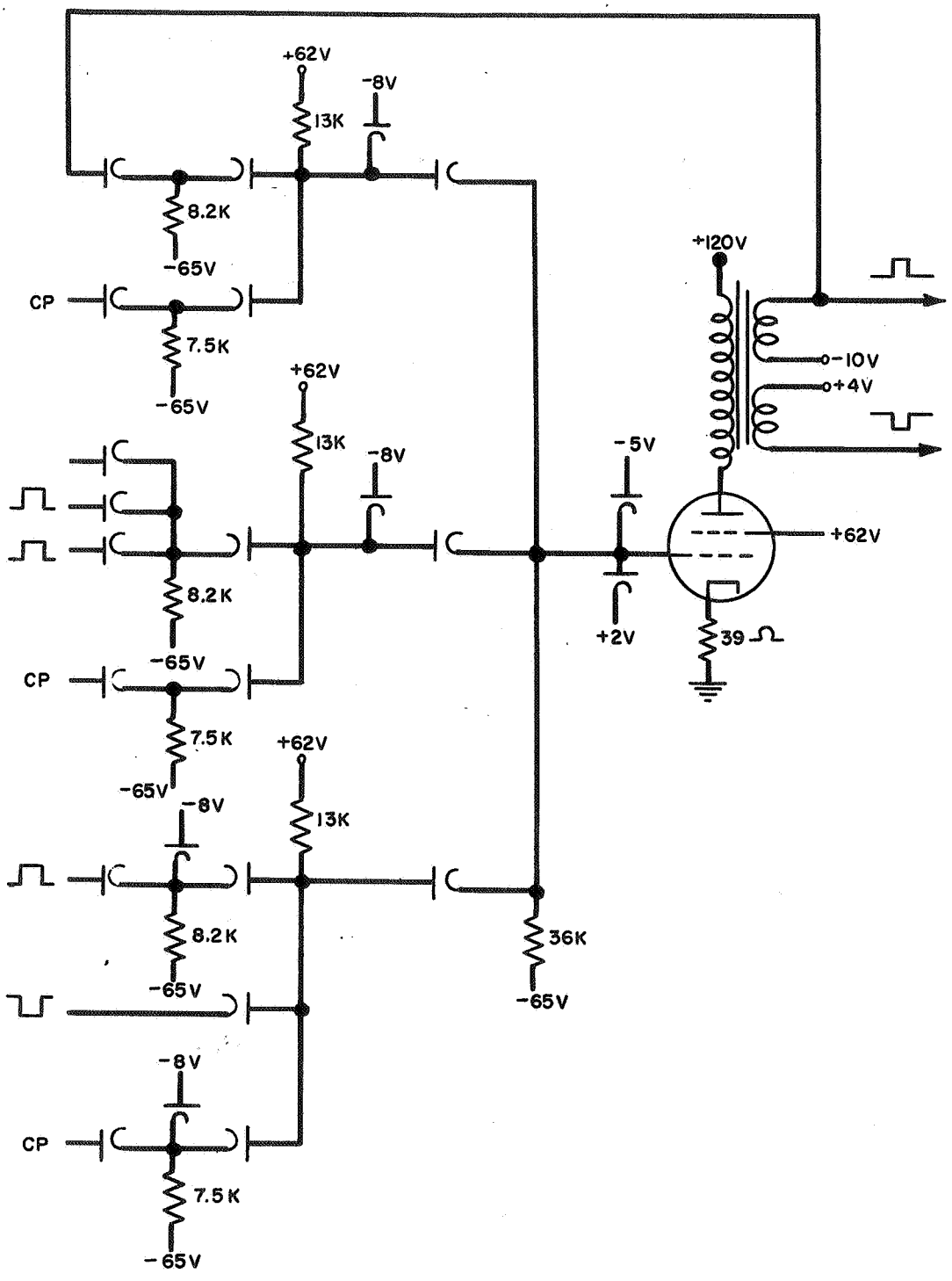

FIGURE 1.13. *Circuit of typical SEAC stage.*

which resembles a small radio-frequency transmitter. The clock signals are not distributed as rectangular pulses or half sine waves, as might be expected, but are full sine waves. There are definite advantages in using sine-wave distribution from the viewpoint of generation at high power levels, distribution without excessive pulse deterioration, and ease of phase shifting to produce the same precise timing in all parts of the computer. As the clock signal passes through the gating structure, only the trapezoidal center portion reaches the grid of the tube. These clock pulses are slightly under one-half microsecond at the top of the gating level. Although the computer could have been designed with a clock having only a single phase, the clock signals are actually distributed in three phases 120 degrees apart, which are named CP_1, CP_2, and CP_3. Because of the slight time delay in each SEAC stage and the overlap of successive clock phases, it is possible to send the output of a stage clocked with CP_1, for example, into the input of a stage clocked with CP_2 without the use of delay lines. Furthermore, three stages of gating may be done with only a 1-μsec delay. This is especially helpful in those parts of the machine where the time available to accomplish the necessary number of logical operations is limited. Figure 1.13 shows how the clock pulse is inserted into each and-gate.

A problem closely related to that of timing is that of pulse reshaping, so that the input signal on the amplifier grid is essentially a clock pulse. This may be accomplished by making sure that the incoming signals to any stage overlap both the leading and trailing edges of the particular clock phase used. As the incoming pulses will certainly be no broader than the clock pulses that produced them, delay lines may be used to achieve the necessary overlap. The method known as regeneration, which was devised shortly before the computer construction program began, accomplishes the same result without delay lines. All that is necessary in this method is that the pulses into a stage overlap the leading edge of the clock pulse. The positive output of the transformer is fed back as one of the inputs of the stage, and thus the pulse is held up until the trailing edge of the clock terminates it. The regeneration line is shown near the top of figure 1.13.

Electrical delay lines play several important roles in the computer. They are utilized in connecting stages where the clock phases are not consecutive; where a circulating register of any given length is required, e.g., the one-word Instruction Register; and where a pulse requires broadening, such as when a negative signal is used in an and-gate for inhibition.

The type of delay line used most generally in SEAC is of the continuous-wound design with an external ground shield. Lines of two different impedances are used: 1,350 ohms into a single gate and 800 ohms into two gates. The type of line used offers several advantages in this kind of computer service, viz., small space requirements, ability to be cut to exact value, satisfactory rise time for half-microsecond pulses, low temperature coefficient, and low attenuation. Delay line lengths in the computer vary from as little as 0.11 to 5.10 μsec.

One of the most frequently used circuits in any digital computer is the familiar Eccles-Jordan flip-flop. Its counterpart in the SEAC type of circuitry is called the dynamic flip-flop. This is not a flip-flop in the usual sense. Whereas the output of a conventional circuit has one of two d-c levels, the dynamic flip-flop output is considered to be in the "one" state when its output is a series of half-microsecond pulses and in the "zero" state when in the unpulsed condition.

The regular gating stage can be connected so as to become a dynamic flip-flop by returning the positive output of the transformer to the input through a delay line. By making the delay around the loop 1 μsec, there will be produced a continuous train of pulses until turned off. Only two and-gates plus a regeneration gate are required. The first gate can turn on the flip-flop with a single pulse, and the second gate serves as the recirculation path. The latter gate must also contain an inhibitor input to turn off the stage when desired.

Although the functions of a given chassis can be traced by using a detailed circuit diagram, this is often extremely arduous because of the maze of signal leads, resistors, tubes, and the like. A set of easy-to-follow symbols was developed during the preliminary period of computer design. These are shown in figure 1.14. As a tube is always associated with a transformer, a single symbol is used to denote both. A small circle indicates a negative output. Gates are symbolized by a closed semicircle, with the arc indicating the output side, thus eliminating the necessity for an arrow. And-gates are distinguished from or-gates by allowing the input lines to come up to the semicircle in the first case and through the semicircle in the second case. Negative pulse inputs

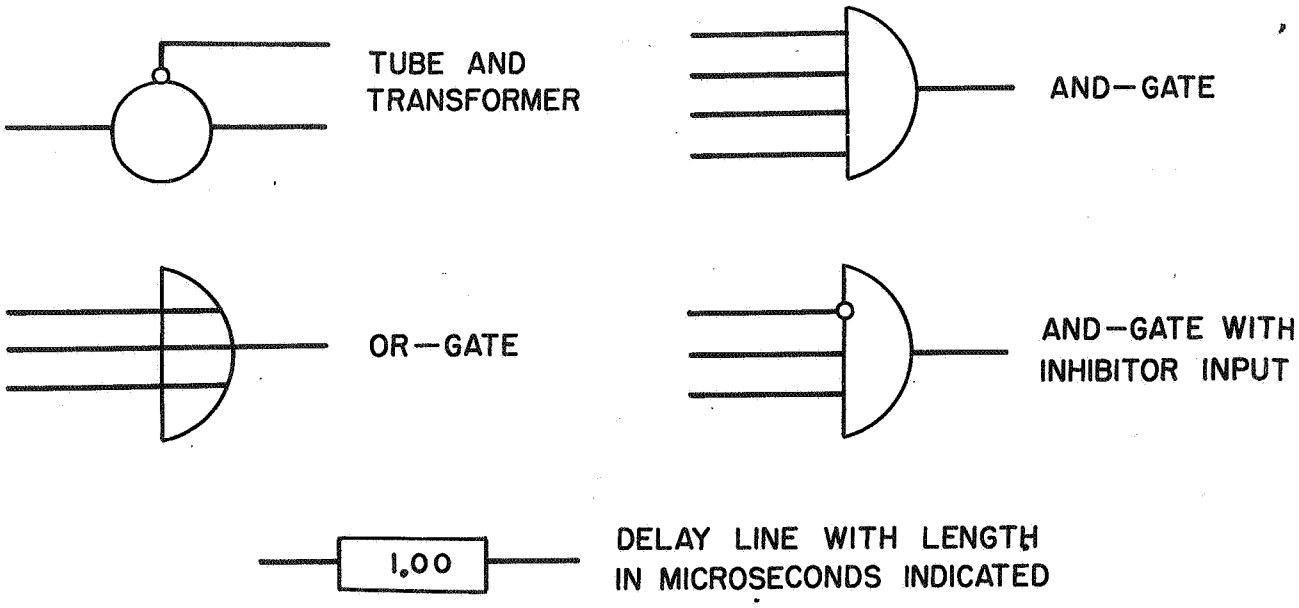

FIGURE 1.14. *Logical symbols used in SEAC.*

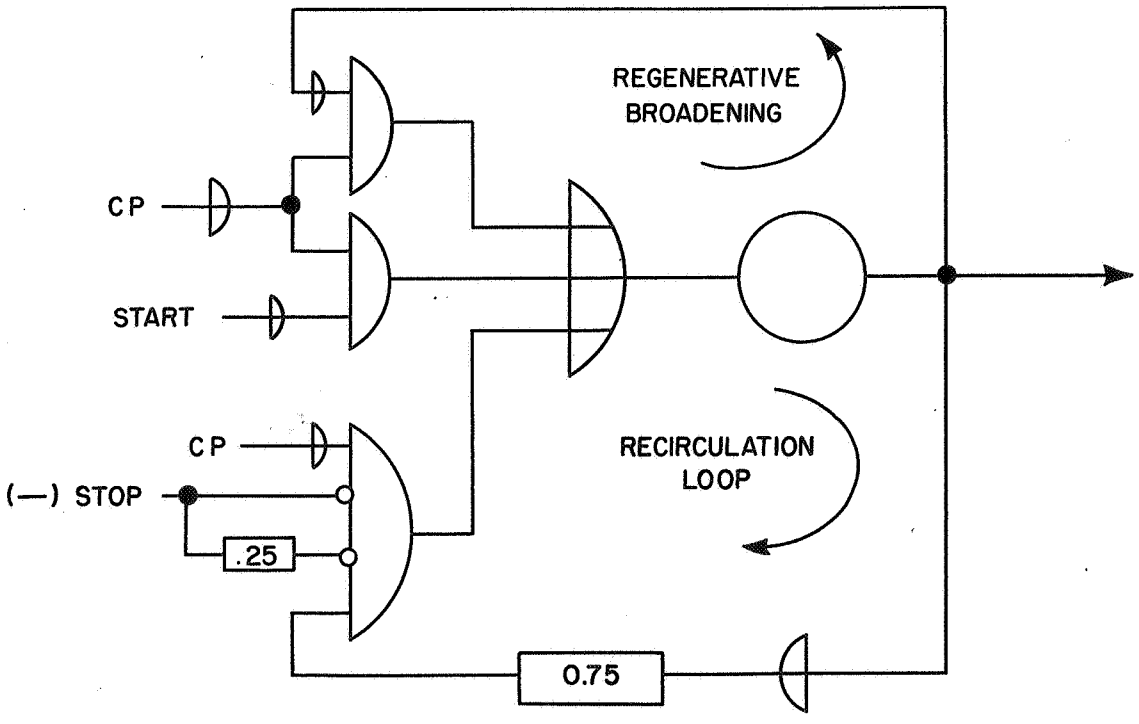

FIGURE 1.15. *Logical diagram of dynamic flip-flop.*

are again indicated by a small circle. Delay lines are symbolized by rectangles with the actual delay period indicated in the box. Figure 1.15 shows how these symbols are used in the logical diagram of the dynamic flip-flop just described.

Several advantages, some very obvious, have resulted from the use of a uniform circuit design. The fact that it allowed concentrated effort on a single type of stage has already been mentioned. Another advantage is that only one tube type is used, and tube selection is based on a single wide specification. The acceptable limits on plate current are 25 to 50 ma, with zero grid bias and + 62 v on the screen and plate. These limits apply when checked with 5.7 v on the filament, as well as with 6.3 v. A tube is also rejected if there is an abnormal plate current variation when checked at the two filament voltage levels.

All diodes in SEAC are subject to the same specification, which, for initial installation, permits only 250-μa back current at 40 v and 2 v forward drop at 20 ma. Before a diode is removed the back current may increase to 500 μa.

It is possible to use unshielded wiring for distances up to 40 or 50 ft without encountering trouble from noise, because of the low effective impedance of the circuits. When the stage is pulsed, the tube-transformer combination presents a very low impedance. During the nonpulsed condition, it is the forward resistance of the −8-v clamping diode that furnishes the low impedance.

5. PHYSICAL CONSTRUCTION

Some of the over-all aspects of the physical construction of SEAC may be of general interest. The frame of the computer consists of two rows of nine standard relay racks (18 in all) with a walkway between. This arrangement does not include the mercury memory and the input-output equipment. When the computer was first put into operation, many of the racks were unfilled. This fitted in with the experimental nature of the machine and allowed for the expansion that was contemplated. At the present time the racks are completely filled by the additions that have since been made. On the interior, all plug-in components are easily accessible as are the interconnections between chassis. On the exterior, all chassis wiring, resistors, and tubes are also readily available. Thus any point on any chassis can be easily inspected either visually or electrically by means of oscilloscope or voltmeter. The accessibility is such that much of the early modification of circuits was done with the chassis in place.

Each relay rack has, on the average, four chassis of varying size. Filament and d-c power are made available at the bottom of each rack, where each line is fused individually. Power is transmitted from one chassis to another merely by plugging each chassis into the one below it.

The three-phase clock system is distributed in very much the same manner as the d-c power. Phasing controls and shaping circuits are provided on each rack for the individual clock phases. The shaping circuits are parallel L-C combinations located at both top and bottom of the rack to help maintain proper sine-wave form.

All signal outputs which must be sent from one chassis to another, are first terminated on a connector strip made especially for this purpose. This terminal strip is a rectangular piece of thin Bakelite on which are mounted pins similar to those used on an octal base, except that they are made available on both sides. For interchassis wiring, flexible insulated wire is used. Small female connectors that fit the pins on the terminal strip are mounted on either end.

Although the mechanical arrangement of components is not the same for all SEAC chassis and reflects the change in ideas that occurred during construction, the majority follow certain practices. Figure 1.16 shows both sides of a typical chassis. It will be noticed that tubes, resistors, and wiring are all located on one side, and the other components are on the other side. Everything except resistors and wiring is plug-in and is easily replaced.

The chassis are essentially two dimensional, although the use of turrets and plug-in components gives a certain amount of depth to the construction. This is achieved without any appreciable loss of accessibility, which is one of the main advantages of the two dimensional layout. Placing tubes and resistors on one side of the chassis and all other components on the other side separates the

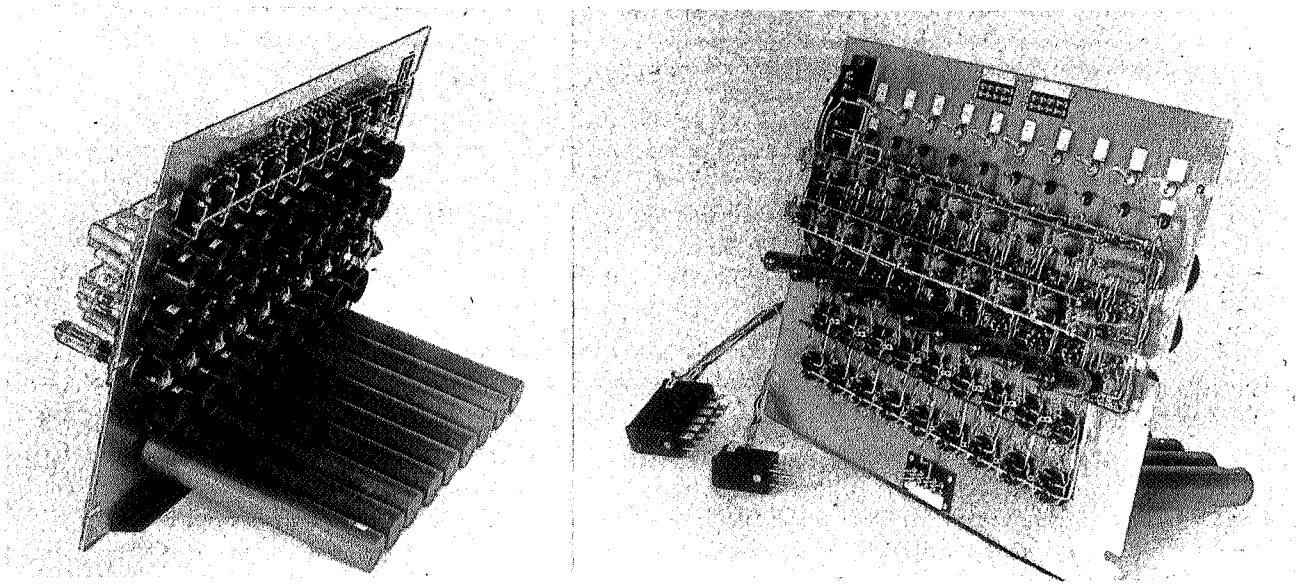

FIGURE 1.16. *Both sides of typical chassis.*

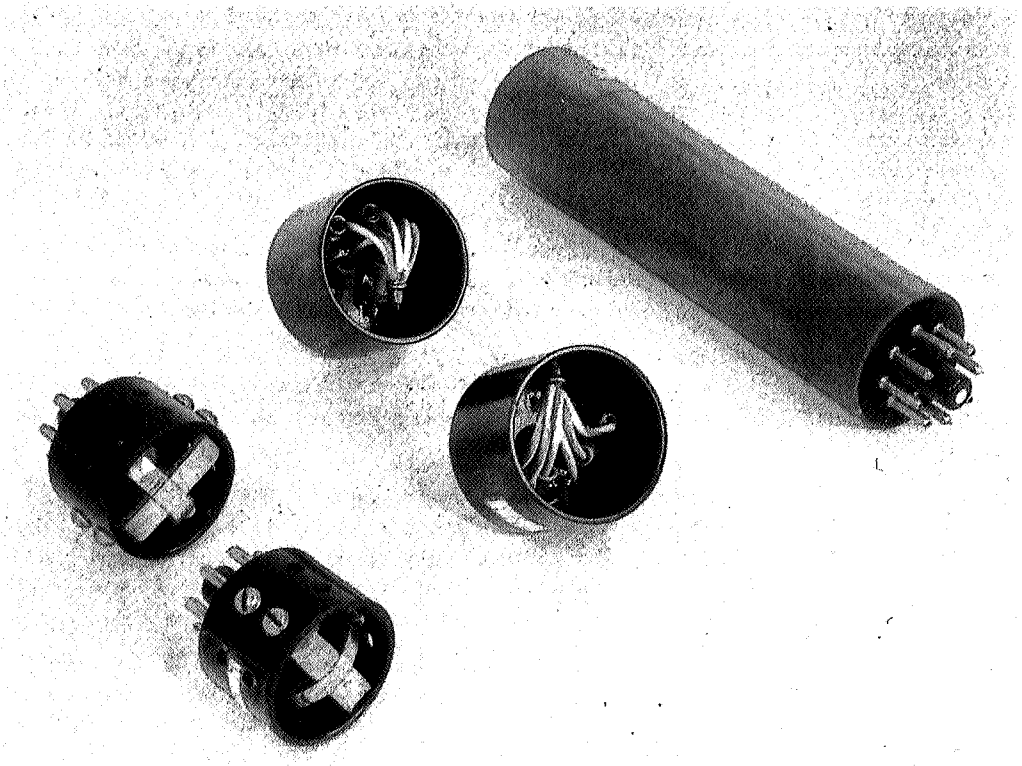

FIGURE 1.17. *Typical plug-in units.*

principal heat-generating elements from the heat-sensitive components, the most sensitive of which are the germanium diodes.

The plug-in components consist mainly of pulse transformers, electrical delay lines, and germanium diodes. Their construction is similar in that all use octal tube bases with solder-dipped connections. In figure 1.16 the first, second, and fourth rows are the diode clusters mounted in octal tube bases. The components in the third row are pulse transformers mounted in similar tube bases. The bottom row contains plug-in delay lines. These are made from a long length of delay line cut into sections of approximately the right length, which are then tailored to the desired value. When the electrical length of the delay line is not more than about 2 μsec, the line can be mounted in an octal tube base and covered with a protective Bakelite tube. Longer lengths of line are coiled in aluminum containers for mounting on the chassis. A more detailed view of typical plug-in units is shown in figure 1.17. The diode clusters, which comprise the majority of the plug in units, consist of from 4 to 7 germanium diodes connected in a variety of ways. By restricting the number of diodes in a cluster to seven, each diode can be checked individually in the unit. As there are over 20 different types, there is sufficient choice to permit the straightforward layout of gating circuitry. When a cluster is rejected from the machine because of diode deterioration, the cluster is salvaged and only the bad diode (or diodes) is replaced.

Depending on their use, transformers are made with several different primary inductances and primary-to-secondary turns ratios. Originally, transformers were potted with a high-temperature wax compound, but later they were bracket-mounted to permit air cooling.

6. OPERATING PERFORMANCE

During most of its 3 years of operation thus far, SEAC has been in use 24 hours a day, 7 days a week. Regularly scheduled computation comprises the bulk of the 168-hour week, with smaller amounts given to routine maintenance and experimental engineering. During routine maintenance periods a continuing check of tubes and diodes is made such that all tubes are checked every 3 months and all diodes every 6 months. In addition, a system of marginal checking is used in which several of the more sensitive gating voltages are shifted up and down. Simultaneously, standard test routines are run and the point at which failure occurs is noted. Any poor tolerances that show up are investigated further. Several other items that are checked during the weekly maintenance period are (1) phasing of 1-Mc clock on each rack, (2) mechanical adjustment of Teletype equipment, (3) gain of Mercury Memory recirculation amplifiers, (4) condition of magnetic tapes.

A fair-sized library of routines has been accumulated for checking the Mercury Memory and various specific machine operations. However, except when unusual difficulties arise, use of two standard test routines is sufficient. One of these checks the memory for its ability to store several different pulse patterns; the other checks the ability of the Arithmetic Unit to perform the various operations. When an error occurs in either routine, the operator can usually diagnose the trouble by analyzing the information printed out.

In a machine as complex as any of the modern digital computers, the operator should be given, in procedure or machine facilities, any aid possible in checking codes and running problems. One of the procedures that has been used to great advantage with SEAC is summing of the memory. For example, after every read-in from magnetic wire, the machine is used to sum the information read-in, after which the sum is compared with the known correct ones. This enables the operator to know immediately whether or not the information has been correctly transferred into the memory.

The use of the sign in the instruction code to halt the computer has already been described. By manipulating one of the switches on the control console, the halt action can be modified in such a way as to help the operator check new codes. On one switch position the machine halts on all negative instructions, on the second position the machine halts only on negative print instructions, and on the third position the machine ignores all coded halts. If the operator uses negative instructions at strategic points (breakpoints), he can more quickly check the accuracy of his coding. Once the code is proved, he can then eliminate these breakpoints merely by throwing a switch without any necessity for changing his code.

Another valuable operator aid is the automonitor feature. The action of printing out the instruction, the result of the operation, and the counter contents is particularly useful when checking out a new code. The operator can set the automonitor switch so that all instructions are monitored or so that only negative instructions are monitored. If a code does not work the first time it is tried, the operator can automonitor the breakpoint instructions. By examining the information printed out, he can determine between what two points in the code the trouble occurred. He can then monitor all instructions between the two points and thus determine the exact point at which the program is in error.

The speed of various arithmetic operations in SEAC is given in table 2. This is arranged by acoustic and electrostatic memories.

TABLE 2

Operation	Time for complete operation, including access time (in milliseconds)			
	Acoustic memory			Electrostatic memory
	max	min	avg	
Addition	1.54	0.19	0.86	0.24
Subtraction	1.54	.19	.86	.24
Comparison	1.20	.19	.70	.19
a. Algebraic.				
b. Absolute.				
Logical transfer	1.54	.19	.86	.24
Logical multiplication	1.54	.19	.86	.24
Multiplication	3.65	2.30	2.98	2.35
a. Major part, unrounded.				
b. Major part, rounded.				
c. Minor part.				
Division	3.65	2.30	2.98	2.35
Base	1.20	.19	.70	.19
File	.86	.19	.52	.24
Clear	1.54	.19	.86	.24

An article on SEAC would be incomplete without some mention of the computation performed since the machine went into operation. During the past 3 years, hundreds of problems covering a wide range of applications have been run on SEAC. A list of broad categories of problems with a few examples in each category follows:

1. Mathematics and statistics:
   Table of Jacobi elliptic functions for real arguments.
   Solution of partial differential equations by Monte Carlo method.
   Generation of optimum sampling plans for the Bureau of the Census.

2. Physics problems:
   Crystal structure.
   Relative abundance of the elements.
   Wave functions for helium atom and for lithium atom.

3. Engineering problems:
   Optical system design.
   Synchrotron design.
   Starting transient in a class C oscillator.
   Transient stresses in aircraft structures.
   Plastic deformation of eccentric columns.

4. Business management and economic problems:
   Problems related to Air Force program planning.
   Problems related to social security accounting procedures.

5. Problems of a security classified nature for the Atomic Energy Commission and the Armed Forces.

2. Dynamic Circuitry Techniques Used in SEAC and DYSEAC

R. D. Elbourn and R. P. Witt

1. INTRODUCTION

Development of the digital computer pulse circuitry to be described began in 1948 with the decision to build the Standards Eastern Automatic Computer, SEAC [1][1]. The functional plan of SEAC was derived from that of the EDVAC built by the Moore School of the University of Pennsylvania. It operates in the serial mode at a 1-Mc pulse-repetition rate. Since the completion of SEAC this circuitry has been improved in reliability and efficiency and has been packaged into just two types of etched-circuit plug-in packages, which are used in the NBS computer, DYSEAC [2].

The first of the decisions that fixed the characteristics of this circuitry was to adopt the serial mode of operation at a 1-Mc repetition rate, as was being used in the EDVAC built by the Moore School of the University of Pennsylvania. The next was to minimize the number of tubes by performing all the logical operations of "and," "or," and "not" between pulses in circuits comprised of germanium diodes and resistors. Such diode circuits were suggested in a preliminary report on UNIVAC by the Eckert-Mauchly Computer Corporation and were described with variations by T. C. Chen [3] in early reports on EDVAC.

To extend the life of the diodes, back voltages were kept low by restricting the amplitude of pulses from 10 to 20 v. On the other hand, complex cascades of diode logic circuits require considerably more driving current than vacuum-tube circuits. Thus there were presented loads of much lower impedance level than vacuum tubes can drive efficiently. An obvious solution was to use small step-down pulse transformers such as had been extensively studied at the Massachusetts Institute of Technology [4]. However, there remained the problem of achieving uniform shape and timing of pulses at the high- but variable-duty cycle that occurs in a serial-type machine.

In addition to supplying large pulse currents at low voltage, the use of pulse transformers has these advantages: ' 1. Eliminating d-c coupling permits all tubes to operate from the same supply voltages. 2. All tubes can operate with positive pulses on the grid, i.e., no inverter stages are required, because with two secondaries each transformer can supply both positive pulses for normal signals and negative pulses for inhibiting. 3. Performance of a-c-coupled pulse-amplifier stages is less critical of tubes, because it depends on only their incremental characteristics.

The disadvantages of transformer coupling stem chiefly from the fact that during a pulse the magnetic flux in the transformer core must increase in direct proportion to the voltage-time area of the pulse, and a corresponding magnetizing current is required in addition to the load current. Then after the pulse, to bring the flux and the magnetizing current down again to their original values, an equal but negative voltage-time area is required. In other words, a negative-going backswing transient must follow each pulse. This limits the maximum duty cycle of pulses to about one-half, so that the speed of the computer is only one-half of what it would be with the same rise time and tolerances if the pulse-envelope or nonreturn-to-zero system could be used. However, this inefficiency is more than compensated for by the greater power that a tube can deliver with a transformer. There do remain, however, some variations in pulse shape and timing due to variations in magnetizing current between the first and later pulses of a train.

In EDVAC the one-word registers needed in the arithmetic and control units are dynamically circulating loops comprised of electrical delay lines, repeater amplifiers, and clocking gates. This scheme is also used in SEAC because it requires fewer tubes than do static flip-flop registers. The logical reduction of this idea to storing an individual pulse in a one-pulse-time circulating loop called a dynamic flip-flop was suggested in the preliminary report on the UNIVAC. The dynamic

[1] Figures in brackets indicate the literature references at the end of this paper.

flip-flop completely replaced the Eccles-Jordan type in SEAC, because it uses only one tube and can drive a number of external gates without additional amplification. These decisions resulted in a 1-Mc repetition rate digital computer circuitry that has basic uniformity in design and clean separation in function: All logical operations are done by diode-resistor circuits, all incidental storage is done by electrical delay lines, and all amplification is done by transformer-coupled pulse amplifiers of a standardized design using only one type of tube.

Since the construction of SEAC, the circuitry has been improved (1) by increasing the positive grid drive, the plate supply voltage, and the turns ratio to obtain more power output; (2) by changing the 1-Mc clock signal from 3-phase to 4-phase to improve timing tolerances; and (3) by substituting a smaller more efficient transformer using a ferrite core [5]. Many features of this circuitry were later adopted by the Moore School in the design of MSAC. Further improvement was achieved by studying the SEAC circuits to find an efficient way to divide them into a few standard plug-in packages. A group at the Air Force Missile Test Center, Patrick Air Force Base, Florida, and another at the Willow Run Research Center of the University of Michigan have each built computers using these packages. More recently the circuitry has been incorporated into etched-circuit dip-soldered packages of just two types. One contains diode gates and buffers with a tube and transformer. The other contains lengths of electrical delay line and suitable terminating circuits.

Although this paper will describe only the vacuum-tube version, it is of interest to note that J. H. Felker has adapted the principles of this circuitry for use with transistors [6]. He retained the configuration of the diode and delay circuits, the repetition rate, and even the impedance levels, but he was able to reduce the levels of voltage and current by a factor of about 10 and to reduce the physical dimensions accordingly.

2. THE TUBE PACKAGE

A tube package contains a tube and transformer, five and-gates, an or-gate for feeding the output of the gates to the grid of the tube, an output buffer to permit the transformer to drive the gates of subsequent packages, and six spare diodes, which may be connected to provide additional inputs to the gates as required. The circuit is shown in figure 2.1. In the normal or quiescent condition of no pulses, the diodes of the gates are conducting because their input terminals are held at slightly below −8 v by being connected to the positive output terminals of preceding packages. Each positive output terminal is held just below −8 v by its −8-v limiting diodes, which are kept conducting by pull-down resistors to −65 v. With the output terminals of the and-gates at about −8 v, the diodes in the or-gate are nonconducting because a limiting diode prevents the 39K (39 kilohm) resistor from pulling the grid down much below −5 v. The 3-v back bias on the or-gate diodes protects the grid from noise such as cross-talk on long leads between packages or variations in forward drop across the −8-v limiting diodes. To achieve the same protection by grid cutoff would require more bias and hence larger pulses, much of which would be wasted in charging the grid capacitance through a region of very low transconductance.

If one compares the direction of low resistance of the diodes in and-gates and in or-gates, it will be apparent that the output voltage of an and-gate approximates its *lowest* input voltage; whereas, the output voltage of an or-gate approaches its *highest* input voltage. Therefore, an or-gate performs the logical "or" function because it will transmit a positive pulse applied to any of its input terminals. On the other hand, an and-gate performs the logical "and" function because it can transmit a positive pulse only when all of its input terminals are pulsed positively.

The choice of resistance values depends upon current requirements, which are calculated by working back from the grid. At the end of a pulse, when the or-gate diodes have all cut off but the grid is still at +2 v, the 39K resistor must pull the grid down by discharging all the parasitic capacitance of the grid circuit. This capacitance is 19 $\mu\mu$f, and a speed of at least 75 v/μsec is required under the most unfavorable combination of 5-percent tolerances on both supply voltages and resistances. At the leading edge of a pulse the 10K resistor in a gate is able to overcome the 39K resistor and to pull the grid up at 75 v/μsec under the worst combination of 5-percent tolerances and with 19-$\mu\mu$f capacitance on the and-gate junction. This includes the capacitance of connecting spare diodes as additional inputs to the gate. At the top of a pulse the 10K resistor supplies grid current required to obtain maximum output from the tube, but the limiting diode connected to +2 v prevents excessive grid current which would occur when two or more and-gates operate simultaneously.

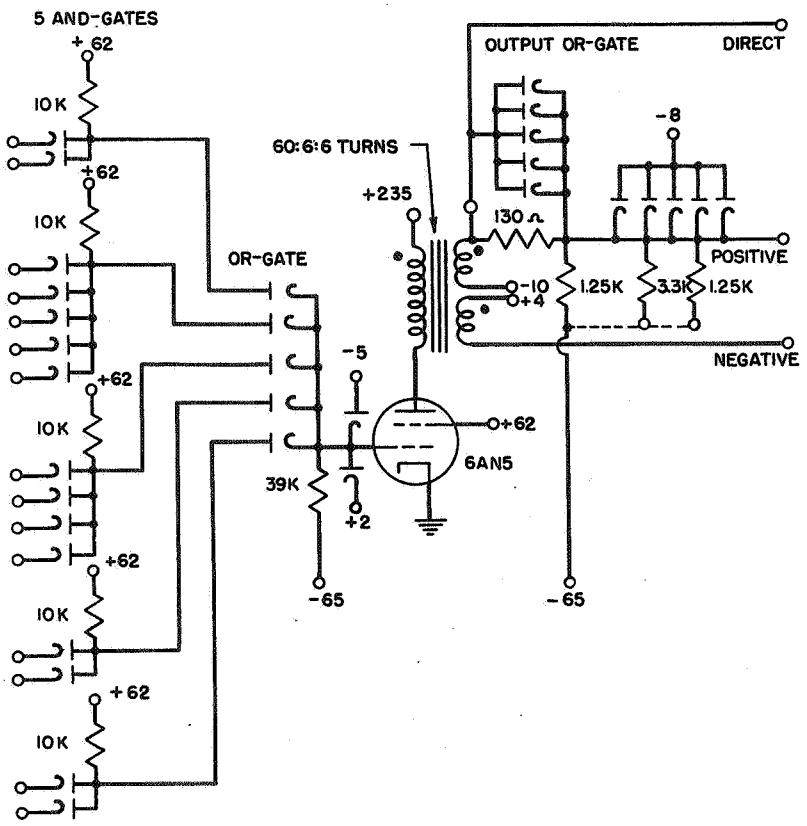

FIGURE 2.1. *Circuit diagram of the tube package.*

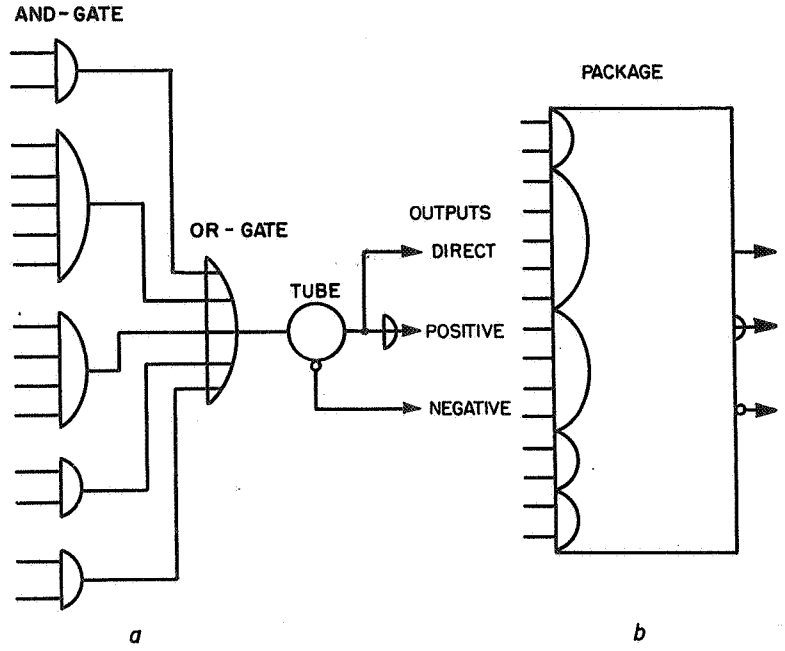

FIGURE 2.2. *Logical diagram symbols for the circuit of the tube package.*
(a) In SEAC notation, (b) in simplified notation.

A diode and-gate imposes quite unusual requirements upon the sources that drive it. When a source pulses positively, its gate diode simply cuts off so that practically no current flows. But when a source is *not* pulsing, it must actively exert its veto power by drawing through its gate diode whatever current is necessary to hold the potential of the and-gate down to about –8 v. Only when *all* the inputs to a gate go positive simultaneously should the 10K resistor be permitted to pull up the output voltage of the gate and, through conduction of its or-gate diode, to transmit a positive pulse to the grid. Whenever some but not all of the inputs to an and-gate are pulsed, the remaining unpulsed inputs must suddenly accept with little change in voltage a different proportion of the current supplied by the 10K resistor; therefore, a low dynamic impedance is required. By themselves, a tube and transformer are not a suitable source, because when not pulsed they may present as much as 300-ohm impedance at 1 Mc. The required low dynamic impedance is achieved by the forward conductance of the –8 v limiting diodes in the output or-gate.

To keep them conducting, even when all other sources pulse, the pulldown resistors that return to –65 v must draw more current than can be supplied by the 10K resistors in all the and-gates connected to the output or-gate. Because the positive pulse secondary of the transformer returns to –10 v, the series diodes in the output or-gate are cut off so that none of this current is trapped in the high dynamic impedance of the transformer. When the tube is turned on, a 20-v pulse appears at the secondary of the transformer, the series diodes conduct, and the transformer supplies the current taken by the resistors to –65 v. Three resistors are provided to permit the load on the positive output to be adjusted to the number of and-gates actually to be driven. Each 1.25K resistor can hold down five gates and the 3.3K resistor can hold down two. The rest of the rated driving capacity of 14 1/2 gates for the package can be used at the negative and the direct outputs. One of the 1.25K resistors is permanently connected to insure that there will be at least enough load to prevent excessive screen dissipation. The 130-ohm resistor that shunts the series diodes of the output or-gate adds no load during a pulse, but it provides somewhat less than critical damping for the negative-going transient that follows a pulse. The combination of the 130-ohm damping resistor and the permanently connected 1.25K resistor is sufficient to prevent the underdamped transient from going above –8 v.

The function of inhibiting an and-gate is accomplished by connecting the negative output of a transformer directly to an input diode of the gate. Because the negative winding returns to +4 v, this diode is normally nonconducting and does not affect the operation of the gate. But whenever a negative pulse is applied to this diode, it becomes the most negative input to the gate and by conducting prevents any positive output at that pulse time. An inhibiting connection does not require an or-gate ahead of it because it carries current only during a pulse, when the tube and transformer present a very low impedance.

The direct output terminal of the transformer is used to drive electrical delay lines and to drive or-gates other than the output or-gate.

For one familiar with Boolean algebra [7] it will be seen that the configuration of diode logic circuits in these packages will allow one to realize any required logical operation. In Boolean algebra "and," "or," and "not" are a complete set of connectives; moreover, the pattern of a set of and-gates feeding one or-gate corresponds to one of the normal forms in which every Boolean proposition can be stated.

For the logical description of computing machines it is certainly desirable to have a more compact symbolism than the complete circuit diagrams. Figure 2.2 shows the circuit of the tube package in a logical symbolism devised when SEAC was designed and also in a briefer symbol appropriate when these packages are used. With the addition of numbers for package location and pin designation, the latter symbol can be the basis of a single-drawing description which can replace logical diagrams, circuit diagrams, and layout charts. Lines carrying negative pulses are marked by a small circle at each end.

Pulses are standardized in shape and timing, and the entire computer is kept in synchronism by making a clock pulse one input to every and-gate. The clock pulses are actually distributed as 1-Mc sine waves at 30- to 45-v peak-to-peak amplitude; however, the effective waveform is just the trapezoidal center slice which lies between the –5- and +2-v grid clipping levels. The delay through a tube and transformer is much less than 1 μsec; in fact, the best timing tolerances are obtained when the clock pulses in successive stages are separated by about 0.25 μsec; therefore, four phases

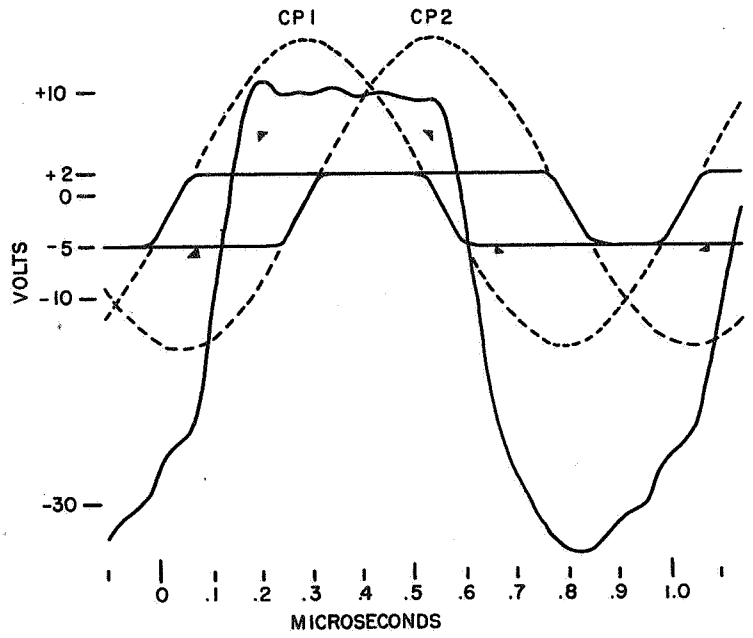

FIGURE 2.3. *Waveform of a typical pulse with the clock pulse from which it was derived and the clock pulse with which it will be reclocked.* Black triangles mark the critical timing limits.

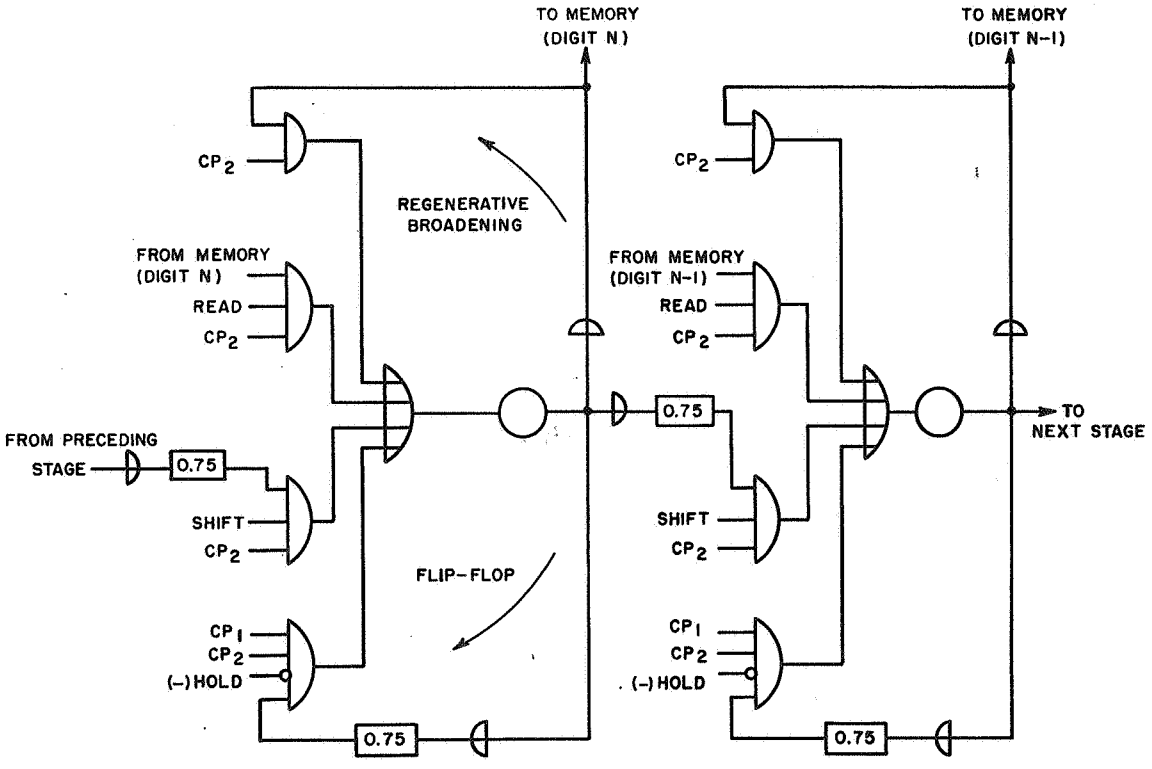

FIGURE 2.4. *Two stages of a typical shifting register.*

of 1-Mc sine waves are used for clock pulses. Figure 2.3 shows the waveform of a typical pulse at the secondary of a transformer. The signal on the grid of that stage was the −5- to +2-v slice of clock phase CP1, while in the next stage the pulse will be gated with clock phase CP2. Notice that the signal pulse does not cover CP2; it cannot because it is too narrow. However, the overlap of the signal pulse with CP2 is sufficient to turn on the next stage; then, once it has been turned on, its own output can be fed back to keep it on until the end of CP2. This trick, called "regenerative broadening," is illustrated in figure 2.4, which shows the logical diagram of two dynamic flip-flops connected together to form part of a shifting register. Either stage may be turned on in one of two ways. The first is by the coincidence of a pulse from the memory and a Read pulse, the second by the coincidence of a pulse from the preceding stage and a Shift pulse. When coincidence does occur the active gate does not rise until such time as the clock pulse CP2 also starts to rise. After the output has risen, the input pulses may fall because the regenerative signal will keep the tube on via the upper gate until the end of CP2. The output signal, delayed 0.75 μsec, arrives at the bottom gate with the next rise of CP2 and so permits the tube to be turned on again. The bottom gate can transmit a signal only during the overlap of CP1 and CP2 (see fig. 2.3). This is wide enough to initiate regeneration but narrow enough to be covered by a negative pulse (−) Hold which can inhibit the bottom gate and so stop circulation in the flip-flop. Other computer circuits are built up in a very similar fashion

3. THE DELAY LINE PACKAGE

An electric delay line is used to enable a transformer to drive a gate which is clocked by a later phase than the next; therefore, only integral multiples of 0.25-μsec delay are required. The problem of reflections from the nonlinear gate loads could be avoided if the characteristic impedance were made so low that the terminating resistance would swamp the nonlinear load of the gate, but this would require a wastefully large driving current. Instead the characteristic impedance is made equal to the pulse voltage divided by the current drawn at the top of a pulse; thus, the line is matched for the main body of a pulse so that only narrow reflections occur during the rise and fall. These are reduced to negligible size by dispersion in transmission and by partial absorption in an input termination.

The type of delay line used was described by Blewett and Rubel [8]. It is built up from the inside out of (1) a core of plastic tubing, (2) a close-wound helix of very fine wire, (3) a sprayed layer of aluminum paint, (4) two layers of Teflon tape, (5) a grounded braid of insulated wires, and (6) a protective cotton serving. Its characteristic impedance is 1,350 ohms, and a 0.25-μsec section is about 5 in. long.

A delay-line package contains one 0.75-μsec section and twelve 0.25 μsec sections along with terminating circuits for five positive pulse lines and for two negative pulse lines. Sections may be connected in series at the socket to obtain other lengths. Figure 2.5 shows the termination circuits connected between a transformer and the line at the input end and between the line and a gate at the output. Spare diodes from a tube package may be connected as shown by dotted lines to form an or-gate between several inputs to a line.

Volt-ampere diagrams in figure 2.6 show how the load-end terminations match the characteristic impedance of the delay line for incident pulses of 16-v amplitude. The terminal voltage and current is a superposition of an incident wave and a reflected wave that must exactly satisfy the terminal resistance conditions. For the incident wave the ratio of voltage to current is just the characteristic impedance, while for the reflected wave it is the negative of this because either the voltage or the current must be reversed by reflection. Dotted lines show the terminal resistance conditions; E_1I_1 denote the incident wave, and E_2I_2 the reflected wave.

For a positive pulse line (fig. 2.6A) the 6.2K resistor returned to −65 v exactly terminates a 16-v incident pulse when the pulse renders the and-gate diode nonconducting. The more obvious termination of a 1.35K resistor to −8 v cannot be used because it would not hold the and-gate down firmly to −8 v whenever there is no pulse on the line.

If an incident pulse arrived when all the other inputs of the and-gate were so positive that the 10K resistor remained connected to the line at the top of the pulse, then a reflected wave E_2I_2 would be produced; however, positive pulses (other than clock pulses) do not rise above +10 v, so

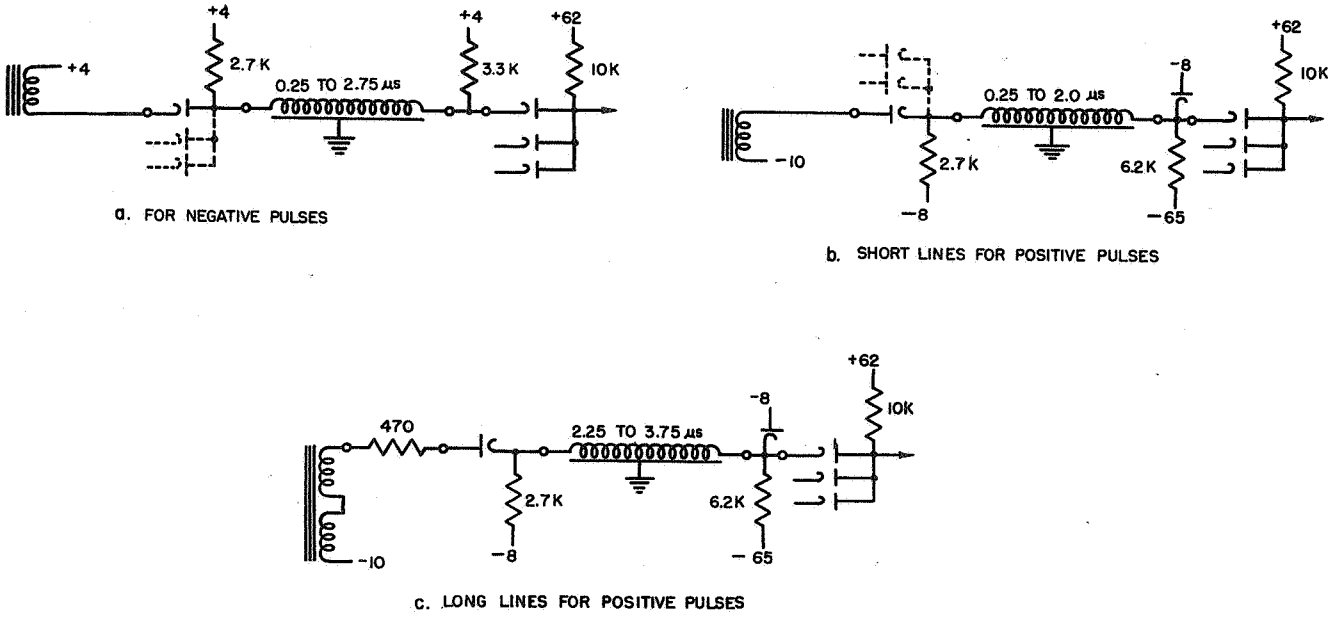

FIGURE 2.5. *Termination circuits for electrical delay lines.*

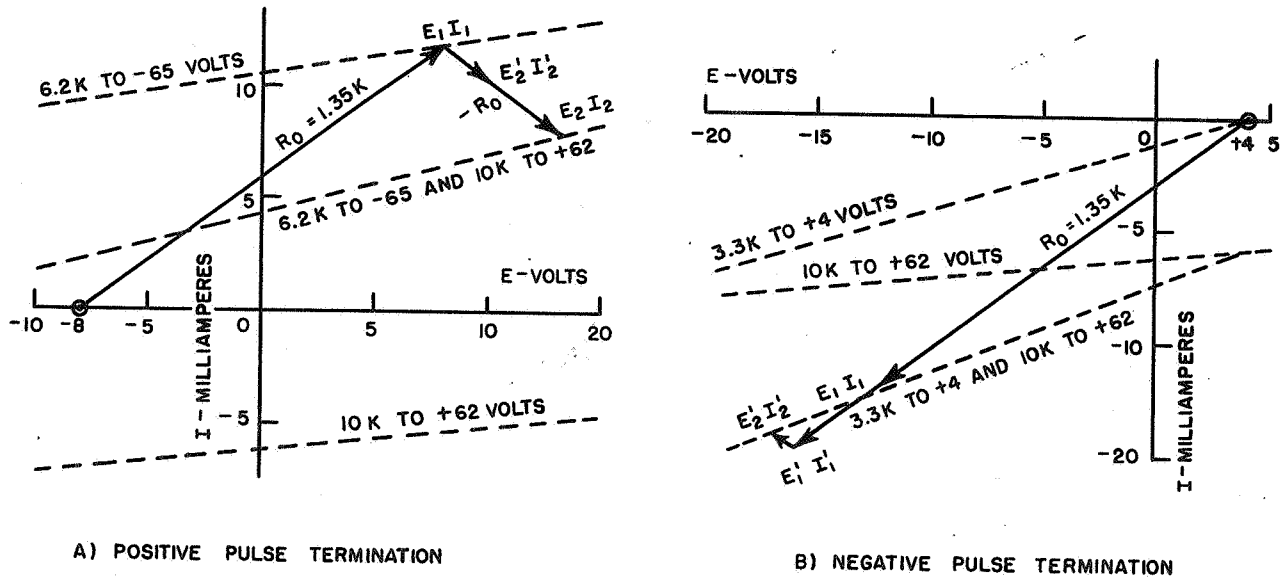

FIGURE 2.6. *Volt-ampere diagrams for delay-line terminations.*

only the smaller reflection $E_2'I_2'$ will be produced. This is comparable in magnitude to the small reflections caused by an incident pulse having more or less than 16-v amplitude because it has suffered more or less attenuation in a longer or shorter delay line than average, or else are caused by variations within the voltage and resistance tolerances.

For a negative pulse line (fig. 2.6B) a 16- to 17-v incident pulse is correctly terminated by the 3.3K and 10K resistors acting together. A 20-v pulse $E_1'I_1'$ will suffer a small reflection $E_2'I_2'$. A somewhat larger reflection is produced if negative pulses from two delay lines arrive simultaneously at the same and-gate and thus have to share the 10K resistor.

The 2.7K resistors in the input terminations absorb enough energy from the small returning reflections to prevent their accumulating seriously in the line, but they do not require as much initial pulse current as would terminations equal to the characteristic impedance of the line. The input diodes disconnect the line from the back-swing transient of the transformer. In long lines the attenuation due to the series resistance of the line (about 1 db/μsec) becomes so great that extra input voltage is required. Connecting both secondaries of the transformer in series gives more than enough voltage, so a 470-ohm series resistor is added to reduce the effective load and to drop the excess voltage, which would produce undesirable reflections.

An output termination intended for a positive line, i.e., a -8-v limiting diode and a 6.2K resistor to -65 v, can be used alternatively as an or-gate between the direct output terminals of several packages and the input of an and-gate, by connecting spare diodes as series input diodes for the or-gate. Two terminations in the delay line package are provided with diodes already attached for this purpose.

4. DESIGN OF THE PULSE AMPLIFIER

The type 6AN5 tube was selected as possessing the best combination of high transconductance, low capacitances, reasonably high current and dissipation ratings, and an efficient heater-cathode structure. Its pertinent characteristics are:

Heater voltage	6.3 v.
Heater current	0.45 amp.
Input capacitance	9.0 $\mu\mu$f.
Output capacitance	5.0 $\mu\mu$f.
Maximum screen dissipation	1.4 w.
Maximum average cathode current	50.0 ma.
Minimum increment of plate current between $E_{c1} = -5$ v and $E_{c1} = +2$ v at $E_p = E_{c2} = 62$ v.	42.0 ma.

The plate dissipation rating is 4.2 w, with 120 v on plate and screen, and 1.7 w with 300 v on plate and screen. In this pulse amplifier the plate dissipation tends to be low because the instantaneous plate voltage is quite low during a pulse. Plate dissipation exceeds 2.0 w in only those tubes which have an unusually large plate current at 5.0-v bias. In service very few heater failures have occurred and no evidence of cathode interface resistance has developed. Some tubes whose heaters were operated at 6.5-v lost emission at about 3,000 hours, but most tubes operated at 6.3 v or below have survived well over 10,000 hours.

Figure 2.7 shows (1) plate-characteristic curves of 6AN5's at grid voltages of -5 and +2, (2) the spread in plate current between high-limit and low-limit tubes, and (3) the load line presented by the output buffer. The reasons for the remarkably low position of the load line and many other design considerations are best explained while following the operation point on the e_p, i_p diagram through a complete pulse cycle.

Before the first pulse the plate is at the supply voltage so the operating point is at A. If the grid is turned on suddenly, the plate current quickly rises to B and must both supply the load and charge all the parasitic capacitances to bring the plate voltage down to C and finally to D. Now, a high ratio of primary to secondary turns on the transformer will give a high ratio of secondary to primary current, but it will also require a high primary voltage to give the required secondary voltage; therefore, more of the plate current will go into the plate capacitance rather than

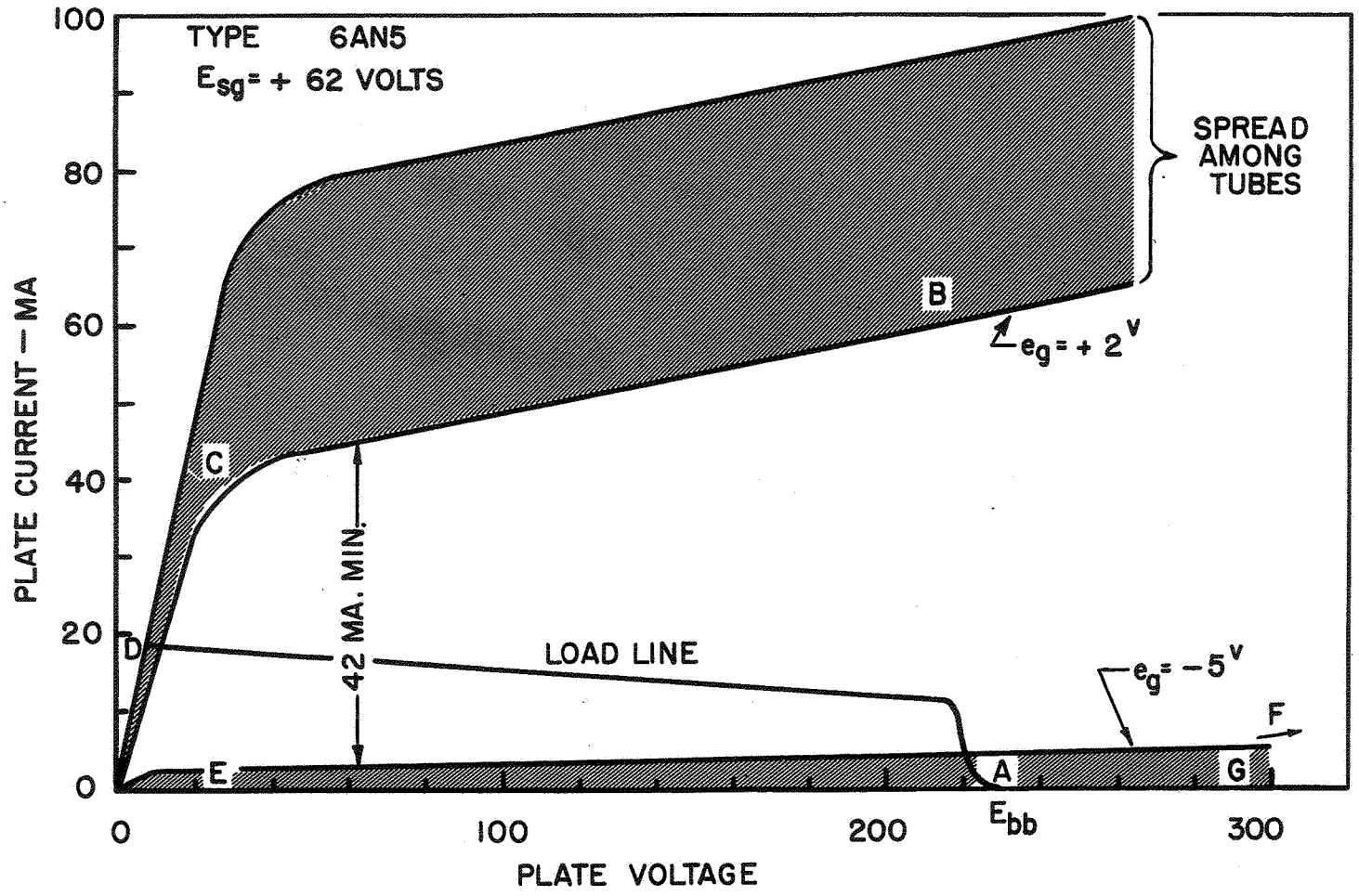

FIGURE 2.7. *Plate characteristics curves with load line.*

into the primary of the transformer. So there is a problem of finding the turns ratio, N, which will give the most secondary current, I_s, for given plate current, I_p, plate capacitance, C_p, required secondary pulse amplitude, E, and allowed rise time, T. If the currents are taken as the average values during the rise, one may write

$$I_s = N(I_p - NEC_p/T).$$

By equating to zero the derivative of I_s with respect to N, one can find the optimum turns ratio

$$N_{opt} = \frac{I_p T}{2EC_p}.$$

This result is easy to remember because it shows that just half the plate current should be used to charge the plate capacitance. The corresponding secondary current is

$$I_s = \frac{I_p^2 T}{4EC_p}$$

Because the secondary current increases with the square of the plate current, it pays large dividends to drive the grid as positive as the dissipation ratings will allow. In this design the plate capacitance, including socket, wiring, and equivalent primary capacitance of the transformer, is 10 $\mu\mu$f; the required secondary pulse amplitude is 20 v; and the allowed rise time is roughly 0.1 μsec. For a plate current of 40 ma obtained from a low-limit tube with positive-grid drive, the optimum turns ratio is 10 and the secondary current 200 ma. This calculation is admittedly only approximate, since it uses average currents during the rise, and the allowed rise time is determined very differently in practice; nevertheless, experiments confirmed the choice of a 10:1- turns ratio. In addition to the delay of charging the plate capacitance, the output pulse is further delayed about 0.02 μsec by the leakage inductance and the load capacitance.

When the plate voltage reaches knee C, the plate current quickly drops to the intersection with the load line at D. At this point a load of at least one 1.25K resistor in the output or-gate is required to prevent excessive screen dissipation. The steep slope of the plate characteristic in this region provides a very uniform pulse height between high limit and low limit tubes and between first and Nth pulses in a train. The high-frequency ringing seen on top of the pulse in figure 2.3 comes from resonance between the leakage inductance and the load capacitance. Inductance in the -10-v supply lead adds directly to the leakage inductance; therefore, close bypassing is desirable.

As the pulse continues, the transformer requires a magnetizing current that increases as the voltage-time area of the pulse, so the operating point gradually drifts up toward C. To prevent its passing around the knee of a low-limit tube before the end of the pulse requires at least 3 mh open-circuit primary inductance.

At the end of the pulse, when the grid turns off, the plate current drops from C to E, and the magnetizing current and load current combine to discharge the parasitic capacitances rapidly to A. Beyond this point the output pulse swings negative as the operating point moves on toward F, because the magnetizing current continues to excite an oscillation of the open-circuit inductance of the transformer with the plate capacitance. The load capacitance is disconnected by the output or-gate. If this oscillation is not damped, a spurious positive pulse will appear in the next half-cycle. On the other hand, if it is overdamped, the magnetizing current will not be quenched before the next pulse time, and it will subtract from the charging current available at the leading edge. The best compromise is to make the transient slightly underdamped in an effort to bring the magnetizing current to zero at the leading edge of the next pulse. In this type of transient the current passes through zero appreciably before the voltage does, so at the start of the next pulse the operating point may be at G; however, the very large charging current available there charges the plate capacitance to B with very little delay.

Because the open-circuit inductances of the transformers employed vary with a standard deviation of about 6 percent, it is not possible always to make the magnetizing current exactly zero at the

start of the next pulse. If the magnetizing current increases by an amount I during each pulse and is attenuated by a factor k in each interval between, then the magnetizing current at the start of an Nth pulse approaches (as N approaches infinity)

$$((Ik+I)k+I)k+\ldots=\frac{Ik}{1-k}.$$

In the worst case, with the primary open-circuit inductance at its upper limit of 4.5 mh, solution of the R-L-C transient gives $k=0.24$. This leads to an estimate of 5.6 ma for the remaining magnetizing current. Experiments with a low-current tube confirm both the slower rise of an Nth pulse with a high-inductance transformer and the earlier fall at the trailing edge when the inductance is too small.

The foregoing theory is not accurate enough to define a final design; instead it provided a reasonable point of departure and helped to interpret the timing tests, which were the real criteria of the design. The central objects of the timing studies are four critical timing limits marked in figure 2.3 by black triangles. Two of these define an interval over which the pulse at the secondary of the transformer must be above +6 v, and the other two define an interval through which it must be below −6 v. The level of +6 v allows for drop in the series diodes of the output or-gate and for attenuation in delay lines. On one hand, these limits are the results of a paper study of the logic circuits in a computer. All the various possibilities for gating or inhibiting between direct pulses or pulses whose waveforms have been distorted by transmission through delay lines were studied to find just what timing limits would insure correct operation. This requires that the pulse to be gated or inhibited is always properly overlapped and yet that no adjacent pulses are improperly affected.

On the other hand, the timing limits are the result of scaling hundreds of photographs of output pulses obtained under the most unfavorable combinations of the following conditions: First versus Nth pulse, high-current versus low-current tube, maximum versus minimum resistive load, no load capacitance versus 300 $\mu\mu$f, 4.5- versus 3.0-mh primary open-circuit inductance, maximum pull-up current in the and-gates with minimum pull-down current in the or-gate versus the opposite, and 45- versus 30-v peak-to-peak clock pulse amplitude. These two definitions of the critical timing limits allow some give and take through adjustable parameters, so the final design was reached by successive approximations.

At the same time a set of loading restrictions was obtained, of which the most noteworthy follow. The maximum resistive load is the equivalent of 14 1/2 gates in addition to the regenerative broadening connection, which is always present. With this load there may be up to 300 $\mu\mu$f of wiring capacitance. With smaller loads there may be more capacitance until a maximum of 1,000 $\mu\mu$f is reached with nine gate loads or less. A negative input to an and-gate counts as only 0.75 of a gate load, a short delay line as 1.75 gate loads, and a long delay line, which requires double amplitude drive, as six gate loads.

5. THE TRANSFORMER

The transformer is completely enclosed by its two-piece cup core in the form of a short cylinder 9/16 in. in diameter by 5/16 in. high. The core is a magnetic ceramic, specifically, sintered manganese-zinc ferrite with approximately the following properties:

Initial permeability	1,000
Saturation induction	3,400 gauss
Curie temperature	130° C
Resistivity	100 ohm-cm.

Its very low core loss and high effective permeability at 1 Mc, as compared with silicon-iron laminations, are primarily due to its resistivity being over 2 million times higher. While the separate losses are quite difficult to measure or to estimate accurately, one can compute that the total loss in the transformer is probably less than 0.1 w because the temperature rise under steady pulsing measures less than 15° C.

Instead of being wound in layers the three windings are arranged side-by-side in deep narrow slots turned in a circular nylon bobbin. The slots for the 6-turn secondaries are just wide enough

for one wire, hence the turns pile up radially. The slot for the 60-turn primary is 5 to 6 turns wide, thus the primary automatically piles up in an approximately bank-wound arrangement, which gives low distributed capacitance. The primary is placed at one side rather than between the secondaries, so that the inside ends of the primary and secondaries can be kept away from each other. Because the positive pulse output has the more critical timing, it is taken from the nearer secondary, which has the smaller leakage inductance. The windings must be carefully insulated from the core because ferrite is very abrasive and is a good enough conductor to provide a breakdown path between primary and secondary.

The core is assembled with no spacer in the butt joint between the ground surfaces of the halves. When one observes that the total reluctance of the magnetic circuit is equivalent to that of an air gap only 0.0006 in. long in the center leg, one can appreciate the importance of cleanliness and of accurate contact of the ground surfaces. Completed transformers, though apparently held together securely by a screw, fiber washers, and lock washers, showed serious inductance changes with rough handling until the practice of dipping in a hard-setting epoxy resin was adopted.

For acceptance, the open-circuit primary inductance is measured at 250 kc with a Q-meter. Acceptance limits are 3.4 to 4.2 mh, although the timing tests were run at 3.0 and 4.5. The small size and high effective permeability make the stray parameters of the transformer quite small. The capacitance between the primary and the nearer secondary is 3.1 $\mu\mu$f, of which only about one-third is effectively across the primary if the assumption that the pulse voltage varies linearly along the windings is valid. The following table shows various short-circuit inductances measured on a transformer whose primary open-circuit inductance was 3.34 mh. Subscripts 1 and 2 denote terminals of the primary; 3 and 4, terminals of the nearer secondary; and 5 and 6, those of the farther secondary:

L_{12}(34 shorted) = 45 μh.

L_{12}(56 shorted) = 80 μh.

L_{34}(12 shorted) = 0.65 μh.

L_{56}(12 shorted) = 0.97 μh.

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3. DYSEAC

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1. INTRODUCTION

The current trend toward the automatization of industrial and commercial operations is opening new areas of interest in which the techniques developed for digital equipment could be exploited. In particular, the unusual flexibility and speed inherent in these techniques could be utilized for automatizing a number of complex industrial control and supervisory tasks. Unfortunately, exploration of these new areas cannot be undertaken efficiently with existing digital computers because of the strong bias in the design of currently operating equipment toward scientific and engineering tasks. If, however, the internal flexibility of machines of this general type were matched by equally flexible means for keeping them in continual communication with devices external to them, digital computers could be used to advantage both in control systems for industry and in information-processing systems for handling the mass paper work of business.

As an example, before digital computers can be successfully incorporated into the often-predicted "automatic factory" and "automatic office" of the future, such equipment must possess ready means for sending intelligence to and receiving intelligence from a variety of external devices performing many diverse functions. Some of these devices will have to store, tabulate, file, convert, display, and sense information; still other devices will have to actuate mechanisms such as servo equipment in response to signals sent out by the computer as a result of information being processed within it. The computer will have to direct all these devices and coordinate their activities into an ensemble operation. Indeed, to achieve the full effect of an ensemble operation, the system needs to have the characteristics of a generalized feedback loop. That is, the computer must not only exert control over these external devices, but they in turn must be capable of calling for alteration in the course of action of the computer. Such requests enter the computer as special signals or information transfers from the external devices.

This feedback arrangement can be used to introduce human monitoring and selective intervention into the normal operation of the system. In its simplest form, pertinent information is displayed to the human monitor who can elect to respond by actuating other external devices that supply the computer with either new data or instructions. This feature will doubtlessly be a highly significant factor in the efficient exploration of the new areas for which digital techniques appear so promising.

The DYSEAC system was planned with just such requirements in mind and is capable of exploring many of these new areas. The planning of the installation has benefited from the component development and system refinement that has flowed out of three years of steady operation and expansion of the SEAC. This experience is embodied in special design features aimed at providing improved reliability, serviceability, and versatility in the installation. Those special features which relate to the system design of the DYSEAC are described in sections 2, 3, and 4 of this article, and those which relate to the physical installation are described in section 5.

The central core of the DYSEAC is a complete general-purpose high-speed digital computer utilizing the same basic electronic circuit elements as those in SEAC. In the DYSEAC, however, these basic building blocks have been organized into a far more powerful system for controlling and responding to auxiliary external devices. As the supervisory and control tasks for which this machine was planned did not require marked increase in computing speeds, the arithmetic powers of the DYSEAC have been only moderately expanded over those in SEAC by reorganizing the computation-control facilities to carry out new and improved arithmetic operations. Major design emphasis was placed, instead, on versatility of control facilities and on latitude for expansion of the installation.

It was deemed important to provide for future expansion of the high-speed internal storage capacity, in case this becomes important for a particular application. Accordingly, the system has been provided with convenient means for supplementing the initial memory capacity of 512 words with additional storage units up to a total capacity of 4,096 words. A more significant provision for expansion, however, concerns the annexation of a wide variety of specialized external devices.

The kind and extent of the external devices to be added will necessarily depend on the particular application which is being explored. Nearly all tasks need some printing and external storage facilities; hence, the initial installation will have a directly connected electromechanical typewriter and one or more magnetic wire cartridges for speedy loading and unloading of the machine. External storage in the form of magnetic tape equipment is also to be included initially in order to handle the more usual computing and data-processing tasks. More demanding tasks requiring somewhat faster access to a rather large volume of data will probably lead to the annexation of one or more magnetic drum units. Still more extensive problems concerned with means for handling masses of paper work will probably lead to the subsequent addition of experimental magnetic disk memory assemblies and experimental versions of the automatic magnetic file. For the exploration of real-time problems, including simulation and control aspects, it will be necessary to annex input and output converters to permit translation of information back and forth from digital to analog form. For example, digital-to-analog conversion is used when visual display of information stored inside the computer is provided externally by means of special cathode-ray tube devices. This listing of external devices includes only those for which serious attention and development are already in progress.

One further device that may be attached to DYSEAC for special experiments is SEAC itself. As the two machines employ the same digital language, this attachment can easily be made through their regular input-output terminals. By use of a coordinated pair of programs, the two machines can be made to work together in common harness on a number of interesting and potentially useful tasks. Indeed, this mode of operation can, by the application of available technology, be extended to a widely dispersed group of information-processing machines that are interconnected by means of a communication network. With suitable feedback facilities and correlated processing programs these machines could even engage in cooperative tasks for which the supervisory functions are transferred back and forth, as the need arises, among the several machines in the network. These new approaches to the problem of automatizing industrial and commercial operations are reasonable extrapolations of current trends and can be expected to lead to practical results if vigorously pursued.

2. SYSTEM FEATURES

The system specifications for DYSEAC are summarized briefly in table 1. Although some of these specifications are similar to those in SEAC or are expansions of SEAC counterparts, many

TABLE 1. DYSEAC system specifications

General operating characteristics:	
Basic repetition rate	One megacycle per second.
Data representation	Binary system; serial mode of representation.
Word length	Forty-four binary numerical digits plus one sign digit.
Instruction system	Three-address system in which a typical instruction word specifies the 12-digit address of first operand (α), second operand (β), and result of operation (γ). Successive instructions are generally located in consecutively numbered memory locations.
Memory	Mercury acoustic delay lines containing eight words each, with a maximum access time of 384 μsec. Minimum capacity: 512 words, stored in a 64-line cabinet; maximum capacity: 4,096 words, stored in eight such cabinets. Automatic parity-digit check of storage accuracy.

TABLE 1. DYSEAC system specifications—Con.

Performance rates of basic operations (including average access time to the memory):

Addition	0.9 msec.	
Subtraction	0.9 msec.	
Accumulate-and-overflow-check	0.7 msec.	
Accumulate-and-store	0.9 msec.	
Summation	0.8 msec.	(plus 0.05 msec. per word).
Multiplication, major (rounded)	3.0 msec.	
Multiplication, minor	3.0 msec.	
Division	3.0 msec.	
Shift	1.1 msec.	(for half-word-length shifts).
Justify	2.0 msec.	(for half word-length shifts).
Logical transfer	0.9 msec.	
Comparison, algebraic	0.7 msec.	
Comparison, absolute	0.7 msec.	
File, unconditional	0.4 msec.	
Breakpoint-file	0.4 msec.	
Input-output	0.3 msec.	(internal program time only).

Special operating features:

Internal program-control features	Dual counter-registers for program sequencing. Base-address and relative-address option.
Joint internal-external control features.	Manual-monitor facilities. Breakpoint-file option. Input-output program-jump option.

are entirely new. Most significant of the new provisions are the Special Operating Features listed at the end of the table. These features are designed to facilitate communication between the DYSEAC and the outside world (i.e., between the machine and the persons operating it or the external devices subsidiary to it) and enable impromptu interchanges of information to occur between them at any time on a completely unscheduled basis. Furthermore, such interchanges can be instigated by either the machine or the outside world, or by both acting jointly.

There are three general properties which give the DYSEAC this versatility:

(1) External-transfer operations, which transfer information between the machine and the external devices, are performed concurrently with internal computing operations; moreover, these transfers can refer directly to any area of the internal memory without restriction as to location or size.

(2) The pace at which the work program is carried out within the machine can be automatically adjusted to the possibly irregular pace at which the external transfer operations are taking place. That is, whenever it is necessary for the internal and external programs to proceed precisely in step with each other, the machine can manage to keep the slower-moving external program abreast of the high-speed internal program by forcing the latter either to halt or to change its course temporarily. This self-regulation property enables optimum use to be made of the concurrent input-output ability of DYSEAC on jobs which require considerable transfer of information into and out of the machine, or which involve searching through voluminous magnetic files.

(3) The work program can be interrupted whenever necessary, and a wide variety of special orders can be interpolated into the program either by the operator of the machine or by the external devices. This interruption property enables the machine to cope with unscheduled job assignments which originate, with little or no advance notice, in external events occurring beyond the supervision of the machine and which must be executed as soon as possible for real-time applications such as air-traffic control.

It should be noted that these three properties, by their combined presence, create a fourth property of considerable power. That is, acting in concert, they enable the machine to be employed effectively as a control element in a generalized feedback loop.

These over-all properties are derived principally from three special operating features of the Program Control, the Input-Output Control, and the Manual-Monitor facilities in the DYSEAC, all

of which will be described briefly in the following sections. A more complete description is contained in the appendix to this paper.

The term "manual-monitor" has been coined to describe five types of operations which are either initiated manually by the machine operator, who for example presses a push-button, or else are initiated by the machine itself under conditions which are specified by means of external switch settings. The former is referred to as a manual operation, and the latter is called a monitor operation because the machine must monitor its internal program to determine precisely when the operation should be performed. The type of operation to be performed as well as the conditions under which it is to be performed are specified by means of external switch settings.

Manual-monitor operations can readily be specified and initiated by external devices as well as by human operators. Furthermore, since all of the external switch settings control only d-c voltages, the external devices can even be remote from the machine itself and they can from a distance (connected to it via ordinary electrical transmission lines) exercise supervisory control over the internal program of the machine.

The five types of manual-monitor operations that can be performed are (1) loading operations, which load new information into specified portions of the machine such as various memory locations and storage registers; (2) print-out operations, which print out the contents of these memory locations and storage registers; (3) insert-in-the-program operations, in which a new instruction is interpolated into the internal program between the items of the scheduled instruction sequence; (4) change-in-the-program operations, in which an entirely new sequence of instructions is substituted for the scheduled instruction sequence; and (5) halt-the-program orders, with warning signal. Various combinations of these five types of operations also can be performed. For example, the machine can be told to perform a compound operation such as the following one which involves both loading and insert-in-the-program operations: Load the entire memory, and take the next instruction from memory location X. (X represents an arbitrary address number previously entered into the machine via the operator's keyboard or from an input unit.)

Monitor operations are performed by the machine whenever the conditions specified by the external switch settings occur in the course of the program. These conditions can be chosen from among a wide variety of program occurrences, e.g., every time the program refers to a new instruction or makes a reference to the memory, any time the program refers to an instruction to which a special monitor symbol is attached, any time the program refers to a Comparison (branch) instruction which results in the selection of either one of the two alternative next instructions, any time the program refers to a location in the memory which matches some specified address number or which falls within certain specified limits, and any combination of these or other special conditions.

By pairing a particular type of manual-monitor operation with a selected set of conditions, a wide variety of special operations can easily be specified and performed. Among the simpler of these are the following examples. (1) Every word written into or read from the memory at each step of the program can be printed out. (2) The contents of a specified memory location can be printed out whenever and as soon as the memory location is referred to in the course of the program, with the option of halting the program at that time if desired. Neither of these operations requires the preparation of any special routine. (3) Various fixed memory addresses or groups of fixed addresses may be continually printed out even while computation is proceeding.

For every manual-monitor operation, the external switches are set to specify not only the type of operation to be performed and the conditions under which it is to be performed, but also the storage places which are to be involved. These storage places can be chosen from a long list of available locations in the high-speed internal memory and from among five different storage registers in the machine. The memory locations may be designated in a variety of ways: either in the usual way, as an address number, or indirectly as an address specified by the current instruction, or as the address scheduled for next reference in the course of the program. These indirect ways are an advantage to the user of the machine who can, for example, direct the machine to print out the result of each operation without knowing (or being required to specify) the address in which each result is to be found.

Thus, by means of the external switches, certain storage areas within the machine may be utilized by devices remote from it. These remotely located devices can direct that information in certain areas of the memory of the machine be transmitted to them. Similarly, they can arrange to insert new information into various portions of the memory. In this way, at the option of either the external devices or the machine program, or both acting jointly, the DYSEAC can share with these remote devices its high-speed memory and consequently every other part of its internal computing and external storage facilities.

This feature makes it possible for two or more full-scale computers (such as SEAC and DYSEAC) to be harnessed together and work in mutual cooperation on a common task. Each member of such an interconnected group of separate computers is free at any time to initiate and dispatch special control orders to any of its partners in the system. As a consequence, the supervisory control over the common task may initially be loosely distributed throughout the system and then temporarily concentrated in one computer, or even passed rapidly from one machine to the other as the need arises.

Further aspects of the control interrelationships available in DYSEAC will be discussed subsequently, after the other Special Operating Features in the machine have been described.

Two other special operating features of the DYSEAC are *Breakpoint-File*, which is a program-control operation, and *Program-Jump*, which is an input-output control operation, Before describing these operations, it will be necessary to outline the program-sequencing features of the machine.

The sequence of instructions which specifies the work program for the machine is normally a consecutive one; i.e., consecutively executed instructions are normally located in consecutively numbered address-locations in the memory. Means for interrupting this consecutive sequencing of instructions and for initiating a new sequence are provided by a variety of choice instructions and counter-setting instructions. (See Comparison and File operations, respectively, in table 2, which describes all of the instructions available in DYSEAC.) The user of the machine, viz., the programmer, has the facility not only of initiating new instruction sequences at any time but also of choosing between two possible alternative sequences. He may, if he wishes, interleave two distinct sequences, periodically jumping from one to the other in an arbitrary manner. This facility is made possible by a scheme which provides two separate counter-registers for program sequencing, each of which holds an address-number. The address-number in either counter-register may be chosen as the address of the next instruction to be performed [1].[1]

The address-numbers in these two counter-registers can also be used for another distinctly different purpose, namely, as *base-points*. That is, at the option of the programmer, the address-number in either counter may be used as a base-point, or origin, for those address-numbers in subsequent instructions which the programmer has designated as *relative* addresses. In other words, if address-number X is designated as a relative address in an instruction, the memory location referred to is no longer X but a new location displaced from X by the number stored in the chosen counter. For example, if the chosen counter contains the number C, then whenever address X is designated as a relative address in an instruction, the memory location referred to is (X + C).

In utilizing this counter-register and relative-address facility, the programmer may elect to follow either of two methods. The first method makes use of a *fixed* base-point, which the programmer modifies only occasionally as the program proceeds. The second method makes use of a *floating* base-point, which is the address of the instruction-word itself and therefore progresses constantly. With this second method, the memory locations of the operands referred to in the program may be specified relative to the location of the instruction word even when that location is not known at the time the program is being planned.

The Breakpoint-File operation can now be described. As indicated in table 2, the control counter-registers can be reset by means of the two types of file operations: File (unconditional) or Breakpoint-File. These two operations allow the programmer to set either control-counter to any arbitrary value, specified either in an absolute manner or relative to its current setting. Since the contents of these counter-registers specify the memory location of the next instruction to be performed, the File operations may readily be used to initiate entirely new branches in the program.

[1] Figures in brackets indicate the literature references on page 57.

TABLE 2. Description of DYSEAC basic operations

Name of operation	Description of instruction
Addition	Form the sum of the word in α and the word in β, and write the result in address γ in the memory.
Subtraction	Form the difference α minus β, and write the result in address γ in the memory.
Accumulate-and-Overflow-Check.	Form the sum of the word in α and the word in β plus the contents of the arithmetic accumulator register. If the sum does not overflow, store the result in the accumulator and proceed to the normal next instruction; if the indicated sum does produce an overflow, however, leave the previous contents of the accumulator unchanged and take the next instruction from address γ in the memory.
Accumulate-and-Store	Form the difference α minus β, add the contents of the arithmetic accumulator register to it, and write the sum in address γ in the memory. Then clear the accumulator.
Summation	Form the sum of the words located in consecutive address locations running from β through α, inclusive, and write the sum in address γ in the memory.
Multiplication, major, rounded.	Form the product of the word in α and the word in β, and write the major part (rounded off) in address γ in the memory and in the arithmetic accumulator register.
Multiplication, minor	Form the product of the word in α and the word in β, and write the minor part in address γ in the memory. Also write the major product, unrounded (with proper sign), into the arithmetic accumulator register.
Division	Form the quotient of the word in β divided by word in α, and write it in address γ in the memory. Also write the remainder into the arithmetic accumulator register with the sign of the dividend.
Shift	Shift the word in α according to the code indicated in the word located in address β in the memory, and write the result into address γ in the memory. The seven numerical digits on the extreme right of the word in memory location β indicate the number of binary places the word is to be shifted and the direction of the shift (left or right).
Justify	Determine the number N satisfying the following inequalities: $[\beta] \leqq [\alpha] 2^N < 2[\beta]$. Write this number with proper sign into the seven digit positions on the extreme right of the word in address γ without altering its other digits in any way. Note: $[\beta]$ means absolute value of the word in address β in the memory, and $[\alpha]$ means absolute value of the word in address α in the memory.
Logical transfer	Write in address γ in the memory those digits of the word in α which correspond to one-digits in the word in β. Leave the word in γ unchanged in those digit positions which correspond to zero-digits in the word in β.
Comparison, algebraic	If the word in α is algebraically greater than or equal to the word in β, take the next instruction from the normal consecutive address position. If, however, the word in α is less than the word in β, take the next instruction from address γ in the memory.
Comparison, absolute	This instruction is similar to algebraic comparison, differing from it only in that the indicated inequalities pertain to the absolute values of the numbers indicated.
File, unconditional	Write the contents of the control counter-register (and certain other control data) in address β in the memory; reset specified counter to γ address-number; adopt contents of specified counter as relative-address base-point in subsequent operations.
Breakpoint-File	This instruction is similar to unconditional file except that it requires the setting of an external Breakpoint-File switch to indicate that its activation is desired. If the switch is not so set, the instruction is passed over without effect.
Input-Output	Load (or print-out) the designated area in the high-speed internal memory from (or to) the designated area in the external storage or input-output unit. After initiating the operation, the program proceeds immediately to the next scheduled instruction. When the external operation is completed, execute program-jump if so indicated.

Furthermore, since these operations cause a complete record of the status of the program to be written into the memory just prior to starting a new branch in the program, the abandoned branch can be resumed without difficulty later on, if desired.

The Breakpoint-File operation has the same characteristics as the File (unconditional) operation except for one important additional feature. It requires the setting of an external switch to indicate that Breakpoint-File activation is desired. If this external switch is not so set, the Breakpoint-File instruction is passed over without any effect on the machine. Therefore, by locating Breakpoint-File instructions throughout the program at strategic points, the course of the program can be changed at these points merely by the turn of a switch. This feature provides a simple and powerful means whereby the course of the internal activities of the machine can be controlled by the external environment.

Before considering the third special operating feature of DYSEAC, namely the Input-Output Program-Jump operation, a typical input-output operation in which information is transferred between an external device and the high-speed memory of the machine will be described. It might be noted again that any consecutive areas of the memory in DYSEAC, ranging in size from a single word to the entire memory, can be loaded or printed out even while a program of computation is proceeding. Automatic interlocks are provided to guard against inadvertent attempts to use a memory location for conflicting purposes. For example, if a print-out order is given, the machine is automatically prevented from writing into any memory location affected by the print-out order until the word in that location has been printed out.

A typical input-output operation proceeds in the following manner. First the machine selects the particular external device or unit with which communication is desired. The code number signifying this unit is specified in the input-output instruction. In the second step of the process, the machine runs through a specified number of words or blocks of words on the selected unit, the starting point being the word lying nearest the reading heads for the magnetic wire or tape units, and a fixed origin on the periphery for the magnetic drums. For other types of applications, this step may be used to introduce a variable delay. In the third step of the process, which begins after the requisite number of words has been counted out, the transfer of words between the external unit and the internal high-speed memory takes place. The transfers commence with the numerically smallest address in the indicated block of words and proceed in consecutive order until the numerically highest address is reached, thereby concluding the operation.

Each input-output instruction not only specifies the particular external unit which is involved in the transfer of information and states whether the transfer is to be a Load or a Print-out operation, but also indicates where the information is to be found and to what destination it is to be transferred. Finally, the instruction indicates whether or not a Program-Jump operation is desired after completion of the input-output operation. If a program-jump is desired, then a signal is produced after the input-output operation is completed which causes the program to jump, i.e., the counter-register being used as the source of the next instruction is temporarily abandoned, and the instruction word in the address location specified by the other counter-register is executed in its stead.

This program-jumping feature is useful in many situations. For most applications which make use of concurrent loading or printing-out of the high-speed memory while computations are proceeding, the precise length of time required to complete the external operation is either indeterminate or else quite difficult to predict. A typical example of an instance of this type occurs when it is necessary to hunt for a particular word or group of words in an unknown location on a long magnetic tape reel, where a word can be identified as one of the desired type only after it has been read into the machine and subjected to an analysis of its characteristics. Since efficiency requires that information be read into the high-speed memory in fairly large blocks, it is desirable during the comparatively slow procedure of reading in the information to make use of the ability of the system to proceed concurrently on other independent phases of the program. By means of the input-output program-jumping feature, the programmer is able to direct that these other independent phases of the program be allowed to proceed uninterrupted until the specified loading of the information is completed and that as soon as the loading is completed, the program should jump to an alternative specified routine which is designed to analyze the newly received information and to decide whether or not to retain it or to continue hunting on the tape.

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An analogous need arises when it is desired to check the accuracy of information printed out on the external medium by reading the information back into the machine and comparing it with its original source. A process of this sort would require a Print instruction followed by a Load instruction. In order to avoid having the program stand by while the print-out operation is being completed, the programmer can arrange for other internal operations to be carried out concurrently which would be interrupted only when the print-out operation is concluded, at which time the Load instruction would be initiated.

More generally, the Program-Jump facility provides a means by which the machine can order an external unit to carry out an assigned task and at the same time periodically report back its progress in carrying out the task so that the machine can maintain the closest possible check on the external operation and redirect it properly as the need arises.

After effecting a program-jump, the new program that is initiated may, as soon as its final instruction is performed, cause the machine to resume the interrupted program where it left off, if the programmer so desires. An automatic interlock relieves the programmer of the burden of having to estimate precisely how long a time will be required for the original input-output operation to be completed and insures that all the steps in the program will be carried out in their proper sequences. The system is so designed that the order which appears first in the program must be satisfied before any subsequent conflicting order can be carried out.

In concluding the discussion of the special operating features of DYSEAC, it should be noted that the various interruption facilities which have been described are based on mutual cooperation between the machine and the external devices subsidiary to it, and do not reflect merely a simple master-slave relationship. With the Breakpoint-File feature for example, the external device which operates the Breakpoint-File switch initiates the request for the branching action, but the actual execution of the operation must await confirmation of the request by the machine, i.e., the occurrence of a Breakpoint-File instruction in its program. In the case of the Input-Output Program-Jump, on the other hand, the initiation of the request originates in the internal program (via an Input-Output instruction containing a jump-order symbol), while the actual execution does not take place until the external device returns the proper signal, signifying termination of the operation. The third variety of internal-external action, the manual-monitor type, exhibits aspects of both types of control relationship. For the simple manual operations, the external unit (or the operator) exercises full control over both the initiation and execution of the request, e.g., by push-button. For the monitor operations, however, the request can be considered as initiated externally (by turning breakpoint-choice switches) but the actual execution of the operation does not occur until the requested conditions arise in the course of the internal program.

These varied internal-external joint-control relationships are summarized in table 3. For each of the special operating features (Breakpoint-File, Program-Jump, and Manual-Monitor operations), table 3 indicates whether an internal or external source initiates the request for the operation and whether an internal or external source decides to execute the operation. This same information is

TABLE 3. Internal-external joint-control properties of DYSEAC special features

	Source which describes operation	Source which initiates operation	Source which decides to execute operation
Special operation:			
Breakpoint-File operation	Internal	External	Internal.
Input-Output Program-Jump feature	do.	Internal	External.
Manual operation	External	External	do.
Monitor operation	do.	do.	Internal.
Conventional operation:			
New instruction brought in from input unit by program.	External	Internal	Internal.

also given for the more conventional method of control, which consists of calling new instruction words into the memory of the machine by means of a programmed input instruction. It is evident that the control interrelationships provided by the special features of DYSEAC are distinctly different for each special operation and that equivalent control versatility cannot be achieved by the more conventional program method. Indeed, the foregoing special features were incorporated into DYSEAC only because the joint-control properties needed for its intended applications could not be secured satisfactorily otherwise, even by the use of special or complex internal programming procedures.

3. OVER-ALL FUNCTIONAL ORGANIZATION

The over-all functional organization of the DYSEAC is indicated in the block diagram of figure 3.1, which shows the major communication routes and control relationships in the system.

The High-Speed Memory shown in the center receives and distributes to the other units the information (numerical and instruction) to which the most rapid access is needed for carrying out the work-program of the machine. The memory communicates principally with five major units of the system. Of these, two are concerned primarily with internal processing affairs and three with external relations. A continuous flow of digital information may be maintained simultaneously between the memory and the inward-looking and outward-looking types of units. The latter types, which serve to communicate with the external devices represented on the left side of the block diagram, include the Input-Output Buffer, the External Selector, the Concurrent Input-Output Control, the Display Staticizer, and the Serializer.

The function of the Input-Output Buffer is to transmit information at the proper repetition rates from the external unit to the internal memory during an input operation, and in the reverse direction during an output operation. The buffer receives words from the memory at the normal 1-Mc internal repetition rate and then transmits them out digit-wise at the proper measured rate appropriate to the external unit. The external unit itself (via the External Selector) specifies the word format and repetition rate appropriate to it. Provision is made in the Input-Output Buffer for handling information in various forms, e.g., in a single-channel serial form for magnetic wire units, in serial-parallel 4-channel or 6-channel form for magnetic tape units or Flexowriter, and in fully parallel 45-channel form for magnetic drum. A wide variety of other formats is also available if needed. The initial range of repetition rate may be up to 16 kc (single channel). If higher rates are desired in the future, an additional buffer storage register may be added to the system.

The External Selector is a high-speed electronic switching device which selects the external unit with which an input-output operation is to be performed. It provides the signal required to operate the proper multichannel electromechanical relay or other device which completes the circuit connections for the lines carrying both the digital information and the control signals needed to operate the external unit. The design of the External Selector has been chosen so as to be readily expandible whenever additional external units become available. The initial model contains provision for selecting among up to 48 distinct external mechanical relay switches, but it can be expanded, with about an equal amount of additional equipment, to be capable of handling up to 256 distinct information channels, such as individual parallel magnetic-drum channels or high-capacity magnetic filing systems.

The External Selector accomplishes its switching function by a process of scanning successive switching channels in synchronism with a counter located in the Input-Output Control Unit, starting from a fixed origin. As a result, a gradation of electronic switching access times is available, ranging from a minimum of about 25 μsec for the channel closest to the origin to a maximum of about 6 msec for the last channel of an expanded 256-channel model. This wide range of switching speed can be matched to the operating rates of the external devices themselves, e.g., the first 20 channels, whose average access time is 0.25 msec, might be chosen to communicate with high-speed external units capable of reacting in 1 to 2 msec, while the last 200 channels, whose average access time is about 4 msec, switch with speeds compatible with the average rotational access time of a 3,600-rpm magnetic drum. A feedback checking feature is provided in the External Selector for insuring that one and only one channel is selected and that it is the channel requested by the Input-Output Control Unit.

The Concurrent Input-Output Control has the function of regulating the detailed progress of all input-output operations requested in the course of the internal program. It directs the flow of traffic between the memory and the Input-Output Buffer, and between the Input-Output Buffer and the External Selector. It instructs the External Selector to step along to the proper switch channel, checks that contact is made with the desired unit, and signals the Input-Output Buffer to proceed to accept digits either from the external unit during an input operation or from the high-speed memory during an output operation. It receives signals from the Input-Output Buffer as each complete word is transferred, and it not only keeps count of the total number of words handled, but also keeps track of which address in the high-speed memory contains the word currently to be transferred. This information is transmitted to the Memory Address Switches at the proper time.

In the comparatively unlikely event that both the Input-Output Buffer and some internal unit should simultaneously demand access to the high-speed memory, the Concurrent Input-Output Control resolves the conflict by according temporary priority to the external operation [2]. Likewise, it referees conflicts or inconsistencies between the internal program and the progress of external operations. It also notifies the Program Control unit at the termination of an input-output operation so that the program-jump may take place. Its other functions include regulation of the memory error-seeking scan process and the Summation operation.

The Display Staticizer and the Serializer are input and output organs adapted especially for real-time operations. The Display Staticizer is a register storing 28 bits statically in parallel for controlling, for example, a digital-to-analog converter that provides deflection voltages for CRT visual displays. The register is loaded periodically, cycling through a chosen group of words in the high-speed memory. The size of this group, one to 32 words, and its location in the memory are adjustable manually. The cycling process proceeds through the specified area independent of the internal program and in no way interferes with the use of the area by any other units, such as Arithmetic Unit or Input-Output Buffer.

The Serializer unit is provided for continuous real-time external input devices. This unit can accept one full word of 45 bits delivered in parallel in the form of asynchronous pulses from an external unit (minimum pulse duration about 50 μsec) and can transmit the word in synchronized normal serial form to any other units of the system capable of reading words out of the high-speed memory. The Serializer, however, can provide words to the other units at about 4 1/2 times the average access rate of the acoustic memory.

The Arithmetic Unit (lower right-hand corner of fig. 3.1) carries out a group of 13 arithmetic or choice operations. Arithmetic results are written directly into the high-speed memory, and control signals specifying the outcome of the discrimination operations are sent directly to the Program-Sequencing and Control Unit where they serve to modify the choice of memory location from which the next instruction is to be read. A third route of communication to the Input-Output Buffer, labelled "special word transfers," represents the facility of loading or printing out the contents of the arithmetic accumulator register directly via the Flexowriter or magnetic input-output units.

The remaining unit in direct communication with the high-speed memory is the Instruction Register. Instruction words are transferred one at a time, as needed, from the memory into the Instruction Register. From this unit, pieces of information contained in different segments of the instruction-word pattern are selected by the Program Control Unit and transmitted to various other internal units throughout the system. From the Program Control Unit, digital address codes pertaining to each phase of each operation are sent to the Memory Address Switches in order to make the specified memory locations available to the Arithmetic Unit and Instruction Register at the proper time. This information is made available to the Concurrent Input-Output Control at the same time for checking against possible conflict with current input-output operations. Furthermore, whenever an input-output instruction is received in the Instruction Register, the Program Control routes it immediately to the Input-Output Control Unit and proceeds to call a new instruction word out of the high-speed memory. Finally, during the File-type operations, various items of program-control information can be written out of the Program-Control Units directly into the memory. This same information can also be transferred into or out of the system via the external input-output units over the indicated special-word-transfer path to the Input-Output Buffer.

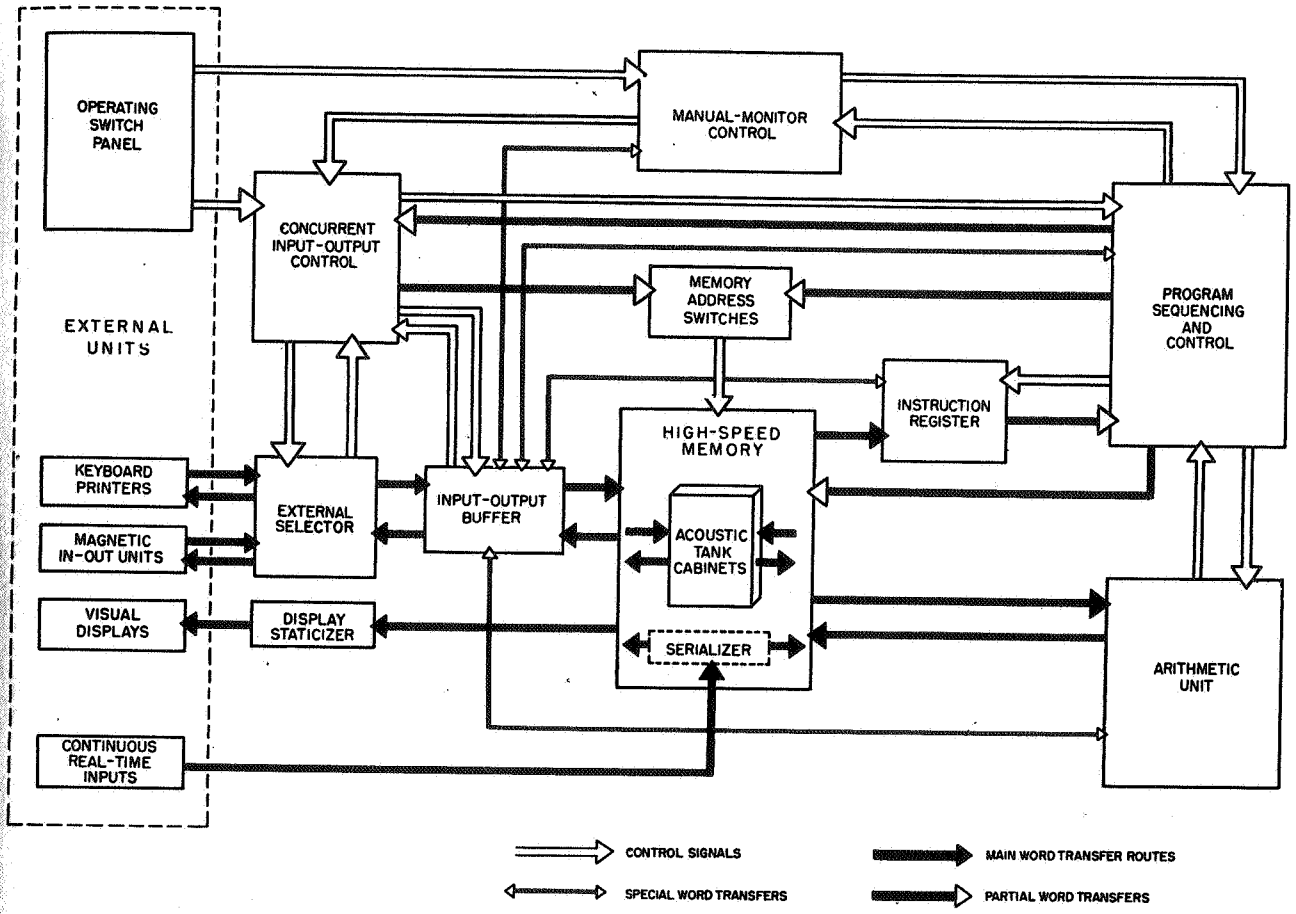

FIGURE 3.1. *Overall functional organization of the DYSEAC system.*

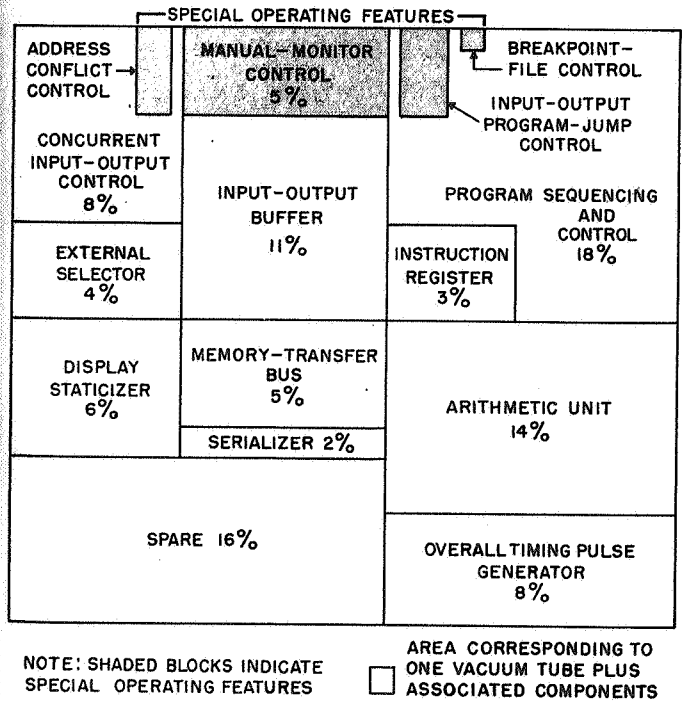

FIGURE 3.2. *Proportion of space required for DYSEAC special operating features.*

The last major unit to be noted is the Manual-Monitor Control. This unit is responsible for regulating and synchronizing the carrying out of joint internal-external operations. Its major functions are (1) to interpret the breakpoint conditions received from the external Operating Switch Panel, (2) to observe the progress of the internal program and recognize when the specified breakpoint conditions arise, and (3) to deliver signals temporarily halting the internal program, if necessary, setting up the required special-word-transfer routes, and initiating the specified interpolated internal or external operation.

The proportion of physical space required by the equipment for carrying out the joint internal-external control operations of DYSEAC is indicated graphically in figure 3.2. The areas marked off on this chart have been made directly proportional to the number of physical packages required for realizing the various functional units just described, exclusive of the memory. It can be seen that the equipment for performing Manual-Monitor operations, Breakpoint-File operations, and Input-Output address-conflict and program-jump operations (shaded areas on the chart) constitute only about 6 percent of this total. Also, about 16 percent of the total physical space available, labelled "spare" on the chart, has been left unused and can be utilized for annexation of other internal computing or control units if so desired.

4. OPERATING CAPABILITIES

As a result of its special features, the DYSEAC possesses three versatile operating properties which may be summarized as follows:

(1) The external devices harnessed to the machine can gain access at any time to all or to any part of the internal memory without disrupting the internal computing program. Moreover, practically continuous input-output access to certain special parts of the internal memory is available for the use of specialized external units needing faster-than-average access, e.g., units which provide continuous visual displays for the operator or which produce certain manual or automatic control signals for the computer.

(2) The DYSEAC can operate with a wide variety of input-output devices ranging from electromechanical typewriters through magnetic storage devices to analog-digital converters associated with different types of sensing devices and servomechanisms. Some of these devices deal with detailed digitalized data at magnetic recording rates. For these, the system contains facilities for accepting and transmitting data at a variety of repetition rates and word formats.

(3) Whenever necessary, the progress of the internal program can be regulated, scaled, and synchronized by events occurring beyond the supervision of the machine. Because of this ability of the machine to turn its attention to any of its wide family of subsidiary devices and to interrupt or redirect its over-all program in order to assist or manage them, DYSEAC can be used for investigating many diverse areas of potential application ranging from the simulation and control of links in a data-communication network to the high-speed processing of business data.

As an example of a potential application which requires such capabilities, consider an installation engaged in the automatic processing of business accounts and records. In an application of this sort the main task of the computer might be the routine processing of monthly accounts. The data to be processed would be withdrawn automatically by the machine from the external magnetically recorded files [3], would then be properly combined with newer data, and finally the up-to-date information would be returned to the files. Even while these operations are progressing automatically, however, the contents of the files would need to be available to the clerical staff of the office for inserting occasional corrections or revisions of data, or for answering scattered spot requests for information. Moreover, in some cases, the computing services of the machine would be needed for carrying out special minor processing tasks on the data being withdrawn from the files in this manner. At the same time, batteries of printers might be systematically going through the files and routinely printing out those portions for which the monthly processing was already complete. Similarly, the routine entry of new data, such as sales records, into the portions of the files not yet reached for processing might be going on.

Obviously, it would be highly desirable to be able to carry out any of these several operations at will, with as little disruption as possible either to each other or to the main task. Because of