X-ray computed tomography flaw phantom development: stepper photolithography and deep reactive ion etching

Fabrication and reference measurements

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Abstract

Stepper photolithography combined with deep reactive ion etching was used to generate controlled flaws to assess X-ray computed tomography (XCT) flaw detectability. Holes ranging in size from a few micrometers to hundreds of micrometers were generated. Various shapes and distribution patterns of holes were demonstrated. Capabilities to generate simple cylindrical holes to more complex cavities with scalloping surfaces representative of metal additive manufacturing lack-of-fusion pores were also demonstrated. A silicon direct bonding method was demonstrated to change the generated holes into pores. Scanning electron microscopic images were acquired to assess the manufacturing quality and to calibrate the flaw sizes. Reference measurement processes and results are discussed.

Keywords

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Acknowledgments

Author Contributions

Felix H. Kim: Conceptualization, Methodology, Investigation, Software, Formal Analysis, Writing- Original draft preparation, Visualization, Data Curation; **Sarah M. Robinson**: Investigation, Data curation, Writing – Review & Editing; **Nikolai N. Klimov**: Investigation, Data Curation; **John Henry J. Scott**: Conceptualization, Methodology, Resources

1. Introduction

X-ray computed tomography (XCT) is becoming a viable nondestructive testing (NDT) method for advanced manufacturing industries such as additive manufacturing (AM). Different types of flaws (e.g., pores and cracks) can form in manufactured parts, which can be examined from XCT images. XCT measurements generate three-dimensional (3D) grayscale images whose grayscale values are quantitatively related to material x-ray attenuation coefficients in the manufactured part, and these flaws (e.g., pores and cracks) often present lower intensities (i.e., low attenuation) in the images around high intensity (i.e., high attenuation) materials. In AM-produced parts, various types of flaws such as lack-of-fusion pores, gas pores, keyhole pores, and cracks can form [1].

The flaws in the parts can be detected by examining these images, either by a human examiner or by a machine agent using a defect recognition algorithm. Alternatively, human-machine teaming strategies may be employed where the algorithm assists human examiners who make the final flaw detection and classification decision. Regardless of the detection methods employed, assessing the detectability of these flaws is critical for qualifying the XCT examination process and for carrying out proper part acceptance tests. An artifact with representative flaws coupled with ground truth information about those flaws (e.g., size and location) provides direct and trustworthy support for assessing the detectability of such flaws in manufactured parts.

In this report, we present a manufacturing method using a commercial stepper lithography technique and deep reactive ion etching to generate controlled flaws. We demonstrate that the technique implemented in this study enables accurate representation of designed flaw shapes to be made, which demonstrates the possibility of designing complex flaw shapes and sizes. We expect this manufacturing method and the phantoms produced to be relevant to nano and micro XCT measurements. A chip bonding method is also demonstrated to cover manufactured holes and turn them into internal pores, which is essential for performance evaluation of automated detection algorithms. We also discuss different reference measurement methods to acquire ground truth information of the manufactured flaws.

2. Manufacturing process

In this study, we demonstrate a phantom manufacturing process using commercial stepper lithography and deep reactive ion etching (DRIE) instruments available in the NIST Center for Nanoscale Science and Technology (CNST) NanoFab. The lithography process was implemented on a Si wafer followed by a DRIE process. The wafer was diced to smaller chips, and the patterned chips were bonded to a blank chip to transform the created surface features into internal flaws. Major steps of the manufacturing process are described in this section. ASML PAS 5500/275D[1] was used for the lithography process, a Suss MicroTec ACS200 automated resist coater was used for the photoresist application process, and a Suss MicroTec delta12AQ automated resist developer was used for the development process after the photolithography step. An SPTS Omega c2L Rapier deep silicon etcher was used for the DRIE process. The various

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[1] Certain commercial equipment, instruments, or materials are identified in this paper in order to specify the experimental procedure adequately. Such identification is not intended to imply recommendation or endorsement by the National Institute of Standards and Technology, nor is it intended to imply that the materials or equipment identified are necessarily the best available for the purpose.

manufacturing processes used are illustrated schematically in Figure 1, with detailed steps discussed below.
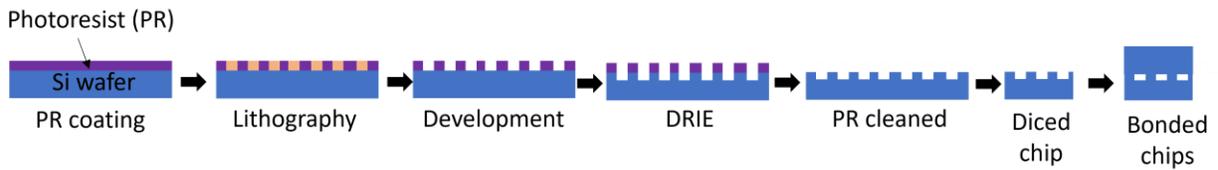
Figure 1: An overview of XCT flaw phantom manufacturing process.

2.1. Pattern design and photomask development

A photomask is a chrome-on-glass plate with patterns of interest printed on it. A dark field photomask was fabricated, which means the created features (e.g., circles for holes) are transparent to light. The photomask was made five times larger than the desired size to be used in the ASML PAS 5500/275D system. The photomask was designed using CNST Nanolithography Toolbox [2] and fabricated using an external vendor using an Alta 3100 system. The physical size of the photomask is 152.4 mm × 152.4 mm × 6.35 mm, but the maximum field size of the stepper is 110 mm × 110 mm on the photomask, which is equivalent to 22 mm × 22 mm on a wafer. Other parts of the photomask include a barcode for identification and alignment markers. Figure 2 shows the photomask design, and Table 1 shows the list of individual patterns. The photomask has 16 different patterns, which were designed to be used separately or combined during the exposure step.

In this study, five different designs were produced on each chip, shown in Figure 3 and Table 2. The designs were repeated in a 2 × 2 pattern to fit in a chip designed to be 9.85 mm × 9.85 mm in size, creating 45 chips on a 100 mm dia. wafer. In Figure 3a, photomask designs 1 through 7 were combined on a single chip to distribute circular holes quasi-randomly in a Sobol sequence, designated as flaw distribution design A in Table 2. The circular hole diameters were 400 µm, 282.8 µm, 200 µm, 141.4 µm, 100 µm, 70.7 µm, 50 µm, 35.4 µm, 25 µm, 17.7 µm, 12.5 µm, 8.8 µm, 6.25 µm, and 4.4 µm. The diameter was reduced by a ratio of $\sqrt{2}$ in each step, which decreased the hole area by a factor of 2. There are four holes of the same size in each pattern. An Optunity package was used in a Python environment to generate the Sobol sequence [3], with the initial 2000 points skipped in the Sobol sequence. In the current batch, photomask design 6 (8.8 µm and 12.5 µm diameter holes) were not included in Q1 (top right) and Q2 (top left) of the chip while photomask design 7 (4.4 µm and 6.25 µm dia. holes) was not included in Q3 (bottom left) and Q4 (bottom right) of the lithography design file. The missing features will be included in a future batch. In Figure 3b, photomask design 8 was used, which has the same size and number of circular holes distributed in a regular rectilinear pattern. We designated this as flaw distribution design B in Table 2. The distance between each pair of holes was designed to be greater than three times the diameter of the smaller hole, measured edge-to-edge. In Figure 3c, photomask design 9 was used, which has rectangular holes with 200 µm width and varying height (400 µm to 4.4 µm) distributed in the same Sobol sequence as in Figure 3a. We designated this as flaw distribution design C in Table 2. In Figure 3d, photomask design 13 was used, in which half circles (40 µm diameter) were overlaid on and subtracted from the perimeters of the same rectangular holes as in Figure 3c. The process is further illustrated in Figure 4. This was designed to represent the rough surface features typically found in AM lack-of-fusion

defects. We called this flaw distribution design D in Table 2. In Figure 2e, photomask design #10 was used, in which the distance between two circular holes were varied. We called this flaw distribution design E in Table 2. The center-to-center distance varied from 0.5× hole dia., 1× hole dia., 1.5× hole dia., 2× hole dia., 2.5× hole dia., and 3× hole dia. The hole diameters were 4.4 µm, 8.8 µm, 17.7 µm, 35.4 µm, 70.7 µm, and 141.4 µm. In addition, a circular hole of varying sizes (50 µm, 35.4 µm, 25 µm, 17.7 µm, 12.5 µm, 8.8 µm, and 6.25 µm diameter) was surrounded by six, larger, equally-sized circular holes (200 µm dia.).
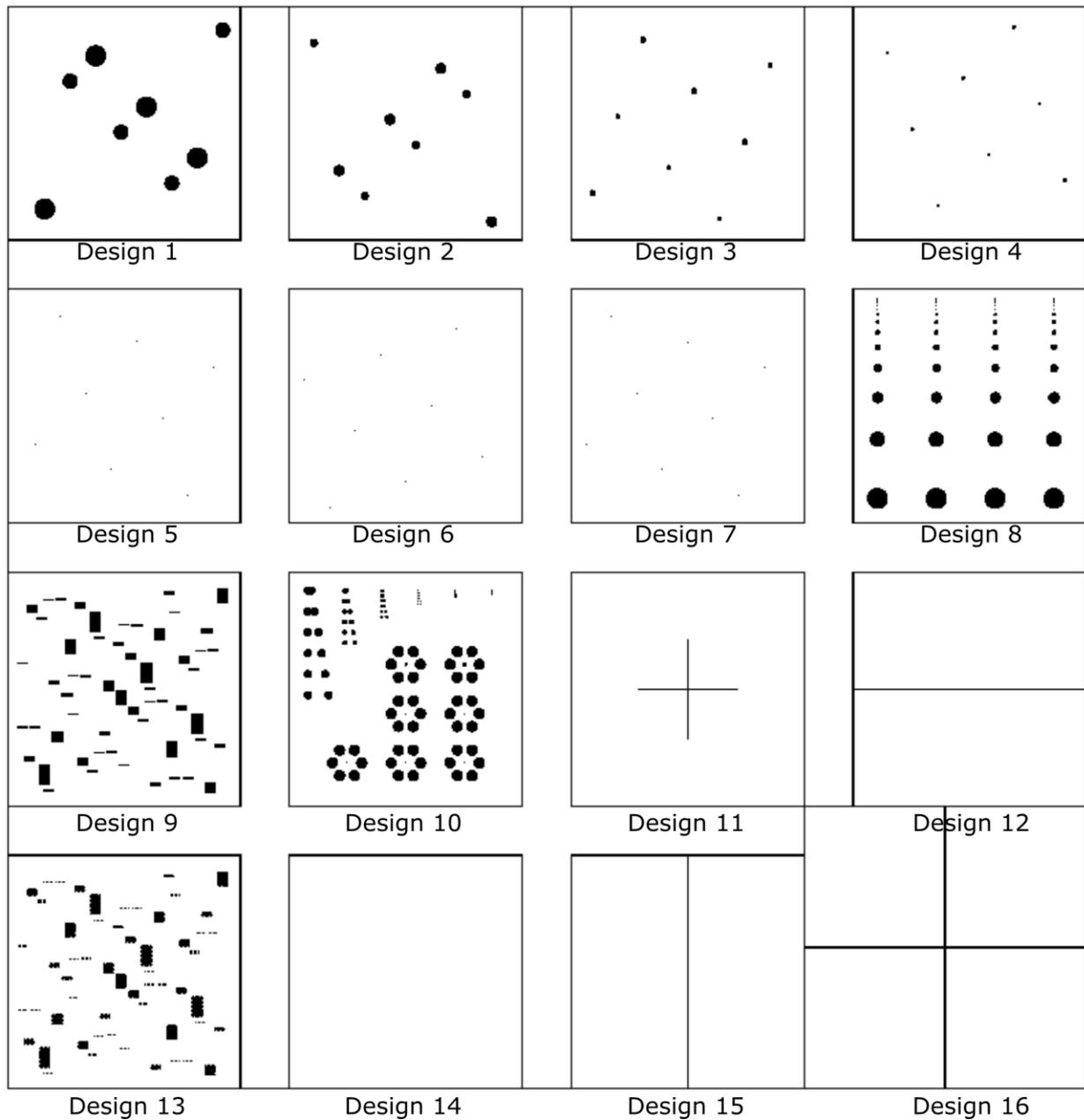
Figure 2: Photomask design used in this study. Labels are added below each design for the purpose of illustration only.

Table 1: Descriptions of photomask designs. The dimensions of the features are what would be transferred on to wafers.

Photomask design	Description
1	Circles with diameters of 400 µm and 282.8 µm distributed following a Sobol sequence
2	Circles with diameters of 200 µm and 141.4 µm distributed following a Sobol sequence
3	Circles with diameters of 100 µm and 70.7 µm distributed following a Sobol sequence
4	Circles with diameters of 50 µm and 35.4 µm distributed following a Sobol sequence
5	Circles with diameters of 25 µm and 17.7 µm distributed following a Sobol sequence
6	Circles with diameters of 12.5 µm and 8.8 µm distributed following a Sobol sequence
7	Circles with diameters of 6.25 µm and 4.4 µm distributed following a Sobol sequence
8	Circles with diameters from 4.4 µm to 400 µm distributed in a regular rectilinear pattern
9	Rectangles with widths of 200 µm and heights varying from 4.4 µm to 400 µm distributed following a Sobol sequence
10	Circle pairs with varying proximity and circles surrounded by larger circles
11	Cross at the center
12	Horizontal line
13	Rectangles identical to design 9 with scalloped sides with half circles with diameters of 40 µm
14	Blank
15	Vertical line
16	Vertical and horizontal lines
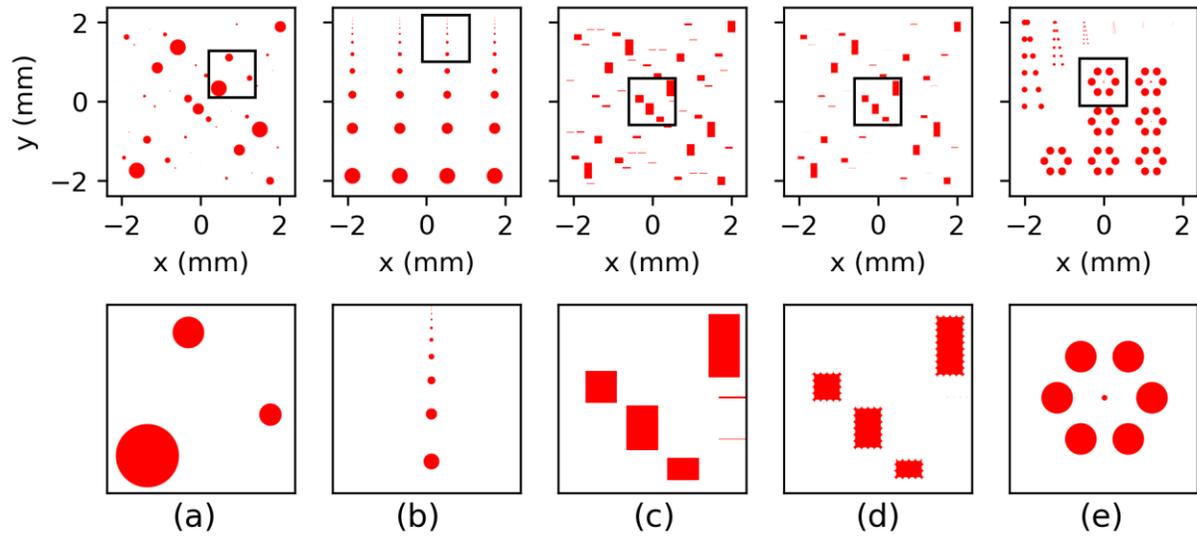
Figure 3: Five flaw distribution designs developed in this study: (a) flaw distribution design A, (b) flaw distribution design B, (c) flaw distribution design C, (d) flaw distribution design D, and (e) flaw distribution design E as described in Table 2. The top row shows the entire design, and the bottom row shows design of the portion within the insets shown in the top row.
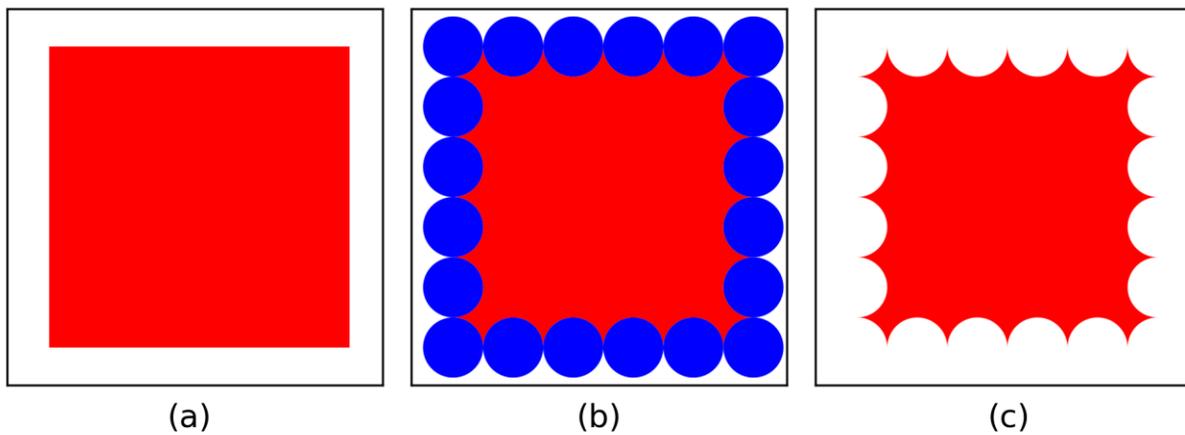
Figure 4: Illustration of scalloped side wall generation process of Figure 2d, (a) a rectangle, (b) circles overlaid at the perimeter of the rectangle, and (c) resulting scalloped surfaces after subtraction process.

Table 2: Description of chip designs

Flaw distribution design	Description
A	A combination of photomask designs 1 through 7
B	Photomask design 8
C	Photomask design 9
D	Photomask design 13
E	Photomask design 10

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2.2. Photoresist coating

Double side-polished (DSP) wafers (400 µm ± 10 µm thickness, n-doped with phosphorus, face in the <100> crystal direction, resistivity 1 Ω·cm to 20 Ω·cm) were used. DSP wafers were selected so that the patterned die could be bonded in multi-die stacks in future prototypes. Current CNST NanoFab instruments are primarily configured for handling 100 mm dia. wafers, which were used for this study. Bottom anti-reflective coating (BARC) was used to have better control of critical dimensions by reducing the swing effect and standing waves in photoresist [4]. A Suss MicroTec ACS200 automated resist coater was then used to apply photoresist (MEGAPOSIT® SPR® 220-3) at a thickness of approximately 3 µm. A softbake (115 ℃ for 90 s) was applied to the wafer with photoresist.

2.3. Stepper photolithography

Lithography is a technique of transferring a pattern onto a solid material such as a silicon wafer. There are many variations of this technique. We used a commercial stepper lithography system-based approach. The process is typically implemented for semiconductor manufacturing. The lithography system uses a light source and a reusable photomask to transfer patterns of the photomask onto the photoresist coated on wafer surface. Unlike a mask aligner where the features on the photomask are transferred to the wafer in the same scale at once, a stepper uses optics to shrink the features in the photomask when transferring them to the wafer (5× in this case), which allows further improvements in the resolution. A small portion of the photomask is scanned on parts of the wafer, and the process can be repeated for different designs on the photomask or for different locations in the wafer. The ASML PAS5500/275D system uses 365 nm wavelength light (i-line). One wafer for each design group was exposed, and each wafer produced 45 chips. In each chip, the design was repeated in a 2×2 pattern. A post-exposure bake was implemented after the lithography process (110 ℃ for 90 s).
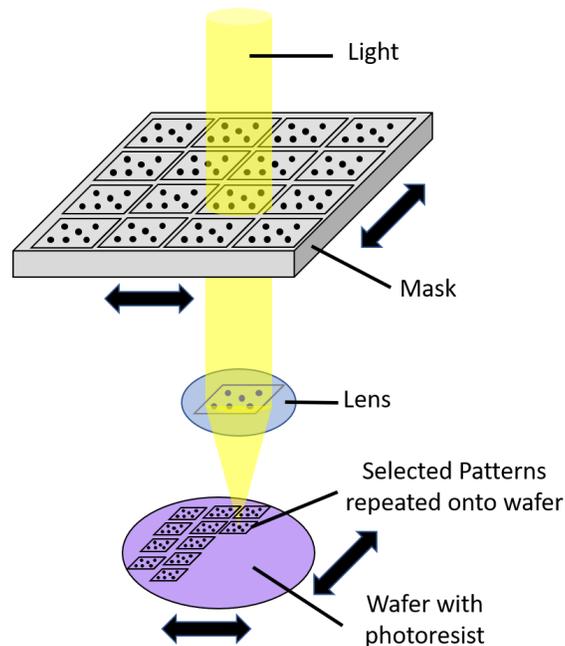
Figure 5: Illustration of stepper lithography process.

2.4.   Photoresist development

The exposed photoresist was developed using the Suss MicroTec Delta12AQ Automated Resist Developer with AZ® MIF300 for 80 s. The exposed areas during the lithography step were polymerized and washed away during the development step. A standard RIE process with oxygen plasma was carried out to dry etch the BARC layer in the exposed areas. The wafers were then baked overnight in a vacuum oven at 90 ℃ followed by ultraviolet light exposure within N_2 environment at 90 ℃ for 10 min to cross-link a thin layer of resist for improved etch resistance [5].

2.5.   Deep reactive ion etching

DRIE is also called the 'Bosch process' as it was originally developed at Robert Bosch GmbH. It is a combination of physical and chemical etching processes. A typical DRIE loop is illustrated in Figure 6 (adapted from[6]). In step 1, CF_x molecules generated from a C_4F_8 plasma deposits a fluoropolymer passivation layer onto the mask and into the etched feature. In step 2, an electrical bias from the platen below causes directional ion milling resulting in removal of the fluoropolymer passivation layer from the base of the feature as well as the photomask. In step 3, fluorine radicals from SF_6 plasma isotropically etch the exposed Si at the base of the feature. The etch rate of the photoresist due to these radicals was slower than the etch rate of Si. The process repeats to generate anisotropic holes (i.e., deep holes). An SPTS Omega c2L Rapier Deep Silicon Etcher was used. In this study, 120 DRIE loops were implemented. As will be shown later, different hole diameters are expected to have different hole depths.
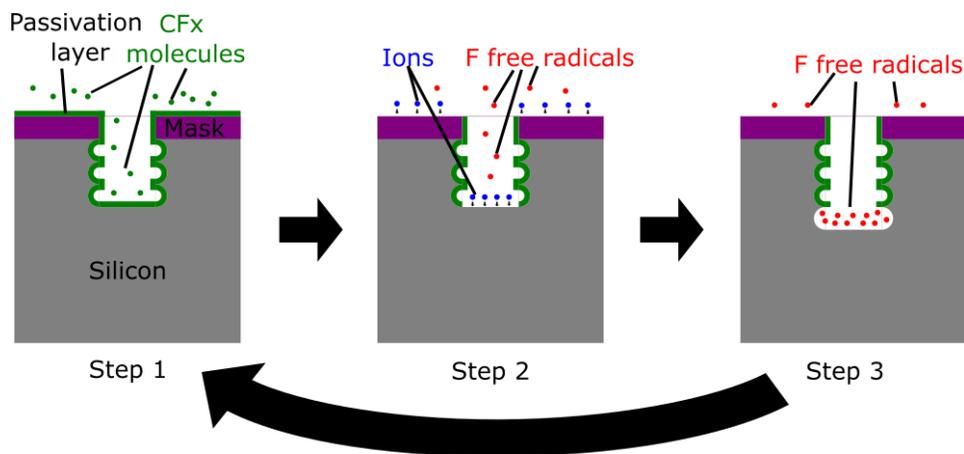
Figure 6: Illustration of DRIE process.

2.6.   Direct (fusion) bonding

After the DRIE process, the wafers were diced to generate multiple chips in sizes of approximately 9.85 mm × 9.85 mm. The DRIE process generated surface features, which need to be covered with solid material to make internal pores. A direct or fusion bonding approach was implemented on the chips. High temperature direct bonding has been demonstrated previously by annealing at temperatures above 1000 ℃ [7, 8]. In this present study, a low temperature direct bonding method was implemented by annealing at around 400 ℃ [9, 10]. A patterned chip and a blank chip were bonded. Both chips were initially cleaned with solvent to remove residual

photoresist applied during the dicing process to protect from Si particles. The chip surfaces to be bonded were then cleaned with Piranha solution (volumetric mixture of three parts H_2SO_4 and one part 30 % (mass fraction) H_2O_2 in H_2O) followed by RCA1 (mixture of five parts H_2O, one part 27 % NH_4OH, and one part 30 % H_2O_2) to achieve hydrophilic surfaces. SSEC brand Single Wafer Cleaning Systems were used for the Piranha and RCA cleaning processes and all recipes included rinsing with water and drying with nitrogen. Prior to bonding, the chip surfaces were activated with oxygen plasma. A commercial RIE tool was initially used, and then an Ontos atmospheric plasma system was used with localized oxygen plasma later when it became available to NanoFab users. The chips were aligned using a custom alignment tool and clamped down for initial bonding as shown in Figure 7a. Polymer chip alignment tools with magnets were also developed to help align corners of the chips when stacking. The bond at this point is reversable. The bonded chip stack was carefully transferred to a rapid thermal annealing system (AnnealSys AS-Master). The chip stacks were annealed at 400 °C in N_2 environment for 1 hr. About five set of phantoms for each design were produced.

(a)   (b)
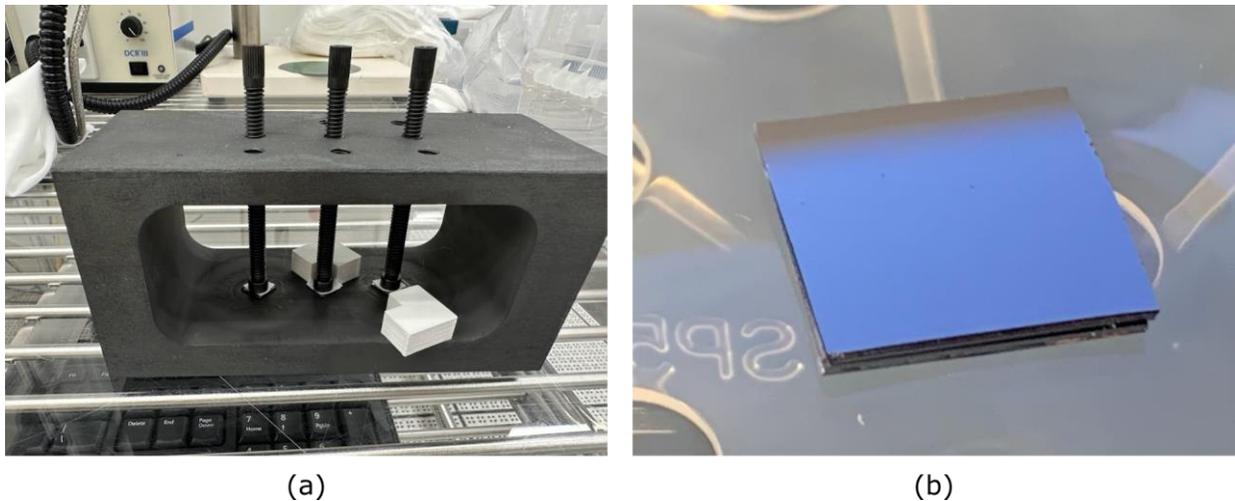
Figure 7: (a) A picture of the chip assembly jig and (b) a bonded chip stack after annealing.

3.   Reference measurements

In this study, the measurand of interest was the pore volumes since they are typically measured in XCT image analysis. We investigated scanning electron microscopy (SEM) – based characterization methods in this study. SEM provides nanometer resolution, which is orders of magnitude higher than typical industrial XCT spatial resolution of a few micrometers and coarser. We measured the cross-sectional areas and hole depths, which were used to estimate the hole volumes. This estimate uses the assumption that the holes have relatively vertical smooth side walls and flat bottom surfaces. We demonstrated the measurement process on the flaw distribution pattern B with cylindrical holes aligned in arrays (Figure 3b). Another assumption is that the manufacturing process is repeatable at least for the same features manufactured on the same wafer, and the level of repeatability will be discussed from reference measurement results. Other potential reference measurements methods may be integrating height maps of optical interferometric microscopy and acquiring focused ion beam (FIB) tomography.

3.1. Cross sectional area measurements

The cross-sectional areas were measured by mounting a sample flat on an SEM sample holder with 0º stage tilt. SEM images of different features are shown in Figure 8. For the holes with simple geometries such as circles or rectangles, diameters of the circles or widths/heights of the rectangles were measured from the SEM images. The cross-sectional areas were estimated based on the measured values. For more complex features such as the flaw distribution pattern D (Figure 4c), image thresholding/segmentation can be used to estimate the cross-sectional areas. Since the positions of the features were known, it was relatively easy to locate the features for SEM measurements. In Figure 9, nominally identical features were measured three times, and the average values and standard deviations are reported for circular holes of flaw distribution pattern B. A ThermoFisher FEI Helios NanoLab 660 FIB/SEM system was used for the measurements. Ellipses were manually fitted in ImageJ, and the major and minor diameters of the ellipses were found. The major and minor diameters were identical in most cases. The measured diameters were very close to but slightly larger than the designed diameters.
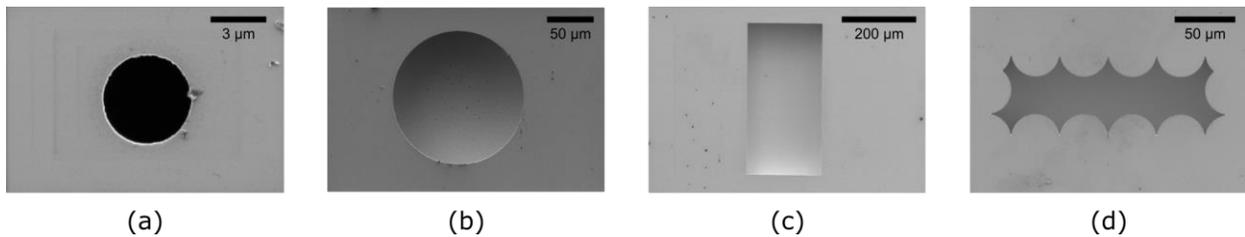
Figure 8: Example SEM images of (a) 4.4 µm dia. circular hole, (b) 141 µm dia. circular hole, (c) 200 µm × 400 µm rectangular hole, and (d) holes with scalloped surfaces created from a 200 µm × 70.7 µm rectangle.
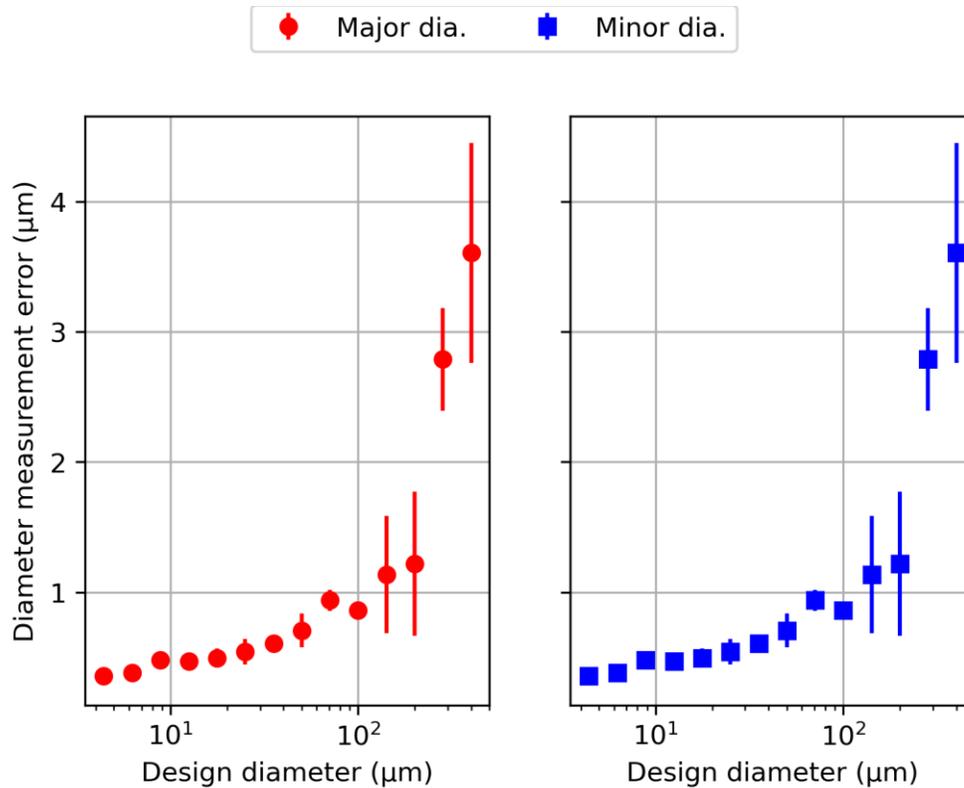
Figure 9: Measured hole major (left) and minor (right) diameters of circular holes of flaw design B compared to design diameters. Error bars are ± 1 standard deviation of 3 measurements.

3.2. Depth measurements

The DRIE process creates holes with relatively straight side walls. The walls have nanometer-level scalloping due to multiple DRIE loops as schematically shown in Figure 6. The size of scalloping is significantly smaller compared to a typical XCT resolution of a few micrometers and the associated error is expected to be negligible. There is also slight tapering on the side walls, which is also considered negligible for the current hole depths. The bottom surfaces of the holes are also not perfectly flat due to the isotropic etching process for each DRIE loop. Since the DRIE process is based on the interaction between gas and substrate, the diffusion rate into higher aspect ratio structures is slower. This limits the level of etching capability, and smaller holes generally have lower depths compared to larger holes. This requires individual characterization of different hole sizes. The etching depths are expected to be consistent for nominally same sized holes on the other hand.

SEM instruments are usually equipped with a tilt stage, and the hole depths can be measured by tilting the stage to reveal the side surfaces. An example SEM image is shown in Figure 10 where an approximately 17.7 µm diameter hole was tilted at 10°. Different tilt angles may be needed for different size of features, and it may not be possible to fully capture the depth depending on the size of the hole. Since the bottom surface of the DRIE-etched holes are rounded, only the shallowest depths near the side walls are measured. The measurement needs to be corrected

based on the tilt angle. Even after tilt correction, we found that the measurement results can potentially vary depending on the tilt angle, magnification, and hole depth.

HV	curr	HFW	dwell	det	mode	tilt	WD	mag ⊞	├── 5 µm ──┤
2.00 kV	0.10 nA	29.9 µm	10 µs	ETD	SE	10 °	3.8 mm	4 997 x	CNST NanoFab Helios FIB 2
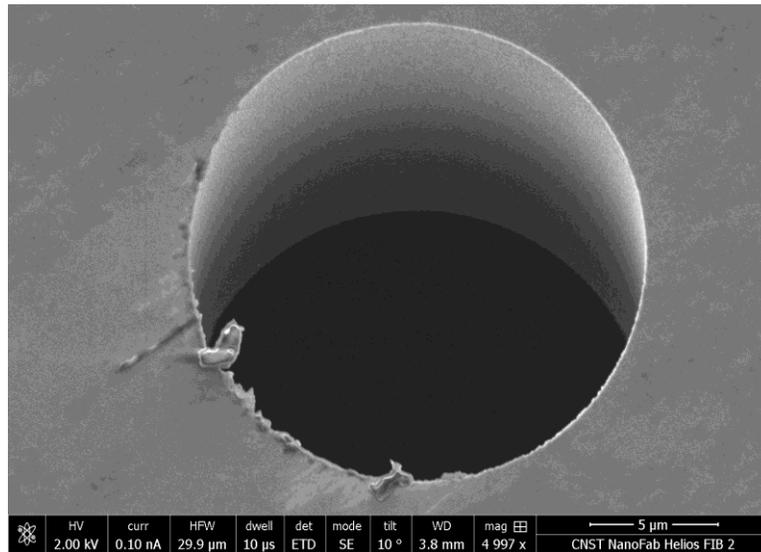
Figure 10: Example stage tilt-based SEM measurements.

Instead of the tilt stage-based measurements, mechanical polishing was implemented to reveal vertical cross sections of the holes in this study. A precision mechanical polishing system equipped with micrometers and a digital dial indicator (Allied multiprep 8 in) was used to carefully polish through the centers of the holes. Lapping films with 30 µm to 0.25 µm abrasive particles were sequentially used to polish down to the target. The polishing progress was periodically checked on an optical microscope throughout the process. Micrometers enabled the angle of polishing to be adjusted during the process. A single cross section (A-A) shown in Figure 11a can reveal depths of all holes for design B when mechanically polished through the centers of the holes. Since the flaw distribution design was repeated in a 2×2 pattern in a single chip, two features of the same size holes were shown in a single cross-sectional image. By comparing the amounts of materials left to polish after each polishing step for two identical features separated by 4.925 mm, the angle of polishing was adjusted. Following the polisher manufacturer's suggestion, a glass cover plate was mounted to the front side of the Si chip with two-part epoxy adhesive and cured in high temperature. During the process, the epoxy filled some holes. Six sets of holes were polished and measured in a Zeiss Gemini 500 FESEM. The depths were measured at two positions: 1) at the end of where DRIE scalloping ends (depth 1) and 2) at the rounded hole bottom (depth 2). An example SEM image of the three smallest holes is shown in Figure 11b. It is clear that the larger diameter holes were etched deeper. Figure 12 shows a plot of hole depth measurements acquired from six different holes for all 14 hole sizes.
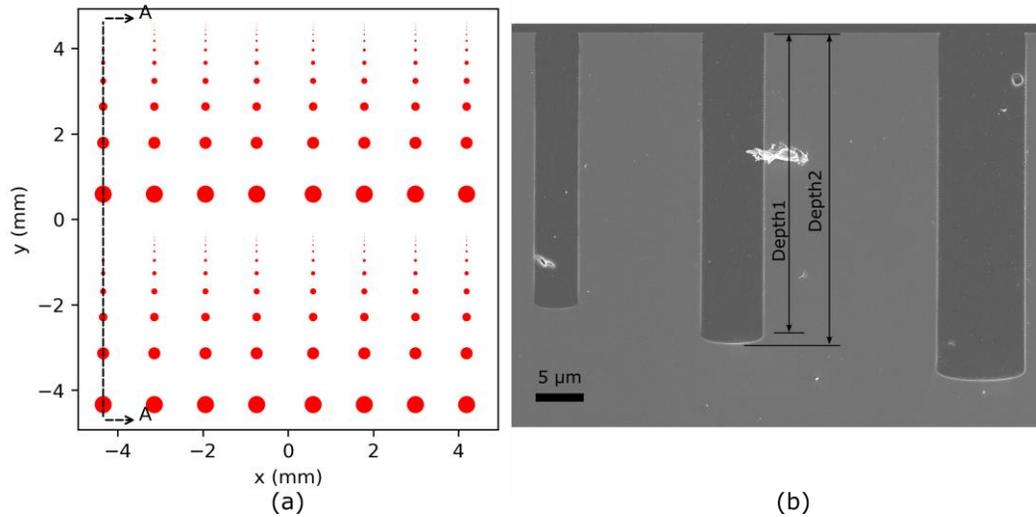
Figure 11: (a) Example illustration of cross sectioned location (e.g., A-A), and (b) SEM cross sectional profile showing 4.4 µm dia. hole (left), 6.25 µm dia. hole (middle), and 8.8 µm dia. hole (right)
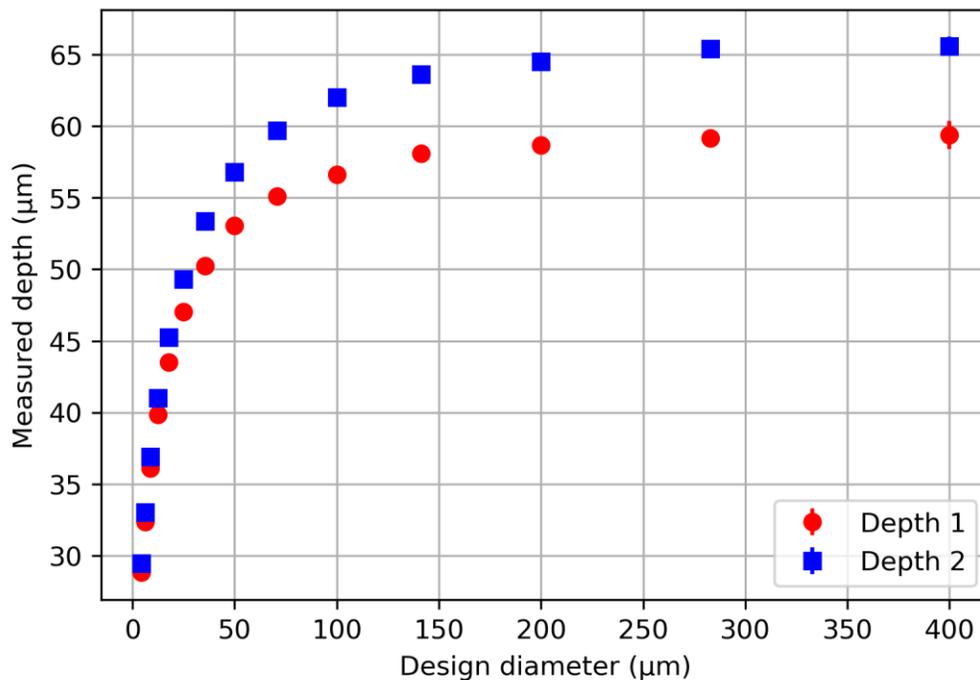
Figure 12: Hole depth measurement results. The error bars are ± 1 standard deviation of 6 measurements.

3.3.   Volume estimation

Hole volumes were estimated based on the cross-sectional areas and depth measurements. As shown from SEM images earlier, the bottom surfaces of the holes are not flat but rounded. Therefore, the hole volume was estimated as a summation of cylinder volume estimated from the depth 1 measurement and a half of the ellipsoid volume as shown in Figure 13. The rounded

bottom surface region was estimated based on the half ellipsoid volume where the three radii were major and minor radii measured from Section 3.1 and the difference of depth 2 and depth 1 measured from Section 3.2. The hole volumes are plotted in Figure 14, and the entire measurement results are shown in Table 3. Average hole volumes were estimated from three independent hole area measurements and six independent hole depths measurements, from which the standard deviation of the hole volumes was also estimated.
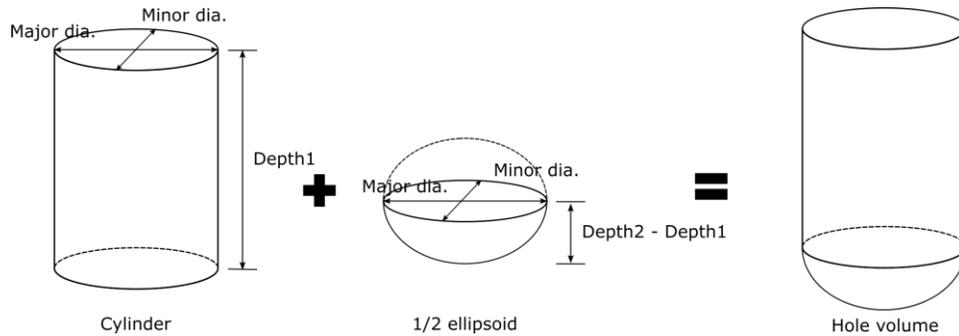
Figure 13: Illustration of hole volume estimation using volumes of a cylinder and a half of an ellipsoid.
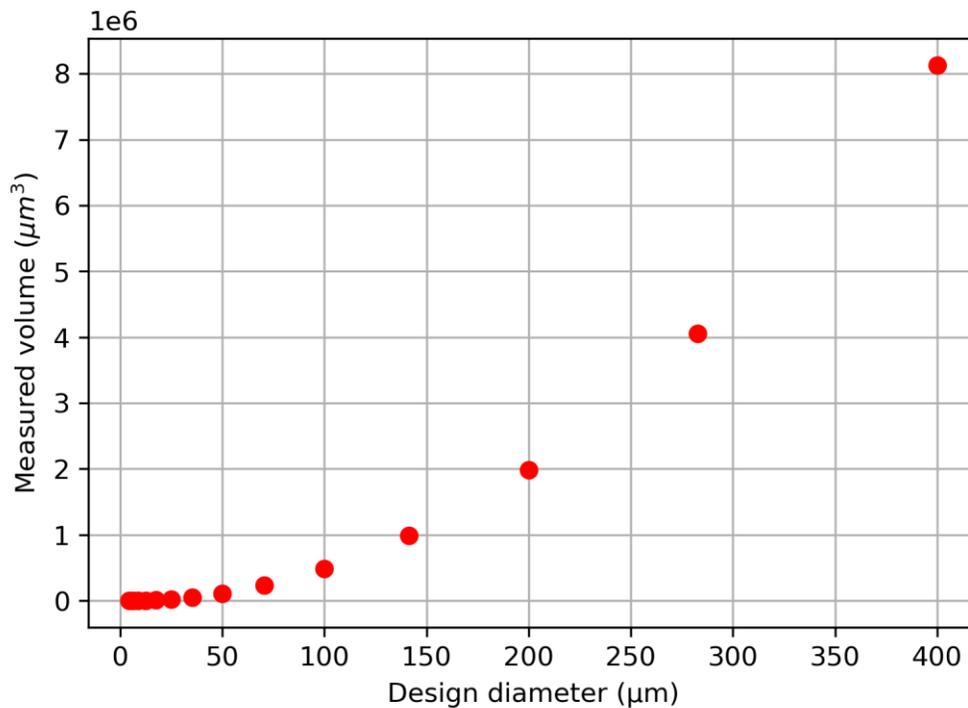
Figure 14: Hole volume measurement plot.

Table 3: Table of measurement results.

Design diameter (µm)	Measured major diameter (µm)	Measured minor diameter (µm)	Measured area (µm²)	Measured depth 1 (µm)	Measured depth 2 (µm)	Measured volume (µm³)
4.40	4.76 ± 0.02	4.76 ± 0.02	17.77 ± 0.10	28.85 ± 0.06	29.45 ± 0.09	519.61 ± 3.10
6.25	6.63 ± 0.02	6.63 ± 0.02	34.53 ± 0.18	32.35 ± 0.18	33.05 ± 0.12	1133.33 ± 8.87
8.80	9.28 ± 0.02	9.28 ± 0.02	67.65 ± 0.19	36.09 ± 0.15	36.93 ± 0.14	2479.21 ± 13.62
12.50	12.97 ± 0.03	12.97 ± 0.03	132.15 ± 0.38	39.85 ± 0.15	40.99 ± 0.09	5367.15 ± 26.44
17.70	18.19 ± 0.08	18.19 ± 0.08	259.99 ± 1.52	43.53 ± 0.34	45.23 ± 0.26	11611.45 ± 117.00
25.00	25.54 ± 0.10	25.54 ± 0.10	512.40 ± 2.76	47.01 ± 0.09	49.31 ± 0.08	24875.71 ± 144.45
35.40	36.01 ± 0.02	36.01 ± 0.02	1018.23 ± 0.95	50.25 ± 0.19	53.35 ± 0.26	53271.18 ± 209.79
50.00	50.71 ± 0.13	50.71 ± 0.13	2019.39 ± 7.35	53.05 ± 0.32	56.81 ± 0.11	112192.77 ± 833.46
70.70	71.64 ± 0.08	71.64 ± 0.08	4030.70 ± 6.41	55.11 ± 0.38	59.67 ± 0.10	234401.07 ± 1821.08
100.00	100.86 ± 0.07	100.86 ± 0.07	7989.65 ± 7.96	56.61 ± 0.17	62.00 ± 0.17	481030.25 ± 1563.82
141.40	142.53 ± 0.45	142.53 ± 0.45	15956.03 ± 71.39	58.07 ± 0.37	63.61 ± 0.14	985462.03 ± 8175.92
200.00	201.22 ± 0.55	201.22 ± 0.55	31799.95 ± 123.71	58.69 ± 0.53	64.49 ± 0.43	1989192.77 ± 23967.59
282.80	285.59 ± 0.39	285.59 ± 0.39	64057.47 ± 124.66	59.15 ± 0.33	65.41 ± 0.54	4056403.79 ± 39060.69
400.00	403.61 ± 0.84	403.61 ± 0.84	127939.21 ± 377.88	59.37 ± 0.99	65.58 ± 0.66	8125490.48 ± 154815.03

3.4.   Discussion

The holes designed to be circular appeared to be highly circular by comparing the major and minor diameter measurements, with the standard deviations of the diameter measurements less than 0.5 % of the mean diameters. Consistent hole depths with low variability were measured; the depth standard deviations were less than 1.7 % of the mean depths for both depth 1 and depth 2 measurements. Here are some sources of variability for the depth measurements:

- Slight variations regarding the vertical cross-section locations are expected. While the mechanical polishing process was targeted to end at the centers of the holes based on optical microscopy measurements made during the polishing process, the measured cross sections may slightly deviate from the true centers of the holes as well as between each other.
- Different SEM magnifications were used to measure holes of different sizes. Lower magnification was used to measure larger holes, which makes the pixel pitch coarser than that of a higher magnification measurement. Therefore, the measurement precision of lower magnification measurement is inherently lower than that of a higher magnification measurement.

- Hole depths were measured manually in the SEM instrument software by using a software measurement tool. Minor human errors of selecting the correct edges are expected.

Despite these potential error sources, repeatable hole volume measurements were achieved where all hole volume standard deviations were within 2 % of the means. SEM calibration error is typically around 1 % and within 3 % based on calibration standard measurements made by the manufacturer. The calibration error can be considered in the uncertainty analysis, and the error can be further reduced by calibrating SEM measurements at each use.

4.   Conclusions and future work

A stepper photolithography and DRIE-based XCT defect artifact development process and reference measurement process were documented in this report. The manufacturing technique showed superior accuracy and reproducibility at the micrometer length scale implemented in this study. The manufacturing process can easily scale up for mass production of reference materials by implementing the automated processes on additional wafers. A precision mechanical polishing technique was found to be a reliable technique to reveal the vertical cross section of the holes for depth measurements. The holes characterized in this study had diameters ranging from 4.4 µm to 400 µm and depths ranging from about 30 µm to 65 µm. SEM-based characterization processes were implemented to measure the ground truth geometric information of the pores. Based on the measurement results, hole volumes were estimated with low variability. The direct bonding process changed the etched holes to internal pores by bonding a chip with holes to a blank chip without adhesives. The fully encapsulated and well-characterized engineered defects will enable quantitative assessment of automated XCT detection algorithms. The artifacts will be measured with XCT using different acquisition settings, and different detection algorithms will be applied to the images. The detection results will be compared with reference measurement values for probability of detection and pore sizing analysis [e.g., 11, 12, 13]. Additional investigation of bonding approaches such as a wafer bonding process and an improved oxide-based bonding process will be further investigated. The mechanical polishing-based hole size characterization process used in this paper can be time-consuming and might need to be modified to accurately characterize smaller holes. Other characterization methods, such as optical interferometry and a FIB-based approach, will be investigated.

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