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Ascon-Based Lightweight Cryptography Standards for Constrained Devices

Authenticated Encryption, Hash, and Extendable Output Functions

Initial Public Draft

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- 83 including related content, potential updates, and document history.

84 **All comments are subject to release under the Freedom of Information Act (FOIA).**

85 **Abstract**

86 87 88 89 90 91 92 93 94 95 96 97 98 99 In 2023, the National Institute of Standards and Technology (NIST) announced the selection of the Ascon family of algorithms designed by Dobraunig, Eichlseder, Mendel, and Schläffer to provide efficient cryptography solutions for resource-constrained devices. This decision emerged from a rigorous, multi-round lightweight cryptography standardization process. This standard introduces a new Ascon-based family of symmetric-key cryptographic primitives designed to deliver Authenticated Encryption with Associated Data (AEAD), hash, and Extendable Output Function (XOF) capabilities, namely Ascon-AEAD128, Ascon-Hash256, Ascon-XOF128, and Ascon-CXOF128. The Ascon family is characterized by lightweight permutation-based primitives and provides robust security, efficiency, and flexibility, making it ideal for resource-constrained environments, such as Internet of Things (IoT) devices, embedded systems, and low-power sensors. The family is developed to offer a viable alternative when the Advanced Encryption Standard (AES) may not perform optimally. This draft standard outlines the technical specifications of Ascon-AEAD128, Ascon-Hash256, Ascon-XOF128, and Ascon-CXOF128, and provides their security properties.

100 **Keywords**

101 Ascon; authenticated encryption; constrained devices; eXtendable Output Function (XOF);

102 hash function; lightweight cryptography; permutation-based cryptography; standardization.

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201 **Acknowledgments**

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209 **1. Introduction**

210 211 212 213 This draft standard specifies the Ascon family of algorithms to provide Authenticated Encryption with Associated Data (AEAD), a hash function, and two eXtendable Output Functions (XOFs). The Ascon family is designed to be efficient in constrained environments. The algorithms specified in this standard are as follows:

- 214 215 1. Ascon-AEAD128 is a nonce-based authenticated encryption with associated data that provides 128-bit security strength in the single-key setting.
- 216 217 2. Ascon-Hash256 is a cryptographic hash function that produces a 256-bit hash of the input messages, offering a security strength of 128 bits.
- 218 219 3. Ascon-XOF128 is an XOF, where the output size of the hash of the message can be selected by the user, and the supported security strength is up to 128 bits.

220 221 222 4. Ascon-CXOF128 is a customized XOF that allows users to specify a customization string and choose the output size of the message hash. It supports a security strength of up to 128 bits.

223 224 225 226 227 228 229 230 231 *Development of the Ascon family.* Ascon (version v1) [\[1\]](#page-39-1) was first submitted to the CAESAR (*Competition for Authenticated Encryption: Security, Applicability, and Robustness*) [1](#page-11-1) in 2014. The submission included two AEAD algorithms: a primary recommendation, Ascon-128, with a 128-bit key and the secondary recommendation, Ascon-96, with a 96-bit key. Updated versions v1.1 $[2]$ for Round 2 and v1.2 $[3]$ for Round 3 included minor tweaks, such as reordering the round constants, and the secondary recommendation was updated to Ascon-128a. In 2019, Ascon-128 and Ascon-128a were selected as the first choice for the lightweight authenticated encryption use case in the final portfolio of the CAESAR competition.

232 233 234 235 236 237 238 239 *NIST Lightweight Cryptography Standardization Process.* In 2015, the National Institute of Standards and Technology (NIST) initiated the lightweight cryptography standardization process to develop cryptographic standards suitable for constrained environments in which conventional cryptographic standards (e.g., AES-GCM $[4, 5]$ $[4, 5]$ $[4, 5]$ and the SHA-2 $[6]$ and the SHA-3 [\[7\]](#page-39-7) hash function families) may be resource-intensive. In February 2023, NIST announced the decision to standardize the Ascon family $[8]$ for lightweight cryptography applications. (For more information, refer to NIST Internal Report (IR) 8268 [\[9\]](#page-39-9), NIST IR 8369 [\[10\]](#page-39-10), and NIST IR 8454 [\[11\]](#page-40-0)).

240 241 *Differences from the Ascon submission v1.2.* The technical differences between this draft standard and the Ascon submission $[8]$ are provided below:

¹CAESAR is a competition organized by a group of international cryptologic researchers to identify a portfolio of authenticated encryption schemes that offer advantages over AES-GCM and are suitable for widespread adoption. The final portfolio of the competition was announced in February 2019. For more information, see [https://competitions.cr.yp.to/caesar.html.](https://competitions.cr.yp.to/caesar.html)

277 the XOF function Ascon-XOF128, and the customized Ascon-CXOF128 and describes their ₂₇₈ security properties. [Appendix](#page-41-0) A provides additional notes and conversion functions for

₂₇₉ implementations. [Appendix](#page-46-0) B provides additional information regarding the construction

280 of initial values.

281 **2. Preliminaries**

 282 Table [1](#page-14-1) lists the acronyms used in this standard.

Table 1. Acronyms

[2](#page-14-2)83 Table 2 defines the terms used in this standard.

Table 2. Terms and definitions

Table 2. Terms and definitions

284 Table [3](#page-16-0) lists the notations used in this standard.

Table 3. Notations

285 Table [4](#page-17-0) lists the basic operations and functions used in this standard.

Table 4. Basic operations and functions

0x Hexadecimal notation $int64(x)$ 64-bit representation of integer x.

286 **2.1. Auxiliary Functions**

287 288 289 290 **Parse function.** The parse (X,r) function parses the input bitstring X into a sequence of blocks $X_0,X_1,...,\widetilde{X}_\ell$, where $\ell \leftarrow \lfloor |X|/r \rfloor$ (i.e., $X \leftarrow X_0 \, \|X_1\| \ldots \| \widetilde{X}_\ell$). The X_i blocks for $0 \leq i \leq \ell - 1$ each have a bit length r, whereas the bit length of the final block \widetilde{X}_{ℓ} is between 0 and $r-1$ (see Algorithm [1\)](#page-18-1).

Algorithm 1 parse (X, r)

Input: bitstring X , rate r **Output:** bitstrings $X_0, \ldots, X_{\ell-1}, \widetilde{X_{\ell}}$

 $\ell \leftarrow ||X|/r|$ **for** $i = 0$ to $\ell - 1$ **do** $X_i \leftarrow X_{[i \times r:(i+1) \times r-1]}$ **end for** $\widetilde{X_\ell}\leftarrow X_{[\ell\times r:\lvert X\rvert-1]}$ return $X_0, \ldots, X_{\ell-1}, \widetilde{X_\ell}$

291 292 293 **Padding rule.** The function pad (X,r) appends the bit 1 to the bitstring X, followed by the bitstring 0^j , where *j* is equal to $(-|X|-1)$ mod r. The length of the output bitstring is a multiple of r (see Algorithm [2\)](#page-18-2).

Algorithm 2 pad (X, r)

Input: bitstring X , rate r **Output:** padded bitstring X'

 $i \leftarrow (-|X|-1)$ mod r $X' \leftarrow X \parallel 1 \parallel 0^j$ r **eturn** X'

 294 **3. Ascon Permutations**

295 296 297 This section specifies the rnd -round $Ascon-p[rnd]$ permutations, where $1 \leq rnd \leq 16$. The permutations follow the Substitution-Permutation-Network (SPN) structure and consist of iterations of the round function p that is defined as the composition of three steps

$$
p = p_L \circ p_S \circ p_C,\tag{1}
$$

299 300 where p_C is the constant-addition layer (see Sec. [3.2\)](#page-19-2), p_S is the substitution layer (see Sec. [3.3\)](#page-20-0), and p_L is the linear diffusion layer (see Sec. [3.4\)](#page-21-0).

301 302 303 Note that $Ascon-p[8]$ and $Ascon-p[12]$ are the main building blocks of the Ascon family, and the permutation instantiated with other numbers of rounds may later be used to standardize other functionalities.

304 **3.1. Internal State**

305 306 The permutations operate on the 320-bit state S , which is represented as five 64-bit words denoted as S_i for $0 \leq i \leq 4$:

307

314

317

298

$$
S = S_0 \parallel S_1 \parallel S_2 \parallel S_3 \parallel S_4. \tag{2}
$$

308 309 310 Let $s_{(i,j)}$ represents the jth bit of S_i , $0 \leq j < 64$. In this specification of the Ascon permutation, each state word represents a 64-bit unsigned integer, where the least significant bit is the rightmost bit. Details on other representations of the state can be found in [Appendix](#page-41-0) A.

311 **3.2. Constant-Addition Layer**

312 313 The constant c_i of round i of the Ascon permutation $Ascon-p[rnd]$ (instantiated with rnd rounds), for $rnd \leq 16$ and $0 \leq i \leq rnd-1$, is defined as

$$
c_i = \text{const}_{16-rnd+i},\tag{3}
$$

315 316 where const $_0,...,$ const $_{15}$ are defined in Table [5.](#page-20-1) The constant-addition layer p_C adds a 64-bit round constant c_i to S_2 in round i, for $i \geq 0$,

$$
S_2 = S_2 \oplus c_i. \tag{4}
$$

318 319 Since the first 56 bits of the constants are zero, in practice, this is equivalent to applying the constant to only the least significant eight bits of S_2 , as shown in Fig. [1.](#page-20-2)

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Figure 1. Constant-Addition Layer

320 **3.3. Substitution Layer**

321 The substitution layer p_S updates the state S with 64 parallel applications of the 5-bit

322 substitution box SBOX, as

323

$$
(s_{(0,j)}, s_{(1,j)}, \dots, s_{(4,j)}) = \text{SBox}(s_{(0,j)}, s_{(1,j)}, \dots, s_{(4,j)})
$$
\n
$$
(5)
$$

324 for $0 \leq j < 64$, as shown in Fig. [2.](#page-20-3)

Figure 2. Substitution layer

325 326 327 The 5-bit SBOX has a 5-bit input $x = (x_0, x_1, \ldots, x_4)$ and computes the 5-bit output using the circuit provided in Figure [3.](#page-21-2) SBOX may also be implemented as a lookup table, as shown in Table [6.](#page-21-1)

Figure 3. 5-bit S-box SBOX

328 **3.4. Linear Diffusion Layer**

329 330 The linear diffusion layer p_L provides diffusion within each 64-bit word S_i , as shown in Fig. [4.](#page-21-3)

Figure 4. Linear diffusion layer p_L

This layer applies the linear functions Σ_i to their corresponding state words as $S_i \leftarrow \Sigma_i(S_i)$, for $0\leq i\leq 4$, where each Σ_i is defined as:

$$
\Sigma_0(S_0) = S_0 \oplus (S_0 \ggg 19) \oplus (S_0 \ggg 28)
$$
\n
$$
(6)
$$

$$
\Sigma_1(S_1) = S_1 \oplus (S_1 \ggg 61) \oplus (S_1 \ggg 39) \tag{7}
$$

$$
\Sigma_2(S_2) = S_2 \oplus (S_2 \ggg 1) \oplus (S_2 \ggg 6)
$$
 (8)

$$
\Sigma_3(S_3)=S_3\oplus (S_3\ggg 10)\oplus (S_3\ggg 17) \eqno{(9)}
$$

$$
\Sigma_4(S_4) = S_4 \oplus (S_4 \ggg 7) \oplus (S_4 \ggg 41) \tag{10}
$$

Note that 5-bit inputs are represented in hexadecimal, (e.g., $x = 1$ corresponds to $(0, 0, 0, 0, 1)$).

331 **4. Authenticated Encryption Scheme: Ascon-AEAD128**

332 333 334 This section specifies the AEAD scheme Ascon-AEAD128, details implementation options (e.g., truncation and nonce masking), lists AEAD requirements, and provides security properties.

335 **4.1. Specification of Ascon-AEAD128**

336 337 Ascon-AEAD128 consists of the encryption algorithm Ascon-AEAD128.enc (specified in Sec. [4.1.1\)](#page-22-2) and the decryption algorithm Ascon-AEAD128.dec (specified in Sec. [4.1.2\)](#page-25-0).

338 339 340 Ascon-AEAD128.enc takes a 128-bit secret key K , a 128-bit nonce N, variable-length associated data A, and variable-length plaintext P as inputs and outputs ciphertext C (where $|C| = |P|$) and 128-authentication tag T (see Section [4.2.1](#page-29-0) for the truncation option):

$$
\text{Ascon-AEAD128. enc}(K, N, A, P) = (C, T),\tag{11}
$$

342 343 Ascon-AEAD128. dec takes key K , nonce N, associated data A , ciphertext C , and authentication tag T as inputs and outputs P if the tag is valid:

$$
\text{Ascon-AEAD128.}\ \text{dec}(K,N,A,C,T) = \begin{cases} P & \text{if the tag } T \text{ is valid} \\ \text{fail} & \text{otherwise} \end{cases} \tag{12}
$$

345 **4.1.1. Encryption**

352

346 347 348 This section outlines the encryption algorithm of Ascon-AEAD128, which comprises four phases: initialization, associated data processing, plaintext processing, and finalization (see Fig. [5\)](#page-22-3).

Figure 5. Ascon-AEAD128 encryption

349 The pseudocode of Ascon-AEAD128.enc is provided in Algorithm [3.](#page-23-0)

350 351 1. **Initialization of the state.** Given 128-bit K and 128-bit N , the 320-bit internal state S is initialized as

$$
S \leftarrow IV \Vert K \Vert N \tag{13}
$$

Algorithm 3 Ascon-AEAD128.enc (K, N, A, P)

Input: 128-bit key K ; 128-bit nonce N ; Associated data A ; Plaintext P **Output:** Ciphertext C ; 128-bit tag T

```
IV \leftarrow 0x00001000808c0001 > \Box initialization
\mathcal{S} \leftarrow IV \Vert K \Vert NS \leftarrow Ascon-p[12](S)\mathcal{S} \leftarrow \mathcal{S} \oplus (\mathbf{0}^{192} \, \| \, K)if |A| > 0 then \triangleright Processing Associated Data
      A_0,\ldots,A_{m-1},\widetilde{A_m}\leftarrow \mathsf{parse}(A,128)A_m \leftarrowpad(\widetilde{A_m}, 128)for i = 0 to m do
            \mathcal{S} \leftarrow Ascon-p[8]((\mathcal{S}_{[0:127]} \oplus A_i) \| \mathcal{S}_{[128:319]})end for
end if
\mathcal{S} \leftarrow \mathcal{S} \oplus (0^{319} \, \| \, 1)P_0, \ldots, P_{n-1}, \widetilde{P_n} \leftarrow \mathsf{parse}(P, 128) \Rightarrow \qquad \qquad \rhd \mathsf{Processing \; Plaintext}\ell \leftarrow |\widetilde{P_n}|for i = 0 to n - 1 do
       \mathcal{S}_{[0:127]} \leftarrow \mathcal{S}_{[0:127]} \oplus P_iC_i \leftarrow S_{[0:127]}S \leftarrow Ascon-p[8](S)end for
\mathcal{S}_{[0:127]} \leftarrow \mathcal{S}_{[0:127]} \oplus \mathsf{pad}(\widetilde{P_n}, 128)\widetilde{C_n} \leftarrow \mathcal{S}_{[0,\ell-1]}C \leftarrow C_0 \, \Vert \, \ldots \, \Vert \, C_{n-1} \, \Vert \, \widetilde{C_n}S \leftarrow Ascon-p[12](\mathcal{S} \oplus (0^{128} \mathbin\Vert K \mathbin\Vert 0^{64})) \triangleright Finalization
T \leftarrow \mathcal{S}_{[192:319]} \oplus Kreturn C, T
```
353 354 355 356 357 358 359 360 361 362 363 364 365 366 367 368 369 370 371 372 373 374 375 376 377 378 379 380 where the initialization value IV is assigned to $0x00001000808c0001$ (see [Ap](#page-46-0)[pendix](#page-46-0) B for the details of determining the IV). Next, S is updated using the permutation $Ascon-p[12]$ as $S \leftarrow Ascon-p[12](S)$ (14) and followed by XORing the secret key K into the last 128 bits of internal state: $\mathcal{S} \leftarrow \mathcal{S} \oplus (0^{192} \| K).$ (15) 2. **Processing associated data.** This step has two parts, including absorbing the associated data (when it is non-empty) and applying the domain separation bit to the state. When associated data A is non-empty (i.e., $|A| > 0$), it is parsed into blocks, as $A_0, A_1, ..., A_{m-1}, \widetilde{A_m} \leftarrow \textsf{parse}(A, 128),$ (16) where $m=\lfloor|A|/128\rfloor$ and $|A_i|=128$ bits for $0\leq i\leq m-1$, and $0\leq |\widetilde{A_m}|< 128$, as explained in Algorithm [1.](#page-18-1) The last block $\widetilde{A_m}$ can be empty. Next, $\widetilde{A_m}$ is padded as $A_m \leftarrow \mathsf{pad}(\widetilde{A_m}, 128) = \widetilde{A_m} ||1 || 0^{127 - |\widetilde{A_m}|}$ (17) so that $|A_m| = 128$, as explained in Algorithm [2.](#page-18-2) Each associated data block A_i ($0 \le i \le m$), is absorbed into the first 128 bits of state as $\mathcal{S}_{[0:127]} \leftarrow \mathcal{S}_{[0:127]} \oplus A_i,$ (18) and the permutation $Ascon-p[8]$ is applied to the state as $S \leftarrow Ascon-p[8](S).$ (19) The final step of processing associated data is to update the state with a constant $\mathcal{S} \leftarrow \mathcal{S} \oplus (0^{319} \| 1)$ (20) that provides domain separation. For empty associated data, only the final step described in [\(20\)](#page-24-0) is applied. 3. **Processing plaintext.** Plaintext P (including empty plaintext) is parsed into blocks as $P_0, P_1, ..., P_{n-1}, \widetilde{P_n} \leftarrow \text{parse}(P, 128),$ (21) where $n = \lfloor |P|/128 \rfloor$ and $|P_i| = 128$ for $0 \le i \le n-1$, and $|\widetilde{P_n}| = \ell$, $0 \le \ell < 128$ using Algorithm [1.](#page-18-1) When $|P|$ mod $128 = 0$, the last block $\widetilde{P_n}$ is empty.

401 **4.1.2. Decryption**

402 403 404 405 Thissection describes each of the phasesfor decryption with Ascon-AEAD128.dec. Decryption in Ascon-AEAD128 consists of four phases: initialization, associated data processing, ciphertext processing, and finalization. Decryption in Ascon-AEAD128 is similar to encryption; only the last two phases differ from the encryption mode.

406 The pseudocode of Ascon-AEAD128.dec is provided in Algorithm [4.](#page-26-0)

Algorithm 4 Ascon-AEAD128.dec(K, N, A, C, T)

Input: 128-bit key K ; 128-bit nonce N ; Associated data A ; Ciphertext C ; 128-bit tag T **Output:** Plaintext Por fail

```
IV \leftarrow 0x00001000808c0001 \triangleright Initialization
\mathcal{S} \leftarrow IV \Vert K \Vert NS \leftarrow Ascon-p[12](S)\mathcal{S} \leftarrow \mathcal{S} \oplus (0^{192} \parallel \hat{K})if |A| > 0 then \triangleright Processing Associated Data
      A_0, \ldots, A_{m-1}, \widetilde{A_m} \leftarrow \textsf{parse}(A, 128)A_m \leftarrowpad(\widetilde{A_m}, 128)for i = 0 to m do
             \mathcal{S}_{[0:127]} \leftarrow \mathcal{S}_{[0:127]} \oplus A_iS \leftarrow Ascon-p[8](S)end for
end if
\mathcal{S} \leftarrow \mathcal{S} \oplus (0^{319} \, \| \, 1)C_0, \ldots, C_{n-1}, \widetilde{C_n} \leftarrow \mathsf{parse}(C, 128) \Rightarrow \qquad \qquad \rhd \mathsf{Processing\,Ciphertext}for i = 0 to n - 1 do
      P_i \leftarrow \mathcal{S}_{[0:127]} \oplus C_i\mathcal{S}_{[0:127]} \leftarrow C_i\mathcal{S} \leftarrow Ascon-p[8](\mathcal{S})end for
\ell = |\widetilde{C_n}|\widetilde{P_n} \leftarrow \mathcal{S}_{[0:\ell-1]} \oplus \widetilde{C_n}\mathcal{S}_{[\ell,127]} \leftarrow \mathcal{S}_{[\ell,127]} \oplus (1||0^{127-\ell})\mathcal{S}_{[0,\ell-1]} \leftarrow \widetilde{C}_nS \leftarrow Ascon-p[12](S \oplus (0^{128} \parallel K \parallel 0^{64})) \triangleright Finalization
T' \leftarrow \mathcal{S}_{[192:319]} \oplus Kif T' == T then
      P \leftarrow P_0 \|\ldots\| P_{n-1} \|\widetilde{P_n}return 
else
      return fail
end if
```


Figure 6. Ascon-AEAD128 decryption

407 408 409 410 411 412 413 414 415 416 417 418 419 420 421 422 423 424 425 426 1. **Initialization of the state.** Given 128-bit K and 128-bit N , the 320-bit internal state S is initialized as $\mathcal{S} \leftarrow IV || K || N,$ (31) where the initial value IV is assigned to $0x00001000808c0001$. Next, S is updated using the permutation $Ascon-p[12]$ as $\mathcal{S} \leftarrow Ascon-p[12](\mathcal{S})$ (32) and followed by XORing the secret key into the last 128 bits of the state as $\mathcal{S} \leftarrow \mathcal{S} \oplus (0^{192} || K).$ (33) This step is exactly the same as Step 1 of the encryption function in Sec. [4.1.1.](#page-22-2) 2. **Processing associated data.** This step has two parts, including absorbing the associated data (when it is non-empty) and applying the domain separation bit to the state. When the associated data A is non-empty (i.e., $|A| > 0$), it is parsed into blocks, as $A_0, A_1, ..., A_{m-1}, \widetilde{A_m} \leftarrow \textsf{parse}(A, 128),$ (34) where $m = \lfloor |A|/128 \rfloor$ and $|A_i| = 128$ bits for $0 \le i \le m-1$, and $0 \le |\widetilde{A_m}| < 128$, as explained in Algorithm [1.](#page-18-1) The last block $\widetilde{A_m}$ can be empty. $\widetilde{A_m}$ is further processed by padding to a full $r = 128$ $r = 128$ $r = 128$ -bit block using Algorithm 2 as $A_m \leftarrow \text{pad}(\widetilde{A_m}, 128) = \widetilde{A_m} || 1 || 0^{127 - |\widetilde{A_m}|}.$ (35) The associated data blocks A_i 's ($0 \le i \le m$), are absorbed to the state $\mathcal S$ as follows: $\mathcal{S}_{[0:127]} \leftarrow (\mathcal{S}_{[0:127]} \oplus A_i),$ (36)

456 **4.2. Implementation Options**

457 **4.2.1. Truncation**

458 459 Some applications may truncate the tag T to a specific length $\lambda \leq |T|$). The truncation function outputs the leftmost λ bits $T_{[0:\lambda-1]}$ of the tag.

460 The requirements on the tag lengths are provided in Sec. [4.3.](#page-29-2)

461

462 **4.2.2. Nonce Masking**

463 This section provides an option to implement Ascon-AEAD128 using a 256-bit key, mainly

464 to maintain the 128-bit security strength of Ascon-AEAD128 in a multi-key setting [\[12\]](#page-40-1). In

465 this option, an additional 128-bit key is used to mask the input nonce.

466 467 Let K be the 128-bit key of Ascon-AEAD128 and K' be an independently generated additional 128-bit key. Ascon-AEAD128 with nonce masking is processed as follows:

$$
E(K \mid K', N, A, P) = \text{Ascon-AEAD128. enc}(K, N \oplus K', A, P),
$$
\n(50)

469 470 $\mathtt{D}(K\big\Vert K',N,A,C,T) = \mathtt{Ascon-AEAD128.dec}(K,N\oplus K',A,C,T)$ (51)

471 472 473 474 Ascon-AEAD128 with nonce masking should only be used when context-commitment security [\[13\]](#page-40-2) and related-key security are not concerns because the encryption of Ascon-AEAD128 with nonce masking always outputs the same (C, T) pair for two different input tuples $(K \mid K', N, A, P)$ and $(K \mid K'', N', A, P)$, where $N \oplus K' = N' \oplus K''$.

475 **4.3. AEAD Requirements**

476 This section specifies requirements for Ascon-AEAD128.

477 478 479 480 **R1. Key generation.** The secret key K and the nonce-masking key K' (if available) **shall** be generated following the recommendations for cryptographic key generation specified in SP 800-133 $[14]$ and using an approved random bit generator that supports at least a 128-bit security strength. The keys **shall** not be used for other purposes.

481 482 483 **R2. Use of unique nonce.** Nonce **shall** be distinct for each encryption operation for a given key to ensure that identical plaintexts encrypted multiple times produce different ciphertext.

484 485 486 **R3. Minimum length of truncated tag.** When an application uses truncated tags, the bit length of the truncated tags **shall** be at least 64 bits, and the tag length **shall** be the same across the life-span of the key.

- 487 488 489 **R4. Limit on the maximum number of decryption failures.** When the tag bit length is λ , $64 \leq \lambda \leq 128$, the maximum number of decryption failures for a fixed key **shall** be at most $2^{\lambda-64}$.
- 490 491 **R5. Data limit.** The total amount of data processed during encryption and decryption, including the nonce, **shall not** exceed 2^{54} bytes for a given key.
- 492 493 494 **R6. Key update.** The key **shall** be updated to a new one when the total number of input data blocks or the number of decryption failures reach their respective limits or if the nonce uniqueness requirement is violated.

495 **4.4. Security Properties**

- 496 497 498 This section provides the security properties of Ascon-AEAD128 in various scenarios, including single-key and multi-key settings, nonce-respecting and nonce-misuse settings, and with or without the truncation option.
- 499 500 501 In the single-key setting, the attacker focuses on a specific key that is shared by one or more users. In contrast, in the multi-key setting with u keys, the attacker aims to compromise any of the u keys used by the users.
- 502 503 The security of the Ascon-AEAD128 mode, in both single-key and multi-key settings, was evaluated in [\[12,](#page-40-1) [15–](#page-40-4)[17\]](#page-40-5).

504 **4.4.1. Single-Key Setting**

505 506 507 508 Ascon-AEAD128 (with no tag truncation) provides a 128-bit security strength in the singlekey and nonce-respecting setting, for the confidentiality of the plaintext (except for its length) and the integrity of the tuple (nonce, associated data, ciphertext, tag), where the total number of input bytes is limited to 2^{54} (i.e., 2^{50} blocks).

509 510 511 512 513 514 515 *Impact of truncation.* When the tag is λ bits, $64 \leq \lambda \leq 128$, the maximum number of decryption failures for a fixed key is limited to $2^{\lambda-64}$. Therefore, the probability that there is a valid forgery is at most 2^{-64} . Once a forgery attempt is successful, the confidentiality of the plaintext can be immediately compromised, as the decryption function may reveal some information about the plaintext. Therefore, in the single-key setting, Ascon-AEAD128 with tag length λ provides (min $\{128,\lambda\}$)-bit security strengths for confidentiality and integrity in the nonce-respecting setting.

516 **4.4.2. Multi-Key Setting**

517 518 519 When u keys are independently selected for an application, $\text{Ascon}-\text{AEAD128}$ (with no tagtruncation) provides a (128 $-$ log₂ u)-bit security strength in the nonce-respecting setting, for the confidentiality of the plaintext and the integrity of the tuple of (nonce, associated

520 521 data, ciphertext, tag), where the total number of input bytes for all u keys is limited to 2^{54} (i.e., 2^{50} blocks).

522 523 524 When the same nonce is used with u keys, an attacker may be able to discover one of the u keys with a time complexity of $2^{128-\log_2 u}$, thereby compromising both confidentiality and integrity.

525 To improve security in a multi-key setting, the nonce masking implementation option (see

526 527 Sec. [4.2.2\)](#page-29-1) can be used. This option provides 128-bit security (rather than $128 - \log_2(u)$) for confidentiality and integrity.

528 529 530 531 532 *Impact of truncation.* When the tag is truncated to λ bits, $64 \leq \lambda \leq 128$, the maximum number of decryption failures for all u keys is limited to $2^{\lambda-64}$. Therefore, the probability of obtaining a valid forgery is expected to be at most 2^{-64} . In the multi-key setting, Ascon-AEAD128 with tag-length λ provides (min $\{128-\log_2 u,\lambda\}$)-bit security strengths of confidentiality and integrity in the nonce-respecting setting.

533 **4.4.3. Nonce-Misuse Setting**

534 535 536 The plaintext confidentiality of Ascon-AEAD128 is lost when a nonce is repeated with the same secret key. However, Ascon-AEAD128 is designed to provide some level of security in case of certain implementation errors that violate the nonce-respecting requirement.

537 538 539 540 541 • In the u -key setting, Ascon-AEAD128 with a λ -bit tag provides (min $\{128-\log_2(u),\lambda\}$)bit security strengths of confidentiality and integrity when a (nonce, associated data) pair is never repeated for two encryptions with each of u keys and the number of nonce repetitions per key for encryption is limited to $2⁸$. In this scenario, the security strengths of Ascon-AEAD128 are summarized in Table [7.](#page-31-1)

542 543 544 545 546 • Ascon-AEAD128 with λ -bit tag also provides a (min $\{128-\log_2(u),\lambda\}$)-bit integrity security strength of the tuple (nonce, associated data, ciphertext, tag) if the number of repetitions of any (nonce, associated data) pair per each of u keys for encryption is limited to 2^8 . In this scenario, the integrity security strength of Ascon-AEAD128 with λ -bit tag is summarized in Table [8.](#page-32-2)

Table 7. Security strength of Ascon-AEAD128 with λ -bit tag in the u -key setting, where (N, (A) pair is unique for encryption.

547 **5. Hash and Extendable Output Functions**

548 549 Hash and extendable output functions are built on the $Ascon-p[12]$ permutation in a sponge-based mode. This section specifies three functions:

- 550 • The hash function Ascon-Hash256, which produces a 256-bit digest,
- 551 • The Ascon-XOF128 function that produces arbitrary length outputs, and
- 552 • The customized XOF Ascon-CXOF128.

553 **5.1. Specification of Ascon-Hash256**

564

554 555 556 557 The mode of operation used by Ascon-Hash256 and Ascon-XOF128 isshown in Fig. [7.](#page-32-3) This mode comprises three main steps: initialization, absorbing the message, and squeezing the output. Note that L, the length of the output, and is 256 for Ascon-Hash256 and $L > 0$ for Ascon-XOF128.

Figure 7. Structure of Ascon-Hash256 and Ascon-XOF128

558 559 560 Ascon-Hash256 takes a variable length message M as input and produces a 256-bit digest. The full specification of Ascon-Hash256 can be found in Algorithm [5](#page-34-0) and operates as follows:

561 562 563 1. **Initialization.** The 320-bit internal state of Ascon-Hash256 is initialized with the concatenation of the 64-bit $IV = 0x0000080100cc0002$ and 256 zeroes, followed by the $Ascon-p[12]$ permutation. That is the initialization step is

 $S \leftarrow Ascon-p[12](IV || 0^{256}).$ (52)

Table 8. Integrity security strength of $Ascon-AEAD128$ with u keys in the nonce-misuse setting

588

565 566 567 568 569 570 571 572 573 574 575 576 577 578 579 580 581 582 583 584 585 586 587 2. **Absorbing the message.** The absorbing phase behaves similarly to the associated data processing of Ascon-AEAD128. The message is partitioned into 64-bit blocks as $M_0, \ldots, M_{n-1}, \widetilde{M_n} \leftarrow \textsf{parse}(M, 64).$ (53) Partial block $\widetilde{M_n}$ is then padded to a full block M_n : $M_n \leftarrow \text{pad}(\widetilde{M_n}, 64).$ (54) Each message block M_i is XORed with the state as $\mathcal{S}_{[0:63]} \leftarrow \mathcal{S}_{[0:63]} \oplus M_i.$ (55) For all message blocks except the final block M_n , the XOR operation is immediately followed by applying $Ascon-p[12]$ to the state. $S \leftarrow Ascon-p[12](S)$ (56) 3. **Squeezing the hash.** The squeezing phase begins after M_n is absorbed with an application of $Ascon-p[12]$ to the state. $S \leftarrow Ascon-p[12](S)$ (57) The value of $\mathcal{S}_{[0:63]}$ is then taken as hash block H_i , and the state is again updated by $Ascon-p[12]$. $H_i \leftarrow \mathcal{S}_{[0.63]}$ (58) $S \leftarrow Ascon-p[12](S)$ (59) Steps [\(58\)](#page-33-1) and [\(59\)](#page-33-2) are repeated alternately until hash blocks H_0,H_1 , and H_2 have been extracted. The final hash block is then extracted but is not followed by the permutation. $H_3 \leftarrow S_{[0:63]}$ (60) The resulting 256-bit digest is the concatenation of hash blocks as $H \leftarrow H_0 \| H_1 \| H_2 \| H_3.$ (61)

Algorithm 5 Ascon-Hash256(M) **Input:** Bitstring $M \in \{0,1\}^*$ **Output:** Digest $H \in \{0,1\}^{256}$ $IV \leftarrow 0 \times 0000080100 \text{cc} 0002$ $\mathcal{S} \leftarrow Ascon-p[12] (IV \parallel 0^{256})$ $M_0, \ldots, M_{n-1}, \widetilde{M_n} \leftarrow \mathsf{parse}(M, 64) \qquad \qquad \rhd \mathsf{Absorbing}$ $M_n \leftarrow \textsf{pad}(\widetilde{M_n}, 64)$ **for** $i = 0$ to $n - 1$ **do** $\mathcal{S}_{[0:63]} \leftarrow \mathcal{S}_{[0:63]} \oplus M_i$ $S \leftarrow Ascon-p[12](S)$ **end for** $\mathcal{S}_{[0:63]} \leftarrow \mathcal{S}_{[0:63]} \oplus M_n$ $S \leftarrow Ascon-p[12](S)$ \triangleright Squeezing **for** $i = 0$ to 2 **do** $H_i \leftarrow \mathcal{S}_{[0:63]}$ $\mathcal{S} \leftarrow Ascon-p[12](\mathcal{S})$ **end for** $H_3 \leftarrow \mathcal{S}_{[0:63]}$ $H \leftarrow H_0 \, \| H_1 \, \| H_2 \, \| H_3$ **return**

616 617 618 619 620 621 622 623 624 625 626 627 628 The value of $\mathcal{S}_{[0:63]}$ is then taken as output block H_i , and the state is again updated by $Ascon-p[12]$. $H_i \leftarrow \mathcal{S}_{[0:63]}$ (68) $S \leftarrow Ascon-p[12](S)$ (69) Steps [\(68\)](#page-36-2) and [\(69\)](#page-36-3) are repeated alternately until output blocks H_0, \ldots, H_{h-1} have been squeezed. The final block is then squeezed without an additional permutation. $H_h \leftarrow S_{[0:63]}$ (70) Finally, the output blocks are concatenated, and the first L bits are returned as output Н. $H' \leftarrow H_0 ||...|| H_h$ (71) $H \leftarrow H'_{[0:L-1]}$ (72) $\mathsf{Algorithm}\ 6\ \text{Ascon-XOF128}(M,\ L)$ **nput:** Bitstring $M \in \{0, 1\}^*$; Output length $L > 0$ **utput:** Digest $H \in \{0,1\}^L$ $IV \leftarrow 0x0000080000c c0003$ \triangleright Initialization $\mathcal{S} \leftarrow Ascon-p[12](IV \parallel 0^{256})$ **I O**

$$
M_0, ..., M_{n-1}, \widetilde{M_n} \leftarrow \text{parse}(M, 64) \qquad \qquad \triangleright \text{Absorbing} \nM_n \leftarrow \text{pad}(\widetilde{M_n}, 64) \n\text{for } i = 0 \text{ to } n - 1 \text{ do} \nS_{[0:63]} \leftarrow S_{[0:63]} \oplus M_i \nS \leftarrow Ascon-p[12](S) \n\text{end for} \nS_{[0:63]} \leftarrow S_{[0:63]} \oplus M_n \n\quad + [L/64] - 1 \n\text{for } i = 0 \text{ to } h - 1 \text{ do} \n\quad_{i} \leftarrow S_{[0:63]} \n\quad S \leftarrow Ascon-p[12](S) \n\text{end for} \nH_n \leftarrow S_{[0:63]} \nH_n \leftarrow S_{[0:63]} \nH'_n \leftarrow H_0 |... || H_h \nH \leftarrow H'_{[0:L-1]} \n\text{return } H
$$

Figure 8. Structure of Ascon-CXOF128

629 **5.3. Specification of Ascon-CXOF128**

630 631 632 633 634 This section specifies the customized version of Ascon-XOF128 called Ascon-CXOF128. Customization extends the functionality of Ascon-XOF128 by allowing users to incorporate a customization string into the computation. For the same input message, two instances of a customized XOF using different customization strings will produce distinct outputs. Ascon-CXOF128 is a customized XOF that differs from Ascon-XOF128 in the following ways:

- 635 636 • For domain separation, Ascon-CXOF128 uses a different IV than Ascon-XOF128. The IV for Ascon-CXOF128 is 0x0000080000cc0004.
- 637 638 • In addition to the message, $Ascon-CXOF128$ takes the customization string Z as input. The length of the customization string **shall** be at most 2048 bits (i.e., 256 bytes).
- 639 • The customization string Z is prepended to the message blocks as
- 640

 $Z_0 || Z_1 || ... || Z_m || M_0 || ... || M_{n-1} || M_n,$ (73)

641 642 where Z_0 is a 64-bit integer that represents the bit-length of the customization string, and Z_1, \ldots, Z_m are 64-bit blocks generated by parsing and padding Z.

643 644 The general structure for Ascon-CXOF12[8](#page-37-1) is shown in Fig. 8 and the full specification is given by Algorithm [7.](#page-38-0)

645 **5.4. Security Strengths**

646 647 The security strengths of Ascon-Hash256, Ascon-XOF128, and Ascon-CXOF128 are summarized in Table [9.](#page-39-0)

Algorithm 7 Ascon-CXOF128(M , L , Z)

Input: Bitstring $M \in \{0,1\}^*$; Output length $L > 0$; customization string $Z \in \{0,1\}^*$, where $|Z| \le 2048$ **Output:** Digest $H \in \{0,1\}^L$ $IV \leftarrow 0x0000080000c\cos 0004$
 \triangleright Initialization $\mathcal{S} \leftarrow Ascon-p[12](IV \parallel 0^{256})$ $Z_0 \leftarrow \text{int64}(|Z|)$ \triangleright Customization $Z_1 \ldots, Z_{m-1}, \widetilde{Z_m} \leftarrow \mathsf{parse}(Z, 64)$ $Z_m \leftarrow \textsf{pad}(\widetilde{Z_m}, 64)$ f **or** $i = 0$ to m **do** $\mathcal{S}_{[0:63]} \leftarrow \mathcal{S}_{[0:63]} \oplus Z_i$ $S \leftarrow Ascon-p[12](S)$ **end for** $M_0, \ldots, M_{n-1}, \widetilde{M_n} \leftarrow \mathsf{parse}(M, 64) \qquad \qquad \rhd \mathsf{Absorbing \; message}$ $M_n \leftarrow$ pad $(\widetilde{M_n}, 64)$ **for** $i = 0$ to $n - 1$ **do** $\mathcal{S}_{[0:63]} \leftarrow \mathcal{S}_{[0:63]} \oplus M_i$ $S \leftarrow Ascon-p[12](S)$ **end for** $\mathcal{S}_{[0:63]} \leftarrow \mathcal{S}_{[0:63]} \oplus M_n$ $S \leftarrow Ascon-p[12](S)$ \triangleright Squeezing $h \leftarrow \lceil L/64 \rceil - 1$ **for** $i = 0$ to $h - 1$ **do** $H_i \leftarrow \mathcal{S}_{[0:63]}$ $\mathcal{S} \leftarrow Ascon-p[12](\mathcal{S})$ **end for** $H_h \leftarrow \mathcal{S}_{0.63}$ $H' \leftarrow H_0 \, \| \ldots \| \, H_h$ $H \leftarrow H'_{[0:L-1]}$ **return**

Table 9. Security strengths of Ascon-Hash256, Ascon-XOF128, and Ascon-CXOF128 algorithms

648 **References**

649 650 651 [1] Dobraunig C, Eichlseder M, Mendel F, Schläffer M (2014) Ascon v1, Submission to Round 1 of the CAESAR competition. Available at [https://competitions.cr.yp.to/roun](https://competitions.cr.yp.to/round1/asconv1.pdf) [d1/asconv1.pdf.](https://competitions.cr.yp.to/round1/asconv1.pdf)

- 652 653 654 [2] Dobraunig C, Eichlseder M, Mendel F, Schläffer M (2015) Ascon v1.1, Submission to Round 2 of the CAESAR competition. Available at [https://competitions.cr.yp.to/roun](https://competitions.cr.yp.to/round2/asconv11.pdf) [d2/asconv11.pdf.](https://competitions.cr.yp.to/round2/asconv11.pdf)
- 655 656 657 [3] Dobraunig C, Eichlseder M, Mendel F, Schläffer M (2016) Ascon v1.2, Submission to Round 3 of the CAESAR competition. Available at [https://competitions.cr.yp.to/roun](https://competitions.cr.yp.to/round3/asconv12.pdf) [d3/asconv12.pdf.](https://competitions.cr.yp.to/round3/asconv12.pdf)
- 658 659 [4] National Institute of Standards and Technology (2001) Advanced Encryption Standard (AES) (U.S. Department of Commerce), Report. [DOI:10.6028/NIST.FIPS.197-upd1](https://doi.org/10.6028/NIST.FIPS.197-upd1)
- 660 661 662 [5] Dworkin MJ (2007) Recommendation for Block Cipher Modes of Operation: Galois/Counter Mode (GCM) and GMAC (National Institute of Standards and Technology), Report. [DOI:10.6028/NIST.SP.800-38D](https://doi.org/10.6028/NIST.SP.800-38D)
- 663 664 [6] National Institute of Standards and Technology (2015) Secure Hash Standard (SHS) (U.S. Department of Commerce), Report. [DOI:10.6028/NIST.FIPS.180-4](https://doi.org/10.6028/NIST.FIPS.180-4)
- 665 666 667 [7] National Institute of Standards and Technology (2015) SHA-3 Standard: Permutation-Based Hash and Extendable-Output Functions(U.S. Department of Commerce), Report. [DOI:10.6028/NIST.FIPS.202](https://doi.org/10.6028/NIST.FIPS.202)
- 668 669 670 671 [8] Dobraunig C, Eichlseder M, Mendel F, Schläffer M (2021) Ascon v1.2, Submission to Final Round of the NIST Lightweight Cryptography project. Available at [https:](https://csrc.nist.gov/CSRC/media/Projects/lightweight-cryptography/documents/finalist-round/updated-spec-doc/ascon-spec-final.pdf) [//csrc.nist.gov/CSRC/media/Projects/lightweight-cryptography/documents/finalist-r](https://csrc.nist.gov/CSRC/media/Projects/lightweight-cryptography/documents/finalist-round/updated-spec-doc/ascon-spec-final.pdf) [ound/updated-spec-doc/ascon-spec-final.pdf.](https://csrc.nist.gov/CSRC/media/Projects/lightweight-cryptography/documents/finalist-round/updated-spec-doc/ascon-spec-final.pdf)
- 672 673 674 [9] Sönmez Turan M, McKay KA, Çalık Ç, Chang D, Bassham I Lawrence E (2019) Status Report on the First Round of the NIST Lightweight Cryptography Standardization Process (National Institute of Standards and Technology), Report. [DOI:10.6028/NIST.IR.8268](https://doi.org/10.6028/NIST.IR.8268)
- 675 676 677 678 [10] Sönmez Turan M, McKay KA, Chang D, Çalık Ç, Bassham I Lawrence E, Kang J, Kelsey J (2021) Status Report on the Second Round of the NIST Lightweight Cryptography Standardization Process (National Institute of Standards and Technology), Report. [DOI:10.6028/NIST.IR.8369](https://doi.org/10.6028/NIST.IR.8369)
- 680 679 681 682 [11] Sönmez Turan M, McKay KA, Chang D, Bassham L, Kang J, Waller N, Kelsey J, Hong D (2023) Status Report on the Final Round of the NIST Lightweight Cryptography Standardization Process (National Institute of Standards and Technology), Report. [DOI:10.6028/NIST.IR.8454](https://doi.org/10.6028/NIST.IR.8454)
- 685 683 684 686 [12] Dobraunig C, Mennink B (2024) Generalized initialization of the duplex construction. *Applied Cryptography and Network Security - 22nd International Conference, ACNS 2024, Abu Dhabi, United Arab Emirates, March 5-8, 2024, Proceedings, Part II*, eds Pöpper C, Batina L (Springer), *Lecture Notes in Computer Science*, Vol. 14584, pp

687 460–484. [DOI:10.1007/978-3-031-54773-7_18](https://doi.org/10.1007/978-3-031-54773-7_18)

- 690 688 689 [13] Bellare M, Hoang VT (2022) Efficient schemes for committing authenticated encryption. *Advances in Cryptology - EUROCRYPT 2022 - 41st Annual International Conference on the Theory and Applications of Cryptographic Techniques, Trondheim, Norway, May*
- 691 *30 - June 3, 2022, Proceedings, Part II*, eds Dunkelman O, Dziembowski S (Springer),
- 692 693 *Lecture Notes in Computer Science*, Vol. 13276, pp 845–875. [DOI:10.1007/978-3-031-](https://doi.org/10.1007/978-3-031-07085-3_29) [07085-3_29](https://doi.org/10.1007/978-3-031-07085-3_29)
- 695 694 696 [14] Barker E, Roginsky A, Davis R (2020) Recommendation for cryptographic key generation, (National Institute of Standards and Technology, Gaithersburg, MD), NIST Special Publication (SP) 800-133 Rev. 2. [DOI:10.6028/NIST.SP.800-133r2.](https://doi.org/10.6028/NIST.SP.800-133r2)
- 700 697 698 699 701 [15] Chakraborty B, Dhar C, Nandi M (2023) Exact security analysis of ASCON. *Advances in Cryptology - ASIACRYPT 2023 - 29th International Conference on the Theory and Application of Cryptology and Information Security, Guangzhou, China, December 4-8, 2023, Proceedings, Part III*, eds Guo J, Steinfeld R (Springer), *Lecture Notesin Computer Science*, Vol. 14440, pp 346–369. [DOI:10.1007/978-981-99-8727-6_12](https://doi.org/10.1007/978-981-99-8727-6_12)
- 702 703 704 [16] Lefevre C, Mennink B (2023) Generic Security of the Ascon Mode: On the Power of Key Blinding, Cryptology ePrint Archive, Paper 2023/796. Available at [https://ia.cr/20](https://ia.cr/2023/796) [23/796.](https://ia.cr/2023/796)
- 705 706 707 [17] Chakraborty B, Dhar C, Nandi M (2024) Tight multi-user security of ascon and its large key extension. *Information Security and Privacy - 29th Australasian Conference, ACISP 2024, Sydney, NSW, Australia, July 15-17, 2024, Proceedings, Part I*, eds Zhu T, Li Y
- 708 (Springer), *Lecture Notesin Computer Science*, Vol. 14895, pp 57–76. [DOI:10.1007/978-](https://doi.org/10.1007/978-981-97-5025-2_4)
- 709 [981-97-5025-2_4](https://doi.org/10.1007/978-981-97-5025-2_4)

710 **Appendix A. Implementation Notes**

711 712 713 714 715 This specification follows the little-endian ordering convention. That is, on little-endian machines, byte strings or words of any size can be loaded from memory directly into the Ascon state without the need to perform any conversion. Neither bytes nor bits need to be reversed. The hexadecimal forms of the padding for Ascon functions are described in Sec. [A.2.](#page-42-0)

716 717 718 719 However, the convention for printing the Ascon state using 64-bit integer words in hexadecimal notation (most significant byte and bit first) is different from printing the Ascon state using byte sequences or bitstrings (least significant byte and bit first). The conversion functions between printing byte sequences and printing integers are specified in Sec. [A.1.](#page-41-1)

720 The least significant bit of S_0 is $s_{(0,0)}$ (or $S_{[0:0]}$) and the most significant bit of S_4 is $s_{(4,63)}$

721 (or $S_{[319:319]}$). Similarly, the least significant byte of S_0 is the first byte of state ($S_{[0:7]}$) and

722 the most significant byte of S_4 is the last byte of the state ($\mathcal{S}_{[312:319]}$). This relationship

723 between state words, bytes, and state bits is shown in Fig. [9,](#page-41-2) where $S_i[j]$ denotes the j^{th}

724 byte of state word S_i for $0 \le i \le 4$ and $0 \le j \le 7$.

Figure 9. Mapping between state words, bytes, and bits

725 **A.1. Conversion Functions**

726 727 When printing values as integers using hexadecimal notation, the most significant byte and most significant bit are shown first.

728 729 730 731 **Integers and byte sequences.** Printing the integer representation of a byte sequence requires the byte order to be reversed. That is, the first element in the sequence of bytes is the least significant byte of the integer, while the last element in the sequence of bytes is the most significant byte of the integer.

732 733 734 735 **Integers and bitstrings.** Printing a bitstring as an integer requires the byte order to be reversed, and additionally, bits within a byte to be reversed. That is, the first element of a bitstring is the least significant bit of the integer (or byte), while the last element of the bitstring is the least significant bit of the integer (or byte).

Table 10. Address for each byte of Ascon state word S_i in memory on little-endian and big-endian machines, where the word S_i begins at memory address a.

736 737 738 739 740 **Loading 64-bit integer words from a byte sequence.** When loading the state from a sequence of bytes stored in memory, the first eight bytes are mapped to the first 64-bit unsigned integer word S_0 in little-endian notation (i.e., without byte reversal on little-endian machines). The next eight bytes are loaded to S_1 . Bytes continue to be loaded in the same way until the final eight bytes of the stored state are loaded into S_4 .

741 742 743 744 An example of the mapping between memory addresses to state word bytes is presented in Table [10](#page-42-1) for both little-endian and big-endian machines. An example of mappings between 64-bit unsigned integers, byte sequences, and bitstrings is shown in Fig. [10.](#page-43-0) Note that 64-bit integers and bitstrings only appear to be reversed in the visual representation.

745 746 747 748 **Writing 64-bitinteger wordsto a byte sequence.** The processfor writing the 64-bit unsigned integer Ascon state words to a byte sequence in memory is simply the reverse of loading a state word from a byte sequence. The byte order does not need to be reversed on little-endian machines.

749 **A.2. Implementing with Integers**

750 751 This section provides additional information for software implementations that employ 64-bit unsigned integers.

752 **Padding.** The padding rule described in Algorithm [2](#page-18-2) appends a one followed by one or

753 more zeroes to data. For an integer x that can be represented with $n < 8$ bytes, an integer

754 y representing a padded version of x is computed as:

755 $y \leftarrow x \oplus (0x00000000000000001 \ll 8n)$

Domain Separation Bit. The hexadecimal integer form of the domain separation bit is 0x8000000000000000. Therefore, the addition of this bit into the state may be imple-

Figure 10. Representation of the Ascon state as 64-bit unsigned integers, byte sequences, and bitstrings, where 64-bit unsigned integers are used to define the permutation, data stored in memory is represented as byte sequences, and bitstrings are used to specify the modes of operation. Note that 64-bit integers and bitstrings only appear to be reversed in the visual representation.

Table 11. Examples of padding an unsigned integer x to a 64-bit block, where x encodes a sequence of bytes each having value 0xFF in little-endian byte order.

mented as:

 $S_4 \leftarrow S_4 \oplus {\tt 0x800000000000000}.$

64-bit Block Absorption. In Ascon-Hash256, Ascon-XOF128, or Ascon-CXOF128, the absorption of a 64-bit message block expressed as the byte sequence 0x00, 0x01, 0x02, 0x03, 0x04, 0x05, 0x06, 0x07 can be implemented as:

 $S_0 \leftarrow S_0 \oplus 0 \times 0706050403020100,$

128-bit Block Absorption. Absorbing a 128-bit associated data or plaintext block represented by byte sequence 0x00, 0x01, 0x02, 0x03, 0x04, 0x05, 0x06, 0x07, 0x08, 0x09, 0x0A, 0x0B, 0x0C, 0x0D, 0x0E, 0x0F can similarly be implemented as:

> $S_0 \leftarrow S_0 \oplus 0 \times 0706050403020100$ $S_1 \leftarrow S_1 \oplus$ 0x0F0E0D0C0B0A0908

Key Addition. Ascon-AEAD128 has keyed initialization and finalization, where the key is added to the state in various locations. For a key represented as a sequence of bytes having value 0x00, 0x01, 0x02, 0x03, 0x04, 0x05, 0x06, 0x07, 0x08, 0x09, 0x0A, 0x0B, 0x0C, 0x0D, 0x0E, 0x0F, the key addition at the beginning of the initialization phase may be written as:

$$
\begin{aligned} S_1 \leftarrow & S_1 \oplus \texttt{0x0706050403020100} \\ S_2 \leftarrow & S_2 \oplus \texttt{0x0F0E0DOCOBOAO908}, \end{aligned}
$$

the key addition at the end of the initialization phase may be written as:

 $S_3 \leftarrow S_3 \oplus 0 \times 0706050403020100$ $S_4 \leftarrow S_4 \oplus \texttt{OxOFOEODOCOBOAO908},$

the key addition at the beginning of the finalization phase can be expressed as:

 $S_2 \leftarrow S_2 \oplus$ 0x0706050403020100 $S_3 \leftarrow S_3 \oplus \texttt{OxOFOEODOCOBOAO908},$

and the key addition at the end of finalization can be implemented as:

 $S_3 \leftarrow S_3 \oplus$ 0x0706050403020100 $S_4 \leftarrow S_4 \oplus \texttt{OxOFOEODOCOBOAO908}.$

756 **Appendix B. Determination of the Initial Values**

757 Each variant of the Ascon family has a 64-bit initial value constructed as

$$
IV = v \|0^8 \|a\|b\|t\|r/8\|0^{16},\tag{74}
$$

759 where

758

- 760 • v is a unique identifier for the algorithm (represented in 8 bits).
- 761 • a is the number of rounds during initialization and finalization (represented in 4 bits).

762 763 764 \bullet b is the number of rounds during the processing of AD, plaintext and ciphertext for AEAD, and the number of rounds during processing the message for hash, XOF and CXOF (represented in 4 bits).

- 765 766 \bullet t is 128 for Ascon-AEAD128, 256 for Ascon-Hash256 and is 0 for Ascon-XOF128 and Ascon-CXOF128 (represented in 16 bits).
- 767 768 • $r/8$ is the number of input bytes processed per invocation of the underlying permutation (represented in 8 bits).

769 770 The values of these parameters for each variant are given in Table [12,](#page-46-1) and initial values for each Ascon variant are specified in Table [13.](#page-46-2)

	η	a			r/8
Ascon variants	(8 bits)	(4 bits)	(4 bits)	(16 bits)	(8 bits)
Ascon-AEAD128		12		128	16
Ascon-Hash256		12	12	256	
$Ascon-X0F128$		12	12		
$Ascon-CX0F128$		12	17		

Table 12. Parameters for initial value construction

Table 13. Initial values as hexadecimal integers

