NIST Special Publication
NIST SP 1282

# Incentives, Infrastructure, and Research and Development Needs to Support a Strong Domestic Semiconductor Industry

*Summary of Responses to Request for Information*

This publication is available free of charge from:
https://doi.org/10.6028/NIST.SP.1282

August 2022


U.S. Department of Commerce
*Gina M. Raimondo, Secretary*

NIST NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY
U.S. DEPARTMENT OF COMMERCE

National Institute of Standards and Technology
*Laurie E. Locascio, NIST Director and Under Secretary of Commerce for Standards and Technology*

NIST SP 1282
August 2022





**Publication History**
Approved by the NIST Editorial Review Board on 2022-08-01

**How to Cite this NIST Technical Series Publication**
National Institute of Standards and Technology (2022) Incentives, Infrastructure, and Research and Development Needs to Support a Strong Domestic Semiconductor Industry: Summary of Responses to Request for Information. (Department of Commerce, Washington, D.C.), NIST Special Publication (SP) NIST SP 1282.
https://doi.org/10.6028/NIST.SP.1282

## Abstract

This report provides a summary of stakeholder responses to the Request for Information (RFI) titled "Incentives, Infrastructure, and Research and Development Needs To Support a Strong Domestic Semiconductor Industry," issued by the U.S. Department of Commerce, with the assistance of the National Institute of Standards and Technology (NIST).

## Keywords

Incentives; NSTC; NAPMP; Request for information (RFI); Semiconductors, Workforce development.

## Table of Contents



## List of Figures

## Organization of the Report

This document is organized around the different sections of the RFI: Semiconductor Financial Assistance Program, National Semiconductor Technology Center, Advanced Packaging Manufacturing Program, and Semiconductor Workforce. The first part of the document gives an executive summary of the report, followed by each section of the RFI, and a summary of responses to questions under those RFI sections.

## Analysis Methodology and Scope

The RFI analysis was performed by Energetics, Inc. with assistance from NIST staff. For the analysis, Energetics, Inc.:

- Developed a database that categorizes responses by RFI section, RFI question, respondent, and organization type.
- Where applicable, mapped comments from text of the responses to specific RFI questions.
- Input gathered during Department-held workshops and listening sessions were also mapped to applicable RFI sections.
- Summarized responses to each question and key recommendations for each of the four sections. Consensus among respondents by organization type was highlighted when found.
- Summarized broad themes and recommendations from all sections of the RFI.

For this summary analysis, Energetics, Inc. focused on RFI responses that provided information relevant to the design and implementation of CHIPS Act programs. While some responses included information on other topics, those topics are not part of this report.

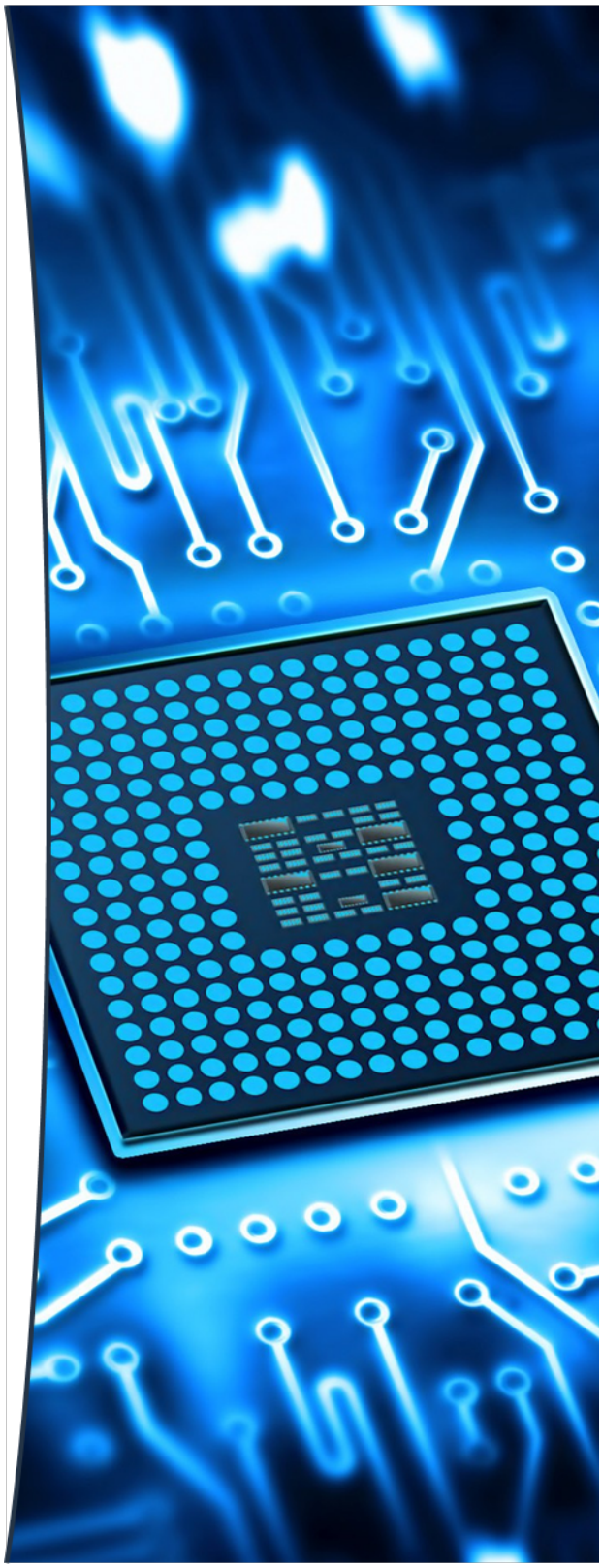
## Acknowledgments

Alex Liddle
Anita Balachandra
Robert Ivester
Robert Rudnitsky
Robin Materese
Sarah Henderson
Alex Roig Vitali
Erik Secula
Paul Hale
Kevin Jurrens
Tim McBride
Sanjay Rekhi
Sree Ramaswamy
Sam Marullo
Shyam Sunder
Marcus Schwaderer
Dave Seiler
Joseph Kline
Kevin Kimball
Tracy Retterer
Dorianna Andrade
Jennifer Nist
Henry Wixon
Regina Powers
Asha Mathew
Beth Grossman
Jim Kushmerick
Kristin Paulsen
Emmanuel Taylor
Kenta Shimizu
Hope Fato
Frank Gayle
Stephanie Shaw
Jason Boehm
Hannah Brown
Diane Sellers
Kristin Paulsen
David Gundlach
Michael Molnar
Jennifer Huergo
George Orji

## Executive Summary

To strengthen the U.S. position in semiconductor R&D and manufacturing, Congress authorized a set of programs in Title XCIX ("Creating Helpful Incentives to Produce Semiconductors for America") of the William M. (Mac) Thornberry National Defense Authorization Act (NDAA) for Fiscal Year 2021 (Pub. L. 116-283). This comprehensive set of programs is intended to restore U.S. leadership in semiconductor manufacturing by providing incentives and encouraging investment to expand manufacturing capacity for the most advanced semiconductor designs as well as those of more mature designs that are still in high demand. These programs would also grow the research and innovation ecosystem[1] for microelectronics, semiconductor R&D and semiconductor manufacturing in the U.S.

On January 24, 2022, the Department of Commerce (DOC or the Department), with the assistance of the National Institute of Standards and Technology (NIST), issued a Request for Information (RFI) seeking information from stakeholders to inform the planning and design of programs authorized under the Creating Helpful Incentives for the Production of Semiconductors (CHIPS) for America Act, if funded by Congress. The Department sought input on the potential set of programs in general and the following topics specifically: Semiconductor Financial Assistance Program, National Semiconductor Technology Center (NSTC), National Advanced Packaging Manufacturing Program (NAPMP), and Workforce Development Needs of the Industry. Comments were invited from all interested parties, domestic or foreign, including semiconductor manufacturers; industries associated with or that support the semiconductor industry, such as materials providers, equipment suppliers, manufacturers, and designers; trade associations; educational institutions; government entities; original equipment manufacturers; semiconductor buyers; semiconductor industry investors; and other stakeholders.



[1] Ecosystem as used in this report refers to everything needed to make and use all types of chips, from materials to consumer applications.

The Department received over 250 responses[2,3] from different sectors of the semiconductor supply chain, including design software developers, integrated device manufacturers, materials suppliers, equipment vendors, fabless companies, and automotive and industrials consumer companies. In alignment with the RFI, the Department hosted twenty-six workshops, and listening sessions with different parts of the semiconductor value chain. The input received during those events, and the ones received through regulations.gov and chips@nist.gov are used for this analysis. Responses include general recommendations and specific replies to one or more of the forty-one questions in the RFI. Figure 1 shows the distribution of responses to different sections of the RFI. Figure 2 shows the distribution of the respondents by organization type.

According to respondents, all parts of the CHIPS Act program should be closely coordinated for maximum impact. This includes collaboration and coordination between the NSTC and NAPMP, and with existing technology hubs and institutions. The financial assistance program, the NSTC and the NAPMP should be designed around state and local incentives to maximize initial impact.

Stakeholders identified intellectual property (IP) as an important factor in determining how they apply for financial incentives. They indicated that IP is a key factor in applying for financial assistance as part of a consortium and participating in the R&D programs or collaborative hubs. As such, IP guidelines should be structured carefully for both the financial assistance and R&D programs and must be explicitly stated upfront.

## Key messages from RFI Sections

## Financial Incentives

- The Commerce Department should support or fund a diverse set of technologies across node sizes, from leading edge to more mature technologies. Such an approach should extend beyond the initial scope of the awards or establishment of centers and hubs. Respondents noted that this makes for a cohesive program and is a lesson learned from similar foreign programs.
- Respondents support a consortium application structure and note that this arrangement would be mutually beneficial for participants if executed correctly.
- An applicant's foreign ownership should not disqualify them from applying for financial

[2] The views and opinions expressed herein do not necessarily state or reflect those of the U.S. Department of Commerce, the National Institute of Standards and Technology (NIST), and the United States Government. The contents of this report do not imply recommendation or endorsement by any part of the United States Government.
[3] Stakeholders" or "Respondents" are defined as RFI respondents who provided feedback on regulations.gov, chips@nist.gov or directly to NIST during public forums and stakeholder events.

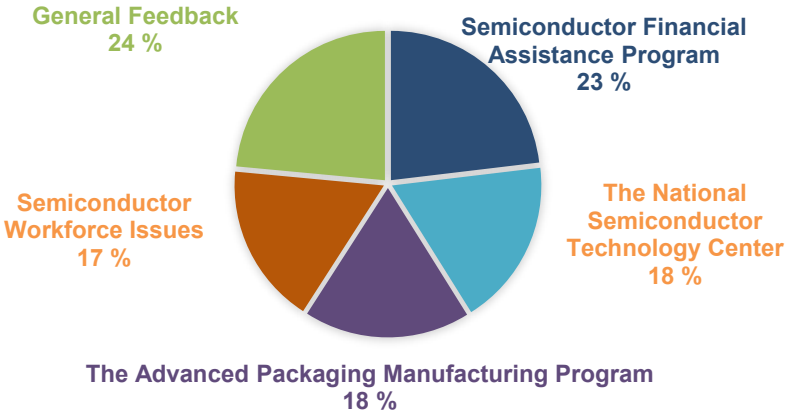



**Fig. 1**. Responses by RFI Section

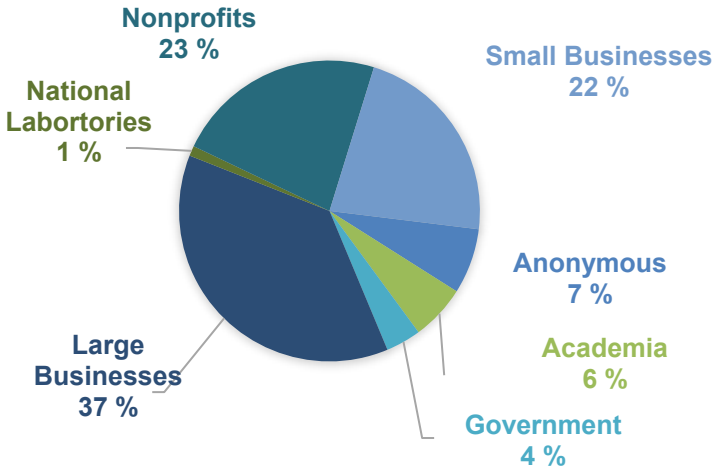



**Fig. 2**. Respondents by Organization Type[4]

incentives. The strength of an applicant's U.S. operations, and sustainability of their proposal are more important.

- The CHIPS Act incentives program should be designed to require cost-sharing, matching funding (with multiplier), and/or in-kind matching. Respondents strongly recommended coupling CHIPS Act funding with federal tax credits (Facilitating American-Built Semiconductors (FABS) Act) to maximize the impact on the domestic semiconductor ecosystem.

[4] Large businesses are classified as commercial organizations with more than 500 employees; Government include state and local governments and their economic development offices. Nonprofits are primarily professional societies, trade associations, and think-tanks.

### Research and Development Programs

- The NSTC and NAPMP should provide a full suite of flexible prototyping capabilities. This should include state-of-the-art (SOTA) equipment and tools that can be accessed by small and medium sized enterprises (SMEs) at cost-effective rates or with tiered membership access. According to respondents, the NSTC, NAPMP and their hubs should provide access to design, modeling, simulation tools, and training for such tools.
- The NSTC should be a neutral nonprofit entity. The governance structure should include a board of directors and technical advisory council with joint decision making from partners and stakeholders, with a hub-and-spoke organizational model.
- NAPMP funding efforts should be focused on chiplets, heterogeneous integration, and prototyping.

### Semiconductor Workforce

- Building a skilled workforce is important to all sectors of the semiconductor ecosystem. Respondents recommended increasing the pipeline of students in science, technology, engineering, and math (STEM) career paths and the semiconductor field specifically and improving partnerships and collaborations between training institutions and employers.
- The NSTC, NAPMP and all collaborators should have a strong workforce component and provide nationally recognized training and certification programs.
- In addition to the NAPMP's R&D focus, it is important to build a skilled workforce to support this sector. Increase access to foreign labor through immigration regulations that attract and retain foreign talent.

## Key Themes by Organization Type

### Large businesses

- Respondents from large businesses support adding a private capital multiplier requirement for the financial assistance program to maximize impact. They strongly recommended coupling it with tax incentives (specifically FABS Act) to encourage additional participation.
- In reviewing applications, the Department should give preference to manufacturers and suppliers that are currently operating in or have a strong history in the U.S., irrespective of the organization's foreign or domestic ownership. This is important since no country or region has end-to-end capabilities within the supply chain.
- Big business respondents also indicated that leading-edge nodes and compound semiconductor nodes (Silicon Carbide and Gallium Nitride, specifically) are key areas of focus needed to maintain future competitiveness, and where aligning facilities, equipment, and other capacity are critical.
- The financial assistance program separately or in coordination with the NSTC should adopt an open foundry model system. Such a system will help provide access to small and medium sized enterprises.

### Small Businesses

- Respondents from small businesses broadly support funding preferences for companies headquartered in the U.S.

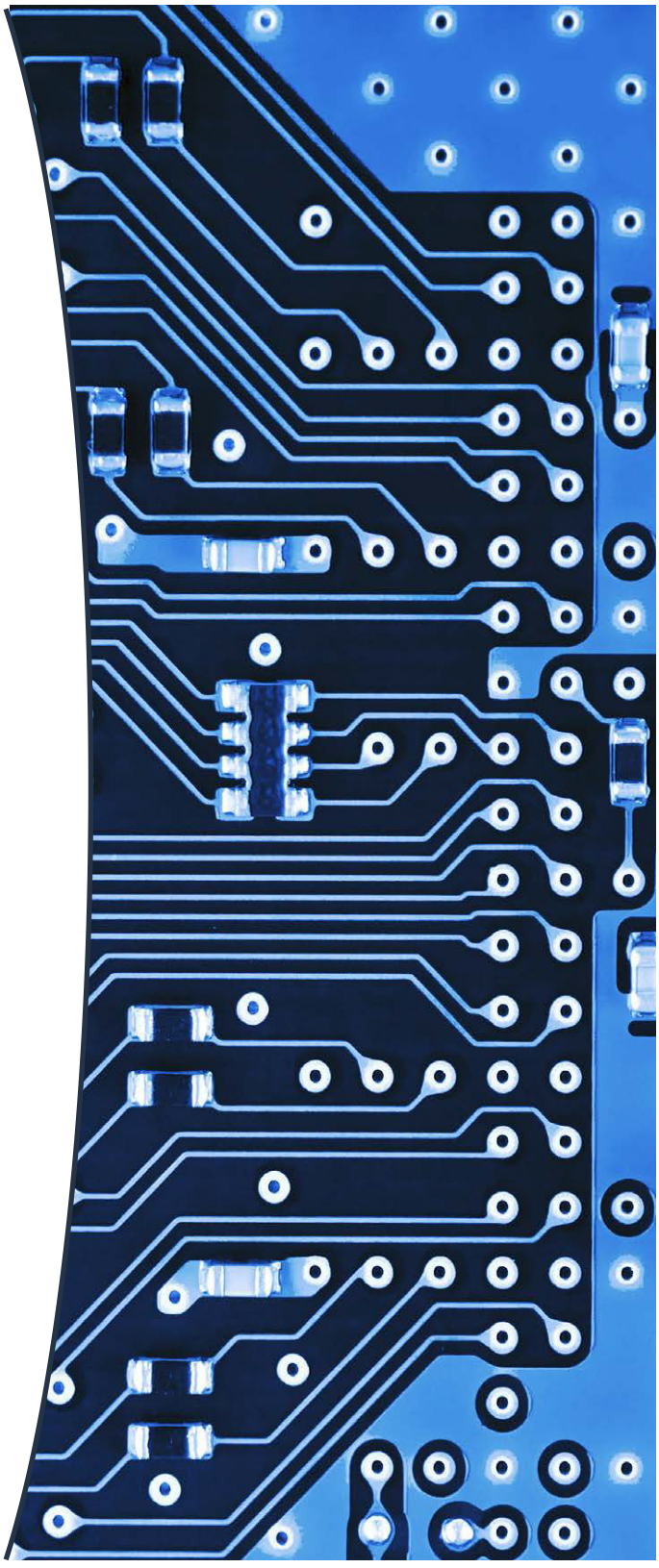
- They indicate that funding from the financial incentives program should be set aside for smaller grants to help spur innovation and competition.
- The NSTC and NAPMP should provide access to low-cost threshold design services, electronic design automation (EDA) services, and process design kit (PDK), and the training required to use these services.

### Nonprofit Organizations

- Respondents from nonprofit organizations, broadly recommended that the NSTC should be modeled as a hub-and-spoke to ensure that its resources are broadly accessible to the semiconductor R&D community. The spokes could be independent R&D centers, manufacturing foundries, and ecosystem service providers, run by either private or public ownership. These strategically located focal points would act as open access innovation clusters for SMEs and provide outcomes such as knowledge spillovers for areas where they are located.
- To ensure skilled worker shortages don't hinder companies from expanding, nonprofit respondents suggested increasing funding for semiconductor-sector-specific grant programs through the NSF Fellows program or the Manufacturing Engineering Education Grant (MEEG) program; or creating an incentive program for community colleges and universities to expand or improve computer science course offerings and trainings.

The programs authorized by the CHIPS for America Act provide a one-of-a-kind opportunity to expand our domestic manufacturing capacity, help grow the research and innovation ecosystem for microelectronics and semiconductors in the U.S. and restore U.S. leadership in semiconductor manufacturing. The responses received in this RFI highlight the needs and recommendations of the semiconductor ecosystem and will inform the design and implementation of the CHIPS Act programs. The Department of Commerce is fully committed to ensuring the successful implementation of these programs.

## 1. Semiconductor Financial Assistance Program



The Semiconductor Financial Assistance Program section of the RFI sought input on how the incentive program, under Section 9902 of the William M. (Mac) Thornberry National Defense Authorization Act for Fiscal Year 2021 (Pub. L. 116-283) (NDAA), if funded by Congress, should be designed. Figure 3 shows the distribution of respondents to questions in this section.

Respondents supported the consortium application structure, especially one with a vertically aligned consortium structure along a particular node size or material class. According to respondents, such an arrangement would be mutually beneficial for all participants if executed correctly. Within a consortium application structure, respondents identified intellectual property as the most important factor they would consider when teaming with other organizations. Respondents felt that these consortia would take up to a year to establish due to negotiations about covered entities, structure, liability, and other legal issues. However, many respondents indicated they were currently aligned with or planning to apply as part of an existing consortium. To ensure clarity and transparency, respondents recommend that DOC issue rules and guidance on the application process as soon as possible.

When reviewing applications for funding, respondents felt that DOC should carefully consider the foreign or domestic ownership of the applicant. Most respondents felt that preference should be given to manufacturers or suppliers currently operating in, or with a strong history of operating in, the U.S., irrespective of the organization's ownership. This sentiment was especially true for respondents from large businesses. According to respondents, the long-term sustainability of the business model and the

experience of the recipient should be weighted equally to reduce the organization's reliance on public funding.

Respondents were in favor of required cost-sharing, matching funds (with multiplier), and/or in-kind matching, and coupling CHIPS Act funding with federal tax credits (FABS Act) to maximize the impact on the semiconductor ecosystem.

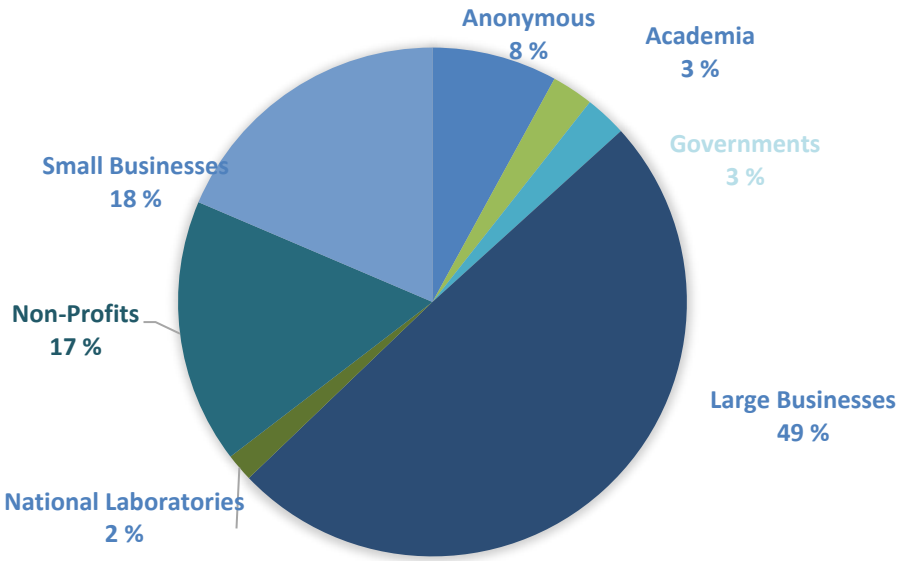



**Fig. 3.** Respondents to questions in the Semiconductor Financial Assistance Program section of the RFI

### 1.1. The term "semiconductor" is not specifically defined in Section 9902 of the NDAA; rather, the legislation leaves it to the Secretary of Commerce to define. What factors do you consider important in developing a definition of "semiconductor" for purposes of a semiconductor manufacturing incentives program?

According to respondents, the definition should be broad and encompass the entire ecosystem.

### 1.2. Section 9902 permits a "consortium" of public and private entities to apply for funding. What factors would public and private entities consider determining whether to apply for funding as part of consortium? How would private entities determine whether to work with a public entity as part of a consortium? How would a private entity consider working with other private entities (such as customers, equipment manufacturers, or capital providers) as part of a consortium?

According to respondents, IP is the most important factor that private entities will consider when determining whether to apply for funding as part of a consortium. Such a consortium would need

proper governing guidelines that all participating entities consider fair and acceptable. This includes retention rights of co-developed IP and protection of existing IP.

In addition, respondents highlighted that the consortium should have R&D objectives that are mutually beneficial for all, a viable technology roadmap with a meaningful financial return on investment, and access by consortium members to required equipment or facilities. Most comments preferred a vertically aligned structure where private entities produce different components for the value chain. According to respondents, such a structure would provide long-term, strategic supply-chain security and a pathway to access next generation technology not otherwise available.

Before applying for funding, a company would want to understand the conditions and obligations placed on it if funding is made available. Many respondents highlighted their membership within existing successful semiconductor consortia with public-private sector partners (e.g., a semiconductor manufacturing foundry for automotive, industrial, defense, and critical infrastructure applications).

### 1.3. Based on the criteria outlined in Section 9902 of the NDAA, what types of facilities, equipment, and other capacity aligned with the manufacture of semiconductors do you see as being most critical to the interests of the United States?

The overwhelming majority of respondents noted that the full supply chain needs to be aligned, and that alignments should be by node size and material. However, they identified packaging and outsourced semiconductor assembly and test (OSAT) as key missing pieces of this supply chain within the U.S.

Large businesses specifically highlighted the need for alignment of leading-edge node facilities. Many noted the U.S.'s strength in leading-edge chip and material design but a complete absence of a corresponding supply chain. For leading-edge nodes (DRAM and logic), process technology R&D investments were identified as critical to enabling the development of cutting-edge product applications involving artificial intelligence and machine learning, 5G, and autonomous vehicles.

Respondents from all organization types noted that if investments in manufacturing leading-edge nodes and legacy nodes were equivalent, the return on investment (ROI) for legacy nodes would be higher due to the current growing demand and broader capacity in RF, analog, mixed-signal, high voltage, and photonics applications. It was also noted that the transportation and defense sectors have the most immediate need for legacy node manufacturing.

Large businesses also highlighted the need for wide bandgap semiconductors. SiC and GaN were called out most often. Scalable end-to-end compound semiconductor manufacturing facilities with advanced, flexible tooling were thought to enable the broadest array of semiconductors like InP, GaAs, GaSb, GaN, and $Ga_2O_3$ for applications in 5G/6G wireless, broadband rural/urban access, data centers, and emerging augmented reality and virtual reality (AR/VR) products. Several respondents noted that fabrication facilities for such materials do not require ultra-small geometries, and processing can often rely on older-generation of silicon fabrication tools that are refurbished and modified for use with compound semiconductor wafers. Therefore, capacity expansion of existing III-V fabs was seen as more cost effective to develop and commercially operate in the U.S.

A common theme for both leading-edge and mature nodes was the need for advanced processing equipment required by all facilities within the supply chain. Many respondents highlighted the

difficulty of acquiring advanced processing equipment required for foundry and packaging facilities. A specific equipment challenge mentioned across all nodes and materials was by far lithography equipment, which has no domestic manufacturer. Also mentioned were steppers, etchers, and bonders for chip-to-wafer and wafer-to-wafer bonding.

### 1.4. Based on the criteria outlined in Section 9902 of the NDAA, what do you see as presenting the biggest challenges for an organization to develop an application for funding as part of a consortium, and how long do you estimate it would take for an organization to prepare the required materials?

Respondents felt that the effort required to develop an application depended on 1) if the organization was already part of an existing team or consortium, 2) if the company planned to apply individually, or 3) if the organization must partner, negotiate, and establish a team or consortium framework first. Respondents felt that the timeframe for the first two situations was on the order of 2 to 4 months. For the latter situation, where the consortium or team must be established, the timeframe could be up to a year.

Factors that would slow the application process specifically for those forming a consortium are organizational, alignment on IP sharing requirements, agreeing on governance and operations models, legal composition (501C, other?), and establishing liability.

Recommendations for expediting the application process were to have more transparency and clarity on the proportion of federal funding for CHIPS Act investments as soon as possible regarding 1) the types of funding mechanisms available, 2) the types of projects and infrastructure each can fund, and 3) the guidelines for what must be met to access those funds.

### 1.5. Subject to the criteria and eligibility requirements outlined in Section 9902 of the NDAA, what other factors should the Secretary consider as important when reviewing applications for Federal financial assistance?

According to respondents, the Secretary should consider on-shore/off-shore ownership of the company, the long-term sustainability of the business model, and the experience of the recipient when reviewing applications for Federal financial assistance.

Foreign or domestic ownership of the applying company should be a key factor for consideration. Most respondents indicated that preference should be given to manufactures/suppliers that currently operate in the U.S. or have a strong history of it, irrespective of the organization's ownership. Respondents representing large businesses felt this should be an important factor and that DOC should not discount applicants with headquarters outside the U.S. A smaller portion of respondents representing a mix of small businesses and non-profit organizations (although not exclusively) said that preference should be given to U.S. headquartered companies, with a few citing IP security concerns.

Another factor was the long-term viability of the business plan. Respondents felt that proposals should have a viable plan to sustain the facility beyond the initial incentives period. Other factors include the company's history of success in the semiconductor manufacturing sector — the recipient must have significant experience and expertise in semiconductor manufacturing to develop and innovate onshore; the speed at which a proposal can be implemented; and the impact that the effort would have on job creation and local workforce development.

### 1.6. Section 9902 defines a covered entity to include, among other things public-private consortia, which could include partnerships between semiconductor firms and customers, suppliers, investors, state and local governments, federally funded research and development centers (FFRDCs), and other entities. How can Section 9902 incentives be designed and deployed to encourage additional and new private capital investment in the semiconductor ecosystem? What can be learned from other technology infrastructure development programs that use such partnerships (e.g., data center facilities or communications infrastructure) that may be applicable to semiconductor facilities?

The primary recommendation from respondents for the design and deployment of financial incentives that maximize private capital are requiring cost sharing, matching funds, and/or in-kind matching as appropriate and feasible. Several respondents suggested requiring a private capital multiplier for every taxpayer dollar spent. This recommendation was mostly from large businesses, who also suggested that providing tax credits or similar financial benefits for capital investments would attract private funding. Respondents from academia and small businesses suggested holding some funds back for smaller grants to spur innovation and competition.

Recommendations on how to attract venture capital funding include structuring a consortium to provide some experimental, model shop, or pilot production facility for smaller companies to advertise new innovative ideas.

Another recommendation is to design/structure the incentive program around state and local incentives and policies. Examples could be existing technology hubs or state-based incentives (e.g., job training programs, tax breaks, state investments). By coupling such programs and incentives, the risk for private investment may be reduced.

Examples of similar programs were the U.S. Small Business Administration's (SBA) risk sharing programs, NASA's Commercial Orbital Transportation Services program, the Department of Defense's Rapid Assured Microelectronics Prototypes – Commercial (RAMP-C) program, and the Human Genome Project. Examples of organizations that have successfully cultivated public private partnerships (PPP) were SEMATECH, Semiconductor Research Corporation (SRC), Interuniversity Microelectronics Centre (imec), and the Manufacturing USA Institutes.

### 1.7. How can federal financial assistance, consortia, or public-private partnerships be structured to maximize the initial scale of projects and to ensure ongoing reinvestment in project expansions, tool upgrades, and productivity improvements for the projects to remain economically viable and competitive over time? What opportunities exist for manufacturers to partner with private capital providers or use project financing to maximize the impact of the Federal financial assistance awards to achieve these objectives?

According to respondents, CHIPS Act funding (financial incentives and investments in research and development) should be coupled with investment tax credits (specifically FABS Act) for maximum impact. A large number of respondents from large businesses and non-profits noted the original bipartisan CHIPS for America Act, which included tax credits. Several respondents noted that CHIPS funding and the tax credits are parts of a complementary, holistic strategy, and both are needed to produce robust, predictable, and durable incentives to restore U.S. semiconductor leadership.

In addition, respondents emphasized the need to maximize the initial impact of investments quickly through modernizing and expanding the capacity of existing fab facilities. These existing facilities already have an experienced team, existing customers, processes, infrastructure etc. and

as such, should be more likely to sustain economic viability. This quote from a respondent exemplifies the input received on this question: "… *there are many 200 mm fabs throughout the U.S. with experienced teams, existing customers, processes, infrastructure etc. These companies cannot access leading edge technology because the toolsets do not exist for 200 mm facilities. Technologies that bring advanced node capability to these older facilities would be a significant advance for the U.S. semiconductor industry."*

### 1.8. How can Federal funds incentivize the creation of a broad semiconductor ecosystem that includes producers of semiconductor manufacturing equipment and other upstream suppliers? What are the largest supply imbalances with respect to manufacturing equipment, tools, materials, and chemicals that need to be addressed by U.S. investment?

See response summary for 1.9

### 1.9. How can the program ensure that semiconductor startups and small and midsized companies have access to commercial fabrication, assembly, testing and packaging facilities and associated technical expertise, including intellectual property products such as "Process Design Kits"?

Responses from small businesses primarily indicated that their needs would be best addressed through the NSTC and NAPMP by creating wafer fabrication services (shuttles), providing low-cost threshold design services, centralized EDA and access to PDK and training. A tiered access model was suggested by several. However, respondents from large businesses indicated that PDKs and design IP blocks are common to all fabs, and their access is not a problem for small and medium sized enterprises (SMEs).

Respondents from large businesses overwhelmingly supported requiring funding recipients to adopt an open foundry model to provide access to SMEs. The funding could be made contingent upon covered entities having startup and user programs, dedicated multi-project wafer (MPW) starts, allocated resources, and cleanroom space. A few recommended a voucher system to subsidize the use of open foundries for small businesses and startups. One common problem highlighted by respondents was that open foundries often de-prioritize SME orders which further puts them at a disadvantage to compete in the open market. To solve this, multiple respondents recommended encouraging/requiring open foundries to dedicate a percentage of fabrication, assembly, testing, and packaging capacity toward SME, up to a determined monthly volume or revenue.

A common barrier for startups to access manufacturing facilities is the requirement for their novel materials and processes to be compatible with existing mass production processes. Commercial foundries are not set up to perform non-standard process development to adopt and qualify novel processes on their well-tuned manufacturing equipment. Startups, at their end, can't justify investing in expensive capital equipment to try one-off experiments for optimizing their proof-of-concept devices toward large scale manufacturability. Therefore, service providers that offer microfabrication prototyping and process development support to multiple startups and small companies are vital for bridging this "lab to fab gap." The financial assistance program can include provisions that enable such service providers to apply for co-investment funds to support equipment purchases or upgrades in return for making the resultant capability accessible to qualified participants.

### 1.10. Under the law, the Secretary may consider whether a covered entity includes a small business concern as defined under Section 3 of the Small Business Act (15 U.S.C. 632). Would it be beneficial for the Department to encourage large entities to partner with medium and small business suppliers?

Respondents stated that encouraging large entities to partner with small and medium sized suppliers would be mutually beneficial and could broaden the semiconductor ecosystem. The enhanced innovation that small businesses bring would complement the market insight, program management, and prototyping assistance inherent in large businesses.

### 1.11. Section 9902 requires a covered entity to make commitments to invest in workers and communities, including through training and education benefits and programs to expand employment opportunity for economically disadvantaged individuals. What constitutes a baseline commitment to worker training in the semiconductor industry and what other workforce investments should be considered? Are there international best practices or cooperation upon which your company finds beneficial? What other community investments should be considered beyond worker training and employment opportunities? How can worker training, other workforce commitments, and other community commitments be maximized and how should program participants be held accountable to their commitments? What types of programs exist, or could be expanded, to improve access for economically disadvantaged individuals to these workforce and community commitments and opportunities?

Respondents to this question recommend the following sets of actions:

- Increase the use of hands-on learning through internships, mentorships, apprenticeships, and co-op programs.
- Ensure that workforce development programs collaborate and form long-term partnerships with local institutes of higher education to help boost the talent pool, and supply engineers and technicians through offering directly applicable trainings such as internships.
- Develop and use portable curricula (such as study modules) that could be shared broadly among institutions. This would provide a cheaper option to trade schools and city colleges and could help attract economically disadvantaged individuals to opportunities, but outside support is needed for the necessary facilities. Some respondents mentioned they had success offering tuition reimbursements to further this goal.
- Support STEM education at the K-12 level. This includes supporting curricula development to grow semiconductor industry skills, and providing training and certification programs. This will help attract people into the industry and support general education, diversity, and inclusion.
- Give preference to funding proposals that show a commitment to establishing hiring and training relationships with local colleges and investing in economically depressed areas.

### 1.12. Section 9902 requires a covered entity to have secured commitments from regional educational and training entities and institutions of higher learning to provide workforce training to be eligible for funding. Looking at the semiconductor sector broadly, what are the greatest workforce development needs, and how can Federal financial assistance meet those needs? What specific types of workforce training programs would be the most beneficial to companies in these sectors? What existing workforce training programs have proven effective and should be expanded, including international exchanges or best practices? How could a program best ensure that workforce training and development meet critical national needs?

According to respondents, increased efforts should be made to retain foreign students after they graduate from U.S. universities. This includes reforming green card policies so students with semiconductor related graduate degrees are eligible for a national interest waiver, fast tracking them to green card and citizenship status. Other suggestions include giving employment preference to U.S. citizens.

Several respondents cited the Department of Defense's Scalable Asymmetric Lifecycle Engagement (SCALE) as an example of a successful workforce training program. Other examples were efforts by the SEMI Career and Apprenticeship Network (SCAN) to expand the semiconductor talent pipeline, and the American Semiconductor Academy to assist the industry in creating greater academic depth and breadth in semiconductor-specific subjects.

Respondents identified workforce gaps in manufacturing operations, equipment and tooling services, hardware and packaging engineering, industrial and quality engineering, and system and silicon design, stemming from challenges in retention of laborers skilled in these fields. Proposed solutions include federal financial assistance to incentivize more domestic capacity onshore, funds to create demand (and then the talent will follow), and having programs aimed at increasing the retention rate.

### 1.13. What is the industry's environmental footprint in terms of its land and resource use, air quality and water quality impact, hazardous or other special-handling material needs, and greenhouse gas emissions impact? What is the industry currently planning or implementing on these dimensions and how will the environmental footprint likely change over the next decade as a result? What effect will semiconductor chip customers' "net zero" announcements or other related incentives have on the industry's environmental footprint? What opportunities exist for the industry to move to a smaller and more sustainable footprint, and how can such opportunities be used to create a stronger domestic market for chips produced with a smaller footprint?

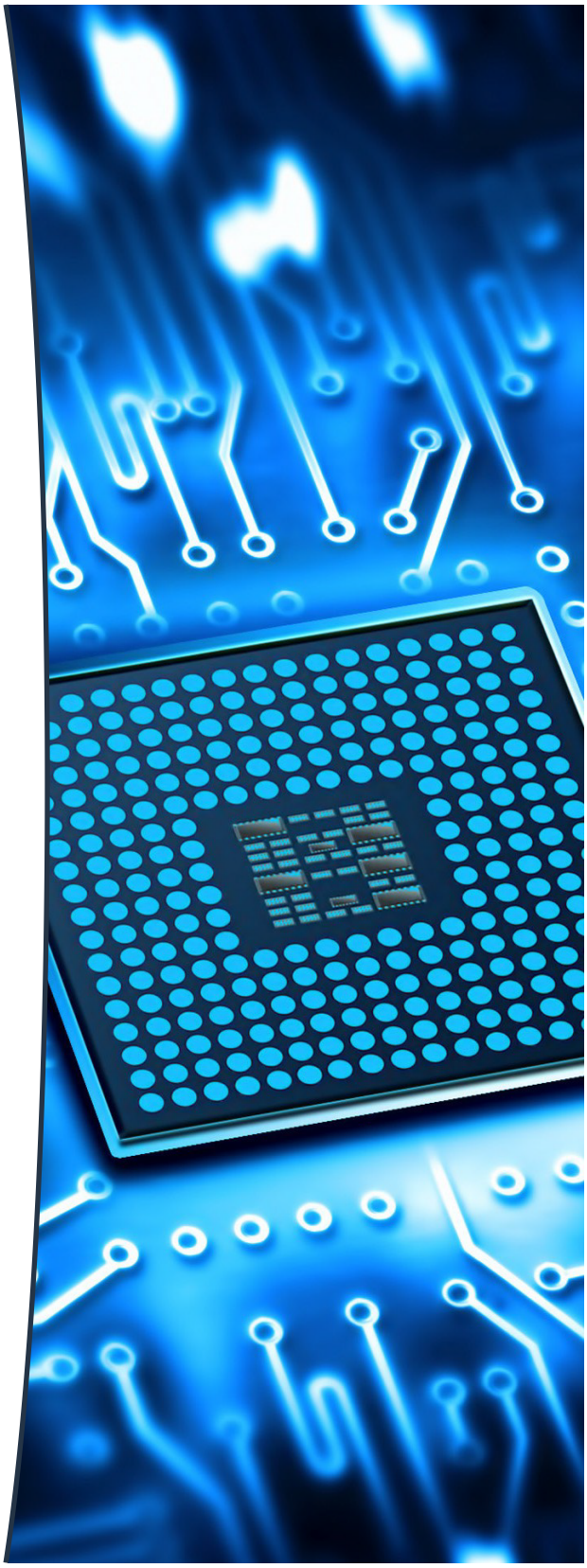
Many respondents are currently implementing effective water reclamation methods to reuse treated wastewater with wet scrubber abatement systems and transitioning from conventional energy to renewable energy sources to decrease greenhouse gas emissions. Several respondents plan to use CHIPS Act funding to implement the use of alternative process materials to reduce their environmental footprint through the reduction of greenhouse gas emissions.

Industry respondents state that net zero announcements will require more sustainable manufacturing methods to reduce footprint such as the use of renewable energy and high-tech control technology to promote efficient operations and energy optimization.

Existing opportunities to reduce industry footprint highlighted by respondents focused heavily on greenhouse gas emission reductions and wastewater treatment. For greenhouse gas emission reductions, suggestions include the use of hydrofluorocarbons (HFCs) and hydrofluoroethers (HFEs) over perfluorinated compounds (PFCs), which are currently used during the etching process. For wastewater treatment, the use of an enzymatic solution to replace sodium bisulfite and sodium hydroxide during the etching/cleaning process serves as an opportunity to eliminate additional treatments needed to remove high levels of total dissolved solids in wastewater. The implementation of an enzymatic solution reduces wastewater treatment costs by reducing additional steps, and drives down costs associated with hazardous chemical handling from conventional etching/cleaning agents. Such opportunities create a stronger domestic market by reducing manufacturing costs compared with conventional methods.

## 2. National Semiconductor Technology Center

Under Section 9906 (c) of the NDAA, the National Semiconductor Technology Center (NSTC) is authorized to conduct advanced semiconductor manufacturing R&D and prototyping; establish an investment fund; and promote and expand workforce training and development opportunities. Figure 4 shows the distribution of respondents to questions in this section.



Overall, respondents support the idea of an NSTC, and see it as a collaborative research environment that should be based on a hub-and-spoke model, where they can access funding for "valley-of-death stage projects," and leading-edge tools. The NSTC is also seen as a place with a comprehensive and industry-focused IP framework and the ability to develop a long-term roadmap(s) to guide future research and investments. They suggest it should be run as a neutral non-profit entity that includes a board of directors and technical advisory council with joint decision making from partners and stakeholders.

Respondents stressed that the NSTC should collaborate with or incorporate existing programs and roadmaps such as those championed by DARPA, the National Nanotechnology Coordinated Infrastructure (NNCI), the Semiconductor Research Corporation (SRC), and IEEE, and should work closely with the National Network for Semiconductor R&D.

Respondents noted that the NSTC's potential ability to broaden and increase one's technical capabilities could be an asset in attracting talent. Most respondents were in favor of targeting early-stage investments, as those are normally the hardest to develop and acquire funding for. Finally, almost all respondents agreed that some collaborative work with imec and CEA-Leti could be mutually beneficial.

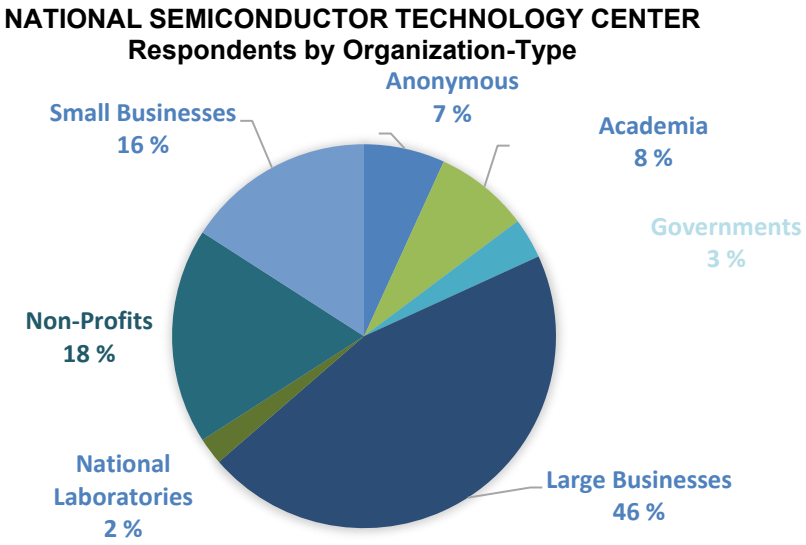



**Fig. 4.** Respondents to questions in the NSTC section of the RFI

**2.1. Based on the functions outlined in section 9906(c) of the NDAA the Department's current vision of the NSTC is as a hub (or multiple hubs) of talent, knowledge, investment, equipment, and toolsets that tackles Moore's Law transitions, post-CMOS research into new materials, architectures, processes, devices, and applications, and that bridges the gap between R&D and commercialization. What attributes are most important for the NSTC to possess or provide to the community (e.g., ease of access, a broad suite of leading edge tools managed as central facility, a collaborative research environment)? What key factors are critical for the NSTC to address the current gaps in the semiconductor R&D ecosystem?**

A collaborative research environment was cited by respondents from academia, industry, and government as the most important attribute for the NSTC to have in order to foster continued advances for the U.S. semiconductor industry. Increased coordination among these stakeholders will help maximize resources and minimize duplication, by linking multiple technology disciplines. According to respondents, the NSTC should develop metrics to measure program success and communicate to stakeholders through roadmaps, newsletters, workshops, conferences, open access days and other forms of outreach and dissemination. The hub-and-spoke model could be a suitable implementation approach, where each hub has a specific focus. In addition, existing U.S. facilities should be leveraged as possible hub locations. The use of existing facilities can encourage networking and the development of innovation clusters, and reduce time and investment needed for impact.

Many respondents stated that the NSTC should increase ease and affordability of access to necessary facilities and tools, potentially providing low-cost access to a broad suite of leading-edge tools and a common library of key process modules and design IP. Some examples of what the NSTC could offer include access to prototyping and fabrication facilities; workforce development gaps/programs such as student training and internship opportunities; advanced metrology methods, imaging tools, defect inspection technologies, and their standardization.

Since one of the biggest challenges in product development is crossing the "valley-of-death" from R&D to commercialization, many respondents state that funding and resources should be focused on lab-to-fab transition to increase the pace of innovation and commercialization. There should be support for research needs across the "full-stack" of innovation to help overcome this "valley-of-death." Some respondents want funding to be directed specifically toward start-ups to help de-risk and attract investors, and also toward breakthrough challenges, revolutionary advances, disruptive technologies, and longer-term R&D.

### 2.2. As authorized, the NSTC would have to be able to work with a wide range of research groups from industry, academia, and government, some of whom will be contributing valuable intellectual property. What approaches to intellectual property should be in place to protect the foundational contributions of members while enabling maximum collaboration and innovation amongst the research community supported by NSTC? What IP issues create unique challenges for middle- and late-stage prototyping collaborations versus early-stage research, design, and proof-of-concept collaborations?

Overall, respondents noted that the NSTC needs to balance its role as a public entity with a mission of ensuring innovation in U.S. industry. As such, most respondents agree that IP that is developed individually should be individually owned, while IP developed jointly should be jointly owned. The NSTC should retain rights only when IP is developed jointly with facility staff. Some respondents suggest using other strategies such as blueprints for an IP strategy (such as imec or the DARPA toolbox initiative). Many respondents specifically mentioned that background IP (BIP), brought to the facility by a participant is the participant's property, but participants must disclose all pertinent BIP.

Recommendations on how the NSTC should handle IP include providing clear guidelines and a comprehensive framework and sharing these as soon as possible. Such a framework must outline IP mechanisms and decision-making processes based on the intended use of the IP. Other suggestions include creating a dedicated organization within the NSTC to manage IP; creating an entity to acquire licenses to critical core IPs to make available to startups at little to no cost; a tiered membership structure where IP use is proportionate to membership contribution; creating security guidelines for handling IP; and making use of non-disclosure agreements (NDAs).

Late-stage prototyping may contain more sensitive information, and as such, the IP issues require additional efforts and expertise.

### 2.3. The federal government has several programs that support microelectronics and associated R&D across many agencies, federal labs, university labs, corporate labs, and other for-profit and nonprofit entities. What existing domestic R&D activities, assets, intellectual property, knowledge, and expertise should be incorporated or otherwise connected to the NSTC, and are any international in nature? How should the NSTC interface with federal labs, university labs, corporate labs and other existing institutions of R&D and prototyping to ensure that R&D projects are supported throughout the technology maturation process so that public research funds are able to improve R&D productivity and attract additional private and venture investment?

According to respondents, existing U.S. government R&D programs that should be connected to the NSTC include DARPA (specifically, ERI and JUMP), NNCI's existing network and user facilities, and NIST user facilities (specifically the Center for Nanoscale Science and Technology

and the Center for Neutron Research). In addition, the NSTC should connect with relevant programs at NSF, Federally Funded Research and Development Centers (FFRDCs), Department of Energy National Labs, the Army Research Lab, Air Force Research Lab, and NIST. Activities at some of these entities could serve as possible models for the NSTC. Most respondents noted that international collaborations with entities such as imec in Belgium and CEA-Leti in France, would be beneficial to the NSTC. They also stressed that strong coordination among all existing institutions and programs and the use of existing research locations and networks are important to maximize innovation and minimize duplication.

The NSTC should interface with existing institutions by focusing on prototyping, taking foundational, low technology readiness level (TRL) research from labs and commercializing it, thus, helping technologies cross the "valley-of-death." In such a role, the NSTC can help assess technology and funding needs, de-risk technologies for investors, and help catalogue existing capabilities and R&D activities.

### 2.4. How should the NSTC connect to National Network for Semiconductor R&D, authorized by Sec. 9903 of the FY 2021 NDAA? What considerations should be given to ensure strong integration between the two efforts? Should there be overlap in the technology readiness levels served by each program?

Most respondents state that the NSTC and the National Network for Semiconductor R&D (NNSRD) programs should be closely connected. Although the focus of the two entities may be different (NSTC on industry and NNSRD on national security), early-stage technologies developed within the NNSRD can be further developed at the NSTC. This will ensure that the work is complementary with no or minimal duplication of efforts. The NSTC and NNSRD should identify dual-use technologies and share common IP when possible.

In general, respondents indicated that the NNSRD should focus on lower TRLs, (1 to 3), while the NSTC should focus on higher TRLs. Almost all respondents who addressed the TRL level question agree that overlap may be useful, if not necessary, between the programs in order to have a seamless transition of technologies between the two.

### 2.5. How should the NSTC ensure that it can identify and invest in what comes next after the first wave of needs are identified in the initial years? To what extent does the semiconductor ecosystem need a long-term roadmap of application requirements, technical needs, and gaps in materials, tooling and equipment, and process capabilities in order to guide future R&D investments? How can the NSTC's investments best support an open roadmap of this type, and how should the NSTC interface with other governments or allied international R&D programs, such as those established under Section 9905 of the FY2021 NDAA, to enable such a roadmap? What existing technology forums, roadmaps, or other initiatives should be incorporated into such efforts?

To ensure it identifies and invests in what comes after the first wave of needs, respondents recommended that the NSTC should invest in breakthrough ideas and challenges. A technical advisory committee with a diverse set of perspectives should be created with representation from leading industries to vet proposed projects.

Some respondents felt the NSTC should rely primarily on industry and to some extent academia for input to guide investments. Overall, activities and investments should be aligned with current trends and priority research areas, which could be based on longer-term roadmaps. Although respondents agreed that roadmaps are important, some wanted the NSTC to lead and coordinate

the development of the roadmap, while others wanted the NSTC to consolidate and inform existing roadmaps.

Roadmaps cited by respondents as being relevant include the IEEE International Roadmap for Devices and Systems, IEEE Heterogenous Integration Roadmap, SRC's Decadal Plan for Semiconductors, and DoD's National Network for Microelectronics R&D.

### 2.6. The NSTC is envisioned as a public-private partnership. What are the most suitable models of public-private partnership for the R&D and prototyping gaps that the NSTC is envisioned to address? What are the roles of the public participants and the private-sector participants in this partnership, including any international participants? How should governance structures, program objectives, investment criteria, and oversight and accountability requirements be structured to maximize the transformative potential of the NSTC in the U.S. R&D ecosystem?

According to respondents, the NSTC should focus on a clear national objective with a laid-out technology roadmap, and then look at collaboration models developed by entities such as NY Creates, imec, Manufacturing USA, SRC, U.S. Transportation network, Cantena-X (based on GAIA-X), FFRDCs, SEMATECH, Tyndall National Institute, RAMP-C, and AIM photonics.

The role of public participants should be to run a competitive bidding process, aggregate downstream demand for upstream capital-intensive infrastructure and foundry services, contribute to broadly applicable technology advancements, acquire prototyping capabilities, and coordinate economic and workforce development. Private sector participants' roles should be to provide strategic insight on commercial and competitive factors, business processes, technologies, infrastructure, investments, and talent. International participants can bridge valuable gaps in onshore capacities.

Many respondents recommended the NSTC should be run by a neutral nonprofit entity with a broadly representative governance, including a board of directors representing both small and large stakeholders and the greater ecosystem (e.g., including government, academia, private sector, national labs, FFRDCs, international participants), a technical advisory council, and rotating leadership. Decision-making at the highest level should be done jointly by partners and the U.S. government. Full participation should be available to all global industry members.

### 2.7. What operational and organizational characteristics, business processes, and practices will be important in ensuring that the resources of the NSTC are broadly accessible and available to the broader U.S. semiconductor R&D community including both small and larger, more established entities? How can the NSTC ensure that smaller and medium-sized companies and startups have access to facilities, expertise, and intellectual property that public funds support?

According to respondents, the NSTC should have a clear and diverse governance structure with a mix of public, private, and academic representatives. A board of directors and a technical advisory board with subject matter experts were recommended to advise and make decisions on larger program goals. In collaboration with industry leaders, governance can set a clear operational structure with open mission statements that focus on domestic long-term sustainable research projects and fostering partnerships with stakeholders.

A hub-and-spoke model was recommended as a way to engender broader participation by smaller companies. Spokes could be independent R&D centers, manufacturing foundries, and ecosystem

service providers, run by either private or public entities. These strategically located focal points would act as open access innovation clusters, with SMEs benefiting from outcomes such as knowledge spillovers.

Additional recommendations include defining IP guidelines and establishing a business unit to handle IP issues. Some respondents believe the NSTC should acquire an initial pool of IP and 'democratize' it. This way, IP can be leveraged by universities, start-ups, and small businesses to develop new technology that they could then license and use in raising capital from investors.

To ensure the NSTC is universally accessible and available, respondents recommended ensuring that the organization's activities and funding opportunities are clearly communicated to stakeholders in all parts of the ecosystem. To encourage participation by SMEs, funding should be allocated to address the needs of SMEs.

### 2.8. For those who currently participate or have participated in a "research consortium" (either domestic or international) made up of public and private partners, what are the important lessons learned or best practices that the NSTC should follow?

Respondents who currently participate or have participated in a "research consortium" had the following recommendations:

- Study other consortia to identify what works or didn't work. Key examples are imec and SEMATECH.
- Make sure the structure is compatible with the goals of the organization.
- Ensure that the NSTC has continued long-term funding. Although some consortia have solid revenue streams, most are not self-sustaining.
- Ensure that the governance structure and roles, IP rules, access, expectations, and long-term technical vision are compatible and transparent.
- The decision-making process should include industry, academia, and government.

### 2.9. What attributes or capabilities of the NSTC would make it attractive and beneficial for companies, universities, and other agencies to want to send employees for assignments at the NSTC? What types of research and training opportunities should be made available at the NSTC for students and early career staff?

According to respondents, the following attributes or capabilities would make the NSTC attractive and beneficial to stakeholders:

- The prospect of solving challenging problems in a collaborative interdisciplinary research environment with a broad range of expertise and experts.
- The presence of state-of-the-art facilities and exposure to new technologies.
- The presence of NSTC sponsored workforce training and certification programs.
- The availability of flexible or part-time assignments.
- The presence of specific programs focused on helping underserved populations.
- The availability of apprenticeships, internships, and fellowships.

### 2.10. For organizations that currently utilize an external semiconductor "fab" as part of their R&D efforts, what services or processes are currently missing in the U.S. ecosystem that the NSTC should provide? Are there specific toolsets that the NSTC should own and operate or provide access to?

One of the major services currently missing in the U.S. ecosystem that respondents identified for the NSTC to provide are full prototyping lines with state-of-the-art tools, including sufficient parallel paths, to ensure predictable and competitive cycle times. The U.S. government could fund an EDA site where members of the NSTCs hubs pay a nominal fee to access the latest EDA tools. Respondents noted that although some services exist at various levels, the ability to provide open access to tools, processes, and IP that would enable co-optimization and full-stack development is missing. Fabless companies need a partner to take them to higher production levels, so respondents recommended that the NSTC should provide fabless companies with IP re-use, lower costs, and help in securing manufacturing partners.

According to respondents, specific toolsets that the NSTC should own and operate or provide access to include:

- 300 mm development and prototyping lines with full equipment sets capable of supporting multiple nodes.
- 200 mm or smaller non-Si flows; access to leading-edge, state-of-the-art CMOS technologies.
- Extreme ultraviolet lithography.
- Advanced packaging foundries and wafer level packaging.

The NSTC does not need to own the entire toolset. Incentives can be provided for companies to acquire these tools and then provide open access. Tools should be of the highest quality and enable users to accelerate commercialization. The NSTC could develop digital tools that allow rapid chip design and test.

### 2.11. As authorized, the NSTC could establish an investment fund, in partnership with the private sector, to support startups and collaborations between startups, academia, established companies, and new ventures, with the goal of commercializing innovations that contribute to the domestic semiconductor ecosystem, including advanced metrology and characterization for leading-edge manufacturing processes, and for security and supply chain verification. How should this investment fund be structured, and what should be the roles of the public and private sectors in capitalizing, operating, and overseeing the fund and selecting its investment targets? Should the investment fund focus on early-stage investing, late-stage investing, or other stages of the process? How should the fund interact with existing private capital, both venture capital and established investment capital, and how can the fund sustain itself through its investments?

Respondents stated that the fund should be managed by a governing council with a board of directors and a technical advisory committee.

The NSTC should ensure the long-term sustainability of the fund by acquiring equity in recipient companies, and through IP licensing fees. The investment fund should focus on all stages of the investment cycle, but with a tilt towards early stage investing. Respondents indicated that support during the early stages could de-risk technology maturation for pre-revenue companies and provide a catalyst for additional investments by traditional or venture capital firms. An alternate

view was for the NSTC to focus on late-stage investing, because such investments fill a crucial funding gap as companies transition from prototyping to mass production.

In addition, respondents recommended that the fund include an incubation space and a technology transfer office where startups can show their innovations and interact with investors, including existing new and established investment firms. If successful, the fund's incubation process could be seen as a "seal of quality," and could help attract additional capital investments.

### 2.12. How should the NSTC's investments and focus overlap or complement the investments and capabilities of foreign institutions such as the Interuniversity Microelectronics Center (imec) in Belgium or the French Laboratoire d'électronique des technologies de l'information (CEA-Leti)?

Most respondents were in favor of having some form of the NSTC collaborating with imec, CEA-Leti, and the Fraunhofer institutes. Such collaborations would ensure that efforts throughout the industry are complementary and could help the NSTC accelerate its development. Respondents indicated that such collaborations should include sharing roadmaps, joint development teams, and dividing the research focus amongst the collaborators. In view of the global nature of the industry, large capital investments, and the announcement of "Chips Funding" by other regions of the world, such collaborations will benefit the industry as a whole and avoid duplication of efforts.

Other respondents pointed out that although collaboration would be mutually beneficial, there is a risk of losing the NSTC's U.S. focus due to possible differences in organizational goals, and the potential for IP leakage to strategic competitors

# ADVANCED PACKAGING MANUFACTURING PROGRAMS

## 3. Advanced Packaging Manufacturing Program

Under Section 9906 (d) of the NDAA, the National Advanced Packaging Manufacturing Program (NAPMP) is authorized to strengthen semiconductor advanced test, assembly, and packaging capability in the domestic ecosystem. Advanced packaging and heterogeneous integration present a significant opportunity for innovation, leading to better yields, lower costs, greater functionality, reuse of intellectual property blocks enabling accelerated design iterations and customization, and improved energy efficiency. With support, there is a unique opportunity for U.S.-based equipment suppliers and manufacturers to lead in this critical area. Figure 5 shows the distribution of respondents to questions in this section.

According to respondents, the NAPMP should serve as a critical resource to develop advanced packaging and related R&D, as part of a larger effort to strengthen the resiliency of the semiconductor supply chain. Developing this sector will bolster the U.S.'s ability to compete on the global stage in semiconductor manufacturing. In view of the U.S.'s current dependence on foreign resources, some respondents noted that advanced packaging is a matter of national security.

To help develop this sector, respondents felt that the NAPMP must be competent in the following areas, 1) heterogeneous integration; 2) chiplets; 3) photonics, and 4) codesign of semiconductors and packaging solutions. The NAPMP should have easily accessible and flexible facilities or hubs that focus on low volume, cost-effective prototyping capabilities. Broad capabilities in material characterization, metrology, modeling and simulation, and standards were noted as important areas for the NAPMP to focus on.

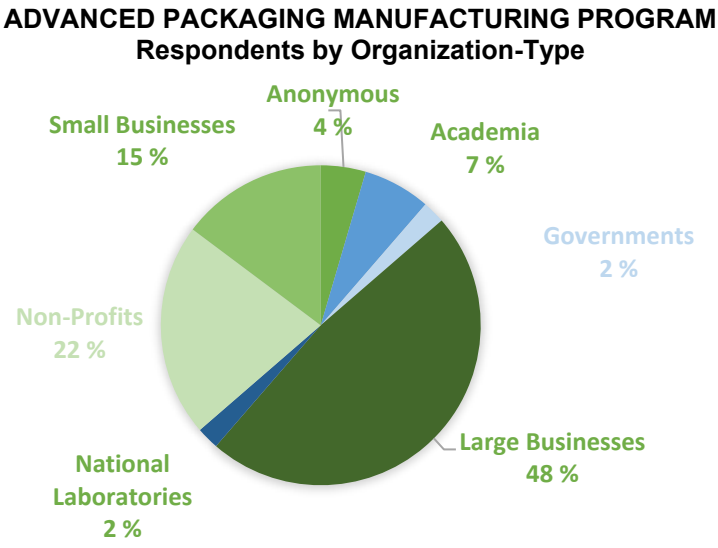



**Fig. 5.** Respondents to questions in the NAPMP section of the RFI

### 3.1. Please describe the application areas that are essential to long-term national leadership in semiconductor packaging, and, where possible, identify groupings where work must be closely coordinated in a program distributed in multiple hubs. Alternative materials to mitigate impact of supply chain disruptions. Examples include but are not limited to:

- **Analog device packaging**
- **Automotive**
- **Defense and aerospace**
- **Energy generation, transmission, conversion, and storage**
- **Harsh environments**
- **High performance computing, quantum computing, data centers**
- **Integrated photonics**
- **Integrated power electronics**
- **Internet of Things**
- **Mature packaging**
- **Medical, health & wearables**
- **MEMS and sensor electronics**
- **Mobile telecommunications**

The majority of respondents noted that all the applications listed above are relevant to long-term national success in semiconductor packaging, and indicated that integrated photonics and automotive applications will help drive the future of advanced packaging in the coming years. Integrated photonics, because it will enable or drive capabilities in different areas; and automotive applications, because of the large range of packaging types used in modern vehicles.

Possible groupings suggested by respondents include wearables for medical and consumer products; automotive, defense and aerospace, and harsh environment; high-performance computing and integrated power electronics; MEMS packaging, System in Package (SiP), flip chip, and 2.5D/3D integration.

Some respondents warned against grouping application areas together, and recommended building hubs around core competencies, specific performance targets, and common-use cases or conditions. Investments could be in general-purpose packaging concerns like chiplets, rather than investing in specific applications. Such hubs could be based on industry drivers, market segments, or geographical considerations.

### 3.2. Please describe the R&D core-competencies that are essential to national leadership in semiconductor packaging, and, where possible, identify groupings where work must be closely coordinated in a program distributed in multiple hubs. Examples include but are not limited to:

- **Alternative materials to mitigate impact of supply chain disruptions**
- **Artificial intelligence for design of packaging**
- **Assembly and test**

- **Emerging materials**
- **Heterogeneous integration, chip stacking, and related technologies.**
- **High-density substrates**
- **Metrology**
- **Modeling and simulation**
- **Package-level design/codesign tools for electrical, thermal and mechanical design of complex packages**
- **Printed circuit boards**
- **Safety and security**
- **Software, firmware, new concepts in programming**
- **Standards**
- **Test solutions to assure yield in complex packages**
- **Thermal solutions**
- **Tooling**

According to respondents, all the examples listed above, plus artificial intelligence and machine learning, and photonics are essential to national leadership in semiconductor packaging. The need for standards, and increased workforce development efforts were highlighted throughout the responses.

Overall, heterogeneous integration, co-simulation and codesign of HI and the need for multi-physics knowledge, and automation were frequently highlighted as important areas to focus on. Responses that were specific to material advancements and reliability, highlighted metrology, tools/equipment, testing, standardization, modeling and simulation, thermal management, and codesign as being critical areas for investment.

A small number of respondents commented on possible groupings, and recommended that geography, technical similarities, competencies, and coordination/collaboration should be the driving factors behind groupings.

### 3.3. A proposed National Advanced Packaging Manufacturing Program could be oriented to address multiple needs, including but not limited to prototyping, the provision of pilot lines, work force development, and supply chain development. Please describe the most critical needs on which the program should focus.

The most critical needs identified by respondents for the NAPMP to focus on are

- Strengthening the resiliency of the semiconductor supply chain.
- Supporting a broad set of technologies and applications.
- Encouraging collaboration and information sharing. Flexible and accessible low-volume prototyping facility.
- Workforce development at all levels.

### 3.4. What attributes are the most important for a National Advanced Packaging Manufacturing Program to deliver? Examples include but are not limited to:

- **Leading edge tools**
- **Characterization services**
- **Collaboration across multiple universities and multiple companies**
- **Development of education and workforce development infrastructure, including building a pipeline of skilled workers**
- **Easy to access facility, with different processes and tools**
- **Expert resident staff for custom development**
- **International participation**
- **Intellectual property protection for inventors**
- **Open access to intellectual property**
- **Post fabrication infrastructure**

According to respondents, all the examples listed above are important attributes for the NAPMP to possess. The most commonly cited attributes were:

- Collaboration across a diverse range of universities and companies
- Development of education and workforce infrastructure to build a pipeline of skilled workers
- Easy access to a wide variety of tools, capabilities, technologies
- Characterization services, expertise, and prototyping activities
- Flexible IP considerations (there should be open access to IP but also guidelines for handling and protection for IP)
- Ensuring that standards align across different stakeholders
- Ensuring that roadmaps align with priorities

### 3.5. What factors are critical to enable a National Advanced Packaging Manufacturing Program to provide a successful packaging R&D hub(s)?

According to respondents, the factors most critical to enabling the NAPMP to provide a successful packaging R&D hub(s) are to:

- Provide support for workforce development
- Ensure secure and sustainable funding (both public and private)
- Develop state-of-the-art equipment and facilities, and a clear technology roadmap or portfolio strategy.
- Encourage collaboration among academia, industry, and government, and fostering of lab-to-fab- efforts
- Ensure alignment of hub location with dominant industry in the area

- Establish clear IP rules and guidelines
- Allow members to install, test, or validate new equipment or technologies.
- Serve as a repository for housing libraries of information (including PDKs, best known methods (BKMs), lessons learned and enabling IP) that are open and easily searchable.
- Enable scaling from TRL 5 to TRL 8/9 that is compatible with mass production, (in-house or outsourced)
- Develop low-cost and environmentally sustainable manufacturing solutions

## 3.6. Identify processes, equipment, measurement capabilities, environmental conditions, and training facilities that are most crucial for facilities provided by a National Advanced Packaging Manufacturing Program. How might organizations access such facilities?

According to respondents, the processes, equipment, measurement capabilities, environmental conditions, and training facilities that are most crucial for NAPMP facilities must enable advanced bonding and assembly techniques, such as heterogeneous integration; and high-performance material characterization, including electrical, mechanical, and thermal characterization equipment.

Specific capabilities include wafer-level processing (including dicing, thinning, and backside processing), wafer-level packaging, optical packaging, optical inspection, lithography, dielectric and metals deposition, process heating, die stacking, 2.5D and 3D integration, thermal management, through-silicon via etching, electroplating, and coating (including liquid and dry film lamination).

Respondents recommended using facilities that can achieve the environmental conditions required to support advanced semiconductor manufacturing, as well as environmental flexibility to enable comprehensive evaluation, including harsh environment testing. It was also suggested that these should be facilities that can support high-volume assembly and packaging, support defect isolation, house the appropriate classes of cleanrooms, and enable maximized purity of materials.

There was a high level of consensus that ease of access to facilities will be critical to the success of the program. Recommended access models included open access to participating companies, a flexible access model based on organization type (e.g., university, supplier, OEM, small company, start-up), a foundry service based on the existing semiconductor foundry model, and access via membership and/or satisfaction of participation requirements.

## 3.7. How closely aligned should the capabilities enabled by a National Advanced Packaging Manufacturing Program be with those provided by the NSTC?

According to respondents, that the NSTC and NAPMP should be closely aligned, as packaging and chip technologies have become highly interrelated. The two programs should be collaborative and complementary to avoid duplication of efforts and resources. Several respondents suggested that prototype development should be able to pass easily from the NSTC to NAPMP through continuous process steps, with chip manufacturing being optimized for subsequent packaging.

In addition, success in establishing a seamless connection between NSTC and NAPMP programs would be best achieved by aligning technology roadmaps, portfolio strategies, TRL designations, workforce development strategies, and supply chain management priorities. This coordination,

according to respondents, can only be achieved through strategic joint leadership. Several respondents suggested that NSTC and NAPMP should either be a single entity or share the same directors and/or advisory board.

Overall, respondents indicated that that co-design, co-development, and co-optimization of semiconductors and packaging solutions should be the norm.

Some respondents indicated that overall coordination and alignment of NSTC and NAPMP could be achieved through co-located facilities, since some of the same infrastructure and process capabilities are required for chip manufacturing and packaging. Other respondents suggested that both chip manufacturing and packaging have technology areas that require significant growth independent of the other and that different facilities would maximize the pace of innovation and increase overall accessibility for participants across the country.

### 3.8. How should the National Advanced Packaging Manufacturing Program connect to National Network for Semiconductor R&D, authorized by Sec. 9903 of the FY 2021 NDAA? What considerations should be given to ensure strong integration between the two efforts? Should there be overlap in the technology readiness levels served by each program?

Many respondents either provided answers very similar to those given in Question 7, suggested that their Question 7 response should be deferred to, or more explicitly stated that the connection between NAPMP and NNSRD should be similar to that of the NAPMP and NSTC.

One common suggestion was that technology produced through NNSRD can be further developed, tested, and prototyped within NSTC and NAPMP.

According to respondents, the relationship between the NAPMP and NNSRD, should be similar to that between the NSTC and NAPMP. Such collaboration will require some overlap in commonly defined TRL levels, and coordination in every stage of development, including strategy, design, operations, and especially during validation and transfer to manufacturing.

Coordination can be facilitated through joint development teams (which may need to be explicitly allocated for in each organization's budget), complimentary roadmaps, aligned goals and objectives, coordination of data rights, IP ownership and licensing, and proprietary information agreements.

In addition, there should be collaboration between the university network of NSTC/NAPMP and the NNSRD. This will help support lab-to-fab efforts and align investments and infrastructure.

### 3.9. Describe anticipated needs in education and workforce development, including retraining and upskilling, in the semiconductor packaging area. How adequate is it currently, and what are future expectations of need? How should the workforce training pipeline be developed?

According to respondents, workforce is the most important component in establishing and sustaining a domestic advanced packaging industry. Due to lack of a robust domestic packaging industry, there are relatively few skilled engineers and scientists who are available to work in this sector or train additional workers.

Respondents indicated that swift action is needed to develop training programs at all levels (high school, community colleges, trade schools, universities, and graduate programs). Internships, apprenticeships, and specific work training programs should be used. The government and

industry should also look at adjacent fields where workers could be retrained to work in advanced packaging.

In addition, respondents recommend developing packaging related curricula or programs with current engineering fields (e.g., mechanical engineering, electrical engineering, computer science, materials science), as well as more targeted specialties to meet specific industry needs. Targeted curricula could include advanced electronic and photonic packaging, materials and process development, artificial intelligence, automation, and modeling/simulation. Strategic investments should be made to recruit and retain faculty.

It was also noted that investment in university research can be increased to support workforce development. Some respondents suggested that research should be industry-sponsored, or that universities should build up their in-house capabilities to support relevant student projects and lab-based classroom learning.

The NAPMP could be used as a training and hands-on experience center for advanced packaging. The NAPMP or a related national coalition could be used to expose students to full-flow packaging lines and provide nationally recognized certification programs for current workers seeking upskilling or reskilling.

It was emphasized that some of the most critical skills for current workers are heterogeneous integration and automation, as well as operating the equipment listed in the Question 6 responses above.

At a higher level, respondents suggested that it may be necessary to incentivize industry and universities to engage in recruitment activities, as well as to offer tax incentives to individuals joining the packaging workforce.

# WORKFORCE DEVELOPMENT NEEDS OF THE INDUSTRY

## 4. Workforce Development Needs of the Industry

The growth and sustainment of the Nation's semiconductor industry depends on a highly skilled workforce capable of meeting current and future needs of the public and private sectors.

According to respondents, the lack of skilled workers is a potential showstopper in reversing the decline in the domestic semiconductor manufacturing capacity. CHIPS Act investments will only be successful if there are skilled workers available to fill positions that will be created when new facilities are built. Figure 6 shows a summary of the respondents to this section. Respondents felt that the government and industry should deploy a multipronged approach using all tools at their disposal. Specific recommendations include:

- Increasing the pipeline of students in science, technology, engineering, and math (STEM) career paths and the semiconductor field specifically and improving partnerships and collaborations between training institutions and employers.
- The NSTC, NAPMP, and all collaborators should have a strong workforce component and provide nationally recognized training and certification programs.
- Increase access to foreign labor through immigration regulations that attract and retain foreign talent.
- Enhance the image and visibility of the semiconductor industry and make it attractive to K-12 students and undergraduates.
- Use marketing at all levels to show that the industry has a long and healthy future in the U.S. Taiwan and Germany were specifically noted several times as countries that we could model our workforce development after, as they have had success in this area. It was also noted that there is no substantial presence of a labor union in the semiconductor industry.

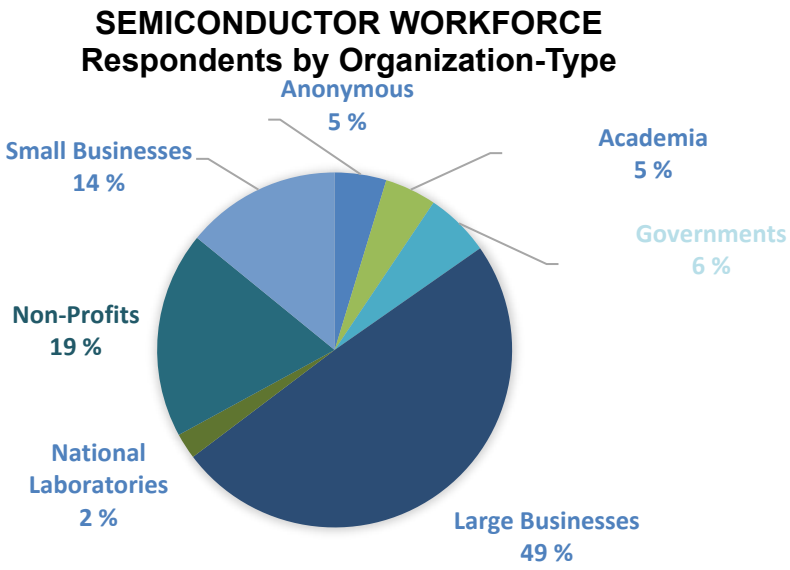



**Fig. 6.** Respondents to questions in the semiconductor workforce section of the RFI

### 4.1. What are the greatest occupational or skills shortages facing employers in the semiconductor sector? What are the consequences of those shortages with respect to the domestic operation of employers in the sector? Considering all aspects of building, equipping, and running semiconductor manufacturing and R&D facilities, what actions have been taken to address these shortages, how effective have they been, and what gaps remain?

According to respondents, the greatest occupational or skills shortages faced by employers are at all levels, from entry-level technicians to PhD researchers. The most common shortages are mid-skill (technicians) and high skill (engineers) and occur at all sectors of the semiconductor value chain. Specific skills and categories include technicians, equipment maintenance and fabrication technicians, and mid to high-level engineers. Fewer entry-level engineers of all types are entering the industry (domestically) and even fewer are staying within the industry to fill senior engineering and technical management positions. This problem is particularly serious in packaging, hardware design, and R&D. There is an expectation amongst respondents that this problem will only worsen with time.

Respondents indicated that this has led to increased costs, unfilled positions, decreased production, and lower quality. More broadly, many respondents expressed concerns that the U.S. is now in a negative feedback loop of decline as costs increase, jobs move overseas, and viable careers for U.S. based engineers decrease. A key message from respondents is that the U.S. semiconductor industry will continue to decline unless there is no significant intervention to strengthen the skills and expertise of the U.S. workforce.

In response to the growing skills gap, many stakeholders in the industry have invested in growing the local labor force. This includes establishing partnerships and training programs with community and local college programs. However, such efforts are seen as steps in the right direction, but not enough.

## 4.2. PART 1: What strategies have been most effective in addressing the shortages? Which states or countries have created the most effective strategies for different types of workforce needs to build, equip, and run semiconductor manufacturing and R&D facilities?

According to respondents, the strategies that have been or could be most effective at addressing shortages include recruiting foreign talent, reskilling non-traditional candidates, providing internships and apprenticeships to young professionals, and investing in marketing and education programs locally.

The short-term approaches to addressing shortages have primarily been through widening the pool of candidates to international talent and non-traditional candidates. Companies currently use international talent while respondents indicated that it can and should be made easier to utilize more.

Other approaching reported by respondents include recruiting international talent, non-traditional candidates, veterans, and candidates from other industries. Respondents noted that apprenticeships and internships (SEMI and their SCAN) have improved the number of qualified workers entering their companies, but not at high enough rates to meet demand.

Increased marketing was mentioned multiple times as a way for the industry to attract younger workers. A few respondents have already been investing in K-degree STEM and semiconductor education which is intended to increase interest in the long-term. These education investments have been regionally located to manufacturer's locations although multiple respondents pointed to SEMI's High-tech U as potentially having a nationwide impact.

Internationally, Germany and Taiwan were frequently mentioned as nations with the most comprehensive strategies for workforce development. Singapore and China were also mentioned for effective programs for workforce development of their semiconductor industries. All were identified as having effective public/private partnerships that prepare workforce for STEM/technical employment. Domestically, New York and Arizona were identified as having effective workforce development programs. Other states identified tended to be influenced by locations of the respondents. New York's P-TECH, SUNY workforce training, and NYCREATES were referred to as effective workforce development partnerships. Arizona was identified as having incentives for attracting higher paying jobs as well as investing in electronics education at the university level.

### PART 2: What industry or other credentials do employers use, or could use, to train and hire workers to fill needed positions? To what extent do employers in the semiconductor sector partner with government institutions such as local workforce boards, economic development organizations, or Manufacturing Extension Partnership centers, or international partners to establish training and/or skill certification programs? To what extent do employers in the semiconductor sector partner with other employers to create joint training programs?

According to respondents, 2-year STEM degrees for manufacturing positions and 4-year degrees for high-skill roles are the basic requirements for most semiconductor manufacturing work. Some respondents suggested that a national credential could improve workforce preparation, and some noted that certificates programs such as NY-RHIT, could be models. Broad industry-wide credentials could reduce the amount of on-the-job training employees need while tailoring education requirements to semiconductor fields.

Multiple employer partnerships with government entities were identified by respondents but other respondents said that such partnerships were rare across the industry as a whole. Partnerships identified were primarily education focused. Many respondents said that the industry would benefit from more government partnership all around.

Workforce partnerships amongst private sector entities is limited. Partnerships through R&D activities or industry associations like SEMI or SRC tend to be the only areas with workforce development focus.

### 4.3. What types of apprenticeship programs or existing partnerships involving workforce development issues in the semiconductor sector should the Department be aware of? What role can unionized labor play in worker training and workforce development, including for economically disadvantaged individuals?

Many companies have their own apprenticeship and development programs. There are multiple instances of companies partnering with universities to provide internships to college students. Programs that were highlighted by respondents as possible models include SEMI and their growing SEMI Career and Apprenticeship Network (SCAN); he National Institute for Innovation and Technology's (NIIT) National Talent Hub; and the Scalable Asymmetric Lifecycle Engagement (SCALE) program from the Department of Defense.

Two government responses pointed out the importance of unions and working with unions, however, the only private industry responses noted that they have no experience working with unions and that most of the semiconductor industry is not unionized.

### 4.4. What have been successful mechanisms used by employers in the semiconductor sector to work with local high schools, career and technical education programs, community colleges, or universities to recruit and train workers?

According to respondents, career technical education (CTE) partnerships between employers and local education institutions are common across the industry. For K-12 education, a common theme is improving the image (marketing) of the semiconductor industry and STEM in general to attract more students into technical degrees. Some employers engage high schools directly and have training or education programs that prepare students to work in manufacturing. Pathways in Technology Early College High School (P-TECH) was referred to as a non-employer driven successful high school and community college education program for transitioning students into technical jobs.

At the university level, internships/apprenticeships/co-ops are the primary method of providing hands-on learning opportunities. Several respondents mentioned funding partnerships with universities through R&D projects, senior capstone projects, school competitions, or developing curriculum as effective workforce education activities that their companies take part in.

### 4.5. Are there any current or planned initiatives in the semiconductor sector to strengthen and expand the recruitment of women and underrepresented minorities, including promotion of such careers at K-12 levels?

Several companies mentioned that there have been efforts to attract underrepresented minorities through high school and college outreach programs. Many of those included outreach efforts to historically black colleges and universities (HBCUs) through internships and grants. While there

has been some success, respondents indicated that more should be done to diversify the workforce. There were multiple initiatives mentioned for both women and underrepresented minorities. K-12 activities were primarily oriented toward increased marketing and increasing interest amongst students in STEM broadly. One response noted that STEM-focused high schools are effective in including minorities and students from socioeconomically disadvantaged areas, and that increasing the number of these schools would allow more students to excel in computer science. At both K-12 and university levels, most established programs happen through larger companies.

### 4.6. To what extent, and for what occupations, do organizations in the semiconductor sector use the H1-B Program to fill positions?

According to respondents, their companies use the H1-B program to fill BS, MS, and PhD engineering positions, especially for specific semiconductor skillsets. Notable exceptions are in the defense industry which cannot use foreign nationals. Some respondents pointed out that H1-B is not enough and should be expanded and made more efficient to increase the flow of top global talent to the U.S. Also, difficulties in transitioning to green card status is a barrier to keeping H1-B talent, and it's noted that STEM employment or STEM degree based green cards, without limits, would help.

### 4.7. Are there opportunities to design the semiconductor incentive program to ensure that worker skills shortages do not hinder companies from expanding operations?

Recommendations by respondents include increasing or improving foreign talent recruitment, increasing the pipeline of students toward STEM and the semiconductor field specifically, helping to market the industry as impactful and growing in the U.S. to draw more talent to the field, and improving partnerships and pipelines between training/schools and employers.

In addition, several non-profit respondents suggested increasing funding for semiconductor-sector-specific grant programs through the NSF Fellows program or the Manufacturing Engineering Education Grant (MEEG) program; or creating an incentive program for community colleges and universities to expand or improve computer science course offerings/trainings.

## INDEX