NBS TECHNICAL NOTE 788

Methods of Measurement for Semiconductor Materials, Process Control, and Devices

Quarterly Report

January 1 to March 31, 1973

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Office of Standard Reference Data — Office of Technical Information and Publications — Library — Office of International Relations.

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[1] Headquarters and Laboratories at Gaithersburg, Maryland, unless otherwise noted; mailing address Washington, D.C. 20234.
[2] Part of the Center for Radiation Research.
[3] Located at Boulder, Colorado 80302.
[4] Part of the Center for Building Technology.

Methods of Measurement for Semiconductor Materials, Process Control, and Devices

Quarterly Report, January 1 to March 31, 1973

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National Bureau of Standards
Washington, D.C. 20234

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FOREWORD

The Joint Program on Methods of Measurement for Semiconductor Materials, Process Control, and Devices was undertaken in 1968 to focus NBS efforts to enhance the performance, interchangeability, and reliability of discrete semiconductor devices and integrated circuits through improvements in methods of measurement for use in specifying materials and devices and in control of device fabrication processes. These improvements are intended to lead to a set of measurement methods which have been carefully evaluated for technical adequacy, which are acceptable to both users and suppliers, which can provide a common basis for the purchase specifications of government agencies, and which will lead to greater economy in government procurement. In addition, such methods will provide a basis for controlled improvements in essential device characteristics, such as uniformity of response to radiation effects.

The Program is supported by the National Bureau of Standards,* the Defense Nuclear Agency,† the Defense Advanced Research Projects Agency,× the U.S. Navy Strategic Systems Project Office,§ the Air Force Weapons Laboratory,+ the Air Force Cambridge Research Laboratories,¶ and the Atomic Energy Commission.# Although there is not a one-to-one correspondence between the tasks described in this report and the cost centers through which the Program is supported, the concern of certain sponsors with specific parts of the Program is reflected in planning and conduct of the work.

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* Through Research and Technical Services Cost Centers 4251126, 4252128, 4254115, 4251140, and 4254140.

† Through Order EA073-800. (NBS Cost Center 4259522).

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METHODS OF MEASUREMENT FOR SEMICONDUCTOR MATERIALS, PROCESS CONTROL, AND DEVICES

QUARTERLY REPORT
JANUARY 1 TO MARCH 31, 1973

This quarterly progress report, nineteenth of a series, describes NBS activities directed toward the development of methods of measurement for semiconductor materials, process control, and devices. Significant accomplishments during this reporting period include (1) development of a comprehensive, large-area test pattern for evaluating planar junction structures, (2) completion of experimental work on the evaluation of the destructive, double-bond pull test for wire bonds, (3) initiation of a scanning electron microscope facility, and (4) completion of the investigation of the mechanism of emitter-base junction reverse breakdown during rapid switching of transistors. Because of the general applicability of the last of these, details are presented in a separate appendix. Work is continuing on measurement of resistivity of semiconductor crystals; characterization of generation-recombination-trapping centers in silicon; study of gold-doped silicon; development of the infrared response technique; evaluation of wire bonds and die attachment; measurement of thermal properties of semiconductor devices; determination of S-parameters, delay time, and related carrier transport properties in junction devices; development of a-c probing techniques; and characterization of noise and conversion loss of microwave detector diodes. Supplementary data concerning staff, standards committee activities, technical services, and publications are included as appendices.

Key Words: Base transit time; carrier lifetime; delay time; die attachment; electrical properties; electronics; epitaxial silicon; four-probe method; generation centers; germanium; gold-doped silicon; infrared response; methods of measurement; microelectronics; microwave diodes; probing techniques (a-c); pull test; recombination centers; resistivity; resistivity standards; semiconductor devices; semiconductor materials; semiconductor process control; silicon; S-parameters; switching transients; thermal resistance; thermally stimulated properties; trapping centers; wire bonds.

1. INTRODUCTION

This is the nineteenth quarterly report to the sponsors of the Joint Program on Methods of Measurement for Semiconductor Materials, Process Control, and Devices. It summarizes work on a wide variety of measurement methods that are being studied at the National Bureau of Standards. The Program is a continuing one, and the results and conclusions reported here are subject to modification and refinement.

The work of the Program is divided into a number of tasks, each directed toward the study of a particular material or device property or measurement technique. This report is subdivided according to these tasks. Highlights of activity during the quarter are given in section 2. Section 3 deals with tasks on methods of measurement for materials; section 4, with those on methods of measurement for process control; and section 5, with those on methods of measurement for devices. References for each section are listed in a separate subsection at the end of that section.

The report of each task includes the long-term objective, a narrative description of progress made during this reporting period, and a listing of plans for the immediate future. Additional information concerning the material reported may be obtained directly from individual staff members identified with the task in the report. The organization of the Joint Program staff and telephone numbers are listed in Appendix A.

An important part of the work that frequently goes beyond the task structure is participation in the activities of various technical standardizing committees. The list of personnel involved with this work given in Appendix B suggests the extent of this participation. Additional details of current standardization activities not associated with a particular task are given in section 2.

Background material on the Program and individual tasks may be found in earlier reports in this series as listed in Appendix D. From time to time, publications are prepared that describe some aspect of the program in greater detail. Current publications of this type are also listed in Appendix D. Reprints or copies of such publications are usually available on request to the author.

2. HIGHLIGHTS

Significant accomplishments during this reporting period include (1) development of an experimental comprehensive, large-area test pattern for evaluating planar junction structures, (2) completion of experimental work on the evaluation of the destructive, double-bond pull test for wire bonds, (3) initiation of a scanning electron microscope facility, and (4) completion of the investigation of the mechanism of emitter-base junction reverse breakdown during rapid switching of transistors.

Highlights of these and other ongoing activities are presented in this section; details of progress in technical areas are given in subsequent sections of the report. This section concludes with a summary of standardization activities being carried out by program staff members.

Resistivity — Two *p*-type silicon crystals, grown by a modified float-zone process, have been evaluated and found suitable for use as sources of standard resistivity wafers. The crystals are being sliced into wafers. An experiment was designed to disclose systematic errors in the resistivity calibration procedure to be used on these wafers.

A commercially available automated instrument for making spreading resistance measurements was installed. Several possibilities for improvements in its effective use were identified and the improvements made. A set of calibration slices is being collected. A standard technique for qualifying and calibrating spreading resistance instrumentation is being explored in conjunction with ASTM Committee F-1 on Electronics.

Doping profiles obtained from the capacitance-voltage characteristics of a gated silicon p^+n junction were studied at various values of gate bias. A correct profile is obtained when the gate bias is at the flat-band potential.

Generation-Recombination-Trapping Centers — An apparatus for measuring the thermally stimulated properties of *p*-*n* junctions was constructed and tested. It can be operated over the temperature range -191 to 400°C and has a maximum heating rate of 7 K/s.

A mask was designed for use in the fabrication of silicon test structures, such as MOS capacitors and *p*-*n* junctions. Twenty different planar test structures were designed to fit on a square silicon chip, 200 mils (5.08 mm) on a side.

A simple expression was developed for finding the carrier lifetime in narrow base diodes from reverse recovery measurements.

Gold-Doped Silicon — Additional measurements of room temperature resistivity as a function of gold density were compared with theoretical calculations for both *n*- and *p*-type silicon. Except for the location of the sharp rise in resistivity of *n*-type

specimens, the calculated curves generally fit the experimental data. However, there are some smaller deviations which appear to be systematic. One possible source of these deviations may be the discrepancy between the computed doping densities for low resistivity crystals (<1 Ω·cm) and those obtained experimentally. This discrepancy arises because of difficulties with the calculation of ionized impurity and mixed mobilities.

Infrared Methods — Infrared response (IRR) measurements were carried out on specimens of five germanium crystals representative of currently available material for gamma-ray detector fabrication. The IRR measurements confirmed the observation of hole trapping in the two specimens for which gamma-ray detector characteristics were known. IRR measurements have been carried out on a lithium-drifted silicon diode before and after heat treatment. The results appear to be in agreement with a similar experiment performed earlier on germanium.

Die Attachment Evaluation — The tape of the revised TRUMP thermal analysis computer program was successfully modified for use on the NBS computer. Measurements, made on transistors bonded to TO-5 headers with void sizes ranging from 15 to 40 percent of the chip bonding area, indicated an increase in sensitivity to the presence of voids of transient thermal response measurements made with a 5-ms wide heating power pulse over that of steady-state thermal response measurements of from four to nearly seven times. Long-term, single-operator measurements of steady-state and transient thermal response to check the repeatability of the transistor die attachment evaluation equipment were also undertaken.

Wire Bond Evaluation — The experimental phase of the investigation of the effects of geometrical variables on the destructive, double bond pull test was completed. Pull strength was measured as a function of loop height, pull angle α, pull angle β, and position of pulling hook for two-level bond pairs. These measurements yielded results which generally agreed with theoretical predictions.

The vibration modes of two unconventional ultrasonic bonding tools were studied during bonding. One was significantly different from conventional tools.

Scanning Electron Microscopy — There has been a considerable increase in use of scanning electron microscopy, which has very much greater depth of field at higher magnification, as an in-process inspection technique and as an element in acceptance specifications for semiconductor devices. In addition, the scanning electron microscope (SEM) provides a possible means of examining complex circuits in operation and detecting faulty regions without the need for probe or other direct contact. Because of the importance of the problems at the wafer level which can be disclosed by SEM examination and because of the increasing use of the SEM in government procurement of

high reliability components, a task concerned with evaluation of SEM inspection procedures and development of methods suitable for industrial use has been initiated.

Thermal Properties of Devices — Thermal resistance measurements were made by the emitter-only switching technique and with an infrared microradiometer on 12 transistors under conditions such that hot spots would occur in devices susceptible to hot spot formation. The results were compared with measurements made previously under conditions such that there were no severe current constrictions or hot spots. The data confirmed the expectation that, when operating at or near the second breakdown or voltage limited (low-current, high-voltage) region of the device safe operating area curve, the electrically measured thermal resistance cannot be relied upon to give the same value of thermal resistance as that calculated from measurements of peak junction temperature made with the infrared microradiometer.

In order to elucidate certain aspects of the model proposed to account for them, the characteristics of the emitter-base voltage and current transients which occur when switching the emitter with a series transistor during measurement of thermal resistance by the emitter-only switching technique were further investigated. Under certain conditions reverse breakdown can occur at the periphery of the emitter-base junction even though the central region remains forward biased. This occurs because of lateral majority carrier flow in the base layer. The results of this work are reported in greater detail in Appendix F.

Microwave Device Measurements — Measurements to ascertain the random uncertainty of the X-band mixer measurement system were resumed. A Schottky-barrier diode designed as a replacement for the 1N23 point-contact type was used for this study because it is believed to be more stable than the point-contact type, whose characteristics are dependent upon whisker position and pressure, which are easily disturbed. Typical runs yielded conversion loss of about 4.53 dB with a sample standard deviation of 0.02 to 0.03 dB.

Carrier Transport in Junction Devices — The delay-time correction technique was successfully applied to measurements on the Sandia bridge of transistors subjected to gain degradation.

The data on the passive devices obtained by the five round-robin participants who used automatic network analyzers for measurement have been examined for both within- and between-laboratory variability. In almost every case, both the within- and between-laboratory variabilities are greater when each laboratory used its own transistor fixture than when all used the same transistor fixture. The results suggest that the calibration procedures are more effective in compensating for the transmission characteristics of the transistor fixture than in precisely locating the reference planes.

Standardization Activities — Standardization activities directly related to particular task areas are reported with the appropriate tasks. However, many of the standardization activities undertaken by program staff are broader than the technical tasks described in the following sections. These activities, which are reported here, involve general staff support in committees, coordination of efforts which may encompass a variety of tasks, and participation in areas where no direct in-house technical effort is underway.

Twelve program staff members attended the Atlanta meeting of ASTM Committee F-1 on Electronics in January. In preparation for this meeting and a letter ballot immediately following it, four new documents and revisions of four existing standards were reviewed editorially. Two new sections of the subcommittee on quality and hardness assurance were formed. One of these sections is concerned with process control; the other, with thin film resistors.

Staff members attended meetings of JEDEC Committees JC-20 on Signal and Regulator Diodes, JC-22 on Rectifier Diodes and Thyristors, and JC-25 on Power Transistors. Work was completed on portions of the Proposed Standards on Power Transistors dealing with second breakdown and thermal resistance measurement; this standard was subsequently approved by JEDEC letter ballot.

Extensive consultation with industry and other government agencies was provided in the areas of wire bonding, hybrid bonding problems, pull test, ribbon wire, surface photovoltage, thermal resistance, and thermal analysis. Work was completed on editorial review of ten papers for the session on Diagnostic Techniques and In-Process Measurements of the Second International Symposium on Silicon Materials Science and Technology to be held at the spring meeting of the Electrochemical Society in Chicago.

Surveys of test methods used in controlling device processing and in thermally and electrically characterizing devices were undertaken. Of particular concern in these surveys are the impact of the procedures used on device reliability and the identification of measurement problems in these areas. Six manufacturers were visited in connection with problems encountered in digital integrated circuits and four in connection with problems encountered in power devices. In addition, visits to NBS in this connection were made by representatives of six other organizations.

To improve staff assistance to standards committees as well as to improve skills in the design of experiments, a course on applied statistics with particular emphasis on design and analysis of interlaboratory tests was conducted for the program staff by Dr. John Mandel of the NBS Institute for Materials Research.

3. SEMICONDUCTOR MATERIALS

3.1. RESISTIVITY

Objective: To develop methods suitable for use throughout the electronics industry for measuring resistivity of bulk, epitaxial, and diffused silicon wafers.

Progress: Two p-type silicon crystals, grown by a modified float-zone process, have been evaluated and found suitable for use as sources of standard resistivity wafers. The crystals are being sliced into wafers. An experiment was designed to disclose systematic errors in the resistivity calibration procedure to be used on these wafers.

A commercially available automated instrument for making spreading resistance measurements was installed. Several possibilities for improvements in its effective use were identified and the improvements made. A set of calibration slices is being collected. A standard technique for qualifying and calibrating spreading resistance instrumentation is being explored in conjunction with ASTM Committee F-1 on Electronics.

Doping profiles obtained from the capacitance-voltage characteristics of a gated silicon p^+n junction were studied at various values of gate bias. A correct profile is obtained when the gate bias is at the flat band potential.

Silicon Resistivity Standards — Two modified float-zone, p-type, silicon crystals were tested for acceptability for use as bulk four-probe resistivity standards. A 1 mm-thick slice was taken from each end of each of the two silicon crystals which were of nominal 0.1 and 10 Ω·cm resistivity at room temperature. The interstitial oxygen content as determined by infrared absorption [1] was less than the detection limit (7×10^{17} cm^{-3} for the 0.1 Ω·cm slices and 9×10^{16} cm^{-3} for the 10 Ω·cm slices). Resistivity uniformity measurements made at room temperature (23°C) on the crystals yielded the following results: The resistivities of the two end slices of the 10 Ω·cm crystal differed by about 10 percent of their mean value; the radial resistivity gradient between the center and half radius was less than 2 percent for both slices. The resistivities of the two end slices of the 0.1 Ω·cm crystal differed by less than 1 percent of their mean value; the radial resistivity gradient between the center and half radius was less than 1 percent for both slices. Dislocation density measurements were made on one slice from each crystal by etch pit counting [2] and x-ray topography; both methods showed the crystals to be essentially dislocation free.

These results indicate that both crystals are acceptable for use as standard wafers; they are being sliced in preparation for calibration of each wafer. A sampling plan to disclose any systematic errors caused by single operator or single instrument

measurement conditions during the calibration procedure has been developed. The sampling plan is a complete factorial experiment involving five wafers from each crystal; each to be measured by two operators on two instruments according to the standard procedure [3]. (J. R. Ehrstein and F. H. Brewer)

Other Standards Activities — A final draft of a method for measuring silicon epitaxial sheet resistance with a collinear four-probe array [4] was approved by ASTM Committee F-1 on Electronics as a new tentative method of test. Final analysis of the round-robin test of this procedure is not yet complete, but it appears that the multi-laboratory relative sample standard deviation is less than 5 percent for seven of the eight epitaxial wafers tested.

Modifications, largely of an editorial nature, but also including a tabular form for the temperature coefficient of resistivity of phosphorus- and boron-doped silicon (NBS Tech. Note 754, pp. 8-9), were made to the ASTM standard method for measuring resistivity of silicon slices with a collinear four-probe array [3]. The method was subsequently approved by Committee F-1 for retention as a standard with revisions.

Initial work has begun to arrange for and publicize a symposium to be jointly sponsored by Committee F-1 and the National Bureau of Standards in June of 1974 at Gaithersburg. The subject of the symposium is electrical measurements by spreading resistance methods and the application of this method to the characterization of starting semiconductor material, to process control, and to characterization of fully fabricated semiconductor devices. The call for papers is reproduced as Appendix E. (J. R. Ehrstein)

Spreading Resistance Methods — Various approaches to making semiconductor measurements with the spreading resistance technique have been reported by several of the major semiconductor device companies [5-8]. Discrepancies between these methods and general inability of other laboratories to reproduce from published information the results of these first few companies have severely hampered the widespread application of the spreading resistance measurement throughout the semiconductor industry. Since vast amounts of data are necessary in order to calibrate and characterize the spreading resistance measurement system, an automated apparatus was procured for this work.

Early work with the apparatus demonstrated the importance of very careful alignment of the probes. When profiling p-n junction regions, misalignment as little as 5 minutes of arc can distort measured profiles. In addition, tests indicated that the stability of the measurement apparatus was strongly affected by ambient building vibrations. Following placement of the instrument on a seismic table, no similar instabilities were observed.

Since the nature of the metal-semiconductor contact is not fully understood, spreading resistance is used as a comparison measurement; to make quantitative measurements, it must be calibrated against wafers of known resistivity. A set of some 80 silicon wafers is being tested for the purpose of developing a set of calibration slices. Because the instrument is expected to be used for a wide variety of applications, calibration curves are being generated for both *p*-type and *n*-type silicon covering the range 0.001 to 100 Ω·cm. (J. R. Ehrstein)

Capacitance-Voltage Methods — Emphasis in this area was shifted from a direct comparison of capacitance-voltage (C-V) and four-probe measurements to a study of doping profiles determined from C-V measurements on a gated, planar, silicon p^+n junction. The gate electrode affords greater control over the depletion region immediately under the oxide. Initial experiments were undertaken to establish the gate bias that results in a spatially uniform doping profile on the (uniform) lightly doped side of the junction. The junction was formed in a phosphorus-doped silicon slice with (111) faces and a room-temperature resistivity of about 8 Ω·cm. Boron was diffused to form a circular *p*-type layer with a sheet resistance of 90 Ω/□ and a surface density of 6.6×10^{19} cm^{-3}. The junction depth was 1.1 μm and the junction area was 0.18 mm^2. The annular aluminum gate electrode which was evaporated over a thermally grown silicon dioxide layer extended over both the *n*-type substrate and the junction. A circular metal-oxide-silicon (MOS) capacitor with an area of 0.083 mm^2 was also formed nearby by another aluminum contact over the silicon dioxide thermally grown on the *n*-type substrate.

Junction capacitance and current and MOS capacitance were measured as a function of gate bias in the dark at room temperature. The capacitance was measured with a 1 MHz, 15 mV rms signal and the current was measured with an electrometer operated in the fast feedback mode. The results shown in figure 1 indicate the inversion, depletion, and accumulation regions for the periphery of the gated junctions. The transition from depletion to accumulation was taken at a gate bias of -14.2 V, the flat-band potential as determined from the MOS C-V characteristic shown in figure 1c. The oxide capacitance was 4.74 pF, which corresponds to an oxide thickness of 6050 Å (605 nm); the fixed oxide charge density was 5.18×10^{11} cm^{-2}.

Junction capacitance was also measured as a function of reverse bias at the gate voltages, V_g, shown in figure 2. Here the transition from depletion to inversion is clearly visible for V_g = -30 and -45 V. Doping profiles computed from these data are shown in figure 3. These profiles were obtained by using an analysis [9] which assumes that the boron diffusion profile is Gaussian and that the peripheral space-charge region is cylindrical. The same values of junction area, junction depth, and surface density given above were used in the analysis of each profile. The profiles for

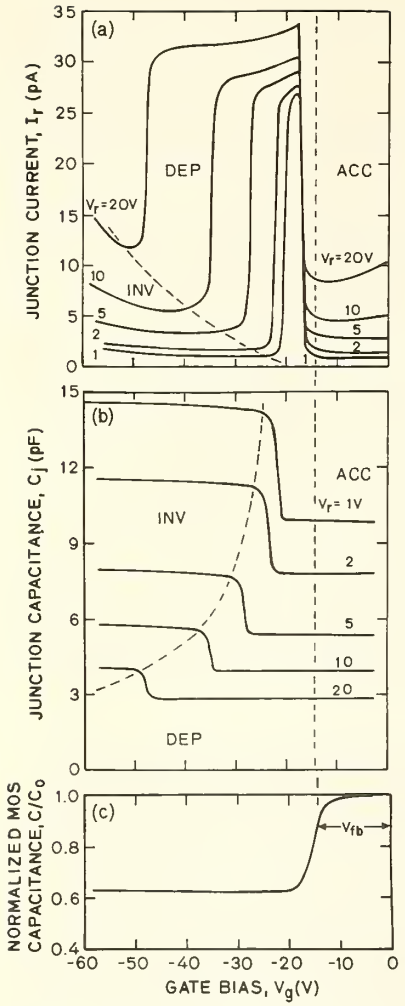


Figure 1. Current and capacitance of a planar, gated p^+n junction as a function of gate bias for various values of reverse junction bias, V_r. (The inversion, depletion, and accumulation regions are indicated by INV, DEP, and ACC, respectively. The flat-band voltage, V_{fb} = -14.2 V, is indicated on the MOS C-V characteristic in the lowest graph. The MOS capacitance is normalized to the oxide capacitance, C_0 = 4.74 pF.)

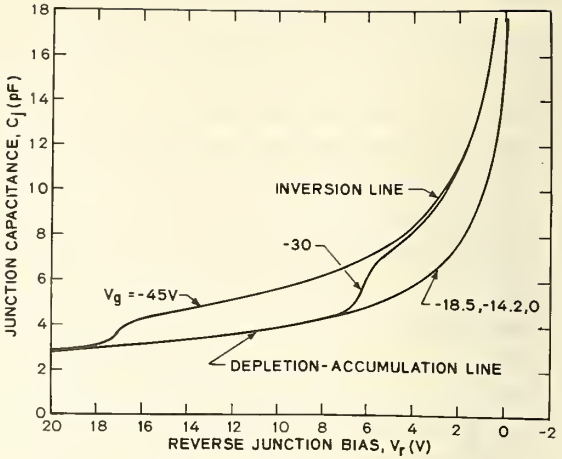


Figure 2. Capacitance-voltage characteristics of a planar, gated p^+n junction for various values of gate bias.

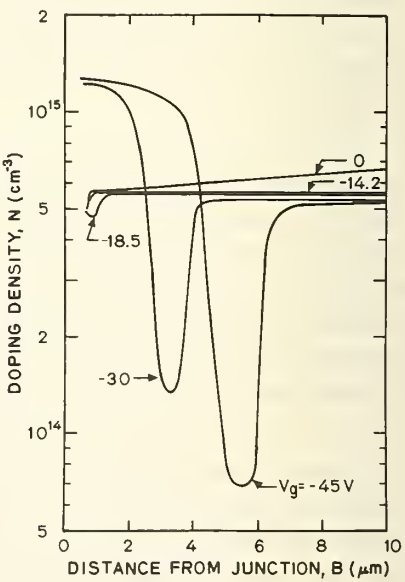


Figure 3. Apparent doping profiles determined from the C-V characteristics of a planar, gated p^+n junction taken at various values of gate bias.

V_g = -30 and -45 V result because the region at the periphery of the junction goes from inversion at small junction bias to depletion at large junction bias; see figure 2. These two profiles, taken at face value, appear to indicate a heavily doped layer near the surface, then a narrow, lightly doped layer, and finally the correct background doping density. For V_g = 0 the surface is heavily accumulated which narrows the space-charge region close to the junction at the surface [10]. This leads to a junction capacitance which is larger than that predicted by the cylindrical approximation so that the background doping density appears to be larger than it actually is. The correct, spatially uniform profile appears for V_g = -14.2 V, the flat-band potential. The background doping density of 5.4×10^{14} cm^{-3} compares favorably with a surface density of 5.8×10^{14} cm^{-3} obtained from measurements on the MOS capacitor since the surface density is expected to be slightly higher than the background density because of phosphorus pile-up during thermal oxidization.

(R. L. Mattis and M. G. Buehler)

Plans: The two silicon crystals intended for resistivity standards will be prepared into wafer sets and the calibration procedure will begin. It is expected that the first sets of wafers will be available for sale by July 1. The cost per set will be determined by the production costs; announcements of price and availability will be made both through electronics industry trade literature and through government publications. The analysis of the round-robin experiment on measurement of the resistivity of epitaxial layers by the four-probe method will be completed. Design of an experiment to test the effects of current, probe force, and probe tip condition on four-probe resistivity measurements of 5 and 25 mm thick *n*- and *p*-type silicon epitaxial layers, postponed this quarter, will be initiated. Generation of the calibration wafers for the spreading resistance method will continue. Various aspects of junction C-V doping profiles will be studied with regard to (a) profiles at various gate biases, (b) profiles at forward biases, (c) profiles of large and small junctions, and (d) diffused layer profiles.

3.2. GENERATION-RECOMBINATION-TRAPPING CENTERS

Objective: To develop electrical measurement methods including mathematical models and test structures for characterizing the electronic properties and density of generation-recombination-trapping (GRT) centers in silicon with emphasis on methods applicable to control of parameters such as lifetime and junction leakage current.

Progress: An apparatus for measuring the thermally stimulated properties of *p-n* junctions was constructed and tested. It can be operated over the temperature range -191 to 400°C and has a maximum heating rate of 7 K/s.

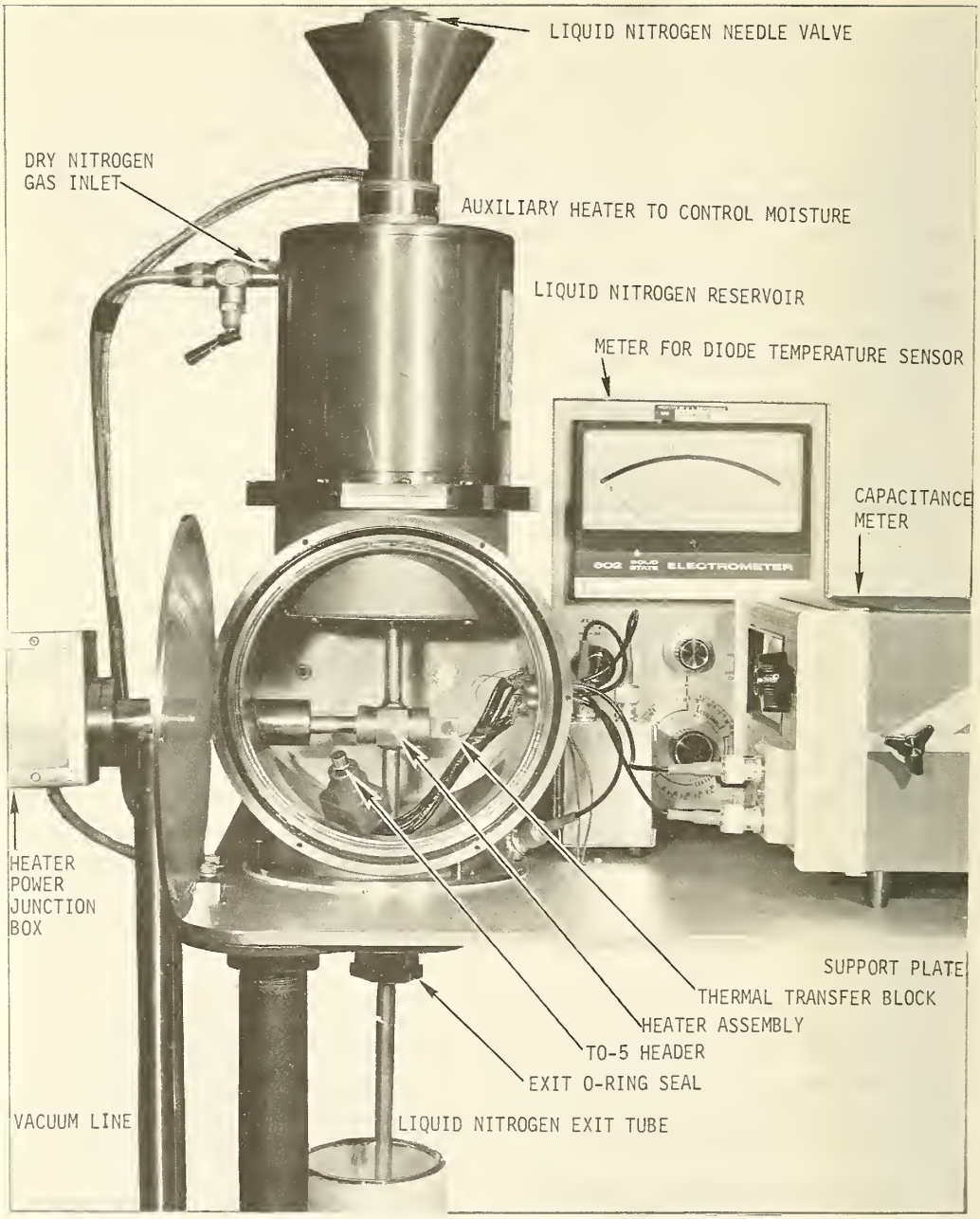


Figure 4. Apparatus for measuring thermally stimulated current and capacitance of *p-n* junctions. (In operation the header is fitted into the hole in the thermal transfer block. The temperature controller, not shown, is mounted directly under the support plate.)

A mask was designed for use in the fabrication of silicon test structures, such as MOS capacitors and *p-n* junctions. Twenty different planar test structures were designed to fit on a square silicon chip, 200 mils (5.08 mm) on a side.

A simple expression was developed for finding the carrier lifetime in narrow base diodes from reverse recovery measurements.

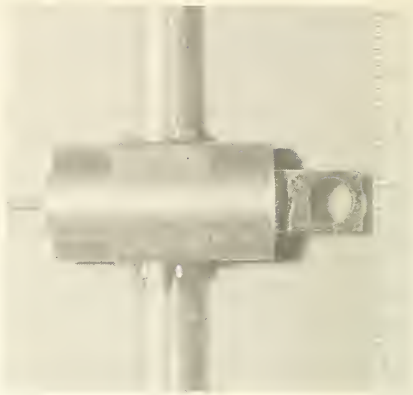
Thermally Stimulated Properties — An apparatus was constructed for the measurement of the thermally stimulated current and capacitance of *p-n* junctions. The apparatus, pictured in figure 4, was designed to facilitate the electrical characterization of a *p-n* junction mounted in a 10-pin, TO-5 header. The junction is mounted on a ceramic chip which isolates the junction from the header [1].

In operation, the TO-5 header is placed in the thermal transfer block, and the chamber is evacuated by a mechanical pump. The header is cooled by flowing liquid nitrogen from the reservoir, through the heater assembly, and out the exit tube. Intermediate temperatures are established by balancing the heat and cold inputs to the header assembly.

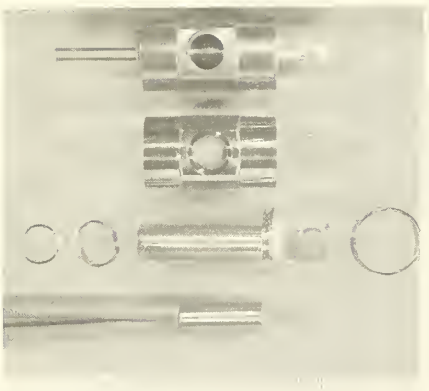
The number of parts in the heater assembly was minimized to reduce vacuum problems; details are shown in figure 5. The stainless steel heater is rated at 150 W at 110 VAC; it was silver soldered into the copper thermal transfer block. This in turn was silver soldered into the stainless steel housing using the rings shown. The remainder of the system was heli-arc welded. The reservoir, heater assembly, and exit tube are assembled into one piece and are suspended from the top of the apparatus near the funnel. This relieves thermal stress by allowing these parts to flex through the exit O-ring seal. To eliminate icing while the system is open to air, dry nitrogen gas is introduced near the top of the reservoir. It flows between the reservoir and outer wall of the upper chamber and enters the main chamber just above the heater assembly.

Initial tests have verified that the system meets most of its design objectives: The electrical capabilities of the system include the capacitance resolution of 10^{-15} F and current resolution of 10^{-14} A. To minimize degradation of measurement accuracy, lead length to measuring instruments is maintained less than 30 cm.

Noise can arise within the cryostat from a variety of sources, such as the heater, stray pick up due to mechanical motion of wires, and improper electrical isolation of junctions. Most of these problems were cured by proper shielding and by shock mounting vibration sources. Heater noise was eliminated by using a zero crossover 110 VAC power controller. Additional external sources of noise, such as the 110 VAC line and ground loops, have also been identified. Noise from these sources is presently being eliminated. The temperature excursion of the system is from -191 to



(a) Side view, with entrance and exit tubes.



(b) Component parts.

Figure 5. Heater assembly.

400°C. The maximum heating rate is 7 K/s. To go from near liquid nitrogen to room temperature takes about 30 s and to return to near liquid nitrogen temperature takes about 2 min. The temperature stability of the system has not been established but is expected to be near 0.1 K over several hours. The temperature is monitored by either a thermocouple mounted on the thermal transfer block or a forward-biased diode mounted on the ceramic chip within the TO-5 header [1].

The main purpose of the vacuum is to eliminate icing problems. The mechanical pump can evacuate the main chamber to a pressure of 20 mTorr (0.27 Pa) in about 1 min.

The ultimate vacuum is less than 5 mTorr (0.07 Pa) which is more than adequate for these measurements. (M. G. Buehler and L. M. Smith)

Test Patterns — Masks were designed for fabricating various test structures, such as MOS capacitors and *p-n* junctions, which can be used to develop, refine, and intercompare measurement methods which determine:

1. Thermally stimulated properties of *p-n* junctions.
2. Lifetimes by means of junction recovery, open circuit voltage decay, MOS recovery, or junction current-capacitance characteristics.
3. Impurity profiles based on *p-n* junction capacitance-voltage characteristics.
4. Resistivity (or resistance) of various layers.
5. Insulator properties such as the fixed oxide charge density and the interface state density.

The overall objective of these measurements is to count atoms, finding where they are, how many are there, and identifying their physical characteristics. The measurements are also suitable for the evaluation of various fabrication procedures and the identification of reliable processes.

The test pattern consists of an array of 20 individual test structures on a square silicon chip 200 mils (5.08 mm) on a side. The list of test structures is given in table 1. A photomicrograph of the processed chip is shown in figure 6, where the numbers refer to the list given in table 1. As seen in the figure, most test structures are circular for simplified data analysis. The test structures are fabricated with standard bipolar processing using thermally diffused boron and phosphorus. Junctions are gated with metal over the collector oxide. These gates extend from the diffused junction to the diffused channel stop. Junction metal contacts are of the non-expanded variety in that they are confined to junction areas; this simplifies data analysis. These contacts extend over the junction oxide thus sealing the junctions from external contamination. Most of these test structures are adaptions of standard configurations; the contact resistors, the collector resistor, and the base-under-the-emitter sheet resistor are based on original concepts.

(M. G. Buehler and T. F. Leedy)

Reverse Recovery Method — A simple expression was derived for the minority carrier lifetime, τ, in narrow base diodes from the general solution of Byczkowski and Madigan [2] for the storage time, t_s, of a diode operating with a forward current, I_f, and a reverse turnoff current, I_r. The general expression is:

$$\sum_{n=0}^{\infty} \frac{\exp\left\{-\left[1 + (n + \frac{1}{2})^2 (\pi \frac{L}{W})^2\right] \frac{t_s}{\tau}\right\}}{1 + (n + \frac{1}{2})^2 (\pi \frac{L}{W})^2} = \left(1 + \frac{I_f}{I_r}\right)^{-1} \frac{\frac{W}{L} \tanh \frac{W}{L}}{2} . \qquad (1)$$

Table 1 — Planar Test Structures

Number	Test Structure	Major Geometrical Dimension,[a] mil
1	Gated circular junction with diffused channel stop	D = 6
2	Ungated circular junction with diffused channel stop	D = 6
3	Ungated square junction with diffused channel stop	S = 5
4	Gated square junction with diffused channel stop	S = 18
5	Ungated circular junction with diffused channel stop	D = 20
6	Gated circular junction with diffused channel stop	D = 20
7	Gated circular junction (small emitter) with diffused channel stop	D = 20
8	Gated circular junction (large emitter) with diffused channel stop	D = 20
9	Gated circular junction with diffused channel stop	D = 60
10	MOS capacitor over collector with field plate and diffused channel stop	D = 6
11	MOS capacitor over collector with field plate and diffused channel stop	D = 20
12	MOS capacitor over collector with distant field plate and diffused channel stop	D = 20
13	MOS capacitor over base without field plate and diffused channel stop	D = 20
14	Base sheet resistor	
15	Emitter sheet resistor	
16	Metal-to-base contact resistor	
17	Metal-to-emitter contact resistor	
18	Collector resistor	
19	Base-under-the-emitter sheet resistor	
20	Hall effect pattern	
21	Alignment marker	

[a] D = diameter of a circle, S = side of a square. Tolerances should be held to ±0.1 mil. If metric dimensions are desired the diameters should be 0.15 mm (for structures numbered 1, 2, 10), 0.5 mm (5-8, 11-13), and 1.5 mm (9), and the sides should be 0.13 mm (3) and 0.44 mm (4); all tolerances should be held to ±0.002 mm.

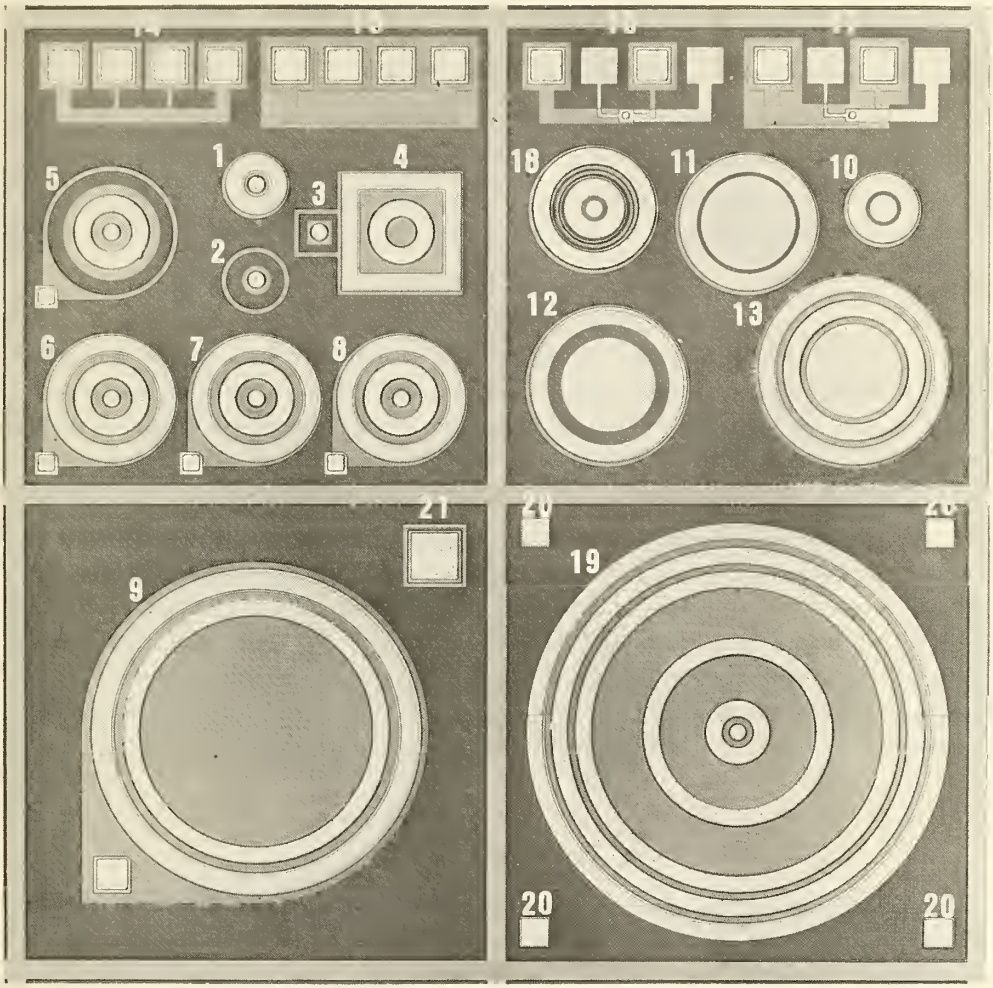


Figure 6. Test pattern, NBS-2, for characterizing the electrical properties of silicon MOS capacitors and p-n junctions. (The 21 elements are identified in table 1. The overall pattern is 200 mils (5.08 mm) on a side.)

where W is the diode base width, the diffusion length $L = (D\tau)^{1/2}$, and D is the minority carrier diffusion coefficient.

For narrow base diodes where $W/L << 3$, just the first term in the series expansion above need be considered. This leads to the expression

$$\ell n(1 + I_f/I_r) = [(1/\tau) + (\pi^2 D/4W^2)]t_s + \ell n\ B \qquad (2)$$

where $B = [1 + (\pi^2 L^2/4W^2)](W/2L) \tanh (W/L)$. The difficulty with this expression is that B contains the unknown τ within L; however, this difficulty can be surmounted if the derivative with respect to t_s is taken. Then the following simple relation results for the lifetime:

$$\tau^{-1} \approx (d/dt_s)\ \ell n(1 + I_f/I_r) - (\pi^2 D/4W). \qquad (3)$$

This expression is easy to solve, for it is not transcendental in τ as are many other lifetime expressions. It does, however, require that the I_f/I_r ratio be measured at two or more t_s values. Preliminary calculations indicate that the lifetime calculated using eq (3) differs from the lifetime calculated using eq (1) by 6.5 percent or less for W/L between 0.2 and 1.5 and $I_f/I_r \geq 2$. (D. C. Lewis and M. G. Buehler)

Plans: The thermally stimulated properties apparatus will be made fully operational, and a second much simpler apparatus for use in a production environment will be constructed. The test mask will be used initially to evaluate in-house fabrication procedures and then to study various measurement methods. Study of simplified analytical procedures for the reverse recovery method will continue with emphasis on the range of validity of the simplified expressions for both wide and narrow base diodes. In addition, study of the injected level dependence of this method will begin.

3.3. GOLD-DOPED SILICON

Objective: To characterize *n*- and *p*-type gold doped silicon in order to develop an energy level model to predict the resistivity of silicon as a function of gold density and to provide inputs for a lifetime model.

Progress: Additional measurements of room temperature resistivity as a function of gold density were compared with theoretical calculations for both *n*- and *p*-type silicon. The calculated curves follow the general trends of the experimental data, but certain, apparently systematic, differences are observed in both types. Investigations to explain these differences were begun.

Resistivity vs. Gold Density in p-Type Silicon — The room temperature resistivity of boron-doped silicon wafers diffused with gold is shown in figure 7 as a function

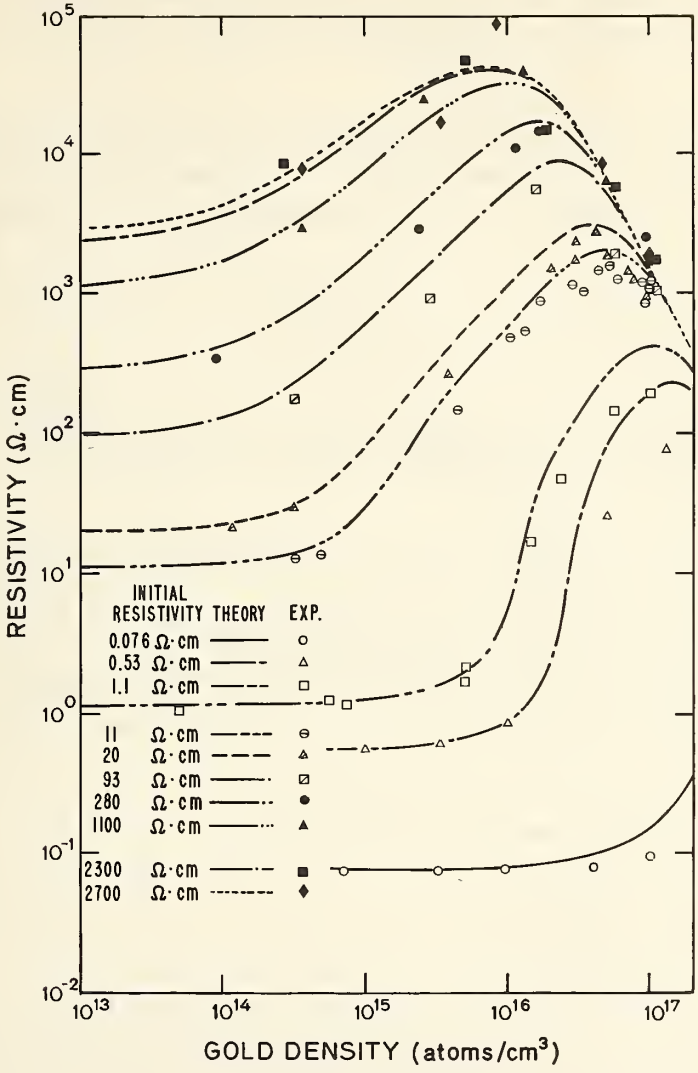


Figure 7. Resistivity as a function of gold density in boron-doped silicon.

of gold density, as determined by neutron activation analysis.* Before the addition of gold, the initial resistivity, ρ_o, at room temperature was 0.076, 0.53, 1.1, 11, 30, 93, 280, 1100, or 2700 Ω·cm as indicated on the figure. The gold density ranged from about 10^{14} cm^{-3} to about 10^{17} cm^{-3}.

Theoretical curves, generated for comparison of the experimental resistivity data as a function of gold density with predictions of the energy-level model for gold-doped silicon, are also shown in figure 7. The curves were derived from calculations based on a solution to the charge balance equation

$$n + N_a^- + N_G^- + N_A^- = p + N_d^+ + N_D^+ \qquad (4)$$

where, for the non-degenerate case of interest here:

$n \approx N_c \exp[(F - E_c)/kT]$ is the electron density,

$p \approx N_v \exp[(E_v - F)/kT]$ is the hole density,

$N_c = 2(2\pi m_e kT/h^2)^{3/2}$ is the density of states in the conduction band,

$N_v = 2(2\pi m_h kT/h^2)^{3/2}$ is the density of states in the valence band,

$N_a^- = N_a/\{1 + g_a \exp[(E_a - F)/kT]\}$ is the ionized (filled) shallow acceptor (boron, etc.) density,

$N_G^- = N_G/\{1 + g_G \exp[(E_G - F)/kT]\}$ is the ionized (filled) gold-coupled shallow acceptor density,

$N_A^- = N_{Au}/(1 + g_A \exp[(E_A - F)/kT]\{1 + g_D \exp[(E_D - F)/kT]\})^{-1}$ is the density of negatively ionized gold (filled acceptors),

$N_d^+ = N_d/\{1 + g_d^{-1} \exp[(F - E_d)/kT]\}$ is the ionized (empty) shallow donor (phosphorus, etc.) density,

$N_D^+ = N_{Au}/(1 + g_D^{-1} \exp[(F - E_D)/kT]\{1 + g_A^{-1} \exp[(F - E_A)/kT]\})^{-1}$ is the density of positively ionized gold (empty donors),

m_e, m_h are the electron and hole effective masses,

k is Boltzmann's constant,

T is absolute temperature,

h is Planck's constant,

F is the Fermi energy,

E_c, E_v are the energies of the conduction and valence band edges,

N_a, N_G, N_{Au}, N_d are the densities of shallow acceptors, gold-coupled shallow shallow acceptors, gold, and shallow donors,

g_a, g_G, g_A, g_D, g_d are the degeneracy factors† of the shallow acceptor, the

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* The activation analyses were performed by T. Gills of the NBS Activation Analysis Section.

† The degeneracy factor is defined by Blakemore [1] as referring to the probability that a level contains an electron.

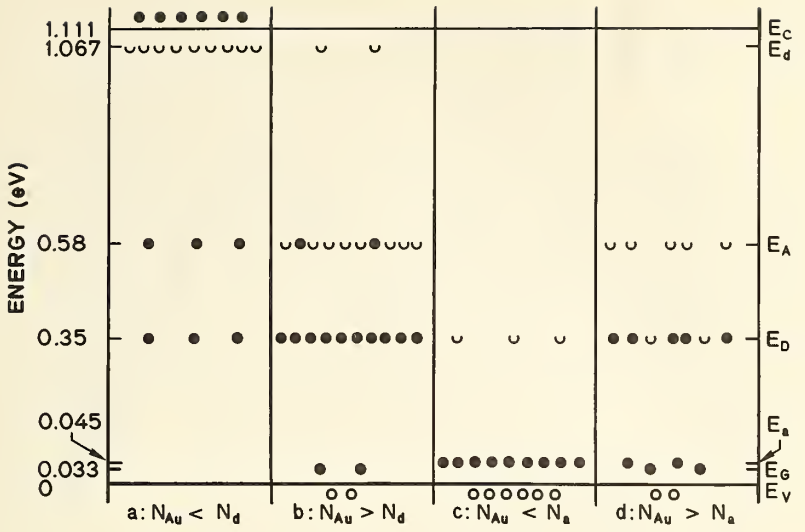

Figure 8. Energy band diagram at 298 K for silicon doped with gold and either phosphorus or boron. (In this model it is assumed that the energy differences $E_A - E_c$ and $E_D - E_v$ do not vary with temperature. The energies given for the shallow donor and acceptor levels are appropriate for phosphorus and boron, respectively. No gold-coupled shallow acceptors are shown for cases a and c as their density is negligible when the gold density is less than 10^{16} cm^{-3}. Levels occupied by electrons are shown as •; levels not occupied by electrons are shown as ∪.)

gold-coupled shallow acceptor, the gold acceptor, the gold donor, and the shallow donor, and

E_a, E_G, E_A, E_D, E_d are the energies of the shallow acceptor, the gold-coupled shallow acceptor, the gold acceptor, the gold donor, and the shallow donor.

For the assumed model, shown in figure 8, T = 298 K; $E_D - E_v = 0.35$ eV and $E_A - E_v = 0.58$ eV [2]; $E_c - E_v = 1.111$ eV [3], $m_e = 1.18\ m_o$ [4], and $m_h = 0.81\ m_o$ [4] (m_o = the free electron mass), so $n_i = \sqrt{np} = 9.6 \times 10^9$ cm^{-3}. The lattice mobility [5] and impurity mobility [6] were combined reciprocally to obtain the carrier mobility used in the calculation of the resistivity. The model also includes the gold-coupled acceptor with $E_G - E_v = 0.033$ eV [7]. Experimental data reported previously (NBS Tech. Note 727, pp. 12-13) suggest that N_G increases approximately as the third power of the gold density with a value of 4.5×10^{15} cm^{-3} for $N_{Au} = 1 \times 10^{17}$ cm^{-3}. In accord with other shallow acceptors in silicon [8], g_G was taken as 4. $E_a - E_v$ and g_a were taken as 0.045 eV and 4, respectively, values appropriate to boron [8].

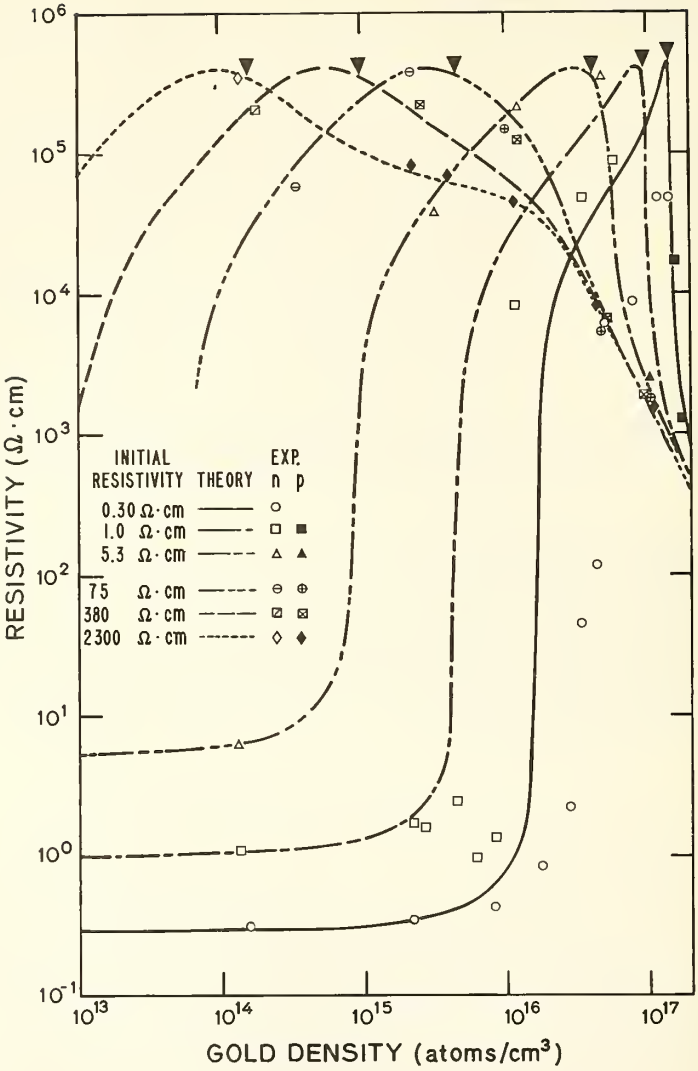

Figure 9. Resistivity as a function of gold density in phosphorus-doped silicon. (To the left of the ▼, the Hall coefficient is negative; to the right it is positive.)

From trial fits to the resistivity data for n-type, gold-doped specimens, g_A was chosen to be $1/8$. None of these last four values enters significantly into the present calculations. From trial fits to these resistivity data, g_D was chosen to be 8. For each crystal, N_a was calculated from eq (4) with the assumption that $N_d = 0$ and $N_{Au} = 0$; values are listed in table 2.

Although the calculated curves generally fit the experimental data, there are some deviations which appear to be systematic. One possible source of these deviations may be the discrepancy between the computed doping densities for low resistivity crystals (<1 Ω·cm) shown in the table and those obtained experimentally [9]. This discrepancy arises in part because of difficulties with the calculation of ionized impurity and mixed mobilities. Two other possible sources of the deviations, compensation by donor impurities unintentionally introduced during the gold diffusion and the previously observed discrepancy between total and electrically active gold [10], are also being considered. Errors in the activation analysis may also contribute to the discrepancies.

Resistivity vs. Gold Density in n-Type Silicon — The measured room temperature resistivity of phosphorus-doped silicon wafers diffused with gold is shown in figure 9. Before the addition of gold the initial resistivity, ρ_o, at room temperature was 0.3, 1.0, 5.3, 75, 380, or 2300 Ω·cm as indicated on the figure. The gold density ranged from about 10^{14} cm^{-3} to about 10^{17} cm^{-3}. At large gold densities, the conductivity type converts from n to p. Specimens with positive Hall coefficients are plotted with solid symbols in the figure. For the lower resistivities a sharp increase in resistivity is observed when the gold density is between one and two times the density of the shallow donor in agreement with earlier observations [10].

Theoretical curves, based on the energy-level model described above, were calculated for each set of data. The theory predicts that the resistivity increases sharply when the gold and shallow donor densities are equal while the experimental results show the increase occurs when the gold density is up to twice the shallow donor density. Elsewhere, however, the theoretical and experimental plots have generally similar form. For the curves plotted in figure 9, $E_d - E_v$ and g_d were taken as 1.067 eV and $1/2$, respectively, values appropriate to phosphorus [8]. Other parameters were chosen as described above; values of N_d, calculated as above for each crystal, are listed in table 2. (W. R. Thurber and W. M. Bullis)

Plans: Hall effect and resistivity measurements as a function of temperature will be resumed to obtain additional data on the energy levels of gold in silicon. As mentioned above, the calculated shallow dopant densities for low resistivity silicon differ somewhat from accepted values due to difficulties with the calculation of ionized impurity and mixed mobilities. Ways of combining the ionized impurity and

Table 2 — Boron or Phosphorus Doping Densities of Silicon Crystals Computed from Measured Room Temperature Resistivity

p-type		*n*-type	
ρ_o, Ω·cm	N_a, cm^{-3}	ρ_o, Ω·cm	N_d, cm^{-3}
0.076	2.28×10^{17}		
0.53	2.59×10^{16}	0.30	1.60×10^{16}
1.1	1.18×10^{16}	1.0	4.62×10^{15}
11	1.20×10^{15}	5.3	8.60×10^{14}
20	6.55×10^{14}		
93	1.40×10^{14}	75	6.10×10^{13}
280	4.72×10^{13}	380	1.20×10^{13}
1100	1.18×10^{13}		
2300	5.76×10^{12}	2300	2.00×10^{12}
2700	4.80×10^{12}		

lattice mobilities will be compared and the calculated values will be checked against experimental ones.

3.4. INFRARED METHODS

Objective: To study infrared methods for detecting and counting impurity and defect centers in semiconductors and, in particular, to evaluate the suitability of the infrared response technique for this purpose.

Progress: Infrared response measurements were completed on specimens of five germanium crystals representative of material currently available for use in lithium-drifted germanium gamma-ray detector fabrication. The diameters of the crystals were approximately 5 cm. For two of the specimens, NBS-817 and NBS-818, IRR spectra of type 2, characteristic of detectors which exhibit hole trapping, were obtained (NBS Tech. Note 733, pp. 17-21). These results are in agreement with the exhibition of hole trapping by the detectors. The IRR spectra of diodes NBS-819 and NBS-820 were also of type 2, and that of NBS-821 was identified as type 5, characteristic of detectors which exhibit electron trapping. The detector characteristics of these latter three diodes have not yet been determined. (H. E. Dyson and A. H. Sher)

The IRR spectrum of NBS-14S, a lithium-drifted silicon detector fabricated at NBS, was obtained both before and after heating in an argon atmosphere to 800°C for

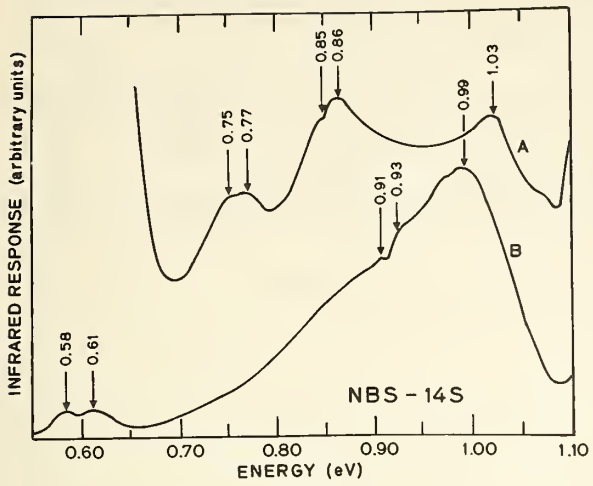

Figure 10. Effect of heat treatment on IRR spectrum of lithium-drifted silicon detector NBS-14S.

approximately 3 h. The effect of heat treatment, shown in figure 10, is similar to that observed in germanium (NBS Tech. Note 598, pp. 14-15). The major features in the IRR spectrum before heat treatment (curve A) are absent in the spectrum after heat treatment (curve B). In the case of germanium, this behavior was in agreement with findings reported in the literature of a continuum of energy levels resulting from thermal damage rather than discrete levels. (Y. M. Liu, H. E. Dyson, and A. H. Sher)

Plans: Study of IRR of germanium and silicon diodes will continue with emphasis on the identification of energy levels and the determination of their effects on detector performance and IRR response. Further IRR analysis on silicon devices not compensated with lithium will be resumed.

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4. SEMICONDUCTOR PROCESS CONTROL

4.1. DIE ATTACHMENT EVALUATION

Objective: To evaluate methods for detecting poor die attachment in semiconductor devices with initial emphasis on the determination of the applicability of thermal measurements to this problem.

Progress: Modifications of the revised TRUMP [1] thermal analysis computer program for use on the NBS computer were completed. Modeling of the various structures to be analyzed has been undertaken. Initial computer runs using both a simplified mesa diode on a TO-5 header and a round silicon chip on an infinite heat sink indicate junction temperatures that are in excess of those that would reasonably be expected. A more detailed study of the modeling and modeling input procedure has been undertaken.

(R. L. Gladhill)

The series of measurements of steady-state and transient thermal response on transistors was completed. Measurements were made on transistors with controlled voids that were approximately 15 and 25 percent of the 35-mil (0.89-mm) square chip bonding area. The voids were formed by ultrasonically machining dimples, 15 and 20 mils in diameter, respectively, into the bonding surface of the TO-5 header. Measurements on transistors with 40-percent void areas were reported previously (NBS Tech. Note 773. pp, 22-24).

For the steady-state measurements, the heating current and voltage were 50 mA and 10 V, respectively. The transient measurements were made 10 μs after the termination of a 5-ms wide power pulse; the heating current and voltage were 150 mA and 10 V, respectively. The spread in thermal response of the devices with the 15-percent void areas was found to be significantly larger than in that of the other devices. Although two groups of transistors were bonded with 15-percent void areas, both thermal response measurements and radiographs indicated that there was poor bonding in the region around the dimples in all but five of these devices from one of the groups. For comparison, nine control devices without voids bonded at the same time were also measured. Nine control devices without voids were also measured with the group of nine devices with 25-percent void areas.

The average percent increase in steady-state and transient thermal response of the devices with voids over their respective controls is shown as a function of percent void area in figure 11. The data presented indicate that, at least for this particular device, measurement of steady-state thermal response (or thermal resistance) would not be an acceptable industrial screening technique to cull out devices with various size voids due to the low sensitivity of the technique, while the transient

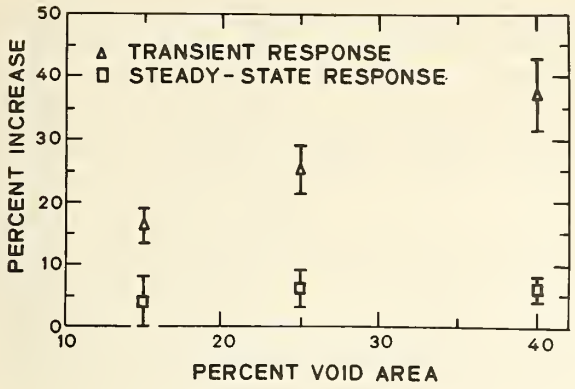


Figure 11. Percent increase in average junction-to-case temperature difference of transistors with voids over that of their respective controls measured under steady-state and transient conditions as a function of percent void area in the transistor die attachment. (Error bars indicate one sample standard deviation above and below the mean.)

thermal response for a particular heating power pulse can discriminate between devices with and without voids.

Measurements of transient and steady-state thermal response were also made on ten commercial transistors that used the same 35-mil (0.89-mm) square transistor chip that was used in the in-house bonded devices. The commercially bonded chips were in solid metal TO-5 cans while the in-house bonded chips were attached to standard iron-nickel-cobalt alloy, glass-backed TO-5 headers. Although the thermal resistance of the two classes of devices is quite different, the thermal resistance of the in-house, glass-backed, devices being approximately 60°C/W and that of the solid metal encased devices being approximately 40°C/W, the average junction-to-case temperature difference for the 5 ms heating power pulse in the commercial devices was 20.3°C (excluding one poorly bonded device), and that for the controls for the in-house bonded devices was 21.3°C. The sample standard deviation in both cases was 0.4°C. Thus, the in-house control of the die-bonding process appears to be of the same order as for the commercially bonded devices.

Long-term, single-operator measurements of steady-state and transient thermal response were initiated to check the repeatability that can be achieved with the transistor die attachment evaluation equipment. Thus far, 12 sets of measurements have been made on two controls and two transistors with 40-percent void areas. Repeatability measurements of transient thermal response, for a heating power pulse of 5 ms, are also being made with the device mounted in a standard socket instead of in the temperature controlled heat sink. (F. F. Oettinger and R. L. Gladhill)

Specimens are being prepared for an experimental study of the relationship between thermal response and voids in power transistor die attachment. The study calls for three groups of 24 devices. Each group consists of 12 *n-p-n* silicon power transistors, 60 mils (1.52 mm) square, bonded to steel, with gold plated molybdenum pad, TO-66 headers with 26-, 34-, or 43-mil (0.66-, 0.86-, or 1.09-mm) diameter dimples ultrasonically machined into the bonding surface to produce voids that are approximately 15, 25, or 40 percent of the total chip bonding area, respectively, and 12 control devices without voids. (T. F. Leedy and J. Krawczyk)

Plans: The long-term, single-operator measurements of steady-state and transient thermal response will be completed. Upon completion of the bonding of power transistors on TO-66 headers with various size controlled voids, measurements of thermal response will be made on the transistors for evaluation of the die adhesion. The analysis of heat flow to determine the limitations of thermal response techniques for detecting poor die adhesion in the diodes previously investigated will resume.

4.2. WIRE BOND EVALUATION

Objective: To survey and evaluate methods for characterizing wire bond systems in semiconductor devices, and where necessary, to improve existing methods or develop new methods in order to detect more reliably those bonds which will eventually fail.

Progress: The experimental phase of the investigation of the effects of geometrical variables on the destructive, double bond pull test was completed. Pull strength was measured as a function of loop height, pull angle α, pull angle β, and position of pulling hook for two-level bond pairs. These measurements yielded results which agreed with theoretical predictions. The vibration modes of two unconventional ultrasonic bonding tools were studied during bonding. One was significantly different from conventional tools.

Pull Test Evaluation — Measurements of pull strength as a function of bond loop height for two-level bonds were repeated using bonds made on two different bonding machines. Machine A had been used in previous two-level studies, while machine B had not. For bond pairs made on both bonding machines with the first bond either to the high pad or to the low pad, the experimental results were in agreement with theoretical calculations based on resolution of forces (NBS Tech. Note 555, pp. 31-25). Figure 12 shows the data obtained for bonds made on machine B. Results previously reported (NBS Tech. Note 754, pp. 21-23) indicated that agreement between experiment (using machine A) and theory was obtained only for bond pairs where the first bond was made to the high pad. Reexamination of the data has shown that the theoretical analysis applicable to single-level bonds had been incorrectly applied to the data.

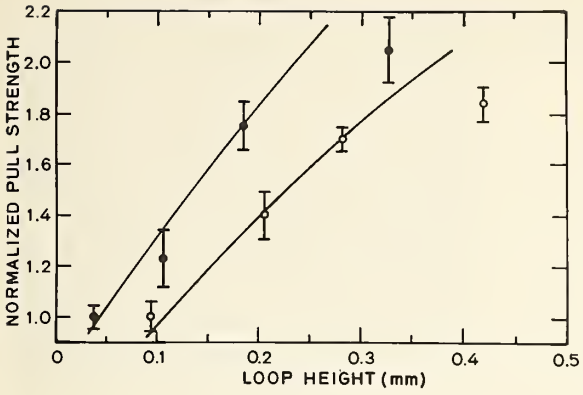
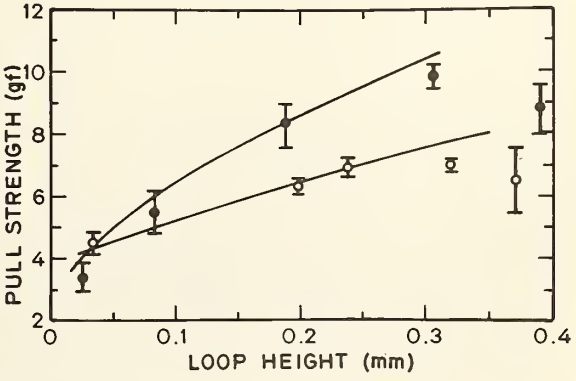


Figure 12. Measured pull strength of unannealed, round-wire, two-level bonds as a function of loop height above the high pad. (The values are normalized to the mean pull strength at the lowest loop height. Solid points are for the first bond made on the high pad; open points are for the first bond made on the low pad. The data points represent the mean of 10 bonds, all of which ruptured at the heel of the first bond. Error bars indicate one sample standard deviation above and below the mean. The solid curves were calculated by resolution of forces.)

Figure 13. Measured pull strength of unannealed, round-wire, two-level bonds as a function of loop height above the high pad. (Solid points are for the first bond made on the high pad; open points are for the first bond made on the low pad. The data points represent the mean of 10 bonds, all of which ruptured at the heel of the first bond. Error bars indicate one sample standard deviation above and below the mean. The solid curves were calculated by resolution of forces.)



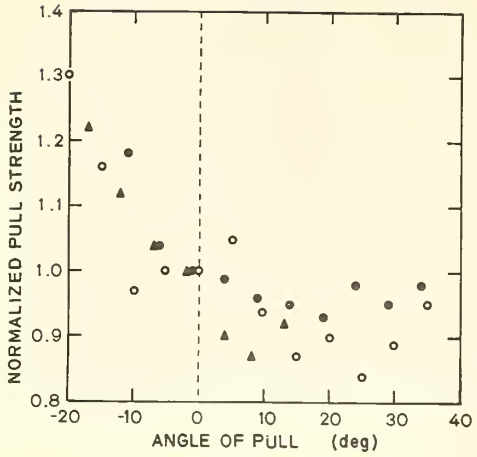


Figure 14. Measured pull strength of bond pairs as a function of the angle of pull in the plane of the bond loop. (The values are normalized to the mean pull strength at 0 deg. Solid points are for two-level bond pairs made with the first bond to the high pad (circles) and with the first bond made to the low pad (triangles); open circles are previously reported data for single-level bond pairs. Except for the solid circles, which represent the mean of 30 bonds, the data points represent the mean of 10 bonds, all of which ruptured at the heel of the first bond. Error bars have been omitted to reduce clutter; typically the sample standard deviation is between 0.05 and 0.1.)

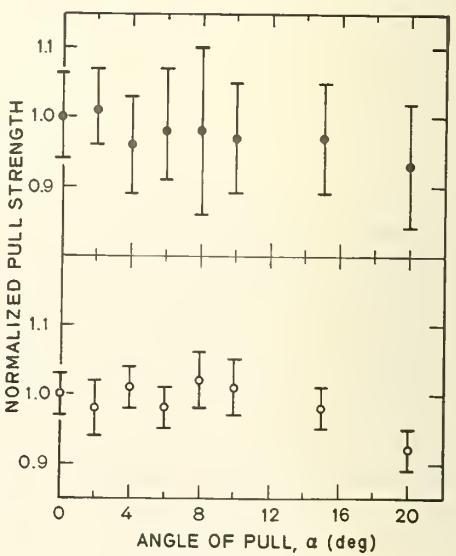


Figure 15. Measured pull strength as a function of angle of pull, α, for two-level bond pairs. (The values are normalized to the mean pull strength at α = 0 deg. Solid points are for bond pairs made on bonding machine A. Open points are for bond pairs made on machine B. The data points represent the mean of 10 bonds. Error bars represent one sample standard deviation above and below the mean.)

Figure 13 shows the results of applying the correct theoretical analysis [1] to the previously reported two-level data. It is evident that agreement is obtained for the first bond made either to the high pad or to the low pad. In these and subsequent experiments the high pad was about 0.25 mm above the low pad and the bond-to-bond spacing was 1.0 mm.

The effect of varying the pull angle β was studied for two-level ultrasonic bond pairs made with machine A. The angle β is the angle between the direction of pulling force and the normal to the lines joining the bond terminals in the plane of the bond loop; it is taken as positive in the direction toward the second bond (NBS Tech. Note 754, pp. 21-22). Measurements of pull strength were made by tilting the substrate while pulling the loop vertically. The results are shown in figure 14 both for bond pairs with the first bond made to the high pad and for bond pairs with the first bond made to the low pad. The pull angle shown is β for the former case and $-\beta$ for the latter. For comparison, previously reported data for single-level bond pairs are also included; in this case the pull angle is ϕ, the angle between the direction of pulling force and the normal to the substrate. It can be seen that the trend in all three cases is about the same.

The effect of varying the pull angle α was studied on bond pairs made on both machines with the first bond made to the high pad. The angle α is the angle between the direction of pulling force and the normal to the substrate in the plane perpendicular to both the substrate and the plane of the bond loop. Measured pull strength, normalized to its value for $\alpha = 0$, is plotted as a function of α for both cases in figure 15. The data include only failures due to rupture of the first bond and are in general agreement with the measurements of pull strength made on single-level bond pairs (NBS Tech. Note 743, pp. 27-28).

The effect of varying the position of the pulling hook on pull strength was studied on two-level bond pairs made on machine A with the first bond made either to the low pad or to the high pad. The results, plotted in figure 16 as measured pull strength normalized to its value at midpoint (0.5 mm) as a function of hook position, are in agreement with calculations based on resolution of forces except for positions between midpoint and the low pad. In this region the pulling hook was observed to slip along the wire loop toward the midpoint position; thus the measured pull strength lies above the predicted value.

These measurements mark the completion of the experimental phase of the investigation of the effects of the geometrical variables on the pull test. The measurements carried out during this phase (NBS Tech. Notes 717, pp. 28-29; 727, pp. 38-43; 733, pp. 28-30; 743, pp. 27-31; 754, pp. 21-23; and 773, pp. 25-27) have shown that the variations in measured pull strength as functions of bond loop height and position of the pulling hook are in agreement with those predicted by resolution-of-forces [2]

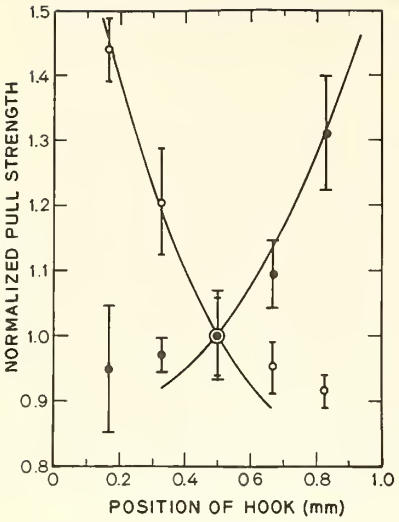


Figure 16. Measured pull strength of two-level bond pairs as a function of the position of the pulling hook. (The values are normalized to the mean pull strength at mid span, 0.5 mm. Solid points are for the first bond made to the high pad; open points are for the first bond made to the low pad. In each case the second bond is at 0 mm and the first bond is at 1.0 mm. The data points represent the mean of 10 bonds all of which ruptured at the heel of the first bond. Error bars indicate one sample standard deviation above and below the mean. The solid curves were calculated by resolution of forces.)

(NBS Tech. Note 726, pp. 60-68) for single- and two-level unannealed wire bond pairs provided that the ratio of the loop height, h, to bond-to-bond spacing, d, was less than about $\frac{1}{3}$. For annealed bonds, agreement was not found. This was attributed to the fact that the stretching of the wire loop during pulling always resulted in h/d values greater than $\frac{1}{3}$.

The slight decrease in measured pull strength with increasing pull angle α in both single- and two-level bond pairs, more pronounced on bonds with large heel deformation, appears to be a result of the twisting or tearing of the bond heel as the wire is pulled out of the plane normal to the substrate plane. In the series of measurements on the effects on pull strength of varying the pull angle β, for both single- and two-level unannealed wire bonds, a large decrease in pull strength was observed as β went from -45 to 0 deg; as β went from 0 to +45 deg, the decrease was much less marked.* This is consistent with the facts that 1) the first bond is stronger than the second bond, and 2) the measured pull strength is lower when the larger component of force is applied to the first bond, and higher when applied to the second bond.

In those cases in which the validity of the resolution-of-forces calculations has been experimentally confirmed, it is now possible to determine the effects of

*The angle β is defined as negative when the pulling force is directed towards the first bond.

varying the geometrical variables for various device package configurations. This information can be used to determine, prior to direct interlaboratory comparisons, the expected variation of the pull test measurement in a variety of situations that approximate application of the test in industrial use.

(A. H. Sher, C. A. Main, and K. O. Leedy)

Bonding Tool Technology — The feed holes for round or ribbon wire in ultrasonic bonding tools are generally very rough and have sharp corners on the exit hole after electro-etch-machining. These defects may scratch the surface of the bonding wire. Small shavings, which have occasionally been observed to come from the wire, could enter the device, causing electrical shorts. In some cases the wire may catch on the sharp points resulting in a non-uniform loop height. An inexpensive, electric vibrating engraving tool was used to polish the wire feed hole in the bonding tool. To do this a steel or bronze wire was fastened by a clamp or soldered to the engraving tool tip and coated with 3 μm diamond paste. The coated wire was inserted into the wire feed hole in the bonding tool. The vibrating motion, approximately 7200 strokes per minute, polished the hole and smoothed the edges in about 30 s. Care has to be taken to adjust the stroke of the engraver to prevent the polishing wire from damaging the heel corner of the bonding surface. This technique is also applicable to polishing the capillary hole in thermocompression bonding tools. (H. K. Kessler)

Studies of Ultrasonic Bonding Tools — Past studies of ultrasonic bonding tools (NBS Tech. Notes 520, p. 32; 527, p. 32) have been confined to tools of conventional design made of tungsten carbide. The vibration amplitude of these tools usually remains approximately constant during bonding. Any significant amplitude changes that may occur generally result from the characteristics of the particular transducer or ultrasonic power supply rather than from the tool.

Recently, a tungsten carbide bonding tool, of thin-line design, sometimes called a 60 deg tool because of the angle that the wire makes with the substrate, and a titanium carbide tool of conventional design have been introduced. Since these two tools represent significant changes from conventional ones, a study was initiated to compare all three types. The data reported here were taken using a single commercial, fixed-tuned, constant-current ultrasonic power supply and matching ferrite-drive transducer. However, additional tests were performed using a nickel magnetrostrictive transducer. The vibration amplitude of the tool was measured with a laser interferometer; measurements were also made with a capacitor microphone which had a 4 mil (0.1-mm) diameter tip (NBS Tech. Note 520, pp. 63-65) [3].

All amplitude measurements were made by synchronizing the laser interferometer at an appropriate time during normal bond formation, generally within the final 5 ms. The actual measurement is made in only about 10 μs. The results were displayed on a

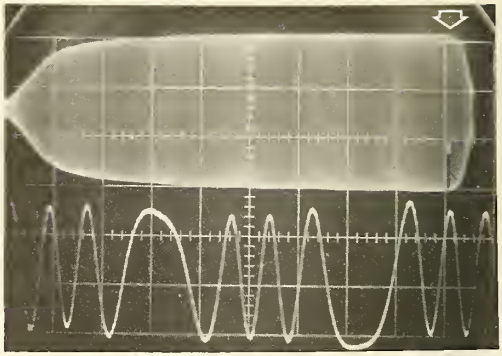


Figure 17. Photograph of typical oscilloscope traces used in measuring modal patterns of ultrasonic bonding tools. (The upper trace is the vibration amplitude envelope as detected by a capacitor microphone; the lower trace is a laser interferometer pattern taken at the synchronization point (arrow). Horizontal scale: 5 ms/div (upper trace), 2 μs/div (lower trace). Vertical scale: 20 mV/div.)

double beam oscilloscope and photographed. A typical photograph is shown in figure 17. The upper trace is the tool tip vibration envelope detected with a capacitor microphone. The arrow near the end of the envelope indicates the time of the laser interferometer measurement. The lower trace is the interferometer wave pattern. Data taken from traces such as this one were used to generate the modal patterns shown in subsequent figures. The synchronization technique was also used to expand part of the vibration amplitude envelope detected by the capacitor microphone in order to reveal any waveform distortions which might be present as shown in subsequent figures.

Laser interferometer measurements were made for the free vibration condition, in which the tool was unloaded, and for a normal bonding load of 25 gf (0.24 N). Measurements on the unloaded tool were made with the end of the transducer horn vibrating with an amplitude of approximately 30 μin. (0.76 μm) peak to peak (p-p). This is a typical horn amplitude for the normal bonding of 1-mil (25-μm) diameter wire; the modal pattern of the bonding tool is generally such that the vibration amplitude is between 40 and 50 μin. (1.0 and 1.3 μm) p-p at the tip. In the case shown, the horn amplitude decreased about 25 percent during bonding. The changing modal pattern of conventionally designed tools tends to increase the tip amplitude and thus compensate for the horn amplitude decrease. For convenience of display both the loaded and unloaded modal patterns shown in figures 18 to 20 have been normalized to a constant horn amplitude. Thus while the loaded curves may have a higher relative amplitude at the tool tip than the unloaded ones, the actual amplitudes under normal operating conditions may be almost equal.

The modal patterns and vibration amplitude envelopes of a tungsten carbide tool of conventional design are shown in figure 18. Loaded nodes are seldom as sharp or as complete as the unloaded ones as can be seen in the modal patterns of figure 18(a). The nodal position during bonding is a function of the mechanical loading of the tool tip during bonding; this is primarily a function of the wire deformation, which was

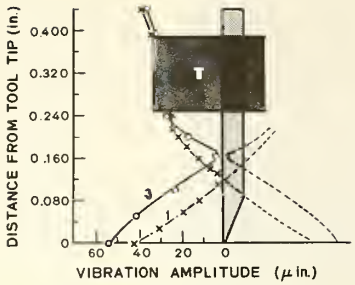
approximately 1.6 for the case shown. A smaller deformation, such as 1.2, may result in a nodal rise of only 20 to 25 mils (0.51 to 0.64 mm) from the unloaded position. This tool showed no significant change in tip amplitude during bonding, but such changes would be expected to become more significant as the bonding force is increased for bonding larger diameter wire; Dushkes [4] has reported reduction of tip amplitude under such conditions.

The upper trace in figure 18(b) is the vibration amplitude envelope of the unloaded tool as detected by the capacitor microphone placed approximately 35 mils (0.9 mm) above the tool tip. The lower undistorted sine wave was expanded from the envelope at the position of the arrow. These traces are typical of those observed under unloaded conditions on all the tools in the present study; unloaded traces are not pictured for subsequent tools.

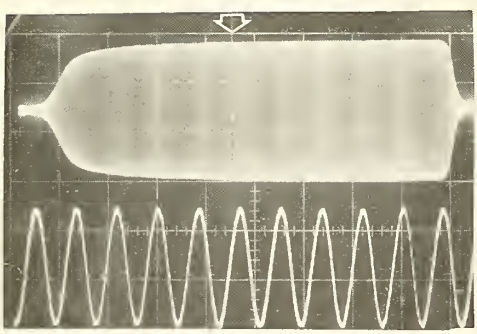
The traces in figure 18(c) were taken from the same tool during the formation of a good metallurgical weld. Although the envelope (upper trace) is nearly the same as that of the unloaded case, some waveshape distortion is apparent in the expanded waveform (lower trace). The degree of distortion can vary considerably if a different transducer or a bonding tool of similar design and material but from a different manufacturer is used. Some tools of conventional design show no waveshape distortion during bonding.

The modal patterns of a titanium carbide tool of conventional design under both loaded and unloaded conditions are shown in figure 19(a). Titanium carbide has a much lower density and is more flexible than tungsten carbide. The nodal position is approximately 20 mils (0.5 mm) above that of a tungsten carbide tool of the same geometry (see figure 18(a)); as a result, the vibration amplitude of the unloaded tool tip is about 20 percent greater for the same transducer drive. As soon as the tool presses against the wire with the normal 25-gf (0.24-N) bonding force, the node becomes blurred and almost ceases to exist. However, except for this difference, the modal pattern has the same general appearance as that of the tungsten carbide tool during bonding. The traces in figure 19(b) were taken on the titanium carbide tool under the same loading conditions as the traces on the tungsten carbide tool shown in figure 18(c). Although the envelope (upper trace) is nearly identical with that of the unloaded tungsten carbide tool (figure 18(b)), some distortion is evident in the expanded waveform (lower trace).

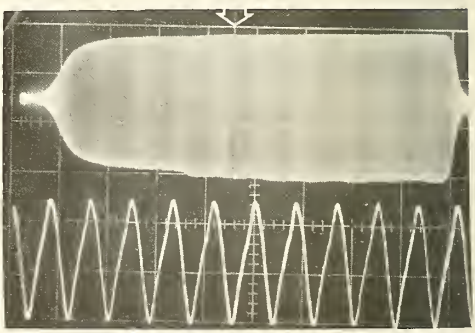
Characteristics of the tungsten carbide tool of a thin-line design are shown in figure 20. This tool is intended to fit into very small spaces such as those encountered in forward, or post-to-die, bonding. Preliminary studies suggested that this tool had rather unusual operating characteristics so the study of loading effects was more thorough than that undertaken for either of the other types of tool.



(a) Modal patterns: Curve 1, unloaded; Curve 3, near end of bonding cycle. The symmetry of the vibration is indicated by the dotted curves; these mirror-image amplitude curves are omitted for subsequent figures. The large dark area (T) represents the position and amplitude of the transducer horn. Note: 0.010 in. ≈ 0.25 mm; 10 μin. ≈ 0.25 μm.

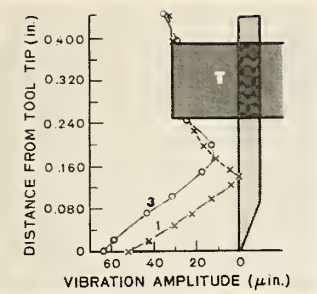


(b) Vibration amplitude patterns for unloaded tool.

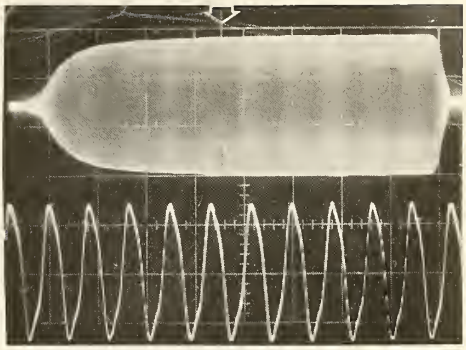


(c) Vibration amplitude patterns for tool during 75-ms long bonding cycle.

Figure 18. Modal patterns and vibration amplitude envelopes of a tungsten carbide bonding tool of conventional design. (In (b) and (c) the upper trace is the vibration amplitude envelope, measured 35 mils (0.9 mm) above the tool tip; the lower trace is the amplitude waveform expanded at the time indicated by the arrow. Horizontal scales: 10 ms/div (upper trace); 20 μs/div (lower trace). Vertical scales: 20 mV/div.)



(a) Modal patterns: Curve 1, unloaded; Curve 3, 5 ms before end of bonding cycle. Note: 0.010 in. ≈ 0.25 mm; 10 μin. ≈ 0.25 μm.



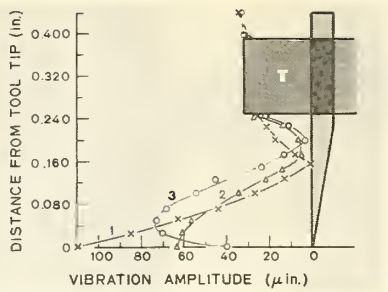
(b) Vibration amplitude patterns for tool during 75-ms long bonding cycle.

Figure 19. Modal patterns and vibration amplitude envelope of a titanium carbide bonding tool of conventional design. (In (b) the upper trace is the vibration amplitude envelope, measured 35 mils (0.9 mm) above the tool tip; the lower trace is the amplitude waveform expanded at the time indicated by the arrow. Horizontal scales: 10 ms/div (upper trace); 20 μs/div (lower trace). Vertical scales: 20 mV/div.)

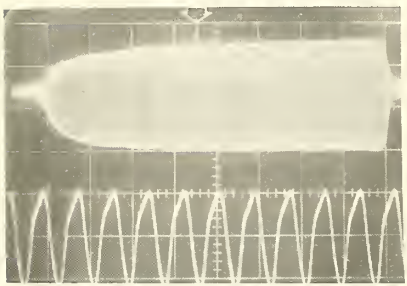
The laser interferometer was synchronized to measure the vibration amplitude 7 ms after the initiation of bonding and again 5 ms before the end of the bonding cycle for each bond made. Thus it was possible to obtain two different modal patterns for the tool during actual bonding in addition to the unloaded modal pattern as shown in figure 20(a). At each position on the tool, both data points obtained under loaded conditions were obtained during the same bonding cycle. Although severe loading of the tip, termed "lug down" and believed to contribute to erratic bonding by Dushkes [4], is apparent at the beginning of the cycle, it is especially pronounced at the end of the cycle. An interesting feature of this tool is that the final tool tip vibration amplitude is less than two-thirds of the initial amplitude.

The vibration amplitude envelope at a position approximately 35 mils (0.9 mm) above the tool tip near the knee of the loaded modal pattern is shown in figure 20(b). This envelope is asymmetrical and its amplitude increases with time in a way similar to the envelopes shown in figures 18(c) and 19(b); this is in agreement with the modal pattern in figure 20(a). The distortion in the expanded waveshape in the lower trace also exhibits asymmetry.

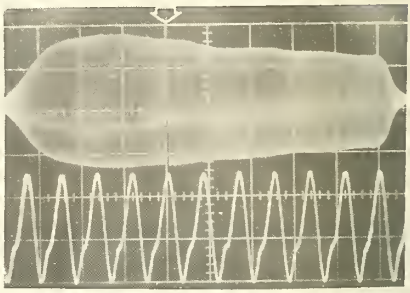
The vibration amplitude envelope and the distortion in the expanded waveshape at a position within 5 mils (0.13 mm) of the bottom of the tool exhibit substantially different characteristics from those observed higher on the tool. These characteristics change from bond to bond. Traces for two successive bonds are shown in figures 20(c) and 20(d). Both bonds resulted in good metallurgical welds and were visually



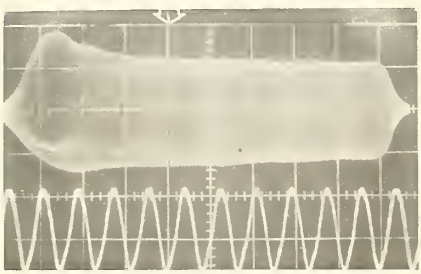
(a) Modal patterns: Curve 1, unloaded; Curve 2, 7 ms after beginning of bonding cycle; Curve 3, 5 ms before end of cycle. Note: 0.010 in. ≈ 0.25 mm: 10 uin. ≈ 0.25 um.



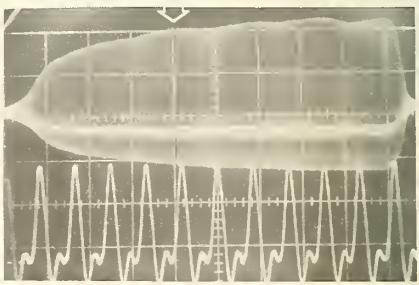
(b) Vibration amplitude patterns, measured 35 mils (0.9 mm) above the tool tip, for a bonding cycle which resulted in a good metallurgical weld.



(d) Vibration amplitude patterns, measured at the tool tip, during second of two successive bonding cycles which resulted in good metallurgical welds.



(c) Vibration amplitude patterns, measured at the tool tip, during first of two successive bonding cycles which resulted in good metallurgical welds.



(e) Vibration amplitude patterns, measured at the tool tip, during formation of poor bond. This bond was intentionally made above a void under the bonding pad.

Figure 20. Modal patterns and vibration amplitude envelopes of a tungsten carbide tool of thin-line design. (In (b)-(e) the upper trace is the vibration amplitude envelope; the lower trace is the amplitude waveform expanded at the time indicated by the arrow. Horizontal scales: 10 ms/div (upper trace (b)); 5 ms/div (upper trace (c)-(e)); 20 μs/div (lower trace (b)-(e)). Vertical scales: 20 mV/div ((b)-(e)).)

identical. These traces, taken on short (∿45 ms) bonding cycles were similar to others at this position taken on the longer (∿75 ms) bonding cycle. The initial peak-to-peak vibration amplitudes of the tool tip during these and other bonds ranged from 30 to 55 percent higher than the final amplitude; it should be noted that ultrasonic power is proportional to the square of the vibration amplitude. This amplitude variation was not observed in either of the other tools studied; in those cases, changing either the microphone position or the bonding time resulted in no significant change in the envelope or the distortion of the expanded waveshape.

Vibration amplitude characteristics of the bonding tool tip during formation of a bond intentionally placed over a void under the pad to obtain a poor metallurgical weld are shown in figure 20(e). The appearance of the vibration amplitude envelope is more characteristic of a position higher on the tool (see figure 20(b)). Distortion of the expanded waveshape is the most severe observed in these tests.

These results suggest that the thin-line tool apparently has some ability to compensate for slight differences in the substrate or wire condition. On the basis of limited tests, not described in detail, it appears that this tool requires careful control of the extension of the tool below the transducer horn in order to achieve the most reproducible results.

This study was limited to short bonding tools, 0.437 in. (11.1 mm) long, installed with a 0.25-in. (6.4 mm) extension. The results reported above cannot be assumed to apply either to short tools installed with a different extension or to other tools, such as 0.828-in. (21.0-mm) long tools that operate with two nodes below the horn.

(G. G. Harman)

Analysis of Failed Wire Bonds — In the course of preparing a paper for presentation at the 1973 Reliability Physics Symposium [5] information was collected regarding methods for opening device packages and methods for removing encapsulating material. This information is summarized in tables 3 and 4. (H. A. Schafft)

Plans: Preliminary analyses of the effects on measured pull strength of varying the pull test parameters using the resolution-of-forces calculations will be begun for representative device package types. The writing of a summary of the experimentally-measured effects and analysis of the results will be begun for future publications as an NBS Technical Note. With the planned arrival of a beam lead bonding machine next quarter, a study of beam lead bonding tests will be begun. The study of the pull test will be extended to include bonds made using larger diameter wire than previously studied. The study of the in-process monitoring technique will continue with investigation of the characteristics of longer ultrasonic bonding tools.

Table 3 — Methods for Opening Packages

A. Flat Pack and Dual In-Line Package Types

1. Mainly Metal or with metal lid.[a]
   Mill,[b] cut with a knife,[c] or sand blast[d] a groove along periphery of lid (e.g., at weld bead) and pry off lid.[e]

2. Mainly Ceramic[f]

   a. Pry off lid after softening adhesive by soaking (5 to 10 min) in boiling acetic acid.[a]
   b. Cleave top ceramic lid by striking gently yet firmly a chisel which is positioned at interface between lid and adhesive on one end of the package.
   c. Sand blast adhesive around periphery of package. Then, while holding the package firmly at its ends in a knife-edged vise with knife edges positioned at interface between lid and adhesive layer, heat lid for a few seconds with a small hot flame (e.g., from a butane torch). The lid should pop off.[g]
   d. Thin top lid by sanding, for example, until a probe can puncture and pry off lid over cavity.
   e. Lap circular groove in ceramic lid with diamond impregnated abrasive and pry off circular section.[e,h]

B. Metallic-Cap Package Types

Mill, file, saw or otherwise make a groove along a circumference of the cap, near its base, and pry off top of cap.[e]

[a] Workman, W. L., Reliability Handbook for Silicon Monolithic Microcircuits, Vol. 3, Failure Analysis of Monolithic Microcircuits, NASA Report CR-1348 (April, 1969). Available from National Technical Information Service, Springfield, Virginia 22151, Accession Number N69-25328.

[b] Preferred method.

[c] Because of need to cut with considerable force there is some risk of damaging package.

[d] Involves most risk of introducing foreign particles into package cavity.

[e] Avoid breaking through lid in process of making groove to prevent introduction of extraneous particles into package cavity. But, make groove deep enough to allow puncture with a probe and to allow lid to be then pried off.

[f] When lead frame is embedded in an adhesive holding together ceramic parts of package, lead frame should be bonded to lower ceramic part (e.g., with epoxy) to provide support (after lid has been removed) for the leads. Adhesive may break loose in places, dislodging leads and wire bonds, in the process of delidding package. Furthermore, adhesive is not strong enough to hold leads in place during even careful handling.

[g] A. Tamburrino, Rome Air Development Center, Griffiss Air Force Base, New York 13441; private communication.

[h] Nicolas, D., and Yarbrough, C., New Techniques for Facilitating SEM Analysis of Microcircuits, *Scanning Electron Microscopy/1970,* Proc. Third Symposium on the Scanning Electron Microscope, pp. 57-61 (IIT Research Institute, Chicago, Illinois, 1970).

Table 4 — Methods for Removing Encapsulating Material

Basic Procedure[a]

1. Encase package base and leads[b] in a castable ceramic material to hold lead frame after removal of encapsulating material and lap material until one lead wire is visible. An alternative procedure is to mill a slot in the material above the region of the wire bonds and die. In this way the material around the wire bonds will be removed first with a sufficient amount of material remaining elsewhere to support the lead frame.[c]
2. Place package in drying oven (at 100°C) for 1 h. Alternatively, dry at a lower temperature under vacuum.[d]
3. Remove package from oven and immediately immerse in solvent.[e]

Material[f]	Solvent	Average Removal Time
epoxy	hot sulfuric acid[g]	25 s
phenolic resin	hot nitric acid[g]	30 min.
silicone	"Uresolve Plus" at 100°C[i,j]	2 h

4. Remove package, let drain for 5 s.
5. Immerse momentarily in boiling water with enough sodium hydroxide added to neutralize acid left on package.
6. Immediately rinse in hot tap water for 30 min.
7. Immerse in absolute alcohol[k] and make preliminary visual examination.

[a] McQuitty, D. W., Microelectronics Reliability as Related to Materials and Processing, *1972 IEEE Region Six Conference Record*, San Diego, California, April 1972, IEEE Publication 72CH0 593-4 REG6, pp. 134-137.

[b] Extensions to leads should be attached before encasing package if electrical measurements via these leads will be made later.

[c] F. Schroeder, Texas Instruments, Inc., Dallas, Texas 75222; private communication.

[d] D. W. McQuitty, Naval Electronics Laboratory Center, San Diego, California 92152; private communication.

[e] A cleaner removal of silicone materials is achieved by suspending the package just above the surface of the heated solvent.[d] The removal time is lengthened however.

[f] If unknown, determine which solvent will dissolve scrapings from the material.[d]

[g] Boil the concentrated acid for two hours to remove moisture which would attack aluminum metallization. An alternative procedure for sulfuric acid is to use fresh 97% sulfuric acid and heat to 220°C before placing device into acid. Using sulfuric acid at significantly lower temperatures (~160°C) may result in some attack of the aluminum metallization. After removal of device immerse in cold sulfuric acid for one to two minutes before rinsing well in deionized water and then in absolute alcohol.[h] An alternative procedure for nitric acid is to use 90% nitric acid to which for every 2 ml of acid one drop of ethyl silicate is slowly added while the acid is stirred. After removal of the device from the acid it should be rinsed in room-temperature 90% nitric acid to remove residues. After final removal from the solvent the device should additionally be washed for 5 min. in warm deionized water, methyl alcohol, and then air dried.[c]

[h] R. A. Kramer and J. Burns, National Semiconductor Corp., Santa Clara, California 95051; private communication.

[i] An alternative procedure for the removal of silicone is to concentrate the proprietary solvent by boiling it until the volume of solvent has decreased by one-half. After removal of the device from the solvent, rinse the device in room-temperature deionized water and examine. Repeat immersion if silicone has not been completely removed. After final removal from the solvent, rinse in room-temperature methyl alcohol and air dry.[c]

[j] Commercial materials are identified only to adequately specify the experimental procedure. In no case does such identification imply recommendation or endorsement by the National Bureau of Standards, nor does it imply that the material identified is necessarily the best available for the purpose.

[k] Store under alcohol to neutralize any acid residues and dissolve any moisture which would corrode the aluminum metallization.

4.3. SCANNING ELECTRON MICROSCOPY

Objective: To evaluate scanning electron microscopy as an inspection, process control, or device characterization tool for use in the electron device industry with initial emphasis on evaluation of inspection procedures and development of methods suitable for industrial use.

Background: Several types of significant potential failure points on integrated circuit chips can be detected by visual (microscopic) investigation. The inherent limitations on magnification and depth of field however severely restrict the usefulness of optical examination on chip patterns with steps. This becomes a particularly important consideration in examining both interconnection bonds and multilevel metallization patterns, which are major sources of failure in semiconductor devices. As a result there has been a considerable increase in use of scanning electron microscopy, which has very much greater depth of field at higher magnification, as an in-process inspection technique and as an element in acceptance specifications for semiconductor devices [1, 2].

With the advent of large scale integration, the availability of circuit test points has become greatly limited while at the same time the number of tests required to exercise the circuit is rising rapidly. The scanning electron microscope (SEM) provides a possible means of examining complex circuits in operation and detecting faulty regions without the need for probe or other direct contact [3].

The results of an extensive literature survey and of discussions with many SEM users have revealed that the SEM is being used by the semiconductor industry in a variety of ways:

1. As an inspection instrument. With its great depth of focus, the SEM is superior to other inspection instrumentation. It provides an excellent image at high magnification and resolution with a final-lens-to-specimen working distance that easily accomodates the inspection of semiconductor components without altering the package.
2. As an analytical tool to study surface potentials in the voltage contrast mode. In this mode, the electron beam is used as a floating probe to measure properties such as threshold voltage, transfer characteristics of inverters, and internally generated clock voltages at any point within complex device circuits. Stroboscopic techniques together with TV scan and video-tape recordings are used to study the dynamic properties of integrated circuits at their maximum operating frequencies.
3. To delineate junctions within semiconductor devices and to measure junction width, carrier lifetime, and doping concentrations in the electron beam induced current mode. The beam induced current comes from hole-electron pairs produced by the primary electron beam. Defects, such as ragged junctions,

discontinuous junctions, shorted junctions, and diffusion spikes, can be observed.

4. As an electron probe micro-analyzer to identify elements. In this mode the SEM is a valuable tool in studies of failed devices and circuits.

The last three modes of SEM operation discussed above are used by the semiconductor manufacturer primarily as an off-line tool. The device designer can verify the operational integrity of his device as well as readily detect design errors, masking faults, or potential reliability problems. The device-analysis engineer can quickly determine failure mechanisms in defective devices.

The instrument is being used in the first mode of operation discussed above, as a high resolution microscope, by all the major manufacturers as an on-line inspection tool to evaluate products and processes routinely. Most of the formal inspection procedures written to date cover the problem of metallization discontinuities over oxide steps and derive from the NASA SEM screening test for high reliability devices [1].

There are limitations to the use of SEM inspection procedures. Specimen preparation and examination usually require a greater amount of time than similar examination by light microscopy. The cost of the SEM is 10 to 100 times that of the light microscope, which reduces the availability of SEM instruments and results in increased costs for SEM inspections. The SEM is a complex instrument which requires trained personnel for operation, maintenance, and analysis of results. Effectiveness of the instrument may be reduced through misinterpretation of results due to inherent distortion effects, machine adjustment affecting resolution, angle of view, and other operational factors.

Whether or not SEM screening degrades semiconductor devices has not been resolved. Generally, specimens, particularly those which do not have conductive surfaces, must be coated with an evaporated metal film to improve surface emission and reduce electron beam instabilities. Further surface contamination can arise through the deposit of a carbon film on the specimen surface during the examination. In addition, the specimen is exposed to low levels of irradiation from the electron beam itself which may induce trapped charges in dielectric layers or cause other radiation damage.

Because of the importance of the problems at the wafer level which can be disclosed by SEM examination and because of the increasing attention to the use of the SEM in government procurement of high reliability components, the initial effort is concerned with evaluation of SEM inspection procedures and development of methods suitable for industrial use. In particular, work will be done to investigate the extent of radiation damage, the effect of trapped charges, and the effect of polymerized carbon in hydrocarbon films on the surfaces of semiconductor devices.

Progress: A scanning electron microscope (SEM) was procured and installed in a laboratory module selected for low residual magnetic field and low vibration level. Familiarization of operators with the basic instrument was essentially completed. Review of the current status of the use of the SEM for inspection of integrated circuits and other semiconductor devices began with search of the technical and report literature and discussions with SEM users in the industry, universities, and government laboratories. (W. K. Croll and W. J. Keery)

A panel discussion on the use of the SEM for device examination was organized and conducted in connection with the January meeting of ASTM Committee F-1 on Electronics in Atlanta. The panel members, all SEM users, included two representatives of major semiconductor manufacturers and three representative users of high-reliability devices. Objections to the use of SEM inspection procedures were raised by the representative of one of the manufacturers who strongly recommended that indiscriminate use of the SEM be avoided. Other users, however, have found that the use of SEM screening has resulted in process improvements which can be used on commercial as well as high reliability device lines. (K. O. Leedy)

Plans: Accessories to complement the basic SEM functions will be incorporated. These will include a eucentric stage for sample manipulation, a stage with vacuum electrical feedthroughs for transistor biasing, and an electron beam-blanking module. Observations of biased transistors and integrated circuits in the voltage contrast and electron beam induced current modes will begin. A literature survey of the permanent changes of device characteristics caused by SEM scanning will be made.

4.4. REFERENCES

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5. SEMICONDUCTOR DEVICES

5.1. THERMAL PROPERTIES OF DEVICES

Objective: To evaluate and improve electrical measurement techniques for determining the thermal characteristics of semiconductor devices.

Progress: Thermal resistance measurements were made by the emitter-only switching technique and with an infrared microradiometer on 12 transistors under conditions such that hot spots would occur in devices susceptible to hot spot formation. The results were compared with measurements made previously under conditions such that there were no severe current constrictions or hot spots. The data confirmed the expectation that, when operating at or near the second breakdown or voltage limited (low-current, high-voltage) region of the device safe operating area curve, the electrically measured thermal resistance cannot be relied upon to give the same value of thermal resistance as that calculated from measurements of peak junction temperature made with the infrared microradiometer.

Further investigations were made into the characteristics of the emitter-base voltage and current transients which occur when switching the emitter with a series transistor during measurement of thermal resistance by the emitter-only switching technique in order to elucidate certain aspects of the model proposed to account for them. The results of this work are reported in Appendix F together with a description of the proposed model.

Standardization Activities — A proposed revision of Method 1012, Thermal Characteristics, of MIL-STD-883, Test Methods for Microcircuits, undertaken at the request of the cognizant agency, was completed and forwarded to the agency for review.

(F. F. Oettinger)

Thermal Resistance Methods — Evaluation of the emitter-only switching technique for measuring thermal resistance continued. Tests on 16 transistors reported previously (NBS Tech. Note 773, pp. 28-30) indicated that, for operating conditions where there were no severe current constrictions or hot spots, the junction-to-case thermal resistance calculated from electrical measurements by the emitter-only switching technique extrapolated to 1 μs after the termination of the heating power pulse was generally within 10 percent of that determined from the infrared measurement. Infrared and electrical, measurements of thermal resistance were made on 12 of these transistors under high-voltage, low-current operating conditions at or near the second breakdown or voltage limited region of the device safe operating area curve. The test conditions were such that current constrictions or hot spots would occur if the devices were susceptible to them. The heating power, voltage, and current ranged from 14 to 22 W, 35 to 175 V, and 0.1 to 0.4 A, respectively. For any given device,

the actual voltage and current combination used depended on the safe operating area constraints. All devices were measured with a case temperature of 25°C. For the electrical measurements, which were made by the emitter-only switching method, the emitter-base voltage was measured 5, 10, 20, 50, and 100 μs after the termination of power with a test current of 6.5 mA.

The differences between the measurements of thermal resistance made under high-voltage, low-current conditions and the previously reported measurements (NBS Tech. Note 773, table 3) made under high-current, low-voltage conditions, expressed as a percentage of the latter, are given in table 5. The data in columns 2, 3, and 4 of the table represent the percent difference for the 50-μs electrical readings, the 10-μs electrical readings, and the infrared measurements, respectively.

The differences between the high-voltage, low-current thermal resistance calculated from the junction temperature determined electrically 50 and 10 μs after the termination of power and that determined from the infrared measurements, expressed as a percentage of the latter, are listed in columns 3, and 4, labeled A and B, respectively, of table 6. For reference, the infrared measurements of thermal resistance made under high-voltage, low-current conditions are listed in column 2 and the device collector voltage, V_{CE}, and collector current, I_C, during the power portion of the measurement cycle are listed in the last columns of the table. It was generally observed, that as the uniformity of the current distribution is decreased and hot spots become more prominent, the difference between the electrically determined thermal resistance and that calculated from the infrared measurement increases. This difference increases further as the delay between cessation of the power pulse and the time of measurement is increased.

The data reported in tables 5 and 6 suggest that severe current crowding has occured in devices 1, 4, and 10. (S. Rubin, D. L. Blackburn, and F. F. Oettinger)

Plans: On completion of the interlaboratory testing, the results of the round-robin experiment on thermal resistance measurements being conducted in cooperation with JEDEC Committee JC-25 on Power Transistors will be summarized. Long-term, single-operator measurements, to check the repeatability of the equipment for measuring thermal resistance of transistors by the emitter-only switching technique, will be carried out. The measurements will be made using both series- and parallel-emitter switching under a variety of device operating conditions. Further studies will be performed to determine whether the measurement of d-c current gain as a function of collector voltage for constant collector current and case temperature can be used to accurately predict when the electrical measurement of thermal resistance deviates significantly from the thermal resistance as derived from the measurement of peak junction

Table 5 — Percent Difference Between Electrical and Infrared Thermal Resistance Measurements Made Under High-Current, Low-Voltage Operating Conditions and Those Made Under Low-Current, High-Voltage Operating Conditions

Device	$\Delta R_{\theta JC}$ (50-μs), %	$\Delta R_{\theta JC}$ (10-μs), %	$\Delta R_{\theta JC}$ (IR), %
1	70.2	80.4	135.3
3	-4.9	-6.7	-6.7
4	165.5	185.3	315.8
5	7.8	-----[a]	8.8
6	0.0	-1.0	0.0
8	0.2	0.0	1.1
9	10.8	-----[a]	21.6
10	55.4	76.4	150.7
13	4.2	-0.3	0.0
14	4.6	2.0	11.5
15	49.0	52.3	68.0
16	56.6	59.0	73.4

[a]Measurement not made because of interference of long electrical transients.

Table 6 — Comparison of Infrared and Electrical Thermal Resistance Measurements Under High-Voltage, Low-Current Operating Conditions

Device	$R_{\theta JC}$ (IR), °C/W	A, %	B, %	V_{CE}, V	I_C, A
1	14.45	-39.6	-32.3	55	0.4
3	2.66	-19.5	-16.5	40	0.4
4	13.97	-55.9	-48.7	140	0.1
5	3.69	-14.1	-----[a]	55	0.4
6	5.21	-11.9	-8.4	35	0.4
8	7.57	-16.5	-12.9	35	0.4
9	4.23	-25.1	-----[a]	55	0.4
10	9.15	-58.9	-47.0	50	0.4
13	3.32	-10.8	-10.2	55	0.4
14	3.50	-16.0	-14.6	55	0.4
15	12.43	-16.3	-10.7	70	0.2
16	12.36	-11.8	-5.3	70	0.2

[a]Measurement not made because of interference of long electrical transients.

temperature made with the infrared microradiometer. The twelve transistors measured this quarter will be used in this study.

5.2. MICROWAVE DEVICE MEASUREMENTS

Objective: To study the problems and uncertainties associated with the measurement of electrical properties of microwave diodes, and to improve the techniques of these measurements.

Progress: Measurements to ascertain the random uncertainty of the X-band mixer measurement system were resumed. Repeated measurements of the conversion loss of a Schottky-barrier diode designed as a replacement for the 1N23 point-contact type were made by means of the incremental modulation method. The Schottky-barrier type was selected for this study because it is believed to be more stable than the point-contact type, whose characteristics are dependent upon whisker position and pressure, which are easily disturbed.

In measuring conversion loss, the local oscillator power was set using the calorimeter power monitor, with the modulation attenuator at the intermediate loss position (about $\frac{1}{2}$ dB) and an output null obtained; the attenuator was then cycled between the 1 dB and 0 dB positions, and the mixer output voltage recorded for each position. In order to reduce the influence of sporadic large deviations in the measured conversion loss caused by meter fluctuations of unknown origin, the attenuator was cycled several times, and the median and mean values of the increments for these several cycles were calculated. In the run yielding the results shown in table 7, five modulation cycles were made at each adjustment of the power and null. Statistical calculations were made using all the data, the medians of all five cycles, the means of all five cycles, the medians of the first three cycles, the means of the first three cycles, and the data from each individual cycle. Of the last, only the first cycle results, which are representative of the others, are shown. In all cases, the individual voltage increments were first converted to conversion (insertion) loss in decibels prior to the statistical analysis.

It can be seen that both the sample standard deviation and the range appear to be reduced by using the group median or mean for three or five modulation cycles as opposed to a single cycle. There also appears to be little difference between the use of three or five cycles, and only a small possible improvement in using the group mean rather than the median. The median would seem the preferable choice since it is easier to obtain and is more nearly free from influence by isolated extreme outliers although it is more susceptible to frequent fluctuations. It is, of course, assumed that future measurements would use the same procedure; i.e., that the group median or

Table 7 — Conversion Loss Measurements; Typical Repeatibility Measurement Run

	Median, dB	Mean, dB	Std. Dev., dB	Range (Max-Min), dB
From mixer measurements				
All data (35 entries)	4.531	4.529	0.027	0.115
Group medians (7 entries)				
All five cycles	4.531	4.528	0.023	0.054
First three cycles	4.547	4.541	0.020	0.061
Group means (7 entries)				
All five cycles	4.531	4.529	0.018	0.058
First three cycles	4.533	4.535	0.020	0.060
First cycle (7 entries)	4.544	4.548	0.028	0.084
Estimates from power measurements (47 entries)			0.015	0.084

mean for a given number of modulation cycles constitutes the single measurement for which the system uncertainty is defined.

To study the performance of the system independently of diode instability, the variability of the conversion loss measurement was also estimated from the variability of the power increment as measured by noting the changes in output voltage of the monitor calorimeter, assumed linear with power, as the modulation attenuator was repeatedly cycled. By calculating the variability of the power increment expressed in decibels, the previously developed expression (NBS Tech. Note 754, pp. 30-31) relating conversion loss variability to attenuator incremental loss variability may be used. As expected, the sample standard deviation of conversion loss predicted from these calorimeter voltage measurements is similar to, but somewhat less than, the directly measured sample standard deviation, as shown in table 7 for a typical run. The ranges are not directly comparable since the numbers of measurements were different.

Prior to making these measurements, part of the waveguide circuit was rearranged to allow simultaneous use of the moving short for reflection measurements and the calorimeter for power monitoring, both at the output side of the harmonic pad. As previously reported (NBS Tech. Note 743, p. 37) this pad is known to be temperature sensitive so that the original position of the calorimeter, at the input side of the pad, was not suitable for power monitoring. (J. M. Kenney)

To add greater rigidity and thermal mass to the harmonic pad, it was remounted (in the course of the waveguide rearrangement) on a ten-inch long aluminum block which supports the pad for its full length. A top plate of the same size is used for clamping. (L. M. Smith)

Responding to proposed changes in JEDEC Publication No. 77, a letter was sent to the Electronic Industries Association urging that a distinction be made between (spot) noise figure and average noise figure, as is done in IEEE standards.

The feasibility of using "noise measure" as a mixer parameter was briefly explored. Because of the behavior of this parameter for values of output noise ratio close to unity, no noise measure limits could be found that even roughly corresponded to typical limits on overall average noise figure. (J. M. Kenney)

Plans: Work will continue on the random uncertainty determination and on the summary of progress to date. If its stability appears satisfactory, the modulation attenuator will be sent to the NBS Electromagnetics Division for calibration. A limited revision of IEC document 47(Central Office)376, an international standard for microwave mixer measurements, will be prepared at the request of the U.S. National Committee.

5.3. CARRIER TRANSPORT IN JUNCTION DEVICES

Objective: To improve methods of measurement for charge carrier transport and related properties of junction semiconductor devices.

Progress: The delay-time correction technique was successfully applied to measurements on the Sandia bridge of transistors subjected to gain degradation.

The data on the passive devices obtained by the five round-robin participants who used automatic network analyzers for measurement have been examined for both within- and between-laboratory variability.

Sandia Bridge Delay-Time Instrumentation — Previous work (NBS Tech. Note 743, pp. 39-40) has shown that for the transistor represented by the small-signal model in figure 21 the term to be added to the measured delay time to correct for the effects of extraneous signal pickup is predicted to be

$$\tau_c = \left\{ \frac{1}{h_{fe}} \frac{(R_z + r_b + r_e)}{R_s} + \frac{r_e}{R_s} \right\} (\tau_s - \tau_{rs}) \qquad (5)$$

where h_{fe} is the small signal, common-emitter current gain, R_z is the characteristic impedance of the bridge (100 Ω), r_b is the transistor base resistance, r_e is the transistor dynamic emitter resistance, and $(\tau_s - \tau_{rs})$ is the delay time zero shift measured

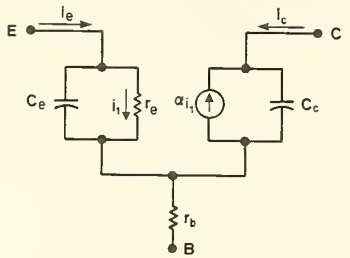

Figure 21. Small-signal modal for transistor.

by the bridge when an emitter-collector short-circuit is replaced by a resistor of value R_s. The quantity τ_c is the negative of the delay time error which arises because of extraneous pickup.

To check this prediction, measurements of delay time of a 2N2219 transistor were made as a function of emitter current and frequency before and after degradation of the h_{fe} by neutron irradiation.* Signal frequencies used were 3 to 15 MHz; collector-base voltage was 5 V. This frequency range was chosen for the measurements since it is in this range that the delay-time measurements previously made on R-C networks showed the greatest frequency dependence (NBS Tech. Note 733, pp. 41-43). Results for an emitter current of 20 mA, typical of results in the 5 to 35 mA range explored, are listed in table 8. The pre-irradiation delay time, τ_{m1}, is relatively independent of frequency. After irradiation, a significant frequency dependence of delay time, τ_{m2}, is observed. The quantity $(\tau_s - \tau_{rs})$ was measured for a through resistor, $R_s = 20\ \Omega$. For the case under discussion $r_e \approx 1.3\ \Omega$ and is negligible compared with both R_s and R_z. For a high-frequency transistor, such as the 2N2219, the base resistance is much less than 100 Ω. Therefore eq (5) can be quite well approximated as

$$\tau_c \approx \frac{1}{h_{fe}} \frac{R_z}{R_s} (\tau_s - \tau_{rs}) = \frac{5}{h_{fe}} (\tau_s - \tau_{rs}). \qquad (6)$$

Even for the largest value of $(\tau_s - \tau_{rs})$, 255 ps at 3 MHz, τ_c is only about 6 ps and the correction to τ_{m1} is not significant before irradiation when $h_{fe} \approx 200$. However, after irradiation, when $h_{fe} \approx 10$, the correction shown as τ_{c2} in the table significantly affects the result as can be seen by comparing the columns headed τ_{m2} and $(\tau_{m2} + \tau_{c2})$ in the table or the curves in figure 22. Note that the frequency variation shown by τ_{m2} alone is almost completely eliminated when τ_c is added. It should also be noted that there are no adjustable constants in the expression for τ_c.

(D. E. Sawyer)

*We are indebted to Capt. P. J. Vail of the Air Force Weapons Laboratory, Albuquerque, New Mexico, for performing the irradiation.

Table 8 — Delay Time of a 2N2219 Transistor Before and After h_{fe} Degradation

f, MHz	τ_{m1}, ps	τ_{m2}, ps	$(\tau_s - \tau_{rs})$, ps	τ_{c2}, ps	$(\tau_{m2} + \tau_{c2})$, ps
3	635	520	255	128	648
5	650	685	-55	-27	658
7	630	590	85	43	633
10	610	585	75	38	623
15	590	590	10	5	595

S-Parameter Round-Robin Measurements — Six laboratories completed their measurements of the S parameters of the transistors and passive devices circulated for the round robin. Five laboratories used automatic network analyzers for the measurements; one used a manual system. While analysis of the data is not complete, some trends can be noted from data obtained on the passive devices by the five laboratories which used automatic network analyzers.

An analysis of variance of the data was made to determine the variability to be expected from repeated measurements within the same laboratory as well as the differences to be expected when the same devices are measured in different laboratories. The variances from all laboratories were averaged to obtain the within-laboratory variance, which procedure is valid if all laboratories are equally capable of reproducing their results in repeated measurements [1]. The between-laboratory variance is a measure of the dispersion of the mean of each laboratory's measurements from the grand mean determined from the measurements of all the laboratories. From these two variances, the within- and between-laboratory sample standard deviations were calculated. Since the magnitudes of the S parameters vary with frequency, the coefficient of variation, which is the sample standard deviation expressed as a percentage of the mean, is used to indicate the variability of the magnitude of the S parameters.

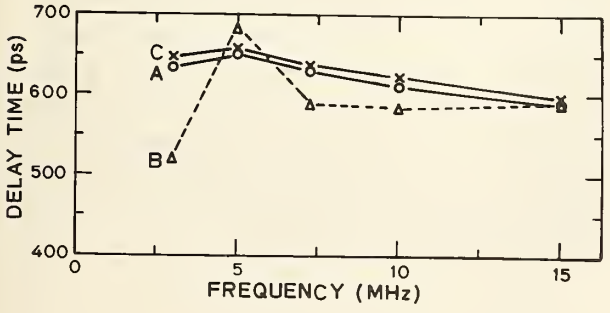

Figure 22. Delay time of a 2N2219 transistor before and after h_{fe} degradation. (A, before degradation; B, after degradation (measured); C, after degradation (corrected).)

Table 9 — Magnitude of S-Parameters, R-C Network 2

Parameter	Frequency, MHz	Mean	Coefficient of Variation, %			
			Within-Laboratory		Between-Laboratory	
			A	B	A	B
S_{11}	300	0.471	0.44	2.36	3.04	2.89
	1000	0.598	0.69	3.47	3.43	2.90
	1700	0.634	1.39	5.66	5.20	8.71
S_{21}	300	0.539	0.34	0.35	0.95	0.68
	1000	0.154	0.95	1.04	1.88	3.22
	1700	0.057	2.07	2.07	1.83	9.62

Table 10 — Phase of S-Parameters, R-C Network 2

Parameter	Frequency, MHz	Mean, deg	Sample Standard Deviation, deg			
			Within-Laboratory		Between-Laboratory	
			A	B	A	B
S_{11}	300	222.8	0.33	0.86	1.42	1.06
	1000	152.0	0.51	2.52	1.41	3.41
	1700	112.0	0.99	3.25	3.22	5.70
S_{21}	300	301.0	0.27	0.43	0.92	1.17
	1000	246.8	0.39	1.28	0.93	3.20
	1700	209.1	0.56	1.78	1.92	4.57

The results of the analysis of the measurements of R-C Network 2 are summarized in tables 9 and 10. The within- and between-laboratory variability is given at three frequencies representative of the range of frequencies covered in the measurements. In table 9 the coefficient of variation is used to describe the variability of the magnitude of S_{11} and S_{21}; in table 10 the sample standard deviation is used to describe the variability of phase measurements. The columns labeled A show the results obtained when all participants used the same transistor fixture to adapt the transistor socket to the coaxial output of the network analyzer, and the columns labeled B show the results when each participant used his own transistor fixture of the same construction. Values for S_{22} and S_{12} are not shown; they are almost the same as those for S_{11} and S_{21}, respectively, since the networks are symmetrical.

In almost every case, the variability is greater when each laboratory used its own transistor fixture than when all used the same transistor fixture. This would be expected unless the calibration procedures completely compensated for the characteristics of the transistor fixtures. In most cases there is less difference in measurements of S_{21} than in measurements of S_{11}, which indicates that the calibration procedures (NBS Tech. Note 773, p. 35) are more effective in compensating for the transmission characteristics of the transistor fixture than in precisely locating the reference planes.

The use of a percentage to express the variability of the magnitude of the S-parameter measurements, table 9, helps to emphasize that the variability does increase with frequency independently of any changes in the magnitude of the S parameter itself. This change is also evident in table 10 where it is seen that the variability of the phase measurements increases with frequency even though the phase angles of both S_{11} and S_{21} decrease with frequency. Variability increases with frequency because errors in locating the reference planes represent a larger fraction of the signal wavelength and hence a larger phase error as the frequency increases. The between-laboratory variation in the phase of the S parameters tends to be larger than the within-laboratory variation because additional errors are introduced by the differences in the transistor fixtures and calibration procedures. (G. J. Rogers)

Plans: Additional measurements of delay time of transistors before and after gain degradation by radiation will be made. The analysis of the S-parameter round robin data will be completed. The within- and between-laboratory variability determined from measurements on the passive devices will be used to assess the extent to which variability in the transistor measurements can be attributed to variability in the measuring systems.

5.4. REFERENCE

5.3. Carrier Transport in Junction Devices

1. Dixon, W. J., and Massey, F. J., *Introduction to Statistical Analysis*, pp. 119-127 (McGraw-Hill Book Co., New York, 1951).

APPENDIX A

JOINT PROGRAM STAFF

Coordinator: J. C. French*
Secretary: Miss B. S. Hope*
Consultant: C. P. Marsden¶†

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APPENDIX B

COMMITTEE ACTIVITIES

ASTM Committee F-1 on Electronics

W. M. Bullis, Editor, Subcommittee 4, Semiconductor Crystals; Secretary, Subcommittee 91, Editorial; Leaks, Resistivity, Mobility, Dielectrics, and Compound Semiconductors Sections; Subcommittee 11, Quality and Hardness Assurance; Advisory Committee

J. R. Ehrstein, Chairman, Resistivity Section; Epitaxial Resistivity, and Epitaxial Thickness Sections

J. C. French, Chairman, Subcommittee 91, Editorial; Subcommittee 11, Quality and Hardness Assurance; Secretary, Advisory Committee

G. G. Harman, Secretary, Interconnection Bonding Section

B. S. Hope, Committee Assistant Secretary

K. O. Leedy, Chairman, Interconnection Bonding Section

T. F. Leedy, Photoresist and Dielectrics Sections

D. C. Lewis, Subcommittee 11, Quality and Hardness Assurance

C. P. Marsden, Committee Secretary; Advisory Committee

R. L. Mattis, Lifetime Section, Editorial Subcommittee

W. E. Phillips, Chairman, Lifetime Section; Secretary, Subcommittee 4, Semiconductor Crystals, Crystal Perfection, Mechanical Properties of Semiconductor Surfaces, Compound Semiconductors; Impurities in Semiconductors, and Germanium Sections

A. H. Sher, Germanium Section

W. R. Thurber, Mobility, Germanium, Compound Semiconductors, and Impurities in Semiconductors Sections

ASTM Committee E-10 on Radioisotopes and Radiation Effects

W. M. Bullis, Subcommittee 7, Radiation Effects on Electronic Materials

J. C. French, Subcommittee 7, Radiation Effects on Electronic Materials

Electronic Industries Association: Solid State Products Division, Joint Electron Device Engineering Council (JEDEC)

J. M. Kenney, Microwave Diode Measurements, Committee JC-21 on UHF and Microwave Diodes

F. F. Oettinger, Chairman, Task Group JC-11.3-1 on Thermal Considerations for Microelectronic Devices, Committee JC-11 on Mechanical Standardization; Technical Advisor, Thermal Resistance Measurements, Committees JC-22 on Rectifier Diodes and Thyristors, JC-20 on Signal and Regulator Diodes, JC-25 on Power Transistors, and JC-30 on Hybrid Integrated Circuits

S. Rubin, Chairman, Council Task Group on Galvanomagnetic Devices

D. E. Sawyer, Task Group JC-24-5 on Transistor Scattering Parameter Measurement Standard, Committee JC-24 on Low Power Transistors

H. A. Schafft, Technical Advisor, Second Breakdown and Related Specifications, Committee JC-25 on Power Transistors

IEEE Electron Devices Group:

J. C. French, Standards Committee

J. M. Kenney, Chairman, Standards Committee Task Force on Microwave Solid-State Devices II (Mixer and Video Detector Diodes)

H. A. Schafft, Chairman, Standards Committee Task Force on Second Breakdown Measurement Standards

IEEE Magnetics Group

S. Rubin, Chairman, Galvanomagnetic Standards Subcommittee

IEEE Parts, Hybrids, and Packaging Group

W. M. Bullis, New Technology Subcommittee, Technical Committee on Hybrid Microelectronics

Society of Automotive Engineers

J. C. French, Subcommittee A-2N on Radiation Hardness and Nuclear Survivability

W. M. Bullis, Planning Subcommittee of Committee H on Electronic Materials and Processes

IEC TC47, Semiconductor Devices and Integrated Circuits:

S. Rubin, Technical Expert, Galvanomagnetic Devices; U.S. Specialist for Working Group 5 on Hall Devices and Magnetoresistive Devices

APPENDIX C

SOLID-STATE TECHNOLOGY & FABRICATION SERVICES

Technical services in areas of competence are provided to other NBS activities and other government agencies as they are requested. Usually these are short-term, specialized services that cannot be obtained through normal commercial channels. Such services provided during the last quarter are listed below and indicate the kinds of technology available to the program.

1. Thin Metal Films (J. Krawczyk)

Thin gold films were evaporated onto quartz plates to be subsequently etched for use as instrument scales by the NBS Microwave and Mechanical Instrumentation Section.

2. Ultrasonic Machining (J. Krawczyk)

Tapered holes were ultrasonically machined through thermocouple heads for the NBS Instrumentation Application Section.

3. Channel Electron Multipliers and Silicon Nuclear Radiation Detectors (Y. M. Liu)*

Evaluation of channel electron multipliers for the NASA Goddard Space Flight Center continued. Acceptance testing of five units was completed, and one flight detector was calibrated in terms of counting response as a function of plate voltage using a ^{63}Ni source.

The cause of failure of a channel electron multiplier was determined. The unit had an open circuit between the high voltage terminals after various phases of testing. It was suspected that a high voltage arc over the collector cap might have burned off the conducting contact. This was confirmed by inducing such arcing in another unit.

4. Ribbon Wire Technology (H. K. Kessler)†

Assistance to the Naval Electronics Laboratory Center, San Diego, in the implementation of NBS-developed ribbon wire technology on their pilot production facility continued. A series of survey measurements was completed to check the characteristics of ultrasonically bonding 1.5 mil by 0.5 mil (38 μm by 13 μm) gold and aluminum ribbon wire and 1-mil (25-μm) diameter aluminum wire to various gold thin and thick films on ceramic substrates. Large variations in pull strength were observed for bonds made with both gold and aluminum ribbon wire for coated substrates obtained from various manufacturers. Bonding was found to be especially difficult on gold thick-film paste containing glass filler.

*NBS Cost Center 4254425

†NBS Cost Center 4254448

APPENDIX D

JOINT PROGRAM PUBLICATIONS

Prior Reports

A review of the early work leading to this Program is given in Bullis, W. M., Measurement Methods for the Semiconductor Device Industry — A Review of NBS Activity, NBS Tech. Note 511, December, 1969.

Quarterly reports covering the period since July 1, 1968, have been issued under the title Methods of Measurement for Semiconductor Materials, Process Control, and Devices. These reports may be obtained from the Superintendent of Documents (Catalog Number C.13.46:XXX) where XXX is the appropriate technical note number. Microfiche copies are available from the National Technical Information Service (NTIS), Springfield, Virginia 22151.

Quarter Ending	NBS Tech. Note	Date Issued	NTIS Accession No.
September 30, 1968	472	December, 1968	AD 681330
December 31, 1968	475	February, 1969	AD 683808
March 31, 1969	488	July, 1969	AD 692232
June 30, 1969	495	September, 1969	AD 695820
September 30, 1969	520	March, 1970	AD 702833
December 31, 1969	527	May, 1970	AD 710906
March 31, 1970	555	September, 1970	AD 718534
June 30, 1970	560	November, 1970	AD 719976
September 30, 1970	571	April, 1971	AD 723671
December 31, 1970	592	August, 1971	AD 728611
March 31, 1971	598	October, 1971	AD 732553
June 30, 1971	702	November, 1971	AD 734427
September 30, 1971	717	April, 1972	AD 740674
December 31, 1971	727	June, 1972	AD 744946
March 31, 1972	733	September, 1972	AD 748640
June 30, 1972	745	December, 1972	AD 753642
September 30, 1972	754	March, 1973	AD 757244
December 31, 1972	773	May, 1973	

Current Publications

As various phases of the work are completed, publications are prepared to summarize the results or to describe the work in greater detail. Copies of most of such publications are available and can be obtained on request to the editor or the author.

Thurber, W. R., Lewis, D. C., and Bullis, W. M., Resistivity and Carrier Lifetime in Gold-Doped Silicon, AFCRL Report AFCRL-TR-73-0107, January 31, 1973.

Kessler, H. K., and Sher, A. H., Microelectronics Interconnection Bonding with Ribbon Wire, NBS Tech. Note 767, April, 1973.

Sawyer, D. E., Rogers, G. J., and Huntley, L. E., Measurement of Transit Time and Related Transistor Characteristics, AFWL Report TR-73-54 (9 March 1973).

Schafft, H. A., Failure Analysis of Wire Bonds, presented as part of a Workshop on Failure Analysis of Semiconductor Devices and Packages, 1973 Reliability Physics Symposium, Las Vegas, Nevada, April 4, 1973.

Sher, A. H., and Kessler, H. K., Microelectronic Interconnection Bonding with Ribbon Wire, presented at Third Annual Symposium on Hybrid Microelectronics, Baltimore, May 3, 1973.

Buehler, M. G., Thermally Stimulated Measurements: The Characterization of Defects in Silicon *p-n* Junctions, *Semiconductor Silicon/1973*, H. R. Huff and R. R. Burgess, eds., pp. 549-560 (Electrochemical Society, Princeton, New Jersey, 1973).

Leedy, K. O., Scanning Electron Microscope Examination of Wire Bonds from High-Reliability Devices, NBS Tech. Note 785, (July, 1973).

Schafft, H. A., Methods for Testing Wire-Bond Electrical Connections, to be presented at the Third Symposium on Reliability in Electronics, Budapest, November 13-16, 1973.

Use of Capacitor Microphones to Study Vibrations in Microelectronics Ultrasonic Bonding Equipment, *Ultrasonics* 11, No. 1, 5-6 (January, 1973). (Based on NBS Technical Note 573).

APPENDIX E

CALL FOR PAPERS

SYMPOSIUM ON

SPREADING RESISTANCE

GAITHERSBURG, MARYLAND

JUNE 13 - 14, 1974

In the past several years electrical measurements by spreading resistance probes have been increasingly used to characterize semiconductor materials, devices, and processing. The purpose of this symposium is to provide an exchange of information and to review the state of the art of measurement by spreading resistance probes.

Papers are solicited on the following subjects:

1. Theory
   - 1.1 Models of contacts and current flow
   - 1.2 Correction factors and their computation for thin and multilayer structures
2. Equipment and Calibration
   - 2.1 Mechanical assembly and probes
   - 2.2 Sample preparation
   - 2.3 Data acquisition and electronics
   - 2.4 Standards
3. Applications
   - 3.1 Characterization of semiconductor starting materials
   - 3.2 Process control
   - 3.3 Device evaluation

Persons intending to contribute papers should submit a descriptive title by September 1, 1973, followed by a 500 to 1000 word summary before December 15, 1973 to enable the reviewers to determine the suitability of the paper for the symposium.

Send to: Dr. James Ehrstein
National Bureau of Standards
Bldg. 225, Room B-346
Washington, D. C. 20234
Phone: 301-921-3625

Camera ready copies of the paper must be submitted to Dr. Ehrstein prior to oral delivery of the paper.

The proceedings of the symposium will be published shortly after the meeting. Only those papers presented at the symposium will be published.

Jointly sponsored by ASTM Committee F-1 on Electronics and the National Bureau of Standards.

APPENDIX F

SWITCHING TRANSIENTS IN TRANSISTORS

The turn-off transient which occurs when the emitter of a transistor is opened rapidly while the base and collector remain connected can result in emitter-base junction breakdown (NBS Tech. Note 773, pp. 30-31). This breakdown may cause deterioration [1] or catastrophic failure of the transistors. The breakdown occurs even though the emitter current is in the direction appropriate to a forward biased emitter-base junction. It arises because of a potential drop along the emitter-base junction induced by the flow of majority carriers out of the base as required to bring the base region back to equilibrium following reduction of electron injection from the emitter. Breakdown can be avoided if the emitter is opened slowly enough that the base can remain in a near neutral condition without rapid flow of charge and the resulting potential build up. Alternatively, the emitter-base voltage can be limited to a value below the breakdown voltage with a protective circuit based on the use of a zener diode. The charge flow in the base during the turn-on and turn-off transients and of the operation of the protective circuit are described in detail below.

To elucidate the details of the charge flow during switching an extensive series of experiments was conducted. In these experiments, the current in various branches of the circuit was measured with a current probe and the voltage across the appropriate transistor terminals was measured with an oscilloscope. The circuit used for these measurements is shown in figure 23. This circuit also contains a protective zener diode circuit (NBS Tech. Note 754, p. 27) which can be incorporated by the switch S_1.

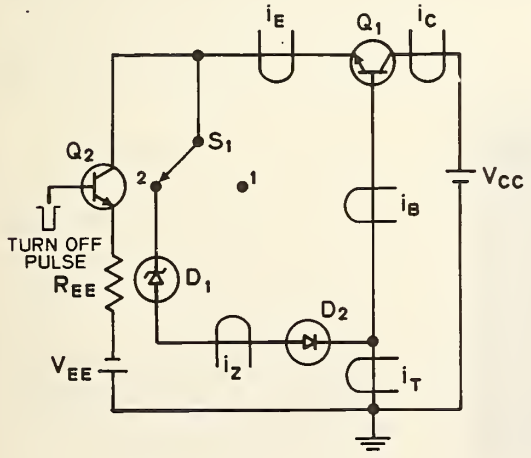

Figure 23. Test circuit. (Current is measured by means of a probe at the loops marked i_X.

The low-level emitter current supply, usually included when measuring thermal resistance, was omitted during this series of experiments; no significant differences, except one which will be noted subsequently, were observed when the low-level emitter current was included.

Turn-on Transient — Consider first the conditions in the on state which are set up during turn on. For explicitness the argument is developed for an *n-p-n* transistor, but it can easily be extended to a *p-n-p* transistor. In the quiescent state the base is grounded and the collector-base junction is reverse biased (collector positive). At a time t = 0, the emitter supply is connected to the emitter contact to foward bias the emitter-base junction (emitter negative) which results in electrons being injected into the base. The injected electrons are minority carriers in the base. They diffuse toward the collector-base junction with a time constant that can be the order of microseconds, but as soon as they enter the base they upset the charge neutrality in the base. To maintain charge neutrality, majority holes flow rapidly into the base from the base contact. The return to neutrality in the base occurs with a time constant determined by the dielectric relaxation time in the base. This time constant is the order of 10^{-12} to 10^{-13} s. Thus, as soon as an electron is injected into the base a hole is created to neutralize it. This process results in a build up of the electron-hole pair density in the base and continues until equilibrium is reached. The turn-on current transients for a 35-W, single diffused transistor with a 1.5 mil (60 μm) wide base are shown in figure 24. During the period of charge build up, the electron current into the base from the emitter is much larger than the electron current leaving the base for the collector, and holes flow into the active region of the base, under the emitter-base junction. Outside the active region the base is thin and long relative to its width. The charge flow across the extrinsic base

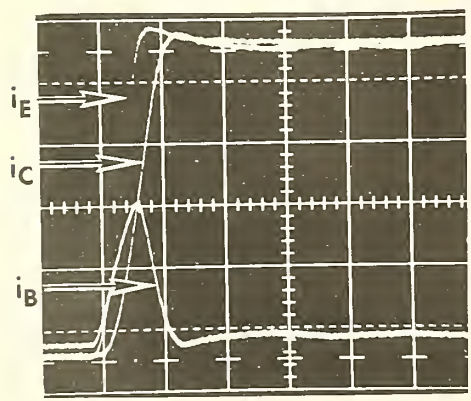

Figure 24. Turn-on base, emitter, and collector current transients. (Horizontal scale: 1 μs/div. Vertical scale: 200 mA/div.)

resistance associated with this region results in a potential drop such that the edge of the active region of the transistor is negative with respect to the base contact. Lateral hole flow across the intrinsic base resistance within the active region, causes an additional potential drop across the emitter-base junction; this potential drop is, of course, in the same direction. It acts to debias the center of the junction and causes the familiar current crowding phenomenon which forces the emitter current to the outer periphery of the junction.

Equilibrium is established when the excess hole-electron pair density in the base region reaches the value appropriate to the injected electron current from the emitter. In equilibrium, holes still flow from the base contact to the active region in order to supply holes for recombination with electrons in the base (base transport losses) and for injection into the emitter (injection efficiency losses). The current associated with these losses is much smaller than either the peak base current during turn-on or the steady-state emitter current. In the example shown in figure 24, the equilibrium base current is 15 mA while the peak base current is approximately 450 mA and the steady-state emitter and collector currents are about 1 A.

Turn-off Transient — When the transistor emitter circuit is opened, electron injection into the base from the emitter decreases. However, the excess carrier density which causes the concentration gradient associated with the diffusion of electrons toward the collector does not change instantaneously; hence, electrons continue diffusing toward the collector-base junction where they are swept out of the base region. This results in a reduction of the electron density in the base which must be accompanied by a reduction of the hole density in order to maintain charge neutrality. Consequently, holes must flow out from the active region of the transistor to the base contact. This flow is in the opposite direction to the flow during the turn-on transient and sets up a potential gradient across the extrinsic base resistance such that the active region of the transistor is positive with respect to the contact. The most positive portion of the base can approach the potential of the collector region.

The simplest turn-off transient occurs for collector-base voltage well below the breakdown voltage of the emitter base junction. To illustrate this case, the current and base emitter voltage turn-off transients are shown for a collector voltage of about 10 V in figure 25. The switch S_1 in the test circuit (figure 23) was set to position 1 so that the protective circuit is not connected. When turn-off begins, as evidenced by a decrease in i_E, v_{EB} begins to rise toward zero from a small negative potential. At the same time, i_B decreases from a small positive value to zero and then increases to a negative value of approximately 165 mA. During this same period i_E begins to decrease rather rapidly, but the collector current does not begin to decrease rapidly until about 0.2 μs after i_E starts to decrease. During this 0.2-μs period, i_B increases in the reverse direction in such a way as to be always equal to

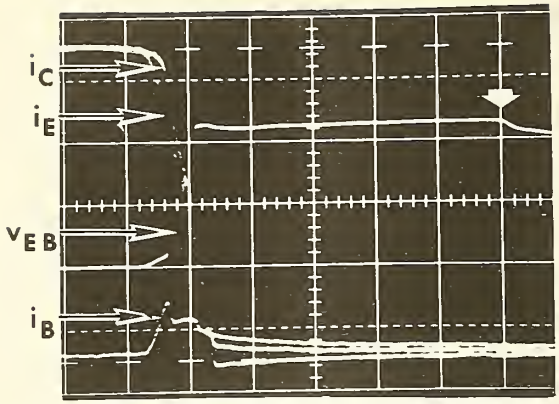

Figure 25. Turn-off emitter-base voltage and base, emitter, and collector current transients for collector-base voltage less than emitter-base junction breakdown voltage. ($V_{CC} \approx 10$ V. Horizontal scale: 1 μs/div. Vertical scales: 5 V/div (v_{EB}); 200 mA/div (i).)

the difference between the magnitudes of i_C and i_E. The action of the currents and the reverse-biased emitter-base voltage during this time period can be explained as follows. Since the injection rate of electrons from the emitter is being reduced while for a time the extraction rate of electrons at the collector remains unchanged, holes must flow out of the active region of the device toward the base contact through the extrinsic base resistance. Since both i_B and v_{EB} increase linearly during this period, it appears that the extrinsic base resistance is constant as one would expect.

About the time i_C begins to decrease significantly, i_B also begins to decrease. Since v_{EB} continues to increase even more rapidly, this suggests that the base resistance is increasing. This could occur if the active area of the emitter changed from the periphery to the central core. Such a change is in accord with the direction of hole flow; in contrast to the situation encountered during turn-on the outer regions of the emitter tend to be debiased. Next i_B stabilizes for a time while v_{EB} continues to increase; then when v_{EB} reaches its maximum value (limited by the collector voltage), i_B decreases toward its new steady-state value (in the present case, zero). At long times, after i_B, i_E, and i_C reach their new steady-state values, v_{EB} begins to decrease to zero or, if $i_E \neq 0$, a small value of forward bias. This is also illustrated in figure 25 (see arrow).

If a higher value of collector voltage is applied, again with the protective circuit not connected, the turn-off transients begin in the same fashion, but when v_{EB} reaches a value near the breakdown voltage of the emitter-base junction it ceases to rise significantly and i_B increases abruptly as illustrated in figure 26. This abrupt increase in i_B is due to the onset of breakdown at the periphery of the emitter-base junction. The active region of the transistor has been pinched in toward the center of the emitter area by virtue of the hole flow out to the base lead as discussed

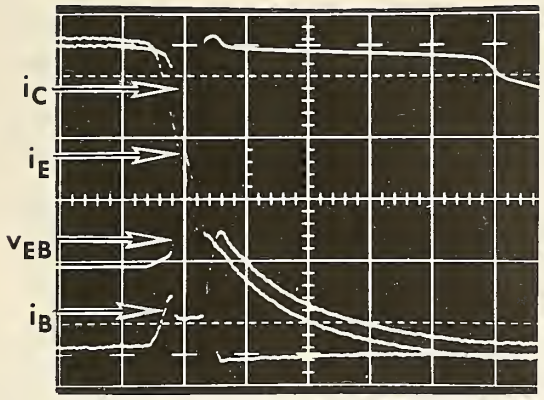

Figure 26. Turn-off emitter-base voltage and base, emitter, and collector current transients for collector-base voltage greater than emitter-base junction breakdown voltage, without protective circuit. ($V_{CC} \approx 20$ V. Horizontal scale: 1 μs/div. Vertical scales: 5 V/div (v_{EB}); 200 mA/div (i).)

above. In this central region the emitter-base junction is forward biased so the emitter potential is only a fraction of a volt more negative than the potential in the central base region. Since the emitter is a low-resistance element the entire emitter is at approximately the same potential. However, the base contact is much more negative than the central region of the base because of the resistive drop associated with the lateral hole flow through the base. As a result, except for the central active area, the emitter-bias junction is reverse biased; this bias can increase until its value at the periphery reaches the limit imposed by the collector voltage or the junction breakdown voltage, whichever is lower. In the latter case, there is a substantial flow of electrons from the base contact, laterally across the extrinsic base resistance, into the emitter across the reverse-biased junction at the periphery, through the emitter layer, to the central region of the emitter where they join the injected electrons from the emitter circuit in crossing the forward-biased portion of the junction, through the base, and into the collector. These electrons serve to retard the rate of decrease of the collector current as can be seen in figure 26.

This model can be verified by considering the transients in the case where the zener diode protective circuit is included and the collector voltage is greater than the zener voltage. In this case as illustrated in figure 27 it is possible to separate the current through the base region and the current through the zener diode which breaks down in much the same way as the peripheral region of the emitter-base junction in the previous case. The i_B transient, which consists of holes leaving the active region of the base, is very similar to the i_B transient when breakdown of the emitter-base junction does not occur (figure 25), while the i_T transient, which is the sum of the base and zener currents, is very similar to the i_B transient when breakdown occurs (figure 26). Note that in this case, the zener current also influences i_E in

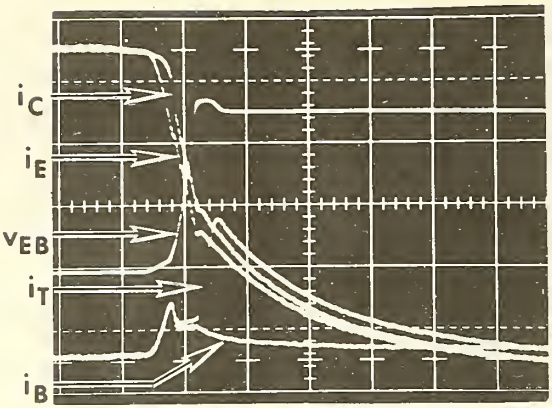

Figure 27. Turn-off emitter base voltage and base, emitter, and collector current transients for collector-base voltage greater than emitter-base junction breakdown voltage with a 12-V zener diode protective circuit. (V_{CC} ≈ 20 V. Horizontal scale: 1 µs/div. Vertical scales: 5 V/div (v_{EB}); 200 mA/div (i).)

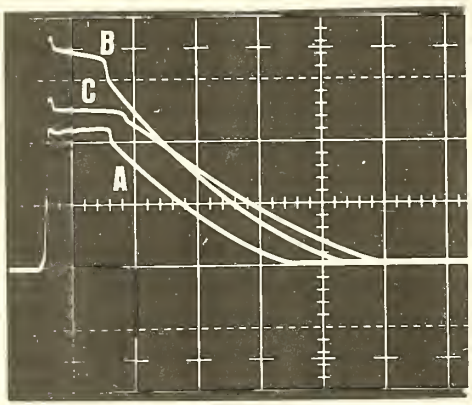

Figure 28. Turn-off emitter-base voltage transients. (A: V_{CC} ≈ 10 V, no protective circuit. B: V_{CC} ≈ 20 V, no protective circuit. C: V_{CC} ≈ 20 V, 12-V zener diode protective circuit. Horizontal scale: 5 µs/div. Vertical scale: 5 V/div.)

contrast to the previous case. With the protective circuit, the fall of v_{EB} is somewhat delayed. This can be seen more clearly in the traces presented in figure 28 which cover a longer time period.

As a final observation, it should be noted that the rate of decay of the v_{EB} transient depends primarily on the nature of the external circuit and not on the device properties. In particular, inclusion of the low-level emitter current supply used for thermal resistance measurements substantially increases the rate of decay.

(S. Rubin)

REFERENCE

1. Verway, J. F., On the Mechanism of h_{FE} Degradation by Emitter-Base Reverse Current Stress, *Microelectronics and Reliability* 9, 425-432 (1970).

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16. ABSTRACT (A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.)

This quarterly progress report, nineteenth of a series, describes NBS activities directed toward the development of methods of measurement for semiconductor materials, process control, and devices. Significant accomplishments during this reporting period include (1) development of a comprehensive, large-area test pattern for evaluating planar junction structures, (2) completion of experimental work on the evaluation of the destructive, double-bond pull test for wire bonds, (3) initiation of a scanning electron microscope facility, and (4) completion of the investigation of the mechanism of emitter-base junction reverse breakdown during rapid switching of transistors. Because of the general applicability of the last of these, details are presented in a separate appendix. Work is continuing on measurement of resistivity of semiconductor crystals; characterization of generation-recombination-trapping centers in silicon; study of gold-doped silicon; development of the infrared response technique; evaluation of wire bonds and die attachment; measurement of thermal properties of semiconductor devices; determination of S-parameters, delay time, and related carrier transport properties in junction devices; development of a-c probing techniques; and characterization of noise and conversion loss of microwave detector diodes. Supplementary data concerning staff, standards committee activities, technical services, and publications are included as appendices.

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