NBS TECHNICAL NOTE 743

Methods of Measurement for Semiconductor Materials, Process Control, and Devices

Quarterly Report

April 1 to June 30, 1972

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[1] Headquarters and Laboratories at Gaithersburg, Maryland, unless otherwise noted; mailing address Washington, D.C. 20234.
[2] Part of the Center for Radiation Research.
[3] Located at Boulder, Colorado 80302.
[4] Part of the Center for Building Technology.

Methods of Measurement for Semiconductor Materials, Process Control, and Devices

Quarterly Report, April 1 to June 30, 1972

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FOREWORD

The Joint Program on Methods of Measurement for Semiconductor Materials, Process Control, and Devices was undertaken in 1968 to focus NBS efforts to enhance the performance, interchangeability, and reliability of discrete semiconductor devices and integrated circuits through improvements in methods of measurement for use in specifying materials and devices and in control of device fabrication processes. These improvements are intended to lead to a set of measurement methods which have been carefully evaluated for technical adequacy, which are acceptable to both users and suppliers, which can provide a common basis for the purchase specifications of government agencies, and which will lead to greater economy in government procurement. In addition, such methods will provide a basis for controlled improvements in essential device characteristics, such as uniformity of response to radiation effects.

The Program is supported by the National Bureau of Standards,[*] the Defense Nuclear Agency,[†] the U.S. Navy Strategic Systems Project Office,[§] the U.S. Navy Electronic Systems Command,[+] the Air Force Weapons Laboratory,[¶] the Air Force Cambridge Research Laboratories,[#] the Advanced Research Projects Agency,[×] the Atomic Energy Commission,[**] and the National Aeronautics and Space Administration.[††] Although there is not a one-to-one correspondence between the tasks described in this report and the cost centers through which the Program is supported, the concern of certain sponsors with specific parts of the program is reflected in planning and conduct of the work.

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[*] Through Research and Technical Services Cost Centers 4251126, 4251127, 4252128, and 4254115.

[†] Through Order EA072-810. (NBS Cost Center 4259522).

[§] Administered by U.S. Naval Ammunition Depot, Crane, Indiana through Project Orders PO-2-0023 and PO-2-0054. (NBS Cost Center 4259533).

[+] Through Project Order PO-2-1034. (NBS Cost Center 4252534).

[¶] Through Delivery Order F29601-71-F-0002. (NBS Cost Center 4252535).

[#] Through Project Order Y72-873. (NBS Cost Center 4251536).

[×] ARPA Order 1889 Monitored by Space and Missile Systems Organization under MIPR FY76167100331. (NBS Cost Center 4254422).

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METHODS OF MEASUREMENT FOR SEMICONDUCTOR MATERIALS, PROCESS CONTROL, AND DEVICES

QUARTERLY REPORT
APRIL 1 TO JUNE 30, 1972

This quarterly progress report, sixteenth of a series, describes NBS activities directed toward the development of methods of measurement for semiconductor materials, process control, and devices. Significant accomplishments during this reporting period include verification of the applicability of resolution of forces in interpreting pull test measurements on unannealed wire bonds on single-level substrates, completion of the feasibility study of ribbon-wire bonding with the important finding that ribbon-wire bonds can be made with a wider range of bonding parameters than round-wire bonds of the same strength, and development of test procedures in preparation for studies of high-frequency measurements of transistors on the wafer by means of probes. Work is continuing on measurement of resistivity of semiconductor crystals; study of gold-doped silicon; development of the infrared response technique; evaluation of wire bonds and die attachment; and measurement of thermal properties of semiconductor devices, delay time and related carrier transport properties in junction devices, and noise properties of microwave diodes. New work has been started on development of procedures for analysis of the characteristics of generation-recombination-trapping centers in silicon. Supplementary data concerning staff, standards committee activities, technical services, and publications are included as appendixes.

Key Words: Aluminum wire; base transit time; carrier lifetime; die attachment; electrical properties; epitaxial silicon; gamma-ray detectors; generation centers; germanium; gold-doped silicon; infrared response; methods of measurement; microelectronics; microwave diodes; nuclear radiation detectors; probe techniques (a-c); recombination centers; resistivity; ribbon-wire bonding; semiconductor devices; semiconductor materials; semiconductor process control; silicon; thermal resistance; trapping centers; ultrasonic bonding; wire bonds.

1. INTRODUCTION

This is the sixteenth quarterly report to the sponsors of the Joint Program on Methods of Measurement for Semiconductor Materials, Process Control, and Devices. It summarizes work on a wide variety of measurement methods that are being studied at the National Bureau of Standards. Since the Program is a continuing one, the results and conclusions reported here are subject to modification and refinement.

INTRODUCTION

The work of the Program is divided into a number of tasks, each directed toward the study of a particular material or device property or measurement technique. This report is subdivided according to these tasks. Highlights of activity during the quarter are given in section 2. Section 3 deals with tasks on methods of measurement for materials; section 4, with those on methods of measurement for process control; and section 5, with those on methods of measurement for devices. References for each section are listed in a seperate subsection at the end of that section.

The report of each task includes the long-term objective, a narrative description of progress made during this reporting period, and a listing of plans for the immediate future. Additional information concerning the material reported may be obtained directly from individual staff members connected with the task as indicated throughout the report. The organization of the Joint Program staff and telephone numbers are listed in Appendix A.

An important part of the work that frequently goes beyond the task structure is participation in the activities of various technical standardizing committees. The list of personnel involved with this work given in Appendix B suggests the extent of this participation. Additional details of current standardization activities not associated with a particular task are given in section 2.

Background material on the Program and individual tasks may be found in earlier reports in this series as listed in Appendix D. From time to time, publications are prepared that describe some aspect of the program in greater detail. Current publications of this type are also listed in Appendix D. Reprints or copies of such publications are usually available on request to the author.

2. HIGHLIGHTS

Significant accomplishments during this reporting period include verification of the applicability of resolution of forces in interpreting pull test measurements on unannealed wire bonds on single-level substrates, completion of the feasibility study of ribbon-wire bonding with the important finding that ribbon-wire bonds can be made with a wider range of bonding parameters than round-wire bonds of the same strength, and development of test procedures in preparation for studies of high-frequency measurements of transistors on the wafer by means of probes.

During this quarter a new task area on generation-recombination-trapping centers was established. Investigations have disclosed that inadequate methods for measurement, and hence for control, of critical electrical properties of semiconductor-grade silicon are an important deterrent to the development of power semiconductor devices which are, in turn, fundamental to the fulfillment of recognized national needs such as reliable and economical power distribution systems meeting expected energy demands without serious environmental impact. This task area has been established to address the measurement problems associated with carrier lifetime control. Although initial efforts are being concentrated on further development of several traditional techniques for measuring minority carrier lifetime, plans have been made to utilize and develop new, more powerful methods for analysis of generation-recombination-trapping centers including thermally and optically stimulated current and capacitance measurements.

Because it has been found that quantitative temperature measurements can be made with commercially available infrared microscopes with less effort, with greater spatial resolution, and with greater precision than with thermographic phosphors, it has been decided that further investigation of these phosphors as a quantitative tool for thermographic measurements is unwarranted at this time. The thermographic phosphors are a valuable qualitative measurement tool, particularly for a quick view of temperature patterns and hot spot positions, and for observing changes under different operating conditions. Consequently, these materials will continue to be used in the laboratory as a qualitative measurement tool.

Highlights of the on-going technical activities are presented in this section; details are given in subsequent sections of the report. This section concludes with a summary of standardization activities carried out by program staff members but not otherwise described in the report.

Resistivity — Further consideration by ASTM Committee F-1 on Electronics at its June meeting of the problem of standard silicon wafers for four-probe resistivity measurements led to the decision to implement a program which includes provision of a limited range of standard reference wafers as soon as the details of certification and validation procedures can be worked out. Tests run on the newly constructed instrument for measuring probe loading of the pins of a four-probe array showed that probe loading can be determined well within the tolerance required for four-probe resistivity measurements made according to ASTM Method F-84. Experimental investigation of the capacitance-voltage (C-V) method continued on diodes with metallized contacts over the diffused areas. No improvement was obtained in either C-V profile flatness or in agreement between doping density as determined by the C-V and four-probe methods over earlier measurements made with unmetallized wafers. A series of experiments was begun to study the effect of the heat treatment cycle during diffusion on the resistivity of the wafer in a further attempt to identify the source of the discrepancy between resistivity determined from capacitance-voltage measurements and that determined by the four-probe method.

Generation-Recombination-Trapping Centers — Study of diode recovery methods continued with emphasis on the dependence of the measurement of storage time in the reverse recovery method on forward and reverse current levels. It was found that the dependence, characteristic of the lumped-constant model, observed in some diodes may be explained on the basis of short base width. A series of measurements of carrier lifetime by the surface photovoltage method was initiated on p-type, gold-doped silicon as part of the study to establish capture cross section values for the gold centers. Investigations of the applicability of various absorption coefficient data to the interpretation of surface photovoltage measurements continued.

Gold-Doped Silicon — The model which includes a gold-related shallow acceptor state was used to calculate new curves of the dependence of resistivity on gold concentration in both n- and p-type silicon at room temperature. Although these curves give the relationships at high gold concentrations more correctly, the position of the sharp increase in n-type silicon is still not correctly accounted for by the model. Preliminary experiments suggest that the high temperature heat treatments associated with gold diffusion introduce compensating donors at concentration up to 10^{13} cm^{-3}.

Infrared Methods — The lithium-drifted germanium gamma-ray detectors studied to date have been grouped according to their infrared response (IRR) spectra into one of the five representative types described last quarter; nearly four-fifths of the poor quality detectors fall into two of the four spectrum types thought to indicate poor crystal quality. The IRR of lithium-drifted silicon detectors was measured for the first time at room temperature as well as near 100 K. Four silicon surface-barrier detectors and two silicon diffused-junction detectors were the first silicon devices that were not lithium-compensated to be studied successfully using the IRR technique.

Die Attachment Evaluation — The analysis of heat flow using the TRUMP computer thermal analysis program to determine the limitations of thermal response techniques for detecting poor die adhesion in semiconductor devices was delayed by program difficulties. The design and fabrication of a revised test circuit to measure transient thermal response of both diodes and power transistors in both the diode and transistor operating modes were undertaken.

Wire Bond Evaluation — The study of the feasibility of using ribbon wire for ultrasonic bonding was completed. The results showed that bonds with high pull strengths and good cosmetic appearance can be made using existing bonding machines with slight modifications. It was shown that ribbon-wire bonds of a given quality can be made over a much greater range of ultrasonic power and time than can round-wire bonds of similar quality. Experimental study of factors that significantly affect the wire bond pull test on single-level substrates continued. It was found that pulling the bond out of the plane of the bond results in a slight decrease in measured pull strength with increasing angle. Further measurements on unannealed round-wire bonds indicated that the measured pull strength could be predicted by the resolution-of-forces calculation for the range of bond parameters normally encountered, but there remains some uncertainty that the same holds for annealed bonds.

Thermal Properties of Devices — Investigations were continued of the measurement of thermal resistance to compare the use of the common-base, emitter-and-collector switching technique with the common-base, emitter-only switching technique. In both cases the emitter-base junction voltage is used as the temperature sensitive parameter. The investigation of the current and temperature dependence of common-emitter current gain continued.

Microwave Device Measurements — Experiments are underway to evaluate the reproducibility of the system for measuring mixer conversion loss by the incremental modulation method and to determine the sensitivity of the measurement to system characteristics such as local oscillator power variations and accuracy of the output circuit null setting. Because a stable and reproducible local oscillator power level is essential to the conduct of reproducibility studies over a long period, the investigation of the stability of the local oscillator power was continued. The initial experiments were conducted to identify the most stable diodes for use in subsequent tests of system stability as well as to obtain sensitivity data.

Carrier Transport in Junction Devices — Analytical work was continued to predict the effects of extraneous signals in delay-time apparatus on the measurement of delay in transistors as represented by an equivalent circuit which realistically incorporates the device passive elements. A large portion of project activity was devoted to assembling equipment and establishing techniques for measurement of transistor high-frequency S-parameters while the devices are at the wafer stage of preparation. The format for specifying the laboratory procedure for intercomparison of S-parameter measurements was completed, and the procedure was tested on discrete devices using an automatic network analyzer.

Standardization Activities — Many of the standardization activities undertaken by program staff are broader than the technical tasks described in the following sections. These activities, which are reported here, involve general staff support in committees, liaison between committees, coordination of efforts which may encompass a variety of tasks, and participation in areas where no direct in-house technical effort is underway.

Twelve program staff members attended the regular summer meeting at Gaithersburg of ASTM Committee F-1 on Electronics. Three staff members chaired section meetings; the Interconnection Bonding Section conducted its fourth successful meeting. Six documents were revised or edited by program staff members.

Most activity in connection with EIA-JEDEC Committees was in the thermal measurements area (see sec. 5.1.). In addition, work on a chapter on maximum operating conditions was completed for the Suggested Standard for Power Transistors being developed by Committee JC-25 on Power Transistors, and extensive assistance was given Task Group 5 of Committee JC-24 on Low Power Transistors in the modification of a report on the accuracies obtainable at the present time in the measurement of transistor scattering parameters (NBS Tech. Note 571, p. 45) for inclusion as an appendix to its Proposed Standard for the Measurement of Small-Signal Transistor Scattering Parameters.

Other standardization activities, directly related to particular task areas, are reported with the appropriate tasks. A summary of the standardization and dissemination activities conducted during FY 1972 is included as Appendix E.

3. SEMICONDUCTOR MATERIALS

3.1. RESISTIVITY

Objective: To develop methods suitable for use throughout the electronics industry for measuring resistivity of bulk, epitaxial, and diffused silicon wafers.

Progress: Further consideration by ASTM Committee F-1 on Electronics at its June meeting of the problem of standard wafers for four-probe resistivity measurements led to the decision to implement a program which includes provision of a limited range of standard reference wafers as soon as the details of certification and validation procedures can be worked out. Tests run on the newly constructed instrument for measuring probe loading of the pins of a four-probe array showed that probe loading can be determined well within the tolerance required for four-probe resistivity measurements made according to ASTM Method F-84. Experimental investigation of the capacitance-voltage (C-V) method continued on diodes with metallized contacts over the diffused areas. No improvement was obtained in either C-V profile flatness or in agreement between doping density as determined by the C-V and four-probe methods over earlier measurements made with unmetallized wafers. A series of experiments was begun to study the effect of the heat treatment cycle during diffusion on the resistivity of the wafer in a further attempt to identify the source of the discrepancy between resistivity determined from capacitance-voltage measurements and that determined by the four-probe method.

Silicon Resistivity Standards — At its June meeting, ASTM Committee F-1 on Electronics further considered the problem of resistivity standards and the ways in which NBS can assist the industry in this regard. It was concluded that the modified collaborative reference program (NBS Tech. Note 727, p. 8) would acceptably serve the needs of the industry. Investigation of the detailed procedures associated with conducting such a program led to the decision to further modify the program to include a standard reference material service covering a limited range of resistivity with provisional certification of the standards. Details of the certification aspects and procedures for validating the quoted values are now being developed. (J. R. Ehrstein)

Other Standards Activities — The round-robin experiment being conducted in conjunction with ASTM Committee F-1 to determine interlaboratory precision of four-probe resistivity measurements on silicon epitaxial layers has now been completed by six of nine participating laboratories. Data are being reduced and tabulated as received; a revised summary of the data is not planned until the experiment is completed. The document detailing the procedure for this method has been revised to incorporate comments made in a subcommittee ballot and submitted for editorial review at the committee level. (J. R. Ehrstein and F. H. Brewer)

Probe Loading — Characterization of the instrument for measuring the loading applied to the points of a four-probe array (NBS Tech. Note 733, pp. 9-10) was completed. To avoid problems, such as punch through of thin layers, which may arise when one probe has a much greater loading than the remaining three, the force applied to each probe point is determined individually. To insure that the loading is measured with the probe at its working extension a reference position is established at the back of the probe needle. With this reference position, rather than with a reference position established at the force gauge, the technique is suitable for measuring the loading as well as for setting the loading to a predetermined value. The force gauge is removable so that one with a suitable range can be used; choice of a gauge which operates on the upper end of its useable range for the probe force being measured insures large movement of gauge linkage parts to minimize the effects of static friction.

During the evaluation of the instrument it became clear that the probe array must be carefully positioned and clamped so that the line joining the probe tips at their working extension must be perpendicular to and that the axes of motion of the probes must be parallel with the motion of the primary gauge linkage; these two requirements arise because positioning or displacement at an angle as small as 5 deg from the normal causes the outermost pins of an array with a probe spacing of 1.59 mm (0.0625 in.) to be measured at effective lengths 0.18 mm (0.007 in.) longer or shorter than the lengths at which they would be used in the resistivity measurement. The resultant error in force depends on the tensioning springs in the probe but is typically 30 percent at the outer pins. To test for misalignment when initially aligning the instrument, it is advisable to run measurements with the probe oriented in two positions 180 deg apart in its support clamp. If alignment is correct, each probe in the array should experience no shift in indicated reference position or applied force as a result of the rotation.

Tests with the instrument were run on three four-probe arrays with nominal loading of 25, 40, and 150 gf (0.245, 0.392, and 1.47 N) per pin. The arrays were not adjusted for uniformity of probe force prior to the tests. The alignment of each array was adjusted for parallelism. Two experiments were made. In the first experiment, designed to determine the scatter which arises from friction and other individual characteristics of the probe pins and gauge linkage, an array was mounted, the reference position was established once for each pin, and the probe loading was measured ten times. The average loading measured and sample standard deviation in each case are given in table 1.

The second test was designed to determine the overall reproducibility of the measurement. In this test each probe array was mounted, the reference position was

Table 1 — Probe Loading Determination, Single Mounting[a]

Array	Pin			
	1	2	3	4
A	19±0.5 gf	18±0.7 gf	18±0.4 gf	16±0.4 gf
B	45±1.0	37±0.5	28±0.5	25±0.5
C	177±2.5	148±0.8	129±2.0	134±1.9

[a] Note 1 gf = 9.8 mN; gages calibrated in newtons are not yet readily available commercially.

Table 2 — Probe Loading Determination, Multiple Mounting[a]

Array	Run No.	Pin			
		1	2	3	4
A	1	18.4 gf	16.4 gf	17.0 gf	14.2 gf
	2	21.2	18.0	19.0	15.2
	3	19.2	17.6	17.6	13.8
B	1	43.0	38.4	27.6	28.2
	2	43.2	41.0	28.6	28.0
	3	46.0	38.3	27.3	27.4
C	1	173.4	155.4	145.2	148.2
	2	172.4	155.2	146.0	151.0
	3	175.7	151.8	138.6	142.7

[a] Note 1 gf = 9.8 mN; gages calibrated in newtons are not yet readily available commercially.

established for each pin, five readings of probe loading were taken on each pin, and the probe array was demounted. This sequence, including determination of the reference position, was repeated three times for each probe array. The average of the five readings for each determination is listed in table 2. It is evident that measurements of probe force can be made well within the ±25.5-gf (±0.25-N), tolerance required for resistivity measurements made according to ASTM Method F-84 [1].

(F. H. Brewer and J. R. Ehrstein)

Capacitance-Voltage Methods — Preliminary experiments were made on diodes from several wafers with both sintered and unsintered evaporated aluminum contacts over the diffused areas. Doping density calculated from the capacitance measurements increased with depth, as also observed in unmetallized diodes, rather than remaining constant. In addition it was observed that the doping density was greater than that calculated from resistivity measured by the four-probe method in contrast to previous observations on unmetallized wafers. Nevertheless, it does not appear that the metallized contacts alter the conditions of the C-V measurement so that the anticipated result can be obtained.

Experiments were begun to investigate the change in resistivity specimens may undergo as a result of the heat cycle during diffusion and to determine if such changes are contributing to the discrepancy between doping density as determined by C-V and four-probe measurements.

Study of procedures for analyzing C-V data was continued with the incorporation into the computer program for analyzing C-V data of a modified edge correction scheme reported by Wilson [2]. The revised edge correction and the one previously used [3] were compared on a sample of data previously taken and were found to yield doping density values with maximum disagreement less than 1.5 percent.

A sample of data was also analyzed using a correction for back depletion into the more heavily doped side of the junction that is based on an analysis performed by Niehaus *et al.* [4]. It was found that flatter profiles and better agreement with four-probe measurements on substrates with doping density greater than 10^{16} cm^{-3} were obtained when the back depletion correction was included. (R. L. Mattis)

Plans: A program to provide silicon resistivity standards for the semiconductor device industry in a form consistent with the consensus of need thus far expressed will be given primary consideration. Further analysis of current and probe-force effects on the measurement of resistivity by the four-probe method will be delayed until plans for this program are completed. Work will continue on coordinating and analyzing the data from the four-probe epitaxial resistivity round robin. Emphasis in C-V measurement will be on studying ways to reduce the observed discrepancy between doping density determined as by C-V and four-probe measurements.

3.2. GENERATION-RECOMBINATION-TRAPPING CENTERS

Objective: To develop electrical measurement methods including mathematical models and test structures for characterizing the electronic properties and density of generation-recombination-trapping (GRT) centers in silicon with emphasis on methods applicable to control of parameters such as lifetime and leakage current.

Background: Investigations have disclosed that inadequate methods for measurement, and hence for control, of critical electrical properties of semiconductor grade silicon are an important deterrent to the development of power semiconductor devices. These devices are fundamental to the fulfillment of recognized national needs such as reliable and economical power distribution systems that can meet expected energy demands without serious environmental impact.

Satisfactory solutions to the pressing problems of long-distance power transmission required by remote sources, of entrance of transmission lines into crowded urban areas, and of electrical system stability have not proved exploitable because of the high cost of available a-c to d-c conversion equipment. Use of semiconductor converter devices may reduce cost of equipment for this purpose by over one-third if suitable devices are made available [1]. Similarly, predicted requirements for power conversion in Navy applications cannot now be met because of material and processing limitations which prevent development of the necessary semiconductor devices [2].

A crucial factor in meeting these needs is spatial control of charge carrier lifetime in silicon, both in the starting material and throughout fabrication processes. This calls for development of reliable lifetime measurement techniques with strong emphasis on adequate spatial resolution, studies of various methods for lifetime control including radiation damage, and characterization of generation-recombination-trapping (GRT) centers in silicon such as those introduced by gold, silver, and copper.

This task area has been established to address the measurement problems associated with carrier lifetime control. Although initial efforts are being concentrated on further development of several traditional techniques for measuring minority carrier lifetime, plans have been made to utilize and develop new, more powerful methods for analysis of GRT centers including thermally and optically stimulated current and capacitance measurements.

<u>Progress</u>: Study of methods for measuring diode recovery continued with emphasis on the dependence of the measurement of storage time in the reverse recovery method on forward and reverse current levels. It was found that the dependence, characteristic of the lumped-constant model, observed in some diodes may be explained on the basis of short base width. A series of measurements of carrier lifetime by the surface photovoltage method was initiated on *p*-type, gold-doped silicon as part of the study to establish capture cross section values for the gold centers. Investigations of the applicability of various absorption coefficient data in the interpretation of surface photovoltage measurements continued.

Diode Recovery Methods — Emphasis was placed on further study of the reverse recovery method. Differences have been reported in the functional relationship between the ratio of storage time, t_s, to lifetime, τ, and the ratio of forward current, I_f, to reverse current, I_r (NBS Tech. Note 733, p. 15). Three diode types tested could be characterised by the logarithmic form appropriate to the lumped-constant model:

$$t_s/\tau \propto \ell n \{A\ [1 + (I_f/I_r)]\}, \tag{1}$$

where A is a constant, while others followed the expected form [3]:

$$\mathrm{erf}\sqrt{t_s/\tau} = [1 + (I_r/I_f)]^{-1}. \tag{2}$$

Four additional diode types were tested this quarter; all followed the relationship of eq (2). In seeking a basis for the behavior of the three previously measured diodes that followed eq (1), attention was directed to the diode geometry since the logarithmic form has also been reported for short-base diodes [4]. In these, a proportionality factor which depends on the ratio of the width of the diode, w, between the junction and the contact on the more lightly doped side and the diffusion length, L, must be included in eq (1).

Examination and measurement of these diodes showed that the base width was less than twice the diffusion length in all cases, confirming that narrow base width may be responsible for the observed behavior which was characteristic of the lumped-constant model. In this case, the base width must be determined and the proportionality factor computed from theory [4, 5] if lifetime is to be deduced from measurements of storage time. In general, lifetime can be computed from a single measurement of storage time only if the correct relationship is used; if the wrong relationship is assumed, the computed lifetime may differ by more than a factor of two from the real value.

It was also observed that at very low forward currents the measured storage times of the diodes fit the relationship of eq (1) even though they fit eq (2) at larger currents. Although the explanation for this observation is not yet understood, it points up another hazard in interpreting single-point reverse-recovery measurements. These are very often made for the condition $I_f = I_r$, which frequently lies in the transition between the regions of applicability of the two functional models so neither can be used to compute the lifetime from the storage time.

A high-speed reverse-recovery apparatus was assembled which utilized a high-speed pulse generator to switch the diode under test, a d-c power supply to forward bias the diode, and a sampling oscilloscope to observe the switching transient. Tests showed that the transients associated with the circuitry were all shorter than 4 ns. (D. C. Lewis)

Surface Photovoltage Method — A series of measurements of minority carrier lifetime made by the surface photovoltage (SPV) method was begun on Hall bars cut from 0.08-, 0.5-, and 1-Ω·cm, *p*-type, gold-diffused silicon wafers in which the shallow acceptor concentration is much greater than the gold concentration. In these wafers, the density of positively charged gold donor recombination centers is essentially equal to the gold density and the lifetime, τ, in seconds is

$$\tau = (\sigma_{e02}\, v_e\, N_{Au})^{-1},$$

where σ_{e02} is the capture cross section for electrons at the positively charged gold donor in square metres, v_e is the thermal velocity of electrons in metres per second, and N_{Au} is the gold density in atoms per cubic metre. Preliminary results are in general agreement with values of σ_{e02} determined from low-level photoconductivity decay measurements [6].

Determination of lifetime from an SPV measurement assumes knowledge of two quantities: the minority carrier diffusion coefficient, which is a function of the impurity concentration in the specimen, and the photon absorption coefficient as a function of wavelength in the region used. Diffusion coefficients have been determined from published data on conductivity and drift mobility. A problem which may be encountered in connection with the choice of the correct absorption coefficient has been discussed previously (NBS Tech. Note 733, p. 15). This quarter, two additional experiments were carried out.

To determine whether a layer of damaged material might be present in undiffused specimens for which Dash and Newman [7] absorption coefficient data were needed to fit the SPV measurements, a specimen was etched a second time to remove a total of 75 μm of material and the SPV results were compared with those obtained after removal of only 25 μm. No significant differences in fit or diffusion length were seen.

Other absorption coefficient data were tried for a specimen which had been diffused only for a short time and for which neither Runyan [8] nor Dash and Newman absorption coefficient data gave a good fit to the SPV results. The data of Braunstein *et al.* [9] gave a slightly better fit than did any other data for this specimen. Only by transmission measurements can it be determined with certainty which absorption coefficient data are most appropriate for the specimen. There was more than a factor of two variation in the diffusion length obtained from the linear region of SPV plots made with the various data. To be certain that the SPV measurements were characteristic of the bulk of the specimen, a second etching was done to remove a 100 μm layer and SPV measurements were repeated. The results were similar to those obtained after the first etching which removed only 25 μm.

These results suggest that the property of the crystal which affects the absorption coefficient is indeed characteristic of the bulk material rather than of a thin surface layer. (W. R. Thurber, A. W. Stallings, and W. M. Bullis)

<u>Plans</u>: Investigation of the current-level dependence of the ratio of reverse-recovery storage time to carrier lifetime will continue. Study of the open-circuit-voltage decay (OCVD) method will resume; the effect of a short base on the decay

transient will be determined. A high-speed OCVD apparatus will be constructed to facilitate investigation of the problems which may be encountered when measuring sub-microsecond lifetimes by this method.

SPV measurements on *p*-type, gold-doped specimens will continue. Low resistivity *n*-type silicon wafers will be diffused with gold to concentrations less than the shallow donor concentration in preparation for study of recombination at the negatively charged gold acceptor. Polished silicon specimens covering a range of thicknesses will be prepared for transmission measurements to obtain the absorption coefficient as a function of wavelength for comparison with published results now used to analyze the SPV lifetime data.

3.3. GOLD-DOPED SILICON

Objective: To characterize *n*- and *p*-type silicon doped with gold and to develop a model for the energy-level structure of gold-doped silicon which is suitable for use in predicting its characteristics.

Progress: To study the influence of the degeneracy factor of the gold acceptor level on the resistivity of initially *n*-type gold-doped silicon, calculations of resistivity as a function of gold density were made for a range of values of the degeneracy factor for an initial donor density of 8.6×10^{14} cm^{-3}. It was found that the degeneracy factor of the gold acceptor at 0.58 eV does not affect the position of the sharp rise in resistivity at the point where the gold density equals the initial donor density, but it does influence the resistivity at larger gold density where the Fermi level is between the gold donor and the gold acceptor. A comparison with calculations of experimental data obtained previously on gold-diffused wafers from an initially *n*-type, 5.3-Ω·cm crystal suggests that the degeneracy factor of the gold acceptor lies in the range 0.0625 to 0.25.

New calculations of resistivity as a function of gold density were made for gold-doped silicon at room temperature. In these calculations the energies of the gold donor and the gold acceptor were taken as 0.35 eV and 0.58 eV, respectively, above the valence band; the energy gap at 300 K, as 1.114 eV; and the intrinsic carrier density, as 1.4×10^{10} cm^{-3}. The electron and hole effective masses were taken as 1.18 and 0.81 times the free electron mass, respectively [1]. The degeneracy factor was assumed to be 0.125 for both the gold donor and the gold acceptor. The lattice mobility [2] and impurity mobility [3] were combined reciprocally to obtain the carrier mobility used in the calculation of the resistivity. Also included was the gold-coupled acceptor located at 0.033 eV above the valence band [4]. Its dependence on gold density is not well established, but experimental data reported previously (NBS Tech. Notes 727, pp. 12-13, and 733, pp. 13-14) suggest that the acceptor density increases approximately as the third power of the gold density with a value of 4.5×10^{15} cm^{-3} at a gold density of 1×10^{17} cm^{-3}.

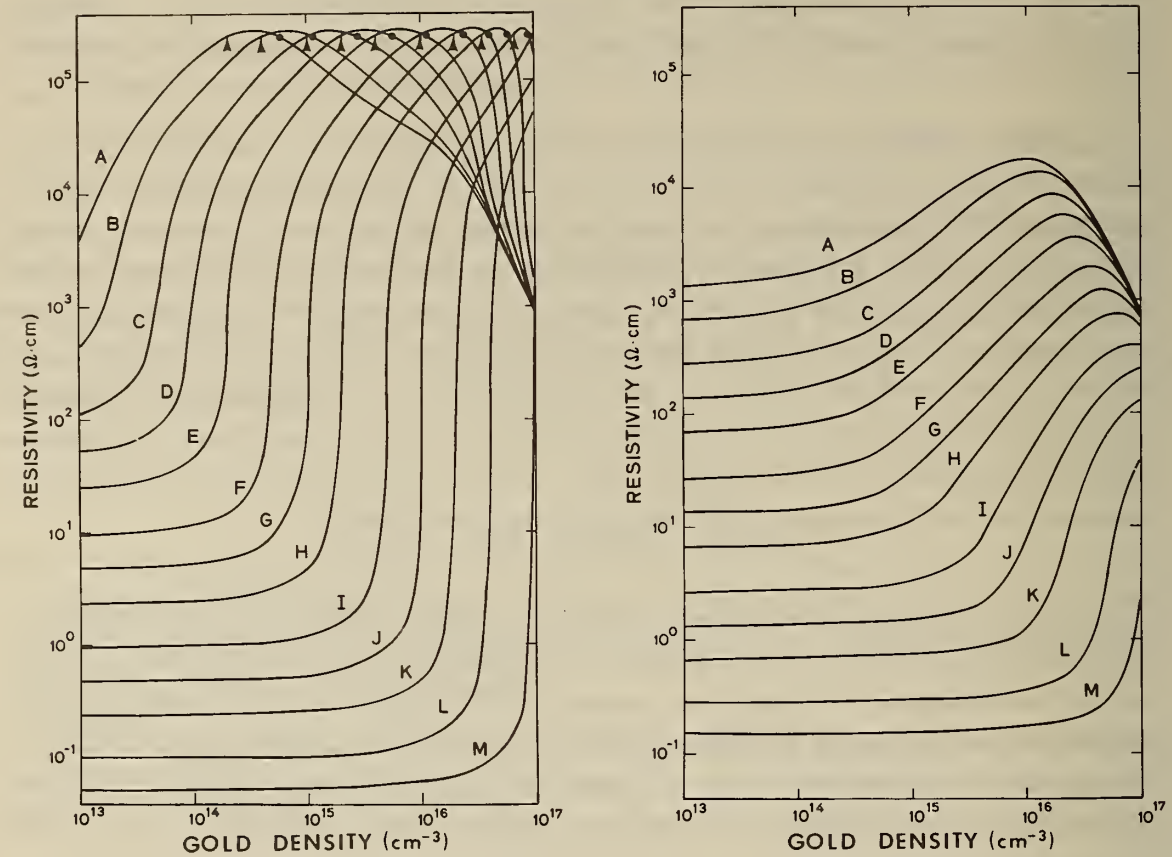
Figure 1a shows the resistivity at 300 K of initially n-type silicon for phosphorus densities from 10^{13} cm^{-3} to 10^{17} cm^{-3} while figure 1b is a similar plot for p-type silicon with boron as the acceptor dopant. A feature of the curves which does not appear to be in agreement with experiment is the position of the sharp increase in resistivity in n-type silicon as a function of the ratio of gold density to shallow donor density. The calculation predicts the increase to occur when the gold and shallow donor densities are equal, but experimental data [5] show that the rise does not occur until the gold density is about twice that of the shallow donor. Diffusions have been started on n-type silicon with initial resistivities of 0.3 and 1 Ω·cm to provide data which may assist in resolving this discrepancy.

(W. R. Thurber and W. M. Bullis)

Sets of p-type, gold-diffused wafers with initial resistivities of 0.08, 1, 300, and 2400 Ω·cm were characterized at room temperature by resistivity and Hall effect measurements. However, for several of the wafers, apparent gold densities determined by activation analysis exceeded the solubility limit for the temperature of diffusion. As the first step in understanding this anomaly, the Hall bars used for the electrical measurements have been submitted for determination of gold density by activation analysis.

Heat treatments in oxygen and argon atmospheres were carried out at 950°C for 168 h and at 1250°C for 8 h on wafers of float-zoned, n- and p-type silicon with initial resistivity at room temperature about 2300 Ω·cm. These treatments were performed in a new diffusion tube prior to its use for gold diffusion, with the same heating and quenching procedures used during gold diffusion. Resistivity (van der Pauw) and hot-probe conductivity-type measurements on the p-type wafers suggest that compensating donors at a density of 10^{12} to 10^{13} cm^{-3} were introduced by the heat treatment in general agreement with previous results on 1100-Ω·cm p-type wafers (NBS Tech. Note 733, p. 15). Greater changes occurred at 1250°C than at 950°C and, at the same temperature, more donors were introduced in the argon atmosphere than in the oxygen atmosphere.

Resistivity changes were measured in two gold-doped specimens annealed at temperatures other than the diffusion temperature. The resistivity of a specimen originally diffused to saturation at 950°C changed after annealing at 1150°C for 24 h to a value consistent with the gold density measured after annealing. Interpretation of this result is complicated by the fact that the total gold density increased by a factor of nearly three on annealing. The resistivity of a specimen diffused to



a. Phosphorous-doped silicon. At the arrowhead (on the ascending part of the curve) the electron density, n, equals the hole density, p. At the dot (on the descending part of the curve) the Hall coefficient, R_H, is zero. To the left of the arrowhead $n > p$; to the right of the dot $R_H > 0$.

b. Boron-doped silicon. The material is *p*-type throughout the entire range.

Shallow impurity densities (cm^{-3}):

A	1×10^{13}	F	5×10^{14}	J	1×10^{16}
B	2×10^{13}	G	1×10^{15}	K	2×10^{16}
C	5×10^{13}	H	2×10^{15}	L	5×10^{16}
D	1×10^{14}	I	5×10^{15}	M	1×10^{17}
E	2×10^{14}				

Figure 1. Calculated curves of resistivity of silicon as a function of gold density at 300 K for shallow impurity densities from 10^{13} to 10^{17} cm^{-3}.

saturation at 1250°C changed in a way consistent with some precipitation on annealing at 1050°C for 72 hours, but the final resistivity appeared to be characteristic of a gold density higher than the solid solubility at 1050°C.

(W. R. Thurber, A. W. Stallings, and J. Krawczyk)

Plans: Hall effect measurements as a function of temperature, begun this quarter, will be continued to determine the activation energies of the gold donor and acceptor levels and the gold-coupled shallow acceptor level. Evaluation of the heat-treated *p*-type silicon wafers will be extended to include Hall effect and lifetime measurements and the heat-treated *n*-type wafers will be characterized similarly.

3.4. INFRARED METHODS

Objective: To study infrared methods for detecting and counting impurity and defect centers in semiconductors and, in particular, to evaluate the suitability of the infrared response technique for this purpose.

Progress: The lithium-drifted germanium gamma-ray detectors studied to date have been grouped according to their infrared response (IRR) spectra into the five representative types described last quarter; nearly four-fifths of the poor quality detectors fall into two of the four spectrum types thought to indicate poor crystal quality.

The IRR of lithium-drifted silicon detectors was measured for the first time at room temperature as well as near 100 K.

Four silicon surface-barrier detectors and two silicon diffused-junction detectors were the first silicon devices that were not lithium-compensated to be studied successfully using the IRR technique.

Infrared Response Measurements on Germanium — Measurement of infrared response (IRR) and the comparison with the five spectrum types previously described (NBS Tech. Note 733, pp. 18-20) for lithium-drifted germanium diodes continued. The IRR spectra of seven diodes were obtained this quarter. Of the 48 diodes studied thus far, 25 percent exhibited spectra corresponding to that of a good quality gamma-ray detector, type (1). The remainder exhibited spectra of types thought to correspond to detectors of poorer quality: 38 percent like type (2); 12 percent like type (3); 4 percent like type (4); and 21 percent like type (5). Nearly four-fifths of the poorer quality diodes examined fell into types (2) and (5).

Table 3 summarizes the measured material characteristics common to most of the diodes found in each representative group. These characteristics are generally

Table 3 — Material Properties of Lithium-Drifted Germanium Detectors

Spectrum Type	Dislocation Density	Oxygen Density	Lithium Mobility
1	<2500 cm^{-2}	$<2 \times 10^{14}\ cm^{-3}$	High
2	<3500 cm^{-2}	$<3 \times 10^{14}\ cm^{-3}$	High
3	>5000 cm^{-2}	$>5 \times 10^{14}\ cm^{-3}$	Low
4	$>10^{4}\ cm^{-2}$	$>1 \times 10^{13}\ cm^{-3}$	High
5	2500-8000 cm^{-2}	$<2 \times 10^{14}\ cm^{-3}$	High

similar to those of the diodes listed previously (NBS Tech. Note 733, table 3, p. 20). It is interesting to note that the crystals yielding the poor quality detectors turn out to be grouped, using the IRR spectra, according to two of the major detector problem areas: trapping of one of the charge carriers or poor lithium drift mobility. The problem of poor diode characteristics (reverse leakage current as a function of bias voltage) does not appear to be separately differentiated by IRR. Of course, carrier trapping and poor diode characteristics are interrelated; if a sufficient field cannot be applied to the device, charge carriers may be trapped before being collected.

Problems manifested by crystals that exhibit IRR spectrum types (3) and (4) seem to be related to either the lithium-oxygen interaction or high dislocation density, respectively. Since these two type of crystals account for only a small fraction of detector problems and these problems can be identified by a lithium mobility measurement or dislocation density measurement before detector fabrication, they will not be considered further.

With regard to carrier trapping, identified with spectrum types (2) and (5), the problem is more complex. The origin of spectrum type (5) has not been identified. Spectrum type (2) is characteristic of the neutron-irradiated reference diode, but it is not possible at present to link the defects known to be produced in germanium by neutron irradiation directly with the defects that produce IRR spectra of this type in the test crystals. (A. H. Sher and H. E. Dyson)

To aid in interpreting the IRR spectra of germanium diodes, the infrared transmission spectra of a series of germanium filters of the various thicknesses used in the IRR measurements has been measured using the digital recording system (NBS Tech. Notes 702, pp. 12-13, and 717, p. 15). These transmission data, punched onto paper tape, can be subtracted from the diode IRR spectrum after proper normalization, thus removing both atmospheric absorption effects and filter transmission effects from the test spectrum. (W. J. Keery)

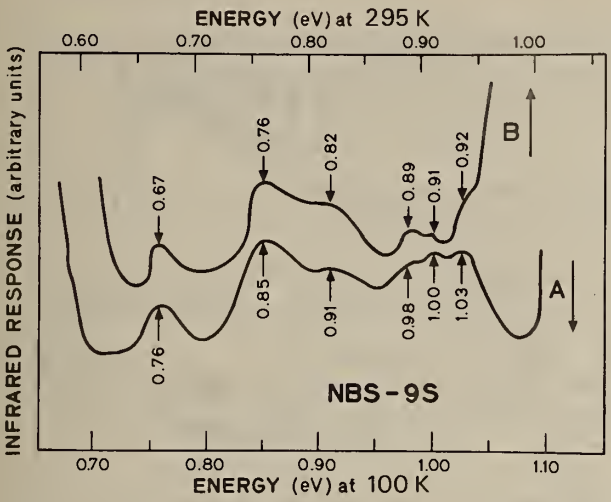


Figure 2. Infrared response spectra of a lithium-drifted silicon detector at 100 K (A, lower scale) and 295 K (B, upper scale).

Infrared Response Measurements on Silicon — Measurements of IRR on lithium-drifted silicon detectors continued. Two such diodes were examined: one, NBS-9S, was fabricated from 1000-Ω·cm, float-zoned, boron-doped silicon; the other, NBS-4S, had previously been studied after proton-irradiation [1], (NBS Tech. Note 727, pp. 18-20). Measurements were made at 100 K and, for the first time, at room temperature (about 295 K).

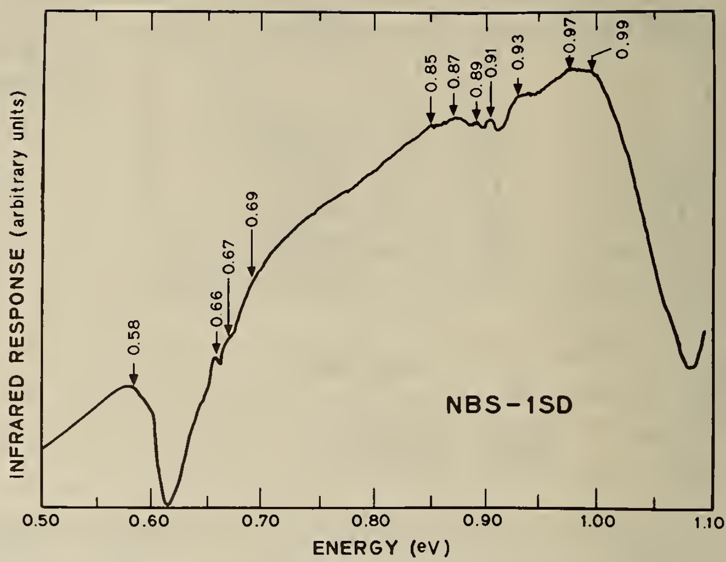
Figure 2 shows the IRR spectra of detector NBS-9S plotted with the room temperature spectrum shifted upwards in energy by 0.09 eV so that corresponding features coincide. This shift represents the energy difference between the bandedge peak energy of 1.17 eV at 100 K (NBS Tech. Note 717, pp. 16-17) and the energy of 1.08 eV at room temperature. The latter is within the range of values determined for the width of the forbidden energy gap in silicon near room temperature by a variety of methods. Possible relationships between the spectral features and energy levels in the forbidden gap have been discussed previously for other detectors [1].

Diode NBS-4S, previously irradiated with 1.9-MeV protons, was examined using the IRR technique after storage for approximately eight months at room temperature. The resulting spectrum showed a reduction in the number of features compared with the spectrum observed shortly after irradiation. That the spectrum was virtually identical to that of diode NBS-3S, the unirradiated companion detector to NBS-4S, is taken as evidence of long-term annealing effects.

(A. H. Sher, Y. M. Liu, and H. E. Dyson)

Late in the quarter, the IRR of four commercially-fabricated silicon surface-barrier detectors and two diffused-junction detectors was measured. This is the first time this technique has been successfully applied to silicon devices that

Figure 3. Infrared response spectrum of a silicon diffused-junction detector at 100 K.



were not lithium-compensated. The four surface-barrier detectors had approximately 15-nm thick gold barrier contacts on phosphorus-doped silicon. Two had depletion depths of 1000 μm and two had depletion depths of 100 μm. The two diffused-junction detectors had been fabricated by diffusing phosphorus into 1600 to 1800 Ω·cm, boron-doped silicon yielded depletion depths of about 100 μm under reverse bias.

Preliminary analysis of the spectra taken at both 100 K and 295 K, showed that the features of the spectra of the four surface-barrier detectors were similar to those obtained previously for the lithium-drifted devices. The spectra of the diffused-junction detectors were, however, different in overall shape. Figure 3 shows the spectrum of diffused-junction detector NBS-1SD obtained at 100 K. The spectra of the two diffused-junction detectors, which were virtually identical, had features which are less prominent compared with the background on which they ride than those of other silicon devices. In addition, features are observed below about 0.70 eV in the diffused-junction devices. In the spectra of other silicon devices, the high energy tail of the peak that is found at one-half the bandgap energy (about 0.58 eV) is continuous with the rest of the spectrum, and no distinct valley like the one at 0.62 eV in the figure is observed. Some of these differences may be due to the layer of damaged semiconductor material, about 0.5 μm thick, at the surface that results from the phosphorus diffusion. (A. H. Sher and Y. M. Liu)

<u>Plans</u>: The studies of IRR on germanium and silicon diodes will continue. The factors affecting the performance and IRR spectra of the germanium diodes that fall into the two main spectral types will be pursued. Further IRR analysis will be performed on silicon devices not compensated with lithium.

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4. SEMICONDUCTOR PROCESS CONTROL

4.1. DIE ATTACHMENT EVALUATION

Objective: To evaluate methods for detecting poor die attachment in semiconductor devices with initial emphasis on the applicability of thermal measurements to the problem.

Progress: The analysis of heat flow to determine the limitations of thermal response techniques for detecting poor die adhesion in semiconductor devices using the TRUMP computer thermal analysis program was delayed by program difficulties. A search is underway to find a tape of the program. (W. E. Phillips)

Experiments to apply the transient thermal response die attachment evaluation technique to transistors were continued. An attempt was made to measure the transient thermal response of a 25-W power transistor both in the transistor and diode operating modes. When the transistor was operated in the diode mode, in which collector is connected to the base and the base-emitter junction voltage is used as the temperature sensitive parameter, it was found that the heating current needed to give a junction-to-case temperature difference, ΔT_{JC}, sufficient for reproducible measurements was beyond the capabilities of the present test circuit.

When the transistor was operated as a transistor using a common-base, emitter-only switching technique (see sec. 5.1.) it was found that for a heating power of approximately 10 W the temperature-controlled heat sink could not be maintained at the set temperature for heating power pulse widths greater than 100 ms. The problem was discovered when it was found that for heating power pulse widths greater than 100 ms, the measured junction-to-case thermal response normalized to heating power, $\Delta T_{JC}/P$, was greater than the measured junction-to-case thermal resistance. This discrepancy is not encountered when measuring thermal resistance in the normal manner since the case temperature of the device under test remains constant, for all practical purposes, during the brief period, usually less than 200 μs, that the heating power is off and the temperature sensitive parameter is measured. The implication here is that even though a heat sink may have sufficient controlling capabilities for thermal resistance measurements, the system may not have sufficient capabilities for measurements of transient thermal response where temperature control at the case reference point has to be reestablished before the heating power pulse is terminated.

To overcome the current handling limitations of the present circuit [2], a new test circuit diagrammed in figure 4 is being constructed. This circuit is capable of measuring thermal response of power transistors in both the diode and transistor operating modes as well as of diodes. The principles of operation of this circuit have been described previously (NBS Tech. Note 727, pp. 27-29). When a diode is

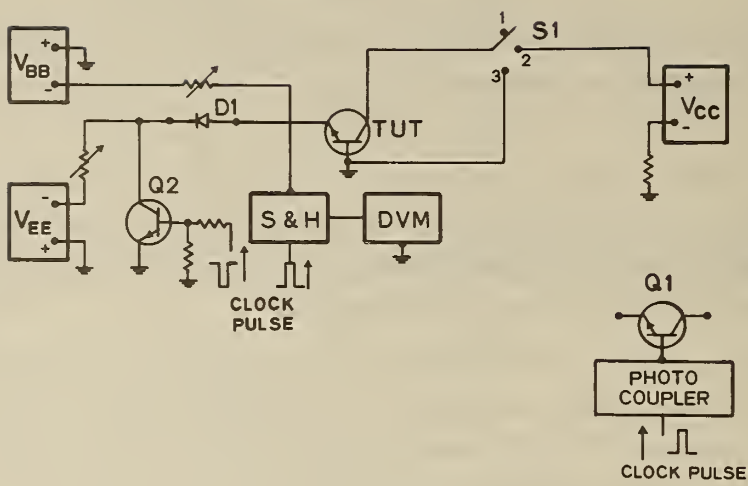

Figure 4. New thermal response measurement system for both diodes and *n-p-n* transistors.

being tested, switch S1 is open (position 1), disconnecting the collector supply. For testing transistors, switch S1 either connects the collector power supply to the device under test for normal transistor operation (position 2) or connects the collector of the device under test to its base terminal for the diode mode of operation (position 3). For some transistors it has been found that faster switching can be accomplished by replacing diode D1 by switching transistor Q1 to disconnect the heating power circuit a few microseconds after it is shunted through transistor Q2 to ground (see sec. 5.1.). Currents up to 5 A can be switched in this circuit.

(F. F. Oettinger and R. L. Gladhill)

Plans: The analysis of heat flow to determine the limitations of thermal response techniques for detecting poor die adhesion in the diodes previously investigated will continue after the revised TRUMP thermal analysis program is received and suitably modified for use on the NBS computer. The fabrication of the new test circuit will be completed. Measurements of thermal response of diode-connected transistors will then be resumed. In preparation for a study of quantitative relationships between thermal response of transistors and voids in the die attachment, several groups of transistors will be bonded to headers with voided regions; at the same time control groups without voids will also be bonded.

4.2. WIRE BOND EVALUATION

<u>Objective</u>: To survey and evaluate methods for characterizing wire bond systems in semiconductor devices and, if necessary, to improve existing methods or develop new methods in order to detect more reliably those bonds which will eventually fail.

<u>Progress</u>: The study of the feasibility of using ribbon wire for ultrasonic bonding was completed. The results showed that bonds with high pull strengths and good cosmetic appearance can be made using existing bonding machines with only slight modifications. It was shown that ribbon-wire bonds of a given quality can be made over a much greater range of ultrasonic power and time than can round-wire bonds of similar quality. Experimental study of factors that significantly affect the wire bond pull test on single-level substrates continued. It was found that pulling the bond out of the plane of the bond results in a slight decrease in measured pull strength with increasing angle. Additional measurements on unannealed round-wire bonds indicated that the measured pull strength could be predicted by the resolution-of-forces calculation for the range of bond parameters normally encountered, but there remains some uncertainty that the same holds for annealed bonds.

Ribbon-Wire Bonding — Since exploratory experiments showed that high quality bonds could be made with ribbon wire (NBS Tech. Notes 727, pp. 32-35, and 733, p. 27), the investigation was broadened to compare ribbon- and round-wire bonds over a wide range of power and time settings. Using the same bonding machine and tool*, bonds of both types were made with bond-to-bond spacings of 0.04 in. (1.0 mm) and loop heights of 0.010 in. (0.25 mm) side-by-side on the same metallized silicon substrate in order to minimize effects of variations in bonding conditions or substrate quality. The aluminum (1% silicon) wires used had approximately the same cross-sectional area. The dimensions were 0.0015 by 0.0005 in. (38 by 13 μm) for the ribbon wire and 0.001-in. (25-μm) diameter for the round wire. The thickness of the aluminum metallization was approximately 1 μm. The bonding tool force was held at 25 gf (245 mN); both power (tool tip displacement) and time were varied.

For each combination of displacement and time, 10 bonds were made and their pull strengths determined by pulling vertically at the midpoint of the loop. The average pull strength for each group is plotted against both time and tool tip displacement of figures 5 and 6 for ribbon- and round-wire bonds, respectively. The data points have been connected by straight lines to define planes each of which includes groups of bonds made at a constant time but with a range of power (tool tip displacement). For convenience, different symbols are used for groups with mean pull strength <7,

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* The use of the same tool for both round and ribbon wire results in less than optimum conditions for bonding ribbon wire.

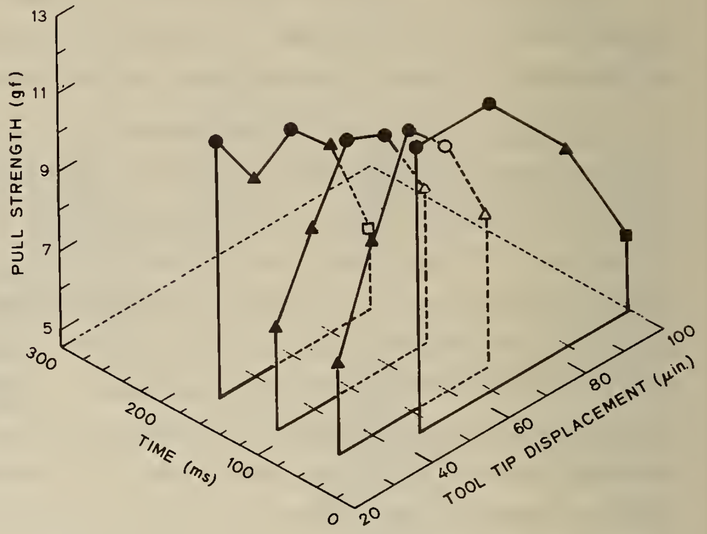


Figure 5. Pull strength of ribbon-wire bonds as a function of time and tool tip displacement. (Bond pull strength range is shown by symbols: ●,○ > 10 gf; ▲,△ 7-10 gf; and ■,□ < 7 gf.)

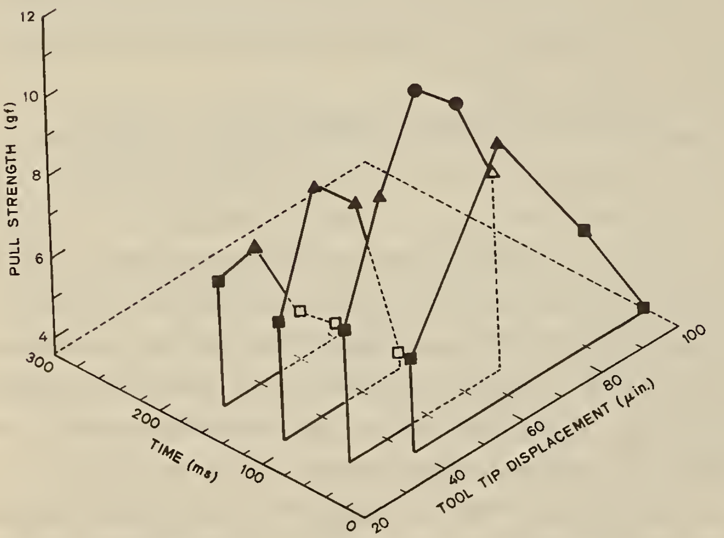


Figure 6. Pull strength of round-wire bonds as a function of time and tool tip displacement. (Bond pull strength range is shown as in figure 5.)

7-10, or >10 gf (<69, 69-98, or >98 mN). For simplicity, the variance is not indicated in the figures. Open points and short dashed lines indicate a portion of a plane lying behind another. In general, at the lower displacements, the major mode of bond failure was bond lift off while at higher power it was breakage at the heel of the bond.

The results of a statistical analysis of the bond data considered as a whole are summarized in table 4. The entries in this table are the averages of the mean pull strength of bond groups with mean pull strength in the specified range and the pooled sample standard deviation for the means. The number of groups included in each category is also given. On the average, bonds made using ribbon wire show a statistically significant 8 percent higher pull strength than bonds made with round wire on the same substrate with the same bonding force. About 90 percent of the ribbon-wire bonds showed

Table 4 — Comparison of Pull Strength of Ribbon- and Round-Wire Bonds[a]

Range (gf)	Ribbon[b]		Round[b]		Ribbon[c]	
	Strength (gf)	No.	Strength (gf)	No.	Strength (gf)	No.
> 10	11.3±0.7	8	10.5±0.2	2	11.0±0.4	14
7 - 10	8.7±0.4	9	8.6±0.6	6	8.8±0.4	5
< 7	6.7±0.4	2	5.3±0.7	11	3.9±0.7	2

[a] Note: 1 gf = 9.8 mN; gages calibrated in newtons are not yet readily available commercially.

[b] Bonds represented in these two columns were made on the same substrate with a bonding force of 25 gf.

[c] Bonds represented in this column were made on a different substrate with a bonding force of 35 gf.

pull strengths greater than 7 gf (69 mN) while only 42 percent of the round-wire bonds did for the power and time settings studied.

Also shown in table 4 are the results from a comparable series of ribbon-wire bonds made on a different substrate using a bonding force of 35 gf (343 mN). In terms of the bond pull strength, the use of higher force appears to result in more of the bonds having pull strength greater than 10 gf (98 mN). However, microscopic examination of the substrate used in the series with higher bonding force after removal of the bonds and metallization indicates detectable damage to the semiconductor substrate. Such damage was not observed in the substrate used at the lower force.

The experiments showed that a major advantage of using ribbon over round wire is that the use of ribbon wire requires less precise controls on bonding machine parameters to yield bonds of a certain quality than does the use of round wire. Although ribbon-wire bonds with high pull strength were obtained over a much wider range of power and time than was indicated in the exploratory experiments, observations confirmed that, as previously reported, the best cosmetic appearance was obtained at low power and long time. (H. K. Kessler and A. H. Sher)

Pull Test Evaluation — Experimental investigation of the influence of the pull rate, hook position, and pull angles on the measured pull strength of unannealed, round-wire bonds on single-level substrates was completed with a study of the pull angle α, the angle between the direction of pull and the normal to the substrate in the plane perpendicular to both the substrate and the plane of the bond loop. Since the principal effect of pulling at a finite value of α is to rotate the plane of the bond loop, the ratio of the force of pull and the force exerted along the wire is the

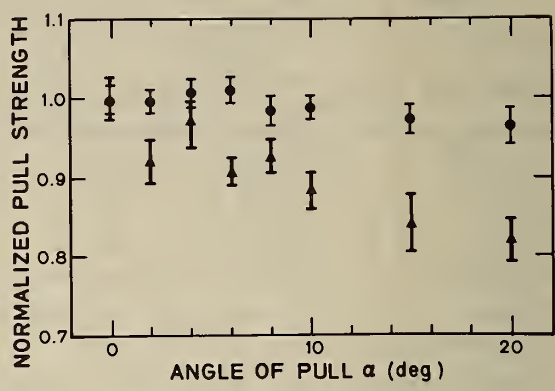


Figure 7. Normalized pull strength as a function of pull angle α for round-wire bonds with small (●) and large (▲) deformation. (Error bars represent the 95-percent confidence interval for the mean.)

same for all values of α. Consequently, no great dependence of the measured pull strength on α would be expected.

Bonds were made on three metallized substrates with 0.001-in. (25-μm) diameter aluminum (1% silicon) wire and a bond-to-bond spacing of 0.04 in. (1.0 mm). All the bonds on a particular substrate were made with the same power setting, but different power settings were used in making the bonds on different substrates to obtain bonds with different degrees of heel deformation. On each substrate, about 35 bonds were pulled at the midpoint of the loop for eight values of α from 0 to 20 deg. The pull angle β, in the plane of the bond loop, was 0 deg. For each group, the mean pull strength and the 95-percent confidence interval for the mean were determined; the measured pull strengths of bonds that did not break at the heel were excluded from the calculations. The pull strengths were then normalized to the mean value obtained at α = 0 deg. The results for bonds with small heel deformation (1¼ to 1½ wire diameters) and large heel deformation (2¼ to 2½ wire diameters) are shown in figure 7. The zero-degree value for pull strength of the bonds with large deformation was approximately half that of the bonds with small deformation. Bonds made on the third substrate had still larger deformation but yielded results essentially the same as those observed for bonds with large deformation.

The results show that as α increases the measured pull strength decreases slightly. This appears to be a result of the twisting or tearing of the bond heel as the wire is pulled out of the plane normal to the substrate plane. These results show that, although little effect on the pull test results from bonds with small to moderate heel deformation pulled at an angle α less than 10 deg, the effect is more pronounced for the bonds with greater heel deformation. It should be possible to control the position of the pulling hook so that the angle α is less than 10 deg by visual inspection, but more precise positioning may be required for bonds with large deformation. (K. O. Leedy, A. H. Sher, and C. A. Main)

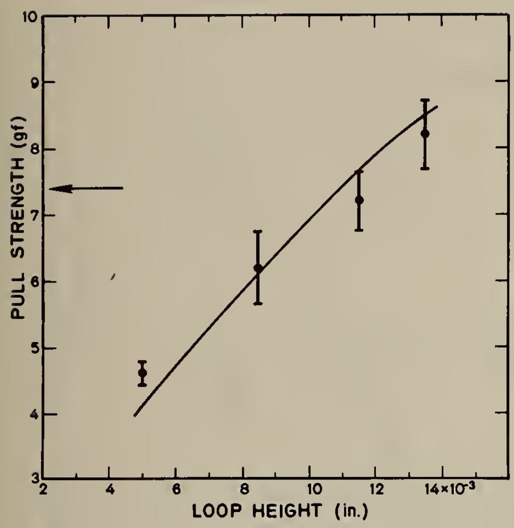
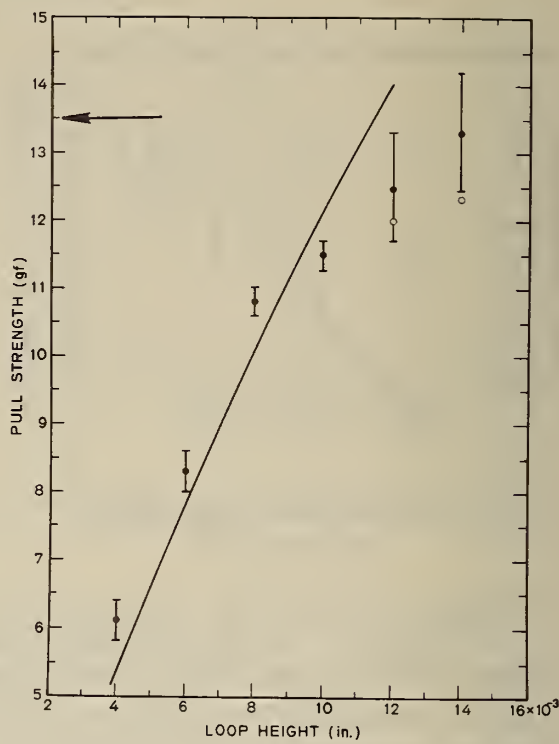


Figure 8. Pull strength of unannealed round-wire bonds as a function of loop height. (The data points represent the mean for up to 10 bonds; only bonds which ruptured at the heel were included. Error bars represent one sample standard deviation. The solid curve is calculated from resolution-of-forces using the wire tensile strength indicated by the arrow.)

Additional study was undertaken of the dependence of measured pull strength on loop height or bond angle to gain greater insight into the extent of applicability of the resolution-of-forces calculation (NBS Tech. Note 555, pp. 31-36). Previous measurements on unannealed bonds suggested that the results could (NBS Tech. Note 717, pp. 28-29) or could not (NBS Tech. Note 571, pp. 24-26) be predicted by resolution-of-forces. Analysis of the new results, shown in figure 8, supports the conclusion that the pull strength calculated by resolution-of-forces does fit the experimental data. Reexamination of the previously reported data in which the calculated best fit differed from that predicted from the resolution-of-forces shows that the data lying below $h/d = 1/3$, which corresponds to a loop height of about 0.013 in. (0.33 mm) for a bond-to-bond spacing of 0.04 in. (1.0 mm), agrees with the resolution-of-forces calculation. Above $h/d = 1/3$, several of the data points fall below the predicted value of pull strength. This is also true of the new data, but points for high h/d are not shown in figure 8. As the loop height increases, more normal pulling force is exerted on the bonds. The results of the study of the influence of the bond angle α suggest that this might cause some peeling of the bond before breakage at the heel occurs, which in turn might lower the measured pull strength. (A. H. Sher)

This conclusion is reinforced by the results of measurements of pull strengths of ribbon wire bonds as a function of loop height shown in figure 9. The solid data points are average pull strengths for groups of up to 10 bonds each, excluding those bonds that failed due to lift off of one of the bond pairs. For the two open data points at the two highest loop heights, values resulting from bond lift-offs were included in the average pull strength calculation. Up to a loop height of about 0.010-in.

Figure 9. Pull strength of ribbon-wire bonds as a function of loop height. (The data points represent the mean for up to 10 bonds. Solid circles include only bonds which ruptured at the heel; open circles include bonds which ruptured at the heel and which failed by lift off. Error bars represent one sample standard deviation. The solid curve is calculated from resolution-of-forces using the wire tensile strength indicated by the arrow.)



(0.25 µm), the variation of pull strength as a function of loop height is in agreement with the resolution-of-forces calculation, but at larger loop heights, the measured pull strength is lower than the predicted value. (H. K. Kessler and A. H. Sher)

Further experiments were also undertaken on annealed bonds. A previous experiment (NBS Tech. Note 717, pp. 28-29) suggested that the pull test data on annealed bonds did not fit the resolution-of-forces prediction although an earlier measurement at a single loop height (NBS Tech. Note 592, p. 36) appeared to have been correctly predicted by resolution-of-forces. The comparison between experimental data obtained on annealed bonds and the resolution-of-forces calculation is complicated by the elongation of the annealed wire. As the pulling force is exerted on the wire loop, the wire stretches with little increase in force in the wire until just before rupture occurs. For the new measurements, bonds were made using the same wire and substrate as those used for the new test on unannealed bonds. The bonds were then annealed by heating them to 505°C for 25 min. The loop heights were calculated from the measured lengths of sections of the rupture. The results thus obtained were confirmed by measurements of other wire spans pulled just to the point of breakage. The total elongation of the wire was found to be as large as 11 percent which results in an increase in loop height by as much as 87 percent for the smallest initial loop height used, about 0.006 in. (0.15 mm). The pull strengths obtained are plotted in figure 10. Both wire breaks and heel breaks were included in the averaging; there

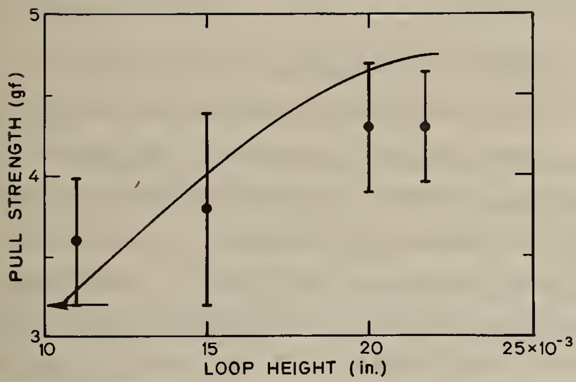


Figure 10. Pull strength of annealed round-wire bonds as a function of loop height. (The data points represent the mean for up to 10 bonds; both bonds which ruptured at the heel and in the wire were included. Error bars represent one sample standard deviation. The solid curve is calculated from resolution-of-forces using the wire tensile strength indicated by the arrow.)

appeared to be no significant difference between the mean strength of bonds that broke in the wire and that of bonds that broke at the heel. Unlike the data for pull strength of the unannealed bonds, statistical analysis shows that these data do not fit the resolution-of-forces prediction. Additional experiments are being conducted to search for the cause of this disagreement. (A. H. Sher)

Bibliography and Critical Review — Editorial review procedures for the critical review and survey paper on fabrication and testing of wire bonds were completed and the camera-copy of the manuscript is being prepared for publication as NBS Technical Note 726. The survey is generally restricted to wire-bond electrical connections made with wire of diameter less than about 0.002 in. (0.05 mm) by either thermocompressive or ultrasonic means. Under the general heading of fabrication, the essential features of the thermocompression and ultrasonic bonding processes, the fabrication procedures, and the characteristics of the constituent materials of the wire bond pertinent to high reliability are surveyed. Also included is a review of the interaction of gold and aluminum which, unless suitable precautions are taken, is one of the primary causes of potential failure of wire bonds. The following test methods are discussed with emphasis on their capabilities and limitations: visual inspection; pull, shear, air blast, push, ultrasonic stress, centrifuge, mechanical shock, variable frequency vibration, vibration fatigue, short-duration stress pulse, temperature cycling, thermal shock, bond interface resistance, and electrical continuity tests; noise measurement; and ultrasonic bond monitoring. Analyses of the pull, centrifuge, mechanical shock and vibration, and temperature cycling tests were made with particular regard to the stress that the tests impose on the wire bond, and the results were used in discussing these test methods. To assist the reader in the use of the extensive review, a subject index has been added and key words or phrases have been placed in the margins.

Preparation of the annotated bibliography of limited distribution reports was resumed. (H. A. Schafft)

Plans: A report summarizing the work on ribbon-wire bonding will be prepared for publication as an NBS Technical Note. Further pull tests as a function of pull rate and bond angle will be made on annealed bonds made on single-level substrates to gain further insight into the reasons for lack of agreement between the measured values of pull strength and the values calculated from resolution-of-forces. Experimental study of the pull test on bonds made on two-level substrates will begin. Substrates will be fabricated, the positioning of the pulling hook will be examined, and the bond pull strength will be measured as a function of loop height or of bond angle to determine the agreement with the resolution-of-forces calculation. Preparation of a report summarizing the effects of various parameters affecting the pull test will begin. The critical survey paper will be published and distributed. Compilation of the annotated bibliography of limited distribution reports on wire bonds will continue. New work will be undertaken to develop aluminum ball bonding techniques.

4.3. REFERENCES

4.1. Die Attachment Evaluation

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2. Lockett, R. A., Bell, H. A., and Priston, R., Thermal Resistance of Low Power Semiconductor Devices under Pulse Conditions, *Mullard Tech. Comm.* 76, 146-161 (1965).

5. SEMICONDUCTOR DEVICES

5.1. THERMAL PROPERTIES OF DEVICES

Objective: To evaluate and improve electrical measurement techniques for determining the thermal characteristics of semiconductor devices.

Progress: Investigations were continued of the measurement of thermal resistance to compare the use of the common-base, emitter-and-collector switching technique with the common-base, emitter-only switching technique. In both cases the emitter-base junction voltage is used as the temperature sensitive parameter. The investigation of the current and temperature dependence of common-emitter current gain continued.

Standardization Activities — The devices for the preliminary round robin on thermal resistance being conducted in cooperation with EIA-JEDEC Committee JC-25 on Power Transistors are in the hands of the sixth participant. The percent relative sample standard deviation of junction-to-case thermal resistance (at delay times of 50 μs) for the four measurements made with the collector-base voltage, V_{CB}, as the temperature sensitive parameter ranged from 10 to 28 percent for the 14 test devices. For 10 of the 14 devices the percent relative sample standard deviation was 16 percent or less for the four measurements. Two of the participants also made measurements using the base-emitter voltage, V_{BE}, as the temperature sensitive parameter. As expected on the basis of previous work (NBS Tech. Note 727, pp. 46-47), the thermal resistance measured using V_{BE} was higher than the value obtained by the same participant using V_{CB}.

Measurements of junction-to-lead-wire thermal resistance were made on 39 axial-lead signal diodes as part of a preliminary round-robin experiment being conducted by EIA-JEDEC Committee JC-20 on Signal Diodes. Measurements were made using the existing die attachment evaluation equipment and a delay time of 50 μs.

A draft report, Methods for Specifying and Measuring Thermal Parameters of Microelectronic Devices, which deals with a number of techniques for electrically measuring the thermal characteristics of microelectronic devices, was prepared. This report is available to people interested in the work of EIA-JEDEC Task Group JC-11.3-1 on Thermal Considerations for Microelectronic Devices.

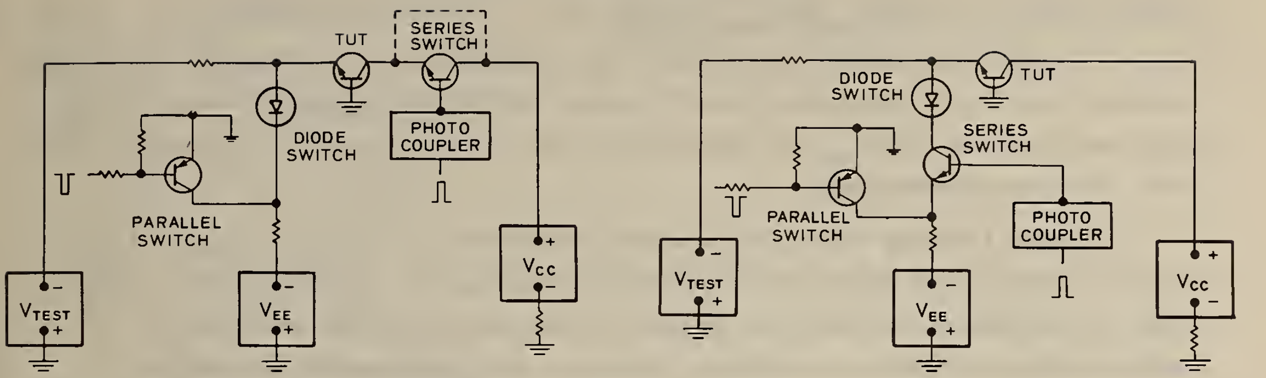
Revision of test procedures for Thermal Characteristics, Method 1012 of MIL-STD-883, Test Methods for Microcircuits, was undertaken at the request of the cognizant agency. Changes are being based on documents on thermal measurements of semiconductor devices prepared for EIA-JEDEC Committee JC-25 (NBS Tech. Note 733, p. 34) and Task Group JC-11.3-1 (see above).

(F. F. Oettinger, S. Rubin, and R. L. Gladhill)

Thermal Resistance Methods — Previous comparison (NBS Tech. Note 733, pp. 34-36) of the emitter-only switching technique with the emitter-and-collector switching technique for measuring thermal resistance indicated that the difference between the straight-line extrapolation to zero power of the measured value of the temperature sensitive parameter (TSP) as a function of power and the d-c calibration value at the zero-power level is reduced when using the emitter-only switching technique. Also it was found that when using this technique the measured junction temperature more closely approached the peak surface temperature as measured with an infrared microradiometer. Since the collector voltage is kept on while measurements are made with emitter-only switching, it is necessary to calibrate the TSP against temperature with the collector voltage on. If the measurement is made between two power levels, it might appear to be necessary to have two calibration curves, one for the collector voltage appropriate to each power level. However, calibration curves made in this manner, although displaced by an amount consistent with the power dissipated, were found to have essentially the same slope. For example, slopes of calibration curves made with a test current of 6.5 mA on a transistor of the single-diffused type at collector voltages of 1, 10, 60, and 80 V were found to vary by less than 1 percent. As a result, negligible error is introduced into measurements using emitter-only switching if the calibration curves derived with a collector voltage of 1 V are used. This is convenient for experimental measurements using many collector voltages.

An experiment was also performed to determine how the measured thermal resistance varies with magnitude of the test current. Previous measurements using emitter-and-collector switching indicated that the measured thermal resistance generally decreased as the test current was increased (NBS Tech. Note 727, p. 47). A preliminary comparison, using a transistor that had previously shown variations in thermal resistance as a function of test current, indicated that for emitter-only switching the variation is considerably less.

Previously, emitter-only switching measurements were made with the circuit shown in figure 11a on a transistor with a base width of 2.5 μm. When wider base devices were used it was found that a significant non-thermal transient when switching from heating to test current lasted up to five times longer than the transient encountered when switching both emitter and collector. The long transient occurred for both high-current, medium-voltage (1 A, 20 V) and moderate-current, high-voltage (400 mA, 70 V) heating conditions. It was found that the diode switch did not switch quickly enough when the parallel switching transistor in the emitter of the transistor under test (TUT in fig. 11a) turned on. This problem appears to be corrected by the addition of a switching transistor in series with the emitter of the TUT as shown in the modified circuit of figure 11b. (S. Rubin and F. F. Oettinger)



a. Emitter-and-collector switching circuit. If the series switching transistor is shorted, as indicated by the dashed line, the circuit becomes the initial emitter-only switching circuit.

b. Emitter-only switching circuit with a transistor switch in series with the diode.

Figure 11. Grounded-base configurations for thermal resistance measurements.

Screen For Hot Spots — Collector current density, through its effect on current gain, h_{FE}, and other device parameters, plays an important role in the initiation and stabilization of hot spots. If one knew the temperature distribution on the surface of a device, the associated current density distribution could be computed. The simplest case is to assume that in a constricted mode all the current is uniformly distributed within the hot spot. Then, the current density would be inversely related to the area of the constricted region. Alternatively, the peak temperature in the hot spot region can be directly related to the power density [1], (NBS Tech. Note 733, pp. 24-26).

Temperature profiles were made by means of an infrared microradiometer on two similar transistors in the region where a hot spot formed. Two profiles were made with the device operating in the constricted mode: one at a collector-emitter voltage, V_{CE}, just below that at which the hot spot was formed, the other at a lower V_{CE} just before the hot spot was quenched. A third profile was made with the device operating in the non-constricted mode. In all cases the collector current was maintained at 0.1 A and the case temperature at 25°C. In repeated measurements in the constricted mode it was found that the peak temperature was about 10 times more reproducible than the separation between the half-power points which is characteristic of the hot-spot diameter. Consequently, the peak temperature was used to estimate the current density.

Just after formation of the hot spot, the current density was about 4.9 times that in the non-constricted mode; at the lower voltage, just below quenching, the current density was lower, about 3.7 times that in the non-constricted mode. Based on typical data from the device data sheet, this decrease in current density and the associated decrease in temperature could account for the 65 percent decrease in h_{FE} which was observed when V_{CE} was reduced from the point of hot-spot initiation to the point of hot-spot quenching.

A circuit is being fabricated so that measurements of h_{FE} as a function of collector current for different temperatures under pulsed conditions (80 μs pulse width, 60 Hz repetition rate) can be made on the actual devices under study. A sample-and-hold circuit is also being made to facilitate these measurements.

(D. L. Blackburn and F. F. Oettinger)

Bibliography — Indexing of articles on thermal measurements of semiconductor devices was continued. Key words were assigned to articles which were published between 1952 and 1962. (F. F. Oettinger)

Plans: Work on standardization activities related to thermal measurements will continue. Thermal resistance measurements will be made using emitter-only switching on a variety of power transistors as a function of device operating conditions. These measurements will be compared with both thermal resistance measurements made with collector-and-emitter switching and infrared microradiometer measurements. The study of the effect of hot-spot formation, stabilization, and quenching on h_{FE} will be continued to determine whether several of the observations made during use of the h_{FE} screen test for hot spots are consistent with proposed theories. The circuits for measuring h_{FE} under pulsed conditions will be completed. The literature search and work on the bibliography on thermal measurements of semiconductor devices will be postponed for several quarters.

5.2. MICROWAVE DEVICE MEASUREMENTS

Objective: To study the problems and uncertainties associated with the measurement of electrical properties of microwave diodes, and to improve the techniques of these measurements.

Progress: Experiments are underway to measure the reproducibility of the system for measuring mixer conversion loss by the incremental modulation method (NBS Tech. Note 733, pp. 39-40) and to determine the sensitivity of the measurement to system characteristics such as local oscillator power variations and accuracy of the output circuit null setting. Because a stable and reproducible local oscillator power level is essential to the conduct of reproducibility studies over a long period, the investigation of the stability of the local oscillator power was continued.

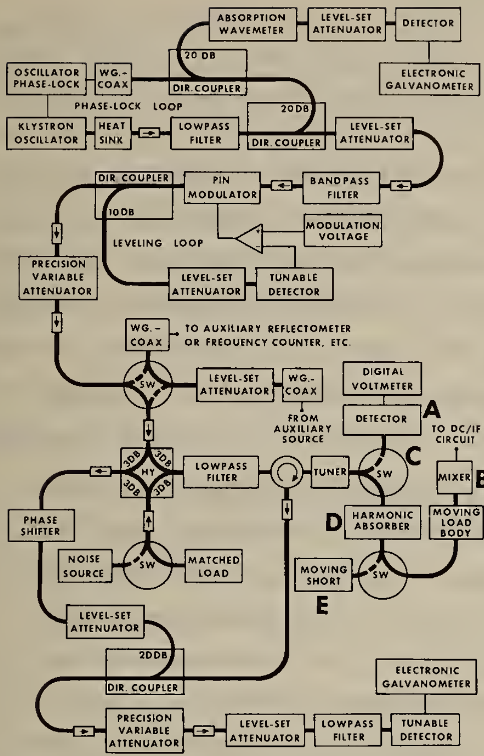


Figure 12. R-f section of microwave mixer measurement system.

Over a period of several weeks, local oscillator power was measured daily with a dry calorimeter (thin-film thermocouple) at the power monitor position (A, fig. 12) near the mixer and with a second dry calorimeter or with a thermistor bolometer at the mixer location (B, fig. 12). A waveguide switch (C, fig. 12) allowed the r-f power to be directed toward either the monitor or the mixer. This switch was tested and found not to introduce any instability into the measurement. Power drift at the mixer location was found to be six to ten times greater than the drift, typically less than 0.3 percent per day, at the power monitor. This drift was determined to arise from the temperature dependence of the attenuation of the unfired steatite harmonic absorption pad (D, fig. 12); considerable improvement was obtained by replacing this pad with one made from nylon. Since even the nylon pad exhibited some temperature sensitivity, the moving short used for reflectometer measurements (E, fig. 12) has been temporarily replaced by a dry calorimeter of the same type as that used in the power monitor position. This new calorimeter can thus monitor the power at the output side of the pad, but at the expense of losing the reflectometer function. The lower loss of the nylon pad may also lead to a somewhat greater systematic error due to a greater return of harmonics generated by the mixer. By permitting measurements to be made at reduced klystron beam voltage, its use may result in longer klystron life.

To permit reproducibility studies over long time periods, it is essential to have a reprodicible local oscillator power standard. The calorimeter replacing the moving short was found to have an output of 499 μV when the local oscillator power available to the mixer from a line-matched source (SWR < 1.01) was 1 mW. This power level was established by replacing the mixer with calibrated thermistors. These bolometric measurements were reprodicible to within ±1 μW including the effects of removal and reattachment of the thermistor mounts. The systematic error in setting the power level from this group of power measurements is presently estimated to be about ±12 μW, most of which (±7 μW) is the uncertainty assigned to the thermistor calibration. The investigation of power uncertainty is still incomplete, however. The calorimeter output can be maintained constant during the course of a measurement to within about ±0.25 μV, indicating an additional random power uncertainty of no more than about ±0.5 μW. (J. M. Kenney)

Initial experiments were conducted to identify the most stable diodes for use in subsequent tests of system stability as well as to obtain sensitivity data. All diodes currently on hand which have a loss less than 6 dB, the specified limit for 1N23 diodes, were measured over 24-h intervals. Of the 35 loss measurements generally made during a sequence, which was usually started in an afternoon and completed the following morning, 16 (every other one but one) were made under one of two non-standard conditions. The non-standard conditions introduced were intentional changes in either in setting the local oscillator power or in establishing the output circuit null used to provide distinct a-c and d-c loads on the mixer. Variations of these two conditions were made separately on an alternating basis, generally with eight power variations and eight null variations.

It was found that conversion loss, which was calculated assuming standard conditions, varied linearly with power over the error range which initially was ±120 μW and later was reduced to ±24 μW. This power sensitivity, slightly less than -0.005 dB/μW, was constant to within the reproducibility of the measurements for all diodes studied. Combining this sensitivity with the estimated power uncertainty discussed above, it can be seen that this factor alone contributes a systematic loss uncertainty of at least ±0.06 dB, of which ±0.035 dB is due to the thermistor calibration uncertainty. This is clearly a major limit on conversion loss measurement accuracy.

The error in conversion loss due to null error, which would affect the d-c self-bias on the diode, and therefore the r-f immittance of the mixer, was, as expected, not consistent for the diodes measured, nor was it linear with null error. For most diodes the loss increased for extreme null errors of one or both polarities, as would be expected for diodes which yield a good r-f line match under nominal conditions, although for some the loss was slightly reduced. Only absurdly large null errors, over 2500 times larger than the range normally maintained during the measurement, resulted in loss values that were obviously distinguishable from the values taken under standard conditions. It was concluded, therefore, that the uncertainty contribution from this source can be neglected.

The reproducibility of these daily measurements is of less significance than that to be determined by the longer-period studies to follow, but it was observed in the five best of these daily runs that more than 90 percent of the loss values measured under standard conditions were within ±0.02 dB of the mean value.

(J. M. Kenney, M. L. Kite, and S. Eshleman)

Plans: The conversion loss reproducibility study will be continued; measurements of longer duration will be made. Only the diodes which appear to be most stable will be used in the final evaluation of reproducibility, and they will be left in the holder continuously during the evaluation period. Several of the 24-h measurement runs will be repeated.

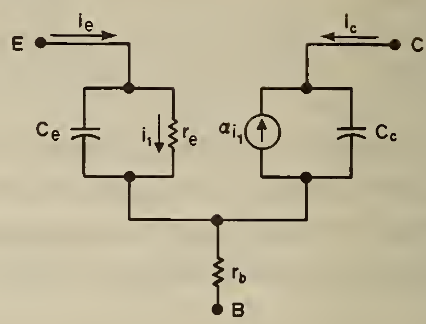
5.3. CARRIER TRANSPORT IN JUNCTION DEVICES

Objective: To improve methods of measurement for charge carrier transport and related properties of junction semiconductor devices.

Progress: Analytical work was continued to predict the effects of extraneous signals in delay-time apparatus on the measurement of delay in transistors as represented by an equivalent circuit which realistically incorporates the device passive elements. A large protion of project activity was devoted to assembling equipment and establishing techniques for measurement of transistor high-frequency S-parameters while the devices are at the wafer stage of preparation. The format for specifying the laboratory procedure for intercomparison of S-parameter measurements was completed, and the procedure was tested on discrete devices using an automatic network analyzer.

Analysis of Effects of Extraneous Signals on Transistor Delay-Time Measurements — The analysis of errors arising from extraneous signals at the measurement frequency was continued with the calculation of the effects of such signals in the Sandia bridge [1] on a transistor as represented by the small-signal model shown in figure 13. In previous work (NBS Tech. Note 733, pp. 41-44) three extraneous signals were included, one each in the emitter, collector, and detector return circuits. Further analysis showed that any source in the detector return circuit does not affect the result since the observation is made under conditions of zero current in this path. If the delay time measurements are referenced to an emitter-collector short, as described previously, the effect of an extraneous signal source in the emitter return circuit is cancelled but that of an extraneous signal source in the collector return circuit is not.

Figure 13. Small-signal model for transistor.



The analysis shows that the measured delay time, τ_m, is given by:

$$\tau_m = \tau_t - \left\{ \frac{1}{h_{fe}} \frac{(R_z + r_b + r_e)}{R_z} + \frac{r_e}{R_z} \right\} \frac{j}{\omega} \, Im\left(\frac{V_b}{V_e}\right),$$

where τ_t is the delay time of the transistor, h_{fe} is the small-signal, common-emitter current gain, R_z is the characteristic impedance of the bridge (100 Ω), r_b is the base resistance, r_e is the dynamic emitter resistance, ω is the measurement frequency, V_b is the extraneous signal source in the collector return circuit, and V_e is the signal source in the emitter circuit. This can also be expressed in terms of the delay time zero shift, $\tau_s - \tau_{rs}$, where τ_s is the value for a short between the emitter and collector terminals and τ_{rs} is the value for a resistor of value R_s:

$$\tau_m = \tau_t - \left\{ \frac{1}{h_{fe}} \frac{(R_z + r_b + r_e)}{R_s} + \frac{r_e}{R_s} \right\} (\tau_s - \tau_{rs}) \, .$$

Measurement of High-Frequency Transistor Parameters at the Wafer Level — Work has been undertaken to assist a sponsor in a project designed to evaluate the S-parameters of each transistor in a special integrated circuit wafer before interconnection. The emitter, base, and collector contacts of each transistor are brought out to arrays of in-line, square bonding pads 2 mils (0.051 mm) on a side, spaced 3 mils (0.076 mm) center-to-center. The sponsor has written the specifications for the probe assemblies to contact the pads for electrical measurements, and has procured six, three of which have the common (or circuit return) probe in the center, and three of which have the common probe at one end. The gold-plated beryllium-copper probes are bonded to the perimeter of a 2.5 mm diameter hole in a sapphire plate approximately 0.65 mm thick. The beryllium-copper pieces are bent 90 deg around the hole rim and end about 0.3 mm below the surface of the sapphire as in-line tips spaced about 3 mils (0.076 mm) between centers. The construction allows one to determine, by looking through the hole in the sapphire plate, which portions of the bonding pads are contacted by the probe tips. The sapphire plate also serves as the dielectric of 50-Ω strip transmission lines made by depositing two metal-film stripes on the sapphire, one connected to each of the two above-ground probes. Each stripe is flanked by deposited metal films connected to the common probe. The probe and strip-line assembly is protected by mounting the sapphire plate in a sturdy, rectangular brass case, open in the center. The case also serves as the mount for two 50-Ω miniature coaxial connectors connected to the ends of the metal-film stripes remote from the probe tips. These probe assemblies may be mounted in an integrated circuit prober, and, with the proper interface equipment, can be used to acquire automatically S-parameter measurement data on transistor arrays. (D. E. Sawyer)

Before S-parameter values for devices connected across the probe tips can be determined, it is necessary to determine the influence of the probe assembly on these measurements. This may be done by considering each of the two circuits beginning at the connectors and ending at the contact pads as two-port networks. Each circuit may be represented by three initially unspecified admittances connected in a pi configuration. By placing known impedances across the probe tips, the network unknowns are determined from impedance measurements at the connector ports. With the network now known completely, the measured S-parameter values may be corrected for the effects of the probe assembly. Relationships between the impedance at the connector ports and the network unknowns have been derived for appropriate combinations of shorts, opens, and resistances across the probe tips. (L. E. Huntely*)

Probe reference units, containing the necessary combinations of shorts, opens, and resistances are being fabricated. The pattern array that was designed also contains a special structure to permit determination of the resistance between the contact pads and the resistor film. (T. F. Leedy, P. M. Sandow, and D. E. Sawyer)

The thin, metal-film resistors have been shown to have a resistance that is independent of frequency over the range of interest; hence their value can be established by conventional d-c potentiometric methods. A work station equipped with a microscope has been assembled to allow probe reference unit wafers to be translated and rotated in the horizontal plane and raised and lowered in the vertical plane so that the resistance of any desired probe reference unit may be measured by bringing it into contact with a set of four electrolytically sharpened probes which are connected to a standard four-probe electrical circuit [2].

An entirely separate work station, with features similar to the one described above, has been assembled for use in obtaining the data necessary to characterize the electrical properties of a high-frequency probe assembly. In this work station, a probe assembly and a probe reference unit wafer can be moved relative to each other,

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* NBS Electromagnetics Division

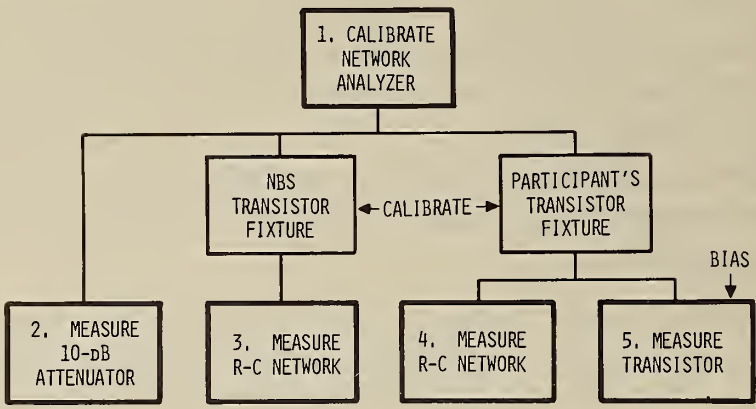

Figure 14. Format for interlaboratory test of S-parameter measurements on transistors.

and thus a known termination such as a short, open, or resistance can be placed across the appropriate probe tips.

The instrument for measuring probe loading (NBS Tech. Note 733, pp. 9-10) was adapted for use in checking the mechanical properites of the probe assemblies by adding suitably designed jigs. It is now ready for measurements of probe restoring force. By pressing the probe tips against a layered strip of aluminum on silicon oxide on silicon placed in the apparatus to simulate transistor bonding pads, it can also be used to record any significant tendency of the probe tips to wander or skate when applied to the contact pads. (F. H. Brewer and G. P. Spurlock)

Interlaboratory Comparison of S-Parameter Measurements — A format specifying the laboratory procedure for intercomparison of S-parameter measurements (NBS Tech. Note 733, pp. 44-45) was developed as indicated in figure 14. Plans call for the measurement of passive elements in addition to transistors so that both the measurement systems and the transistor measurements can be compared. The NBS transistor fixture, a 10-dB fixed attenuator, an R-C network, and the test transistors are to be circulated among the participants.

Measurement by all the participants of the same 10-dB fixed attenuator permits comparison of the measurement systems and their calibration without the transistor fixture. Measurement of an R-C network mounted on a TO-72 header using each transistor fixture serves to check the calibration of the fixtures and to disclose differences in results caused by differences in the transistor fixtures or their calibration.

The transistor measurements are to be made only with the participant's fixture. Variations may occur because of differences in bias, temperature, or transistor characteristics in addition to differences in the measurement systems. The transistor bias and temperature must be monitored closely enough to minimize the effect of these parameters. Auxiliary conditions have been defined to assure that the transistor characteristics are as stable as possible and to detect such changes in transistor characteristics as may occur during the interlaboratory comparison. These include use of transistors which have been burned-in for 168 h and measurements of their characteristics before, during, and after the tests. The results of the 10-dB attenuator and R-C network measurements are expected to provide additional means for distinguishing differences in results caused by the measurement system from those caused by changes in transistor parameters.

A single-operator, single-laboratory trial of this procedure conducted with the facilities at the NBS Boulder Laboratories disclosed no major flaws in the procedure or conditions of measurement. (G. J. Rogers)

Plans: Sources of error in delay-time measurement instruments other than the Sandia bridge will be investigated, and means of reconciling the measured values of delay time obtained from the several systems being investigated will be explored. Measurements of the mechanical attributes, such as probe force and possible motion of the probe tips, of the probe assemblies will be made. Transistor S-parameter measurements will be continued, and S-parameter measurements on the R-C plug-in elements will begin.

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5.3. Carrier Transport in Junction Devices

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2. Standard Method for Measuring Resistivity of Silicon Slices with a Collinear Four-Probe Array, ASTM Designation F84-72, *Annual Book of ASTM Standards*, Part 8. Available as a separate reprint from American Society for Testing and Materials, 1916 Race St., Philadelphia, Pa. 19103.

APPENDIX A
JOINT PROGRAM STAFF

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Consultant: C. P. Marsden

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APPENDIX B
COMMITTEE ACTIVITIES

ASTM Committee F-1 on Electronics

- W. M. Bullis, Editor, Subcommittee 4, Semiconductor Crystals; Leaks, Resistivity, Mobility, Dielectrics, and Compound Semiconductors Sections
- J. R. Ehrstein, Chairman, Resistivity Section; Epitaxial Resistivity, and Epitaxial Thickness Sections
- J. C. French, Committee Editor
- G. G. Harman, Secretary, Interconnection Bonding Section
- B. S. Hope, Committee Assistant Secretary
- K. O. Leedy, Chairman, Interconnection Bonding Section
- T. F. Leedy, Photoresist and Dielectrics Sections
- C. P. Marsden, Committee Secretary
- R. L. Mattis, Lifetime Section
- W. E. Phillips, Chairman, Lifetime Section; Secretary, Subcommittee 4, Semiconductor Crystals; Crystal Perfection, Dielectrics, Encapsulation, Thin Films, and Thick Films Sections
- A. H. Sher, Germanium Section
- W. R. Thurber, Mobility, Germanium, Compound Semiconductors, and Impurities in Semiconductors Sections

ASTM Committee E-10 on Radioisotopes and Radiation Effects

- W. M. Bullis, Subcommittee 7, Radiation Effects on Electronic Materials
- J. C. French, Subcommittee 7, Radiation Effects on Electronic Materials

Electronic Industries Association: Solid State Products Division, Joint Electron Device Engineering Council (JEDEC)

- J. M. Kenney, Microwave Diode Measurements, Committee JC-21 on UHF and Microwave Diodes
- F. F. Oettinger, Chairman, Task Group JC-11.3-1 on Thermal Considerations for Microelectronic Devices, Committee JC-11 on Mechanical Standardization; Technical Advisor, Thermal Resistance Measurements, Committees JC-22 on Rectifier Diodes and Thyristors, JC-20 on Signal Diodes, JC-25 on Power Transistors, and JC-30 on Hybrid Integrated Circuits
- S. Rubin, Chairman, Council Task Group on Galvanomagnetic Devices
- D. E. Sawyer, Task Group JC-24-5 on Transistor Scattering Parameter Measurement Standard, Committee JC-24 on Low Power Transistors
- H. A. Schafft, Technical Advisor, Second Breakdown and Related Specifications, Committee JC-25 on Power Transistors

IEEE Electron Devices Group:

- J. C. French, Standards Committee
- J. M. Kenney, Chairman, Standards Committee Task Force on Microwave Solid-State Devices II (Mixer and Video Detector Diodes)
- H. A. Schafft, Chairman, Standards Committee Task Force on Second Breakdown Measurement Standards

IEEE Magnetics Group

- S. Rubin, Chairman, Galvanomagnetic Standards Subcommittee

IEEE Parts, Hybrids, and Packaging Group

- W. M. Bullis, New Technology Subcommittee, Technical Committee on Hybrid Microelectronics

Society of Automotive Engineers

- J. C. French, Subcommittee A-2N on Radiation Hardness and Nuclear Survivability
- W. M. Bullis, Planning Subcommittee of Committee H on Electronic Materials and Processes

IEC TC47, Semiconductor Devices and Integrated Circuits:

- S. Rubin, Technical Expert, Galvanomagnetic Devices; U.S. Specialist for Working Group 5 on Hall Devices and Magnetoresistive Devices

APPENDIX C
SOLID-STATE TECHNOLOGY & FABRICATION SERVICES

Technical services in areas of competence are provided to other NBS activities and other government agencies as they are requested. Usually these are short-term, specialized services that cannot be obtained through normal commercial channels. Such services provided during the last quarter are listed below and indicate the kinds of technology available to the program.

1. Channel Electron Multipliers (Y. M. Liu)*

   Evaluation of channel electron multipliers for the NASA Goddard Space Flight Center continued. Gain and resolution as a function of voltage and count rate were measured. Neutron radiation damage effects on charge sensitive preamplifiers were also studied.

2. Electrical Burnout Studies (W. K. Croll and H. A. Schafft)†

   Microscopic and in some cases scanning electron microscope examinations were conducted on 45 quadruple, two-input, positive NAND gates for the Harry Diamond Laboratories to assist in establishing degradation and failure modes.

3. Thin Metal Films (J. Krawczyk)

   Thin films of gold, nickel, or chromium were vacuum evaporated onto various polymeric films for fabrication into piezoelectric and pyroelectric detectors by the NBS Instrumentation Applications Section.

4. Ultrasonic Machining (J. Krawczyk)

   Precision ultrasonic machining of glass discs and washers was performed for the NBS Dimensional Technology Section.

5. Crystal Preparation (M. Cosman)

   A 1-in. square silicon target, 0.002-in. thick, was fabricated for the NBS Photonuclear Physics Section.

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* NBS Cost Center 4254429

† NBS Cost Center 4251541

APPENDIX D
JOINT PROGRAM PUBLICATIONS

Prior Reports:

A review of the early work leading to this Program is given in Bullis, W. M., Measurement Methods for the Semiconductor Device Industry — A Review of NBS Activity, NBS Tech. Note 511, December, 1969.

Quarterly reports covering the period since July 1, 1968, have been issued under the title Methods of Measurement for Semiconductor Materials, Process Control, and Devices. These reports may be obtained from the Superintendent of Documents (Catalog Number C.13.46:XXX) where XXX is the appropriate technical note number. Microfiche copies are available from the National Technical Information Service (NTIS), Springfield, Virginia 22151.

Quarter Ending	NBS Tech. Note	Date Issued	NTIS Accession No.
September 30, 1968	472	December, 1968	AD 681330
December 31, 1968	475	February, 1969	AD 683808
March 31, 1969	488	July, 1969	AD 692232
June 30, 1969	495	September, 1969	AD 695820
September 30, 1969	520	March, 1970	AD 702883
December 31, 1969	527	May, 1970	AD 710906
March 31, 1970	555	September, 1970	AD 718534
June 30, 1970	560	November, 1970	AD 719976
September 30, 1970	571	April, 1971	AD 723671
December 31, 1970	592	August, 1971	AD 728611
March 31, 1971	598	October, 1971	AD 732553
June 30, 1971	702	November, 1971	AD 734427
September 30, 1971	717	April, 1972	AD 740674
December 31, 1971	727	June, 1972	AD 744946
March 31, 1972	733	September, 1972	

Current Publications:

As various phases of the work are completed, publications are prepared to summarize the results or to describe the work in greater detail. Copies of most of such publications are available and can be obtained on request to the editor or the author.

Harman, G. G., and Leedy, K. O., An Experimental Model of the Microelectronic Ultrasonic Wire Bonding Mechanism, *10th Annual Proceedings, Reliability Physics 1972,* Las Vegas, Nevada, April 5, 1972, pp. 49-56.

Oettinger, F. F., and Rubin, S., The Use of Current Gain as an Indicator for the Formation of Hot Spots Due to Current Crowding in Power Transistors, *10th Annual Proceedings, Reliability Physics 1972,* Las Vegas, Nevada, April 5, 1972, pp. 12-18.

Sher, A. H., Liu, Y. M., and Keery, W. K., Infrared Response Measurements on Radiation-Damaged Si(Li) Detectors, *IEEE Trans. Nucl. Sci.* NS-19, No. 3, 312-217 (June, 1972).

Liu, Y. M., and Coleman, J. A., Radiation Damage Effects by Electrons, Protons and Neutrons in Si(Li) Detectors, *IEEE Trans. Nucl. Sci.* NS-19, No. 3, 346-352 (June, 1972).

Marsden, C. P., Tabulation of Published Data on Electron Devices of the U.S.S.R. Through December 1971, NBS Technical Note 715 (June, 1972). (Supersedes NBS Technical Note 526).

Sawyer, D. E., Prevalent Error Sources in Transistor Delay-Time Measurements, presented at 1972 IEEE Annual Conference on Nuclear and Space Radiation Effects, Seattle, Washington, July 24-27, 1972.

Schafft, H. A., Testing and Fabrication of Wire-Bond Electrical Connections — A Comprensive Survey, NBS Technical Note 726 (September, 1972).

Mattis, R. L., and Baroody, A. J., Jr., Carrier Lifetime Measurement by the Photoconductive Decay Method, NBS Tech. Note 736 (September, 1972).

Phillips, W. E., Interpretation of Steady-State Surface Photovoltage Measurements in Epitaxial Semiconductor Layers, *Solid-State Electronics* 15, 1097-1102 (October, 1972).

Blackburn, D. L., Schafft, H. A., and Swartzendruber, L. J., Nondestructive Photovoltaic Technique for the Measurement of Resistivity Gradients in Circular Semiconductor Wafers, to be published in *J. Electrochem. Soc.*

APPENDIX E
STANDARDIZATION AND DISSEMINATION ACTIVITIES

(A summary for fiscal year 1972)

STANDARDS COMMITTEE ACTIVITIES:

- Editorial Review (ASTM, F-1): 16 documents
- Substantive Technical Comments: 11 documents
- Technical Revisions or New Drafts Prepared: 12
- Round-Robin Experiments: 7
- Committee Participation:

  ASTM (F-1, E-10)
  EIA-JEDEC (JC-11, 20, 21, 22, 24, 25, 30)
  IEEE (G-ED, MAG, PHP)
  SAE (H, A-2N)
  IEC (TC 47)

  Staff Members Active: 18
  Offices Held by Staff Members: 16
  Task Force, Section, Subcommittee, or Committee Meetings Attended: >80

FIELD VISITS: 52 to industrial, academic, and government installations

PUBLICATIONS AND TALKS: 23 in addition to quarterly progress reports which now go by request directly to more than 1200 individuals

VISITS TO NBS: 77 for specific information exchange
21 formal and reports to sponsors
5 tour groups (>125 individuals)

CONSULTATIONS: >400

BENEFITS:

- Guidance to Program
- Rapid Utilization of Results by Industry

FORM NBS-114A (1-71)

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	NBS-TN-743		

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Methods of Measurement for Semiconductor Materials, Process Control, and Devices. Quarterly Report, April 1 to June 30, 1972.

5. Publication Date December 1972

6. Performing Organization Code

7. AUTHOR(S) W. Murray Bullis, Editor

8. Performing Organization

9. PERFORMING ORGANIZATION NAME AND ADDRESS

NATIONAL BUREAU OF STANDARDS
DEPARTMENT OF COMMERCE
WASHINGTON, D.C. 20234

10. Project/Task/Work Unit No. See Item 15

11. Contract/Grant No. See Item 12

12. Sponsoring Organization Name and Address NBS, DNA (EA072-810), Navy Strategic Systems Project Office, NAD, Crane, Indiana (PO-2-0023 and PO-2-0054), NAVELEX (PO-2-1034), AFWL (F29601-71-F-0002), AFCRL (Y72-873), ARPA (MIPR FY76167100331), AEC, NASA (S-70003-G).

13. Type of Report & Period Covered Interim April 1 to June 30, 1972.

14. Sponsoring Agency Code

15. SUPPLEMENTARY NOTES
4251126, 4251127, 4252128, 4254115, 4259522, 4259533, 4252534, 4252535, 4251536, 4254422, 4254425, 4254429.

16. ABSTRACT (A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.)

This quarterly progress report, sixteenth of a series, describes NBS activities directed toward the development of methods of measurement for semiconductor materials, process control, and devices. Significant accomplishments during this reporting period include verification of the applicability of resolution of forces in interpreting pull test measurements on unannealed wire bonds on single-level substrates, completion of the feasibility study of ribbon-wire bonding with the important finding that ribbon-wire bonds can be made with a wider range of bonding parameters than round-wire bonds of the same strength, and development of test procedures in preparation for studies of high-frequency measurements of transistors on the wafer by means of probes. Work is continuing on measurement of resistivity of semiconductor crystals; study of gold-doped silicon; development of the infrared response technique; evaluation of wire bonds and die attachment; and measurement of thermal properties of semiconductor devices, delay time and related carrier transport properties in junction devices, and noise properties of microwave diodes. New work has been started on development of procedures for analysis of the characteristics of generation-recombination-trapping centers in silicon. Supplementary data concerning staff, standards committee activities, technical services, and publications are included as appendixes.

17. KEY WORDS (Alphabetical order, separated by semicolons)
Aluminum wire; base transit time; carrier lifetime; die attachment; electrical properties; epitaxial silicon; gamma-ray detectors; generation centers; germanium; gold-doped silicon; infrared response; methods of measurement; microelectronics; microwave diodes; nuclear radiation detectors; probe techniques (a-c); recombination centers; resistivity; ribbon-wire bonding; semiconductor devices; semiconductor materials; semiconductor process control; silicon; thermal resistance; trapping centers; ultrasonic bonding; wire bonds.

18. AVAILABILITY STATEMENT	19. SECURITY CLASS (THIS REPORT)	21. NO. OF PAGES
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