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U.S. DEPARTMENT OF COMMERCE / National Bureau of Standards

A Satellite-Controlled Digital Clock

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A Satellite-Controlled Digital Clock

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CONTENTS

FIGURES

A SATELLITE-CONTROLLED DIGITAL CLOCK

J. V. Cateora, D. D. Davis, and D. W. Hanson

A digital clock, resettable and controlled by the time code relayed by NOAA's SMS/GOES satellites, is discussed. The clock's design is based upon a four-bit microprocessor and uses the redundancy of the data to improve its performance. Satellite position is included in the clock's display for delay corrections to the received time.

A discussion of the generation, distribution, and reception of the time code is also included to aid the explanation of the clock's operation and performance.

Key Words: Clock; microprocessor; satellite; time; time code.

1. INTRODUCTION

This report describes a digital clock developed by the National Bureau of Standards (NBS) which is controlled by a time code transmitted from the National Oceanic and Atmospheric Administration's (NOAA's) meteorological satellites. The first two satellites launched in this series are known as the Synchronous Meteorological Satellites (SMS) with all others following designated as Geostationary Operational Environmental Satellites (GOES). Long-range plans for these NOAA Satellites call for the positioning of one satellite at approximately 135 degrees West Longitude, another at 75 degrees West Longitude, and a third to be an in-orbit spare. The approximate coverage of these satellites is shown in figure 1. As these satellites deteriorate with age, replacement satellites will be launched. This planned configuration of satellites is expected to be in effect by early 1976. During most of 1975, one satellite was operated from 115 degrees West Longitude, an intermediate point between the two planned locations mentioned.

The time code is used by NOAA in a data collection program where the SMS/GOES satellites relay data from remote observing platforms such as buoys, automatic weather stations, ships, aircraft, and balloons to a processing facility. Many of these platforms will use the time code to date the data as they are collected or to time order their data transmissions to the satellites. NBS designed and implemented the time code for these satellites. To insure compatibility of the time code with the data collection platforms (DCP), NBS designed a digital clock using a simple low-cost microprocessor. The microprocessor approach to the digital clock design was taken because it offered the lowest cost and provided the flexibility to include or delete functions through software changes rather than hardware redesign.

The microprocessor-based digital clock described in this report has a number of interesting and innovating features. It uses a priori information to improve the effective bit error rate experienced in the satellite link. It also provides the information needed to compute the propagation path delay corrections to the received signals. The total system performance has indicated a 20 μs precision with accuracies better than 100 μs. The digital clock, once set by the satellite time code, continues to keep time with or without reference to the satellite signal.

The parts cost for the digital clock without the power supply is less than $200 at the time of this writing. Power input is approximately 7 watts or 160 mA at -10 volts dc and 1 ampere at 5 volts dc.

2. SYSTEM DESCRIPTION

This section describes the time code system including its generation, distribution, format, and reception. The reception of the time code is described assuming the use of a receiver which was developed under a NOAA contract. This receiver is part of the Data Collection Platform Radio Set (DCPRS) designed for

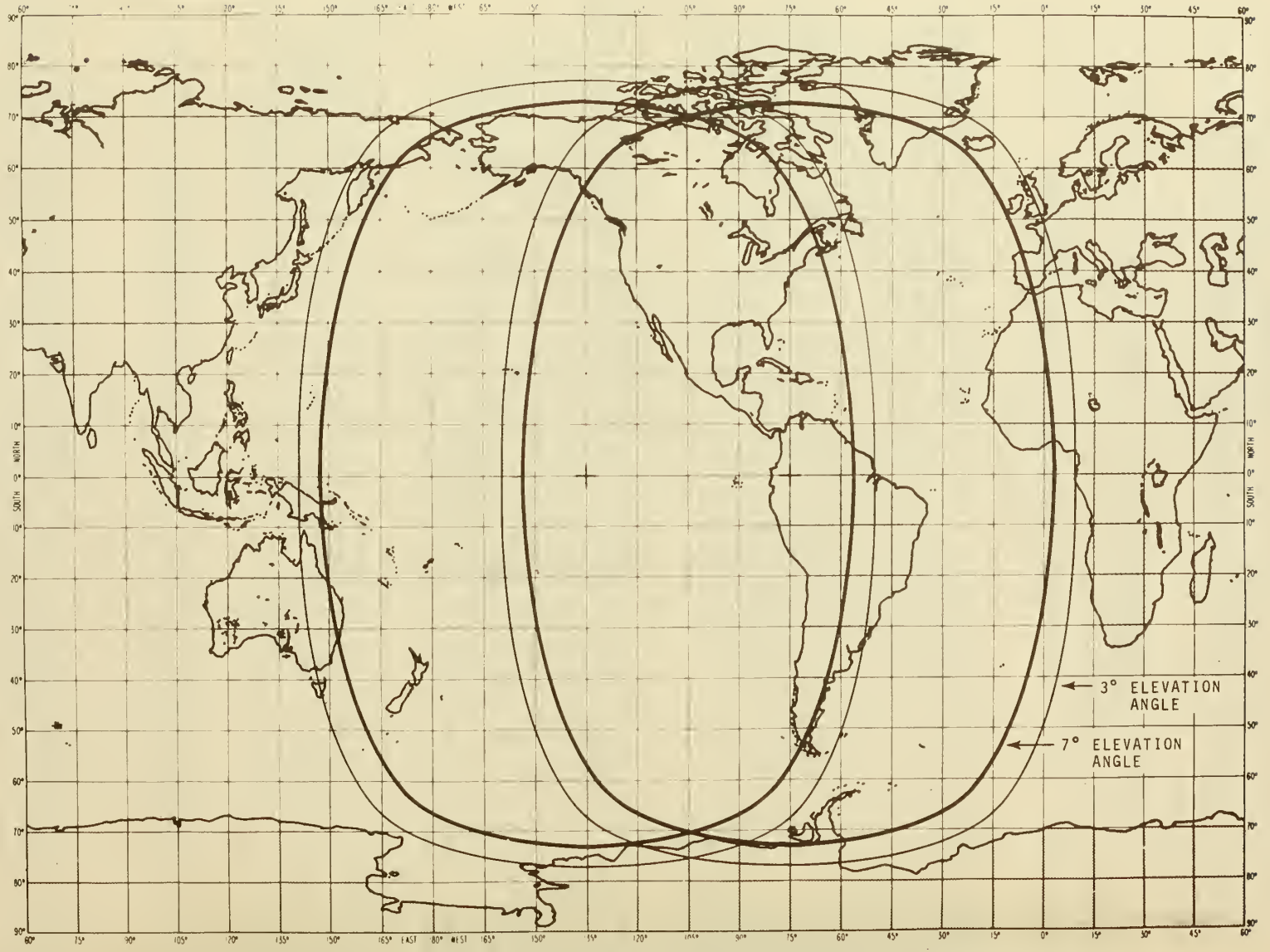

FIGURE 1. SMS/GOES COVERAGE

unattended operation over long periods of time, severe environments, and low power consumption. Obvious improvements can be achieved if the receiver is designed as a timing receiver and the above mentioned requirements relaxed. Because no other receiver existed at this time, all references to reception assume the use of this receiver.

2.1 FORMAT

The time information, a digital time code, is multiplexed into an interrogation message format relayed by the SMS/GOES satellites. The interrogation message is used to activate a transfer of a DCP's collected data to NOAA's Wallops Island, Virginia, facilities via the SMS/GOES satellites. The format consists of a 15-bit maximum-length sequence (MLS) for message synchronization immediately followed by 31 bits comprising a (31, 21) binary Bose-Chaudhuri-Hocquenghem (BCH) code. Four additional bits preceed each MLS sequence beginning on the 0.5 second and comprise a binary coded decimal (BCD) character of the time code.

Figure 2a shows the interrogation message format: Four time code bits followed by 15 bits of the message synchronization word and 31 bits of the address word. The pattern is repeated every 0.5 second, at a 100 bits per second rate. The leading edge of the first bit to every time code character defines the UTC 1/2 second mark. Figure 2b is the time code format; four bits are extracted from the interrogation frame every half second for 30 seconds. The first 40 bits is the time code synchronization message consisting of 10 BCD character A's beginning on the UTC minute mark and 10 BCD 5's beginning at the UTC half minute mark.

Following the code synchronization message are 10 BCD characters of the time code followed by 13 BCD characters representing the satellite's current position in geocentric longitude and latitude and its radial departure from a reference orbit expressed in microseconds.

2.2 TIME CODE DISTRIBUTION

The interrogation message is sent to the SMS/GOES spacecraft at S-Band from Wallops Island, Virginia, and is retransmitted to the earth through a global antenna at approximately 469 MHz. The Manchester coded message phase-modulates the carrier ±60 degrees. The interrogation message is received mainly by data collection platform radio sets (DCPRS) which provide the communication interface with rain and river gauges, ships, buoys, seismograph stations, tide gauges, and tsunami detectors. The DCPRS recovers the data and a data clock from the received interrogation message, the data clock being used for symbol synchronization.

When a DCPRS is addressed, its stored data are transmitted to the SMS for relay to the Wallops Island Command and Data Acquisition Station (CDA). In some cases, such as the monitoring of seismic activities, it is desirable to label the data with the date of occurrence. Attempts to use internal clocks set by infrequent clock carries or by reception of HF or LF radio signals are expensive, labor intensive, and subject to an unacceptable failure rate. The time-of-year code in the interrogation format eliminates these problems and provides the SMS/GOES DCS user with a cheap, reliable, and simple system for data labeling or any other time ordered function required at remote sites or in difficult environments.

Figure 3 illustrates the time code distribution. Derived from atomic clocks located at the CDA in Wallops Island, Virginia, the time code is combined with the current satellite position, multiplexed with the interrogation address and sync word and transmitted to the satellites at S-Band. The satellites transpond the signal back to earth at approximately 469 MHz where it is received by the DCPRS's.

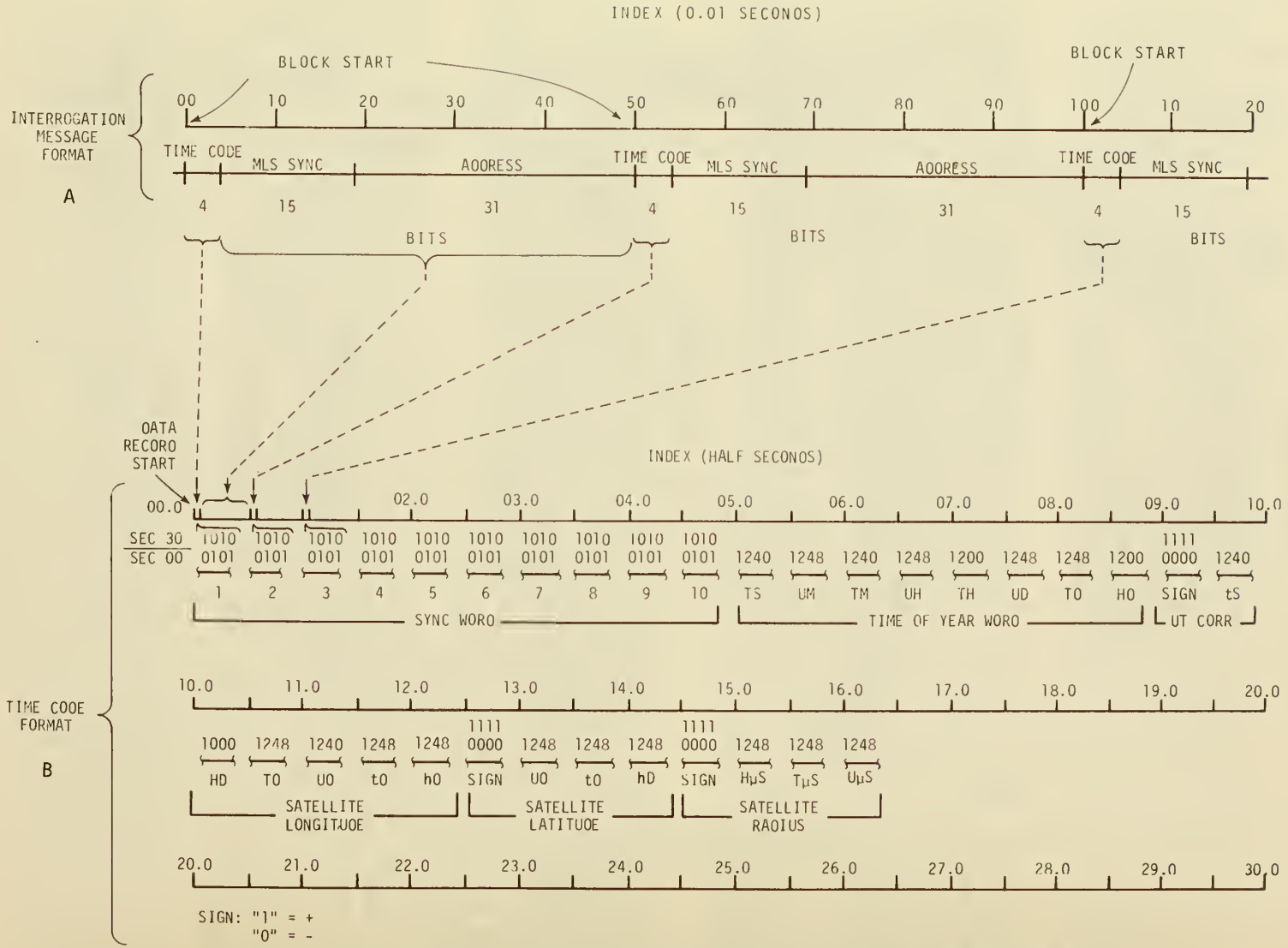

FIGURE 2. INTERROGATION MESSAGE AND TIME CODE FORMATS

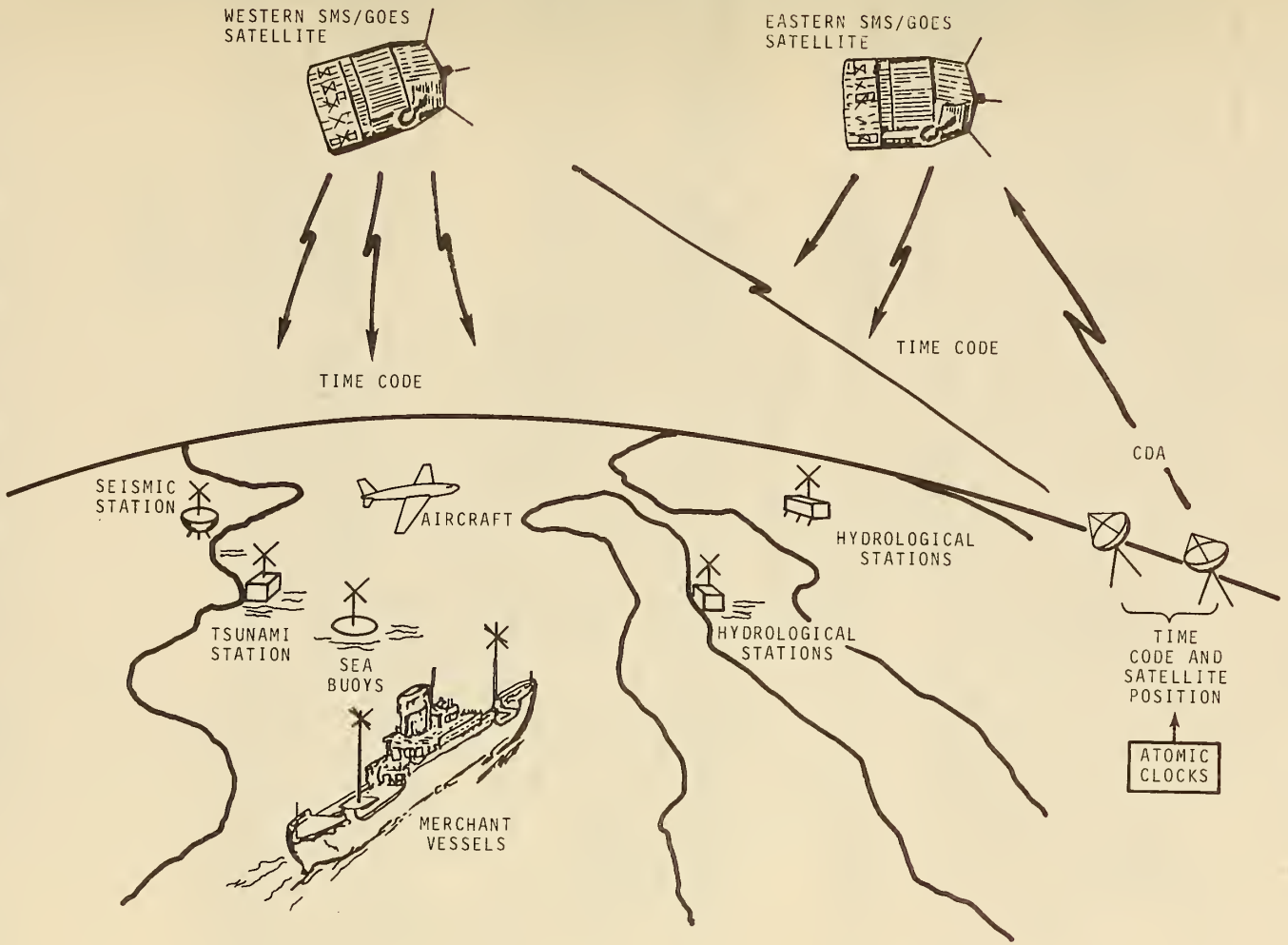

FIGURE 3. TIME CODE DISTRIBUTION

2.3 TIME CODE GENERATION

NBS has installed at the CDA at Wallops Island, Virginia, equipment to generate the time code and maintain Coordinated Universal Time (UTC) to within a few microseconds of the master clock at NBS in Boulder, Colorado. Figure 4 is a block diagram of the equipment. There are two atomic frequency standards each driving a clock and format generator making two independent systems. Each system provides the time code and satellite position to DCS racks A and B for multiplexing into the interrogation channels of the two SMS/GOES satellites. All components of each system are backed with rechargeable batteries with sufficient capacity to operate four hours without primary power. Should a failure be experienced in one of the time reference systems the other can be switched in until it is repaired. The frequency of the atomic frequency standards can be compared to the NBS frequency standard in Boulder, Colorado, using a frequency meter operating on television signals. This comparison is accomplished by NBS staff at routine intervals. Satellite position is computed at NBS Boulder from orbital elements issued by NASA's Goddard Space Flight Center and sent to Wallops Island by telephone. An automatic answering system connects the telephone line to a memory bank which stores the positions in the form of a large table valid for 128 hours for the two satellites. The time code format generator addresses the memory with the date (days, hours, and minutes) and fetches the currently valid position for multiplexing into the interrogation message.

The interrogation channels on both satellites are monitored continuously in Boulder. Any failure or drift of the clocks at Wallops Island is automatically noted for appropriate action.

2.4 TIME CODE RECEPTION

The interrogation channel is received by the DCPRS which usually consists of a receiver and transmitter. A block diagram of the receiver is shown in figure 5. The transmitter section of the DCPRS has been left out since it has no bearing on this discussion. The demodulator consists of a phase lock loop with a 10 Hz loop bandwidth and a timing recovery loop to derive the data clock[1] for symbol synchronization. The demodulator provides outputs of data and data clock, the two inputs to the digital clock. The signals from the satellite occupy a bandwidth of 400 Hz, and have a signal level of approximately -139 dBm at the output of an isotropic antenna. A DCPRS receiver and digital clock has been successfully and reliably operated using both linearly and circularly polarized antennas with gains as low as 3 dB.

The signal delay from Wallops Island to the earth's surface via the SMS/GOES satellites is nominally 260,000 μs. This delay is a function of distance from the subsatellite point as shown in figure 6. As a first order correction for delay, the time signals are advanced by 260,000 μs at Wallops Island thereby forcing them to be nearly on time when arriving at the earth's surface. Since the satellite is not in a perfect geostationary orbit, that is, it has some inclination and eccentricity, the delay experienced at any one point has a diurnal component. The magnitude of the diurnal is also position dependent. Typical peak-to-peak values of the diurnals for the Eastern and Western satellites are shown in figures 7a and 7b.

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[1]The data clock is a sequence of alternating ones and zeros used for symbol synchronization. The RAM clock measures the accumulation of time. The microprocessor clock is the oscillator governing the function of the microprocessor. The digital clock refers to the system (microprocessor, software, I/O, and display) used to maintain time referenced to the time code from the satellite.

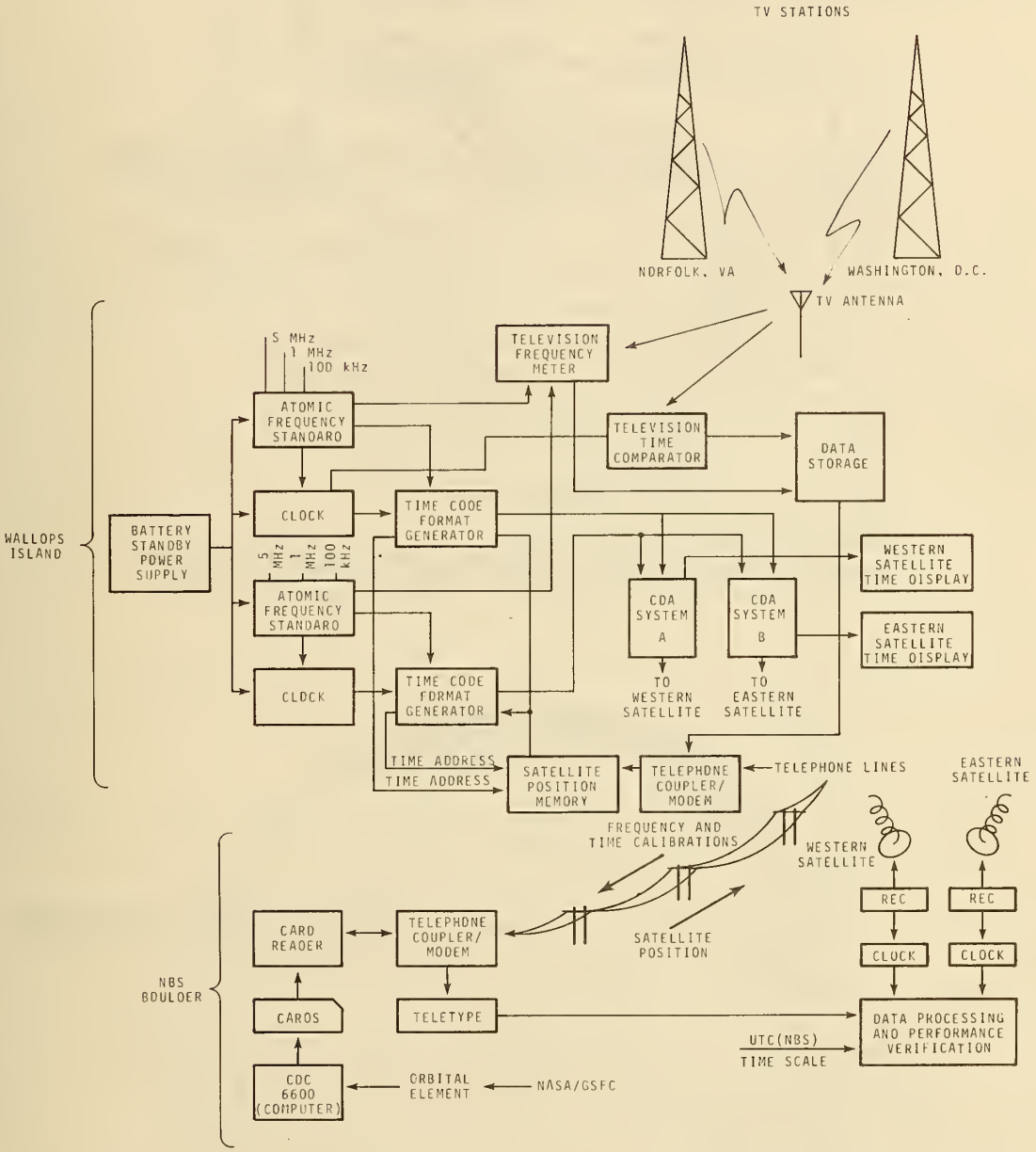

FIGURE 4. TIME CODE GENERATION AND CONTROL EQUIPMENT

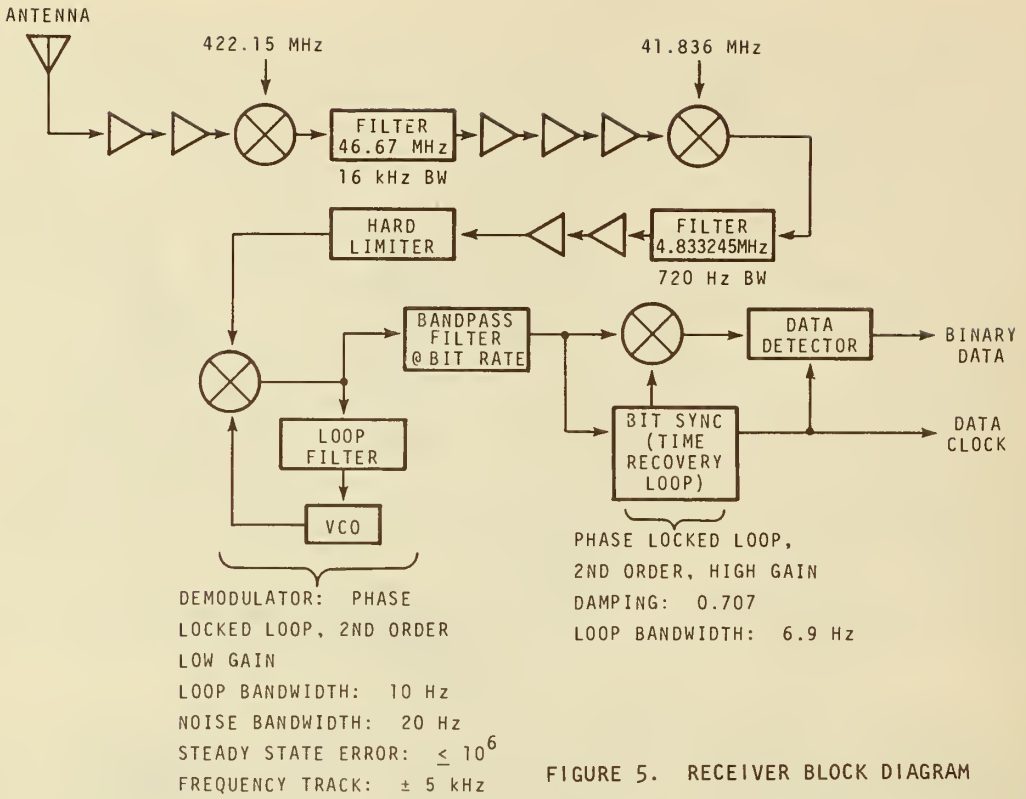

FIGURE 5. RECEIVER BLOCK DIAGRAM

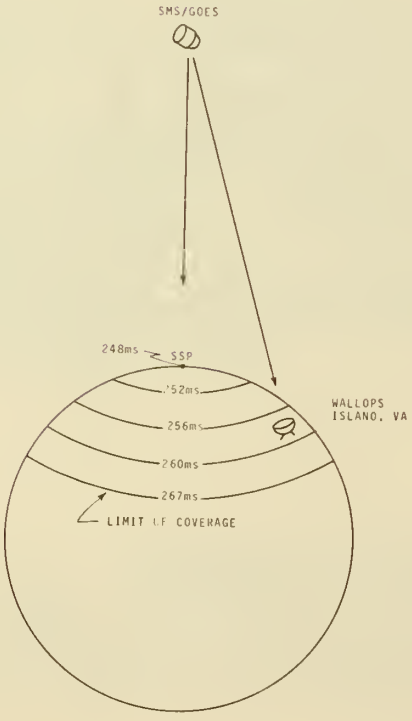

FIGURE 6. TIME DELAY THROUGH A GEOSTATIONARY SATELLITE AT 115° WEST LONGITUDE

FIGURE 7a. TYPICAL DELAY DIURNALS FOR THE EASTERN SATELLITE WITH WALLOPS ISLAND TRANSMITTING

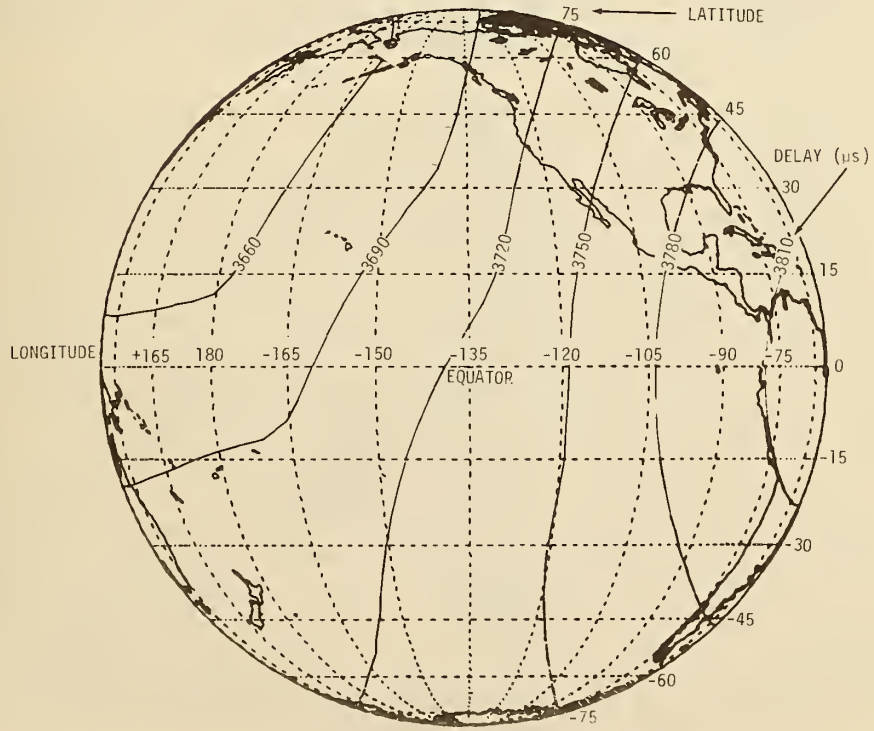

FIGURE 7b. TYPICAL DELAY DIURNALS FOR THE WESTERN SATELLITE WITH WALLOPS ISLAND TRANSMITTING

3. DIGITAL CLOCK DESCRIPTION

The digital clock was built to interface with NOAA's DCPRS's as they existed in early 1974. A microprocessor design was chosen because of its potential low cost and simplicity. The microprocessor design replaced a previous random logic design amounting to 80 integrated circuit packages. Special features and properties of time messages were used in the microprocessor design. For example, each successive time-code frame differs only by 30 seconds, the length of the frame. Thus the messages have a large degree of redundancy. This fact was used to, in effect, increase the signal-to-noise ratio or lower the bit error rate. The a priori information was used as follows: The microprocessor stores the time-of-year in random access memory (RAM) and continually updates itself by counting the 100 Hz data clock. During every time-code frame received from the satellite the microprocessor compares its RAM time with the new time message. If there is agreement, everything is assumed to be in order. If there is disagreement, the microprocessor will continue to assume that the RAM clock has the correct time, but after four consecutive time frame disagreements the RAM clock is assumed to be in error. The microprocessor will then reset its RAM clock to the next time code message providing the satellite time is being received as evidenced by the presence of the MLS and time code synchronization word. This procedure is referred to as an error bypass capability.

The 100 Hz data clock from the receiver is also subject to noise introducing additional zero crossings that can be interpreted by the microprocessor as 0.01 second increments in time. To minimize the effect of this noise and provide a reliable and continuous 100 Hz to count even without the satellite signal, the microprocessor system crystal oscillator is divided down to 100 Hz and phase locked to the received data clock. The phase locked 100 Hz is then used as the time base for the microprocessor time-of-year (TOY) clock.

The two above mentioned procedures have used the cyclic nature of the data and data clock to improve the performance of the digital clock.

The satellite ephemeris is displayed as received. Consequently, it is susceptible to more error than the TOY. One can only look for consistency in the display from frame to frame. The display is updated at the 00 and 30 seconds. Two successive frames of the same data insure the correct satellite position data is being displayed.

To fully understand the details of the operation of the digital clock, it is well to review the basic tasks it accomplishes. A thorough familiarity with the format of the interrogation channel is important to this understanding. Repeated reference to the software flow chart, figures 8a and 8b would also be helpful. We begin the explanation by assuming that the digital clock has just been connected to the receiver and is receiving the interrogation channel properly. The digital clock has available to it the data and the data clock. It must look at the data clock for a negative going transition to identify when to sense the data and acquire one bit of information. In other words, it acquires symbol synchronization by looking at the data clock. When the proper data clock transition is recognized, it samples the data and stores the sampled bit in memory, an index register of the CPU. In fact, the last 15 bits of data have been stored in index registers. After each bit is received and stored, the last 15 bits stored are examined for the MLS (100010011010111). If the latest stored 15 bits match the sequence stored in program memory, MLS synchronization is declared. The microprocessor now knows the location of the four bits in every interrogation frame constituting a time code BCD character. The microprocessor then loads these four bits every half second into an index register and examines it to determine if it is part of the time code synchronization word, a BCD A or 5 depending on whether the frame is in the first or second half of the minute. When 10 consecutive A's or 5's are found, time code synchronization is declared. The next four bits to be loaded are the tens of seconds (TS) of the time code, then unit minutes (UM), tens of minutes (TM), etc., for the next 11 1/2 seconds or 21 four bit characters finishing with the units of microseconds of the satellite distance. These data are all written into RAM memory.

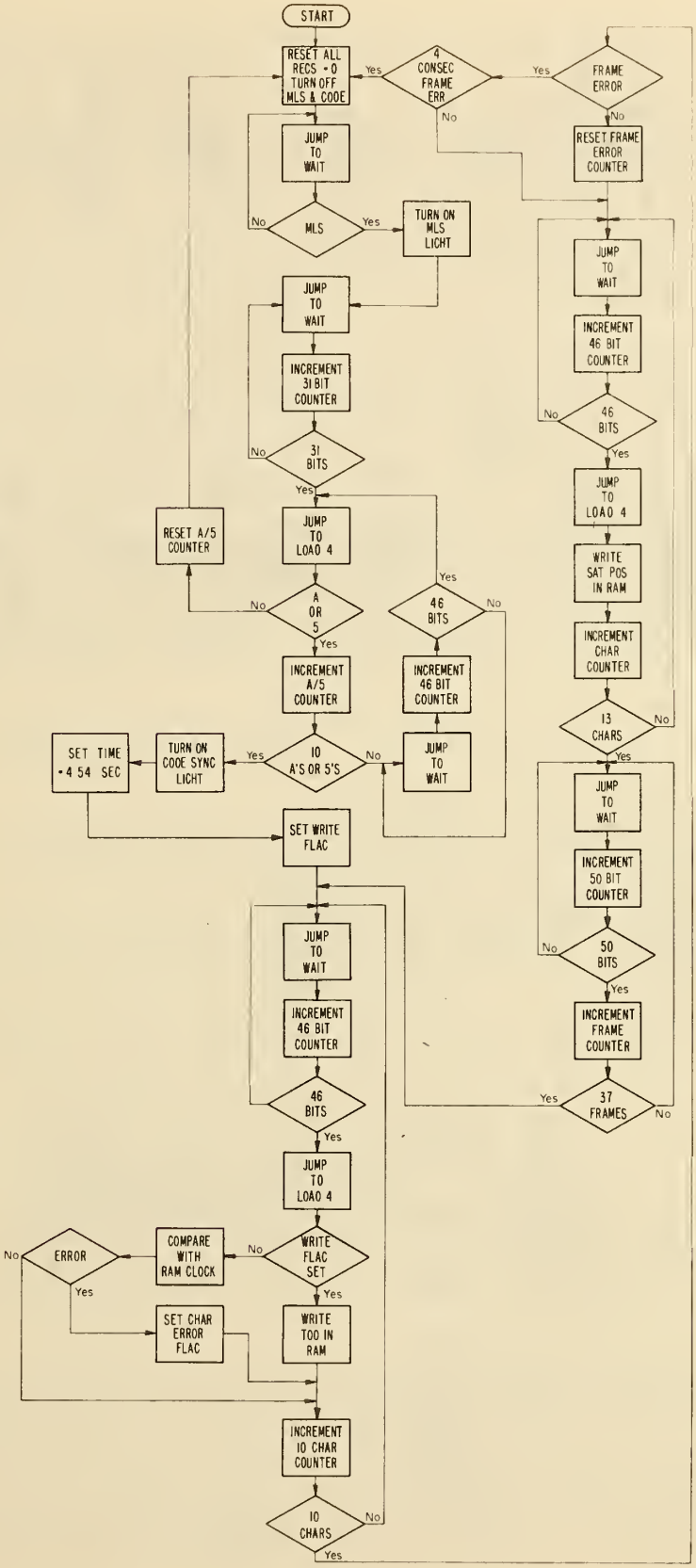

FIGURE 8a. SOFTWARE FLOW CHART

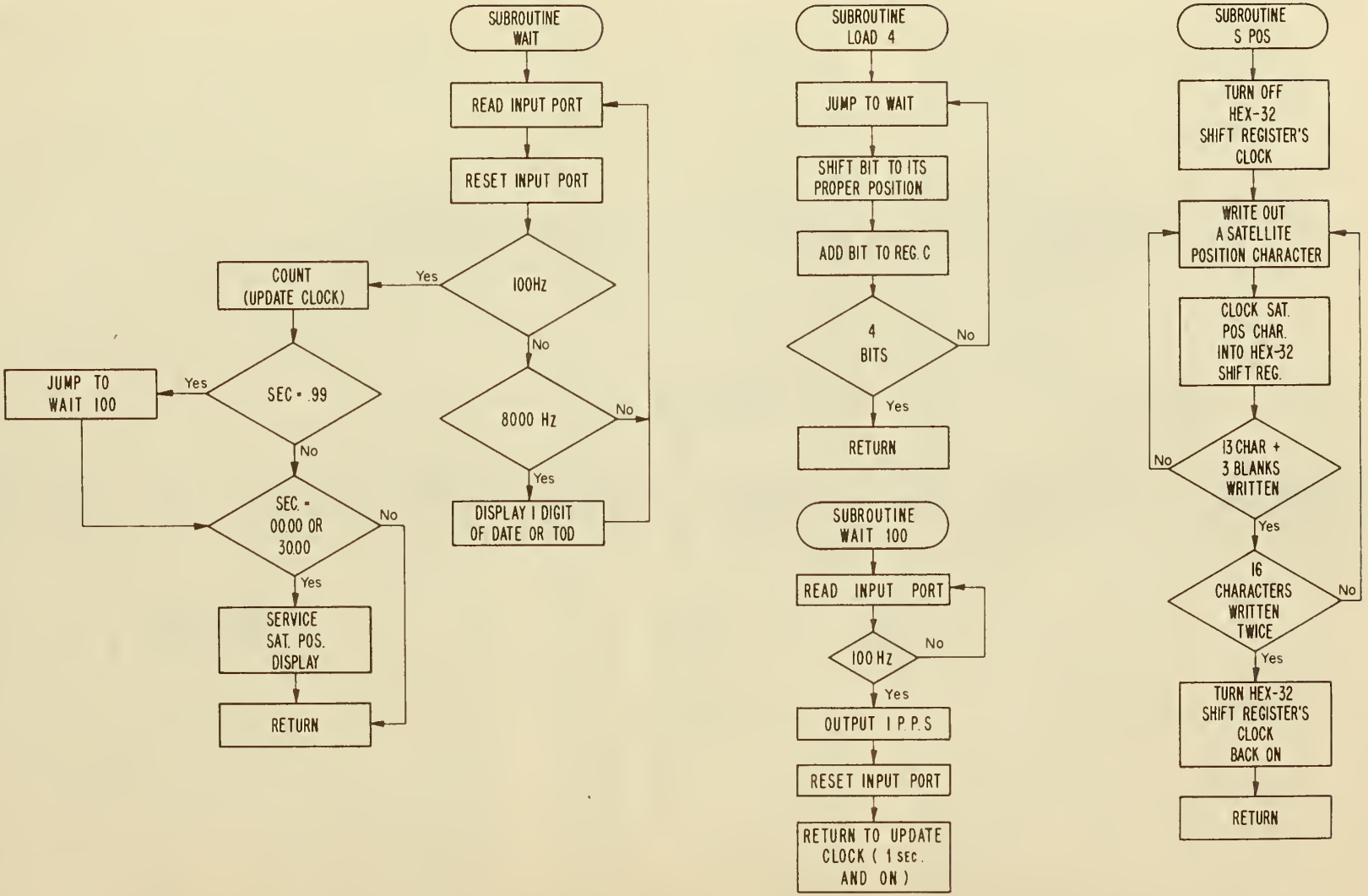

FIGURE 8b. SOFTWARE FLOW CHART (CONTINUED)

The microprocessor now counts bits and frames until it arrives at the TS character of the next frame. It does not search for MLS or code sync again since total synchronization may be maintained by simply counting the 100 Hz time base over to the beginning of the next time code frame. On the second pass of a time code frame the microprocessor only compares the newly arrived character of the TOY with the corresponding internal RAM character. Should this comparison fail anywhere in the TOY frame it will be counted as a frame error. If four consecutive frame errors occur, the microprocessor will begin a new search for MLS and time code sync. When successfully achieved the satellite TOY will be written into the RAM clock, resetting the RAM clock. If the microprocessor does not find MLS and time code synchronization it will not disturb the RAM clock. This prevents the RAM clock from being reset when no satellite signal is present.

The RAM clock consists of characters representing days, hours, minutes, seconds, tenths of seconds, and hundredths of seconds. The data clock is derived at Wallops Island from an atomic clock. Each cycle of the data clock represents 1/100 of an atomic second and is counted by the microprocessor to update its RAM clock. The microprocessor has its system oscillator phase locked to the incoming data clock. If the data clock is lost, the internal oscillator will continue to provide the 0.01 s count to keep the RAM clock accurate.

The RAM clock, excluding the 0.1 s and 0.01 s digits, is multiplexed for display by LED's under microprocessor control. The satellite position is loaded into RAM memory every frame as received. At the 00 and 30 second RAM storage of position is transferred to an external shift register and multiplexed to LED's under independent control. Consequently, if the satellite signal is lost, the satellite position will also disappear from the display.

The program for controlling the microprocessor occupies two 8 bit x 256 programmable Read Only Memories (pROMs), that is, 512 eight-bit bytes. The actual program requires about 460 bytes.

The program consists of a main program called START of about 210 bytes, subroutine WAIT of about 175 bytes, subroutine SPOS of about 25 bytes, subroutine LOAD4 of about 30 bytes and subroutine WAIT100 of about 20 bytes.

The main program START first establishes "MLS" sync by comparing the latest 15 bits received with the 15 bits of the known MLS pattern stored in pROM. This locates the correct starting point in the bit stream to start looking for BCD characters, that is, identifies the BCD characters of the time code.

Next, START looks for 10 "A" or 10 "5" characters in order to establish "CODE" or frame sync. Every 30 seconds the code contains either ten 1010_2 (BCD character "A") patterns starting at 00 s or ten 0101_2 (BCD "5") patterns starting at 30 s. Once "CODE" sync has been established the next BCD character received will be tens of seconds. Establishment of "MLS" and "CODE" sync is indicated by lights on the digital clock's display board.

When the digital clock is first turned on, and after both sync words are found, the received TOY and satellite position are written into RAM by START. In subsequent passes of the received code only position information is written into RAM unless discrepancies are found between the received TOY and the TOY stored in RAM.

Subroutine WAIT is called by START to find data bits as they appear at the input port. When one is found, WAIT increments the RAM clock by 0.01 s. WAIT also contains the coding for displaying the TOY. When an 8000 Hz transition is sensed at the input port, WAIT displays one digit of the TOY.

Subroutine SPOS is called by WAIT after the RAM clock has been updated and the time is 0.00 or 30.00 s. When called, SPOS loads the satellite position characters from RAM into the position display hardware which otherwise runs independently of the microprocessor.

LOAD4 is called by main program START to reconstruct a BCD character from four data bits. LOAD4 calls WAIT to locate the necessary four bits and stores the built-up BCD character in an index register reserved for this purpose.

WAIT100 is a subroutine of 18 bytes whose only purpose is to keep the clock's 1 pps as nearly on time as possible. It is called by WAIT when time is .99 s and waits only for the next .01 s pulse to occur, the instant when the 1 pps should be output, and ignores any 8000 Hz pulses for display. As soon as the .01 s pulse is sensed by WAIT100 it outputs the 1 pps. If a scheme such as WAIT100 were not used, the microprocessor could sense an 8000 Hz pulse and be occupied by performing its display function when the .01 s pulse, signaling a change in unit seconds, occurs and could not output the 1 pps until many program steps later. The use of WAIT100 keeps the 1 pps on time within about 30 μs. Without WAIT100 the 1 pps occurs randomly within 400 μs of being on time.

A complete listing of the program appears on pages 28 through 35. Figures 9a and 9b show the microprocessor's register maps. Figure 10 shows a logical block diagram of the program.

3.1 DIGITAL CLOCK CIRCUITRY

The 4004 Central Processing Unit (CPU), 4702A programmable Read Only Memory (pROM), 4002 Random Access Memory (RAM), 4008 Address Latch and 4009 Input/Output Multiplexers, 4201 Clock Generator, and TTL random logic packages form the microprocessor digital clock (see figure 10). The 4000 family of MOS microprocessor chips was chosen primarily because they are low cost four-bit devices and well suited for handling four-bit characters. The 4004 CPU was selected because of its low cost, easy availability and its proven history of use.

The microprocessor has one four-line input port, to which the received satellite signals are connected and eight four-line output ports which are assigned as follows:

Output Port	Function
0	Input port reset
1	Satellite position BCD character
2	Time-of-Year display strobe
3	Time-of-Year BCD character
4	"MLS" and "CODE" sync indicator lights
5	1 pulse per second voltage pulse
6	spare
7	spare

One RAM output Port is also used to disable the satellite position display clock while the satellite position display is being serviced.

The hardware is divided between two circuit boards. One board contains the microprocessor along with its input and output circuitry. The other board contains seven-segment Light Emitting Diodes (LED's) and associated TTL random logic to display the 22 time-of-year and satellite position characters. The 9 time-of-year LED's are multiplexed one digit at a time at approximately an 8000 Hz rate under microprocessor control. The 13 satellite position characters are stored in a hex-32 shift register and multiplexed by a free-running hardware clock at about a 60 kHz rate. The satellite position display is updated by the microprocessor every half minute at 00 and 30 seconds. This combination of display methods was chosen to avoid LED flicker associated with multiplexing 22 characters under the control of a processor with many other sequential tasks.

EVEN	B 4 2 1	REG. PAIR	8 4 2 1	ODD
E	31 and 46 Counter	P7	31 and 46 Counter	F
C	Reconstruct BCD Char	P6	10 A/S Counter, Write Flag, Frame Error Counter	D
A	RAM Chor Write Select, 37 Counter	P5	RAM Char Write Select, 37 Counter	B
B	Save Data In "2" Bit	P4	TOY Char. Error	9
6	TOY Output Port Select	P3	TOY Choracter	7
4	Multiplex Port Select	P2	Multiplex Counter	5
2	General Use	P1	General Use	3
0	General Use	P0	General Use	1

FIGURE 9a. RAM MAP

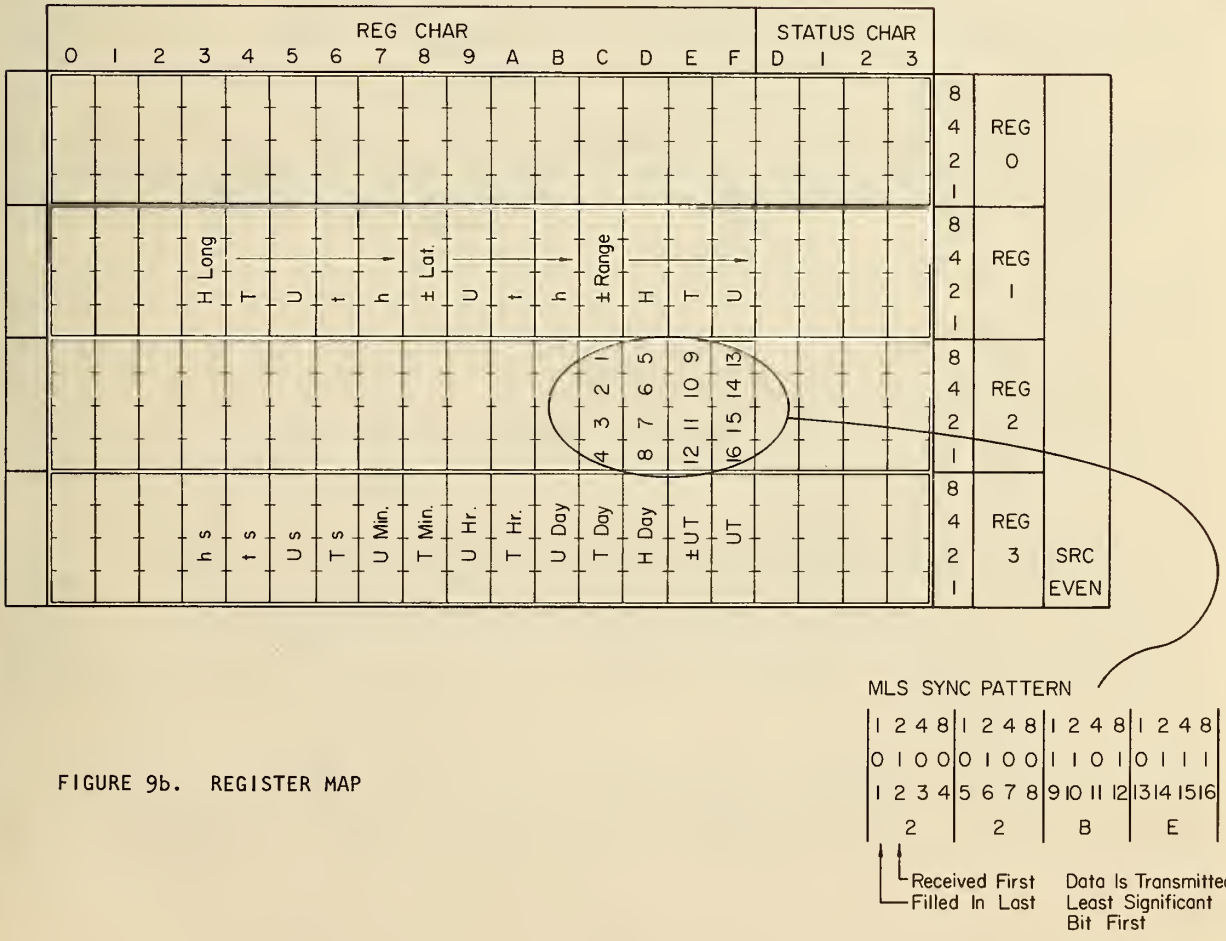

FIGURE 9b. REGISTER MAP

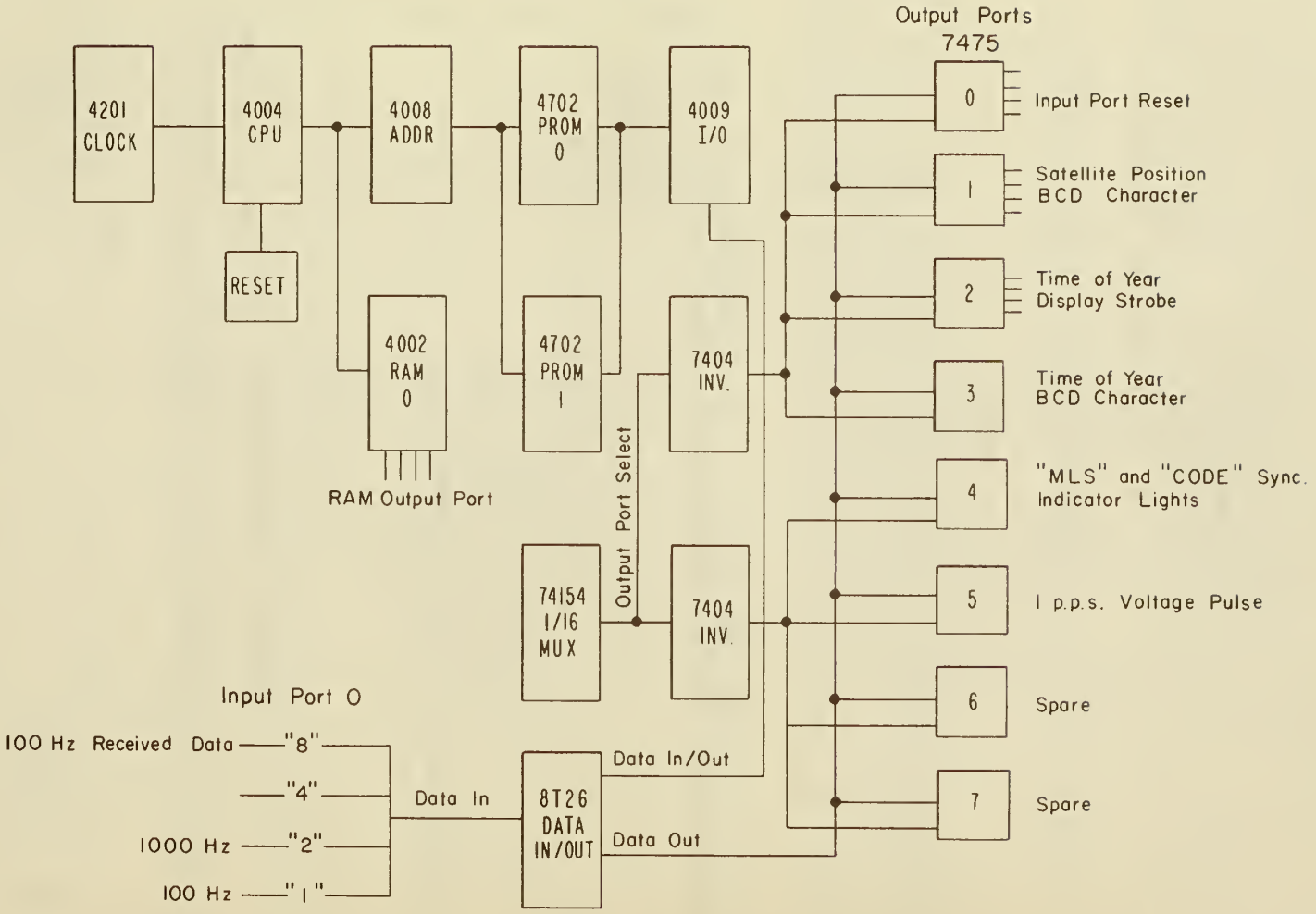

FIGURE 10. DIGITAL CLOCK BLOCK DIAGRAM

The Manchester encoded TOY and position data phase modulates the 469 MHz carrier ±60 degrees. Fron this are derived a 100 Hz data clock and serial binary data. The microprocessor's basic clock is 4.096 MHz which is frequency divided by 8x2x16x16x10 (=40960) to provide a frequency of 100 Hz. This 100 Hz signal is phase compared with the 100 Hz data clock and a voltage proportional to the phase difference is fed back to a pair of varactor diodes in parallel with the 4.096 MHz microprocessor clock crystal to phase lock the 4.096 MHz clock to the recovered data clock. Figure 11 is a block diagram of the phase lock loop and microprocessor input circuitry. The phase lock loop and input port arrangement is important because if the satellite signal is lost for any reason or for any length of time, the 100 and 8000 Hz signals will still be present as they are now being derived from the crystal controlled microprocessor system clock. Fven though the 100 Hz data clock is lost, the microprocessor will continue to update its RAM clock with the accuracy of the microprocessor's system clock. The satellite position information is not updated under these conditions and will be lost.

The microprocessor's one input port is connected as shown in figure 12. The 100 Hz satellite data clock is fed to the input port's "1" line through a 7474 latch. The "2" line is fed the 8000 Hz, through a latch also, derived from the frequency divider chain operating on the 4.096 MHz microprocessor clock. The input port "4" line is not used and the "8" line is connected to the received 100 Hz serial binary data.

The microprocessor, through software program control, samples the input port "1" line connected to the 100 Hz satellite data clock. If a 100 Hz transition is sensed the program updates an internal BCD clock stored in RAM by 0.01 s. The RAM clock is in the form of 11 4 bit BCD characters representing DDD, HH, MM, SS, ts, hs, that is, Day, Day, Day, Hour, Hour etc., down to .ls, .01 s. The .01 s update of the RAM clock and the appropriate carries ripple up to the tens of hours BCD character. The characters representing days are set by actually reading the received code into RAM.

The sensing of a 100 Hz transition at the input port "1" line also triggers the storage of data present at the "8" line as one bit of the four bits of a BCD charater. Four 100 Hz data clock transitions, sensed at the appropriate time, will therefore cause the RAM clock to be updated and one BCD character representing TOY or satellite position to be saved.

After looking for a 100 Hz transition, and whether or not one is found, the microprocessor next attempts to sense an 8000 Hz transition at the input port's "2" line. If an 8000 Hz transition is sensed, one digit of the date will be displayed on a 7-segment LED display character. If no 8000 Hz transition is sensed the microprocessor loops back and continues attempting to find either a 100 or an 8000 Hz transition. Basically then, the microprocessor spends its time looking for one of two conditions, a 100 or an 8000 Hz transition and then either updates its RAM clock or displays a character. Although the RAM clock contains BCD characters representing .01 and .1 s they are not displayed.

The microprocessor continuously compares the received TOY characters with the TOY characters stored in RAM. If four consecutive comparison frame errors occur the next received TOY character is rewritten into RAM and will be displayed. Four consecutive frame errors were chosen as the criterion for resetting the RAM clock to lessen the possibility of a noisy or marginal received signal causing an unintentional time reset. Experience with the digital clock under noisy signal conditions has shown this to be a good choice, but not necessarily the optimum strategy for all environments.

Display of TOY is accomplished by a 7-segment decoder on the display board which receives the BCD data and time-of-day characters from output port #3 and drives the display segments. The associated multiplex count from output port #2 is decoded by a 1 to 16 multiplexer with 2N3638 transistors driving the LED strobe inputs.

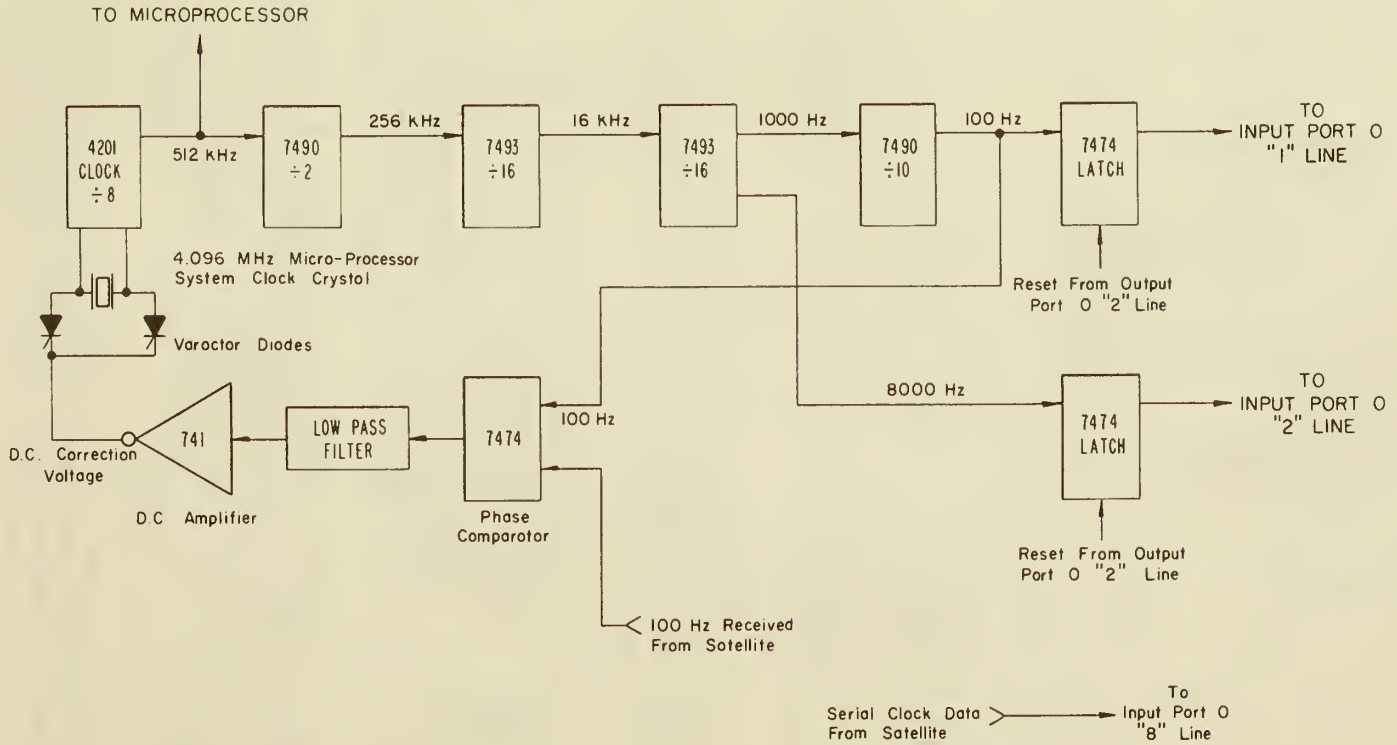

FIGURE 11. MICROPROCESSOR CLOCK PHASE LOCKED TO DATA CLOCK

76 x 6248

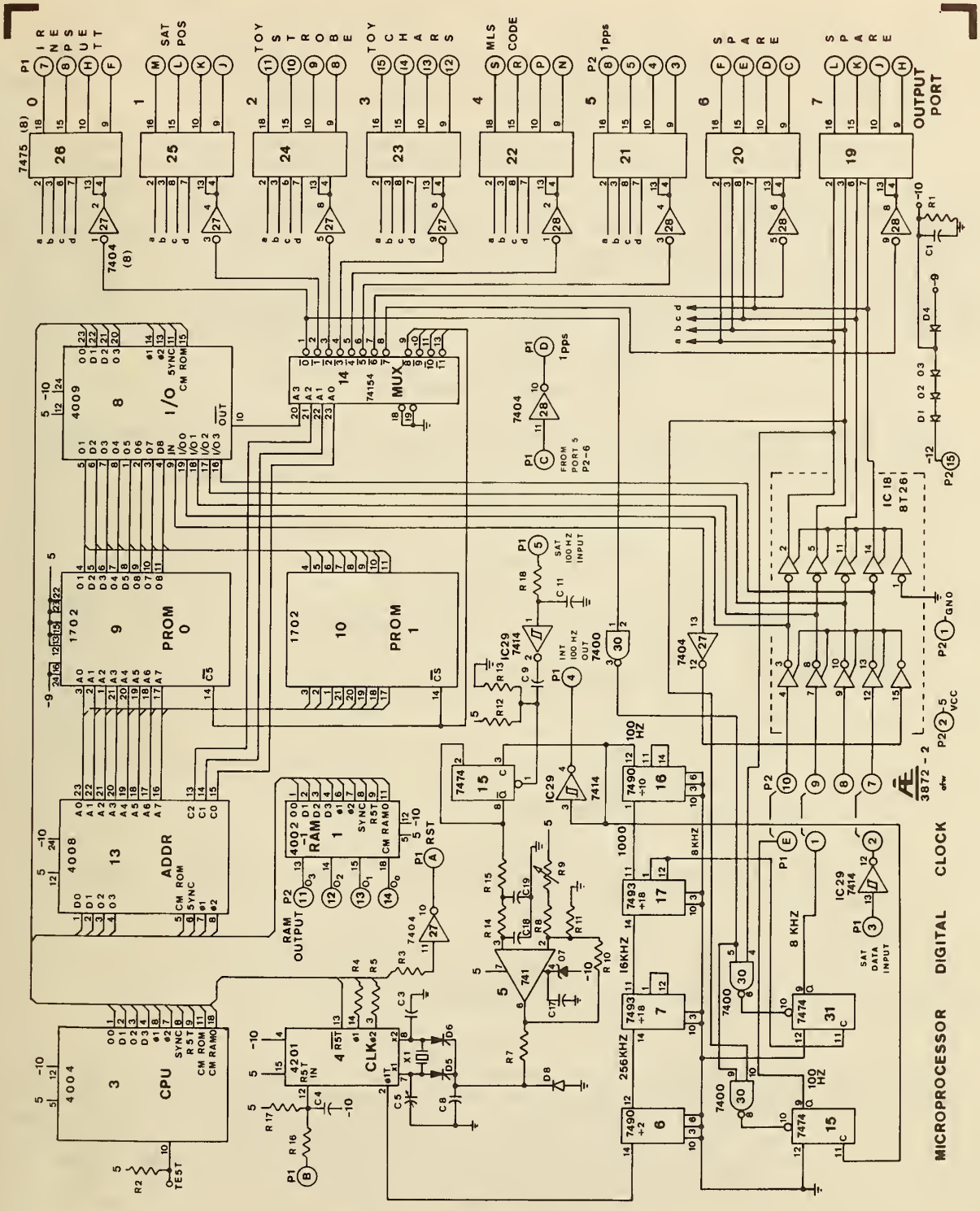

FIGURE 12. DIGITAL CLOCK SCHEMATIC

Figure 13 shows the wiring diagram of the display board. Figure 14 shows the clock, display, and a "delay slide rule." This slide rule is used to compute the delays from Wallops Island, VA, to the user's location via the satellite using the satellite position data contained in the time code format. See references 1-3 for more detail on the design and use of this slide rule. Figures 15a - 15f provide board layout and component location information.

The satellite position display consists of a hex-32 shift register which stores the 13 satellite position characters plus three blank characters twice over. The 32 characters are then clocked out of the shift register in sequence by a hardware clock on the display board that runs independently of the microprocessor. The output of the shift register goes into a 7-segment decoder and the 13 position characters are displayed. The position display runs by itself and receives attention from the microprocessor only at 00 and 30 s when the hex-32 shift register is reloaded. Presently the satellite position changes only each half hour and the shift register receives the same satellite position information 60 consecutive times. However, in the future it may become desirable to update the position information at a higher rate.

3.2 SOFTWARE LISTING

Pages 28-35 show a listing of the digital clock's software. The program was punched into standard 80 column data processing cards only as a convenient method of documentation. The format of the listing is as follows:

Column	
1	Hexadecimal page or ROM chip number
2	Blank
3-4	Hexadecimal instruction address within ROM chip
5	Blank
6-7	Hexadecimal microprocessor instruction
8	Blank
9-18	1 to 10 character label
19	Blank
20-22	1 to 3 character operation mnemonic
23	Blank
24-33	1 to 10 character operand (data, register, condition, label, etc.)
34-37	Blank
38-80	Comments

Some 4004 instructions require two bytes in which case the second line of the instructions may contain data or a jump address.

3.3 DIGITAL CLOCK PERFORMANCE

The digital clock has been in operation for many months in a number of locations but at this time only NBS at Boulder has explored its full potential. The chart shown in figure 16 illustrates the long-term performance of the digital clock. The chart represents the time difference between the NBS master clock and a 1 pps from the digital clock and was obtained using the equipment shown in figure 17. The chart shows a peak-to-peak noise of less than 40 μs. The chart also shows the delay diurnal with a peak-to-peak value of approximately 450 μs. This chart was made during November 1975, when the satellite's inclination was approximately 1/2 degree.

The accuracy of the digital clock is dependent upon the correct assignment of path and equipment delays. The receiver and digital clock delays were studied

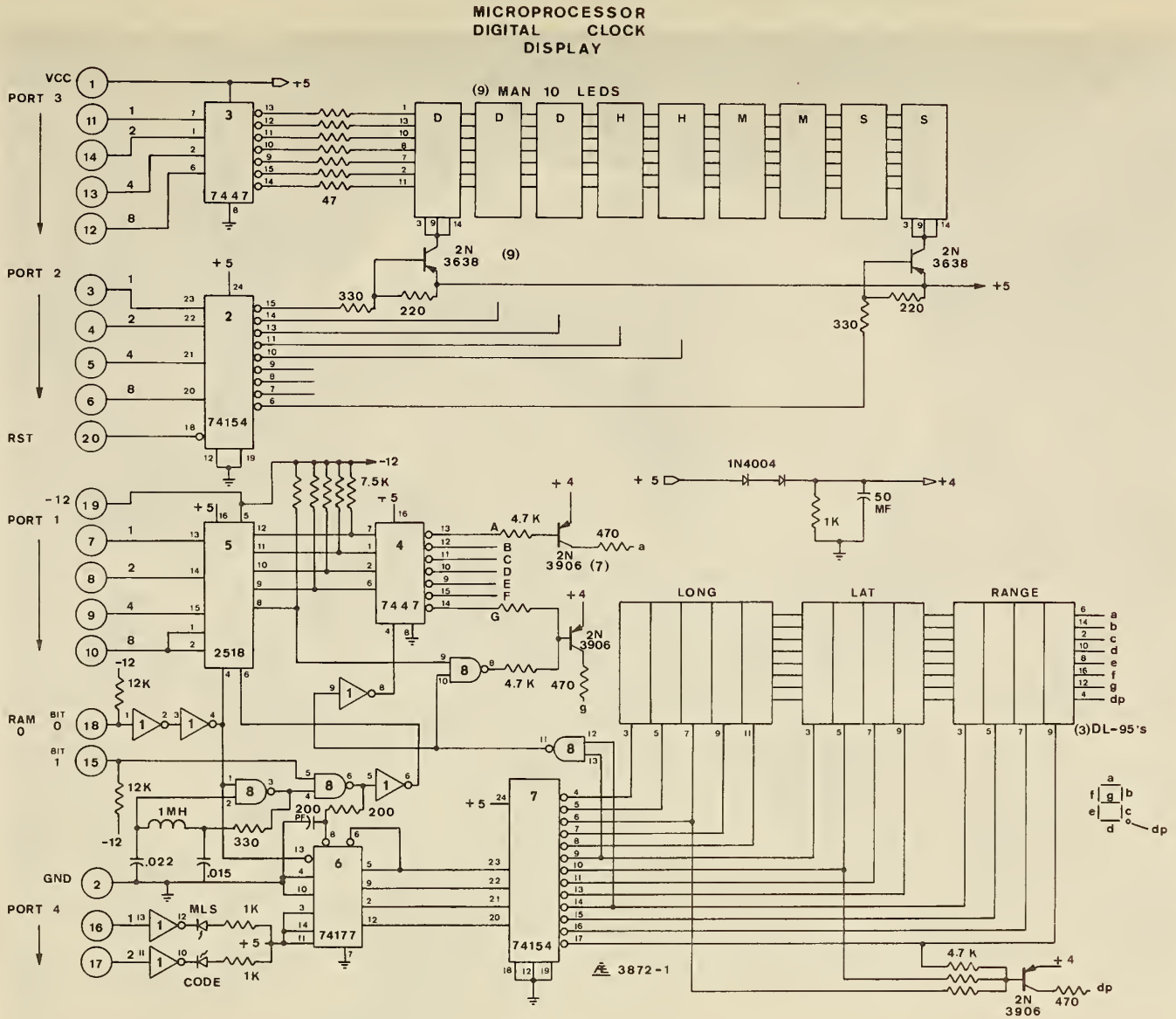

FIGURE 13. DIGITAL CLOCK DISPLAY SCHEMATIC

FIGURE 14. DIGITAL CLOCK, DISPLAY, AND PATH DELAY SLIDE RULE

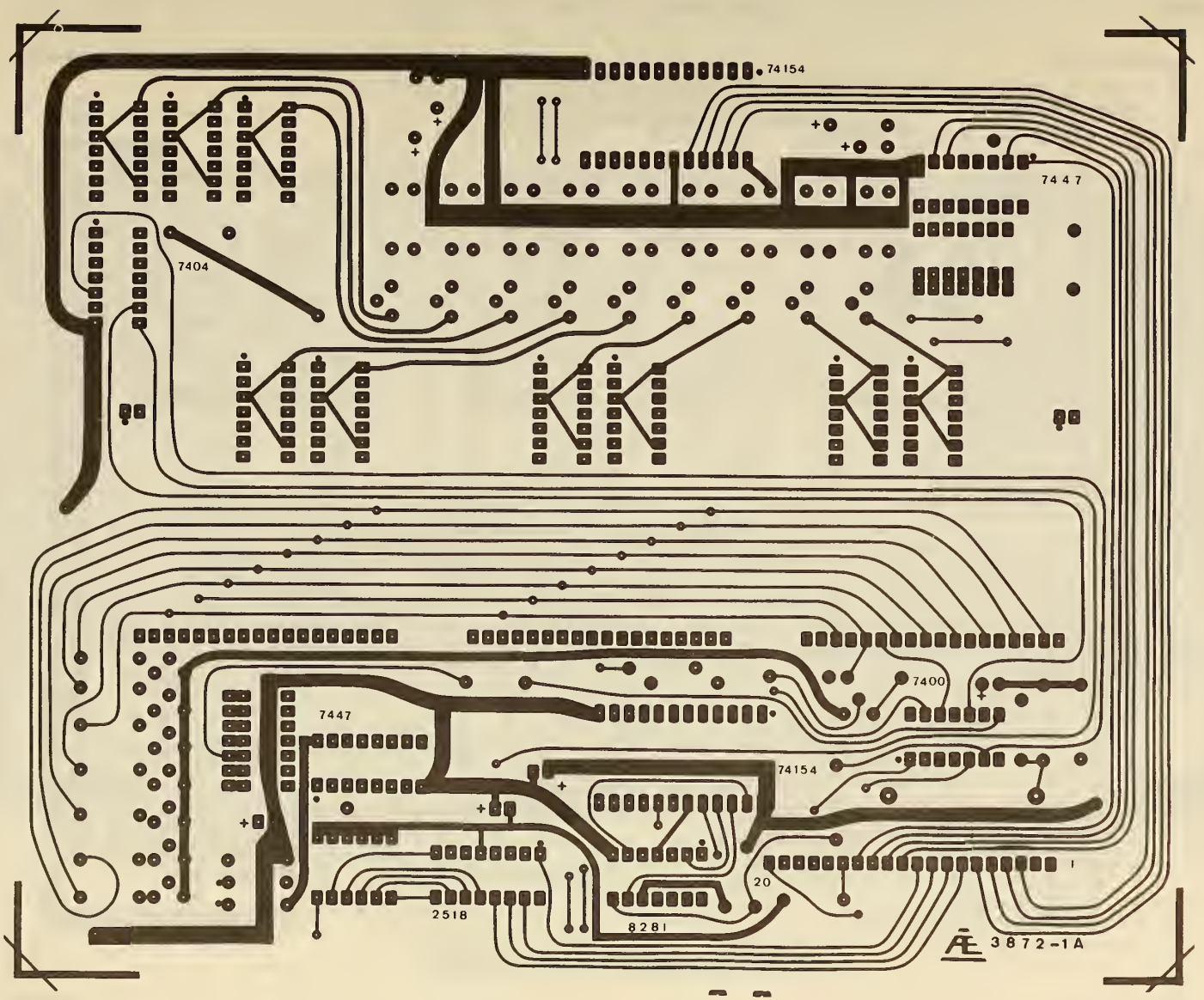

FIGURE 15a. DISPLAY BOARD (FRONT)

76x 6252

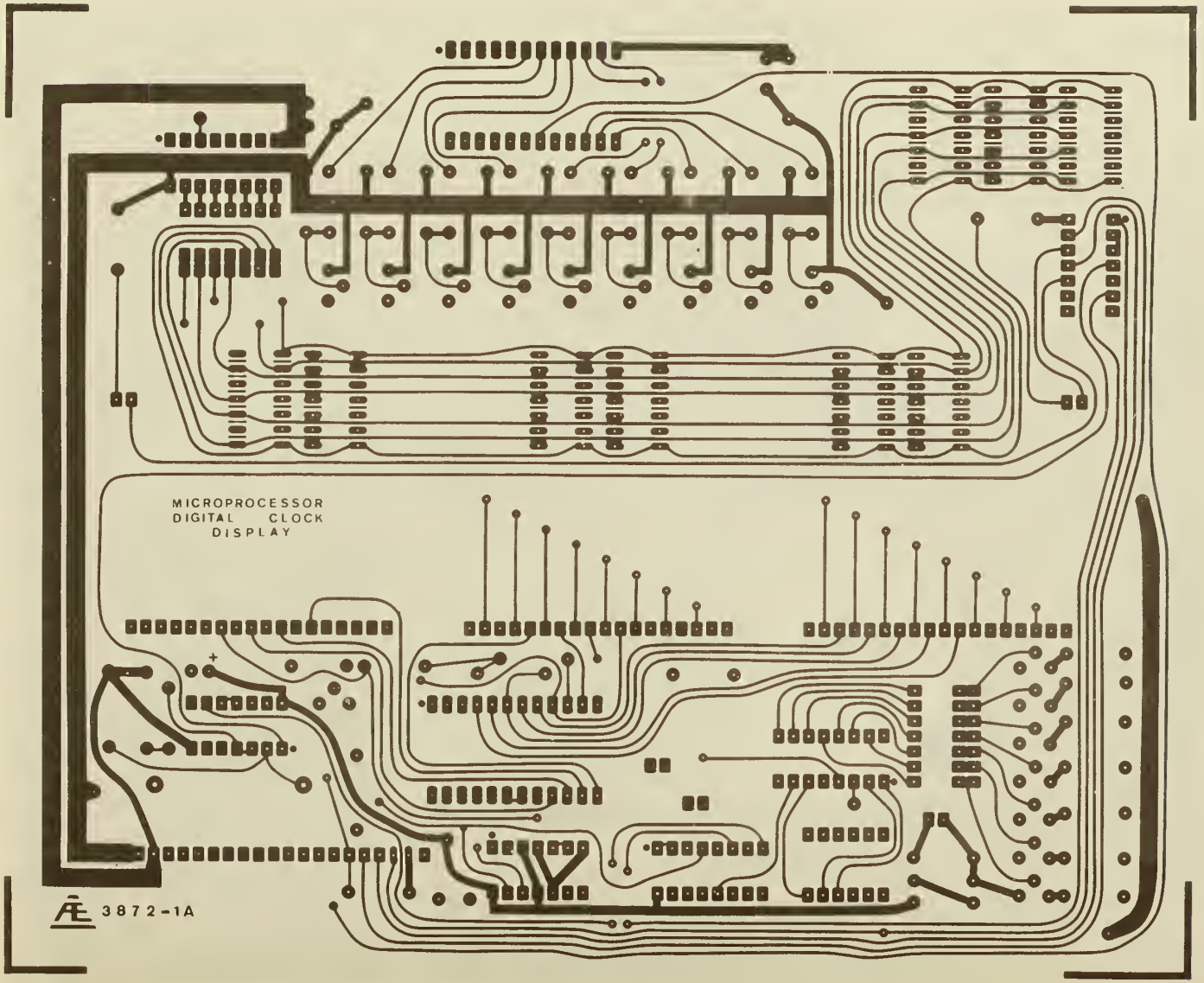

FIGURE 15b. DISPLAY BOARD (BACK)

76x 6251

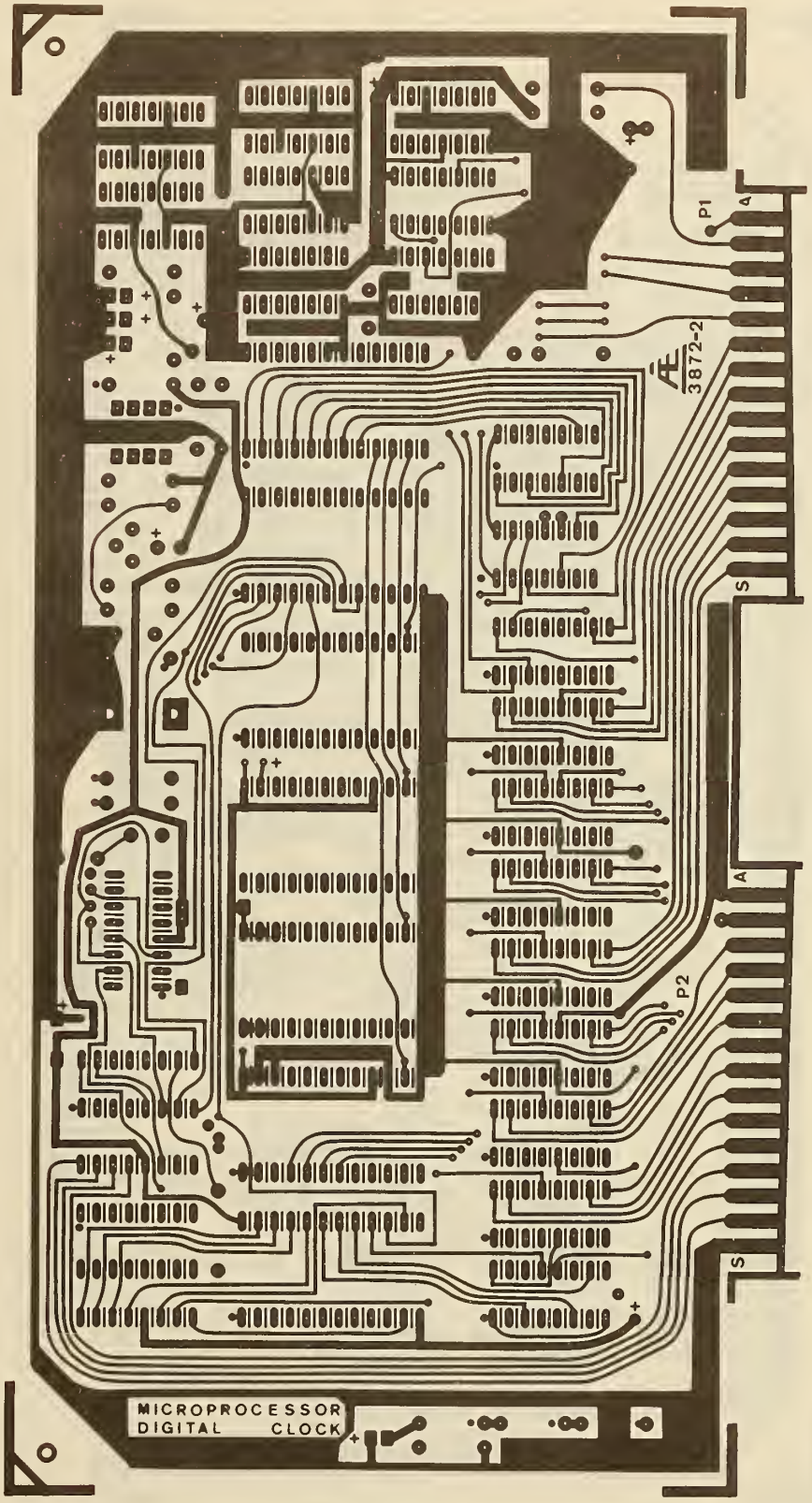

FIGURE 15c. CLOCK BOARD (FRONT)

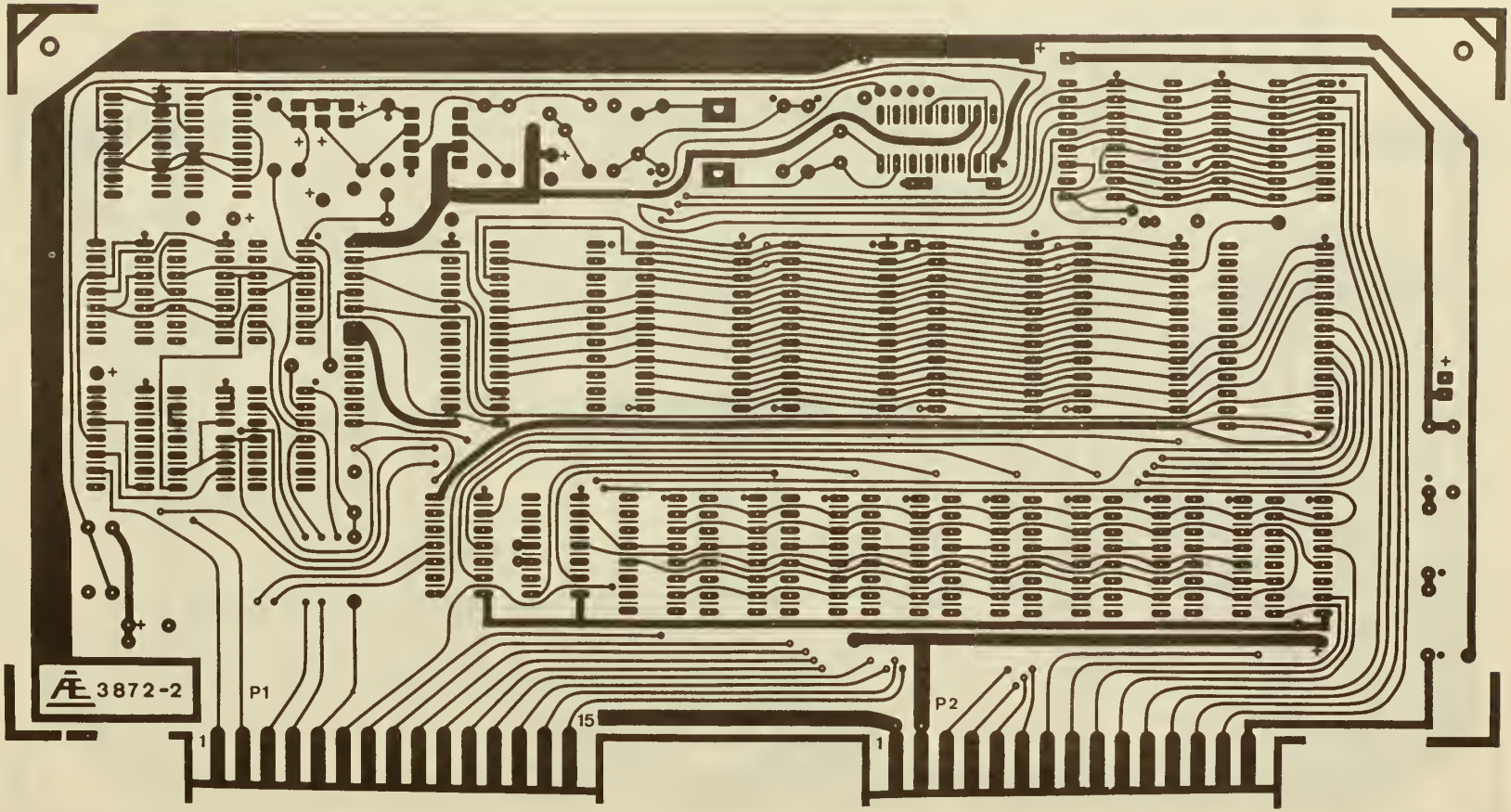

FIGURE 15d. CLOCK BOARD (BACK)

76X 6253

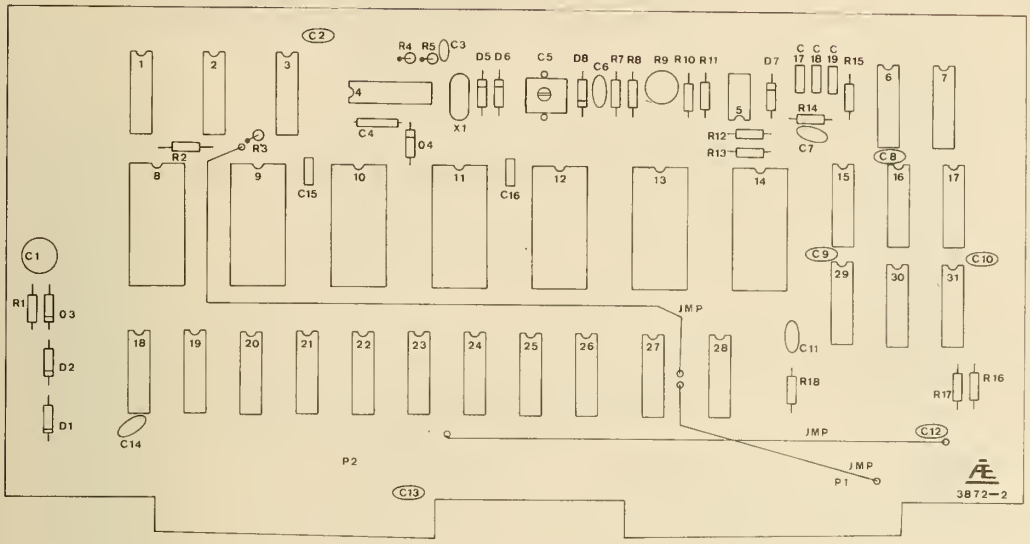

FIGURE 15e. CLOCK BOARD COMPONENT LAYOUT

R1 - 1k
R2 - 4.7k
R3 - 7.5k
R4 - 47
R5 - 47
R7 - 10k
R8 - 10k
R9 - 20k pot
R10 - 100k
R11 - 10k
R12 - 2.7k
R13 - 2.7k
R14 - 10k
R15 - 10k
R16 - 10k
R17 - 1M
R18 - 270

D1 - IN4004
D2 - IN4004
D3 - IN4004
D4 - IN4004
D5 - MV1628
D6 - MV1628
D7 - IN4004
D8 - IN4004

X1 - 4.096 MHz

C1 - 47 µf 16V
C2 - 4.7 µf tant.
C3 - 22 pf silver mica
C4 - 1 µf
C5 - 5.5-18 µf
C6 - 0.1 µf 10V
C7 - 4.7 µf tant.
C8 - 4.7 µf tant.
C9 - .001 µf
C10 - 4.7 µf tant.
C11 - 0.1 µf 10V
C12 - 4.7 µf tant.
C13 - 4.7 µf tant.
C14 - 4.7 µf tant.
C15 - 4.7 µf tant.
C16 - 4.7 µf tant.
C17 - 4.7 µf tant.
C18 - 4.7 µf tant.
C19 - 4.7 µf tant.

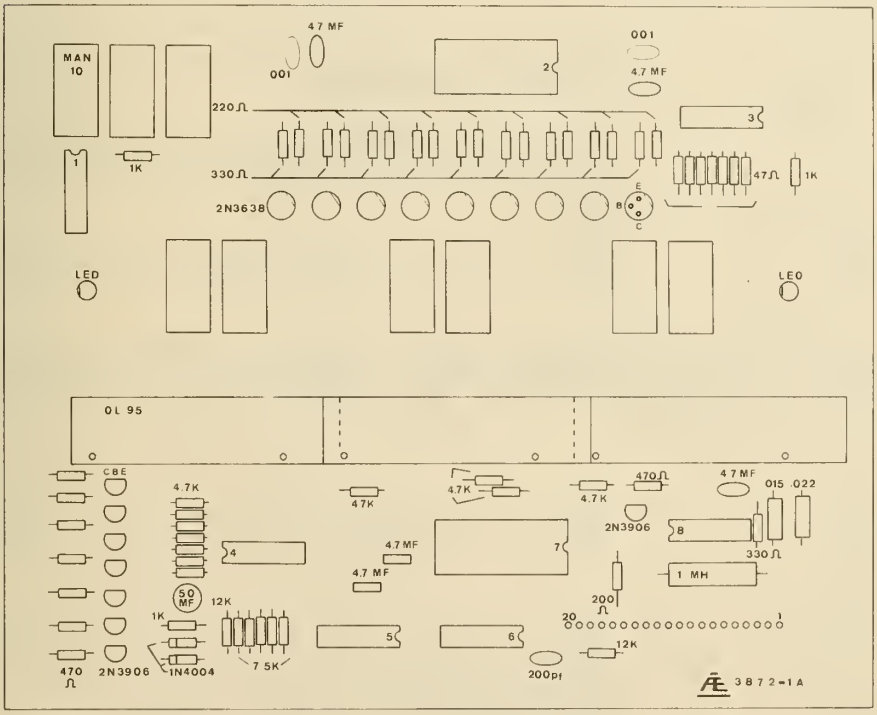

FIGURE 15f. DISPLAY BOARD COMPONENT LAYOUT

ROM ADDRESS	INSTRUCTION		MNEMONIC		COMMENTS
0	00				NBS SATELLITE CONTROLLED DIGITAL CLOCK,
0	01				TIME OF YEAR AND SATELLITE POSITION
0	02	F0 START	CLB		IN THIS VERSION THE 1 HZ OUTPUT IS
0	03	22	FIM	P1	CONTROLLED TO WITHIN 30 MICRO SECONDS
0	04	00	0	0	
0	05	24	FIM	P2	
0	06	00	0	0	
0	07	26	FIM	P3	
0	08	00	0	0	
0	09	28	FIM	P4	SET INDEX REGISTERS 2 THRU F = 0
0	0A	00	0	0	
0	0B	2A	FIM	P5	
0	0C	00	0	0	
0	0D	2C	FIM	P6	
0	0E	00	0	0	
0	0F	2E	FIM	P7	
0	10	00	0	0	
0	11	20	FIM	P0	
0	12	40	4	0	TURN OFF MLS AND CODE SYNC LIGHTS
0	13	21	SRC	P0	
0	14	DF	LDM	F	
0	15	E2	WRR		
0	16	40	JUN	-	
0	17	20	-	020	
0	18				
0	19				
0	1A				
0	1B				
0	1C				
0	1D				
0	1E				
0	1F				
0	20				
0	21	51 ANOTHER	JMS	-	GO TO WAIT AND STAY UNTIL A 100 OR AN 8000
0	22	00	-	WAIT	HZ TRANSITION OCCURS
0	23	22	FIM	P1	
0	24	2C	2	C	SELECT RAM 0/REG 2/CHARS C THRU F WHERE
0	25	F0	CLB		15 BIT MLS SYNC PATTERN WILL BE STORED AS
0	26	23 SERIAL	SRC	P1	THE BITS ARE RECEIVED
0	27	E9	RDM		
0	28	F6	RAR		SHIFT RAM CHARS C THRU F (MLS) RIGHT ONE
0	29	E0	WRM		BIT TO MAKE ROOM FOR A NEWLY RECEIVED BIT
0	2A	73	ISZ	R3	
0	2B	26	-	SERIAL	
0	2C	0E	THIS DATA IS THE MLS SYNC PATTERN AND IS STORED HERE BECAUSE THESE ROM		
0	2D	08	ADDRESSES ARE THE SAME AS THE RAM CHARACTER ADDRESSES OF THE RECEIVED		
0	2E	02	MLS SYNC PATTERN AND THIS SIMPLIFIES THEIR COMPARISON LATER AT ADD. 046		
0	2F	02	(WILL BE EXECUTED AS NOPS)		
0	30				
0	31				
0	32	E9	RDM		
0	33	F6	RAR		CHAR F STILL SELECTED IN RAM -- SETS 16TH
0	34	F1	CLC		BIT OF 4 MLS RECEIVED CHARACTERS = 0
0	35	F5	RAL		
0	36	E0	WRM		
0	37	F0	CLB		
0	38	A8	LD	R8	REG 8 CONTAINS A DATA BIT IN ITS 2 POSITION
0	39				THIS WAS STORED IN REG 8 BY WAIT WHEN A 100
0	3A				HZ TRANSITION WAS SENSED AND A JUMP TO
0	3B	F5	RAL		COUNT OCCURRED
0	3C	F5	RAL		SHIFT DATA BACK TO THE 8 POSITION READY TO
0	3D	20	FIM	P0	ADD TO RAM
0	3E	2C	2	C	SELECT RAM 0/REG 2/CHAR C
0	3F	21	SRC	P0	

```
0 40 EB              ADM             ADD NEWEST BIT RECEIVED TO 8 POSITION OF
0 41 E0              WRM             CHARACTER C, I.E. STORE IT IN RAM
0 42 21 OK           SRC P0
0 43 32              FIN P1          PUT CONTENTS OF ADDRESS 0C INTO P1
0 44 FC              CLB
0 45 A3              LD  R3          PUT CONTENTS OF R3 (= E) INTO ACCUMULATOR
0 46 E8              SBM             SUBTRACT RAM CHAR C FROM ACCUMULATOR
0 47 1C              JCN A1
0 48 21              -   ANOTHER
0 49 71              ISZ R1          IF CHAR C = (ACCUMULATOR) INCREMENT R1 AND
0 4A 42              -   OK          JUMP TO OK TO TEST NEXT RAM CHARACTER
0 4B 20              FIM P0          AGAINST DATA
0 4C 40              4   0           IF THIS POINT IS REACHED MLS MATCHES --
0 4D 21              SRC P0          TURN ON MLS LIGHT
0 4E 0E              LDM E
0 4F E2              WRR
0 50 2E              FIM P7          SET UP P7 TO COUNT 31 CALLS TO WAIT
0 51 1E              1   E
0 52 51 AGAIN        JMS -
0 53 00              -   WAIT        MAKE 31 CALLS TO WAIT TO SKIP 31 BITS
0 54 7E              ISZ RE          BETWEEN MLS AND BCD CHARACTER
0 55 52              -   AGAIN
0 56 7F              ISZ RF
0 57 52              -   AGAIN
0 58 D6              LDM 6           INITIALIZE 10 A/5 COUNTER
0 59 BD              XCH RD
0 5A 51              JMS -           CALL LOAD4 TO MAKE 4 CALLS TO WAIT TO GET
0 5B E0              -   LOAD4       ONE BCD CHARACTER
0 5C 40              JUN -
0 5D 68              -   CODE SYNC
0 5E 2E MORE         FIM P7          SET UP TO MAKE 46 CALLS TO WAIT
0 5F 2D              2   D
0 60 51 MORE+2       JMS -
0 61 00              -   WAIT
0 62 7E              ISZ E           SKIP 46 BITS BETWEEN BCD CHARACTERS -- ONCE
0 63 60              -   MORE+2      MLS SYNC IS ESTABLISHED FRAME SYNC AND CODE
0 64 7F              ISZ F           RECEIVING IS DONE BY SKIPPING BITS BETWEEN
0 65 60              -   MORE+2      BCD CHARACTERS
0 66 51              JMS -           GET NEXT BCD CHARACTER
0 67 E0              -   LOAD4
0 68 F0 CODE SYNC    CLB
0 69 2C              FIM PC          SET UP TEST FOR A OR 5 CHARACTER, THAT IS
0 6A A5              A   5           LOOK FOR FRAME SYNC
0 6B A0              LD  P0          LOAD THE CHARACTER A INTO THE ACCUMULATOR
0 6C 9C              SUB RC
0 6D 14              JCN A0          JUMP TO CONTINUE IF CONTENTS OF RC =
0 6E 78              -   CONTINUE    CHARACTER A
0 6F FC              CLB
0 70 A1              LD  R1          LOAD CHARACTER 5 INTO ACCUMULATOR
0 71 9C              SUB RC
0 72 14              JCN A0          JUMP TO CONTINUE IF CONTENTS OF RC = 5
0 73 78              -   CONTINUE
0 74 D6              LDM 6
0 75 BD              XCH RD          RESET THE 10 A/5 COUNTER TO 6, I.E. GET
0 76 40              JUN -           READY TO COUNT 10 AS OR 10 5S AND GO BACK
0 77 02              -   START       TO START
0 78 7D CONTINUE     ISZ RD          GO TO MORE IF NOT 10 AS OR 10 5S FOUND
0 79 5E              -   MORE
0 7A 2C              FIM PC          CODE SYNC IS ESTABLISHED IF THIS POINT IS
0 7B 40              4   0           REACHED
0 7C 21              SRC P9          TURN ON CODE SYNC LIGHT (KEEP MLS LIGHT ON
0 7D 0C              LDM C           ALSO)
0 7E E2              WRR
0 7F
```

```
0 80 DC             LDM 0               R0 IS NOW USED FOR THE WRITE TIME OF YEAR
0 81 B0             XCH R0              (TOY) FLAG --- SET IT = 0
0 82 22             FIM P1
0 83 33             3   3               SELECT TOY .01 SECOND CHARACTER IN RAM
0 84 23             SRC P1
0 85 D4             LDM 4
0 86 E0             WRM                 WRITE HUNDREDTH SECOND CHARACTER = 4 IN RAM
0 87 63             INC R3
0 88 23             SRC P1
0 89 D5             LDM 5
0 8A E0             WRM                 WRITE TENTH SECOND CHARACTER = 5 IN RAM
0 8B 63             INC R3
0 8C 23             SRC P1
0 8D D4             LDM 4
0 8E E0             WRM                 WRITE UNIT SECOND CHARACTER = 4 IN RAM
0 8F 40             JUN -
0 90 A0              -  U/C
0 91
0 92                                    FINDING 10 AS OR 10 55 CONSTITUTES CODE
0 93                                    SYNC, THAT IS LOCATES START OF TOY CODE --
0 94                                    CODE SYNC OCCURS AT 4.54 AND 34.54 SECOND
0 95                                    THEREFORE SET       UNIT SECOND = 4
0 96                                                      TENTHS SECOND = 5
0 97                                                  HUNDREDTHS SECOND = 4
0 98
0 99
0 9A
0 9B
0 9C
0 9D
0 9E
0 9F
0 A0 2A ITOD        FIM P5              SET UP TO SELECT RAM 0/REG 3/CHARS 6 THRU F
0 A1 36             3   6               TIME OF YEAR (TOY)
0 A2 DC             LDM C               SET R9, TOY CHARACTER ERROR FLAG = C
0 A3 B9             XCH R9
0 A4 2E NEXT10      FIM P7              SET UP 46 BIT COUNTER
0 A5 2D             2   D
0 A6 51 AGAIN10     JMS -
0 A7 09              -  WAIT
0 A8 7E             ISZ R6              SKIP 46 BITS BETWEEN BCD CHARACTERS
0 A9 A6              -  AGAIN10
0 AA 7F             ISZ R7
0 AB A6              -  AGAIN10
0 AC 51             JMS -               GET NEXT TIME OF YEAR CHARACTER
0 AD E0              -  LOAD4
0 AE AD             LD  R0
0 AF 1C             JCN A1              TEST WRITE FLAG (R0) -- IF NOT = 0 JUMP TO
0 B0 C6              -  COMPARE         COMPARE -- ELSE WRITE TOY INTO RAM
0 B1 28             SRC P5
0 B2 AC             LD  RC              WRITE TOY CHARACTERS INTO RAM 0/REG 3/
0 B3 E0             WRM                 CHARACTERS C THRU F
0 B4 76 RETURN      ISZ R8              INCREMENT AND TEST FOR 10 TOY CHARACTERS
0 B5 A4              -  NEXT10          READ AND WRITTEN INTO RAM OR COMPARED
0 B6 A9             LD  R9
0 B7 1C             JCN A1              TEST R9 (TOY CHAR ERROR FLAG) TO SEE IF AT
0 B8 BD              -  INCREMENT       LEAST ONE TOY CHARACTER ERROR OCCURRED
0 B9 DC             LDM C               DURING THE LAST FRAME.  IF IT DID -- GO TO
0 BA BC             XCH RC              INCREMENT TO INCREMENT FRAME ERROR COUNTER
0 BB 40             JUN -               ELSE RESET FRAME ERROR COUNTER TO BE ABLE
0 BC 08              -  ISAT            TO COUNT 4 CONSECUTIVE FRAME ERRORS
0 BD 6D INCREMENT   INC RD
0 BE AD             LD  RD              INCREMENT TOY CHAR ERROR COUNTER
0 BF
```

```
0 C0 14             JCN A0
0 C1 02              -  START        IF RD = 0 THEN 4 CONSECUTIVE FRAME ERRORS
0 C2 4C             JUN -           OCCURRED -- GO BACK TO START -- ELSE GO ON
0 C3 D8              -  ISAT        TO RECEIVE SATELLITE POSITION INFORMATION
0 C4
0 C5
0 C6 2B COMPARE     SRC P5          ARRIVE HERE IF WRITE FLAG (RD) IS NOT = 0
0 C7 AC             LD  RC          TO COMPARE TOY CHARACTER IN RC WITH TOY
0 C8 E8             SBM             CHARACTER IN RAM
0 C9 F1             CLC
0 CA 14             JCN A0
0 CB B4              -  RETURN      GO TO RETURN IF TOD CHARACTER IS THE SAME
0 CC D1             LDM 1
0 CD B9             XCH R9          SET R9, CHAR ERROR FLAG =1 AND GO TO RETURN
0 CE 40             JUN -           IF TOY CHARACTER IS NOT THE SAME
0 CF B4              -  RETURN
0 D0
0 D1
0 D2
0 D3
0 D4
0 D5
0 D6
0 D7
0 D8 2A ISAT        FIM P5          INITIALIZE 13 WORD COUNT AND SELECT OF
0 D9 13             1   3           RAM 0/REG 1/CHARACTERS 3 THRU F SATELLITE
0 DA 2E NEXT13      FIM P7          POSITION
0 DB 20             2   0           INITIATE 46 BIT COUNTER
0 DC 51 AGAIN13     JMS -
0 DD 0C              -  WAIT
0 DE 7E             ISZ R6          SKIP 46 BITS BETWEEN SAT. POS. CHARACTERS
0 DF DC              -  AGAIN13
0 E0 7F             ISZ R7
0 E1 DC              -  AGAIN13
0 E2 51             JMS -           GET NEXT SATELLITE POSITION CHARACTER
0 E3 E0              -  LOAD4
0 E4 2B             SRC P5
0 E5 AC             LD  RC          WRITE SAT. POS. CHAR. INTO RAM
0 E6 E0             WRM
0 E7 7B             ISZ RB          INCREMENT SAT. POS. CHAR. ADDRESS IN RAM
0 E8 DA              -  NEXT13
0 E9 40             JUN -           WHEN THIS POINT IS REACHED 13 SAT. POS.
0 EA F0              -  0F0         CHARACTERS HAVE BEEN RECEIVED AND WRITTEN
0 EB                                INTO RAM
0 EC
0 ED
0 EE
0 EF
0 F0 2A             FIM P5          INITIALIZE FOR 37 FRAME COUNT
0 F1 B0             B   0
0 F2 2F NEXT37      FIM P7          INITIALIZE FOR 50 BIT COUNT
0 F3 EC             E   C
0 F4 51 AGAIN50     JMS -
0 F5 0C              -  WAIT
0 F6 7E             ISZ R6
0 F7 F4              -  AGAIN50     SKIP 50 BITS IN A FRAME
0 F8 7F             ISZ R7
0 F9 F4              -  AGAIN50
0 FA 7A             ISZ R2
0 FB F2              -  NEXT37      SKIP 37 FRAMES BETWEEN END OF SATELLITE
0 FC 7B             ISZ RB          POSITION AND START OF TIME OF YEAR
0 FD F2              -  NEXT37
0 FE 40             JUN -           GO BACK TO RECEIVE TIME OF YEAR AGAIN
0 FF A0              -  ITOD
```

```
1 00 F0 WAIT      CLB             CLEAR ACCUMULATOR AND CARRY
1 01 22           FIM P1
1 02 00           0   0           SELECT IN/OUT PORT NO. 0 FOR INPUT AND
1 03 23           SRC P1          RESET
1 04 EA           RDR
1 05 F6           RAR
1 06 12           JCN C1          IF 100 HZ IS PRESENT JUMP TO COUNT
1 07 30            -  COUNT
1 08
1 09 F6           RAR             ROTATE 8000 HZ INTO CARRY POSITION
1 0A 12           JCN C1
1 0B 0F            -  DISPLAY     IF 8000 HZ IS PRESENT JUMP TO DISPLAY
1 0C 41           JUN -
1 0D 00            -  WAIT        CONTINUE LOOKING FOR 100 OR 8000 HZ
1 0E                              TRANSITION
1 0F D2 DISPLAY   LDM 2           RESET 8000 HZ
1 10 E2           WRR
1 11 A7           LD  R7
1 12 1C           JCN A1          TEST IF R7, RAM TOY CHAR ADDRESS IS NOT = 0
1 13 18            -  NZERO
1 14 26           FIM P3
1 15 35           3   5           IF R7 = 0 RESET RAM CHIP/REG/CHAR SELECT
1 16 24           FIM P2          AND RESET MUX STROBE AND MUX OUTPUT PORT
1 17 25           2   5           FOR TIME OF YEAR CHARACTER
1 18 27 NZERO     SRC P3
1 19 00           LDM 0           WRITE BLANK DATA (BLANK = NOT 0 = F)
1 1A E2           WRR
1 1B 25           SRC P2
1 1C A5           LD  R5          WRITE OUT TIME OF YEAR STROBE
1 1D F4           CMA
1 1E E2           WRR
1 1F 27           SRC P3
1 20 E9           RDM
1 21 F4           CMA             WRITE OUT TIME OF YEAR CHARACTER
1 22 E2           WRR
1 23 67           INC R7          INCREMENT RAM TOY CHARACTER ADDRESS
1 24 65           INC R5          INCREMENT STROBE
1 25 41           JUN -
1 26 00            -  WAIT        GO BACK AND WAIT FOR ANOTHER 100 OR 8000 HZ
1 27                              TRANSITION
1 28
1 29
1 2A
1 2B B6 COUNT     XCH R6          SAVE INPUT PORT NO. 0 IN R6 TEMPORARILY
1 2C 01           LDM 1           WRITE OUT 1 TO RESET 100 HZ LATCH ON
1 2D E2           WRR             OUTPUT PORT NO. 0
1 2E 22           FIM P1
1 2F 20           2   0           POINT TOY STROBE AT DISPLAY DIGIT NO. 0
1 30 23           SRC P1          WHEN 8000 HZ OCCURS TO MINIMIZE DISPLAY
1 31 DF           LDM F           FLICKER -- PREVENTS A DIGIT FROM STAYING ON
1 32 E2           WRR             WHILE CLOCK IS BEING UPDATED
1 33 B8           XCH R8          RESTORE INPUT PORT NO.0 DATA TO ACCUMULATOR
1 34 F1           CLC             CLEAR 100 HZ FROM CARRY
1 35 F6           RAR
1 36 F1           CLC             CLEAR 8000 HZ (IF PRESENT)
1 37 B8           XCH R8          SAVE DATA IN R8 2 BIT POSITION
1 38 22           FIM P1          SELECT RAM 0/REG 3/CHAR 3 THRU F, THAT IS
1 39 33           3   3           START WITH TOY .01 SECOND CHARACTER
1 3A 23           SRC P1
1 3B E9           RDM             READ .01 SECOND CHARACTER INTO ACCUMULATOR
1 3C F2           IAC             INCREMENT RAM CLOCK BY .01 SECOND
1 3D F8           DAA             IF CY=1 OR ACCUMULATOR IS GREATER THAN 9
1 3E EC           WRM             SET ACCUMULATOR = ACCUMULATOR + 6
1 3F 63           INC R3          WRITE .01 S BACK INTO SAME RAM LOCATION
```

```
1 40 23              SRC P1          INCREMENT RAM CHARACTER ADDRESS
1 41 F7              TCC             CLEAR ACCUMULATOR, MOVE CARRY TO 1 POSITION
1 42 EB              ADM             OF ACCUMULATOR, CLEAR CARRY
1 43 FB              DAA             ADD .1 S IN RAM TO CARRY FROM .01 S
1 44 E0              WRM             CHARACTER IN RAM -- DECIMAL ADJUST ACCUM.
1 45 12              JCN C1
1 46 60               -  USEC        IF CY FROM .1 SECOND = 1 DONT TEST FOR 9S
1 47 20              FIM P0          BECAUSE AFTER THE SUBTRACTION CY IS CLEARED
1 48 90              9  0
1 49 90              SUB R0          TENTHS SECOND STILL IN ACCUMULATOR -- TEST
1 4A 1C              JCN A1          FOR TENTHS SECOND = 9
1 4B 58               -  NOTNINE
1 4C F1              CLC
1 4D 20              FIM P0
1 4E 33              3  3
1 4F 21              SRC P0
1 50 E9              RDM             READ .01 SECOND INTO ACCUMULATOR AND TEST
1 51 20              FIM P0          FOR .01 SECOND = 9
1 52 90              9  0
1 53 90              SUB R0
1 54 1C              JCN A1
1 55 58               -  NOTNINE
1 56 41              JUN -           IF .1 AND .01 SECOND = .99 JUMP TO SPECIAL
1 57 B0               -  WAIT100     WAIT ROUTINE WHICH ONLY WAITS FOR 100 HZ
1 58 F1 NOTNINE      CLC             TRANSITION -- ELSE OUTPUT 0 TO PORT NO. 5
1 59 20              FIM P0
1 5A 50              5  0
1 5B 21              SRC P0          OUTPUT F (NEG. LOGIC 0) TO PORT NO. 5
1 5C DF              LDM F
1 5D E2              WRR
1 5E
1 5F
1 60 63 USEC         INC R3          SELECT UNIT SECOND CHARACTER IN RAM
1 61 23              SRC P1
1 62 F7              TCC
1 63 EB              ADM             ADD UNIT SECOND CHARACTER IN RAM TO CARRY
1 64 FB              DAA             FROM TENTHS SECOND IN ACCUMULATOR
1 65 E0              WRM             WRITE UNIT SECOND CHARACTER INTO RAM
1 66 63              INC R3
1 67 23              SRC P1          SELECT TENS OF SECOND CHARACTER IN RAM
1 68 F7              TCC
1 69 EB              ADM
1 6A E0              WRM             WRITE TENS OF SECOND CHARACTER INTO RAM
1 6B DA              LDM 10
1 6C EB              ADM             ACCUMULATOR STILL CONTAINS TENS OF SECOND--
1 6D 1A              JCN C0          ADD 10 -- IF TENS OF SECOND WAS A 6,THEN A
1 6E 71               -  MINUTE      CARRY OCCURS -- IF SO SET TENS SECOND = 0
1 6F D0              LDM 0           AND ADD THE CARRY TO UNIT MINUTES.  IF TENS
1 70 E0              WRM             SECOND CARRY = 0 THEN SET TENS SECOND = 0
1 71 63 MINUTE       INC R3
1 72 23              SRC P1          SELECT UNIT MINUTE CHARACTER IN RAM
1 73 F7              TCC
1 74 EB              ADM             ADD UNIT MINUTE IN RAM TO CARRY FROM TENS
1 75 FB              DAA             OF SECOND
1 76 E0              WRM             WRITE UNIT MINUTES INTO RAM
1 77 63              INC R3
1 78 23              SRC P1          SELECT TENS OF MINUTES CHARACTER IN RAM
1 79 F7              TCC
1 7A EB              ADM             ADD TENS OF MINUTE CHARACTER IN RAM TO
1 7B E0              WRM             CARRY FROM UNIT MINUTES IN ACCUMULATOR AND
1 7C DA              LDM 10          WRITE TENS OF MINUTES INTO RAM
1 7D EB              ADM             IF TENS OF MINUTES = 6 CARRY OVER TO UNIT
1 7E 1A              JCN C0          HOURS
1 7F 82               -  HOUR        JUMP TO HOUR IF TENS OF MINUTES CARRY = 0
```

```
1 80 D0             LDM 0
1 81 E0             WRM
1 82 63 HOUR        INC R3
1 83 23             SRC P1
1 84 F7             TCC
1 85 EB             ADM
1 86 F8             DAA
1 87 E0             WRM                 WRITE UNIT HOUR INTO RAM
1 88 63             INC R3
1 89 23             SRC P1              SELECT TENS OF HOURS CHARACTER IN RAM
1 8A F7             TCC
1 8B EB             ADM
1 8C E0             WRM                 WRITE TENS OF HOURS INTO RAM
1 8D FC             CLB
1 8E 22             FIM P1
1 8F 35             3   5
1 90 23             SRC P1
1 91 E9             RDM                 READ UNIT SECOND INTO ACCUMULATOR
1 92 14             JCN A0
1 93 95              -  TEST03          IF UNIT SECOND = 0 GO TEST FOR TENS OF
1 94 C0             BBL                 SECOND = 0 OR 3 -- ELSE RETURN
1 95 22 TEST03      FIM P1
1 96 36             3   6
1 97 23             SRC P1
1 98 E9             RDM                 READ TENS OF SECOND INTO ACCUMULATOR
1 99 14             JCN A0
1 9A A2              -  TENTHS
1 9B 22             FIM P1
1 9C 30             3   0               IF TENS OF SECOND = 0 OR 3 GO TEST TENTHS
1 9D 92             SUB R2              SECOND = 3 -- ELSE RETURN
1 9E 14             JCN A0
1 9F A2              -  TENTHS
1 A0 FC             CLC
1 A1 C0             BBL
1 A2 22 TENTHS      FIM P1
1 A3 34             3   4
1 A4 23             SRC P1
1 A5 E9             RDM                 IF TENTHS OF SECOND = 0 GO TEST FOR
1 A6 14             JCN A0              HUNDREDTHS OF SECONDS = 0 -- ELSE RETURN
1 A7 A9              -  HUNDREDTHS
1 A8 C0             BBL
1 A9 22 HUNDREDTHS  FIM P1
1 AA 33             3   3
1 AB 23             SRC P1              IF HUNDREDTHS SECOND = 0 GO SERVICE
1 AC E9             RDM                 SATELLITE POSITION DISPLAY -- ELSE RETURN
1 AD 14             JCN A0
1 AE C4              -  SPOS
1 AF C0             BBL
1 B0 F0 WAIT100     CLB                 SPECIAL WAIT ROUTINE TO KEEP 1HZ ON TIME
1 B1 20             FIM P0
1 B2 00             0   0               SELECT IN/OUT PORT NO.0 FOR INPUT AND RESET
1 B3 21             SRC P0
1 B4 EA READ        RDR
1 B5 F6             RAR
1 B6 1A             JCN C0              IF 100 HZ IS NOT PRESENT GO BACK AND WAIT
1 B7 B4              -  READ            SOME MORE -- ELSE OUTPUT 1 HZ
1 B8 20             FIM P0
1 B9 50             5   0
1 BA 21             SRC P0              OUTPUT E (NEG. LOGIC 1) TO PORT NO. 5
1 BB DE             LDM E
1 BC E2             WRR
1 BD D1             LDM 1               WRITE OUT 1 TO RESET 100 HZ LATCH ON
1 BE E2             WRR                 OUTPUT PORT NO. 6
1 BF F0             CLB
```

```
1 C0 41              JUN -
1 C1 60               - USEC          GO BACK TO PROCESS UNIT SECONDS
1 C2
1 C3
1 C4 20 SPOS         FIM P0          SET UP SELECT OF RAM 0/REG 1/CHARACTERS 3
1 C5 13              1   3           THRU F, SATELLITE POSITION
1 C6 21              SRC P0
1 C7 D1              LDM 1           WRITE A 1 TO RAM OUTPUT PORT TO TURN OFF
1 C8 E1              WMP             2518 SHIFT REGISTERS CLOCK
1 C9 22              FIM P1          SET UP OUTPUT PORT NO. 1 SELECT AND P3
1 CA 1E              1   E
1 CB 21 RPAM         SRC P0
1 CC E9              RDM             READ A SATELLITE POSITION CHAR FROM RAM
1 CD 23              SRC P1
1 CE F4              CMA
1 CF E2              WPR             WRITE OUT A SATELLITE POSITION CHARACTER TO
1 D0 21              SRC P0          OUTPUT PORT NUMBER 1
1 D1 D3              LDM 3
1 D2 E1              WMP             WRITE A 2 TO RAM OUTPUT PORT TO CLOCK DATA
1 D3 D1              LDM 1           INTO 2518 SHIFT REGISTER -- BUT A 1 MUST
1 D4 E1              WMP             STILL BE GOING OUT TO KEEP SHIFT REGISTERS
1 D5 71              ISZ R1          CLOCK OFF
1 D6 CB               - RPAM         INCREMENT SATELLITE POSITION CHAR ADDRESS
1 D7 73              ISZ R3          FILL HEX-32 SHIFT REGISTER (2518) TWICE,
1 D8 CB               - RPAM         THAT IS, 2*(13 CHAR + 3 BLANKS) = 32 CHAR
1 D9 D0              LDM 0
1 DA E1              WMP             WRITE A 0 TO RAM OUTPUT PORT TO TURN SHIFT
1 DB C0              BBL             REGISTERS CLOCK BACK ON
1 DC
1 DD
1 DE
1 DF
1 E0 DC LOAD4        LDM C           CLEAR RC IN PREPARATION TO RECONSTRUCT BCD
1 E1 BC              XCH RC          CHARACTER IN RC
1 E2 51              JMS -
1 E3 00               - WAIT         GO TO WAIT TO GET BCD CHARACTER 1 BIT
1 E4 A6              LD  R6
1 E5 F1              CLC
1 E6 F6              RAR             MOVE DATA BIT TO 1 POSITION AND ADD TO RC
1 E7 8C              ADD RC
1 E8 BC              XCH RC
1 E9 51              JMS -           GET BCD CHARACTER 2 BIT
1 EA 00               - WAIT
1 EB A8              LD  R8
1 EC 8C              ADD RC          DATA BIT IS ALREADY IN 2 POSITION -- JUST
1 ED BC              XCH RC          ADD IT TO RC
1 EE 51              JMS -
1 EF 00               - WAIT         GET BCD CHARACTER 4 BIT
1 F0 A8              LD  R8
1 F1 F1              CLC
1 F2 F5              RAL             MOVE DATA BIT TO 4 POSITION AND ADD TO RC
1 F3 8C              ADD RC
1 F4 BC              XCH RC
1 F5 51              JMS -           GET BCD CHARACTER 8 BIT
1 F6 00               - WAIT
1 F7 A8              LD  R8
1 F8 F1              CLC
1 F9 F5              RAL
1 FA F5              RAL             MOVE DATA BIT TO 8 POSITION AND ADD TO RC
1 FB 8C              ADD RC
1 FC BC              XCH RC
1 FD C0              BBL
1 FE
1 FF
```

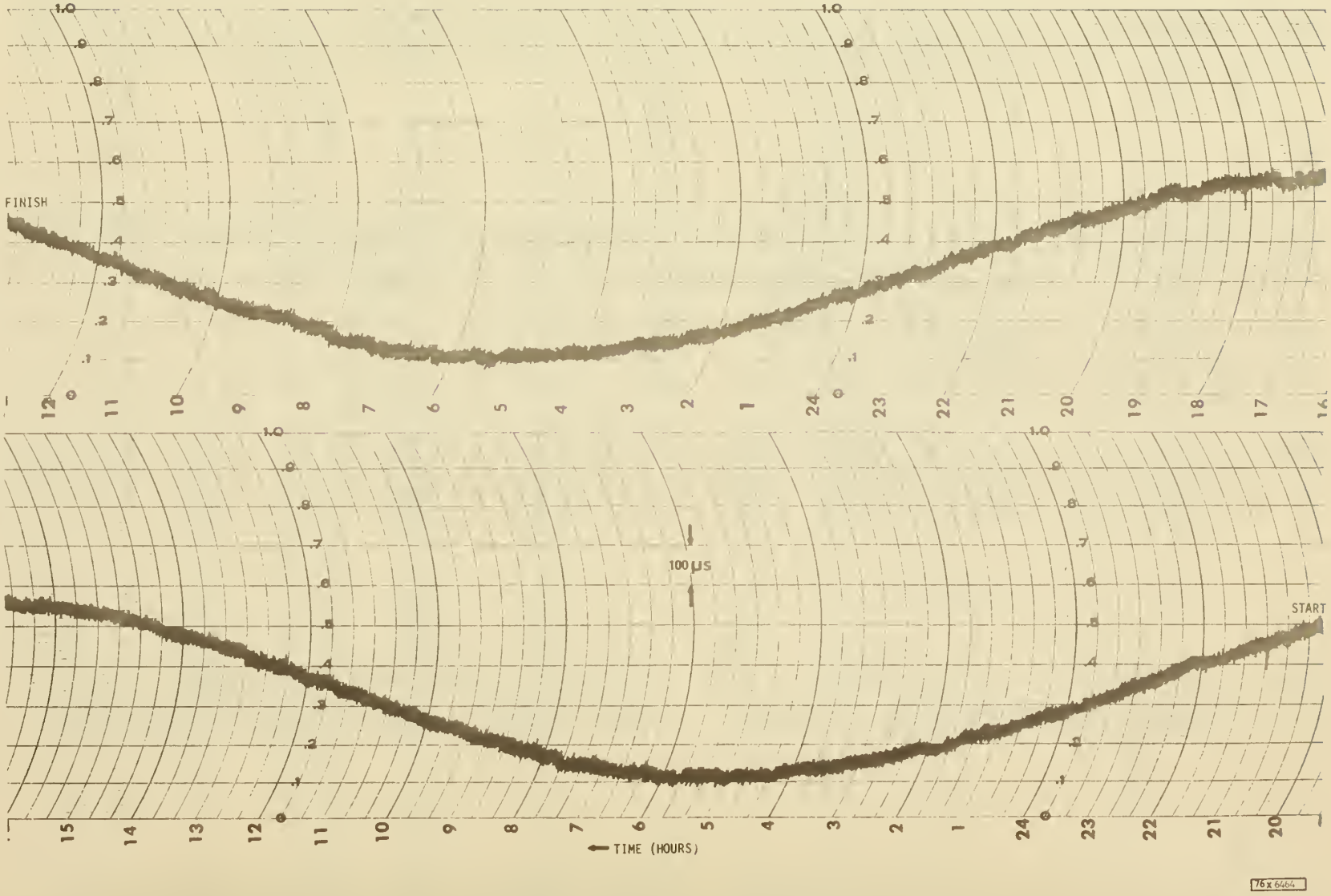

FIGURE 16. UTC(NBS) - SATELLITE CLOCK (MICROPROCESSOR)

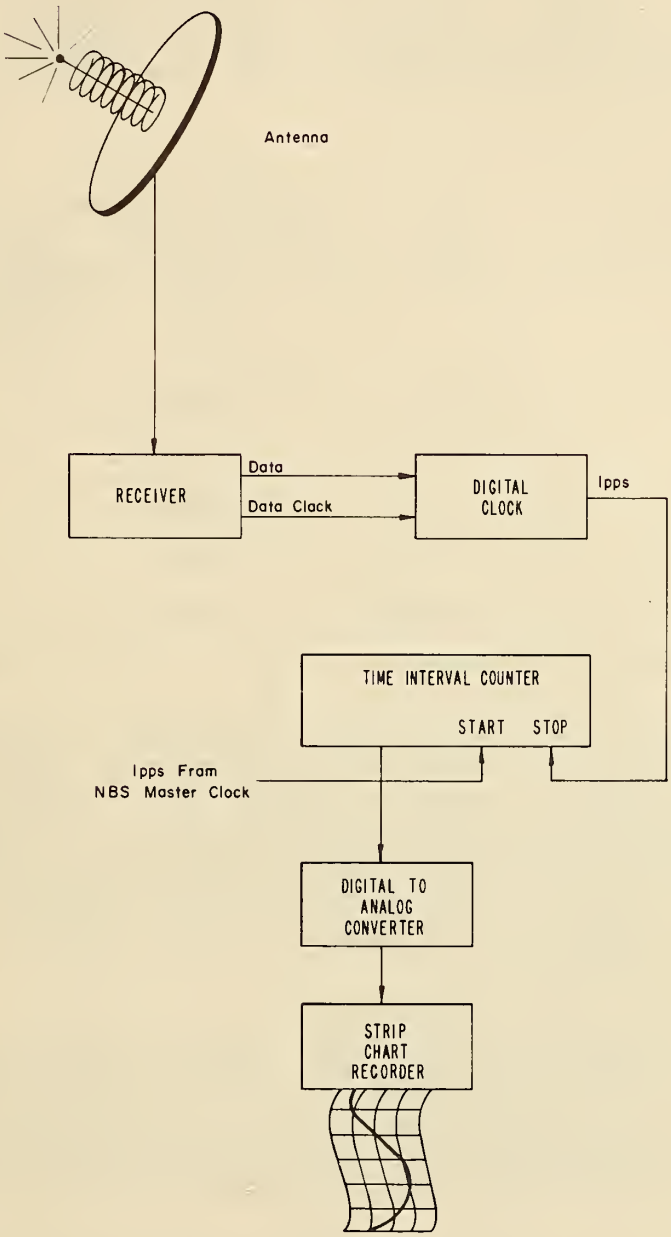

FIGURE 17. DIGITAL CLOCK PERFORMANCE MEASUREMENT SETUP

separately. The digital clock's delay was measured to be -5074 μs with no significant variation over an observed time of a few weeks. The delay is rather artificial since it is a function of software and can be set to any value by instruction. As an example the software can be adjusted to effectively remove delay from the digital clock. The receiver's delay was measured as a function of signal level and modulation index with the results shown below. The manufacturer specified the receiver's operating range to be between -100 and -130 dBm. The receiver delay for different modulation index was also investigated.

Input Signal Level	Delay (μs) Modulation Index		
(dBm)	±50°	±60°	±70°
-100		10,874	
-105		10,844	
-110	10,838	10,829	10,814
-115		10,800	
-120		10,748	
-125		10,697	
-130	10,626	10,598	10,576

The delay versus signal level over the full manufacturer's specified range amounted to nearly 300 μs with rather small sensitivity to modulation index. The receiving system variability implies problems when attempting to achieve a 100 μs time synchronization. A change in antenna gain, local interference adding to the receiver's total power input, or receiver gain changes can cause problems. The reason for the receiver's delay sensitivity is believed due to the absence of automatic gain control (AGC). A limiter was used in the second IF only. It must be remembered that this receiver was optimized to enhance an ability not directly related to time recovery. Simple modifications should stabilize its delay considerably.

A discussion of path delay correction will be based on the results shown in figure 18 taken in the same manner as that of figure 16, but using a clock which counts the 100 Hz transitions using only TTL circuitry rather than under microprocessor software control. The resolution of the TTL approach is better than 10 μs whereas the microprocessor, using 4 machine cycles (instructions 1B4 through 1B7), had a peak-to-peak variation of approximately 40 μs. In either case the following discussion is valid. The equipment delay in this case was 46,162 μs, most of this due to the clock using TTL only for 100 Hz transition counting.

In figure 18, at point X, the time interval counter indicates UTC(NBS) - Satellite Clock = 40370 μs. The satellite clock also for point X provides the satellite's position as:

Satellite Longitude	114.92°W
Satellite Latitude	- 0.38°
Satellite Radius	46 μs

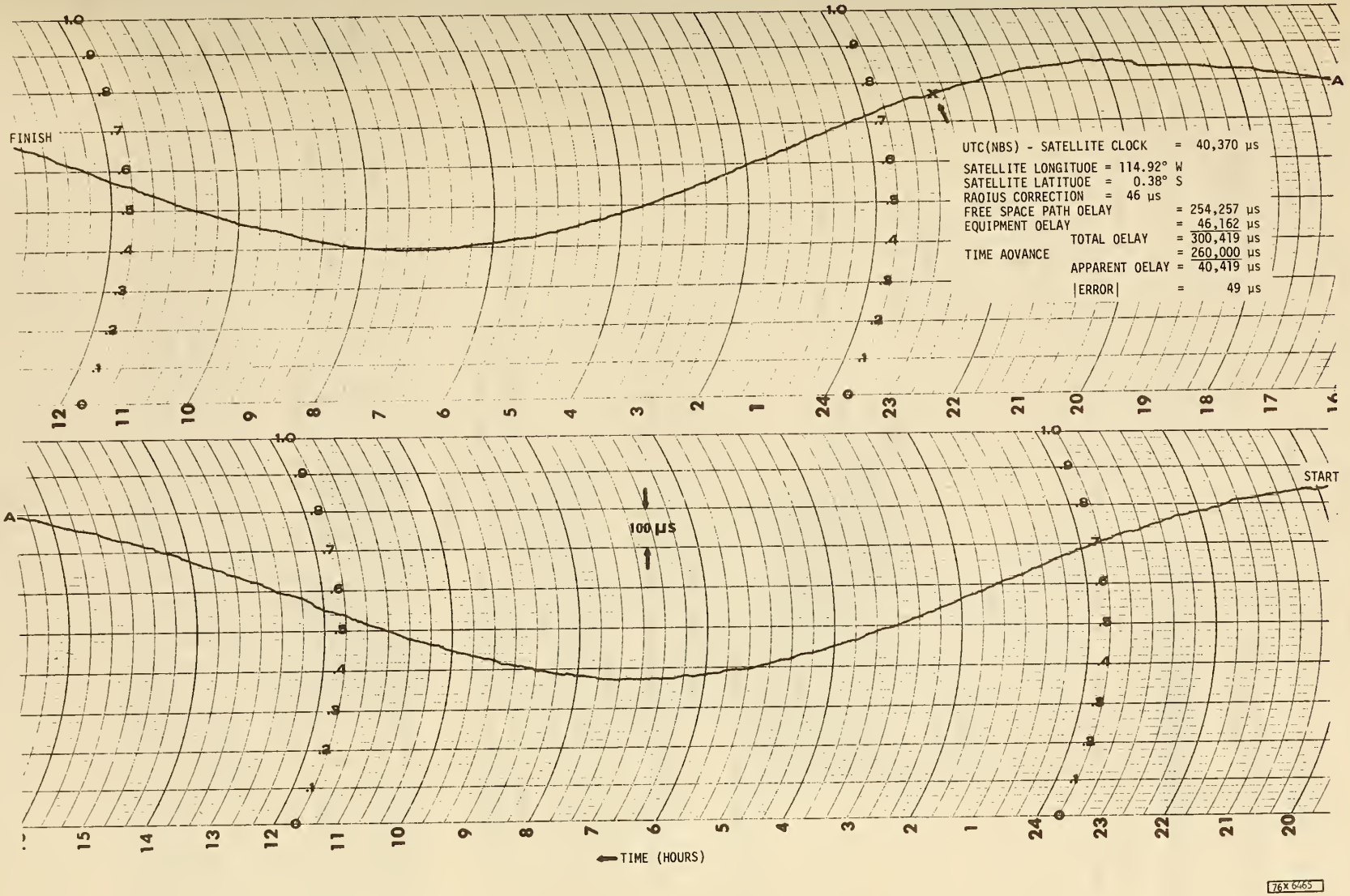

FIGURE 18. UTC(NBS) - SATELLITE CLOCK (TTL)

The coordinates of NBS Boulder, Colorado, and Wallops Island, Virginia, are:

	Longitude	Latitude
NBS/Boulder, CO	105.26°W	40.00°N
Wallops Island, VA	75.46°W	37.85°N

Using the delay slide rule, the path delays are computed to be:

Wallops Island to SMS2	128839 μs
SMS2 to NBS/Boulder	125418 μs
Total Path Delay	254257 μs
Equipment Delay	46162 μs
Total Delay	300419 μs
Time Advance at Wallops Island	260000 μs
Expected Time Difference of Decoder Clock 1 pps and NTC(NBS) UTC(NBS) - Digital Clock =	40,419 μs
The measured value was UTC(NBS) - Digital Clock =	40,370 μs

It is therefore concluded that

Wallops Island - UTC(NBS) = 49 μs

Part or all of this difference can be associated with:

a) Satellite position error
b) Equipment delay error at Boulder
c) Clock error at Wallops Island
d) Equipment delay at Wallops Island (assumed negligible)
e) Ionosphere and troposphere (not accounted for)

4. CONCLUSION

A simple and inexpensive clock has been designed using a four-bit microprocessor which is set and controlled by the interrogation channel of a SMS/GOES satellite. Preliminary measurements show the clock and its associated system to provide a time resolution of better than 40 microseconds and an accuracy better than 100 microseconds. The accuracy is presently limited by the delay uncertainty in the system, mainly the receiver, and by the uncertainty in the satellite's predicted position.

NBS is continuing an effort to reduce and account for all sources of error. A delay stable receiver to reduce the equipment delay uncertainty will be developed in later phases of the program. A potentially more accurate satellite ephemeris generator will replace the present generator and a path delay correcting clock will be developed, as an extension to the basic clock described, to allow for high accuracy automatic time recovery.

5. REFERENCES

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16. ABSTRACT (*A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.*)

A digital clock, resettable and controlled by the time code relayed by NOAA's SMS/GOES Satellites, is discussed. The clock's design is based upon a four bit microprocessor and uses the redundancy of the data to improve its performance. Satellite position is included in the clock's display for delay corrections to the received time.

A discussion of the generation, distribution, and reception of the time code is also included to aid the explanation of the clock's operation and performance.

17. KEY WORDS (*six to twelve entries; alphabetical order; capitalize only the first letter of the first key word unless a proper name; separated by semicolons*)

Clock; microprocessor; satellite; time; time code.

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