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Technical Note 68

TRANSISTORIZED BUILDING BLOCKS FOR DATA INSTRUMENTATION

U. S. DEPARTMENT OF COMMERCE
NATIONAL BUREAU OF STANDARDS

THE NATIONAL BUREAU OF STANDARDS

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Technical Note

68

SEPTEMBER 1960

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J. A. Cunningham and R. L. Hill

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TRANSISTORIZED BUILDING BLOCKS FOR DATA INSTRUMENTATION

by J. A. Cunningham and R. L. Hill

The National Bureau of Standards has developed a number of modular transistorized digital circuits that have been used in automatizing many data recording and preliminary processing tasks encountered in its scientific operations. These versatile building blocks can be connected together systematically to form digital circuits that accept raw data from experimental equipment and transpose these data into a form suitable for input to a high-speed electronic computer. These blocks can be used where: 1) data are produced in large volumes; 2) data taking is extremely fast, extremely slow, or extremely precise; 3) a need exists to minimize human error, tedium and eyestrain; or 4) computation is extensive. This report describes 5 major packages and 8 special-purpose packages.

Each assembly of packages can be tailored to fit the special requirements of the project and can be used at the site of the experiment. The output from the system can be: 1) fed directly to a computer, 2) recorded on a medium (paper tape, magnetic tape, etc.) suitable for computer input at a later date, or 3) used to drive display equipment that keeps the scientist informed of the progress of his experiment.

General System and Package Specifications

The following specifications apply to all packages and to any system built up from them:

1) All major functions may be performed up to 50 kc operating speed.
2) The temperature can range from 0 to 50°C (32 to 122°F).

3) The supply voltages are:
   a) -12 volts (Care should be taken not only in ground distribution but also in ensuring that this voltage appears at the terminals of the package. This supply is usually filtered with an electrolytic capacitor as well as a smaller mylar capacitor that has a lower impedance to high frequency transients).
   b) +12 volts.
   c) other special voltages required for references (analog comparison) and for driving mechanical devices.
4) The digital pulses have:
   a) a minimum range of 0 to -6 volts,
   b) a propagation delay averaging 0.5 μsec,
   c) a 6-volt rise in not more than 1 μsec.

Each package is constructed on a 4" x 5" plug-in printed-board and uses electronic components that are common stock items to avoid replacement problems. Most of the packages contain type 2N414 transistors, and some contain types 2N363 or 2N123 transistors. In most of the packages some components or subassemblies are left unconnected and must be wired externally to the package. Connecting these components externally allows greater flexibility in combining them.

Design Requirements and Considerations

Three factors were emphasized as the main considerations in designing these packages: reliability, cost, and versatility.

Reliability

1) The circuits are designed to permit wide variations from the nominal values of the characteristics and parameters of the components.
2) The majority of the electrical outputs from the packages can be short-circuited to ground or to the negative voltage

supply without damage to any of the components.

3) Pin-type connectors with high-pressure contacts are used rather than printed-circuit edge-type connectors.
4) Signal swings are at least 6 volts.
5) All connectors have gold-plated pins.
6) All back panel wiring is by taper pins for ease and convenience in making external connections. Taper pins also eliminate solder joints.

Economy

1) "Entertainment"-type germanium transistors are used throughout the circuitry.
2) The wide tolerances permit using unselected "off-the-shelf" components. However, transistors and diodes are tested for open or short circuits before assembly into the packages.
3) All connections, including those to the connector, are made by dip-soldering the board.
4) The simplified layout permits mechanized assembly.
5) The board is self-supporting on its connector without special guides in the chassis.

Versatility

1) Two triggering gates are included with each flip-flop circuit to permit connecting the package as either a counter or a register without having to use additional gates from some other package.
2) The bases of the transistors on flip-flop circuits are accessible at the connector so that an unlimited number of additional input gates can be connected.

As product control of transistors appears to improve and then to stabilize over a period of several years after introduction of the type, only those transistor types that have been in long-time production were considered reliable enough for the packages. Thus, future buyers of these types will have reasonable assurance that the parameter

distributions will still be much the same as they were when the types were originally chosen. This consideration removes the need for possible future readjustment of other component values or for radical redesign of the circuitry, as changes in the transistor parameters probably will not occur to any serious extent.

Not only stability of parameter distribution was considered essential, but ready availability and low price of transistors as well. The only transistors that seem to satisfy these requirements are those of the "entertainment"-types that are normally manufactured in large volume by several producers. The circuits were therefore designed to accommodate the wide range in parameters that can occur in these types so that a large yield of useable packages would result. As an example of the wide range of values in only one parameter, current gain, (Fig. 1) shows the distribution of beta for samples of an alloy junction transistor delivered to the Bureau over a period of 4 years.

The packages were designed with the expectation that they would be used only under normal laboratory conditions. These everyday circumstances considerably narrow the range of temperatures (0 to 50°C) over which the transistors would be expected to work. Therefore, germanium transistors were the obvious economical choice.

Two basic types of transistor circuits seemed to have the versatility required for resolving the majority of the Bureau's instrumentation problems. These were a flip-flop with its triggering circuitry and an or-inverter or an and-inverter.

One and-or inverter circuit appeared to satisfy the requirements; thus, only one such circuit had to be optimized, and much original engineering time was saved. Resistor-coupled logical circuits appeared to be too slow for the transistor in this inverter, and direct-coupled transistor logic increased the cost too much. Therefore, diode-coupled circuits were chosen as they provide sufficient operating speed, decrease the number of transistors and widen the operating margins.

The operating speed of the flip-flops consistent with the requirements of instrumentation problems appeared to be less than 100 kc. To operate above this speed, another type of transistor and closer operating margins would be needed. Moreover, the extensive logical fanout and the wide operating tolerances required for the flexibility of these packages make necessary a low operating speed. Therefore, the speed was chosen to be 50 kc. Since the input is a-c coupled this circuit provides the advantage of allowing coupling from external vacuum-tube or transistorized equipment.

To achieve the required degree of versatility, the basic flip-flop circuit makes use of a diode, resistor, and capacitor triggering circuit to satisfy such logical functions as RS, T, and JK.[1/] If the base connection of the transistor is left available for external connection, then external trigger circuits can be added to produce multi-input variations of RST, T, and JK logical functions.

Two 12-volt power supplies were selected for all package circuitry, except for those devices requiring special supplies or for coupling to other circuits. The operating levels are 0 volts and at least -6 volts. With the common Eccles-Jordan circuit, the minus level can swing between -6 and -12 volts depending on the load condition of the flip-flop.

The possibility of using clamping diodes was considered for fixing the voltage levels. However, for maximum reliability, circuits had to be designed that could be over-loaded or short-circuited--conditions under which the diodes would surely fail. Therefore, the decision was made to eliminate the clamping diodes and to let the voltages vary between -6 and -12 volts.

The base connector, shown in Fig. 2, was chosen on the basis of the Bureau's satisfactory experience with it, although a number of other designs are available that would work equally well. The connector contains 25 gold-plated pins, which is sufficient for the number of external connections required by any of the packages. Its strength is

also sufficient to support the etched-circuit board without the aid of guiding supports. The absence of such supports decreases the cost and complexity of the package-holding chassis. The connector may also be plugged into printed-circuit wiring for special applications.

Circuit Design

To facilitate the design of the circuitry, a general medium-speed junction transistor equivalent circuit [2] was developed that is valid for small- or large-signal modes of operation. The equivalent circuit was developed primarily for practical application by the circuit designer. By including the nonlinearity of the base-to-emitter diffusion elements, the circuit is made to respond correctly to driving sources with any value of internal impedance. Solutions for the non-linear differential equations of the equivalent circuit in response to large-signal driving pulses can be obtained from graphical, analytic, or analog computer techniques. The general equivalent circuit is shown in Fig. 3; Figs. 4 and 5 illustrate some results obtained when the equivalent circuit was simulated on an analog computer. This equivalent circuit was used to optimize the two basic circuits of the package series--the flip-flop and the and-or inverter.

One package was developed for each of the five most frequently used circuits. They are:

1) flip-flop
2) and-or inverter
3) trigger or gating circuits for the flip-flop
4) "one-shot" pulse generator, and
5) analog switch.

The Flip-Flop Circuit

The flip-flop package consists of 2 bistable flip-flop circuits and the necessary logical gating for converting each to one of several modes of operation. A normally open switch can be connected to the collector of either transistor to reset the flip-flop. Sufficient circuitry is in each package to construct one bit of a double-rank shift register or two

bits of a serial shift register. The output of the package can drive 5 other flip-flops, 5 or-inverter circuits, 8 gate resistors, or 5 gate capacitors.

The flip-flop circuit shown in Fig. 6 is a modified conventional Eccles-Jordan circuit. The major change was the elimination of both diodes in the cross-coupling network and the parallel resistor to the input of the transistor. These were replaced with a pull-down resistor (R4) to serve as a current source to the transistor base. A further change was an increase in the value of the cross-coupling capacitor (C1). It serves to reduce both the turn-off and turn-on times of the transistor. However, its value cannot be increased too much as it decreases the operating speed or resolution time of the flip-flop and it requires an increased trigger pulse width to change the d-c state of the circuit. An a-c trigger circuit is added to each flip-flop, shown in Fig. 7, to increase the versatility of the circuit. As the transistor base connection of the flip-flop is easily available, additional input triggers can be connected without any practical limitation on their number.

The And-Or Inverter

These packages can be used either as a positive and-inverter or as a negative or-inverter. They contain four separate 4 input inverter circuits. For negative input pulses, the 4 input-diodes function as an or-gate; for positive inputs, the diodes serve as an and-gate. The output of the gate is amplified and inverted. One of these packages can drive 6 other similar packages, 6 flip-flops, 8 gate resistors, or 6 gate capacitors.

The basic 4-input and-or inverter circuit is shown in Fig. 8. Four diodes are connected to a common resistor-capacitor input network. The capacitor C1 serves to reduce the turn-on time of the transistor, and resistor R1 limits the turn-on current regardless of the number of negative input signals.

Resistor R2 speeds up turn-off by removing the stored minority carriers, i.e., by discharging the input diffusion capacitance of the transistor. The values of the collector resistor (R3) and the base resistor (R1) determine the drive or fanout conditions. The desired number of drives, determined by analyzing instrumentation problems, was set at 6. These input-output requirements were used in optimizing the design of the circuit on an analog computer.

The diodes and the resistors, R1 and R2, serve as a bleeder to provide a threshold value for the input signal. This circuit eliminates the need for a current source connected to the base of the transistor.

Depending on the polarity of the input voltages, this circuit will perform either the SHEFFER STROKE or PIERCE functions, which have the property that any switching network can be constructed from either of them alone. For instance, flip-flops could be formed by connecting 2 inverters together. However, these would be d-c coupled and would not have the previously mentioned advantages of a-c coupling that have been designed into the flip-flop packages.

Trigger Or Gating Circuit

The gating package (Fig. 17) contains 8 logical gating circuits consisting of resistor-diode networks with capacitor inputs. They are mainly for supplementing the gates in the flip-flop packages to complete the component requirements of shift registers, counters, or other systems. They can transfer information from a shift register or form feed-back paths in various counting configurations. These gates can be driven by the output of a flip-flop, a "one-shot" pulse generator, an or-inverter, or a power driver.

The component values of the trigger circuit depend on two considerations. First, the RC time constant for charging the capacitor limits the maximum speed at which the flip-flop can operate. It also determined the input requirements to change the d-c state of the flip-flop. Second, the performance of the flip-flop is affected by two parameters of the input signal--the input amplitude and its rise time.

Fig. 9 shows a curve of input signal amplitude (at a constant rise slope of 6 volts per μsec) required for switching 114 flip-flops. The component values and tolerances determine both the slope and the horizontal position of this curve. Values were chosen so that the curve would fall in the position shown in Fig. 9.

One-Shot Pulse Generator

The pulse generator (Fig. 10) can deliver a single pulse whose duration is variable from 10 to 10,000 μsec. Regardless of the duration of the pulse, the circuit is prepared to generate a new pulse 20 μsecs after the termination of the first pulse.

This package consists of a flip-flop identical to the one in the flip-flop package, together with an integrator, discriminator, and an amplifier. After the flip-flop is triggered, its output is integrated. When this integrated signal reaches a predetermined level, the discriminator is triggered. Its output is differentiated, amplified, and inverted, then differentiated again before being fed back to reset the flip-flop. The circuit can be connected so that it will either turn itself off or be turned off by an external signal before its pre-set time is up.

The output of the package, which can be either positive or negative, has the same driving capabilities as the flip-flop package. Although this circuit is made up from a standard flip-flop plus an integrator, comparator, and amplifier combination, which is rather expensive, most systems use so few that its cost is not important.

Analog Switch

The analog switch package (Fig. 11) contains a flip-flop that controls an electronic single-pole two-position switch that connects the output to ground or in the opposite state to an analog input voltage that may range from minus to plus 10 volts. The analog switch is essentially a single-pole, two-position switch which seems to meet the majority of instrumentation needs. A group of these switches can make a commutator, a distributor, or a digital-to-analog converter of any of several types. With the analog voltage comparator package described

in the appendix, this can be made into an analog-to-digital converter of the ramp, count-up-count-down, or bit-by-bit types.

The switch can pass analog voltages between plus and minus 10 volts, and is able to pass these voltages within 5 millivolts of the input. This tolerance makes possible converters that have 0.1% accuracy, which is equivalent to the least significant of 10 binary digits.

Other Packages

From time-to-time, it has been necessary to devise other special-purpose packages to meet the special requirements of some instrumentation problem. These packages include

1) magnetic drum (or tape) read circuit
2) magnetic drum (or tape) write circuit
3) amplifier for driving mechanical devices
4) power gate driver for large parallel-drive applications
5) decimal decoding circuit
6) octal or hexadecimal decoding circuit
7) pulse generator circuit
8) voltage comparator circuit
9) indicator circuit (This circuit can drive 10 incandescent bulbs rated at 12 v, 18 ma, or electromechanical equipment within the power limits of its 2N363 transistors.)

Details and specifications on all of these packages are included in the appendix.

Package Tester

A Universal Package Tester, shown in Fig. 12, was built around a punched-card controlled switch. A different punched-card for each of the packages properly sets up switch connections inside the tester, thus making possible the testing of any existing or future packages. The block diagram is shown in Fig. 13.

Engineering Applications

The Bureau has used these packages in a number of combinations to solve a variety of instrumentation problems. The following is a list of some applications drawn from the Bureau's experience:

1) nucleonic instrumentation needs, such as preparation of printed copy and punched-paper tape from pulse height analyzers and scalers.
2) logical control and decoding for a high-speed printer.
3) control and logical functions of a rapid film reader.
4) reading and decoding punched-paper tape to control an X-Y plotter.
5) preparing punched-paper tape and printed copy from an automatic device for measuring characteristics of transistors.
6) automatic data distributor for high-speed teletype system.
7) analog-to-digital and digital-to-analog converters (10 bits).
8) most of a digital differential analyzer.
9) digital time clocks for display and control functions.
10) special-purpose computer with drum memory for the Weather Bureau's rotating-beam ceilometer (shown in Figs. 14 and 15).

Conclusion

Approximately 2,000 packages have been supplied to the Bureau by contractors. Unselected components were used except for the diodes and transistors. The reverse voltage of the diodes was checked and an open or short test applied to the transistors.

Yield of useful packages has been high. Upon receipt of the packages, the flip-flops were subjected to 2 tests--d-c stability and input trigger sensitivity; the yield was better than 98%. All other types of packages have had similar yields. Including rejects and costs chargeable to final testing, the average cost per package has been less than $30.00.

The reliability of the packages can be determined only from their performance in various applications for a long period of time. In the first year of use, no packages failed because of component drift. Two out of 10,000 transistors failed for unknown reasons, and several more from mishandling by technicians. All of these failures have been in equipment during the initial troubleshooting phase; no failures have occurred under operating conditions, although the equipment has been in use over one year.

1/ Montgomery Phister, Jr., "Logical Design of Digital Computers," Chapter V, John Wiley and Sons, Inc., New York, 1958.

2/ S. Geller, P. Mantek and D. Boyle, "A General Junction Transistor Equivalent Circuit for Use in Large-Signal Switching Analysis," submitted to the Proc. of the IRE.

APPENDIX A

Detailed Building Block Descriptions

Physically, each package consists of a 4" x 5" etched-circuit board of single-clad XXXP phenolic laminate with a 25-pin right-angle connector soldered to one end of the board. This connector plugs into a socket having two taper-pin receptacles for each of the 25 contacts.

Components used throughout the circuitry are all stock (or off-the-shelf) items and are, therefore, readily available. The majority of the packages, except the indicator and a portion of the analog switch, utilize type 2N414 transistors. Type 2N363 transistors are used in the indicator package. Type 2N123 transistors are used as a voltage switch in the analog switch packages.

Flip-Flop

This package consists of two bistable flip-flop circuits (Fig. 7) plus logical gating necessary for converting each to either RS, JK, or T type flip-flops. In normal use, the diode of each half of the trigger circuit is connected to the base of its respective transistor. To be used as an RS-type flip-flop (Fig. 16-a), one of the input capacitors is used as an R input for resetting the flip-flop to "zero" state; the other is used as an S input to set it to the "one" state. A JK-type flip-flop (Fig. 16-b) would be connected in the same manner with J as the set and K as the reset input. For use as a T-type (Fig. 16-c) both input capacitors would be connected to form a single input. The polarities shown in the logical symbols (Fig. 16) indicate the level of either output of the flip-flop in its zero state. To facilitate connection of the desired type of flip-flop each of the gating inputs is brought out to a connector pin. To operate as an RST-type flip-flop, additional gating may be obtained from a gating package which can supply gates for either the RS or T function. Thus, a flip-flop may serve as a multi-input circuit.

The emitter of each transistor is normally grounded, but in the package each emitter is brought out to a separate pin (6, 8, 18, 20) so that provisions may be made for manually resetting the flip-flops by

opening the proper emitter-ground circuit with a normally closed push-button switch. Also, non-saturating circuitry may be constructed by the addition of an RC network between each emitter and ground.

Gating Package

Eight gating circuits are contained in each package (Fig. 17). These gates are used primarily to supplement those of the flip-flops when wiring shift registers, counters, etc., or they may be used for transferring information from a register. Also, the gates may be used as feedback paths for producing various counting configurations.

These gates may be driven by the output of a flip-flop, one-shot, or-inverter, or power driver. A schematic diagram plus the logical symbol for a gate circuit is shown in Fig. 18. Normally, the resistor is connected to a d-c signal, the capacitor to a pulse or a d-c signal, and the diode to the base of a flip-flop transistor. Thus, a positive d-c signal on the resistor with a positive going pulse on the capacitor provides a pulse which turns off the transistor to which it is connected, thereby causing a negative signal on the transistor collector. The driving pulse to the capacitor must always be positive with an amplitude of six volts or greater and a rise time of not more than one microsecond.

One-Shot

This package (Fig. 10) consists mainly of a flip-flop circuit identical to that of the flip-flop package, an integrator, a discriminator, and an amplifier. After the flip-flop is triggered by a positive pulse to pin 1, its output is integrated. When this integrated signal reaches a predetermined level the discriminator is triggered. Its output is differentiated, amplified and inverted, then differentiated again before being fed back to reset the flip-flop. Inputs 1 and 11 may be connected to insure placing the flip-flop in the correct state. This mode (T-type) of operation is preferred, however, it is optional. The trailing edge of the negative output of this package may be differentiated and used as a delayed trigger for other circuits.

The standard package is capable of generating a single pulse with a duration which is variable from less than 10 microseconds to beyond 10,000 microseconds. Socket pin connections (pin 12 and ground) are provided for modifying the package by adding additional capacitance with which a maximum pulse duration of up to approximately one second may be obtained. Regardless of the duration of the pulse being generated within the above limits, the recovery time of this circuitry is approximately 20 microseconds; that is, 20 microseconds after the termination of any pulse the circuit is prepared to begin generation of a new one. Coarse control of the pulse duration, 10-10,000 microseconds, is achieved by grounding of the appropriate capacitor (C_1, C_2, or C_3, respectively). The 1K miniature potentiometer is used for fine control. A positive or negative output is obtainable and, like the flip-flop package, it is capable of driving 5 flip-flops, 5 or-inverters, 8 gate resistors, or 5 gate capacitors.

And-Or Inverter

Each of these packages (Fig. 19) contains four separate four-input inverter circuits. For negative input pulses the four-input diode gate performs a logical or-function, but for positive inputs the diodes perform a logical and-function. The output of the gate is fed into an amplifier and inverted.

For example, if a negative voltage is assumed to be a binary one and a positive voltage a binary zero, then the application of a binary one on any input will result in a positive voltage at the output. In like manner, when a positive voltage is assumed to be a binary one and a negative voltage a binary zero, then all inputs must be positive, or binary ones, to obtain a negative output voltage. With these circuits properly connected in series, the function performed may be and-or-and-or-etc.

Approximately 0.5 microsecond is the average pulse propagation time through one of these circuits. An inverter circuit is capable of driving six similar inverter circuits, six flip-flops, eight gate

resistors, or six gate capacitors. The logical symbols used for these circuits are shown in Fig. 20.

Analog Switch

This package (Fig. 11) contains one standard flip-flop which controls an analog switch capable of switching an analog voltage (pin 17) of up to plus or minus 10 volts within 5 millivolts of the input. By proper selection of the resistance (R_1 and R_2 plus the potentiometer) at the output of the switch, an analog presentation may be obtained for a quantity or digit represented by it. A miniature potentiometer is used as a trimmer for fine adjustment of the output weighting resistance. For normal operation, pins 6, 8, 16, and 22 are grounded; pin 3 is connected to pin 5; 7 to 10; 4 to 19; 9 to 21; and pin 1 to pin 11 for the input. Pins 15, 23, and 25 are left floating and the remainder of the package is connected as indicated on the schematic diagram.

Analog Voltage Comparator

This package (Fig. 21) is used to compare an unknown voltage input (pin 21) with an analog voltage (pin 17), both of which are related to ground. The critical point of this comparison is stable to within 3 millivolts. An output pulse is produced when the analog voltage input is more negative than or equal to the unknown voltage (V_x). If there is an output it should appear within 3 microseconds. Transistor T_1, in the blocking oscillator remains in the cut-off state when its base-emitter voltage (V_{be}) is positive, but oscillation begins when this voltage becomes negative by approximately 0.1 or 0.2 volt. An oscillating condition exists when $V_x \geq V_a$. With $V_a = V_x$ the balance control is adjusted until the blocking oscillator is at the brink of oscillation. This insures that the forward voltage drop across the emitter-base diode of transistor T_1 is not added to V_x. Transistor T_2 is an amplifier for producing a positive output (pin 1) referred to the system ground. Oscillation ceases and, therefore, comparison is inhibited whenever a positive input pulse is applied at pin 15.

The $\pm$V (12 volts) supply of the comparator is floating and separate from the collector voltage ($-V_{cc}$) supply for the output amplifier which is related to ground. This enables the generation of full voltage output pulses for differences as low as 10 millivolts between V_x and V_a. With $V_a > V_x$ the input impedance (Z_{in}) is fairly high, but for $V_a \leq V_x$, Z_{in} is relatively low.

Decimal Decoder

The function of this package is to take the outputs of a binary decimal counter, of either the 8-4-2-1 or 4-2-2-1 type, and furnish an output for each of the counter's ten states to drive some type of visual decimal indicator, such as lamps, a projection-type decimal readout, a nixie, etc. No. 344 incandescent lamps may be driven directly from the decoder package, or, by leaving out the collector resistors, the package may drive relays which in turn operate mechanical devices. Connections for each type of counter are shown in the schematic diagram (Fig. 22).

Octal-Hexadecimal Decoder

This package may be used singly for decoding an octal counter by using the three inputs designated A, B, and C (weighted 4, 2, 1 respectively) and their complements. To decode a hexadecimal counter, two packages are used, one for the outputs 0 through 7 and the second for 8 through 15. Inputs for this case are designated A, B, C, and D (8, 4, 2, 1) and complements thereof. The 0-7 package will have one $\bar{A}$ connection common to all gates and the 8-15 package one common A connection to all gates. The connections for B, C, D, and their complements, as shown in Fig. 23, would be used for A, B, and C, respectively when decoding an octal counter.

Power Driver

The power driver package (Fig. 24) is composed of two units and used primarily for driving gate circuits which in turn are used for transferring information from one flip-flop to another or for resetting flip-flops. Each unit is capable of controlling up to 20 gate circuits.

The two inputs to a power driver must be of opposite phase and may be provided by a flip-flop, a one-shot, or an inverter package. In normal use pin 9 is connected to pin 2 ($-V_{cc}$). A precaution that must be observed is that neither ground nor -V should be applied at the output of these circuits. The result would be certain failure of an output transistor.

Indicator

This package (Fig. 25) contains driver circuits for ten G. E. No. 344 incandescent lamps which draw approximately 18 ma at 12 volts. These circuits use a type 2N363 general-purpose audio frequency transistor which has a maximum voltage rating of 40 volts with a power dissipation of 168 milliwatts. In addition to driving indicator lamps this package may also be used to drive electromechanical devices if their requirements are within the above limits.

The logical symbol for an indicator connected to a flip-flop is also shown in Fig. 25. In normal use the indicator is turned on when the side of the flip-flop to which it is connected goes negative.

Read Package

The read package is used for converting digital input signals, of approximately 0.3 volt peak and alternating polarities, from a magnetic drum or tape, to standard (12 volt) negative output pulses. This circuit is normally used with non-return-to-zero type recordings but could be adapted to other types. Positive output pulses with less than one microsecond rise time for triggering flip-flops, etc., may be obtained by passing the output of the read package through an or-inverter stage. A schematic diagram of the circuit is shown in Fig. 26. The 100-ohm balancing potentiometer is adjusted until equal-amplitude pulses are obtained at test point no. 5. In its present application this package is used with a Brush BK110 head.

Record Package

The record package is used to drive a read-write head for recording on a magnetic drum or tape. It has been used for non-return-to-zero

(NRZ) recording, but should be equally suitable for rectangular-pulse recording. The circuit is designed to drive a center-tapped winding for producing saturation of the magnetic medium in either direction. This package has been used satisfactorily with a Brush BK 110 head. With such a head, reversal of the flux requires about 100 microseconds. The required saturation current, which may be adjusted with the 500-ohm potentiometer, for the same head was approximately 30 milli-amperes. The and-inverter, or-inverter, and flip-flop, shown with the schematic diagram of the circuit in Figure 27 demonstrate a method of using the package for NRZ recording.

Pulse Generator Package

This package, Fig. 28, consists of a free-running blocking oscillator, a transformer-coupled amplifier, and a flip-flop. The blocking oscillator operates at a variable frequency determined by the adjustment of the 200K potentiometer. A frequency range of 10Kc to 100Kc may be obtained by using the component values as shown with a -12 volt collector supply. By changing the value of the .005 mfd capacitor and the potentiometer, the frequency range may be extended from a few cycles per second to beyond 100Kc. If desired, an output pulse may be taken directly from the blocking oscillator transistor (pin 16). However, when more drive is required the amplifier output (pin 22) may be used.

The flip-flop included in this package is of the standard type with pin connections identical to those of the lower-numbered half of the flip-flop package.

APPENDIX B

Transistorized Building Block Package Tester

An instrument is available for testing the five major types of packages, and contains provisions for testing others, if desired. Fig. 12 is a photograph, and Fig. 14 is a block diagram of the tester. The circuitry is fully transistorized using type 2N414 transistors except for a type 2N363 in the output indicator. The nucleus of this tester is a Hickok Cardmatic Switch. When there is a blank card in the switch, which is spring-loaded, all pins along a bus are interconnected. Inserting a card, with selected holes punched, trips a solenoid which activates the switch and allows the undesired pins along each bus to be released. This switch greatly simplifies the testing procedures and increases the versatility of the instrument. The switch has been modified to provide 33 bus lines instead of the original 11, with a minimum of 5 external contacts for each bus. Each pin of the test package socket is connected to one or more of these contacts. Also, connected to particular contacts are the input and output selector switches plus the output load switch and the indicator lamps.

Fig. 29 is a diagram of the layout of a switch card. The number or letter within a circle designates a pin number of the test package socket, rotary switch contact, or an indicator lamp which is connected to a particular card switch contact.

A notation along the bus line (-V, +V, etc.) designates the function of that group of contacts. To utilize a card switch contact, the card is left unpunched for that particular position. For example, in an indicator package only 24 is grounded. Therefore, all circles along the 3 ground buses (D, E, and F, 11 through 16) will be punched out except the circle at location E-16.

A test signal with adjustable amplitude (3 to 8 volts) is provided by a standard flip-flop (Fig. 30) triggered by blocking oscillator (Fig. 31) that free-runs at 50Kc (high) or 20 cps (low). Alternatively, the oscillator may be triggered by a Schmitt circuit (Fig. 32) to provide

a single-pulse signal. The input test signal is available at the front panel to be observed and/or used for sync purposes. The desired input pulse repetition rate may be selected manually with the rotary switch so labeled. This input signal is normally fed into all inputs of a package, but for an or-inverter package the input is switched among the input diodes by the input selector switch (Fig. 33). Each output of the package may be selected for observation by the output switch (Fig. 34). The output signal may be observed either with no load or with a maximum design load of simulated flip-flops or or-inverters selected by the output load switch (Fig. 35). The output is normally observed on an oscilloscope, but an output indicator lamp (Fig. 36) is provided to permit quick check with a single pulse or low frequency input.

Power requirements for the tester are 110 volts a-c for the card switch solenoid, +12 volts at approximately 50 ma, -12 volts (greater than 300 ma when indicators are being checked), and for Analog Switch packages, a reference voltage source (for quick checks -12 volts may be used).

General testing procedure is as follows:

1) After connecting power sources, insert the Hickok switch card which has been punched to correspond with the package to be tested. Packages are color coded with a strip of colored tape along the top edge according to type, and the switch cards are coded to match.
2) Set repetition rate control to desired test frequency.
3) Adjust amplitude of input signal while observing it at the test signal terminal with an oscilloscope. This is normally set at 6 volts.
4) Select desired load condition with load selector switch.
5) Insert package which is to be tested.
6) The output waveforms of the package may now be selected by the output switch and observed at the output terminal with an oscilloscope. For merely determining whether or not an output is

produced from a package, at low rep. rate or single pulse, the output indicator lamp may be observed.

Additional testing details which apply specifically to particular packages are described below.

Flip-Flop

For testing purposes the flip-flop package is connected as two T-type flip-flops with a common input. The exact pulse amplitude required for triggering each circuit may be determined by observing the test signal while increasing the input amplitude until the flip-flop is turned on.

The output switch is used to select either side of each flip-flop (1 and 2 for flip-flop A, 3 and 4 for flip-flop B). Using the load selector switch the output may be loaded with either five flip-flop or five or-inverter circuits.

Gating

The Gate package is tested by connecting the eight gate circuits in 4 pairs which may be selected with the output switch. Through this switch these gates are fed into a standard flip-flop which is built into the tester. Normally, the test signal amplitude is set at six volts and the load selector at zero. For properly operating gates a flip-flop output will be observed at the output terminal.

One-Shot

The One-shot package is normally tested at the low repetition rate or with a single pulse input of six volts amplitude. One of the three integrating capacitors must be grounded through the input selector switch at position 1, 2, or 3 (pins 17, 19, and 21 respectively). A negative output pulse may be observed with output switch in position 1 or a positive pulse at position 2. Available output loads are zero, 5 flip-flops, or 5 or-inverters.

And-Or Inverter

The input selector switch is used to select one of the four input diodes of each of the four circuits and the output switch is used to select one of the four circuits (inverter transistors). Available output loads are zero, 6 flip-flops, or 6 or-inverters.

Analog Switch

To test the Analog Switch package it is necessary to provide a reference voltage supply in addition to the normal plus and minus 12 volts. However, for a quick check the -12 volt supply may also be connected to the reference voltage terminal.

For testing purposes the package is connected with pins 4 to 21, 9 to 19, and 22 grounded. The flip-flop is connected as a T-type. With the output switch in position 1 the output waveform at pin 20 may be observed.

Indicator

The Indicator package is normally tested with either low repetition rate or single pulse input. Its operation is determined by observing the row of 10 indicator lamps (Figure 37) at the top of the tester, which are triggered by the indicator package. To test this package the -12 volts source must be capable of supplying 0.35 amps.

Power Driver

Complementing inputs are provided for both circuits of the Power Driver package. The output of either half may be observed by selecting output switch position 1 or 2. A simulated load of 20 flip-flop circuits may be introduced at the output with the load selector in flip-flop position.

APPENDIX C

Figures 38 through 50 are illustrations of etched-circuit layouts, for the various types of packages, with components and their values. In each the component side of the board is shown.

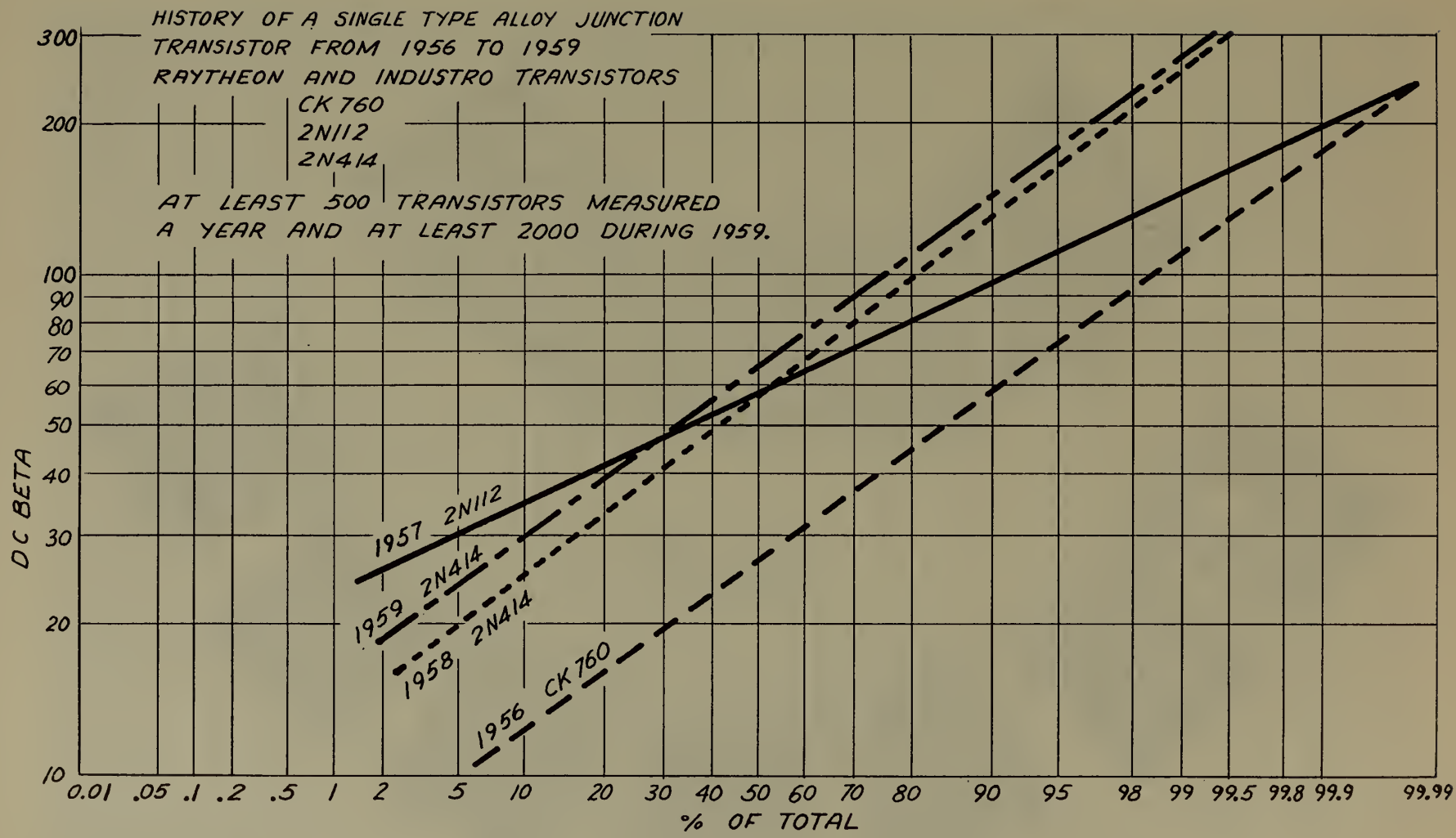


Figure 1. Normal Distribution of Current Gain for a Single Type Alloy Junction Transistor.

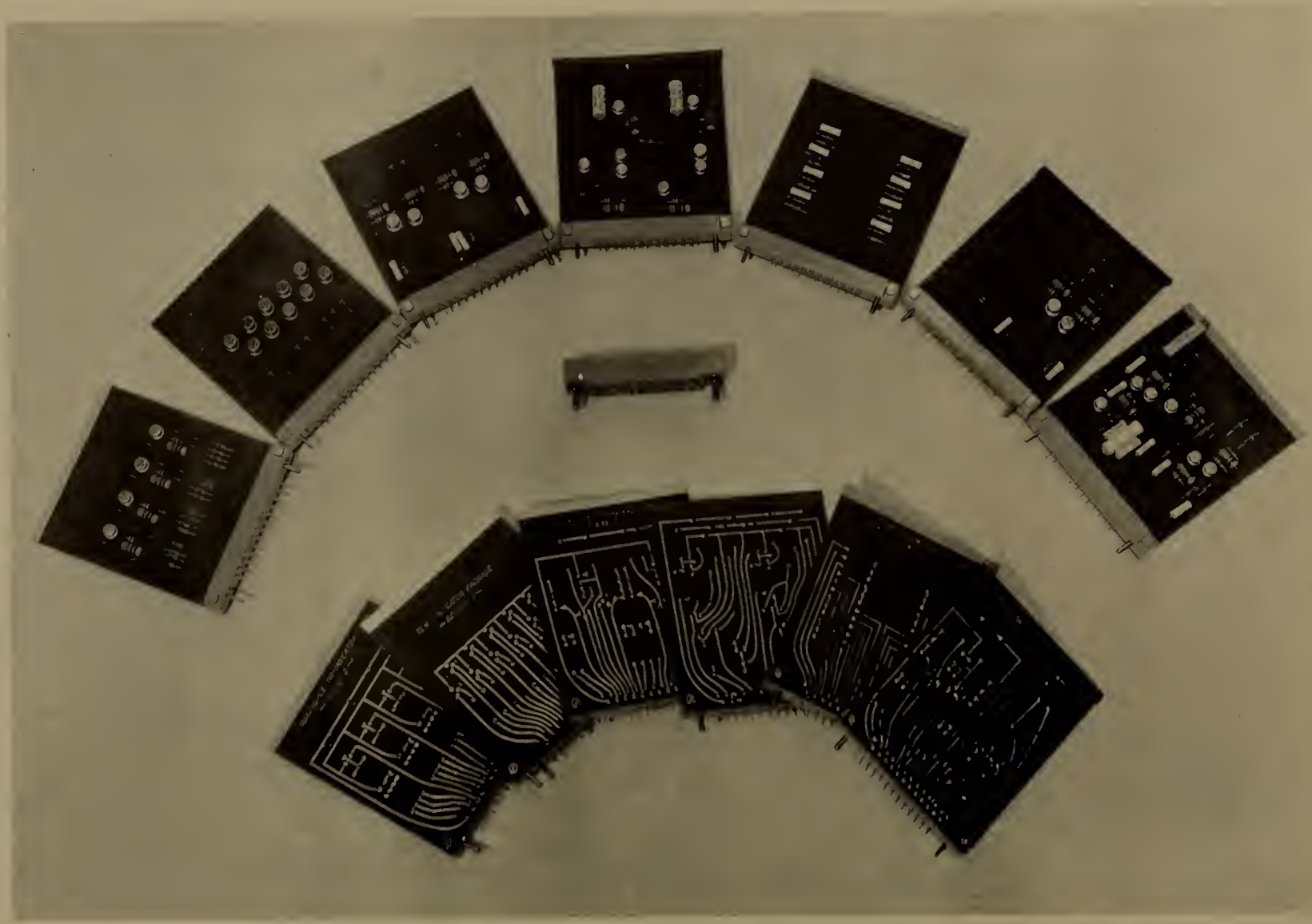
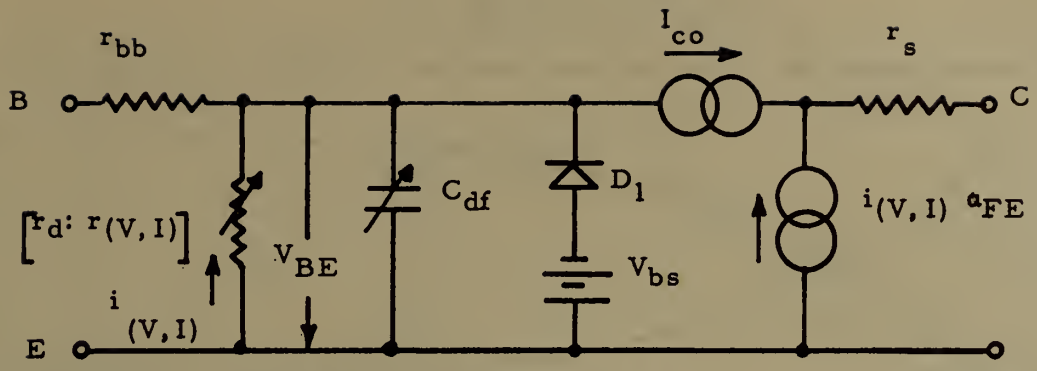
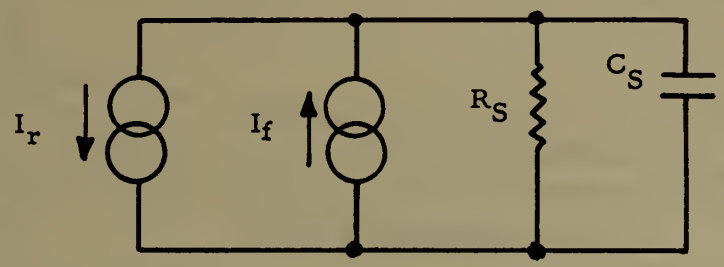


Figure 2. Transistorized Logical Building Blocks.



General Transistor Equivalent Circuit
(Common Emitter Mode)



Storage Time Section

REQUIRED MEASUREMENTS:

$T^*_B = r_d \times C_{df}$; Inverient Time Constant Factor.

V_{BE} vs I_B = Static Base To Emitter V-I Characteristic. Represented by $[r_d : r_{(V,I)}]$ Element.

$K_S = R_S C_S$. Storage Time Factor.

r_S = Collector Saturation Resistance.

α_{FE} = D-C Short Circuit Current Gain.

r_{bb} = Extrinsic Base Resistance.

I_{CO} = Collector Reverse Saturation Current.

Figure 3. A General Equivalent Circuit of an Alloy Junction Transistor.

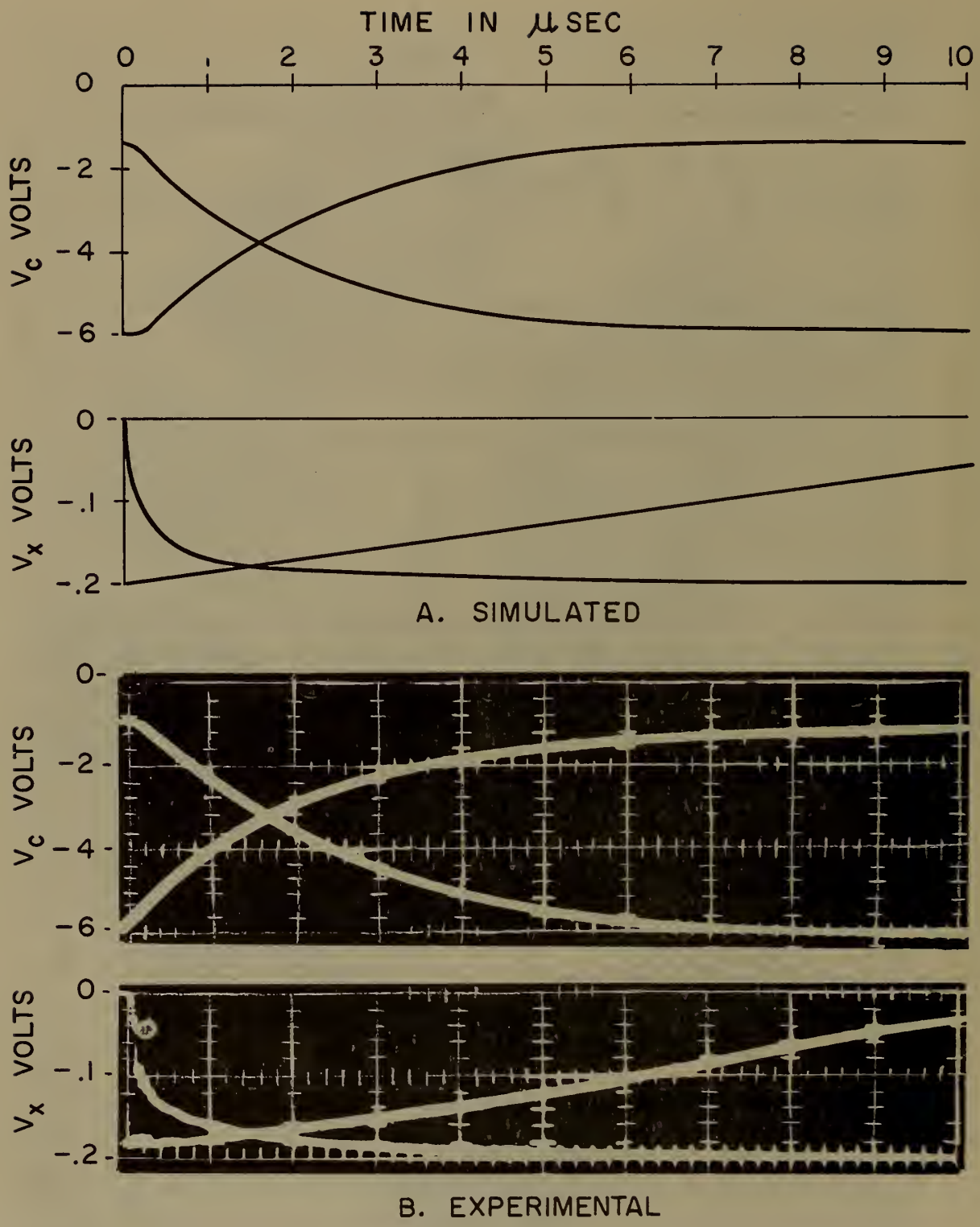


Figure 4. Analog Simulated Results with Experimental Oscilloscope Traces. (1st Case)

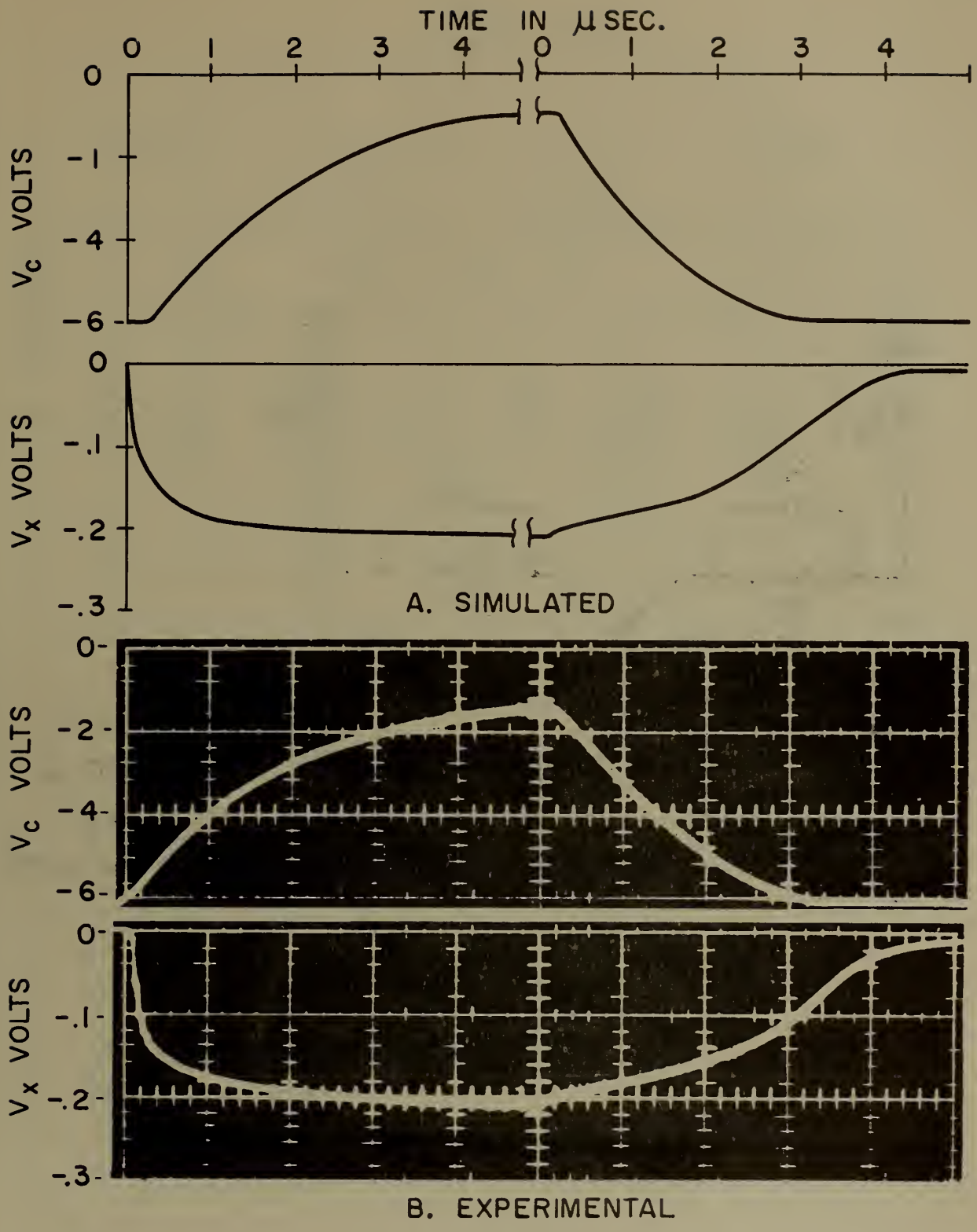


Figure 5. Analog Simulated Results with Experimental Oscilloscope Traces. (2nd Case)

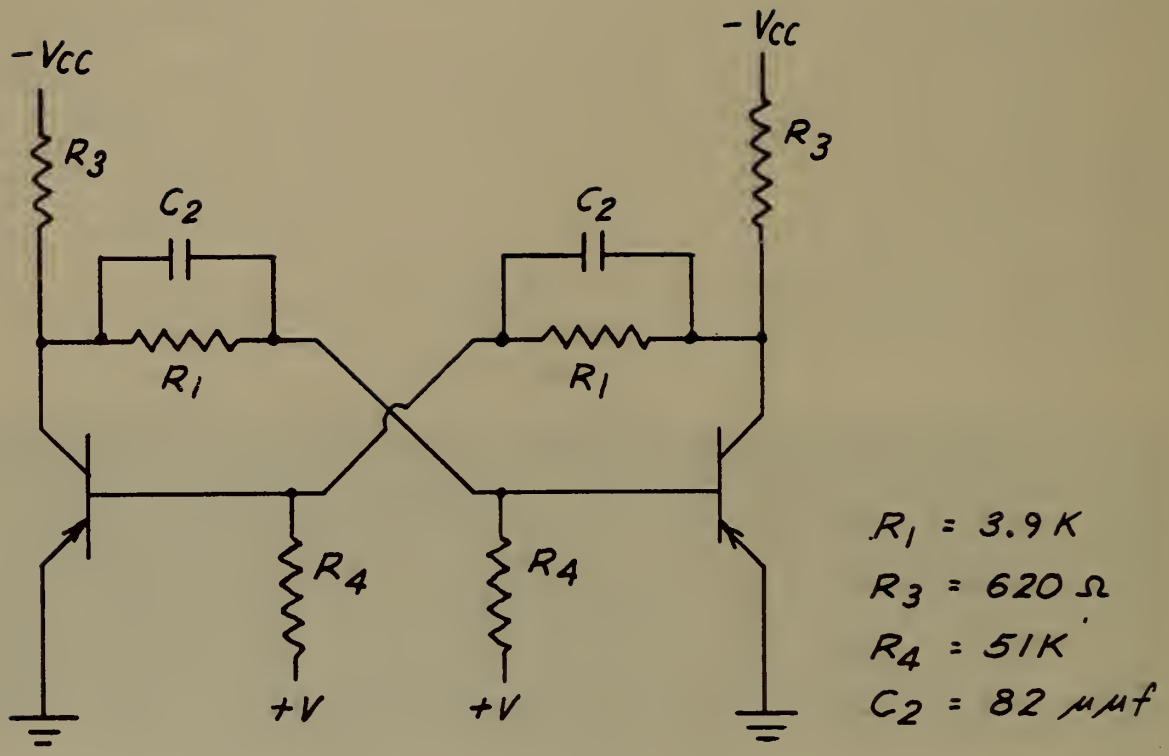
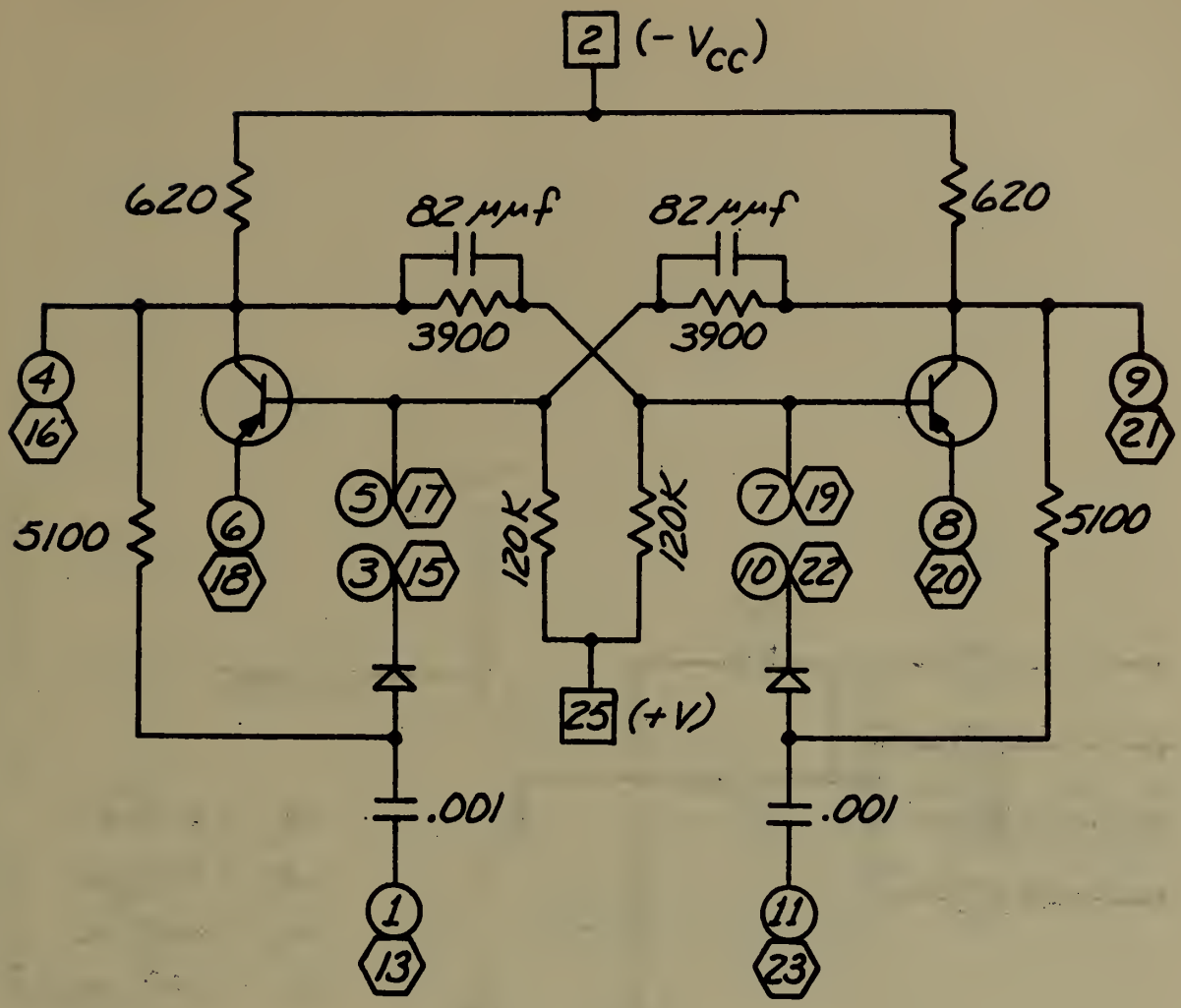


Figure 6. Basic Flip-Flop Circuit.



○ = FLIP-FLOP A

⬡ = FLIP-FLOP B

□ = COMMON TO BOTH FLIP-FLOPS

TRANSISTORS : 2N414

DIODES : DR435

TWO CIRCUITS PER PACKAGE

Figure 7. Flip-Flop with A-C Trigger Inputs.

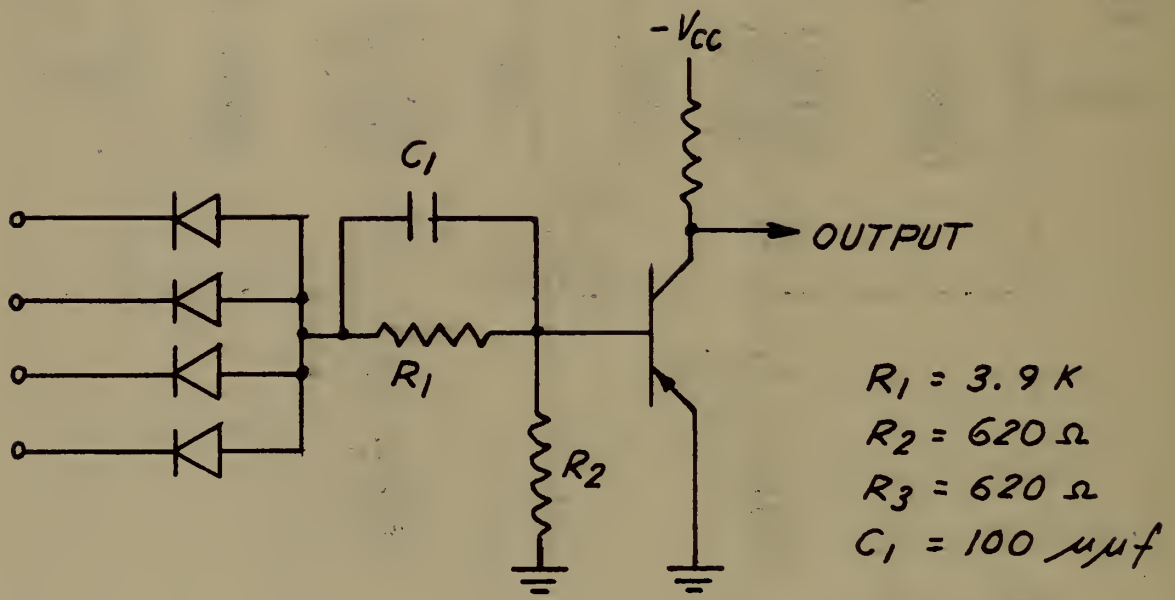


Figure 8. A Four Input And-Or Inverter.

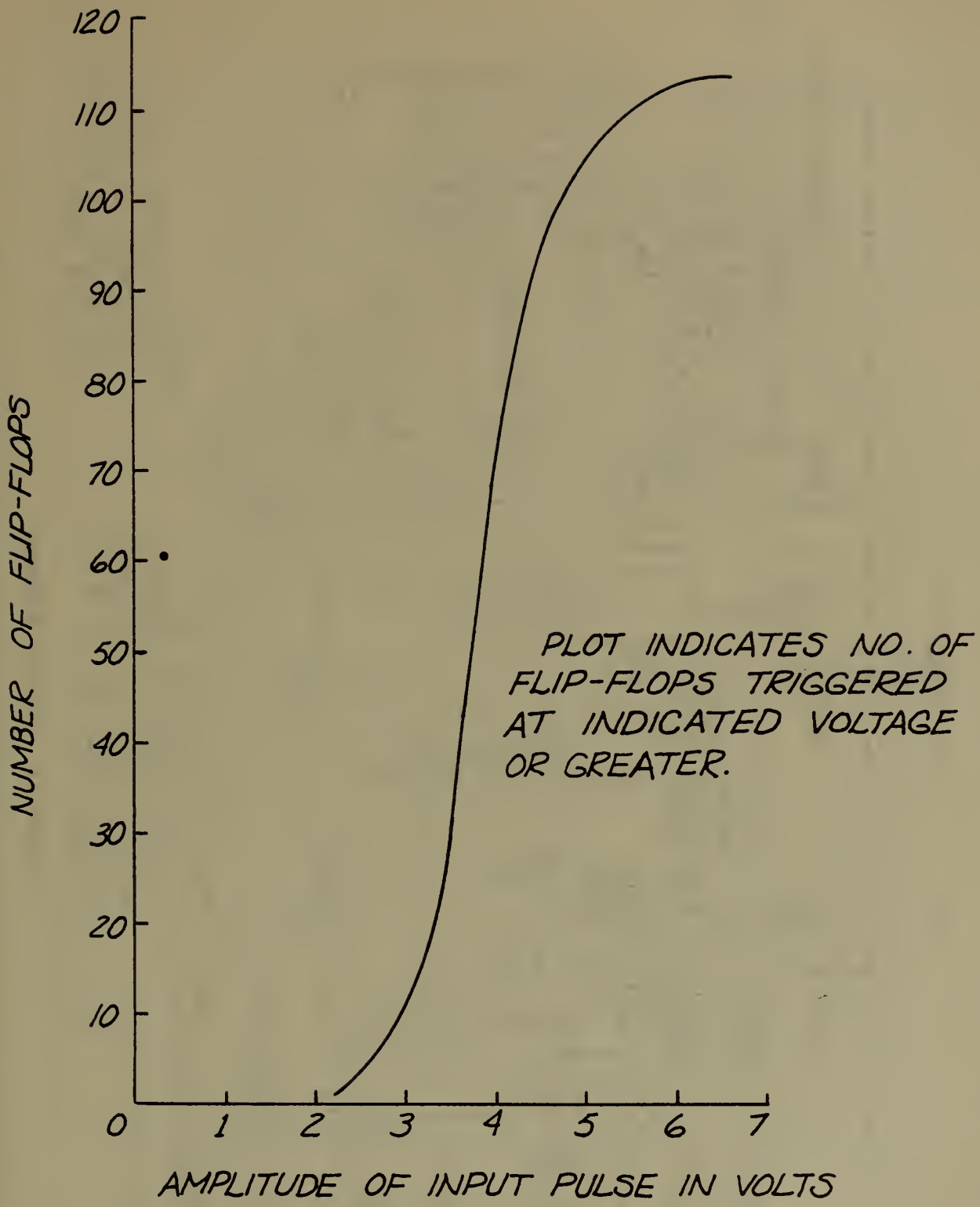


Figure 9. Input Characteristic of Flip-Flops.

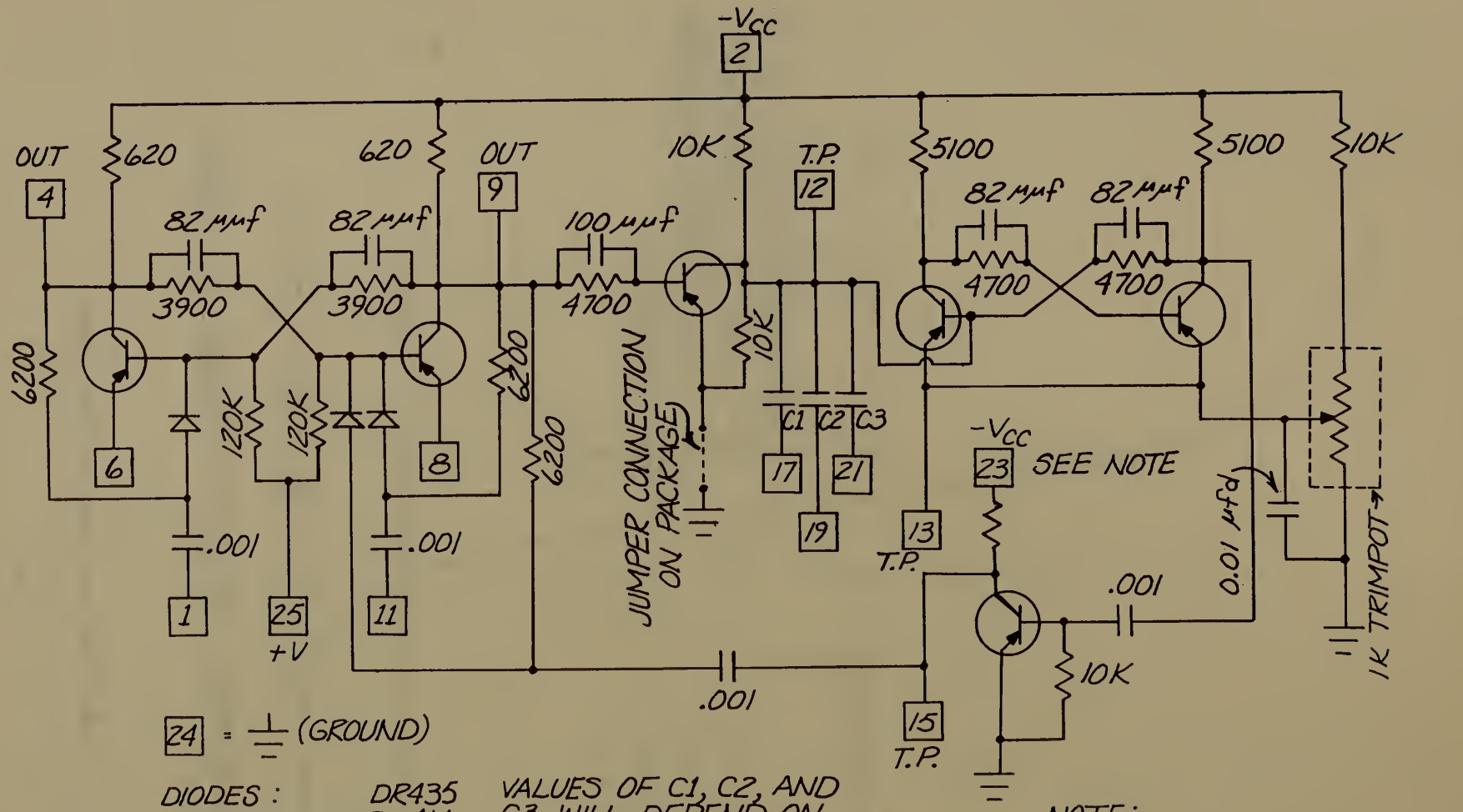


Figure 10. One-Shot Package.

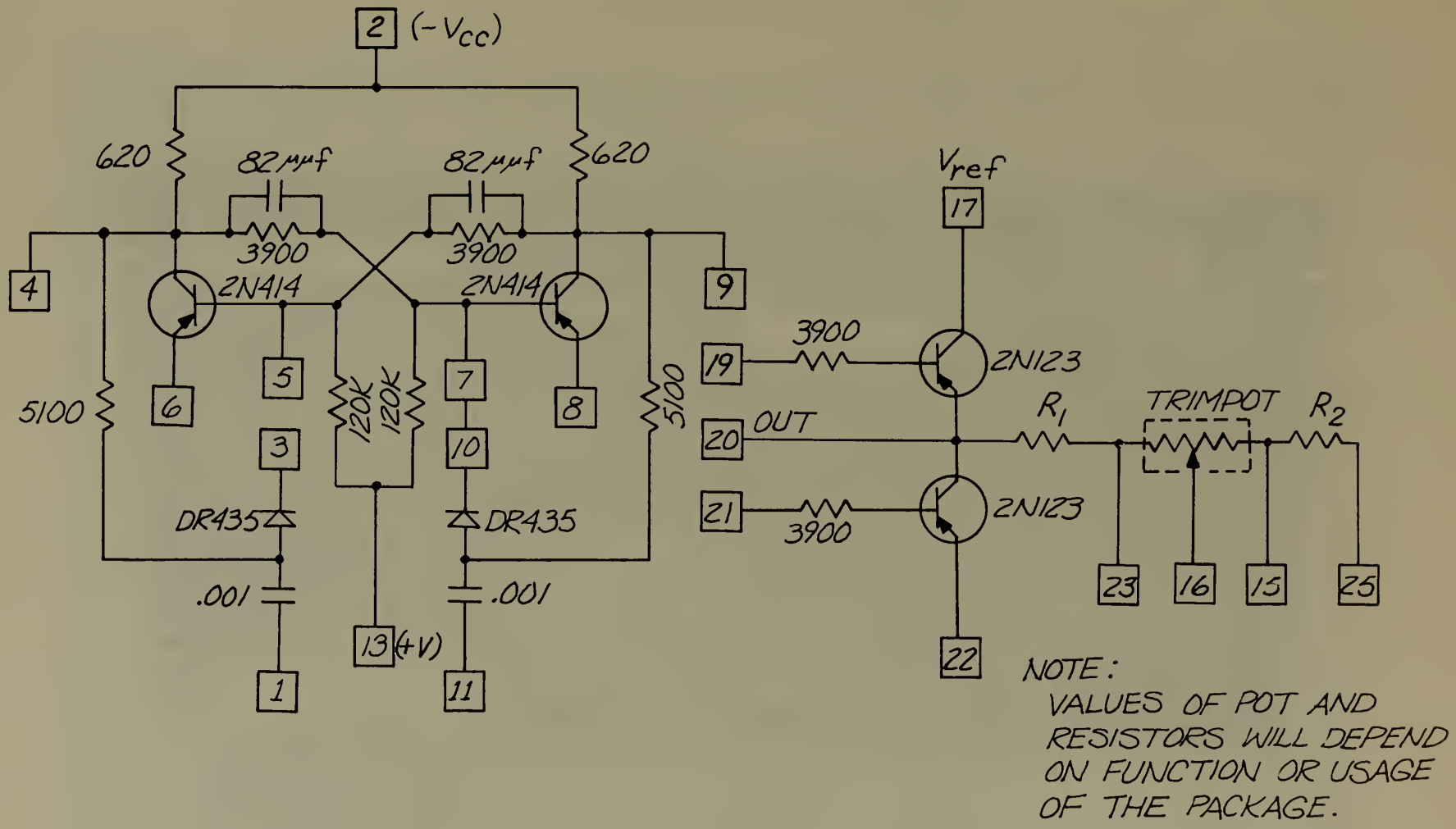


Figure 11. Analog Switch Package.

Figure 12. Building Block Package Tester.

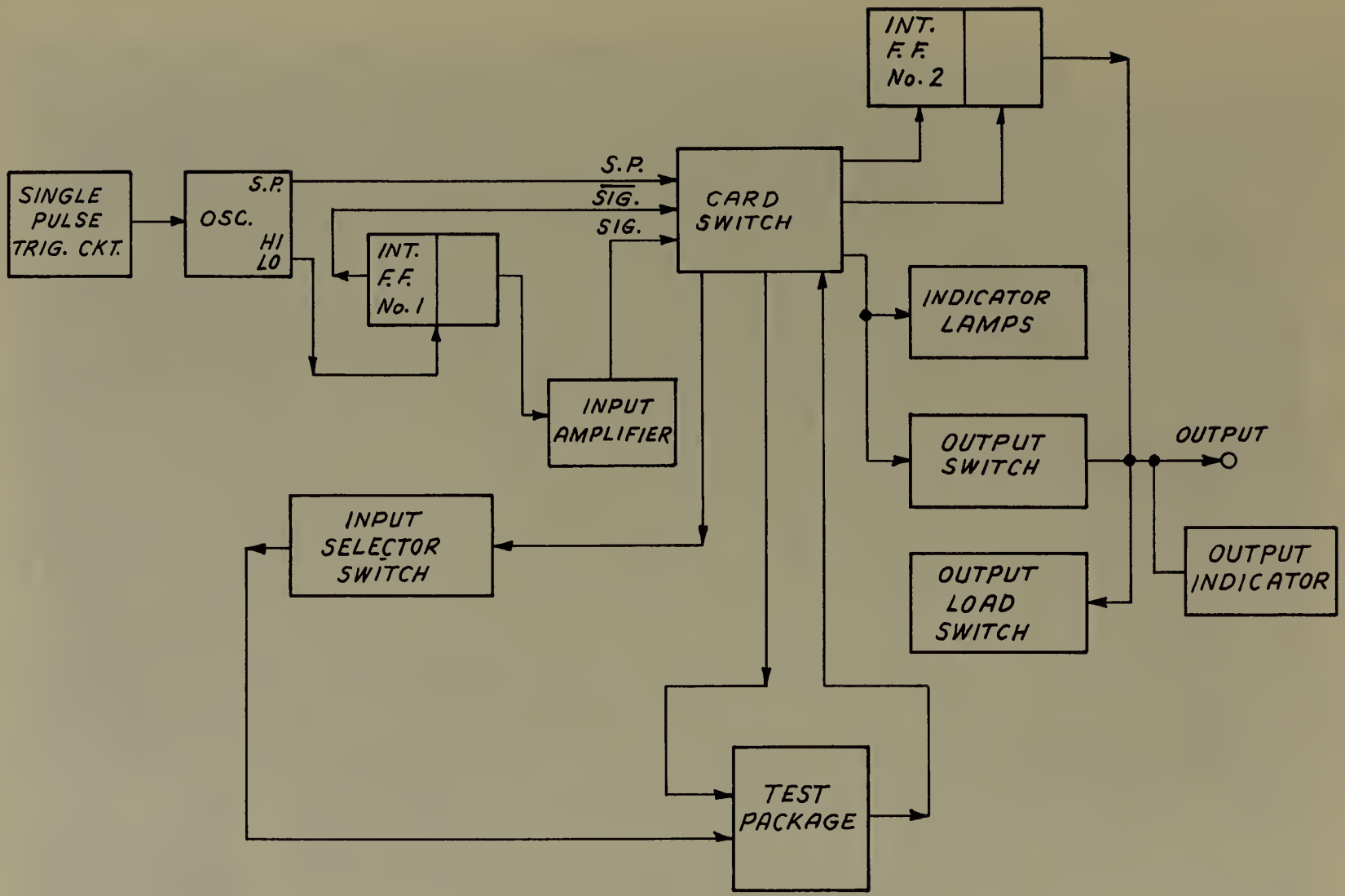


Figure 13. Block Diagram of Package Tester.

Figure 14. Rotating Beam Ceilometer Computer.

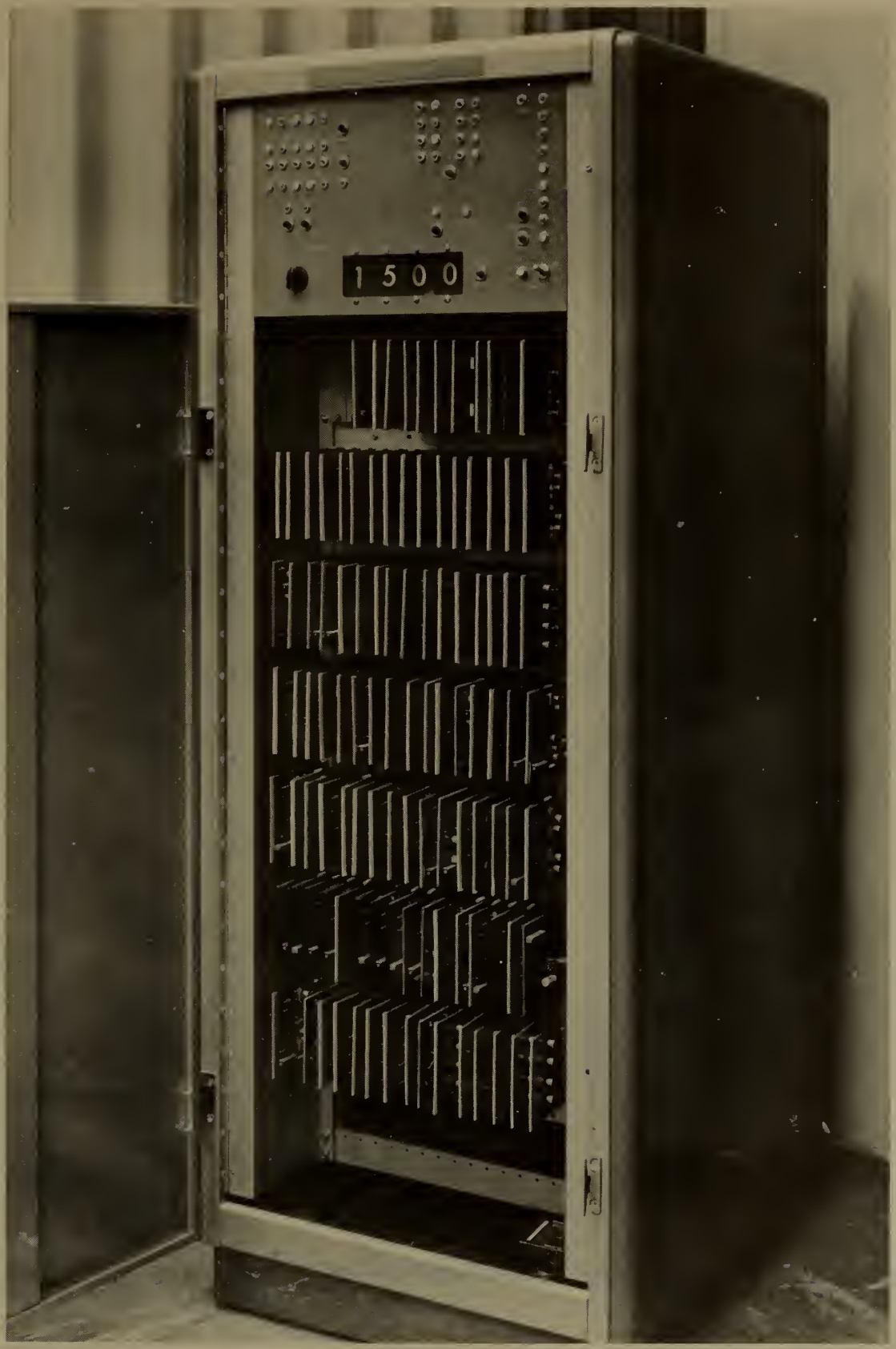
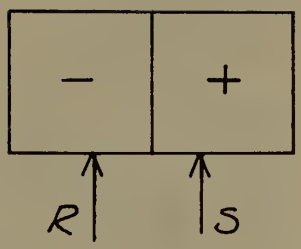
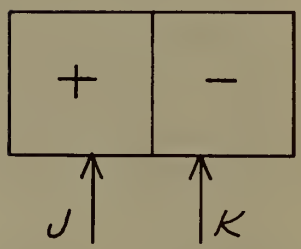


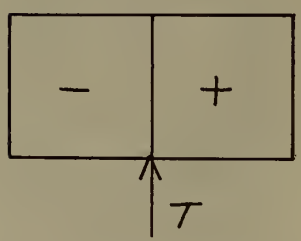
Figure 15. Inside View of Ceilometer Showing Building Block Packages.



(a) RS FLIP-FLOP
(RESET AND SET)



(b) JK FLIP-FLOP
(J IS EQUIVALENT TO SET
AND K TO RESET)



(c) T FLIP-FLOP
(TURN OVER INPUT)

Figure 16. Suggested Logical Symbols for Flip-Flops.

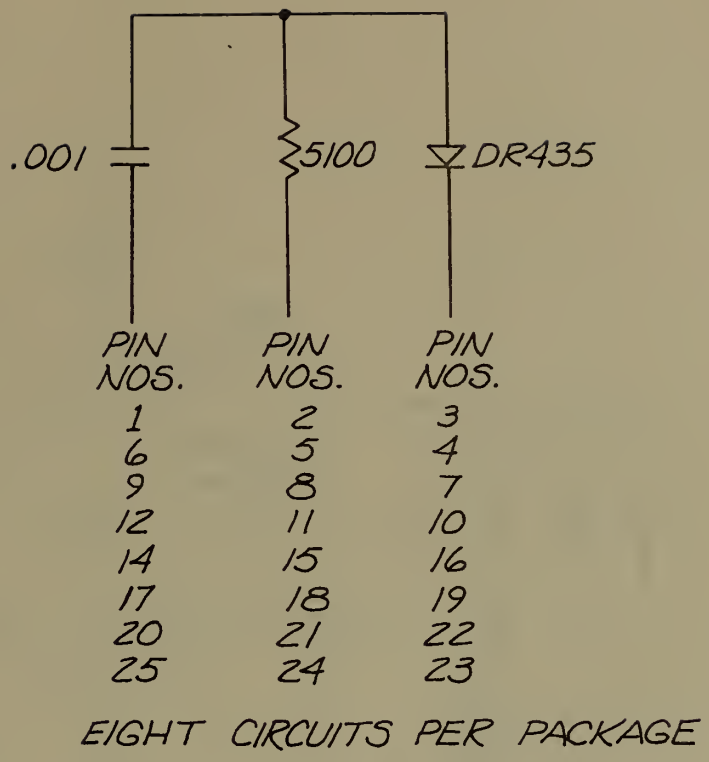


Figure 17. Gating Package.

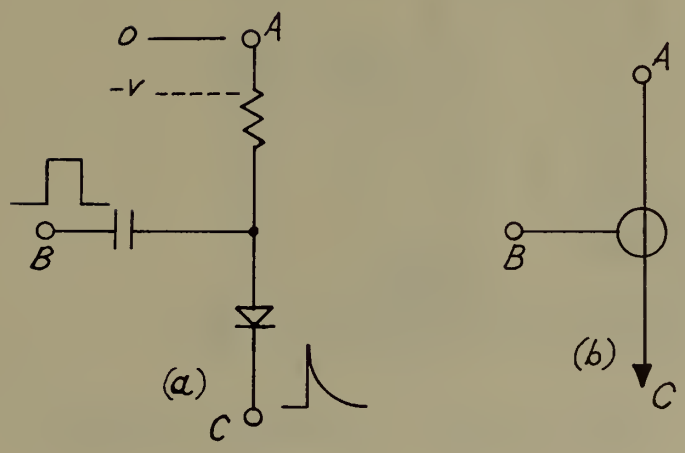


Figure 18. Schematic Diagram with Waveforms and Logical Symbol for Gating Structure.

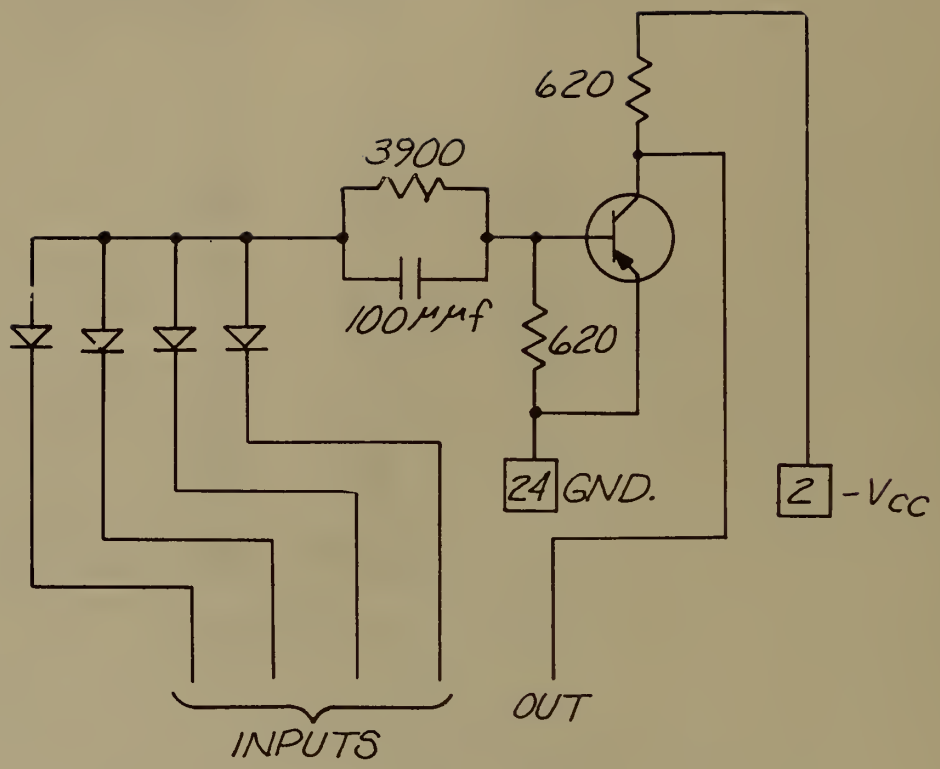


Figure 19. And-Inverter, Or-Inverter Package.

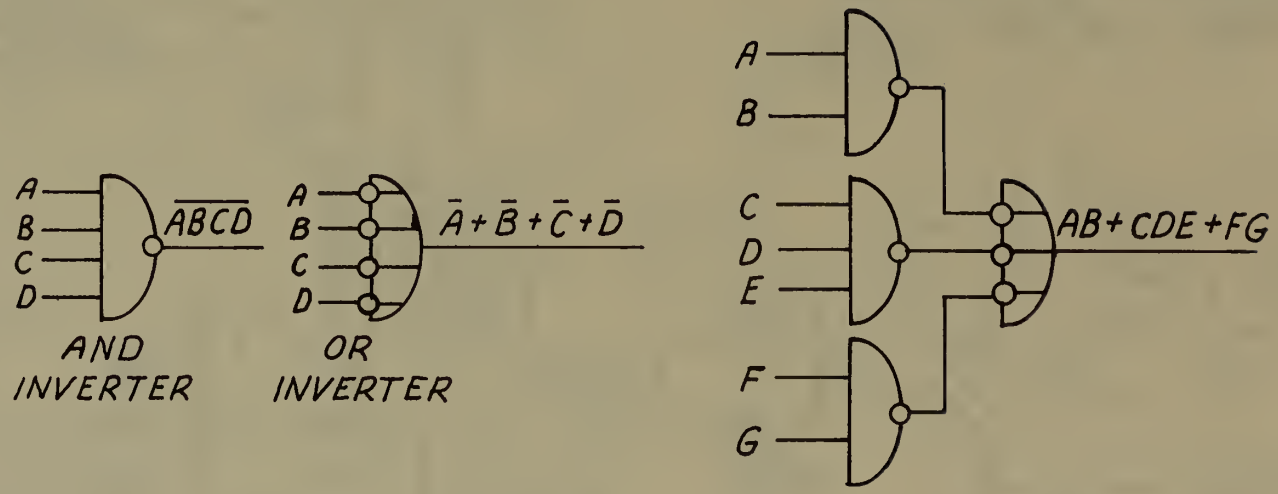


Figure 20. Logical Symbols for And-Or Inverter Circuits.

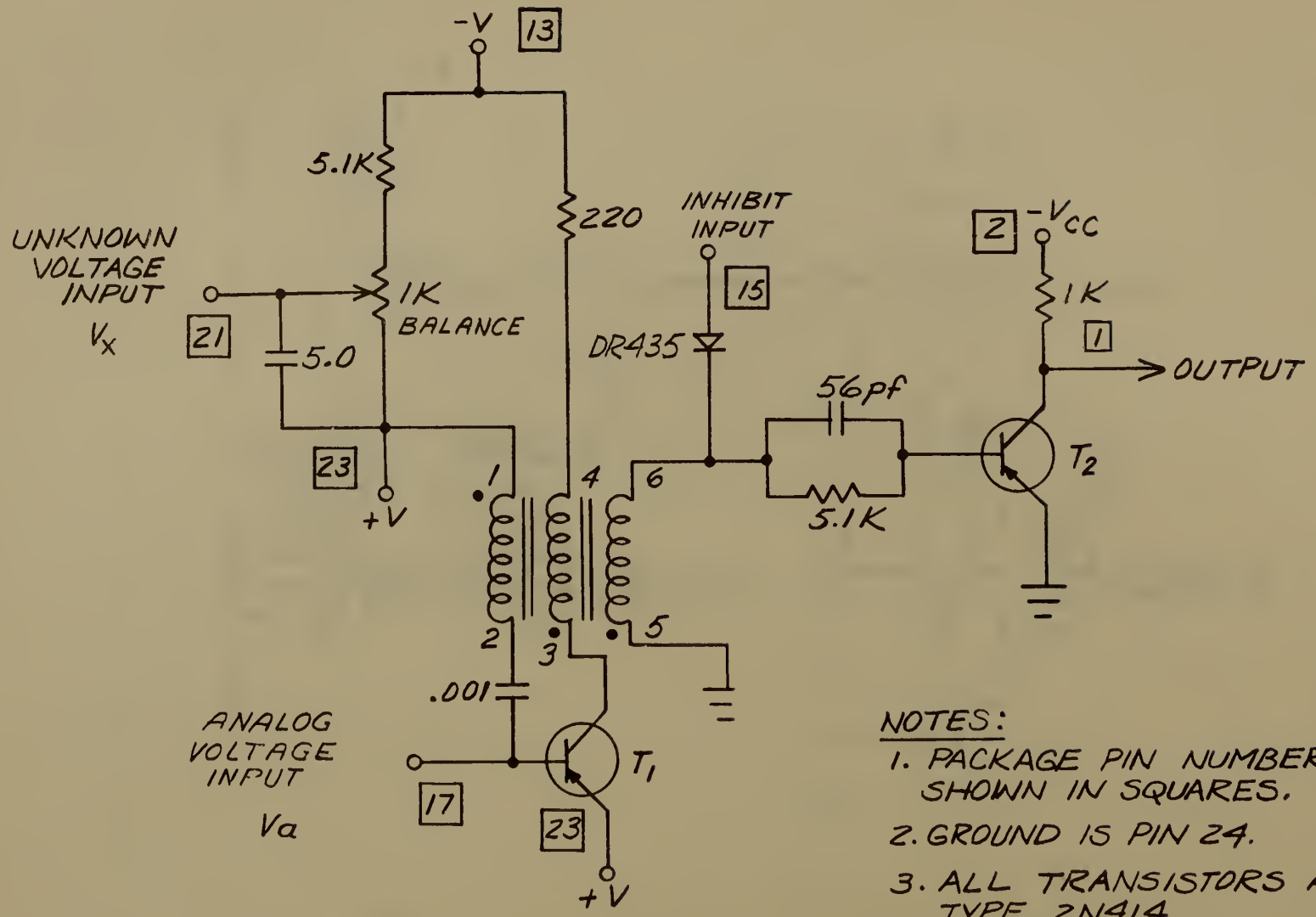
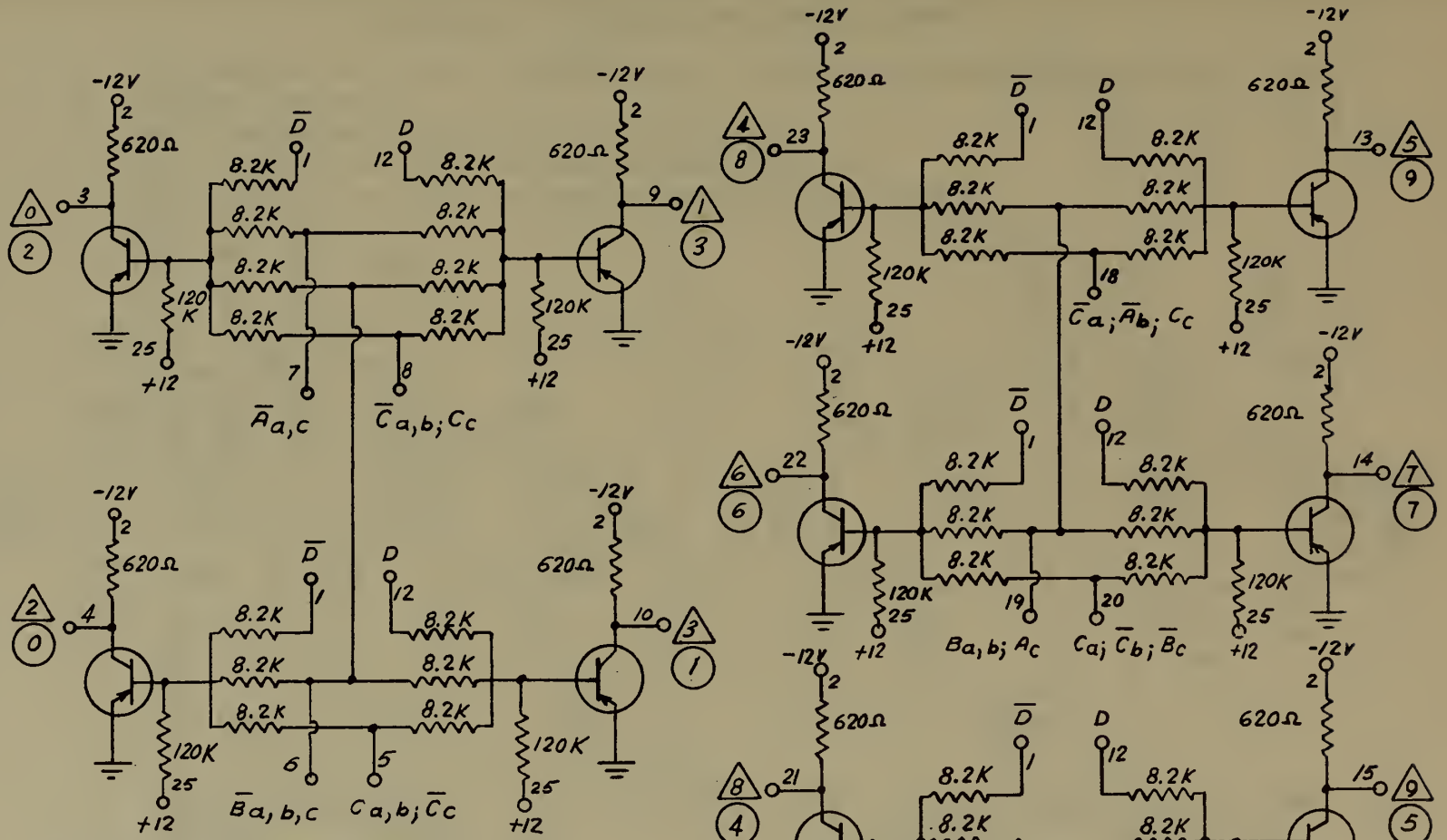
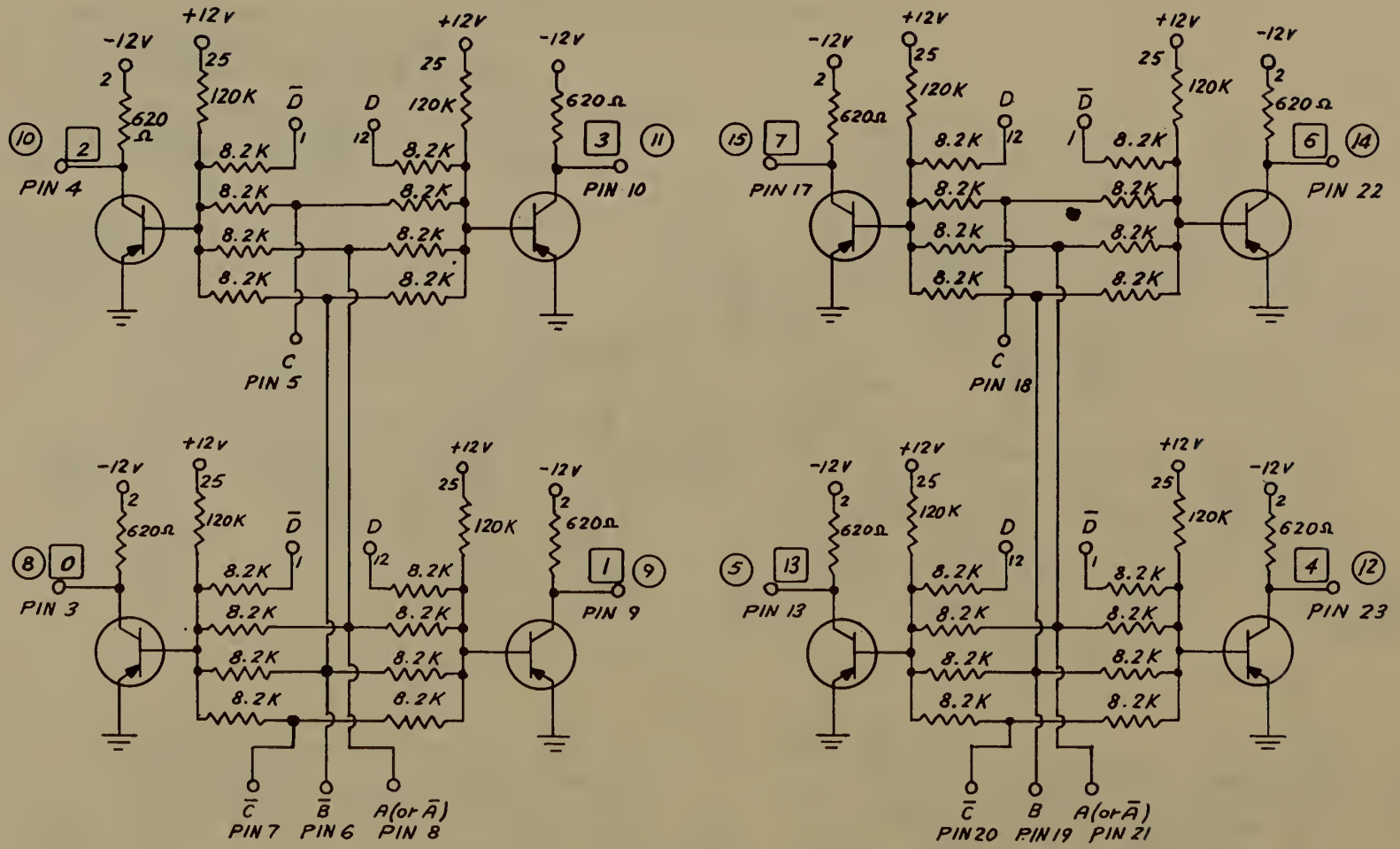


Figure 21. Analog Voltage Comparator Package.



1. SUBSCRIPT (a) = 1-2-4-8 COUNTER
2. " (b) = 1-2*-2*-4 "
3. " (c) = 1-2*-2-4 "
4. △ = DECIMAL OUTPUTS FOR 1-2*-2*-4 AND 1-2-4-8 COUNTERS.
5. ◯ = DECIMAL OUTPUTS FOR 1-2*-2-4 COUNTER.
6. * DESIGNATES FEEDBACK SIGNAL.
7. ALL TRANSISTORS TYPE 2N414.
8. GROUND - PIN 24.

Figure 22. Decimal Decoder Package



1. ◯ = OUTPUTS FOR 2ND PACKAGE OF HEXADECIMAL DECODER.
2. INPUTS D(or $\bar{D}$) USED ONLY FOR HEXADECIMAL DECODING.
3. ALL TRANSISTORS TYPE 2N414.
4. GROUND PIN No. 24.
5. □ = OUTPUTS FOR OCTAL DECODER OR 1ST PACKAGE OF HEXADECIMAL DECODER

Figure 23. Octal-Hexadecimal Decoder Package.

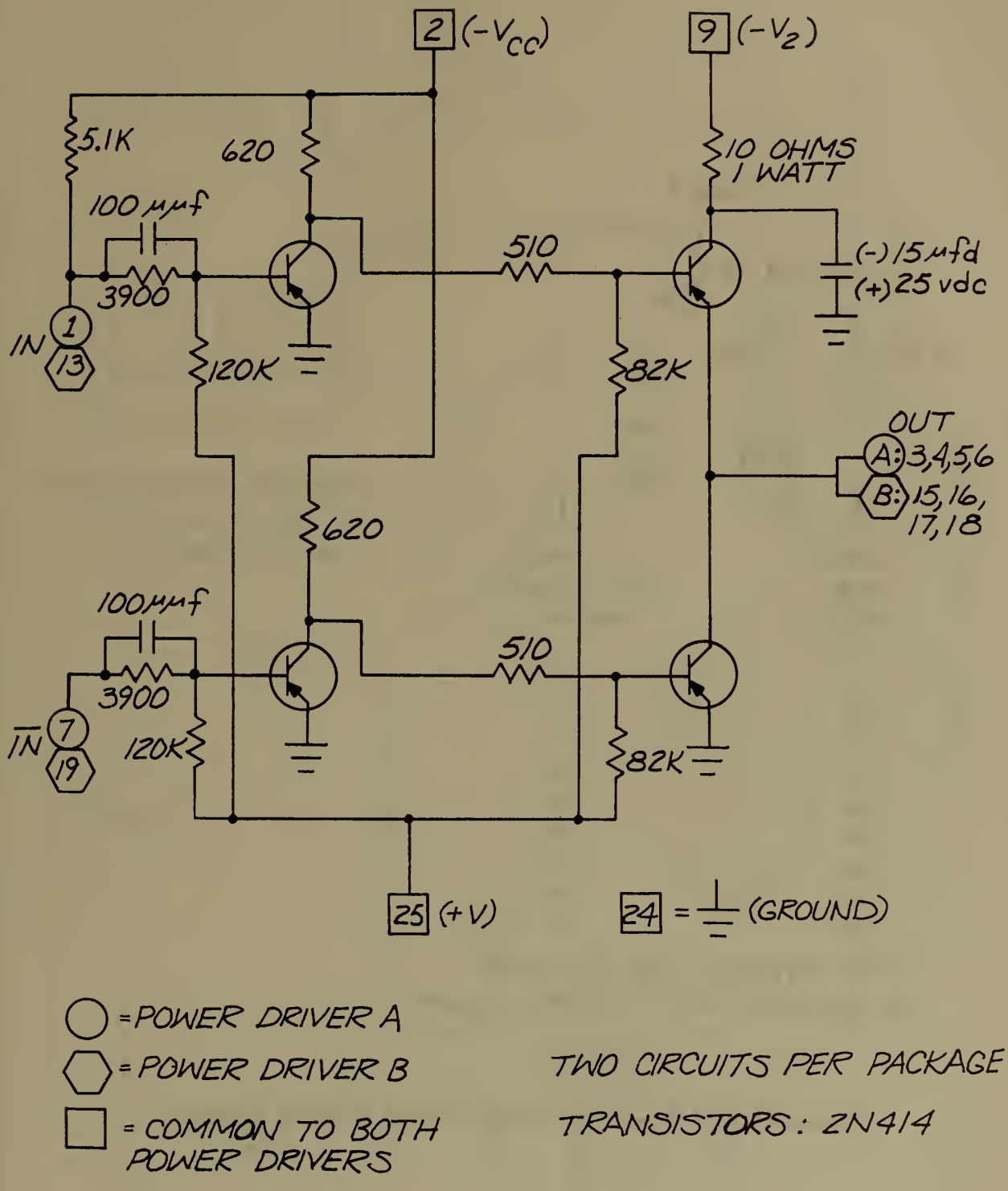


Figure 24. Power Driver Package.

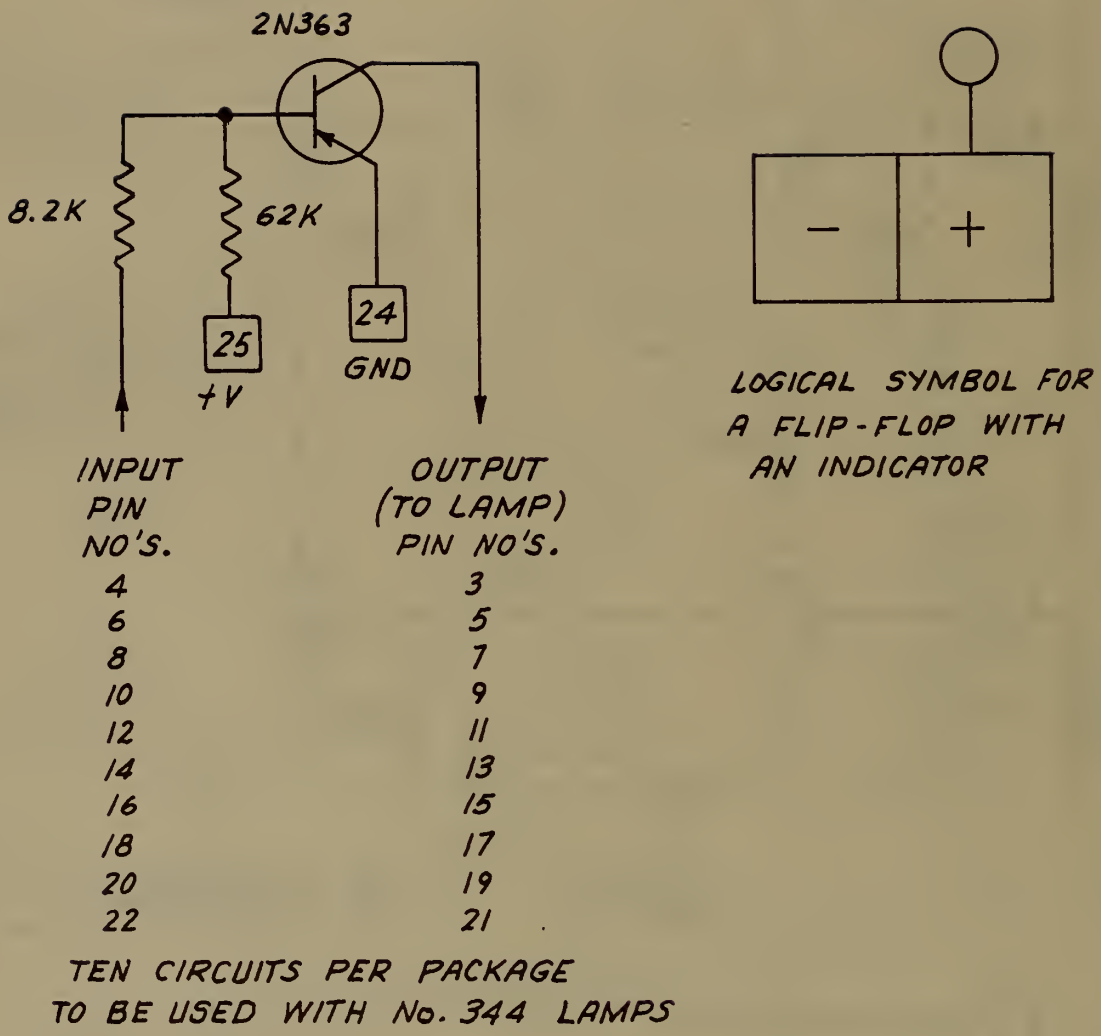


Figure 25. Indicator Package and its Logical Symbol.

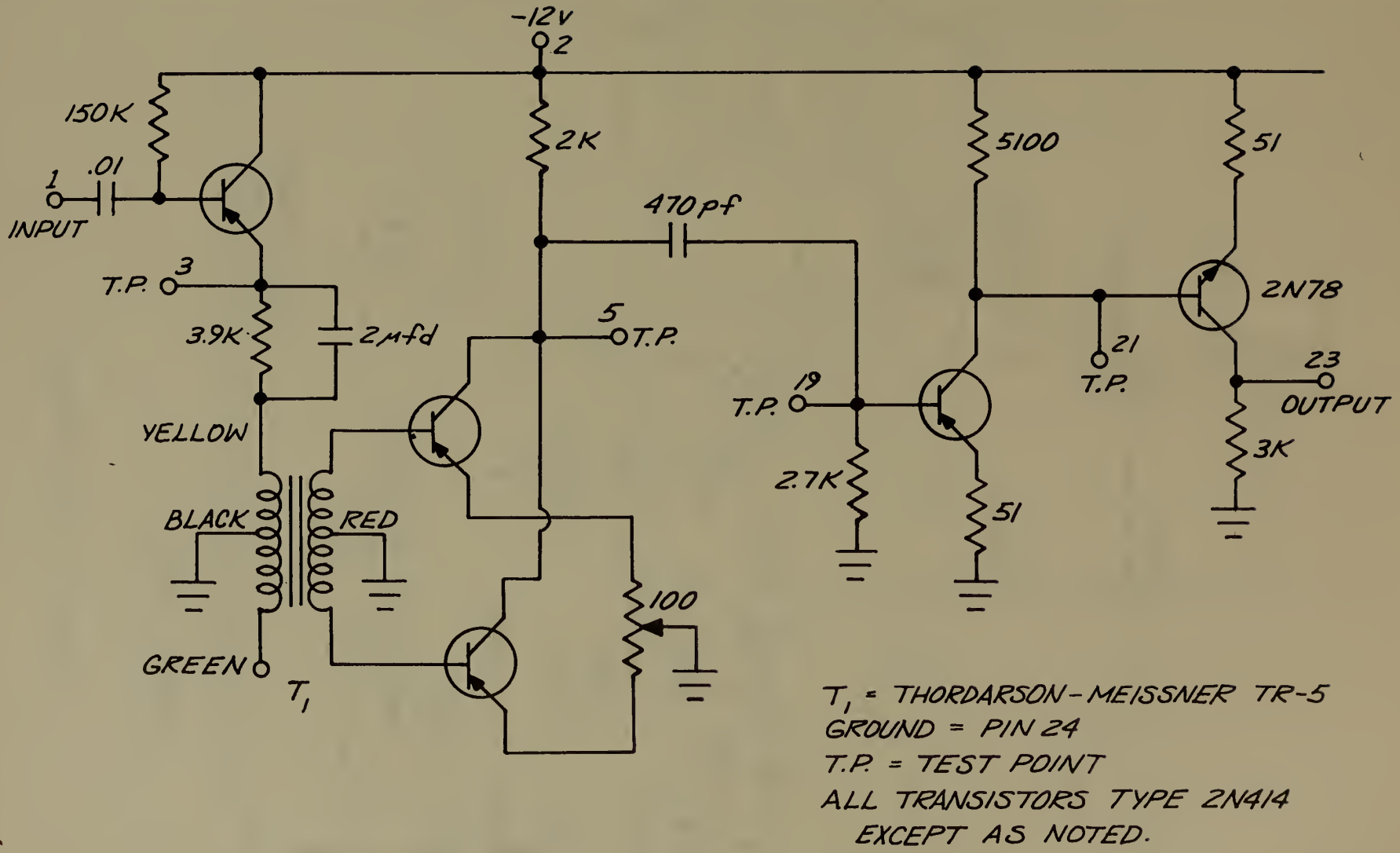


Figure 26. Read Package.

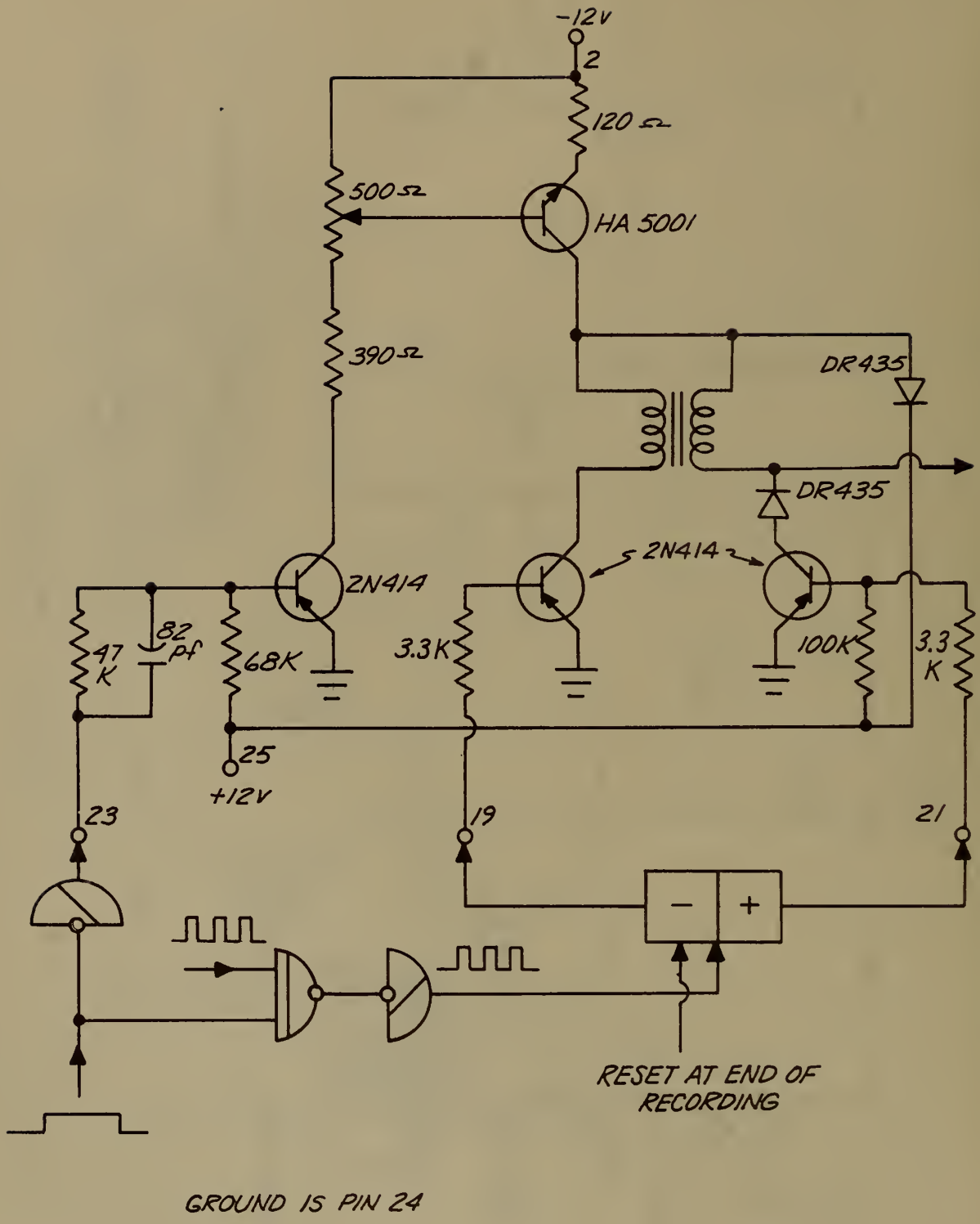


Figure 27. Record Package.

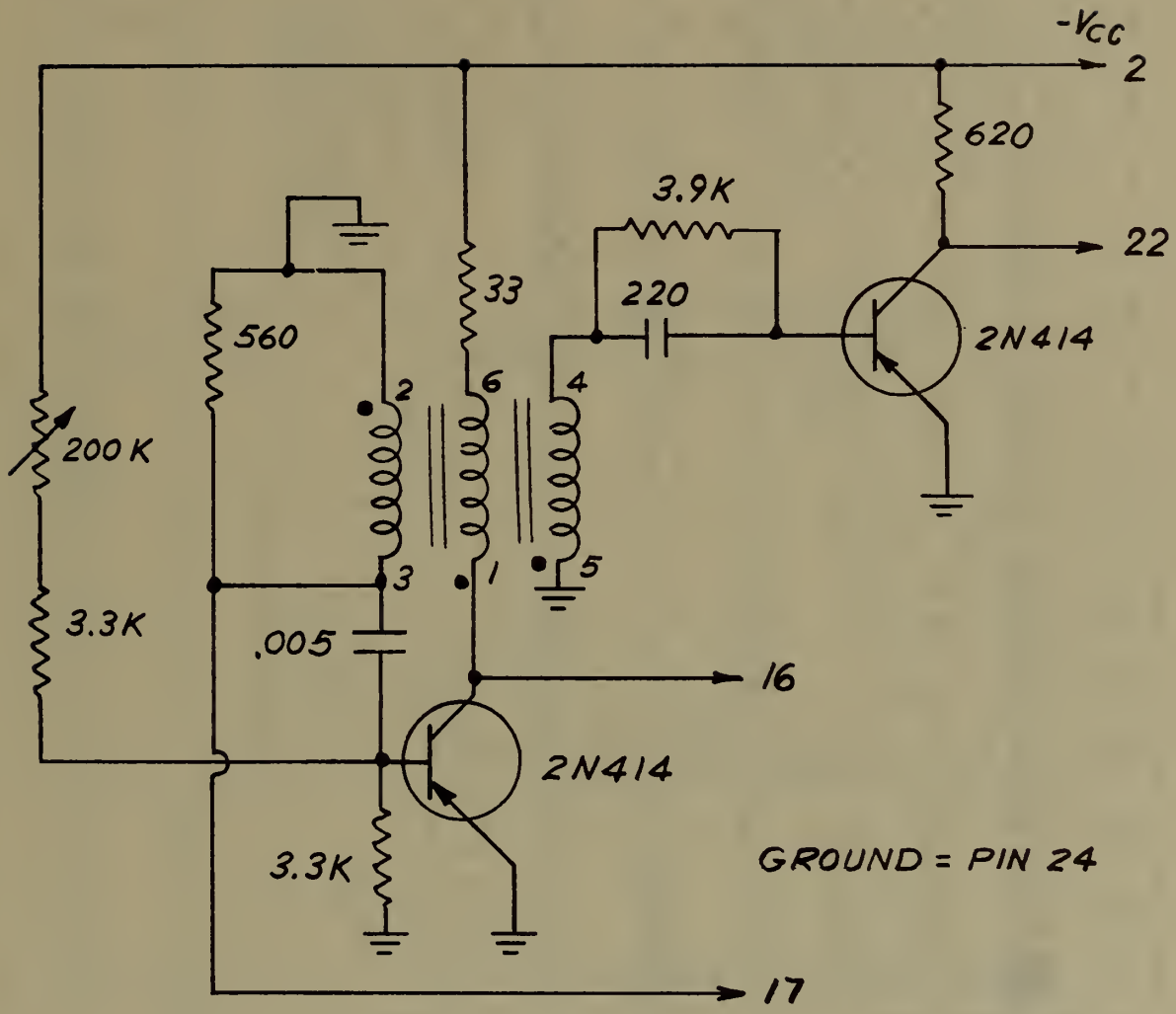
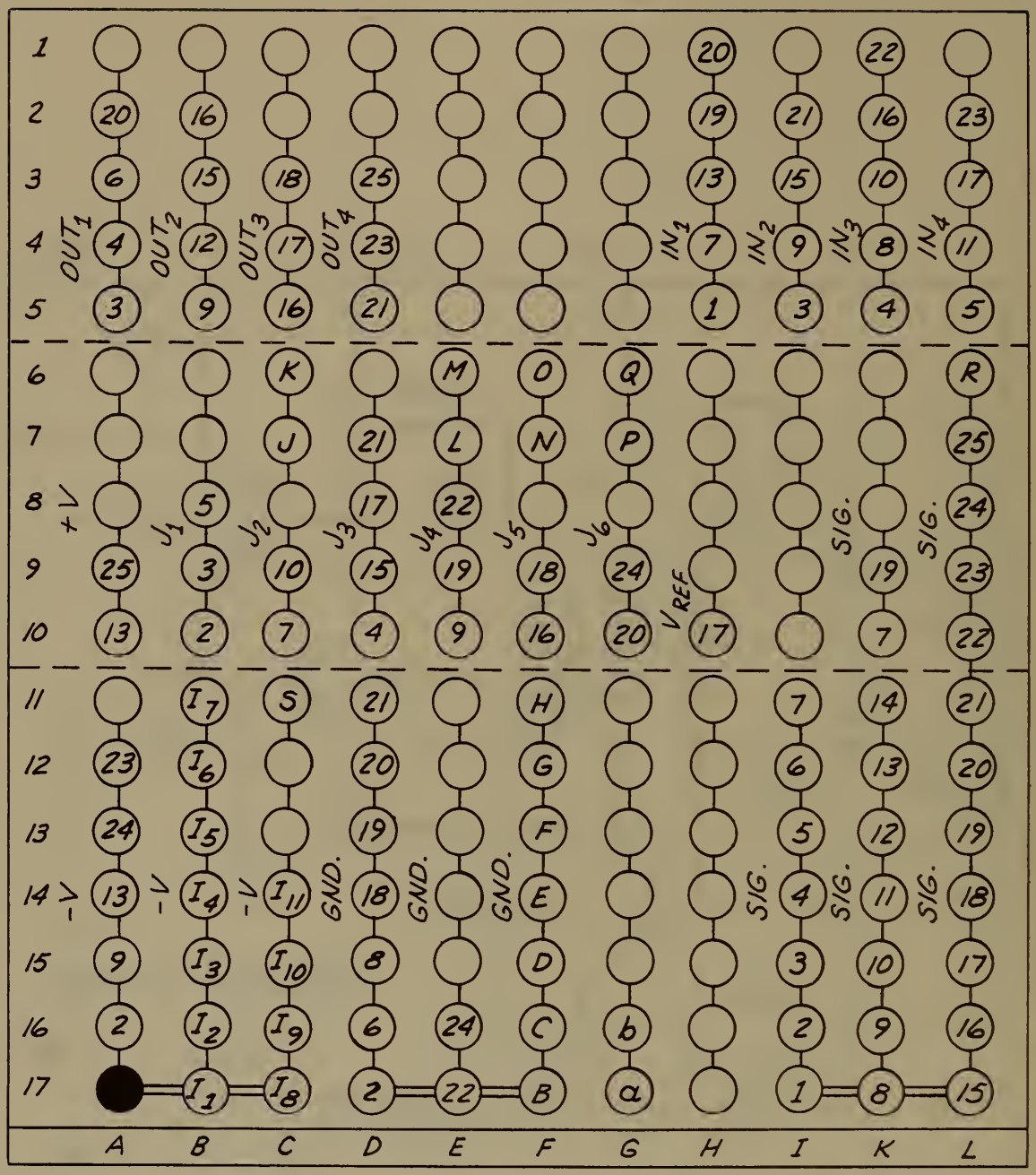


Figure 28. Pulse Generator Package (flip-flop not shown).



DOUBLE LINES INDICATE SHUNTS ADDED AT TERMINAL STRIPS. NUMBER WITHIN CIRCLE INDICATES TEST SOCKET PIN WHICH IS CONNECTED TO THIS POINT. LETTER INDICATES ROTARY SWITCH CONTACT.

I = INDICATOR LAMP

J_1 THRU J_6 = SHUNTS

Figure 29. Cardmatic Switch Card.

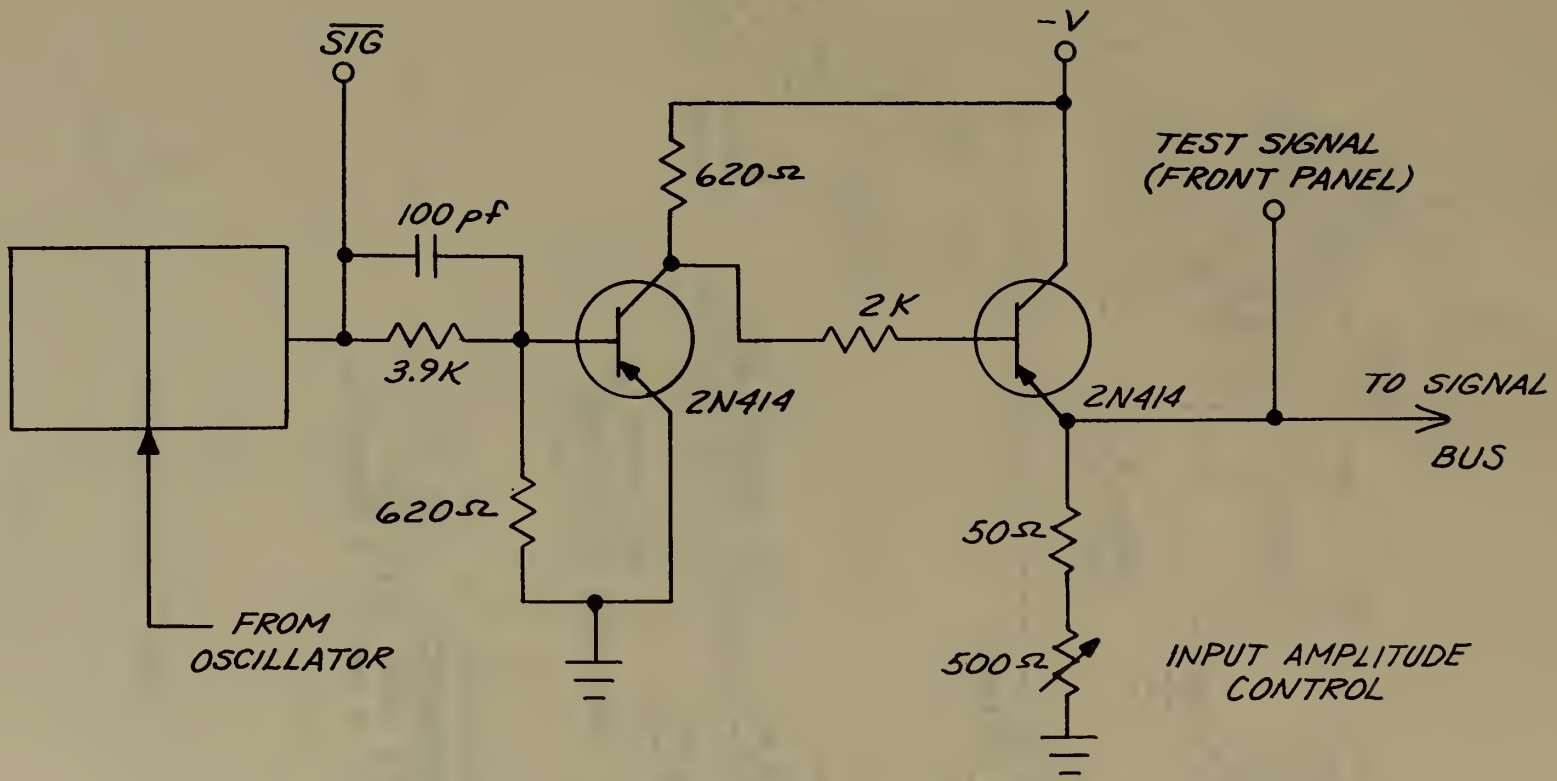
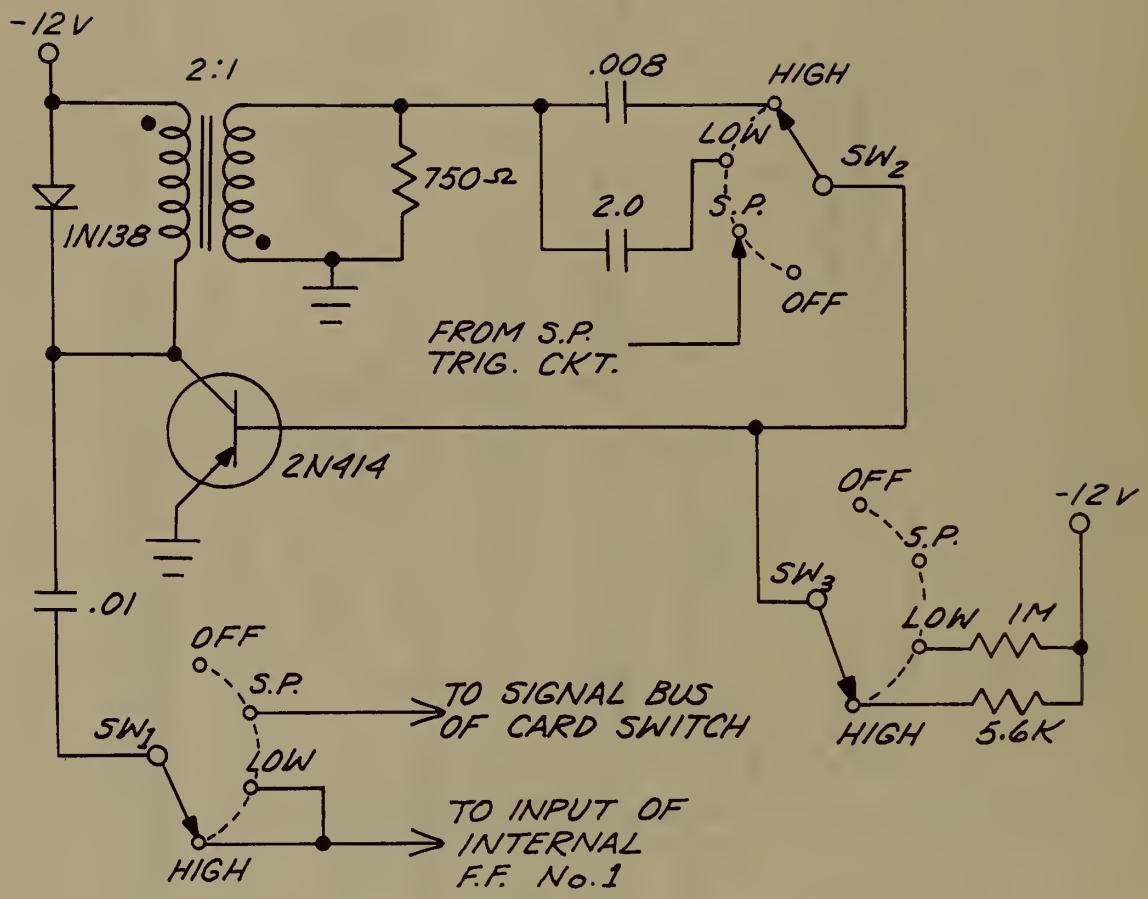


Figure 30. Internal Flip-Flop No. 1 with Amplifiers.



LOW FREQUENCY $\approx$ 20 CPS
HIGH FREQUENCY = 50 KC
SW_1, SW_2, AND SW_3, ARE
GANGED - 3 POLE, 4 POSITION

Figure 31. Input Pulse Generator.

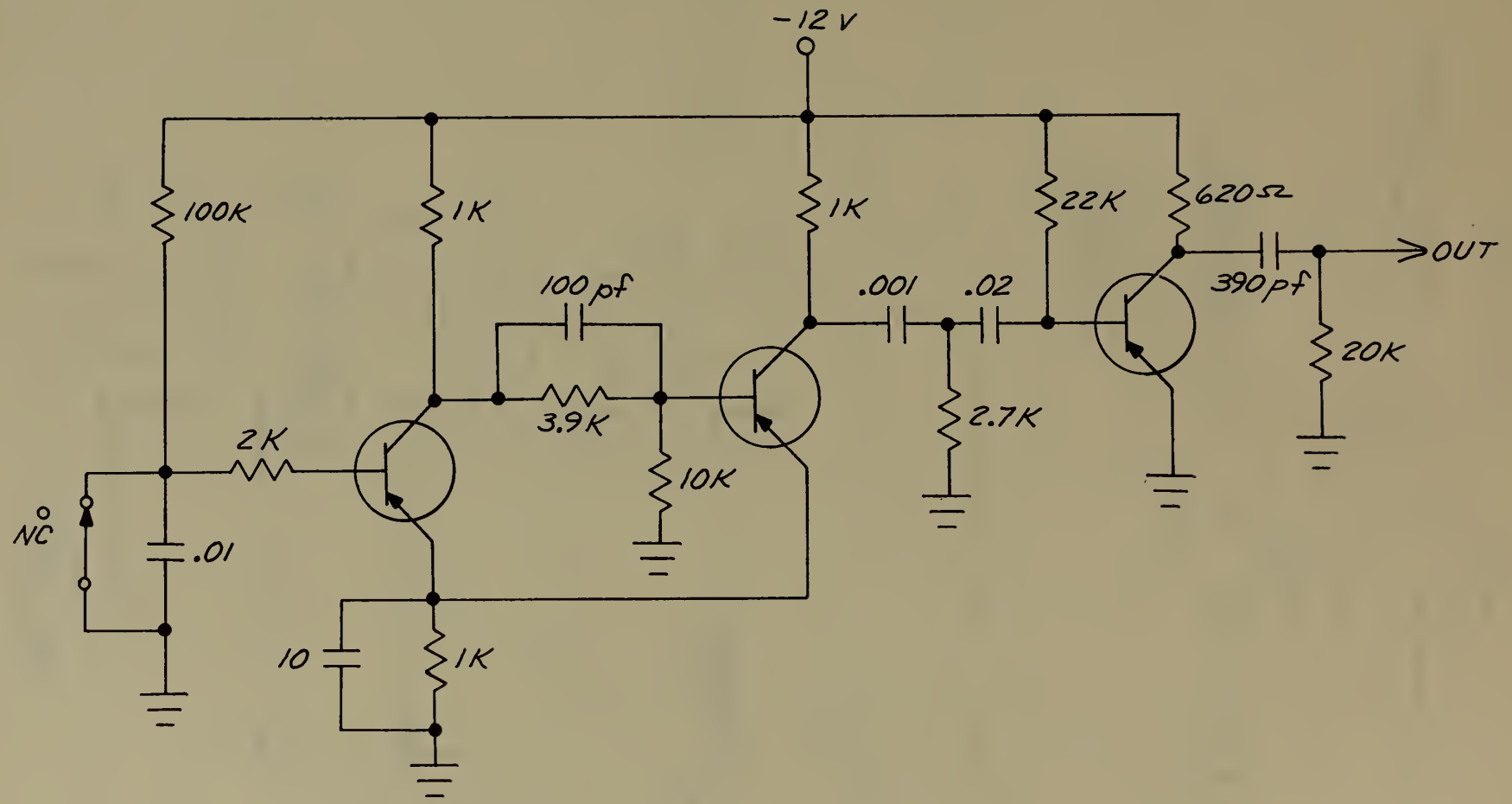


Figure 32. Schmitt Trigger Circuit with Amplifiers.

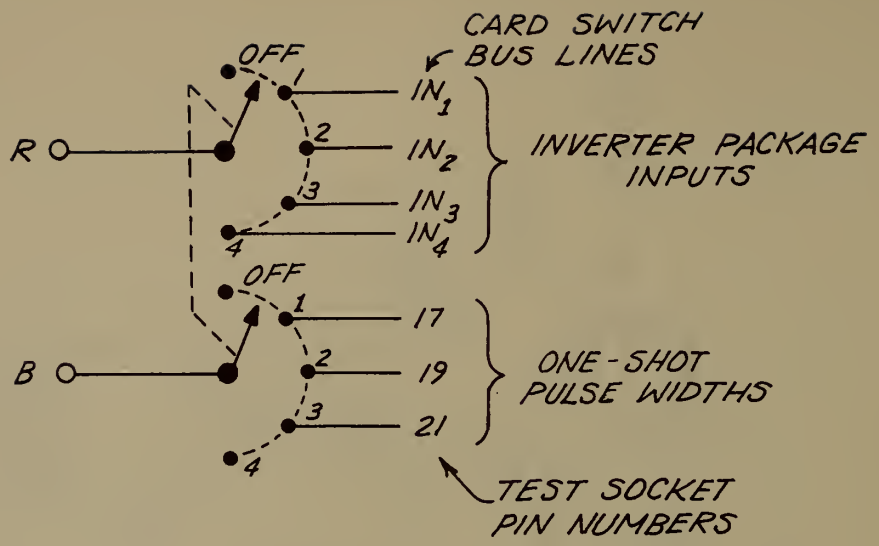


Figure 33. Input Selector Switch.

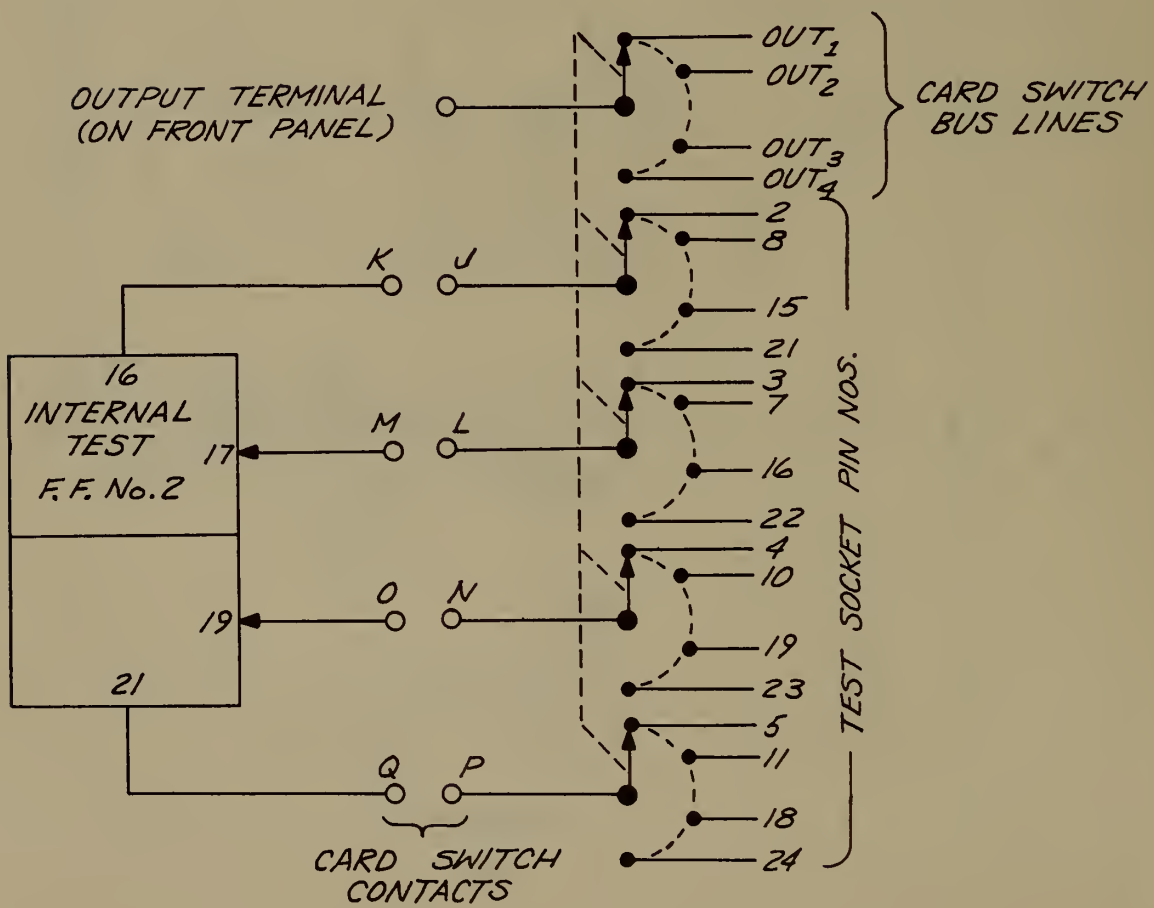


Figure 34. Output Selector Switch with Test Flip-Flop.

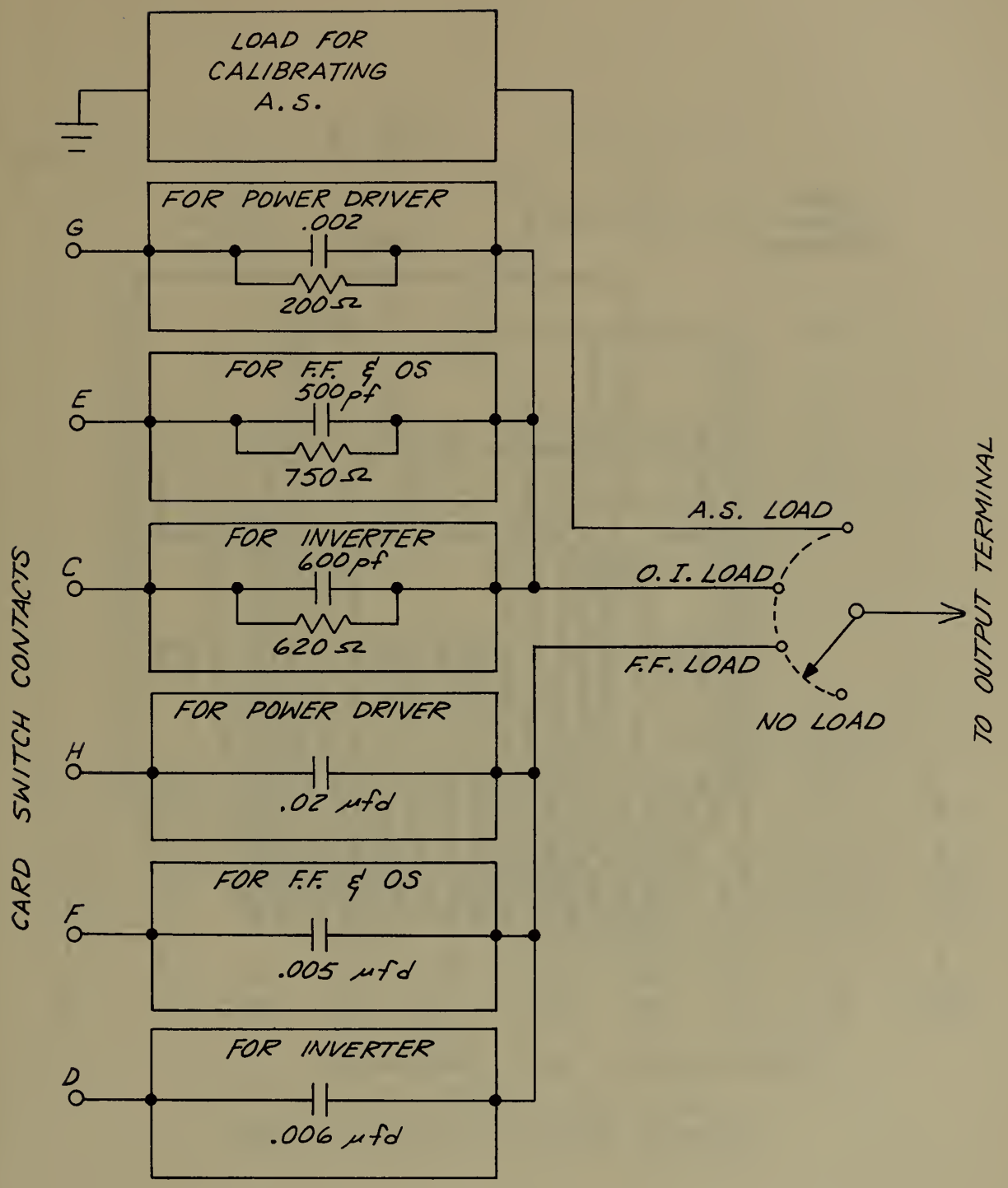


Figure 35. Load Selector Switch.

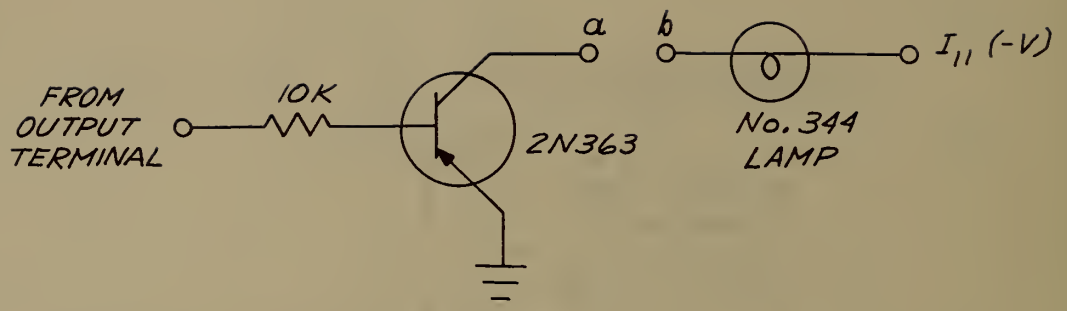


Figure 36. Output Indicator.

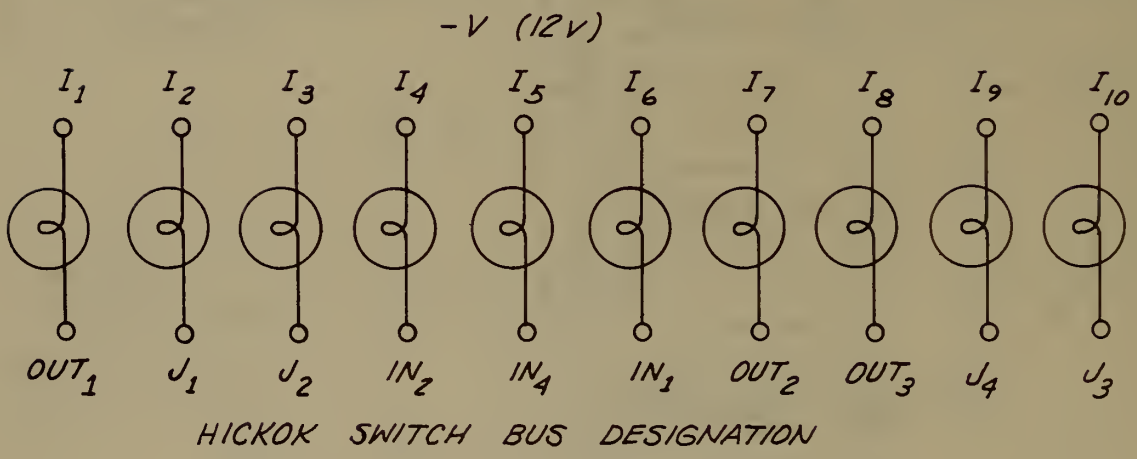


Figure 37. Indicator Package Test Lamps.

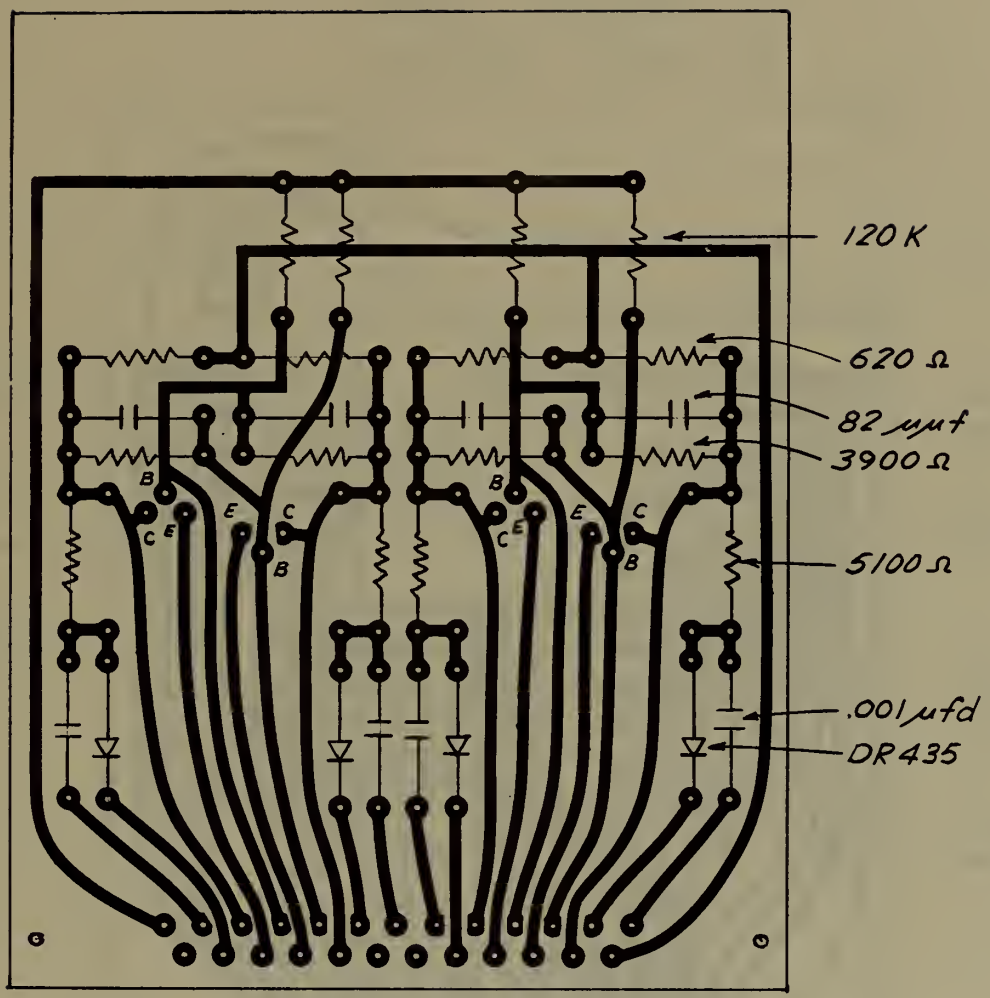


Figure 38. Flip-Flop Package. Layout.

ALL CAPACITORS - .001 μf
ALL RESISTORS - 5.1K
ALL DIODES - DR435

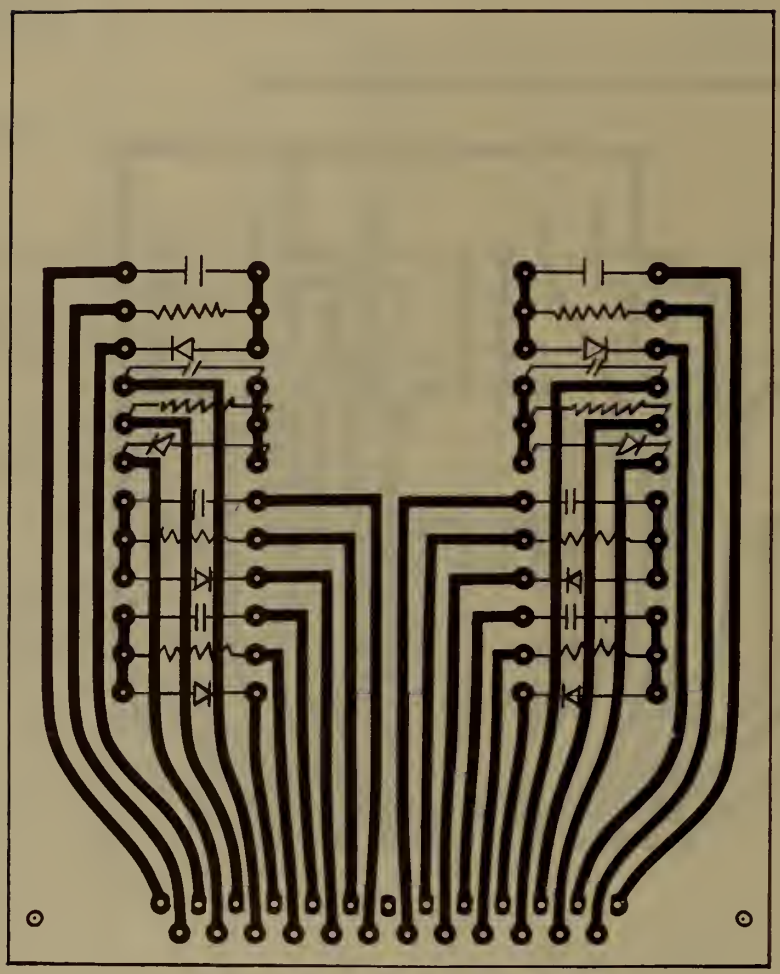


Figure 39. Gate Circuits Package.Layout.

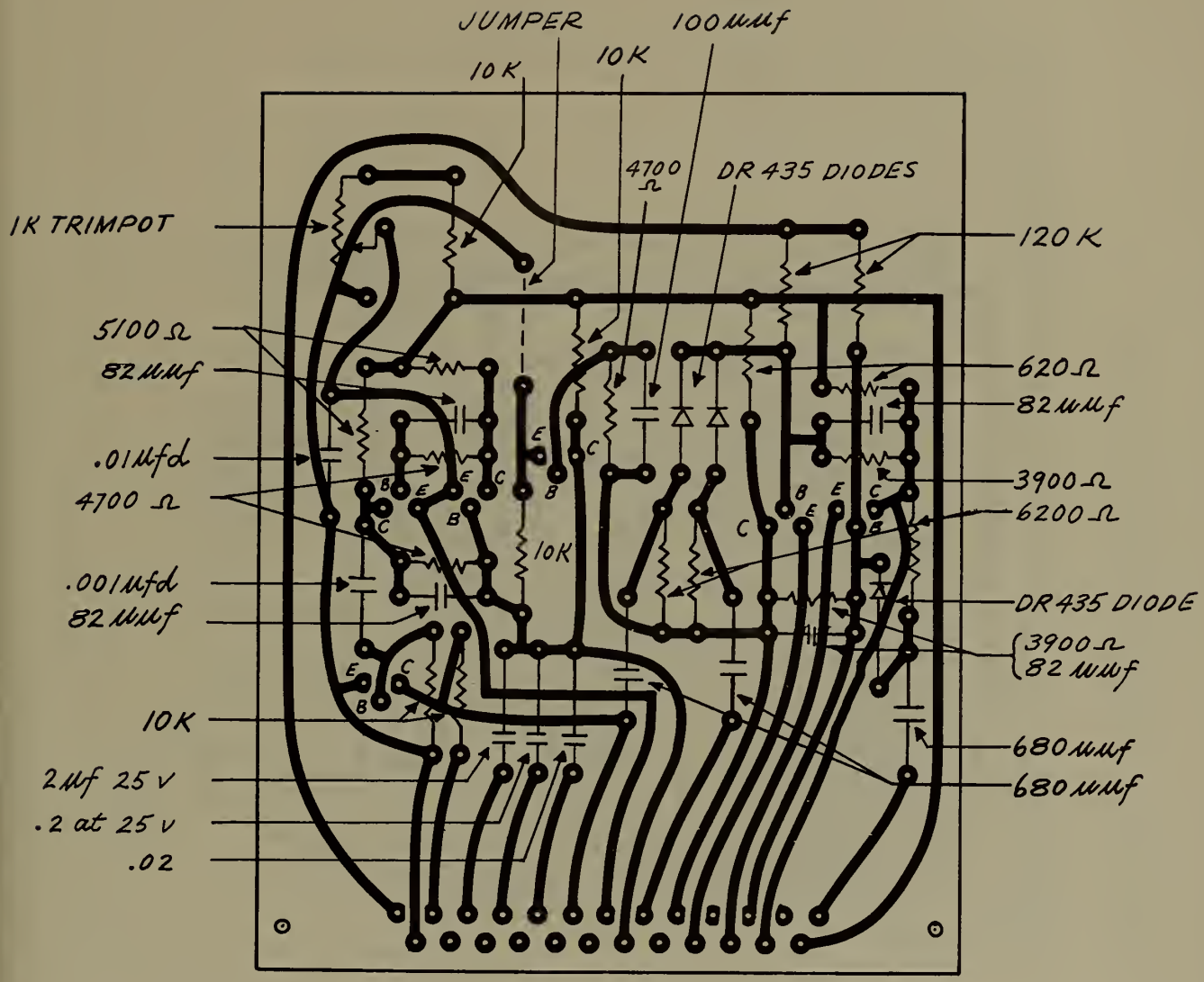


Figure 40. One-Shot Package Layout.

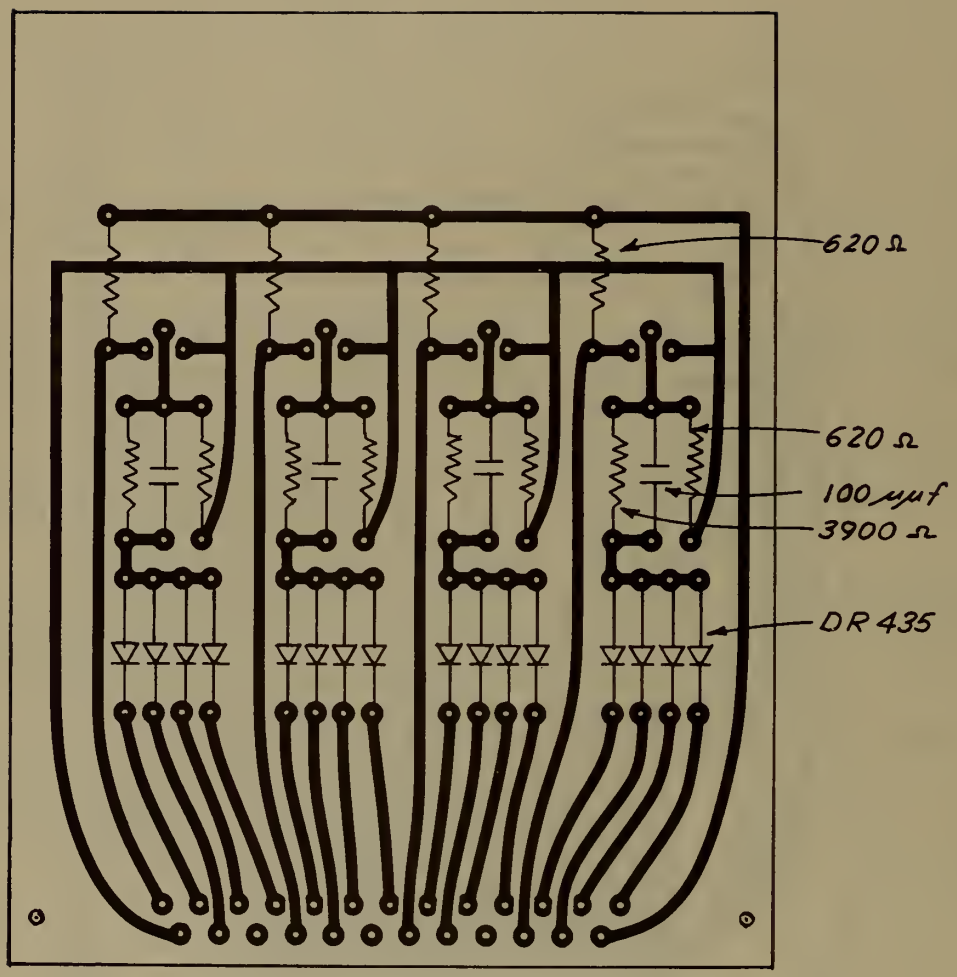


Figure 41. And-Or Inverter Package Layout.

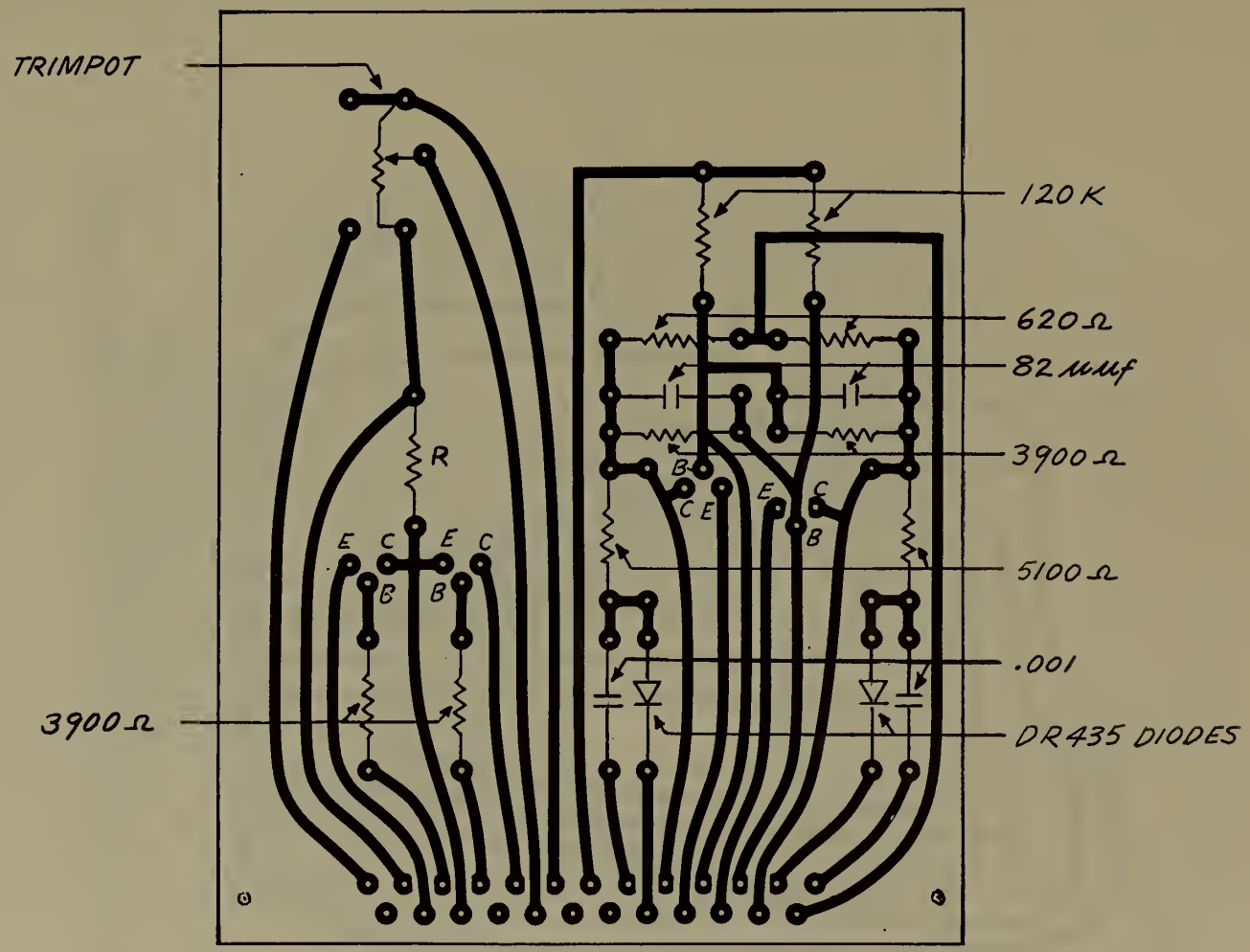


Figure 42. Analog Switch Package Layout.

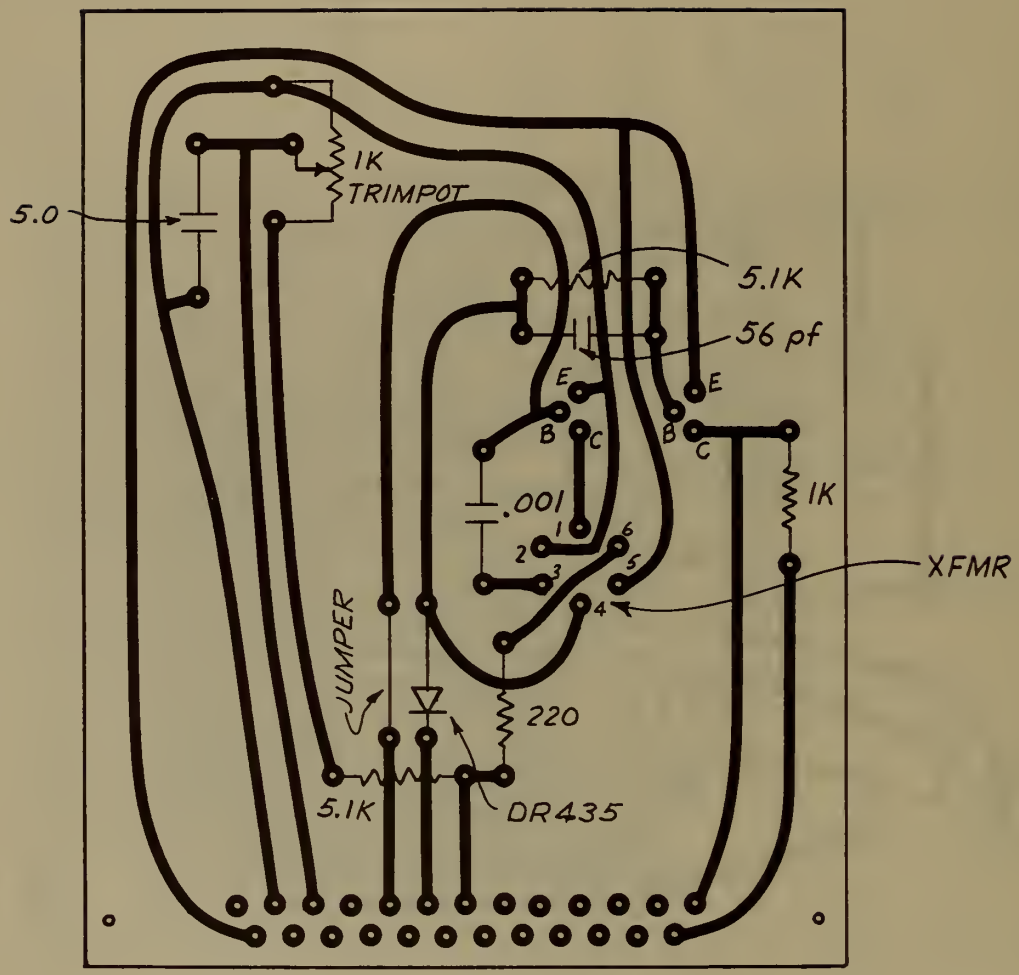


Figure 43. Analog Voltage Comparator Package Layout.

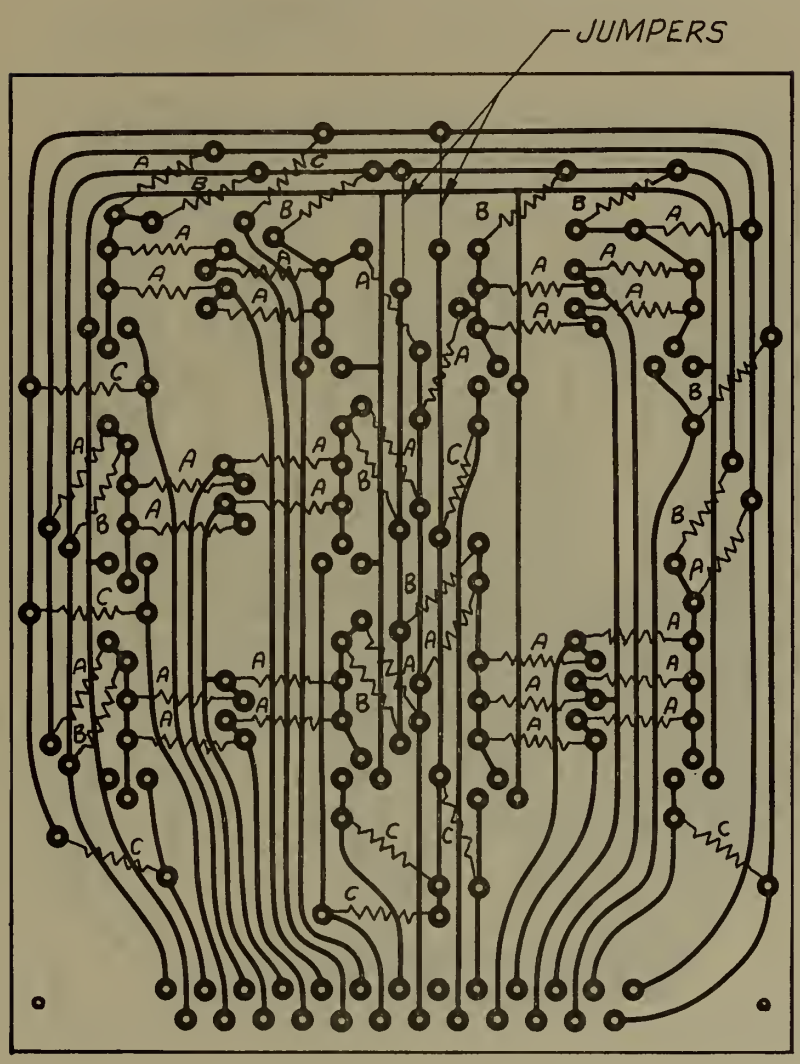


Figure 44. Decimal Decoder Package Layout.

A - GATE RESISTORS 32/PKG. 8.2K
B - BASE RESISTORS 8/PKG. 100K (TO +V.)
C - COLLECTOR RESISTORS 8/PKG. 1K (TO -V.)

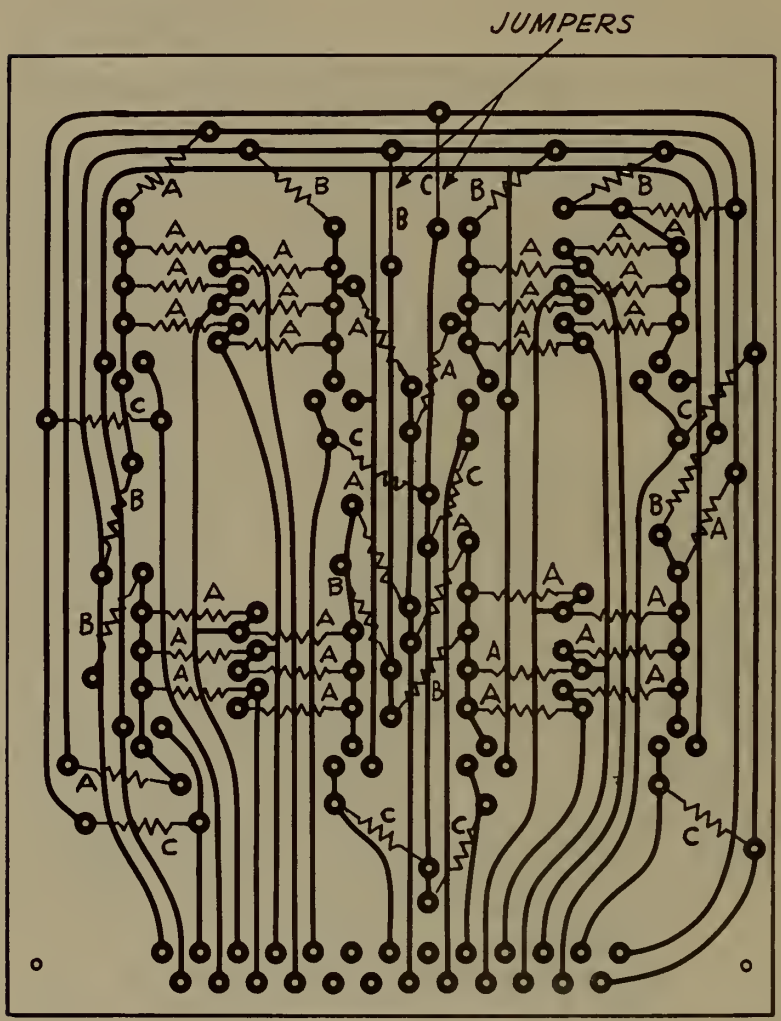


Figure 45. Octal-Hexadecimal Decoder Package Layout.

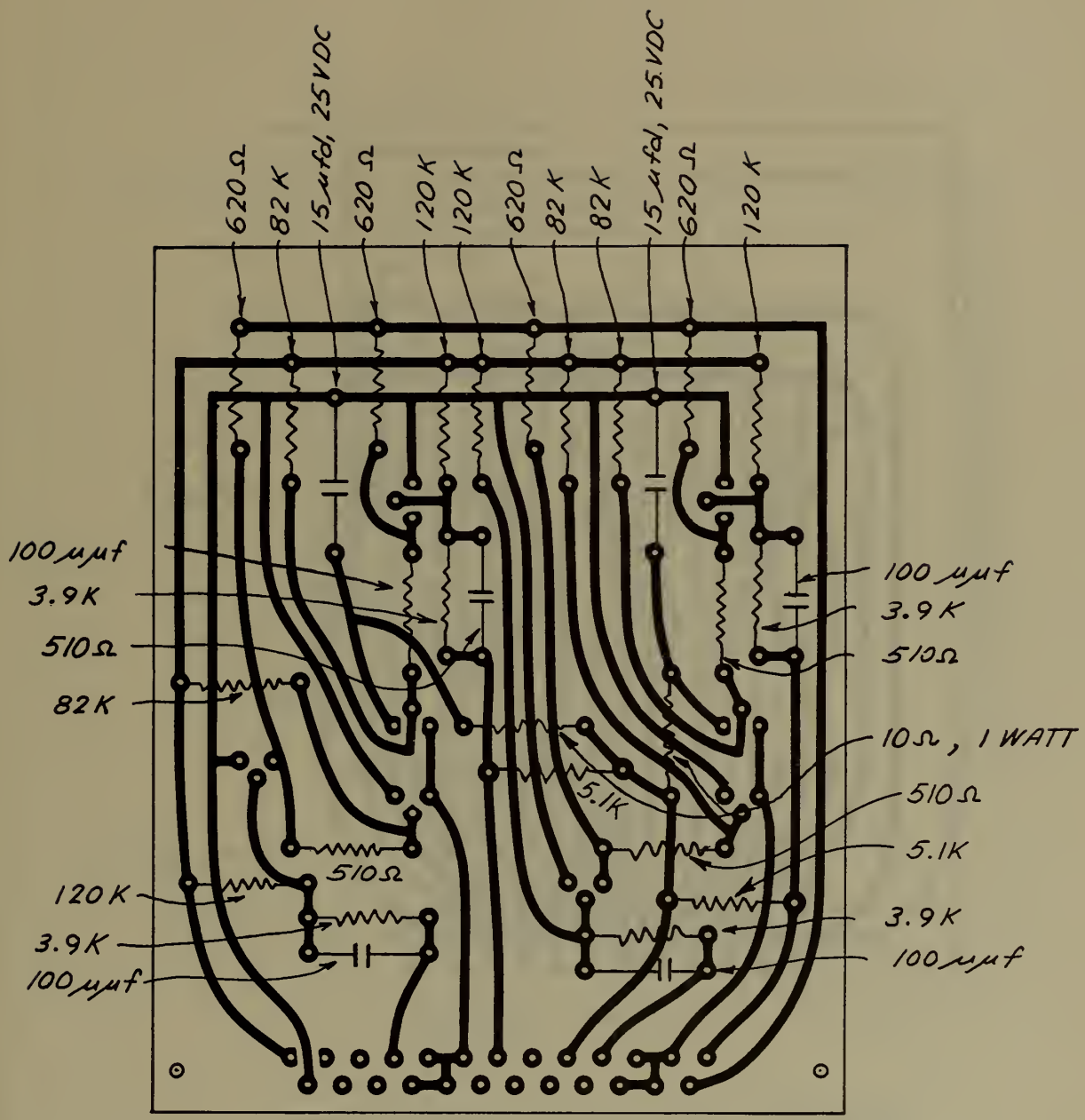


Figure 46. Power Driver Package Layout.

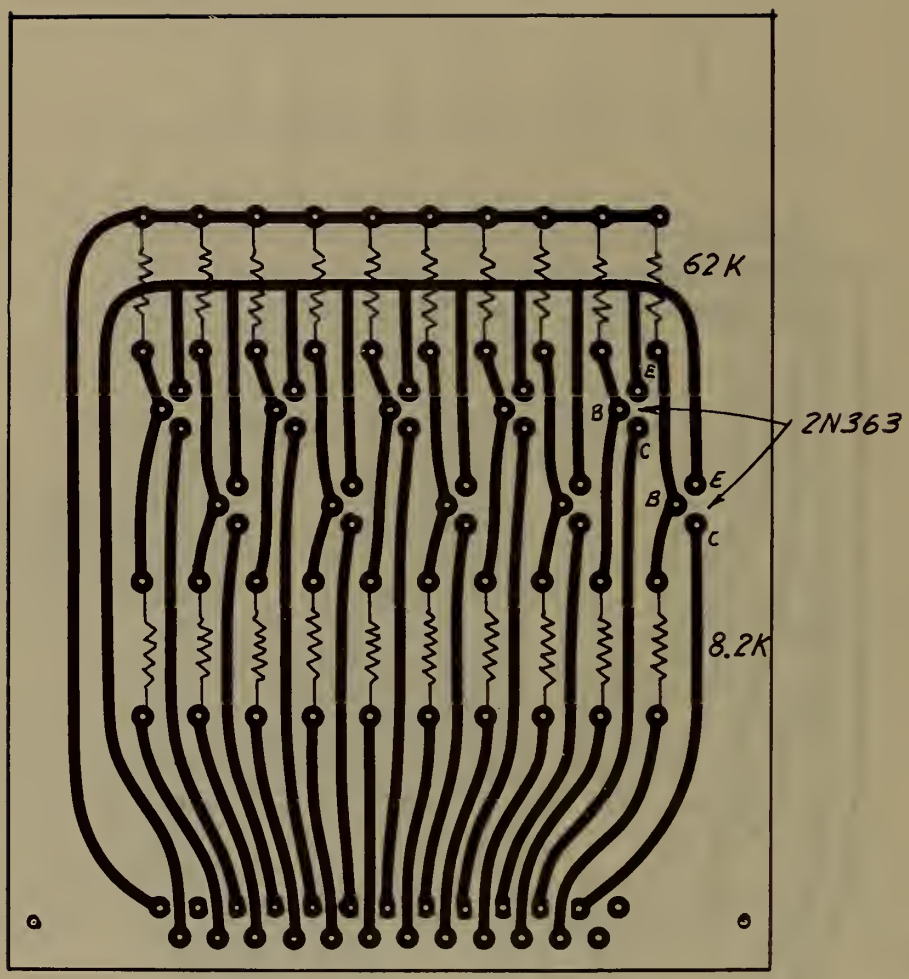


Figure 47. Power Driver Package Layout.

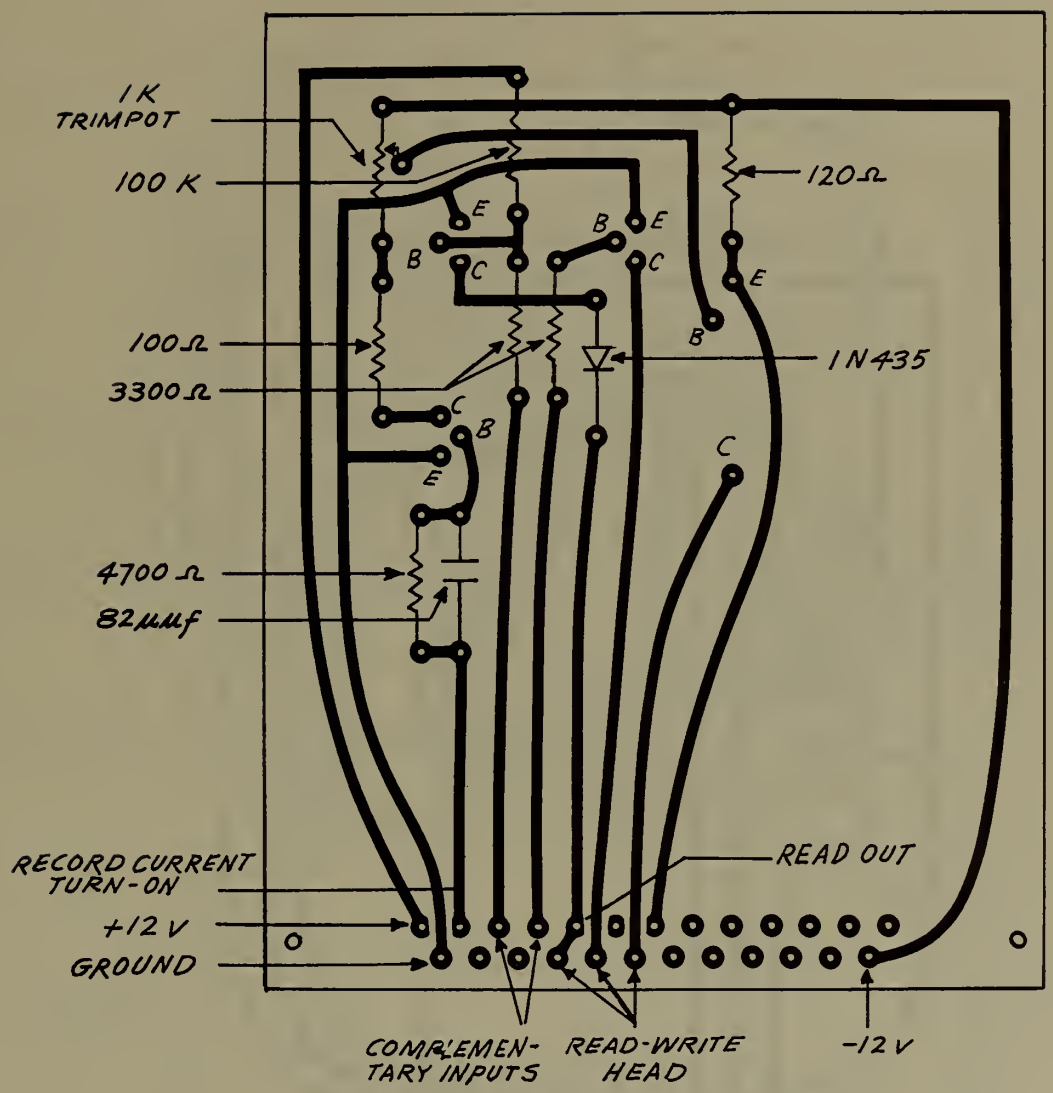


Figure 49. Record Package Layout.

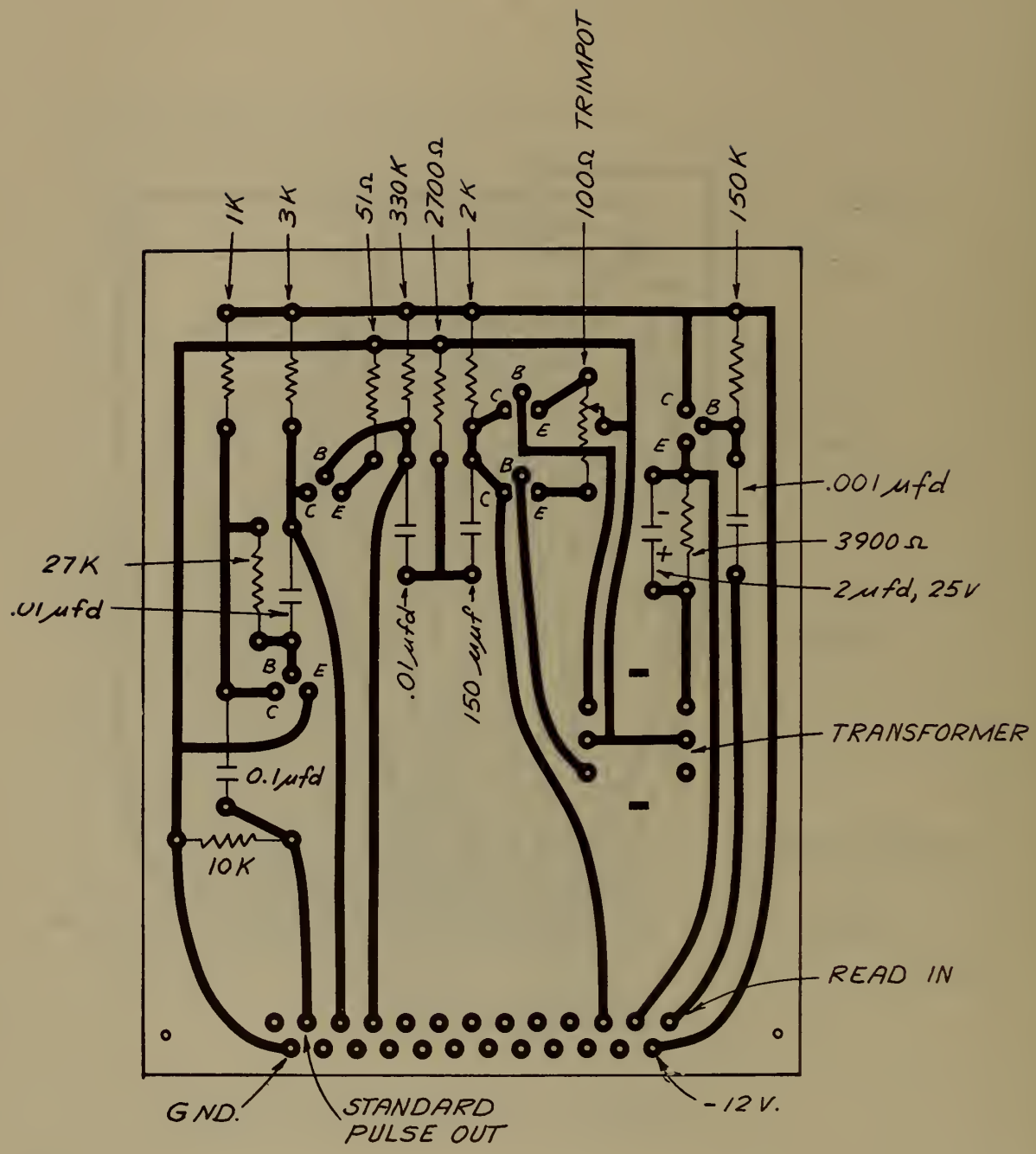


Figure 48. Read Package Layout.

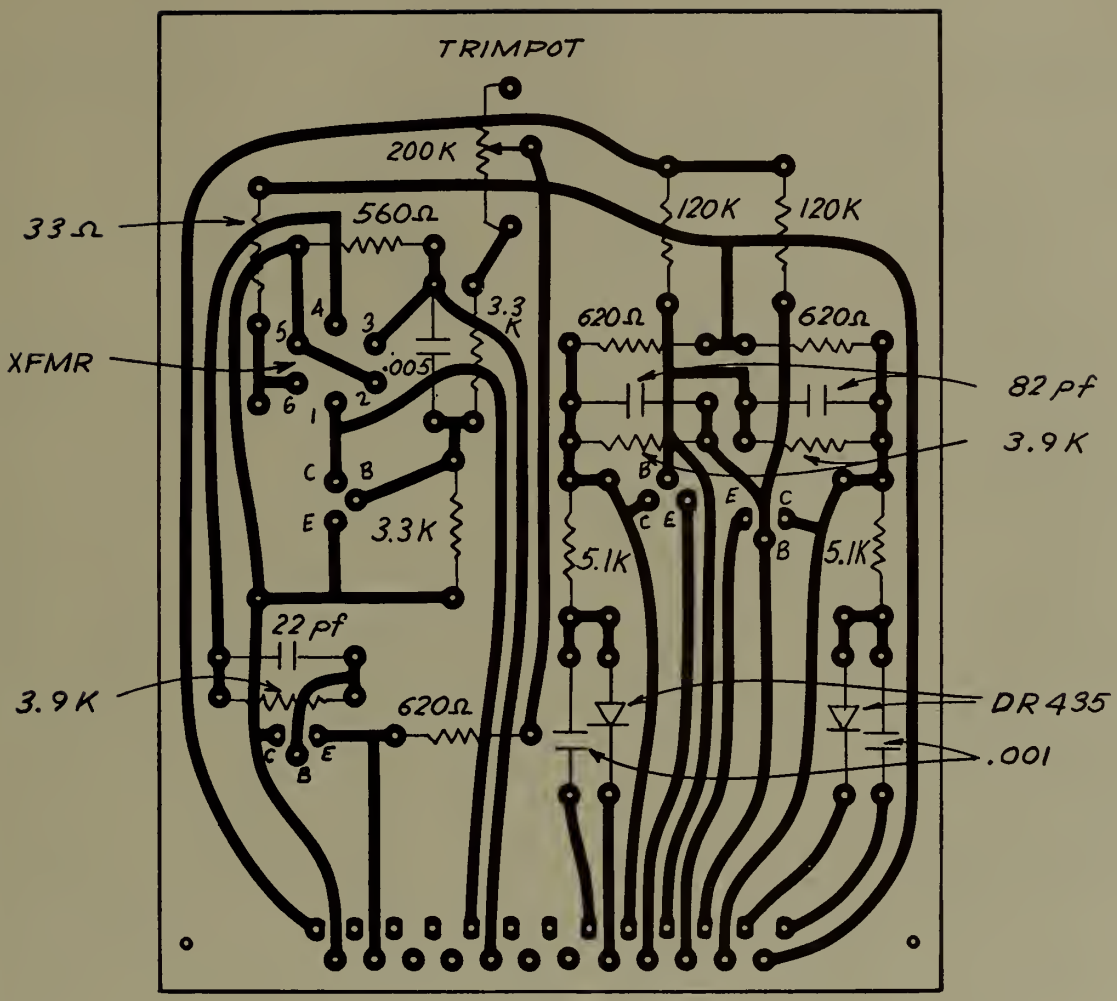


Figure 50. Pulse Generator Package Layout.

U.S. DEPARTMENT OF COMMERCE
Frederick H. Mueller, *Secretary*

NATIONAL BUREAU OF STANDARDS
A. V. Astin, *Director*

THE NATIONAL BUREAU OF STANDARDS

The scope of activities of the National Bureau of Standards at its major laboratories in Washington, D.C., and Boulder, Colo., is suggested in the following listing of the divisions and sections engaged in technical work. In general, each section carries out specialized research, development, and engineering in the field indicated by its title. A brief description of the activities, and of the resultant publications, appears on the inside of the front cover.

WASHINGTON, D.C.

ELECTRICITY. Resistance and Reactance. Electrochemistry. Electrical Instruments. Magnetic Measurements. Dielectrics.

METROLOGY. Photometry and Colorimetry. Refractometry. Photographic Research. Length. Engineering Metrology. Mass and Scale. Volumetry and Densimetry.

HEAT. Temperature Physics. Heat Measurements. Cryogenic Physics. Rheology. Molecular Kinetics. Free Radicals Research. Equation of State. Statistical Physics. Molecular Spectroscopy.

RADIATION PHYSICS. X-Ray. Radioactivity. Radiation Theory. High Energy Radiation. Radiological Equipment. Nucleonic Instrumentation. Neutron Physics.

CHEMISTRY. Surface Chemistry. Organic Chemistry. Analytical Chemistry. Inorganic Chemistry. Electrodeposition. Molecular Structure and Properties of Gases. Physical Chemistry. Thermochemistry. Spectrochemistry. Pure Substances.

MECHANICS. Sound. Pressure and Vacuum. Fluid Mechanics. Engineering Mechanics. Combustion Controls.

ORGANIC AND FIBROUS MATERIALS. Rubber. Textiles. Paper. Leather. Testing and Specifications. Polymer Structure. Plastics. Dental Research.

METALLURGY. Thermal Metallurgy. Chemical Metallurgy. Mechanical Metallurgy. Corrosion. Metal Physics.

MINERAL PRODUCTS. Engineering Ceramics. Glass. Refractories. Enameled Metals. Constitution and Microstructure.

BUILDING RESEARCH. Structural Engineering. Fire Research. Mechanical Systems. Organic Building Materials. Codes and Safety Standards. Heat Transfer. Inorganic Building Materials.

APPLIED MATHEMATICS. Numerical Analysis. Computation. Statistical Engineering. Mathematical Physics.

DATA PROCESSING SYSTEMS. Components and Techniques. Digital Circuitry. Digital Systems. Analog Systems. Applications Engineering.

ATOMIC PHYSICS. Spectroscopy. Radiometry. Mass Spectrometry. Solid State Physics. Electron Physics. Atomic Physics.

INSTRUMENTATION. Engineering Electronics. Electron Devices. Electronic Instrumentation. Mechanical Instruments. Basic Instrumentation.

Office of Weights and Measures.

BOULDER, COLO.

CRYOGENIC ENGINEERING. Cryogenic Equipment. Cryogenic Processes. Properties of Materials. Gas Liquefaction.

IONOSPHERE RESEARCH AND PROPAGATION. Low Frequency and Very Low Frequency Research. Ionosphere Research. Prediction Services. Sun-Earth Relationships. Field Engineering. Radio Warning Services.

RADIO PROPAGATION ENGINEERING. Data Reduction Instrumentation. Radio Noise. Tropospheric Measurements. Tropospheric Analysis. Propagation-Terrain Effects. Radio-Meteorology. Lower Atmosphere Physics.

RADIO STANDARDS. High frequency Electrical Standards. Radio Broadcast Service. Radio and Microwave Materials. Atomic Frequency and Time Standards. Electronic Calibration Center. Millimeter-Wave Research. Microwave Circuit Standards.

RADIO SYSTEMS. High Frequency and Very High Frequency Research. Modulation Research. Antenna Research. Navigation Systems. Space Telecommunications.

UPPER ATMOSPHERE AND SPACE PHYSICS. Upper Atmosphere and Plasma Physics. Ionosphere and Exosphere Scatter. Airglow and Aurora. Ionospheric Radio Astronomy.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