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Measurement Methods for the Semiconductor Device Industry —A Summary of NBS Activity

U.S. DEPARTMENT OF COMMERCE
NATIONAL BUREAU OF STANDARDS

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Foreword

The work reported in this technical note resulted from the efforts of many NBS staff members. J. C. French has been instrumental in all phases of the activity since its inception. F. H. Brewer and Dr. L. J. Swartzendruber carried out much of the work on the resistivity project. H. A. Schafft conducted the projects on second breakdown and resistivity inhomogeneity. The germanium program was begun in cooperation with Dr. J. A. Coleman; significant contributions have been made by W. K. Croll, Dr. A. H. Sher, and W. R. Thurber. R. L. Mattis and Dr. W. E. Phillips carried out much of the work on the lifetime project. Present project responsibilities are identified in the Quarterly Progress Reports for the present program on Methods of Measurement for Semiconductor Materials, Process Control, and Devices (see reference 33).

Acknowledgement is made to various other agencies which sponsored portions of the work: Advanced Research Projects Agency (resistivity), Air Force Materials Laboratory (lifetime), Arms Control and Disarmament Agency (germanium), Atomic Energy Commission (germanium), National Aeronautics and Space Agency (resistivity), and Rome Air Development Center (inhomogeneities, second breakdown).

In addition it must be emphasized that success of both past and present projects depends on the cooperation which has been obtained from industrial members of the various standards committees in which project staff are participating.

Measurement Methods for the Semiconductor Device Industry - A Summary of NBS Activity

W. Murray Bullis

Work at NBS which led to the development of a broad program on Methods of Measurement for Semiconductor Materials, Process Control, and Devices is described. Initial work was concentrated on resistivity of silicon wafers and second breakdown in transistors. In the first case, the basis for a significant improvement in the method for measuring resistivity of silicon wafers was established, and in the second, concepts were developed which formed the basis of a new type of specification for operating conditions free from second breakdown. Work was extended to include other projects, including studies of germanium for gamma-ray detectors, carrier lifetime, and resistivity inhomogeneities which are still in progress. Formation of the broad program in response to increased interest in improved measurement methods is described.

Key Words: carrier lifetime; germanium; lithium-drifted gamma-ray detectors; resistivity; resistivity inhomogeneities; second breakdown; silicon.

1. Introduction

The semiconductor device industry is one of the most technologically advanced industries in the world. The properties of these devices depend on the presence of exceedingly small but controlled amounts of impurities in some of the purest and most perfect crystalline material known to man. Not only the amount of impurity but also its spatial location must be controlled to exceedingly fine dimensions. Although much sophisticated technology is employed, the manufacture of semiconductor devices is still done on a batch basis. The basic unit in the process is a slice or wafer of semiconductor material. From each wafer one or many thousand devices may be fabricated depending on the use and size of the device. Many steps in the processing, particularly the assembly and packaging operations, are still done by hand.

The manufacturing process is exceedingly complex; many chemical, metallurgical, and mechanical steps are involved. The measurement requirements in such processing can be grouped into three broad areas. First is acceptance of incoming materials which include the semiconductor wafer itself; processing materials such as water, acids and solvents, carrier and doping gases, and photoresists; and the materials used in assembly and packaging of finished devices. Next is the actual fabrication of the device. The widely used epitaxial, planar process, for example, involves vapor deposition of single crystal material; oxidation; selective etching of the oxide by means of photolithographic techniques;

selective high-temperature, solid-state diffusion of impurities to controlled depths; evaporation of metals to form interconnections; assembly; and packaging. Each individual step must be closely controlled in order to obtain the desired device at the end of the line. Finally, it is necessary to test the finished device in order to determine that the desired characteristics have been achieved and also to establish some measure of the expected life of the device.

The Electronic Technology Division has been concerned with the first and last of these areas for some time. Recently, increased demands for improved device performance in terms of operation at higher power levels, at higher frequencies, and with greater reliability under both normal and abnormal conditions have led to increasingly severe control requirements at all stages in device processing. This in turn has led to a need for improved measurement methods throughout the manufacturing process.

This note describes the two projects with which the division's involvement in this measurement area began. Growth of the program in order to meet present requirements and the new activities now in progress are also discussed.

2. Resistivity

In 1960, NBS was asked by Committee F-1 on Materials for Electron Devices and Microelectronics of the American Society for Testing and Materials (ASTM) to investigate the problems associated with the measurement of silicon wafers. Resistivity of wafers is the most important parameter in the exchange of silicon and germanium across the interface between crystal grower and device manufacturer. The importance of this parameter arises from the fact that for device-quality silicon and germanium there is a well-documented relationship between resistivity and impurity concentration in the region of room temperature.[1,2] The free carrier concentration which is the important consideration in device design is controlled by the concentration of impurities in the semiconductor.

Although the measurement of resistivity is relatively simple and adaptable to production processes, problems and disagreements had plagued the industry for some time. Two methods of measuring the resistivity were in common use. The four-probe method[3] was the preferred one since it was not necessary to cut a particularly shaped sample in order to make the measurement. In this method, four equally spaced point contacts are placed on a flat surface of the material as shown in Fig. 1a. A current, I, is passed through the outer pair of contacts and the potential difference, V, across the inner pair is measured with a sensitive, high-impedance voltmeter. The resistivity may be calculated from:

$$\rho = \frac{V}{I} 2\pi s, \tag{1}$$

where s is the spacing between adjacent probes, if the specimen is a semi-infinite sample. If measurements are made on wafers of finite dimensions, additional correction factors must be included in order to account for thickness and diameter. An additional factor to allow for unequal probe spacings may also be included.

In the two-probe method[4] a specimen is cut from the crystal in the form of a rectangular parallelepiped as shown in Fig. 1b. The contacts through which the current, I, passes are plated with a metal so that each end of the specimen is an equipotential plane. The potential difference, V, between a pair of point contacts placed a distance, ℓ, apart is measured and the resistivity calculated from:

$$\rho = \frac{V}{I} \frac{wt}{\ell}, \qquad (2)$$

where w and t are the width and thickness of the specimen.

Despite the preference for the four-probe method, it was generally believed in the industry that the two-probe method was the more precise. It was proposed therefore that NBS should certify standards of semiconductor materials of various resistivities as determined by the two-probe method and furnish them for use in calibrating four-probe systems in the field. Calibration standards with 1 per cent accuracy were expected to be satisfactory.

Because two-probe and four-probe measurements were to be compared, it was first necessary to solve the potential distribution problem encountered in making four-probe measurements on thin, rectangular wafers. These correction factors could not be obtained in closed form, so computer programs for the computation of correction factors for a variety of circumstances were developed and published.[5] Differences in the results obtained from the two-probe and four-probe measurements led to a study of the homogeneity of silicon wafers.

In order to carry out this study without having to cut rectangular samples in each case, correction factors for off-center measurements in circular wafers were calculated in detail. Again these correction factors could not be obtained in closed form, but detailed tables of their value for the cases of interest were calculated and published.[6] In addition to their application in the study at hand, these tables proved to be extremely useful to the industry as a whole; more than 1500 copies of the technical note containing them have been distributed, and they have been widely reprinted and distributed by material manufacturers themselves.

The identification of the homogeneity problem led to an analysis of the effect of inhomogeneities on four-probe measurements.[7] Calculations were carried out for several idealized models which consisted of a circular region with resistivity $\rho + \Delta\rho$ embedded in a thin sheet of infinite extent with resistivity ρ.

It was concluded that the specimen uniformity available at the time was inadequate to provide certified standards of the precision that the industry desired. It was also found during these experiments that the reproducibility of measurements by the four-probe method appeared to be as good as that which could be obtained with the two-probe method. Therefore the goals of the project were reoriented toward the development of a four-probe method with procedures and conditions-of-measurement which were sufficiently well defined that the reproducibility desired by the industry could be obtained.

Detailed experiments on various aspects of the four-probe method were carried out. The effects of variations in probe force, surface roughness, and point material were investigated. From the results of these experiments it was possible to specify optimum surface preparation procedures and point contact characteristics. It turned out that tungsten carbide points applied with a load of 175 grams on a surface lapped with 5 µm abrasive gave satisfactory results without undue point wear or probe wander.

The probe wander which results from several circumstances is worthy of special consideration. A photograph of a typical probe is shown in Fig. 2. The construction is such that four independently sprung pointed wires are guided in hard bearings. Typically the spacing between the centers of adjacent probe points is 1.6 mm. Therefore a variation in position of only 16 µm represents a 1 per cent change in probe spacing. Some freedom must be allowed the probes in order for them to glide up and down within the bearings as the probe assembly is applied to the specimen surface. If this freedom is too great, excessive wander will take place. Furthermore, if the direction of travel of the probe as it is applied to the specimen is not exactly perpendicular to the surface, some gliding along the surface will take place. The probe wander associated with a good probe is less than 0.3 per cent of the mean probe spacing. Additional wander may be expected if the specimen surface is exceedingly rough. The points may then slide down hills which they encounter on being applied to the surface of the specimen. Hence, the need for lapping with fine abrasive.

A second criterion for probe quality is equality of the probe spacing. A test in which the imprint of the probes on a polished silicon wafer is measured was developed in cooperation with ASTM Committee F-1 to enable the operator to verify the quality of his own probe both as to probe wander and probe spacing. To allow for unequal probe spacing, a correction factor, which could be calculated by the operator for his probe and applied to the results of his measurement, was developed for the case of measurements on thin wafers.

In addition, a test for the quality of the electrical measuring circuit both as to accuracy and input impedance was developed. This test involved the use of large resistors in series with a standard precision resistor in order to simulate both probe contact and specimen bulk resistances. Test circuits with the standard resistor equal to 0.1, 0.01, and 0.001 Ω were designed and constructed as part of the project. Larger standards were assembled from commercially available components.

Another factor to be considered was the temperature dependence of the resistivity. When measurements are made at room temperature it is often naively assumed that the temperature of the room is sufficiently well controlled that no further control is necessary. Unfortunately, this is not usually the case. Imposition of a requirement that the measurements be made at some specified, fixed temperature would considerably reduce the flexibility and ease with which the measurement could be made. Since it was found that a thin wafer of silicon or germanium placed on a massive copper block assumes the temperature of the block in a very short time---the order of half a minute or so---even if it is electrically isolated from the block by a thin sheet of mica, it was concluded that if such a heat sink were employed and if its temperature were measured at the time of the resistivity measurement one would know the temperature of the wafer.

Detailed studies of the temperature variation of resistivity of silicon and germanium showed that over the temperature range between 18 and 28°C it was possible to fit the resistivity-temperature curve for extrinsic specimens with a straight line. In such cases, a linear temperature coefficient was obtained which the operator could use to correct resistivity measured at a temperature t in this range to a reference temperature which was selected as 23°C.[8] It was found that the linear temperature coefficients for both silicon and germanium were 1 per cent per degree or less. Linear temperature coefficients could not be obtained for germanium with resistivity greater than a few ohm-centimeters because of the influence of carrier pairs thermally generated across the forbidden gap (intrinsic conduction).

An improved test method based on these findings was prepared in cooperation with ASTM Committee F-1.[9] During the preparation of the method several round-robin tests were conducted by the Committee to establish the precision which could be achieved.[10] In the first of these, a few silicon wafers with resistivity in the range of 10 Ω-cm at room temperature and of as good a uniformity as could be obtained were selected and circulated among five groups experienced in precision measurements of resistivity. In order to reduce the number of variables as much as possible and to establish the validity of the test for the quality of the probe, a probe was included with the samples so that everyone in the test used the same mechanical equipment. In each case a standard deviation less than 1 per cent was achieved. In 1967, a second round-robin test was conducted. This time wafers with resistivities between 0.01 and 1000 Ω-cm were included. All of the experienced laboratories obtained values which gave a standard deviation less than 1 per cent on all wafers except an inhomogeneous 1000 Ω-cm specimen. Inexperienced laboratories participating in a parallel round-robin test encountered numerous difficulties principally centered about sensitivity and accuracy of their electrical measuring equipment.

The results of several round-robin tests made in the last decade are summarized in Fig. 3. The data included are for samples with resistivity of 100 Ω-cm or less. The 1967 data are based on the results of the round robin among experienced laboratories. The beneficial effects of including controls for environmental conditions and tests for both probe and electrical measuring systems are evident since these were included only on the 1967 round robin.

While the method was being improved, a direct-reading apparatus, which contained circuits to compensate for the diameter, thickness, and off-center correction factors was designed and built. This instrument, shown in Fig. 4, permits measurements to be made with a precision of 5 per cent or better over a wide range of geometrical conditions.[11] Corrections for both temperature and unequal probe spacing could easily be added to the system. Another output of the project was a comprehensive bibliography of methods of measurement of resistivity which was compiled in 1964.[12]

At the present time additional work is being carried on in cooperation with ASTM Committee F-1 to extend further the range of applicability of this method. In addition, studies are being made of the effect of relaxation of certain of the test conditions so that the method may be applied in circumstances other than the testing of bulk silicon wafers. For example, in the measurement of diffused layers one requires that the measurement be made on whatever surface one obtains after the diffusion process takes place. Similarly, measurements on epitaxially deposited layers require that the measurement be made on the shiny surface which results after the epitaxial growth process. Application of this method in these important areas of process control is extremely important to the industry.

3. Second Breakdown

At about the same time that the Resistivity Project was undertaken NBS was asked by Committee JS-6 on Power Transistors, of the Joint Electron Device Engineering Councils, to investigate problems associated with the phenomenon later to be known as second breakdown. In transistors, where second breakdown was first identified, its initiation is characterized by a sharp decrease in the voltage between the collector and emitter together with a constriction of the current in the transistor.

The three regions of a transistor---emitter, base, and collector---are doped in such a way that rectifying *p-n* junctions occur between each pair of regions. In normal operation, the emitter-base junction is biased in the forward or conducting direction and the collector-base junction in the reverse or blocking direction. Most of the minority carriers, which are injected from the emitter to the base, diffuse through the base and are collected in the collector to form a current in the collector circuit. A small fraction of these carriers recombines in the base with majority carriers to form a very small current in the base circuit. This is the normal or amplifying mode of operation of the transistor. In this mode the collector current is controlled by the much smaller base current and, above a rather small collector-emitter voltage, is essentially independent of voltage for a given value of base current. If the emitter-base junction is reverse biased, then the current in the collector circuit is usually very small until a voltage is applied across the collector-base junction which is high enough to cause a sufficiently large avalanche multiplication current. The transistor is then said to be operating in the avalanche breakdown mode. If the voltage in the collector circuit is increased further, the collector-base voltage will initially decrease and then approach a constant value as the collector current continues to increase. When the collector current reaches a value, usually called I_m, the collector-base voltage decreases sharply. Further increases in the collector current occur as a result of this decrease and the finite resistance in the collector circuit. Since this decrease in collector-base voltage occurs after the first or avalanche breakdown, the phenomenon associated with the second change of voltage was called second breakdown. It was later observed that second breakdown could also occur in a transistor with zero or forward base-current drive, as shown in Fig. 5, and in diodes.[13] It was also found that rather than being unique, I_m depended on the operating conditions of the transistor.

Although a transistor is not necessarily harmed by an excursion into second breakdown, irreversible damage can occur if the current is sufficiently large. The characteristic catastrophic failure mechanism is a collector-to-emitter short circuit which arises because the current tends to become localized in a small region of the transistor which is then melted by the large localized dissipation of power. At the time NBS was asked to investigate the problem a number of conflicting models for second breakdown had been proposed and it was impossible to specify operating conditions which would avoid the phenomenon.

As with the resistivity project, work began with visits to various companies interested in the problem in order to establish its extent and the scope of effort which would be required. Initial experimental work demonstrated that all the existing models were inadequate to explain the effect and showed that second breakdown was a characteristic of all transistors.[13] Pulse measurements of second breakdown revealed the existence of a delay time between the start of the pulse and the initiation of second breakdown as shown in Fig. 6. This observation led to the concept of a triggering energy for second breakdown dependent on the operating condition of the transistor which formed the basis of a new type of specification for maximum operating conditions free of second breakdown.[14,15] This type of specification is now almost universally used in the industry. In Fig. 7, which shows the essential features, the maximum safe dwell times are given for the amplifying mode of operation of a transistor. The operating limits governed by the lines with a slope of -1 show where the transistor is limited by straightforward thermal considerations. Regions where the slope is steeper are those where the transistor is second breakdown limited. If most high power and high frequency transistors are to be utilized at all realistically, they must be operated under conditions where second breakdown could occur if certain precautions were not observed. Thus, as capabilities of transistors have been extended in power and frequency these specifications have increased in importance.

Some of the work which was carried out during this project was directed toward better defining the conditions under which second breakdown can occur. Observations of the current distributions in transistors under various conditions of operation were made with the use of temperature-sensitive phosphors.[16] The temperature of the device will increase in areas of high current density. The current constriction associated with second breakdown was demonstrated by these experiments. It was also shown that the site of the constriction occurs in a region of high current density which can result from various types of structural irregularities in the transistor. Some of the structural irregularities that can significantly alter current distributions are localized regions of reduced base width,[17] regions of reduced collector avalanche breakdown voltage, poor or nonuniform heat sinking of the transistor wafer, diffusion-induced dislocations,[18] and precipitates.

Despite the better characterization of the phenomenon, improved specifications for avoiding it, and the development by the industry of device designs and circuit conditions which reduce the incidence of second breakdown, the problem is still not under complete control. Further, because of the complexity of the interacting mechanisms believed to be important, the phenomenon itself is not yet fully understood. Several invited papers have been prepared at various times in the last several years in order to summarize and review the status of the second breakdown field.[15,19,20] In 1967, a comprehensive review[21] and a comprehensive bibliography[22] of work in the field of second breakdown were compiled and published. In addition, tutorial lectures have been presented throughout this period at a number of meetings and liaison has been maintained with Committee JS-6 regarding various aspects of specification and data formats related to the second breakdown problem.

4. New Activities

Specification of Germanium Several years ago the scope of the overall program was expanded in several directions. For some time a group had been engaged in the fabrication of lithium-drifted germanium and silicon nuclear radiation detectors. These detectors are *p-n* junctions which have extremely wide high-resistance region between thin *p*-type and *n*-type layers. This region is formed by the compensation of residual impurities in this volume with lithium atoms. By the end of 1965 serious difficulties in attempting to fabricate lithium-compensated germanium detectors were encountered at many laboratories. The origin of the difficulties was traced to the starting materials used in the fabrication of the devices, but the exact cause was not identified. Although suitable material, primarily from foreign suppliers, has subsequently become available, neither the cause of the past trouble nor a satisfactory means of identifying "poor" quality material prior to the drifting of lithium has been discovered. The problem, then, was one of developing specifications for germanium material which could be used in selecting this material for application to lithium-drifted detectors.

Only a few properties were customarily specified at the time of the start of this program. These included room temperature resistivity, dislocation density, and minority carrier lifetime as determined from measurement of photoconductive decay. It was apparent that knowledge of these few properties was not sufficient to discriminate between good quality and poor quality crystals. A series of isolated experiments at various laboratories had suggested that some other parameters such as lithium precipitation rate[23] or low-temperature electron drift mobility[24] might be correlated with material quality. The approach[25] adopted was to characterize a sizable group of germanium crystals as fully as possible with respect to the standard parameters such as resistivity, etch pit density, and lifetime as well as other parameters such as Hall mobility at various temperatures, electron drift mobility at liquid nitrogen temperature, infrared absorption due to interstitial oxygen, and lithium precipitation and drift rates. After a detector was fabricated from the characterized crystal by means of a standardized procedure, its performance was determined by measuring a number of device characteristics such as leakage currents, noise, capacitance, energy resolution, and charge collection efficiency, in order to determine whether correlations exist between detector quality and initial material properties.

In addition to the experimental work now going on, ASTM Committee F-1 was assisted in setting up a task force to study germanium properties. This task force is now developing a standard method for measuring the drift rate of lithium in germanium. In its original version, this procedure required a drift time of 100 hours or more. A new version of the method is being prepared to incorporate findings from experimental work at NBS[26] which enable one to predict the mobility from the measurement of junction capacitance during the first few hours of the drift. It was also shown that characteristics previously attributed to low drift mobility of the lithium ion may also be caused by precipitation of lithium atoms during the drifting process. The questions related to the specification of germanium for this application are not completely resolved at the present time and it is expected that considerable additional work will need to be done.

Carrier Lifetime In 1966, a second project was undertaken in order to study the relevance of the existing standard method for measuring carrier lifetimes in semiconductors--the method of photoconductive decay.[27] In this method, carriers in excess of the equilibrium density are generated in a block of semiconductor material by means of a pulse of light of sufficient energy to excite electron-hole pairs across the forbidden energy gap. After the pulse is abruptly terminated, the decay of conductivity is measured. The time constant of this decay is associated with the time constant of the decay of the excess carriers. In cases where each electron recombines directly with a hole, the determination of lifetime is unambiguous. On the other hand, if the recombination takes place through impurity centers and if the charge density of the impurity center population changes during the recombination process, then the electron and hole lifetimes need not be the same. Under these circumstances the decay time associated with the photoconductivity may be different from the lifetimes associated with either carrier population. Since this mode of recombination--through impurity centers--is the prevalent one in both germanium and silicon, the possibility that the photoconductive decay technique is not measuring the true lifetime of the minority carrier, is a real one. Since it is the minority carrier lifetime that is important in the operation of junction devices it is desirable to establish convenient ways of measuring this quantity more directly.

In the project attempts are being made both to define better the conditions appropriate to the measurement of the photoconductive decay time and to establish other means for measuring lifetime. Experimental work on several aspects of the diode recovery technique, on the spectral dependence of the surface photovoltage, and on steady state photoconductivity and photomagnetoelectric effects has been initiated. The output of the first phase of this project has been a preliminary delineation of the conditions which affect photoconductive decay measurements[28] together with a comprehensive bibliography on methods of measuring minority carrier lifetime.[29] The second phase of the project, which is now in progress, involves further delineation of the characteristics of the photoconductive decay method together with measurements which enable the results obtained by the various techniques to be compared.

Resistivity Inhomogeneity A third project was designed to investigate the homogeneity of silicon wafers. As larger and larger areas of a single wafer are utilized for high power devices, nuclear radiation detectors, or large area integrated circuits, homogeneity of the material becomes more and more important. Since the most important single characteristic is the resistivity, work was undertaken to establish ways of determining resistivity homogeneity on semiconductor wafers. This had been done previously with the four-probe method but it had been shown that this method is not sensitive to variations which occur over regions with linear dimensions smaller than about one-fourth the probe spacing.[7] A number of years ago a photovoltaic method was introduced for use on thin germanium filaments.[30] The initial objective of the project was to verify the use of this method on germanium filaments and extend it to silicon filaments. The feasibility of applying this technique to silicon at least on a laboratory scale was demonstrated quite quickly, and it was decided to extend this study to include uncut wafers during the first phase. Detailed analysis of measurements on whole wafers are complicated by the fact that the illuminated portion of the wafer is shunted by unilluminated portions. Since the theoretical analysis of this problem had not yet been carried out, the preliminary experimental results were analyzed by ignoring the shunting effects. Both heavily-doped *p*-type regions diffused into a p-type wafer in specific pattern, and the core which occurs in most high resistivity *n*-type silicon were observed in qualitative fashions. The results[31] obtained in these preliminary experiments were sufficiently encouraging that it was decided to continue the project along these lines. Also as a part of the first phase, a bibliography of methods of measurement of various kinds of inhomogeneities in semiconductor wafers was compiled and published.[32]

Other Areas In the process technology area, facilities are being expanded to include diffusion, sputtering, and photomasking operations in addition to the alloying, evaporation, and contacting facilities which had been required for earlier projects. Studies of various types of measurement techniques for in-process control are being considered.

A major effort has been mounted in the study of methods of evaluating wire bonds to semiconductor wafers. Failure of the bond structure is the largest single cause of the failure of low-power semiconductor devices in high reliability applications. At the request of several other government agencies, detailed studies of measurement methods appropriate to the evaluation of wire bonds were undertaken.

5. Present Program

If high device reliability is required in a system, as for example in military and space applications, some sort of assurance that a particular device will perform adequately must be obtained before the system is assembled. At the present time the most common way of achieving this is with the use of screening tests at the end of the device line. In addition to being expensive, this approach is frequently unsatisfactory since it is virtually impossible to develop tests which will simulate all of the conditions subsequently encountered by the circuit in the field. When one adds to this the possibility of operator error in performing the tests or improper design of test conditions the failure rate observed may be abnormally large.

A broader approach is to develop techniques which will help to build reliability into devices. This approach covers the entire spectrum of device fabrication procedures rather than just a testing sequence on the finished device and forms the basis of the Program on Methods of Measurement for Semiconductor Materials, Process Control, and Devices[33] which is now being undertaken in the Division. The three major tasks of this program are (1) to evaluate the technical adequacy of relevant measurement methods developed in industrial or agency organizations and make recommendations for necessary modifications, (2) to develop specific methods in accordance with the guidance received from participating groups, and (3) to provide to standardizing groups in industry and government agencies such technical or other assistance as is appropriate to encourage rapid development, publication, and implementation of improved measurement method standards.

The concepts and methodology of this program have evolved from the earlier projects described above. One of the key elements is cooperation and liaison with both manufacturers and users. This is essential in the development of realistic, useful standards and is accomplished through participation in technical committees of organizations such as the ASTM and the Electronic Industries Association, through consultations with and sponsorship from various government agencies, and through personal contacts in industrial plants and government laboratories. These contacts also serve to provide project staff members with a broader view of the problems faced by industry and help in insuring that the output of the projects will be usable in the field.

It is possible to select only a few properties for detailed study. The primary objective of such study is the development of a technical basis for a standard method for measuring the property to an established precision. Since existing methods form the basis of these studies, an important step taken soon after a study begins is a thorough review of the state-of-the-art. Based on this review particular methods are selected for detailed investigation. In addition bibliographies on methods of measurement of a given property and summary review papers are prepared as may be appropriate. Because the program is rather small when considered relative to the total R & D capability of the semiconductor device industry, the areas which must be emphasized are those where considerable leverage can be applied and the value of the work extended beyond direct application of the results of specific experimental investigations.

In the case of the resistivity project, the usefulness of the method to the industry has been documented in a benefit-cost analysis conducted in 1967 as part of a Bureau-wide study. Improvements in other measurement techniques are expected to yield corresponding value to manufacturers and users alike and will assist in solving the problem of securing high reliability devices for specialized applications.

6. References

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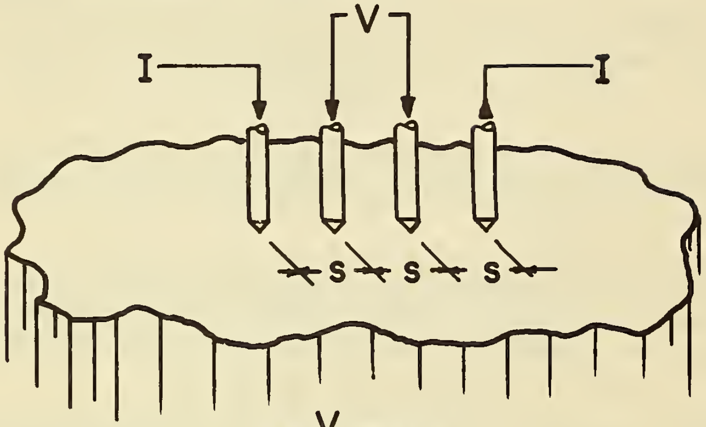
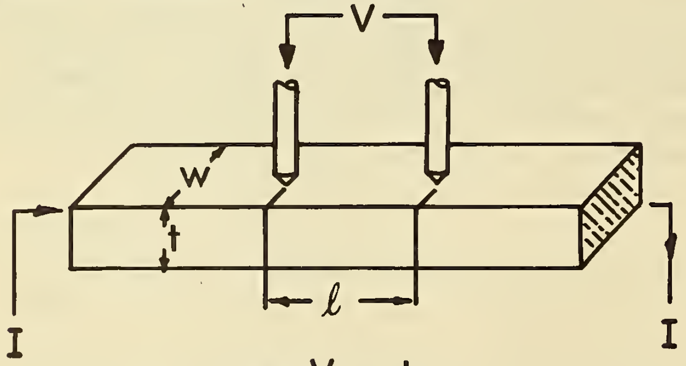
(a) FOUR-PROBE METHOD



$$\rho = \frac{V}{I} 2\pi S$$

(b) TWO-PROBE METHOD



$$\rho = \frac{V}{I} \frac{wt}{\ell}$$

Where:

ρ = Resistivity
V = Potential Difference
I = Current
S = Probe Spacing
w = Width
t = Thickness
ℓ = Length

Figure 1 - Geometrical Arrangements for Four-Probe and Two-Probe Methods for Measuring Resistivity of Semiconductor Crystals.

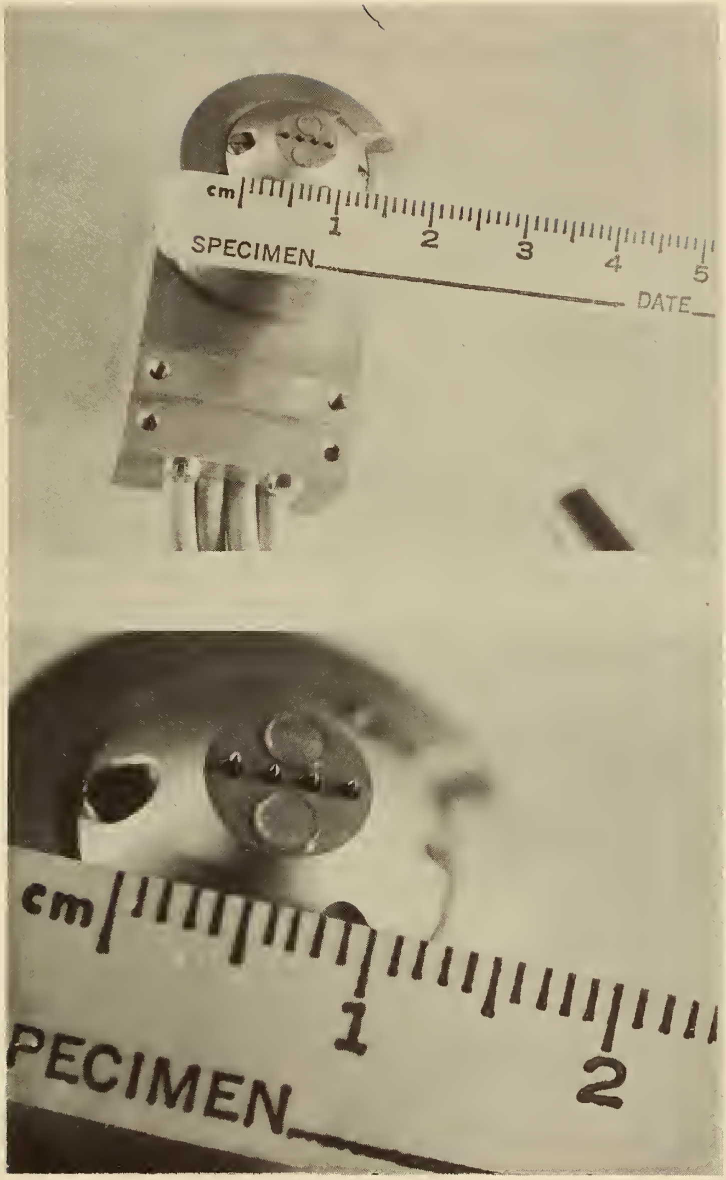


Figure 2 - Typical Four-Point Probe with 1.6-mm Spacing.

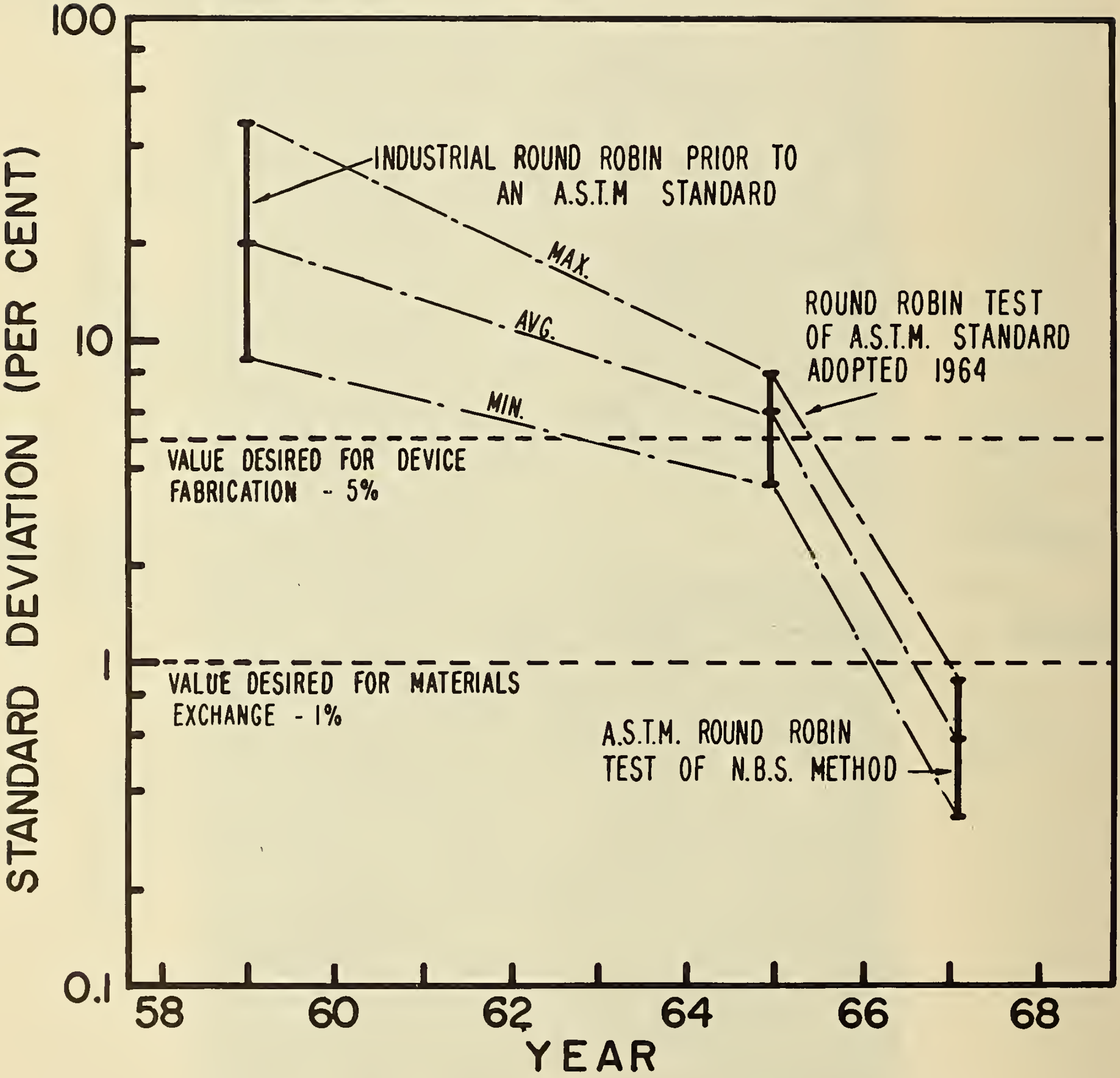


Figure 3 - History of the Interlaboratory Precision of Measurement of Silicon Resistivity in the Range 0.01 to 100 Ω-cm, by the Four-Probe Method, Showing the Spread of the Sample-Dependent Standard Deviations by the Vertical Bars.

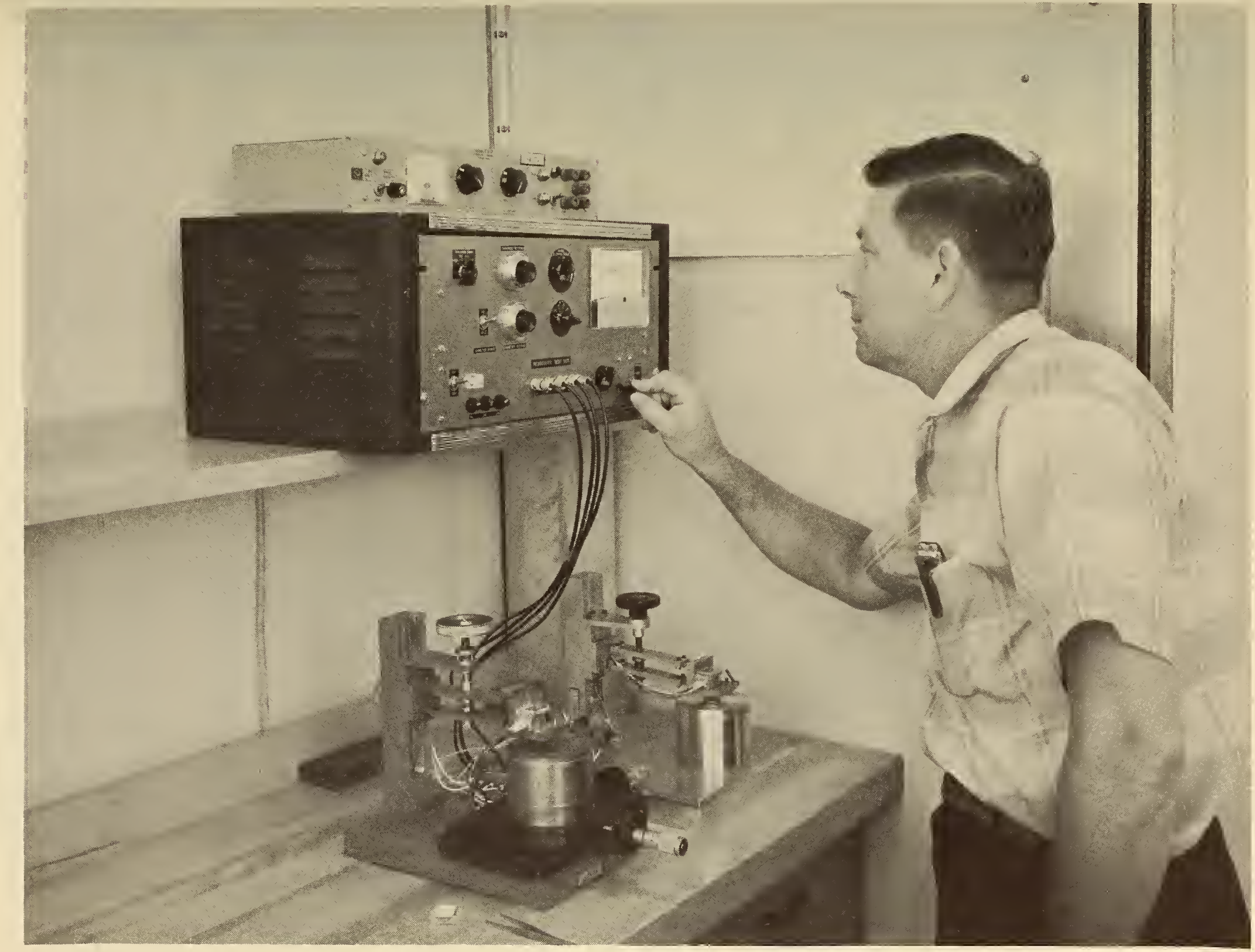


Figure 4 - Direct-Reading Four-Probe Apparatus.

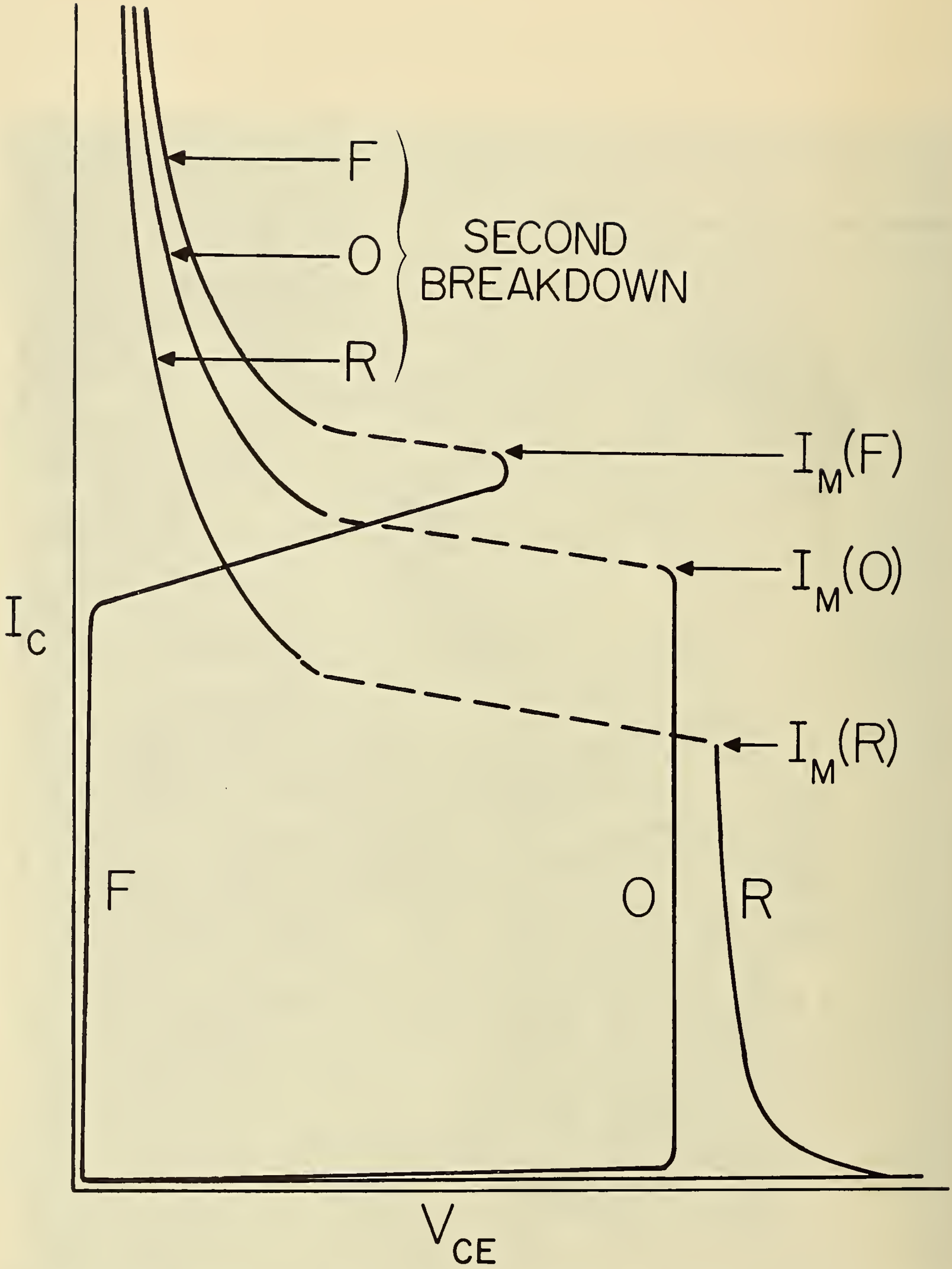


Figure 5 - Sketch of the swept V_{CE} - I_C characteristics of a transistor with constant forward (F), zero (0), and reverse (R) base current drive. The characteristics are drawn for only the first half of the sweep cycle. Second breakdown is initiated at currents $I_M(F)$, $I_M(0)$, and $I_M(R)$.

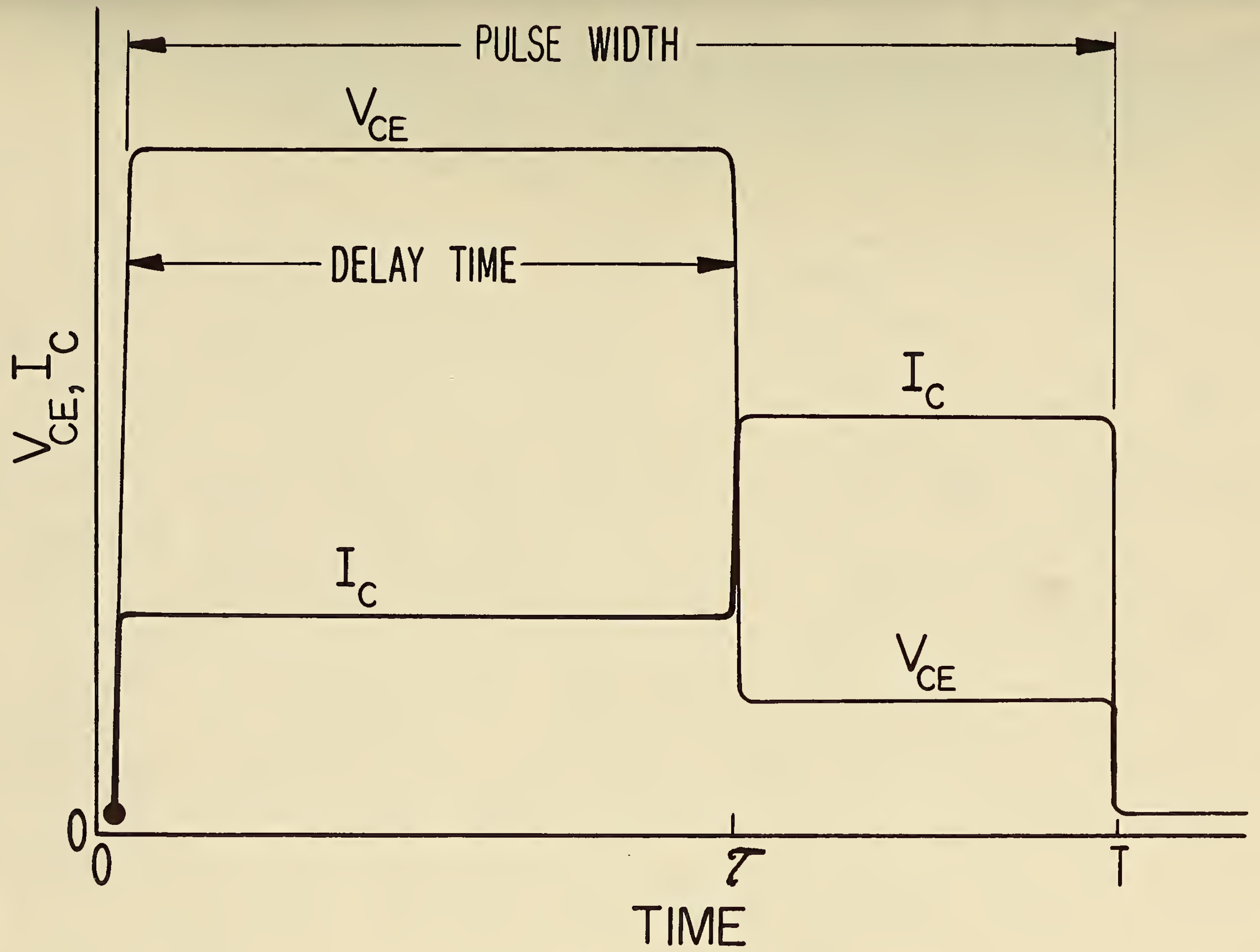


Figure 6 - Sketch of V_{CE} and I_C as a function of time while a rectangular voltage pulse of duration T is applied to the collector. Second breakdown is initiated at time τ.

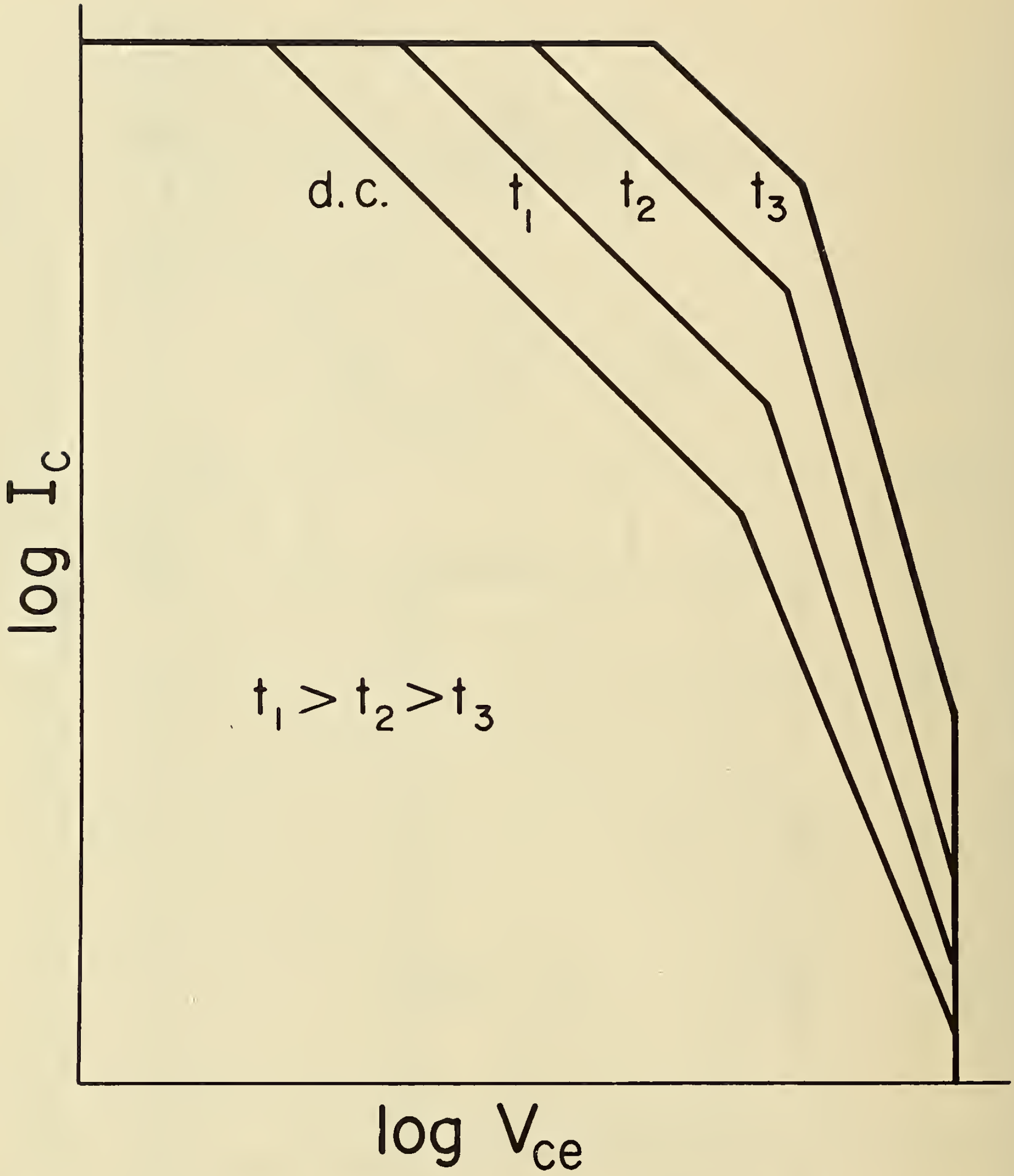


Figure 7 - A presentation of safe areas of operation for forward-base drives indicating the regions safe for dc operation and for pulsed operations with dwell times t_1, t_2, and t_3. Logarithmic scales are used to show more clearly the voltage range over which the transistor is thermally limited in the usual sense (where the slope of the line has a vlue of -1) and the range over which the transistor is second-breakdown limited.

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