NBS TECHNICAL NOTE

371

Transistorized Low Voltage Regulator Circuits and Design

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TRANSISTORIZED LOW VOLTAGE REGULATOR CIRCUITS AND DESIGN

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TABLE OF CONTENTS

FIGURES

TABLES

TRANSISTORIZED LOW VOLTAGE REGULATOR CIRCUITS AND DESIGN

John H. Rogers

Simplified design equations and circuits are presented for three separate transistor voltage regulator circuits covering the range of 2 to 30 volts. Examples of design, use of equations, selection of components and performance data are presented. An appendix is included to show the use of recent integrated circuit (I. C.) voltage regulators.

1. INTRODUCTION

With the increased use of transistor circuitry, both discrete and integrated, the need for regulated low voltage power supplies is most urgent. Often the regulated power supply will cost several times the price of the circuit to be powered.

The purpose of this Tech Note is to give reasonably simple and workable design equations and to show experimental results for several transistorized voltage regulator circuits. Three complete designs are shown, giving low, medium, and high gain operation of each regulator circuit. It is hoped that these circuits will be an aid to the scientist, engineer, and technician by making it possible to put together voltage regulated power supplies with a minimum of design and construction time. All the designs presented use standard components which are easily obtained.

Design equations for voltage regulator circuits are available in many different textbooks and manuals; however, several such texts are often needed to get a clear picture of the procedure and proper equations to use. This report has condensed and organized the design equations. The calculations have been kept simple by proper choice of design equations and by the inclusion of one variable resistor to compensate for the difficulty of obtaining the exact value of the resistor calculated. This allows the designer to select the nearest standard value of resistance, plus or minus, except when there is the notation $\geqq$ or $\leqq$. To precisely determine the value of each resistance in the circuits to be presented would require more involved calculations; the present method was adequate in all ten cases tried. Each circuit was tested at 23°C and found reliable. The design equations do not take into consideration extremes in ambient temperature variations. If extremes in temperature above or below 23°C is expected then further testing is recommended.

A voltage regulator must of necessity be preceded by a source of d-c voltage. This report will assume the source to be a full wave bridge rectifier shown in Figure 1. The transformer is chosen to supply the necessary power (voltage and current). The voltage output, under load, should be 3 to 6 volts a-c more than the desired regulated output d-c voltage. The designs to be presented indicate the transformer voltage used.

The amount of ripple voltage that can be tolerated at the output of a regulator circuit must be determined by the designer. If the circuit selected from this report shows the ripple content to be too high, then more filtering between the voltage source and voltage regulator is necessary. Usually this can be accomplished by increasing the size of C_1 in any one of the regulator circuits shown. In extreme cases it may be necessary to replace C_1 with a capacitor-resistor π type filter. However, the value of C_1 cannot be increased to the point where charging current through the rectifier diodes exceeds the diode peak current rating. This can be recognized by large spikes at the input to the regulator circuit instead of the normal ripple voltage.[1] Should large spikes occur, a small resistance ($<10\Omega$) may be placed in series with the diodes to increase the forward resistance and thereby decrease peak charging current.

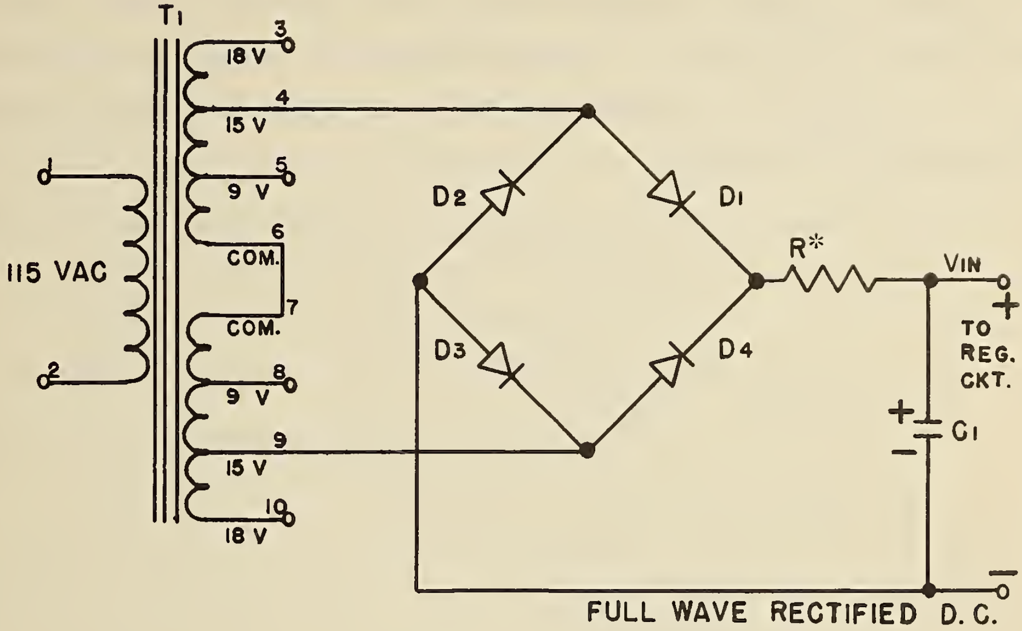


Figure 1. Full Wave Bridge Rectifier Circuit

* R = 0 to 10 Ω, See text.

T_1 = TE, No. 801000.

D_1, D_2, D_3, D_4 = 1N4004 for output current < 0.5 amp.

D_1, D_2, D_3, D_4 = 1N1613 for output current > 0.5 amp.

C_1 = as noted in Text.

2. REGULATOR CIRCUIT NO. 1

The basic regulator circuit shown in Figure 2 is recommended because of its simplicity. The measured performance is tabulated in Table I. The design can be used for output voltages of 6 to 30 V at output currents up to 0.5 amps.

The approximate design formulas used to determine the value of the various resistors are as follows:

$$R_1 = \frac{V_o - V_{Z1} - V_{BE2}}{I_{divider}}$$

$$R_2 = \frac{V_{BE2} + V_{Z1}}{I_{divider}}$$

$$R_P = 0.1\ R_2 \text{ (see text page 7)}$$

$$R_3 \geqq \frac{Vin_{min} - V_{Z1}}{I_{C2} + I_{B1}}$$

$$R_4 + R_5 + R_6 \geqq \frac{Vin_{min} - V_{Z1}}{I_Z - I_{C2}}$$

where the symbols used above and in subsequent formulas are defined in Appendix B.

In the above equations the leakage current I_{CO} has been purposely left out. This is permissible at room temperatures but not at elevated temperatures. Besides the above shown formulas, there are calculations to determine base currents and collector currents of the transistors, these will be shown in an actual design example.

Before the formulas can be used, the following decisions must be made:

a. Output voltage and current, V_o and I_o.

b. Minimum input voltage, Vin_{min}.

c. The h_{FE} or d-c gain and power rating of the transistors to be used at the operating current.

d. Zener diode (Z_1) breakdown or regulating voltage V_Z.

The minimum input voltage (see Figure 1) should be at least 3 volts greater than the desired V_o. This is assuming that the capacitor C_1 can adequately filter the large a-c ripple.

Values of h_{FE} for the transistors used throughout are tabulated with each circuit diagram. These are typical values only, arrived at through experience and are suitable for the current levels (I_C) indicated in the text at 23°C. Appendix B shows the maximum and minimum values of h_{FE} that can be encountered, however the manufacturers specification sheets should be consulted if wide temperature variations are expected. An advantage of the designs presented is that the resistor networks make the precise value of h_{FE} less important.

The regulating voltage V_Z of the zener diode, or breakdown voltage, should be, if possible, in the range of 5 to 6 volts in order to take advantage of the near-zero temperature coefficient. Also for this type circuit,[2] Z_1 should regulate at lower voltage than the desired output voltage. Ordinarily a zener of 5 to 6 volts can be used, but when a lower output voltage is desired, the forward drop across a silicon diode (or several in series) is recommended. The low voltage zeners (around 2 volts) are not recommended in this application.

As an example, the formulas will be used to show the design of a regulator circuit to provide an output voltage V_o of 6 volts, with an output current I_o of 100 mA. The minimum input voltage Vin_{min} will be 9 volts, Q_1 is a TIP24, and the typical h_{FE} at 100 mA is 50:

$$I_o = I_{C1} = 100 \text{ mA},$$

$$I_{B1} = I_{C1}/h_{FE1} = 100 \times 10^{-3}/50 = 2 \text{ mA}.$$

Q_2 is a 2N3904 and must supply at least 2 mA to Q_1 as noted above, and the h_{FE} is typically 100. It is necessary for good control that the I_{C2} be greater than the I_{B1} of Q_1; assume two-times greater:

$$I_{C2} = 2I_{B1} = 4 \text{ mA} .$$

The base current for Q_2 is calculated as

$$I_{B2} = I_{C2}/h_{FE2} = 4 \times 10^{-3}/100 = 0.04 \text{ mA}.$$

For good stability the current through the divider R_1, R_2 must be greater than the base current of Q_2 (I_{B2}). How much greater depends largely upon the magnitude of the output current (I_o). The following rules have been used and found to be satisfactory for determining or setting the value of divider current:

$I_{divider} = 0.5$ mA or $20\ I_{B2}$, whichever is greater when $I_o \leqq 500$ mA;

$I_{divider} = 50\ I_{B2}$, when $I_o > 500$ mA;

here, $20\ I_{B2} = 0.8$ mA = current through R_1 and $R_2 = I_{divider}$

The zener diode selected is a 1N750 which will provide a 4.7-volt drop (10% tolerance) when the current through it is 15 to 20 mA. For the calculations, V_Z can be considered to be 4.7 volts, any variations being compensated for by R_P. The values of R_1 and R_2 are:

$$R_1 = \frac{V_o - V_Z - V_{BE2}}{20\ I_{B2}} = \frac{6 - 4.7 - 0.7}{0.8 \times 10^{-3}} = 750\Omega,$$

$$R_2 = \frac{V_{BE2} + V_Z}{20\ I_{B2}} = \frac{0.7 + 4.7}{0.8 \times 10^{-3}} = 6.75\ k\Omega,$$

$$R_P = 0.1\ R_2 = 675\ \Omega \approx 1k\ \Omega$$

By reducing the value of resistors R_1 and R_2, potentiometer (R_P) can be included as shown in Figure 2. This will give an output control of several volts.

The collector current of Q_2 has been set at 4 mA. Of this, 2 mA will flow through Q_1 as its base current. The remainder of 2 mA must flow through resistor R_3:

$$R_3 = \frac{Vin_{min} - V_Z}{I_{C2} + I_{B1}} = \frac{9-4.7-.7}{(4+2) \times 10^{-3}} = 715\ \Omega.$$

To improve regulation the network R_4, R_5, and R_6 is included to provide a source of current (I_Z) to the zener diode. Zener current (I_Z) should be 10 mA or more including that current flowing thru Q_2.

The current thru Q_2 is

$$I_{E2} = I_{C2} + I_{B2} = (4 \times 10^{-3}) + (.04 \times 10^{-3}) = 4.04\text{mA}.$$

The I_{B2} is small and can be dropped from further calculations. To make $I_Z = 10$ mA, the current thru R_4, R_5, R_6 network must be

$$I_Z - I_{C2} = (10 \times 10^{-3}) - (4 \times 10^{-3}) = 6\text{mA},$$

$$R_4 + R_5 + R_6 = \frac{Vin_{min} - V_Z}{I_Z - I_{C2}} = \frac{4.3}{6 \times 10^{-3}} = 700\Omega.$$

The value of 700Ω can be divided up into three separate resistors of about equal value. Two 5-10 -μF capacitors will improve the filtering.

If this power supply or subsequent ones in this report are to be operated no load to full load the resistor divider netowrk R_1, R_2 will normally load the supply sufficiently to stop voltage surges. Should it be necessary an additional resistor can be placed across the output to preload the supply and hold the voltage, V_o, constant between no load and full load.

This completes the design of regulator circuit No. 1 as shown in Figure 2. Note that the resistor values calculated do not agree exactly with those shown in Figure 2. The nearest RETMA value can be used, but the ratio of R1 and R2 calculated should be maintained. When the exact value of R1 and R2 cannot be obtained, select lower resistance values to increase the divider current.

Table I shows the performance of regulator circuit No. 1. The Regulation Factor shows how well the circuit regulates against input line voltage variations and is defined as

$$\text{Regulation Factor} = RF = \Delta V_o / \Delta Vin_{ac} \Big|\, I_o \text{ constant.}$$

The output resistance is a measure of how well the circuit regulates against load changes and is defined as

$$\text{Output Resistance} = RO = \Delta V_o / \Delta I_o \Big|\, Vin_{ac} \text{ constant.}$$

Table I also shows the ripple voltage measured at the output. Appendix A will explain circuitry that can be incorporated to reduce output ripple voltage of this circuit and the following circuits.

A heat sink for Q_1 is recommended regardless of how low the output current I_o is. Q_1 must always dissipate the power supplied by the source minus the output:

$$P_D = (Vin - V_o)(I_o),$$

where P_D is the power dissipated in Q_1. The TIP24 (Q_1) of Figure 2 was bolted to a 1/16-inch thick copper plate 1 inch wide by 2 inches long. The exact determination of heat sink area can be calculated,[3] and should be when the circuit is to be used in enviroments with high ambient temperature. Even with a heat sink, the entire Regulator Circuit No. 1 was built on a plug-in card that measured 3 x 5 inches.

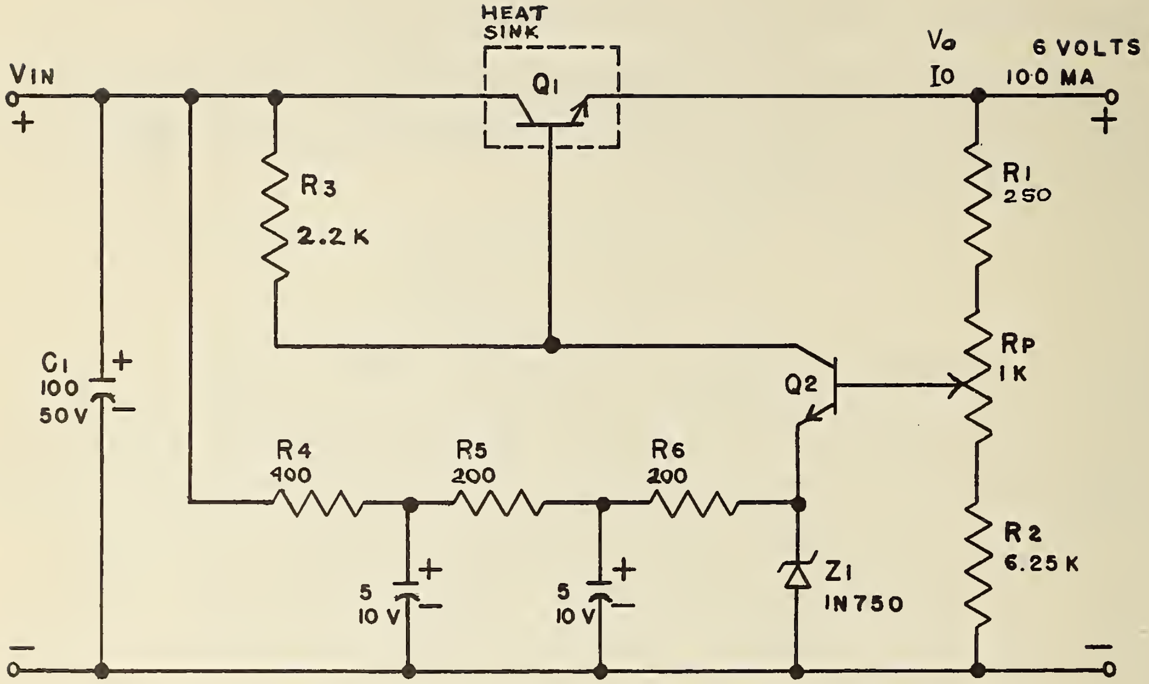


Figure 2. Schematic Diagram for Regulator Circuit No. 1.

Component Values:

All Resistance in ohms, All capacitance in μF.

Transistors used for $I_o \leqq .5$ amps.

$$Q_1 = \text{TIP24},\ Q_2 = \text{2N3904}$$

Typical transistor D C Gain (h_{FE}). For maximum and minimum values see Appendix B.

TIP24, $h_{FE} \approx 50$ at 100 m A

2N3904, $h_{FE} \approx 100$ at 2 m A

TABLE I

PERFORMANCE OF REGULATOR CIRCUIT NO. 1

Regulation Factors $RF = \frac{\Delta V_{out}}{\Delta Vin_{a-c}} \Big|\ I_{out}$ constant

TA = 23°C

Input Voltage Change a-c	ΔVin_{a-c}	ΔV_{out}	Reg	% Reg
85 - 95	10	.077	.0077	.77
105 - 115	10	.031	.0031	.31
125 - 135	10	.024	.0024	.24

Output Resistance $R_o = \frac{\Delta V_{out}}{\Delta I_{out}} \Big|\ V_{input}$ constant

TA = 23°C

Output Current Change d-c A	ΔI_{out}	ΔV_{out}	R_o Ω
90 mA - 100 mA	10 mA	.008	.8
100 - 110	10 mA	.006	.6
100 - 200	100 mA	.115	1.15
120 - 130	10 mA	.008	.8

Output Ripple Voltage

TA = 23°C

Ripple Voltage = 0.075 V. P. P. when C_1 = 100μF

Ripple Voltage = < 1 mv P. P. with circuit of Figure 6a

3. REGULATOR CIRCUIT NO. 2

Regulator circuit No. 2 is recommended for output current greater than 0.5 A and reduced output ripple voltage. A reduction in ripple voltage by a factor of 2 can be expected as compared with the previous Regulator Circuit No. 1.

The regulation is improved and ripple voltage reduced by the addition of a preregulator circuit. This additional circuitry is shown in Figure 3 and consists of Q_3, R_3, R_7, and Z_2. This circuit will provide a constant current of reduced ripple to the collector of Q_2 and hence to the base of Q_1. The zener diode Z_2 will hold the base voltage of Q_3 fixed, and the negative feedback voltage developed across R_3 will tend to keep the collector current constant.

In addition to the preregulator circuit, there is the added transistor Q_4. Whenever output currents (> 0.5 amps) are desired, it is wise to include Q_4 because Q_2 may not be capable of supplying the increased base current to Q_1. Here, Q_4 and Q_1 can however be considered as one transistor as the calculations will subsequently show.

The resistor values shown in Figure 3 were determined by using the same formulas presented previously plus additional formulas for the preregulator section. The formulas for designing the preregulator are as follows:

$$R_3 \geqq \frac{V_{Z2} - V_{EB3}}{I_{C2} + I_{B4} + I_{B3}}$$

$$R_7 \leqq \frac{V_{Vin\,min} - V_{Z2}}{I_{Z2} + I_{B3}} .$$

The transistor used as Q_3 should be a complementary transistor to Q_2. It must be capable of carrying a current equal to or greater than the collector current of Q_2 and of maintaining a high gain. The zener diode Z_2 should regulate at a lower voltage than that of Z_1, preferably 1 or more volts lower. The proper selection of Z_2 will allow the input voltage to drop to a lower value before control is lost.

The calculation of the resistor values shown in Figure 3 are as follows for a regulator to provide 1 amper output current (I_o) at 6 volts (V_o). The minimum input voltage Vin_{min} is again 9 V and Z_1 is a 1N750 which regulates at about 4.7 V. It is assumed that all transistor leakage currents are small and will be neglected in the following calculations. All h_{FE} values are typical and are shown in Figure 3.

Q_1 and Q_4 can be considered as one transistor which has a gain of $(h_{FE1})\ (h_{FE4})$:

$$h_{FE_{total}} = (h_{FE1})\ (h_{FE4})$$

$$I_{B_{total}} = I_o / h_{FE_{total}}$$

This $I_{B_{total}}$ is what must be supplied by transistor Q_2;

Q_1 is a TIP24; Q_4 is a 2N1308; and

$$h_{FE_{total}} = 50 \times 80 = 4{,}000, \text{ typical},$$

$$I_o = 1 \text{ amp},$$

$$I_B \text{ for } Q_4 = I_{B4} = I_o / h_{FE_{total}} = 1/4000 = 0.25\,\text{mA}.$$

Q_2 a 2N3904, must supply this 0.25 mA (I_{B4}), and for stability its collector current must be greater. When the extra transistor Q_4 is used, the over-all requirements placed on Q_2 are reduced (compare to calculations for Regulator Circuit No. 1). Because of this, the factor 4 is used instead of 2 in the previous example for determining I_{C2}:

$$I_{C2} = 4\, I_{B4} = (4)\,(0.25 \times 10^{-3}) = 1.0\,\text{mA}$$

$$I_{B2} = \frac{I_{C2}}{h_{FE2}} = \frac{1 \times 10^{-3}}{100} = 0.01\,\text{mA}$$

$$I_{divider} = 50\, I_{B2} = (50)\,(0.01\,\text{mA}) = 0.5\,\text{mA}$$

(see page 6 for factor of 50)

$$R_1 = \frac{V_o - V_{Z1} - V_{BE}}{50\, I_{B2}} = \frac{6 - 4.7 - 0.7}{0.5 \times 10^{-3}} = 1.2\,\text{k}\Omega$$

$$R_2 = \frac{V_{BE2} + V_{Z1}}{50\, I_{B2}} = \frac{0.7 + 4.7}{0.5\,\text{mA}} = 10.8\,\text{k}\Omega\ .$$

$$R_p = 0.1\, R_2 = 1.08\text{k}\Omega \approx 1\text{k}\Omega\ .$$

The preregulator replaces the function of R_3 in the previous example of regulator circuit No. 1. Thus far, the calculations show that the preregulator must carry the current I_{C2} minus the base current of Q_4. The 2N3906 is chosen because it has high gain, can carry the current, and is a good complement of Q_2. A 2N3906 has a typical h_{FE} of 100 at this collector current range. The zener diode selected is a 1N746, which has a breakdown voltage of 3.3 volts ±10% when the current through it is between 15 to 20 mA:

$$R_3 \geqq \frac{V_{Z2} - V_{EB4}}{I_{C2} + I_{B4} + I_{B3}} = \frac{3.3 - 0.7}{(1 + 0.25 + 0.01) \times 10^{-3}} = 2.06\text{k}\Omega\,,$$

$$R_7 \leqq \frac{Vin_{min} - V_{Z2}}{I_{Z2} + I_{B3}} \cong \frac{9 - 3.3}{15\,mA} \cong 380\Omega.$$

It may be noted that the current through Q_2 and hence through Z_1 is much smaller in this example than in the previous one. To have zener current equal to about 15 mA, there must be more current supplied by the resistor network R_4, R_5, and R_6:

$$R_4 + R_5 + R_6 \geqq \frac{Vin_{min} - V_{Z1}}{I_Z - I_{C2}} \cong \frac{9 - 4.7}{15 \times 10^{-3}} \cong 290\Omega.$$

The value of 290 Ω can be replaced by three 100 Ω resistors. The precise zener current is not critical.

A heat sink must be used to dissipate the heat from Q_1. The circuit of Figure 3 was built on a 3 x 5 inch plug-in card with capacitor C_1 and transistor Q_1 mounted externally. The heat sink used for Q_1 was about 3" x 4" with a total of 20 fins on each side.

Table II shows the regulation factor and output resistance of Figure 3. The a-c ripple voltage indicated about doubles when the pre-regulator circuit is replaced with a resistor. If the value of C_1 is increased from 600 to 1000 μF, the ripple will decrease to less than 5 mV.

Some high gain feedback regulator circuits such as illustrated in Figure 2 and Figure 3, will oscillate at a high frequency. This will not affect the regulation a great amount, but it is very evident at the output as observed on an oscilloscope. Capacitors (about 0.05 μF) placed in a number of places will stop this; the 0.05 μF shown in dashed box on Figure 3 is for this purpose. The best place for this capacitor is found by trial and test because circuit layout will have some effect on high frequency oscillations.

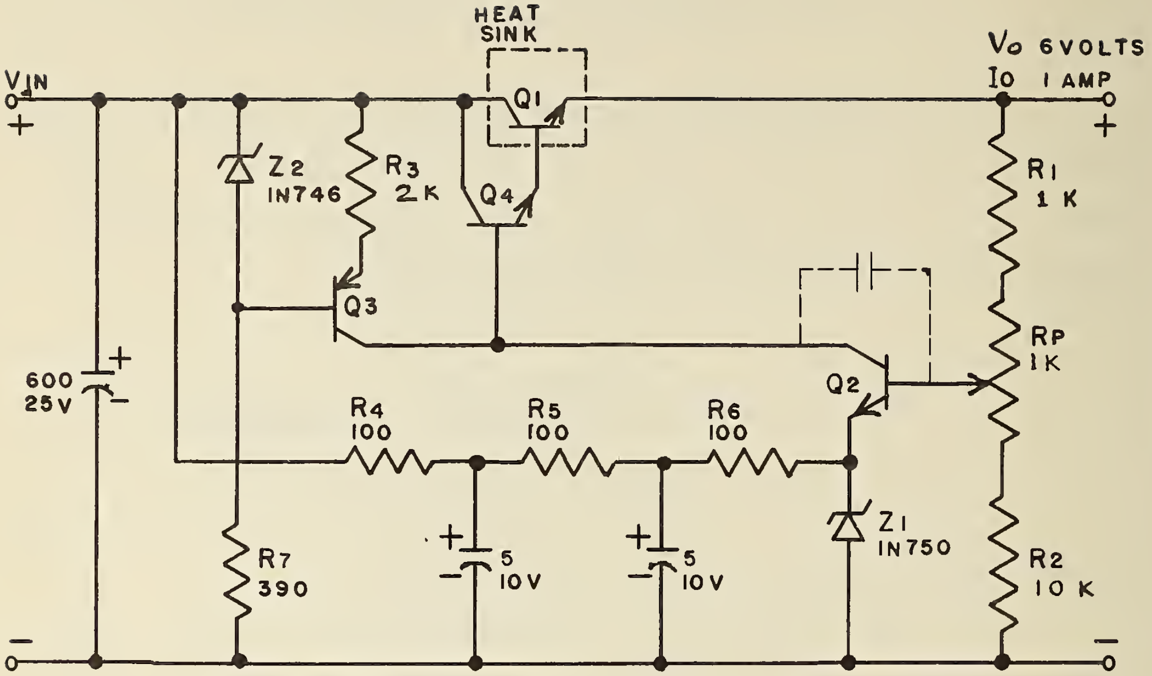


Figure 3. Schematic Diagram for Regulator Circuit No. 2

Component Values:

All Resistance in ohms, All capacitance in μF.

Transistors:

$I_o \leqq 1$ amp Q_1 = TIP24, Q_2 = 2N3904, Q_3 = 2N3906,
Q_4 = 2N1308

$I_o \geqq 1$ amp Q_1 = 2N1546, Q_2 = 2N3906, Q_3 = 2N3904,
Q_4 = 2N1309*

Typical transistor d-c gain (h_{FE}). (For maximum and minimum values see Appendix B):

TIP24, $h_{FE} \approx 50$ at 1 amp

2N1546, $h_{FE} \approx 90$

2N1308 or 2N1309, $h_{FE} \approx 90$

2N3906 or 2N3904, $h_{FE} \approx 100$

*When these transistors are used, the input voltage polarity must be reversed. The three electrolytic and capacitors and Z_1 and Z_2 must have their respective connections reversed.

TABLE II

PERFORMANCE OF REGULATOR CIRCUIT NO. 2

Regulation Factor $RF = \left.\frac{\Delta V_{out}}{\Delta Vin_{a-c}}\right| I_{out}$ constant

TA = 23°C

Input Voltage Change a-c	ΔVin_{a-c}	ΔV_{out}	Reg	% Reg
100 - 110	10	.021	.0021	.21
105 - 115	10	.021	.0021	.21
110 - 120	10	.019	.0019	.19
115 - 125	10	.018	.0018	.18

Output Resistance $R_o = \left.\frac{\Delta V_{out}}{\Delta I_{out}}\right| Vin_{a-c}$ constant

TA = 23°C

Output Current Change d-c A	ΔI_{out} amps	ΔV_{out}	R_o Ω
1 - .8	.2	.011	.055
1 - 1.2	.2	.009	.0045

Output Ripple Voltage TA = 23°C

Ripple voltage ≦ 0.03 V. P. P., when C_1 = 600μF

4. REGULATOR CIRCUIT NO. 3

This circuit is superior to that of regulator circuits No. 1 and No. 2 in its ability to regulate against line and/or load changes, to reduce ripple voltage, and be somewhat insensitive to ambient temperature changes. The circuit has been used to regulate voltage at 2, 12, 22, and 30 volts at output currents (I_o) up to 2 amps.

The circuit is shown in Figure 4. Note that the comparison amplifier (Q_2 and Q_5) is a differential type amplifier with emitter coupling between the two. This provides an increase in gain and helps cancel drift due to temperature variations. Q_2 has a constant base bias as set by Z_1 and varying emitter bias as determined by Q_5 emitter current flowing through R_5. The Z_1 bias is a forward bias, the bias from R_5 is reverse, and the proper balance of these two bias voltages is reached when output voltage is as determined by the setting of R_P.

The design formulas are nearly the same; the same type transistors can be used as in the previous examples and the circuit can be constructed on a 3 x 5 inch plug-in card. The same consideration for C_1 and input voltage hold as was stated for the two previous examples. When necessary the transistor Q_1 must be mounted on a suitable heat sink and this may require separation from the plug-in card. When this is the case, the leads should be kept short,and heavy wire should be used to minimize resistive losses.

The resistance values shown in Figure 4 were derived from the following formulas and are for a 12 volt output at 2 amps. The design example is as follows:

Q_1 is a 2N1546, $h_{FE} \approx 90$ at 2 A

Q_4 is a 2N1309, $h_{FE} \approx 90$ at 20 mA

Z_1 is a 1N752, $V_Z \approx 5.6$ volts at 15 to 20 mA

$$I_{B4} = \frac{I_o}{h_{FE_{total}}} = \frac{2}{90 \times 90} \approx 0.25\,\text{mA}$$

$I_{C2} \geqq I_{B2} = 4 I_{B2} = 1\,\text{mA}$. (See Regulator Circuit No. 2 calculation.)

The above formula shows that the collector current of Q_2 must be 1 mA. A transistor must be picked which will provide good gain at 1 to 2 mA. collector current. The 2N3906 used previously is adequate for Q_2 and the same transistor should be used for Q_5:

Q_2 and Q_5 = 2N3906, $h_{FE} \approx 100$ at 1 to 2 mA.

To insure good coupling of the error signal thru R_5, as previously pointed out, it is necessary that Q_5 collector current be greater than Q_2 collector current. For this particular circuit, experience has shown that I_{C5} must be about twice I_{C2} to provide this coupling:

$$I_{C5} = 2I_{C2} = 2\,\text{mA}.$$

$$I_{E2} = I_{C2} + I_{C5} = 1\,\text{mA} + 2\,\text{mA} = 3\,\text{mA}$$

$$R_5 = \frac{V_o - V_{Z1} - V_{BE2} - V_{R4}}{I_{E2}} \text{ ; where } V_{R4} = R_4 I_{B2}\,.$$

If R_4 is no greater than 1kΩ, which has proved adequate, then V_{R4} is small and can be omitted:

$$R_5 = \frac{V_o - V_{Z1} - V_{BE2}}{I_{E2}} = \frac{12 - 5.6 - 0.7}{3 \times 10^{-3}} = 1.9\,\text{k}\Omega\,.$$

Determine R_3 for $I_{Z1} = 15\,\text{mA}$;

$$R_3 = \frac{V_o - V_{Z1}}{I_{Z1}} = \frac{12 - 5.6}{15\,\text{mA}} = \frac{6.4}{15\,\text{mA}} = 430\Omega\text{, use } 470\Omega .$$

As previously mentioned, a zener current of 15 to 20 mA is adequate for proper regulation of most zener diodes in the range of 4 to 6 volts:

$$I_{B5} = I_{C5}/h_{FE} = 2 \times 10^{-3}/100 = 20\mu A$$

$$I_{divider} = 50\, I_{B5}$$

$$I_{divider} = 50 \times 20 \times 10^{-6} = 1\,\text{mA} .$$

The factor 50 is used because output current I_o is greater than 0.5 amp (see part Regulator Circuit No. 1 calculations, page 6):

$$R_{divider} = R_D = R_1 + R_2$$

$$R_D = V_o / 50\, I_{B5} = 12\,k\Omega$$

$$R_1 = \frac{V_{Z1}}{I_{R1}} = \frac{5.6}{I_D + I_{B5}} = \frac{5.6}{1.02\,\text{mA}} = 5.49\,k\Omega$$

$$R_2 = \frac{V_o - V_{Z1}}{I_D} = \frac{12 - 5.6}{1 \times 10^{-3}} = 6.4\,k\Omega.$$

$$R_p = 0.1\ R_2 = 640\,\Omega \times 1k\Omega$$

By reducing R_2 and R_1, a 1kΩ potentiometer can be inserted between the two as R_P, which again gives some control over output voltage.

Let Z_2 be a 2.4 volt, zener diode or three silicon diodes in series, which experience has shown will regulate at about 2 volts when zener current is between 6 and 10 mA.

Let Q_3 be a 2N3904, which can carry the current (1 mA) of Q_2 and maintain an h_{FE} of 100.

The V_{Z2} of 2.2 volts is a compromise between the 2.4 as rated and the 2.0 volts at which many of these devices regulate, we find:

$$R_6 \geqq \frac{V_{Z2} - V_{EB3}}{I_{C2}} = \frac{2.2 - 0.7}{1 \times 10^{-3}} = 1.5\text{k}\Omega ,$$

$$R_7 \geqq \frac{Vin_{min} - V_{Z2}}{I_{Z2}} = \frac{15 - 2.2}{8 \times 10^{-3}} = 1.6\text{k}\Omega .$$

For this regulator the taps on T_1 should be used which provide 21 volts no load. After rectification and filtering the Vin_{min} to the regulator section will be near 18 VDC.

This completes the design of regulator circuit No. 3 to provide 12 volts regulated at 2 amps output current.

Table III shows the measured RF and R_o of this circuit. The ripple voltage at the output is indicated with the same considerations as stated for the two previous examples.

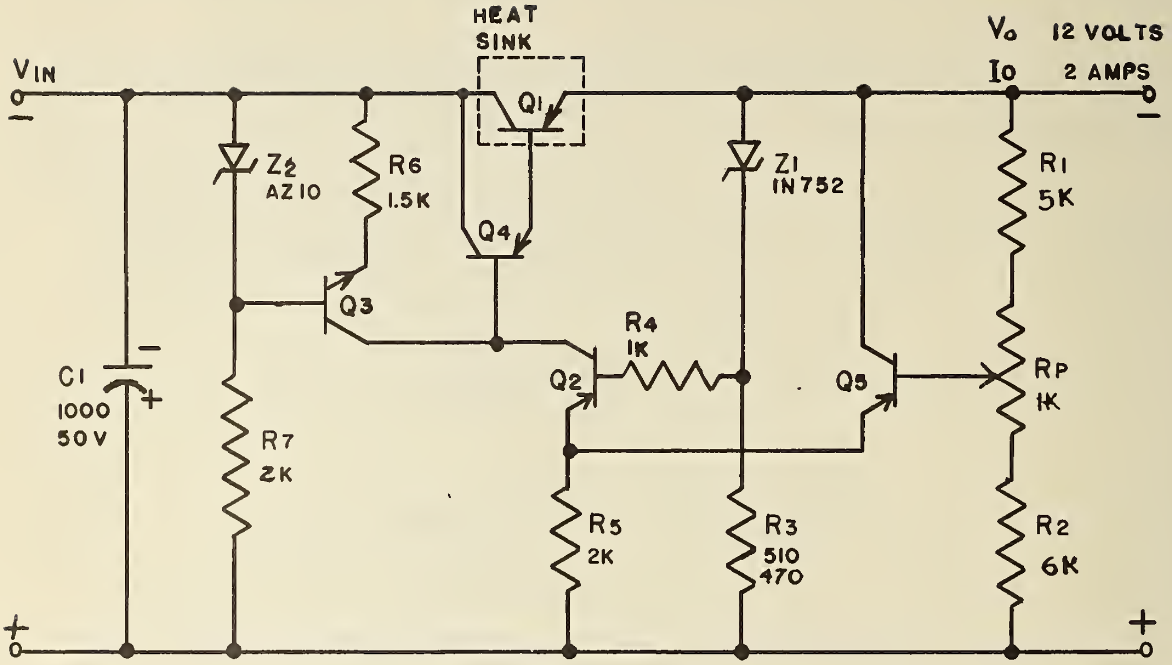


Figure 4. Schematic Diagram for Regulator Circuit No. 3.

Component Values:

All Resistance in ohms, all capacitance in μF.

Transistors used for I_o = 2 amps.

Q_1 = 2N1546, Q_2 = 2N3906, Q_3 = 2N3904, Q_4 = 2N1309
Q_5 = 2N3906.

Typical transistor DC Gain (h_{FE}) (For maximum and mimimum values see Appendix B):

2N1546, $h_{FE} \approx 90$
2N1309, $h_{FE} \approx 90$
2N3906, $h_{FE} \approx 100$
2N3904, $h_{FE} \approx 100$

TABLE III

PERFORMANCE OF REGULATOR CIRCUIT NO. 3

Regulation Factor $RF = \frac{\Delta V_{out}}{\Delta Vin_{a-c}} \Big|\ I_o$ constant

TA = 23°C

Input Voltage Change a-c	ΔVin_{a-c}	ΔV_{out}	Reg	% Reg
105 - 115	10	.43	.043	4.3%
115 - 125	10	.007	.0007	.07%

Output Resistance $R_o = \frac{\Delta V_{out}}{\Delta I_{out}} \Big|\ Vin_{a-c}$ constant

TA = 23°C

Output Current Change d-c A	ΔI_{out} amps	ΔV_{out}	R_o Ω
.5 - 2.0	1.5	.046	.03
1.5 - 2.0	.5	.011	.022
2.0 - 2.3	.5	.203	.403

Output Ripple Voltage TA = 23°C

Ripple voltage = 0.003 V.P.P. @ I_o = 2 A

Ripple voltage = 0.001 V.P.P. @ I_o = 1 A

5. DUAL VOLTAGE POWER SUPPLY FOR OPERATIONAL AMPLIFIERS

The majority of transistorized and integrated operational amplifiers require a ± 15 volt power supply. There are ways of adapting a 30 volt regulator to provide a dual output of ± 15 volts.[4] Some of the circuits available have been tried and found to be lacking in temperature stability and isolation between the two outputs. A more positive approach is to design two 15 volt supplies using the design formulas and circuit of regulator circuit No. 2 or No. 3. The following design example will be for a 15 volt regulator to provide 40 mA output current. Regulator circuit No. 2 and design formulas will be used. Figure 5 shows the circuit, two identical 15 volt supplies.

The following transistors and zener diodes were used:

Q_1 = TIP24, $h_{FE} \approx 50$

Q_2 = 2N3904, $h_{FE} \approx 100$

Q_3 = 2N3906, $h_{FE} \approx 100$

Q_4 = 2N1308, $h_{FE} \approx 90$

Z_1 = 1N750 = 4.7 volts @ 15 to 20 mA

Z_2 = 1N746 = 3.3 volts @ 15 to 20 mA.

The following shows the computation necessary to determine the resistance values:

$$I_{B4} = I_o / h_{FE_{total}} = 40 \times 10^{-3} / 50 \times 90 = 8.9 \mu A$$

$$I_{C2} = 4\, I_{B4} = 4(8.9 \times 10^{-6}) = 35.6 \mu A$$

$$I_{B2} = I_{C2} / 100 = 0.356 \mu A \quad .$$

$I_{divider} = 50\ I_{B2}$ = much less than 0.5 mA. Therefore, the $I_{divider}$ will be set at 2 mA:

$$I_{divider} = 2\,\text{mA}$$

$$R_1 = \frac{V_o - V_{Z1} - V_{BE}}{2 \times 10^{-3}} = \frac{9.6}{2 \times 10^{-3}} = \quad \text{k}\Omega$$

$$R_2 = \frac{V_{BE2} + V_{Z1}}{2 \times 10^{-3}} = \frac{0.7 + 4.7}{2 \times 10^{-3}} = \frac{5.4}{2 \times 10^{-3}} = 2.6\ \text{k}\Omega\,.$$

$$R_P = .1 R_2 = 260\ \Omega \approx 500\ \Omega$$

$$R_3 \geqq \frac{V_{Z2} - V_{EB4}}{I_{C2} + I_{B4} + I_{B2}} = \frac{3.9 - 0.7}{44.8 \times 10^{-6}} \approx 71.4\,\text{k}\Omega$$

$$R_7 = \frac{Vin_{min}\ V_{Z2}}{I_{Z2}} = \frac{17 - 3.3}{15 \times 10^{-3}} = 900\Omega$$

$$R_4 + R_5 + R_6 \geqq \frac{Vin_{min}\ V_{Z1}}{I_{Z1} - I_{C2}} = \frac{17 - 4.7}{(15 - 0.036) \times 10^{-3}} = 820\Omega$$

$$R_4 = R_5 = R_6 = 270\ \Omega\,.$$

It should be mentioned that the same transformer as recommended in Figure 1 is used. The connections are such that there are two separate secondaries. These connections provide the very minimum voltage necessary to the input of each regulator. The regulation for each circuit when connected as a dual ± 15 volt regulator is about 1% for line voltage variations from 95 to 115 volts. The R_o is less than 0.1 ohm and ripple voltage is less than 0.002 V, peak to peak (V. P. P.).

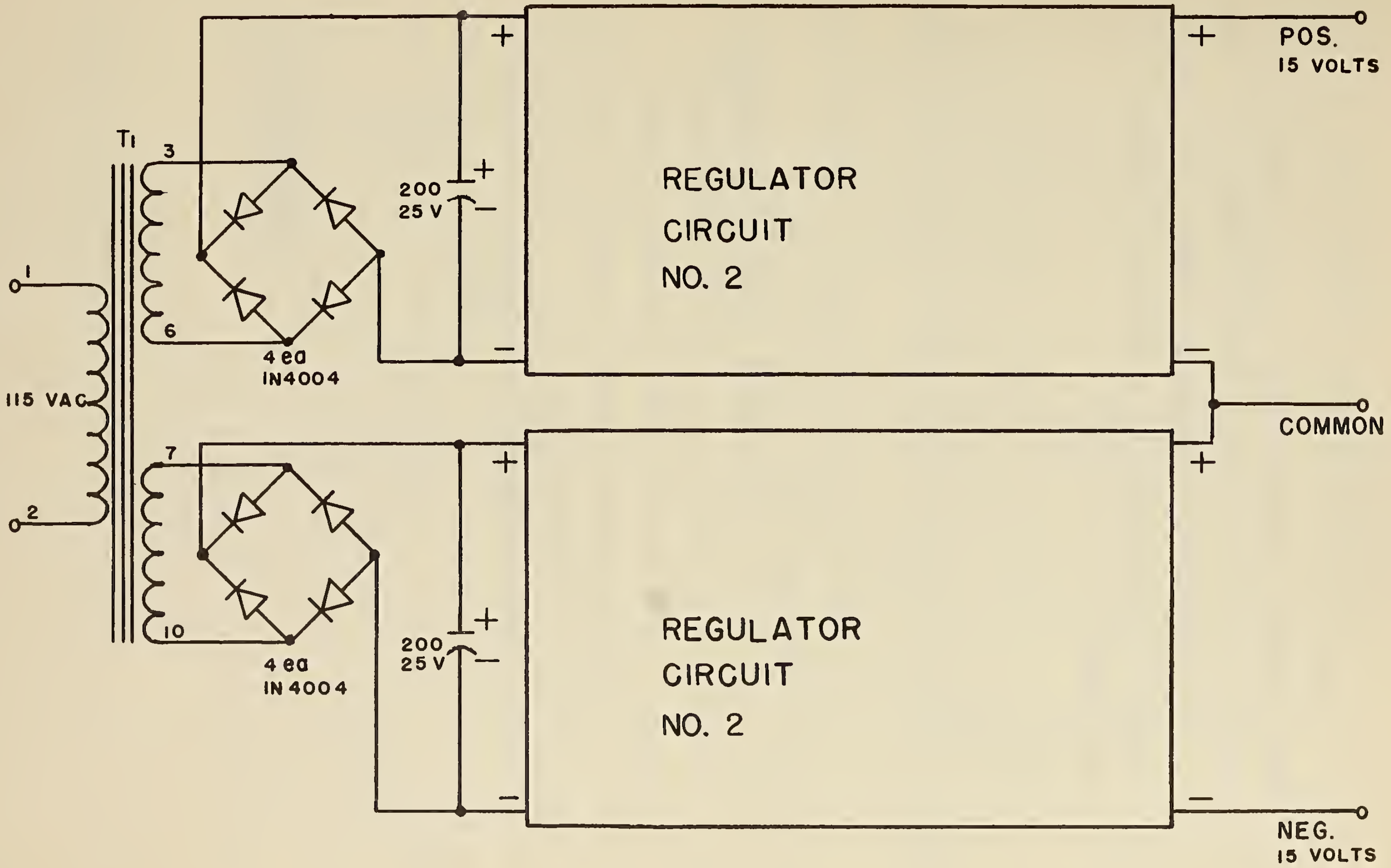


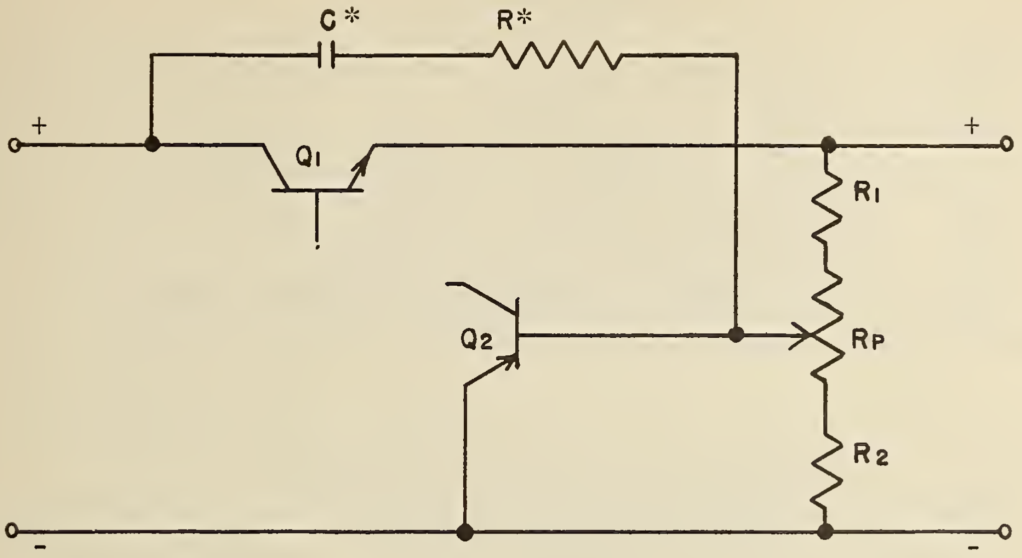
FIGURE 5
DUAL POWER SUPPLY

6. APPENDIX A

The subject of ripple voltage at the output was discussed previously in the text with the indication that the value of C_1 can be increased to reduce the ripple. It was also stated that there are limitations on how large C_1 can be. The following are two methods which can be used to reduce ripple voltage without increasing the size of C_1; in fact, C_1 can usually be reduced in size.

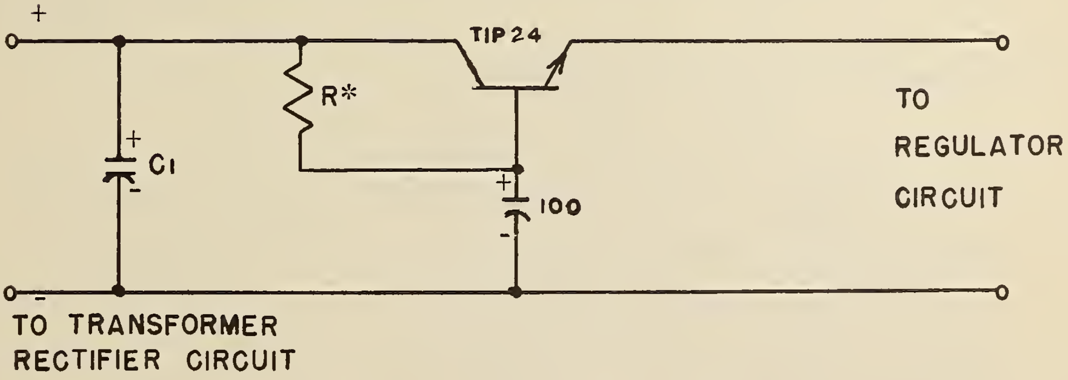
With any regulator circuit there is always the possibility of injecting ripple voltage into the amplifier section in the proper phase and amplitude to cancel that at the output. Figure 6a shows how this can be accomplished with regulator circuits No. 1 and No. 2. The values of C and R shown can be found experimentally, and when properly adjusted, will reduce the output ripple to very near zero.[5]

At the expense of increased input voltage requirement and additional parts, the circuit of Figure 6b can be used to reduce ripple voltage at the output.[3] The transistor used is suitable for output current (I_o) up to 1 amp and resistor R must be selected. Ordinarily the input voltage must be increased by about 3 volts. The size of C_1 can be reduced and the ripple will be greatly reduced when R is the proper value to bias the transistor. In one application the circuit of Fig. 6b was used with a regulator 6.3 volts (V_{out}) at 0.5 amperes (I_o) with half-wave rectification on the input. The value of C_1 was 500µF, and R was 500 ohms. The output ripple from the regulator was less than 1 mV, P. P. However, it was necessary to increase the input voltage at the transformer secondary by about 3 volts.



* See text for value of R and C.

Figure 6a. Network to reduce ripple voltage which can be added to regulator circuits No. 1 and No. 2.



* See text for value of R.

Figure 6b. Transistor filter circuit to reduce ripple voltage.

7. APPENDIX B

Vin_{ac} = Input a-c line voltage.

Vin = Input d-c voltage to the regulator section.

V_o = Output d-c voltage of the regulator.

V_Z = Zener diode breakdown voltage.

V_{BE} = Transistor base to emitter volts $\approx$ 0.7 VDC.

I_o = Output d-c current of the regulator.

I_C = Transistor collector current.

I_E = Transistor emitter current.

I_B = Transistor base current.

I_Z = Zener diode current.

h_{FE} = Transistor d-c gain.

R_p = Potentiometer resistance, see page 3, ff.

Transistor gain (h_{FE}) characteristics:

TIP24, h_{FE} = 19 to 136 @ 1.5 amps.
2N1546, h_{FE} = 75 to 150 @ 3 amps.
2N3906, h_{FE} = 100 to 300 @ 10 mA.
2N3904, h_{FE} = 100 to 300 @ 10 mA.
2N1309, h_{FE} = 80 to 150 @ 10 mA.
2N1308, h_{FE} = 80 to 150 @ 10 mA.
2N5036, h_{FE} = 20 to 70 @ 3 amps.

For operation at room temperature, typical values are given in the text. For temperatures above or below room temperature, consult the manufactures specifications.

8. APPENDIX C

Since the conception of this Tech Note, integrated circuit (IC) linear amplifiers have become readily available. Included in this general classification of linear amplifiers are complete voltage regulators with all the amplifier transistors, and reference diodes included. One such unit, the LM300, is capable of regulating voltages from about 2 vdc to 20 Vdc. For high output currents (greater than 20 ma) external series pass transistors must be added.

This section (appendix) illustrates the design of a 5V-2A regulated supply using the IC as the basic sensor and amplifier. An external series pass transistor is used to increase the current capability. The base current drive required by this transistor will make it necessary to add a second transistor. Figure 7 shows the complete design.

The 2N5036 is used as Q_1 because of its current and power capacity. The h_{FE} is typically 30 when I_C is 2 amp. The leakage current of the 2N5036 can be omitted from the calculations within the temperature limits shown in Table IV. The base current drive, I_{B1}, is calculated:

$$I_{B1} = I_{C1} / h_{FE} = \frac{2 \text{ Amp}}{30} = 67 \text{ mA} .$$

To provide this I_{B1} of 67 mA, another transistor amplifier is used, Q_2, which is a 2N1309. The h_{FE} will be typically 80 when its collector current is 100 mA. It is necessary that Q_2 provide the needed 67 mA to the base of Q_1 plus an additional amount of current through R3. Some current must flow through R3 for stability purposes as explained in the previous regulator examples. To leave a good margin of regulation, choose I_{C2} to be 1.5 times I_{B1} :

$$I_{C2} = I_{B1} + I_{B1} / 2 = 1.5 \times 67 = 100 \text{ mA} .$$

The 100 mA is well within the current rating of the 2N1309.

The emitter of Q_2 is connected to pin 3 of the LM300 and this voltage should be a minimum of 9 Vdc for reliable operation. Assuming $V_{E2} = 9V$, we calculate

$$R_3 = \frac{V_{E2} - V_o}{I_{C2} - I_{B1}} = \frac{9 - 5}{(100-67) \times 10^{-3}} = 120\,\Omega .$$

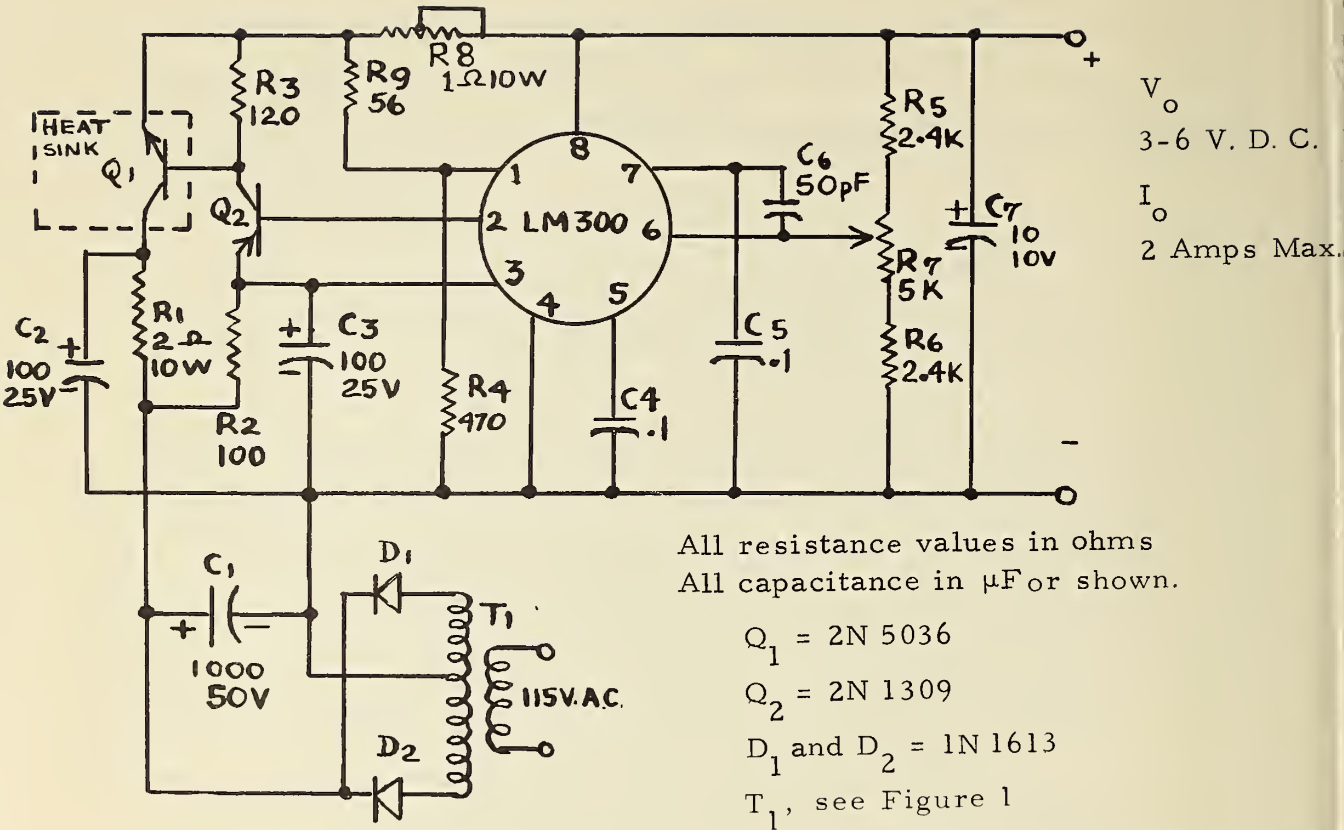
From the specification sheet for the integrated circuit the value of $R_5 + R_6$ should be about 9.5 k Ω. Figure 7 shows these two resistors to be 2.4 k Ω each with a potentiometer between them. This potentiometer, R_7, will allow output voltage to be set between 3 and 6 volts. The values of R_4, R_9, and R_8 are as suggested by the specification sheet. Making R_8 a tapped resistor, the current limiting (fold over type) can be adjusted by trial and test method.

Because of the requirement of 9 volts to pin 3 of the LM300, R_1 was added to dissipate some of the power instead of dropping it all across Q_1. The R_2 and C_3 were added as a pre-filter for the transistor Q_2 and the integrated circuit. At higher output voltages, R_1 and R_2 can be left out of the design.

The transformer and rectifier scheme must provide a minimum of 9 Vdc to the integrated circuit. For best results, a good quality transformer should be used that will not load down and subsequently supply abnormally high voltage when the load decreases.

A heat sink is used to limit the temperature of Q_1. For the circuit shown a heat sink as described for Regulator Circuit No. 2 was used, cut in half, lengthwise. This was done to make it possible to mount it and all other components except C_1 and T_1 on a 4 x 5 inch plug-in card.

Table IV is similar to the preceding tables with the stud temperature of Q_1 at various output currents included. The ambient for these temperature measurements was $23^{\circ}C$.



V_o
3-6 V. D. C.

I_o
2 Amps Max.

All resistance values in ohms
All capacitance in μF or shown.

Q_1 = 2N 5036
Q_2 = 2N 1309
D_1 and D_2 = 1N 1613
T_1, see Figure 1

Figure 7. Schematic Diagram and Component Values for I. C. Regulator Circuit.

TABLE IV

Regulation Factors $RF = \frac{\Delta V_{out}}{\Delta V_{in\ a-c}}$ | I_{out} constant

TA = 23°C

Input Voltage Charge a-c	$\Delta V_{in\ a-c}$	ΔV_{out}	Reg	% Reg
110 - 120	10	.002	.0002	.02 %
115 - 125	10	.004	.0004	.04 %

Output Resistance $R_o = \frac{\Delta V_{out}}{\Delta I_{out}}$ | $V_{in\ a-c}$ constant

TA = 23°C

Output Current Change d-c A.	ΔI_{out} amps	ΔV_{out}	R_o Ω
0.8 - 1.0	1.	.109	.109
2.0 - 1.0	0.2	.02	.100
2.0 - 0.5	1.5	.144	.096

Output Ripple Voltage TA = 23°C

Ripple Voltage = < 1 mv P. P. when C_1 = 1000 µF

Q_1 Mounting Stud Temperature

E_o volts	I_o amps	Q_1 Temp. Degrees C	Ambient Temp. Degree C
5	2	55	23
5	1.5	50	23
5	.1	35	23
3.6	2	59	23
3.6	1.5	50	23

9. ACKNOWLEDGEMENTS

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