NBS

Technical Note 168

TRANSISTORIZED BUILDING BLOCKS
FOR DATA INSTRUMENTATION

ROGER L. HILL

U. S. DEPARTMENT OF COMMERCE
NATIONAL BUREAU OF STANDARDS

THE NATIONAL BUREAU OF STANDARDS

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Contents

ABSTRACT

The National Bureau of Standards has developed a
number of modular transistorized digital circuits that
have been used in automatizing many data recording and
preliminary processing tasks encountered in its scientific
operations. These versatile building blocks can be con-
nected together systematically to form digital circuits
that accept raw data from experimental equipment and
transpose these data into a form suitable for input to a
high-speed electronic computer.

Each assembly of packages can be tailored to fit
the special requirements of the project and can be used
at the site of the experiment. The output from the system
can be: 1) fed directly to a computer, 2) recorded on a
medium (paper tape, magnetic tape, etc.) suitable for
computer input at a later date, or 3) used to drive display
equipment that keeps the scientist informed of the progress
of his experiment.

As a result of experience in the application of these
units, some of the original packages have been modified
and additional types developed. In addition to describing
the modified and new package types, this report also
includes a description of a new series of packages con-
sisting of identical circuitry, but utilizing a different
type of mating connector and a smaller circuit-board.

TRANSISTORIZED BUILDING BLOCKS
FOR DATA INSTRUMENTATION

by Roger L. Hill

I   INTRODUCTION

NBS Technical Note 68, published in May 1960, described a
series of "Transistorized Building Blocks for Data Transmission",
also identified as Series 2 Packages. Since then, several additional
circuits have been added to this series. In addition, some of the
original circuits have been modified, and these modifications as well
as corrections of errors that occurred in the original descriptions are
noted. Many suggestions from various sources which have been in-
corporated into Series 2 have also generated another Series (Series 3).
The primary change between the two series is in the physical features
and not the electrical circuit configuration. Series 3 Packages are
physically smaller and stronger, with test points on the top edge of the
packages.

Well over 25,000 packages have been produced and are incor-
porated into equipments ranging from simple instrumentation tasks to
complex computer systems. However, we have only had the oppor-
tunity to check and follow approximately 40% (10,000) of these with
detailed production yield and operating reliability figures. This
experience and data are extremely valuable and give us a very good
indication of the performance of the packages from a long-term stand-
point. These data are reported in Section VII of this report.

One of the most frustrating phases of interpreting logical designs
has been due to the lack of acceptance of a set of uniform symbols.
The primary purpose of the symbols should be to convey as much
logical information about the electrical circuit as possible, and yet be
simple and easy to draw. Since there has been no specific set of
symbols adopted by many of the organizations working on this task, we
have selected our own after much deliberation. These are shown and
explained in detail in Section V of this report.

Again it should be emphasized that these series of packages are
designed for laboratory equipments primarily because of an upper
temperature limitation of 50ºC. The construction techniques and en-
vironmental conditions become more important as the number of
packages or size of the system grows. We take this opportunity to
again state the general operating specifications and also to discuss
and explain several techniques (tricks of the trade) which have proved
invaluable from the standpoints of reliable system performance and
simplicity in trouble shooting or debugging procedures. The success
of any system is dependent not only on the performance of the
individual circuits, but also on the logical design and construction
technology adopted in the system.

II. GENERAL SYSTEM AND PACKAGE SPECIFICATIONS

The following specifications apply to all packages and to any system constructed with them:

1) All major functions may be performed at an operating speed of up to 50 kc.

2) Ambient temperature range may be from 0° to 50°C. (32° to 122°F).

3) The supply voltages are:

   a) -12 volts (Care should be taken not only in ground distribution but also in ensuring that this voltage appears at the terminals of the package. This supply is usually filtered with an electrolytic capacitor in parallel with a smaller mylar capacitor which has a lower impedance to high frequency transients.)

   b) +12 volts.

   c) Other special voltages required for references (analog comparison) and for driving mechanical devices.

4) The digital pulses have:

   a) A minimum range of 0 to -6 volts,

   b) A propagation delay averaging 0.5 μsec,

   c) A rise of at least 6 volts in 1.0 μsec.

Each package is constructed on a plug-in printed-board and uses electronic components that are common stock items to avoid replacement problems. Most of the packages contain type 2N414 transistors, and some contain types 2N363, 2N123, or 2N1302 transistors. In some of the packages components or subassemblies are left unconnected and must be wired externally to the package. Connecting these components externally allows greater flexibility in combining them.

III. SERIES 2 PACKAGES

The packages described in this Section were either developed or modified since NBS Technical Note 68 was issued. For all of NBS applications a zero ±0.5 volt signal is considered a logical "one" and a negative (-6 to -12 volts) signal as a logical "zero". In portions of this text, flip-flops will be referred to in terms of their input lines, such as R-S, J-K, or T. The logical characteristics [1]/ of each type are outlined in the following paragraphs.

An R-S flip-flop has two inputs. Input S, the set line, puts the flip-flop in the "one" state, and input R, the reset line, puts it into the "zero " state. These rules are true only if a "one" is applied to the particular input line and a "zero" to the other input line. If both R and S are "zero", the flip-flop will do nothing. However, if both R and S are "one", the action of the flip-flop is indeterminate.

The J-K flip-flop has the properties of an R-S type, except that if both J and K are "one" the circuit will change to the opposite state.

The T flip-flop has a single input line which causes the circuit to change state when it is "one", but leaves it in its former state otherwise.

Gated "T" Input, Series 2

The gated "T" input package is used for furnishing a T input connection to a flip-flop. This T input may be inhibited by a control pulse to allow shifting of other information into a flip-flop without permitting the propagation of a new pulse condition to succeeding flip-flops.

A schematic diagram of the gated T input circuit is shown in Fig. 1.[*] Four similar circuits are contained in each package. Each circuit consists of a pair of our standard pulse gates (enclosed by dashed lines) with the d-c level of each resistor determined by a one-transistor switch (Q_1 or Q_2). These switches are controlled by a combination of the turn-on command and the d-c levels of the flip-flop collectors to which they are connected.

The presence of a negative turn-on command pulse enables the switch (Q_1 or Q_2), with its emitter connected to the "one" (zero volts level) collector of the flip-flop, to turn on. This places the d-c level of its gate resistor (R_1 or R_2) at ground. Therefore, if a positive pulse is applied to the counting pulse input the flip-flop to which the diodes (CR_1 and CR_2) are connected will function as one stage of a binary counter with a T-input.

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[1]/   Logical Design of Digital Computers by Montgomery Phister, Jr. John Wiley & Sons, Inc., 1958.

[*]   Figures appear in consecutive order in back of the Appendix.

A positive level (ground) at the turn-on command (enable) input will inhibit the counting pulse and allow the transfer of new information into the flip-flop without propagation of a false carry signal.

A typical example of an application of this package is shown in the logical diagram of Fig. 2 which illustrates a series of flip-flops being used as a counter and also a shift register. During the shift register input the T inputs to the flip-flops are inhibited by maintaining a positive (ground) level on the enable line.

One-Shot, Series 2A

The pin configuration of this one-shot package is directly interchangeable with that of the Series 2 Model. To alleviate a problem of having the flip-flop "hang-up" in the wrong state a threshold circuit has been developed which provides a d-c reset to the flip-flop. Positive monostable operation is assured with this circuit.

Initially, transistors $Q1$ and $Q6$ are conducting and all others are in the cut-off state. For normal operation, pin 4 is connected to pin 10 and a positive going input pulse is applied to the input terminal (pin 1). This triggers the flip-flop (Q_1 and Q_2), and Q_2 assumes the conducting state, cutting off Q_6. The timing circuit, composed of resistor R_1 and one or more of capacitors C_1, C_2, and C_3, begins to charge toward a terminal voltage determined in part by the adjustment of the 1K potentiometer (R_3) which is used for fine control of the output pulse width. Coarse control is obtained by grounding one of the timing capacitors (pin 17, 19 or 21). Pulse widths ranging from below 10 μsecs to above 7 msecs may be obtained by using the capacitor values shown in the schematic diagram. For wider pulses (from 7 msecs to beyond 1 sec) an external capacitor may be used from pin 12 to ground. Consistency of pulse widths above 10 msec is very dependent upon the leakage and over-all quality of the capacitor.

When the timing circuit is charged to its selected voltage level the threshold circuit, which consists of a complementary transistor circuit (Q_3 and Q_4) is triggered. This turns on a transistor, Q_5, which clamps the collector of the normally on transistor, Q_1, of the flip-flop to ground at the end of the timing cycle; thereby, returning the flip-flop to its initial state.

Trigger diodes (CR_1 and CR_2) have been added from both the timing circuit and the discharge transistor (Q_6) to the threshold circuit in order to achieve faster switching of the threshold circuit. These diodes enable the circuit to switch rapidly even when a large timing capacitor is being used. A two-input diode or-gate (CR_3 and CR_4) has been inserted from the flip-flop and the restart input to the input circuit of the discharge transistor.

A positive going trigger pulse output which occurs at the trailing edge of the one-shot output is available, at the collector of

4

transistor Q_7 (pin 9), for triggering an external circuit such as a flip-flop.

The restart mode of operation permits the timing cycle to be stopped and started without resetting the flip-flop. A negative pulse applied to the restart input turns on the discharge transistor and halts the timing cycle which may be started again when the restart input is restored to ground level. This package may be used for sensing a gap in a series of pulses by applying negative pulses to both the normal input and the restart input as shown in Fig. 4. The trailing edge of the first pulse sets the flip-flop which initiates the timing waveform. Each successive negative pulse restarts the timing wave-form until a gap occurs in the pulse train and allows the timing wave-form to reach the threshold, thus ending the timing cycle in the normal manner.

Alternatively, the timing cycle may be ended synchronously as shown in Fig. 5 with an external pulse train which is applied to the capacitor (pin 3) of the trigger gate. During the timing cycle the d-c level of this gate resistor will normally be negative until the cycle ends and the level returns to ground. This allows the gate capacitor to charge and respond to the following pulse which turns off the flip-flop. A jumper connection to pin 10 on the socket determines whether the package is to be used for the restart mode of operation or for the synchronous turn-off mode. A block diagram for each mode with external wiring and input-output waveforms is shown in Figs. 4 and 5.

Pulse Gate Driver Package, Series 2A

The pulse gate driver package, Series 2A, is intended to replace the Series 2 version without requiring wiring changes in any previous system applications. The circuit requires a single input that is complementary to the output since inversion takes place. Two cir-cuits are contained on one board with connections as shown in Fig. 6. The former model had two stages of inversion, therefore, the output followed the input on pin 7 (or 19). Since no connections are made to these two pins on the new package, no wiring changes are necessary when it is substituted for the old series 2 package.

The input impedance of the pulse gate driver presents 2 or-inverter loads to any driving circuit. The circuit output will drive 20 flip-flops or 24 and/or inverter loads at a repetition rate of 50 kilo-cycles. Greater loads can be driven provided the frequency of operation is decreased. For example, the circuit will drive 30 flip-flop loads at a repetition rate of 20 kilocycles. The fall time in-creases with an increase in capacitive load thus extending the recovery time of the circuit.

The pulse gate driver is basically a three-transistor circuit with two grounded emitter amplifiers operating in parallel with one (Q_1) driving an emitter follower (Q_2). The grounded emitter amplifier (Q_3)

5

acts as a low impedance discharge path for the capacitive portion of the load when the transistor is turned on by a negative going input signal. The emitter follower (Q_2) is a low impedance discharge path for the load capacitance when the input signal is positive going and turning off Q_1 which drives Q_2. The circuit operates as an inverting power amplifier for either pulses or levels with a minimum rise of 6 volts in one microsecond. When a positive going signal brings the input terminal to ground Q_1 is turned off and the output voltage falls toward -8 volts at a rate determined by R_1 and the impedance of the saturated transistor Q_2 in series with the capacitive and resistive load. When a negative going signal is applied to the input, Q_1 is turned on which turns off Q_2. The grounded emitter amplifier, Q_3, is turned on bringing the output to ground.

The β of all three transistors should be greater than 55 with V_{CE} = 6V and I_C = 1 ma.

Preamplifier Package, Series 2

The preamplifier package is intended for use where a standard output pulse is desired for triggering digital logic packages in this series, such as the flip-flop and one-shot. The input to this package may be a push-pull or single-ended sinusoidal waveform with a repetition rate which is variable from 50 kc down to 7 cps. The input signal must have a peak-to-peak amplitude of at least 0.5 volt. The output pulse will swing from -12 volts (the collector supply voltage) to ground potential with a rise time of less than one microsecond.

This package (Figure 7) contains a push-pull amplifier stage which may be modified by means of an external jumper for single-ended input signals. When used in this fashion, it has a gain of approximately 10. The input amplifier is followed by a Schmitt trigger circuit which switches rapidly in response to slowly varying input voltages, providing an output pulse having the desired rise time and amplitude. Since the amplifier and trigger circuit are direct-coupled, there is no shift in threshold with repetition rate.

A threshold control is provided for establishing a suitable triggering level in order to avoid multiple triggering on irregular waveforms and to provide discrimination against background noise. In addition, a balance control is provided on the push-pull input stage. This is useful for obtaining balanced clipping on large push-pull input signals, and is necessary to obtain correct operation with single-ended connection. A feature of the input amplifier is that a substantial d-c level or common-mode component may be accommodated in the triggering signal. When used with a push-pull signal, the amplifier will tolerate a common-mode d-c shift of -3 to +10 volts.

When used as a push-pull amplifier, the input signal is applied to terminals 5 and 7. With single-ended input signals, terminal 5 is grounded and the input signal is applied to terminal 7. The input

6

erminals are connected through current limiting resistors R_1 and R_2 to the bases of transistors Q_1 and Q_2 which are connected as an emitter-coupled amplifier stage. The emitters of Q_1 and Q_2 are connected through a 100-ohm balance potentiometer, R_5, which provide some degeneration. The potentiometer wiper is connected to the collector of transistor Q_3, which serves as a constant-current source, and appears as a very high impedance. This leads to the high common-mode rejection obtained from the push-pull amplifier stage.

The operation of Q_3 as a constant-current source can be explained as follows: The base of Q_3 is connected to a low-impedance voltage divider consisting of R_6 and R_7, which places the base at about +11 volts. The emitter is returned to +12 volts through a 120-ohm resistor, R_8. The transistor attempts to maintain the emitter at a potential close to that of the base, resulting in a drop of about one volt across R_8, and a steady current through it of about 8 ma. The current through R_8 flows mainly in the collector circuit; thus a constant collector current of 8 ma is obtained over a wide range of collector voltages.

The emitter-coupled amplifier has good overload characteristics in that it recovers rapidly from overloads of either polarity. The present circuit is direct coupled throughout, so there are no capacitors which might charge during an overload.

The amplifier output is a single-ended signal for either push-pull or single-ended inputs. This signal may be viewed with an oscilloscope at a test point brought out to terminal 3. The signal is applied to a potentiometer, R_{10}, which serves as a threshold control and drives a trigger amplifier stage, Q_4. This is an NPN transistor connected as an emitter follower and furnishes positive trigger signals to the output stage which is a Schmitt trigger circuit consisting of transistors Q_5 and Q_6. These transistors are emitter-coupled with the emitters being returned to +12 volts through a 1000-ohm resistor, R_{14}. This furnishes a large amount of coupling between the two transistors. Additional regeneration is afforded by the coupling network, R_5 and C_1, from the collector Q_5 to the base of Q_6. The emitters of Q_5 and Q_6 rest approximately at ground potential, with Q_5 normally conducting and Q_6 cut off. Application of a positive trigger signal to the base of Q_5 results in Q_5 turning off and T_6 turning on. It would also have been possible to use negative signals, turning the "off" side "on"; however, it has been observed that there is less tendency for the output signal to follow the input (which would deteriorate the rise time) if the "on" side is triggered "off".

Both collectors of the Schmitt circuit are brought out, providing complementary output signals; however, terminal 16 is the one which goes positive when triggered, and hence is the one that would normally be used for triggering other circuits, such as flip-flops and one-shots. Generally speaking, it is the leading edge of this signal which will be used; the width is subject to wide variation, depending on the triggering

7

signal. The Schmitt circuit is bistable and will remain in its triggered state as long as the input signal exceeds the threshold. A typical connection diagram is shown in Figure 8.

The +12 volt supply is essential to the circuit operation and is not merely a bias supply for use at elevated temperatures. Both the -12 volt supply and the +12 volt supply must be connected as indicated

Pulse Stretcher Package, Series 2

The pulse stretcher package is intended for use where an analog amplitude value is to be retained for a brief interval. The value is stored as a charge on a 1.0 µfd low leakage, capacitor and may be retained for several milliseconds or longer, depending upon the required accuracy. Circuits are provided for rapidly discharging and charging the capacitor, and an output isolation stage is provided which permits the stored voltage value to be read out while presenting a high impedance to the capacitor.

The package was originally developed for use with an analog-to-digital converter. In this application the pulse stretcher is supplied with a series of negative pulses of different amplitudes obtained by sampling a continuously varying waveform. The pulse stretcher then maintains these amplitude values during the time required for the conversion process. In the original application the amplitude values were retained within 5% over a 5 millisecond interval. The width of the input pulse was 200 microseconds to assure complete charging of the storage capacitor.

The pulse stretcher package (Fig. 8) normally requires two signals for its operation. The input signals should be negative pulses of varying amplitude from 0 to -10 volts, with a pulse width between 100 and 200 microseconds to fully charge the 1.0 µfd storage capacitor, C_1. The capacitor is charged by an emitter follower, which presents a reasonably high impedance greater than 50 kilohms to the input source, while providing a low impedance for charging the capacitor. Across C_1 is a transistor, Q_2, which is turned on to discharge the capacitor before a new value is read in. An emitter follower stage containing Q_3 is included to provide a means of reading out the voltage stored on C_1. This stage presents an impedance greater than 50 kilohms to C_1 in order not to discharge the capacitor at an excessive rate, and at the same time presents a reasonably low output impedance of approximately 5 kilohms depending upon the circuit being driven.

The discharge pulse which is applied to Q_2 for discharging the storage capacitor should be a negative pulse of 8 to 12 volts with a duration of 100 to 200 microseconds.

In order to provide for flexibility in the connection of the pulse stretcher package a number of connections have been brought out to terminals.

8

The timing of the input and discharge signals is illustrated on the schematic diagram (Fig. 9). It can be seen that each input pulse should be preceded by a discharge pulse to assure that any residual charge on Cl is removed prior to recharging. Fig. 10 is a diagram showing typical connections for an application of the pulse stretcher package.

Sampler Package, Series 2

The sampler package is intended for use where the contents of a large number of registers are to be transferred, one by one, to a single buffer register. Normally, gating packages might be used for this purpose; however, it is not satisfactory to bring more than 7 or 8 gate diodes to the base input of a flip-flop. The sampling package was developed when a need arose to accommodate a much larger number of inputs. The limiting quantity has not been ascertained, but at least 15 registers may be sampled in this manner. The registers being sampled may be connected in any way, such as counters, subtractors, shift registers, display buffers, etc., just so long as standard logic levels are maintained. The contents will not be disturbed during sampling, but should be held stationary for the sampling interval, which is 20 microseconds, in order that a true sample be obtained. In other words, the leading edge of a sampling pulse must precede the transfer pulse by a minimum of 20 μsec. A typical application of sampler packages being used to sample three different registers is shown in Figure 11 with the sampling and transfer pulse waveforms.

There are 8 sampling circuits per package, and each circuit consists of a transistor and diode with appropriate resistors (Fig. 12). One circuit is needed for each stage that is to be sampled. The transistor is used as a two-input and-gate with the emitter attached to the collector of a stage which is at ground potential for a "one", and the base connected to a turn-on signal which is negative during sampling. An example of the connection of a typical stage is shown in Fig. 13.

The sampler package may also be used for making an absolute comparison between registers as illustrated in Fig. 14. The collector is connected through a diode to the resistor of a diode gate at the input of a flip-flop in the buffer register. Up to thirteen collectors may be in parallel to this gate resistor achieving in effect a multi-input or-gate. An external resistor must be connected between this point and $-V_{cc}$ so that this point will normally be held negative. The gate, then, will only be able to charge when a stage containing a "one" is being sampled. Under this circumstance, the selected sampling transistor will have its emitter at ground potential. When turned on by the sampling pulse, its collector will move toward ground causing the diode gate to charge. After the sampling pulse has been on for 20 microseconds the capacitor of the diode gate may be pulsed, transferring the "one" to the buffer register. It is possible, of course, to transfer "zeros" rather than "ones", if desired.

9

It has been noted that there is a diode in the collector lead of each sampling transistor. These diodes are necessary to keep the transistors off in case the collectors should become positive with respect to their emitters. This would occur when an unselected transistor is sampling a "zero" (emitter negative); while a selected transistor on the same collector line is sampling a "one", bringing the collector line up to ground potential. The remaining components on the sampling packages are pull-down resistors from base to emitter (620 ohms) and current-limiting resistors in series with each base lead (8.2K ohms).

The value of external resistors used with the collector lines should be low enough to offset any leakage current which might result when a large number of sampling circuits are connected in parallel. However, it should not be so low that the sampling circuit imposes an appreciable load on the stage being sampled, or that excessive base current is required to turn the sampling circuit fully on. A value of 5,000 ohms has been found quite suitable. When long registers are being sampled, up to 13 sampling circuits can be connected to the same base turn-on line. Some 12 or 13 stages should be about the limit when the turn-on signal is provided by a single or-inverter or flip-flop, although the turn-on line could be supplied by two or more drive circuits or a pulse gate driver. In some applications it may be possible to save circuitry by terminating the sampling pulse simultaneously with the start of the read-in pulse. The storage associated with the diode gate allows this to be done.

Because of the fact that the sampling circuits are connected to trigger gates via the resistor input, and are d-c connected throughout, it is not necessary that rise times be preserved in the cabling to and from the sampling packages. Thus, the registers being sampled may be widely separated from the buffer register.

Read Package, Series 2E

The Read Package, Series 2E, is intended for reading low level (10 millivolt) signals from a magnetic drum or magnetic tape. It is designed for use either with NRZ (non-return-to-zero) or return-to-bias recordings. When used with a magnetic drum the frequency of operation was 50,000 pps (pulses per second) although it is useful to higher frequencies. It has also been used with tape at 3,000 pps. The coupling capacitors in the amplifier portion may be varied to optimize performance for various conditions such as overload characteristics and pulse repetition rates greater than 50 kc. However, the rise time of the output pulse is not a function of frequency. Since the amplifier portion of the circuit is a-c coupled there may be a significant settling time after a disturbance such as the application of a writing signal or a transient due to electronically selecting heads.

The circuit (Fig. 15) consists of two stages of push-pull amplification (Q_1Q_2 and Q_3Q_4) and is intended for use with balanced signals

10

uch as those obtained across a full head winding. If the winding is center-tapped the center tap would normally be grounded; however, the circuit works well even if the center tap is left floating. The amplification is controlled by introducting degeneration in the first stage. The amplifier stages drive two independent trigger circuits, the outputs of which can be combined when used with NRZ signals. The trigger circuits consist of an impedance-matching stage, Q_5 and Q_6; a trigger amplifier, Q_7 and Q_8; and a Schmitt trigger circuit, Q_9Q_{10} and $Q_{11}Q_{12}$. The impedance-matching stage serves to establish a d-c level for the signal which then remains d-c coupled through the remainder of the circuit. This stage drives the trigger amplifier which is normally biased off and conducts on negative-going swings. The trigger amplifier drives the Schmitt trigger circuit which furnishes an output pulse with a rise of at least 9 volts in less than one microsecond. This is adequate for application to flip-flops, one-shots, or external trigger gates. A pair of trigger gates is included on the package, in addition to the pulse outputs. The trigger gate outputs (pins 15 and 21) may be directly combined for application to a flip-flop or one-shot. The positive rise of the output pulse does not quite reach ground potential but remains slightly negative; hence, it should not be used as the input to an or-inverter. The duration of the output pulse will be determined by the duration of the input waveform, which is generally a function of the input pulse frequency. With NRZ signals it is possible that the output pulse from one trigger circuit may overlap that of the other circuit. This poses no problem, however, since the trigger gates respond only to leading edges and these will be well separated. A balance adjustment (R_2) is provided so that the two trigger circuits may be adjusted to respond to equal excursions of their respective waveforms. Each circuit responds to negative-going excursions, but since they are driven by opposite outputs of a push-pull amplifier these represent opposite swings of the input signal. A test point (pin 13 or 23) is brought out from the input to each trigger circuit at a low impedance point. The signals are still in essentially analog form at these points although some waveshaping may have taken place. Fig. 16 illustrates these various output waveforms.

When return-to-bias recording is used with a pulse spacing which is so close as to produce crowding of adjacent pulses a particular form of envelope distortion occurs, making it difficult to establish a suitable threshold. This can be corrected by adding a "d-c restorer" diode (CR_1 and CR_2) at the point where the signal passes from a-c to d-c coupling (the input to the impedance-matching stage). With return-to-bias recording a "one" is read as a positive to negative excursion, with the trigger circuit responding to the negative excursion. The restorer diode clips off any excessive swing in the positive direction and results in charging of the coupling capacitor (C_1 or C_2). The stored voltage then adds to the negative-going excursion which results in a much more uniform envelope. The coupling capacitor at this point must be small enough (approximately .001 μfd) to permit significant charging during one half-cycle.

11

A value this small may result in some loss of signal, necessitating a somewhat higher gain setting. At a frequency of 50,000 pps a value of .001 μfd for this capacitor gave satisfactory results.

As a result of the restorer diodes, the waveforms visible at the test points will appear to be half-wave rectified, having only negative excursions.

Typical applications of the Read Package are as shown in Fig. 17.

Indicator/Amplifier Package, Series 2

The circuitry for this package (Fig. 18) consists of that of our original indicator package plus a resistor (usually 620 ohms) for each transistor from -V to its collector. This enables the ten circuits in the package to be used either as a type 344 incandescent lamp driver with -V (pin 1) open, or as a common-emitter amplifier by providing -V (-12 volts).

Dual Write Package, Series 2A

This package is used for recording on magnetic tape or drum. It is intended for use with a center-tapped recording head and may be used for a variety of recording schemes such as non-return-to-zero (NRZ) or return-to-bias. There are two complete and independent circuits per package. Each circuit can provide up to approximately 200 milliamperes of write current, the actual value being determined by the recording head resistance and the value of the fixed current-limiting resistors on the package.

For normal operation, using the lower numbered half of the package (Fig. 19), a complementary input signal is connected to pins 2 and 11. The outputs (pins 3 and 5) are connected to the read-write busses (two lines common to the opposite sides of recording head windings). Pins 1 and 7 are terminals on a voltage divider from the read-write busses and may serve as inputs to a read package.

Pulse Generator with Flip-Flop, Series 2

A diagram (Fig. 20) of the circuit for this package is included only to show the proper wiring and pin connections when using a typical pulse transformer. The only other variation is in the value of the resistor, R_1 (56 ohms), across the feedback winding of the transformer. The function of this resistor is to prevent oscillations between pulses, therefore, its value which is dependent upon the inductance of the transformer may vary slightly.

A diagram (Fig. 21) of the circuit for this package, as for the previous one, is to show proper pin connections when using a typical pulse transformer.

IV SERIES 3 PACKAGES

After modifying some of the original circuit layouts and designing additional types of circuits for the Series 2 Packages, increasing costs (nearly doubled) of the mating connectors reached a level where we could not justify one of our original design criteria - that of economy. Since there was no directly replaceable connector available, it was decided that we change the connector type. This necessitated the redesign of all printed circuit layouts. For these reasons, plus the desire for a more compact unit, a complete set of Series 3 Packages were designed. A photograph of some Series 3 Packages plus two mating connectors is shown in Fig. 22. The conversion from Series 2 was accomplished without sacrificing reliability of the units and in some cases versatility was increased. The cost for each unit was considerably reduced so that at present the average cost per package, including mating connectors in quantities of 500 (assorted types), is less than fourteen dollars.

Major physical differences between the two series are: The Series 3 Units are constructed on smaller (3 1/8" x 4 3/4") fire retardant glass epoxy boards vs 4" x 5" XXXP phenolic for Series 2; the Series 3 connector is a 23-terminal blade-type vs. a 25-terminal pin-type; voltages and ground, where necessary, are located on common pin numbers for each package type; and test point jacks in assorted colors, which also serve to identify the package type, are at the top edge of most boards.

Using the Series 3 Packages in one of our standard drawer-type chassis, the density is increased from 72 to 110 packages per drawer. Figures 23 and 24 show the package and the wiring sides, respectively, of a typical drawer in one of our systems.

To conserve space and avoid repetition the only Series 3 packages described in this section are those with modified or entire circuitry which is unique to the Series 3 unit. Otherwise, as noted in Table 1, the descriptions of the circuits shown in Figures 25 through 38 may be found either in the Series 2 package descriptions of this report or in NBS Technical Note No. 68. In most cases the circuitry for both series is identical and differs only in pin numbers.

13

SERIES 3 PACKAGE TYPE	LOCATION OF DESCRIPTION	FIGURE NUMBER OF SCHEMATIC DIAGRAM (In this report)
Analog Switch	NBS Tech Note 68	25
Analog Voltage Comparator	"	26
Decimal Decoder	"	27
Dual Flip-Flop	"	28
Gated-T Input	This Report, Series 2	29
Indicator/Amplifier	"	30
Octal-Hexadecimal Decoder	NBS Tech Note 68	31
One Shot, Series 3	"	32
One Shot, Series 3A	This Report, Series 2	33
Pulse Gate Driver	"	34
Pulse Generator with Flip-Flop	"	35
Read	"	36
Sampler	"	37
Dual Write	"	38

TABLE 1

Dual Pulse Generator, Series 3

The circuitry for this package (Fig. 39) consists of a free-running blocking oscillator with its output connected to an inverting amplifier. Both circuits are identical to that included in the pulse generator with flip-flop package. The amplifier output may be inhibited by the application of a positive signal at pin 5 or 20. Two independent pulse generators are included on a board.

Pulse Gate, Series 3

The circuitry for this package (Fig. 40) is identical to that of the original gate package, series 2 with the exception that two of the input capacitors (pins 19 & 21) are connected on this board. This was necessary in order to place eight gate circuits on the board.

Amplifier, Series 3

This package (Fig. 41) consists of nine independent two transistor amplifiers which have an input impedance of approximately 40K and an output impedance of approximately 1K. The output remains in an off state (-12 volts) when the input level is between ground and -1 volt. An input signal of -2 to -12 volts amplitude will cause the amplifier to turn on causing the output to swing very near to ground (<0.5 volts).

And/Or Inverter, Series 3

The basic circuit (Fig. 42) of the and/or Inverter has not been changed but, in order to increase the versatility of this package the input diode configuration has been modified. There are four independent inverters, one with four fixed input diodes and three with one fixed input diode. Also, included on the board are a group of three diodes and a separate pair of diodes. Each of these two combinations have a common anode connection which may be tied into any of three of the inverters with a connection brought out from its base circuit. In this manner multiple input inverters may be formed with a maximum of nine inputs to a single inverter on one board.

BCD Counter, Series 3

This package (Fig. 43) consists of four of our standard flip-flops connected as a serial binary 1-2-4-8 counter with the necessary feedback gating to enable it to function as a binary coded decimal counter. The counter may be reset electronically by applying a positive going pulse with a minimum of six volts amplitude (referenced to -V) and a rise of at least six volts in one microsecond. If it is desired that the counter be reset manually the emitter bus (pin 15), which is common to one emitter of each flip-flop, is connected through a normally closed switch to ground. Opening this switch would reset the counter. If a manual reset is not required the

emitter bus may be tied directly to ground (pin 22). Both collectors
of each flip-flop are brought out to individual pins. The input signal
characteristics are the same as for a standard flip-flop.

V. LOGICAL SYMBOLS

In the absence of the adoption of a standard set of logical
symbols by any of the national organizations responsible for this task
we have developed the following symbols which we feel convey an
adequate representation of the logical functions of the various
schematic diagrams.

Pulse Gate

(circuit and symbol)
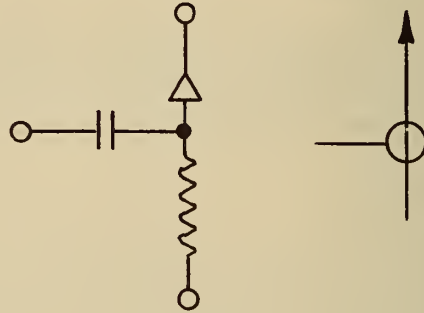
Flip-Flop

T input

Relative voltage levels for
zero or reset state is indicated
($\pm$) inside symbol
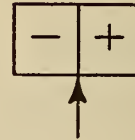
JK inputs

(Internal pulse gates)

16
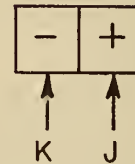
RS inputs

Requires external pulse gates

Note: external gate connections
to base are shown by
placing arrows at the
corners of the block.
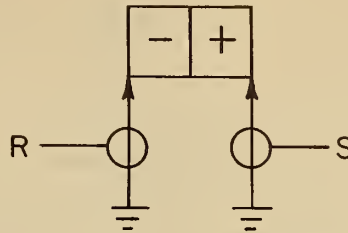
SYMBOLS FOR INTERCONNECTED FLIP-FLOPS

SHIFT PULSE
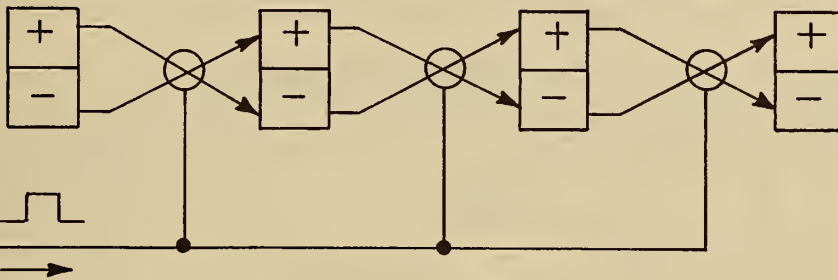
Shift Register -using internal gates

Each circle in the above diagram symbolizes
the common connection of a pair of capacitors
which are included in the two internal pulse
gate circuits contained in the flip-flop to its
left.

SHIFT PULSE
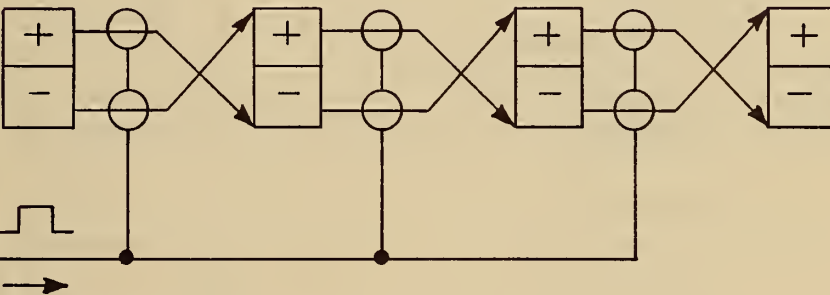
Shift Register -using external gates

Each circle in the above diagram symbolizes
the capacitor of a standard pulse gate as
previously noted.

17
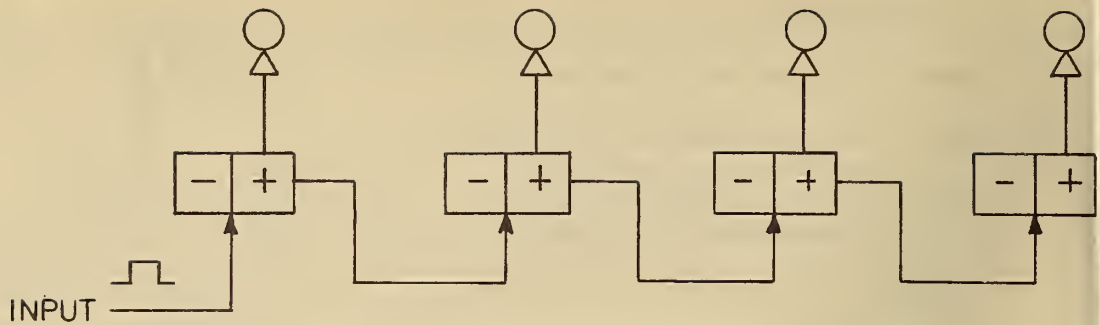
<u>Serial Binary Counter</u> -with indicators

In the above diagram, the symbol above each flip-flop
(circle and triangle) represents an indicator/amplifier driver.

<u>AND/OR INVERTER</u>
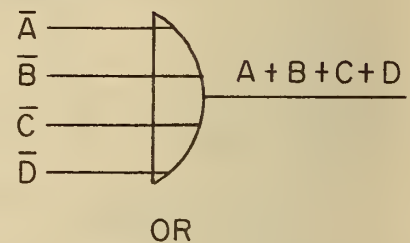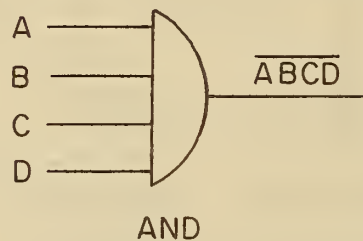
This symbol was adopted not only for its ease of drawing but
also because it readily indicates whether the circuit is used as a
logical AND or a logical OR. One may start at the beginning, middle,
or end of a logical diagram and know, at any point, what the signal
polarity is.

The above symbols are modified for the series 3 package to
indicate the internal connection, if it is used, for increasing the
number of available inputs. Its symbols are shown below with one
internal connection (6 to 17) and typical pin numbers.

18
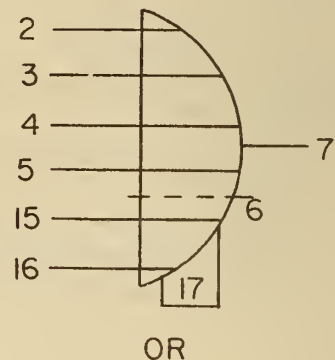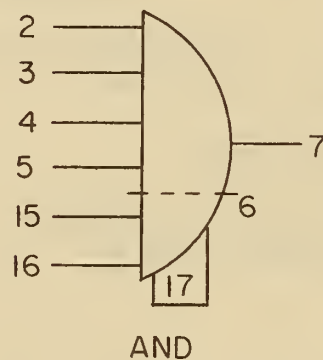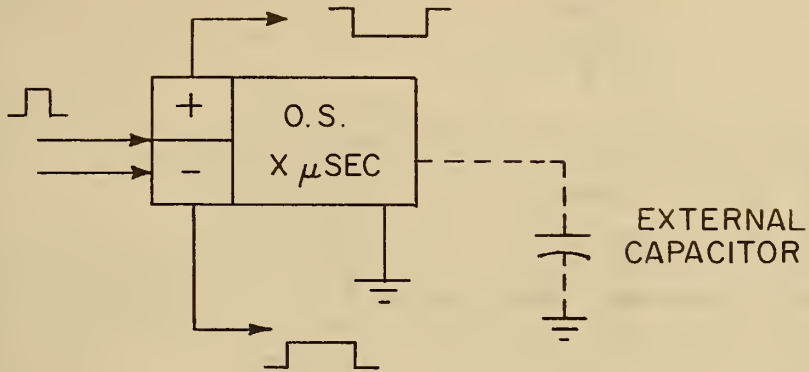
This composite symbol, which represents a one-shot, is a flip-flop with input and output lines of a one-shot package joined to a block indicating the internal capacitor ground, or external capacitor used and duration of the output pulse.

SAMPLER
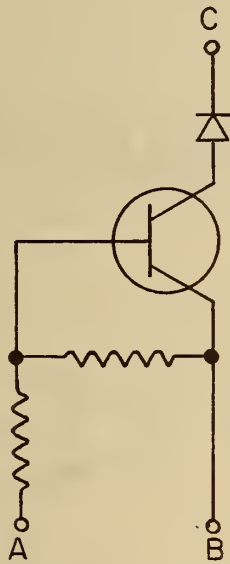
CIRCUIT

SYMBOL

GATED-T INPUT

CIRCUT

SYMBOL
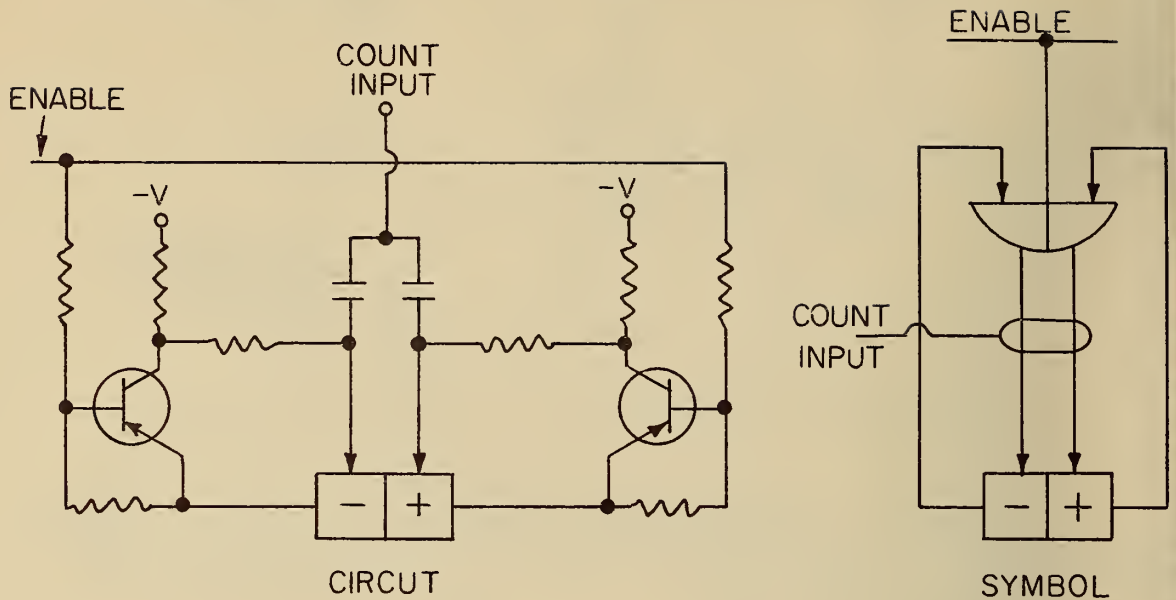
The example above shows one bit of a counter/register with feedback coming from the outputs of the flip-flop to which the Gated-T input is connected. This is the normal feedback; however, for special applications feedback connection may come from another flip-flop.

OTHER CIRCUITS

Circuits such as the Pulse Gate Driver, Read, Write, and special packages are denoted by a block so labeled with input-output lines indicated as shown below:
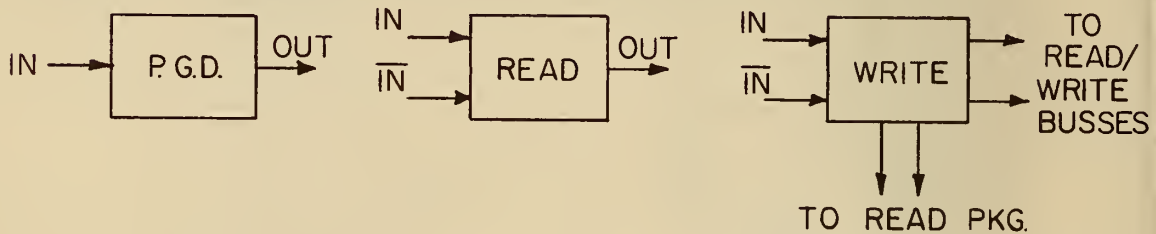
VI.   EXAMPLES OF DESIGN PROBLEMS

The following examples were chosen to emphasize a few logical design techniques. Also, this section demonstrates the use of our adopted logic symbols.

The first example is the design and logic of a binary decimal four bit counter. As one knows, there are several methods of constructing a counter but there are two basic techniques, serial and parallel. In a serial counter each flip-flop change occurs after that of a preceding stage. The number and type of stages determine the total time required for the counter to reach its quiescent state. In a parallel counter each flip-flop assumes its final state simultaneously. Therefore, this type counter is faster and allows one to examine or remove contents of the counter in much less time than from a serial counter. Using the techniques described in M. Phister's text, * "Logical Design of Digital Computers", an example of the design of a parallel binary coded decimal (BCD) counter is described below.

As stated in Phister*, the originally defined behavior of a flip-flop is that it changes its state after the initial application of an input pulse. This is necessary if one of the flip-flop outputs is connected to an input and-gate. It insures that changing of the flip-flop state will not affect the gate because the flip-flop change does not occur until the input pulse is no longer present. Since our flip-flops change state only when a positive rise is sent into the input, and we are using and-inverter stages for gating structures on the inputs, the flip-flops will not change state until the trailing edge of an input pulse. This type of input connection has not only the logical value indicated, but also may be used for another which is; there is now a specification on the input pulse shape. It must be at least 10 microseconds in duration to satisfy the input time constant required for charging the input capacitors of the flip-flops. Therefore, no noise pulse of shorter duration may trigger the flip-flops.

The simplest input equations for a parallel BCD counter are:

$$J_A = BCD, \; K_A = D$$
$$T_B = CD$$
$$T_C = \overline{A}D$$
$$T_D = 1$$

A logical diagram illustrating the parallel BCD counter described above is shown in Fig. 44.

Serial counters may be constructed as shown in Fig. 45. These counters propagate the signal from flip-flop to flip-flop, resulting in a considerable time delay before the last flip-flop in the series assumes its proper state.

* cit. , p. 3.

The second example of a design problem is the logical design of a parallel adder which is incorporated into ACCESS, a computer being designed and constructed for the Office of Emergency Planning.

A parallel adder requires a few more packaged circuits in the actual adder section than for a serial adder; however, it simplifies the logic and decreases the number of packages required in the control circuitry in addition to operating at a higher speed.

Consider the addition of bits An and Bn of the A and B registers, as shown in Fig. 46. The present states of An and Bn must be combined with the carry from the previous stage, if there is one, to determine the state of An after the addition (A contains the sum) and the state of the carry to the next stage.

Table A represents Cn + 1, the carry to the next stage (n + 1), and An^{n+1}, the state of the adder stage under consideration (n) after the addition, as functions of the three variables An, Bn, and Cn, the present states of the nth stage of A and B and the carry from the previous stage. From this table Cn + 1 and An^{n+1} are represented as Boolean functions and simplified as follows:

$$Cn + 1 = \overline{A}nBnCn + An\overline{B}nCn + AnBn\overline{C}n + AnBnCn$$

Simplified,

$$Cn + 1 = AnBn + AnCn + BnCn$$

and

$$An^{n+1} = \overline{\overline{A}n\overline{B}nCn} + \overline{A}nBn\overline{C}n + An\overline{B}n\overline{C}n + AnBnCn$$

An	Bn	Cn	C_{n+1}	An^{n+1}
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

TABLE A

22

Employing the input equation of a T input flip-flop,

$$T = \overline{Q^n} \; Q^{n+1} + Q^n \; \overline{Q^{n+1}},$$

where Q^n is the present state and Q^{n+1} the desired state of the flip-flop after the input, T. This is a function for the input to An as a T input flip-flop so that it represents the function An^{n+1}. The sum in the addition is

$$T = Bn\overline{C}n + \overline{B}nCn$$

These functions for the sum and carry can be developed for each stage of a multi-stage adder, and are implemented in the general stage as in Fig. 47.

The actual addition of B to A, the input to An if the variables are in the appropriate states, occurs at the trailing edge of the add command. However, the conditions setting up Cn for each stage must be stable before such an add command is given. Note that the condition of each Cn depends upon that of the previous stage, and that this dependence continues until the least significant stage of the adder is reached, at which point the carry is merely a function of $A_{stage\ 1}$ and $B_{stage\ 1}$. Thus, as soon as the least significant stages have been set up for the add operation, the carry exists as a variable for the next adder stage.

The time necessary for the carry to be set up at the most significant end of the adder, after completing the setup of the least significant stage, is known as the propagation or ripple time of the adder. This time, the sum of the propagation times of the individual stages, limits the speed of the parallel adder. In ACCESS the propagation time through the one word length adder is on the order of 18 microseconds and for double word length, 36 microseconds.

The ACCESS parallel adder, as shown in Fig. 48 consists of two sections, each section containing 12 stages controlled by common micro-operation lines. These micro-operations to the adder are the add command, either single or double word length; and the carry command. The carry command is activated for all operations involving the adder except Modulus 2 Add.

The basic adder adds the absolute values of A and B. In the complete addition operation it is necessary to consider the signs of A and B, and to sequence through control operations according to certain rules. Table B shows the procedure to be followed for each of the four possible combinations of A and B.

	Original Signs		Comp	Carry	No Carry	Final Sign
	A	B	A			
1.	+	+	no	set OF		+
2.	+	-	yes	add 1		-
					comp	+
3.	-	+	yes	add 1		+
					comp	-
4.	-	-	no	set OF		-

TABLE B. Addition Procedure

Interpretation of the Table is as follows:

1. If both A and B are positive, S (sum) equals A + B, and if a carry exists from the addition the overflow flip-flop is set. The sign of the final sum is positive.

2. If A is positive and B is negative, A is complemented before adding it to B. When a carry exists from this addition, a "one" is added to the sum. In this case the final sign is negative. If there is no carry, the sum is complemented and the final sign is positive.

3. If A is negative and B is positive, A is complemented, then added to B. If there is a carry, "one" is added and the final sign is positive. If there is no carry, the sum is complemented and the final sign is negative.

4. If both A and B are negative, A is added to B, the final sum being negative, and the overflow flip-flop is set if a carry occurs.

A block diagram of the micro-operations required to carry out this procedure is shown in Fig. 49. The following steps, referenced by number to this figure form the add operation sequence.

1. Transfer the word to be added from the operand address to the B register.

2. Compare the signs of A and B. If they are different, complement A and set the complement flip-flop.

3. Add B to A, leaving the sum in A.

4. If a carry exists from the most significant stage of the adder, set the carry flip-flop.

5. If the complement flip-flop and the carry flip-flop are both on, reset B to "one". Otherwise, reset B to all "zeros".

6. If the carry flip-flop is on and the complement flip-flop is off, set the overflow flip-flop.

7. If the complement flip-flop is on and the carry flip-flop is off, complement A.

8. If the complement flip-flop and the carry flip-flop are both on, add the "one" in B to A.

The actual control logic utilized to set the various flip-flops is shown in Fig. 50.

This sequence of operations is executed by developing a special set of timing pulses for the addition operation. The time necessary

25

for each part of the sequence includes the various add commands and commands for setting flip-flops as well as the time necessary for the carry propagation before the actual addition can occur. Since most of the control is the same for single or double length addition, the timing for the two modes is similar. The carry propagation is twice as long for a double length as for a single length word, so pulses are divided by two for double length operation, providing more than sufficient time for the propagation.

Fig. 51 shows the add timing pulses: Sector Compare, (1), (2), and (3). All operations occur at either the leading or trailing edge of these pulses. The pulses (1), (2), and (3) are generated by feeding the bit pulses (or the bit pulses divided by two for double length operation) into a three-stage counter. The separate lines for pulses (1), (2), and (3) are activated as the counter reaches the appropriate states.

The actual Control sequence for the addition operation is as follows:

At Ta   The beginning of the operation resets the overflow, carry, and complement flip-flops.

At T_{sc} During the sector compare time the word to be added is transferred from memory into the B register. If the operation is double length, the sector compare pulse remains on for two word times.

At Tb   If the signs of A and B are different, complement A and set the complement flip-flop. The time between Tb and Tc is occupied by the carry propagation which occurs after complementing A, if this is done.

At Tc   The actual add occurs and the carry flip-flop is set if conditions are as specified in the procedure.

At Td   B is reset to "zero" or "one", the overflow flip-flop is set, and A is complemented if conditions are correct.

At Te   B is added to A if B has been set to "one" and the end of operation signal is given.

All sections of the control are identical for single or double length operation except the add command. The add command is actually fed to both halves of the adder in the double length mode.

Other operations employing all or part of this addition control circuitry are Subtract, Mod 2 Add, Multiply, and Divide. The Subtract operation changes the sign of the word from the memory immediately after its transfer into the B register, then executes the add operation in its entirety. The Mod 2 Add operation merely adds the operand to A without activating the carry command and causing no change in the signs of the A register.

VII. YIELD AND RELIABILITY

A majority of the transistors used in our transistorized building blocks are type 2N414 alloy junction units. In our original designs, a few years ago, this type was specified because a transistor type of the entertainment variety such as the 2N414 (an RF amplifier) was the best choice for obtaining low-cost, stable characteristics transistors. At that time this particular type was being produced by only one manufacturer, but now it is produced by many companies which has helped to keep the cost down.

To maintain low manufacturing costs for our building blocks we do not require our contractors to perform qualitative tests on the transistors used. It is only necessary that a unit exhibit transistor action regardless of the other parameters. Therefore, our requirements are for a consistently uniform distribution of characteristics from one transistor order to another.

Our circuits using 2N414 transistors are designed for a beta range of 20 to 200. Normally, if one purchases a number of this type transistor off-the-shelf from a wholesaler, the beta can be expected to fall within this range virtually 99.9% of the time. A graph of the normal distribution of current gain for a 2N414 type transistor is shown in Fig. 52. The data used for these plots was obtained from d-c beta measurements of a random selection of units produced by four manufacturers and purchased from a wholesaler. These measurements were taken with I_c = 1 ma and V_c = 6 volts. A distribution such as that exhibited by manufacturer B has proven to be most satisfactory. Using transistors with this distribution in our building blocks the rejection rate for modules containing them has consistently remained at less than 5% which is quite acceptable.

An effort was made to devise a simple measurement technique for determining the acceptability of a group of transistors by making a single measurement on each unit. After experimenting, it was decided that measurements of f_t (frequency at which h_{fe} = 1) would provide the most applicable data. The gain (h_{fe}) of a type 2N414 transistor is linear at the lower frequencies (below 1 mc) and then rolls off at a slope of 6 db/octave. The gain-bandwidth product along this slope is constant; therefore, a circuit was designed (Fig. 53) for measuring gain at a fixed frequency of 1 mc, to determine the gain-bandwidth product for the test unit. Since our frequency is fixed at 1 mc, gain is interpreted as f_t.

27

In our test circuit the input generator is set at a frequency of 1.0 mc and an amplitude of 0.1 volt peak-to-peak which provides an i_b of 10 μa. The 500K pot is then adjusted until the I meter reading is 6 ma which assures a d-c collector voltage (V_c) of 6 volts. The voltage drop across the 10 ohm resistor, which is observed on the VTVM, is very nearly equal to the small signal a-c collector voltage (v_c) because the drop across the 5 μf capacitor is negligible. The small signal a-c collector current (i_c) may be determined from this value. Then the gain (h_{fe}) is equal to i_c divided by i_b which, because of the circuit values used, may be read directly from the VTVM if it is set on the proper (X 10,000) scale.

Fig. 54 shows the distribution of f_t for a group of 2N414 transistors which includes the same units used for the previous graph. Units with a distribution such as that exhibited by manufacturer B produced a very satisfactory yield when used in our modules.

Judging from both graphs it appears that the units produced by manufacturer D should operate equally well with an acceptable yield. However, at present the number of transistors from this source which are used in our modules has been rather limited and not sufficient for an acceptable appraisal of yield and reliability.

APPENDIX

The diode designated as type DR435 is a gold-bonded germanium unit with controlled forward voltage drop and the following characteristics:

peak inverse voltage - 20 volts

minimum forward current - 10 ma at 0.37 volts

maximum average rectified current - 100 ma

maximum reverse current at 25°C - 10 μa at 10 volts

Although type DR435 is indicated on the drawings, any diode meeting the above specifications would be satisfactory.

In all schematic and board layout drawings the following component notations shall apply:

1. All capacitors not specified as micromicrofarads (μμf) shall be in microfarads.

2. All resistors shall be 1/2 watt units unless specified otherwise.

3. All resistors are in ohms unless specified as kilohms (K) or megohms (M).

4. The voltage rating of all capacitors shall be 15 volts or greater unless specified otherwise.

5. The notation NC on a potentiometer terminal indicates no connection.

The Board Layouts (Figs. 55 to 84) show enlarged views of each printed-circuit board with components layout for any new series 2 packages designed since NBS Technical Note 68 as well as any which have been modified. Also included is a complete set of series 3 layouts. In all cases the printed-circuit side of the board is shown.

29
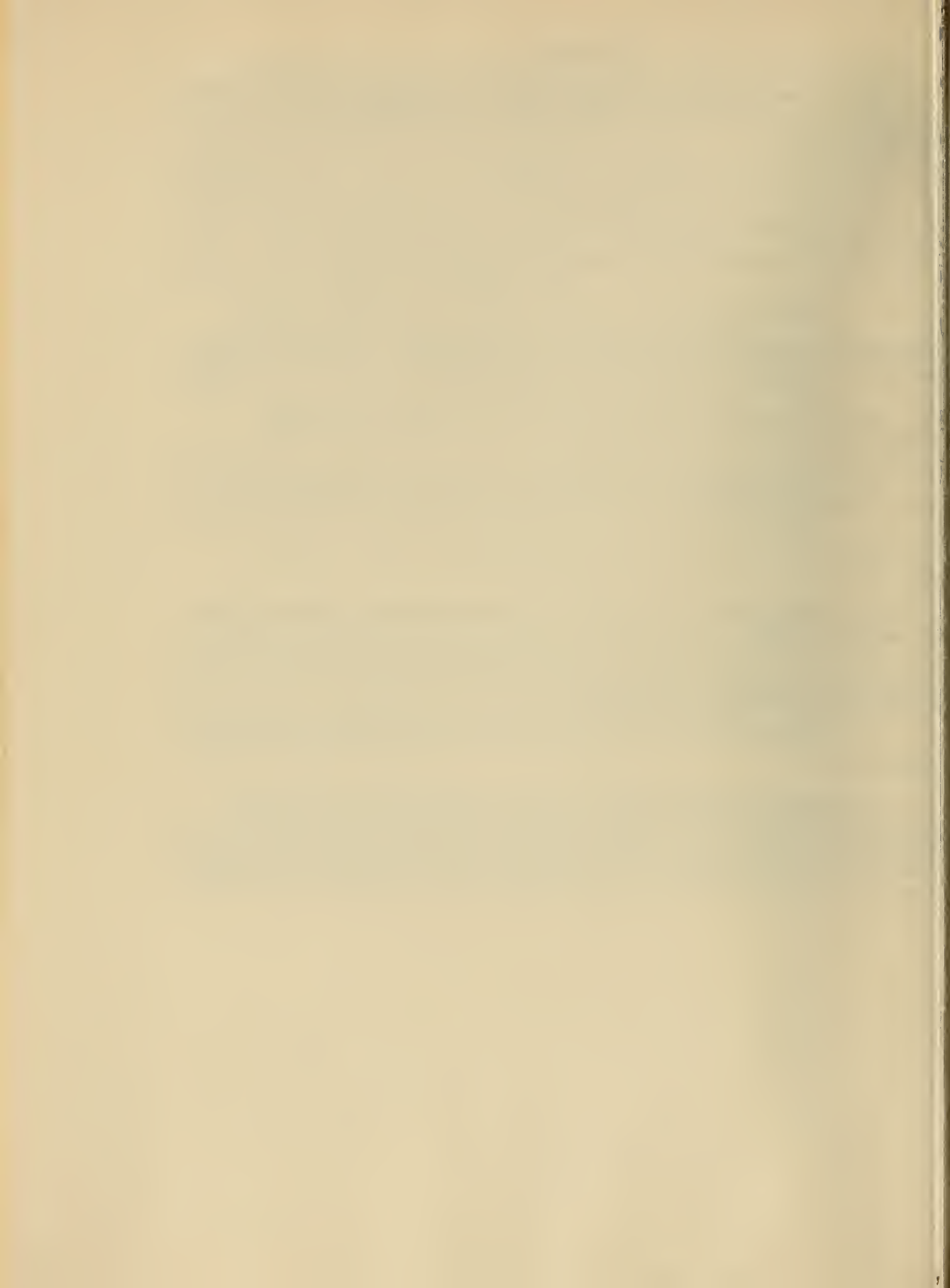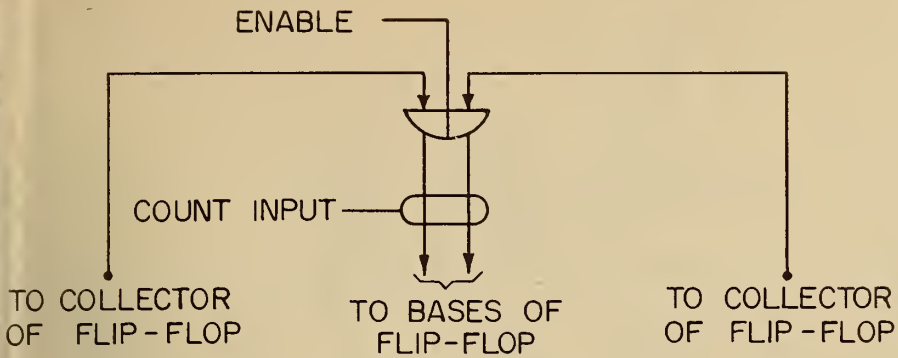
GATED "T" INPUT SYMBOL
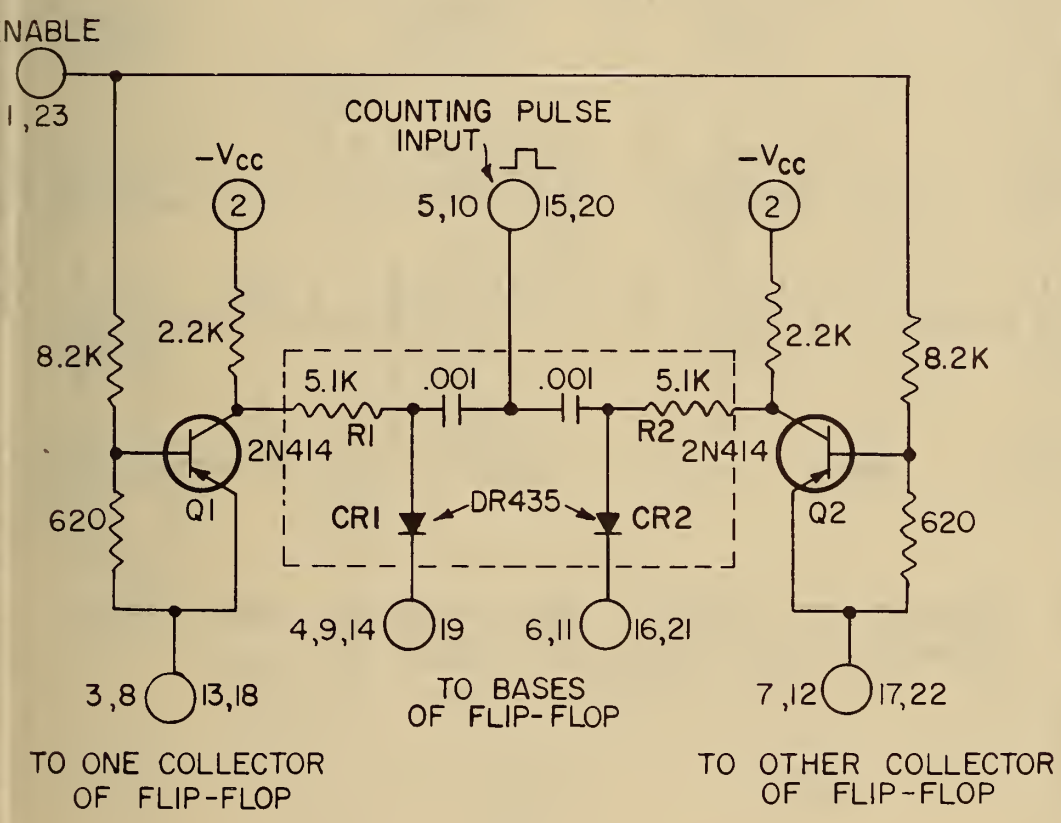
FIGURE I. GATED "T" INPUT, SERIES 2
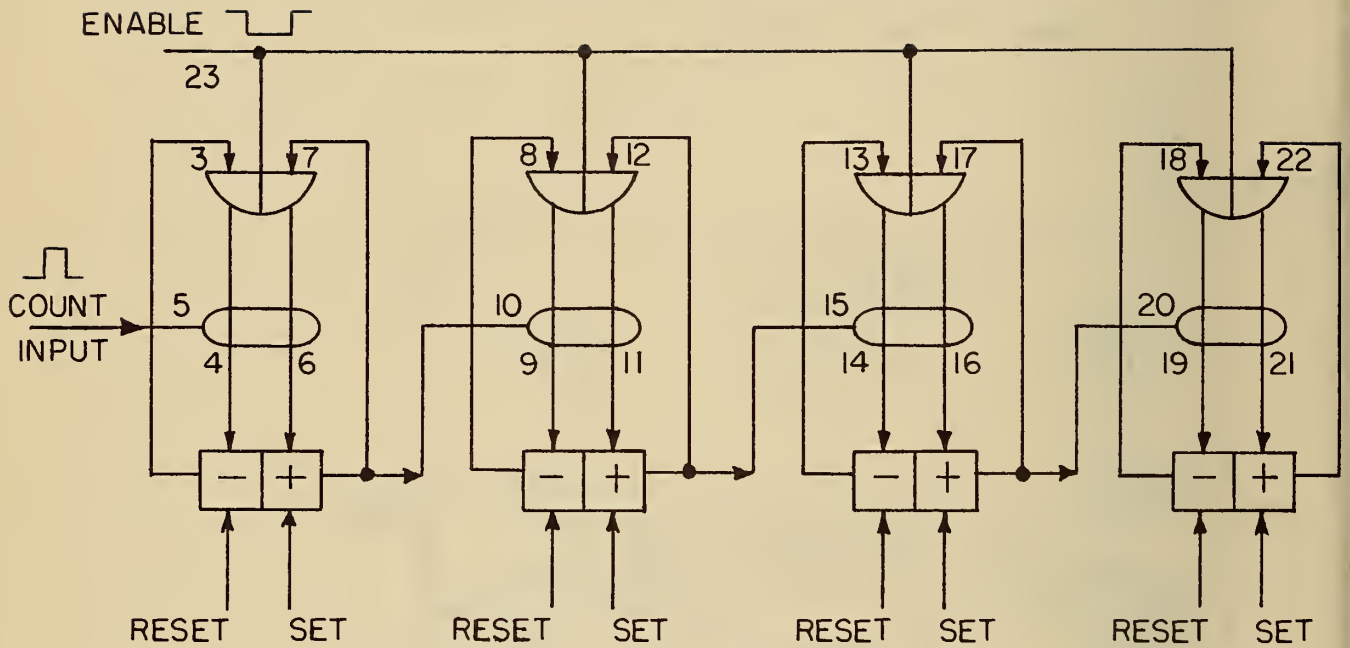
FIGURE 2. EXAMPLE OF GATED-T INPUT PACKAGE USED WITH COUNTER/ SHIFT REGISTER (SERIES 2).
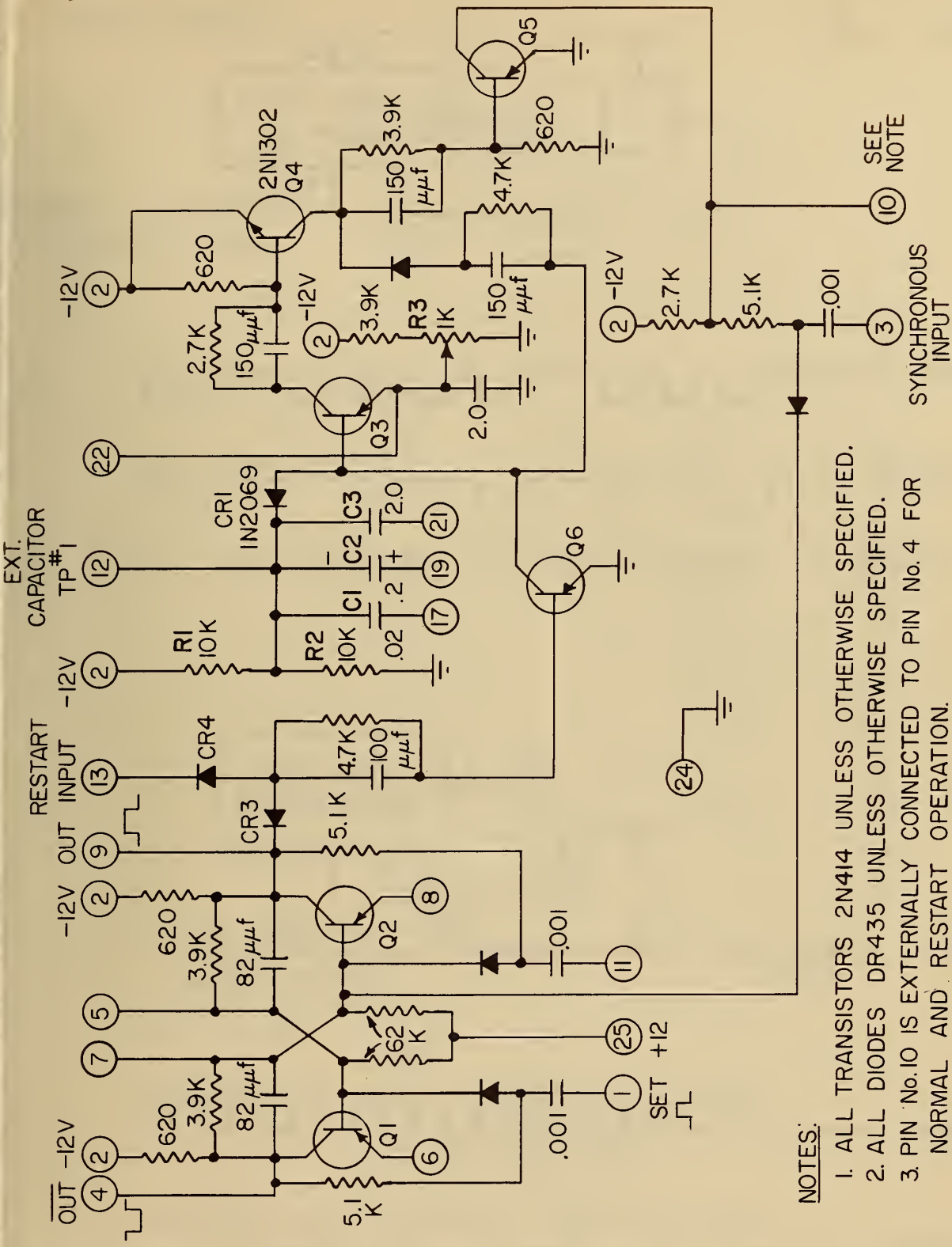
FIGURE 3. ONE-SHOT SERIES, 2A

NOTES:
1. ALL TRANSISTORS 2N414 UNLESS OTHERWISE SPECIFIED.
2. ALL DIODES DR435 UNLESS OTHERWISE SPECIFIED.
3. PIN No. 10 IS EXTERNALLY CONNECTED TO PIN No. 4 FOR NORMAL AND RESTART OPERATION.

SEE NOTE

SYNCHRONOUS INPUT

EXT. CAPACITOR TP#1

RESTART INPUT

OUT

SET

2N1302 Q4
Q5
Q3
Q6
Q1
Q2

CR1 IN2069
CR3
CR4

R1 10K
R2 10K
R3 1K

C1 .02
C2 .2
C3 2.0

INPUT →

RESTART INPUT

I

I3

TIMING AND
TRIGGER CKT.

+ | −

EXTERNAL JUMPER
PIN 4 TO PIN IO

INPUT

OUTPUT

FIGURE 4.   RESTART OPERATION FOR ONE-SHOT, SERIES 2A.

TIMING AND
TRIGGER CKT.

+ | −

INPUT →
PIN I

TRIGGER GATE
INPUT (PIN 3)

INPUT

OUTPUT
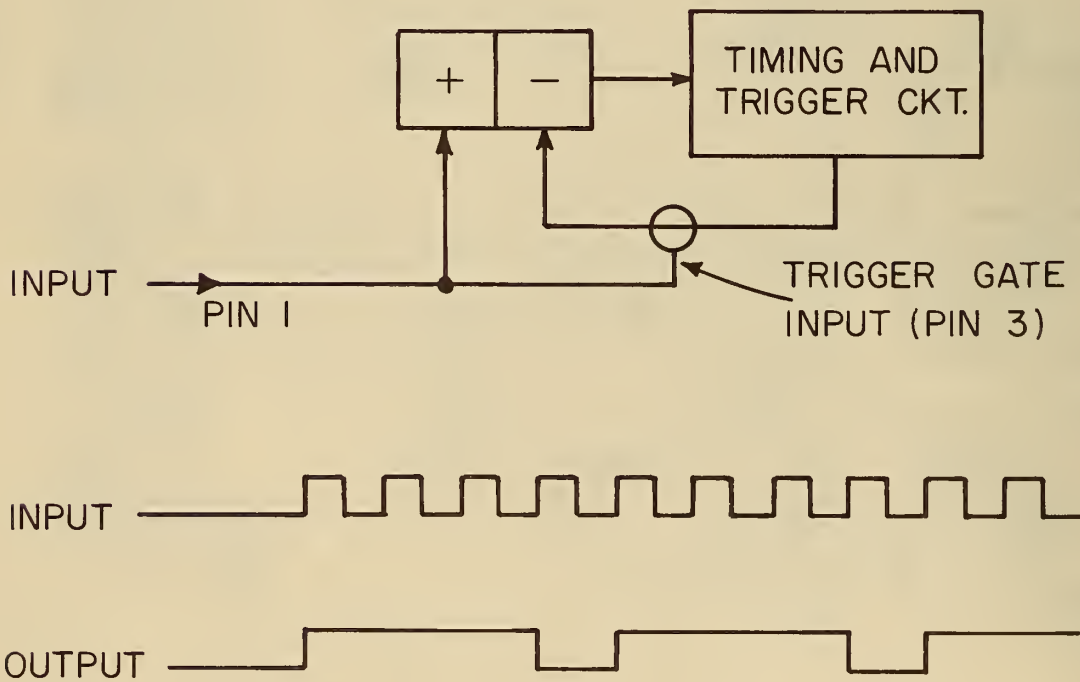
FIGURE 5.   SYNCHRONOUS TURN-OFF OPERATION FOR
ONE-SHOT, SERIES 2A.
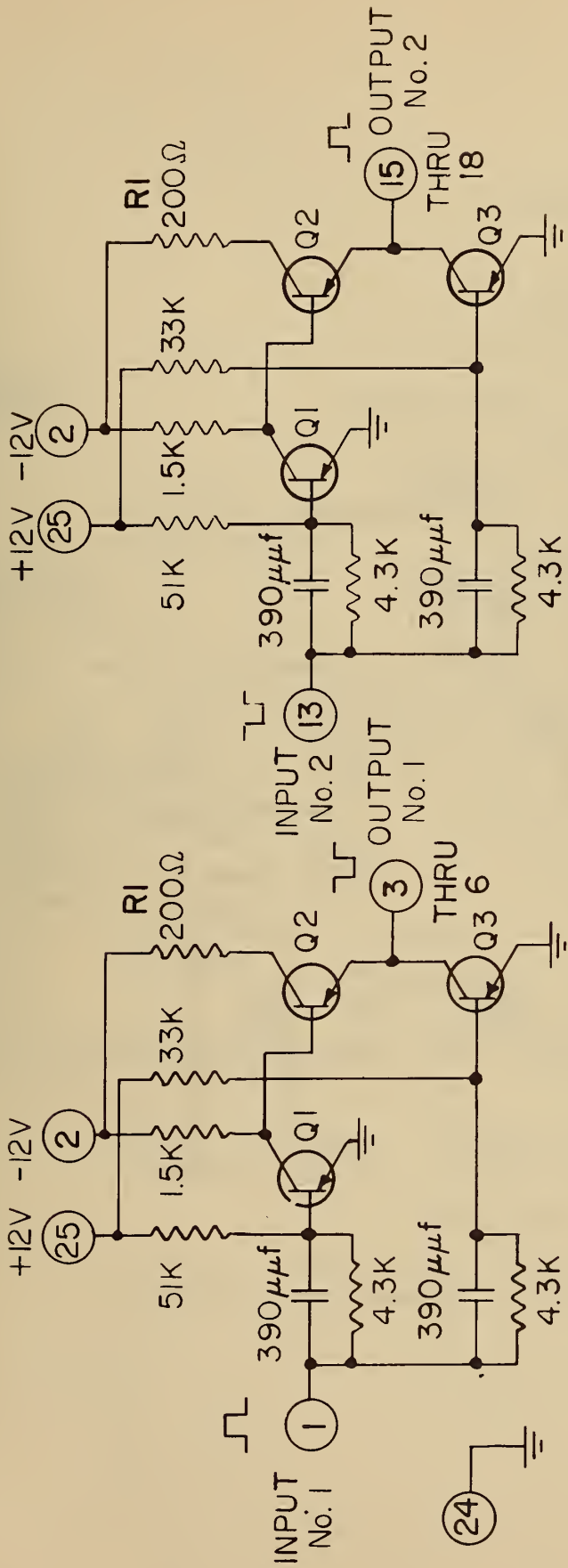
ALL TRANSISTORS 2N414.
ALL RESISTORS 1/2 WATT.

FIGURE 6. PULSE GATE DRIVER, SERIES 2
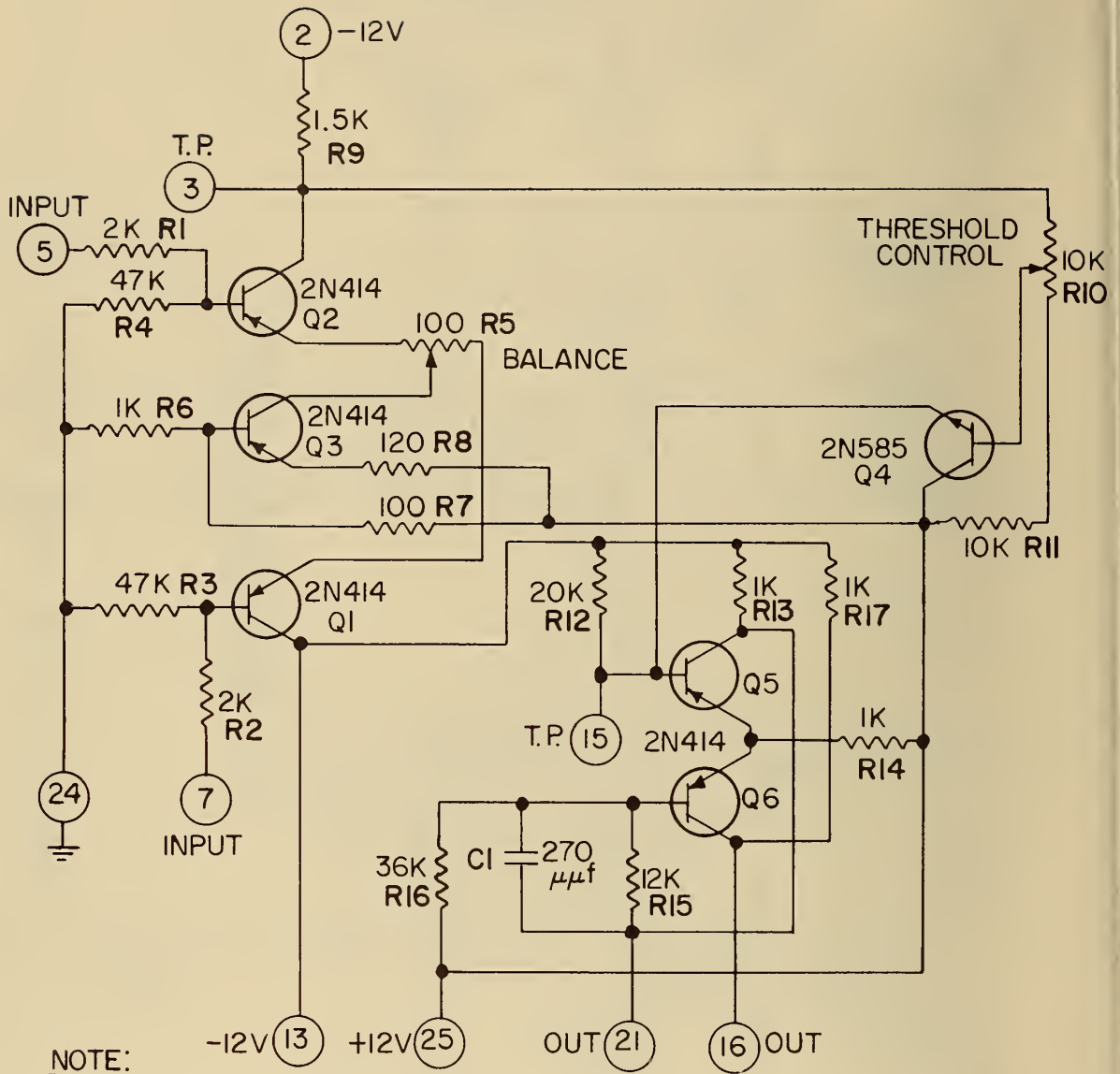
FIGURE 7. PREAMPLIFIER, SERIES 2
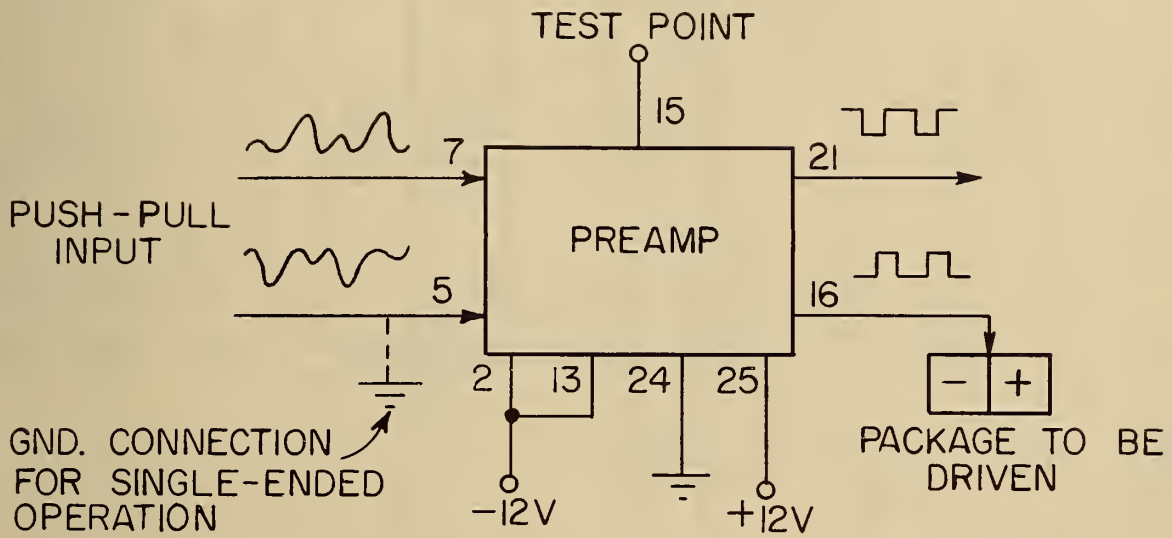
FIGURE 8. CONNECTION DIAGRAM FOR PREAMPLIFIER PACKAGE
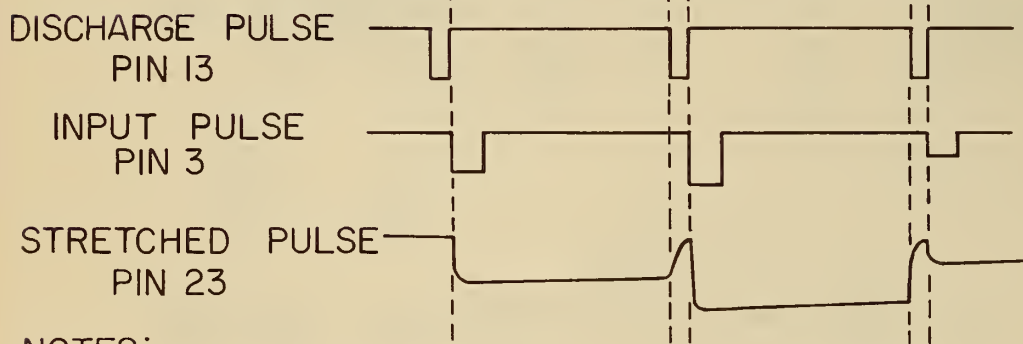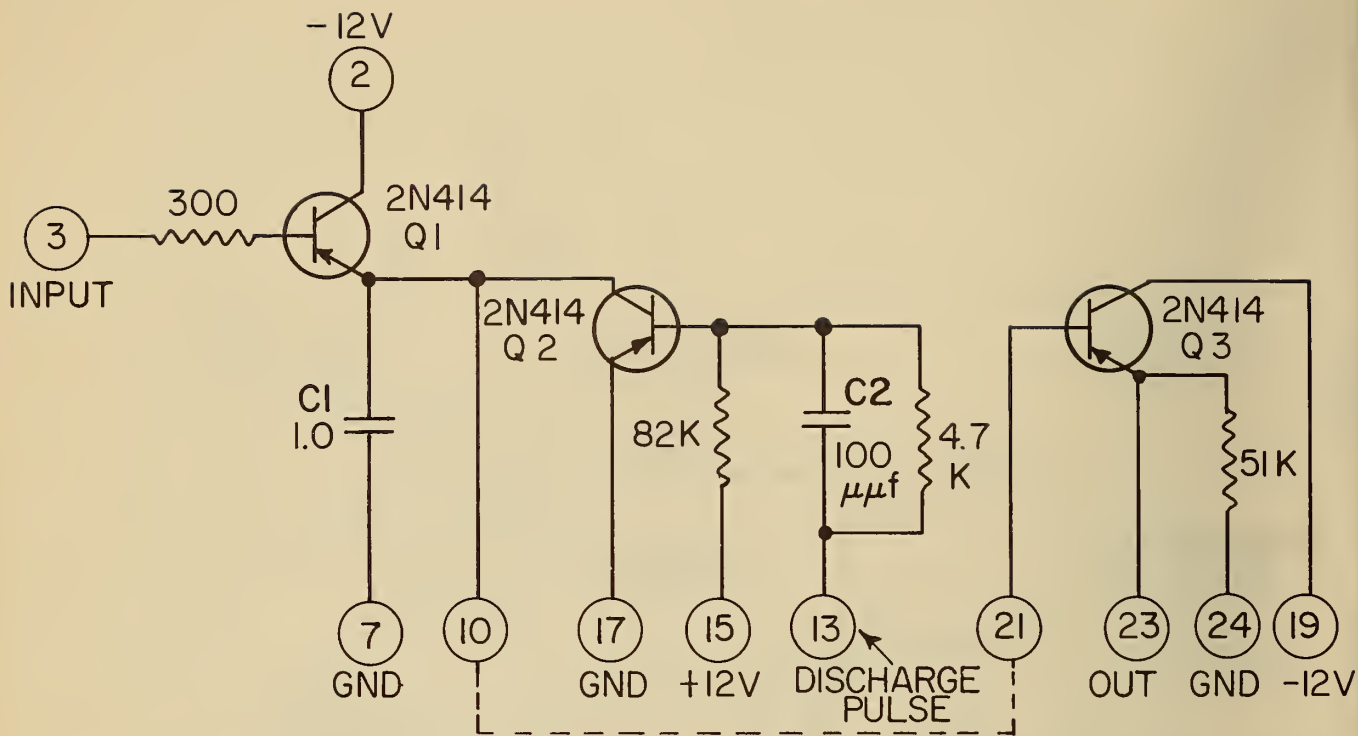
NOTES:

    1. PINS 10 AND 21 CONNECTED FOR NORMAL OPERATION.
    2. R AND C VALUES ARE TYPICAL, BUT SUBJECT TO
       CHANGE DEPENDING ON APPLICATION.
    3. ALL RESISTORS ARE 1/2 WATT.

FIGURE 9.   PULSE STRETCHER PACKAGE, SERIES 2
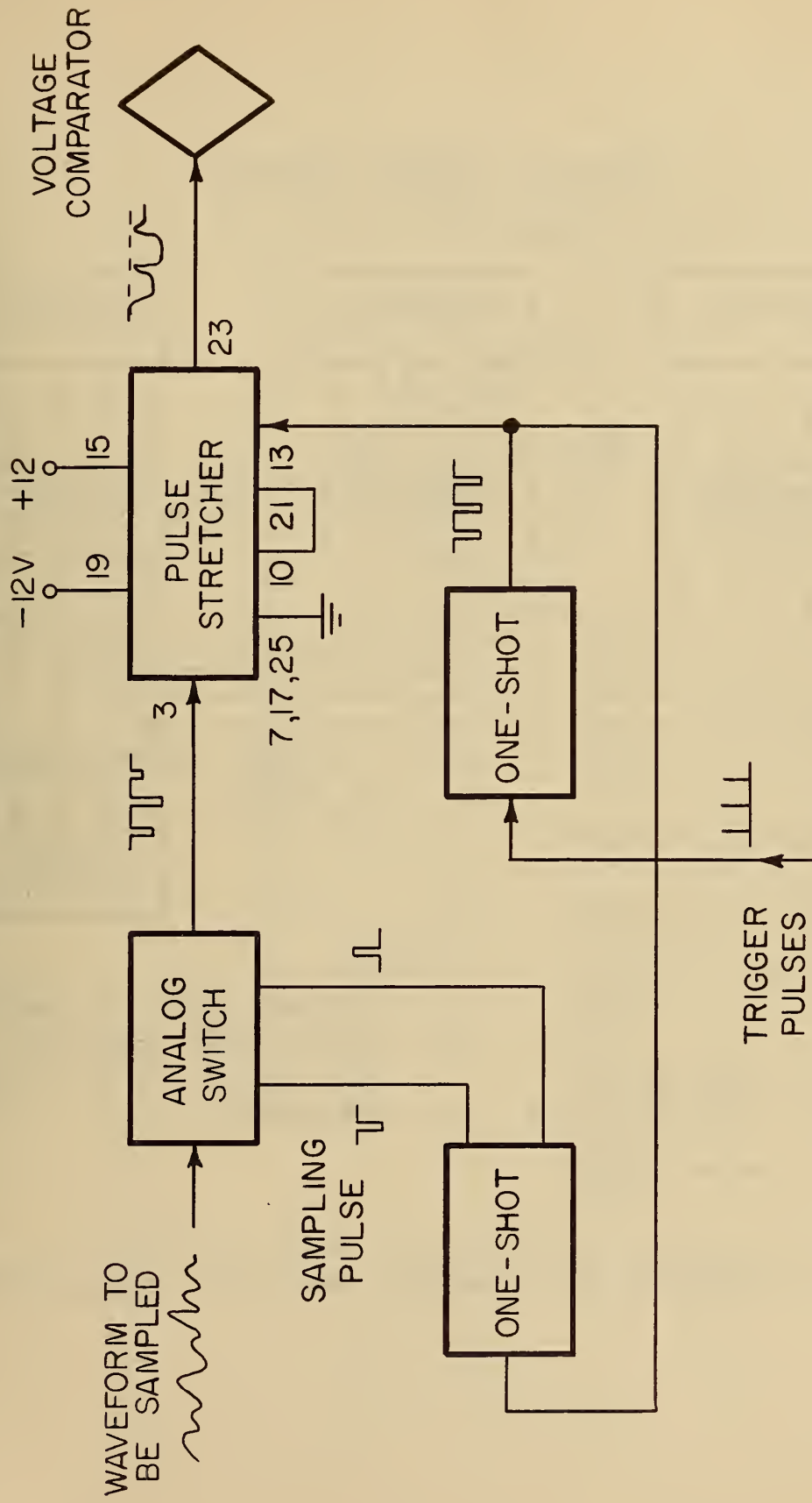
FIGURE 10. TYPICAL CONNECTION DIAGRAM FOR PULSE STRETCHER PACKAGE
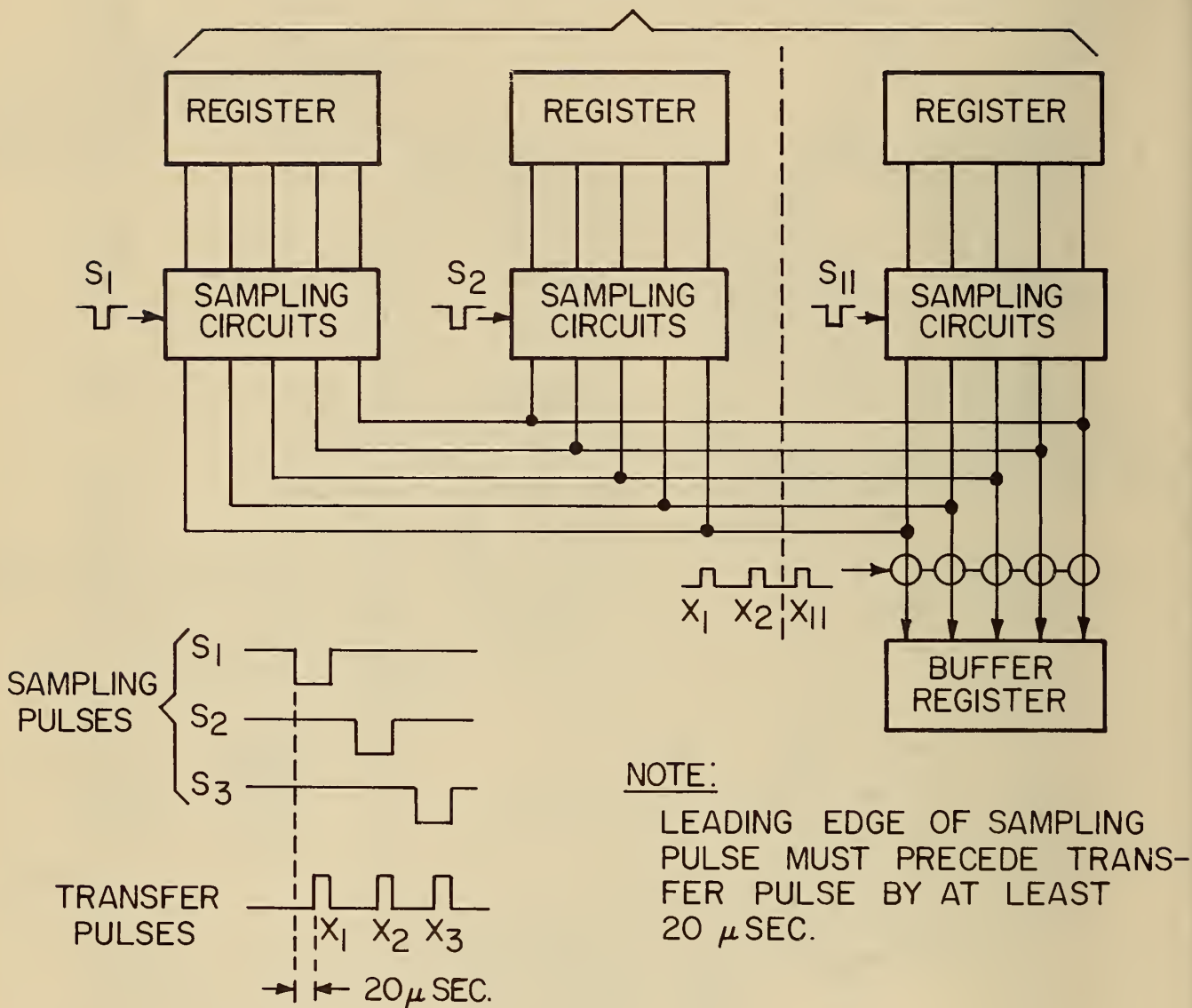
FIGURE II. EXAMPLE OF SAMPLER PACKAGE APPLICATION

SYMBOL

2N4I4

620   HB-2

8.2K

a   b   c

PIN NOS	PIN NOS.	PIN NOS.
1	2	3
6	5	4
9	8	7
12	11	10
14	15	16
17	18	19
20	21	22
25	24	23
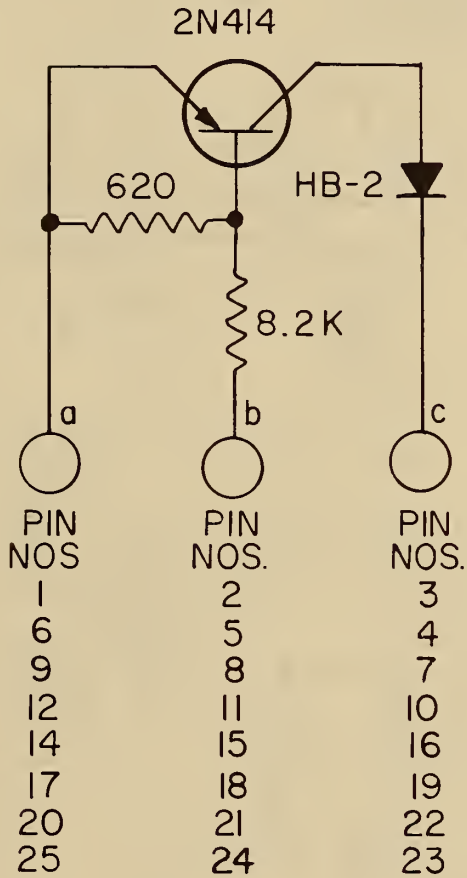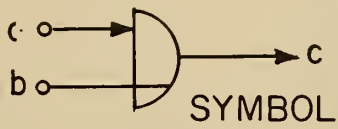
8 CIRCUITS PER PACKAGE

FIGURE 12. SAMPLER PACKAGE, SERIES 2
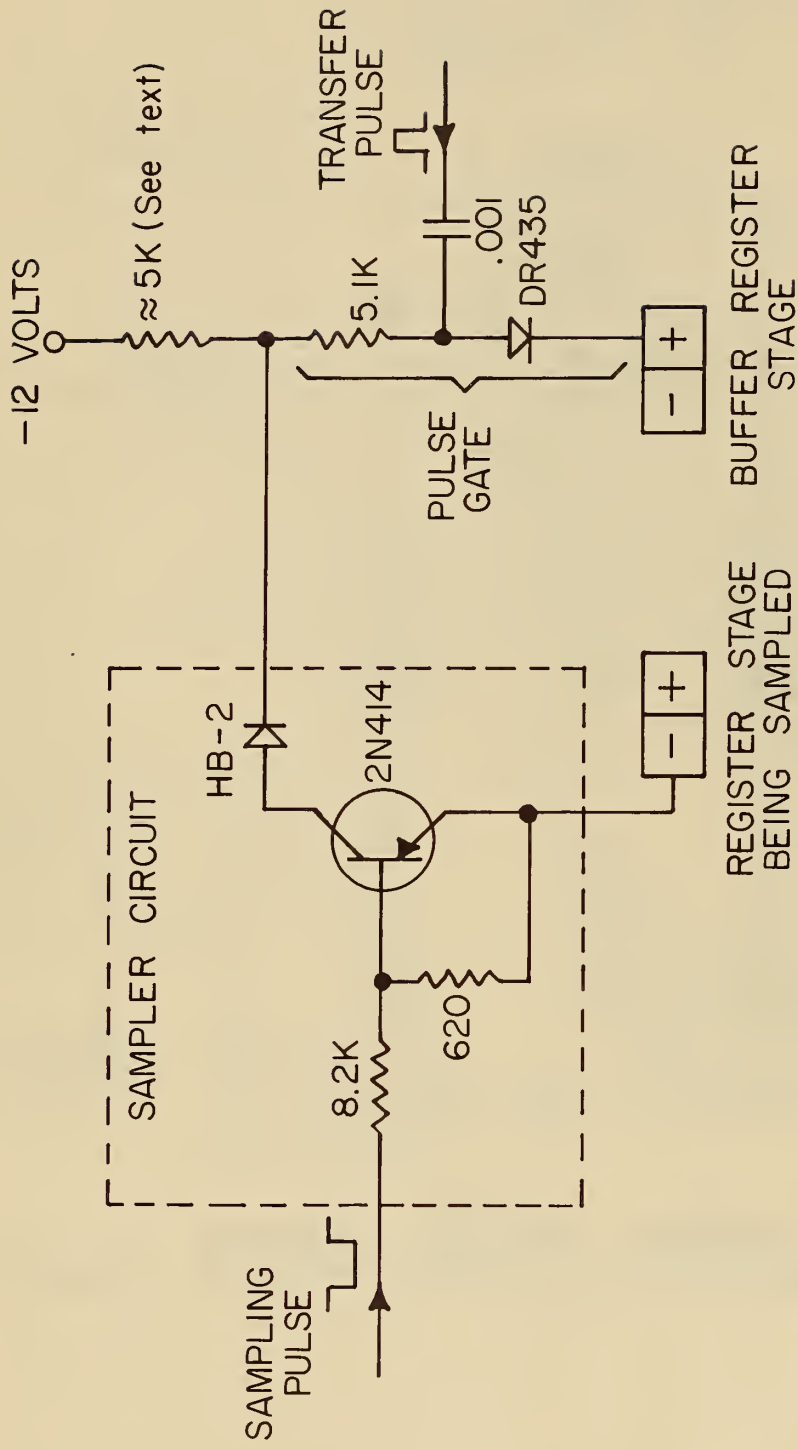
FIGURE 13. WIRING CONNECTIONS FOR SAMPLING ONE STAGE OF REGISTER.
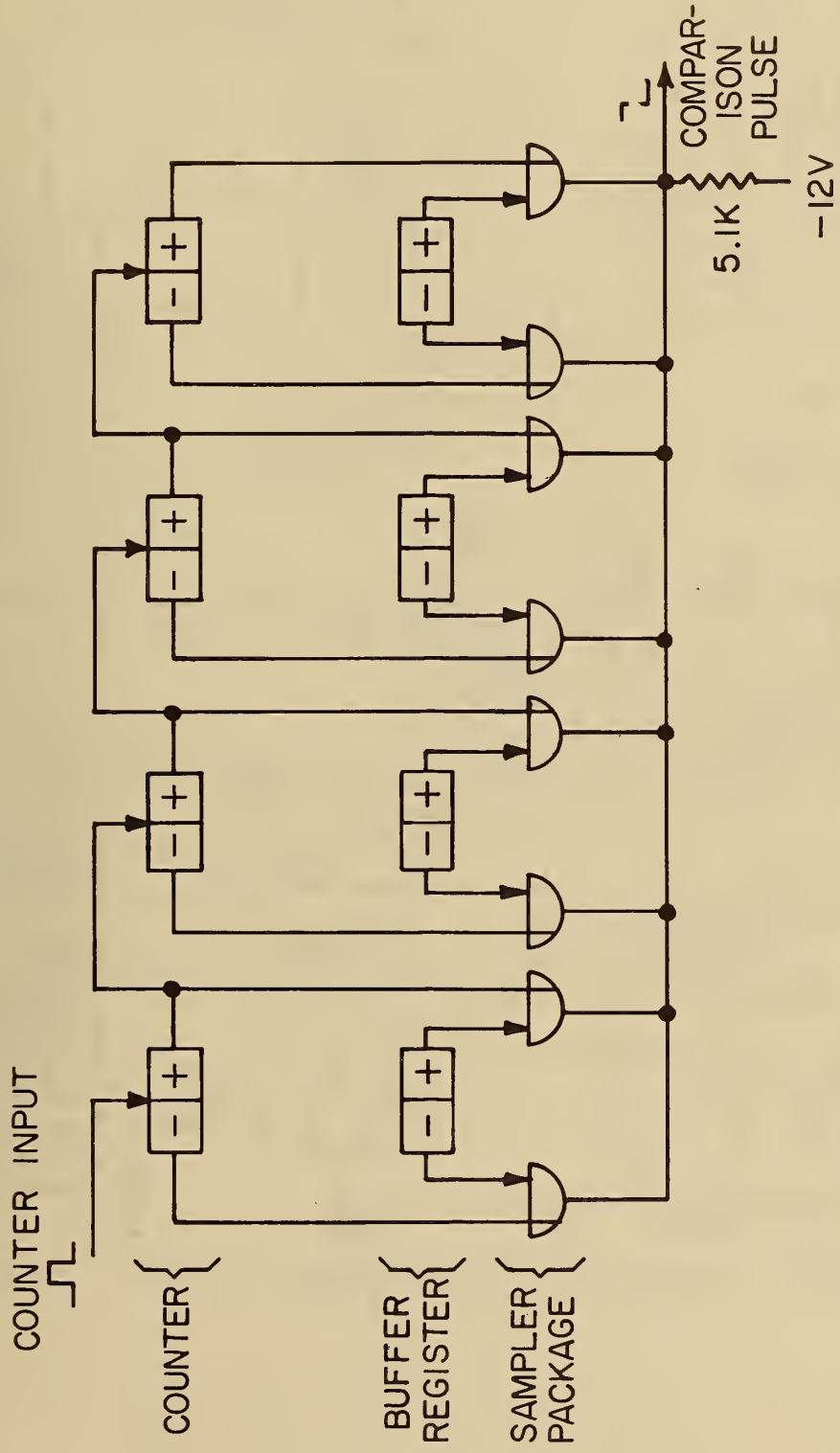
FIGURE 14. SAMPLER PACKAGE USED AS ABSOLUTE COMPARATOR BETWEEN A SERIAL COUNTER AND A BUFFER REGISTER.
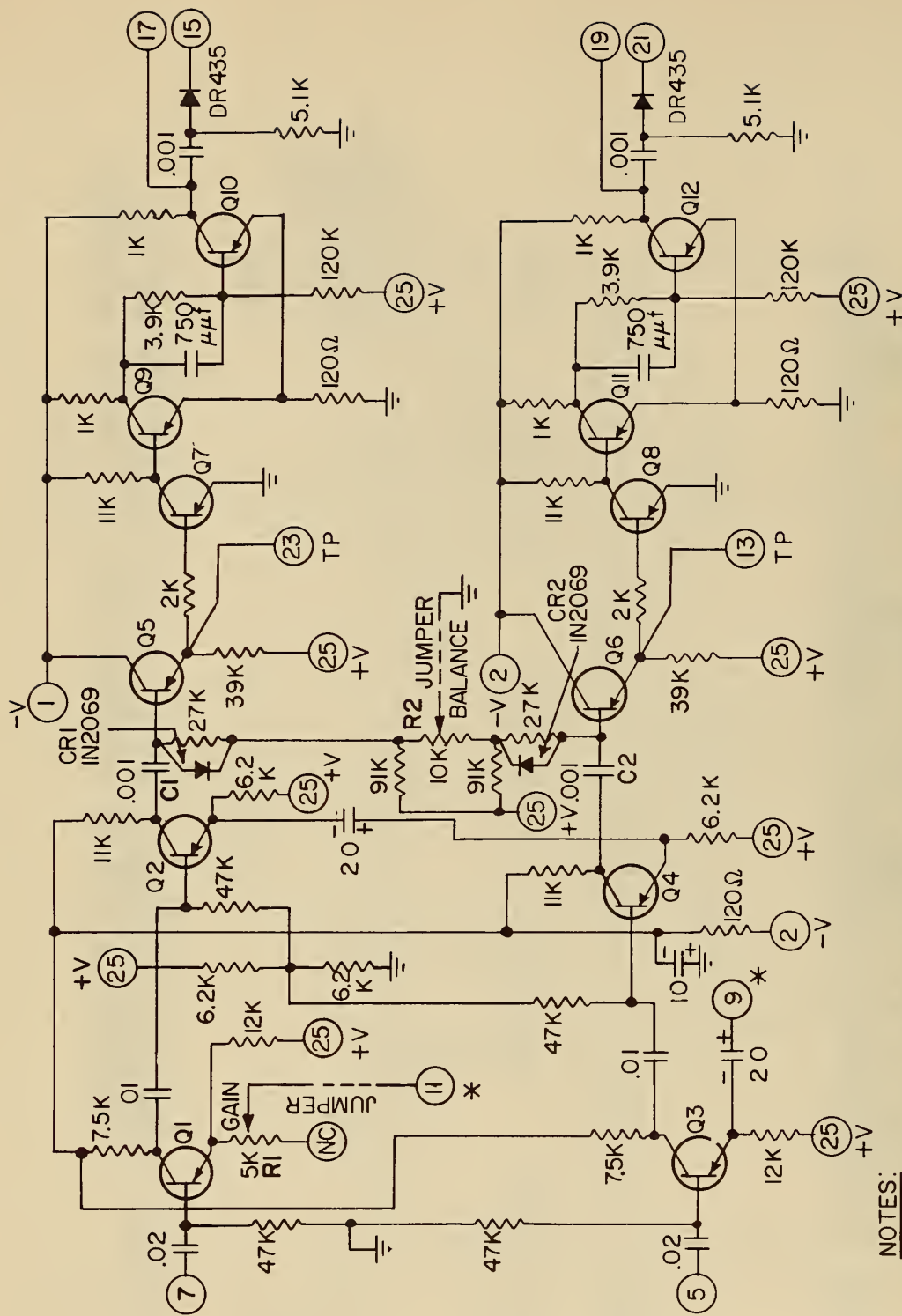
NOTES:

* * EXTERNAL GAIN CONTROL MAY BE INSERTED HERE, OTHERWISE JUMPER 9-11.
2. CR1 & CR2 USED WITH RETURN - TO BIAS.
3. ALL TRANSISTORS 2N414.
4. ALL RESISTORS 1/2 W.
5. -V = -12 VOLTS.
6. +V = +12 VOLTS.
7 GND. = PIN 22.

FIGURE 15. READ PACKAGE, SERIES 2E
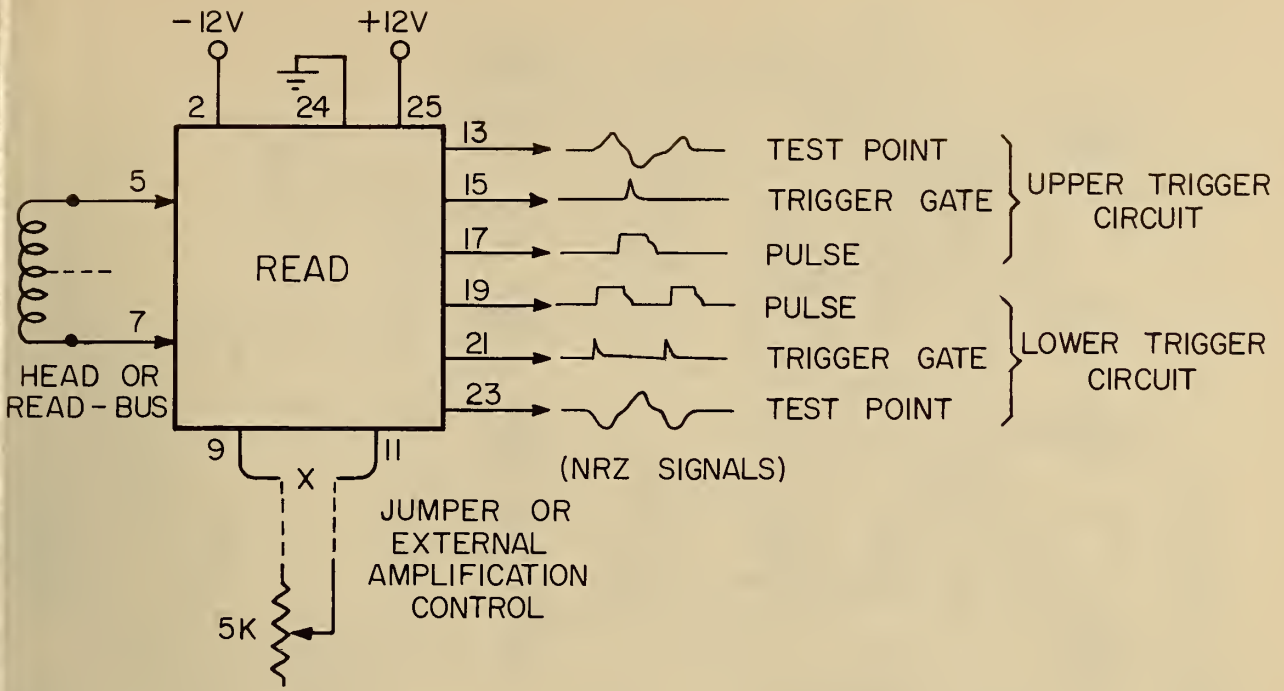
FIGURE 16. READ PACKAGE, SERIES 2E CONNECTIONS AND
OUTPUT WAVEFORMS.
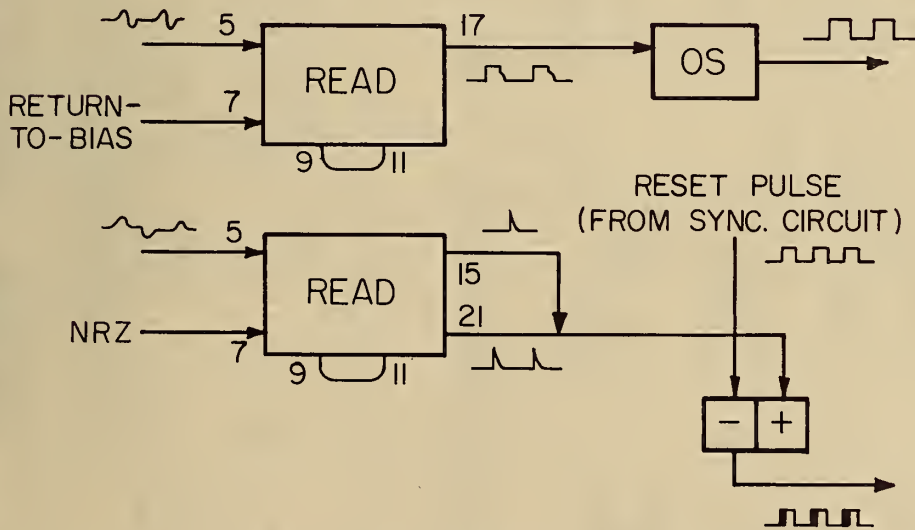
FIGURE 17. TYPICAL APPLICATIONS OF READ PACKAGE, SERIES 2E
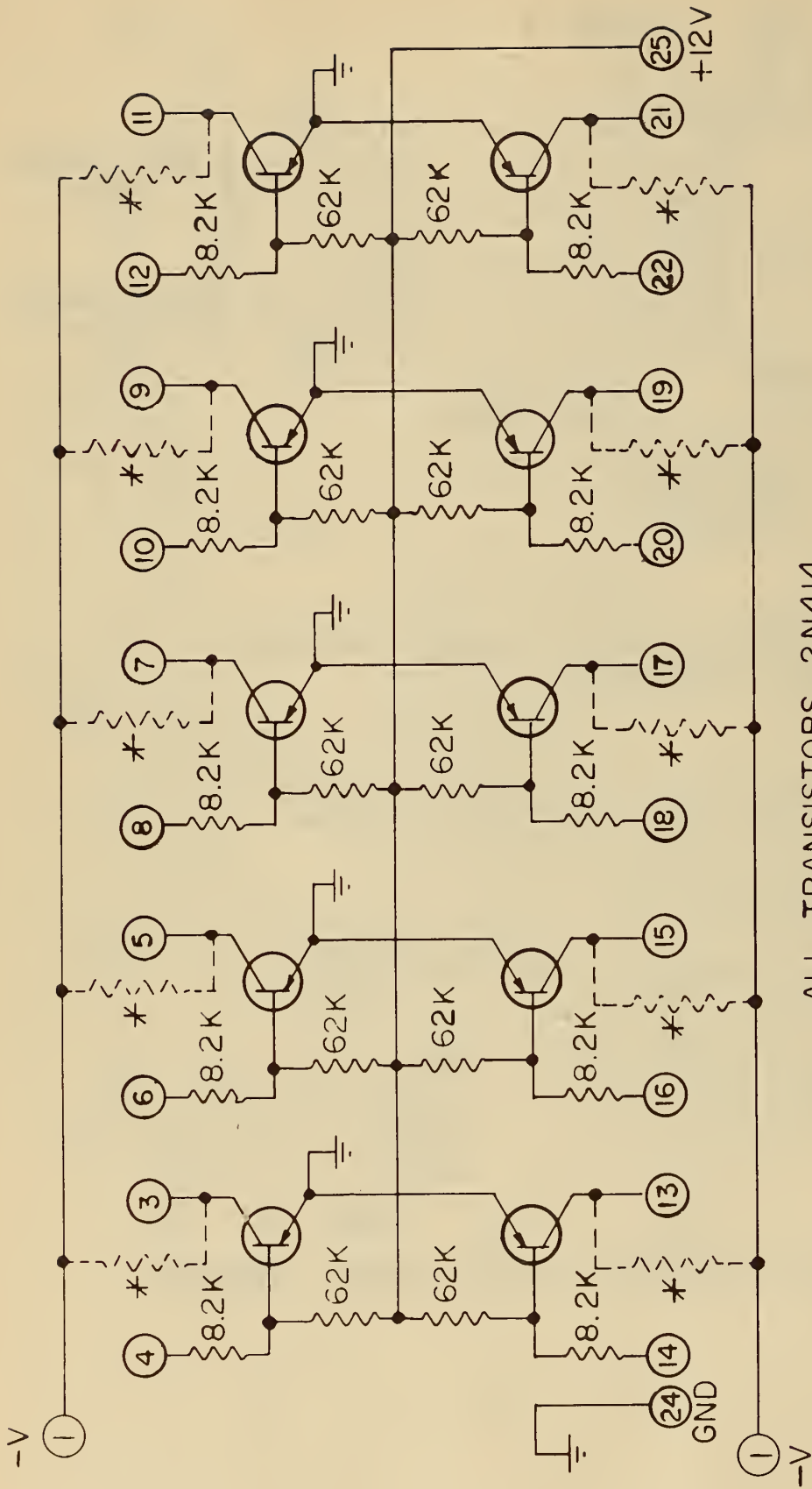
ALL TRANSISTORS 2N414.
8.2K RESISTORS 1/2 WATT.
62K RESISTORS 1/4 WATT.

* THESE RESISTORS REQUIRED ON
CIRCUITS USED AS AMPLIFIERS
(USUALLY 620 Ω).

FIGURE 18.   INDICATOR/AMPLIFIER,   SERIES 2
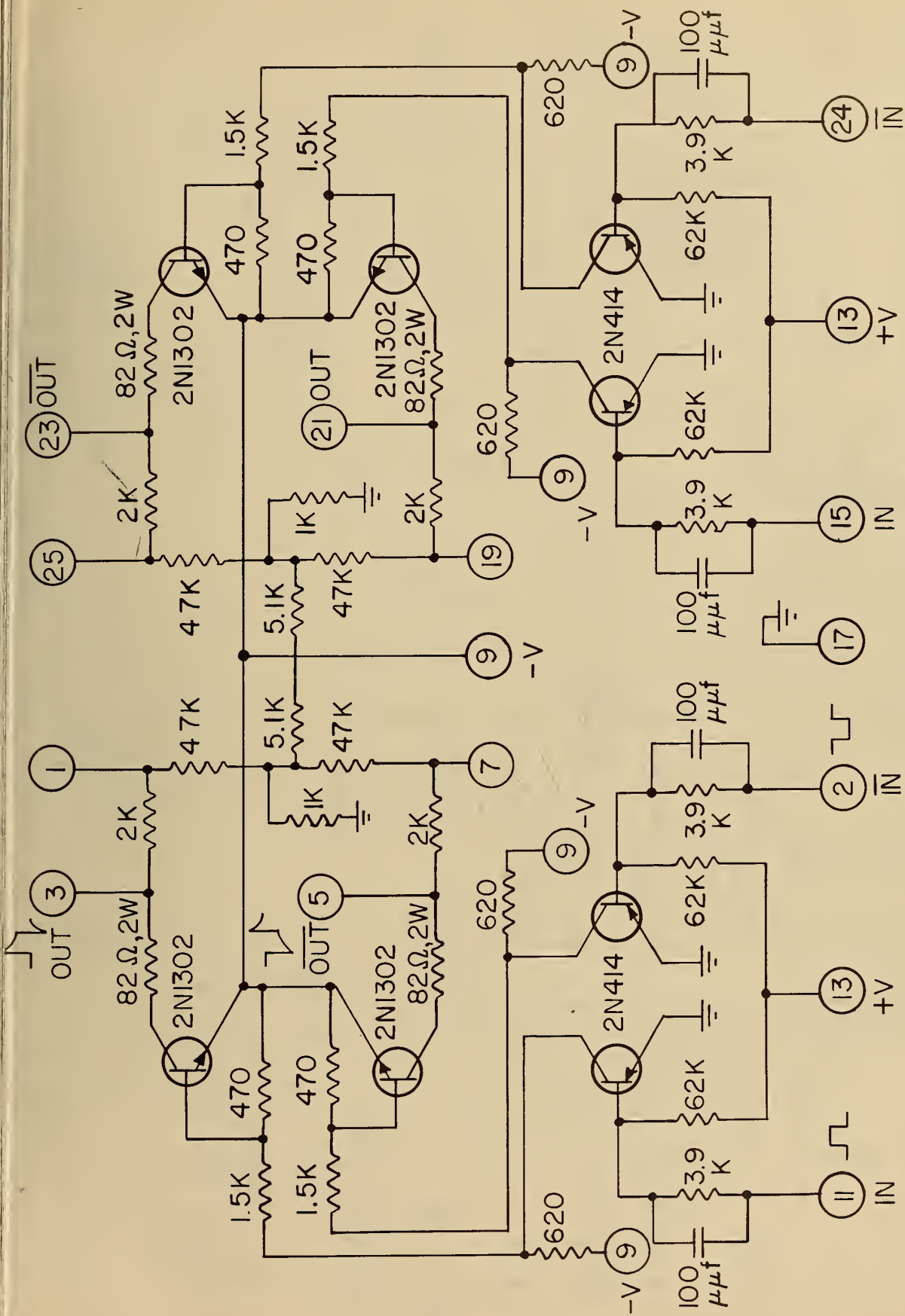
ALL RESISTORS 1/2 WATT EXCEPT
WHERE SPECIFIED.

FIGURE 19. DUAL WRITE PACKAGE SERIES 2A

FIGURE 20. PULSE GENERATOR WITH FLIP–FLOP, SERIES 2
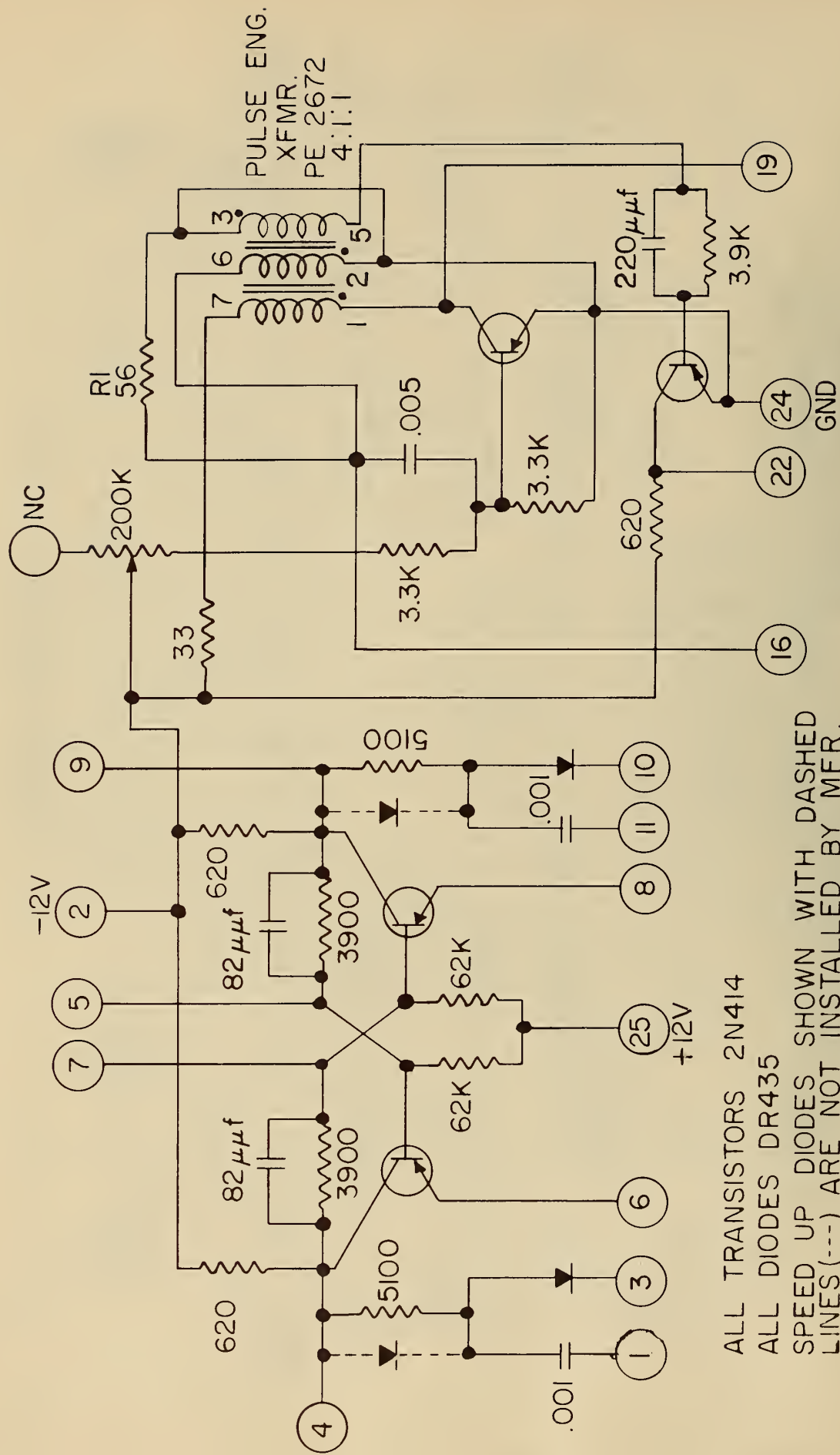
ALL TRANSISTORS 2N414
ALL DIODES DR435
SPEED UP DIODES SHOWN WITH DASHED
LINES(---) ARE NOT INSTALLED BY MFR.
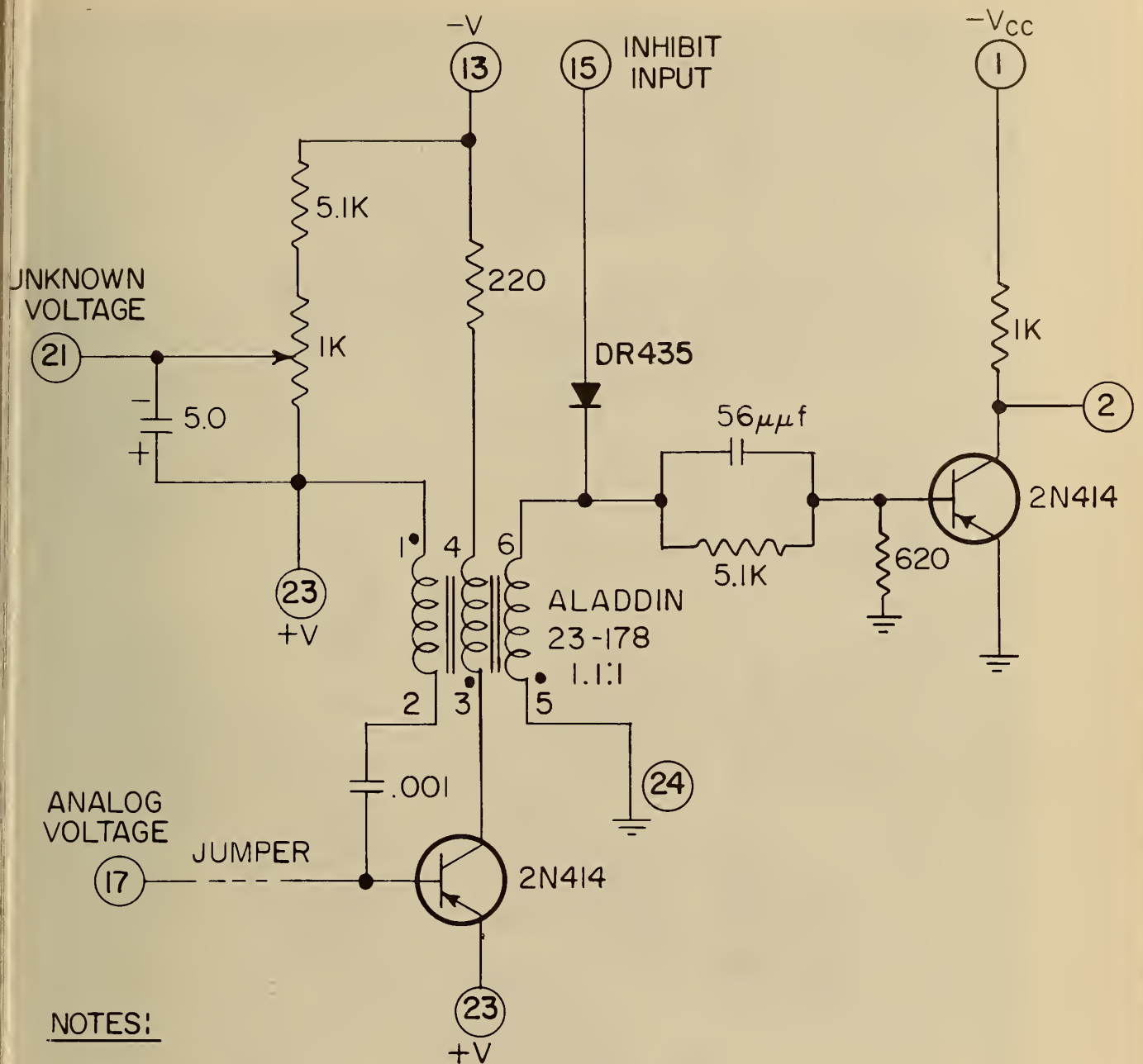
FIGURE 21. ANALOG VOLTAGE COMPARATOR, SERIES 2

NOTES:

1. $-V_{cc} = -12$ VOLTS.
2. +V AND −V ARE TERMINALS OF A FLOATING POWER SUPPLY.
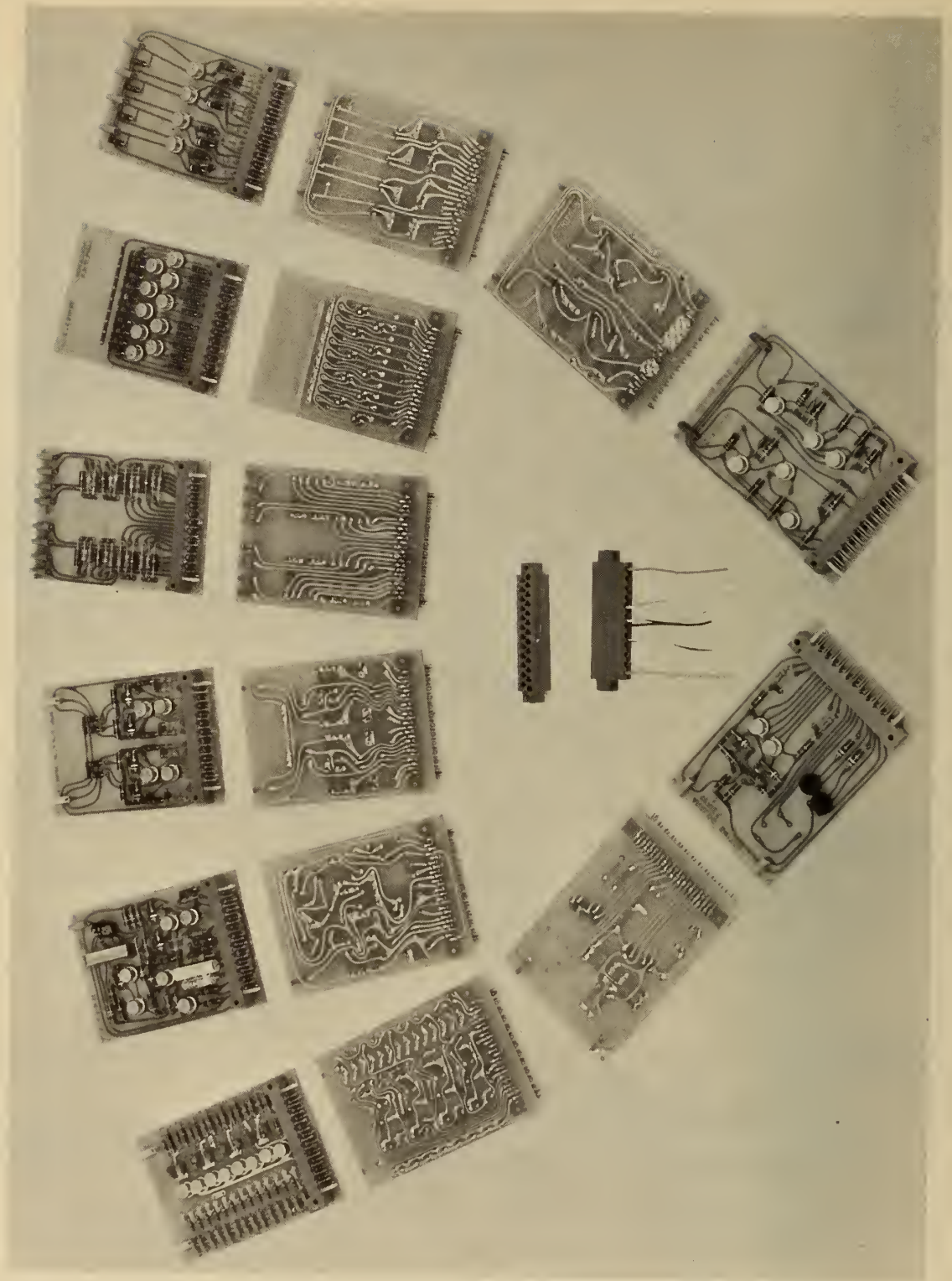
FIGURE 22. SERIES 3 PACKAGES
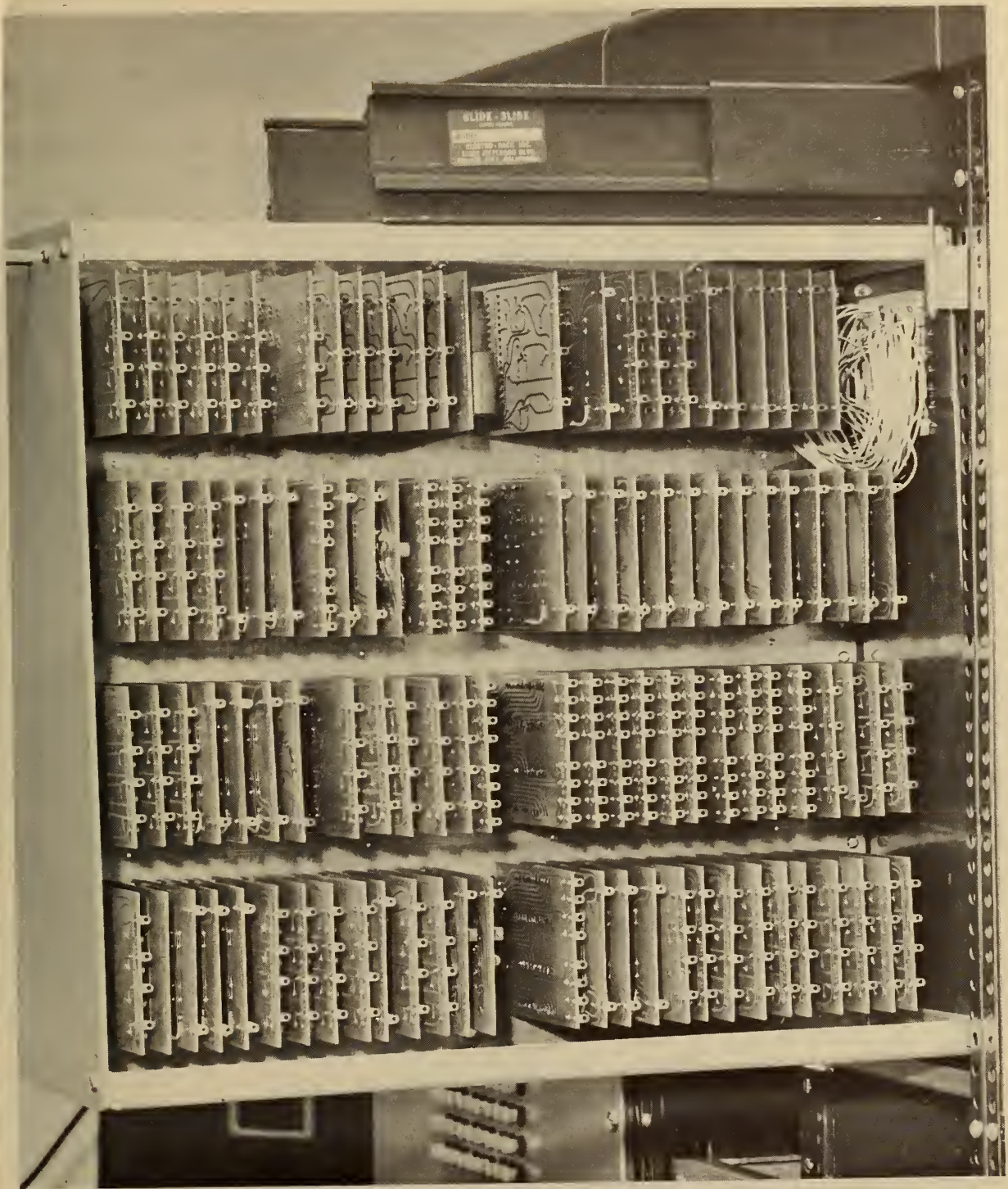
FIGURE 23. PACKAGE SIDE OF A TYPICAL DRAWER CHASSIS

FIGURE 24. WIRING SIDE OF A TYPICAL DRAWER CHASSIS
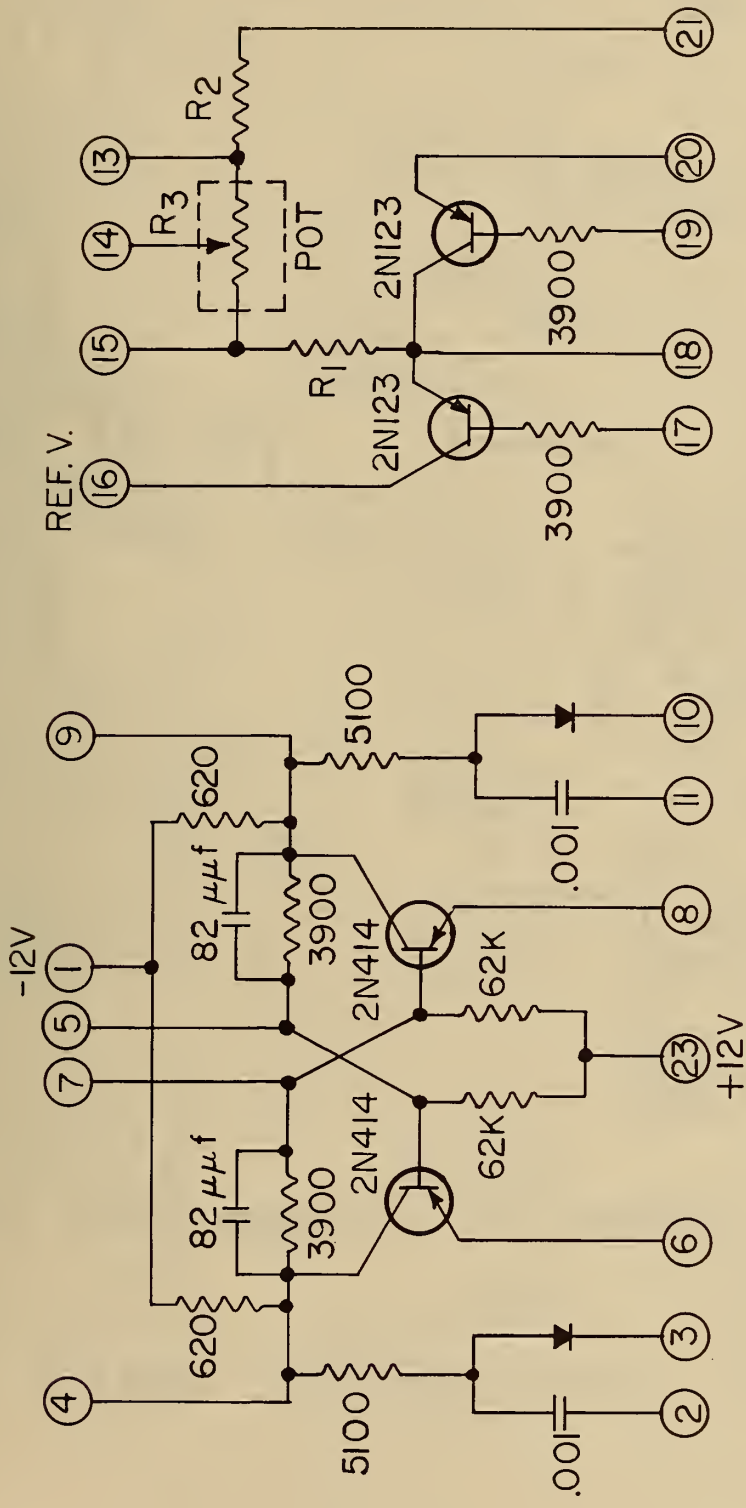
ALL DIODES DR435
ALL RESISTORS 1/2 WATT
VALUES OF R1, R2, R3 WILL DEPEND
ON FUNCTION OF THE PACKAGE

FIGURE 25. ANALOG SWITCH PACKAGE, SERIES 3
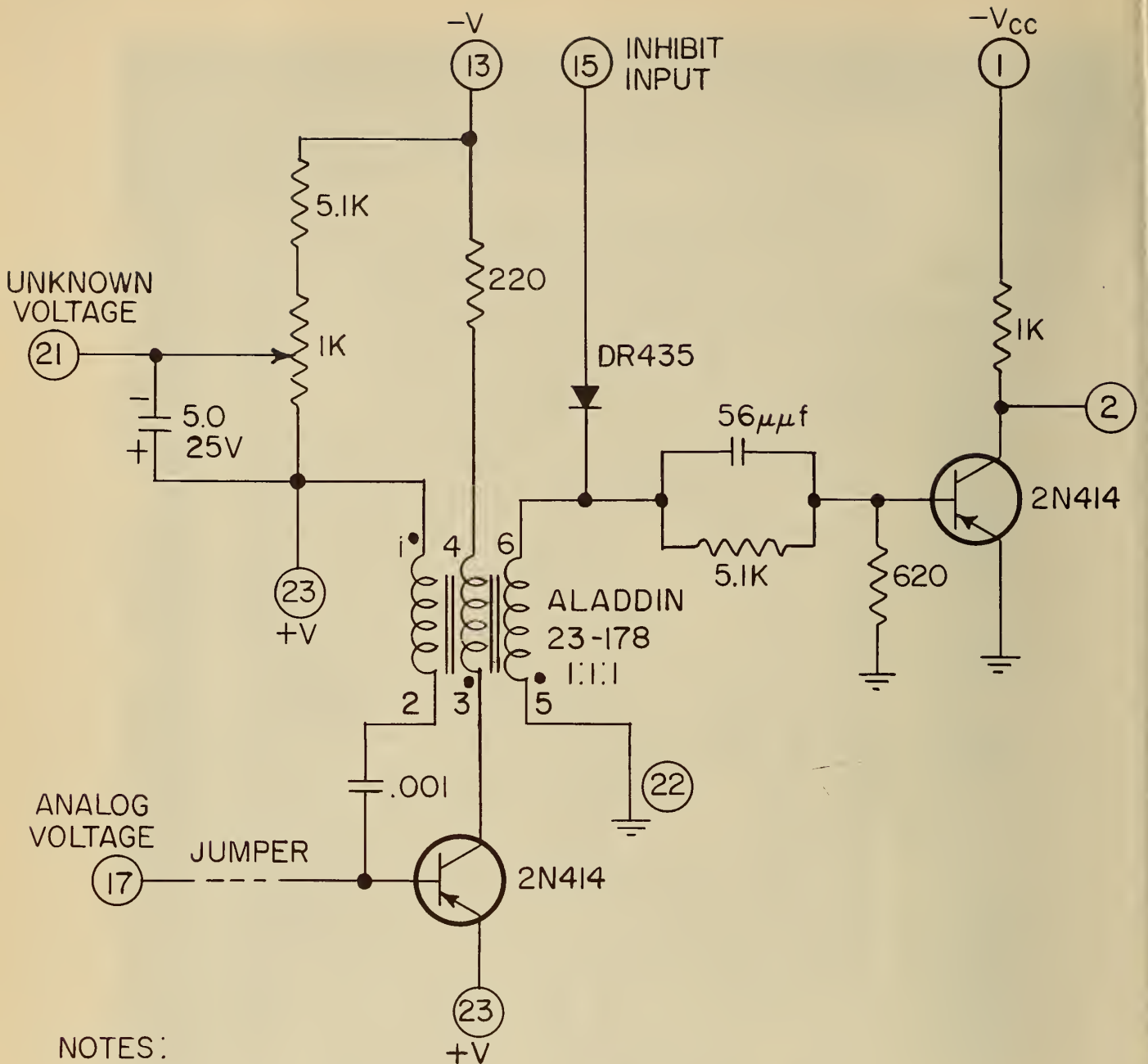
FIGURE 26. ANALOG VOLTAGE COMPARATOR, SERIES 3

NOTES:

1. $-V_{cc} = -12$ VOLTS.

2. $+V$ AND $-V$ ARE TERMINALS OF A FLOATING POWER SUPPLY.

FIGURE 27. DECIMAL DECODER SERIES 3
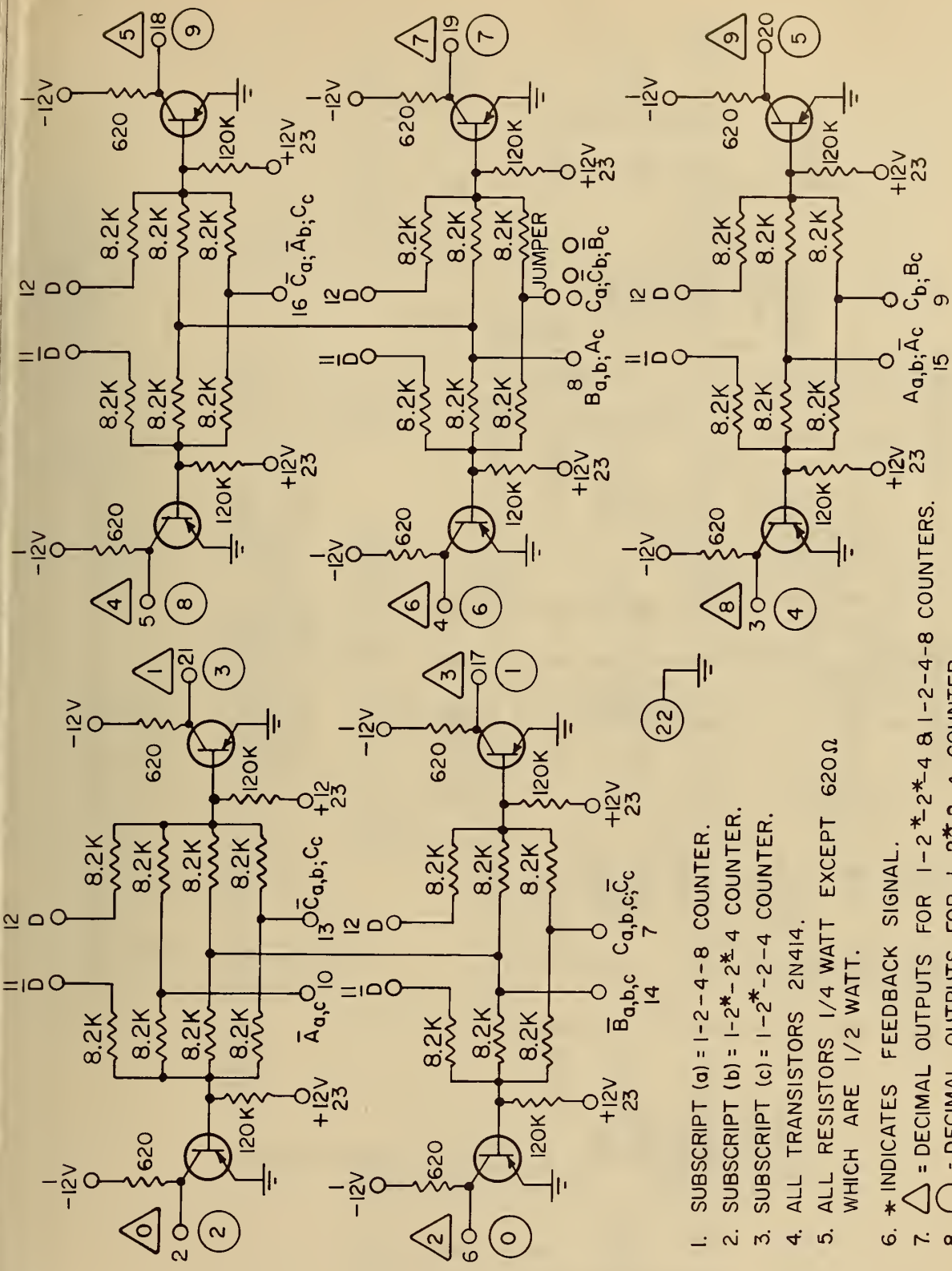
1. SUBSCRIPT (a) = 1-2-4-8 COUNTER.
2. SUBSCRIPT (b) = 1-2*-2*-4 COUNTER.
3. SUBSCRIPT (c) = 1-2*-2-4 COUNTER.
4. ALL TRANSISTORS 2N414.
5. ALL RESISTORS 1/4 WATT EXCEPT 620Ω WHICH ARE 1/2 WATT.
6. * INDICATES FEEDBACK SIGNAL.
7. △ = DECIMAL OUTPUTS FOR 1-2*-2*-4 & 1-2-4-8 COUNTERS.
8. ○ = DECIMAL OUTPUTS FOR 1-2*-2-4 COUNTER.
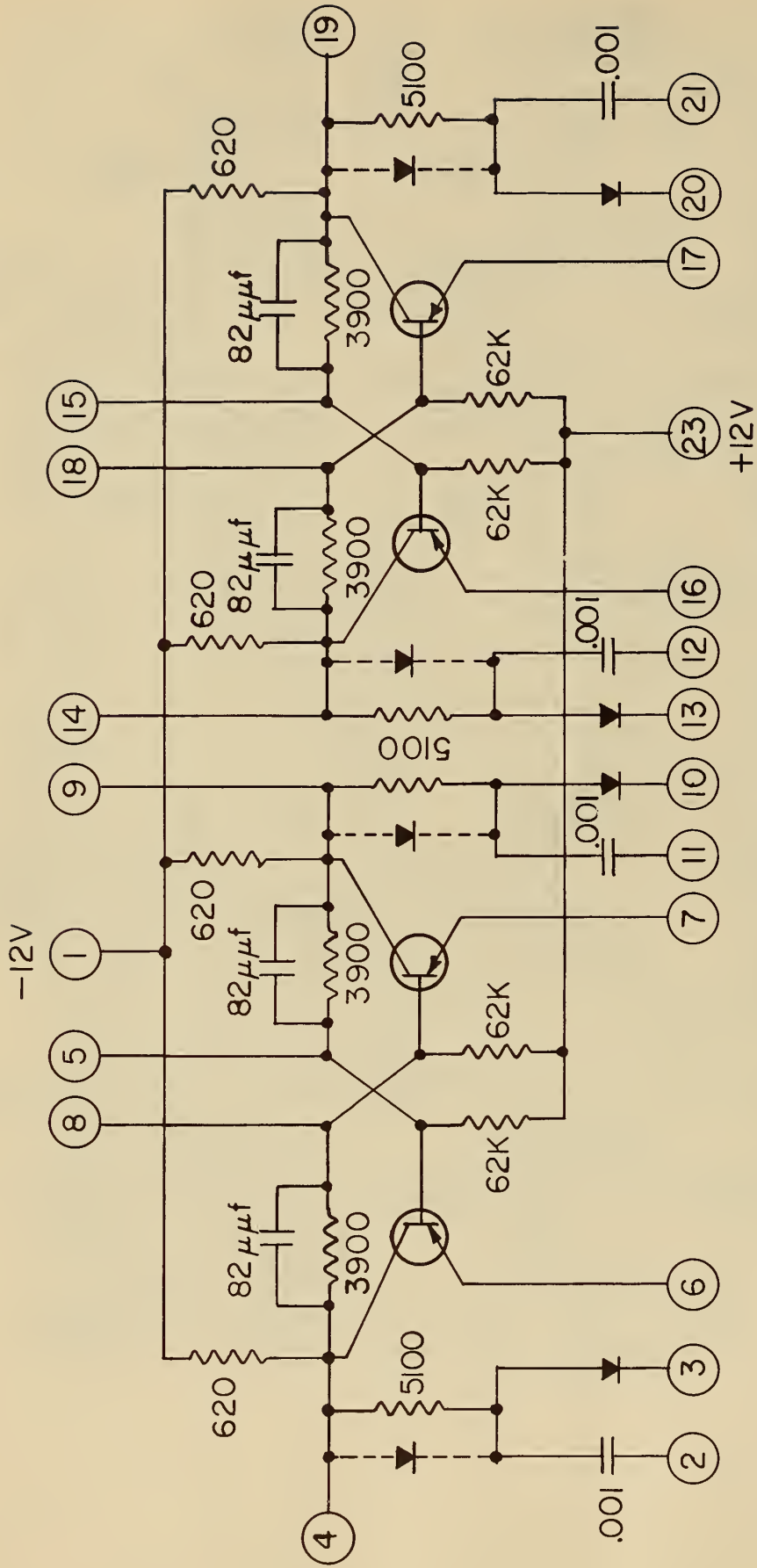
ALL TRANSISTORS 2N414
ALL DIODES DR 435
SPEED-UP DIODES SHOWN WITH DASHED LINES (---)

FIGURE 28. DUAL FLIP-FLOP, SERIES 3
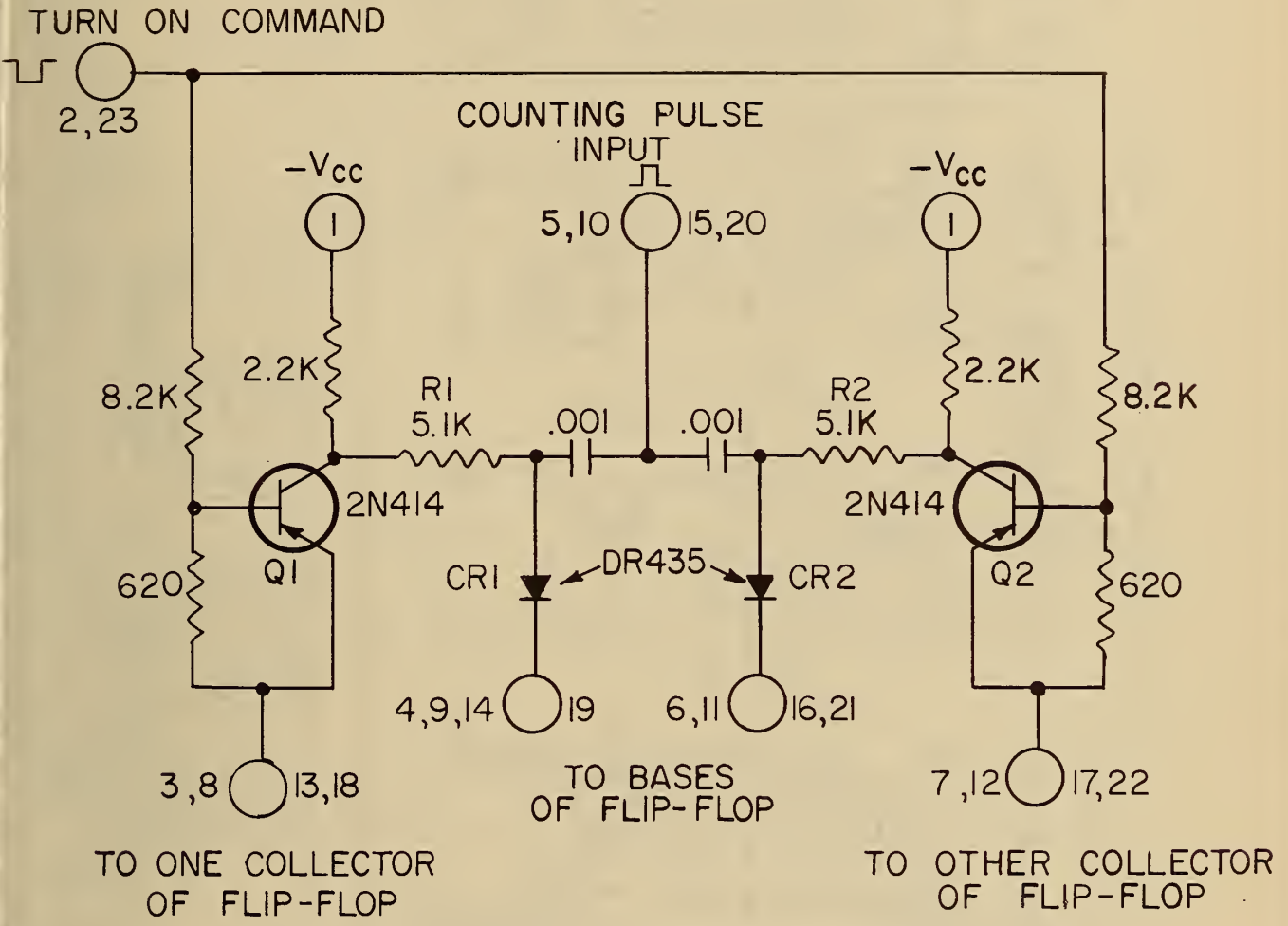
FIGURE 29. GATED "T" INPUT, SERIES 3
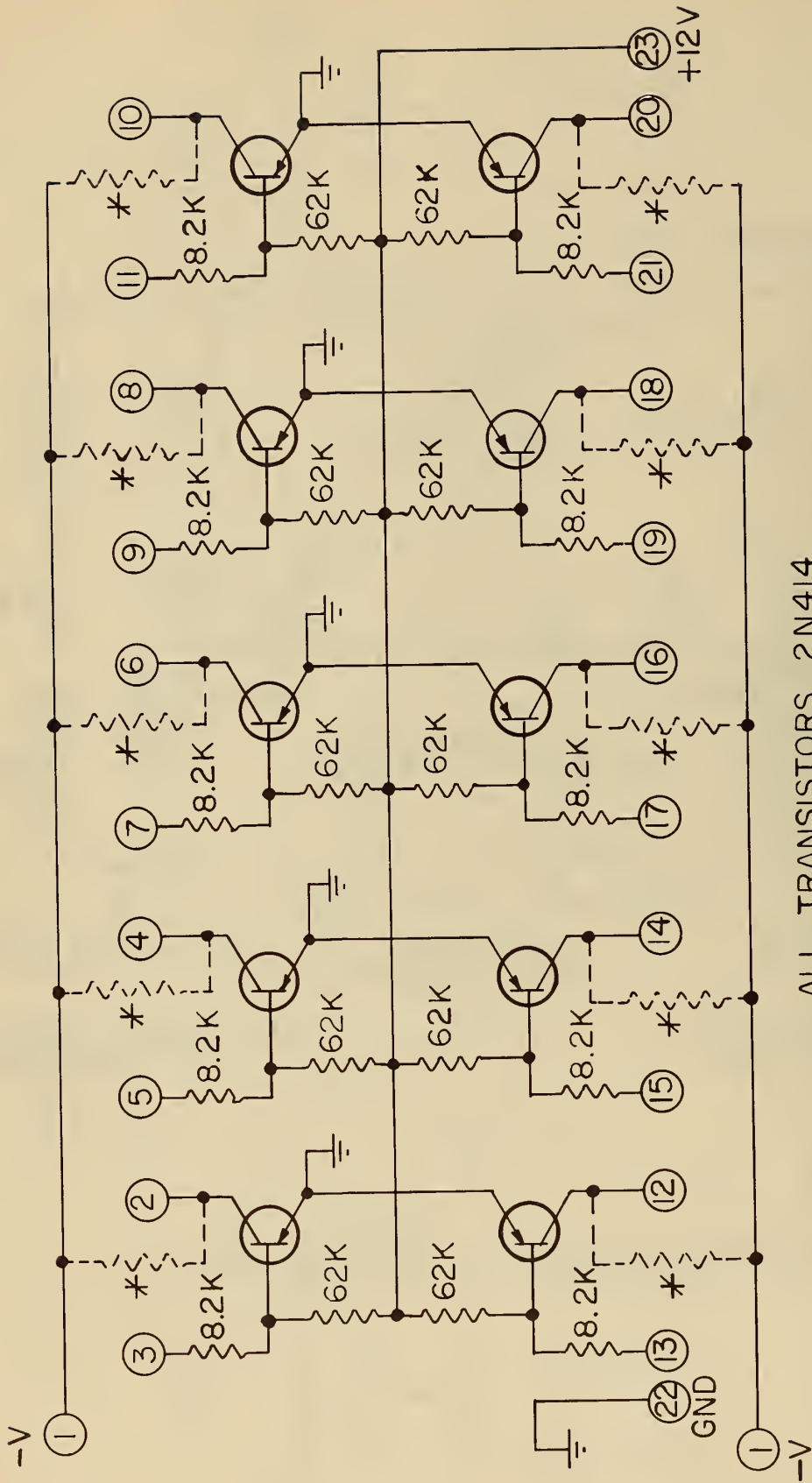
ALL TRANSISTORS 2N414.
8.2K RESISTORS 1/2 WATT.
62K RESISTORS 1/4 WATT.
✳ THESE RESISTORS REQUIRED ON
CIRCUITS USED AS AMPLIFIERS
(USUALLY 620 Ω).

FIGURE 30. INDICATOR / AMPLIFIER , SERIES 3

FIGURE 31. OCTAL - HEXADECIMAL DECODER, SERIES 3
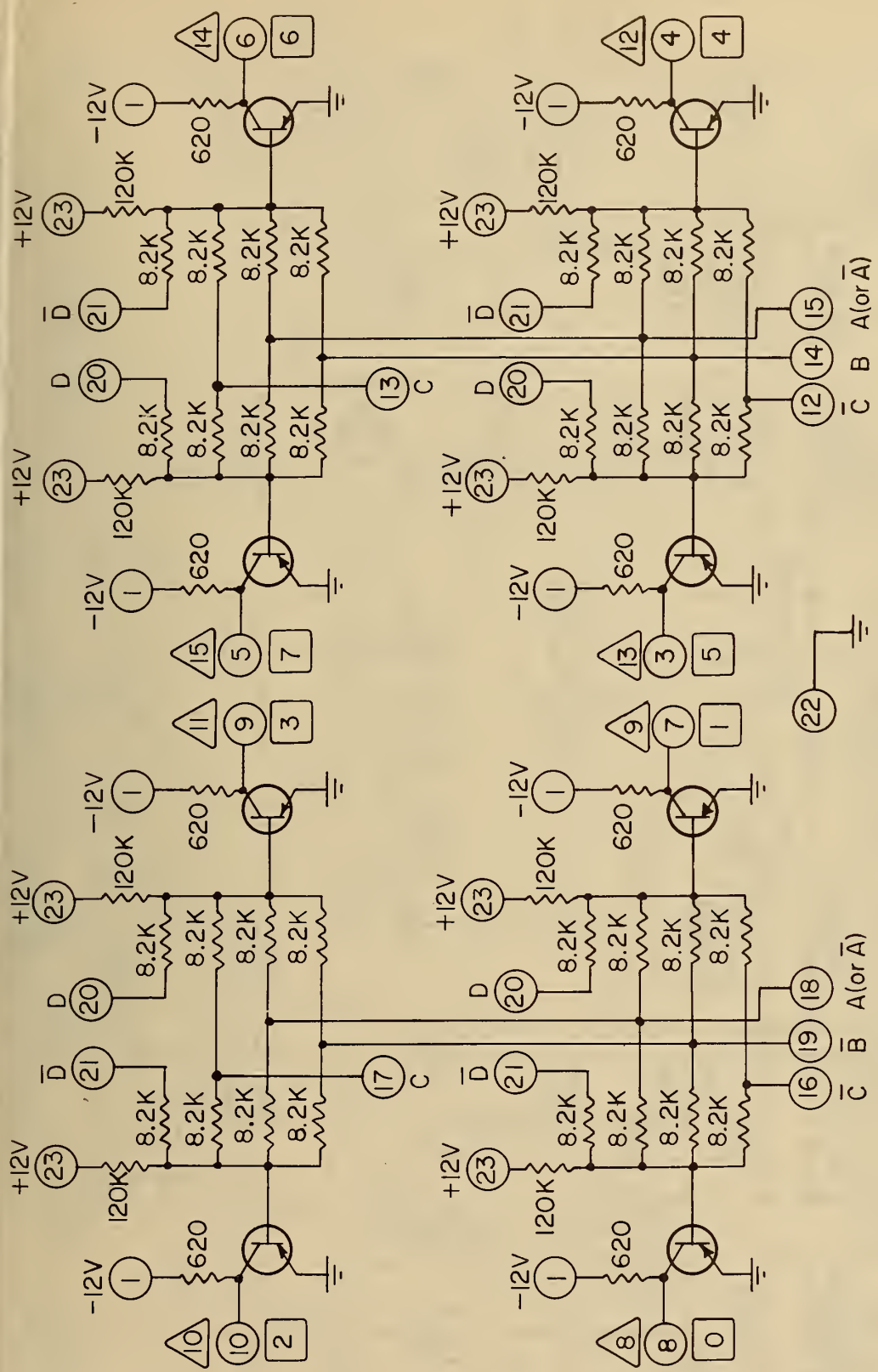
1. ☐ OUTPUT FIRST PACKAGE.
2. △ OUTPUT SECOND PACKAGE.

3. ALL TRANSISTORS 2N414.
4. 620Ω RESISTORS 1/2 WATT, ALL OTHER 1/4 WATT.

FIGURE 32. ONE SHOT PACKAGE, SERIES 3
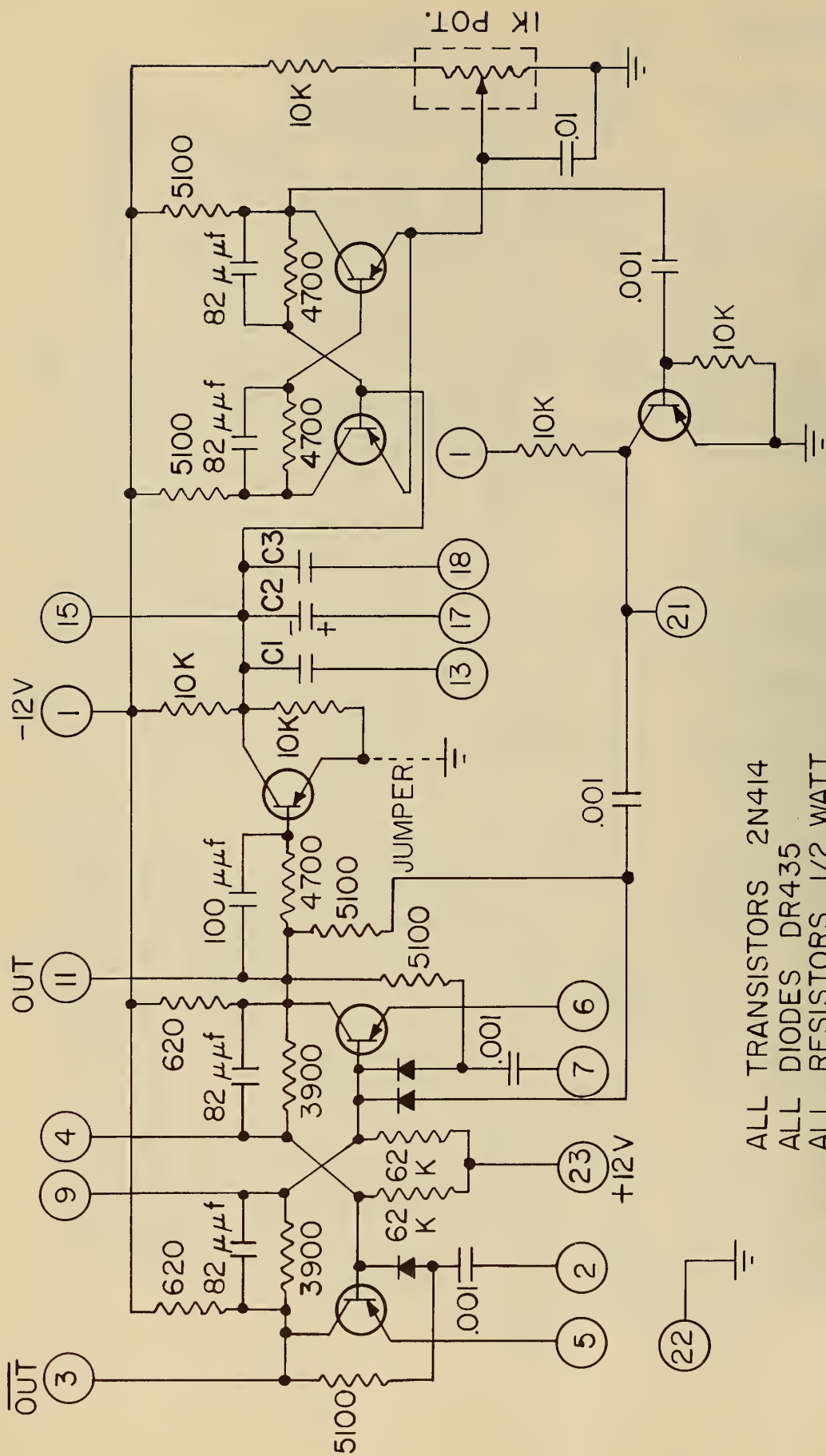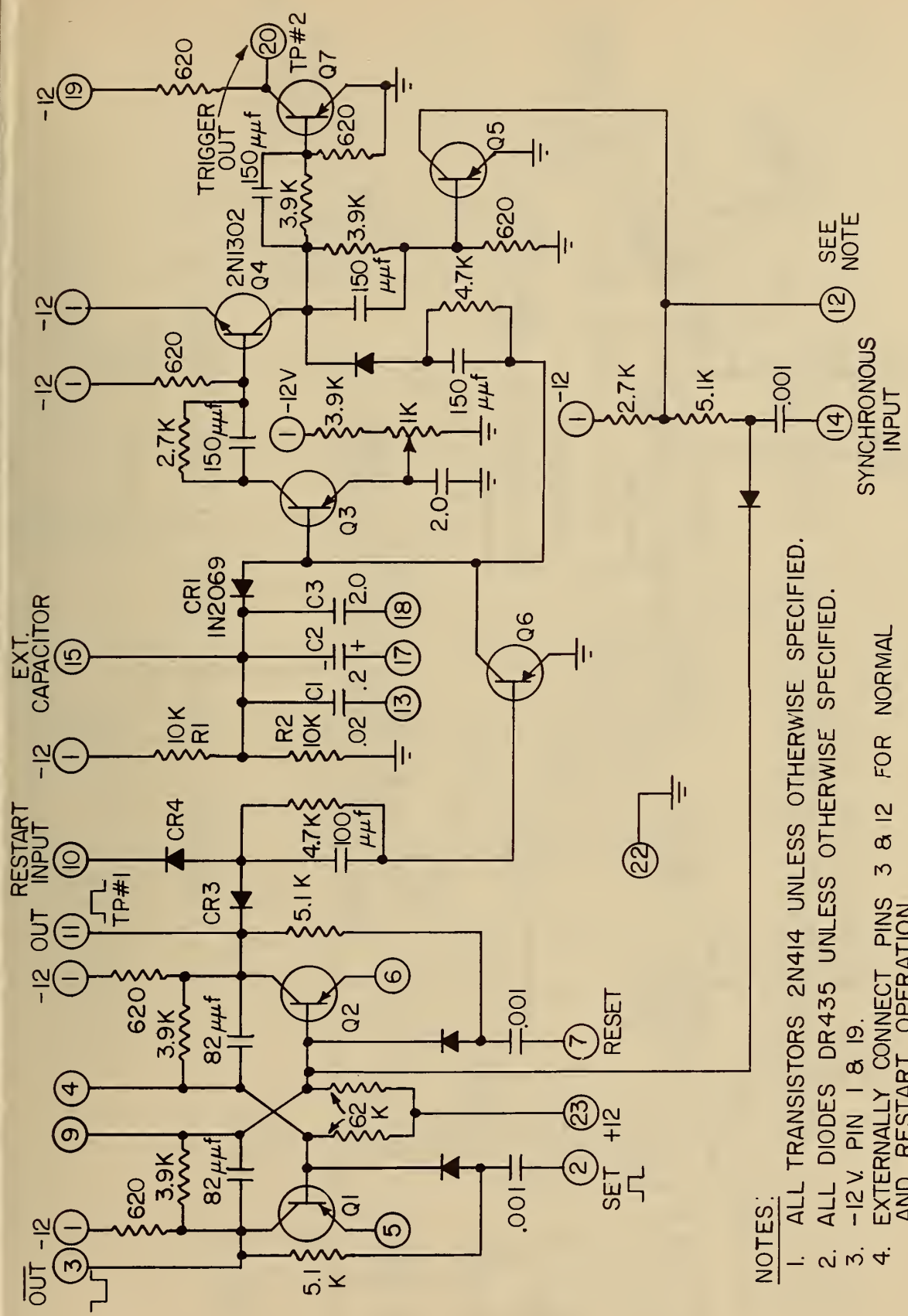
ALL TRANSISTORS 2N414
ALL DIODES DR435
ALL RESISTORS 1/2 WATT
VALUES OF C1, C2, AND C3 WILL DEPEND ON
PULSE DURATION DESIRED. VALUES USED IN
PRESENT MODEL ARE .02, .2, AND 2.0 μf.

FIGURE 33. ONE-SHOT, SERIES 3A

NOTES:
1. ALL TRANSISTORS 2N414 UNLESS OTHERWISE SPECIFIED.
2. ALL DIODES DR435 UNLESS OTHERWISE SPECIFIED.
3. -12V PIN 1 & 19.
4. EXTERNALLY CONNECT PINS 3 & 12 FOR NORMAL AND RESTART OPERATION.
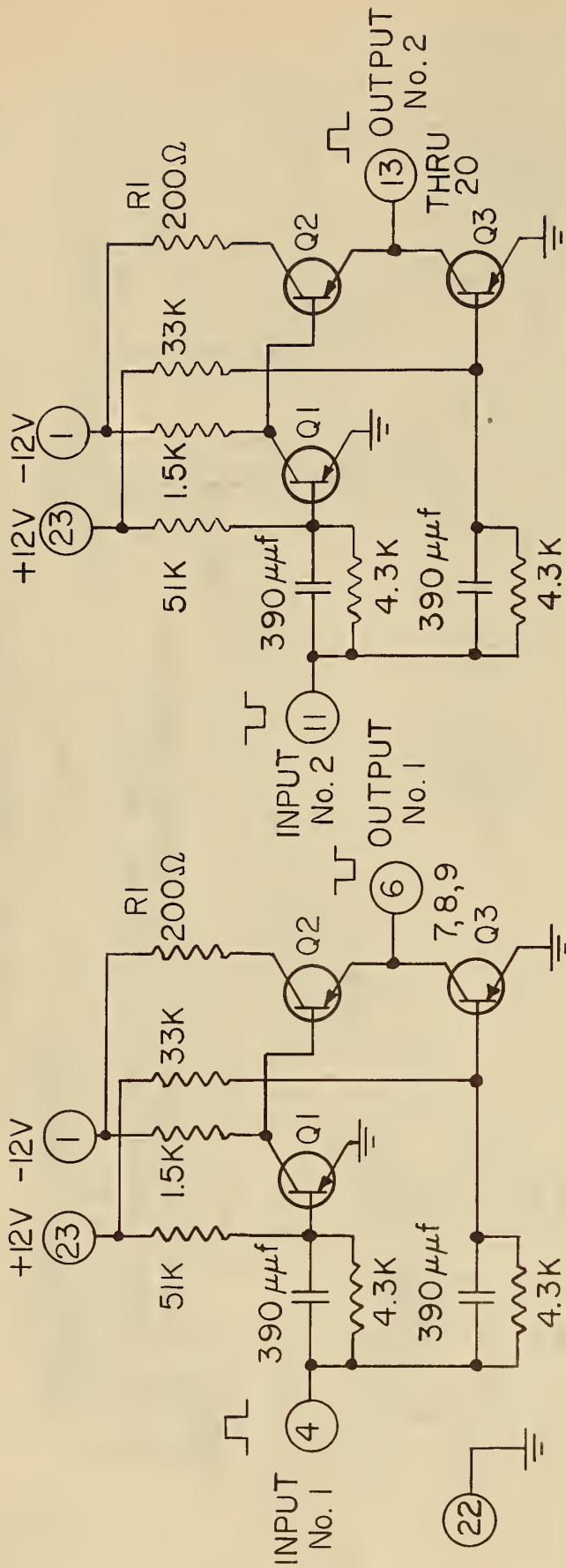
ALL TRANSISTORS 2N414.
ALL RESISTORS 1/2 WATT.

FIGURE 34. PULSE GATE DRIVER, SERIES 3
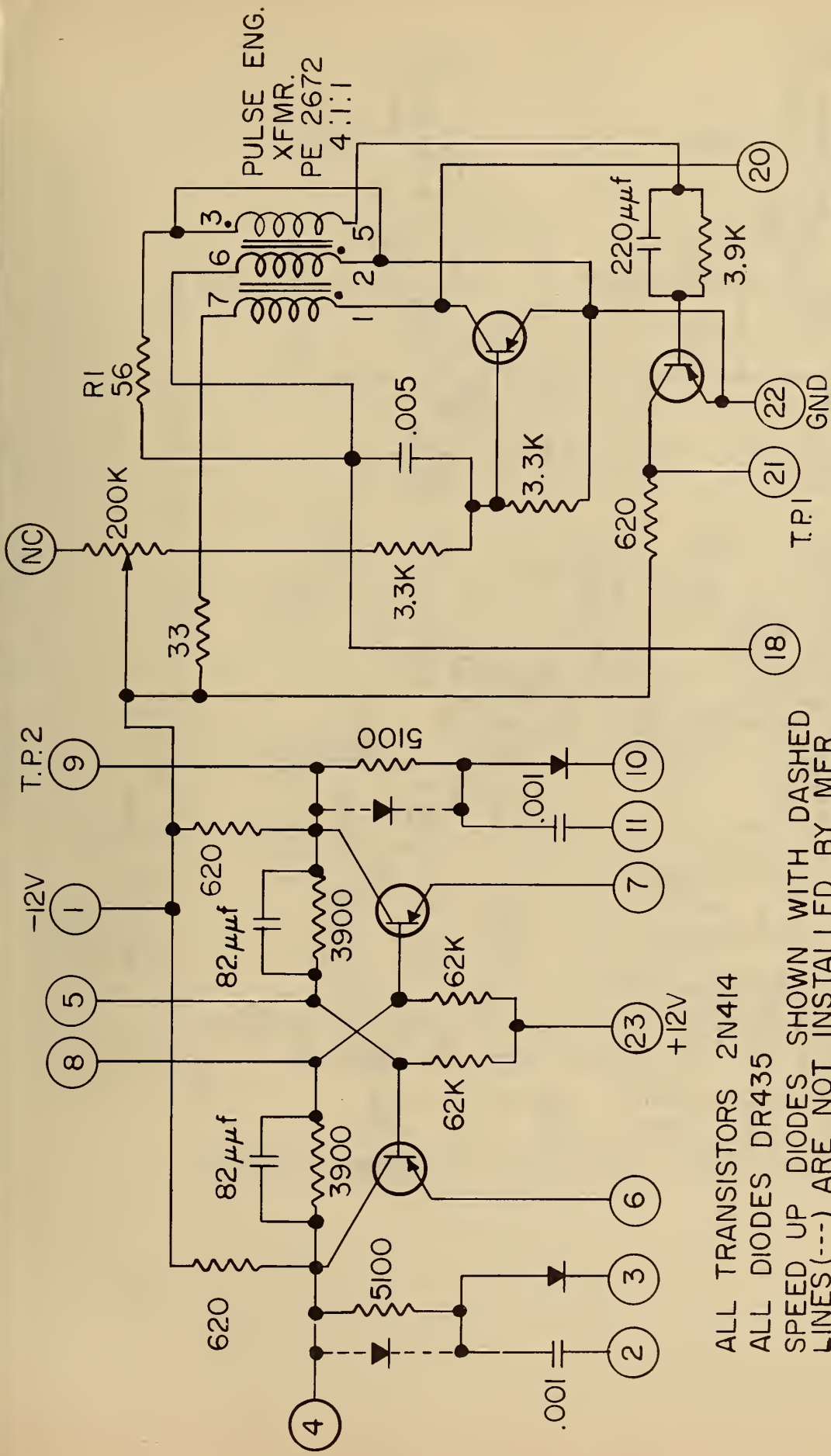
FIGURE 35. PULSE GENERATOR WITH FLIP-FLOP, SERIES 3
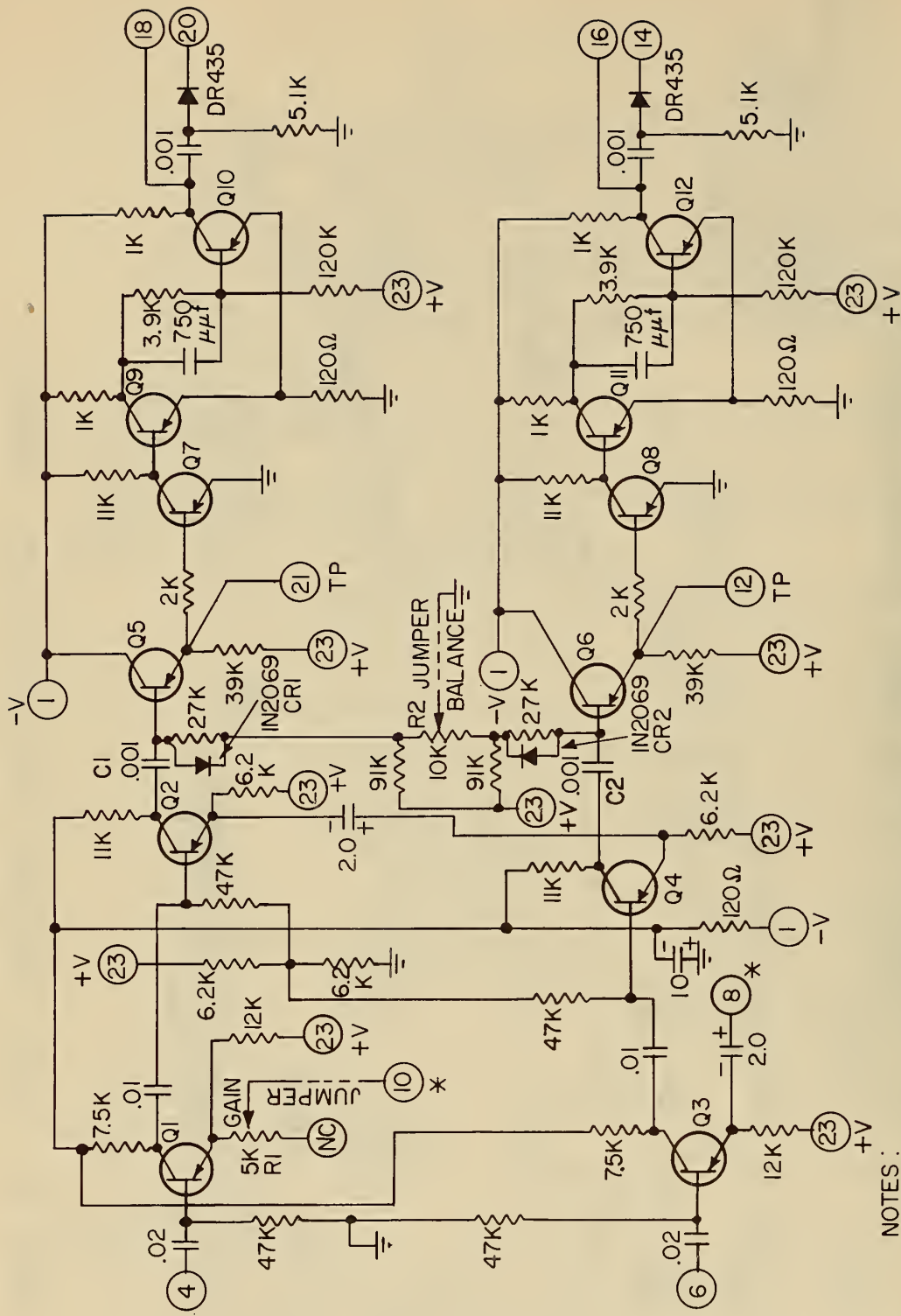
NOTES:
1. * EXTERNAL GAIN CONTROL MAY BE INSERTED HERE, OTHERWISE JUMPER 8-10.
2. CR1 & CR2 USED WITH RETURN –TO BIAS.
3. ALL TRANSISTORS 2N414.
4. ALL RESISTORS 1/2 W.
5. –V = –12 VOLTS.
6. +V = +12 VOLTS.
7. GND. = PIN 22.

FIGURE 36. READ PACKAGE, SERIES 3

2N4I4

620   HB-2

8.2K

PIN NOS.	PIN NOS.	PIN NOS.
I	2	3
4	5	6
7	8	9
IO	II	12
I4	I5	I6
I7	I8	I9
20	2I	22
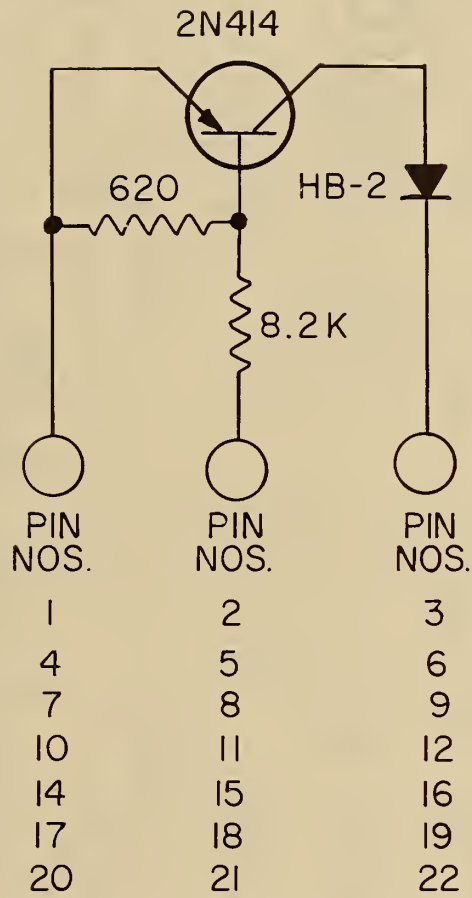
7 CIRCUITS PER PACKAGE

FIGURE 37. SAMPLER PACKAGE, SERIES 3
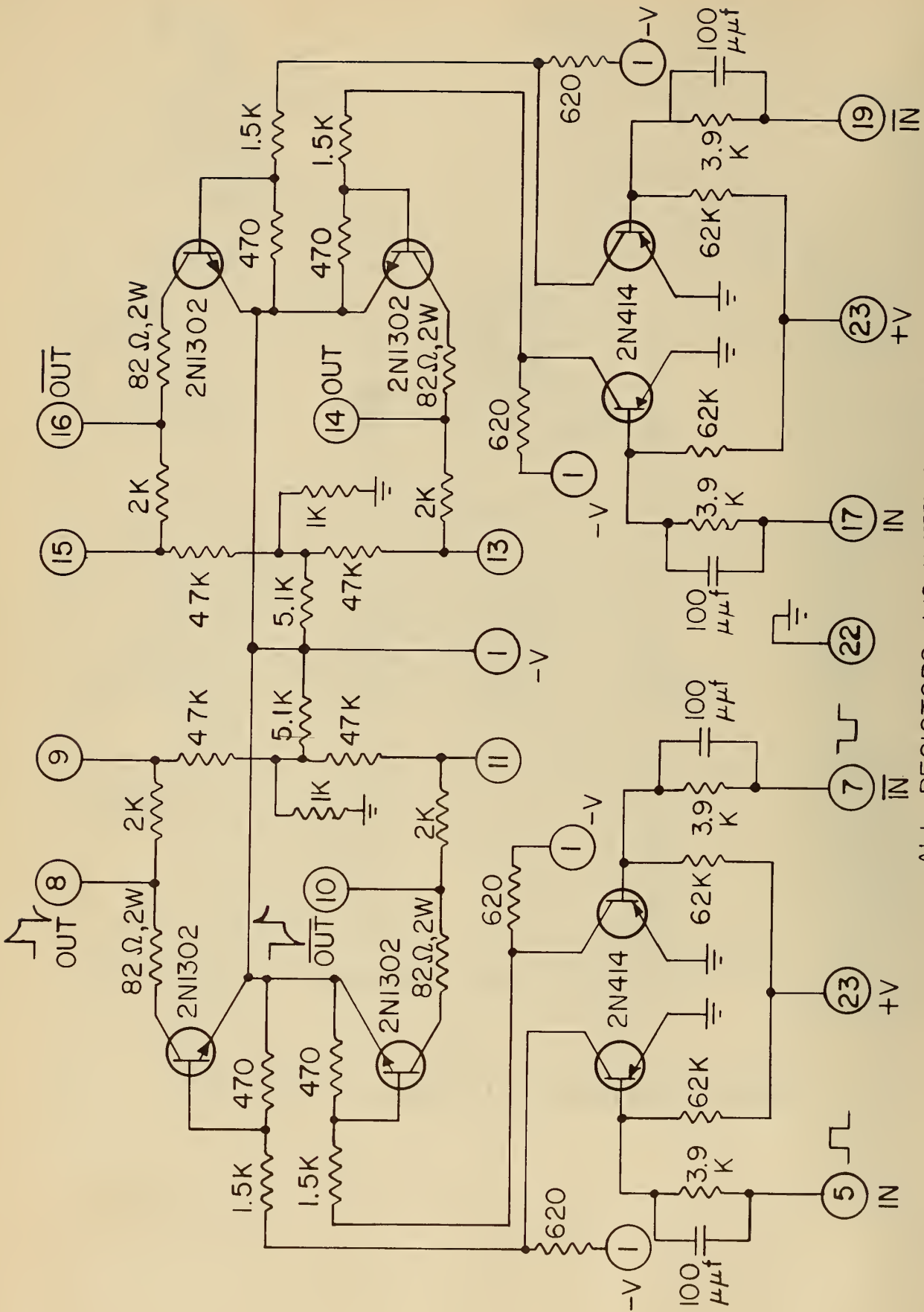
ALL RESISTORS 1/2 WATT EXCEPT
WHERE SPECIFIED.

FIGURE 38. DUAL WRITE PACKAGE, SERIES 3
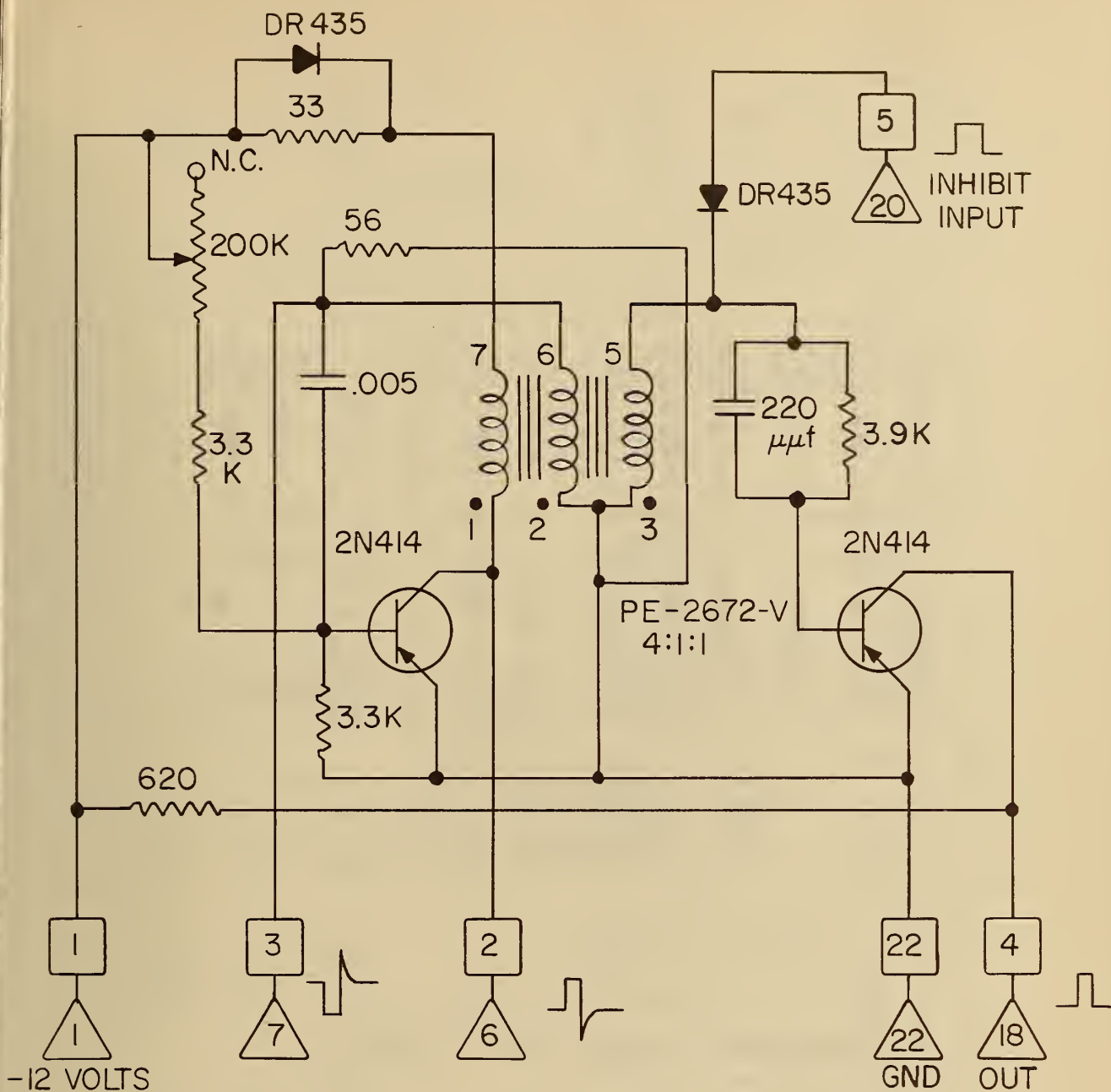
FIGURE 39. DUAL PULSE GENERATOR, SERIES 3
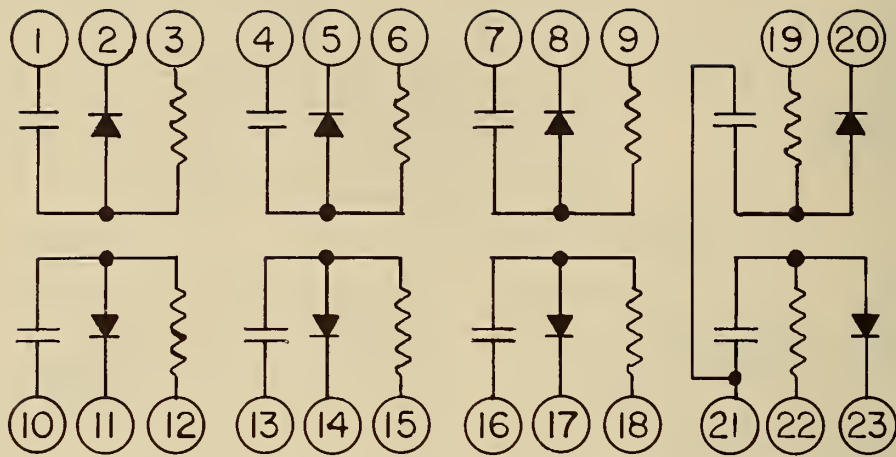
ALL DIODES DR 435
ALL CAPACITORS .001μf
ALL RESISTORS 5100 Ω

FIGURE 40. PULSE GATE, SERIES 3
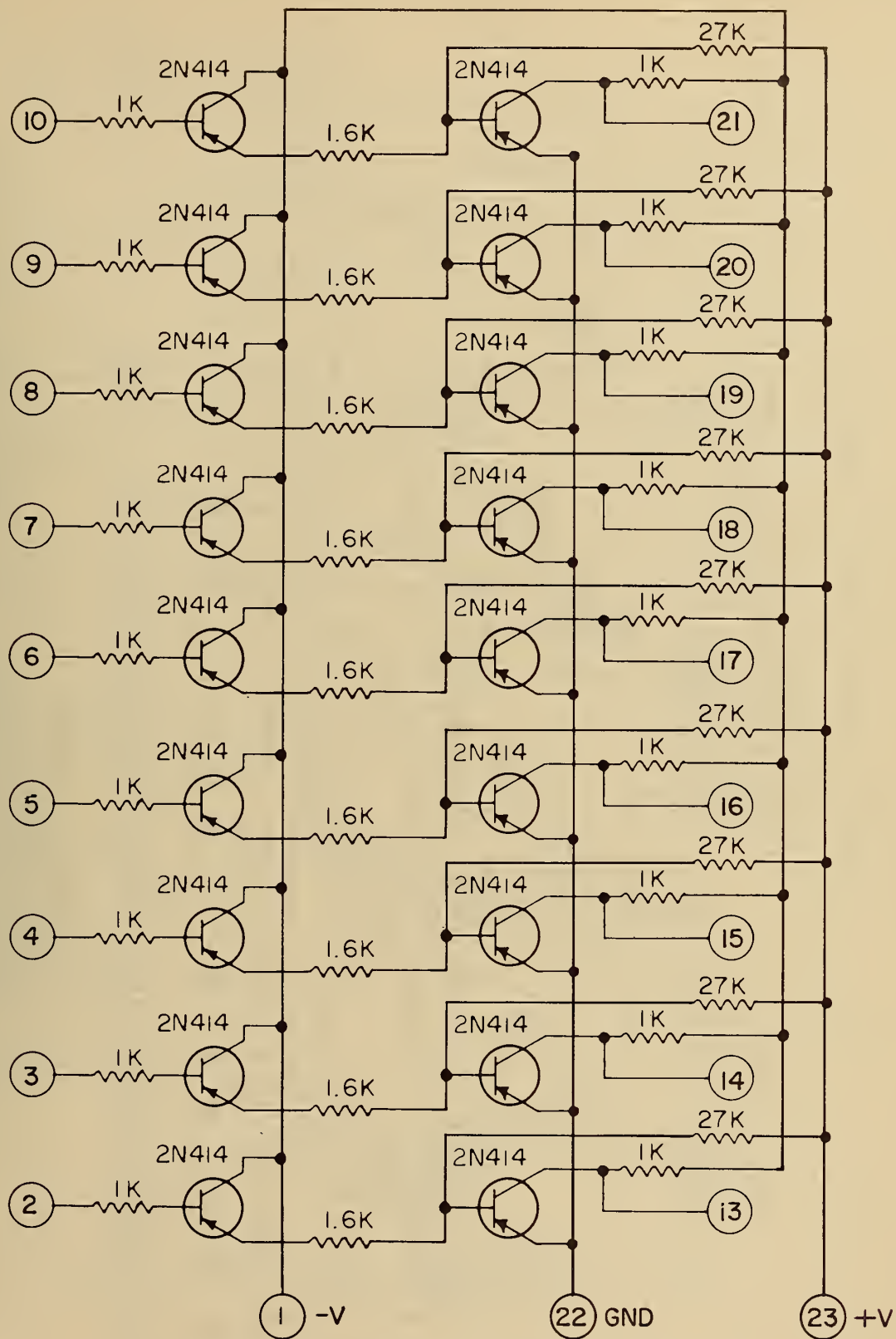
FIGURE 41. AMPLIFIER CIRCUIT, SERIES 3
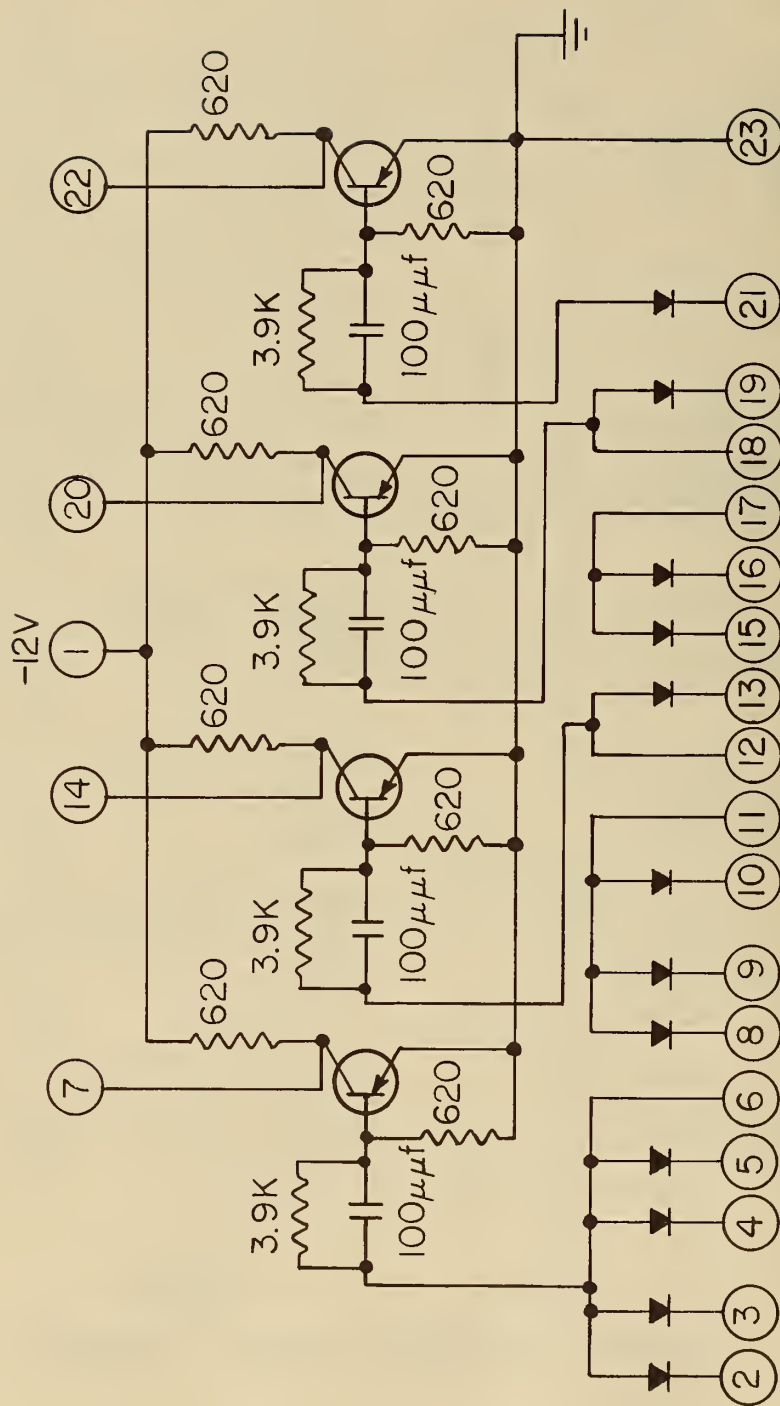
ALL TRANSISTORS 2N414
ALL DIODES DR435
ALL RESISTORS 1/2 WATT

FIGURE 42. AND/OR INVERTER, SERIES 3

FIGURE 43. B.C.D. COUNTER, SERIES 3

ALL DIODES DR435.
ALL TRANSISTORS 2N414.
ALL RESISTORS SHALL BE 1/4 WATT
EXCEPT THE 620 Ω, WHICH SHALL
BE 1/2 WATT.
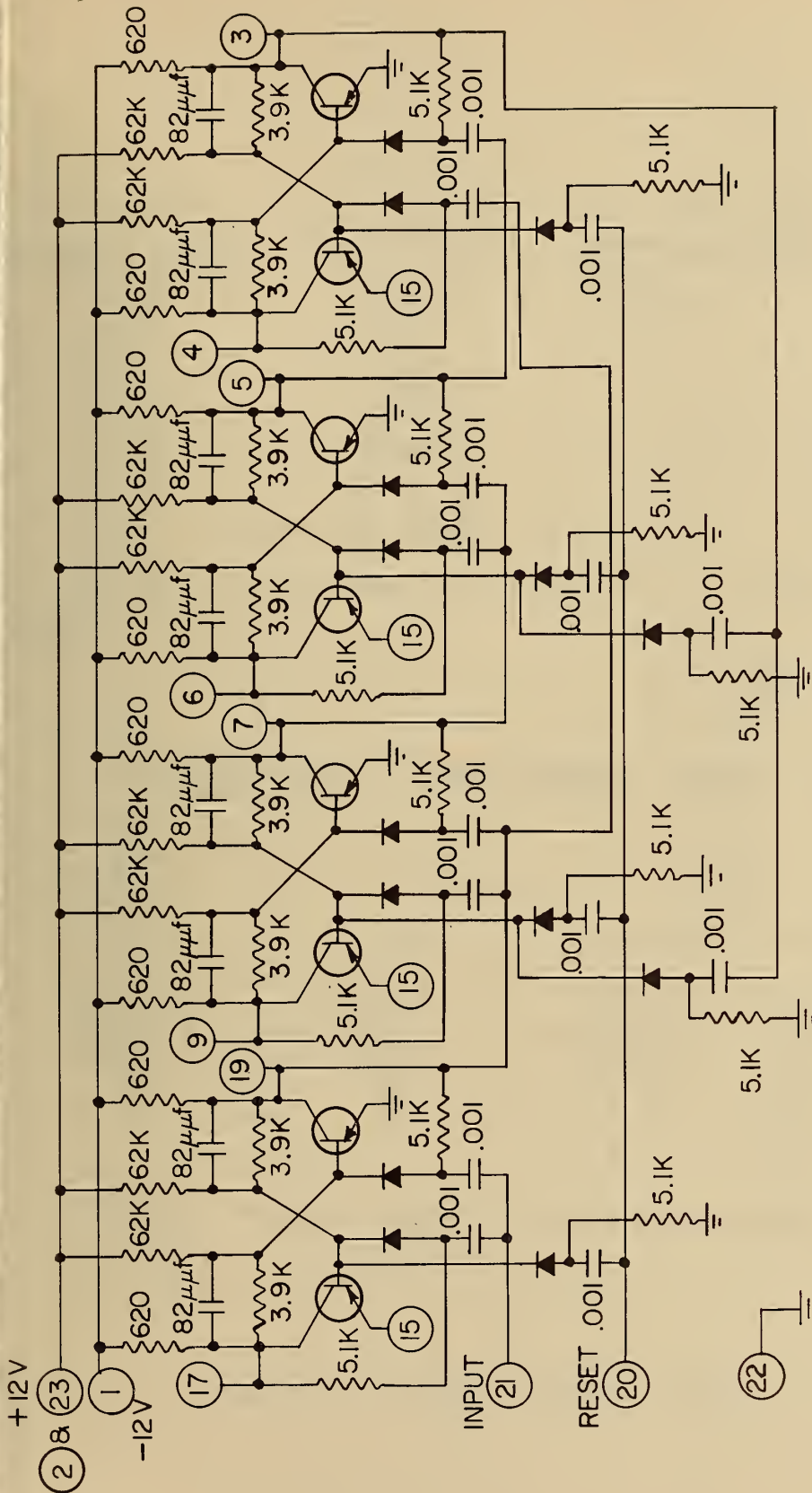
(15) = GROUND - MAY BE
GROUNDED THROUGH
N.C. SWITCH FOR
MANUAL RESET.
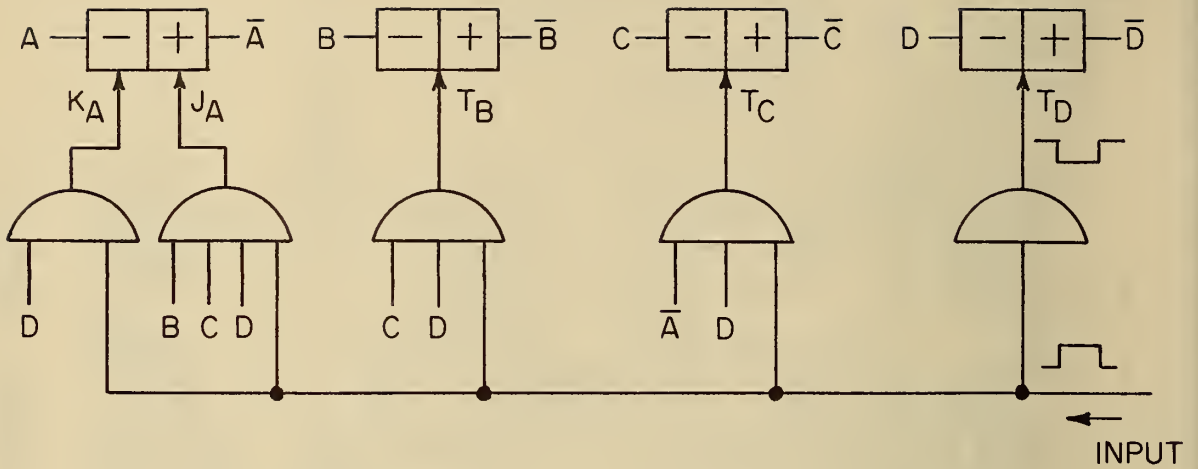
FIGURE 44. LOGICAL DIAGRAM FOR A BCD COUNTER
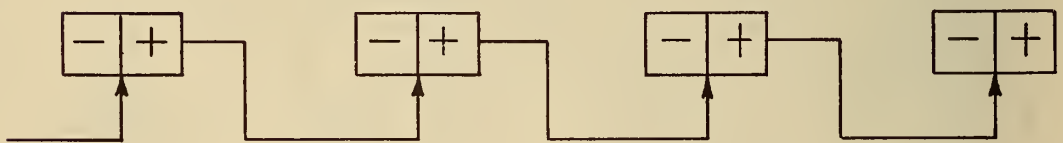
FIGURE 45. LOGICAL DIAGRAM OF A SERIAL BINARY COUNTER
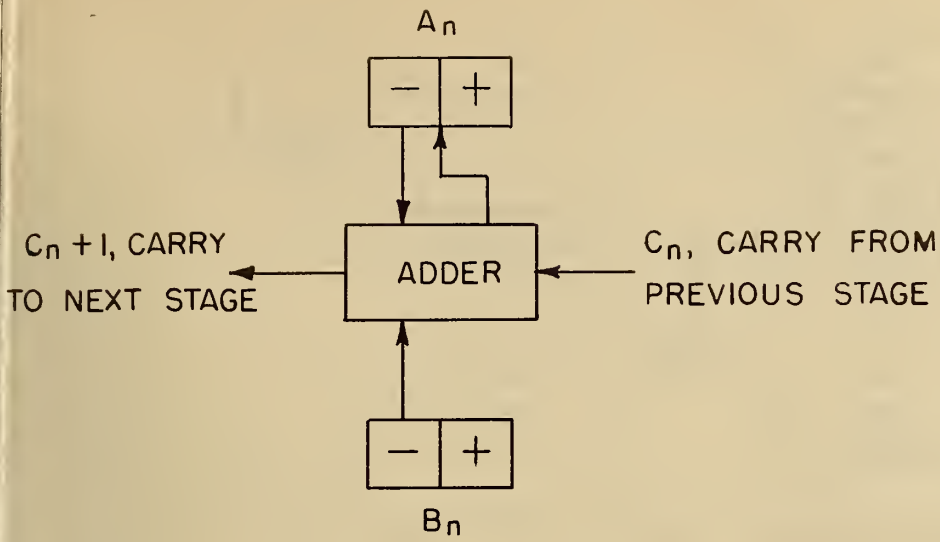
FIGURE 46. ADDER STAGE n
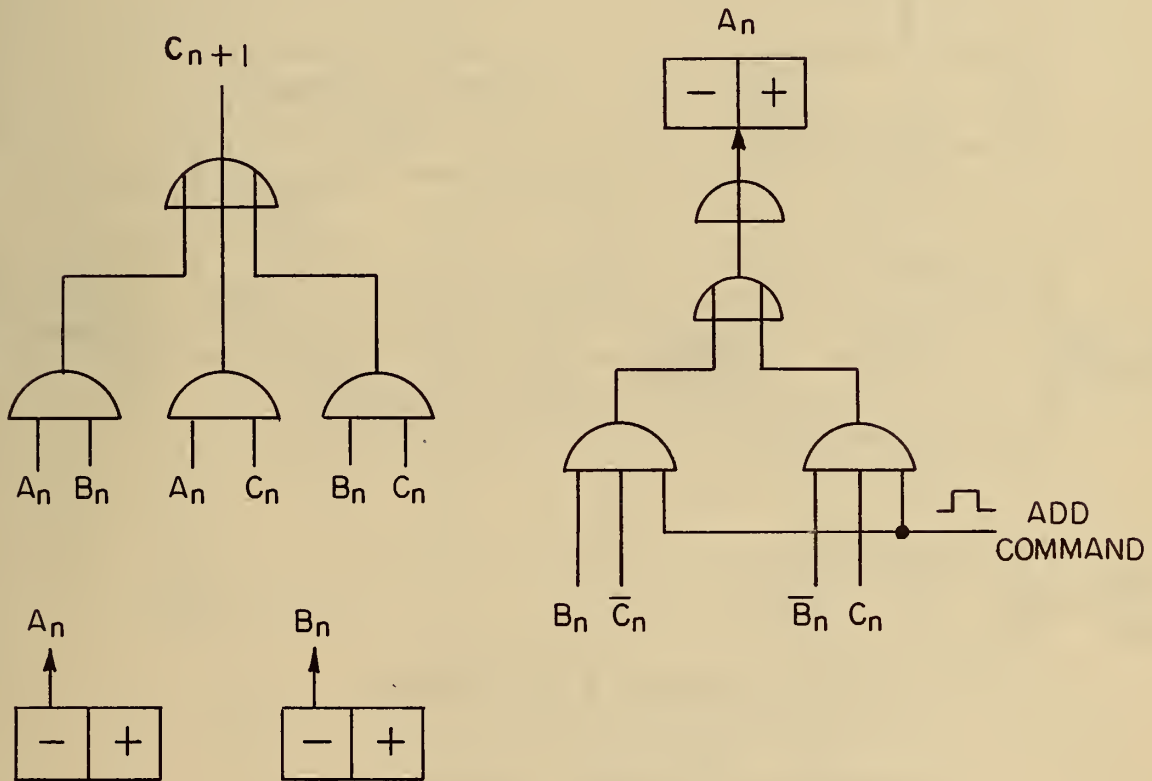
FIGURE 47. GENERAL ADDER STAGE
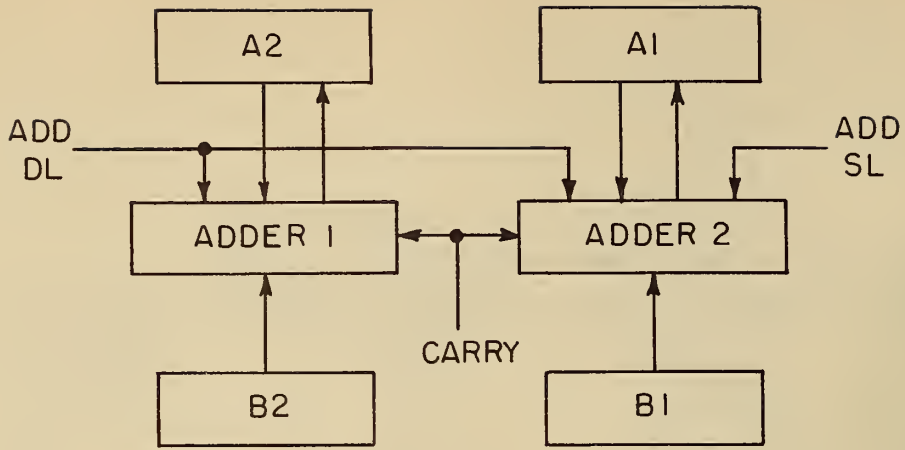
FIGURE 48. ADDER MICRO - OPERATION
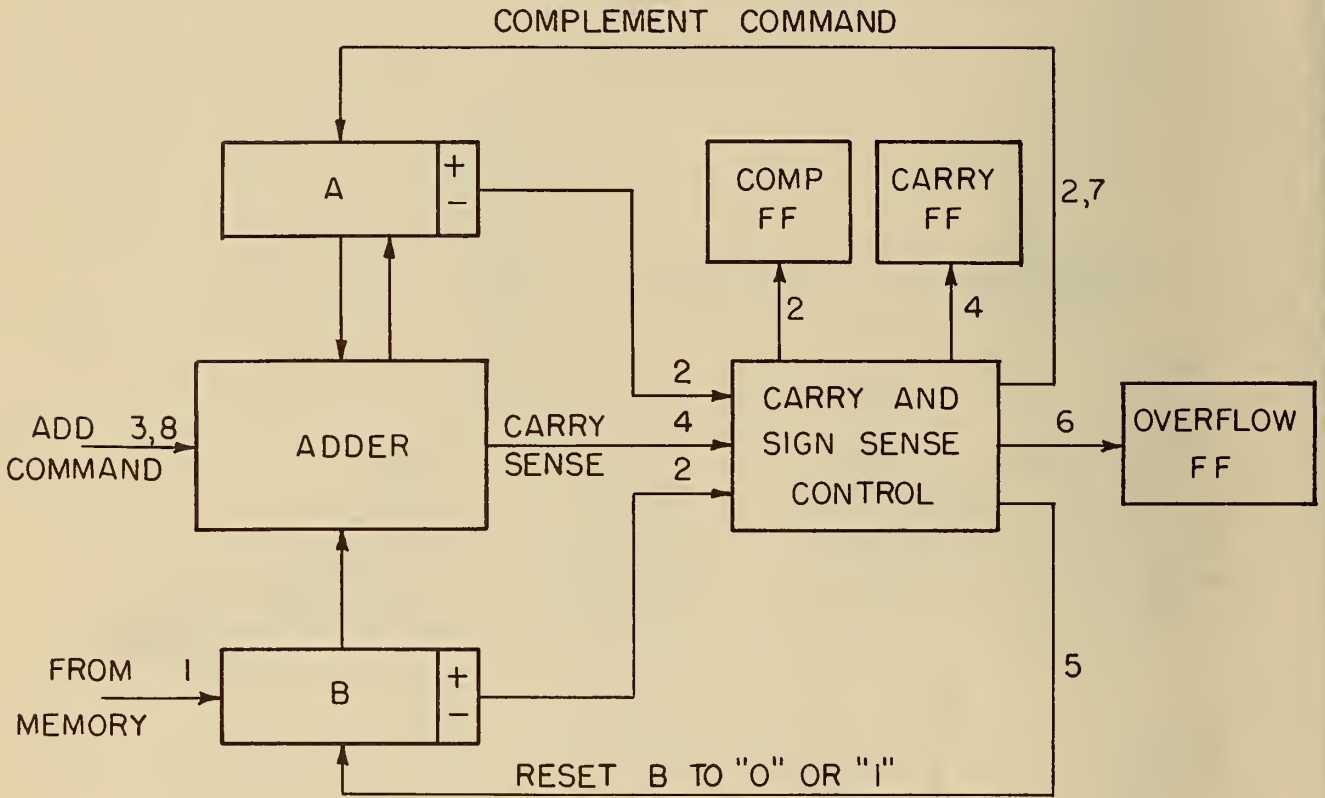
FIGURE 49. ADDITION CONTROL
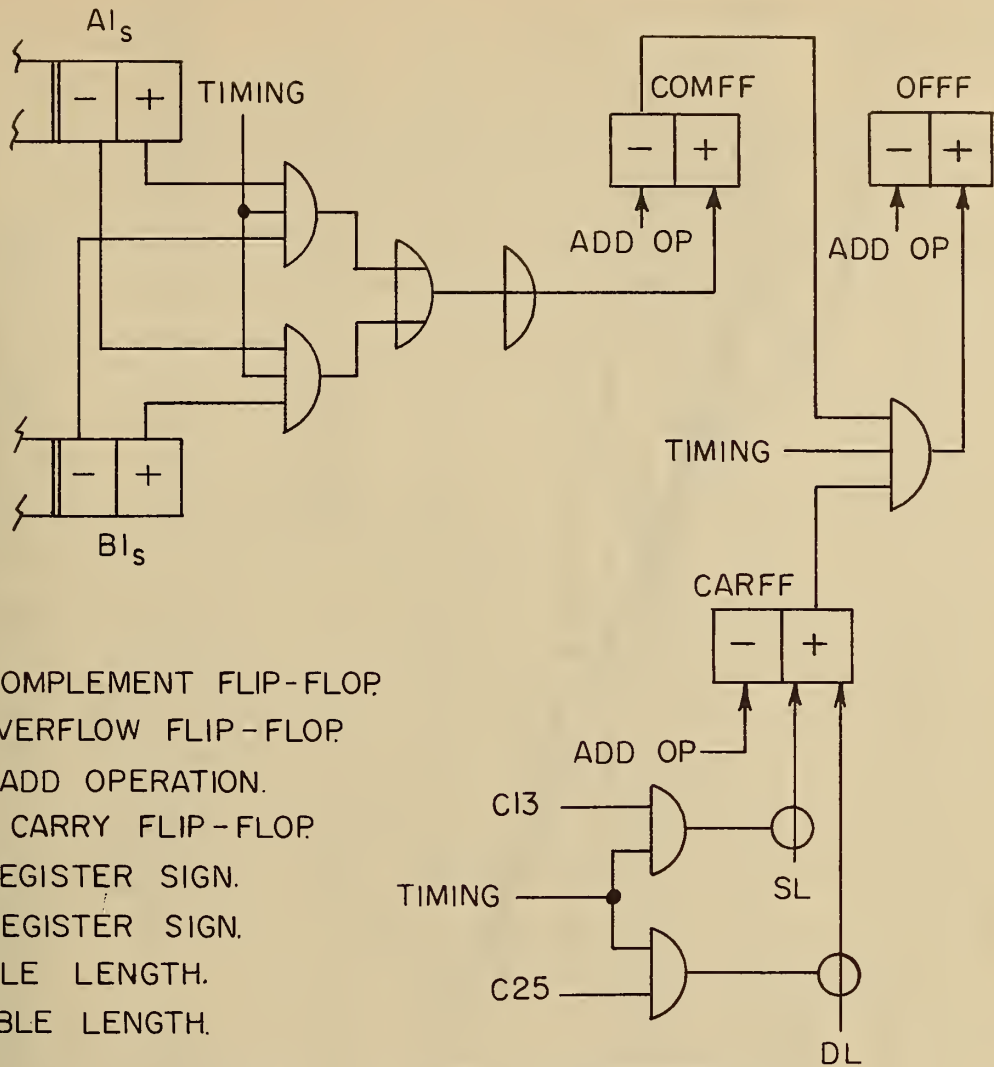
COMFF = COMPLEMENT FLIP-FLOP.
OFFF = OVERFLOW FLIP-FLOP.
ADD OP = ADD OPERATION.
CAR FF = CARRY FLIP-FLOP.
AI_s = A REGISTER SIGN.
BI_s = B REGISTER SIGN.
SL = SINGLE LENGTH.
DL = DOUBLE LENGTH.

FIGURE 50. ADDITION CONTROL LOGIC
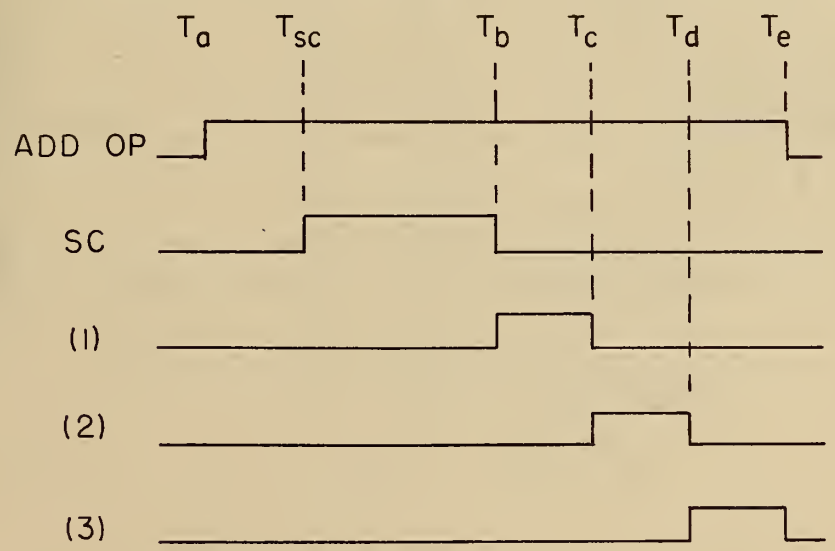
FIGURE 51. ADDITION TIMING
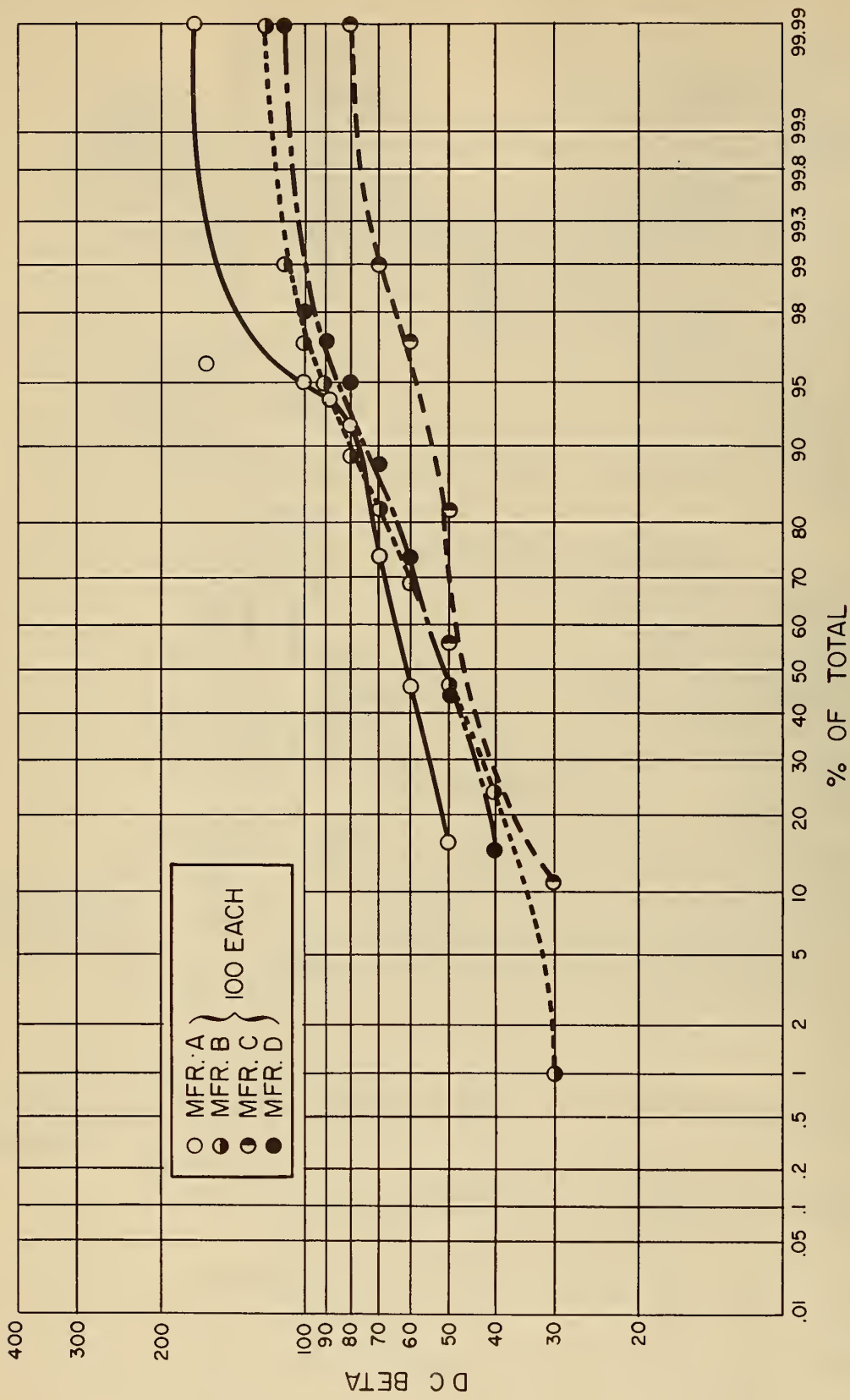
FIGURE 52. NORMAL DISTRIBUTION OF CURRENT GAIN FOR A 2N414 TYPE ALLOY JUNCTION TRANSISTOR (FROM FOUR MANUFACTURERS)
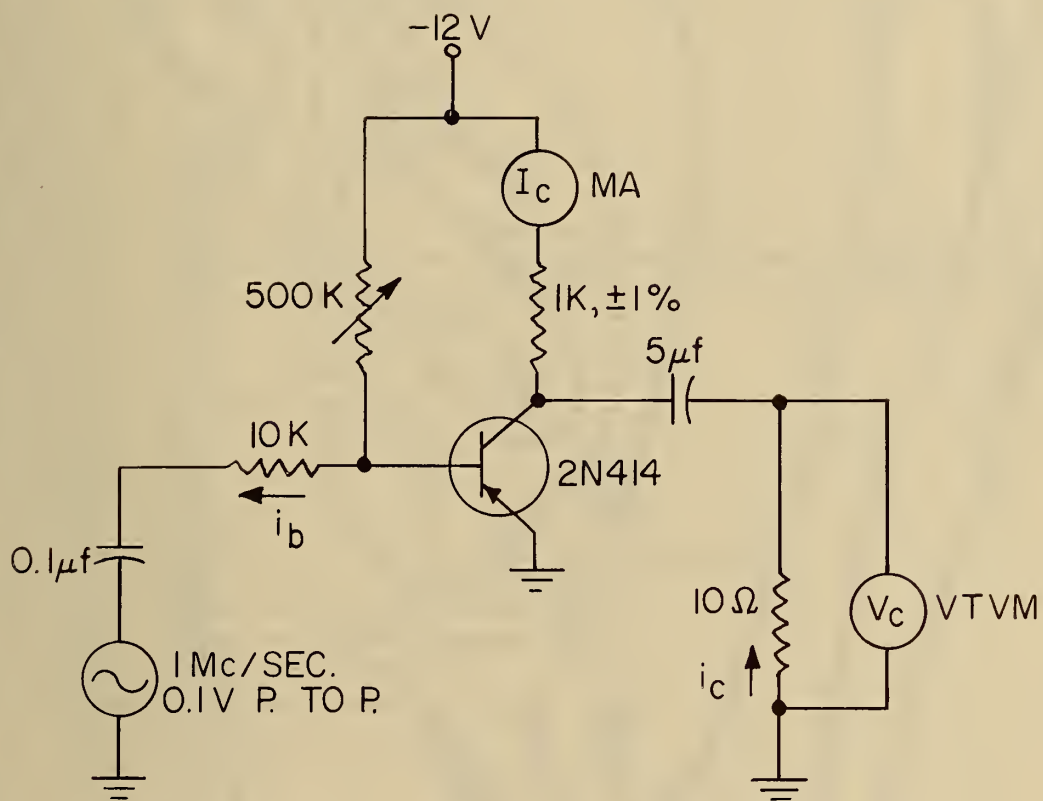
FIGURE 53. CIRCUIT FOR MEASURING f_t OF 2N414 TRANSISTOR
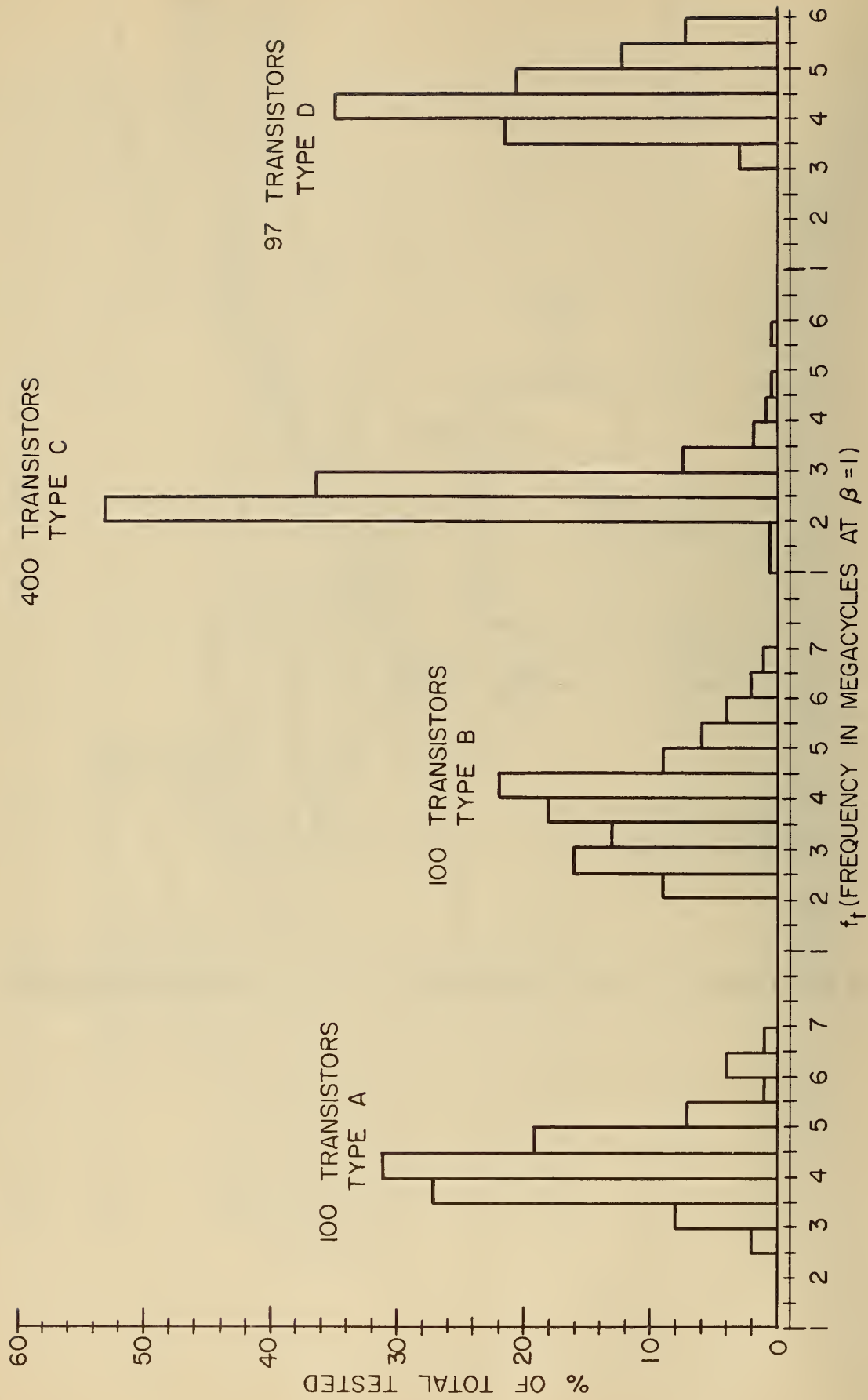
FIGURE 54. DISTRIBUTION HISTOGRAM FOR 2N414 TRANSISTORS FROM FOUR MANUFACTURERS

ANALOG VOLTAGE COMPARATOR
SERIES 2
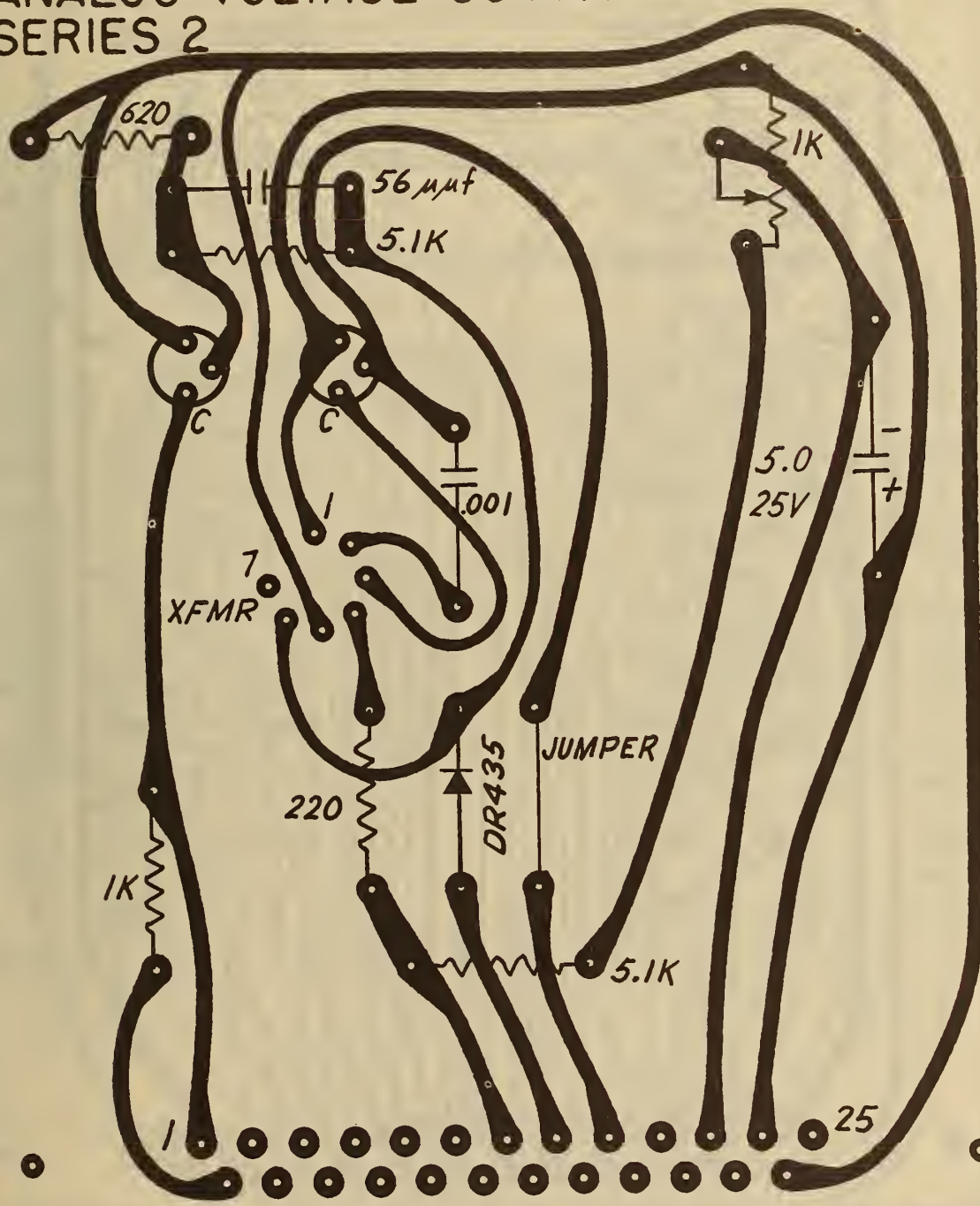
FIGURE 55
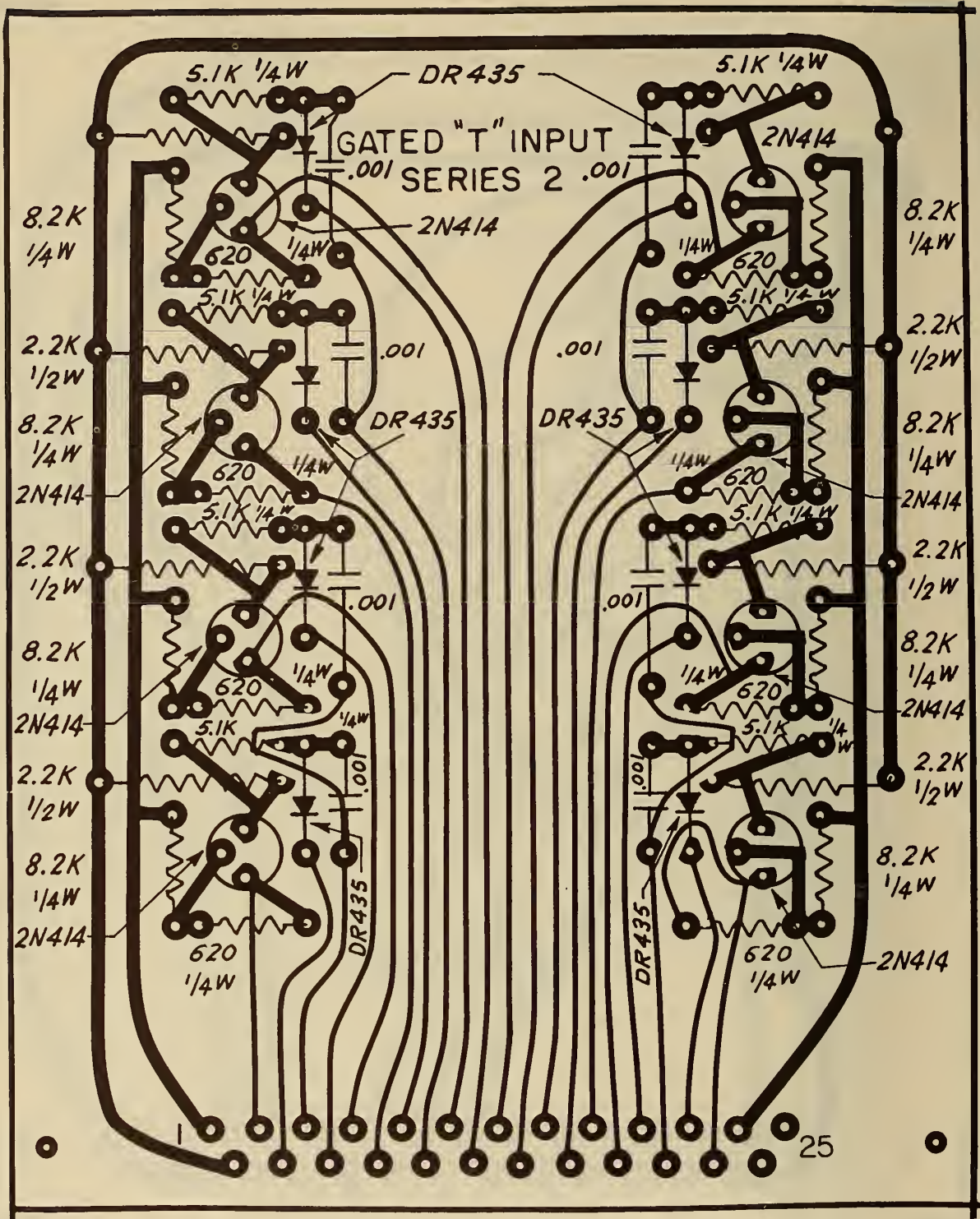
FIGURE 56

INDICATOR / AMPLIFIER
SERIES 2

Rc

62K   1/4W

2N414

2N414

8.2K
1/2W

1   25
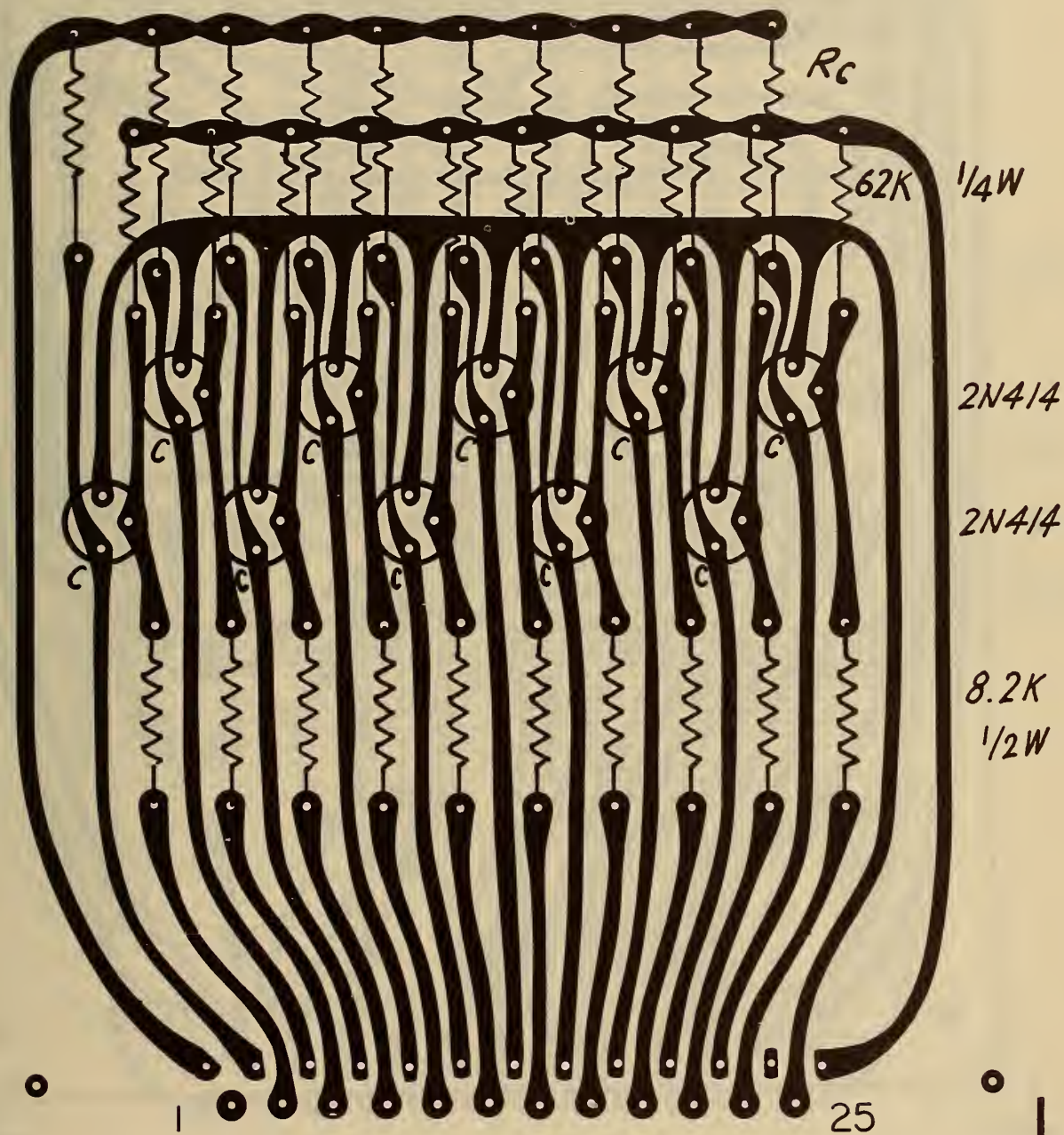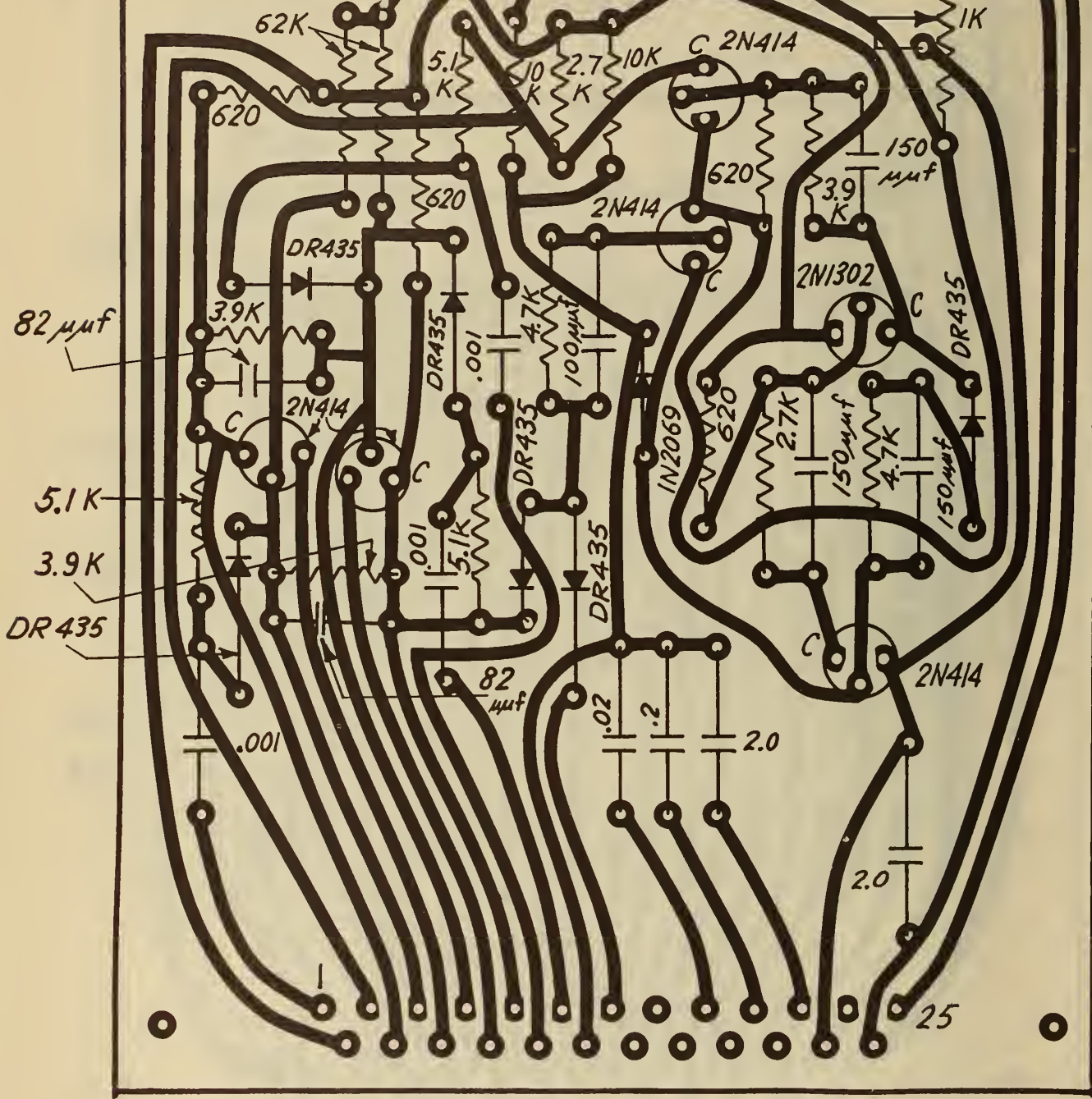
FIGURE 57

FIGURE 58

PREAMPLIFIER, SERIES 2

FIGURE 59

PULSE GATE DRIVER   SERIES 2
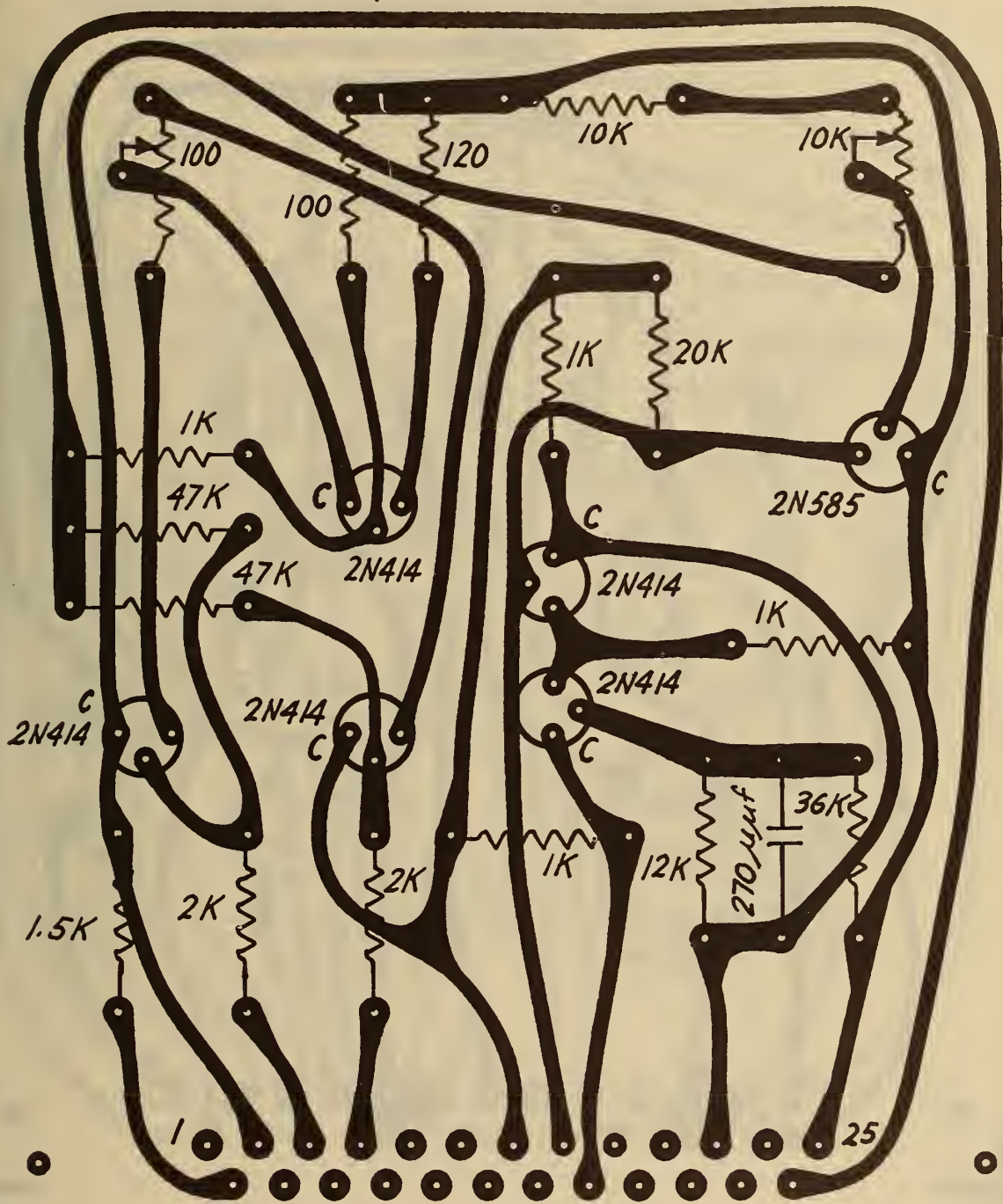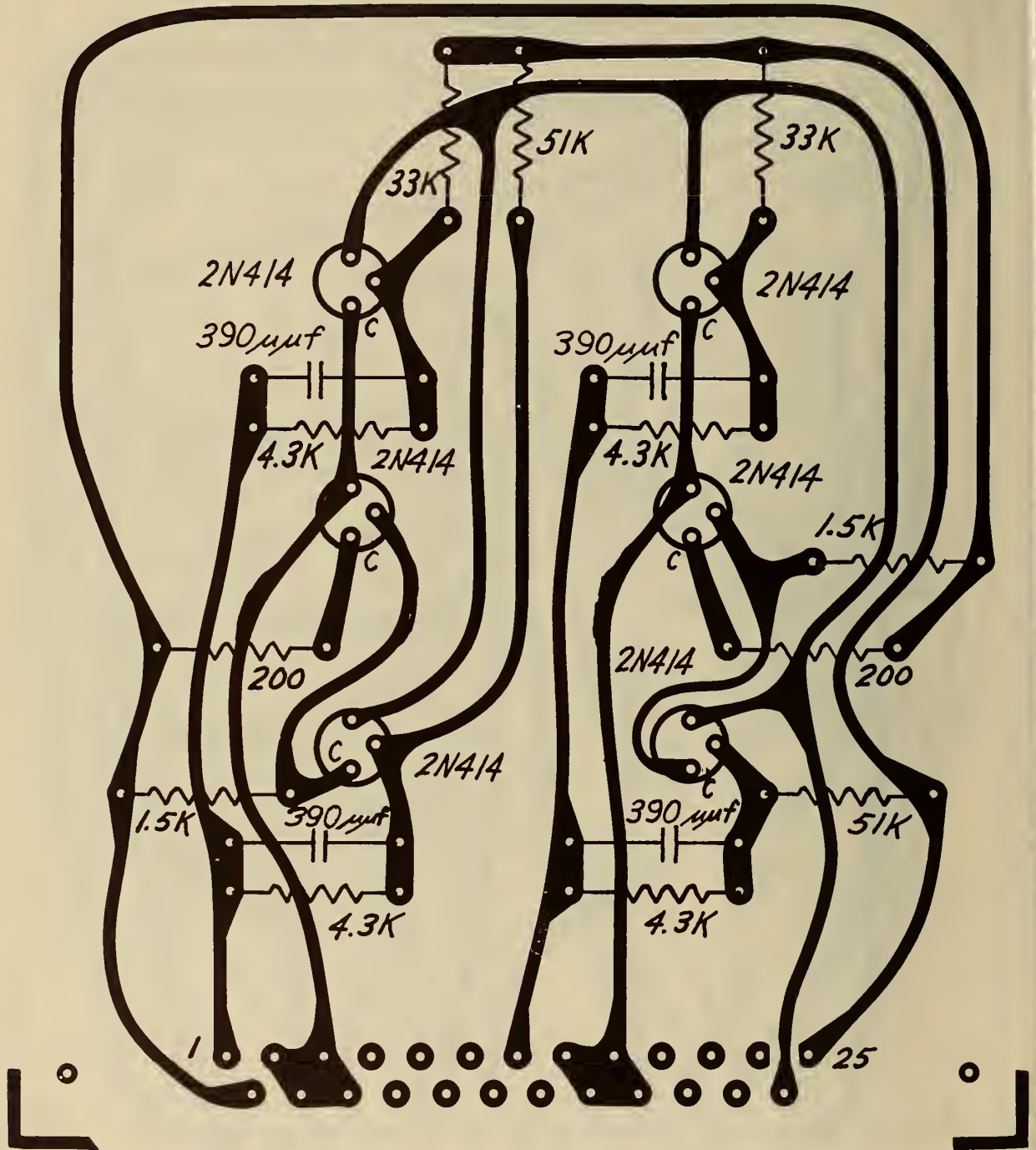
FIGURE 60

PULSE GENERATOR WITH FLIP-FLOP SERIES 2
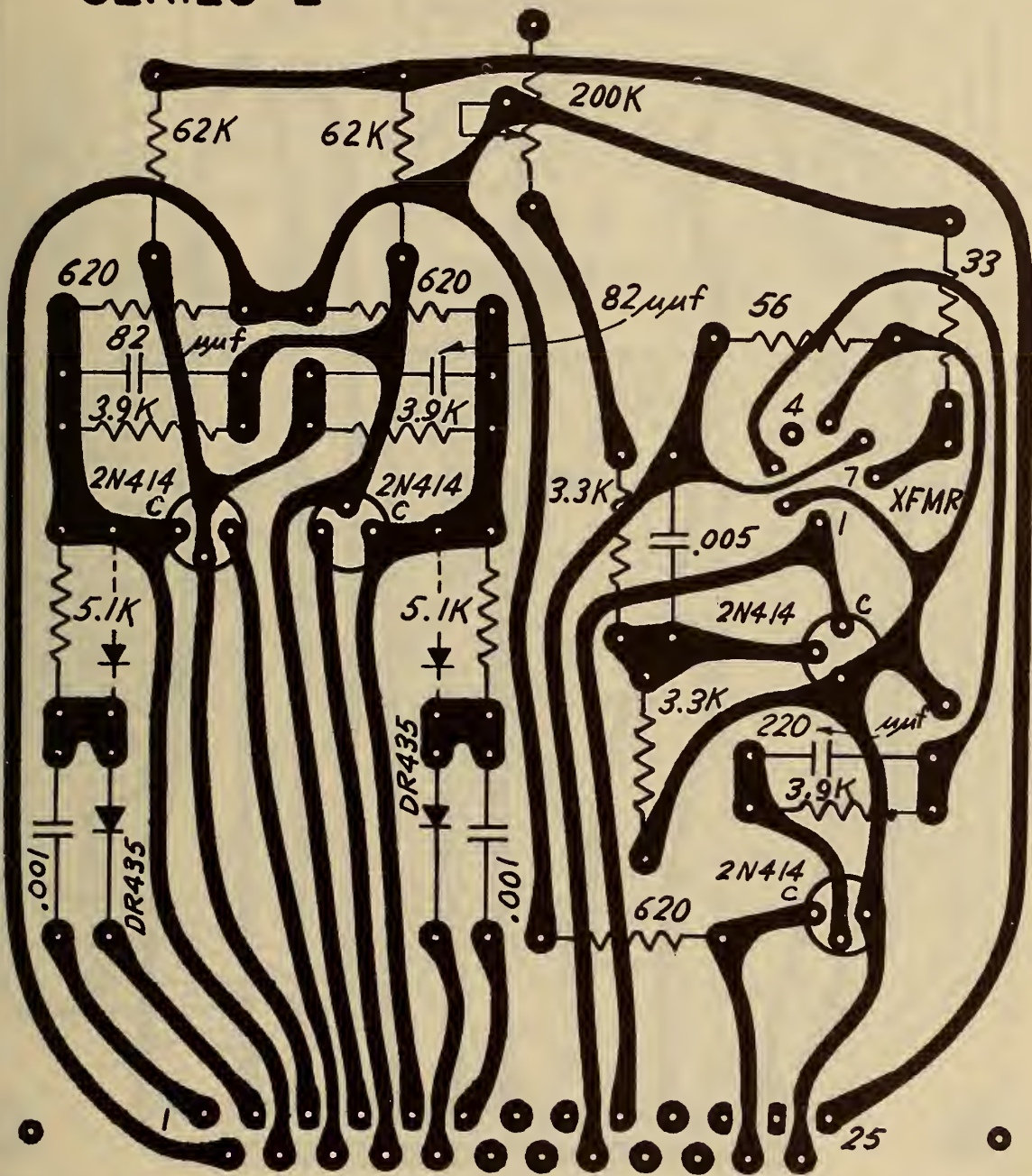
FIGURE 61

PULSE STRETCHER   SERIES 2

ALL TRANSISTORS 2N414
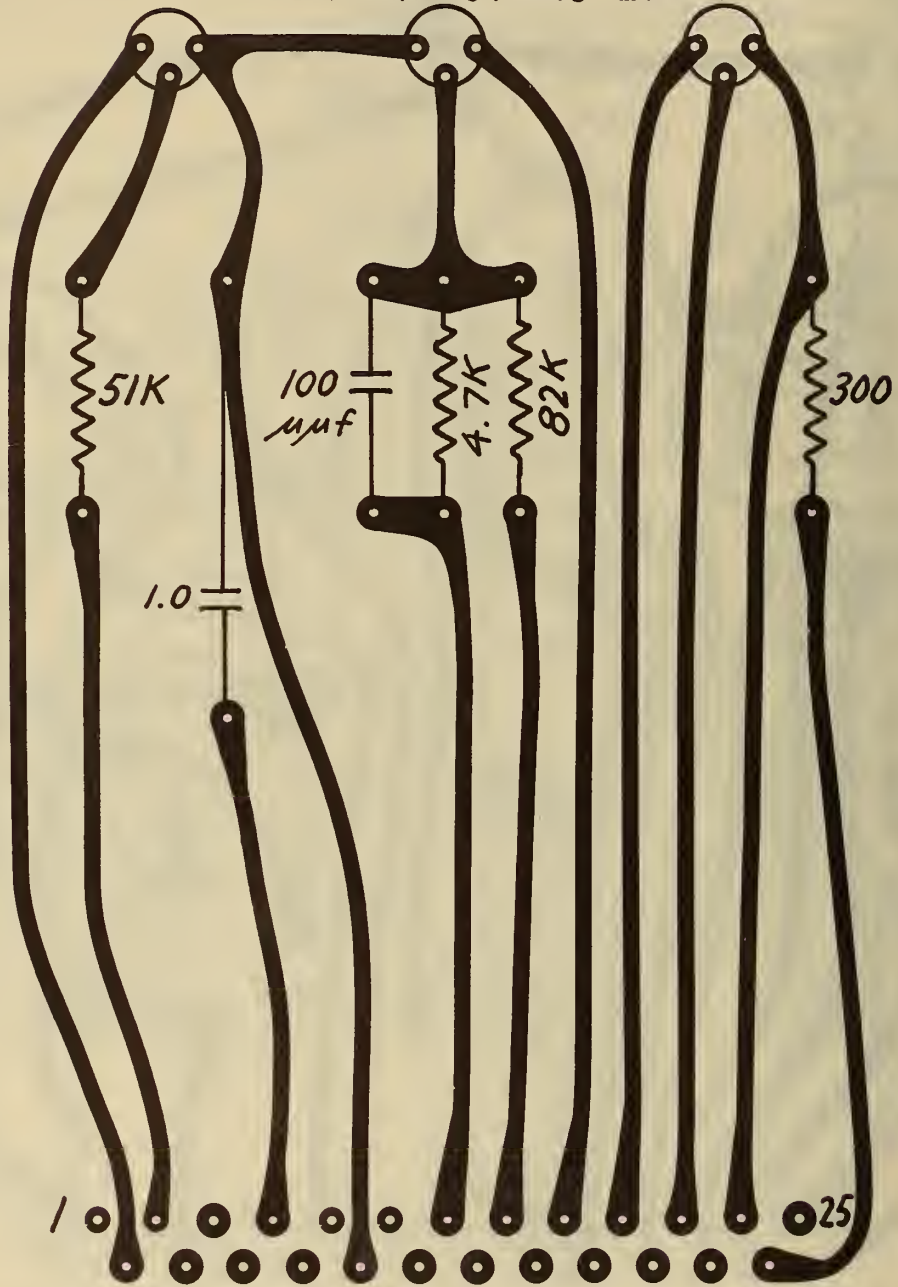
FIGURE 62
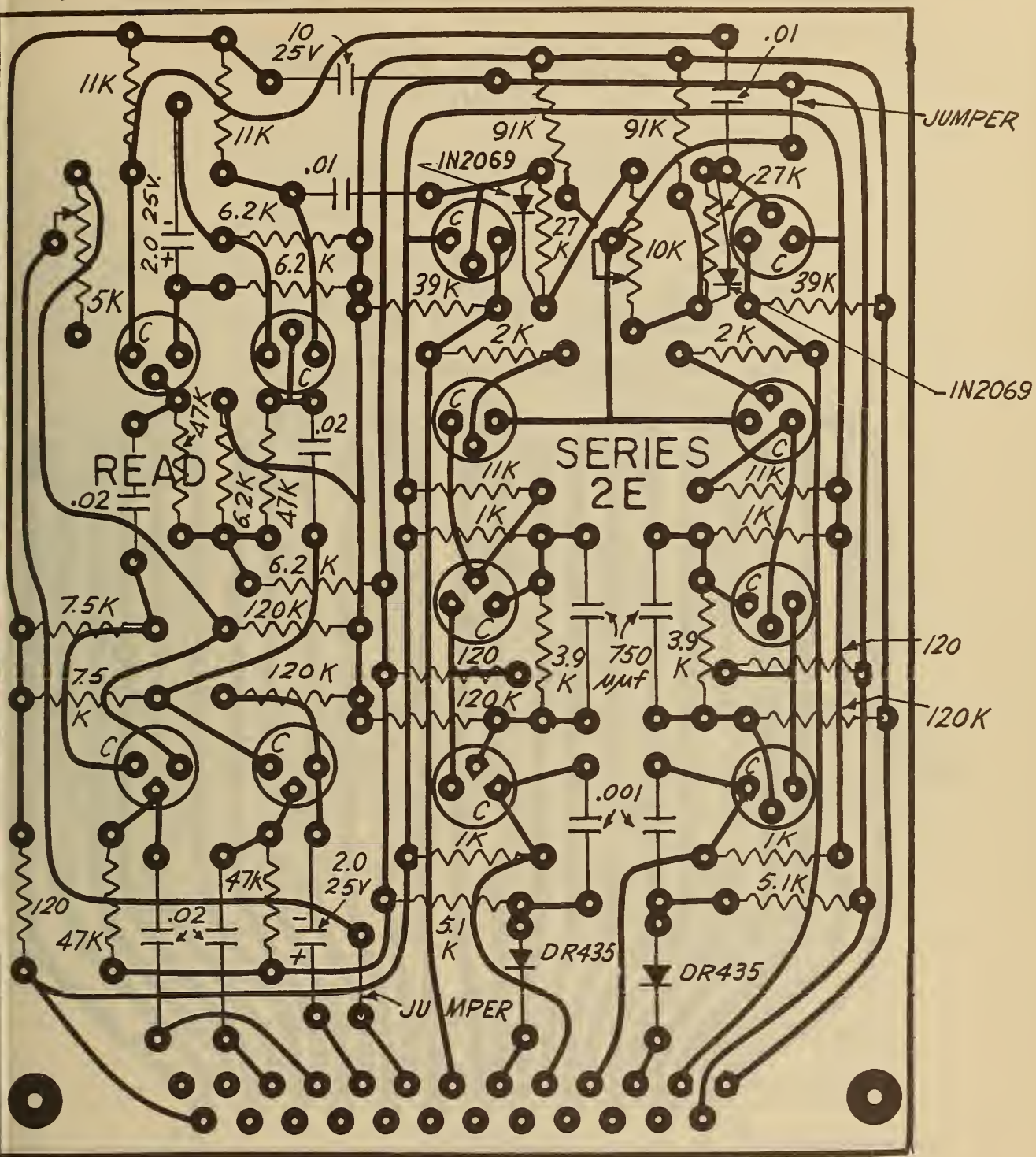
ALL TRANSISTORS ARE 2N414

FIGURE 63

SAMPLER PACKAGE
SERIES 2

ALL TRANSISTORS ARE 2N414
ALL DIODES ARE HB-2
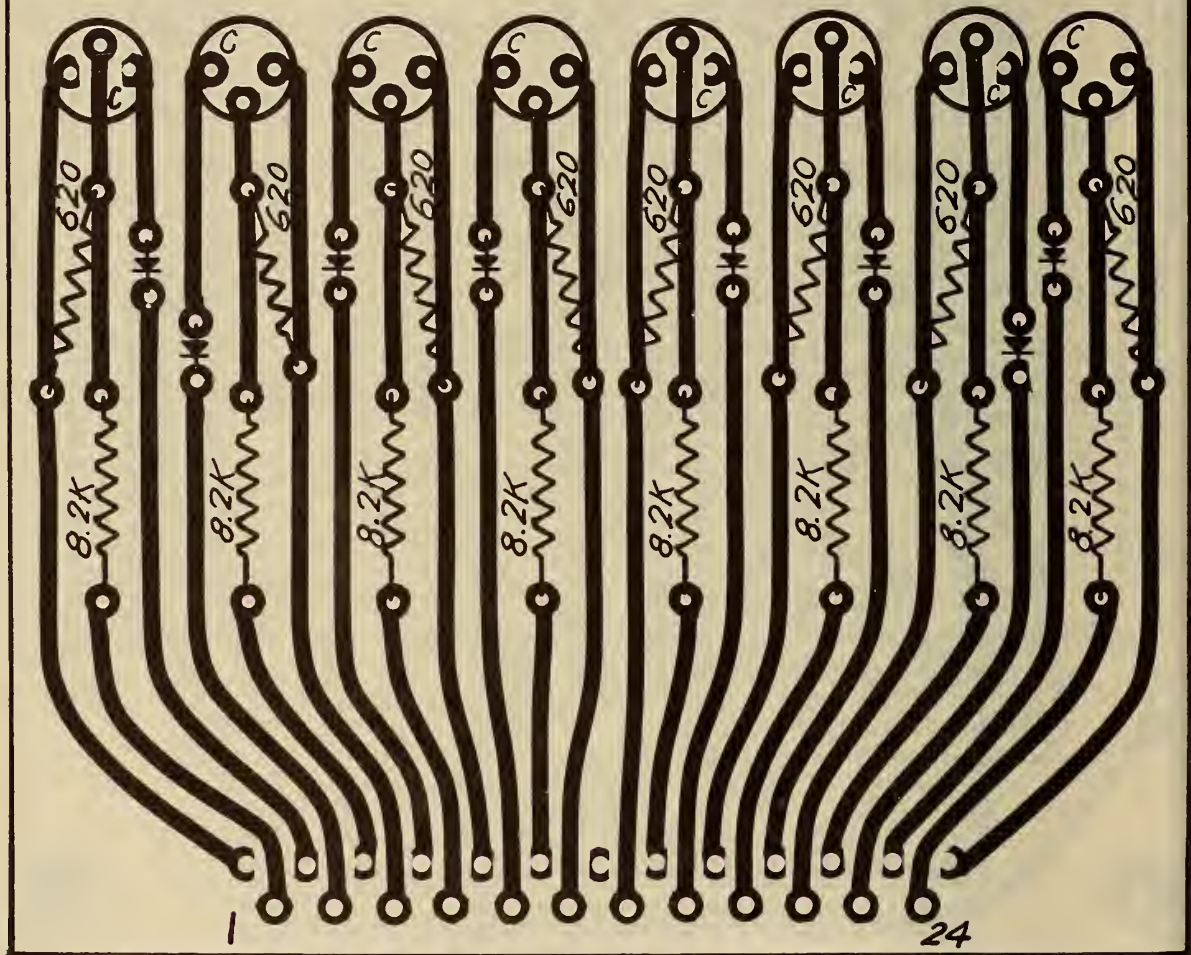
FIGURE 64

DUAL WRITE PACKAGE
SERIES 2

FIGURE 65

FIGURE 66

FIGURE 67

FIGURE 68
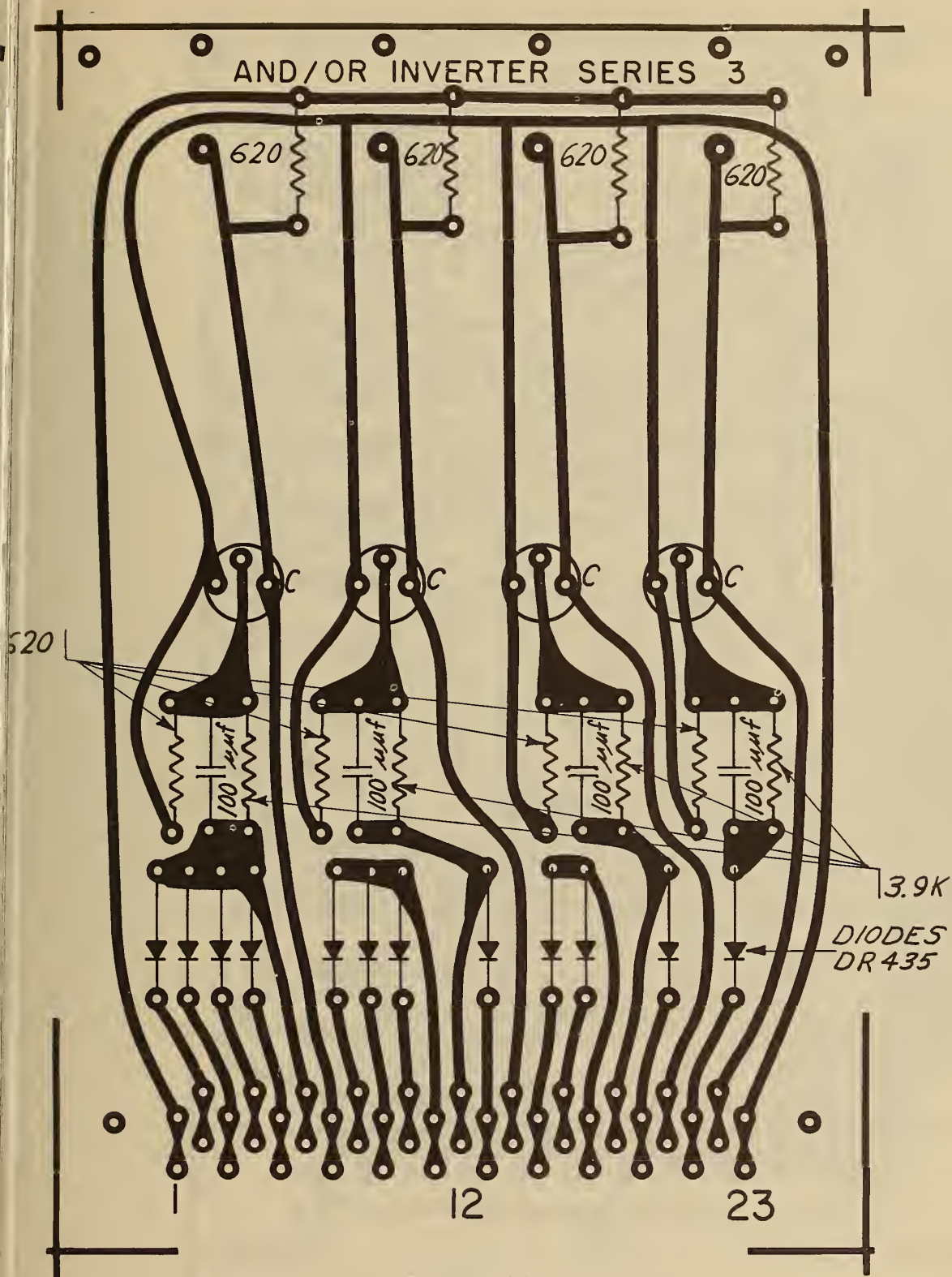
FIGURE 69

FIGURE 70

DECIMAL DECODER SERIES 3
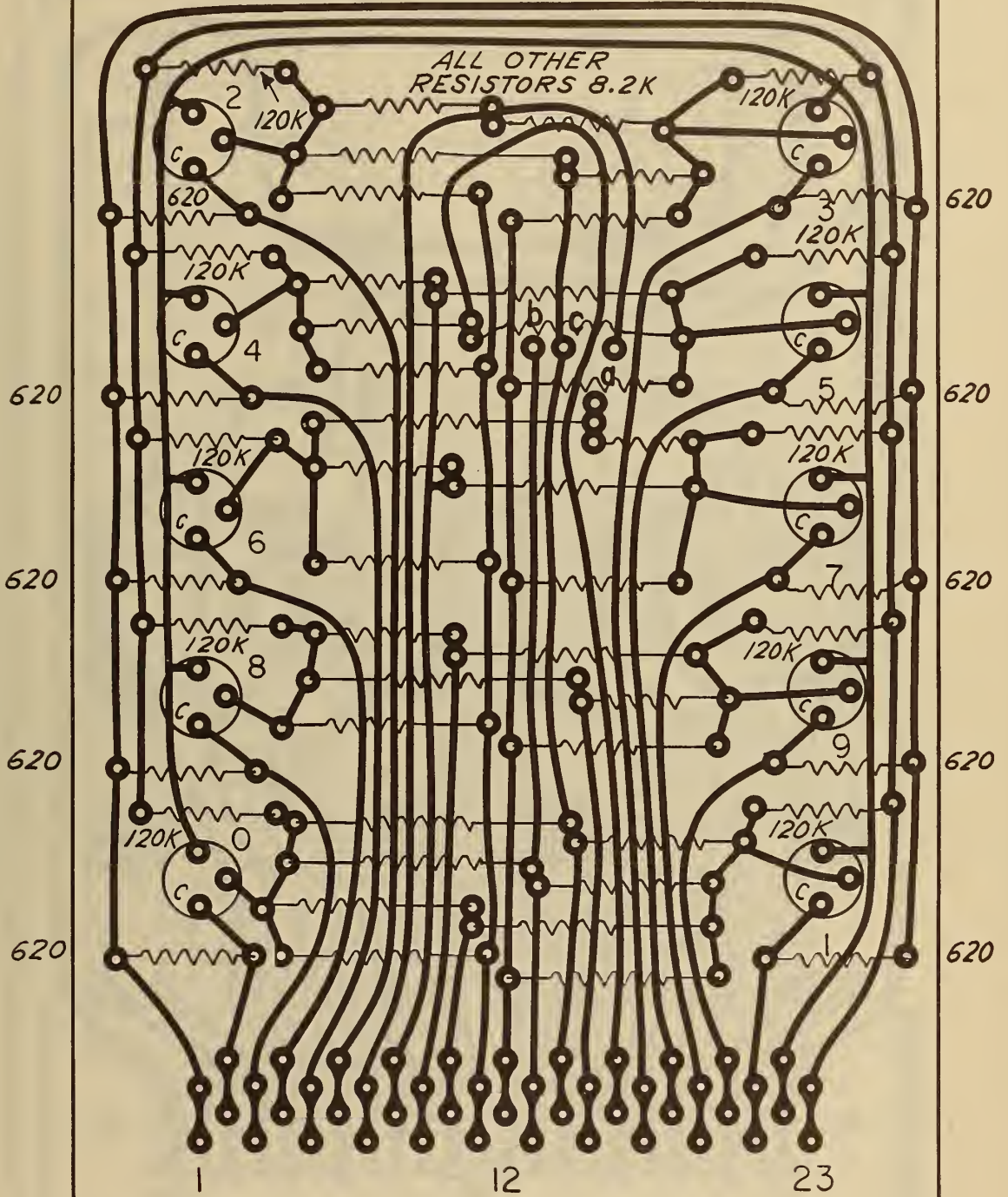
FIGURE 71
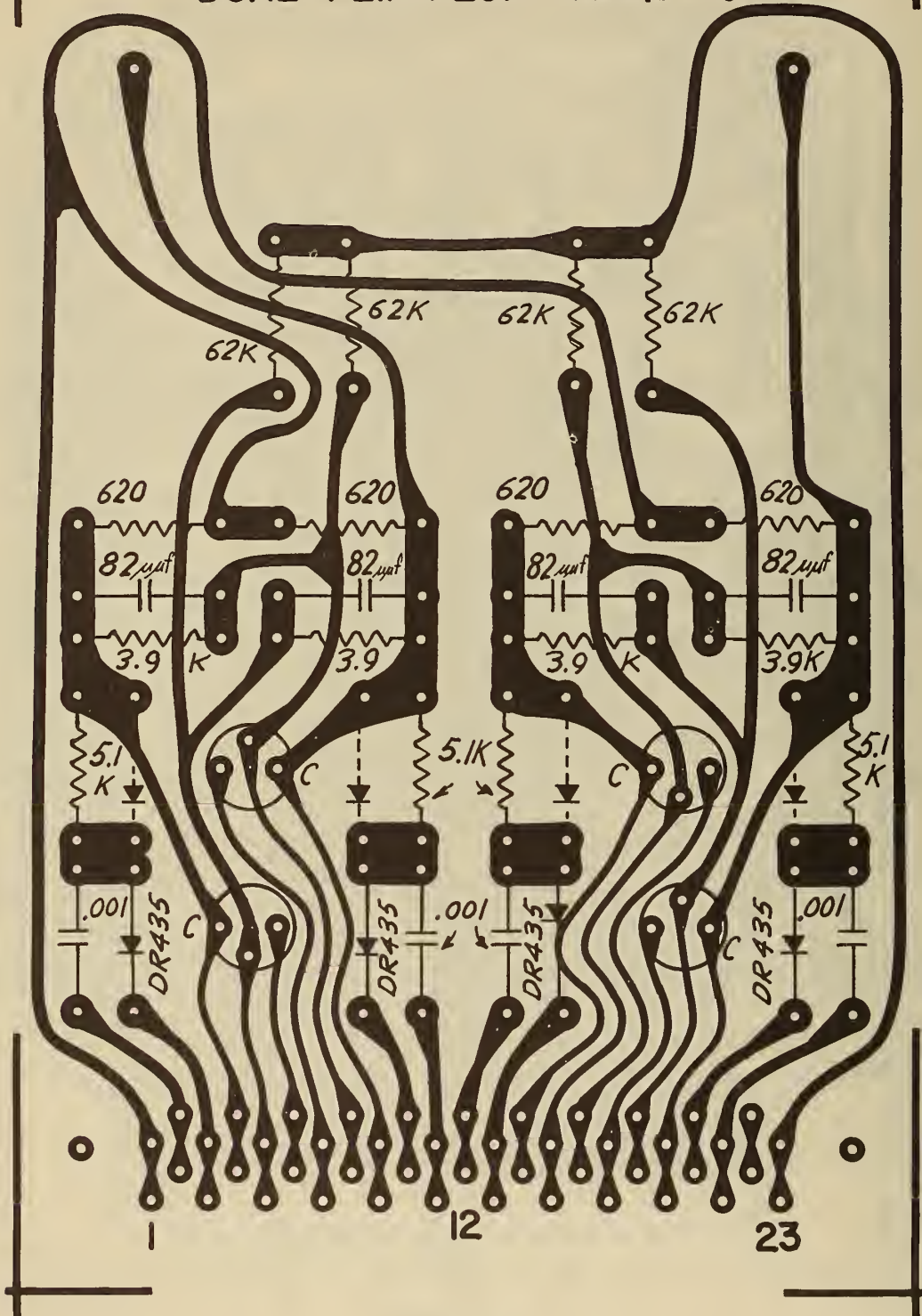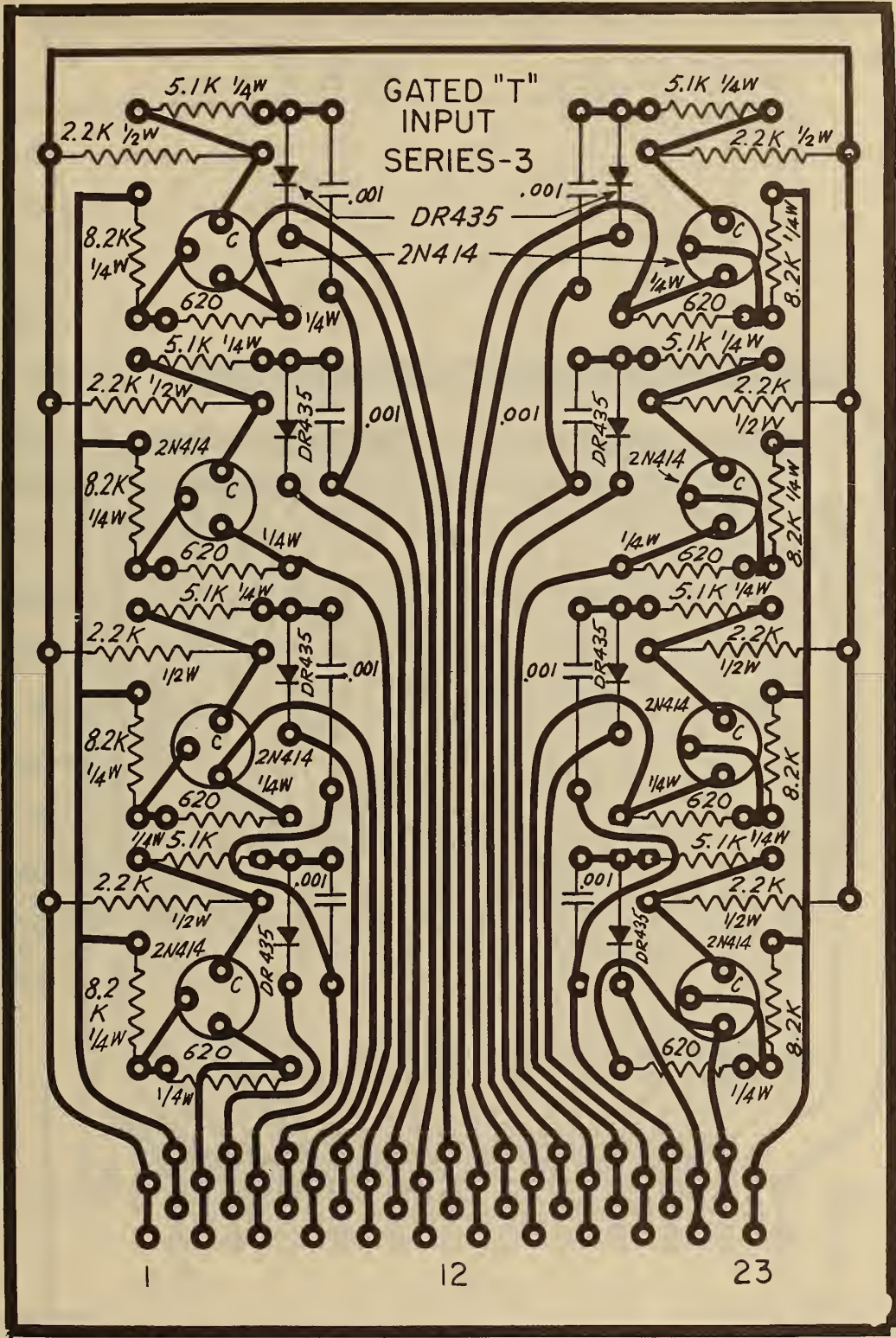
FIGURE 72

FIGURE 73

INDICATOR/
AMPLIFIER SERIES-3

Rc

62 K
1/4 W

2N414

8.2K
1/2W

1 12 23

FIGURE 74

OCTAL – HEXADECIMAL DECODER
SERIES – 3

620 ½W
120K ¼W
620 ½W
120K ¼W
620 ½W
120K ¼W
620 ½W
120K ¼W
620 ½W
120K ¼W
620 ½W
120K ¼W
620 ½W
120K ¼W

8.2K ¼W

TRAN-
SISTORS
2N414

−V   12   23   +V

FIGURE 75

FIGURE 76

FIGURE 77

PULSE GATE SERIES-3

5.1K
DR435
.001

1   12   23

FIGURE 78

FIGURE 79

FIGURE 80

FIGURE 8I

FIGURE 82

FIGURE 83

DUAL WRITE SERIES 3

FIGURE 84

THE NATIONAL BUREAU OF STANDARDS

The scope of activities of the National Bureau of Standards at its major laboratories in Washington, D.C., and Boulder, Colorado, is suggested in the following listing of t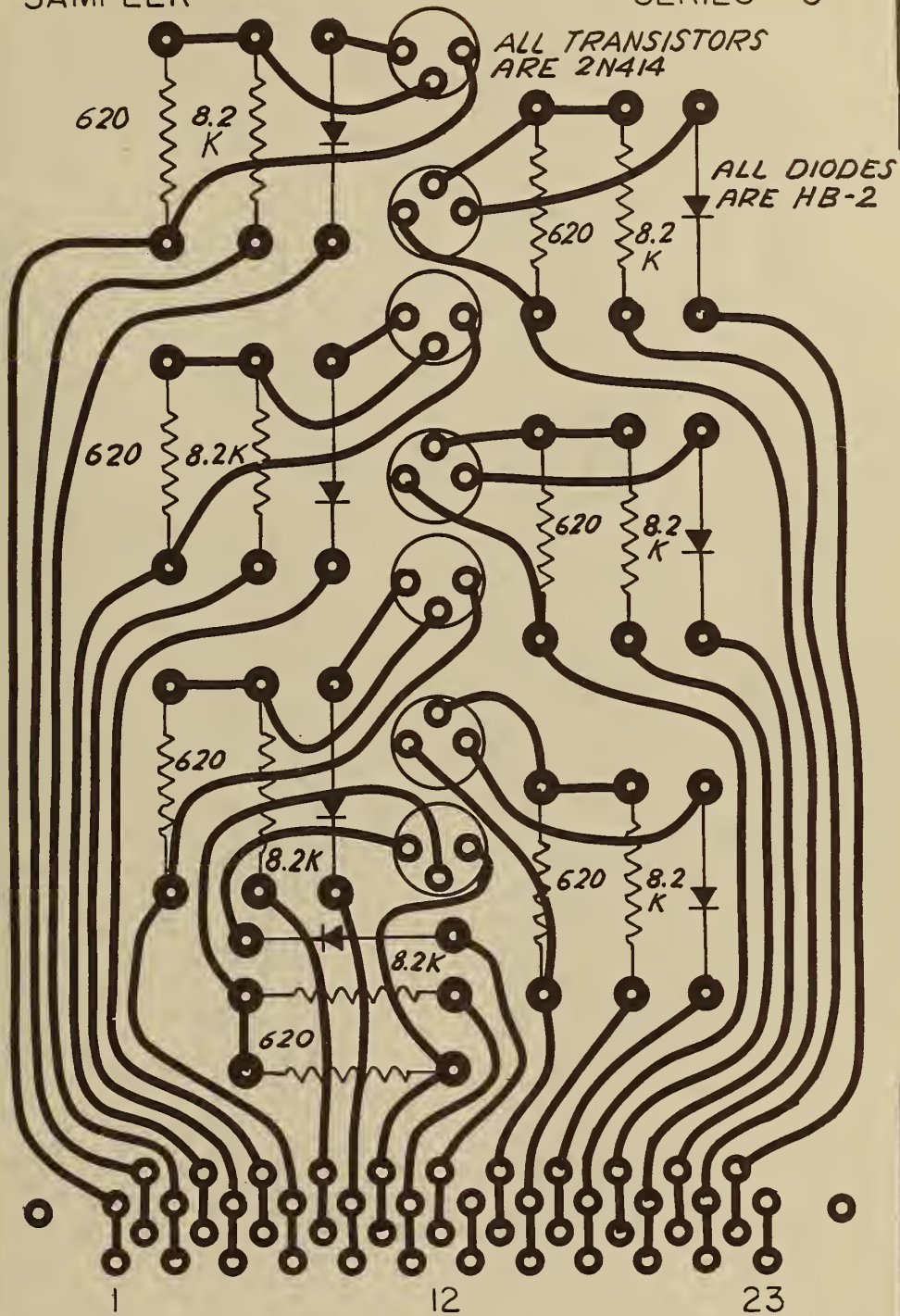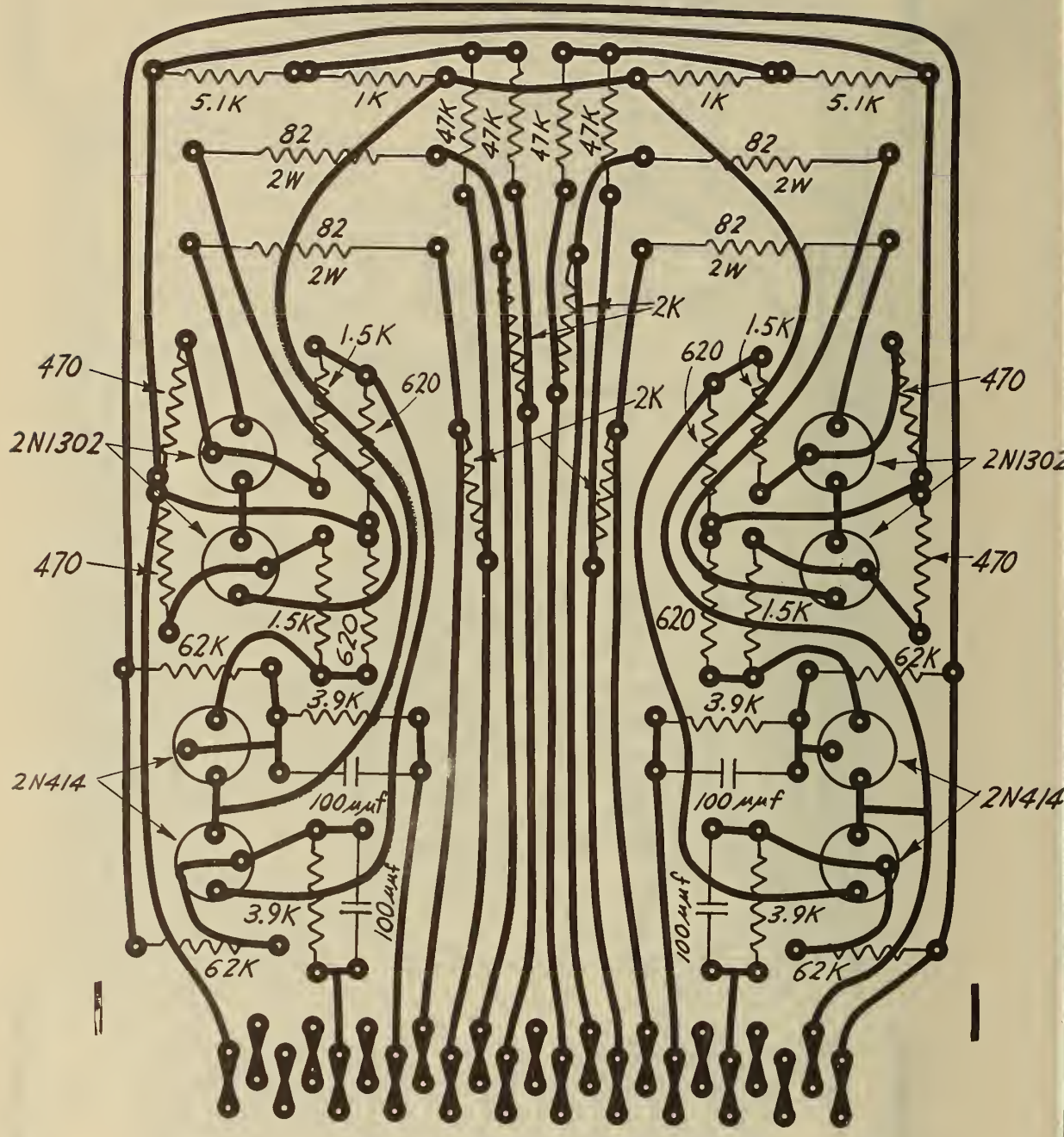he divisions and sections engaged in technical work. In general, each section carries out specialized research, development, and engineering in the field indicated by its title. A brief description of the activities, and of the resultant publications, appears on the inside of the front cover.

WASHINGTON, D. C.

Electricity. Resistance and Reactance. Electrochemistry. Electrical Instruments. Magnetic Measurements. Dielectrics. High Voltage.

Metrology. Photometry and Colorimetry. Refractometry. Photographic Research. Length. Engineering Metrology. Mass and Scale. Volumetry and Densimetry.

Heat. Temperature Physics. Heat Measurements. Cryogenic Physics. Equation of State. Statistical Physics.

Radiation Physics. X-ray. Radioactivity. Radiation Theory. High Energy Radiation. Radiological Equipment. Nucleonic Instrumentation. Neutron Physics.

Analytical and Inorganic Chemistry. Pure Substances. Spectrochemistry. Solution Chemistry. Standard Reference Materials. Applied Analytical Research. Crystal Chemistry.

Mechanics. Sound. Pressure and Vacuum. Fluid Mechanics. Engineering Mechanics. Rheology. Combustion Controls.

Polymers. Macromolecules: Synthesis and Structure. Polymer Chemistry. Polymer Physics. Polymer Characterization. Polymer Evaluation and Testing. Applied Polymer Standards and Research. Dental Research.

Metallurgy. Engineering Metallurgy. Microscopy and Diffraction. Metal Reactions. Metal Physics. Electrolysis and Metal Deposition.

Inorganic Solids. Engineering Ceramics. Glass. Solid State Chemistry. Crystal Growth. Physical Properties. Crystallography.

Building Research. Structural Engineering. Fire Research. Mechanical Systems. Organic Building Materials. Codes and Safety Standards. Heat Transfer. Inorganic Building Materials. Metallic Building Materials.

Applied Mathematics. Numerical Analysis. Computation. Statistical Engineering. Mathematical Physics. Operations Research.

Data Processing Systems. Components and Techniques. Computer Technology. Measurements Automation. Engineering Applications. Systems Analysis.

Atomic Physics. Spectroscopy. Infrared Spectroscopy. Far Ultraviolet Physics. Solid State Physics. Electron Physics. Atomic Physics. Plasma Spectroscopy.

Instrumentation. Engineering Electronics. Electron Devices. Electronic Instrumentation. Mechanical Instruments. Basic Instrumentation.

Physical Chemistry. Thermochemistry. Surface Chemistry. Organic Chemistry. Molecular Spectroscopy. Elementary Processes. Mass Spectrometry. Photochemistry and Radiation Chemistry.

Office of Weights and Measures.

BOULDER, COLO.

Cryogenic Engineering Laboratory. Cryogenic Equipment. Cryogenic Processes. Properties of Materials. Cryogenic Technical Services.

CENTRAL RADIO PROPAGATION LABORATORY

Ionosphere Research and Propagation. Low Frequency and Very Low Frequency Research. Ionosphere Research. Prediction Services. Sun-Earth Relationships. Field Engineering. Radio Warning Services. Vertical Soundings Research.

Radio Propagation Engineering. Data Reduction Instrumentation. Radio Noise. Tropospheric Measurements. Tropospheric Analysis. Propagation-Terrain Effects. Radio-Meteorology. Lower Atmosphere Physics.

Radio Systems. Applied Electromagnetic Theory. High Frequency and Very High Frequency Research. Frequency Utilization. Modulation Research. Antenna Research. Radiodetermination.

Upper Atmosphere and Space Physics. Upper Atmosphere and Plasma Physics. High Latitude Ionosphere Physics. Ionosphere and Exosphere Scatter. Airglow and Aurora. Ionospheric Radio Astronomy.

RADIO STANDARDS LABORATORY

Radio Physics. Radio Broadcast Service. Radio and Microwave Materials. Atomic Frequency and Time-Interval Standards. Radio Plasma. Millimeter-Wave Research.

Circuit Standards. High Frequency Electrical Standards. High Frequency Calibration Services. High Frequency Impedance Standards. Microwave Calibration Services. Microwave Circuit Standards. Low Frequency Calibration Services.