United States Department of Commerce
Technology Administration
National Institute of Standards and Technology

NIST Technical Note 1420

NIST High-Accuracy Sampling Wattmeter

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August 1996

U.S. Department of Commerce
Michael Kantor, Secretary

Technology Administration
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National Institute of Standards and Technology
Arati Prabhakar, Director

National Institute of Standards
and Technology
Technical Note 1420
Natl. Inst. Stand. Technol.
Tech. Note 1420
54 pages (Aug. 1996)
CODEN: NTNOEF

U.S. Government Printing Office
Washington: 1996

For sale by the Superintendent of
Documents
U.S. Government Printing Office
Washington, DC 20402

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Abstract - A high-accuracy sampling wattmeter was developed at the National Institute of Standards and Technology (NIST) to investigate the feasibility of using waveform sampling techniques for making very accurate power measurements at frequencies from 50 Hz to 1000 Hz. The goal of this effort was to develop an instrument having a full scale measurement uncertainty over these frequencies of less than ± 50 μW/W. The prototype instrument that came out of the development was used to demonstrate the accuracy achievable with the digital sampling method. The new high-accuracy sampling wattmeter was built around a wideband instrument developed earlier at NIST. The new wattmeter uses 16-bit analog-to-digital (A/D) converters and includes a two-stage current transformer in one of the input modules. This wattmeter operates with asynchronous sampling as did the previous wattmeter. The high accuracy is achieved by approximately synchronizing the interval over which samples are taken with the period of the input signal. Special care was taken to design input stages with a flat frequency response and low temperature sensitivity. The wattmeter has been calibrated using the NIST Audio-Frequency Power Bridge. The two instruments agreed to better than ± 50 μW/W, of full scale, over the 50 Hz to 1000 Hz frequency range at a wide range of power factors.

1. Introduction

The NIST High-Accuracy Sampling Wattmeter (HASW) was designed and fabricated at the National Institute of Standards and Technology (NIST) to meet the need for a high-accuracy (± 50 μW/W) power measurement of low-distortion power signals in the power frequency range (fundamental frequency of 50 Hz to 1 kHz) and to examine to what level of uncertainty the sampling method for power measurement can be extended. The operation and the performance of the HASW is described in this report. It is a second generation instrument, which uses portions of an earlier 12-bit Wideband Sampling Wattmeter [1,2]. This report also describes the changes made to the Wideband Sampling Wattmeter. The power measurement technique used in the new instrument is basically the same as that used in the earlier wattmeter: dual-channel sampling using commercial track-and-hold (T/H), analog-to-digital (A/D) conversion, real-time multiplication, and microcomputer control. The reports on the earlier wattmeter [1,2] should be used to understand the operation of those portions of the new wattmeter that were not changed and are not described in this report.

The HASW uses two opto-isolated plug-in input modules (channels) to sample the input voltage and current signals at sampling rates up to 75 kHz, using 16-bit A/D converters. A high-speed digital multiplier-accumulator is used to calculate the power in real time from a large number of

input signal samples. The real-time multiplier-accumulator, together with the microcomputer, allows the wattmeter to calculate the power by averaging a large number of samples. The wattmeter has a relatively constant uncertainty for signal frequencies from 50 Hz to 1 kHz. The wattmeter response for higher frequencies is primarily limited by the response of the input modules. A feature unique to the earlier wideband sampling wattmeter, and used on this new wattmeter, is the use of programmable time-delay circuits to compensate for differential time delay between the two input channels.

Section 2 describes the basic operating principles of the HASW. A brief description is given of the various circuit operations. Section 3 provides a detailed description of the new hardware that was designed and fabricated to achieve the performance of the new wattmeter. It also describes the changes that were made to the hardware of the earlier wattmeter that was not completely replaced. Schematics and the operation of the circuits are given for the new hardware: the amplifier and current-converter module, amplifier and voltage-converter module, and the multiplier-accumulator board. Schematics and explanations are also given for the following changes in the old hardware: the direct-memory-access (DMA) board and the frequency counter and programmable time delay board. Section 4 describes the changes to the software that were necessary for control of the new wattmeter. Section 5 describes the performance of the new HASW based on the comparison of its power measurement readings with the NIST Audio Frequency Power Bridge [3].

2. System Operation

2.1. Power Sampling Basics

Periodic power signals with a voltage at time t of $v(t)$, a current of $i(t)$, and having a period of T seconds contain an average power, P, of

$$P = \frac{1}{T}\int_0^T v(t)\, i(t)\, dt \ . \tag{1}$$

Sampling wattmeters calculate the average power by performing the integration numerically, eq (2). The input voltage and current waveforms are sampled simultaneously, converted to digital values, and the product of their digital values, the instantaneous power, is calculated. The average power is computed by averaging many samples of instantaneous power. If the voltage at time t_k is denoted as $v(t_k)$ and the current as $i(t_k)$, then the approximate average power, W, is given by

$$P \approx W = \frac{1}{n}\sum_{k=0}^{n-1} v(t_k)\, i(t_k)\,, \tag{2}$$

where n is the number of samples used in the average. The major error in determining the power, W, comes from the limitations inherent in the sampling process, and the imperfections of the hardware used to make the measurements [4 to 7]. Section 5 discusses the errors due to limitations of the hardware.

2.2. General Operation

This Section presents a brief description of the principle blocks of the HASW, and how they perform the power measurement operations. Drawing 1 is a simplified block diagram of the HASW. The voltage and current signals are sampled and converted to 16-bit digital quantities in the two input modules. The input signals are also scaled to produce the two opto-isolated analog outputs, trigger 1 and trigger 2 signals. The two 16-bit digital samples are sent to the multiplier-accumulator and to the DMA circuit, and the two trigger signals are sent to the interval control circuitry. The interval control circuit synchronizes the summation period with the input signals and generates the sample command pulses that control the sampling rate. Although the summation interval is synchronized with the input signals, the sample command pulses are not. The sampling pulses are derived from a fixed, crystal-controlled oscillator, and their repetition rate can be selected by the front panel keyboard. The microcomputer controls the summation interval, reads the data from the multiplier-accumulator, calculates the average power, displays the results and the wattmeter parameters, and interfaces with the operator through the keyboard. The summation interval is controlled to preserve high accuracy independent of the input signal frequency and of the sampling rate.

The programmable delay circuit enables setting a time difference between the voltage- and current-sample command pulses. The delay compensates for the differences in response of the two input channels and preserves the sampling accuracy. The DMA circuit saves 4096 samples of the two input signals. These samples are used for calculating the average and rms voltage and current.

3. Hardware Changes[1]

This section describes the operation and the performance of the new hardware and the changes that were made to the existing hardware. It also provides schematics and explanations for the various circuits. The new hardware (Drawing 1) consists of the amplifier and the 16-bit voltage-converter module, the amplifier and the 16-bit current-converter module, and the multiplier-accumulator board. The existing hardware to which changes were made are the DMA board and the frequency counter and programmable time delay board. The modifications to the earlier two

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[1] This document reports on equipment developed at the National Institute of Standards and Technology. Certain commercial components are identified in order to adequately describe the design and operation of the equipment. Such identification does not imply recommendation or endorsement by the National Institute of Standards and Technology nor does it imply that the components are necessarily the best available for the purpose.

12-bit input modules to enable their use with the new HASW are also described. The last part of this Section discusses the efforts to reduce the induced noise and to improve the system performance, including the layout of the ground planes, the opto-isolation of the input module's front end, and the independent power supplies.

3.1. Amplifier and Conversion Modules

The current and voltage-input modules provide the interface and the impedance transformation for converting the analog voltage and current signals into 16-bit binary digital words. Drawing 2 shows the basic block diagram of the current-input module. Each of the modules includes a mother board, a plug-in A/D converter card and a plug-in clock-synchronizer card. Both modules have input voltage ranges of 255 V rms, 127 V rms, and 3 V rms ($\pm$4.5 V peak). The current-input module includes a two-stage current transformer and a current-to-voltage (I/V) converter card that give it additional current ranges of 5.5 A rms, 1.1 A rms, and 50 mA rms.

The voltage attenuators and the two-stage transformer and I/V converter card have an output signal in the range of $\pm$4.5 V peak. This signal is buffered with a unity-gain instrumentation amplifier. The output of the amplifier is connected to the A/D converter and to the opto-isolation amplifier. The isolated analog output is used to synchronize the sampling summation interval with the input signal (trigger 1 or trigger 2). Drawings 2, 3, and 4 show that the front end of the input module is opto-isolated from the main system. This feature reduces the noise introduced by any ground loop currents, enables the front end to float to the potential of the input power signals, and separates the noisy oscillator synchronizer circuit from the front end.

The plug-in A/D converter cards holds the A/D converter, the 4.5 V dc reference voltage, two DC/DC converters for $\pm$5 V dc, the data latch, and the circuitry for the delay and the strobe signals to the mother board. The plug-in clock-synchronizer card (Drawing 5) includes an oscillator and a synchronizing circuit. The clock-synchronizer provides the clock pulses to the A/D converter board. The synchronization circuit allows for the option of synchronizing the Hold command to the A/D converter with the rising edge of the clock signal, in response for each Sample (SMPL) command input initiated by the frequency counter and programmable time-delay board.

3.1.1. Voltage Inputs

The voltage-mode specifications for the voltage- and the current-input modules are the same. Table 1 gives a summary of the features for the voltage inputs.

Referring to Drawings 6 and 7, the calibration ($\pm$4.5 V peak) input is protected by a 1/16 A fuse because it is connected directly to the input of the instrumentation amplifier. The two other voltage inputs are not protected, assuming that the RC voltage attenuators at the input to the instrumentation amplifier, the 200 Ω resistor in series with the output of the instrumentation

amplifier, and the two limiting diodes across the input to the A/D converter provide sufficient protection.

Table 1 Voltage-Input Module Features

Input Range	Input Impedance
±4.5 V peak	$5 \times 10^{12}\ \Omega \| 6$ pF
127 V rms	100 kΩ‖10 pF
255 V rms	100 kΩ‖10 pF

3.1.1.1. The Attenuator

Each of the two voltage attenuators (Drawing 8), are resistor-capacitor (RC) dividers. The resistors of both voltage dividers were selected so that the input impedance of the attenuator is about 100 kΩ at dc. The resistors have a specified temperature coefficient of 10 (μΩ/Ω)/°C, the capacitors have a specified temperature coefficient of 30 (μF/F)/°C, and the adjustable capacitors are piston-air capacitors. The adjustable capacitors are used to give a flat response over the frequency range of interest. The capacitors are adjusted so that the wattmeter gives the same reading for a 4 kHz input voltage as for a 50 Hz input voltage.

3.1.1.2. Instrumentation Amplifier

The instrumentation amplifier (Drawing 8), U19, serves as a unity-gain buffer to drive the analog input of the A/D converter and the analog opto-isolated amplifier, U1. U19 was selected because of its good temperature stability, low noise, low offsets, high common-mode rejection ratio (CMRR) and high input impedance (noise = 0.3 μVpp, Vos = 0.05 mV, Ios = 10 nA, ΔVos = 0.5 μV/°C, CMRR = 120 dB, bandwidth = 1 MHz, differential input impedance = $5 \times 10^{12}\ \Omega \| 6$ pF, and common-mode input impedance = $2 \times 10^{12}\ \Omega \| 1$ pF). Even though the bandwidth of U19 is only 1 MHz, it is adequate for analog input signals in the 50 Hz to 1 kHz range.

For testing purposes, jumpers can be used to change the normal signal flow in the input modules. With various jumpers, the front-end signal can bypass the instrumentation amplifier, the input ground of the instrumentation amplifier can be connected or separated from its output ground, and the input to the A/D converter can be shorted to its input ground. For normal operation the front-end signal passes through the instrumentation amplifier, and the input and output ground of the amplifier are connected to the A/D analog ground. To enable offsetting the instrumentation amplifier, U19, from the front panel, a plastic rod connects the offset potentiometer's P1 setting screw to the front panel.

3.1.1.3. A/D Converter Cards

Two pairs of plug-in A/D converter cards (Drawings 6, 7) were fabricated. One pair uses ADC4203 A/D converters from Analogic, and the other pair uses CS5101 A/D converters from Crystal. The ADC4203's maximum sampling rate is 40 k samples per second while the CS5101 can be operated at up to 80 k samples per second. To enable the A/D converters to operate at their maximum sampling rates, the ADC4203 needs a 4 MHz clock and the CS5101 needs an 8 MHz clock. The plug-in clock-synchronizer card provides the clock pulses. For each A/D converter type, the appropriate crystal oscillator is plugged into the clock-synchronizer card. Each pair of converters uses the same input signals from the mother board and generate similar output signals (16-bit two's complement data and strobe signals). The analog input voltage to the A/D converters is protected by two clamping diodes D1 and D2.

The converter cards include: a ± 5 V power supply, a 4.5 V reference source for the A/D converters, and the circuitry needed for data latching and generating the strobe signals.

A. Timing Signals

The two timing signals to the A/D converter board, CLK and HOLD, are generated by the clock-synchronizer card (Drawing 5). By placing the clock-synchronizer card away from the A/D converter card and eliminating a common ground between these cards by opto-isolation, the clock noise induced on the input signal is reduced considerably. The falling edge of the Hold signal places the internal track-and-hold circuit of the A/D converter in the hold mode and initiates an analog-to-digital conversion cycle. The CLK signal is a TTL-level square wave signal. The signal is fed into the clock input of the A/D converter to synchronize its conversion cycle. The frequency of the CLK signal is determined by the crystal oscillator chip used (Drawing 5, U1). For the ADC4203 A/D converter, a 4 MHz oscillator is used. For the CS5101 A/D converter, an 8 MHz oscillator is used.

B. Output Data and Signals

The two output control signals from the A/D converter card, EOC-OUT and CLK1, (Drawings 6 and 7) indicate the end of a conversion cycle. On the rising edge of CLK1 the 16-bit data from the A/D board is latched into registers U7 and U8 on the mother-board. The rising edge of EOC-OUT signals the system that the data are ready to be read. The EOC-OUT signal and the data are passed to the system's multiplier-accumulator board via opto-isolators (U5, U9 to U17).

C. The 4.5 V DC Reference Source

The voltage reference circuit recommended by Crystal was implemented on the A/D converter boards. The value of the dc reference source (4.5 V) determines the maximum analog input signal level (± 4.5 V peak) and the scale of conversion. The dc reference-source output impedance and

regulation frequency response matches the power input impedance of the A/D converter. This impedance matching reduces the noise induced in the conversion from changes in power consumed by the A/D converter during the conversion cycle.

D. The CS5101 A/D Converter Card

The CS5101 converter (Drawing 7) clocks the 16-bit two's complement data serially (the most significant bit first and the least significant last) through the output SDATA during conversion. The output SCLK provides 16 synchronized pulses for latching the data. Two shift registers, U5 and U6 in cascade, provide a 16-bit shift register to collect and store the data for each conversion. The output SDATA is connected to the input of the shift register and output (SCLK) is connected to the clock input of the two shift register devices. After the data are stored in the 16-bit shift register, the output TRK1 goes from high to low, signaling the end of conversion and that the data are ready to be read. The output TRK1 is inverted and fed to the one-shot U4A. At the end of conversion, U4A provides the CLK1 and the EOC-OUT signals to latch the data into the registers on the mother board and to signal the multiplier-accumulator board that the data are ready to be read.

E. The ADC4203 A/D Converter Card

The ADC4203 A/D converter (Drawing 6) latches the 16-bit two's complement data into an internal tri-state buffered register. The outputs of the shift register, U6, provide the pulses for retrieving the data. The output EOC\ is connected to the input of U6 and the master clock signal, CLK, is connected to the clock input of U6. At the end of conversion, the output EOC\ goes from high to low for a period of about 24 master clock cycles. The output C0 of U6 is connected to the input RD\ to enable the internal register of the A/D converter. The outputs C3 and C6 provide for CLK1 and EOC-OUT output signals.

3.1.2. Current Inputs

Table 2 gives a summary of the features of the current-mode inputs available on the current-input module. All three current-input ranges are fuse protected. The input impedance of each of the three ranges is the resistance of the corresponding protection fuse measured at room temperature.

Table 2 Current-Input Module Features

Input Range	Input Impedance
50 mA	6.12 Ω (0.1 A fuse)
1.1 A	85 mΩ (1.5 A fuse)
5.5 A	34 mΩ (6 A fuse)

3.1.2.1. Two-Stage Input Transformer

The two-stage input transformer is used to scale down the input current to ±50 mA full scale. The output current of the transformer is fed into the I/V converter card. The use of a two-stage transformer [8] reduces the error introduced by scaling down the input current. The benefits of using an input transformer are the isolation that it provides and the ease of use by eliminating the need for a low-value, high-power shunt resistor. The disadvantage is that the module can not measure dc current. Drawing 9 shows the schematic representation, the equivalent circuit, the construction of the two-stage transformer, and some set-ups for measuring the two-stage transformer parameters.

Two identical torus-shaped cores with a square cross section (core one and core two) having the Magnetics model number AK026 50103-4F, and a torus-shaped magnetic shield box with a square cross section, made of a high-permeability material, were used for fabricating the two-stage transformer. Table 3 gives the dimensions of the components used to make the transformer.

Table 3 Dimensions of Transformer Components

	ID	OD	Height
Core	2.00" (50.8 mm)	3.00" (76.2 mm)	0.50" (1.27 mm)
Case	1.94" (49.3 mm)	3.13" (79.5 mm)	0.63" (1.60 mm)
Shield	1.38" (35.1 mm)	3.50" (88.9 mm)	0.75" (1.91 mm)

The tertiary winding (100 turns of a 16-gauge wire) and the cascade winding (one turn of a 20-gauge wire) were wound on core two, then core two was placed into a two-part magnetic shield. To eliminate the shield from forming a closed one-loop winding, the inner diameter of the two halves of the shield are isolated as indicated in Drawing 9 by a bigger gap. Core one was placed on top of the magnetic shield and the secondary winding (100 turns of 18-gauge wire) was wound around core one, core two, and the magnetic shield. The two primary windings were wound over the secondary winding. One primary winding is for the 5.5 A range (one turn formed from five turns wired in parallel), and the other is for the 1.1 A range (five turns of 14-gauge wire). The scale-down ratios of the 1.1A and the 5.5A input ranges are 20:1 and 100:1, respectively.

To confirm that the tertiary and the secondary windings both have the same number of turns, the two windings were connected in series to a source in a manner that their flux contributions cancel (Drawing 9). Because of the construction of the transformer (the windings of the secondary include the winding of the tertiary), the flux through the tertiary is very small when both windings

have the same number of turns. Therefore, a voltmeter connected across the tertiary should measure a small reading. By adding or subtracting one turn from the secondary, it can be verified whether the number of turns is equal.

To cascade the input transformer to an external two-stage transformer for increasing the range of the current to be measured, the secondary and the tertiary windings of the external transformer can be connected to the one-turn primary and to the one-turn cascade winding of the input transformer. Because the cascade winding is a one-turn winding, it can be combined only with the one-turn primary winding (range 5.5 A) of the input transformer. The magnetic shield is connected to the front panel through the connector labeled Trans. Guard. Grounding this connector reduces the capacitive coupling of common-mode signals to the wattmeter.

The two-stage transformer is connected such that the current to be scaled, I_p, is applied to the primary of the transformer and the scaled output current is the sum of the currents in the secondary, I_s, and the tertiary, I_t, windings. The scaling ratio ideally should be the ratio of the number of turns of the primary, N_p, to the number of turns of the secondary winding, N_s, which is equal to the number of turns of the tertiary winding, N_t. The scaling error of the two-stage transformer, ε, is the deviation of the ratio from this ideal. This error is given as

$$I_s + I_t = I_p \frac{N_p}{N_s}(1 - \varepsilon) \ . \tag{3}$$

The scaling error can be calculated by using the equivalent circuit [8] to calculate the sum of the secondary and tertiary currents. The sum is given as

$$I_s + I_t = I_p \frac{N_p}{N_s}(1 - \varepsilon_s \varepsilon_t) \ , \tag{4}$$

where ε_s and ε_t are the error if the secondary or the tertiary windings were used separately and are given by

$$\varepsilon_s = \frac{Z_s + Z_{b1}}{Z_{m1}} \ , \tag{5}$$

and

$$\varepsilon_t = \frac{Z_t + Z_{b2}}{Z_{m2}} \ . \tag{6}$$

Z_s and Z_t are the impedances of the secondary and tertiary windings, Z_{m1} and Z_{m2} are the magnetic impedances of core one and two, and Z_{b1} and Z_{b2} are the burden impedances for the secondary and tertiary windings. The magnetic impedances are described below.

It should be mentioned that the errors introduced by the various capacitances (between the

windings and the windings to the ground) and the eddy current were not considered. To take those errors into consideration a more elaborate equivalent circuit is needed.

From eqs (5) and (6) it is clear that the scaling error can be reduced by shorting the outputs of the secondary and the tertiary, reducing the winding resistances (the real part of Z_s and Z_t), and choosing cores that yield a high magnetic impedances (Z_{m1}, Z_{m2}) [8].

The magnetic impedance is a function of the core dimensions, the frequency, and the relative initial permeability and is given by

$$\frac{Z_m}{N^2} = \frac{4\,\pi\,10^{-7}\,\mu\,A\,\omega}{l}\,, \tag{7}$$

where Z_m is the magnetic impedance, N is the number of turns, μ is the initial permeability, A is the cross section of the core, ω is the input signal frequency, and l is the mean path length of the magnetic flux inside the core. Assuming the relative initial permeability, μ, is 6×10^4, the input signal frequency, ω, is 60 Hz, and the number of turns, N, is 100, then by eq (7) the calculated magnetic impedances of the two-stage input transformer, Z_{m1} and Z_{m2}, are about 200 Ω. After fabrication, the resistances of the windings and the magnetic impedances of the transformer were measured for frequencies of 50 Hz, 1 kHz and 10 kHz and the measured values are about two times the calculated values. The dc resistance of the secondary is about 0.3 Ω and that of the tertiary is about 0.1 Ω. The measured impedance values and scaling errors are shown in Drawing 9 and summarized in Table 4.

As can be seen from Table 4, the scaling errors caused by the winding resistance are negligible. For 1 kHz and higher frequencies, the errors caused by the stray capacitances and the eddy current are probably dominant and much more than those caused by the winding's impedance.

Table 4 Magnetic Impedances and Scaling Error

Freq. (Hz)	Z_{m1} (Ohms)	Z_{m2} (Ohms)	Scaling Error (parts in 10^6)
50	450	433	0.2
1 k	2.5 k	2.5 k	negligible
10 k	12 k	12.5 k	negligible

3.1.2.2. I/V Card

A schematic of the current-to-voltage (I/V) converter circuit is shown in Drawing 10. The basic I/V circuit, shown in Figure 1, consists of the feedback resistor and capacitor, R_f and C_f,

a compound amplifier (identical amplifiers A1 and A2), the resistive attenuator R_1 and R_2, and the RC attenuator R_a and C_a. The resistive attenuator is necessary to prevent oscillations and its attenuation should be set to the lowest possible ratio that gives a minimum reduction in the compound amplifier's gain, as explained below.

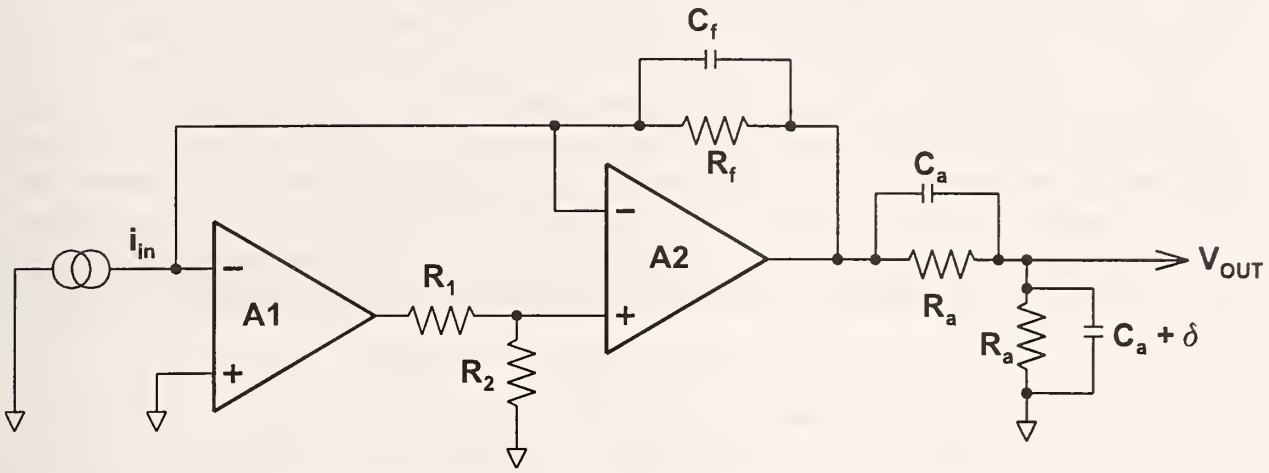


Figure 1 Simplified Diagram of Current-to-Voltage Converter.

The transfer function G of the I/V converter relates the output voltage, V_{out}, to the input current, I_{in}, as $V_{out} = G\, I_{in}$. An approximation of G is given by

$$G \approx -\frac{1}{1 + j\,\omega\, R_f\, C_f}\, R_f\, \frac{1 + j\,\dfrac{\omega}{\omega_t\,\rho}}{1 - \dfrac{1}{\rho}\left(\dfrac{\omega}{\omega_t}\right)^2 + j\,\dfrac{\omega}{\omega_t\,\rho}}\, \frac{(1 - j\ 0.5\ \omega\, R_a\, \delta)}{2}\,, \tag{8}$$

where ω is the input signal frequency, ω_t is the unity gain frequency of A1 and A2, δ is the incremental capacitance added to the lower portion of the RC attenuator, R_a and C_a are the values of the upper and the lower portions of the RC attenuator, and ρ is given by

$$\rho = \frac{R_2}{R_1 + R_2}\,. \tag{9}$$

The approximation for G is valid provided that ω, δ, and ρ are such that

$$(\omega\, R_a\, C_a)^2 \ll 1\,, \qquad \delta \ll C_a\,, \qquad \text{and} \qquad \frac{1}{\rho}\left(\frac{\omega}{\omega_t}\right)^2 \ll 1\,. \tag{10}$$

The first factor of the expression for G represents the effects of the feedback capacitor, C_f. The second factor describes the effects of the finite bandwidth, ω_t, of the amplifiers A1 and A2 and

the resistive attenuator, R_1 and R_2. In the frequency range that satisfies the third inequality in eq (10), the denominator and numerator of this factor cancel each other and the response from this factor is very close to the dc gain, which is R_f. The third inequality of eq (10) also indicates that the frequency range for a flat response increases as the value of the divider ratio, ρ, goes higher. For the HASW design, ρ was set to the value of 0.001. The third factor of the expression for G represents the effect of unbalancing the RC voltage divider by adding a small capacitance, δ, in parallel to its lower portion (small meaning that the second inequality of eq (10) is satisfied). The first and third factors show that C_f and δ produce very similar effects on the transfer function; thus, either approach can be used to adjust the time delay of the circuit. Since the RC voltage attenuator is a part of both the current and voltage sections of the current-input module, the method used for the HASW was to use the feedback capacitor, C_f, to adjust the time delay of the current inputs and the RC voltage attenuator to adjust the time delay of the voltage inputs. It was found experimentally that the overall response of the HASW is best if C_f is set to 15.9 nF.

3.1.3. Clock-Synchronizer Card

The clock-synchronizer card (Drawing 5) supplies the A/D converter with the master clock pulses. By plugging the proper oscillator into the card, it supplies a 4 MHz clock to the A/D board with the ADC4203 converter or 8 MHz to the A/D converter with the CS5101 converter. The other function of the board is to synchronize the input sample (SMPL) command from the frequency counter and the programmable time-delay board with the master clock. When jumper JM3-4 is set for the synchronizing (SYNC) mode, for each SMPL command a synchronized positive HOLD pulse is emitted, signaling the A/D converter to start a conversion. The resolutions of the A/D converters are verified for the SYNC and the unsynchronized (DIR) modes. Both A/Ds converters produce a smaller spread in the codes under the DIR mode. For that reason the board is set to the DIR mode.

The clock-synchronizer board is plugged into the lower side of the mother board. It is thus shielded from the A/D converter by the systems ground plane, as part of the efforts to minimize the induced noise to the analog-to-digital conversion portion of the input modules. To eliminate more noise induced by the oscillator, this board's ground is separated from the A/D converter board's ground, and the master clock and the HOLD command are transferred to the mother board via opto-couplers.

3.1.4. Scale Factors

The analog input voltages or currents are transformed into a voltage, V_{in}, which is applied to the A/D converter for conversion to a corresponding digital word. Each voltage input has a particular gain, G_v, and each input current has its particular transconductance, G. The 16-bit number N is the digital value of V_{in} scaled to the reference voltage, V_{ref}, by the A/D converter. For numerical calculation, N has to be multiplied by a scale factor, S, to determine the value of the

analog input signal. The input current, I_{in}, is given by $I_{in} = S_i N$ and the input voltage, V_{in}, is given by $V_{in} = S_v N$. For the HASW the approximate scale factors in terms of the least significant bit (lsb) of the converter are given by

$$S_v = \frac{V_{ref}}{2^{n-1}} \frac{1}{G_v} \approx \frac{4.5}{2^{15}} \frac{1}{G_v} , \tag{11}$$

and

$$S_i = \frac{V_{ref}}{2^{n-1}} \frac{1}{G_i} \approx \frac{4.5}{2^{15}} \frac{1}{G_i} . \tag{12}$$

The approximate scale factors for the various ranges are given in Table 5.

Table 5 The Approximate Scale Factors

Input Range	Approximate Scale Factor
Voltage Cal., 4.5 V	137.5 μV/lsb
127 V	5.488 mV/lsb
255 V	10.985 mV/lsb
Current Cal., 50 mA	2.29 μA/lsb
1.1 A	45.8 μA/lsb
5.5 A	229 μA/lsb

3.2. Multiplier-Accumulator Board

The multiplier-accumulator board multiplies the digitized current and voltage values and sums the resultant products. At the end of the hardware accumulation period, the sum is stored in a latch and an interrupt is sent to the microcomputer. Drawing 11 shows a general block diagram of the multiplier-accumulator board and Drawing 12 shows a second block diagram with more details of the sequencer, which controls the operation of the multiplier-accumulator, and additional details of the extended accumulator. The circuits are shown in Drawings 13, and 14. The hardware accumulation period is controlled by the terminal count, TC, signal produced by the frequency counter and programmable time-delay board. The multiplying and summing of the sampled data is controlled by the pulses generated by the sequencer. The arithmetic operations are carried out in a high-speed multiplier-accumulator (LSI device TDC1010J). This device contains a 16-bit by 16-bit multiplier, a 35-bit accumulator, and an internal latch.

The multiplier-accumulator board has four modes of operation. The mode controls which data are multiplied and summed on the board. Depending on the mode, the board accumulates either power products, voltage values, current values, or sample counts. The operation of the sequencer, the extended accumulator, and other support circuitry on the multiplier-accumulator board are described in the following sections.

3.2.1. The Sequencer

The sequencer controls the operation of the multiplier-accumulator board by generating a series or cycle of pulses after receiving a start sequence pulse, SEQ, from the end-of-conversion combiner circuit. The sequencer produces three different pulse cycles, depending on the terminal count (TC) pulse from the frequency counter and programmable time-delay board. The initial cycle starts the hardware accumulation period by clearing the accumulator, R3 (Drawing 12), and latching into it the first product of the sampled data of the new accumulation period. The normal cycles that follow each of the next data conversions add the product of the sampled data to the accumulator, R3. Upon receipt of the TC pulse, the sequencer generates the terminal cycle that adds the last product of the hardware accumulation period into the accumulator, R3, latches the accumulator data into the buffer register, R7, and sends an interrupt to the microcomputer. The sequencer starts the next hardware accumulation period at the next data conversion by generating the initial cycle pulses.

The timing diagram (Drawing 15) of the sequencer shows three cycles, the first one is the last normal cycle (designated by N-1) of a hardware accumulation period, the second (designated by N) is a terminal cycle and the third one is the initial cycle (designated by 1) of the next accumulation period. As can be seen, for every cycle the train of pulses, C0 to C11, are initiated by the SEQ signal. The TC signal, together with the CEOC signal, control the initiation of a terminal cycle followed by an initial cycle of the next hardware accumulation period. The differences between the three different cycles is related to the control signals LTC, ACC, TSL, and the conditional signals, CCn, that are also produced by the sequencer. The LTC signal is derived from TC and CEOC signals and it controls the terminal cycle by enabling the various conditional pulses CCn that latch the data accumulated during the hardware accumulation period into the buffer register, R7, which is accessible by the microcomputer. The ACC signal is initiated by the falling edge of the LTC signal, and by going low, it enables the initial cycle to clear the accumulator, R3. The TSL signal controls data multiplexing of the common outputs of the least significant product (LSP) buffer and register R5. This multiplexing enables either the output data of register R5 to be latched into register R2 or enables the data in the accumulator, R3, to be latched into the buffer register, R7.

Two shift registers connected in series, R8, that are clocked by an 8 MHz oscillator, are used to generate the positive pulse train, C0-C11. Each of the Cn pulses has a duration of 250 ns and the time difference between the rising edge of each successive pulses is 125 ns. The CCn (conditional) pulses, which are derived from the Cn series, are generated only during the terminal cycle for

latching the content of the accumulator, R3, into the buffer register, R7, (multiplier-accumulator output data latch).

3.2.2. The Extended Accumulator

The internal accumulator, R3 (Drawing 12), of the multiplier-accumulator device TDC1010J is 35 bits wide. It can only accumulate the sum of sixteen 16-bit by 16-bit products when each multiplicand has the maximum value in two's complement notation before overflowing. To overcome this limitation an accumulator extension was added. To implement the extension, it is necessary to detect the overflows and the underflows of the accumulator, R3, and to increment or decrement accordingly an external binary counter. An overflow is characterized by the transition from high to low of the two most significant bits (P33, P34) of R3 and an underflow is characterized by the transition from low to high of the same bits. The two D flip flops, U21A and U21B, hold the previous values of bits P33 and P34. By connecting the outputs of U21A and U21B, and the inverse of bits P33 and P34 into the input of the NAND gate, U23A, its output will switch from high to low when an overflow of R3 occurs. Similarly, by connecting the inverted outputs of the D flip flops, U21A and U21B, and the bits, P33 and P34, to the input of U23B, its output will switch from high to low when an underflow of R3 occurs. U24, U25, and U26 are three 4-bit up/down binary counters cascaded together to form a 12-bit binary counter. The counter is enabled whenever an underflow or overflow occurs by connecting the output of the NAND gate U31B to the ENT and ENP inputs of the first counter, U24. The U/D input of all the counters is connected to the output of the NAND gate, U23B, thus counting up when an overflow occurs and counting down when an underflow occurs. The count-up or down occurs on the rising edge of the C7 pulse of the sequencer. At the beginning of each hardware accumulation period, the sign of R3 has to be transferred to the extension. To accomplish this, all the data inputs of the three counters are connected together through NAND gate buffer, U31C, to the MS bit, P34 of R3. During the first cycle of every hardware accumulation period the ACC signal is low, thus enabling storing the product in R3, and also loading the value of bit P34 into the extension counters on the rising edge of the C7 pulse. To get the right values, the extension should never overflow or underflow. Adding 12 bits to the accumulator, R3, brings the total capacity to 47 bits and that enables it to sum at least 65,536 16-bit by 16-bit products without overflow or underflow.

3.2.3. End-of-Conversion Combiner Circuit

The end-of-conversion (EOC) combiner circuit (Drawing 16) enables the use of two different input modules with different A/D conversion times. When a sequence of a sample SMPL command followed by an end-of-conversion (EOC) signal from each input module are detected by this circuit, it sends the output signals, SEQ and CEOC, to the sequencer circuit, and the DMA-EOC signal to the DMA board, to indicate that a pair of 16-bit sampled data are ready.

3.2.4. Interface with Microcomputer

At the end of each hardware accumulation period the buffer register, R7, of the multiplier-accumulator board (Drawing 12) interrupts the microcomputer to retrieve its contents, which is a 47-bit two's complement number. These data are stored in six 8-bit registers (five AM25LS2520 and one 8212). Since the data bus is 8 bits wide, the microcomputer must address R7 six times, and reconstruct the data based on the retrieved byte's addresses. To change the mode of operation of the multiplier-accumulator board, the microcomputer writes the new mode byte into the mode-latch register, R6. Table 6 summarizes the addresses of registers R6 and R7. The addresses of the registers comprising R7 are listed from the least significant byte (LSB) to the most significant byte (MSB).

Table 6 Addresses for Buffer Register, R7 and Mode-Latch Register, R6

Register R7 Read Address	Component Drawing 13
0E0 Hex LSB	U20
0E2 Hex	U19
0E4 Hex	U18
0E6 Hex	U17
0E8 Hex	U28
0EA Hex MSB	U27
Register R6 Write Address	**Component Drawing 13**
0E4 Hex	U5

3.2.5. Mode Control

The multiplier-accumulator board (Drawings 12, 13) can operate in four modes designated 0, 1, 2, and 3. The mode controls which data are latched into registers R4 and R5 on the rising edge of the C0 pulse at the beginning of each multiply accumulation cycle. Table 7 summarizes the values of the data that are latched into R4 and R5 for each mode. For power measurement the system uses mode 0, which is the default mode when the system is powered up. The mode can be changed by the front panel keyboard. When the system detects a mode-change request, an 8-bit word is written into register R6.

Table 7 Mode Summary

Mode	R4 latched data	R5 latched data
0	16-bit channel 1 data	16-bit channel 2 data
1	Numerical value 1	16-bit channel 2 data
2	16-bit channel 1 data	Numerical value 1
3	Numerical value 1	Numerical value 1

The quantity measured depends on the mode of the multiplier-accumulator board. For mode 0 the output reading is power; for mode 1 the output is the average of the channel two signal level; for mode 2 the output is the average of the channel one signal level. For mode 3 the output is the numerical value 1, which indicates that the frequency counter and programmable time delay board is measuring the same number of samples during each multiply and accumulation period as the multiplier-accumulator board. Modes 1 and 2 are used to measure the offsets of the input modules.

3.3. Noise Considerations

In this section, some design features of the system that are associated with the effort to reduce noise will be addressed: the ground planes, opto-isolation, and power supplies.

3.3.1. Grounding

There are six principle ground planes in the HASW system (Drawings 4, 17, and 18). Five of them follow the main blocks of the system: the microcomputer, the voltage-module digital circuitry, the voltage-module analog circuitry, current-input-module digital circuitry, and the current-input module analog circuitry. The sixth ground is the chassis ground. Some grounds are connected together at selected locations to reduce noise.

The six ground planes are referenced by the following names:

a. The chassis ground (CHS GND).
b. The system ground plane (SYS GND).
c. The voltage-input module digital ground plane (DGTL GND).
d. The voltage-input module analog ground plane (ANLG GND).
e. The current-input module digital ground plane (DGTL GND).
f. The current-input module analog ground plane (ANLG GND).

The CHS GND consist of the cabinet and the case of all the assemblies that are located within it.

This ground is connected to the ground pin of the power plug. The SYS GND is the ground plane of the microcomputer mother board and the plug-in boards (Drawing 18). The SYS GND and the CHS GND are connected together at the point where the microcomputer power supply crate is attached to the cabinet. Each of the input modules include three ground planes, the ANLG GND, and the DGTL GND of that module, and the SYS GND. All the input module components that are powered from the main system share the SYS GND. The DGTL GND and the ANLG GND of each input module are isolated from the CHS GND and from the SYS GND. The DGTL GND and ANLG GND of each module are isolated from the DGTL GND and ANLG GND of the other module. This isolation is achieved by using separate linear power supplies for each module (Drawing 4). The DGTL GND and the ANLG GND of each input module are connected together at one point on the back of the plug-in A/D converter card through jumper JP3 (Drawings 6 and 7). Using one point of connection is done to minimize the induced noise from the digital circuitry into the analog circuitry and particularly into the analog section of the A/D converter.

3.3.2. Optical Isolation

The two dotted lines through the opto-isolators, shown on the input module block-diagram (Drawing 3), indicates the boundary between the isolated analog front-end of the input module and the digital circuitry that interfaces directly with the microcomputer system. The opto-isolators, while transferring the digital and the analog signals, serve as high-impedance isolators that reduce the ground-loop currents. Another benefit of the opto-isolation is the convenience in use of the HASW due to the ability of the front-end input modules to float at the potential of the monitored system. The maximum allowable voltage difference between the front end and the system ground is 500 V.

3.3.3. Power Supplies

Every power supply common is connected to, and thus associated with, a ground plane (Drawings 4, 18).

The $\pm$15 V SYS AC/DC converter common is connected to the SYS GND and supplies power to the system side of the opto-isolated analog amplifier U1.

The +5 V SYS AC/DC converter common is connected to the SYS GND and it supplies power to

1. the EOC one-shot and associated components,
2. the clock-synchronizer card, and
3. the system side of the opto-isolators.

For each input module, the common of a $\pm$15 V ANLG AC/DC converter is connected to the ANLG GND of the input module and it supplies power to

1. the instrumentation amplifier, U3,

2. the current-to-voltage converter card (only on the current-input module),
3. the isolated input of the opto-isolated analog amplifier, U1, and
4. the A/D converter card.

For each input module, the common of a ±5 V DGTL AC/DC converter is connected to the DGTL GND of the input module and it supplies power to

1. the data latch, R2,
2. the isolated-input front-end side of the opto-isolators, and
3. the digital circuits on the A/D converter card (the data latch R1, and the time delay and associated components).

The use of separate power supplies for the analog and the digital circuits of each of the input modules serves to reduce the noise induced onto the analog input signal and into the analog section of the A/D converter.

3.4. Other Hardware Changes

3.4.1. 12-bit Input Modules

Two changes were needed to allow the previous 12-bit input modules to operate in the 16-bit environment. The first was to change the A/D converter output data into a 16-bit integer. The second was to change the 12-bit two's complement integer into a 16-bit integer by connecting the most significant bit (of the 12-bit integer) to the five edge-connector pins corresponding to the five upper bits of the 16-bit integer.

3.4.2. DMA Board

The DMA board was originally built to accommodate 16-bit integers, except that its four most significant bits were connected together to accommodate the older 12-bit modules. The only change necessary was connecting each of those four bits separately to the 60-pin edge connector.

3.4.3. Frequency Counter and Programmable Time-Delay Board

The frequency counter and programmable time-delay board (Drawings 19, 20) provides the Sample SMPL command pulses to the two input modules. To allow for differential time delays between these modules, the two pulses can be shifted relative to each other. Previously, the board could shift the channel-one sample command -60 ns to 200 ns relative to the channel-two sample command. This range was sufficient for the 12-bit input modules but not for the new 16-bit modules. The new modules require a relative time shift of about 800 ns. To achieve this longer delay, an additional programmable delay was introduced ahead of the two output programmable-delay components, PTTL-DL60-1 and PTTL-DL15-16, which were already implemented on the board. The output of the D flip flop, U9A, is connected to the input of the shift register, U39.

A 6 MHz clock is connected to the clock input of U39. The delay between consecutive outputs of the shift register is thus 166.6 ns. The outputs of the shift register are connected to the inputs of the multiplexer, U40. By setting switch SW2, a delay between 166.6 ns to 1333.3 ns can be selected. The table in Drawing 19 summarizes the switch, SW2, setups for the different delays and how to select the two channels.

4. Software Changes

The software in the HASW is a minor revision of the previous software used in the Wideband Sampling Wattmeter. This earlier software is extensively described in an NBS Technical Note [2]. The software description here will highlight the changes made in the two upgrades that have occurred to the software since that description. The first upgrade was to accommodate the addition of an IEEE 488 interface to the earlier wattmeter and the change in microcomputer used to control the wattmeter. The second software upgrade was the one made to accommodate the changes made for the HASW upgrade. The software is written in a combination of Pascal and assembly language. The assembly language software provides the interface to the hardware for the Pascal routines. Assembly routines are used to set and read the hardware registers and to respond to the interrupts. The Pascal routines provide the main control software of the wattmeter.

4.1. Software Changes for IEEE 488 Interface

The IEEE 488 interface is provided by the ZT 85/38 Multibus to IEEE 488 interface card from Ziatek Corp. The IEEE 488 address of this board is set via a dip switch on this board. Assembly language routines initialize and interface with this board, and Pascal routines read commands sent to the wattmeter and respond with wattmeter data and status.

As part of this general software upgrade, additional measurement capabilities were added to the earlier wattmeter, including direct access to the DMA contents as well as four additional measurement functions. Two arrays of the measurement values saved in the DMA can be sent on the IEEE 488 interface to an attached computer for further analysis. The number of values sent can be selected to be from 1 to 4096. The new measurement functions are energy, energy count, and clip count for channel 1 and channel 2. A new parameter was added in connection with the energy function, the clock correction factor. This factor corrects for the error in the frequency of the crystal that controls the sampling rate. The energy is displayed in Joules and the energy count gives the number of samples used in the currently displayed energy measurement. The two clip counts give the number of DMA stored values, which are at either the positive or negative saturation level. If these counts are not zero, then the measurement results are in error due to amplitude clipping of the input signals by the analog-to-digital converters.

The way many operational parameters are set via the software has been modified to make the control of the wattmeter easier. These modifications include the way the scale factors and delay times are

set for the two channels and the way functions are displayed on the wattmeter display. Also, new parameters have been added to control the way measurement data are sent over the IEEE 488 interface.

Table 8 IEEE 488 Commands

Char	Function
A	Up (↑)
B	Down (↓)
C	Left (←)
D	Right (→)
E	Home
F	Run
G	FUp (F↑)
H	FDown (F↓)
I	na
J	na
K	DumpAr1
L	DumpAr2
M	ResetE
P	FullReset
Q	na
R	na
S	(488Sing)
T	na
V	na
W	na

Char	Function
a	na
b	(Ar2End)
c	(MCh1SF)
d	na
e	(Ar2End)
f	(SampFreq)
g	na
h	na
i	(IntgPer)
j	(Ar1Beg)
k	(Ar1End)
l	na
m	(DispP)
p	na
q	(488Cont)
r	(ShuntR)
s	(Send488)
t	(TrigLev)
v	(MCh2SF)
w	(Source)

Char	Function
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
0	0
.	.(Dec)
CR	
LF	

The following discussion describes the commands that can be sent over the IEEE 488 interface bus to control the wattmeter. The control is similar to the way the wattmeter is controlled via the

24-button keyboard on the front panel of the wattmeter. Table 8 gives the function of each alphanumeric character sent over the IEEE 488 interface bus. Characters with a function "na" have no affect, those marked in a box have the same affect as the corresponding ones entered from the keyboard, and those with functions in parentheses control the state of the software as described below.

Table 9 Selection Menu and Default Values

Top of List		
Sample Pulse	Sample Freq.	300 kHz
	Pulse Width	1.00 μs
	Conv Cmd Delay	0 ns
	Clock Cor	1097 μs/s
Synchronization	Multiplexer	4.68 kHz
	Trigger Level	0.0 V
	Trigger Delay	1 sample
Integration	Hardware Accum.	
	MA Mode	Power
Scale Factor	Shunt Res	1.0
	Ch 1 Scale Factors	(12 Chan 1 SF's)
	Ch 1 Delays	(12 Chan 1 Delays)
	Ch 2 Scale Factors	(12 Chan 2 SF's)
	Ch 2 Delays	(12 Chan 2 Delays)
Display	Display Delay	1000 ms
	Display Ix	(10 Disp Func)
DMA Param	DMA Trigger	TC
	DMA Truncation	None
	DMA Ave	(Blank)
Set Array Lim	Array 1 Beg	0 loc
	Array 1 End	5 loc
	Array 2 Beginning	4096 loc
	Array 2 End	4101 loc
Set 488	Ix=Disp x	(20 Disp Func)
Set State		(See text)

The wattmeter parameters are set by changing the state of the wattmeter and entering the appropriate data for the current state. From the front-panel keyboard the current state can be determined by observing the 32-character display and using the arrow keys to change the state. Table 9 shows the display messages, the sequence of state selections and the default values of the corresponding parameters. Up, Down arrows move from top to bottom in Table 9 and Left, Right arrows move between columns. The list wraps at the top and bottom, i.e., an Up arrow at "Top of List" moves to "Set State" and a Down arrow at "Set State" moves to "Top of List."

The wattmeter state also can be set via the IEEE 488 interface by using the same sequence of commands. The command "E" sets the state to the "Top of List" state. Then, a sequence of arrow commands ("A", "B", "C", or "D") will change the wattmeter state to the desired parameter entry. The parameter value can be changed by entering the proper numeric value or using additional arrow entries, as is appropriate for the specific parameter. A quicker method of changing to some states is to first send the "EA" command, which changes the wattmeter to the "Set State" state. The next character changes the wattmeter to the state given in parentheses in Table 8. As an example, in Table 8, the lower case letter "c" is next to the function MCh1SF, which means to modify the channel 1 scale factors. Thus, to change to the state for modifying the channel 1 scale factors, the command "EAc" is sent.

There are two formats for data transferred from the wattmeter via the IEEE 488 interface. The first format is used for the data dumped from the wattmeter display. These data are sent as a string of 32 characters followed by a CR and LF. Since these data are first written to the display, it can be seen during the transmit process. The second format is used for the hex data from the two DMA arrays. These data are sent as a string of 29 characters followed by a CR and LF. Each of these strings contains the data for six array locations. Each location is represented as four hex characters followed by a space. The hex code used is 0 to 9 for the first 10 numbers and :, ;, <, =, >, and ? for A, B, C, D, E, and F respectively.

The wattmeter originally was controlled by an 8086 microprocessor on an Intel SDK-86 computer board. As part of the upgrade to add the IEEE 488 interface to the wattmeter, the control was changed to an Intel 86/12A Multibus microcomputer, which also contains an 8086 microprocessor. This change required the re-addressing of the programmable peripheral interface (PPI) device and the interrupt handler device.

4.2. Software Changes for HASW Upgrade

The software upgrade for the changes to convert the Wideband Sampling Wattmeter to the HASW involved the differences with the new multiplier-accumulator board. The multiplier-accumulator, (MA) mode setting is accommodated as is the reading of the larger hardware accumulator, 47 bits vs 35 bits. Also, the allocation of time between the number of hardware accumulations and the number of software accumulations is changed. Depending on the MA mode, the wattmeter calculates and displays the input power, the average of the channel 1 inputs, the average of the

channel 2 inputs, or the ratio of the number of samples counted by the frequency control and programmable time delay board and the number of samples counted by the multiplier-accumulator board. This last measurement should always be the numerical value 1 for a properly operating wattmeter.

5. Performance

The critical factors that are of interest for the performance of the HASW are the noise level, frequency response, and temperature coefficients of the input circuitry. The noise levels of the input circuitry were measured by applying a constant dc signal or a short circuit to the voltage- and current-input modules and then recording the range of digital codes generated by the modules. The final design achieved an approximate noise level of plus/minus one code width. The data shows about 60 percent of the output at one code, 15 percent to 25 percent at each of the adjacent codes, and 1 to 2 percent at plus and minus two codes. Figure 2 shows a typical distribution of codes for 100 samples of the voltage-input module with the input terminal shorted. Similar results are observed for the current-input module.

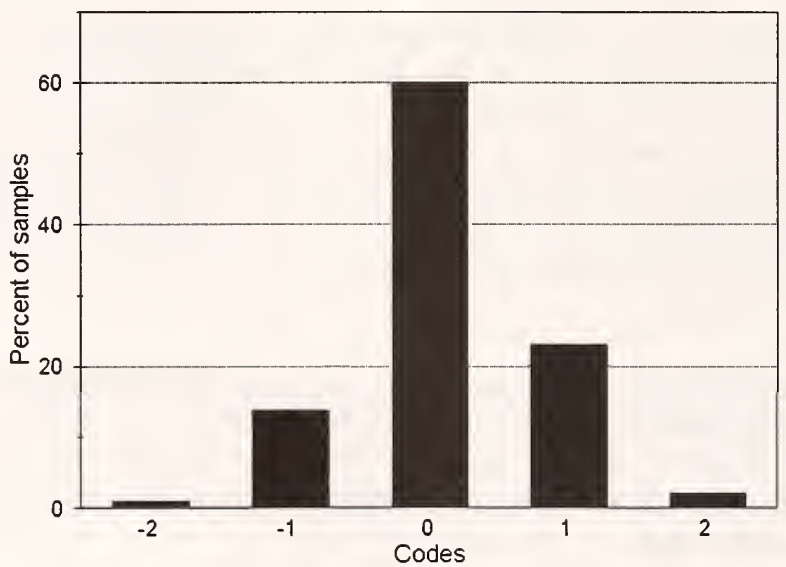


Figure 2 Typical Distribution of Voltage Codes for Shorted Input.

The frequency response of the two input modules was determined using sine waves from a standard commercial calibrator, and using an ac/dc thermal voltage-converter comparator to measure the amplitude of the test signals. Figure 3 shows the frequency response of the current-input module and Figure 4 shows the frequency response of the voltage-input module. The frequency response of the 255 V range is marginal for achieving the project goal of an uncertainty less than ± 50 μW/W of full scale. Attempts will be made to reduce the errors for this input range

by redesigning the attenuator for this range. The other ranges have errors that are well within the uncertainty goal.

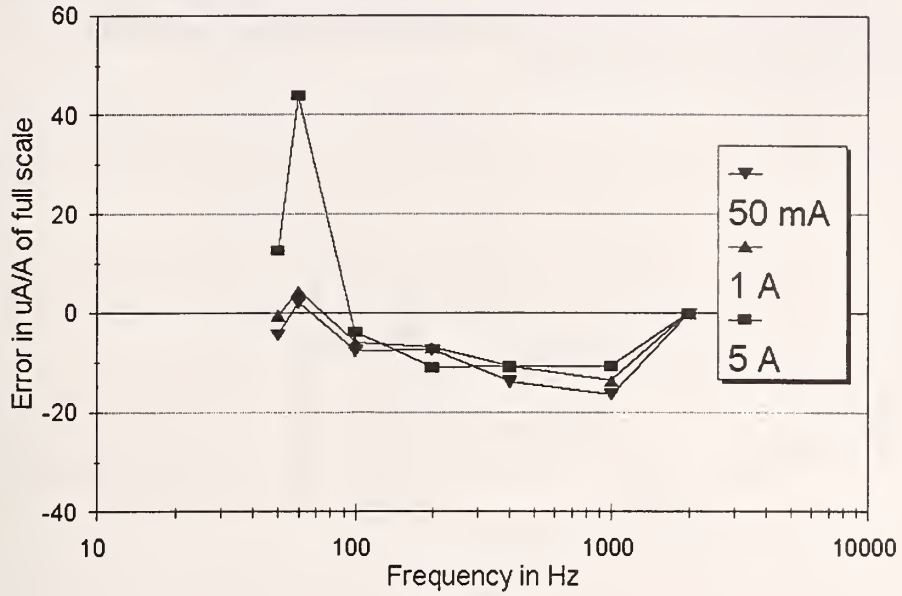


Figure 3 Frequency Response of Current-Input Module.

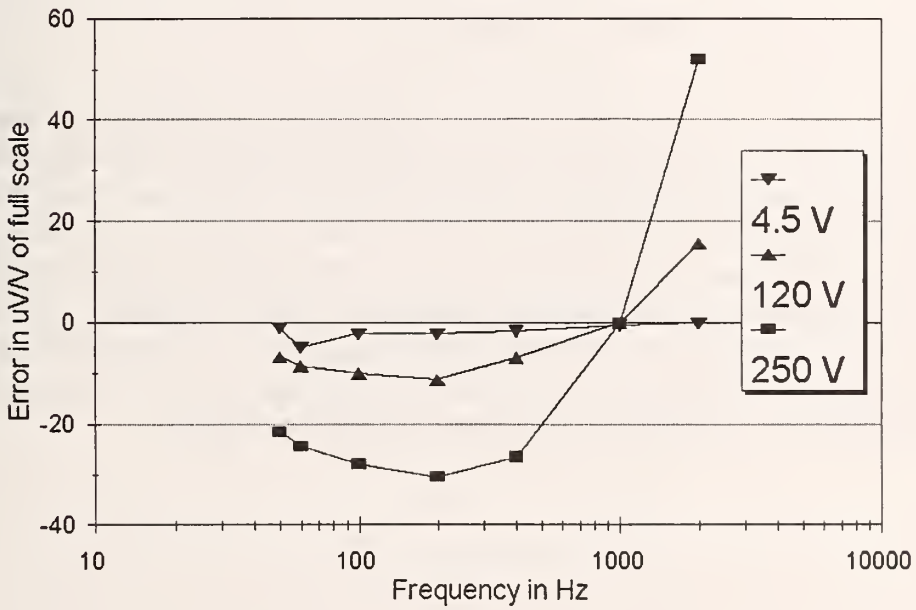


Figure 4 Frequency Response of Voltage-Input Module.

The power frequency response was measured using the NIST Audio-Frequency Power Bridge [3]. Figure 5 shows the typical results for calibration of the HASW for power measurements. This graph shows the power errors for unity and zero power-factor lead and lag signals with voltage and current amplitudes of 120 V and 1 A. These results show that the power uncertainty goal of less than ± 50 μW/W of full scale range was achieved.

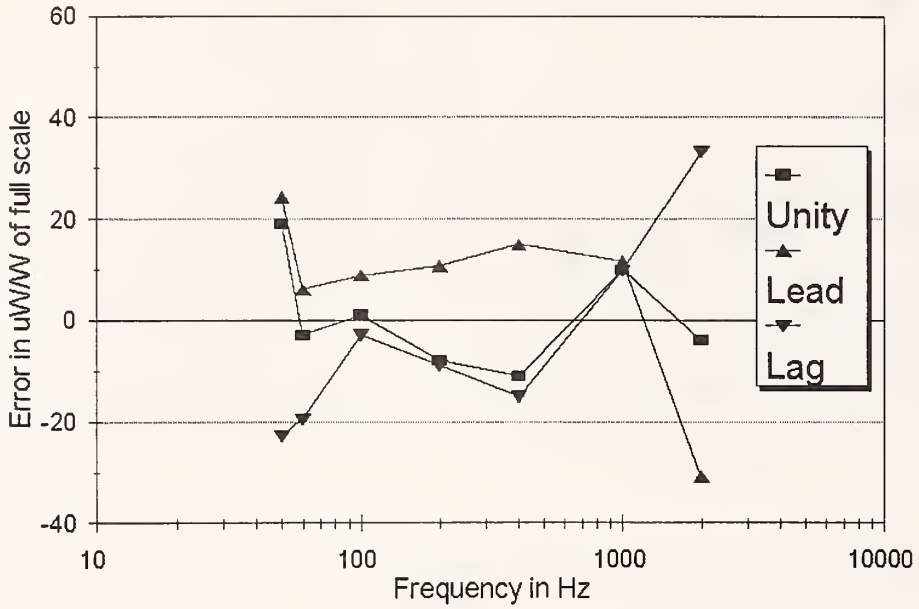


Figure 5 Frequency Response of Power Measurements.

The temperature sensitivities of the two input modules were measured for a temperature change of about 25 °C, from 10 °C to 35 °C. Table 10 shows the results of these tests. The first three rows are the results obtained for the voltage-input module and the last two rows show the results obtained for the current-input module. The temperature sensitivities range up to 2.6 parts in 10^6/°C for the voltage-input module and up to 3.6 parts in 10^6/°C for the current-input module. Based on these data, the expected power temperature sensitivity is about 5 parts in 10^6/°C. However, each of the module sensitivities were measured independently, so no information was obtained to determine the temperature sensitivity of the phase of each module. Thus, the power sensitivity may be significantly larger, particularly for low power-factor signals.

Table 10 Temperature Sensitivities for the Input Modules in parts in 10^6/°C

Range	50 Hz	400 Hz	1 kHz
3 V	0.9	2.6	2.6
120 V	2.1	2.3	-1.3
240 V	0.4	1.1	1.6
1 A	2.5	2.5	2.9
5 A	3.6	3.2	2.9

Acknowledgments

The authors gratefully acknowledge the assistance of T. Michael Souders with the design of the two-stage current-transformer, the help of Owen B. Laug with the design of the input circuitry, the aid of Nile M. Oldham in solving several calibration problems, the assistance of Bryan C. Waltrip and Mark Parker with performing power calibrations, the help of Robert Palm in preparing the drawings and the editorial support and review provided by Barry A. Bell.

References

[1] G.N. Stenbakken, "A Wideband Sampling Wattmeter," *IEEE Trans. Power Appar. Syst.,* PAS-103, pp. 2919-2926, Oct. 1984.

[2] G.N. Stenbakken, O.B. Laug, T.H. Kibalo, B.A. Bell, and A.G. Perrey, "NBS Wideband Sampling Wattmeter," NBS Technical Note 1221, (U.S. Government Printing Office, Washington, DC, May 1987).

[3] B.C. Waltrip and N.M. Oldham, "Performance Evaluation of a New Audio-Frequency Power Bridge," *IEEE Trans. Instrum. Meas.,* IM-40, pp. 380-383, Apr. 1991.

[4] R.S. Turgel, "Digital Wattmeter Using a Sampling Method," *IEEE Trans. Instrum. Meas.,* IM-23, Dec. 1974.

[5] M.F. Matouka, "A Wide-Range Digital, Power/Energy Meter for Systems With Nonsinusoidal Waveforms," *IEEE Trans. on Industrial Electronics,* IE-29, pp. 18-31, Feb. 1982.

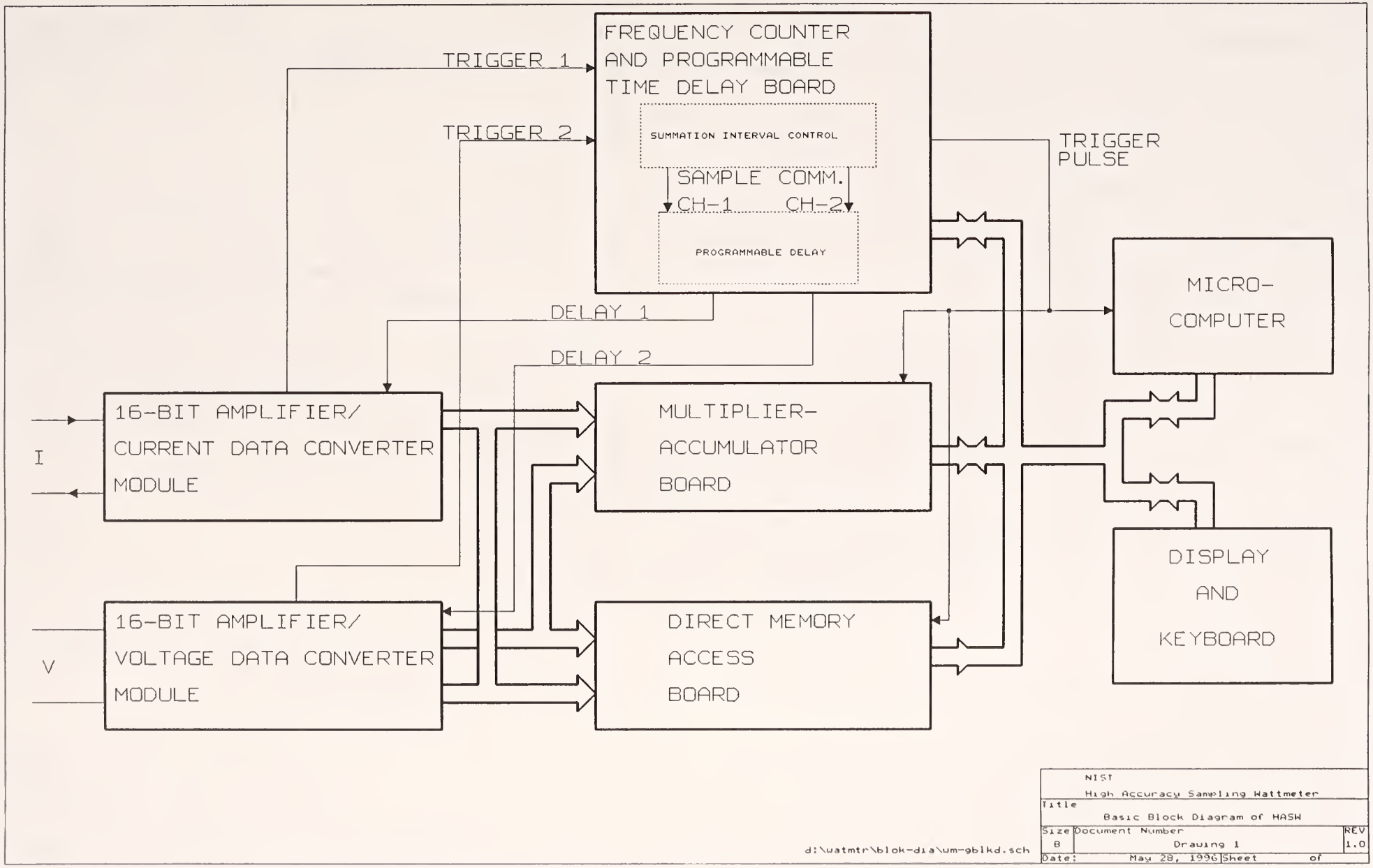
[6] J.J. Hill and W.E. Alderson, "Design of a Microprocessor-Based Digital Wattmeter," *IEEE Trans. on Industrial Electronics and Control Instrumentation,* IECI-28, Aug. 1981.

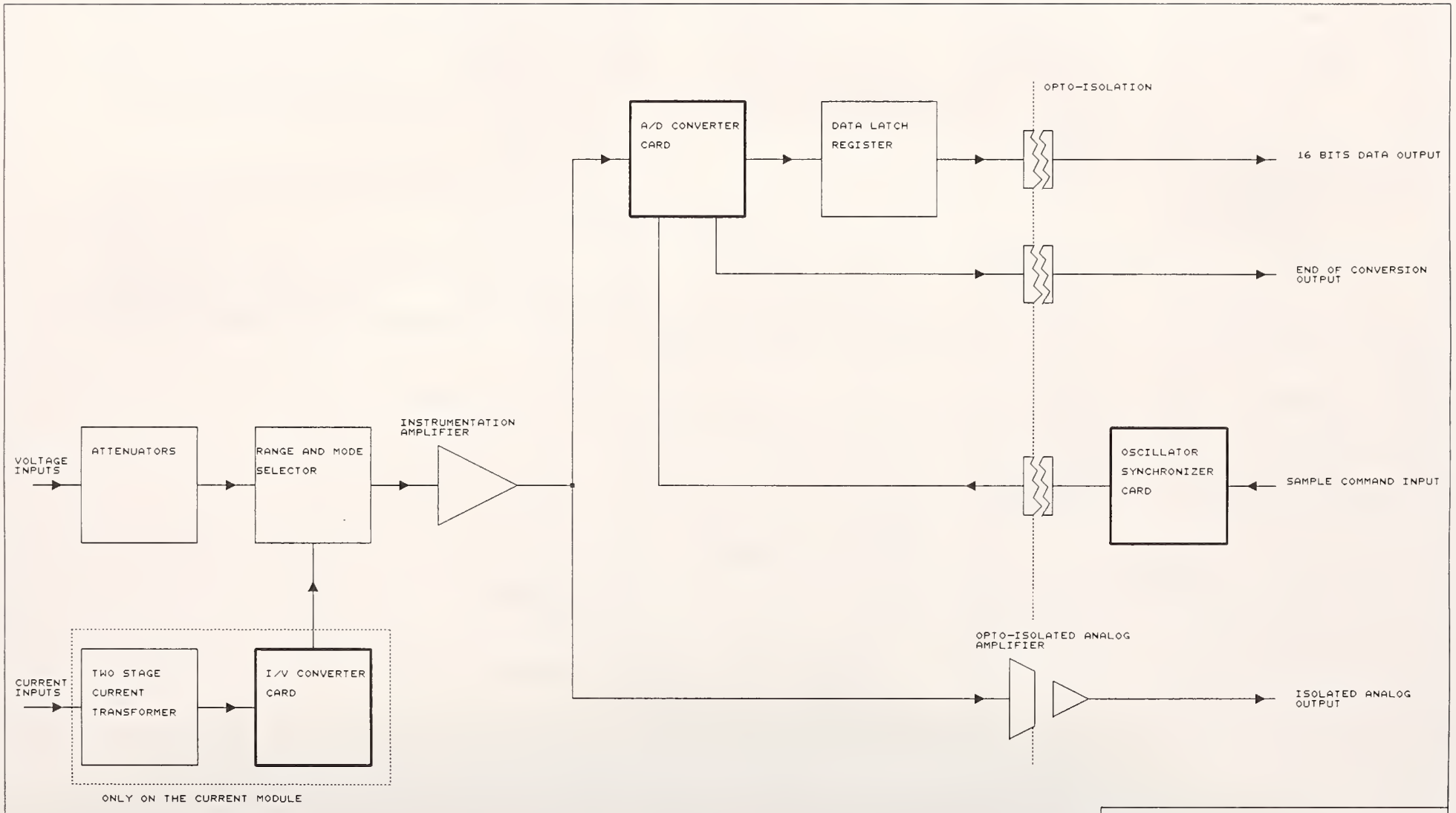
[7] F.J.J. Clark and J.R. Stockton, "Principles and Theory of Wattmeters Operating on the Basis of Regularly Spaced Sample Pairs," *Jour. of Physics E: Scientific Instruments,* Vol. 15, No. 6, pp. 645-652, June 1982.

[8] T.M. Souders, "A Wide Range Two-Stage Current Transformer of High Accuracy," *IEEE Trans. Instrum. Meas.,* IM-21, pp. 340-345, Nov. 1972.

Appendix - Drawings

The following drawings show the parts of the wattmeter that were changed during the upgrade from the NIST Wideband Sampling Wattmeter to the NIST High-Accuracy Sampling Wattmeter.


FREQUENCY COUNTER
AND PROGRAMMABLE
TIME DELAY BOARD
SUMMATION INTERVAL CONTROL
SAMPLE COMM.
CH-1 CH-2
PROGRAMMABLE DELAY
TRIGGER 1
TRIGGER 2
TRIGGER
PULSE
DELAY 1
DELAY 2
MICRO-
COMPUTER
16-BIT AMPLIFIER/
CURRENT DATA CONVERTER
MODULE
I
MULTIPLIER-
ACCUMULATOR
BOARD
DISPLAY
AND
KEYBOARD
16-BIT AMPLIFIER/
VOLTAGE DATA CONVERTER
MODULE
V
DIRECT MEMORY
ACCESS
BOARD
NIST
High Accuracy Sampling Wattmeter
Title
Basic Block Diagram of HASW
Size
B
Document Number
Drawing 1
REV
1.0
Date:
May 28, 1996
Sheet
of
d:\watmtr\blok-dia\um-gblkd.sch



NIST
High Accuracy Sampling Wattmeter
16-bit Amp./Data curr. & Volt. Conv. Modules

Title: Block Diagram of Amp./Data Conv. Modules

Size	Document Number	REV
B	Drawing 2	1.0

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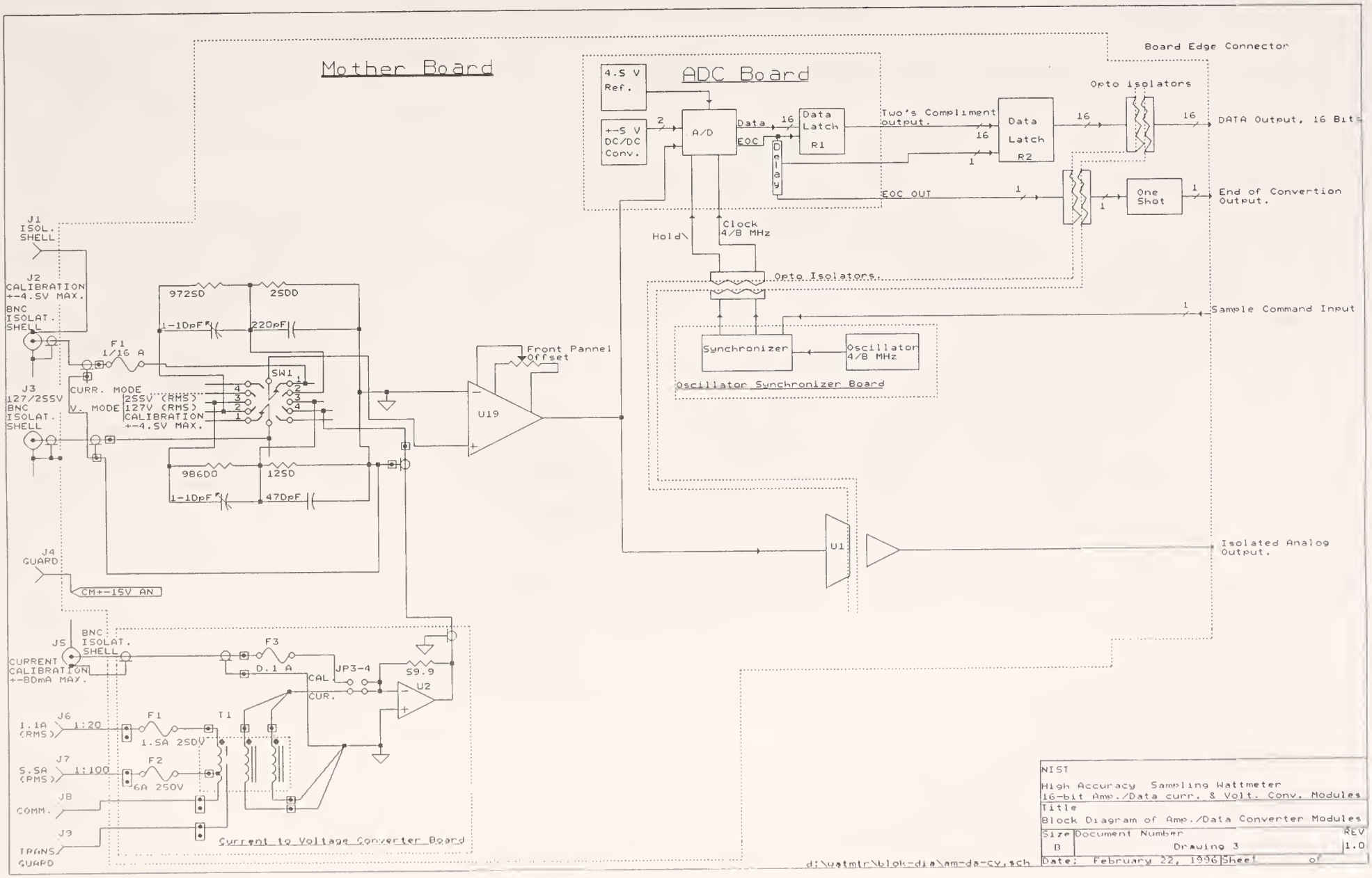
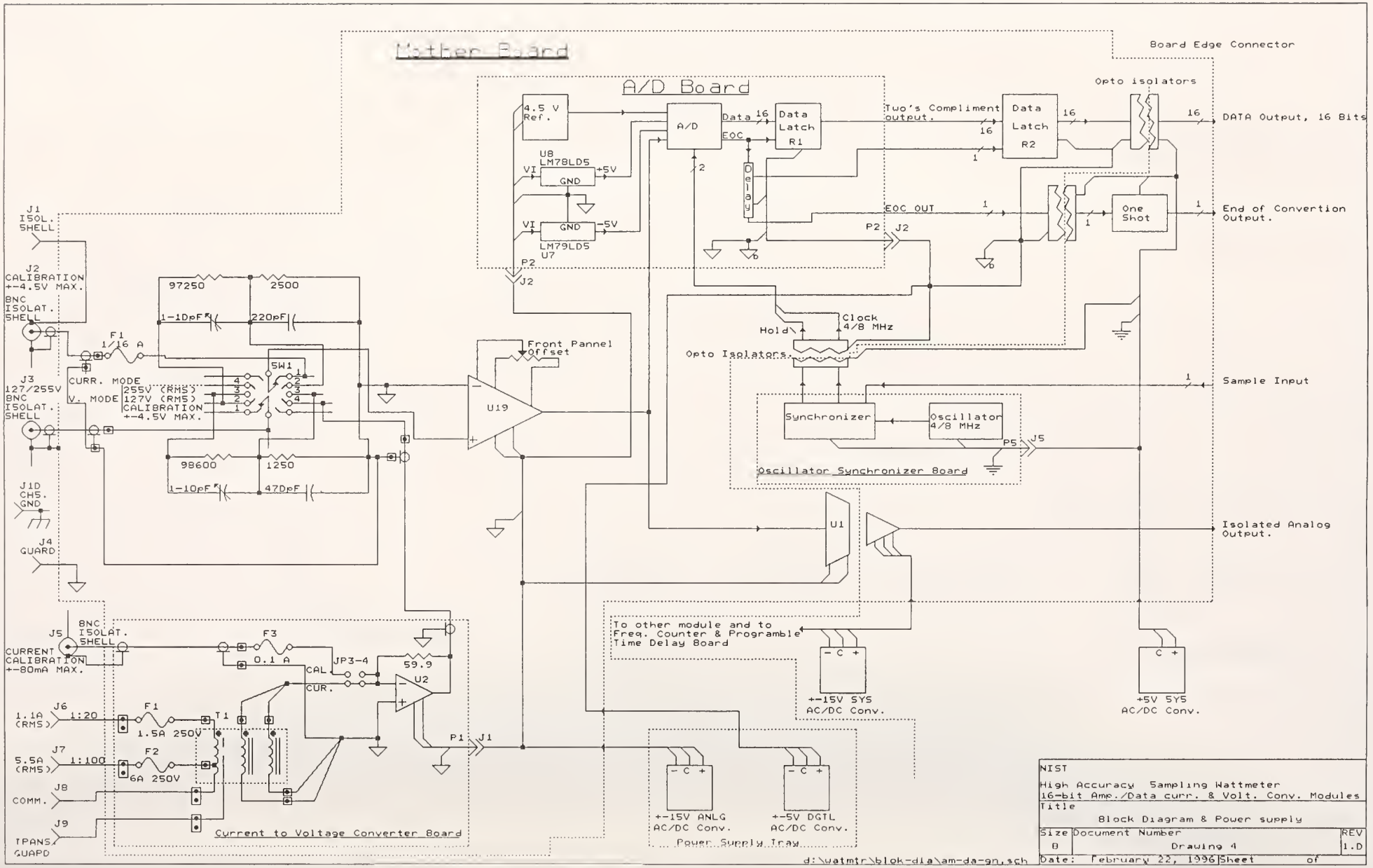
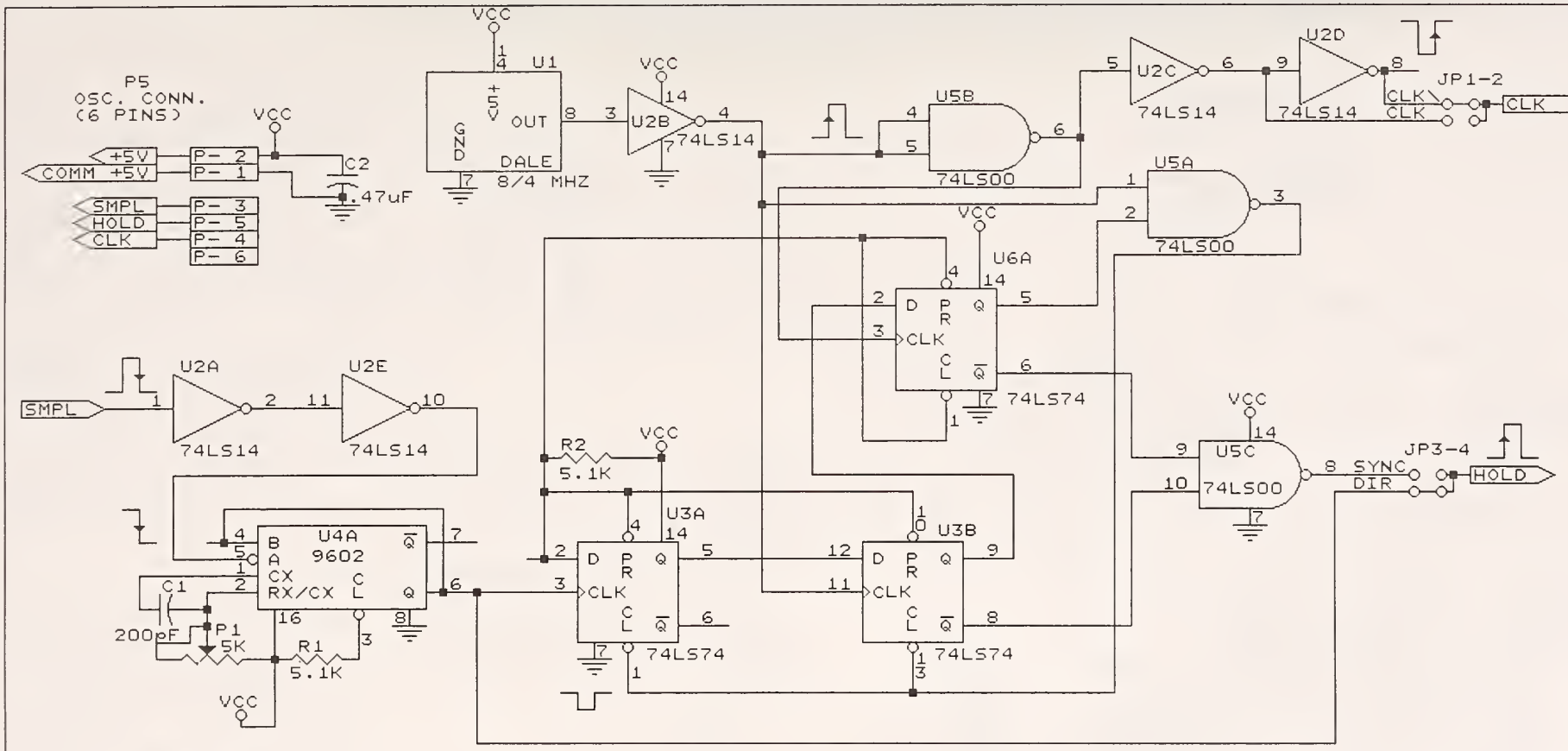
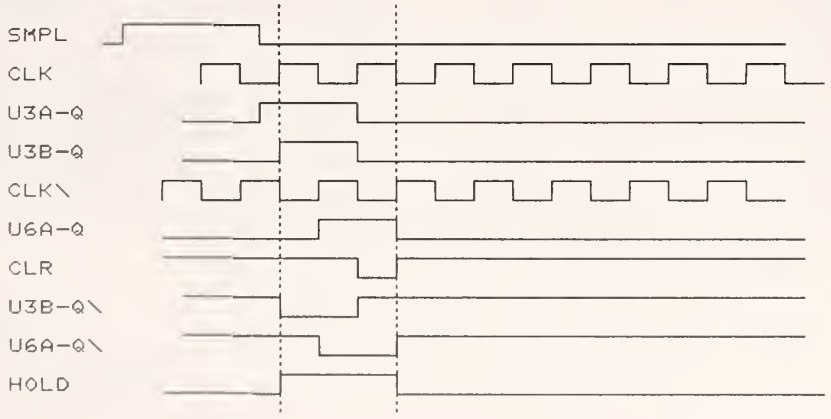

Mother Board
ADC Board
4.5 V Ref.
+-5 V DC/DC Conv.
A/D
Data
EOC
Data Latch R1
Two's Compliment output.
Data Latch R2
Opto isolators
Board Edge Connector
DATA Output, 16 Bits
Delay
EOC OUT
One Shot
End of Convertion Output.
Hold\
Clock 4/8 MHz
Opto Isolators.
Sample Command Input
Synchronizer
Oscillator 4/8 MHz
Oscillator Synchronizer Board
J1 ISOL. SHELL
J2 CALIBRATION +-4.5V MAX.
BNC ISOLAT. SHELL
F1 1/16 A
J3 127/2SSV BNC ISOLAT. SHELL
CURR. MODE
V. MODE
2SSV (RMS)
127V (RMS)
CALIBRATION +-4.5V MAX.
SW1
972SD
2SDD
1-1DpF
220pF
986DD
12SD
47DpF
Front Pannel Offset
U19
U1
Isolated Analog Output.
J4 GUARD
CM+-15V AN
J5 BNC ISOLAT. SHELL
CURRENT CALIBRATION +-80mA MAX.
F3
0.1 A
JP3-4
CAL
CUR.
S9.9
U2
J6 1.1A (RMS)
1:20
F1
1.5A 250V
T1
J7 5.5A (PMS)
1:100
F2
6A 250V
J8 COMM.
J9 TRANS GUARD
Current to Voltage Converter Board
NIST
High Accuracy Sampling Wattmeter
16-bit Amp./Data curr. & Volt. Conv. Modules
Title
Block Diagram of Amp./Data Converter Modules
Size B
Document Number Drawing 3
REV 1.0
Date: February 22, 1996
Sheet of
d:\watmtr\blok-dia\am-da-cv.sch

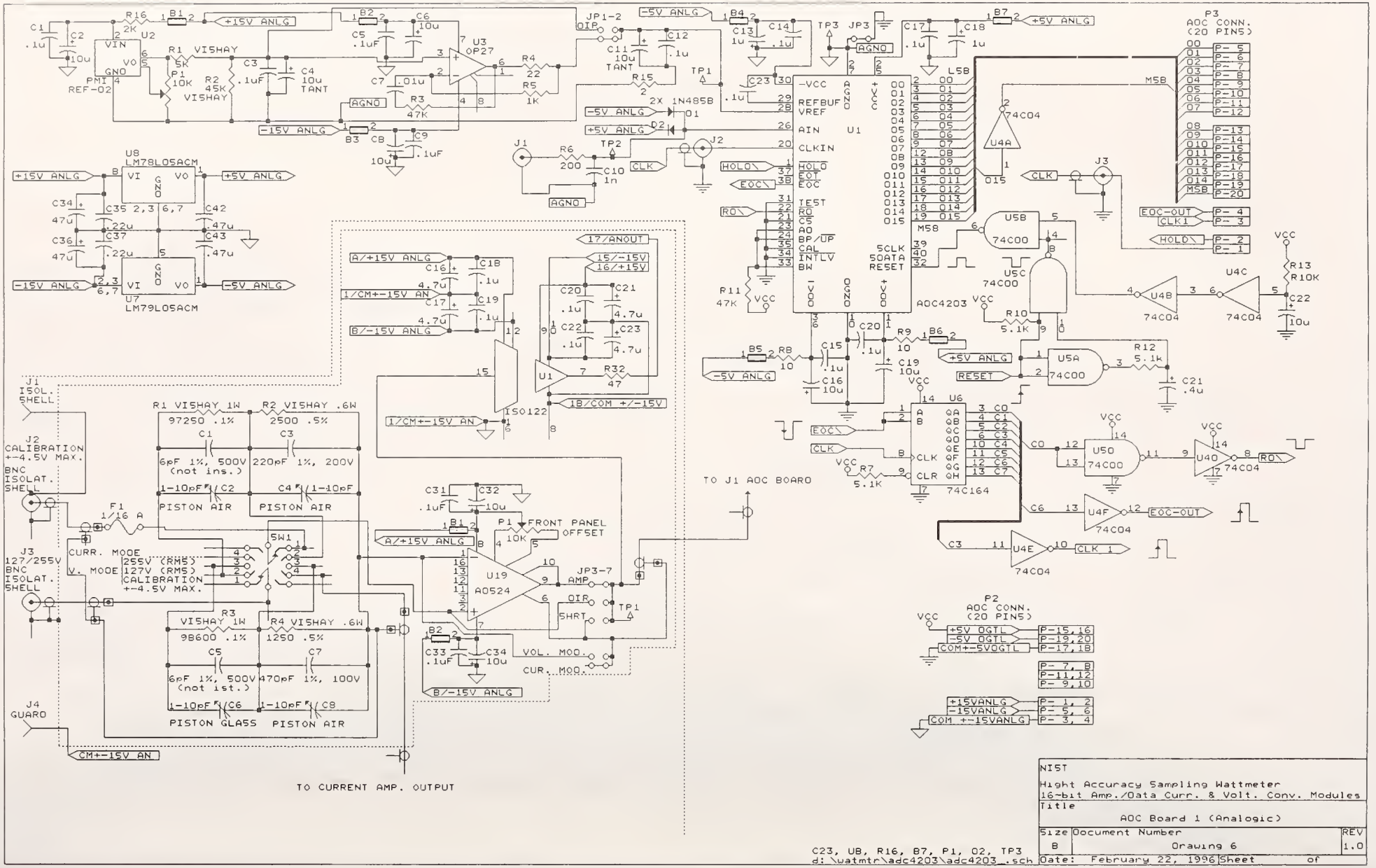

Mother Board
A/D Board
Board Edge Connector
Opto isolators
4.5 V Ref.
A/D
Data
EOC
16
Data Latch R1
Two's Compliment output.
Data Latch R2
DATA Output, 16 Bits
U8 LM78LD5
VI
GND
+5V
-5V
LM79LD5 U7
Delay
EOC OUT
One Shot
End of Convertion Output.
P2
J2
J1 ISOL. SHELL
J2 CALIBRATION +-4.5V MAX.
BNC ISOLAT. SHELL
97250
2500
1-10pF
220pF
F1 1/16 A
Hold
Clock 4/8 MHz
Opto Isolators.
Front Pannel Offset
SW1
CURR. MODE
V. MODE
255V (RMS)
127V (RMS)
CALIBRATION
+-4.5V MAX.
J3 127/255V BNC ISOLAT. SHELL
U19
Sample Input
Synchronizer
Oscillator 4/8 MHz
P5
J5
Oscillator Synchronizer Board
98600
1250
1-10pF
47pF
J1D CH5. GND
J4 GUARD
U1
Isolated Analog Output.
To other module and to Freq. Counter & Programble Time Delay Board
+-15V SYS AC/DC Conv.
+5V SYS AC/DC Conv.
J5 BNC ISOLAT. SHELL
CURRENT CALIBRATION +-80mA MAX.
F3
0.1 A
JP3-4
CAL
CUR.
59.9
U2
J6 1.1A (RMS)
1:20
F1
1.5A 250V
T1
J7 5.5A (RMS)
1:100
F2
6A 250V
J8 COMM.
J9 IPANS GUAPD
P1
J1
Current to Voltage Converter Board
+-15V ANLG AC/DC Conv.
+-5V DGTL AC/DC Conv.
Power Supply Tray
NIST
High Accuracy Sampling Wattmeter
16-bit Amp./Data curr. & Volt. Conv. Modules
Title
Block Diagram & Power supply
Size B
Document Number
Drawing 4
REV 1.D
Date: February 22, 1996
Sheet of
d:\watmtr\blok-dia\am-da-gn.sch





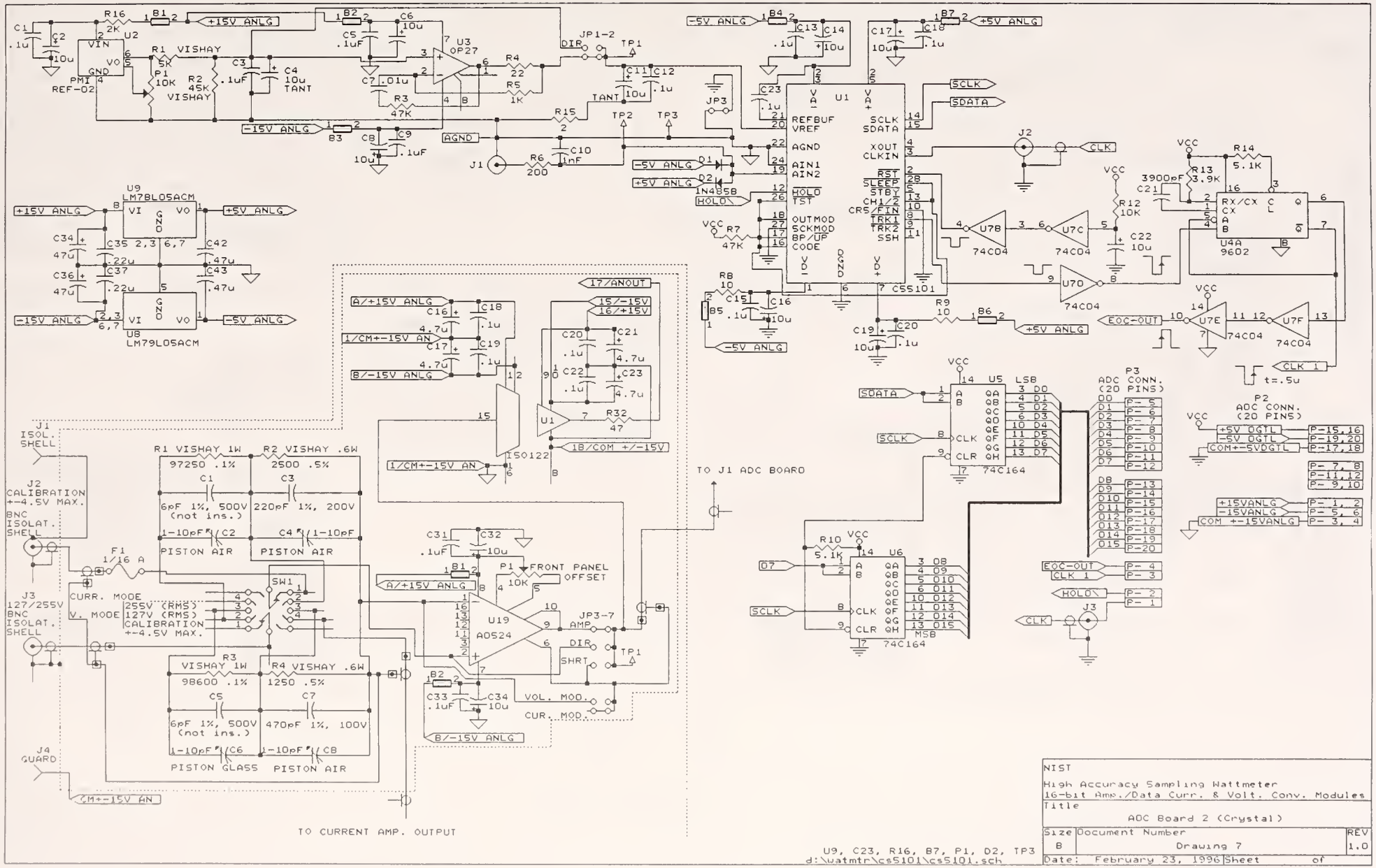
U6, R2, C2, P1
d:\watmtr\in-mod2\sync2.sch

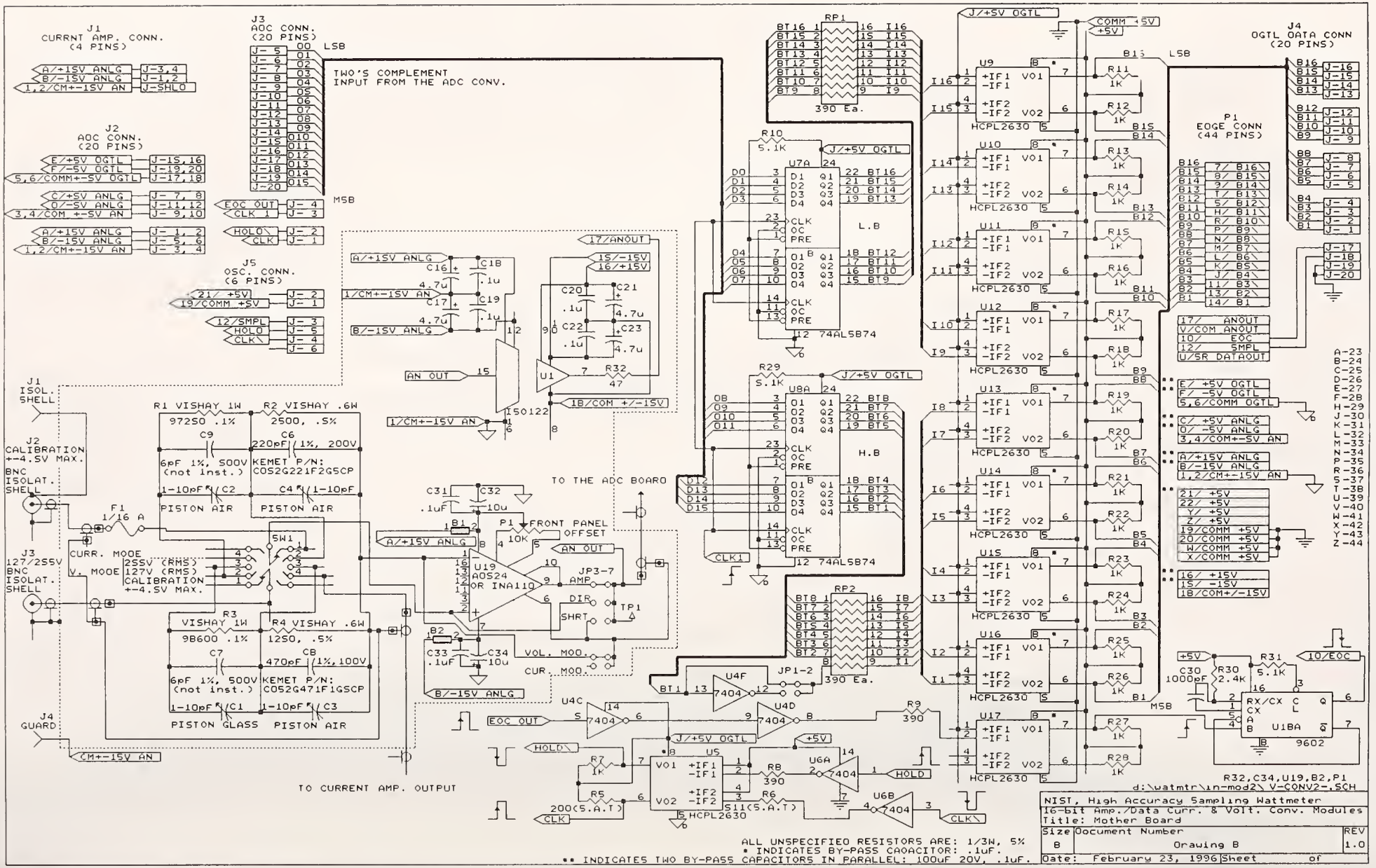
NIST		
High Accuracy Sampling Wattmeter 16-bit Amp./Data Curr. & Volt. Conv. Modules		
Title Clock Synchronizer Board		
Size A	Document Number Drawing 5	REV 1.0
Date: February 22, 1996	Sheet of	



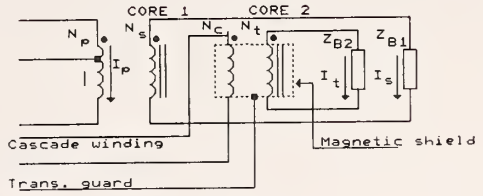
NIST		
Hight Accuracy Sampling Wattmeter		
16-bit Amp./Data Curr. & Volt. Conv. Modules		
Title		
AOC Board 1 (Analogic)		
Size	Document Number	REV
B	Drawing 6	1.0
Date: February 22, 1996	Sheet of	

C23, U8, R16, B7, P1, O2, TP3
d:\watmtr\adc4203\adc4203_.sch

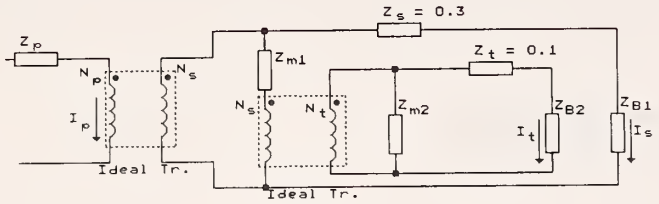

+15V ANLG
-15V ANLG
+5V ANLG
-5V ANLG
AGND
DIR
JP1-2
TP1
TP2
TP3
JP3
U1
CS5101
REFBUF
VREF
AGND
AIN1
AIN2
HOLD
TST
OUTMOD
SCKMOD
BP/UP
CODE
SCLK
SDATA
XOUT
CLKIN
RST
SLEEP
STBY
CH1/2
CRS/FIN
TRK1
TRK2
SSH
J1
J2
CLK
R1 VISHAY
R2 VISHAY
R3
R4
R5
R6
R7
R8
R9
R10
R12
R13
R14
R15
R16
P1
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
C15
C16
C17
C18
C19
C20
C21
C22
C23
U2
U3 OP27
U4A 9602
U5 LSB
U6 MSB
U7C
U7E
U7F
U7O
U78
74C04
74C164
U9 LM78L05ACM
U8 LM79L05ACM
REF-02
VISHAY
TANT
1N4858
EOC-OUT
CLK 1
t=.5u
P3 ADC CONN. (20 PINS)
P2 ADC CONN. (20 PINS)
TO J1 ADC BOARD
J1 ISOL. SHELL
J2 CALIBRATION +-4.5V MAX.
BNC ISOLAT. SHELL
J3 127/255V BNC ISOLAT. SHELL
J4 GUARD
F1 1/16 A
SW1
CURR. MODE
V. MODE
255V (RMS)
127V (RMS)
CALIBRATION +-4.5V MAX.
R1 VISHAY 1W 97250 .1%
R2 VISHAY .6W 2500 .5%
R3 VISHAY 1W 98600 .1%
R4 VISHAY .6W 1250 .5%
6pF 1%, 500V (not ins.)
220pF 1%, 200V
470pF 1%, 100V
PISTON AIR
PISTON GLASS
U19 AD524
FRONT PANEL OFFSET
VOL. MOD.
CUR. MOD.
ISO122
TO CURRENT AMP. OUTPUT
NIST
High Accuracy Sampling Wattmeter
16-bit Amp./Data Curr. & Volt. Conv. Modules
Title
ADC Board 2 (Crystal)
Size B
Document Number
Drawing 7
REV 1.0
Date: February 23, 1996
Sheet of
U9, C23, R16, B7, P1, D2, TP3
d:\watmtr\cs5101\cs5101.sch


J1
CURRNT AMP. CONN.
(4 PINS)
A/+15V ANLG
B/-15V ANLG
1,2/CM+-15V AN
J3
AOC CONN.
(20 PINS)
LSB
MSB
TWO'S COMPLEMENT
INPUT FROM THE ADC CONV.
J2
AOC CONN.
(20 PINS)
E/+5V OGTL
F/-5V OGTL
5,6/COMM+-5V OGTL
C/+5V ANLG
D/-5V ANLG
3,4/COM +-5V AN
EOC OUT
CLK 1
HOLD\
CLK
J5
OSC. CONN.
(6 PINS)
21/ +5V
19/COMM +5V
12/SMPL
HOLD\
CLK\
RP1
390 Ea.
74AL5B74
L.B
H.B
HCPL2630
J/+5V OGTL
COMM +5V
+5V
J4
OGTL DATA CONN
(20 PINS)
P1
EDGE CONN
(44 PINS)
17/ ANOUT
V/COM ANOUT
10/ EOC
12/ SMPL
U/SR DATAOUT
E/ +5V OGTL
F/ -5V OGTL
5,6/COMM OGTL
C/ +5V ANLG
D/ -5V ANLG
3,4/COM+-5V AN
A/+15V ANLG
B/-15V ANLG
1,2/CM+-15V AN
21/ +5V
22/ +5V
Y/ +5V
Z/ +5V
19/COMM +5V
20/COMM +5V
W/COMM +5V
X/COMM +5V
16/ +15V
15/ -15V
18/COM+/-15V
J1
ISOL.
SHELL
J2
CALIBRATION
+-4.5V MAX.
BNC
ISOLAT.
SHELL
J3
127/255V
BNC
ISOLAT.
SHELL
J4
GUARD
R1 VISHAY 1W
9725O .1%
R2 VISHAY .6W
2500, .5%
C9
6pF 1%, 500V
(not inst.)
C6
220pF (1%, 200V
KEMET P/N:
C052G221F2G5CP
1-10pF C2
PISTON AIR
C4 1-10pF
PISTON AIR
F1
1/16 A
SW1
CURR. MODE
V. MODE
255V (RMS)
127V (RMS)
CALIBRATION
+-4.5V MAX.
R3
VISHAY 1W
9B600 .1%
R4 VISHAY .6W
125O, .5%
C7
C8
470pF (1%,100V
KEMET P/N:
C052G471F1G5CP
6pF 1%, 500V
(not inst.)
1-10pF C1
PISTON GLASS
1-10pF C3
PISTON AIR
CM+-15V AN
TO CURRENT AMP. OUTPUT
TO THE ADC BOARD
C31 .1uF
C32 10u
B1
P1 10K
FRONT PANEL
OFFSET
AN OUT
U19
AD524
OR INA110
JP3-7
AMP
DIR
SHRT
TP1
B2
C33 .1uF
C34 10u
VOL. MOD.
CUR. MOD.
B/-15V ANLG
A/+15V ANLG
C16 4.7u
C18 .1u
C17 4.7u
C19 .1u
1/CM+-15V AN
B/-15V ANLG
17/ANOUT
15/-15V
16/+15V
C20 .1u
C21 4.7u
C22 .1u
C23 4.7u
AN OUT
U1
R32 47
IS0122
1B/COM +/-15V
1/CM+-15V AN
R10 5.1K
R29 5.1K
U7A
U8A
CLK1
RP2
390 Ea.
U4F
7404
JP1-2
U4C
U4D
R9 390
EOC OUT
HOLD\
R7 1K
R8 390
R5 200(5.A.T)
R6 511(5.A.T)
U5
HCPL2630
U6A
U6B
CLK
CLK\
U9
U10
U11
U12
U13
U14
U15
U16
U17
R11 1K
R12 1K
R13 1K
R14 1K
R15 1K
R16 1K
R17 1K
R18 1K
R19 1K
R20 1K
R21 1K
R22 1K
R23 1K
R24 1K
R25 1K
R26 1K
R27 1K
R28 1K
10/EOC
C30 1000pF
R30 2.4K
R31 5.1K
RX/CX
CX
A
B
U1BA
9602
R32,C34,U19,B2,P1
d:\watmtr\in-mod2\ V-CONV2-.SCH
ALL UNSPECIFIED RESISTORS ARE: 1/3W, 5%
* INDICATES BY-PASS CAPACITOR: .1uF.
** INDICATES TWO BY-PASS CAPACITORS IN PARALLEL: 100uF 20V, .1uF.
NIST, High Accuracy Sampling Wattmeter
16-bit Amp./Data Curr. & Volt. Conv. Modules
Title: Mother Board
Size B
Document Number
Drawing B
REV 1.0
Date: February 23, 1996
Sheet of

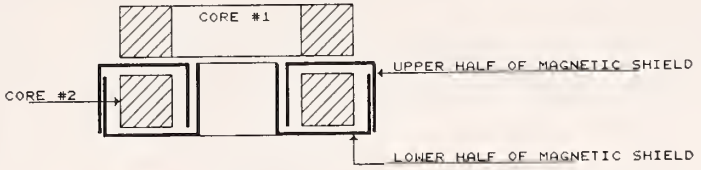
N_p = 1/5 Turns N_s = 100 Turns N_c = 1 Turn N_t = 100 Turns



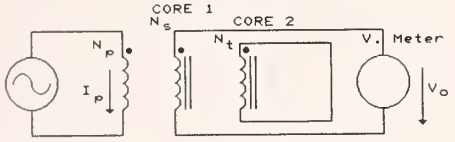
Two stage transformer
Schematic representation



Equivalent circuit



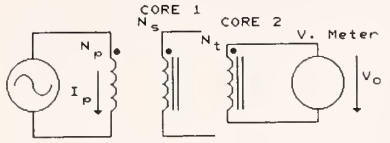
Construction scematic



N_p= 10 Turns N_s= 100 Turns N_t= 100 Turns

Freq. (Hz)	I_p (A)	V_o (v)	Z_{m1} (OHM)
50	0.04	1.8	450
1K	0.0206	5.13	2490
10K	0.0094	11.8	12K

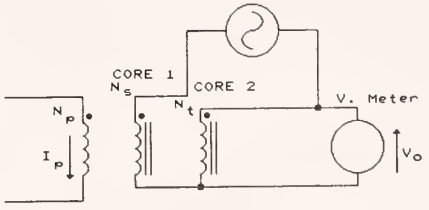
Set-up for measuring Zm1



N_p= 10 Turns N_s= 100 Turns N_t= 100 Turns

Freq. (Hz)	I_p (A)	V_o (v)	Z_{m2} (OHM)
50	0.0385	1.67	433
1K	0.017	5.2	2470
10K	0.0094	11.31	12.5K

Set-up for measuring Zm2



SEt-up for verifying that the number of turns of both cores are equal.

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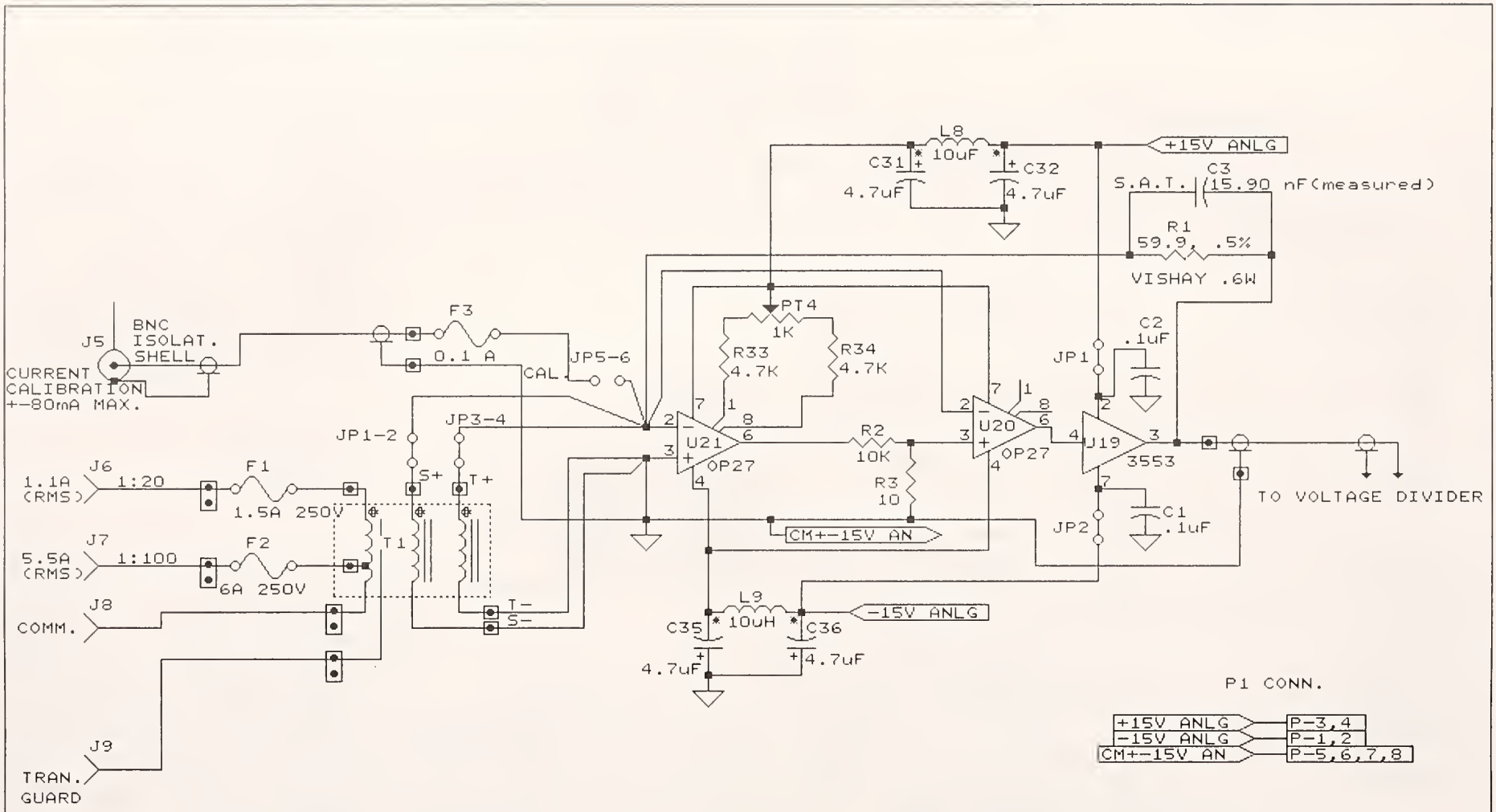
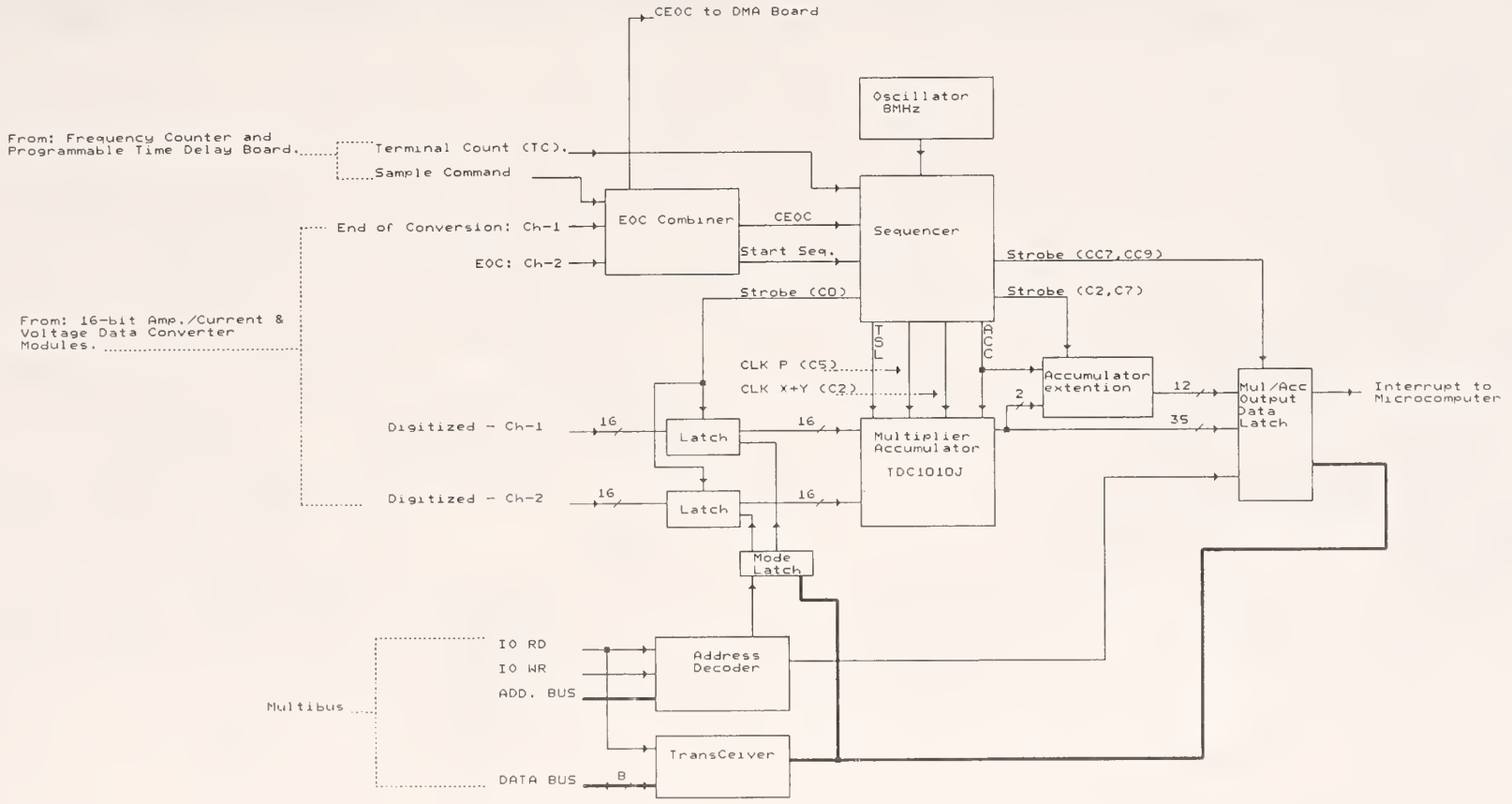
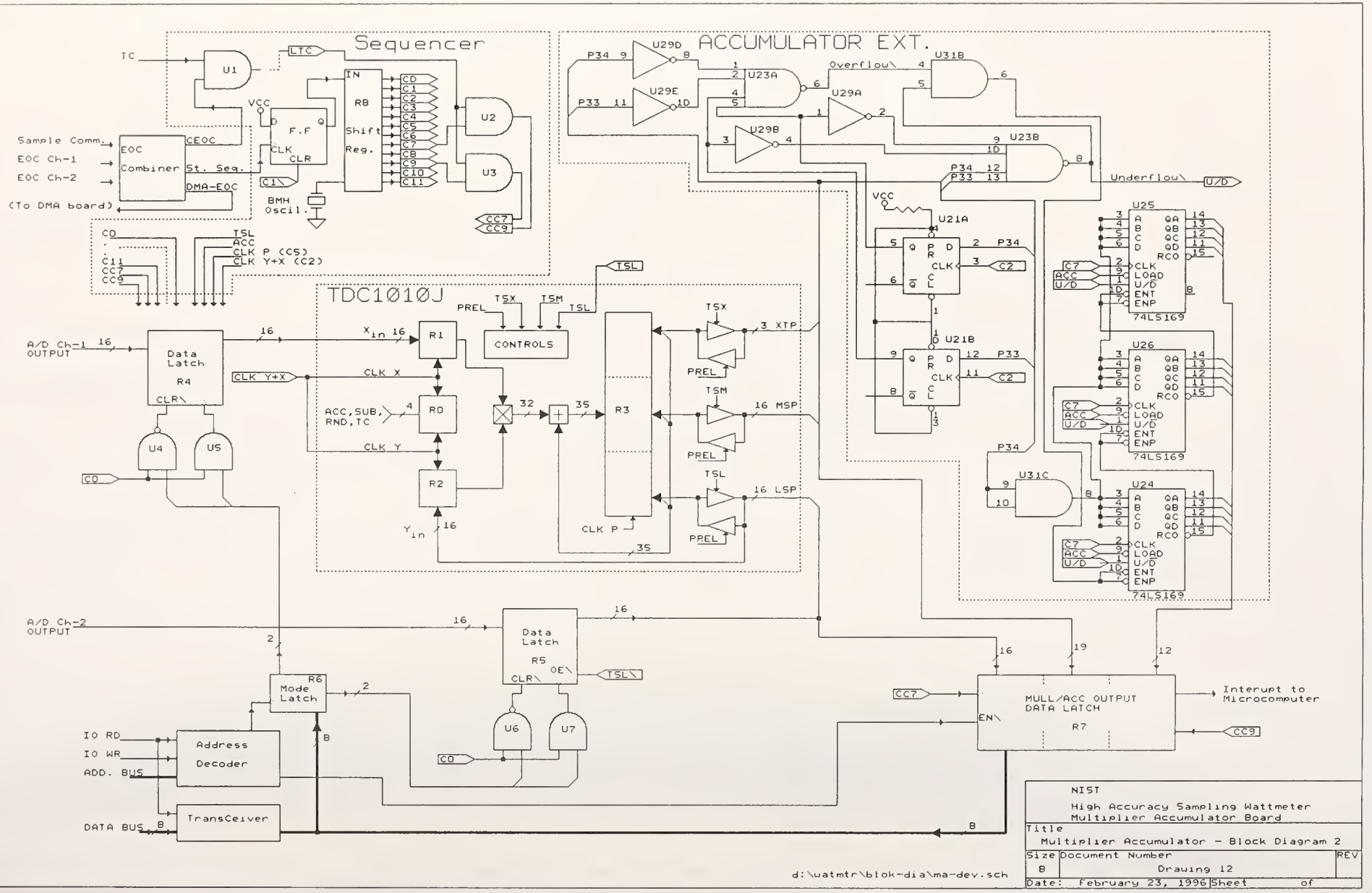
NIST High Accuracy Sampling Wattmeter 16-bit Amp./Data Current Conv. Module		
Title Current transformer scematic		
Size B	Document Number Drawing 9	REV 1.0
Date: February 23, 1996	Sheet of	

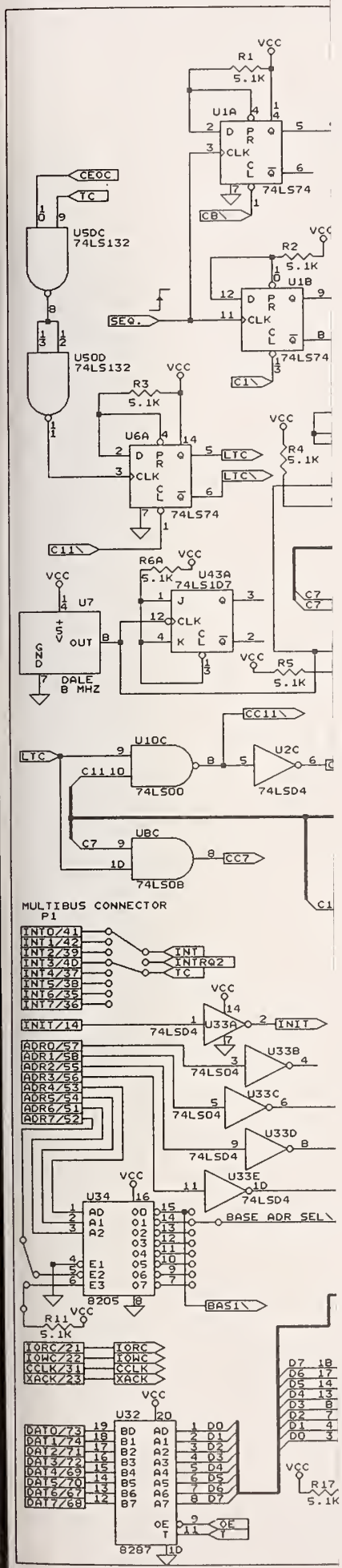


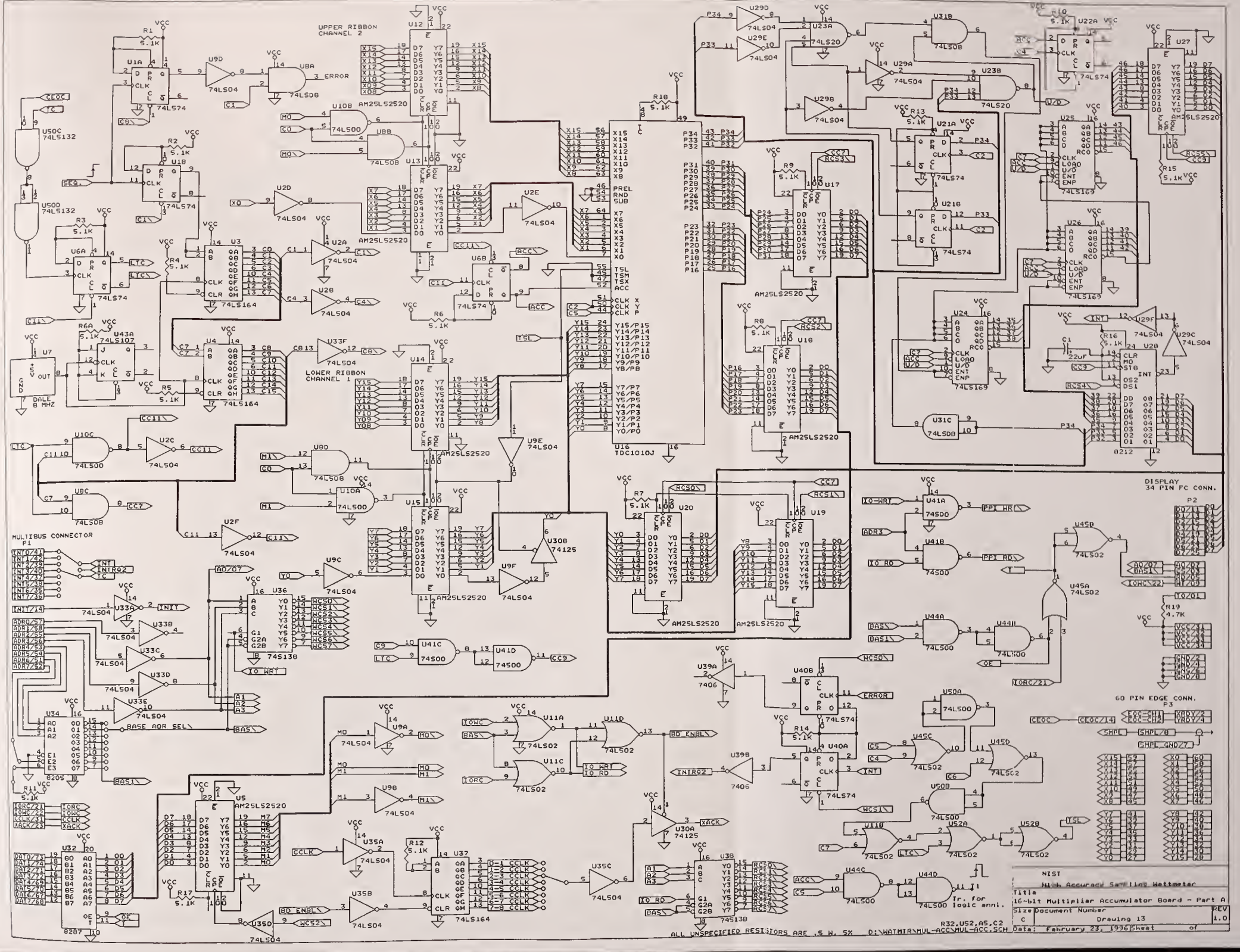
NIST		
High Accuracy Sampling Wattmeter 16-bit Amplifier/Data Curr. Converter Module		
Title Current-to-Voltage Converter Board		
Size A	Document Number Drawing 10	REV 1.0
d:\watmtr\in-mod2\i-conv2.sch	Date: February 23, 1996	Sheet of

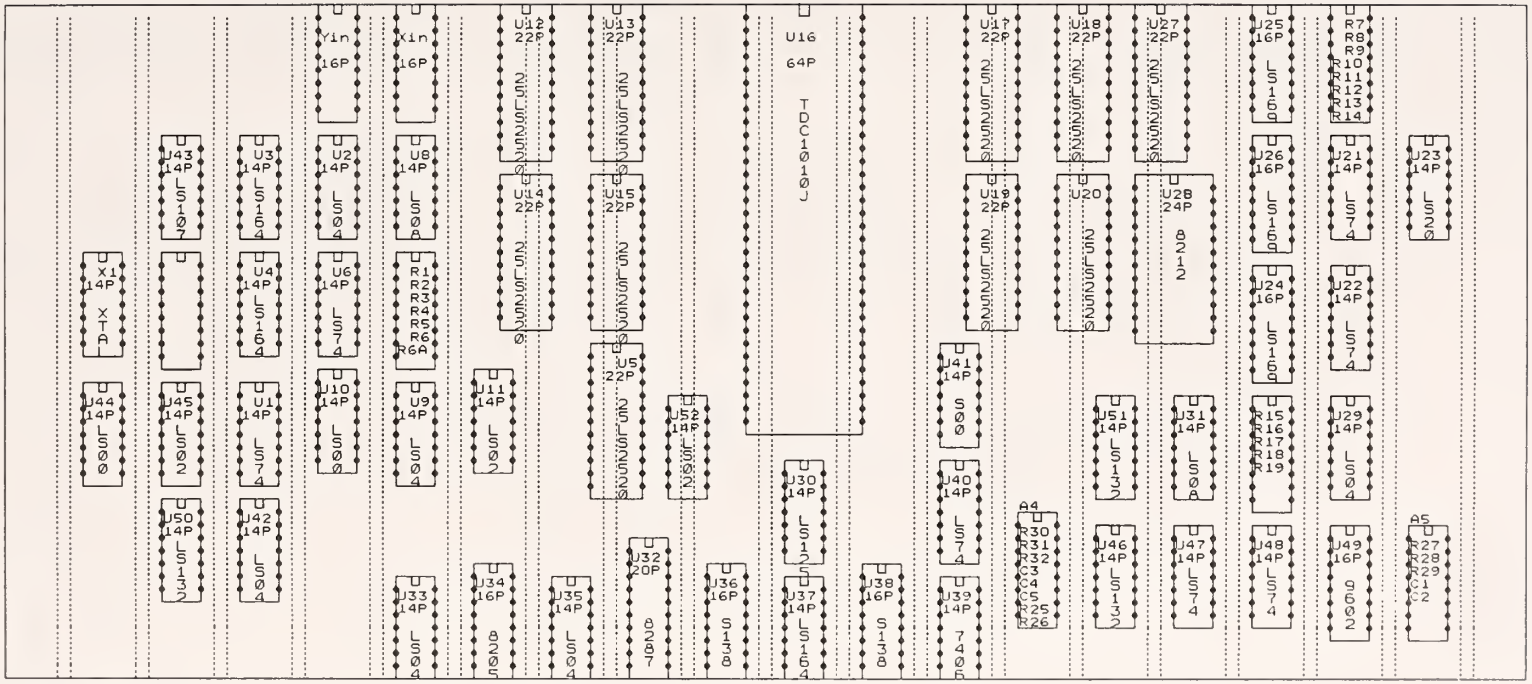


NIST High Accuracy Sampling Wattmeter Multiplier Accumulator Board		
Title Multiplier Accumulator - Block Diagram 1		
Size B	Document Number Drawing 11	REV 1.0
d:\watmtr\blok-dia\mul-acc.sch	Date: February 23, 1996	Sheet of


Sequencer
ACCUMULATOR EXT.
TDC1010J
TC
LTC
U1
VCC
F.F
CLK
CLR
IN
RB
Shift
Reg.
CD
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
U2
U3
CC7
CC9
Sample Comm.
EOC Ch-1
EOC Ch-2
(To DMA board)
EOC
Combiner
CEOC
St. Seq.
DMA-EOC
C1\
BMH
Oscil.
CD
C11
CC7
CC9
TSL
ACC
CLK P (C5)
CLK Y+X (C2)
P34
P33
U29D
U29E
U29B
U23A
U29A
U31B
U23B
Overflow\
Underflow\
U/D
U21A
U21B
U31C
U25
U26
U24
74LS169
A
B
C
D
QA
QB
QC
QD
RCO
CLK
LOAD
U/D
ENT
ENP
C7
ACC
U/D
P34
P33
C2
A/D Ch-1 OUTPUT
16
Data Latch
R4
CLR\
CLK Y+X
CLK X
CLK Y
ACC,SUB, RND,TC
4
R0
R1
R2
X_{in} 16
Y_{in} 16
CONTROLS
PREL
TSX
TSM
TSL
32
35
R3
CLK P
35
3 XTP
16 MSP
16 LSP
U4
U5
C0
A/D Ch-2 OUTPUT
Data Latch
R5
OE\
CLR\
TSL\
R6
Mode Latch
2
B
U6
U7
C0
IO RD
IO WR
ADD. BUS
Address Decoder
DATA BUS
8
TransCeiver
MULL/ACC OUTPUT DATA LATCH
R7
EN\
CC7
CC9
16
19
12
Interupt to Microcomputer
B
d:\watmtr\blok-dia\ma-dev.sch
NIST
High Accuracy Sampling Wattmeter
Multiplier Accumulator Board
Title
Multiplier Accumulator - Block Diagram 2
Size
B
Document Number
Drawing 12
REV
Date: February 23, 1996
Sheet of


VCC
R1
5.1K
U1A
74LS74
CE0C
TC
U5DC
74LS132
CB
R2
5.1K
U1B
SEQ.
U5DD
74LS132
C1
R3
5.1K
U6A
LTC
R4
5.1K
C11
R6A
5.1K
U43A
74LS1D7
U7
DALE
8 MHZ
R5
5.1K
CC11
U10C
74LS00
U2C
74LS04
C7
U8C
CC7
74LS08
MULTIBUS CONNECTOR
P1
INT0/41
INT1/42
INT2/39
INT3/40
INT4/37
INT5/38
INT6/35
INT7/36
INT
INTRQ2
TC
INIT/14
U33A
INIT
U33B
U33C
U33D
U33E
74LS04
74LSD4
ADR0/57
ADR1/58
ADR2/55
ADR3/56
ADR4/53
ADR5/54
ADR6/51
ADR7/52
U34
8205
BASE ADR SEL
BAS1
R11
5.1K
IORC/21
IOWC/22
CCLK/31
XACK/23
IORC
IOWC
CCLK
XACK
U32
8287
DAT0/73
DAT1/74
DAT2/71
DAT3/72
DAT4/69
DAT5/70
DAT6/67
DAT7/68
D7
D6
D5
D4
D3
D2
D1
D0
R17
5.1K
OE


UPPER RIBBON CHANNEL 2
LOWER RIBBON CHANNEL 1
MULTIBUS CONNECTOR P1
DISPLAY 34 PIN FC CONN. P2
60 PIN EDGE CONN. P3
U16 TDC1010J
U5 AM25LS2520
U20 AM25LS2520
U19 AM25LS2520
U15 AM25LS2520
U14 AM25LS2520
U13 AM25LS2520
U12 AM25LS2520
U17 AM25LS2520
U18 AM25LS2520
DALE 8 MHZ
BASE ADR SEL
ERROR
INT
INTR02
XACK
CCLK
BD ENBL
IO WRT
IO RD
PPI WR
PPI RD
ALL UNSPECIFIED RESISTORS ARE .5 W, 5%
D:\WATMIR\MUL-ACC\MUL-ACC.SCH
NIST
High Accuracy Sampling Wattmeter
Title
16-bit Multiplier Accumulator Board - Part A
Size C
Document Number
Drawing 13
REV 4.0
Date: February 23, 1996
Sheet of



NIST		
High Accuracy Sampling Wattmeter 16-bit Multiplier Accumulator Board		
Title: Board Layout Schematic		
Size: B	Document Number: Drawing 14	REV: 1.0
Date: February 21, 1996	Sheet	of

U52, R32, C5

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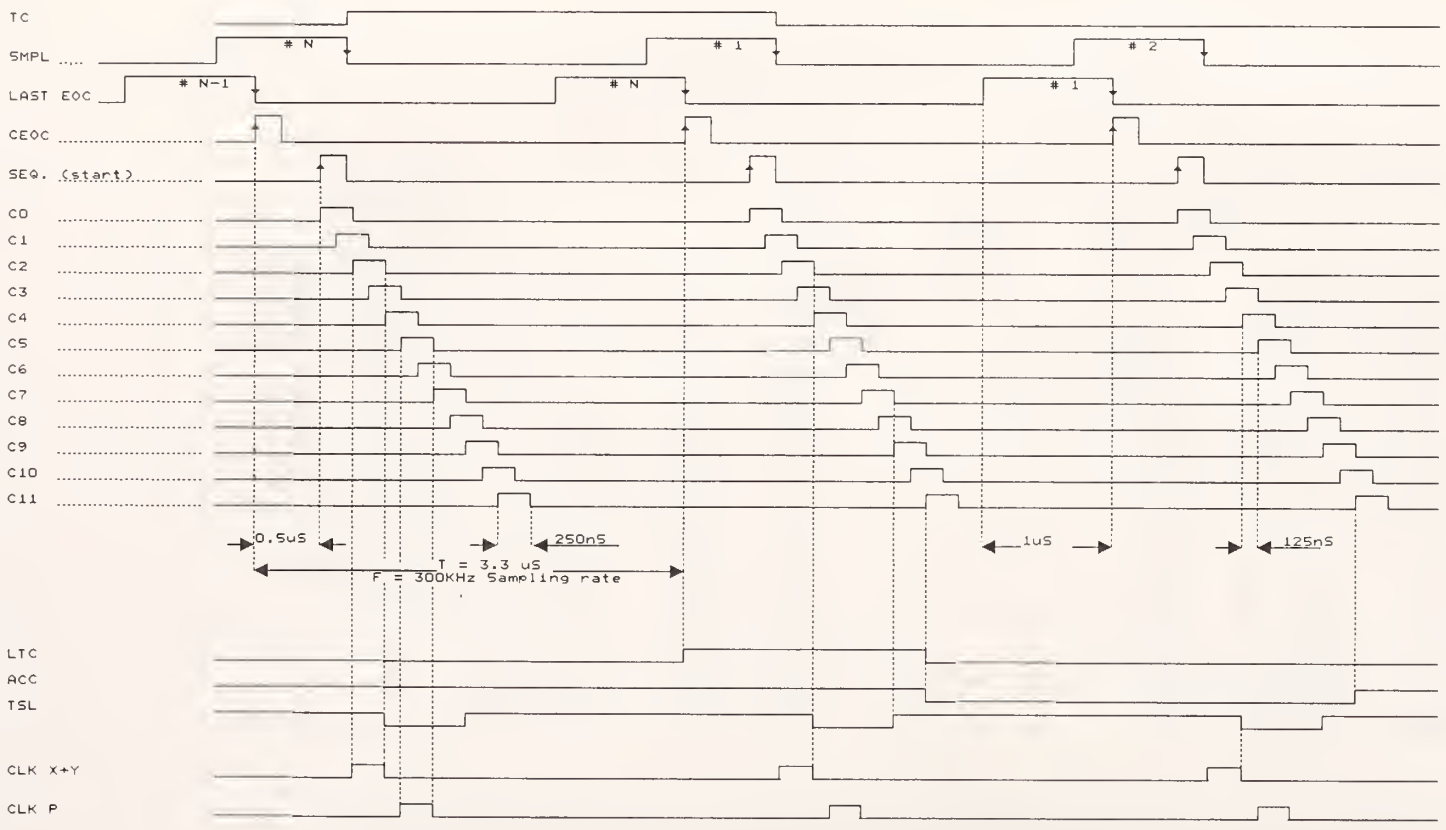
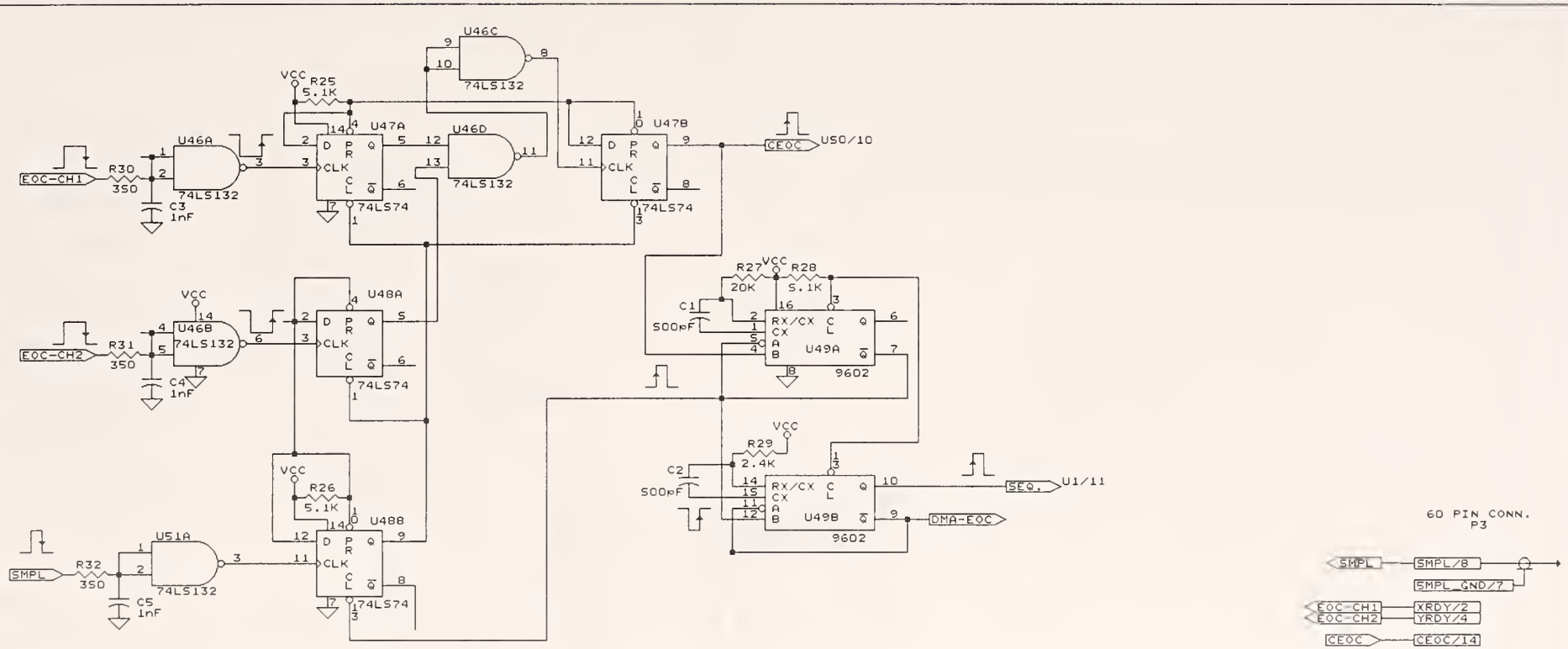


NIST

High Accuracy Sampling Wattmeter
16-bit Multiplier Accumulator Board
Sequencer Block

Title		
Sequencer Timing Diagram		
Size	Document Number	REV
B	Drawing 15	1.0
d:\watmtr\blok-dia\seq-timg.sch	Date: February 23, 1996	Sheet of



A4

R30	100
R31	100
R32	100
C3	1nF
C4	1nF
C5	1nF
R25	5.1K
R26	5.1K

A5

R27	2.4K
R28	5.1K
R29	2.4K
C1	500pF
C2	500pF

R32, U51, C5, A5,
D:\watmtr\mul-acc\ceoc.sch

NIST

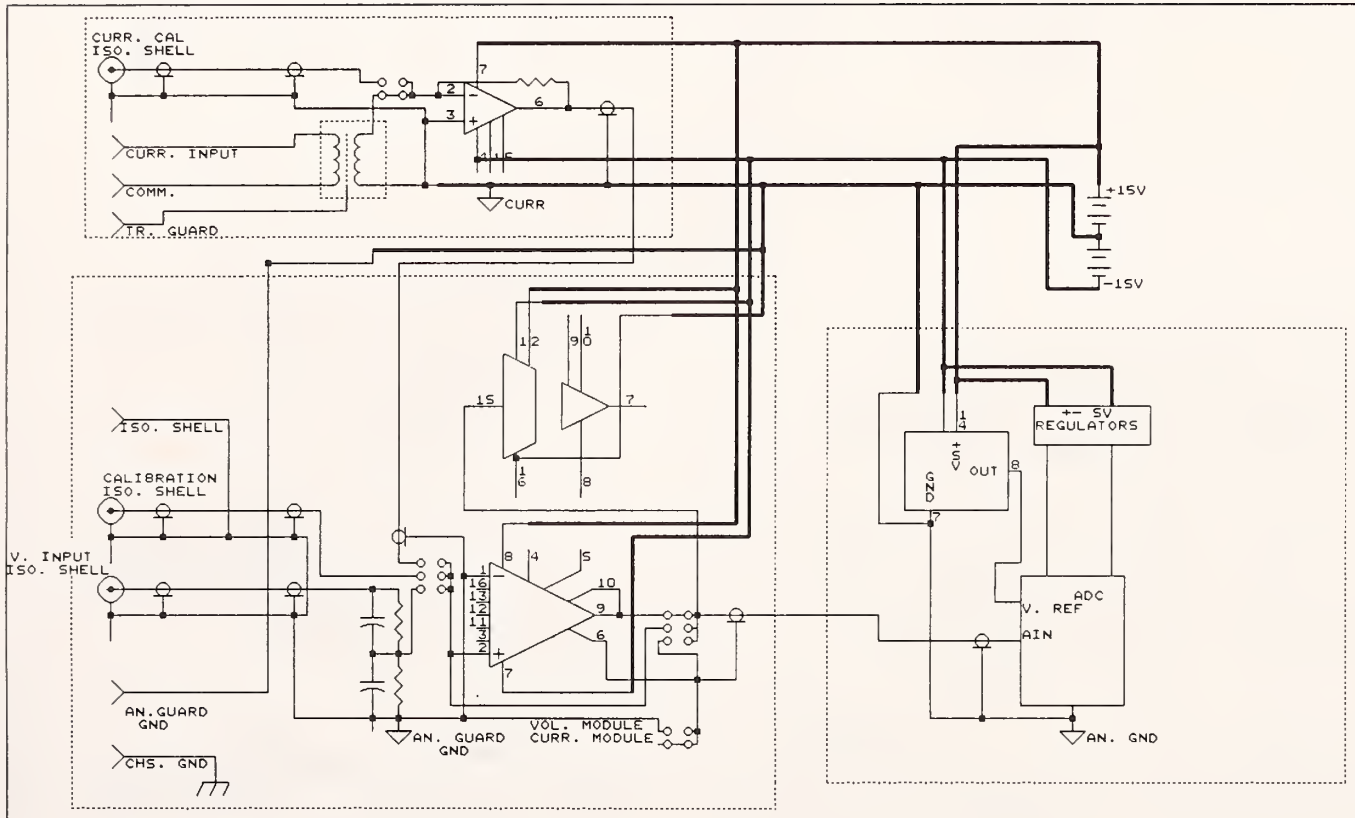
High Accuracy Sampling Wattmeter
16-bit Multiplier Accumulator Board - Part B

Title

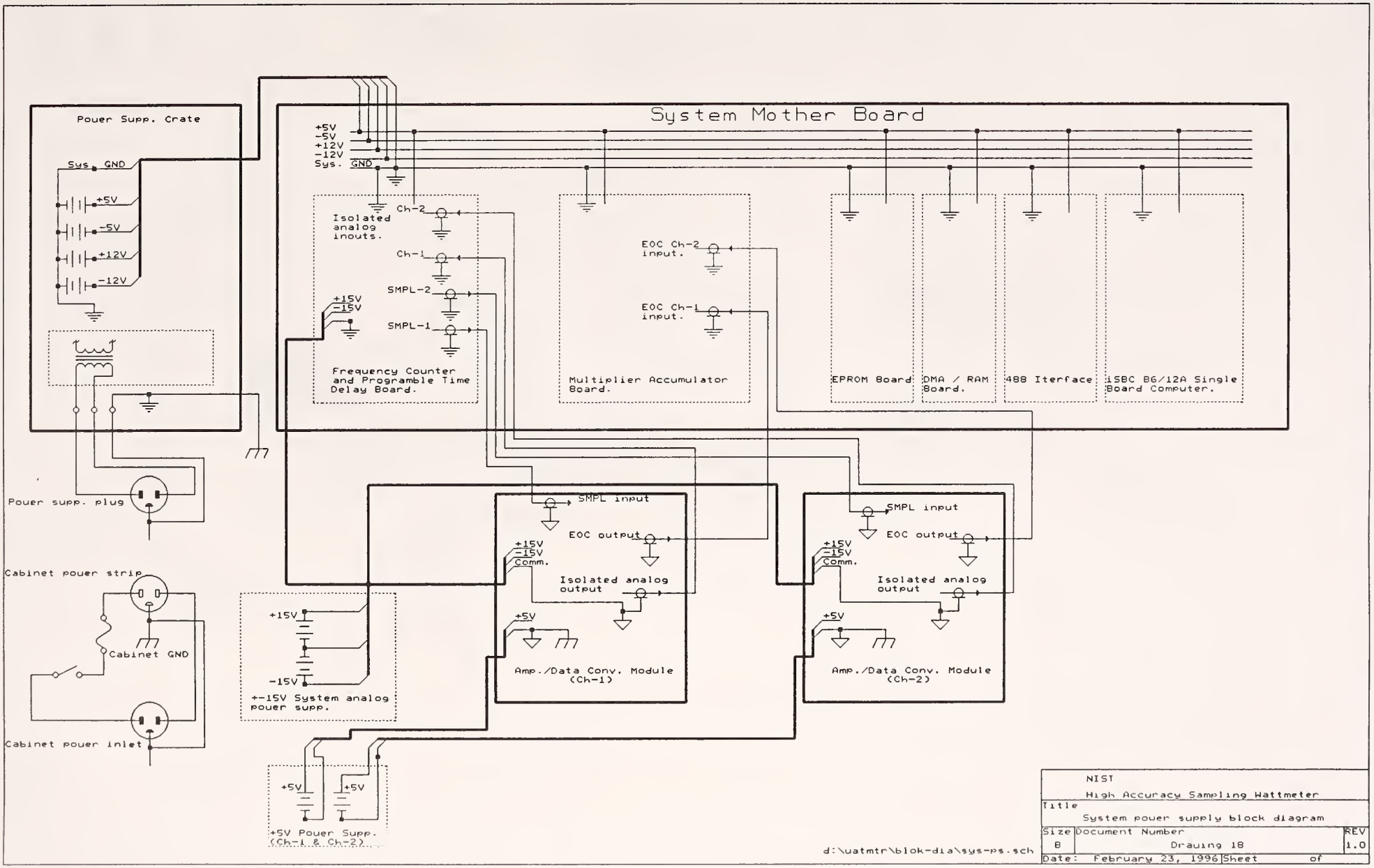
End-of-Conversion Combiner Curcuit

Size	Document Number	REV
B	Drawing 16	1.0

Date: February 23, 1996 Sheet of

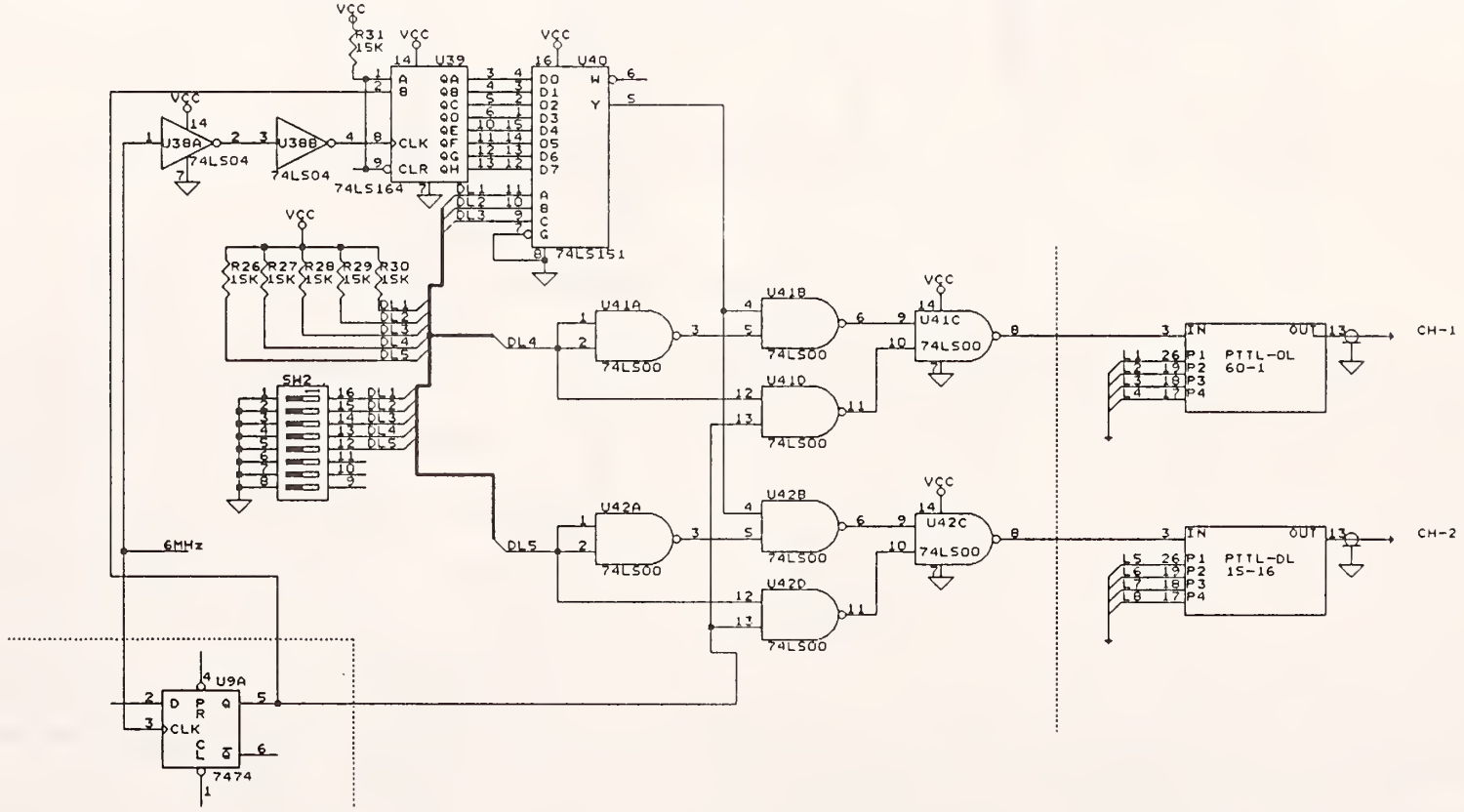


NIST		
High Accuracy Sampling Wattmeter 16-bit Amp./Data Curr. & Volt. Conv. Modules		
Title Ground Connection Schematic		
Size B	Document Number Drawing 17	REV 1.0
D:\WATMTR\GND\GND.SCH	Date: February 23, 1996	Sheet of



d:\uatmtr\blok-dia\sys-ps.sch

NIST		
High Accuracy Sampling Wattmeter		
Title: System power supply block diagram		
Size: B	Document Number: Drawing 18	REV: 1.0
Date: February 23, 1996	Sheet of	



U38 14P LS04
R26 R27 R28 R29 R30 R31
U39 14P LS164
U40 16P LS151
U41 14P LS00
SW2 16P
U42 14P LS00

SW2			DELAY
1	2	3	[nS]
ON	ON	ON	166.6
OFF	ON	ON	333.3
ON	OFF	ON	500.0
OFF	OFF	ON	666.6
ON	ON	OFF	833.3
OFF	ON	OFF	1000.0
ON	OFF	OFF	1166.6
OFF	OFF	OFF	1333.3

SW2		CH-1	CH-2
4	5		
OFF	OFF	NO ADDED DELAY	NO ADDED DELAY
OFF	ON	NO ADDED DELAY	ADDED DELAY
ON	OFF	ADDED DELAY	NO ADDED DELAY

NIST
High Accuracy Sampling Wattmeter
Freq. Counter and Prog. Time Delay Board

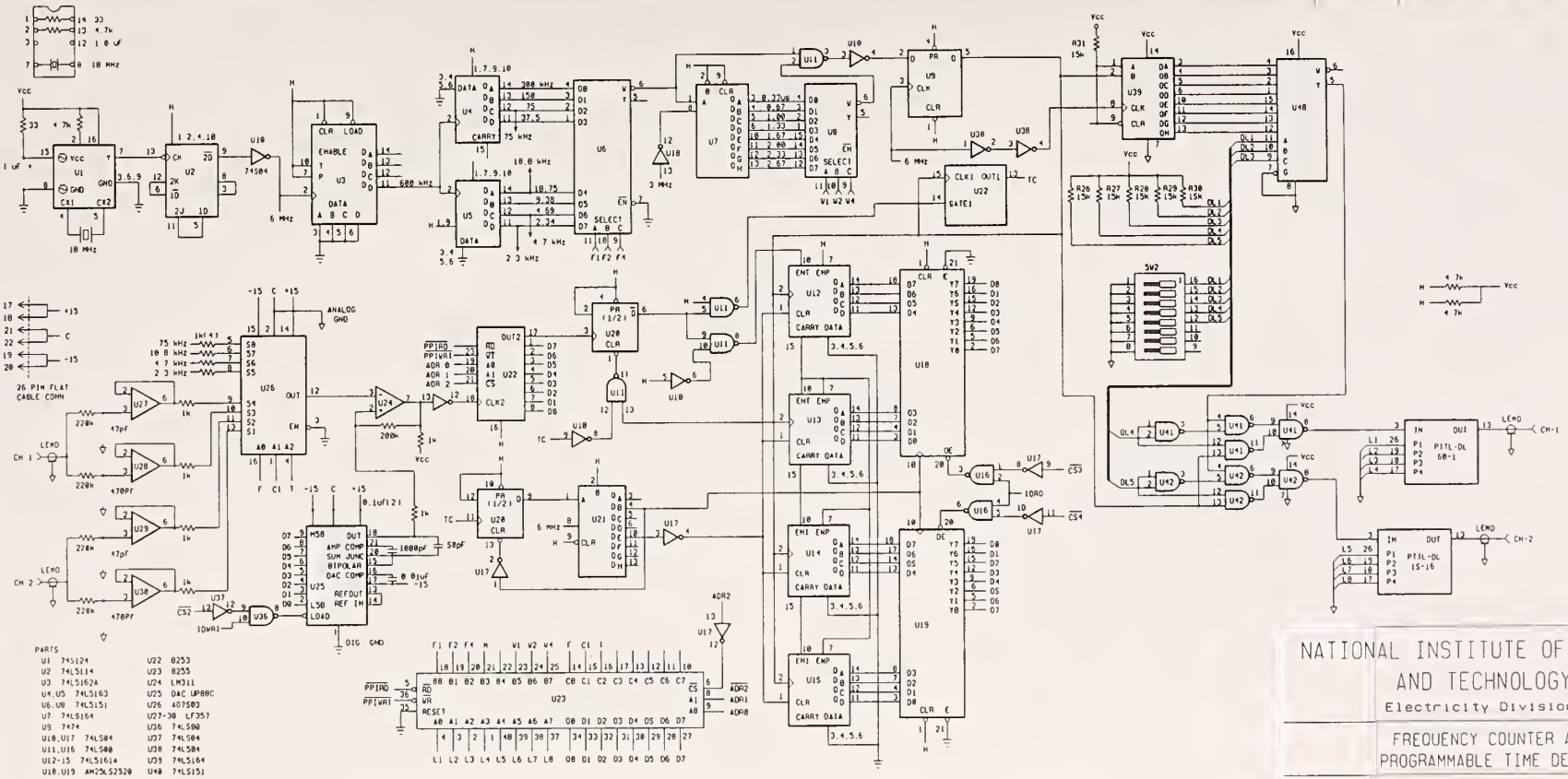
Title: Time delay extension

Size	Document Number	REV
B	Drawing 19	1.0

Date: January 14, 1991 Sheet of

D:\WATMTR\TD\TD.SCH

DATE	REVISION
05 MAY 91	REDRAWN AND ADDED U38-42



NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY

Electricity Division

FREQUENCY COUNTER AND PROGRAMMABLE TIME DELAY

For:

Date: 6-5-81 | Scale: | By GNS

Distances in INCHES

Tolerance:		
	X.X	+/-0.020
	X.XX	+/-0.010
	X.XXX	+/-0.001

Angles in DEGREES

	X	+/-1.0
	X.X	+/-0.2

Disc AMOS 051791 | Drawing 20

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