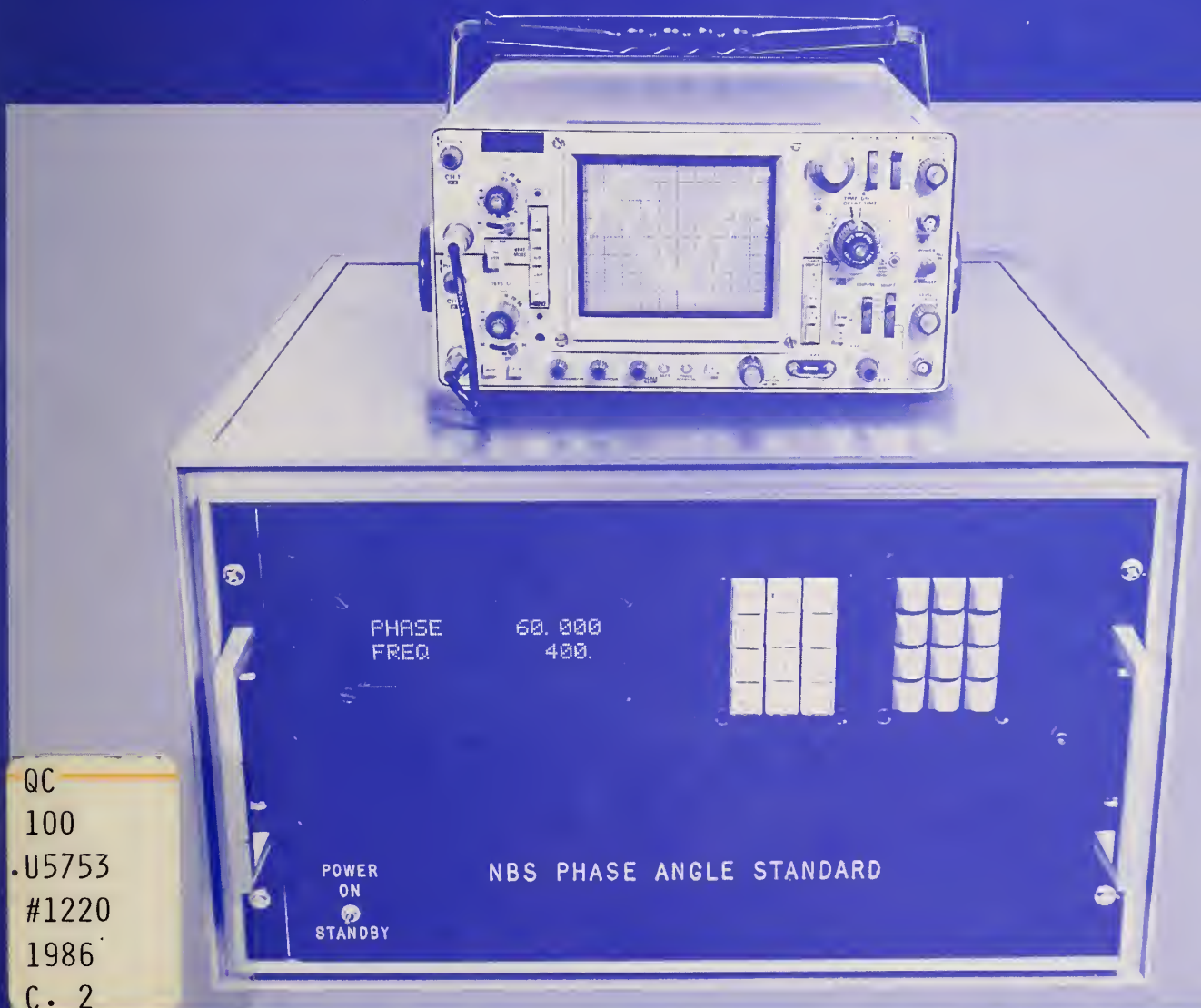
NBS Technical Note 1220

NBS 50 kHz Phase Angle Calibration Standard

R. S. Turgel



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[1]Headquarters and Laboratories at Gaithersburg, MD, unless otherwise noted; mailing address Gaithersburg, MD 20899.
[2]Some divisions within the center are located at Boulder, CO 80303.
[3]Located at Boulder, CO, with some elements at Gaithersburg, MD.

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Electrosystems Division
Center for Electronics and
Electrical Engineering
National Engineering Laboratory
National Bureau of Standards
Gaithersburg, MD 20899

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NBS 50 kHz PHASE ANGLE CALIBRATION STANDARD

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A detailed description is given of the features of an electrical phase angle calibration standard designed for operation over a frequency span of 2 Hz to 50 kHz. The phase resolution of this calibrator extends from just below 2 millidegrees at the low end of the frequency range to about 5 millidegrees at the high end. The uncertainty in the phase angle is a function of frequency, amplitude, and amplitude ratio of the two outputs. It varies from 5 - 50 millidegrees.

The phase angle calibration standard is a source of two sinusoidal signals with an accurately known phase angle between them. The signals are generated using digital waveform synthesis and are programmable in amplitude (0-100 V) and in frequency (2 Hz-50 kHz). Operation is controlled from a front panel keyboard, or remotely via an IEEE-488 bus interface, under control of a microprocessor. Selected signal parameters are displayed on an alpha-numeric readout and can be transmitted over the bus.

To ensure accuracy, the system uses an auto-zero feedback loop that compensates for residual differential phase shifts in the output amplifiers. The compensation scheme measures the departure of the output phase angle from true quadrature, for a nominal 90-degree setting, and applies a correction to the computation of the digital sine wave synthesis.

key words: calibration; digital waveform synthesis; phase angle; phase meter; sine wave generator; standard.

1. INTRODUCTION.

The present publication describes in detail the design and operation of an audio-frequency phase angle calibration standard, with a frequency range from 2 Hz to 50 kHz, constructed at the National Bureau of Standards (NBS). A previous version of this standard (with a maximum 5 kHz operating range) has been described in NBS Technical Note 1144 [1][1]. The development of these standards was undertaken because of a need to provide a high accuracy audio-frequency phase angle reference, so that both manufacturers and users of phase measuring equipment could obtain consistent measurements throughout industry and other user communities.

The work was sponsored, in part, by the Department of Defense through the Calibration Coordination Group (CCG) which has a particular interest in the phase angle standard. The publication of a detailed description of the instrumentation system was suggested by the CCG to encourage commercial production of a phase angle standard based on the NBS design.

The principle of operation was described in a 1978 paper [2] and many of the circuit details of the earlier, 5 kHz version can be found in [1]. The present publication contains a description of the changes in both hardware, software, and operating procedures for the 50 kHz version of the NBS Phase Angle Standard. The revised specifications are shown in table 1.1[2]

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[1] Numbers in brackets refer to the literature references listed at the end of this report.

[2] In order to describe the system discussed in this report adequately, commercial equipment and instruments are identified by their manufacturer's name or model number. In no case does such identification imply recommendation or endorsement by the National Bureau of Standards, nor does it imply that the material or equipment identified is necessarily the best available for the purpose.

Phase Angle:	
Range	-999.999 to +999.999 degrees
Resolution	0.0014 degrees (1 part in 2^{18})
Systematic Uncertainty (Equal Amplitude)	
at 60 Hz	0.003 degrees
at 400 Hz	0.004 degrees
at 5 kHz	0.008 degrees
at 15 kHz	0.016 degrees
at 30 kHz	0.027 degrees
at 50 kHz	0.040 degrees
Systematic Uncertainty (Amplitude Ratio 7:1)	
at 60 Hz	0.004 degrees
at 400 Hz	0.006 degrees
at 5 kHz	0.011 degrees
at 50 kHz	0.080 degrees
Output Frequency:	
Range	2 Hz to 50 kHz
Resolution	1 Hz up to 5 kHz; 10 Hz above 5 kHz
Accuracy	0.06 %
Stability	1 ppm
Output Amplitude:	
Effective Range	0.5 to 100.0 V rms
Resolution	steps of approx. 2 mV, up to 7 V steps of approx. 24 mV, 7 to 100 V
Accuracy	0.1 %
DC Offset Voltage	< 0.5 mV for Outputs to 7 V rms < 5 mV for Outputs 7 to 100 V rms

Table 1.1 Performance Specifications

2. DESIGN CONSIDERATIONS.

This section presents a brief overview of the features of the 50 kHz Phase Angle Standard that are significantly different from those of the 5 kHz version. Further information can be found in the appropriate sections describing the hardware and software in more detail.

2.1 Waveform Generation

The Phase Angle Standard is a signal source of two sine waves that are synthesized from sets of digital data. The digital data are computed so that the phase angle between the resulting pair of sine waves is precisely determined, and the data are then converted to sinusoidal voltages by dual digital-to-analog converters. This process is described in detail in [1]. As in the first version of the Phase Angle Standard, 16-bit digital-to-analog converters are used for output frequencies up to 5 kHz; these converters have the advantage of generating waveforms with high phase resolution, but are limited to maximum conversion rates of 400 kHz. Because of settling time limitations, the 16-bit converters cannot cope with the higher conversion rates needed to produce low distortion sine waves with frequencies from 5 kHz to 50 kHz. Therefore, for the upper range of frequencies, waveform generation is carried out by faster, 12-bit converters which permit 10 times higher conversion rates. The increase in speed is obtained at the cost of some loss of phase angle resolution as a consequence of the shorter word length. The implications of 12-bit quantization of the data used for waveform reconstruction on the theoretical and practical limitations of angular resolution are more fully discussed in [3].

The timing requirements for operating in the higher frequency range demand not only higher speed digital-to-analog converters, but also a change in operating mode. When synthesizing sinusoidal waveforms up to 5 kHz, a pair of new digital values is computed every 2.5 microseconds, an interval long enough for calculations to be carried out in real time. Above 5 kHz, however, when using the 12-bit digital-to-analog converters capable of up to 4 million conversions per second, the available interval is not sufficient for real-time calculations. The sets of selected values from which the waveform is reconstructed must therefore be calculated ahead of time and stored in random access memory. The stored values can then be transfered to the digital-to-analog converters at the required speed.

2.2 Quadrature Phase Detector

One of the critical components of the Phase Angle Standard system is the quadrature phase detector. It is part of the auto-zero feedback loop which corrects residual differential phase errors in the output amplifiers. The 5-kHz version of the NBS Phase Angle Standard uses resistive attenuators as part of the phase detector which are adequate for the lower frequency range, but unsuitable for the extended range up to 50 kHz. Therefore, the phase detector circuit has been redesigned to use binary inductive voltage dividers to

attenuate the signals to the appropriate levels. These voltage dividers are constructed with special torroidally wound transformers chosen for their low inherent phase errors [4].

Because inductive voltage dividers tend to saturate in the presence of even small dc currents, dc offset voltages in the signals to be attenuated have to be nulled. The dc offset in each channel is effectively removed by injecting a compensating current into the output amplifiers. The compensating current is adjustable under software control, and its magnitude is computed based on iterative measurements of the dc offset voltage by the system.

2.3 Instruction Set

The set of operating instructions for the Phase Angle Standard has been divided into two subsets; the Phase Calibration (normal) Mode and the Test (diagnostic) Mode. The first subset is almost identical with the operating instructions given in [1]; the diagnostic subset is designed to help with trouble-shooting procedures and provides more direct access to some of the hardware. The instruction set is more fully explained in chapter 3 below.

2.4 IEEE-488 Bus

An interface has been provided for a connection to an IEEE-488 bus which allows the Phase Angle Standard to be controlled remotely. Commands can be transmitted to the Phase Angle Standard and status information and messages can be returned to the instrument controller. Further details are given in chapter 5 on Hardware and chapter 6 on Software.

3. OPERATING INSTRUCTIONS

3.1 External Connections

(a) Power Cord. The power cord for the 120-volt 60-hertz line plugs into a receptacle at the left rear of the instrument. A 15-volt standby power supply is always energized whenever the cord is connected to the line.

(b) Output Connectors. The Reference and Variable output voltage signals are available through the lower two BNC connectors at the rear of the instrument.

3.2 Front Panel Controls

(a) Power Switch. The toggle switch on the left-hand side of the front panel controls a solid-state relay which connects the 120-volt power line to the instrument power supplies.

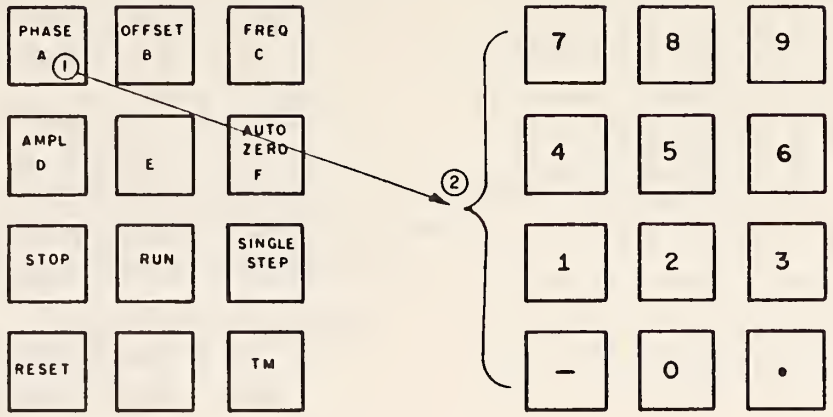
> Note: A 15-volt power supply remains on even when the switch is in the "off" (stand-by) position to provide the control current for the solid-state power relay.

(b) Keyboard. The Phase Angle Standard is operated from push-button keys on the front panel arranged as a 12-button Command keyboard and a 12-button Numerical keyboard. Ease of operation was an important criterion in the design and layout of the controls. In the normal phase angle calibration (PHASE CAL.) mode, the desired function is selected by pressing a command key and the operating parameters are then entered on the numerical keyboard. Details of these key entry sequences for various functions are shown in diagrammatic form in tables 3.1 to 3.6. Additional information can also be found in chapter 3 of [1]. With minor exceptions the main operating procedures are the same for the 5 kHz and 50 kHz versions of the Phase Angle Standard.

(c) STOP and RUN. In the normal (PHASE CAL.) mode the STOP and RUN function perform the following actions:

Actuating the STOP key inhibits further computation by the waveform generating microprocessor and sets the output amplitude to zero on both channels. Also, the default restart address of this microprocessor, "06," is set up internally and displayed on the readout. The address can be changed, if desired, by entering two hexadecimal digits. (For instance, a program starting at address "A0" provides dc output voltages proportional to phase angles or offset angles entered from the keyboard. This program can be used to test the digital-to-analog converters.)

PHASE ANGLE



(1) Select PHASE function.

(2) Enter phase angle on numeric keyboard.

Note: (a) Range: - 999.999 to 999.999 degrees.

Note: (b) 3 digits after the decimal point must be entered to complete entry.

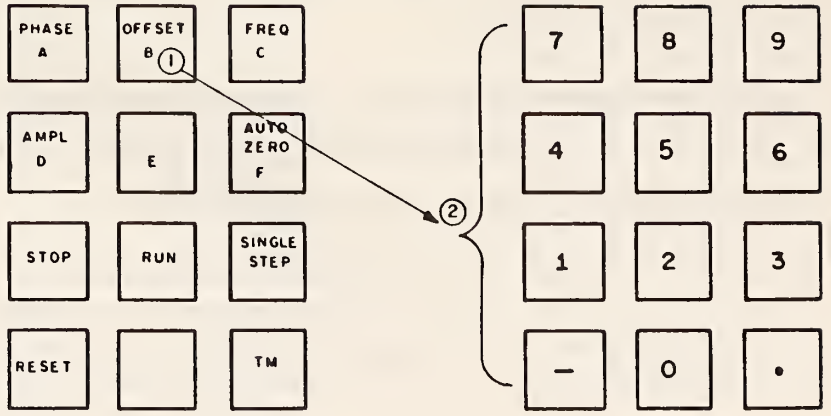
Note: (c) If 3 digits are entered ahead of the decimal point, the decimal point will be entered automatically.

(3) Repeat step (2) to enter new phase angle.

(4) To correct entry before entry is completed, repeat steps (1) and (2).

Table 3.1

OFFSET ANGLE



(1) Select OFFSET function.

(2) Enter offset angle on numeric keyboard.

Note: (a) Range: 999.999 to 999.999 degrees.

Note: (b) 3 digits after the decimal point must be entered to complete entry.

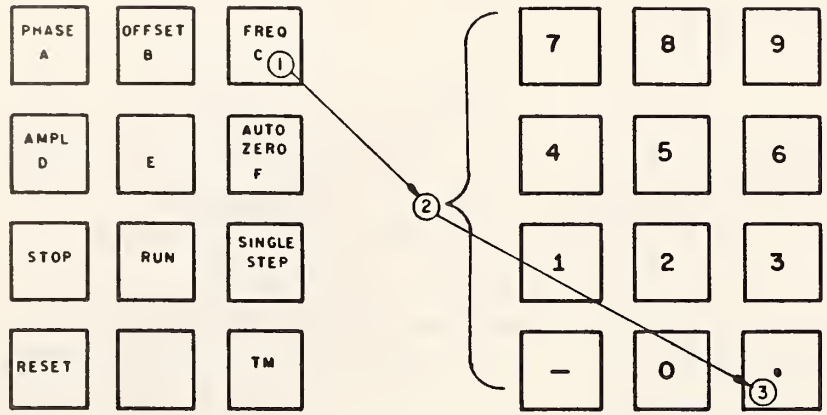
Note: (c) If 3 digits are entered ahead of the decimal point, the decimal point will be entered automatically.

(3) Repeat step (2) to enter new offset angle.

(4) To correct entry before entry is completed, repeat steps (1) and (2).

Table 3.2

FREQUENCY



(1) Select FREQUENCY function.

(2) Enter frequency in Hz.

Note: Range 2. Hz to 50000. Hz.

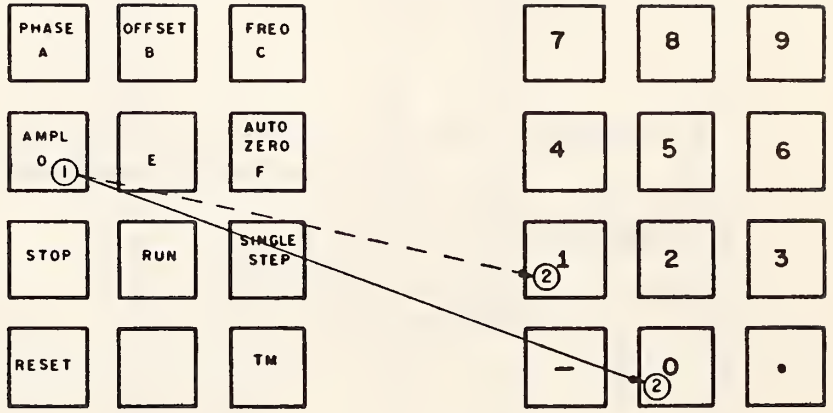
(3) Enter decimal point to complete entry.

(4) Repeat steps (2) and (3) to enter new frequency.

(5) To correct entry before entry is completed, repeat steps (1), (2), and (3).

Table 3.3

AMPLITUDE SETTING (PHASE CAL. MODE)



(1) Select AMPLITUDE function.

(2) Select either channel "0" (Reference), or channel "1" (Variable).

(3) Enter 4-digit output voltage (Volts, rms)

Note: Ranges 0.000 to 7.071
7.080 to 99.99
and 100.0

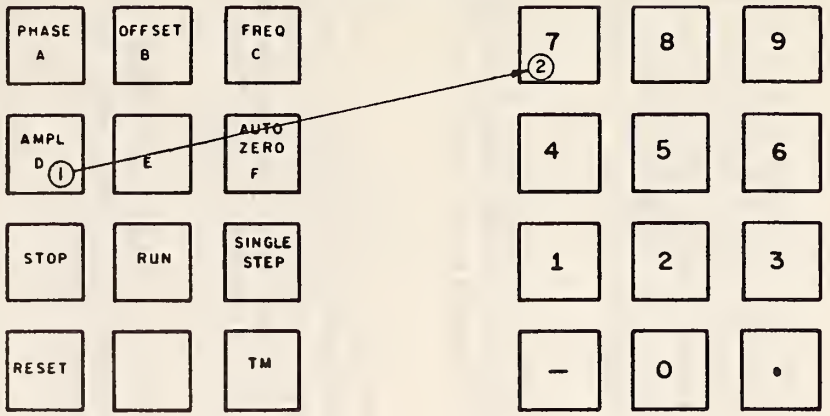
Note: Amplitude setting displayed on readout is rounded to 12-bit resolution.

(4) Repeat step (3) to enter new amplitude on the same channel.

(5) To correct entry before entry is completed, reapeat steps (1), (2), and (3).

Table 3.4

SEVEN-VOLT MODE



(1) Select AMPLITUDE function.

(2) Enter "7".

Note: The seven-volt mode connects the output of the filter amplifier directly to the output to provide a nominal 7.071 V rms.

Table 3.5

AUTO-ZERO

(1) Select AUTO-ZERO function.

Notes: (a) The auto-zero function should be activated whenever

(i) one amplitude is changed, or
(ii) both amplitudes are changed, or
(iii) the frequency is changed from the 2 Hz to 5 kHz range to above 5 kHz, or vice versa.

(b) To display corrections determined at each iteration of the auto-zero procedure, the TEST MODE must have been activated prior to selecting the AUTO-ZERO function by the following procedure:

(2) Select TEST MODE.

(3) Select normal mode [RUN Key].

(4) Select AUTO ZERO.

Table 3.6

When the RUN key is subsequently pressed, the amplitudes are restored to their previous values, and the waveform generating microprocessor restarts at the address indicated ("06" for normal operation).

Note: If the RUN key is activated without first operating the STOP function, an error condition will exist because no starting address for the microprocessor has been set up. The error condition can be cleared by operating any other (valid) command key.

(d) RESET. The RESET key is linked directly to the display and keyboard control microprocessor and restarts the Phase Angle Standard to its default (power-on) setting, whatever its present state. It can be used to reinitialize the system in case of a temporary malfunction, or if the system does not restart by itself after external power is interrupted.

(e) Test Mode. In addition to the normal operating mode (PHASE CAL. MODE), the Phase Angle Standard can be switched to a TEST MODE. This mode allows more direct interaction with certain hardware components for diagnostic purposes. It provides the capability to access microprocessor memory locations which store the signal amplitude and attenuator settings in binary form and to modify these values from the keyboard. With a suitable choice of entered values, individual bit-lines leading to the output amplitude and phase detector attenuator control can be checked (using the AMPL key or the PHASE key respectively). At the same time the relays associated with these functions can be tested.

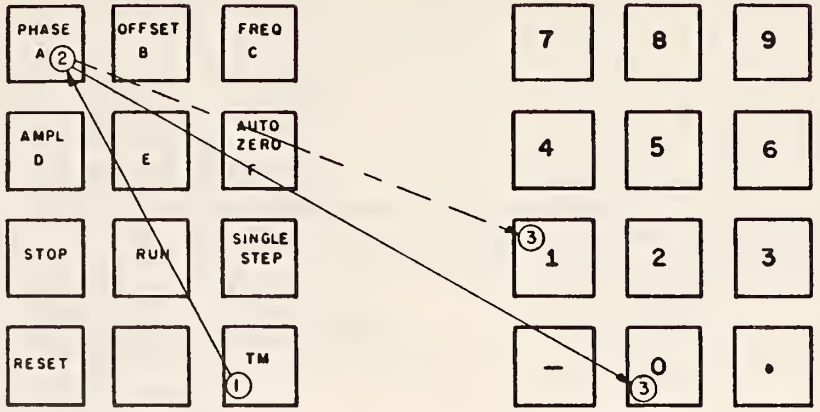
Other test functions available in the TEST MODE permit exercising of the signal channel interchange relay which is located at the input to the phase detector circuit (using the STOP key), digital measurement of the phase detector output (SINGLE STEP key), manual and automatic adjustment of the dc offset in both output channels (OFFSET key), and changing the tolerance and delay parameters used with the auto-zero procedure (blank key between RESET and TM).

The TEST MODE also provides a readout of the auto-zero correction determined by the system at both the auto-zero frequency and the current operating frequency (AUTO ZERO key). This information is useful as a check of the auto-zero performance.

To accommodate the instructions for the extra functions of the test mode and entry of hexadecimal numbers without adding additional keys, multiple key-stroke commands are necessary. These begin with the TM key (lower right-hand command key) followed by one or more command keys and hexadecimal number entries. Details of key-stroke sequences required for various functions can be found in tables 3.7 to 3.14.

Note: For hexadecimal entries in the TEST MODE, the command keys marked A to F are used in addition to the numerical keyboard.

PHASE DETECTOR ATTENUATOR SETTING



(1) Select TEST MODE.

(2) Select PHASE Detector Attenuator.

Note: Display shows position of channel reversing switch.

(3) Select either channel "0" (REF), or
channel "1" (VAR).

(4) Enter four hexadecimal digits.

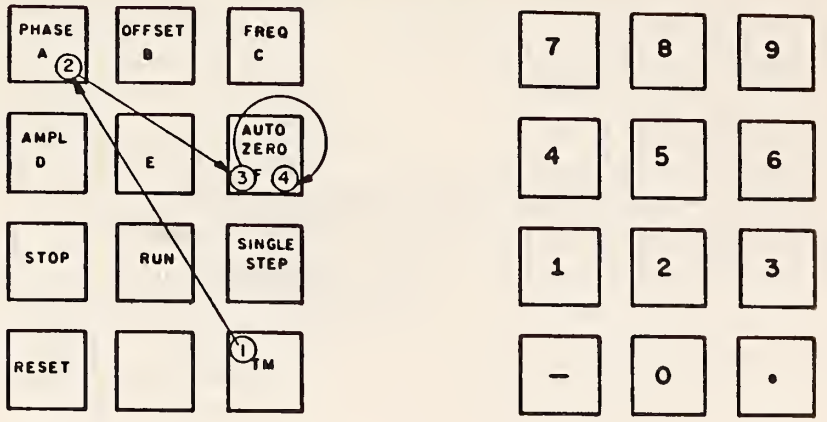
1st and 2nd digit - 00 to 7F control attenuator relays
3rd digit - no function
4th digit - if digit is odd (least significant bit "High")-low range
(0-7 volts)

- if digit is even (least significant bit "Low")-high range
(7-100 volts)

Note: The attenuator is disconnected if bit 1 is "High"
(4th digit is either 2, 3, 6, 7, A, B, E, or F)

Table 3.7

AUTOMATIC PHASE DETECTOR ATTENUATOR SETTING



(1) Select TEST MODE.

(2) Select ATTENUATOR.

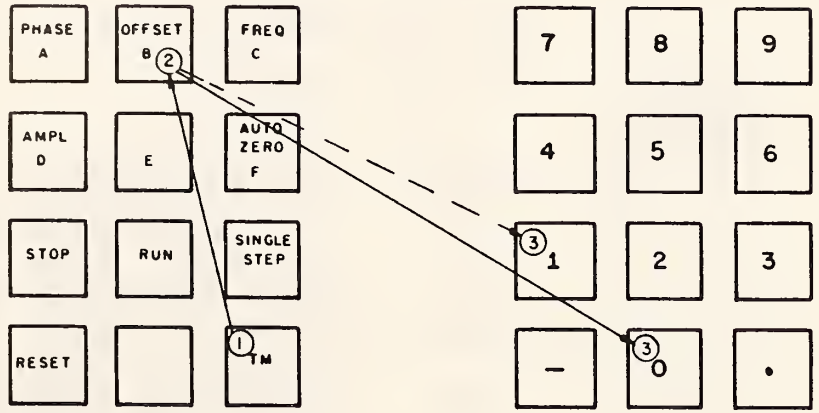
(3) Set both attenuators automatically to appropriate values for auto-zero operation and display channel "0" setting.

(4) Display channel "1" setting.

Note: Second line of display shows position of channel reversing switch.

Table 3.8

OC OFFSET CONTROL



① Select TEST MOOE.

② Select OC OFFSET.

③ Select either channel "0" (REF.) or channel "1" (VAR).

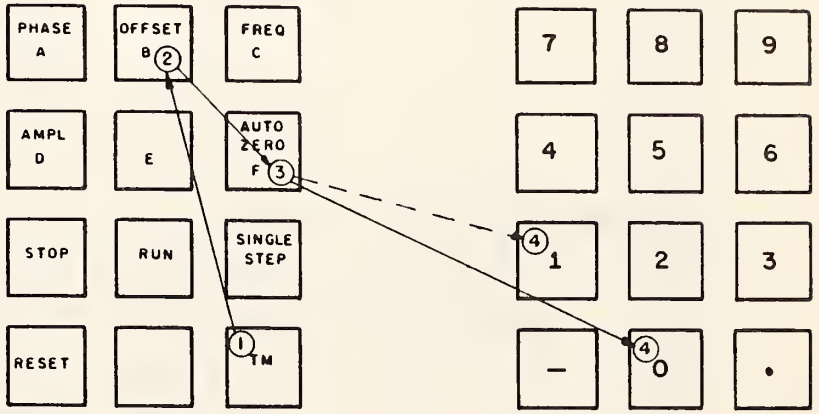
④ Enter two hexadecimal numbers.

Note: Second line of display shows dc offset as measured by "Oigitizer". (Hexadecimal numbers in two's complement).

⑤ Repeat step ④ if desired.

Table 3.9

AUTOMATIC DC OFFSET CONTROL



① Select TEST MOOE.

② Select OC OFFSET.

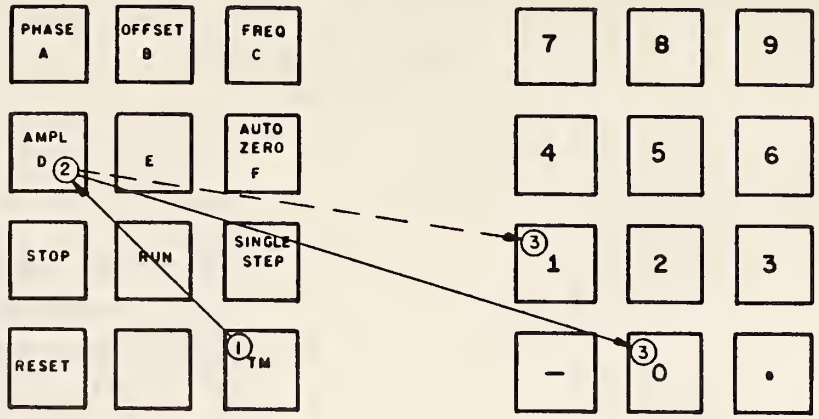
③ Select Automatic Operation.

④ Select either channel "0" (REF) or channel "1" (VAR).

Note: Second line of display shows dc offset as measured by "Oigitizer". (Hexadecimal numbers in two's complement).

Table 3.10

AMPLITUDE SETTING (TEST MODE)



(1) Select TEST MODE.

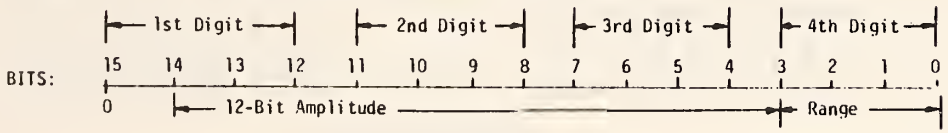
(2) Select AMPLITUDE.

(3) Select either channel "0" (REF) or channel "1" (VAR).

(4) Enter 4-digit hexadecimal numbers.

Repeat step (4) if desired.

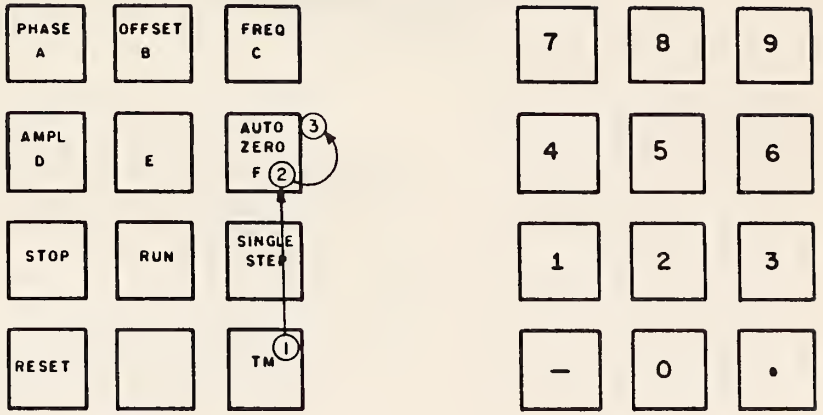
Hexadecimal Amplitude Control Format:



0-7 V Range Bit 0 High
7-100 V Range Bit 0 Low
7-Volt Range Bit 0 & Bit 1 High
16-Bit Converter Bit 2 Low
12-Bit Converter Bit 2 High

Table 3.11

DISPLAY OF AUTO-ZERO CORRECTION



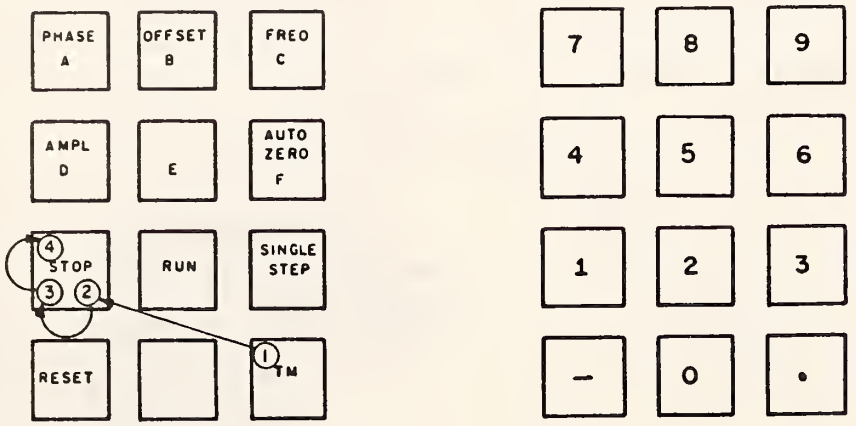
(1) Select TEST MODE.

(2) Display auto-zero correction adjusted for selected output frequency.

(3) Display auto-zero correction as determined at 4096 Hz or 32.77 kHz.

Table 3.12

CHANNEL REVERSING SWITCH
(of PHASE DETECTOR)



① Select TEST MODE.

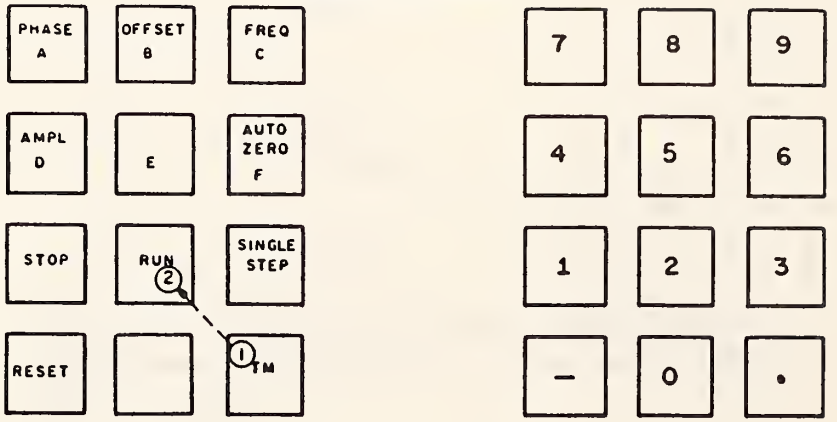
② Select CHANNEL SWITCH [STOP Key].

③ NORMAL position.

④ REVERSE position.

Table 3.13

RETURN FROM TEST MODE TO
NORMAL OPERATING MODE

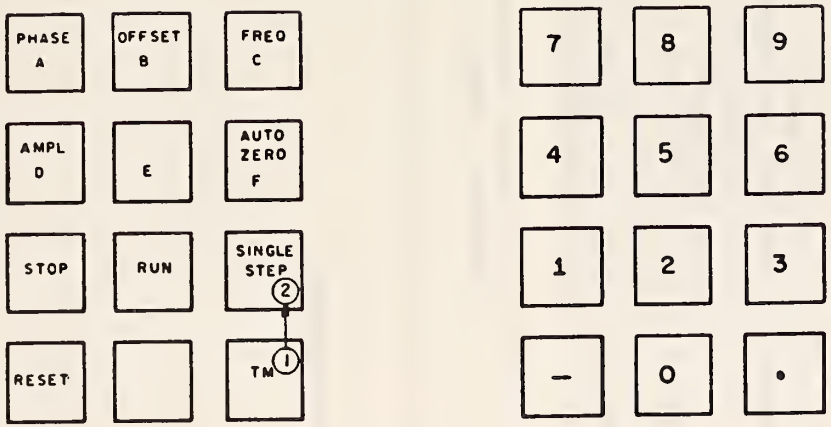


① From any TEST MODE operation.

② Select PHASE CAL. MODE [RUN Key].
(Normal operating mode).

Table 3.14

DIGITIZER (A/D CONVERTER)



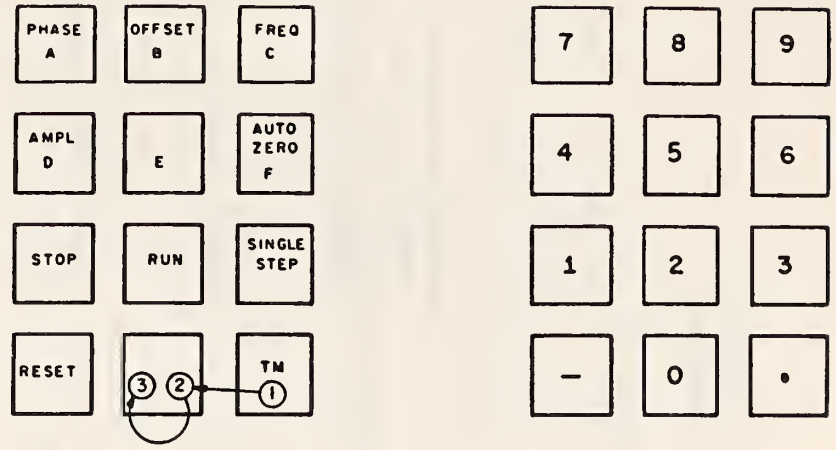
① Select TEST MODE.

② Convert and display output from Phase Detector Circuit Board [SINGLE STEP Key].

Note: Repeat step ② for additional conversions.

Table 3.15

READING DELAY (WAIT) AND AUTO-ZERO TOLERANCE ADJUSTMENT



① Select TEST MODE.

② Select delay time (WAIT).

Enter 4-digit hexadecimal number (decimal equivalent ≈ milliseconds).

③ Select auto-zero tolerance.

Enter 4-digit hexadecimal number.

Note: (a) Number entries are optional and can be repeated to make changes in delay time or tolerance setting.

(b) A "0000" entry will set default values for either delay time or tolerance.

Table 3.16

3.3 Error Messages

Table 3.17 shows the error messages the system can display and the remedial action to be taken.

ERROR MESSAGE	FAULT	REMEDIAL ACTION
HIGH FREQUENCY	Frequency selected above 50 kHz	Enter correct frequency
LOW FREQUENCY	Frequency selected below 2 Hz	Enter correct frequency
HIGH VOLTAGE	Amplitude selected above 100 volts	Enter correct amplitude
SYSTEM STOPPED	Waveform generating processor clock stopped	Push 'STOP,' then 'RUN,' enter frequency, or 'RESET'
FIFO FULL	Command register overflow	Reset system, push 'RESET'
DC OFFSET	Dc offset adjustment out of range	Readjust dc offset controls on the appropriate Output Circuit Board
PROM 1 (2,3,4,5)	Read-only memory faulty or misread	Retry 'RESET,' if fails, replace PROM integrated circuits (Ckt. Bd. D11)
UNDEFINED FUNCT.	Illegal entry	Re-enter command or parameter

Table 3.17 Error Messages

4. OPERATING PRINCIPLES

4.1 Introduction

As already briefly mentioned in chapter 2, the Phase Angle Standard generates two sinusoidal output waveforms with an adjustable and accurately known relative phase angle. The output sine waves can be applied directly to a phase meter under test to check its calibration.

The phase angle, frequency, and amplitudes for each channel can be set from the front panel keyboard or from a controller using the IEEE-488 bus. The key strokes entered, or message data bytes sent over the IEEE-488 bus, are interpreted by an 8-bit microprocessor that converts the ASCII format of the commands and operating parameters into an internal binary code. The internal code in turn controls the functions of the Phase Angle Standard and routes commands and data over various busses or dedicated lines. A generalized block diagram of the system is shown in figure 4.1.

The output waveforms are generated by a digital signal processor consisting of a high-speed 20-bit microprocessor, dual-channel digital-to-analog converters, low-pass filters, and amplifiers. The internal arrangement of the 20-bit processor and its instruction code are described in detail in chapter 5 of [1].

4.2 Method of Signal Generation

The output waveforms are generated by direct digital synthesis. Sets of data points, spaced at equal time intervals along the waveforms, are calculated so that they correspond to instantaneous values of the amplitude, as shown in figure 4.2. The digital data are converted to voltages using dual-channel digital-to-analog converters followed by amplifiers with appropriate filtering to remove the harmonic components introduced by the sampled-data process. A more complete description of the basic waveform generation scheme can be found in [1]. As pointed out already in chapter 2, the details of the process vary somewhat with the frequency range.

Functional Block Diagram of NBS Phase Standard

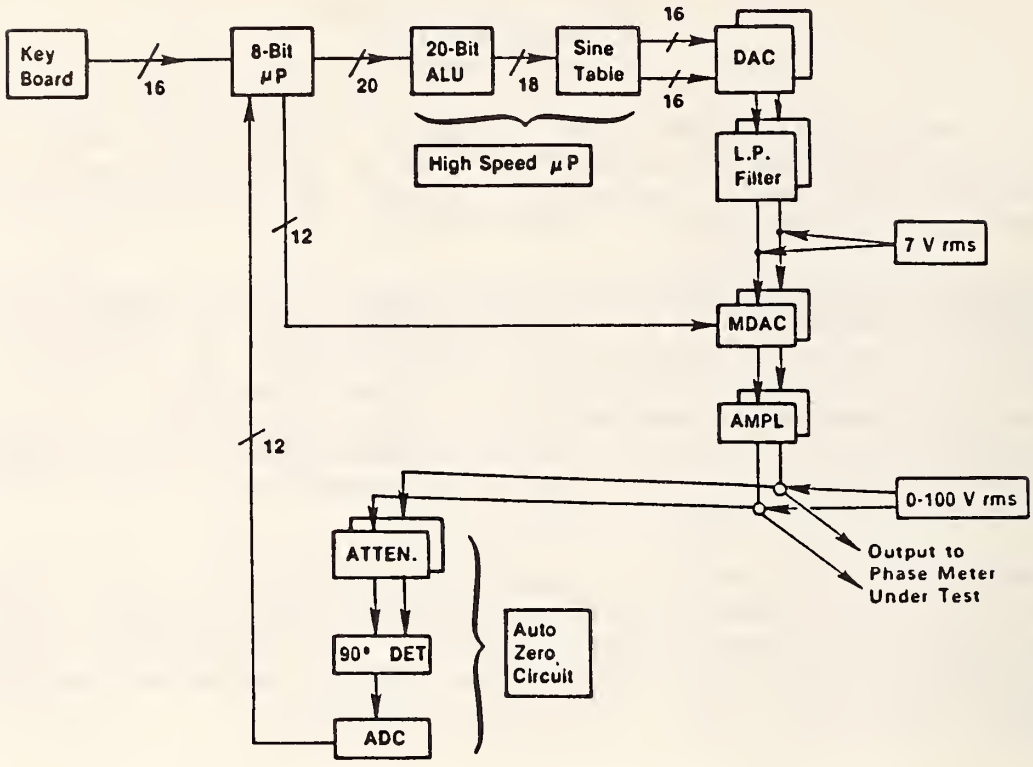


Figure 4.1

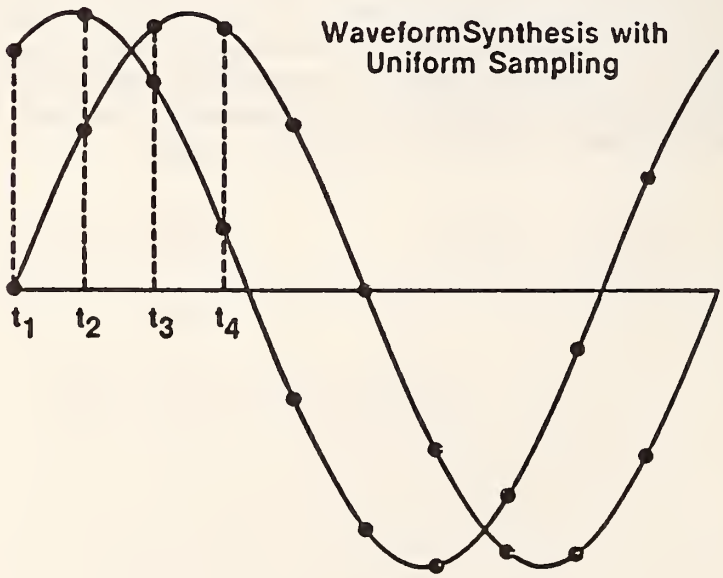


Figure 4.2

4.2.1 Signal Generation from 2 Hz to 5 kHz

For sinusoidal output frequencies up to, and including, 5 kHz, the digital data from which the waveforms are synthesized are computed in real time. The number of sample points per waveform is selected from a binary sequence with 64 samples at the highest frequency, 5 kHz, and increasing up to 131072 samples at 2 Hz. The number of samples is chosen so that the sampling rate remains in the band from 200 kHz to 400 kHz for all sinusoidal output frequencies in the range from 2 Hz to 5 kHz. Referring to figure 4.2, the sampling points, t_i, along the time axis are equivalent to "instantaneous" phase values for each sinusoid, referenced to the appropriate zero crossing. The choice of the two initial phase values, at time t_1, then determines the relative phase angle of the output waveforms. The calculations for a set of data points involve the following steps:

(a) determination of the "instantaneous" phase value for each of the two waveforms,

(b) computing the sine function for the instantaneous phase values,

(c) storing the computed values for each channel so that they are available to be applied to the digital-to-analog converters at the proper time, and

(d) determining the appropriate sampling time intervals.

(a) Two 20-bit accumulators, one for each channel, compute and store the instantaneous phase values. The initial value loaded into the accumulator is the binary equivalent of the phase angle (or offset angle) entered through the keyboard. For each subsequent data point, a phase increment (equivalent to 360 degrees divided by the number of sample points per waveform) is added until the waveform is completed. To start the next waveform, the initial phase value, or a new value, is reloaded into the accumulator and the computing procedure is repeated.

(b) The instantaneous phase values from the accumulator are converted to their corresponding sine function using a look-up table and interpolation algorithm which is implemented in a special hardware module. The resulting angular resolution is 2^{18} (0.0014 degrees) and the sine value is expressed as a 16-bit, two's complement number. The total conversion time is less than 400 ns. The Angle-to-Sine/Cosine Converter circuit board is described in more detail in [1].

(c) The pair of sine values required for each data point are calculated sequentially, and the results of the calculation are stored in corresponding locations of two banks of 1024-word random access memories. The modulo-1024 memory address register, pointing to the current location in memory, is incremented after every read operation, so that every memory location is traversed in rotation.

(d) During a memory read operation a strobe pulse, derived from a crystal controlled frequency synthesizer, latches the 16-bit data into each digital-to-analog converter channel. The synthesizer has four decimal digits of resolution in each of the two frequency ranges used (200-400 kHz; 2-4 MHz), and the strobe frequency is set by the 8-bit system control microprocessor. The microprocessor uses a look-up table to determine the number of sample points per waveform, and then calculates the strobe pulse rate so that the desired sinusoidal output frequency of the Phase Angle Standard is obtained .

The numerical data latched into each converter channel are held stable until the next strobe pulse enters new data. During the stable period, the data are fed to the digital-to-analog converters and are finally converted into output voltages while at the same time the next pair of values is computed.

4.2.2 Signal Generation from 5 to 50 kHz

While it is necessary to store only one digital word at a time for each channel for outputs up to 5 kHz, the entire set of points on a particular waveform must be stored in the random access memory for the frequency range from 5 kHz up to 50 kHz . Complete waveform storage is necessary because the digital-to-analog conversion rate required at these frequencies does not provide a long enough time interval between data points for real-time calculations.

Each data point of a set that defines the waveform is computed and stored in one of the 1024 locations of the memory bank using the same procedure as for low frequency generation. The strobe frequency (timing pulse rate) is set equal to one tenth of the final conversion rate which leaves enough time to carry out the calculations. As soon as all the data are stored, further computation is inhibited by trapping the waveform generating microprocessor in a "do-nothing" program loop. The strobe pulse rate from the independent frequency synthesizer is then increased by a factor of ten, so that the output sine wave of the Phase Angle Standard has the desired frequency. This rate change is accomplished by changing the least significant bit of the range setting which switches the crystal controlled frequency synthesizer to its next higher range (x100 kHz to x1 MHz).

As before, the number of data points per waveform is selected from a binary sequence with a minimum of 64 samples at the highest output frequency, 50 kHz, and increasing the number of samples to 1024 at output frequencies just above 5 kHz. The choice is made so that the resulting sampling rate (strobe frequency) falls in the 2-to 4-MHz band.

4.3 Digital-to-Analog Converters

To accommodate the conversion rates for both frequency ranges, two types of digital-to-analog converters are necessary. For output frequencies from 2 Hz to 5 kHz, a 16-bit converter is used which settles in 2.5 microseconds, the minimum time interval between strobe pulses in that range. The advantage of the 16-bit digital-to-analog converter is its inherent low quantization noise and therefore lower harmonic distortion in the sine waves synthesized from its output. Also, the 16-bit word length, coupled with a minimum number of 64

samples per waveform, permits a theoretical phase resolution of better than 0.001 degrees with the waveform reconstruction scheme employed [3].

In the upper frequency band, from 5 kHz to 50 kHz, the available time between strobe pulses can be as short as 0.25 microseconds, so that faster 12-bit digital-to-analog converters must be used. The 12-bit wordlength limits the theoretical phase resolution that can be achieved and raises the harmonic distortion of synthesized sine waves because of higher quantization noise. However, with 64 samples per waveform, theoretical analysis shows that an average resolution of better than 0.005 degrees is still possible (see reference [3]).

The stepped sine waves produced by either the 16-bit or 12-bit digital-to-analog converters are passed through low-pass filters which remove the harmonics introduced by the sampled-data process. For each converter type, separate active filters are used with cut-off frequencies appropriate for the respective sampling rates.

4.4 Output Amplifiers

As shown in figure 4.1, the seven-volt signal passes from the active low-pass filter to the programmable amplitude control (multiplying digital-to-analog converter, MDAC in the figure) where it is attenuated with a resolution of 2^{12} steps. The attenuated signal is then passed through a low-voltage amplifier to provide 0 to 7.07 volts at the output terminal. For output voltages from 7.07 to 100 volts, an additional amplifier is inserted into the signal path with a (nominal) fixed gain of 14.14. Because the additional amplifier introduces a 180-degree phase shift, a compensating adjustment in the output phase angle is made by the waveform generating microprocessor.

The gain-adjustable amplifiers can be bypassed by selecting the SEVEN-VOLT-MODE from the keyboard. The output is then taken directly from the active filter with a nominal amplitude of 7.071 volts. To minimize differential phase shifts caused by the amplifiers, both channels are simultaneously switched to the Seven-Volt-Mode. Resetting either channel to a different amplitude also switches the other channel from the Seven-Volt Mode to the gain-adjustable mode at a nominal amplitude setting of 7.07-volt.

4.5 Auto-Zero Correction

The output amplifiers, and particularly the filter circuits, are carefully matched so that corresponding channels on the two output circuit boards have nearly identical frequency response characteristics. The match cannot be perfect, however, and small residual differential phase errors will remain and have to be corrected. The auto-zero procedure measures the deviation from the ideal response at quadrature and applies the result of the measurement to the waveform generating circuits in the form of a digital phase angle correction.

Because of the well matched filter characteristics, the differential phase errors vary essentially linearly with frequency in each of the two frequency ranges. It is therefore sufficient to carry out the auto-zero determination at only one frequency in each range, and the appropriate

correction for the actual frequency in use is then calculated. The two values chosen for the auto-zero determination, 4096 Hz and 32.77 kHz (32768 Hz rounded up), are convenient, numerically, for calculating the corrections at other frequencies. Also, these frequencies lie near the upper end of their respective ranges where the error is larger.

The iterative auto-zero procedure repeatedly determines the departure from true quadrature of the output of the Phase Angle Standard and applies a correction to the waveform generator until the quadrature error falls within preset tolerances. The default values of the tolerances for the low and high frequency ranges are approximately equivalent to 2.75 and 5.5 millidegrees respectively.

To eliminate any possible errors in the phase detector itself, measurements are made at +90 and -90 degrees, and again with the signal channels interchanged. Internal feedback in the phase detector compensates for possible dc offsets in the input signals, reversing the 90-degree angles compensates for dc offsets in the output of the phase detector, and interchanging channels compensates for possible phase offsets in the detector circuitry.

Before actually measuring the quadrature error, the auto-zero procedure performs a self-calibration to determine the sensitivity of the detector circuit for the particular signal amplitudes applied. The sensitivity calibration factor establishes the relation between the phase detector output voltage and the angular correction necessary to modify the output of the waveform generator. To prevent overshoot when the correction determined by this procedure approaches its final value, the incremental angular correction resulting from the iteration is reduced below the calculated value (by a factor of two) when the quadrature error is within twice the tolerance value. This more gradual approach to the final value generally will add only one or two additional iterations, but, on the other hand, it will prevent prolonged oscillation around the final level of the correction in most cases.

Since the phase detector must handle a wide range of input signals, programmable attenuators condition the signal in each channel. As indicated in chapter 2, the attenuators consist of specially wound torroidal, 7-bit, binary inductive voltage dividers that have very low inherent phase shift. The input and the output of the dividers are buffered with operational amplifiers. When the Phase Angle Standard is not in the auto-zero mode, the attenuators are disconnected from the circuit, but the phase detector input amplifiers always remain in the circuit so that they present a constant load to the outputs of the Phase Angle Standard. With the attenuators disconnected, either signal from the output of the Phase Angle Standard can be routed through the phase detector input amplifier directly to the digitizing circuit to measure its dc-offset voltage.

The voltage output from the phase detector circuit board is connected to the Digitizer Circuit Board (A13), where it is filtered and amplified by an instrumentation amplifier before being digitized using a 12-bit, dual-slope analog-to-digital converter. The filtering removes the ripple from the quadrature detector stage during the auto-zero determination and removes the ac component from the signal when measuring the dc offset. A differential input connection prevents small voltage differences between ground planes of the two circuit boards from introducing offsets into the signal.

After the final auto-zero correction has been determined, the output phase angle is set to zero and the frequency originally selected is restored. The correction is adjusted for the frequency in use, and it is applied automatically to any subsequent phase angle setting until another auto-zero procedure is performed.

5. 50-kHz HARDWARE MODIFICATIONS.

5.1 General Remarks.

In redesigning the NBS Phase Angle Standard to extend its frequency range to 50 kHz, it was possible to use the same backplane connections as in the 5-kHz version of the standard with few exceptions. This was a convenience, particularly during the transition stage when both sets of circuit boards could be operated in the same system. As development work progressed, a few additional backplane connections were installed without destroying the compatability with the circuit boards of the 5-kHz version.

To reduce heat and power dissipation, all relays on the Output and Phase Detector circuit boards are of the latching type, and the necessary switching pulses are generated by a combination of relay driver logic hardware and software. Major circuit changes involve the Output, Phase Detector, Digitizer, and Memory-Latch boards. Only relatively minor modifications have been necessary in the Synthesizer (strobe pulse generator) and microprocessor circuit boards. A special board has been added for the IEEE-488 bus interface. The arrangement of the circuit boards in the card cage as viewed from the front panel access door is shown in figure 5.1

5.2 Output Circuit Board.

The circuit boards located in position A7 and A9 generate the two Phase Angle Standard output voltages. These two boards are identical and contain the analog waveform generating circuits and the amplitude control circuits (figure 5.2a).

5.2.1 Waveform Generating Circuits

The digital data, from which the output waveform is generated, are transfered from memory to a set of latches on the Memory-Latch circuit board (D4) with every strobe pulse. The output data from these latches is then connected by separate, dedicated 16-bit busses to the Output Circuit Boards (A7 and A9) where the data are again latched into a pair of octal registers, U1-U2. The double latching buffers the data and helps to reduce noise picked up during transfer from the Memory to the Output circuit. The second latch delays the information by an additional clock (timing pulse) period but does not affect the throughput rate.

As shown in the circuit diagram, figure 5.2, the input pins of the 16-bit and 12-bit digital-to-analog converters (U3 and U4) are connected in parallel to the output of the 16-bit latches so that the 12 most significant bits always feed both converters simultaneously. The current outputs of each converter are connected to the summing junction of a separate active filter (AR2-AR3 and AR1) which has a 3-dB frequency of 25 kHz (4-pole Butterworth) or

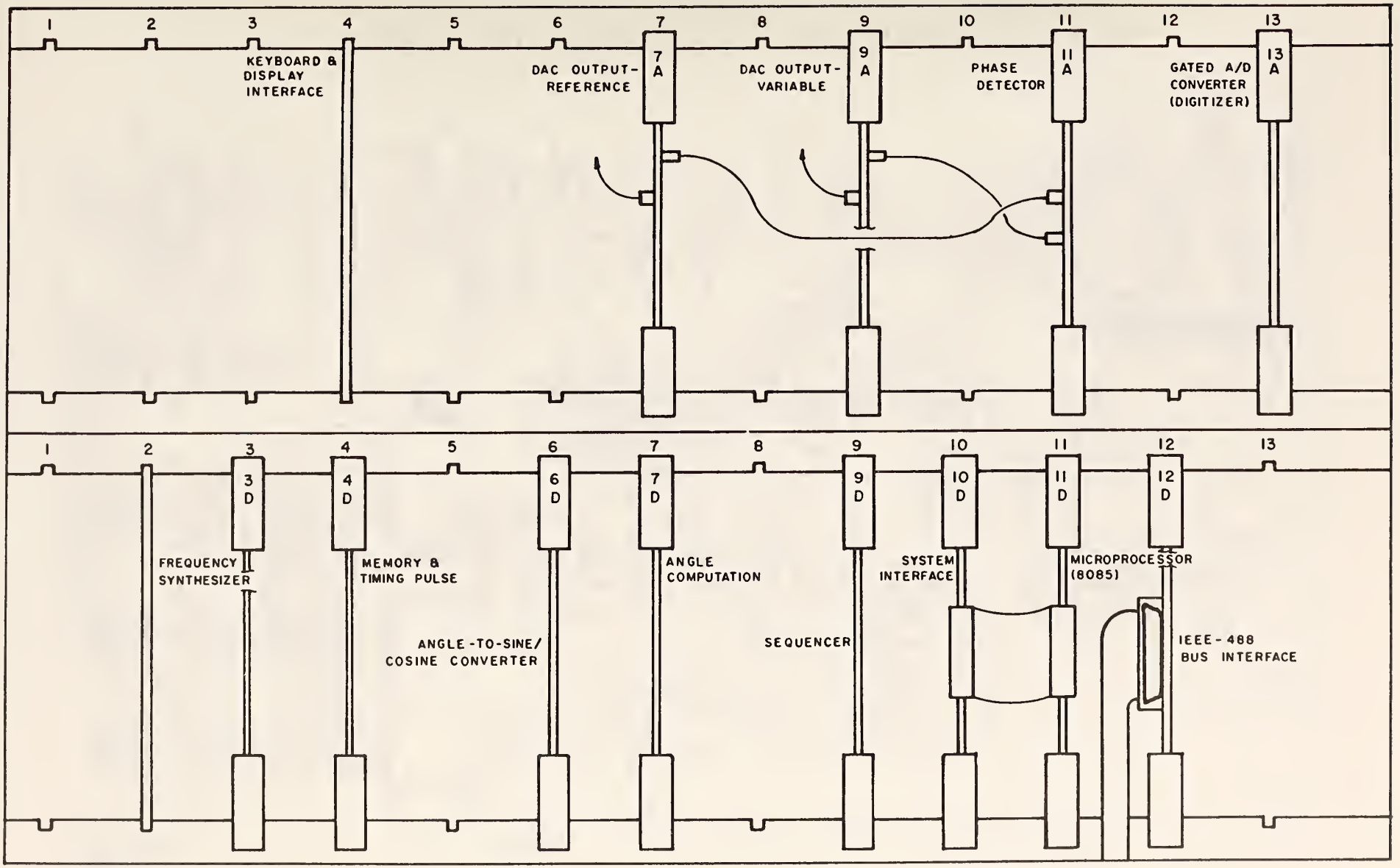
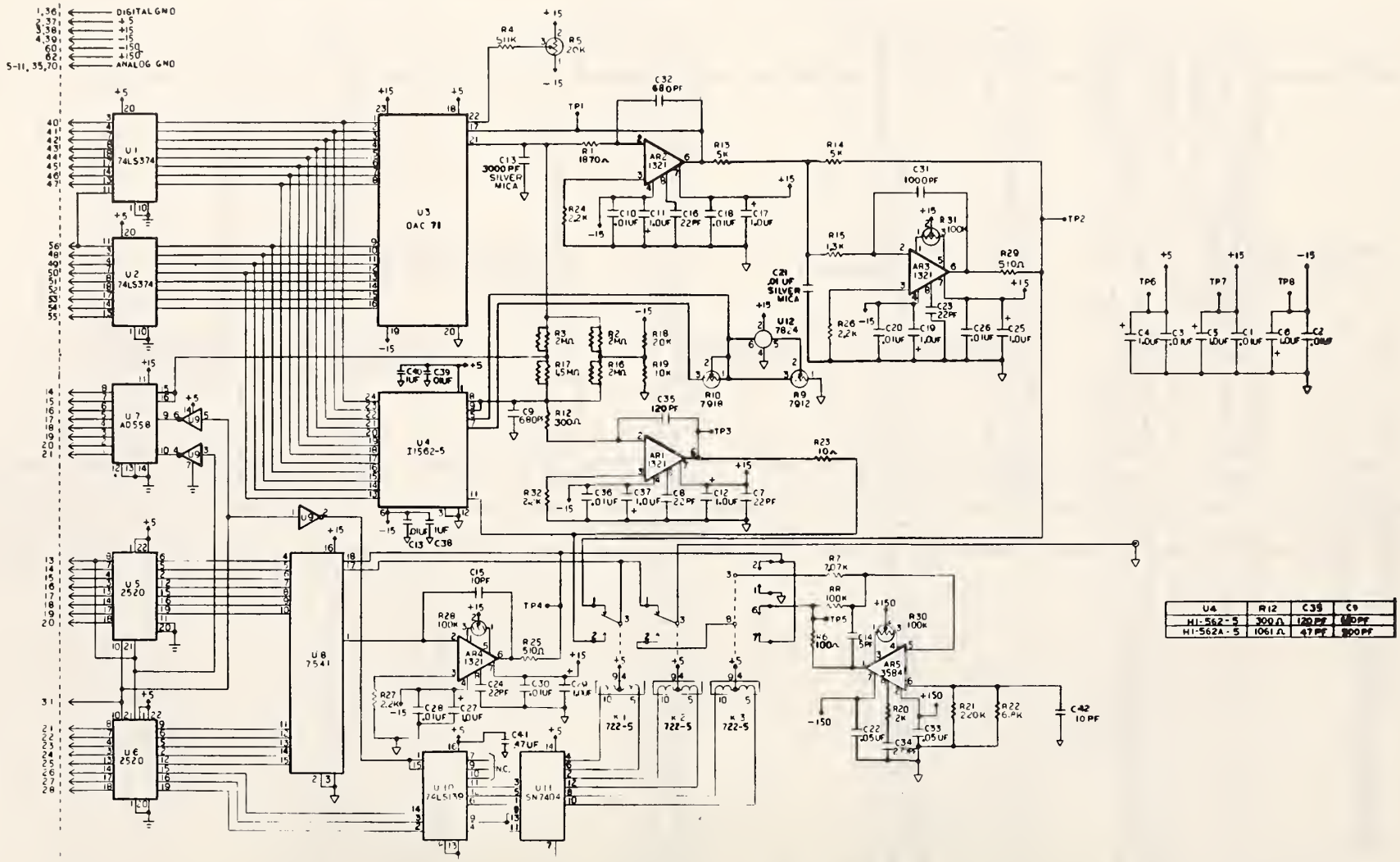


Figure 5.1 Circuit Board Arrangement, Card Cage (Front View)



U4	R12	C38	C9
HI-562-5	300Ω	120PF	680PF
HI-562A-5	1061Ω	47PF	300PF

Figure 5.2(a) Output Circuit Board (Schematic Diagram)

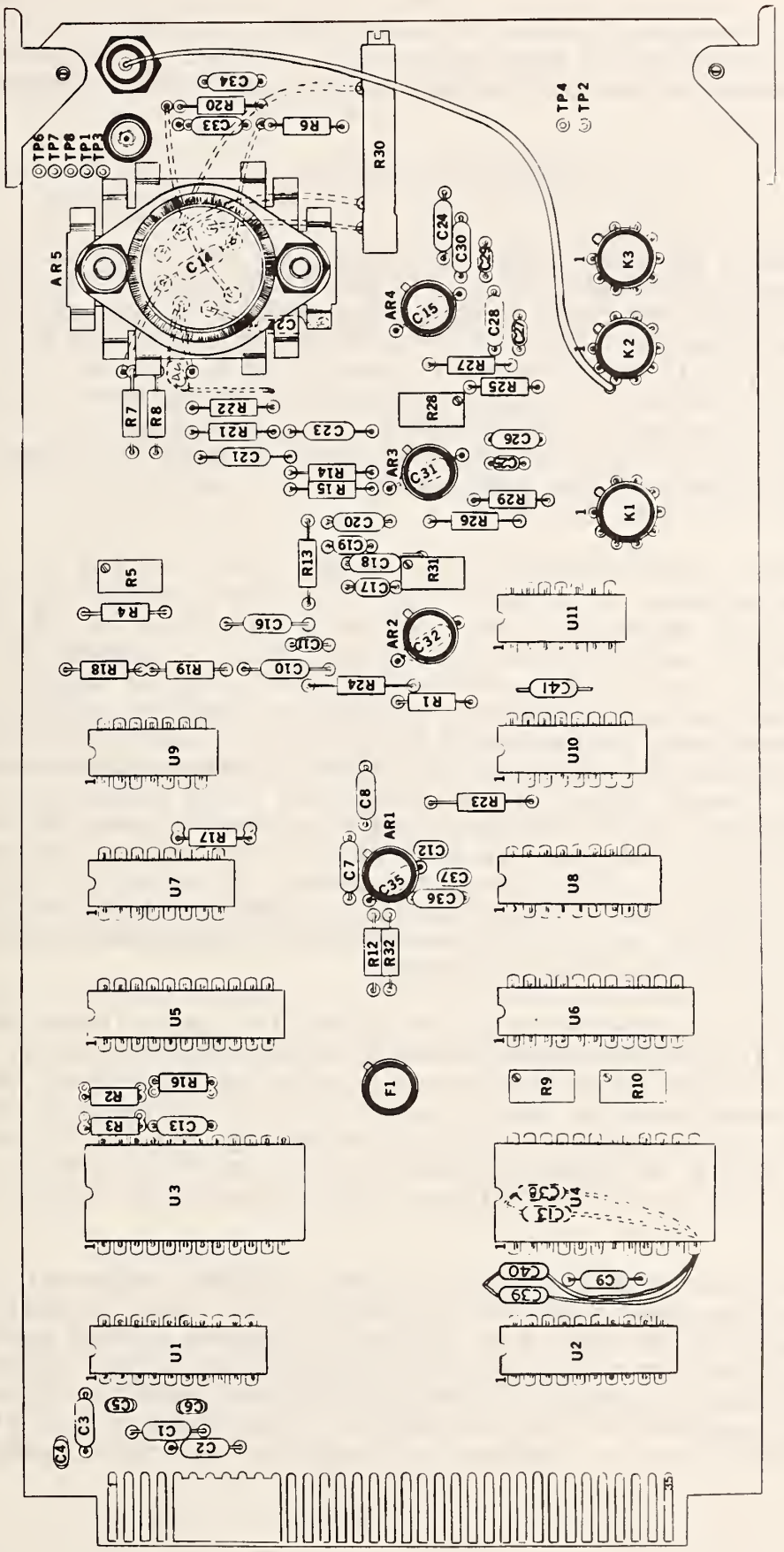


Figure 5.2(b) Output Circuit Board (Parts Layout)

310 kHz (2-pole Butterworth) for the 16-bit and the 12-bit channels respectively. Both converters produce an analog output waveform at all times, irrespective of the selected frequency range, though only the appropriate converter is connected through a relay (K1) to the rest of the circuitry.

5.2.2 Amplitude Control

The programmable amplitude control and associated amplifiers are common to the signal paths from both the 16-bit and 12-bit converters. From the active filter the signal is routed through relay (K1) to a 12-bit multiplying digital-to-analog converter (U8) which is configured as a resistive attenuator with 2^{12} steps, providing output voltages from 0 to 7.069 volts in approximately 2 millivolt increments. Depending on the position of a second relay (K2) in the signal path, the attenuated voltages can be fed either to the output connector of the Phase Angle Standard, or switched (through relay K3) to the high voltage amplifier (AR5) which has a fixed gain of 14.14 and provides outputs from 7.1 to 100 volts.

The amplitude control information, range selection, and dc offset adjustment are encoded on a 16-bit bus in a binary format as shown in table 5.2 which gives examples of the composite code formats. If the bus information contains amplitude control settings, this is indicated by bit 15 being "low." Bits 3 to 14 then contain the 12-bit digital input to the multiplying digital-to-analog converter. At the same time, the amplitude range selection is controlled by setting bit 0 "high" for the low-voltage range or "low" for the high-voltage range. For the Seven-Volt-Mode, both bit 0 and bit 1 are set "high," thereby selecting the appropriate relay connections which bypass the amplitude control multiplying digital-to-analog converter, and the information in bits 3 to 14 then has no effect on the output voltage. The selection of the 16-bit or 12-bit conversion channel is encoded in bit 2 which is set "low" for the 16-bit converter. If the bus contains dc offset information, bit 15 is set "high," and bits 7 to 14 then contain the 8-bit control setting for the dc-offset adjustment.

The 16-bit bus is connected to latches U5-U6, for the amplitude and range information, and also to the digital-to-analog converter used for dc-offset control, U7, which has its own internal latch. As mentioned, the most significant bit, edge connector pin 13, selects the two functions by enabling either the latches or the 8-bit digital-to-analog converter. The range information is further decoded by U10 which also generates the pulses to operate the relays using the software controlled pulse signal at edge connector pin 31.

The digital-to-analog converter for the dc-offset compensation has an actual output voltage range from 0 to +10 volts. This range is modified to provide an effective range from -5 to +5 volts by applying a fixed negative 5-volt bias through resistor network R18-R19. The converter voltage output, and the the bias voltage, are connected through high-value resistors (R3 and R17) to the summing junctions of the two active filter input stages with the resistors chosen to provide appropriate ranges of dc-offset compensation currents.

Control Bits																Output Voltage
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	0	0	0	0	1	0	0	1	0	0	0	0	1	c	0	1	0.499
	.....																.....
	0	1	0	1	1	0	1	0	1	0	0	0	0	c	0	1	5.000
	.....																.....
	0	1	1	1	1	1	1	1	1	1	1	1	1	c	0	1	7.069
	0	x	x	x	x	x	x	x	x	x	x	x	x	c	1	1	7-V-Mode
	0	0	0	0	1	0	0	1	1	0	0	1	1	c	0	0	7.50
	.....																....
	0	1	0	1	1	0	0	1	1	0	0	1	1	c	0	0	70.00
	.....																.....
	0	1	1	1	1	1	1	1	1	1	1	1	1	c	0	0	99.98
	1	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	-5*(00)**
	.....																.. ..
	1	1	1	1	1	1	1	1	1	x	x	x	x	x	x	x	+5 (FF)

*DC offset compensation, effective voltage source range from -5 V to +5 V
**Corresponding hexadecimal digits displayed on readout in Test Mode.

c= 0 for 16-bit conversion channel; c= 1 for 12-bit conversion channel
x= don't care

bit 0 and bit 1 are range control bits;
bit 15 is the dc offset/amplitude select.

Table 5.2 Amplitude/Range/DC Offset Control (Binary) Format

5.3 Memory Circuit Board.

As explained in chapter 4, for outputs with frequencies above 5 kHz, the digital data for an entire waveform must be stored so that data can be converted at megahertz rates. Two banks of memory with 1024 16-bit words each are provided for the waveform data storage and are shown as U19-U22 and U23-U26 on the circuit diagram, figure 5.3. The first memory bank is dedicated to the "reference output" channel and the other to the "variable output" channel. A modulo 1024 counter (U1-U3) furnishes the memory address for both banks and always points to the current location.

The pair of 16-bit data words computed by the waveform generating processor,one for each output channel, are transmitted successively along the 16 most significant bits of the 20-bit data bus to pairs of octal bus transceivers (U6-U7,U8-U9). A bus instruction (see chapter 5 of [1] for details), generated by the processor and latched into U13, directs the data word to the designated data bank and inserts it at the location given by the address counter. The instruction initiates a (ground true) write pulse, 'FE' or 'VE' for the reference or variable channel respectively, which enables the corresponding transceivers and writes the data into the appropriate memory.

The strobe pulse (timing pulse), originating in the frequency synthesizer (Circuit Board D3), arrives at edge connector pin 65 ("TP" on the circuit diagram), passes through clock control chip U18, and latches the contents of the memory locations specified by the address counter into the octal latches U4-U5 and U10-U11. The strobe pulse is also used to advance the counter to the next memory address. A third function of the strobe pulse is to acknowledge to the processor that the data have been read out of memory. This acknowledgement takes the form of a 1-bit signal that modifies the program flow of the waveform generating hardware so that the calculation of the next pair of data points can be initiated. The bit is "OR'ed" into the next address register of the sequencer section of the 20-bit processor (circuit board D9) which causes the processor to exit from its wait-loop. Details of this action are described in chapter 5 of [1].

For output frequencies up to 5 kHz, the action described above is repeated for every sampled data point. Above 5 kHz, a similar procedure is followed until all 1024 memory locations have been filled with the waveform data. The frequency synthesizer is then switched to its next higher range (range 7) which increases the strobe rate by a factor of ten. At the same time edge connector pin 67 is driven high so that the octal latch, U13, is cleared and the inputs to the AND gate, U16, are driven low. Consequently, the input at one of the D-type flip-flops, U14, is at a low level which prevents the propagation of the acknowledge ("OR") signal to the output edge-connector pin 68. As mentioned above, without this signal, the the waveform generating program remains idling, trapped in an endless loop. No new data are therefore computed and stored in memory until a software command resets the waveform generating processor.

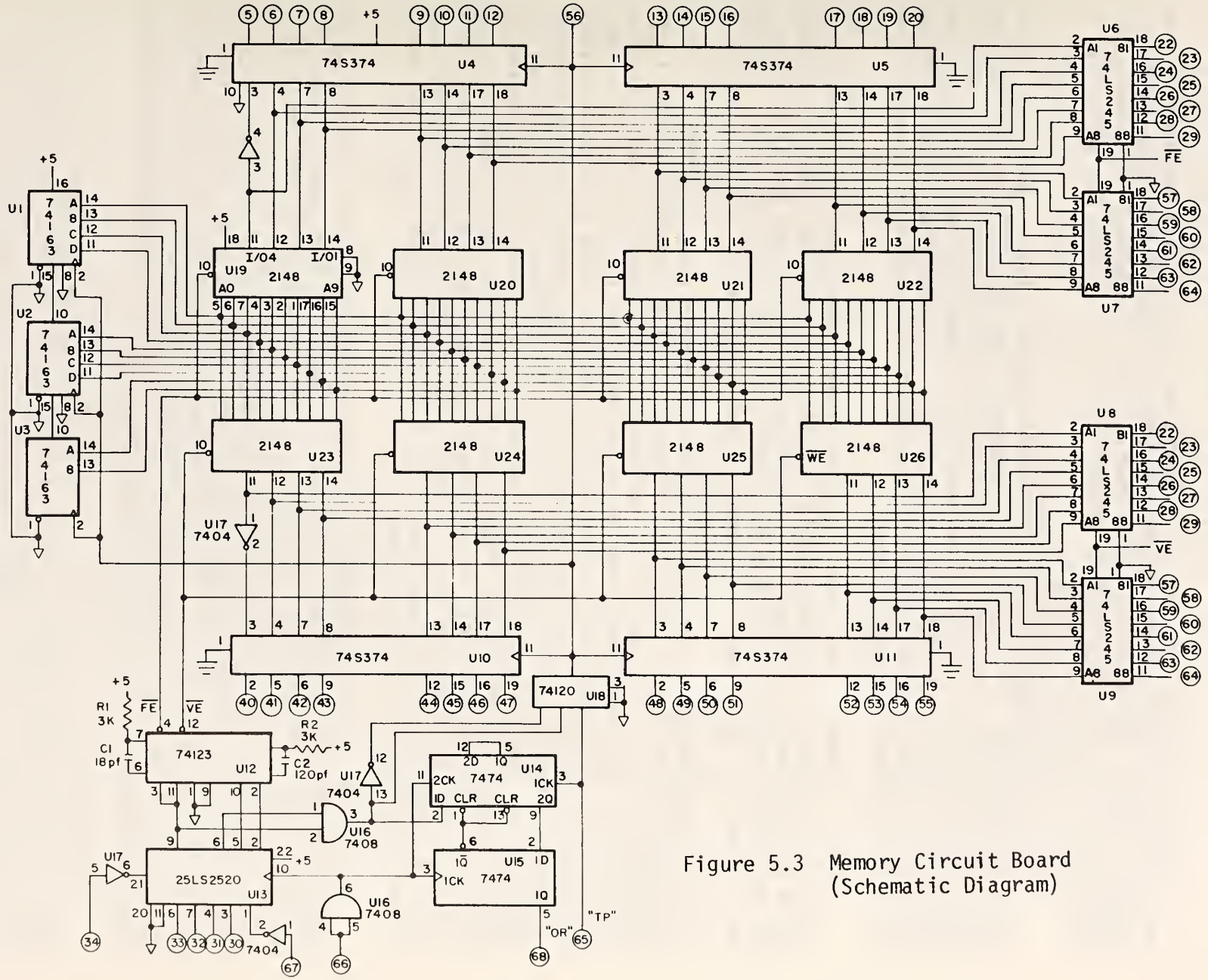


Figure 5.3 Memory Circuit Board (Schematic Diagram)

5.4 Phase Detector Circuit Board

The circuitry on the the phase detector circuit board (figure 5.4) has two functions: to measure the quadrature error of the Phase Angle Standard output, and to determine the dc offsets in the "Reference" and "Variable" signals applied to the phase detector. These functions are more fully described in section 4.5 above.

The two output waveforms enter the phase detector circuit board at input jacks (J1 and J2). The signal path connects the input jacks through the channel interchange (reversing) relay, K16, and the range relay, K17, to the input amplifiers U1 and U2. These amplifiers have either unity gain (low range), or a gain of 1/14.14 (high range). The range switching is necessary to accommodate signals up to 100 volts rms while not exceeding the 10 volts peak limit of the operational amplifiers.

Since the amplifiers have a high but finite impedance, they represent a load on the output of the Phase Angle Standard and may influence the phase angle to some extent, especially at the upper frequencies. For this reason, the amplifiers are left connected even when not in the auto-zero mode, so that the loading will not change when changing from auto-zero to normal operation.

While the inputs of amplifiers U1 and U2 remain connected when not in the auto-zero mode, the amplifier outputs are disconnected from the their attenuators to prevent possible overload or saturation of the inductive dividers. In the normal mode, the output of amplifier U2 is connected to edge connector pin 59 through both contacts of relay K19. With this connection, either of the output signals can be fed from the Phase Angle Standard (through the channel interchange relay K16) to the integrating analog-to-digital converter on circuit board A13 (via the backplane). In this configuration, a "dynamic" dc-offset measurement determines the sum of the dc offsets through the amplifier chain as well as dc components introduced by the switching action of the waveform generating digital-to-analog converter. The numerical value of the dc offset is thus transmitted in digital 12-bit, two's complement format to the control microprocessor.

The outputs of the attenuators are buffered by amplifiers U3 and U4 which also provide the necessary gain to bring the signals to the 5-volt level for the quadrature phase detector (U5A-U5D). The half-wave version of the circuit described in [1] (pp 121-126) is used in the present phase detector circuit board. The second set of diodes in the feedback circuits of U5B and U5C serve only to keep the feedback currents symmetrical. The discussion in [1] (bottom of page 123) indicates that the half-wave circuit does not compensate as completely for the amplifier or signal offsets as does the full-wave version. Nevertheless, the uncompensated offset signal components are cancelled by the algorithm which computes the phase detector output.

As pointed out in [1], for satisfactory operation, one of the input signals to the phase detector circuit must always be slightly larger than the other. Because the 7-bit attenuators in the present version provide a sufficient number of signal levels, the unequal signal requirement is taken care of by the software rather than by the hardware. The attenuator settings are computed so that one signal is larger by approximately 12.5 percent.

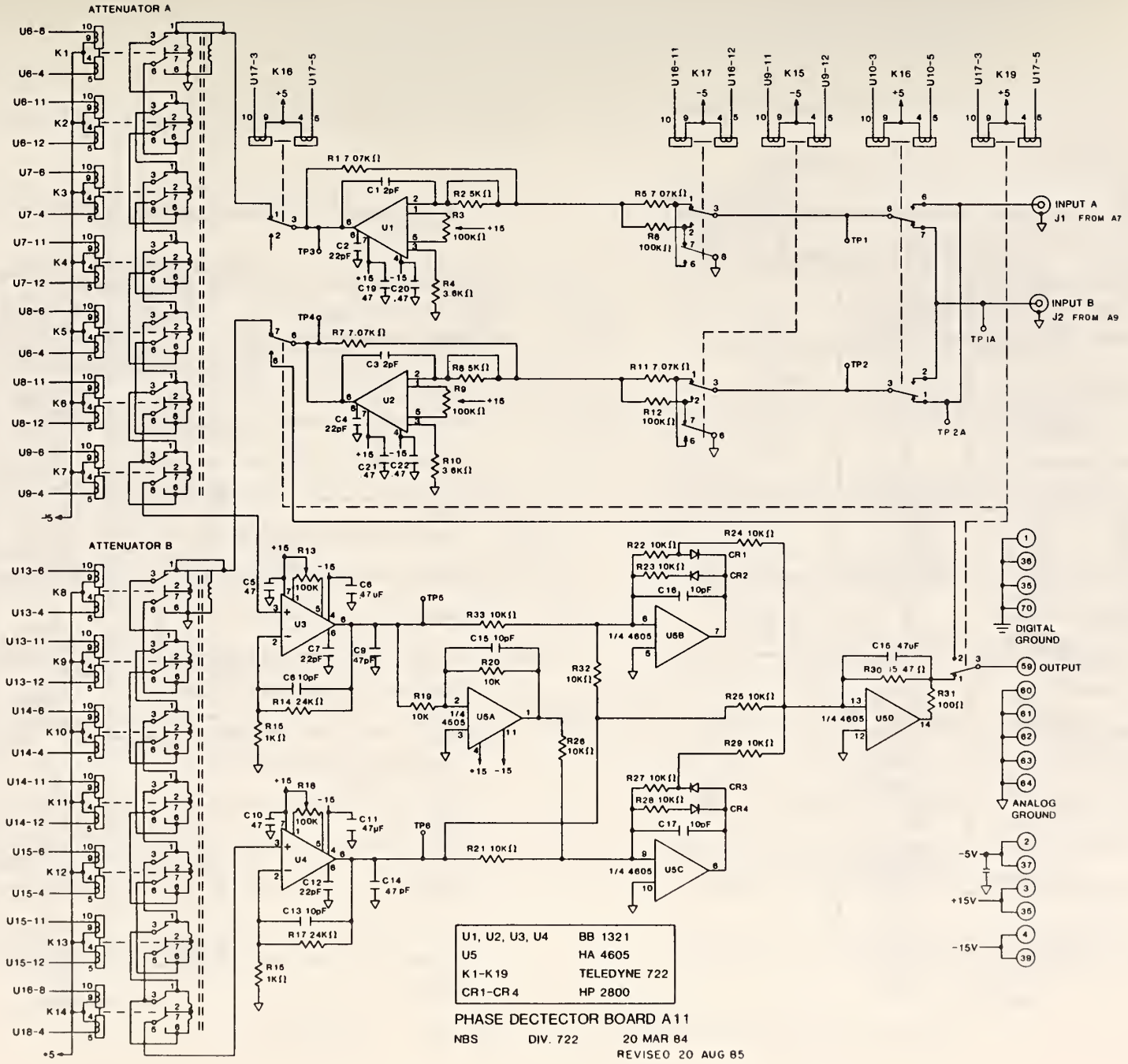


Figure 5.4(a) Phase Detector Circuit Board (Schematic Diagram)

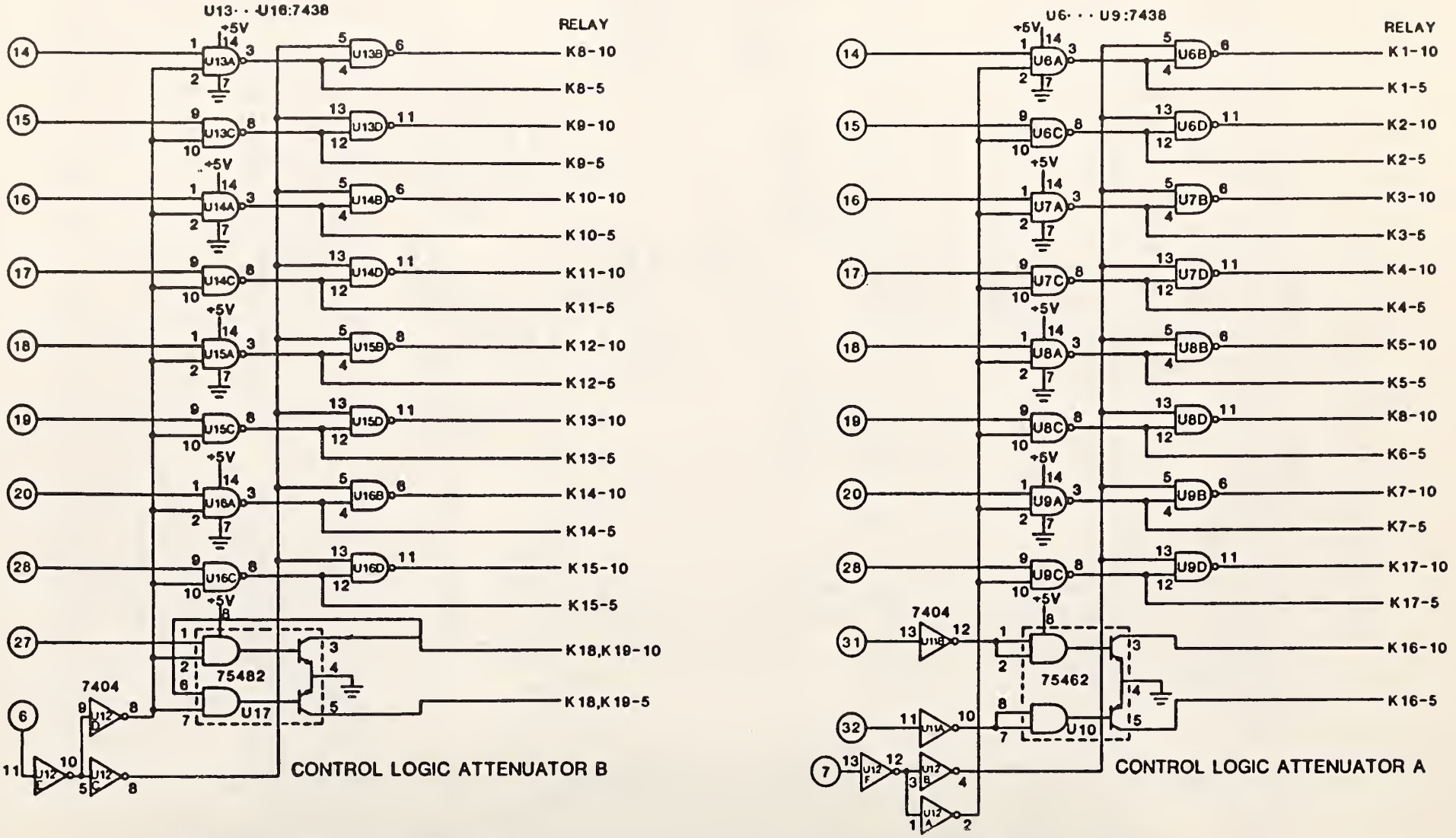


Figure 5.4(b) Phase Detector Circuit Board, Relay Driver Circuits

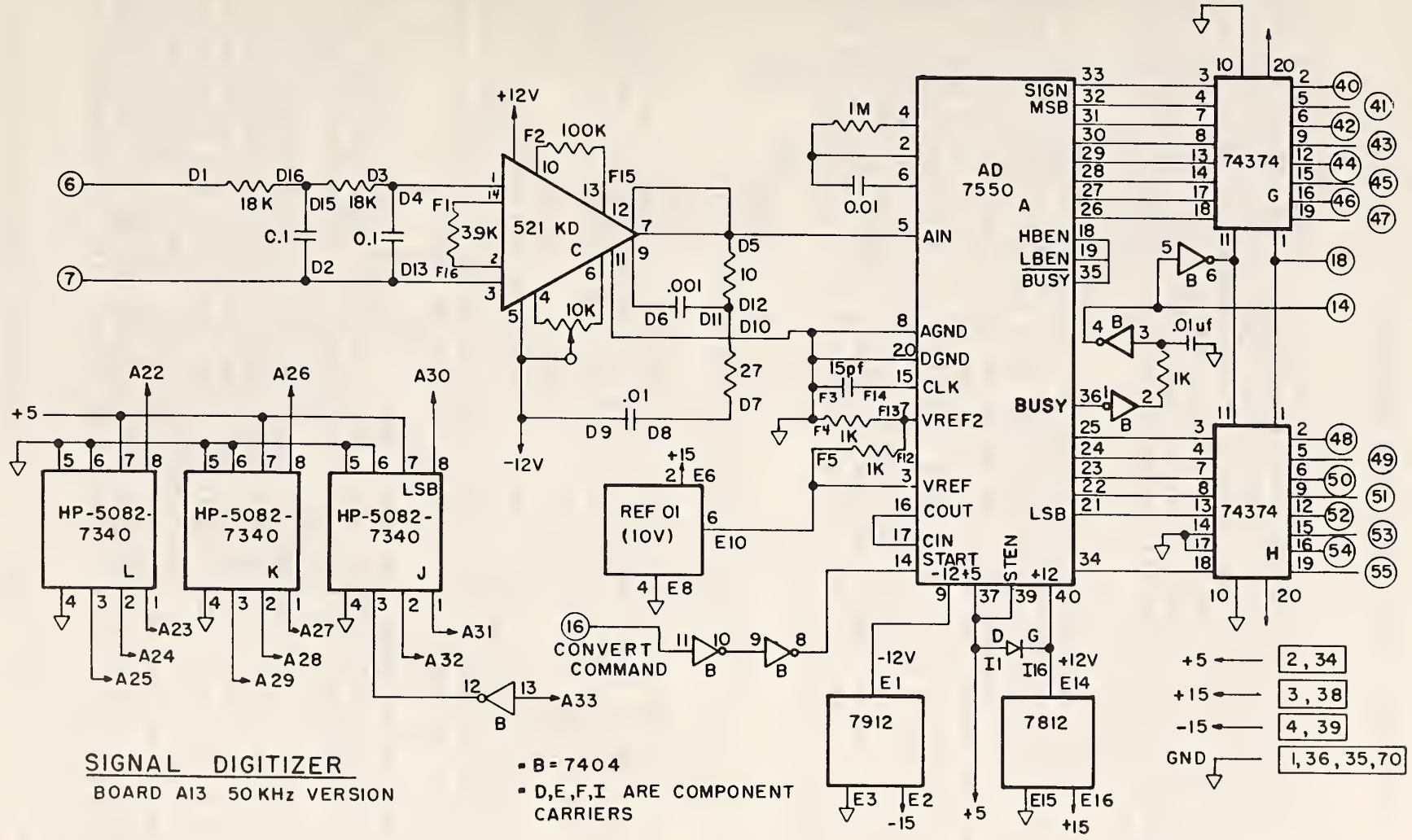


Figure 5.5 Digitizer Circuit Board (Schematic Diagram)

5.5 Digitizer (Analog-to-Digital Converter) Circuit Board.

The output signal from the phase detector circuit board (figure 5.4a) enters the differential input of the instrumentation amplifier, C, through edge-connector pins 6 and 7, and the amplified signal is then applied to the analog-to-digital converter, A. The gain of the instrumentation amplifier is approximately 25, scaled so that an input equivalent to roughly 1.5 degree phase error will give a full scale reading on the 12-bit analog-to-digital converter. The maximum incremental correction in each auto-zero iteration is therefore about 1.5 degrees.

The twelve most significant bits from the converter are transfered to octal latches, G and H, on the trailing edge of the "busy" signal supplied by the converter. To allow for set-up times, the busy signal is delayed with a time constant of 10 microseconds. The output of the latches are bussed to the system Interface Circuit Board (D10) over the 16-bit low-speed bus (edge connector pins 40 to 55). The delayed busy signal is also connected to edge connector pin 14 and is used to indicate that the conversion is complete and that the data can be read by the control microprocessor (8085) via the Interface Circuit Board. (Note that edge connector pin 14 is required to be at a "low" level in order for the system to function normally except for the analog-to-digital conversion.)

5.6 Microprocessor Circuit Board

The basic arrangements and functions of the 8085 microprocessor circuit board are the same as those described in [1]. The microprocessor communicates with the rest of the system through the Interface Circuit Board (D10), through a 34 line cable at the front of the board.

To provide for address space for additional read-only memory and the IEEE-488 bus, the address decoding circuitry was rearranged to decode 15 bits of address and, as before, using the most significant bit for memory mapped input/output. The revised circuit diagram is shown in figure 5.6.

To accommodate the additional code needed for 50 kHz operation as well as communication though the IEEE-488 bus, a fifth read-only memory has been added with room for expansion for further read-only memories, if required.

Connections to the IEEE-488 bus interface are routed from the data bus through transceiver, U4, and backplane connector pins 3-10. If address bits 11 through 13 are high and bits 14 and 15 are low, the signal at backplane edge connector pin 40 will be low and the IEEE-488 bus interface and transceiver, U4, will be enabled. Address bit 3 (backplane edge connector pin 14) selects either the bus address switch or the interface chip itself. Read and write commands are routed via backplane edge connector pins 15 and 16. The registers of the IEEE-488 bus interface are selected by address bits 0-2 (backplane edge connector pins 11-13).

The remainder of the circuit functions and connections have been described in

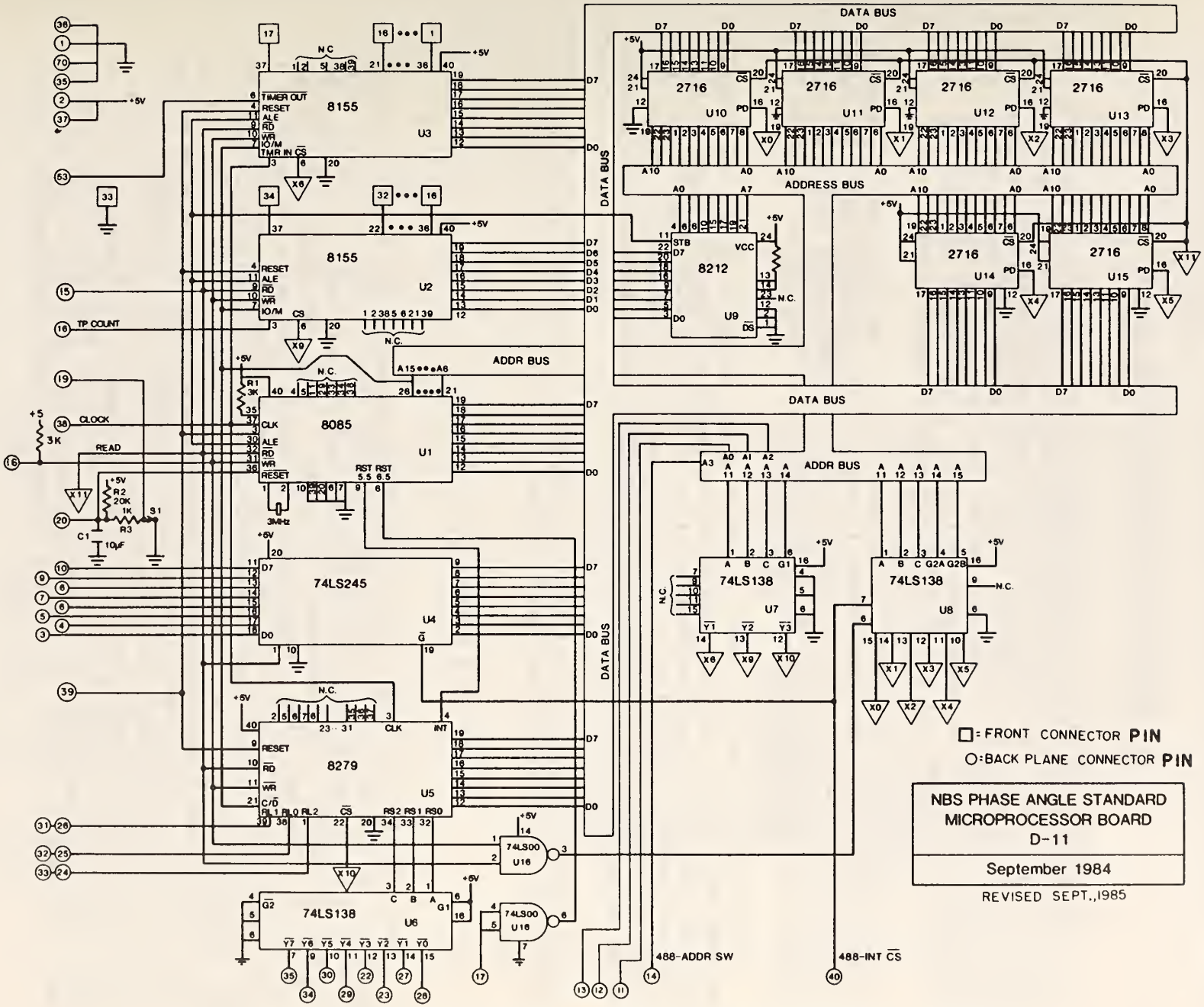


Figure 5.6 Control Microprocessor Circuit Board (Schematic Diagram)

detail in [1]. The microprocessor controls the keyboard via the decoders U5 and U6 and is connected through I/O ports U2 and U3 to the System Interface board. The System Interface distributes the data to various busses and decodes several of the control functions. Its operation is described in [1].

5.7 IEEE-488 Bus Interface Circuit Board

The IEEE-488 interface circuit (figure 5.7) is based on the (Intel 8291A) GPIB Talker/Listener integrated circuit, U1. The IEEE-488 bus connection is made through octal transceivers, U3-U4, and the interface circuit communicates via the 8-bit data bus with the (8085) control microprocessor through the backplane, connector pin numbers 12 to 19. The internal registers of the GPIB integrated circuit are addressed using the least three significant bits (backplane connector pins 11 to 13) of the microprocessor address bus.

The GPIB Talker/Listener integrated circuit is programmed to send a negative going (low) interrupt signal to the control microprocessor through connector pin 17. This mode is chosen so that the Phase Angle Standard system can be operated without the IEEE-488 bus interface card in place, since in TTL circuitry an open connection is at a high level.

Four bits of the IEEE-488 bus address are selected using the rotary hexadecimal switch, and the outputs of the switch are fed to a gated buffer, U2. The input to the register of the buffer is hard-wired to complete the 8-bit bus address, and the tri-state buffer output is enabled by bit A3 (backplane connector pin number 14) of the microprocessor address bus through the decoding gates, U5.

All eight bits of the data bus are connected to a terminating resistor network, U6, to eliminate spurious responses.

5.8 Frequency Synthesizer

The operation of the frequency synthesizer which generates the timing pulses to define the sampling interval is described in detail in [1]. The circuit is substantially unchanged from the version referred to in [1] except for a minor modification which enables automatic range switching (from range six to range seven). The range change increases the output frequency by a factor of ten. Referring to figure 5.8, the synthesizer frequency is controlled by four binary-coded-decimal inputs on edge connector pins 5 to 20. The system requires only a limited frequency span in each decade, from 200 to 400 kHz and from 2 to 4 MHz, so that the most significant bit (pin 5) of the most significant binary-coded-decimal digit is always zero. Therefore, this bit can be used to effect the range change. As shown on the circuit diagram, the bit line from the input latch A (pin 2) is connected to the range control input (pin D) of the synthesizer module. When the most significant bit is "low," the range multiplier is set for output frequencies in the 100 kHz range, and when the bit is "high," the frequencies are in the megahertz range.

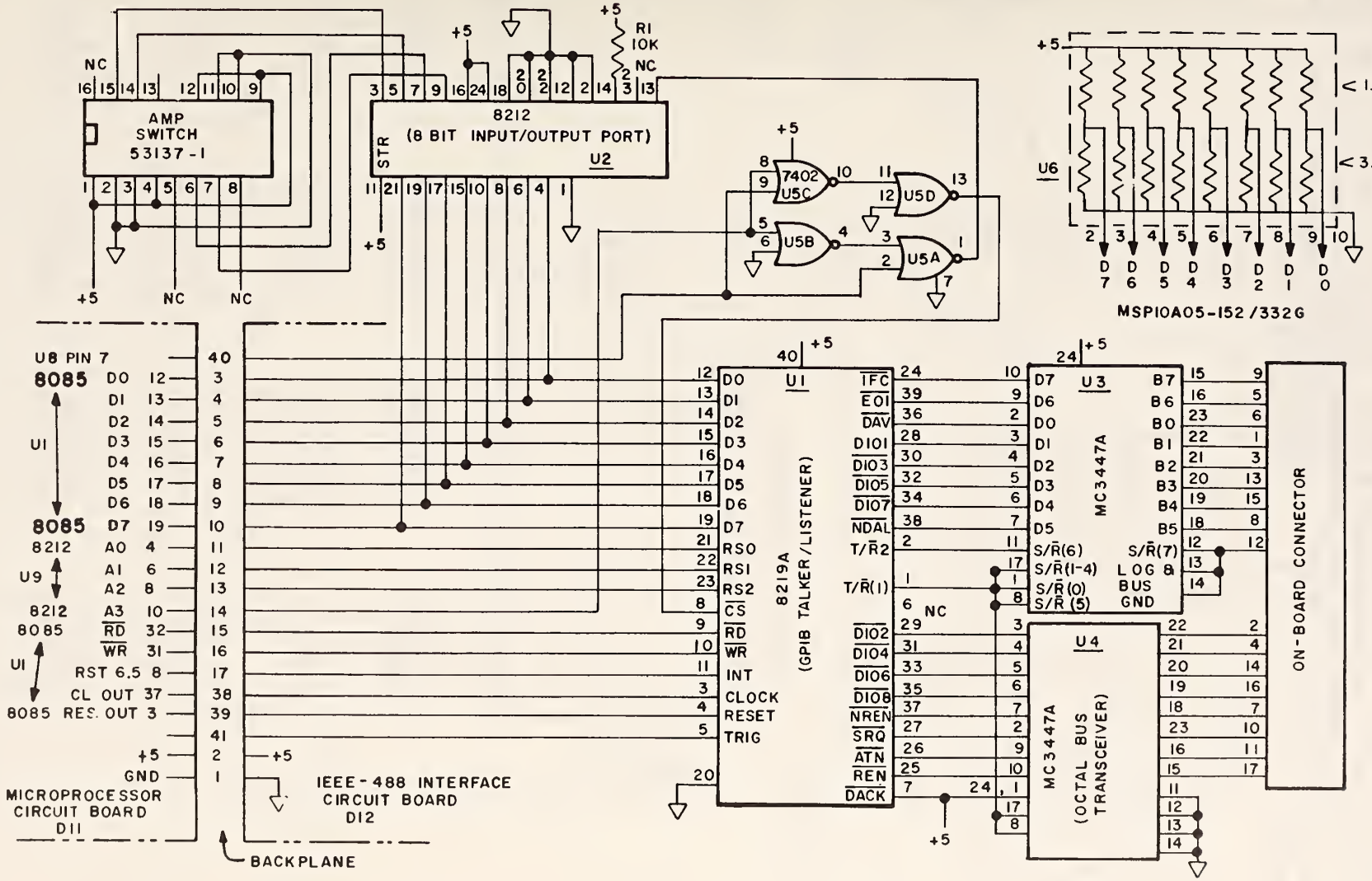


Figure 5.7 IEEE-488 Bus Interface (Schematic Diagram)

As in the original design, an external pulse signal input at edge connector pin 23 will override the synthesizer output if it is in a frequency range so that it will retrigger one-shot G and consequently keep pin 1 of gate H "high." A test point for the synthesizer output is available at edge connector pin 25 (and at a special connector near the front edge of the circuit board).

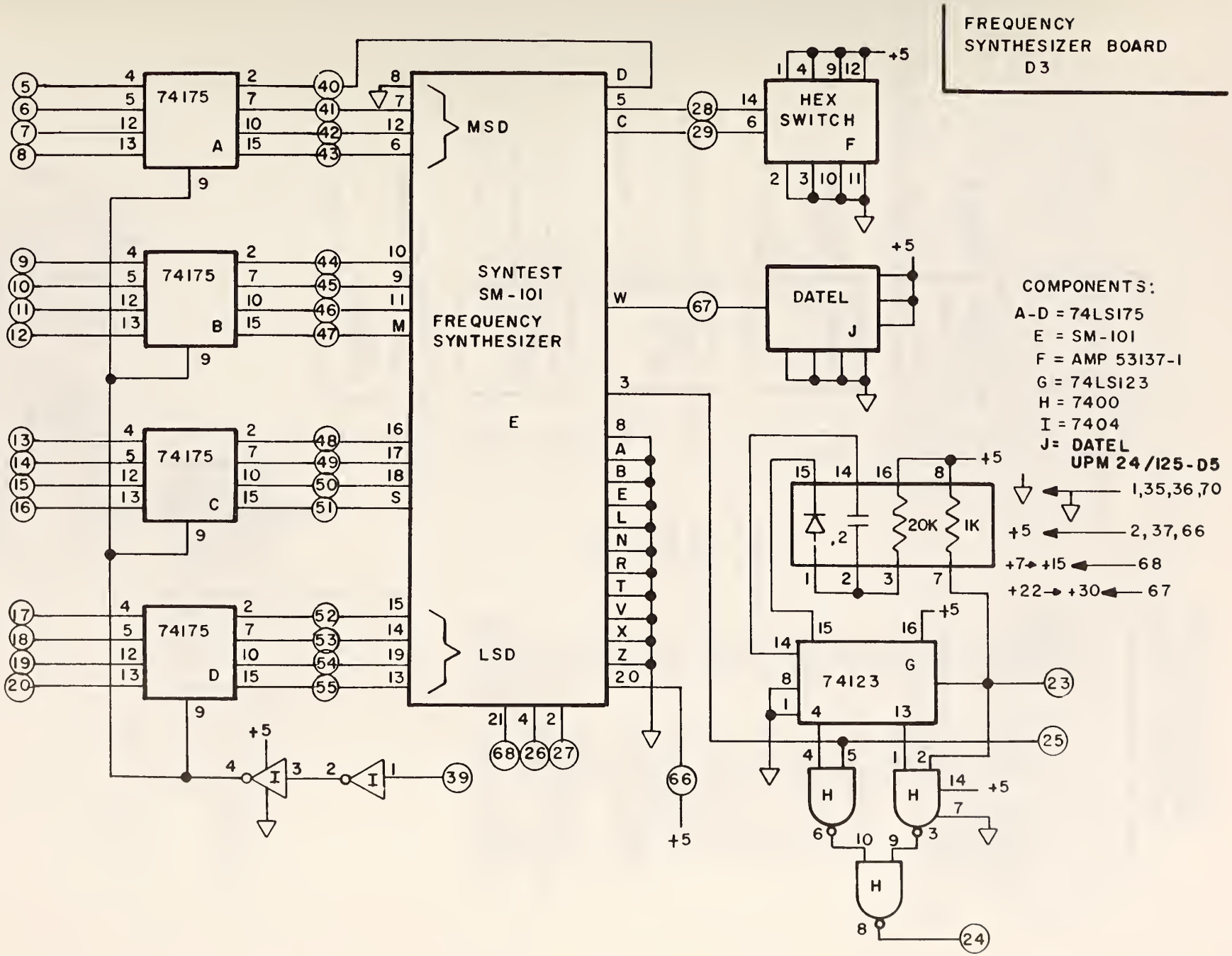


Figure 5.8 Synthesizer, Timing Pulse Generator (Schematic Diagram)

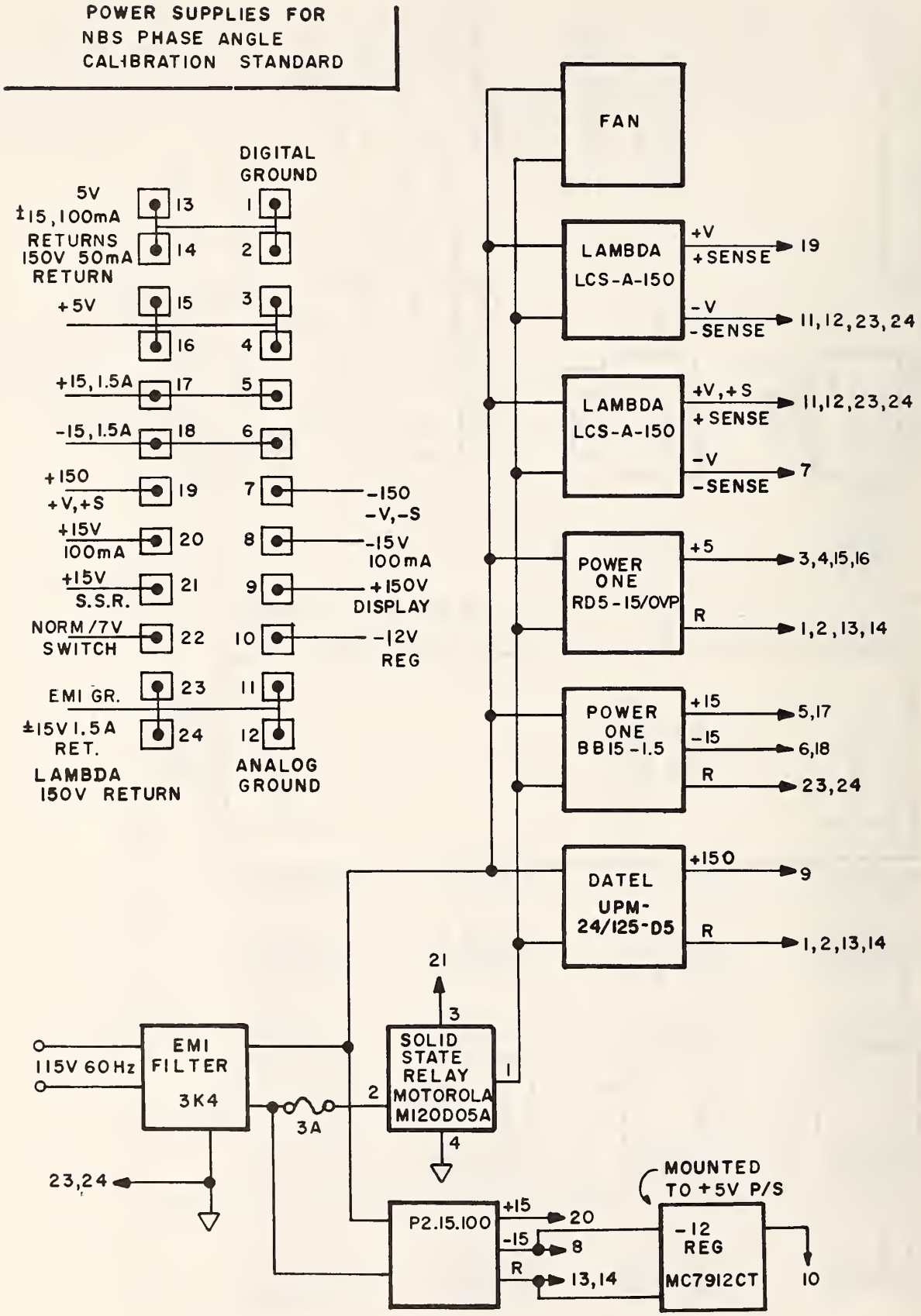


Figure 5.9 Power Supplies (Schematic Diagram)

5.9 Power Supplies.

The power supply modules are assembled from commercially available units. The arrangement is shown in figure 5.9. The digital and analog ground returns are kept separate to prevent voltage drops due to ground currents in the digital circuitry from influencing the analog voltages. However, the analog and digital grounds are joined, unavoidably, at several places on the Output and Digitizer circuit boards, as described in sections 5.2 and 5.5.

Except for one 15-volt supply that is always energized, the ac-power to the other supplies is switched through a solid state relay which is controlled by a front-panel switch (see also section 3.2-a).

6. SOFTWARE FOR THE 8085 PROCESSOR.

6.1 Overview

The 8085 system control microprocessor carries out four separate functions. The first and most important function is the interpretation of keyboard commands and parameters and the conversion of the entered data into an internal code which in turn is used to implement the commands in the hardware. Much of this scheme has been discussed in greater detail in [1], and many of the routines shown on flow charts in the referenced NBS Technical Note 1144 follow the same logic outline, although the details have been changed.

The second function of the software, linked intimately with the first, is the management of display information: operating parameters, operator prompts, error messages, and identification of the version of the code in the read-only memories. Added to this list is the message handling procedure over the IEEE-488 bus to transmit operating data to the device controller and to display bus status information on the readout.

The third function of the software for the control microprocessor is connected with the auto-zero feedback procedure. Data from the phase detector and associated hardware are averaged, scaled, and saved in "software" correction registers before finally being applied to the waveform generating hardware.

A fourth function of the software provides help for diagnostic tests on the Phase Angle Standard system. The so-called "Test Mode" is not used in normal operation (and access can be restricted by means of a special code). Some of the subroutines, however, are shared with those used for normal operation.

6.2 Process Control Software

Data entered from the keyboard go through several steps of decoding. First, an interrupt routine detects when a key has been depressed and the keyboard control hardware scans the input lines to determine the grid position of the activated key. The position information is transformed into an address of a look-up table containing the assigned ASCII equivalent for the key (table 6.2). The ASCII byte is then stored in a software first-in-first-out register (FIFO), implemented as a section of random-access-memory that is configured as a circular list and can hold up to 64 command or parameter bytes. The list is accessed using "in" and "out" pointers. Insertion of the information into the list completes the action of the keyboard interrupt routine, and the program execution of the original task is then resumed.

PHASE	OFFSET	FREQ	"7"	"8"	"9"	Key Label
E1	E2	E0	C1	C2	C0	Key Cross-point Address
A	B	C	7	8	9	ASCII Equivalent
AMPL	"E"	AUTOZ	"4"	"5"	"6"	Key Label
E9	EA	EB	C9	CA	CB	Key Cross-point Address
D	E	F	4	5	6	ASCII Equivalent
STOP	RUN	SINGLE	"1"	"2"	"3"	Key Label
F1	F2	F0	D1	D2	D0	Key Cross-point Address
S	R	I	1	2	3	ASCII Equivalent
RESET	" "	TM	"-"	"0"	"."	Key Label
	FA	FB	D9	DA	DB	Key Cross-point Address
	K	L	-	0	.	ASCII Equivalent

Table 6.2 Keyboard Conversion Data

The table shows key labels, associated key addresses resulting from the wiring scheme of the cross-point switches, and the software generated ASCII equivalent.

In normal operation, the system is in a wait ("input") state continually scanning the first-in-first-out register for the next instruction or data byte. If a byte is found, that is the "in" and "out" pointers no longer indicate that the register is empty, the byte is "removed" by transferring the information to a microprocessor register and by repositioning the "out" pointer. The command or parameter byte is then compared with "numeric" and "command" look-up tables which are keyed to subroutine addresses, and the program branches so that numeric data are further processed by a number handling routine and the individual command bytes by the corresponding special function routines.

The special function routines set up a status byte to identify the command function, fetch and display the information for the readout, and then return for more "input" if required. After all the necessary numerical information has been gathered, it is converted to the appropriate number format and, with the help of internally generated hardware instruction codes, is then transmitted over the 20-bit or the 16-bit data bus. Phase angle, offset angle, or frequency dependent phase steps (increments) needed to calculate the waveform data are transmitted to the waveform generating microprocessor over the 20-bit data bus, while amplitude, dc offset, and frequency information for the synthesizer are sent over the 16-bit data bus.

Numerical conversions are mostly handled in two steps. The ASCII keyboard information is transformed to binary-coded-decimal numbers which are then converted to scaled binary numbers by an algorithm using a series of special look-up tables. The table look-up method is convenient, because various decimal to binary conversion ratios depend on the system function. So, for instance, positive full-scale in two's complement binary (0111111...) corresponds to 359.999 in angle, or 7.071 in amplitude, and so on. Using the

look-up algorithm, the same routine can handle all conversions simply by changing tables. The same tables are also used for the inverse transformation from binary to binary-coded-decimal numbers. Because the decimal-angle-to-binary-angle conversion requires 40 bits to conserve resolution and accuracy, nearly all numerical conversions are carried out in a 5-byte (40-bit) format, even though the final result is truncated or rounded to 16 or 20 bits.

Other numerical routines provide multi-byte add, subtract, and compare functions, as well as a 16 by 16 bit multiply and divide operation with a 32-bit product or dividend. When 16-bit accuracy is sufficient, a similar but faster set of routines (using only the microprocessor registers) is provided to save computation time.

In carrying out the various functions of the Phase Angle Standard, the software keeps track of its current state so that sub-tasks are scheduled in the correct sequence and, among other things, prevent application of damaging voltages or transients to circuit components. This safety feature is particularly important when changing relay positions while output voltages are high. When generating output signals above 5 kHz, a fairly complicated sequence of events must be maintained to achieve the desired results. The routine for the frequency function is illustrated in the flow chart (figure 6.1).

6.3 Display Software

The two-line readout can display 16 characters in each line. The first eight character spaces of each line are reserved for alphabetical designation of the functions, such as PHASE, OFFSET, FREQ, etc. The remaining 8-character field displays the operating parameters or numerical keyboard entries. The function selected by the command key is underlined on the display. A prompt or error messages may take a full line or the whole two-line display. The functions or parameters displayed prior to an error message or prompt are restored after the error has been cleared, or after a valid response to a prompt.

The text for the messages is contained in the read-only memory, while numerical operating parameters are stored in random access memory. The format of the information in the read-only memory includes a top-line/bottom-line flag and a character count in the byte that precedes the actual ASCII text. The three bytes following the message contain the number of parameter bytes associated with the particular function as well as the address of the parameter memory locations. Top- and bottom-line pointers hold the addresses for the text sections displayed on the two lines of the readout. To display error messages or prompts, the pointer information is pushed onto the microprocessor stack and replaced by a memory reference for the special message. When the special messages are no longer needed, the pointer information is retrieved from the stack and the original display content is restored.

Frequency Calculation

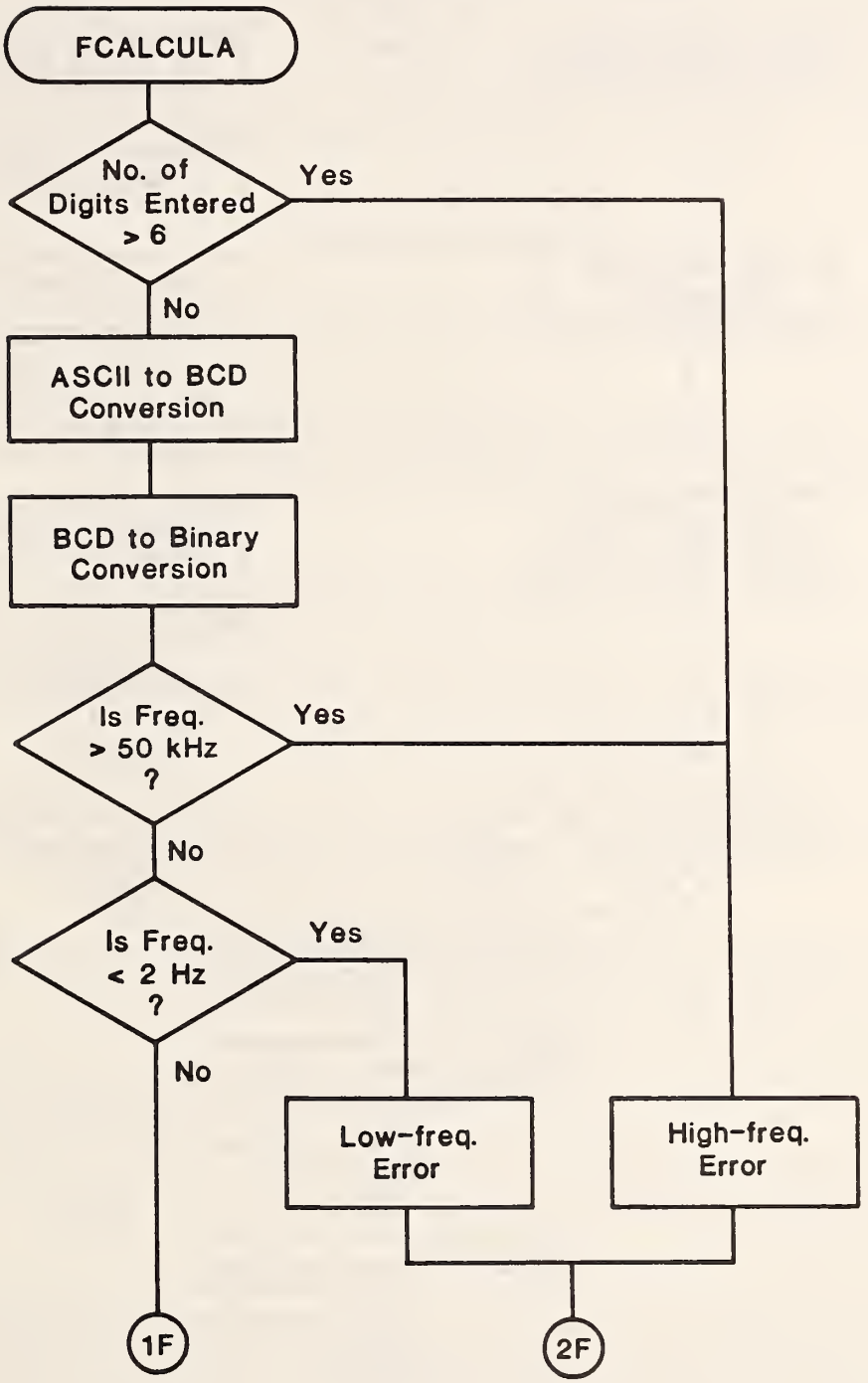


Figure 6.1(a)

Frequency Calculation (Continued)

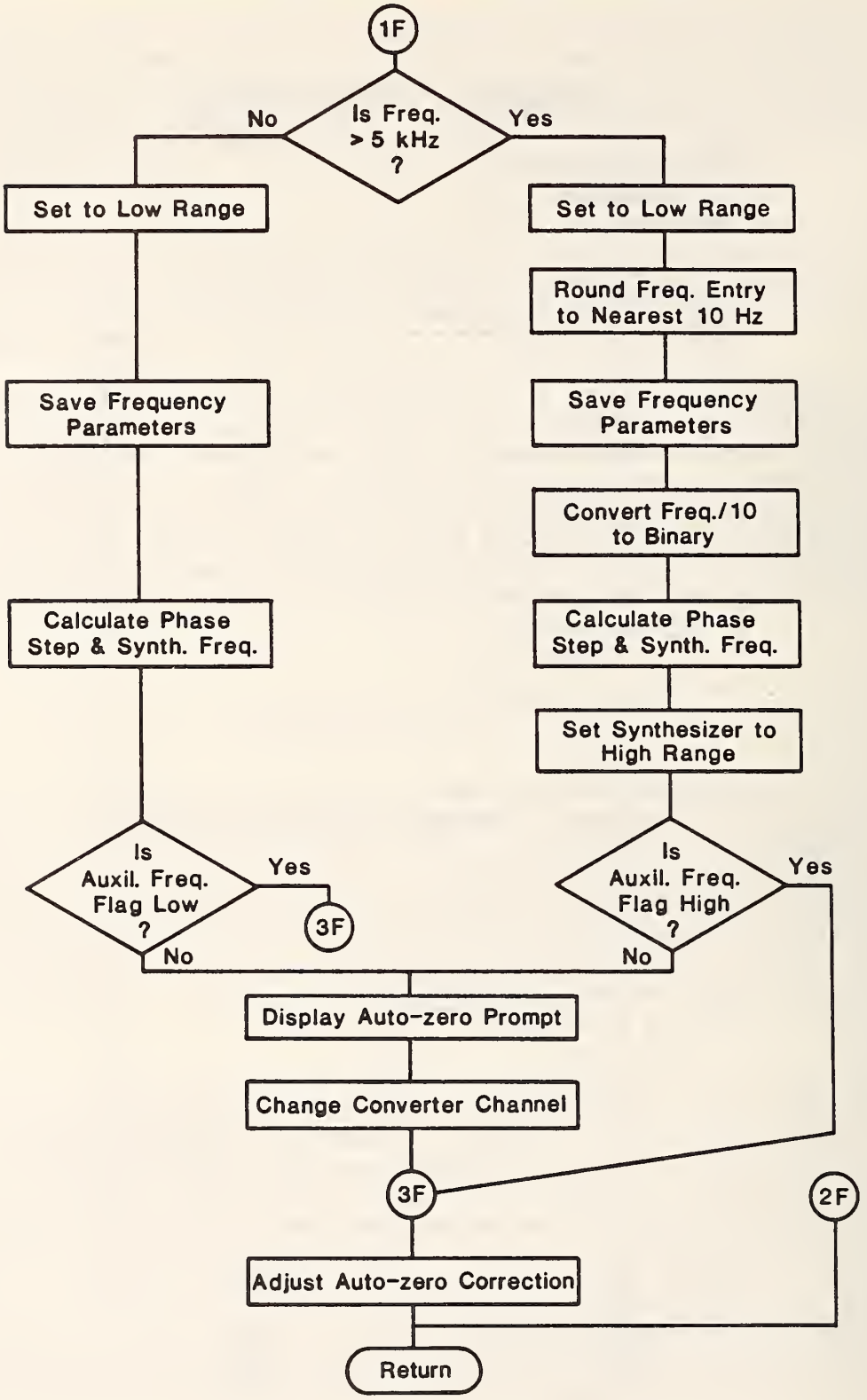


Figure 6.1(b)

During the intial power-up routine, and every time the system is reset, a cyclic redundancy check is carried out on the content of all five read-only memory circuit components. The results of the cyclic redundancy calculation are checked against values stored in the last ten bytes of the fifth read-only memory. If an error is found, a message on the readout will indicate which of the memories is faulty. Also, at the beginning of the reset routine, a message identifying the software version in the read-only memories is flashed onto the readout for a few seconds. This identification is useful when correlating the system code with the printed listing and when making changes.

6.4 Auto-Zero Software

The software for the auto-zero procedure can be broken down into several sub-tasks listed below:

(a) Determines whether the operating frequency is in the high or low range, saves the frequency value, and sets the auto-zero frequency accordingly to either 4096 Hz or 32770 Hz (32768 Hz rounded up).

(b) Measures the dc offset and adjusts offset compensation control until dc offset is nulled on both channels.

(c) Determines the value of the sensitivity calibration factor for the amplitudes of the two signals applied to the phase detector.

(d) Measures the phase error at 90 and -90 degrees with phase detector inputs in the normal and interchanged mode, and calculates phase error correction .

(e) Checks whether the incremental correction is within tolerance. If not within tolerance, applies correction to waveform generator and repeats step (d), else does step (f).

(f) Determines amplitude ratio, and if not equal, adjusts phase angle correction for ratio.

(g) Saves correction, restores original operating frequency, adjusts correction for operating frequency, and sets phase to zero.

Sub-task (a) is straight forward. Any previous auto-zero correction and scratch memory are cleared and the current frequency value is saved. The auxiliary frequency flag indicates the range of the current operating frequency, and the appropriate auto-zero frequency, tolerance, and settling delay times are selected accordingly. The calibration factors are set to nominal values.

(b) The dc voltage offsets of the reference output waveform and of the variable output waveform are each measured in an iterative procedure. The

waveforms are routed through one of the phase detector circuit board input amplifiers to the integrating amplifier and analog-to-digital converter (digitizer) where the time average of the sine wave (dc component) is digitized. To eliminate effects of noise or random fluctuations, four readings are averaged for each measurement, and, in addition, all individual readings are discarded that differ (by more than 0.2%) from the reading immediately preceding it. Using the results of these measurements, the offset compensation current is adjusted by setting the 8-bit digital-to-analog converter from which the current is derived (see also section 5.2.2). During each iteration, the incremental dc-offset correction is calculated (by dividing the average reading by four and truncating the result). The increment is then added to the 8-bit setting of the converter. To prevent hang-ups when the calculated correction is less than one (and therefore truncated to zero), the incremental correction is adjusted to +1 (or -1) in these cases. The iteration is terminated when the measured offset is within tolerance. The final value of the dc-offset correction is saved in six-member arrays (one for each output channel), providing storage for dc-offset values for each amplitude (low range, 7-volt range, high range) and for both the 16-bit and 12-bit converters. When switching amplitude or frequency ranges, the appropriate (approximate) offset corrections are then automatically applied. More exact corrections for the particular conditions are redetermined during the auto-zero procedure.

The calibration factor for the phase-offset correction is determined by measuring the difference of the phase detector response when the angle is changed by 0.351 degrees (a convenient round number in binary). The phase angle is first set to a nominal 90 degrees and shifted, if necessary, so that the excursion by 0.351 degrees falls within the quasi linear range of the quadrature phase detector and within the range of the 12-bit digitizer following it. Determinations are made in both the normal mode and with the channels interchanged. If the ratio of the two values so obtained is 0.8 or greater, the larger of the two values is used as the calibration factor. If the ratio is less than 0.8, the determination is repeated.

The determination of the phase error at quadrature consists of a sequence of four sets of readings as already outlined. Each set is an average of four individual readings taken under the same conditions and within a short time period. Using the same criterion as for the dc-offset measurement, the individual readings are rejected if successive readings do not agree closely. The two averages of the readings at -90 degrees are subtracted from the sum of those at +90 degrees. The result is then divided by the calibration factor and scaled so that the least significant bit of the correction angle coincides with the least significant bit of the 20-bit data bus. The 12-bit span provided by the analog-to-digital converter is equivalent to about plus or minus 1.5 degrees of phase angle which is, therefore, the largest correction that can be applied in a single step.

The incremental phase correction is compared to the default tolerances chosen for each of the two frequency ranges, or to a tolerance value entered from the keyboard. As pointed out before, to achieve a more gradual approach to the final value of the phase correction, the correction steps applied to the waveform generating circuits are reduced from their calculated values as the phase error comes close to the tolerance value. The following three conditions are considered. If the phase error is larger (in absolute value) than twice the given tolerance, the incremental correction is added to the sum

of previously determined correction steps and applied to the phase offset register of the waveform generator via the 20-bit bus. If the phase error is greater than the tolerance, but less than twice the tolerance, the incremental correction is divided by two before being added to the total correction which is then applied to the hardware. In both of these cases, further iterations of phase error measurements are carried out. Finally, if the phase error is less than the tolerance value, the calculated incremental correction is ignored, and the previously accumulated correction becomes the final value.

Experimentally, it was found that the phase detector quadrature measurement was biased if the signal amplitudes were unequal, and that the additional correction needed varied very nearly linearly with the logarithm of the amplitude ratio. For a ratio of 10:1 (Variable amplitude/Reference amplitude), the additional correction necessary is 0.020 degrees of phase angle. A look-up table is provided linking the corrections from 0 to 20 millidegrees, in steps of 1 millidegree, with the amplitude ratios calculated using the logarithmic relation. The ratio values are expressed as integers by multiplying them by 4096. When the amplitude ratio is less than one, the corrections from the table corresponding to the reciprocal of the ratio are subtracted.

As a last step in the auto-zero procedure, the original output frequency is restored, the phase angle is set to zero, and the phase and frequency values are displayed. The phase correction is then adjusted for the actual output frequency. Also, the status flag is set to zero (idle condition) from its "auto-zero" condition. Clearing the status flag has two consequences. The phase detector attenuators are disconnected when the amplitudes are restored after the channel interchange relay is returned to its normal position, and also, a "busy" status byte will no longer be sent in response to a serial poll on the IEEE-488 bus. The busy signal is intended to prevent an interruption by the bus controller that might interfere with the auto-zero procedure while it is in operation.

6.5 IEEE-488 Bus Interface Driver Software.

The software, shown in flow-chart form in figures 6.2 to 6.8, is based on the Intel 8291A GPIB Talker/Listener integrated circuit. For detailed operating conditions for the 8291A see [5]. Also, see section 5.7 describing the interface hardware.

In normal operation, if an interrupt is generated in the bus interface circuit due to a change of state on the IEEE-488 bus, the system control microprocessor (8085) responds by passing program control to an interrupt handling subroutine. This routine, first of all, checks the status of the Phase Angle Standard system. If the Phase Angle Standard system is able to respond, the internal interrupt registers of the 8291A interface circuit are examined to determine the source of the interrupt. However, if an auto-zero determination is in progress, or if the command first-in-first-out register is already full, a "busy" status byte is sent to the controller over the IEEE-488 bus. The program steps are indicated on the flow chart for the IEEE-488 Bus Interrupt Routine (figure 6.3).

8291A Initializing Subroutine

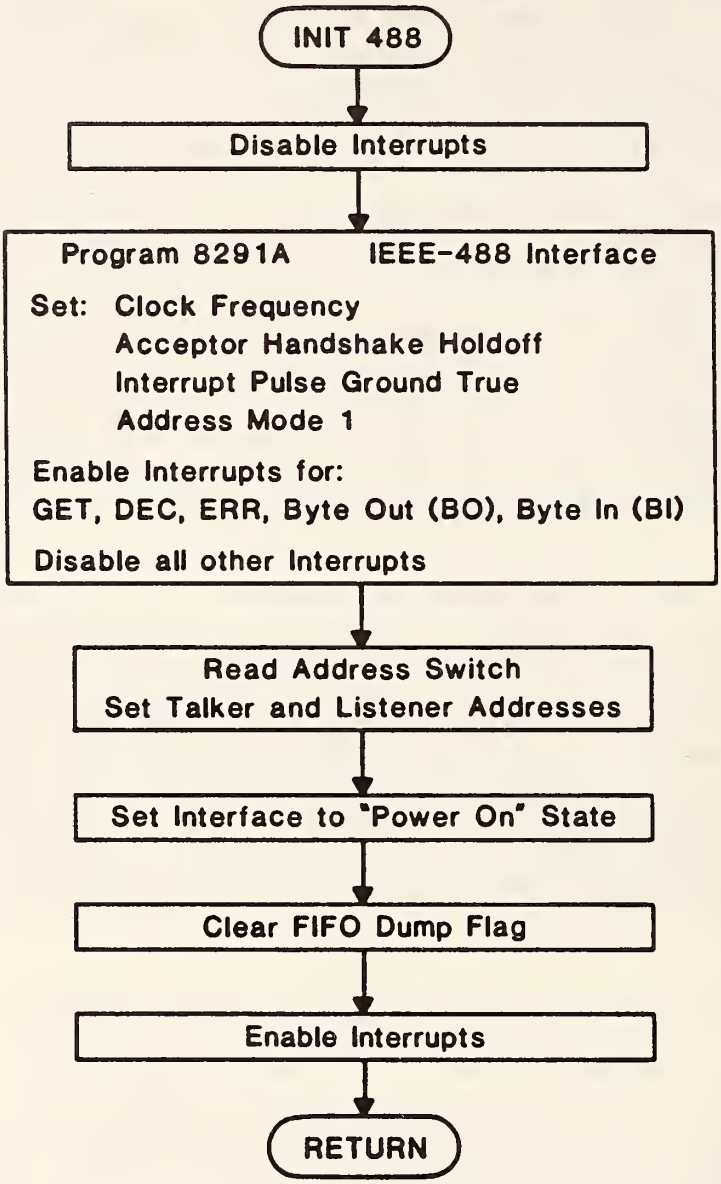


Figure 6.2

IEEE-488 Bus Interrupt Routine

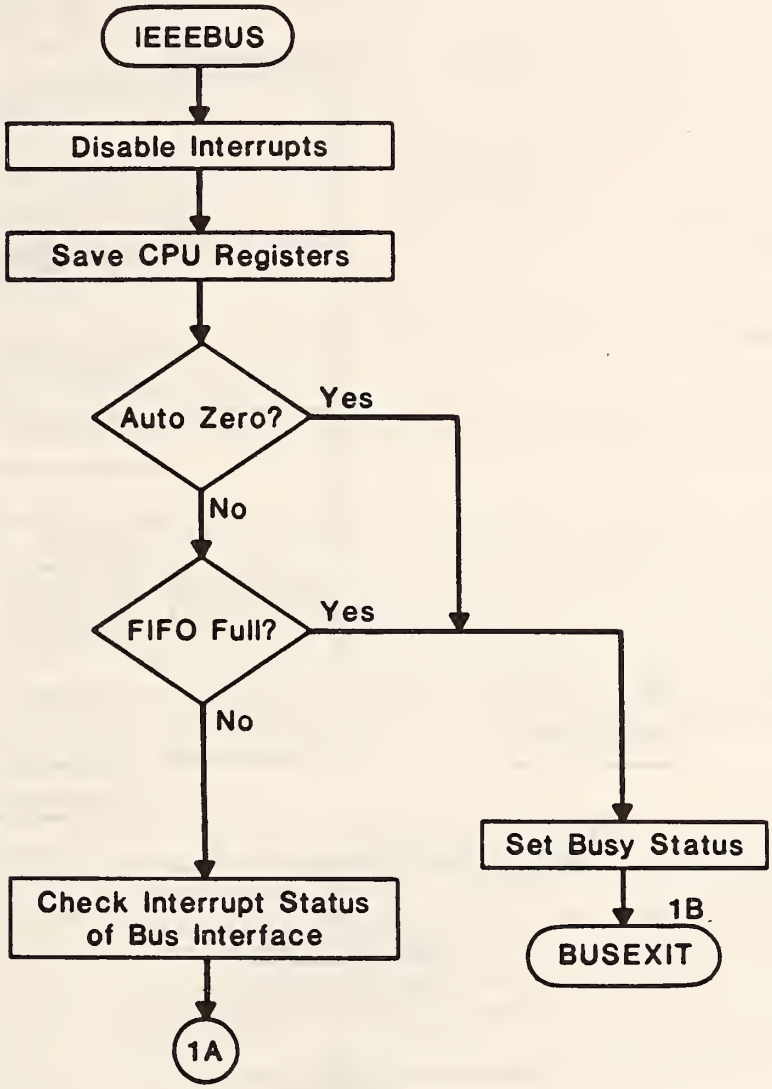


Figure 6.3(a)

IEEE-488 Bus Interrupt Routine (continued)

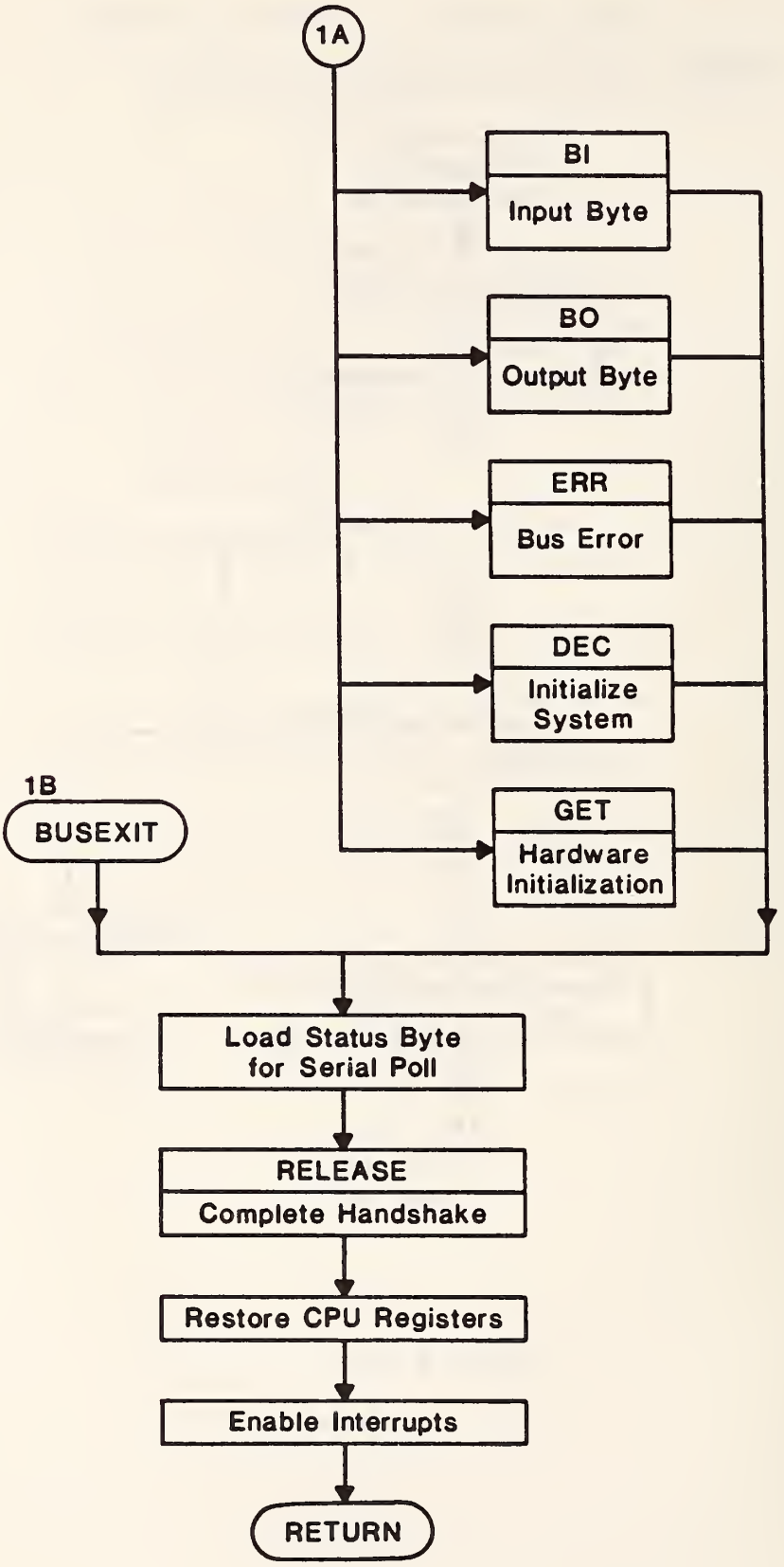


Figure 6.3(b)

Of the possible interrupt responses by the hardware [5], the following have been implemented:

(a) Request for a byte transfer from the controller to the system (Input)

(b) Request for a byte transfer from the system to the controller (Output)

(c) An error condition on the IEEE-488 bus

(d) A Device Clear command (DEC); resets the Phase Angle Standard system

(e) Local Lockout (LLO and LLOC); disables the keyboard of the Phase Angle Standard

(f) Local Lockout change (LLOC); resets interface and keyboard

(a) The input byte (ASCII character) is checked against a list of valid commands and parameters (figure 6.4). If a match is found, it is inserted into the software first-in-first-out register (see section 6.2 above); if no match is found, it is ignored. This screening prevents the 64-byte command and parameter storage area from being filled with meaningless information. As long as the first-in-first-out register is not completely full, the serial poll status byte is set to zero (normal condition); otherwise, a warning message is sent and the status byte is set to "busy."

(b) If the controller requests a message byte to be sent from the Phase Angle Standard (figure 6.5), it is assumed that a character string has already been stored in the interface output buffer. Further action now depends on the number of characters in the buffer which for the purpose of this program can take on a negative value. There are four cases: As long as the character count is greater than zero, characters are transfered, one by one, from the buffer to the bus. If the character count is zero, all characters have been sent and a carriage return is appended. The count is now -1, and on the next call from the interrupt routine a line feed character is sent. If the count is less than -1, no action is taken.

(c),(d),(e), and (f) Not shown in detail on the flow chart are the responses to an interrupt by the last four conditions. An error on the IEEE-488 bus causes an error status byte to be loaded into the serial poll status register. A "Device Clear" command causes a jump to the Phase Angle Standard system initialization routine, and the "Local Lockout" reconfigures the interrupt mask of the 8085 microprocessor so that it no longer responds to the keyboard (except for RESET). Reversing the Local Lockout is accomplished by reinitializing the IEEE-488 bus interface which resets the 8085 interrupt mask.

If an error condition has been encountered in Phase Angle Standard system rather than on the bus (figure 6.6), the stored system commands cannot be carried out. It is then necessary to insert a command to clear the error condition. To do this insertion, the first-in-first-out command storage register has to be reset to allow a command to be entered for immediate

execution. In order not to lose the stored commands, the bus output routine first transmits to the controller any remaining instruction or parameter bytes still in the first-in-first-out register and then sends the error message. The command and parameter bytes are therefore "saved" in the bus controller so that they can later be reloaded into the system while in the mean time an appropriate instruction is inserted to correct the error.

To make sure that various controllers recognize the end of a message from the system, a carriage return-line feed is sent and the end-or-identify (EOI) line is asserted.

Input Byte Subroutine

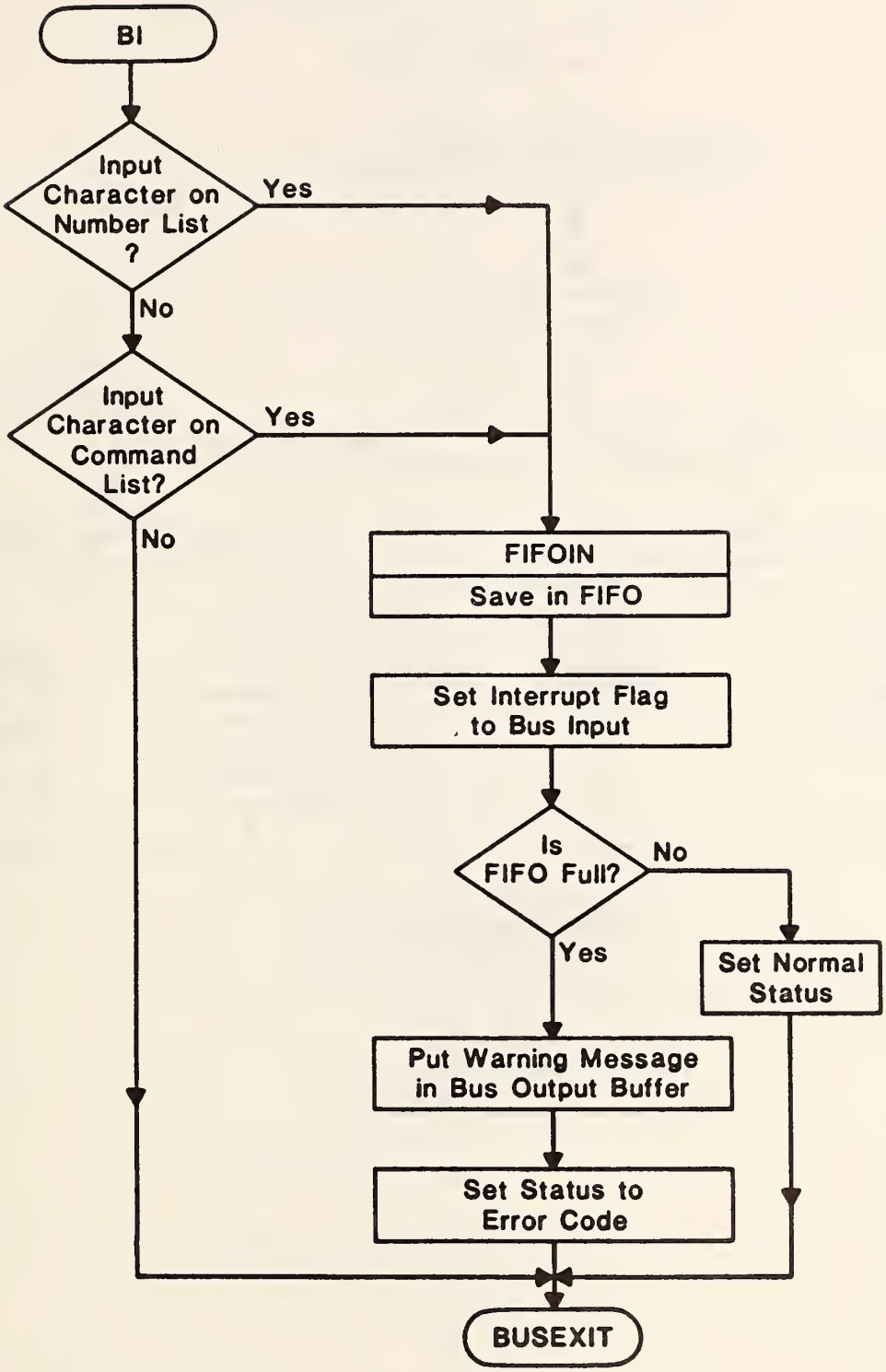


Figure 6.4

Output Byte Subroutine

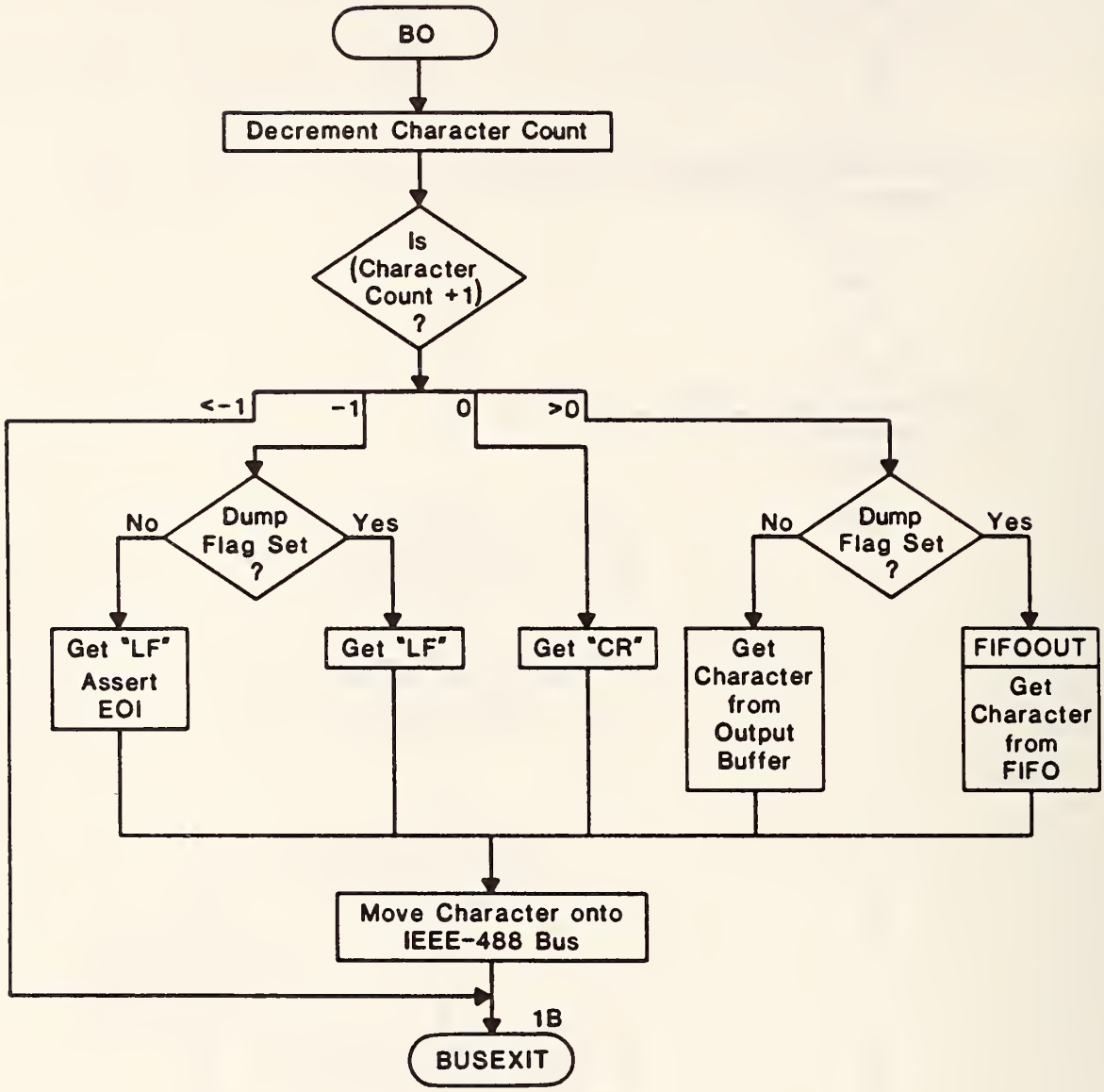


Figure 6.5

Error Routine for IEEE-488 Bus

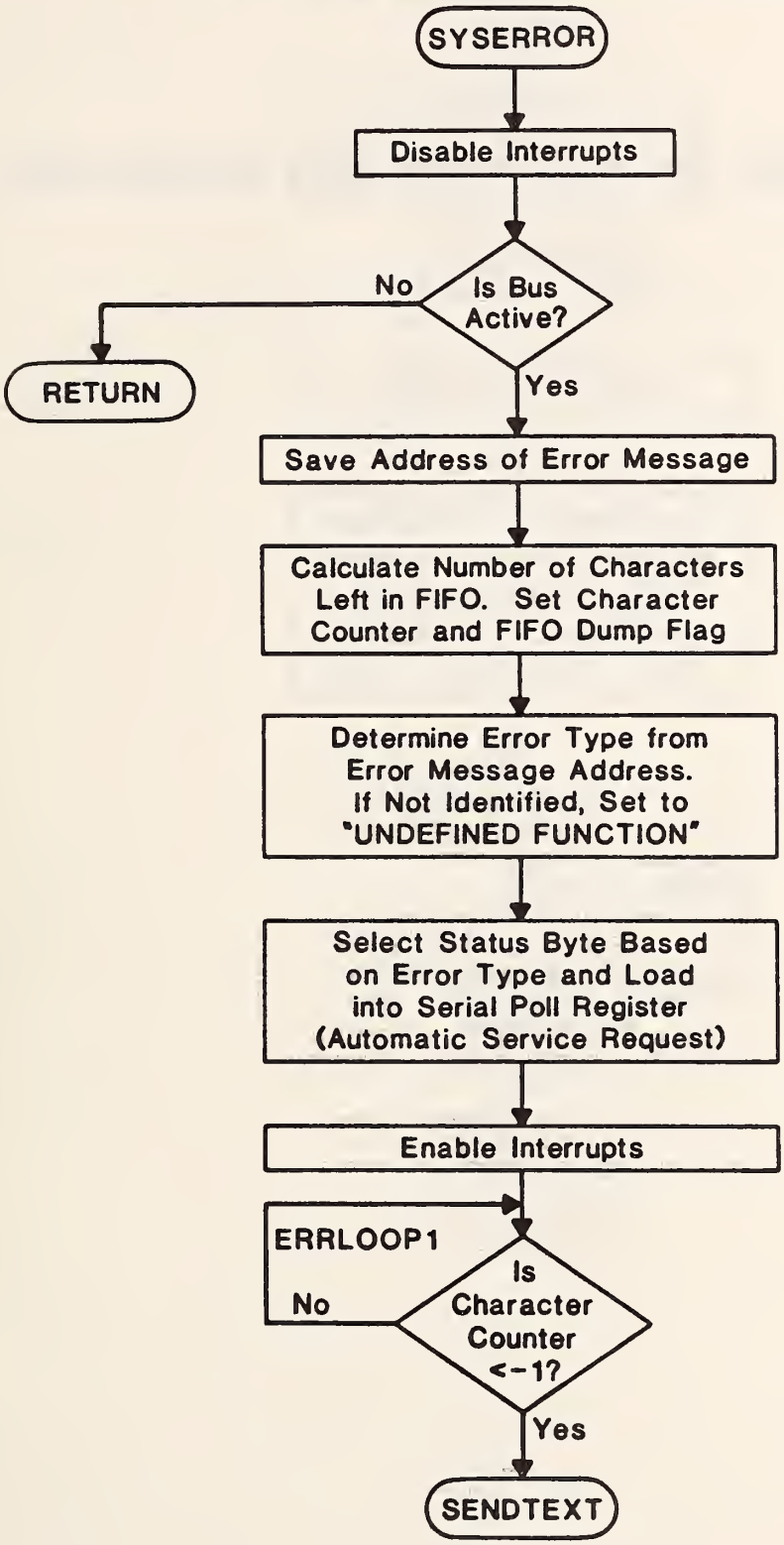


Figure 6.6(a)

Error Routine for IEEE-488 Bus (continued)

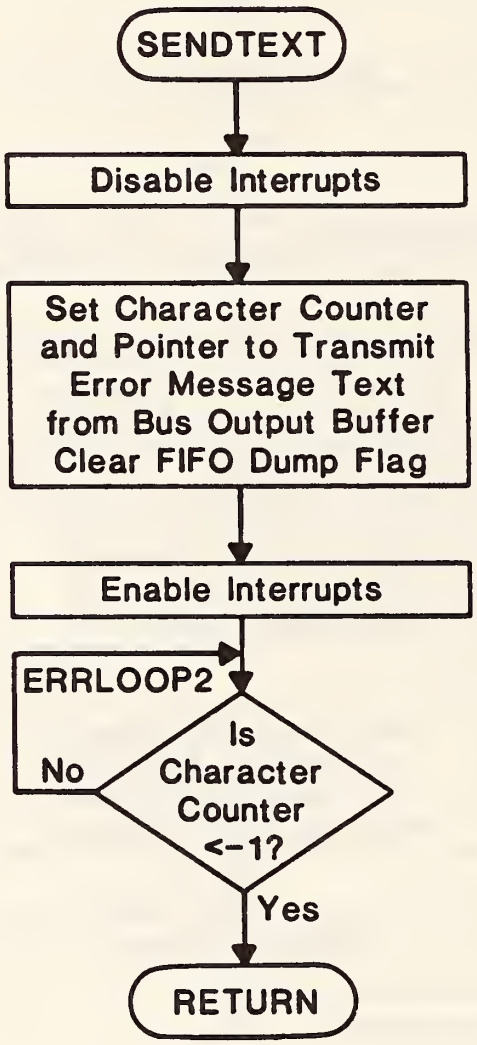


Figure 6.6(b)

Readout Text Transmission Subroutine

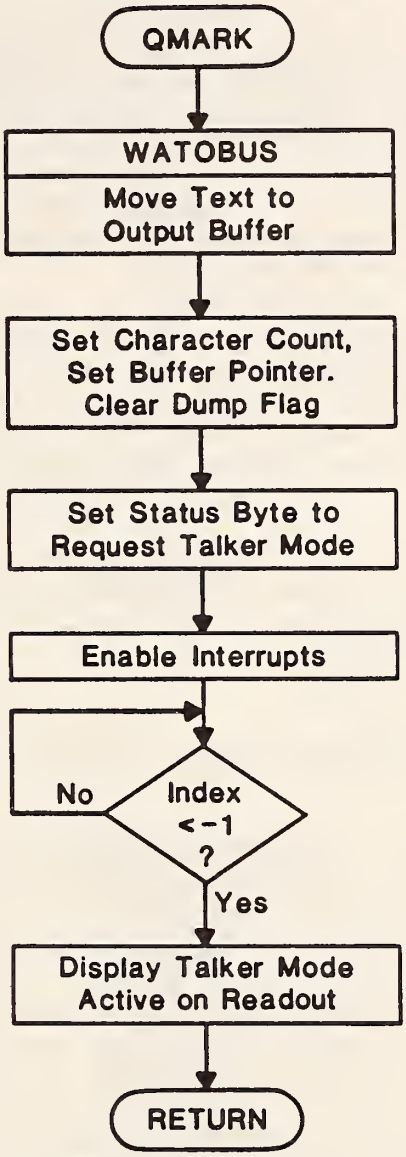


Figure 6.7

The ASCII character "Q" has been reserved as a Phase Angle Standard system command (sent from the bus controller) which causes the system to transmit the line on the instrument readout indicating the currently active function. The routine "QMARK" (figure 6.7) moves the 16 characters from the readout to the interface buffer area in memory, sets the character count (Index), and then puts a status byte on the bus requesting the talker mode. The routine continues by idling in a loop until the controller responds with a series of interrupts, and characters are transmitted, one by one, as described above (Output Byte Subroutine, figure 6.5).

Not shown on the flow charts is a time-out provision which is activated when the Phase Angle Standard system is in the talker mode. If for any reason transmission of the message to the controller is not completed, the interface circuitry is reset and an audible warning is given by the system. This prevents hang-ups on the bus due to incomplete hand-shakes or other disturbances.

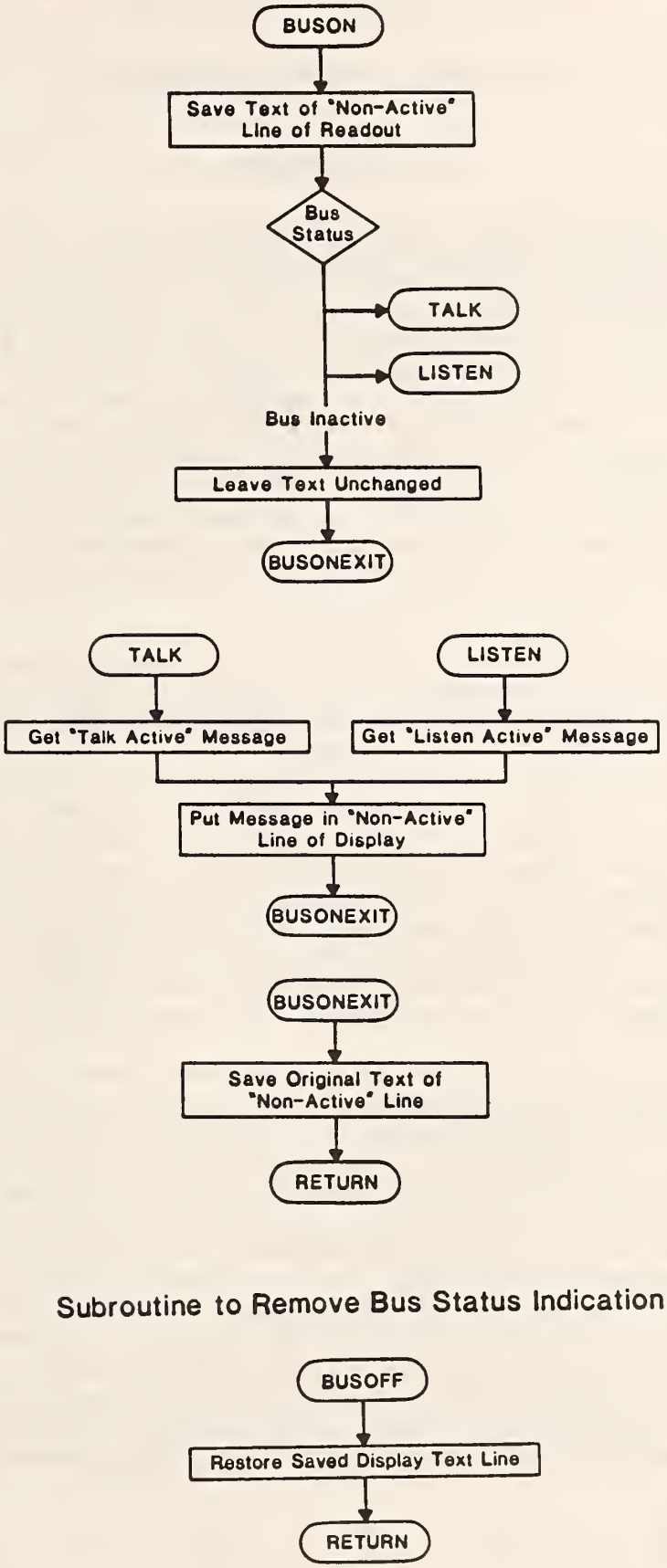
The routines indicated in figure 6.8 provide for an indication on the ("inactive" line of the) readout of the Phase Angle Standard whether the system is in the Listener Active or Talker Active mode and remove this indication when the bus is no longer active.

6.6 Test Mode Software

The Test Mode software has been designed primarily to provide operator interaction with some of the stored parameters at the bit level (see also discussion in section 3.2 (e)). A conversion routine, using a simple look-up table to translate the ASCII information from the keyboard input into hexadecimal numbers, and vice versa, permits setting and detecting individual bits on the 16-bit data bus. Applying these conversion routines, special routines are provided to set amplitudes, to set the phase detector attenuator, or to set the dc offset. Since the relays that control the amplitude range and select the digital-to-analog converter channel are also operated by bit combinations on the 16-bit bus, a further look-up table decodes the relay settings and displays the functional equivalent in readable form. Other Test Mode routines access auto-zero tolerance and settling time (delay) parameters to display or change their value.

Also part of the Test Mode software are some display oriented routines that work in conjunction with the auto-zero function. If the Test Mode has been activated any time after the system has been initialized or reset, a flag is set that causes a special set of display and conversion subroutines to be called. When the auto-zero function is activated, in the normal mode, these subroutines display, on the two lines of the readout, both the incremental and the total auto-zero correction (in degrees) after every iteration of the procedure. This display makes it possible to observe whether the auto-zero function converges properly or overshoots. After the auto-zero procedure is completed, it is also possible , using Test Mode routines, to display at any time the auto-zero correction previously determined as well as the frequency adjusted value of that correction.

Subroutine to Indicate Bus Status on Readout



Subroutine to Remove Bus Status Indication

Figure 6.8

7. PHASE ANGLE STANDARD PERFORMANCE

7.1 Test Methods

Two main parameters must be checked to evaluate the performance of the Phase Angle Standard, phase offset and phase linearity. Essentially, what needs to be determined is the correlation of a set of phase angles keyed into the standard, which can be thought of as equivalent to a "scale" of an instrument, with the actual phase angles measured between the two sinusoidal output signals. Since the system is intended to have a linear "phase angle scale," linearity is one of the performance characteristics that must be verified. It is dependent both on the accuracy of the computed digital signals from which the waveform is synthesized, as well on the digital-to-analog conversion process which includes converters, amplifiers, and filters. Fortunately, experience has shown that the properties of the components involved are very stable so that once the linearity parameters have been determined, frequent retests are not required.

Another important characteristic, the phase offset, must also be checked. This test can be thought of as aligning the "phase angle scale" so that the physical phase angle between the output waveforms coincides with the corresponding value entered into the standard. Phase offset may be caused by differential phase shifts in the converters, filters, and amplifiers of the two channels. In the Phase Angle Standard, the phase offset is compensated by the action of the auto-zero function. However, residual offsets cannot be completely eliminated, because the auto-zero correction is subject to noise and finite tolerances. Also contributing to the residual phase offset is the error arising from the approximation used in calculating the frequency compensated value of the auto-zero correction. The calculation is based on the assumption that value can be interpolated linearly with frequency. The experimental agreement with that assumption is close but not perfect.

A 180-degree bridge method may be used to check both linearity and phase offset. A more detailed discussion of this method will be found in [1] and [3]. The bridge is formed by the two outputs circuits of the Phase Angle Standard which are connected to opposite arms of a voltage divider. A tuned detector is connected from the tap on the voltage divider to the common (ground) terminal of the Phase Angle Standard. With the phase angle of the standard adjusted to a nominal 180 degrees, the bridge is balanced for amplitude by adjusting the tap on the divider, and for phase by fine adjustment of the phase setting of the standard. At frequencies up to about 10 kHz, an inductive voltage divider can be used for the arms of the bridge circuit. For higher frequencies the bridge arms can be assembled from two high-quality gas capacitors at least one of which should be variable. It is important to select components so that currents flowing through the divider do not exceed the capability of the generator at the test frequency.

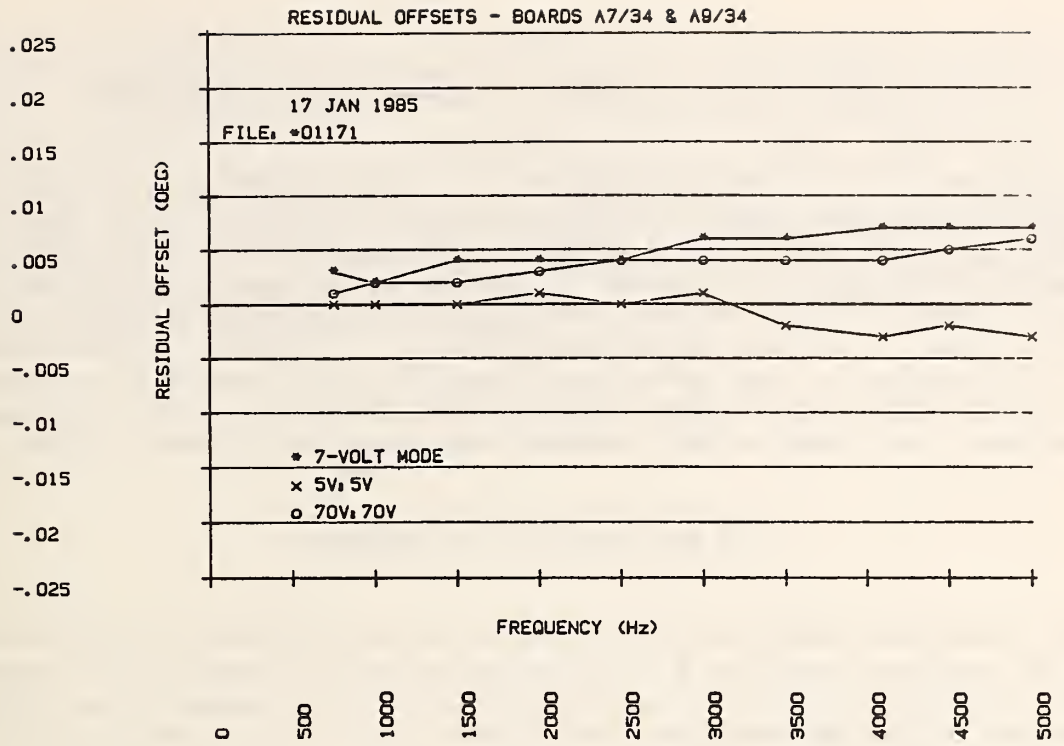


Figure 7.1 (a) Residual Phase Offsets after Auto-Zero, 0.5 - 5 kHz

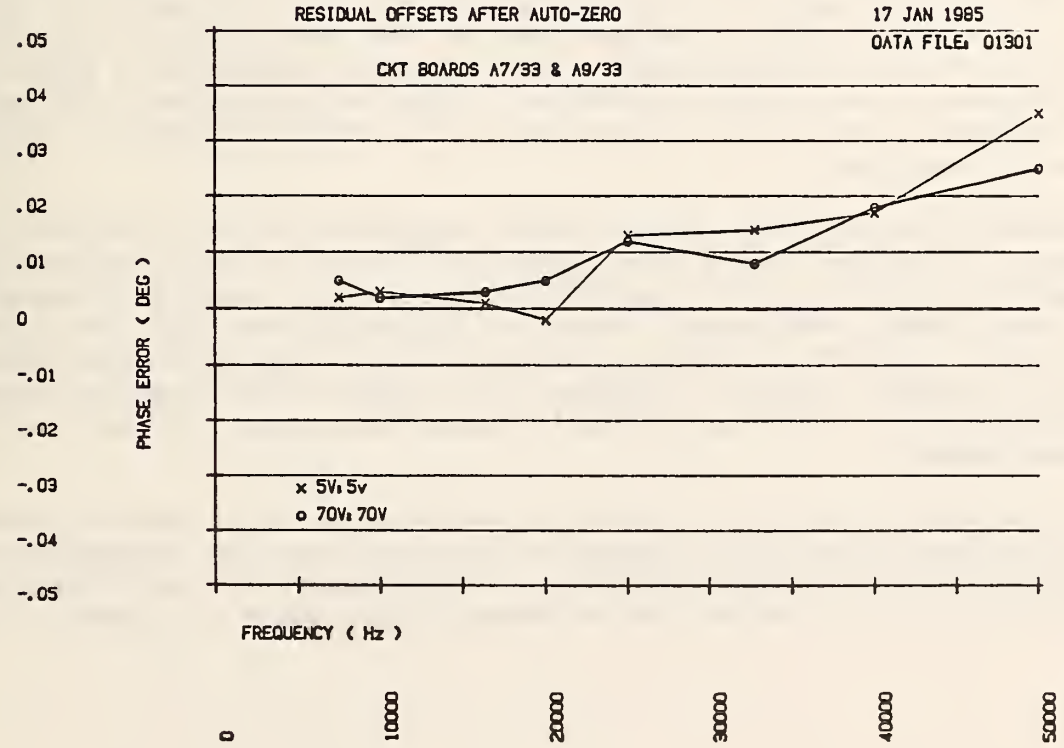


Figure 7.1 (b) Residual Phase Offsets after Auto-Zero, 5 - 50 kHz

7.2 Residual Phase Offsets after Auto-Zero Correction

The residual (uncompensated) phase errors are plotted as a function of frequency for various signal amplitudes (figure 7.1). From 2 Hz to 20 kHz the errors are contained within a band of 0.007 degrees and then increase to a maximum of 0.035 degrees at 50 kHz. As part of the procedure to determine the residual phase errors, the phase setting of the Phase Angle Standard must be displaced from its nominal value. Any such shift is subject to the linearity error. Consequently, the offset and linearity error contributions cannot be separated for this measurement. Usually, the linearity error component is smaller than the offset, except possibly near the upper frequency limit.

7.3 Amplitude Ratio Correction

As mentioned when describing the auto-zero software in section 6.4, a table is used to correct for a bias in the phase detector circuit when the output amplitudes of the Phase Angle Standard are unequal. The results of measurement of the residual phase error when using this look-up correction table are shown in figure 7.2.

7.4 Resolution and Linearity

The interrelation between the theoretical phase angle resolution and the combination of the number of samples per waveform and the number of voltage levels of the digital-to-analog converter has been discussed in [3]. As pointed out in the referenced paper, the attainable resolution is better than 0.001 degrees when a 16-bit converter is used and approaches 0.005 degrees, on the average, for 12-bit conversion at the highest frequency range (64 samples per waveform).

Because the converters are not ideal components, and also because of the presence of electrical noise, the theoretical linearity limits can never quite be reached in practice. It is therefore necessary to investigate experimentally how closely the actual linearity approaches the ideal. The number of measurements involved in an exhaustive test of the linearity is too large for practical purposes. However, advantage can be taken of the symmetry properties of the method of waveform generation to reduce the angular interval that must be investigated.

In terms of linearity, the worst case conditions exist when the waveform is synthesized from only 64 samples. For this case, the waveshape and its phase relative to some fixed reference, is determined by the instantaneous amplitude levels at the 64 sample points. As the phase is changed by 360/64

degrees, the same amplitude levels are again used to synthesize the shifted waveform, although the sequence of the set of amplitude levels has been rotated. Intermediate phase angles can be obtained by changing one or more pairs of amplitude levels. If a new set of amplitude levels is selected, yielding a waveform with a particular intermediate phase angle, then a shift by 360/64 degrees will result in a waveform which is reconstructed from the same, "new" set of amplitude levels but with sequence of amplitudes rotated as before. Therefore, it is sufficient to establish the linearity characteristics in one such 360/64-degree interval. The linearity properties of all other similar intervals can then be inferred.

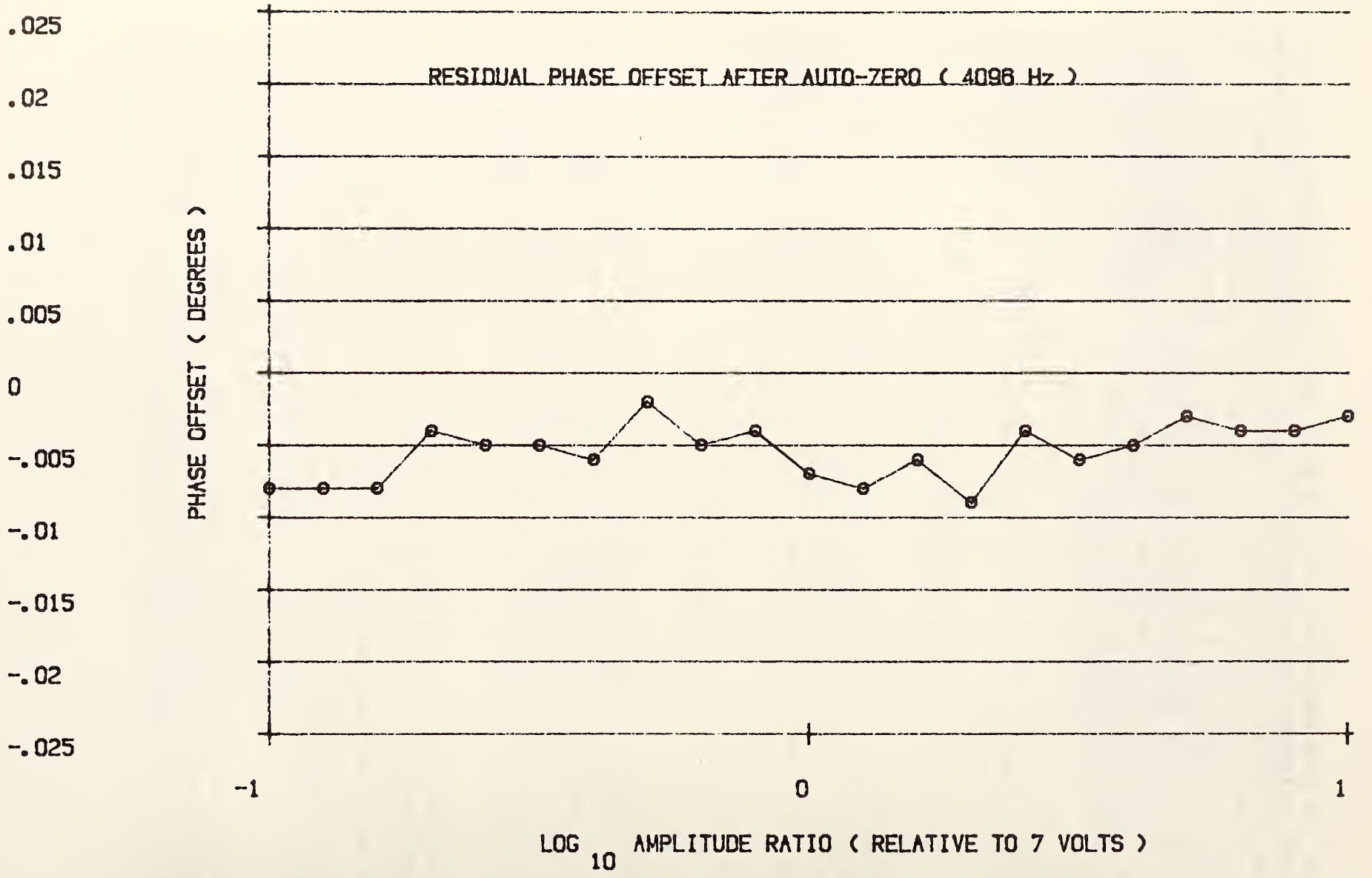


Figure 7.2 Residual Phase Offsets as a Function of Amplitude Ratio

Even for one such interval, however, testing every possible configuration is still an impractically long time-consuming procedure. Instead, an estimate of the limits of the linearity error can be obtained by making spot checks at about twenty phase angles selected so that they are not a binary subdivision of the interval. While spot checks do not determine the limits of error with absolute certainty, experience has shown that a repeatable and useful estimate can be obtained.

The linearity check of the phase angle scale can be performed with help of the 180-degree bridge already described. A design feature of the Phase Angle Standard permits the phase of each output to be varied independently with respect to an internal reference marker that is common to both signal channels. The calculations of the sine values from which the two waveforms are synthesized are carried out so that the instantaneous phase of each output can be set for the "initial" sample point. Thus, if it is desired to set the phase difference between the two output signals to 180 degrees, this can be accomplished by setting the "Reference" channel to any desired phase angle and adjusting the "Variable" channel so that the difference is 180 degrees. For example, the choices might be 0.000 and 180.000, 2.002 and 182.002, etc.

In general, the bridge balances at the selected phase angles will result in a series of phase differences that depart from the nominal 180 degrees. These departures from nominal will be due to the sum of a fixed systematic offset (of the phase angle scale) and a variable component caused by the linearity error. The variation due to non-linearity can be determined by subtracting the first reading (or the average of all readings) from each subsequent phase angle difference determination. Experimental results are shown in graphs for the two frequency ranges (16-bit and 12-bit digital-to-analog converters), figures 7.3 and 7.4.

7.5 Spectral Response

Strictly speaking, a phase angle between two waveforms is defined only if the waveforms are identical. Although the definition does not specify any particular waveshape, in practice it is difficult to generate identical waveforms except for pure sine waves. The spectral purity of the output of the Phase Angle Standard is therefore an important performance characteristic, particularly for wide-band phase meters. Fortunately, most high-precision phase meters are designed so that they are insensitive to even order harmonic components in the signal.

Using a spectrum analyzer, measurements were made at output frequencies of 50 Hz, 60 Hz, 5 kHz, and 50 kHz. The results of these measurements are shown in figures 7.5 to 7.7. At 50 and 60 Hz the harmonic components are -85 dB or less relative to the fundamental, at 5 kHz the relative harmonic amplitudes are -75 dB, and at 50 kHz the spectrum shows components up to -60 dB. The larger harmonic content at the upper frequency range is partially due to the higher quantization noise of the 12-bit converter, and some additional 10 dB of harmonic content must be attributed to distortion introduced by the converter and associated amplifiers.

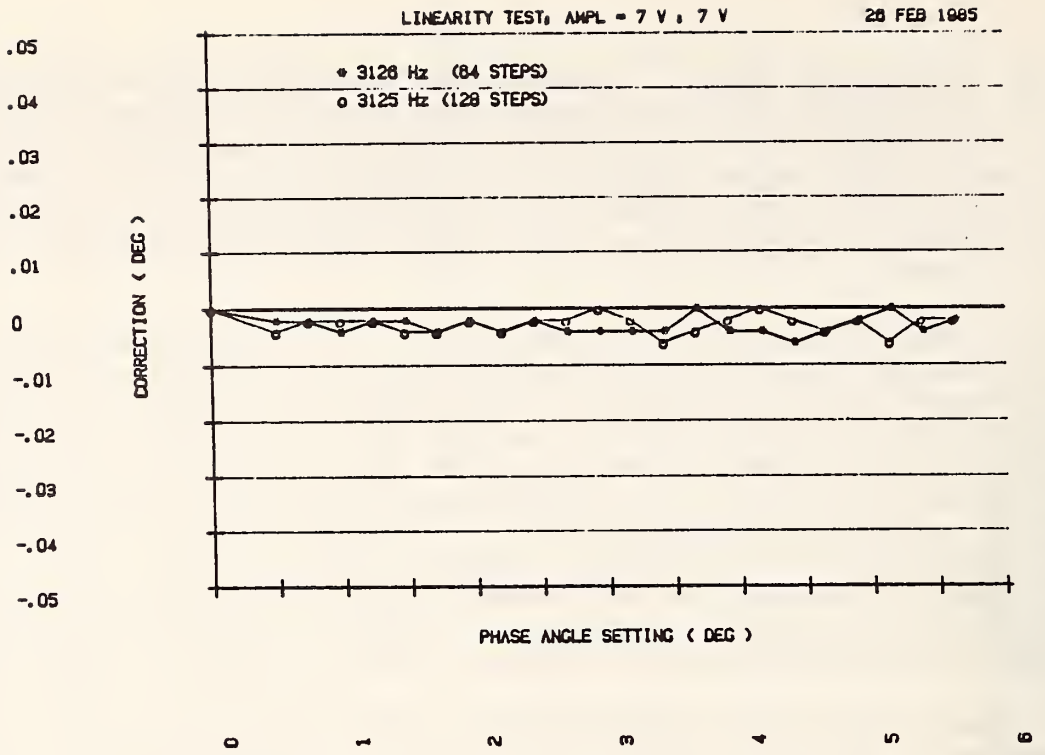


Figure 7.3 Phase Angle Linearity Test (3 kHz)

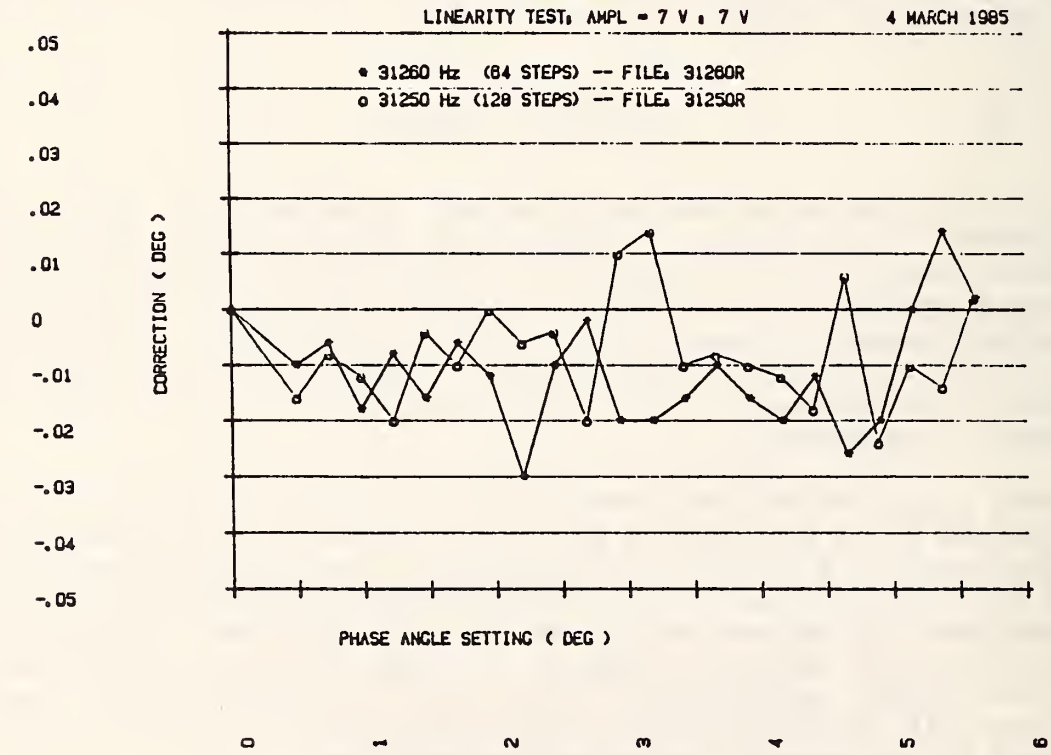


Figure 7.4 Phase Angle Linearity Test (30 kHz)

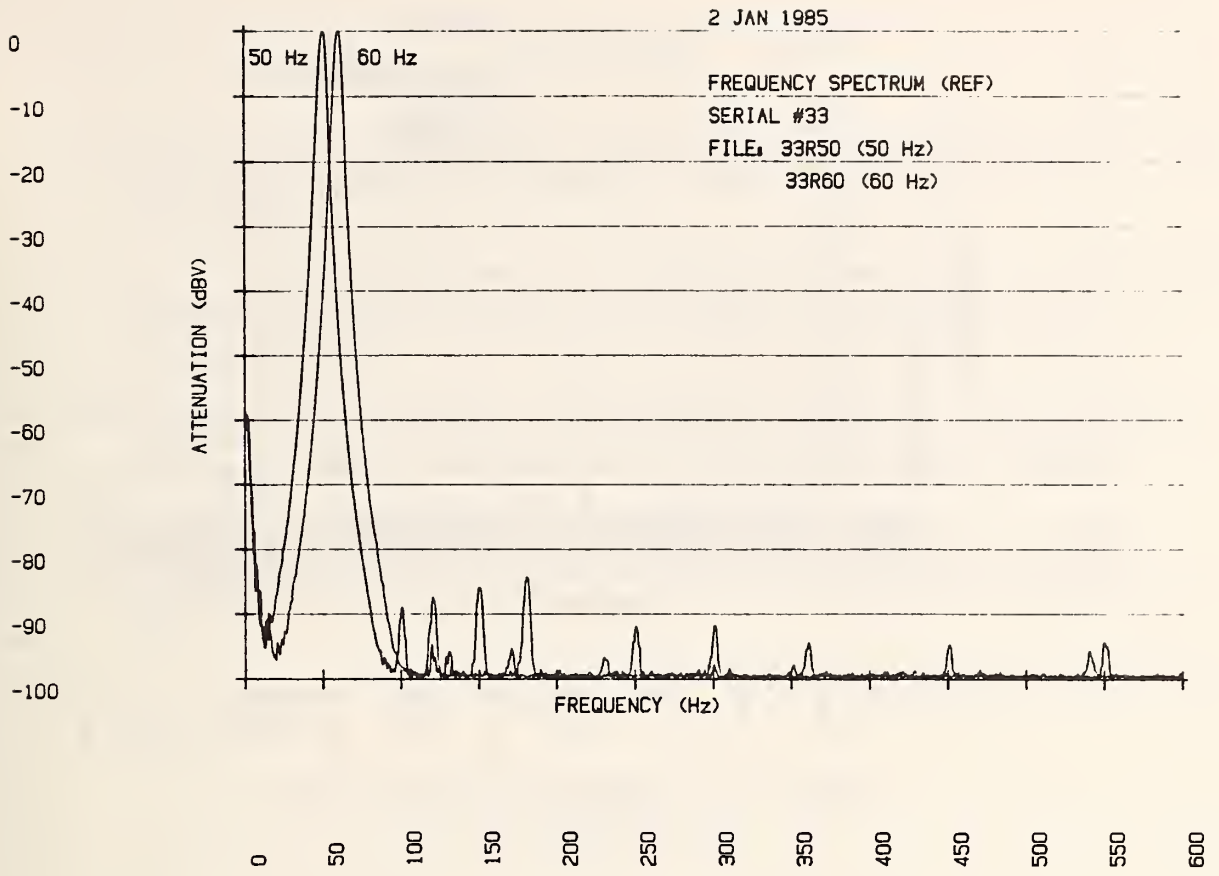


Figure 7.5 Frequency Spectrum (50 and 60 Hz)

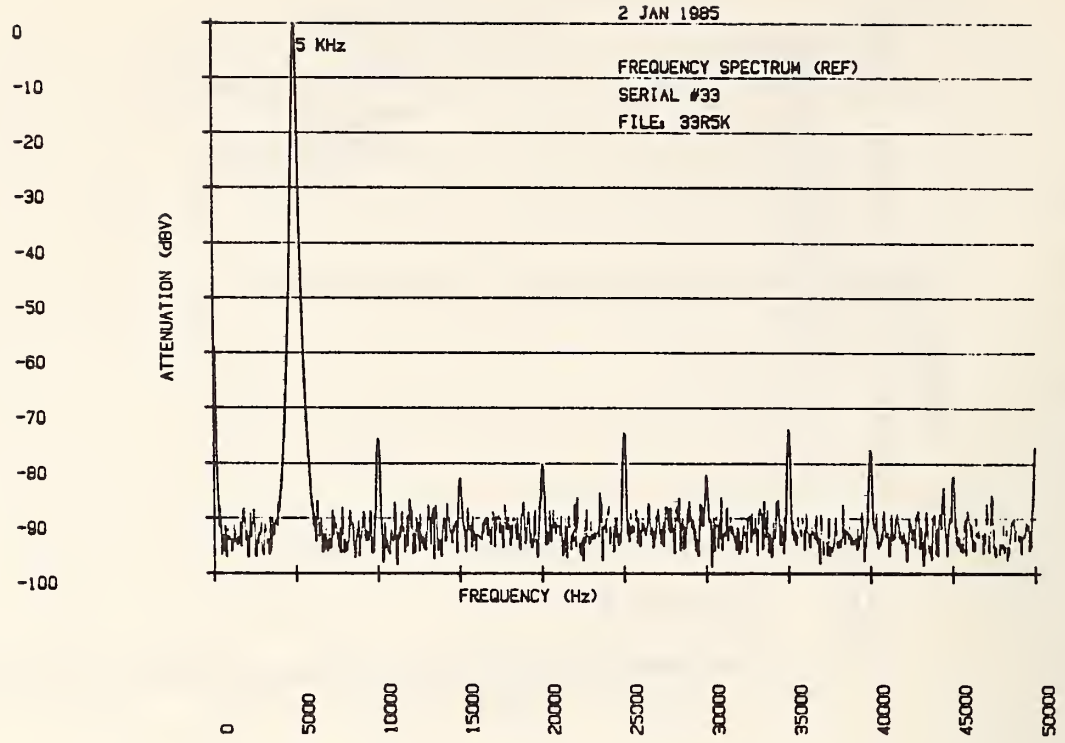


Figure 7.6 Frequency Spectrum (5 kHz)

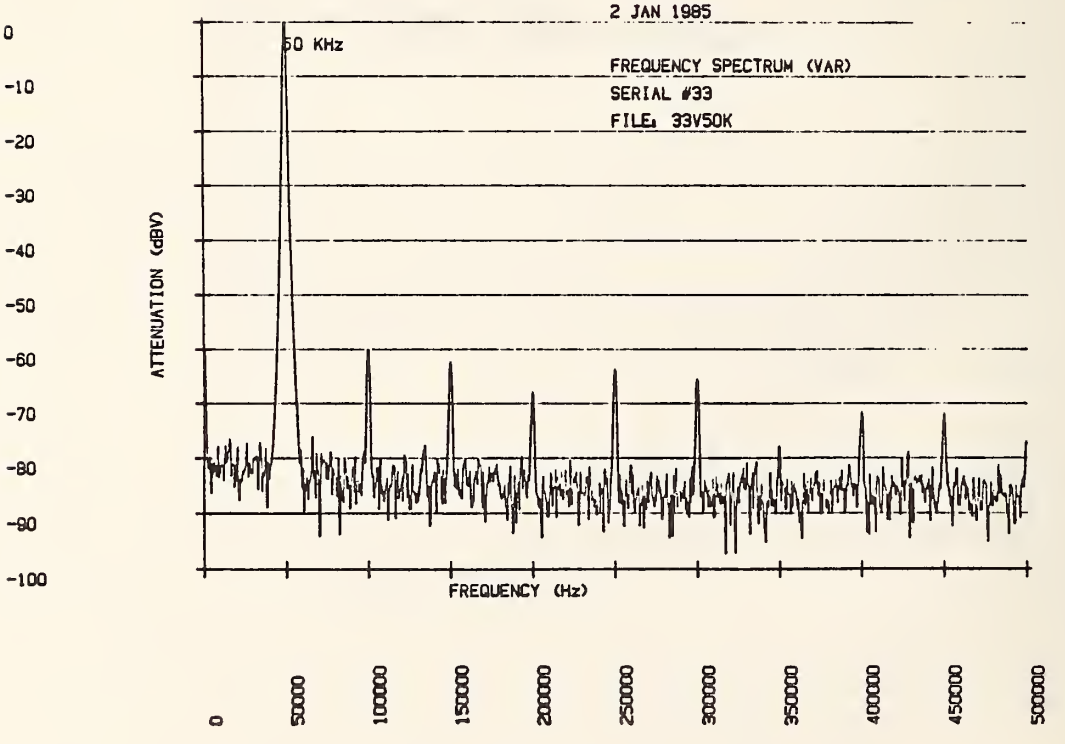


Figure 7.7 Frequency Spectrum (50 kHz)

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A detailed description is given of the features of an electrical phase angle calibration standard designed for operation over a frequency span of 2 Hz to 50 kHz. The phase resolution of this calibrator extends from just below 2 millidegrees at the low end of the frequency range to about 5 millidegrees at the high end. The uncertainty in the phase angle is a function of frequency, amplitude, and amplitude ratio of the two outputs. It varies from 5-50 millidegrees.

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