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Technical Note 113

A TRANSISTOR-MAGNETIC CORE DIGITAL CIRCUIT

U. S. DEPARTMENT OF COMMERCE
NATIONAL BUREAU OF STANDARDS

THE NATIONAL BUREAU OF STANDARDS

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NATIONAL BUREAU OF STANDARDS

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113

JUNE 1961

A TRANSISTOR-MAGNETIC CORE DIGITAL CIRCUIT

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GLOSSARY OF SYMBOLS

SECTION 1.

x	measures the excitation at the input to an element or an element-group; or, it measures the externally induced portion of the total excitation, in the case of the propagation function.
y	is a measure of the output signal from an element-group.
n	is the number of element- or element-group transmissions that a signal has undergone.
r	serves to define the binary ONE signal ($x > r$), and the binary ZERO signal ($x < r$).
g	is called the signal gain. It is the slope of the transfer-function $y = f(x)$ at $x = r$.
L_2, L_1	are the upper and lower limits on the output from an element or an element-group.
s	is the maximum possible value ($L_2 - L_1$) of the signal that can be emitted by an element or element-group. It is the magnitude of the full binary ONE signal. The full binary ZERO signal has zero magnitude.
a	is the bias introduced into the element transfer-function in order to produce ZERO-stability.
a_n, a'_n	see Figure 12, b.
m	is the signal magnitude m disturbance-free transmissions before the introduction of the external excitation x.
t_δ	is the time interval between disturbances to a given signal.
Δf	is the element or element-group bandwidth.
P	is the element- or element-group gain-bandwidth product $g\Delta f$.

SECTION 2.

t_d	is the element-group delay time. It is the time interval between the moment of arrival of a signal at an element-group input and the beginning of the transmission of that signal to the next element-group. See Figure 22.
T	is the element-group cycle time. It is the time required for the element-group to go through all the states involved in the passage of a signal and to return to its initial state. See Figure 22.
t_r	is the element-group receive-interval or rise-time $t_r \simeq (\Delta f)^{-1}$.

GLOSSARY OF SYMBOLS (Continued)

SECTION 3.

n_1	is the number of turns in the magnetic core input winding.
n_2	is the number of turns in the core output winding.
v	represents instantaneous voltage.
x, y	in the case of the magnetic amplifier and the transistor-core amplifier are measured in volt-seconds.
ϕ	represents magnetic flux.
v_c	is the instantaneous core input voltage.
s_w	is the constant-current switching coefficient of the core material.
l	is the core mean magnetic path length.
i	is the core input winding current.
i_o	is the core input magnetizing threshold current.
τ	is the time required to switch the core from one full remanent state to the other.
ϕ_r	is the full remanent flux of the core.
R_c	is the dynamic switching resistance of the core, referred to its input winding.
R_s	is the value of the core input series resistor.
v_o	is the peak value of the clock sine wave voltage.
t_o	See equation 30 and Figure 34.
m	is defined by $m = i_o R_s/v_o$. It is a measure of the threshold nonlinearity of the resistor-core transfer-function.
v_{co}	is the peak value of the core input voltage.
i'_o	is the core indepently variable threshold current defined by $i'_o = i_o + i_b$, where i_b is an external bias current.

SECTION 4.

V_p	is the d-c pull-up supply voltage.
R_p	represents a pull-up resistance. See Figure 44.
R_{po}, R_{p1}	See Figure 51.

SECTION 5.

B_1	is a small bias voltage shown in Figure 52.

SECTION 6.

β	is the common-emitter current gain of the transistor.
α	is the transistor common-base current gain.
$f_{\alpha b}$	is the transistor alpha cutoff frequency.
V_e	is the emitter supply voltage.

SECTION 6 (Cont'd)

R_e represents the value of the transistor emitter resistor. See Figure 53.

V_c is the collector supply voltage.

X equals $x\ (\frac{v_o T}{\pi} - 1)$

Y equals $y\ (\frac{v_o T}{\pi} - 1)$

G in this section, represents the emitter-follower incremental-area (volt-seconds) stretching factor. It is, for example, the slope of the portion of the curve in Figure 56 between 2 volt-μsec and 2.4 volt-μsec. In Figure 55 it is the ratio of the shaded area to the dark area.

SECTIONS 8, 9 and 10.

y_n is the volt-second output signal of a negating core element.

A_1, A_2 See Figure 68.

y_a is the volt-second output signal of an assertive core element.

SECTION 11.1.

G in Section 11 denotes current gain.

N denotes logical fan-out.

L_{co} is the saturation inductance of the magnetic core output winding.

$\hat{i}$ is the peak value of the total current drawn by the core input winding during the receive interval.

$\underline{\hat{i}}$ is the peak value of the excess current drawn by the core input winding during the receive interval.

L_{c1} is the effective full-switching inductance of the core output winding.

G_c is the maximum current gain of the core, i.e., the gain when fully loaded.

μ is the average permeability within the volume of the core output winding.

A is the cross-sectional area enclosed by the core output winding. See Figure 78.

A_m is the cross-sectional area of the core magnetic material. See Figure 78.

μ_m is the switching permeability of the magnetic core material.

μ_o is the permeability of free space.

F_s is the space-factor, A_m/A, of the core output winding.

k_m is the effective switching relative permeability of the core material.

B_r is the core remanent flux-density.

H_c is the d-c coercive force of the core material.

F_{w1} is the winding factor, n_1/l, of the core input winding.

F_{w2} is the winding factor, n_2/l, of the core output winding.

GLOSSARY OF SYMBOLS (Continued)

SECTION 11. 1 (Continued)

$\Delta\phi$, ΔB represent changes in core flux and flux density respectively.

Z is the dimensionless fractional switching variable, $\Delta B/2B_r$.

f_c is the operating frequency, or clock frequency. $f_c = T^{-1}$.

$P_R(1)$ is the core resistance-frequency product $R_c f_c$. It has a constant value $P_R(l_o)$ for a given wound core bobbin.

$P_G(1)$ is the core current-gain frequency-squared product $G_c f_c^2$. It has a constant value $P_G(l_o)$ for a given wound core bobbin.

$P_s(1)$ is the core spacefactor-frequency product $F_s f_c$. It has a constant value $P_s(l_o)$ for a given wound core bobbin.

p_R represents the product $R_c f_c^{5/4}$. It has a constant value when the core design is scaled in accordance with equation (105), which preserves a constant space-factor.

p_G represents the product $G_c f_c$. It is constant when the core is scaled according to (105).

p_1 represents the product $(1/l_o)f^{1/4}$. It is constant when the core is scaled according to (105).

SECTION 11. 2.

G_i is the current gain of the transmag amplifier input circuit. See equation (118a).

$\hat{i}_c$ is the peak value of the core input current during the receive interval. In 11. 1 it was represented by i.

i_p in the constant-current case, is the least value of the current that must flow in one input AND-gate in order to transmit a full ONE to the input circuit. Or it is the instantaneous value of the AND-gate current when this current varies. See Figure 81.

i_b represents the instantaneous value of the transistor base current. See Fig. 81.

i_D is the current in the input power diode D_{pi}. See Figure 81.

$\hat{i}_b$ is the maximum value of i_b.

I_D is the minimum permissible value of i_D.

$\hat{i}_{b1}$ is the value of $\hat{i}_b$ under case 1 in Section 11. 2.

C_i is the virtual capacitance in the emitter-follower input equivalent circuit.

X_i is the reactance of C_i at the frequency $\omega = 2\pi f_c$.

R_L is the complete emitter-follower load.

r_b is the transistor base resistance.

ω_{ab} is the transistor radian alpha cut-off frequency.

ω equals $2\pi f$ or $2\pi f_c$.

SECTION 11.2 (Continued)

β_o is the low-frequency small-signal beta of the transistor.

G_F is the current gain of the emitter-follower alone.

v_b is the transistor base instantaneous voltage. See Figure 82.

I_{Do} is the current at which the forward small-signal resistance of D_{pi} equals 100 ohms.

I_p is the minimum permissible value for i_p such that sufficient charge is stored by the base to give adequate signal stretching.

i_{po} is the value of i_p when $\omega t = o$.

r_D is the forward resistance of the input power diode D_{p1}.

r_{Do} is the value of r_D at the forward current value I_{Do}.

$f_{\alpha bo}$ is the minimum required alpha-cut-off frequency for the emitter-follower transistor.

h_{ao} is the collector dissipation for the (unclamped) assertive amplifier for all ZEROs. See Appendix VIII.

h_{c1} is the collector dissipation for the assert-negate amplifier for all ONEs. See Appendix VIII.

h_{a1}, h_{co} See Appendix VIII.

SECTION 11.3

C_s is ground (stray) capacitance of a fan-out lead.

I_o is the minimum current required to keep D_{po} conducting, and to ZERO the core through its input winding.

C'_s See Figure 85.

A TRANSISTOR-MAGNETIC CORE DIGITAL CIRCUIT

E. W. Hogue

ABSTRACT

A digital amplifier of simple noncritical design incorporating an emitter-follower and a small magnetic amplifier is described. Timing and some of the operating power are provided by a 300-kc 2-phase 7-volt sine-wave source. In structure and mode of operation, the amplifier is particularly suited for use with two-level diode gating to provide the AND and OR logical operations. A NOT-amplifier provides negation with amplification. The volt-second transfer characteristic of the stage critically determines the stability of propagation of binary signals. Factors governing the required shape of this transfer characteristic are discussed.

1. INTRODUCTION

The transistor-core digital circuit is useful in itself, but what is more important, it provides a detailed example of the application of binary-signal network concepts and methods of analysis that the autnor believes can prove fruitful as a systematic approach to the invention and design of solid-state computer circuits particularly well suited to increasingly severe requirements for high speed, micro-miniaturization and automatic fabrication.

Computer nets are here regarded, in a very general way, as interconnected open and closed sequences of identical nonlinear elements or element-groups that receive and transmit the signal during alternating nonoverlapping time intervals, and that are therefore capable of signal retention, or storage. All that is required for stable propagation of binary signals is that the element- or element-group transfer-function be properly nonlinear. Elements that are, in themselves, improperly nonlinear are shown to be combinable into properly nonlinear groups.

Then a set of propagation-functions that describes the binary signal itself, giving its magnitude and stability margins at every element-junction, is derived from the transfer functions. The ratios of the stability margins to the full-signal magnitudes indicate the circuit resistance to interference and are needed in the calculation of power gain and maximum fan-out.

Finally because in well-designed synchronous systems the chief source of failure is the synchronizer, a formula is derived which gives the maximum permissible unsynchronized signal input frequency $\hat{f}_i$ as a function of the element-group delay time t_d, the element-group transfer-function slope g, and any specified maximum probability p for the occurrence of an imperfect output signal from the synchronizer. $\hat{f}_i$ is ordinarily less than one-twentieth the element-group reaction speed

t_d^{-1} in synchronous systems and bears roughly the same ratio to the reaction speed or reciprocal response time t_r^{-1} of the active components in the elements of asychronous systems, although f_i for asychronous systems is not mathematically defined.

The internal bit-rate, on the other hand, can be as high as one-half the element-group reaction speed in synchronous systems, while in asynchronous systems it must not exceed $\hat{f}_i$. At bit-rates higher than $\hat{f}_i$, asynchronous systems become chaotic. Such systems require nearly ideal (square-loop) element transfer-functions. These are possible only at low bit-rates, relative to t_r^{-1}, with active computer elements that are self-regenerative through positive feedback.

It is shown that elements having no positive feedback and whose transfer-functions are far from ideal may be used to construct synchronous high-bit-rate computing systems having predictable synchronization failure rates.

2. REQUIREMENTS FOR STABLE BINARY-SIGNAL PROPAGATION

The preservation of the identity of a binary signal during its propagation in a computer network requires that the elements of the network fulfill certain conditions. In the simplest case a computer network may be thought of as made up of cascades and rings of (ideally) identical unilateral elements. Fig. 1a shows a cascade of six elements, and Fig. 1b shows a ring of six elements. The signal is

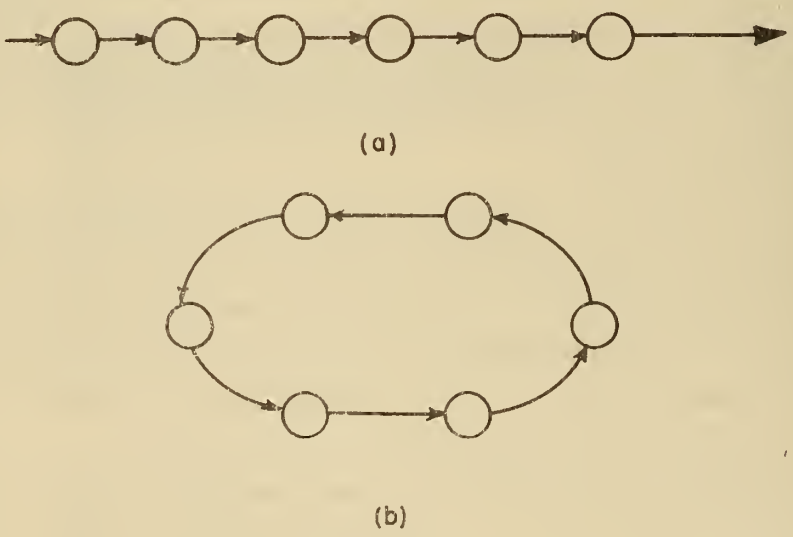


Figure 1. a. A cascade of computer elements
b. A ring of computer elements

propagated through each element in succession, and may traverse many elements, each only once, in the case of a long cascade; or it may traverse a few elements, repeatedly, many times in the case of a ring. The nature of the signal transfer-function of an element, must therefore be governed by how

it affects the overall transfer function, or propagation function resulting from n transmissions of the signal as n approaches infinity.

If f(x) is the transfer function of one element, then after n undisturbed transmissions through that element, or others like it, a signal, whose initial value was x, has the value $y = f^n(x)$. $f^n(x)$ is the transfer function for n transmissions of a signal through elements each having the individual transfer-function f(x). n denotes the number of iterations of f(x). For example, if n = 3,

$$f^3(x) = f\{ f [f(x)] \} \qquad (1)$$

Observe also that $f^1(x) = f(x)$, and $f^0(x) = x$.

Before anything more can be said about the nature of f(x) it is necessary to define the binary signal in terms of the transmitted quantity x. If r is some fixed value of x, then the binary ONE is sufficiently defined if it is identified with values of $x > r$; and the binary ZERO is sufficiently defined by $x < r$. See Fig. 2. Up to this point r may have any value, but practical

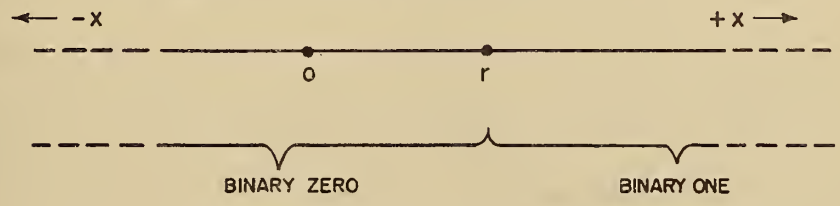


Figure 2. Representation of the binary digits

considerations will be shown to restrict its choice somewhat.

2.1 Evolution of the Digital Amplifier Transfer Function

Returning to the transfer function f(x), if it is postulated to be gx; (g = constant > 0) which is that of an ideal linear non-inverting amplifier having a gain g equal to the slope of the curve in Fig. 3, it is seen that if r = 0, $y = f^n(x) = g^n x$ preserves the relationships $y > r$ for $x > r$, and

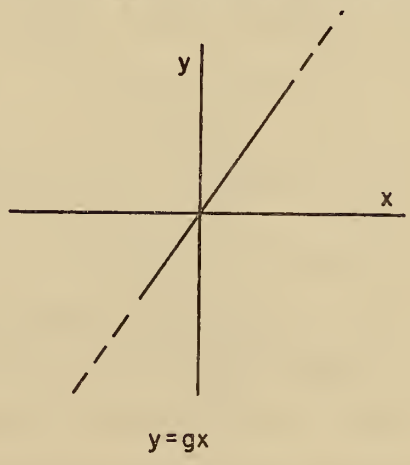


Figure 3. Transfer-function of the ideal, linear, non-inverting amplifier

$y < r$ for $x < r$ for any n provided $g \geq +1$. However, if $|g| < 1$, $y = g^n x$ approaches zero with increasing n, and if $g < 0$ the sign of $g^n x$ alternates. Therefore if $f(x) = gx$, g should be equal to or greater than unity for successful binary signal propagation.*

A further modification of f(x) becomes necessary in any physical embodiment of the computer element to prevent the occurrence of infinite signals, since $y = f^n(x) = g^n x \rightarrow \infty$ as $n \rightarrow \infty$ if $g > 1$. y must therefore be limited to some finite range $L_1 < y < L_2$. See Fig. 4, which illustrates the transfer function

$$f(x) = \left\{ \begin{array}{l} gx;\ L_1/g < x < L_2/g \\ L_2;\ x > L_2/g \\ L_1;\ x < L_1/g \end{array} \right\} \quad g > +1$$

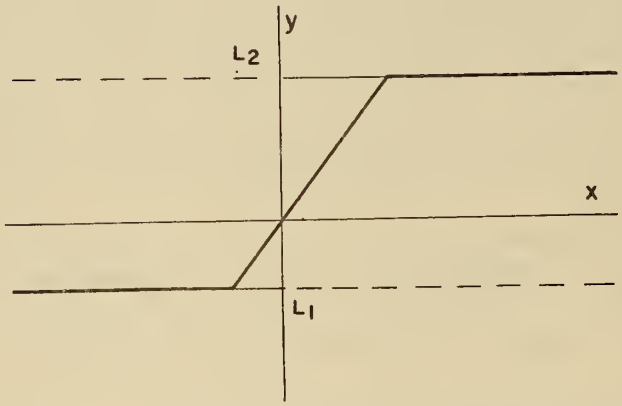


Figure 4. Saturating amplifier with positive and negative output limit-levels

Then, (for simplicity,) L_1 is set at zero so that the element has a unipolar output. See Fig. 5, which illustrates the transfer-function

$$f(x) = \left\{ \begin{array}{l} gx\ ;\ 0 < x < L_2/g \\ L_2\ ;\ x > L_2/g \\ 0\ \ ;\ x \leq 0 \end{array} \right\} \quad g > +1$$

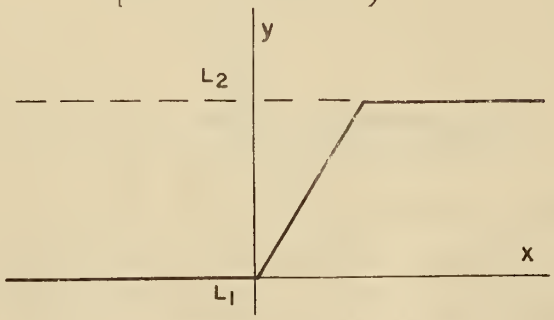


Figure 5. Amplifier with zero and positive output limit levels

* See, however, section 9 and Appendix IX where it is shown that $g<0$ is also admissible, provided $|g| > 1$.

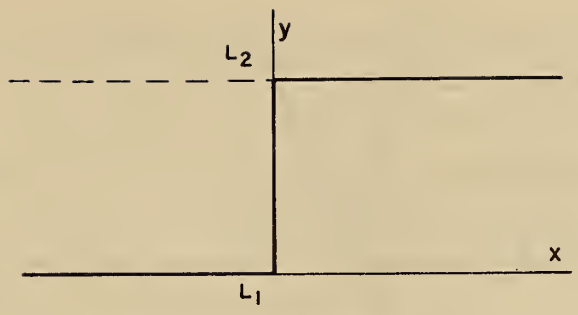


Figure 6. Overall transfer-function of an infinite cascade of elements having individual transfer-functions similar to Figure 5.

Fig. 6, which shows the transfer-function

$$f^{\infty}(x) = \begin{cases} L_2 & ; \quad x > 0 \\ 0 & ; \quad x < 0 \end{cases}$$

now reveals a serious practical defect in the transfer function of Fig. 5. It is that the noise sensitivity of a cascade of n elements having this transfer function approaches infinity as $n \longrightarrow \infty$. In the presence of a.c. input noise, the steady-state output of a cascade of many elements is a random sequence of binary ONES and ZEROS. Such a cascade is said to be astable because it has no output that can persist in the absence of an input signal and in the presence of input noise.

If a ring of even a small number of elements each having the transfer-function of Fig. 5 is formed, the ring transfer-function, in the steady state, will also have an infinite slope g^{∞}, because the ring, while finite, is endless so that the number of times a signal or disturbance is transmitted by an element becomes infinitely large with increasing time. In fact the transfer-function of a finite ring includes that of the infinite cascade of Fig. 6. But the ring is not astable; it is monostable or more precisely, ONE-stable. The characteristic of Fig. 5 guarantees that, in the presence of any noise having a positive component, all elements will ultimately transmit full binary ONE signals having a magnitude s determined by the upper limit level L_2. And since each element continually transmits a signal of magnitude s, each element continually receives a signal of magnitude s from the one ahead of it. This is shown by the point marked S on the transfer function for a single element as postulated so far. See Fig. 7. Remembering that a binary ONE is any signal greater than zero, it is seen that the continued presence of a negative disturbance at the input of an element, greater in magnitude than s, is required to produce a binary ZERO output. With the removal of this disturbance, the ring reverts to the ONE state.

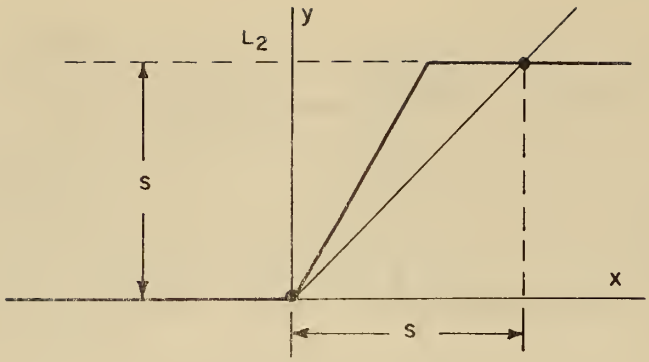


Figure 7. Definition of the full signal magnitude s

The steady-state transfer function of a finite ring of elements having individual transfer-functions of the type shown in Fig. 7 can now be drawn. It is shown by the heavy line in Fig. 8,

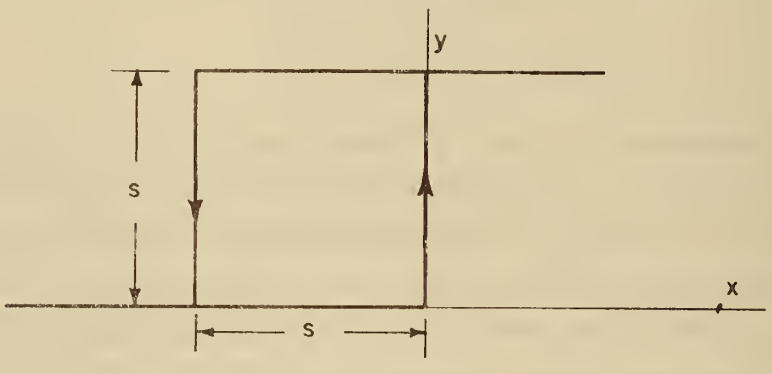


Figure 8. Steady-state transfer-function of a finite ring of elements, each having the transfer function of Figure 7

which represents the steady-state magnitude y of a circulating signal as a function of an externally generated signal x. The arrows on the vertical segments indicate that these are not reversible paths. The function exhibits the property of hysteresis. The degree of stability is measured by the magnitude of the smallest positive or negative excursion from x = 0 that will result in a change in the y-output. The degree of ZERO-stability is seen to be zero, while the degree of ONE-stability is equal to s, the full signal magnitude. The ring of elements just described exhibits the property of storage. A device is said to store if the application of a disturbance greater than a certain minimum value produces a persistent change in its state which is detectable as an output, while disturbances less than the minimum value produce no such change. This minimum value is called the threshold. The device may be thought of as storing a quantity equal and opposite to the threshold that must be overcome to change its state. The unstable infinite cascade has no threshold and stores nothing. The monostable ring has a single threshold, and stores a quantity equal to + s. In the presence of a noise level equal to or exceeding s, the monostable ring becomes unstable.

The linear saturating single-element transfer function of Fig. 7 is still not suitable for propagation of binary signals because it leads to cascades whose sensitivity to noise increases without limit as the number of elements is increased, and because, in the presence of an arbitrarily small noise-level, rings of elements having this transfer function are ONE-stable only.

The next step in the evolution of the single-element transfer function is the introduction of a bias a. The resulting transfer-function, shown in Fig. 9 is obtained by translating the curve in Fig. 7 to the right by an amount equal to a, keeping $a < (s - s/g)$, and $g > +1$. Then the new curve crosses the unity gain line at three points: At the origin O; at S, which has the coordinates $x = s$, $y = s$; and at R, a point that lies between O and S, and has the coordinates $x = r$, $y = r$. The gain, y/x, of this transfer function is not constant, but depends on x. It is less than unity for $x < r$ and for $x > s$; and it is greater than unity for $r < x < s$. The equation for the curve in Fig. 9 is

$$y = f(x) = \begin{cases} g\,(x-a); & a < x < (a + s/g) \\ s \quad ; & x > (a + s/g) \\ 0 \quad ; & x < a \;;\; g > +1 \end{cases} \qquad (2)$$

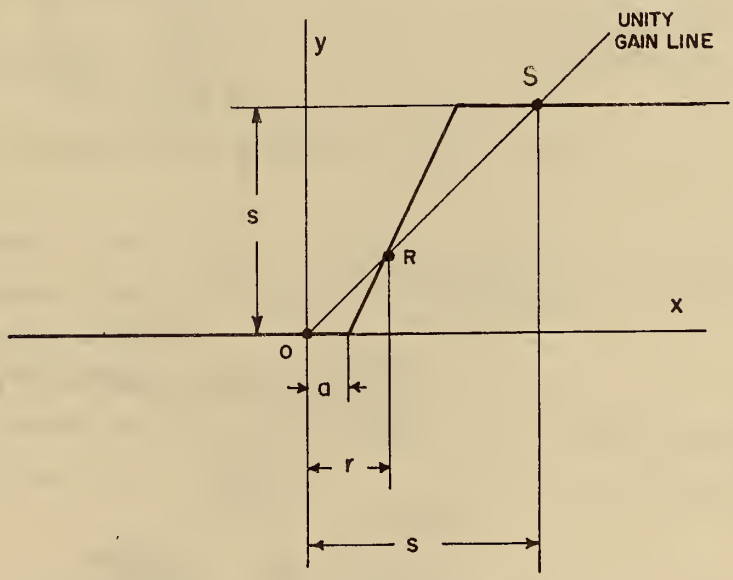


Figure 9. Biased, linear, saturating, element transfer-function

This is now the complete transfer function of a single element. To determine its suitability for binary signal transmission we must find $f^n(x)$ and examine its properties as $n \longrightarrow \infty$. In the range $x < a$, it is obvious from (2) that $f^n(x) = 0$ for all n; and, in the range $x > (a + s/g)$, $f^n(x) = s$ for all n. Then, making use of the example in equation (1), in the range $a < x < (a + s/g)$,

$$f^1(x) = g(x-a)$$

$$f^2(x) = f\left[f(x)\right] = g\left[g(x-a) - a\right]$$
$$= g^2x - a(g^2 + g)$$

$$f^3(x) = f\left\{f\left[f(x)\right]\right\}$$
$$= g\left\{g\left[g(x-a) - a\right] - a\right\}$$
$$= g^3x - a(g^3 + g^2 + g),$$

and in general

$$f^n(x) = g^nx - a(g^n + g^{n-1} + g^{n-2} + \ldots + g)$$
$$= g^nx - a\sum_{1}^{n} g^n$$
$$= g^nx - a\left[\frac{g(1-g^n)}{1-g}\right]$$
$$= g^n\left(x - \frac{ag(1-g^n)}{g^n(1-g)}\right)$$
$$= g^n(x - a_n) \; ; \; a_n < x < (a_n + s/g^n)$$

Then for any x, the transfer-function for n transmissions of the signal, or for n iterations of the single-element transfer function (2) is

$$f^n(x) = \begin{cases} g^n(x - a_n); & a_n < x < a_n + s/g^n \\ s \quad ; & x > a_n + s/g^n \\ 0 \quad ; & x < a_n \end{cases} \qquad ; \; g > +1 \tag{3}$$

where

$$a_n = \frac{ag(1-g^n)}{g^n(1-g)} \tag{4}$$

$f^n(x)$ for n = 1 and for n = 2, with g = 2, are illustrated by the lines $OP_1 Q_1 S$ and $OP_2 Q_2 S$ in Fig. 10. The slopes of these functions are equal to $2^1 = 2$ for $f^1(x) = f(x)$; and $2^2 = 4$ for $f^2(x)$. The intercepts or thresholds are, from (4)

$$a_1 = a\,\frac{2(1-2)}{2(1-2)} = a$$

$$a_2 = a\,\frac{2(1-4)}{4(1-2)} = \frac{3}{2}\,a$$

The line O, P_∞, Q_∞, S in Fig. 10 represents $f^\infty(x)$, the limiting case of $f^n(x)$, as g^n becomes very large or, what is the same thing, if g-1 is not infinitesimal, as n becomes large. For $g \geq 2$, $f^3(x)$ is practically speaking the equivalent of $f^\infty(x)$. The slope of $f^\infty(x)$ is $g^\infty = \infty$, and its x intercept a_∞ is given by

$$a_\infty = \lim_{n \to \infty} a_n = \lim_{n \to \infty} \frac{ag(1-g^n)}{g^n(1-g)} = \frac{ag}{g-1} \tag{5}$$

$f^\infty(x)$ can therefore be written as

$$f^{\infty}(x) = \lim_{n \to \infty} f^{n}(x) = \begin{cases} s \; ; & x > a_{\infty} \\ \\ 0 \; ; & x < a_{\infty} \end{cases} \tag{6}$$

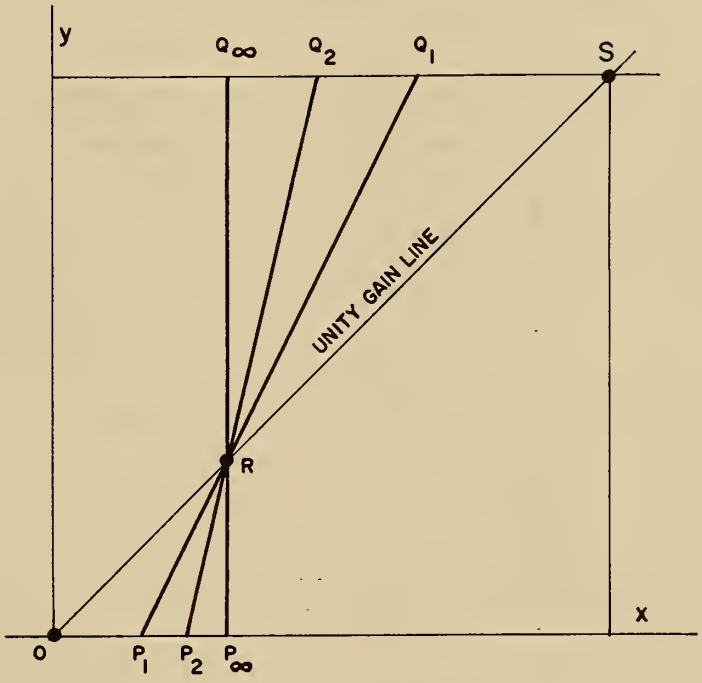


Figure 10. $f^{n}(x)$, as defined in equation (3), for n=1, 2 and ∞

Now the only point, outside the regions of cut-off and saturation, that is common to all the curves $f^{n}(x)$ is the point R where $y = f^{n}(x)$ crosses the unity gain line. At this point $y = x = r$. To find r, the abscissa of R, set

$$y = f^{n}(x) = x = g^{n}x - \frac{ag(1-g^{n})}{(1-g)}$$

$$x(1 - g^{n}) = \frac{-ag(1-g^{n})}{(1-g)}$$

$$x = \frac{-ag(1-g^{n})}{(1-g^{n})(1-g)} = \frac{ag}{g-1} = r \tag{7}$$

By comparing (7) with (5) it is seen that $r = a_{\infty}$. Therefore, given $y = f(x) = g(x-a)$, to find $y = f^{\infty}(x)$, a perpendicular to the x-axis is erected through the intersection point R of $y = f(x)$ with the unity gain line. This perpendicular is the infinite-slope portion of $y = f^{\infty}(x)$. The curves $y = f^{n}(x)$ all pass through R and lie between $y = f(x)$ and the perpendicular curve $y = f^{\infty}(x)$. Figure 11 shows how $f^{\infty}(x)$ is derived from f(x) graphically. It is seen that only the two quantities r, the abscissa of the second point of intersection of f(x) with the unity gain line; and s, the abscissa of

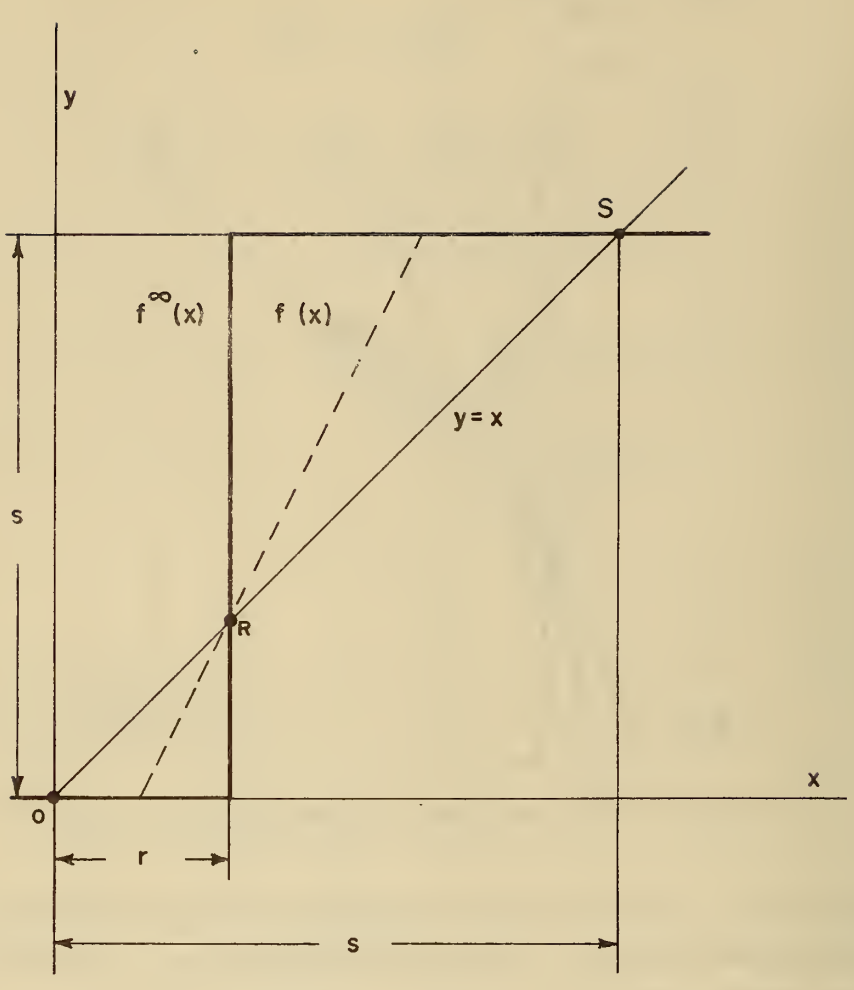


Figure 11. Graphical derivation of $f^{\infty}(x)$ from f(x)

the third point of intersection of f(x) with the unity gain line, are needed to determine $f^{\infty}(x)$. s is the full signal magnitude and r is the transmission threshold of $f^{\infty}(x)$.

$y = f^{n}(x)$ describes the progress of a signal introduced into an open cascade. It represents the magnitude of a disturbance, originally having the value x when introduced into the input element of the cascade, after it has traversed n elements. If the cascade is sufficiently long, the disturbance will ultimately have one of only two possible values, $y = s$, or $y = 0$. It is apparent that any disturbance smaller than r will remain smaller than r, and in fact will diminish to zero. Conversely, any disturbance greater than r will grow until it reaches the full magnitude s. The quantity x here represents total excitation, signal plus noise, at the input to the first element.

2.2 The Propagation Function

We now wish to distinguish between signal and noise, and in doing this we will consider the general case of an element embedded in a cascade or ring. In the definition of $f^{n}(x)$ on page 3 it was stated that $y = f^{n}(x)$ gives the magnitude after n transmissions, of a signal whose initial value was x. This is true provided x is generalized to represent the total input excitation both external (including noise) and internal to the cascade or ring. But if x is taken to represent only the externally induced signal or disturbance, the propagational transfer function must be altered to make up for the loss in generality in the definition of x.

We define a new transfer function called the propagational transfer function. It is

$$F^{n}(x) = f^{n}(x_{o} + x) \qquad n \geq 0$$

where, in particular,

$$F^{o}(x) = f^{o}(x_{o} + x) = x_{o} + x$$
$$F^{1}(x) = F(x) = f(x_{o} + x)$$

Here, x_{o} represents the existing excitation at the time and the place at which the external signal or disturbance is introduced. It is an initial condition, so to speak. In practice it will come from the output of the previous element in the sequence. Therefore x_{o} may be replaced by the quantity $f^{m}(\xi)$ where ξ represents the total excitation m disturbance-free transmissions (i.e., and which existed m elements ahead of the one at which disturbance x is introduced) before the introduction of the external excitation x, and we have

$$F^{n}(x) = f^{n}\left[f^{m}(\xi) + x\right] \qquad (8)$$

for the propagational transfer function for an externally induced signal x introduced into a cascade or ring at the time and place where the existing signal was $f^{m}(\xi)$.

Now ξ may have had any value between 0 and + s. (ξ may be imagined as the output of a disturbed element). Therefore, if m is small, (in a practical case 3 or less) $f^{m}(\xi)$ might also have any value between 0 and + s. However if m is not small, or more precisely, if g^{m} is large, the probability that $f^{m}(\xi)$ will have a value other than 0 or + s is so small that we can let

$$f^m(\xi) = \begin{cases} s \\ 0 \end{cases} ; \quad g^m \text{ large}$$

and

$$F^n(x) = \begin{cases} f^n(s + x) \\ f^n(0 + x) \end{cases} ; \quad g^m \text{ large} \qquad (9)$$

Fig. 12 b is a graph of the function $y = F^n(x)$ and Fig. 12 a shows $y = f^n(x)$ for comparison. $F^n(x)$ is seen to be double-valued over a certain range, and single-valued outside this range. There is the threshold a_n to positive disturbances, and an additional threshold - a'_n to negative disturbances.

$F^n(x)$ is completely specified when n and three of the four parameters a_n, a'_n, s, and g are known. This can be seen from Fig. 12 a which shows that

$$a_n + a'_n + s/g^n = s$$

or

$$a_n + a'_n = s\left(\frac{g^n - 1}{g^n}\right). \qquad (10)$$

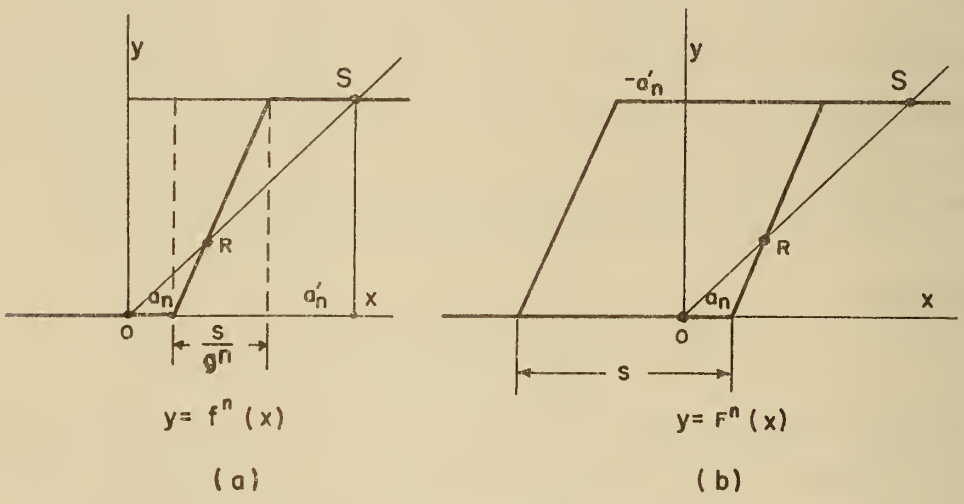


Figure 12. a. $f^n(x)$ for the biased saturating element

b. $F^n(x)$ derived from $f^n(x)$

As in the case of $f^n(x)$, a_n is given by

$$a_n = \frac{ag(g^n - 1)}{(g-1)\,g^n} \qquad (4)$$

Then, remembering that $\frac{ag}{g-1} = a_\infty = r$,

$$a_n = r\left(\frac{g^n - 1}{g^n}\right); \qquad (11)$$

and, from (10)

$$a'_n = s\left(\frac{g^n - 1}{g^n}\right) - a_n$$

$$= (s - r)\left(\frac{g^n - 1}{g^n}\right) \qquad (12)$$

n, and the three quantities s, r, and g completely determine $F^n(x)$.

Then as $n \longrightarrow \infty$, $\frac{g^n - 1}{g^n} \longrightarrow 1$ so that only the two quantities s and r are needed to determine the steady-state propagational transfer function which is given by

$$F^\infty(x) = \lim_{n \to \infty} F^n(x) = \begin{cases} f^\infty(s+x) = \begin{cases} s\ ;\ (s+x) > r \\ 0\ ;\ (s+x) < r \end{cases} \\ f^\infty(0+x) = \begin{cases} s\ ;\ x > r \\ 0\ ;\ x < r\ ;\ g^m \text{ large} \end{cases} \end{cases}$$

$$= \begin{cases} s\ ;\ x > -(s-r) \\ 0\ ;\ x < -(s-r) \\ s\ ;\ x > r \\ 0\ ;\ x < r \qquad ;\ g^m \text{ large} \end{cases} \qquad (13)$$

in which $r = a_\infty$, and $s - r = a'_\infty$.

This function is shown in Fig. 13 b with $f^\infty(x)$ shown in Fig. 13 a for comparison. It is seen to be single-valued for $x < -(s - r)$ and for $x > r$; and double valued [and depending on $f^m(\xi)$] for $-(s - r) < x < r$. The arrowheads show the only direction in which $y = F^\infty(x)$ may vary along the

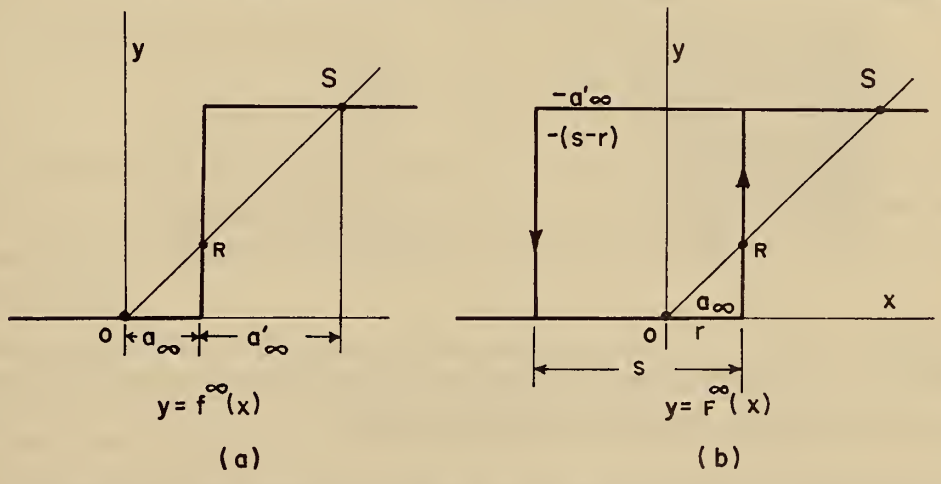


Figure 13. a. $f^\infty(x)$ for the biased saturating element showing one threshold.

b. $F^\infty(x)$ derived from $f^\infty(x)$, showing two thresholds

vertical segments. The horizontal segments of $F^{\infty}(x)$ may be traversed in either direction. The full signal magnitude is s, and there are two thresholds r and -(s-r) corresponding to the two stored quantities -r and (s-r). $F^{\infty}(x)$ shows that the propagation of signals in cascades and rings of elements having the transfer function (2) is bistable, and that in the steady-state only signals having zero magnitude, or signals having a magnitude s can exist. If we call the former full binary ZEROS, and the latter full binary ONES, it is seen that a positive disturbance must overcome the stored quantity -r in order to change the state of the signal from a full ZERO to a ONE. Weaker disturbances will have no permanent effect upon the signal. Similarly, a negative disturbance must overcome the stored quantity (s-r) to change the state of the signal from a full ONE to a ZERO. In other words, in the case of an alternating disturbance, the noise-to-signal ratio must not exceed r/s or 1 - r/s, whichever is smaller. These quantities are both at a maximum, of course, when $r = \frac{1}{2}$ s. In this case the signal survives noise-to-signal ratios up to the very large value of 0.5.

Such a large value can be tolerated, however, only when g^m is large, which is assumed in the definition of $F^{\infty}(x)$ in equation (13). Physically speaking, this means that the time t_δ between disturbances to a given signal must include enough transmissions to keep g^m large. Thus if g = 2, then disturbance-free intervals for which $m \geq 3$ would be sufficient; but if g = 1.3, the intervals must allow $m \geq 8$. The probability that $f^m(\xi)$, defined as in (3), will have values different from 0 or s when ξ is equally likely to have any value from 0 to s diminishes as $1/g^m$. Fig. 14 a indicates the distribution of the functions $y = f^{\infty}\left[f^m(\xi) + x\right]$ when g^m is small, and Fig. 14 b

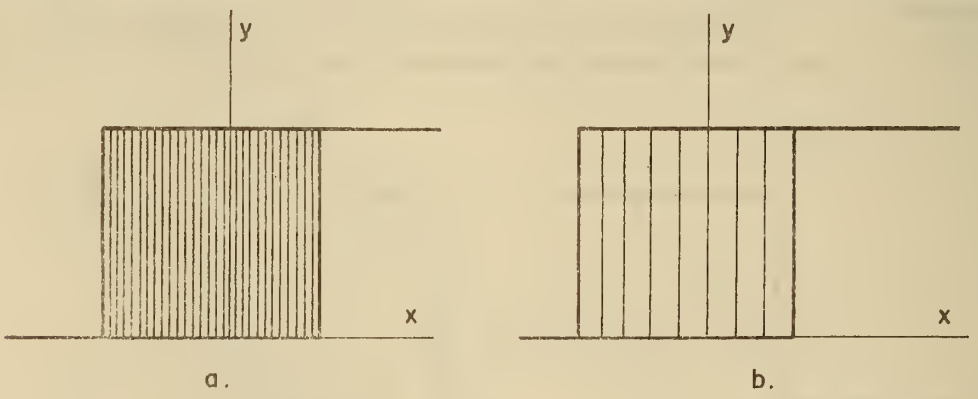


Figure 14. a. Probability density of imperfect propagation functions when g^m is small
b. Density when g^m is appreciably larger

indicates the distribution when g^m is appreciably larger. The outer limiting function is, of course, $F^{\infty}(x)$ as given in (13). As $g^m \longrightarrow \infty$ the probability of the existence of a propagation function, other than $F^{\infty}(x)$, approaches zero. Any vertical segment in Fig. 14 may be chosen to represent a possible function $f^{\infty}\left[f^m(\xi) + x\right]$. Since functions other than $F^{\infty}(x)$ are

undesirable, g^m is a kind of propagation figure of merit. The chance of survival of a signal in the presence of disturbances is improved when g^m is increased.*

2.3 The Signal Gain g, and Amplifier Bandwidth

Now g, speaking generally, is the slope of the single-element transfer-function f(x) in the neighborhood of R; and the number of transmissions ot a signal by an element (or elements) required to convert a given partial ZERO, or a given partial ONE into a full ZERO or a full ONE decreases as g is made larger. g is thus a measure of the growth of a binary signal upon passage through one element, and will therefore be called the signal gain of the element. (It is to be distinguished from the signal-parameter gain y/x; and it is not the power gain). Now m, the number of transmissions between disturbances, is proportional to the time rate at which transmissions occur, and this is proportional to the reciprocal-delay-per-element or Δf, the bandwidth of the element. In this way g^m leads to $g^{\Delta f}$, a figure of merit, which is a measure of the element reaction speed. In the case of elements for which the gain-bandwidth-product $g\Delta f = P$ has a fixed value, $g^{\Delta f}$ can be written as $g^{P/g} = (\sqrt[g]{g})^P$ where g is always greater than unity. The function $\sqrt[g]{g}$ approaches unity for $g \rightarrow 1$ and for $g \rightarrow \infty$; and it has its maximum value at $g = e$ for which $\sqrt[g]{g} = \sqrt[e]{e} \simeq 1.44$. It is seen that $\sqrt[g]{g}$ for $g \geq 1$ is only slightly dependent upon g. However, for constant P, $(\sqrt[g]{g})^P = g^{\Delta f}$ may be strongly dependent upon g if P is large. The same can be said for $(\sqrt[g]{g})^{Pt_\delta} = g^{t_\delta \Delta f} = g^m$ where t_δ is the time interval between disturbances to the signal: Large values of Pt_δ make g^m strongly dependent upon g, when P is held constant. In the particular case where g has been optimized, $g = e$. Then

$$g^{\Delta f} = (\sqrt[e]{e})^P \simeq (1.44)^P \qquad (14)$$

and

$$g^{t_\delta \Delta f} = g^m \simeq (1.44)^{Pt_\delta} \qquad (15)$$

At optimized signal gain, the element reaction speed $g^{\Delta f}$ is 1.44 raised to a power equal to its gain-bandwidth product P. The propagation figure of merit g^m is equal to the element reaction speed raised to a power equal to the time t_δ between disturbances to the signal.

2.4 The Element-Group

It has been shown that the steady-state propagational transfer function, $F^\infty(x)$, for a signal travelling in a long cascade or in a ring made up of identical unilateral elements, having the individual element transfer-function f(x) defined in (2), can be represented by a square graph which

* In reference (1) Kochen considers the case in which several or all the transducers in a ring are subject to a noise-level large enough that there is a finite probability that a signal will be destroyed in them. He proves that all signals will ultimately disappear, and calculates the rate of loss.

is completely determined by two quantities: By s, the full signal magnitude, which is the abscissa of S, the point of third intersection of f(x) with the unity gain line; and by r, the abscissa of R, the point of second intersection of f(x) with the unity-gain line. If, however, the elements are not all alike, the propagation function is more complex. In any practical case the different elements will occur in some regularly repeating order such that, if there are i different kinds of elements, the (N + i)th element is like the Nth element. See Fig. 15 a, which shows a ring of six elements of

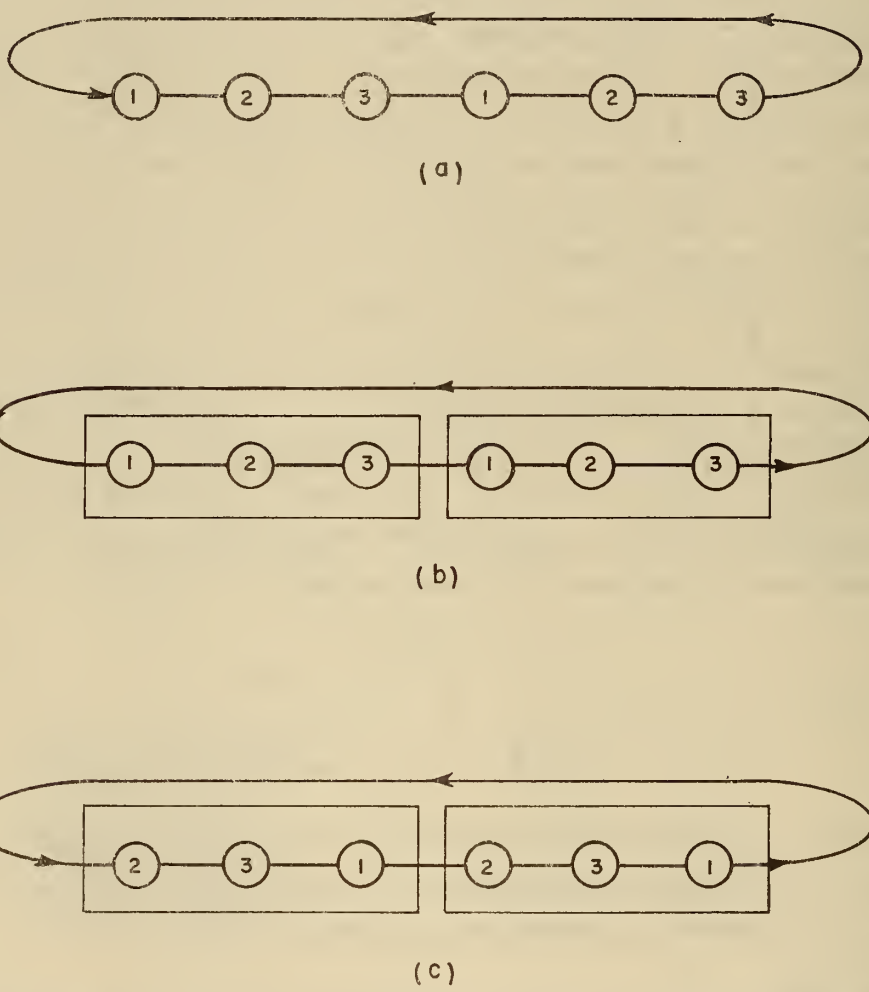


Figure 15. a. A ring of six computer elements of three different kinds

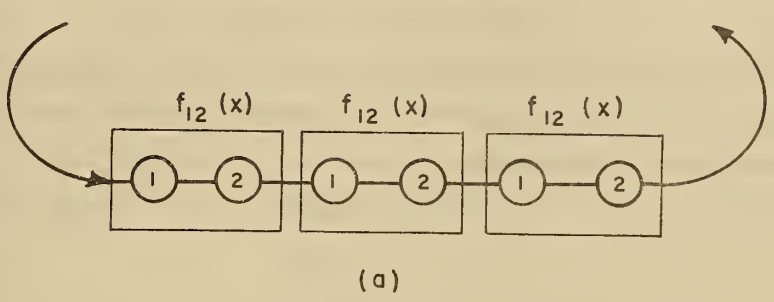
b. One possible grouping of the elements in the ring

c. Another possible grouping

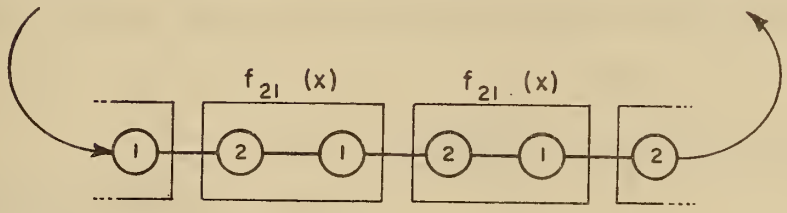
three different kinds. Such a ring can be divided into an integral number of identical element-groups, as is shown in Fig. 15 b and in Fig. 15 c. Then if the transfer-function of the element-group is known, a propagation function graph similar to that of Fig. 13 b can be drawn. But this is not

sufficient because there are i different ways to form element-groups such that the groups contain the individual elements in different order. For example, compare Fig. 15 b with Fig. 15 c. The overall transfer function of a group depends upon the ordering of its component elements because the operations indicated by $f_3 \left\{ f_2 \left[f_1(x) \right] \right\}$ are not, in general, commutative.*

The simplest case of a ring made up of only two types of elements serves to illustrate the nature of the solution. Fig. 16 shows the groups formed from a six-element ring containing type 1 and



(a)



(b)

Figure 16. a. One of two possible element-groups and group-transfer-functions formable from a ring having two kinds of elements

b. The other possible element-group and group-transfer-function

type 2 elements. In Fig. 16 a the group transfer-function is

$$f_2 \left[f_1(x) \right] = f_{12}(x),$$

and in Fig. 16 b, it is

$$f_1 \left[f_2(x) \right] = f_{21}(x)$$

Assume $f_1(x)$ and $f_2(x)$ to have the form $f(x)$ defined in equation (2), and that, outside the regions of saturation and cutoff,

* The operations indicated by $f_1 \left[f_2(x) \right]$ are commutative, for example, when either one or both equal Cx where C is a constant.

$$f_1(x) = g(x-a)$$

$$f_2(x) = h(x-b)$$

Then

$$f_{12}(x) = h\left[g(x-a) - b\right] \qquad (16)$$
$$= gh\left[x - (a+b/g)\right] \text{ , and}$$

similarly,

$$f_{21}(x) = gh\left[x - (b+a/h)\right] \qquad (17)$$

It is seen that the slope gh is the same in each case, but that the x-intercepts are different. The intercept of f_{12} is a + b/g. The intercept of f_{21} is b + a/h. Therefore, in the total propagation function there will be two values for r, namely

$$r_{12} = (a + b/g)\ \frac{gh}{gh-1} \qquad (18)$$

$$r_{21} = (b + a/h)\ \frac{gh}{gh-1} \qquad (19)$$

which correspond to the two kinds of element-groups which may be formed from the elements present. There will also be, in general, two possible full-signal magnitudes s_{12} and s_{21}. As a result, the complete propagational transfer function, which is designated by $\phi^{\infty}(x)$, is made up of two propagation functions $F_{12}^{\infty}(x)$ and $F_{21}^{\infty}(x)$, and requires a double graph. See Fig. 17. In general,

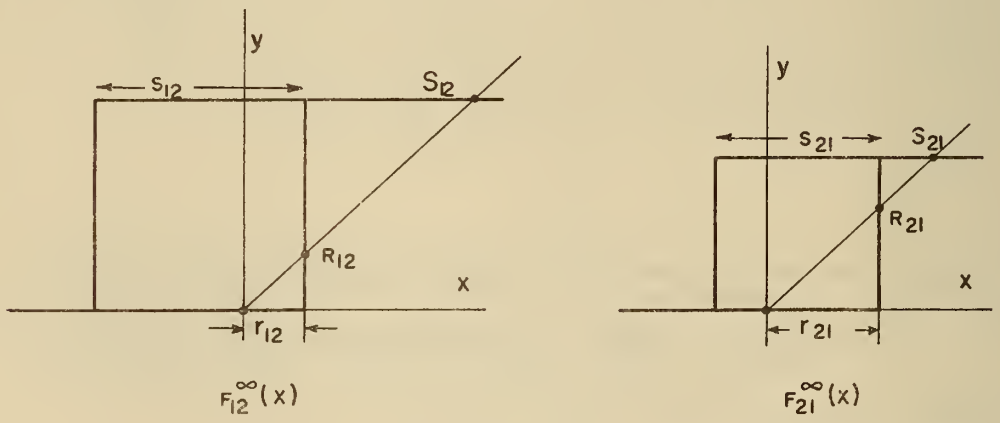


Figure 17. The complete, steady-state propagation functions $\phi^{\infty}(x)$ for an alternating sequence composed of two kinds of computer elements

if there are i different kinds of elements in a sequence, the complete propagation function $\phi^{\infty}(x)$ will include i different functions $F^{\infty}(x)$, one for each kind of element-group which can be formed in the sequence. The graph of $\phi^{\infty}(x)$ is then composed of i separate graphs, one for each $F^{\infty}(x)$.

$\phi^{\infty}(x)$ as graphed in Fig. 17 shows that the full signal amplitude at 2, 1 junctions is greater than at 1, 2 junctions. The threshold to positive disturbances is smaller at 2,1 junctions than at 1, 2

junctions, but the threshold to negative disturbances is greater at 2,1 junctions than at 1, 2 junctions. If the same magnitudes of positive and negative disturbances can be expected at both junctions, the smallest thresholds in $\phi^{\infty}(x)$ then indicate the margins of stability of the signal. As shown in Fig. 17 these would be $+r_{12}$ and $-(s_{21} - r_{21})$.

2.5 The General Element-Group Transfer-Function

In the last section it was shown that stable binary signal propagation results if the element transfer function or the element-group transfer function f(x) has the form (2) represented by the graph of Fig. 9. It was also shown that, as far as the steady-state propagation function $F^{\infty}(x)$ is concerned, the essential features of f(x) are simply the three points O, R and S at which its graph crosses the unity-gain line. This suggests that a function f(x) which is more general than (2) might generate the same $F^{\infty}(x)$ and therefore be sufficient for stable binary signal propagation. Such a function is illustrated in Fig. 18 and is defined only by the following restrictions:

$$\begin{aligned} y/x &< 1 \quad \text{for } x < r \text{ and } x > s \\ y/x &> 1 \quad \text{for } r < x < s \\ y/x &= 1 \quad \text{for } x = r \text{ and for } x = s \\ y &< s \quad \text{for } x < s \end{aligned} \tag{20}$$

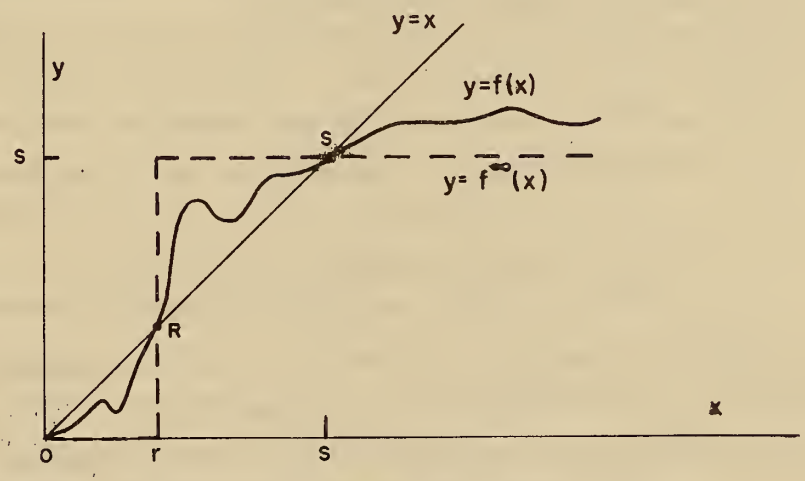


Figure 18. A generalized element-group transfer function

It can, in fact, be proved that $f^{n}(x)$, the nth iteration of f(x) as just defined, will converge to $f^{\infty}(x)$ as shown by the dotted line in Fig. 18 and will therefore result in the same $F^{\infty}(x)$ as was derived from the more restricted form. It is only necessary to carry out the proof for the portion between O and R since the proof for the other regions is similar.

For the region $0 < x < r$, in which $y/x < 1$ by definition, it is only necessary to show that the curve $y = f^{n}(x)$ approaches the x-axis; or, in other words, that $\lim_{n \to \infty} f^{n}(x) = 0$; $0 < x < r$.

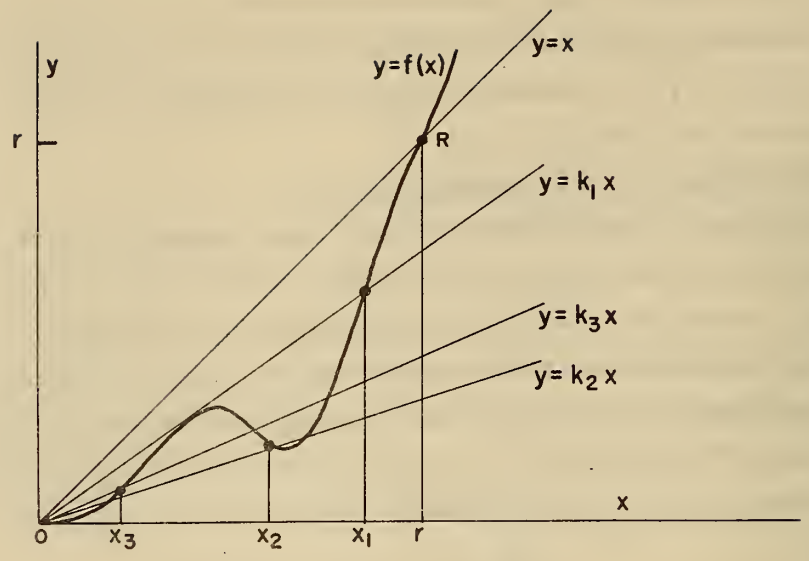


Figure 19. Proof that the generalized transfer function converges to a step function

Fig. 19 which represents the portion of f(x) between O and R, shows that, for a given value of x, say x_1, $f(x_1)$ may be replaced by its equivalent $k_1 x_1$, where $k_1 = y_1/x_1$ on the curve $y = f(x)$. $f^n(x_1)$ may then be deduced as follows: (See also Fig. 19.)

$$f(x_1) = f^1(x_1) = k_1 x_1 = x_2$$

$$f^2(x_1) = f(x_2) = f(k_1 x_1) = k_2 \cdot k_1 x_1 = x_3$$

$$f^3(x_1) = f(x_3) = f(k_2 \cdot k_1 x_1) = k_3 \cdot k_2 \cdot k_1 x_1 = x_4$$

$$\cdots \qquad \cdots \qquad \cdots$$

$$f^n(x_1) = f(x_n) = f\left[\prod_{1}^{n-1} k_i \, x_1\right] \cdots = \left[\prod_{1}^{n} k_i\right] x_1$$

Now if x_1 is confined to the range $0 < x_1 < r$, then $k_1 < 1$ with the result that $x_2 < x_1$. Then, since $x_2 < x_1 < r$, $k_2 < 1$, making $x_3 < x_2$. And again, since $x_3 < x_2 < x_1 < r$, $k_3 < 1$, . . . , and so on. This sequence shows that the values k_i remain less than unity. But for $0 \leq k_i < 1$

$$\lim_{n \to \infty} \prod_{1}^{n} k_i = 0$$

Therefore,

$$\lim_{n \to \infty} f^n(x_1) = \lim_{n \to \infty} \left[\prod_{1}^{n} k_i\right] x_1 = 0$$

and hence

$$f^{\infty}(x) = \lim_{n \to \infty} f^n(x) = 0 < x < r$$

In similar fashion it can be shown that $f^{\infty}(x)$ coincides with the line $y = s$ for $x > r$.

2.6 The Propagation-Function of the Flip-Flop

We have seen that binary signals are propagated in stable fashion in sequences of elements which may be subdivided into element-groups having transfer-functions each of which crosses the unity-gain line at the three points O, R and S.* The functions $f^{n}(x)$ and $F^{n}(x)$, which describe the transient behavior of a signal, apply only to sequences in which an element-group receives and transmits the signal sequentially, during discrete time intervals. Also, a somewhat detailed knowledge of the shape of the graph of f(x) is needed to predict $f^{n}(x)$ and $F^{n}(x)$. But $f^{\infty}(x)$, $F^{\infty}(x)$ and $\phi^{\infty}(x)$, which describe the steady state of the signal, are determined only by the values of r and s for the possible element-groups in the sequence.

Even when the element-groups do not receive and transmit in separate time intervals, it is possible to describe the steady state of a solitary signal by means of $\phi^{\infty}(x)$. This is illustrated for the case of the vacuum tube flip-flop in Fig. 20a. The flip-flop can be thought of as a ring composed of two elements, each being a vacuum tube with its associated circuit. The signal-carrying parameter x is the difference between the plate (or the grid) potential and the lowest plate (or grid) potential V_o. This difference is called the signal voltage. If the elements have transfer functions with negative slopes; or if their transfer functions are different, they must then be combined into element-groups. Fig. 20 b shows the flip-flop regarded as a ring composed of a single element-group having element 1 as its input, and element 2 as its output. Fig. 20 c shows the same flip-flop considered as a ring composed of a single element-group in which the element order is reversed. Two values of r and s, one for each element-group, are required to determine $\phi^{\infty}(x)$. The steady-state signal at the 2, 1 junction is described by $F^{\infty}_{12}(x)$ derived from the 1, 2 element-group of Fig. 20 b. The steady-state signal at the 1, 2 junction is given by $F^{\infty}_{21}(x)$ derived from the element-group 2, 1 of Fig. 20 c. As these groups are shown, it is seen that the parameter x corresponds to plate signal-voltage. The grids could as well have been chosen for the element junctions with x representing grid signal-voltage, and with only a scale factor difference in $\phi^{\infty}(x)$.

Figure 21 shows the output voltage (plate voltage of the first tube) of element 1 plotted on the outer vertical axis, versus its input voltage (plate voltage of the second tube) plotted on the lower horizontal axis. The portion of this curve which is included within the inner coordinate axes, having their origin at the point V_{02}, V_{01}, is $f_1(x)$ in terms of these axes. V_{02} is the lower limit of excursion of the second plate. The outer axes measure voltage above ground; the inner axes

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* It should be pointed out that the element-transfer functions need not, in themselves, satisfy these stability requirements. It is sufficient that the transfer-functions of all possible groups satisfy them.

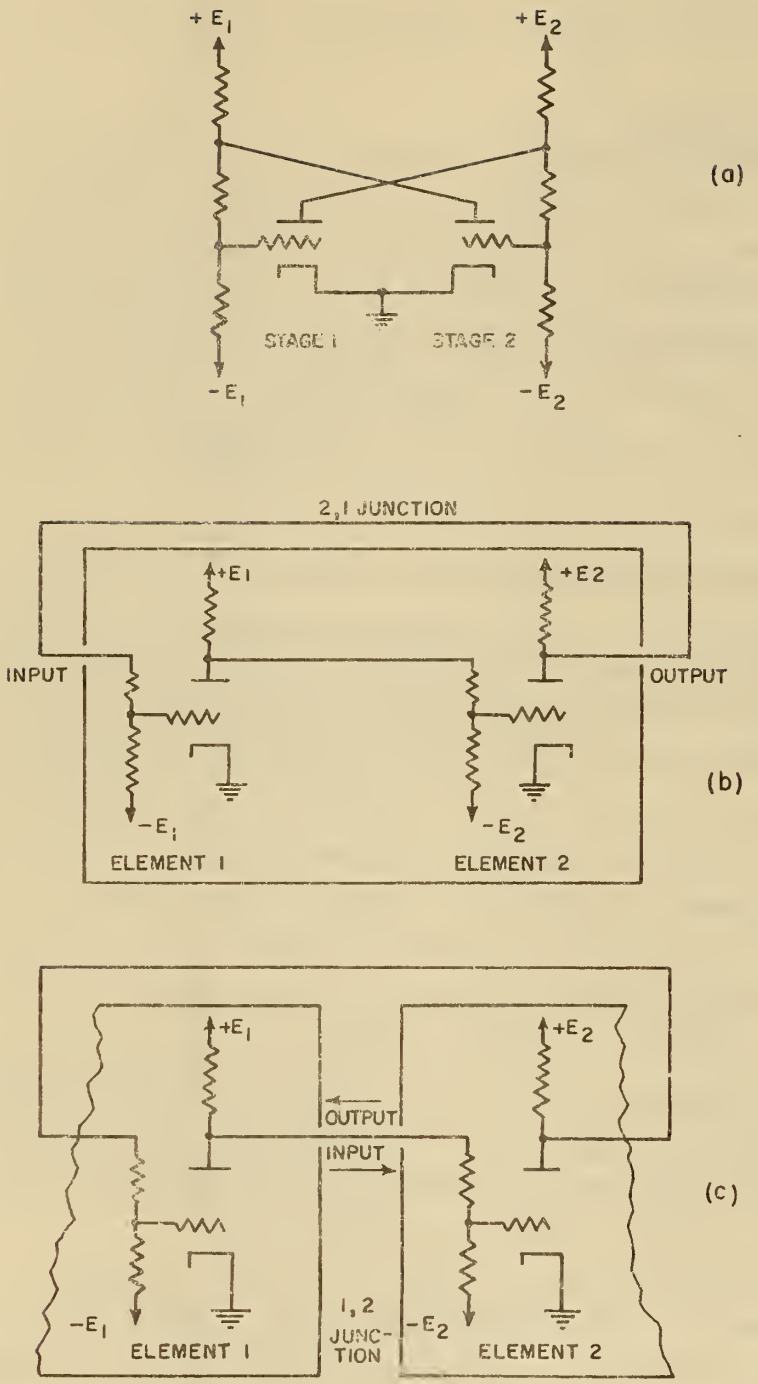

Figure 20. a. The vacuum tube flip-flop

b. The flip-flop regarded as a ring composed of a single 1-2 element-group

c. The flip-flop regarded as a ring of one 2-1 element-group

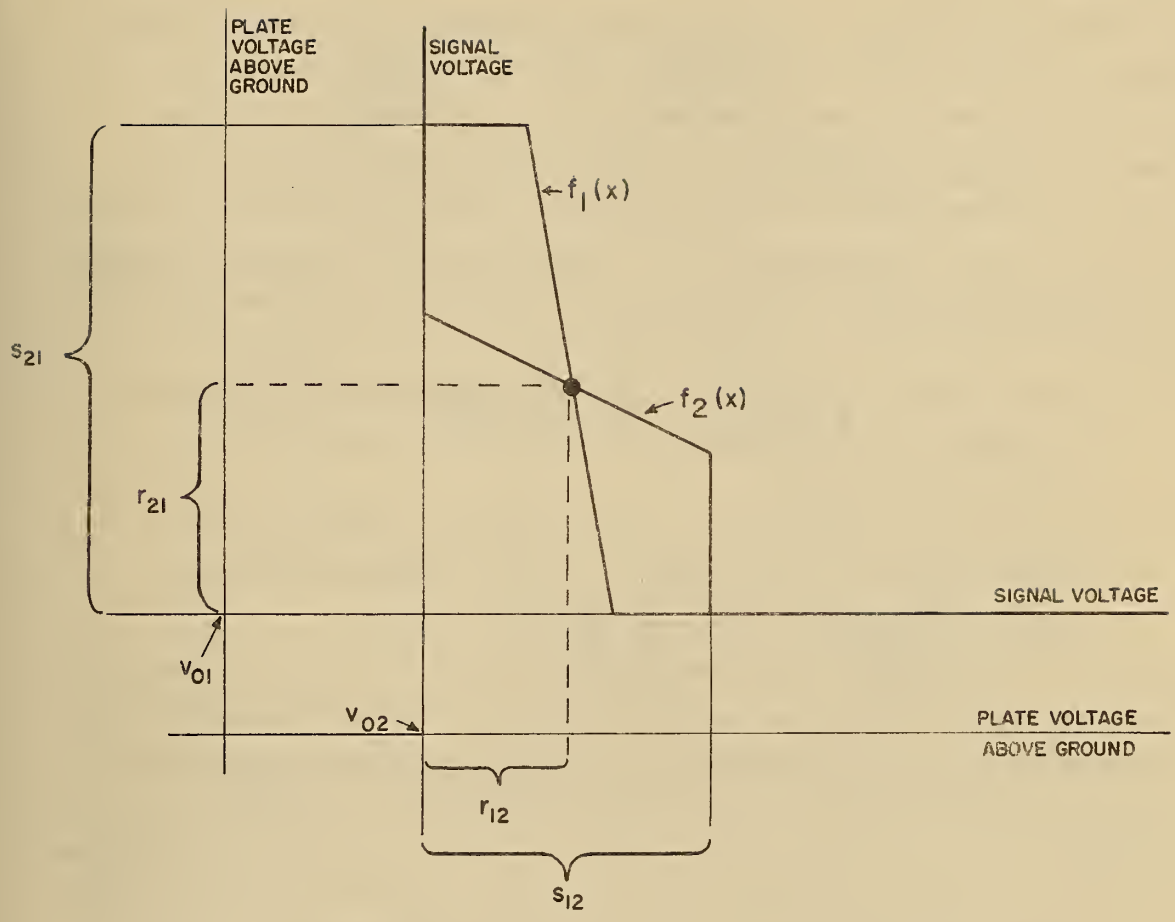

Figure 21. Graphical determination of r_{12}, s_{12}, r_{21}, and s_{21} for the flip-flop

represent signal-voltage, as already defined. Superimposed on this is a graph of the output of the second element, plotted on the horizontal axes, versus its input, plotted on the vertical axes. V_{0i} is the lower limit of excursion of the first plate. Using these superimposed graphs, the functions $f_{12}(x) = f_2\left[f_1(x)\right]$ and $f_{21}(x) = f_1\left[f_2(x)\right]$ can be constructed. They resemble f(x) shown in Fig. 9. But the values of r_{12}, s_{12}, r_{21}, s_{21} are easily found immediately, as indicated in Fig. 21, and from these the functions $F_{12}^{\infty}(x)$ and $F_{21}^{\infty}(x)$ can be graphed, as was shown in Fig. 17. s_{12} gives the voltage amplitude of a full binary ONE at the plate of the second tube. In the case of a full binary ZERO this plate remains at the potential V_{02}. r_{12} is the ZERO-stability margin at the 2, 1 junction, and $s_{12} - r_{12}$ is the ONE-stability margin. At this junction the noise-to-signal ratio must be kept less than $\frac{r_{12}}{s_{12}}$ or $1 - \frac{r_{12}}{s_{12}}$, whichever is smaller. Similarly, at the 1, 2 junction, the noise-to-signal ratio must be less than the smaller of the two quantities $\frac{r_{21}}{s_{21}}$ or $1 - \frac{r_{21}}{s_{21}}$.

3. SIGNIFICANT TIME INTERVALS IN THE DIGITAL AMPLIFIER OPERATION CYCLE

In the case of the flip-flop, $\phi^{\infty}(x) = \lim_{n \to \infty} \phi^{n}(x)$ is found to predict the steady-state correctly; but, even though $f_{12}(x)$ and $f_{21}(x)$ are known in detail, $\phi^{n}(x)$ does not give the flip-flop transient response because the successive transmissions of a disturbance through the element-group in the loop provided by the positive feedback connection are not separate and distinct events whose cumulative effect can be deduced by a simple iteration of the element-group transfer function.

The element-groups employed in digital computing devices differ markedly from the kind used in the flip-flop in one very important respect: The computer element-groups receive and transmit the signal sequentially during separate and distinct time intervals. As a direct result of this fact it follows that:

1. No fewer than two element-groups at a time, in a single sequence, can accomplish the propagation of a single binary signal. (One group must receive while the preceding group transmits.)
2. No more than two element-groups in a single sequence are involved at one time in signal propagation. (The group that is receiving a signal cannot begin transmitting it to the next one until the receiving interval is finished.)

As a result, the binary signals in a single sequence of element-groups have definite spatial and temporal identity. Their extension and duration, and their location in time and space are always well defined. The state of one element-group in a single sequence is a function of not more than one signal at a time. Furthermore, in dynamic circuits the signal moves at a constant rate determined by the delay time of the element-groups in the sequence. The element-group delay time t_d is defined to be the interval between the moment of arrival of a signal at the element-group input and the beginning of the transmission of that signal by that group to the next group. See Fig. 22.

The number of signals per second transmitted (or received) by an element-group is called the bit-rate. The bit rate is the reciprocal of the element-group cycle-time T. The latter is defined as the time required for the element-group to go through all the states involved in the passage of a signal and to return to its initial state. At its maximum, the element-group cycle time includes a receive interval, followed by a store interval, followed by a transmit-interval, followed by a recover interval. See Fig. 22. By definition, the receive-, transmit-, or transmit-recover intervals are equal in dynamic circuits; the other intervals may have different lengths relative to these. In dynamic circuits these intervals have constant predetermined lengths; but in static asynchronous systems there is no fixed cycle-time. The store and transmit intervals are not fixed, and are usually much longer than the receive interval. There is no recover interval in static systems. In this paper we are principally concerned with dynamic systems.

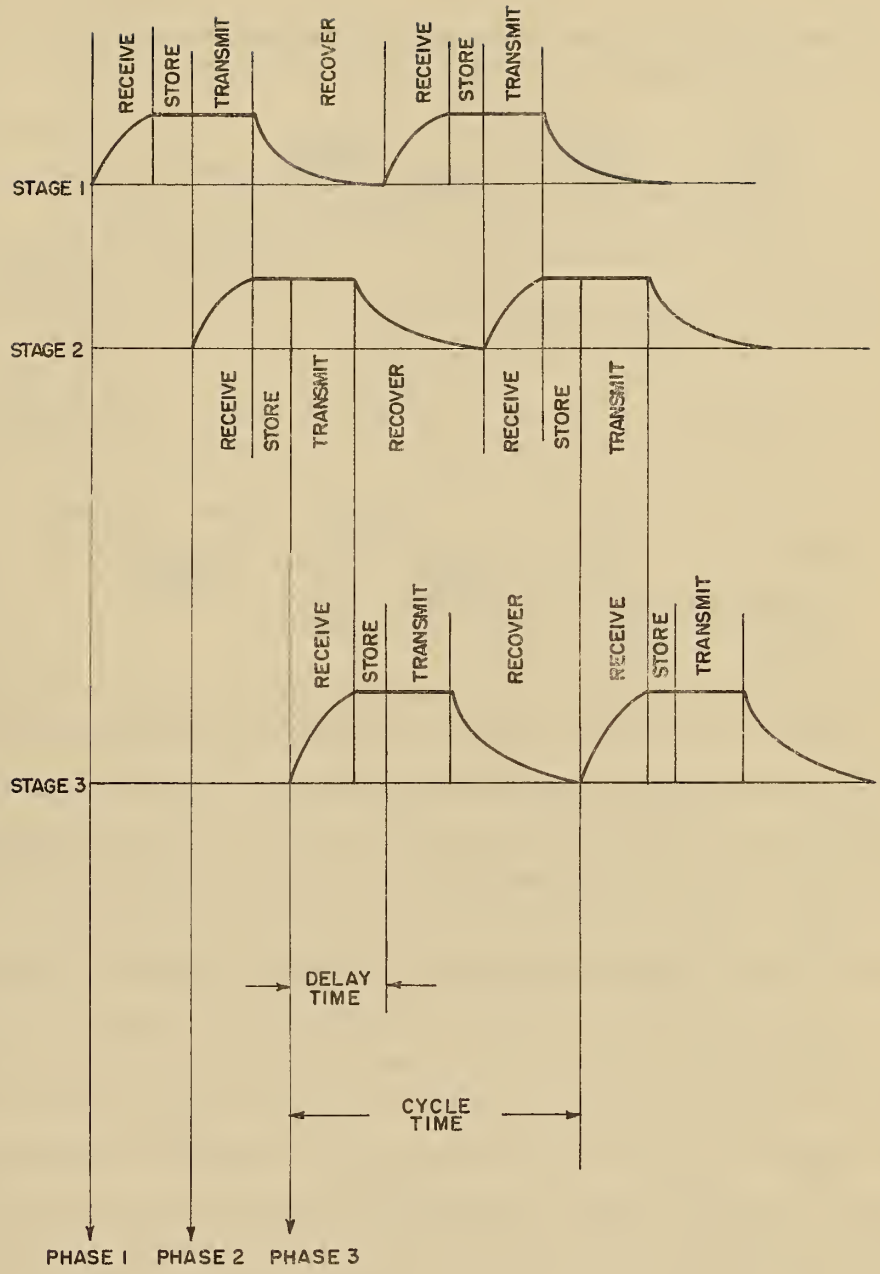

Figure 22. Significant time intervals in the digital amplifier operation cycle

Synchronous circuits differ in respect to what is done with the store-, and recover intervals. The minimum cycle time results when the store-interval is eliminated, and the recover operation is eliminated or is combined with the transmit operation. This is called a two-phase system. A two-phase system of the second kind is shown in Fig. 23.

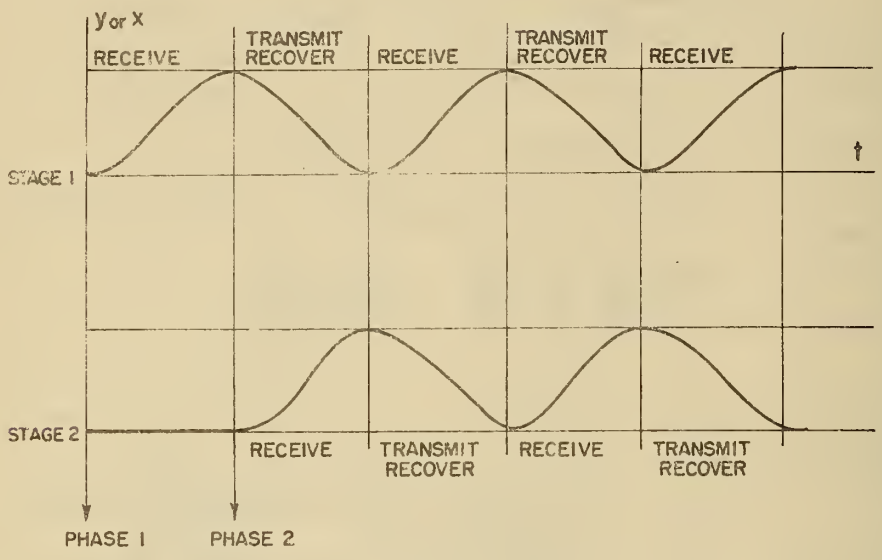

Figure 23. The dynamic operation-cycle that gives the maximum bit-rate

Now while the number of signals transmitted per second by an element group (the bit rate) is inversely proportional to the element-group cycle time, the number of element-groups traversed per second by a signal is the reciprocal of the element-group delay time, which is the interval between the beginning of the receive-interval and the beginning of the transmit interval. Therefore, if the delay time is short compared with the cycle time, a signal introduced into a sequence will traverse many element-groups before the first one in the sequence has completed its cycle and is ready to accept the next signal. The number of element-groups traversed equals the number of phases in the multi-phase system that results. Fig. 22 shows a three-phase system. It is seen that the number of phases can be increased by minimizing the store-interval and by maximizing the recover-interval. The latter, however, is undesirable because it lowers the bit-rate. Fig. 24 shows the result of eliminating the store-interval. The number of phases then equals the ratio of the cycle-time to the receive-interval, or element-group rise time.

If it is assumed that logical operations can be performed on the signal at each transmission through an element-group, then, for a given bit-rate, the number of operations per second is proportional to the number of phases. The elimination of the store-interval would therefore seem completely desirable. But with a certain kind of computer element the store-interval serves a useful purpose. This element, exemplified by the flip-flop, is called a regenerative element.

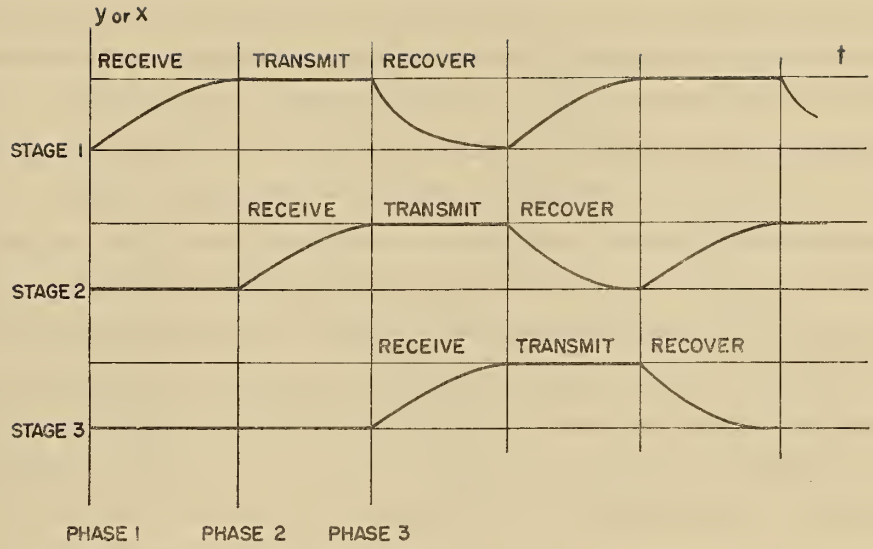

Figure 24. The minimum cycle-time achievable by elimination of the store interval results in a three-phase system

It has been pointed out that the element-group from which the flip-flop is formed is unsuitable, in itself, for use in computer networks because it is incapable of divorcing the transmit-interval from the receive-interval. In order to accomplish this separation, an element-group must be capable of storing the quantity measured by the signal parameter x. The addition of the positive-feedback connection to the flip-flop element-group, to form the single element called the flip-flop, results in a device that will regenerate and store a binary ZERO as a full binary ZERO, and a binary ONE as a full binary ONE. To obtain the full benefit of regeneration the state of the flip-flop must not be sensed-, that is to say, its state must not be transmitted, to the following element, until it (the first element) has had time to approach the steady state. The figure of merit $g^{\Delta f\, t_d}$ gives an indication of the degree of signal regeneration obtained if Δf is the bandwidth of the element-group from which the flip-flop was formed, t_d is the receive interval plus the store-interval, and g is the slope of the voltage transfer-function (small-signal gain) of the element group where it crosses the unity-gain line. The probability that the flip-flop will transmit other than a full ZERO or a full ONE is proportional to $g^{-\Delta f\, t_d}$. The store interval is therefore seen to be useful in minimizing the occurrence of marginal binary signals. If $g^{\Delta f\, t_d}$ is very large, the flip-flop becomes a computer element having the ideal signal-parameter transfer-function shown in Fig. 13 b.

$g^{\Delta f\, t_d}$ can also be expressed as g^{t_d/t_r}, where $t_r = 1/\Delta f$ is the rise-time, or delay-time around the flip-flop internal loop. This shows that the store interval should be made as large as possible relative to t_r. Now t_r may be taken as the practical lower limit on the receive interval of the flip-flop used as a computer element. Therefore, for the most nearly ideal response from the

flip-flop element, the receive-interval should be made equal to t_r, and the ratio of the store-interval to the receive-interval should be kept as large as possible, consistent with the requirement that the element delay-time (receive-, plus store interval) be no greater than one-half the element cycle-time. Otherwise, the ratio of cycle-time to delay-time, which equals the number of phases, assumes non-integral values. Therefore the sum of the largest value of the store interval and the receive-interval must equal the sum of the transmit-interval and the recover-interval. But the transmit-, and receive-intervals are equal (by definition); therefore the store-, and recover intervals must also be equal if the store-interval is to have its maximum value. In other words, at its maximum, the store-interval equals the recover-interval. This results in a two-phase system. Furthermore, if the bit-rate is to be maximized, the practical minimum value for the recover-interval is equal to that of the rise-time, or receive-interval for the element. The result is a two-phase system in which the receive-, store-, transmit-, and recover intervals are each equal to the element rise-time t_r. See Fig. 25.

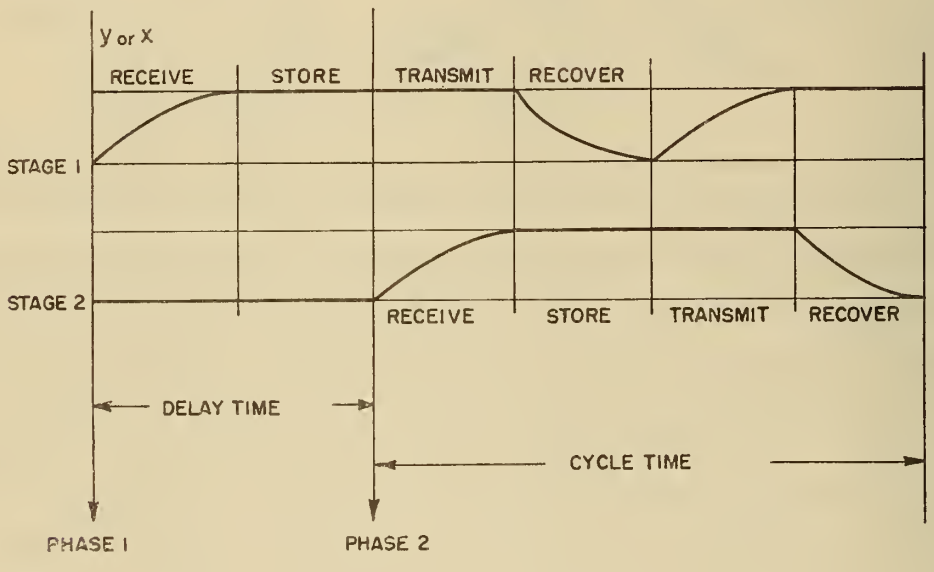

Figure 25. The dynamic operation-cycle that maximizes the store-interval and the bit rate

In this system, the figure of merit $g^{\Delta f t_d} = g^{t_d/t_r}$ equals g^2, remembering that t_d is the sum of the receive-interval and the store-interval. The smallest value for g^{t_d/t_r} is g, which results when the store-interval is eliminated. If this is done at maximum-bit-rate, a three phase system results. See Fig. 24. Then, as has been mentioned earlier, if the recover-operation is eliminated,[2] or is combined with the transmit-operation, a two-phase system having the shortest possible cycle-time, and hence the maximum possible bit-rate. See Fig. 23. The figure of merit for this system is also equal to g. Such a system can be realized with flip-flops using a synchronous static scheme.[2]

Although the elimination of the store-interval reduces the figure of merit of the flip-flop to that of the simple "non-feedback" computer element, the need for positive feedback remains. For it provides the flip-flop element with the property of storage which it needs in order to separate the transmit-interval from the receive-interval. The signal, which accumulates during the receive-interval, remains throughout the transmit-interval, and is removed during the recover-interval.

4. DERIVATION OF THE MAGNETIC DIGITAL AMPLIFIER TRANSFER-FUNCTION

The property of storage is essential to the computer element-group. In the case of the flip-flop, the signal-carrying parameter is a voltage, and voltage amplitude is the relevant quantity stored and transmitted. (Physically speaking, the charge on the stray capacitance to ground from the grids and plates is the stored quantity.) We now wish to describe a computer system in which the elements transmit and store, as signal parameter, a quantity equal to, or proportional to the time integral of voltage. The principal component in this system, a magnetic amplifier, in itself provides:

1. The essential property of storage, without positive feedback,
2. The essential power gain, and
3. The desirable feature that the operations of transmit and recover are accomplished simultaneously.

But the magnetic amplifier alone is not sufficient as a computer element principally because its volt-second transfer characteristic does not fulfill the requirement for stable propagation of binary signals: It does not cross the unity gain line in all three essential points O, R, and S. To overcome this deficiency other components have been associated with the magnetic amplifier forming a circuit whose element-groups have the desired transfer-function properties. The result is a two-phase system of maximum bit-rate, such as is shown in Fig. 23. The analysis of this circuit (called Transmag) is the principal subject of this paper.

The magnetic amplifier used consisted of a ring-shaped core of high-permeability, highly retentive magnetic material (4 - 79 Mo. Permalloy, 1/8 mil., ribbon stress-wrapped on a 0.1 inch stainless steel bobbin) having two toroidal-windings, an input winding of n_1 turns, and an output winding of n_2 turns. See Fig. 26. The flux, ϕ, versus ampere-turn, ni, diagram for this core is essentially that shown in Fig. 27. Figures 28 (a) and 28 (b) show typical paths of core operation in the Transmag circuit. The operation cycle consists of a receive interval followed by an equal transmit-recover interval as shown in Fig. 23.

Passage of a signal through the magnetic amplifier takes place as follows: At the beginning of the receive-interval the core is always in the state of negative remanence, which is appropriately taken as the origin in Figs. 28 (a) and 28 (b). Then, during the receive-interval, which has a duration $T/2$, the incoming signal voltage $v_1(t) \geq 0$ produces a positive flux change $+ \Delta_1 \phi$ having a magnitude

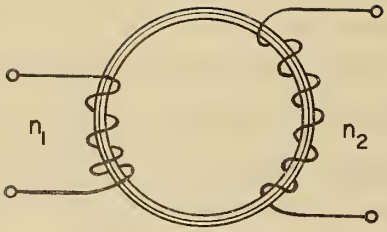

Figure 26. The magnetic amplifier

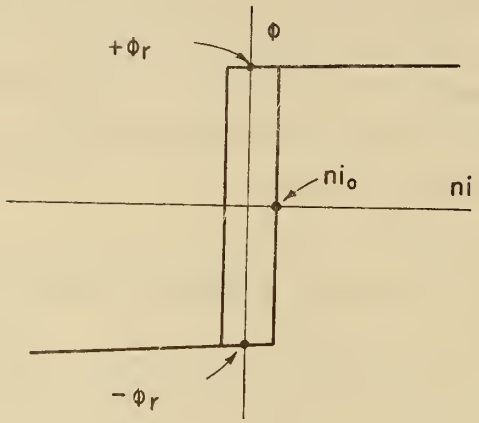

Figure 27. The saturation flux versus ampere-turn diagram of the magnetic amplifier core

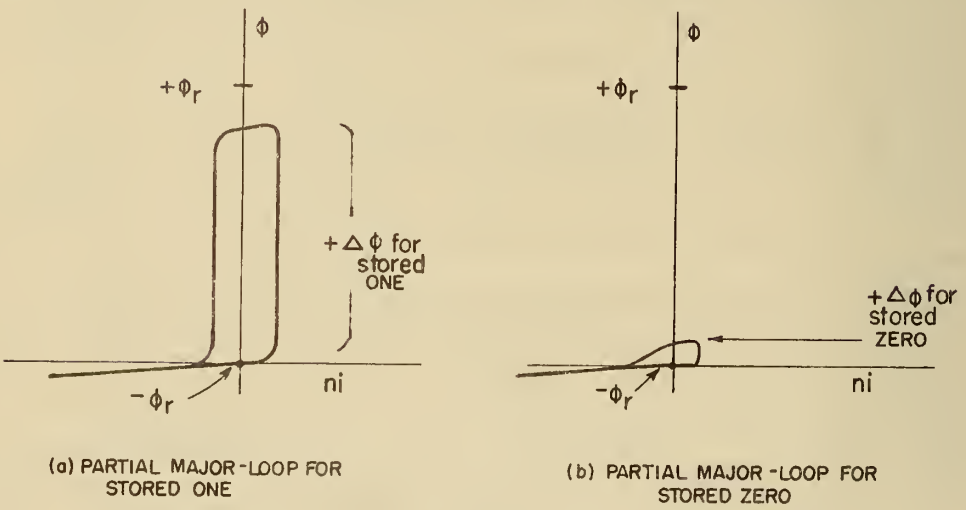

Figure 28. a. Partial major-loop for a stored ONE

b. Partial major-loop for a stored ZERO

$\Delta\phi_1 = \int_0^{T/2} \frac{v_1(t)}{n_1}\,dt$ so that at the end of the receive-interval, the core is in the state $-\phi_r + \Delta_1\phi$. The core, being highly retentive, even in partial major loops, then stores the quantity $\Delta_2\phi \simeq \Delta_1\phi$ which is proportional to the signal parameter $x = \int v\,dt$. Then during the transmit-recover interval, load current is switched into the output winding in the proper sense to return the core to its initial state. The resulting output signal from the amplifier is then obtained from $\int_0^{T/2} \frac{v_2(t)}{n_2}\,dt = \Delta_2\phi$. Then if $x = \int_0^{T/2} \frac{v_1(t)}{n_1}\,dt$ is the input signal, and $y = \int_0^{T/2} \frac{v_2(t)}{n_2}\,dt$ is the amplifier output signal, $\frac{x}{n_1} = \Delta_1\phi \simeq \Delta_2\phi = \frac{y}{n_2}$, and $y = \frac{n_2}{n_1}\,x$, provided $x \leq 2n_1\phi_r$. Therefore the transfer characteristic of the amplifier is linear with a slope g equal to n_2/n_1 up to the saturation point $x = 2n_1\phi_r$, $y = 2n_2\phi_r$.

The graph in Fig. 5 illustrates the shape of the transfer-function of the magnetic amplifier alone. It fails to cross the unity gain line at the point R.

The fact that the slope $g = \frac{n_2}{n_1}$ of the magnetic amplifier transfer function can easily be made greater than unity invites an attempt to achieve an acceptable transfer function by making $n_2/n_1 > 1$ and then introducing a signal threshold. To produce this threshold advantage was taken of the fact that the core itself possesses a magnetizing current threshold. See Fig. 27. To convert this to a voltage (and therefore volt-second) threshold a resistor was put in series with the input winding.

As a first step in deriving the volt-second transfer-function of the resistor-core combination the voltage transfer function is now worked out. The core is first shown to behave as a resistor having a current threshold.

Faraday's law (ignoring the sign)

$$v_c = n\dot{\phi},$$

and the constant-current, domain wall motion switching equation of Manyuk & Goodenough [3]

$$S_w = (H - H_o)\,\tau \qquad (21a)$$

$$= (n/l)\,(i - i_o)\,\tau \qquad (21b)$$

where

v_c = voltage across the core winding

n = number of winding turns

$\dot{\phi}$ = time rate of change of core flux

S_w = constant-current switching coefficient of the core material

l = core magnetic path length

i = winding current

i_o = core magnetizing current threshold*

τ = time required to switch a fixed fraction of the core total flux

regulate the behavior of the core during switching. Now τ may be defined by

$$\tau = \frac{2\phi_r}{\overline{\dot{\phi}}} \tag{22}$$

where $\overline{\dot{\phi}}$ is the average rate of change of flux brought about during time τ by the constant current i. If we make the simplifying assumption that $\dot{\phi}$, the instantaneous rate of change of flux, is constant during this time, then $\overline{\dot{\phi}} = \dot{\phi}$, and $\tau = 2\phi_r/\dot{\phi}$. Substituting for τ in (21b), gives

$$\frac{\phi}{i - i_o} = \text{constant} = \frac{2n\phi_r}{S_w l} \tag{23}$$

where $\dot{\phi}$ and i are now instantaneous flux-rate and current. Then, from Faraday's law, one obtains

$$\frac{v_c}{i - i_o} = \frac{2n^2 \phi_r}{S_w l} = R_c, \tag{24}$$

which defines the core switching resistance R_c as the ratio of the core voltage v_c to the core <u>excess</u> current $i - i_o$. Fig. 29 is a plot of v_c versus i showing the threshold i_o and constant slope R_c. Fig. 30 shows the core, in series with a resistor R_s, being driven by a voltage source v.

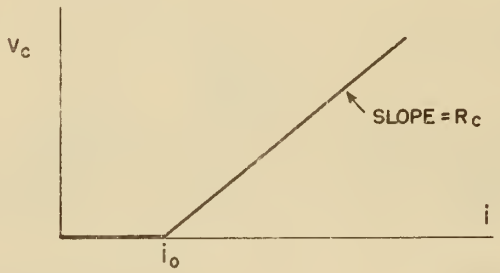

Figure 29. Switching volt-ampere diagram of the magnetic amplifier

* i_o materially exceeds the dc coercive current when τ is of the order of a few microseconds or less.

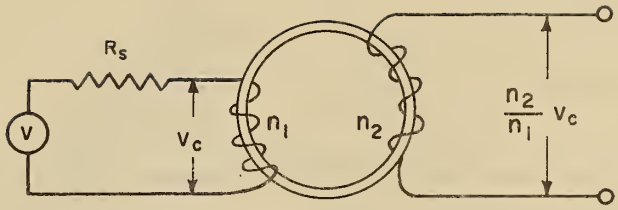

Figure 30. The computer element that consists of R_s and the magnetic amplifier

Remembering that R_c has a threshold i_o, the circuit equation is

$$\left.\begin{aligned} R_s i + R_c (i - i_o) &= v \; ; i \geq i_o \\ R_s i + 0 (i - i_o) &= v \; ; i < i_o \end{aligned}\right\}$$

and for $i \geq i_o$,

$$i = \frac{v + R_c i_o}{R_s + R_c} .$$

Then

$$\begin{aligned} v_c &= (i - i_o) R_c \\ &= iR_c - i_o R_c \\ &= \frac{v + R_c i_o}{R_s + R_c} R_c - i_o R_c \\ &= \frac{R_c}{R_s + R_c} \left[v - i_o R_s \right] \end{aligned} \qquad (25)$$

gives the relationship between core voltage and the voltage applied across the resistor and core in series. This is graphed in Fig. 31, showing the constant slope $\frac{R_c}{R_s + R_c}$ and the voltage threshold $i_o R_s$.

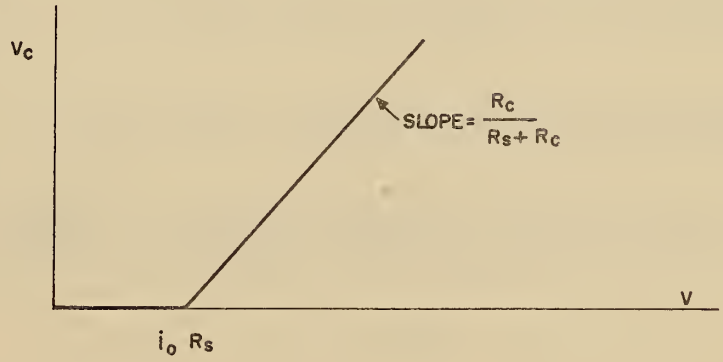

Figure 31. Switching plot of core-input voltage v_c versus v, the voltage applied to R_s

To get the resistor-core volt-second transfer function y = f(x) we set

$$x = \int_o^{T/2} v(t)dt, \text{ and}$$

$$y = \frac{n_2}{n_1} \int_o^{T/2} v_c(t)\, dt = {}^{n_2}/_{n_1} \frac{R_c}{R_s + R_c} \int_o^{T/2} \left[v(t) - i_o R_s\right] dt$$

Here it is necessary to assume some form for v(t). In the magnetic digital amplifiers described in this paper $v = v_o \sin 2\pi t/T$. Therefore

$$x = \int_o^{T/2} v_o \sin 2\pi t/T \quad dt \tag{26}$$

and

$$y = \frac{n_2}{n_1} \frac{R_c}{R_s + R_c} \int_o^{T/2} \left[v_o \sin 2\pi t/T - i_o R_s\right] dt \tag{27}$$

It proves easier to deal with y = f(x) graphically than to attempt to relate y and x in an equation. The graph of y = f(x) is obtained by plotting y and x as functions of the parameter t over the range $0 < t < T/2$. Integrating (26) gives

$$x = 1/2 \left[1 - \cos 2\pi t/T\right] \frac{v_o T}{\pi} \tag{28}$$

Observe that $\frac{v_o T}{\pi}$ is the voltage-time-area of the half sine-wave. To integrate (27) we refer to Fig. 34 and write,

$$y(t) = \frac{n_2}{n_1} \left[\int_o^{t_o} v_c\, dt + \int_{t_o}^{t} v_c\, dt \right],$$

and because $v_c = 0$ for $0 < t < t_o$

$$y(t) = \frac{n_2}{n_1} \frac{R_c}{R_s + R_c} \int_{t_o}^{t} \left[v_o \sin 2\pi \frac{t}{T} - i_o R_s\right] dt$$

$$= \frac{n_2}{n_1} \frac{R_c}{R_s + R_c} \left\{ \frac{v_o T}{2\pi} \left[- \cos 2\pi \frac{t}{T} \right]_{t_o}^{t} - i_o R_s (t - t_o) \right\}$$

$$= \frac{n_2}{n_1} \frac{R_c}{R_s + R_c} \left\{ \frac{v_o T}{2\pi} \left[\cos 2\pi \frac{t_o}{T} - \cos 2\pi \frac{t}{T} \right] - i_o R_s (t - t_o) \right\} \tag{29}$$

$$= \frac{1}{2} \frac{n_2}{n_1} \frac{R_c}{R_s + R_c} \left[\left(\cos 2\pi \frac{t_o}{T} + 2\pi \frac{i_o R_s}{v_o} \frac{t_o}{T}\right) - \left(\cos 2\pi \frac{t}{T} + 2\pi \frac{i_o R_s}{v_o} \frac{t}{T}\right) \right] \frac{v_o T}{\pi}$$

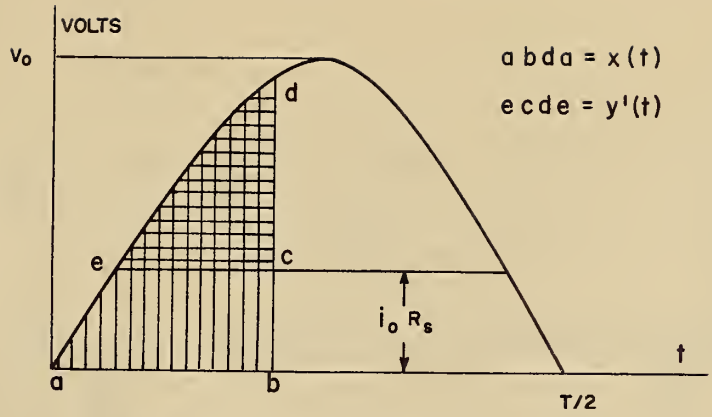

Figure 32. The relationship of y'(t) to x(t)

over the range $t_o < t < T/2 - t_o$. Then, from the figure it is seen that the angle $2\pi t_o/T$ can be evaluated from

$$\sin 2\pi \frac{t_o}{T} = \frac{i_o R_s}{v_o} = m, \tag{30}$$

The ratio m is a measure of the threshold nonlinearity that is introduced by means of the drop $i_o R_s$. Observe that for m = 0, $t_o = 0$ and the right side of (29) reduces to that of (28) making y = x.

The nonlinearity measured by m is seen in a plot of the quantity

$$y' = \int_o^t (v - i_o R_s)\, dt \tag{31a}$$

$$= 1/2 \left[(\cos 2\pi \frac{t_0}{T} + 2\pi m \frac{t_0}{T}) - (\cos 2\pi \frac{t}{T} + 2\pi m \frac{t}{T}) \right] \frac{v_o T}{\pi} \tag{31b}$$

versus

$$x = \int_o^t v\, dt$$

$$= 1/2 \left[1 - \cos 2\pi\, t/T \right] \frac{v_o T}{\pi} \tag{28}$$

where y' is the area ecde in Fig. 32, and x is the area abda.

Curve 1 in Fig. 33 shows this plot for m = 0.36, which is close to the value used in the experimental magnetic amplifier. Here $2\pi \frac{t_o}{T} = \arctan 0.36 \simeq 0.37$ radians, and cos 0.37 radians = 0.93. Thus

$$y'(t) = 1/2 \left[.93 + .37(.36) - (\cos 2\pi\, t/T + .36 \cdot 2\pi\, t/T) \right] \frac{v_o T}{\pi},$$

which is plotted against

$$x(t) = 1/2 \left[1 - \cos 2\pi\, t/T \right] \frac{v_o T}{\pi} \quad \text{over the range } 0 < t < T/2, \text{ or}$$

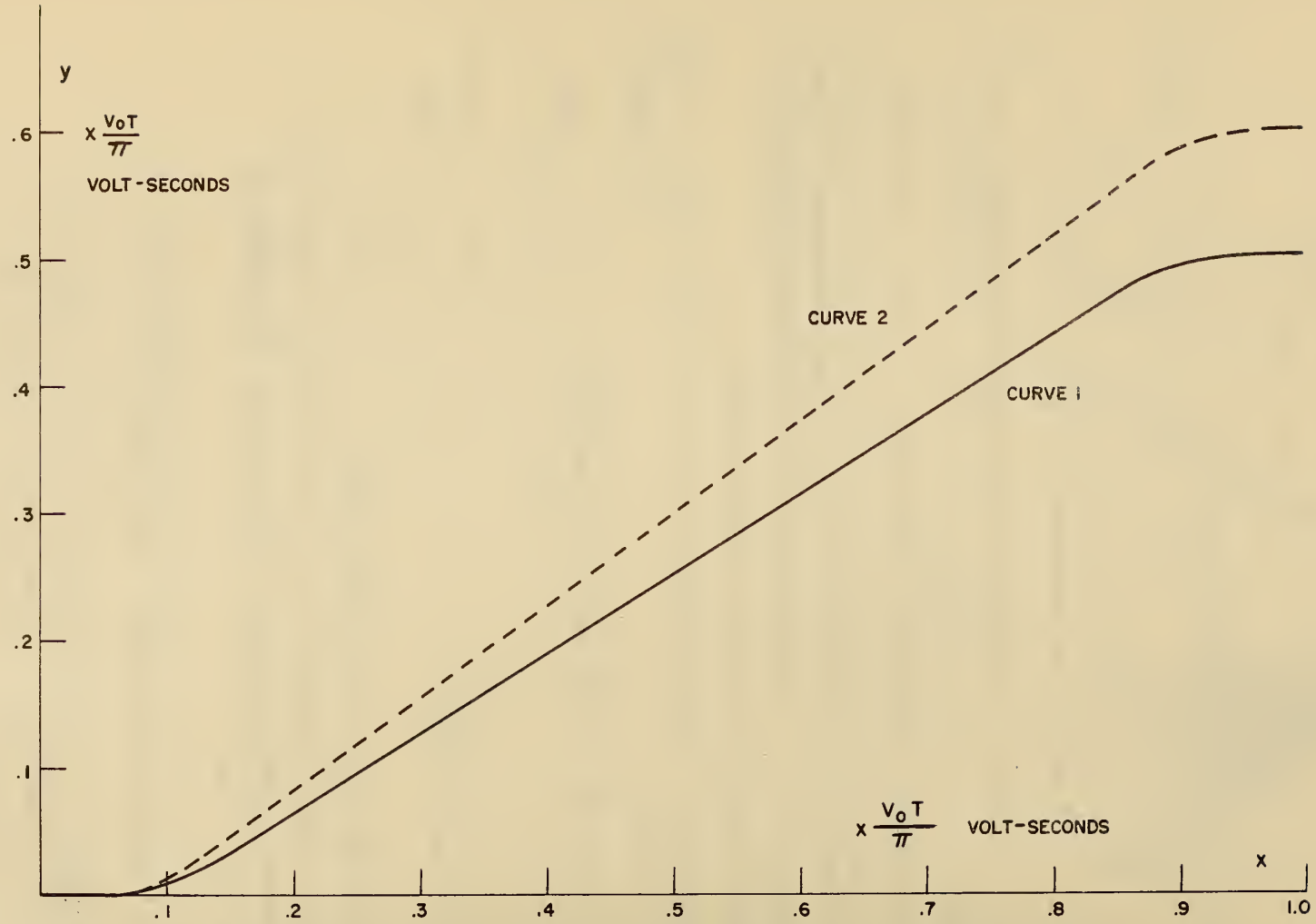

Figure 33. The volt-second transfer-function for the element that consists of R_s and the magnetic amplifier

$$x = 0 \text{ to } x = \frac{v_o T}{\pi} .$$

Curve 2 shows $y = f(x)$ where

$$y(t) = \frac{n_2}{n_1} \int_o^t v_c(t)\, dt = \frac{n_2}{n_1} \int_o^t \frac{R_c}{R_s + R_c} (v - i_o R_s)\, dt$$

$$= \frac{n_2}{n_1} \frac{R_c}{R_s + R_c} y' \simeq 1.2\, y'$$

with $n_2/n_1 = 2$, and $\frac{R_c}{R_s + R_c} = \frac{750}{470 + 750} \simeq 0.6$, which are the experimental values used.

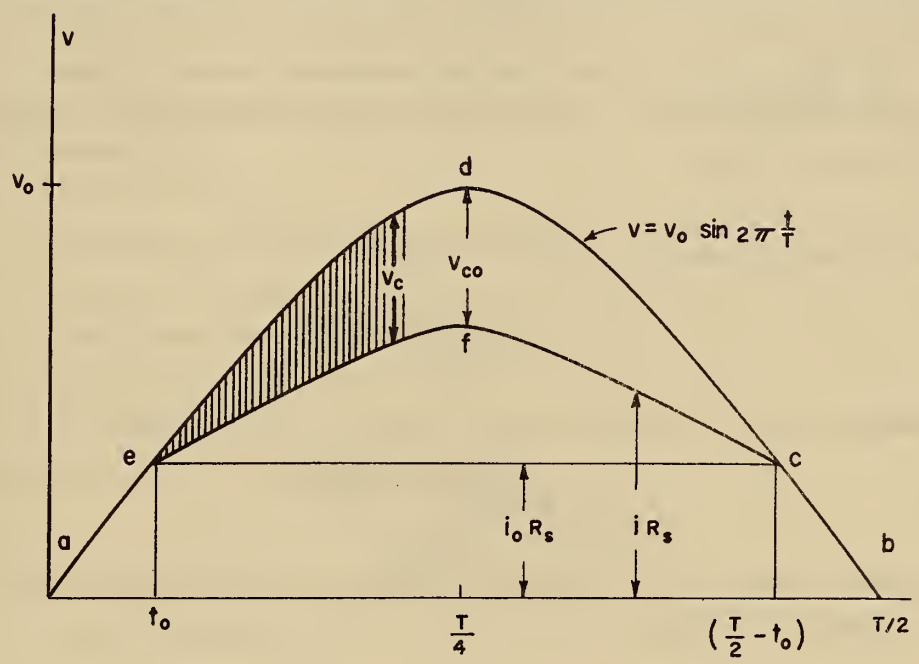

Figure 34. The relationship between v, v_c, iR_s, i_oR_s, t_o and T/2

Fig. 34 shows the relationships between the quantities

$$v = v_o \sin 2\pi\, t/T = 10v \sin 2\pi\, (300 \text{ kc})$$

$$v_c = (i - i_o) R_c = \frac{R_c}{R_s + R_c} (v - i_o R_s) = .6(v - 3.6v)$$

$$v_{R_s} = iR_s = i(470 \text{ ohms})$$

$$i_o R_s = 3.6v$$

$\frac{n_2}{n_1} \cdot v_c = 2v_c$

$v - i_o R_s = v - 3.6v_o$

The shaded area is equal to $\int_o^t v_c \, dt$.

Curve 2, Fig. 33 exhibits some threshold, but lacks sufficient slope to cross the unity-gain line. The slope of the whole curve could be increased by increasing the product $\frac{n_2}{n_1} \cdot \frac{R_c}{R_s+R_c}$, but it would be preferable to preserve the threshold region and increase the slope near $x = v_o T/2\pi$. This effect might be achieved by increasing both $\frac{n_2}{n_1} \frac{R_c}{R_s+R_c}$ and m --- or by a suitable combination of $\frac{n_2}{n_1}$, $\frac{R_c}{R_s+R_c}$ and m. Because m is a measure of the nonlinearity sought, and because, generally speaking, $\frac{n_2}{n_1} \frac{R_c}{R_s+R_c}$ affects the slope of the transfer function, we have the problem of maximizing these quantities subject to circuit constraints and practical limitations. We now wish to consider how this may be done.

Equation (25) may be written as

$$\frac{v_c}{v} = \frac{R_c}{R_s+R_c}\left(1 - \frac{i_o R_s}{v}\right);$$

and in particular,

$$\frac{v_{co}}{v_o} = \frac{R_c}{R_s+R_c}\left(1 - \frac{i_o R_s}{v_o}\right), \tag{32}$$

where v_{co} is the peak value of the core voltage v_c. See Fig. 34. Solving (32) explicitly for $i_o R_s/v_o = m$ as defined in (30) gives

$$\frac{i_o R_s}{v_o} = m = \frac{1 - v_{co}/v_o}{1 + \frac{v_{co}}{i_o R_c}} \tag{33}$$

See Appendix I.

Then making the substitution

$$\frac{v_{co}}{v_o} = \frac{R_c}{R_s+R_c}\left(1 - \frac{i_o R_s}{v_o}\right) = \frac{R_c}{R_s+R_c}(1-m) \tag{34}$$

one has finally, see Appendix II, that

$$m = \frac{1}{1 + \frac{R_c+R_s}{R_s} \cdot \frac{v_{co}}{i_o R_c}} = \frac{1}{1 + \frac{v_{co}}{i_o R_p}} \tag{35a}$$

in which

$$1/R_p = 1/R_s + 1/R_c \tag{35b}$$

To equations (34) (35a) and (35b, which will prove useful in optimizing m, must be added a necessary relation involving n_2/n_1.

$$\frac{n_2}{n_1} \underset{\text{must}}{\leqq} \frac{v_o}{v_{co}} \tag{36}$$

This expresses a constraint imposed by the nature of the particular transistor-magnetic-core amplifier reported on here. The reason for this constraint will be explained in the description of the circuit.

The problem of maximizing the threshold parameter m is considered first, and is here worked out in the following steps:

1. Assume there is given:
   a. A magnetic core having the known parameters
      ϕ_r, S_w, l, and H_o,
   b. with an input winding of n_1 turns
   c. to operate at a frequency $f = 1/T$.
2. If the core is to be fully switched by a full input signal, ϕ_r, n_1 and T will determine v_{co}. It can be shown, see Appendix III, that

$$\frac{v_{co}T}{\pi} \simeq \int_o^{T/2} v_c dt.$$

   Then, for full switching

$$\frac{v_{co}T}{\pi} \simeq \int_o^{T/2} v_c dt = n_1 \int_{-\phi_r}^{+\phi_r} d\phi = 2n_1 \phi_r$$

3. Making use of equations (35a) and (35b) we see that to maximize m we must maximize $i_o R_p$.
4. Because i_o is already fixed by the core parameters H_o, and l, and by n_1, we must maximize R_p.
5. At frequencies above 100 kc the core resistance R_c, which is given by

$$R_c = \frac{2n_1^2 \phi_r}{lS_w} \tag{24}$$

   sets the upper limit on R_p.

6. This limit is approached when $R_s >> R_c$.

For this case, the design equations are:

$$m \simeq \frac{1}{1 + \frac{v_{co}}{i_o R_c}} \qquad (37a)$$

$$\frac{v_o}{v_{co}} \simeq \frac{R_s}{(1-m)R_c} \qquad (37b)$$

$$\frac{n_2}{n_1} \leq \frac{v_o}{v_{co}} \qquad (37c)$$

$$R_p \simeq R_c$$

$$R_s >> R_c$$

But this arrangement is not practical because, as (37b) shows, it results in an excessive ratio of v_o to v_{co}. See Fig. 35, for example, in which the shaded area shows the volt-seconds applied to R_c. This is inefficient because most of the input power is wasted in R_s.

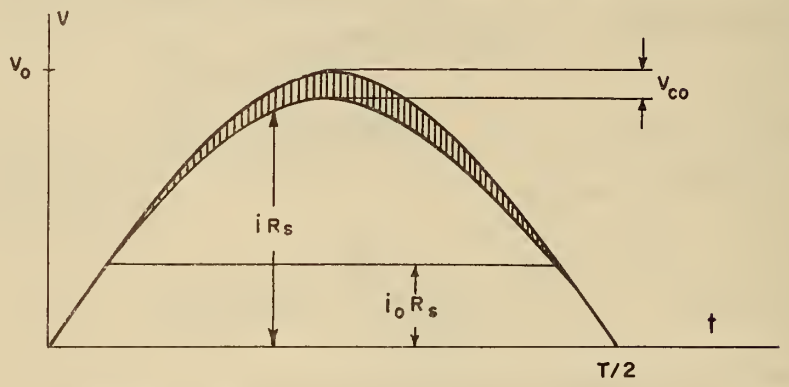

Figure 35. Large ratio of v_o to v_{co} when $R_s >> R_c$

7. The maximum practical value for R_p, i.e., the point of diminishing returns, is where $R_s = R_c$. Then, for this optimum case, the design equations are

$$m = \frac{1}{1 + \frac{2v_{co}}{i_o R_c}} \qquad (38a)$$

$$\frac{v_o}{v_{co}} = \frac{2}{1-m} \qquad (38b)$$

$$R_p = R_c/2$$

$$R_s = R_c$$

$$\frac{n_2}{n_1} \leq \frac{v_o}{v_{co}} \qquad (38c)$$

For the optimum case we see that the core parameters completely determine v_{co}, m, v_o and the upper limit on n_2/n_1 at a given frequency, when the core is fully switched.

8. In the transistor-core amplifier the situation was more favorable than this because it was possible, by means of a core bias current i_b (derived from an auxiliary current source) to produce an independently variable effective threshold current $i'_o = i_o + i_b$. The optimum case design equations then become

$$m = \frac{1}{1 + \frac{2v_{co}}{i'_o R_c}} \qquad (39a)$$

$$\frac{v_o}{v_{co}} = \frac{2}{1-m} \qquad (39b)$$

$$R_p = R_c/2$$

$$R_s = R_c$$

$$i'_o = i_o + i_b$$

$$\frac{n_2}{n_1} \leq \frac{v_o}{v_{co}} \qquad (39c)$$

in which m and hence v_o and n_2/n_1 are freely adjustable through i'_o.

For example, if we make $i'_o R_s = 2v_{co}$, then $m = 0.5$, $v_o = 4 v_{co}$, and $n_2/n_1 \leq 4$. See Fig. 36. Or if we make $i'_o R_s = v_{co}$, then $m = 0.33$, $v_o = 3 v_{co}$, and $\frac{n_2}{n_1} \leq 3$. See Fig. 37. The largest practical value of m for this case is probably 0.35. *

---

* The fact that R_c is actually not constant during switching results in a better threshold than is predicted by m, however.

9. Finally we consider the alternative case, achievable only at lower frequencies, * for which $R_p > R_s$. The design equations then are:

$$m \simeq \frac{1}{1 + \frac{v_{co}}{i'_o R_s}} \qquad (40a)$$

$$\frac{v_o}{v_{co}} = \frac{1}{1 - m} \qquad (40b)$$

$$\frac{n_2}{n_1} \leq \frac{v_o}{v_{co}} \qquad (40c)$$

$$R_p \simeq R_s$$

$$R_c >> R_s$$

Fig. 38 illustrates this case for m = 0.5, a very large value. However, even for this large value, v_o is only a little over twice v_{co}. This case permits the smallest ratios v_o/v_{co} and $\frac{n_2}{n_1}$ for a given value of m.

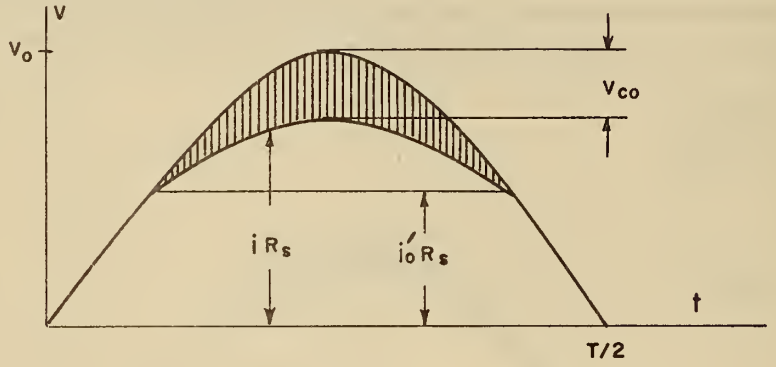

Figure 36. Large value of $m = i'_o R_s/v_o = 0.5$ achievable through the use of a bias current. $R_s = R_c$

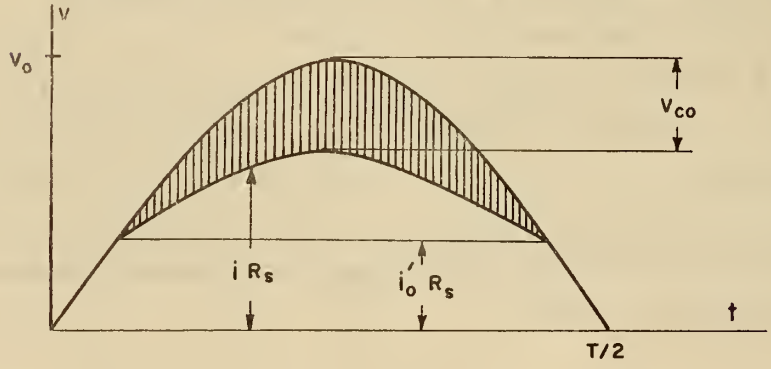

Figure 37. $v_o = 3v_{co}$ and $m = 0.33$ when $R_s = R_c$ and $i'_o R_s = v_{co}$

* At lower frequencies, larger values for ϕ_r and n_1 are possible.

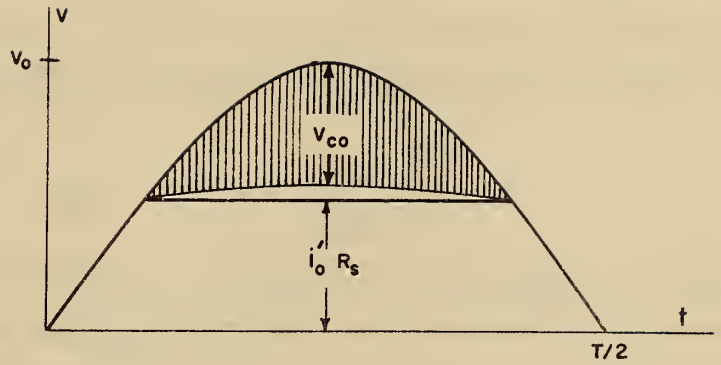

Figure 38. Large value of m and small value for v_o/v_{co} achievable when $R_c >> R_s$

We now take up the problem of maximizing the slope of $y = f(x)$. It has been stated that this slope will, generally speaking, be proportional to $\frac{n_2}{n_1} \quad \frac{R_c}{R_s + R_c}$. But in the particular application being considered here n_2/n_1 is subject to the restriction (36); and this combined with (34) gives

$$\frac{n_2}{n_1} \quad \frac{R_c}{R_s + R_c} = \frac{R_s + R_c}{R_c (1-m)} \cdot \frac{R_c}{R_s + R_c} = \frac{1}{1 - m} \tag{41}$$

as the maximum value for $\frac{n_2}{n_1} \quad \frac{R_c}{R_s + R_c}$.

The actual slope of $y = f(x)$ is found by taking the ratio of dy/dx to dx/dt.

$$\frac{dy}{dt} = \frac{n_2}{n_1} \quad \frac{R_c}{R_s + R_c} \quad \frac{dy'}{dt} = \frac{n_2}{n_1} \quad \frac{R_c}{R_s + R_c} (v - i_o R_s) \tag{42}$$

(see equation (31a) and Fig. 32), and

$$\frac{dx}{dt} = v. \tag{43}$$

From which

$$\left.\begin{aligned} \frac{dy}{dx} &= \frac{n_2}{n_1} \quad \frac{R_c}{R_s + R_c} \left(1 - \frac{i_o R_s}{v}\right) \\ &= \frac{n_2}{n_1} \quad \frac{R_c}{R_s + R_c} \left(1 - \frac{i_o R_s}{v_o \sin 2\pi t/T}\right) \\ &\quad \text{for } t_o < t < T/2 - t_o. \\ &= 0, \text{ for } t_o > t > T/2 - t_o. \end{aligned}\right\} \tag{44}$$

Then from (41)

$$\left.\begin{aligned} \frac{dy}{dx} &= \frac{1 - \frac{m}{\sin 2\pi t/T}}{1 - m} \; ; \; t_o < t < T/2 - t_o \\ &= 0, \; t_o > t > T/2 - t_o \end{aligned}\right\} \tag{45}$$

This shows the slope of the transfer function to be maximum at $t = T/4$, at which time

$$\left.\frac{dy}{dx}\right|_{\substack{T/4 \text{ or} \\ x = \frac{v_o T}{2\pi}}} = 1 \tag{46}$$

At all other parts of the half-cycle $\frac{dy}{dx}$ is less than unity, approaching zero at t_o and at $T/2 - t_o$.

Thus we have the important result that, subject to the restriction (36), the volt-second characteristic of the core-resistor combination cannot cross the unity-gain line. Therefore core-resistor combinations alone, when operated in this way, are incapable of stable binary signal propagation. Fig. 39 indicates possible transfer functions whose slopes are given by (45). See Appendix IV.

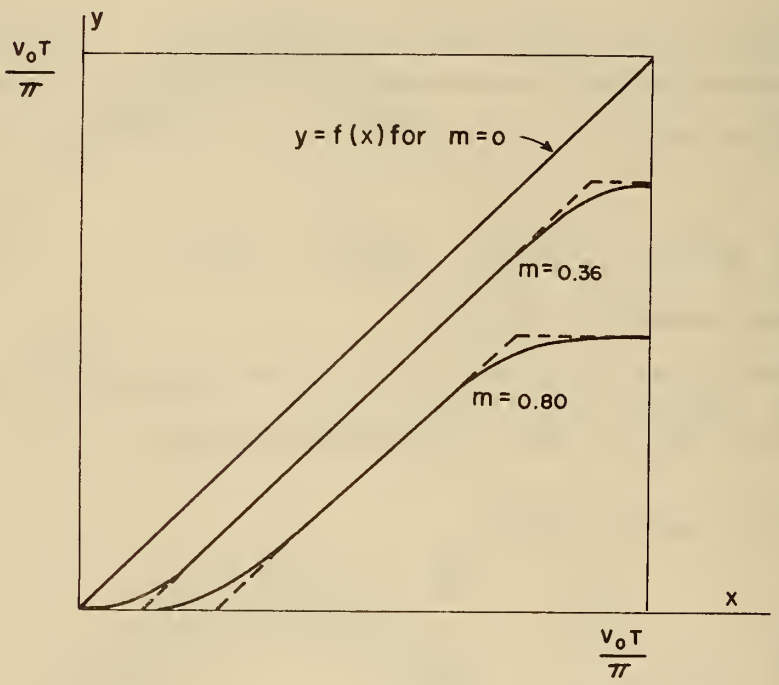

Figure 39. The volt-second transfer function of the resistor-magnetic-amplifier element for different values of m

During the transmit interval, the core is restored to negative remanence, not by v_c, but by a voltage $v = -v_o \sin 2\pi t/T$, (Observe that during the transmit interval, $T/2 \leq t \leq T$, the

sin $2\pi\, t/T < 0.$) applied to its output winding by means of a (current-limited) voltage source. Thus the voltage gain between the input to the core-resistor series combination and the core output winding is unity. The result is that volt-second gain, or loss, appears as time gain, or time loss --- as signal "stretching", or as signal curtailment. When the ratio n_2/n_1 is subject to the restriction (36), curtailment is the only possible result, with a consequent core flux-gain of less than unity. The proof of this is as follows:

$$\text{In general } \frac{dy}{dx} = \frac{dy/dt}{dx/dt} = \frac{(n_2/n_1)\, v_c}{v}.$$

Then, in the particular case where n_2/n_1 is restricted by (36), we have, from (45),

$$\frac{n_2}{n_1}\,\frac{v_c}{v} = \frac{dy}{dx} = \frac{1 - m/\sin 2\pi\, t/T}{1 - m}$$

$$\frac{v_c}{n_1} = \frac{v}{n_2}\,\frac{1 - m/\sin 2\pi\, t/T}{1 - m} \qquad (47)$$

where $v_c/n_1 = \dot{\phi}\,(t)$ in the core during the receive interval, and $v/n_2 = \dot{\phi}\,(t)$ during the transmit interval. See Fig. 40. Now, if during the receive interval $o \leq t < T/2$, the core, starting at negative remanence, experiences a flux change $\int_o^{t_1} \frac{v_c}{n_1}\, dt$, then during the transmit interval

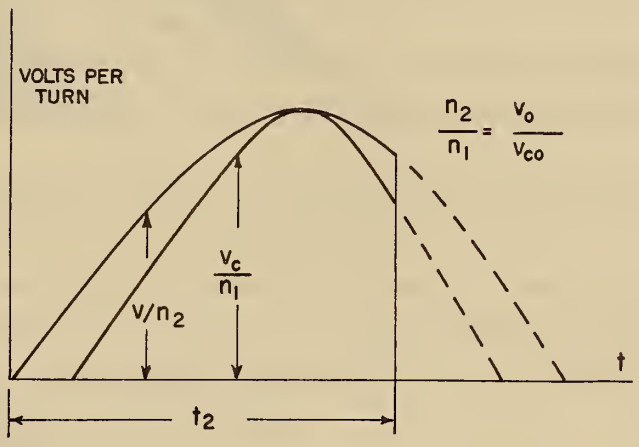

Figure 40. Core flux-gain is less than unity when $n_2/n_1 = v_o/v_{co}$

$T/2 \leq t \leq T$, the core will be restored to negative remanence in a time t_2 (measured from the beginning of the interval) determined by

$$\int_o^{t_1} \frac{v_c}{n_1}\, dt = \int_o^{t_2} \frac{v}{n_2}\, dt \qquad (48)$$

But, from (47) $\frac{v_c}{n_1} < \frac{v}{n_2}$ except at one point.

Therefore

$$t_2 < t_1. \tag{49}$$

See Figure 41. Now the flux change received by the next core in the sequence is

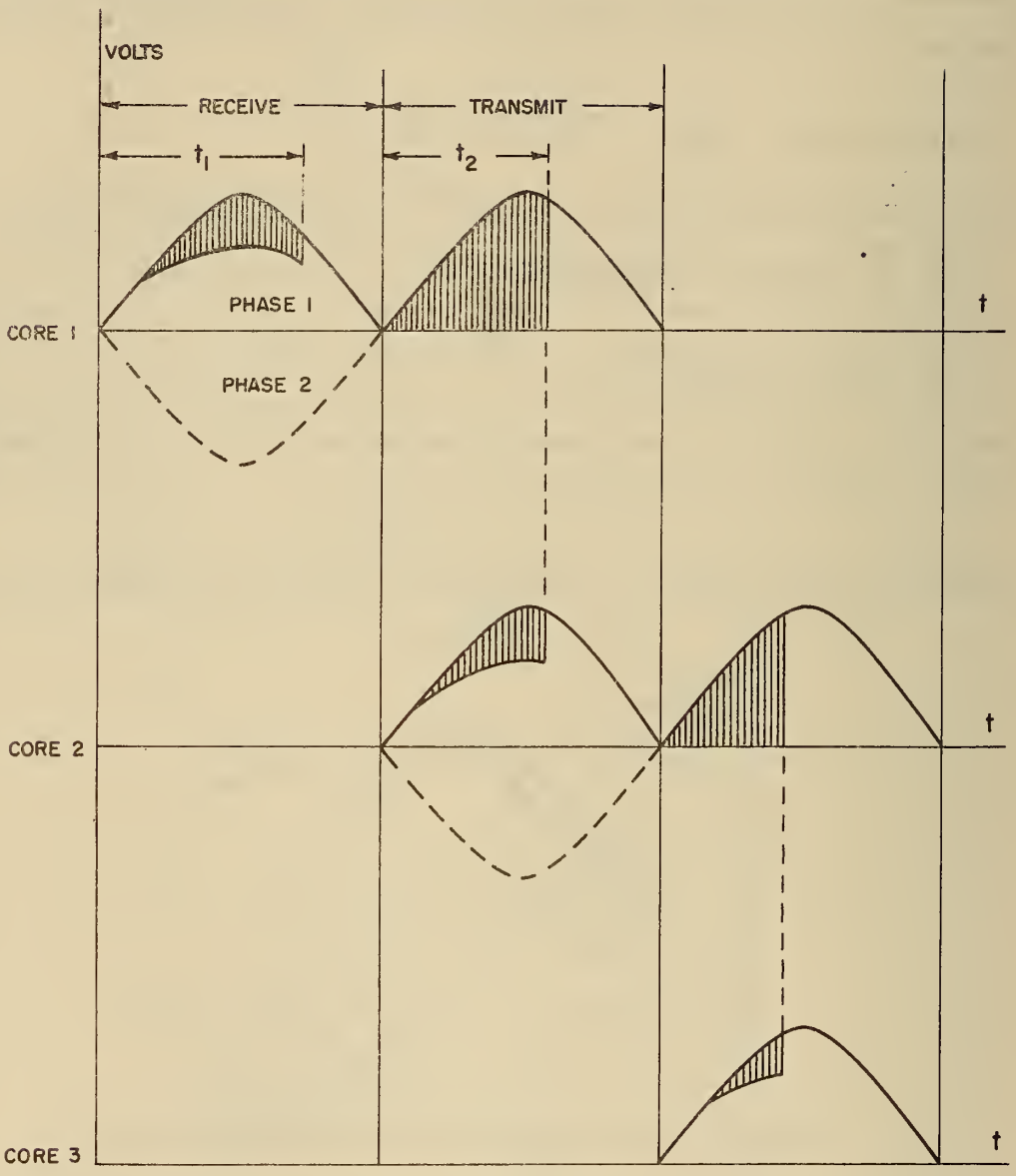

Figure 41. The progressive curtailment of core switching-time when $n_2/n_1 \leq v_o/v_{co}$ results in a flux-gain less than unity

$\int_0^{t_2} \frac{v_c}{n_1}\, dt$, and we have also by (47) that

$$\int_0^{t_2} \frac{v_c}{n_1}\, dt < \int_0^{t_2} \frac{v}{n_2}\, dt \qquad (50)$$

See also Fig. 40.

Thus by (48)

$$\int_0^{t_2} \frac{v_c}{n_1}\, dt < \int_c^{t_1} \frac{v_c}{n_1}\, dt \qquad (51)$$

which shows that the restriction

$$\frac{n_2}{n_1} \leq \frac{v_{co}}{v_o} \qquad (36)$$

results in flux gain which is less than unity.

See Fig. 40.

In similar manner it can be shown that if n_2 is arbitrarily increased, keeping all other quantities the same, the flux gain can be made greater than unity. For this case $t_2 > t_1$, (signal stretching) and the inequality (50) is reversed, although the corresponding inequality of the integrands is not at all times reversed. See Fig. 42 and Fig. 43.

When $t_2 > t_1$ it may happen that $t_2 > T/2$, and the core will not be returned to negative remanence. This undesirable situation can always be avoided, however, by making $v_o T/\pi \geq 2n_2 \phi_r$.

5. THE INTER-ELEMENT COUPLING NETWORK AND ITS EXPANSION INTO TWO-LEVEL SWITCHING

The core-resistor computer element just described requires a source of ac power to operate it and a means for coupling the binary signal to other computer elements. The simple circuit employed for these purposes in the magnetic- and transistor-magnetic amplifiers reported on here satisfies the following indispensible requirements:

1. It provides a voltage-source drive.
2. But, at the same time, it limits the current supplied to useful load current. It is a current-limited voltage source.
3. It provides unilateral transfer of signal from the transmitting element to the receiving elements.
4. It provides effective decoupling between the elements when they are not intended to communicate.
5. It decouples the receiving elements from each other.

6. It is expandable to form multi-input; multi-level logical coupling of the binary signal to each element,

7. It provides an effective means for driving the fan-out lead capacitance.

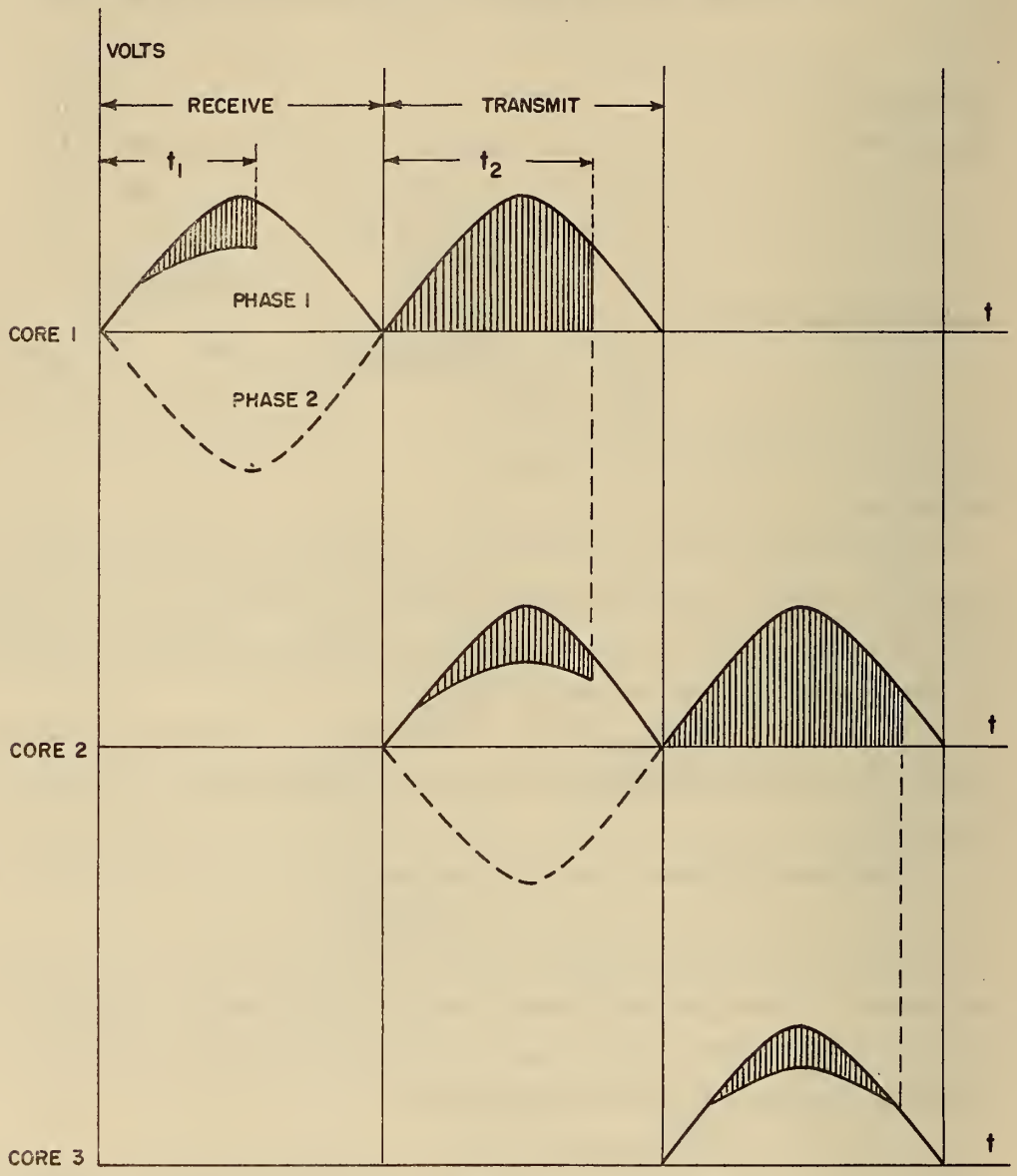

Figure 42. The progressive lengthening of core switching time when $n_2/n_1 > v_o/v_{co}$ results in a flux-gain greater than unity.

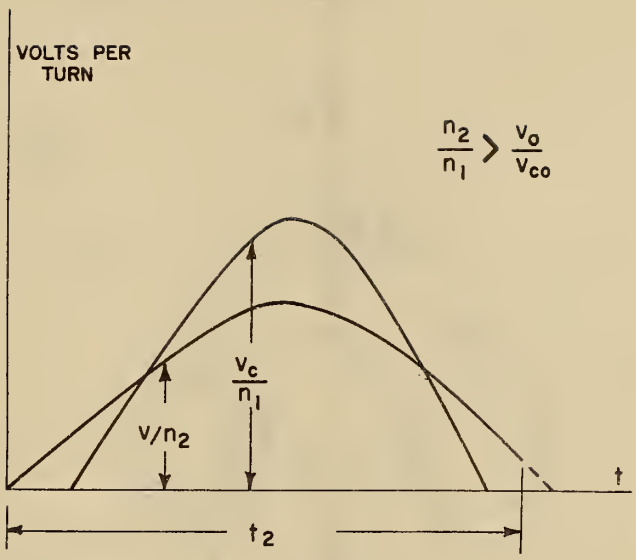

Figure 43. A flux-gain greater than unity can result if $n_2/n_1 > v_o/v_{co}$

Figure 44 shows this inter-element coupling circuit, drawn in heavy lines. It consists of a d-c voltage source + V_p, an alternating voltage-source $v = v_o \sin 2\pi t/T$, a "pull-up" resistor R_p, a diode D_p called the "power diode", and a diode D_o called the "output diode." V_p and R_p are made large enough that the current in R_p remains effectively constant. This current is adjusted so that it exceeds the sum of the magnetizing current of core A plus v_o/R_s, the maximum input current to core B, by enough to maintain D_p in full conduction, even at the peak positive value, v_o, of the power source.

It is necessary to examine the operation of this coupling circuit both during the positive half-cycle of the power source, and during the negative half-cycle. During the positive half-cycle the cores are communicating therefore this is called the coupling half-cycle. A is transmitting its information to B. Some of the pull-up current entering the branch point J through R_p is being used to restore core A to its initial (ZERO) state; some is serving to magnetize B; the remainder maintains D_p in conduction so that the impedance to ground from J remains low. (It equals the forward resistance of D_p.) During this time v_c is negative and, because of the winding polarities (shown by the dots), tends to aid in restoring core A. Thus the current drawn from J by A is reduced by the presence of the current applied to the input winding through R_s. However, because the impedance to ground at J is only a few ohms while the equivalent resistance $(\frac{n_2}{n_1})^2 R_s$ of the primary circuit

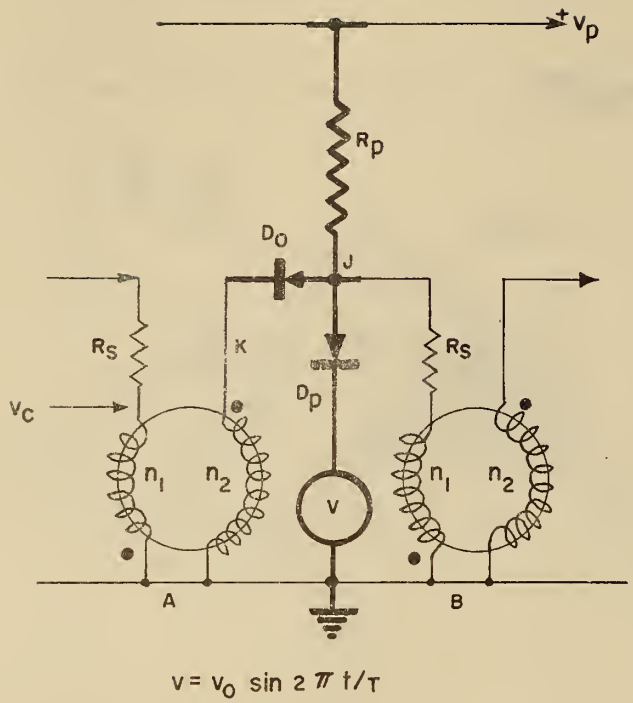

Figure 44. The inter-element coupling network

when referred to the secondary winding is typically several hundred ohms, the core is effectively controlled by the voltage v_J at J. If, at any part of the coupling half-cycle, it should happen that $\frac{n_2}{n_1} v_c > v$, diode D_o would simply open, and the excess portion of the pull-up current would be diverted through D_p with negligible effect on v_J. However, under the restriction (36) of section this condition would not come about. Furthermore, an increase in n_2 alone could not serve to bring it about because this would produce a compensating reduction of v_c, as may be deduced from Fig. 45, which shows everything referred to the core output winding. D_o would remain conducting and the core would remain under the control of the coupling circuit.

When core A saturates (at negative remanence) its c.e.m.f. drops to zero. As a result J is pulled to ground by the output winding, which takes the entire pull-up current, leaving D_p open for the remainder of the coupling half-cycle.

During the negative -, or decoupling half cycle, A and B are not communicating. A is receiving while B is transmitting. Under restriction (36), $v_{co} \frac{n_2}{n_1} \leq v_o$, with the result that D_o remains open. Thus, while it is receiving, core A is completely under the control of the incoming signal voltage applied to R_s. If A saturates before the end of its receive interval the cathode of D_o returns to ground potential without having any affect on core B.

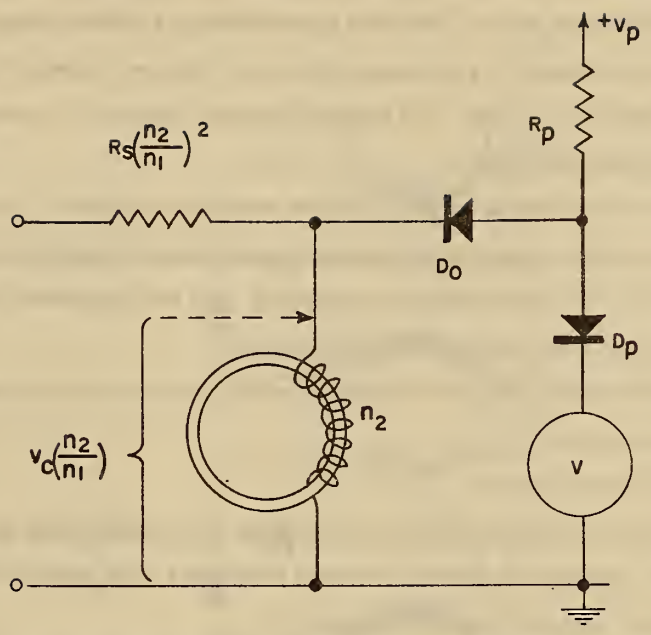

Figure 45. Core impedance presented to the inter-element coupling network during transmission of a ONE

It is during the decoupling half-cycle that the restriction (36) is made necessary. For if n_2 is increased to make $\frac{n_2}{n_1} v_c$ greater than v_J at any time, then during this time D_o conducts, control of core A passes from the input winding to the output winding (since the core is controlled by the lowest impedance source presented to it), and reception of information is interfered with. We see that restriction (36) is imposed by the requirement that D_o be kept non-conducting during the decoupling half-cycle. During both half-cycles R_s serves the indispensable purpose of preventing the excess flow of current from J when the impedance of the input winding disappears, upon core saturation.

Because the magnetic amplifier operation cycle consists of two equal intervals, receive, and transmit-recover, it is a two-phase system. In a sequence of these amplifiers, for every coupling circuit that is performing the coupling function, there is another that is simultaneously performing the decoupling function. Thus all the odd-numbered coupling circuits are driven by sources of common phase, which might be called phase 1; and the even-numbered circuits are driven by sources having the opposite phase, called phase 2. Then if we identify each computer element* with the phase

* When the element transfer functions are inadequate, and elements must be combined into groups, the word element-group should replace the word element in the following discussion.

of the power source for which that element transmits, the odd-numbered elements will be called phase 1 elements and the even-numbered elements, phase 2 elements. Obviously, an element can communicate only with those of opposite phase. Since the transmission of a binary signal requires the simultaneous cooperation of an element of each phase, there are then two elements for each binary bit of information travelling in a cascade. (In n-phase systems there are n elements for every binary bit, if elements alone provide the delay.)

Figure 46 shows a portion of a cascade of magnetic digital amplifier elements. Figure 47 shows: How a binary ONE is transmitted from element A to element B; how B and C are decoupled; how a ZERO is transmitted from C to D; and how D and E are decoupled. All the operations shown are being carried out simultaneously by different portions of the circuit.*

We now wish to show specifically how the inter-element coupling circuit just described provides the requirements previously enumerated.

1. It provides a voltage source drive.

   As long as the power diode D_p remains conducting, the impedance to ground from the branch point J equals the dynamic forward resistance of D_p because the impedance of the power source is kept effectively zero.

2. But at the same time it limits the current supplied to useful load current. It is a current-limited voltage source.

   During the positive half-cycle, the largest current that can flow from J through the core output winding is the pull-up current $i_p = V_p/R_p$ even though the winding impedance drops to zero. Ni_p is the load current which must be accepted by the transmitting element in order to communicate with N receiving elements.

   During the negative half-cycle D_p continually conducts, but D_o prevents the flow of negative current from J to the left-hand core; and the current to the right-hand core is limited by R_s.

3. It provides unilateral transfer of signal from the transmitting element to the receiving elements.

   This is ensured by the fact that R_s is much larger than the impedance to ground from J.

4. It provides decoupling between the elements when they are not intended to communicate.

   During the decoupling half-cycle diode D_o remains open at all times. See Fig. 47(b) and (d) which shows the voltages v_K and v_J at the cathode and anode of D_o during this time.

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* Oscillograms of the waveforms shown in Figure 47 can be found in reference (4), Figure 12.

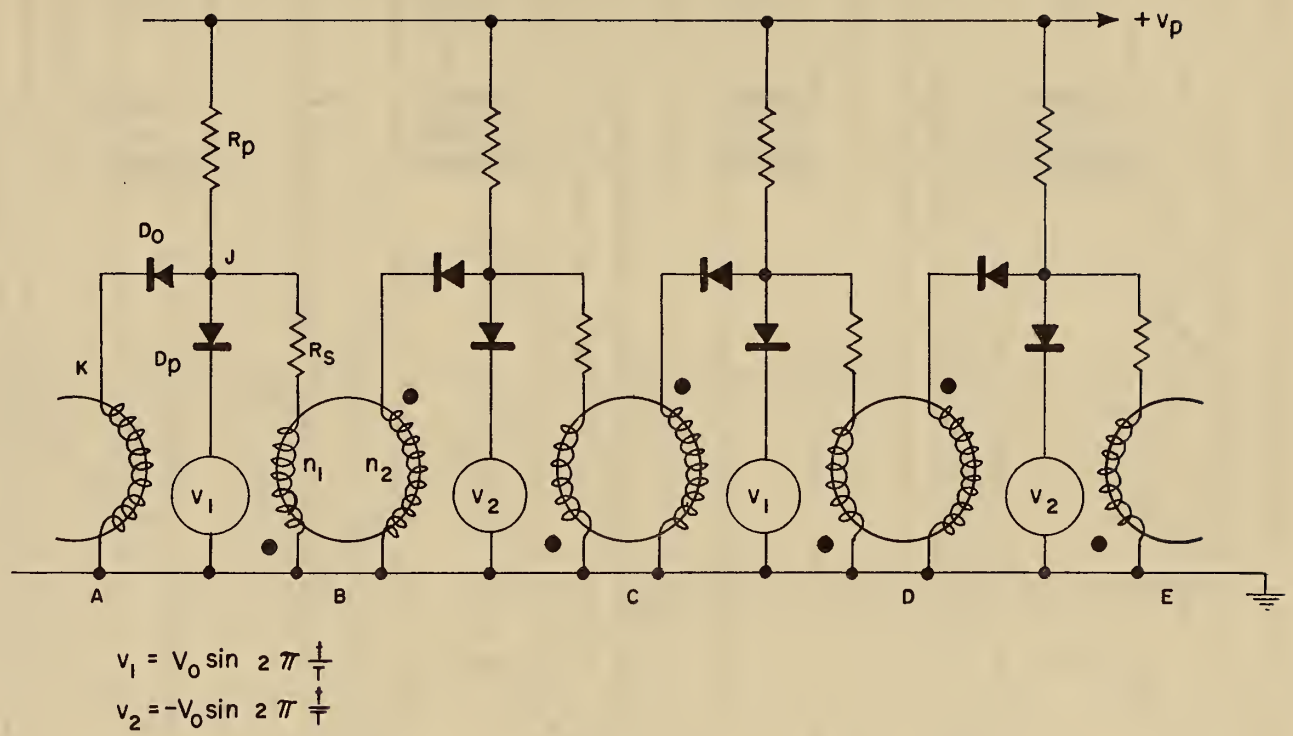


Figure 46. Part of a cascade of magnetic digital amplifiers

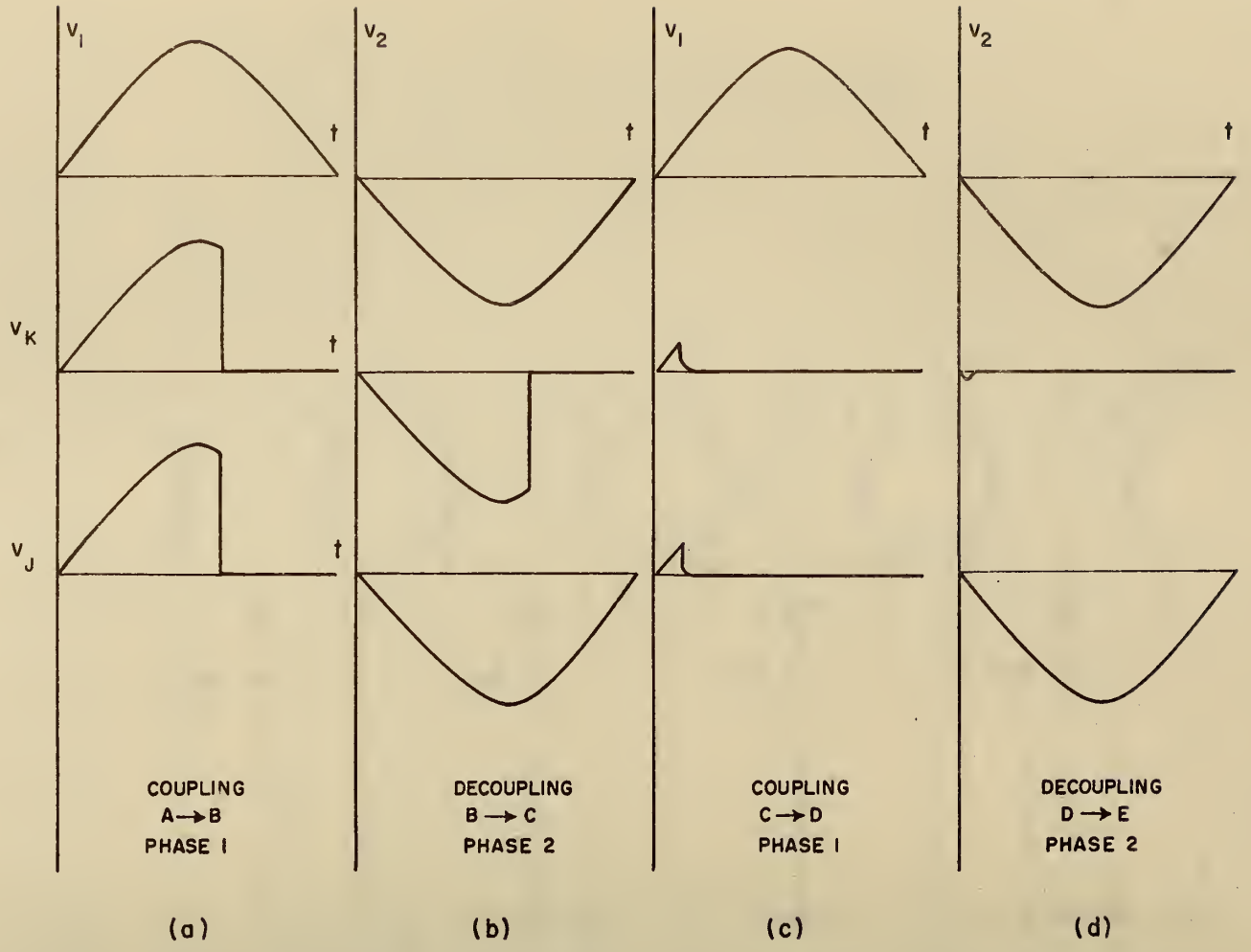


Figure 47. Voltage waveforms that occur during the reception and transmission of ONES and ZEROS

5. It decouples the receiving elements from each other.

This can be seen from Fig. 48 which shows three elements simultaneously receiving a signal from a single transmitting element. From the disposition of the diodes D_o it is apparent that neither positive nor negative current can flow from the point J of any receiving element to the point J of any other.

6. It is expandable to form multi-input-, multi-level logical coupling of the binary signal to each element.

Fig. 49 shows that, with the simple addition of diodes D_o in parallel, a logic AND-gate is formed. Here it should be pointed out that i_p must be large enough to reset all the transmitting cores and the receiving core during the coupling half-cycle; and also that if any of the input cores transmits a ZERO, the power to reset the remaining input cores must be supplied individually through their input windings. This somewhat undesirable result is rectified, however, by the seventh requirement. Fig. 50 shows how a second level of logic, the OR-gate, is formed simply by the addition of diodes D_2. Here it should be noticed that the current entering J from the gating structure may be zero, i_p or 2 i_p depending upon the disposition of the signals at the AND-gate inputs. In the first case $v_J = 0$; for the other cases, even with many AND-gates, $v_J = v_o \sin 2\pi t/T$, neglecting the small forward drop across D_p. Thus, due to the buffering action of D_p, which absorbs the excess pull-up current, the signal into the receiving element is made insensitive to the logically irrelevant ways in which signals can arrive at the AND-gates.

7. It provides an effective means for driving the fan-out lead capacitance.

It is apparent from the foregoing that the inter-element coupling circuit is simply an AND-gate having the a-c power source, or "clock", as it is called, for one of its inputs. Fig. 51 shows how this AND-gate, drawn in heavy lines, is inserted between the core output and the logic load (close to the core and ahead of the lead fan-out) to provide, not only the current to reset the transmitting core, but also all the current required to charge the sometimes considerable total lead capacitance to ground. This gate is called the output AND-gate. It is necessary because the core has a high output impedance during the transmission of ONEs, and is therefore incapable of developing an acceptable signal across the lead capacitance. The current in R_{po} is made large enough to charge the strays at a rate at least as great as the maximum positive rate of change of the binary ONE signal. The strays are rapidly discharged through D_{po} during the negative half-cycle. The necessity for the output AND-gate is treated more fully in the section on factors affecting logical gain.

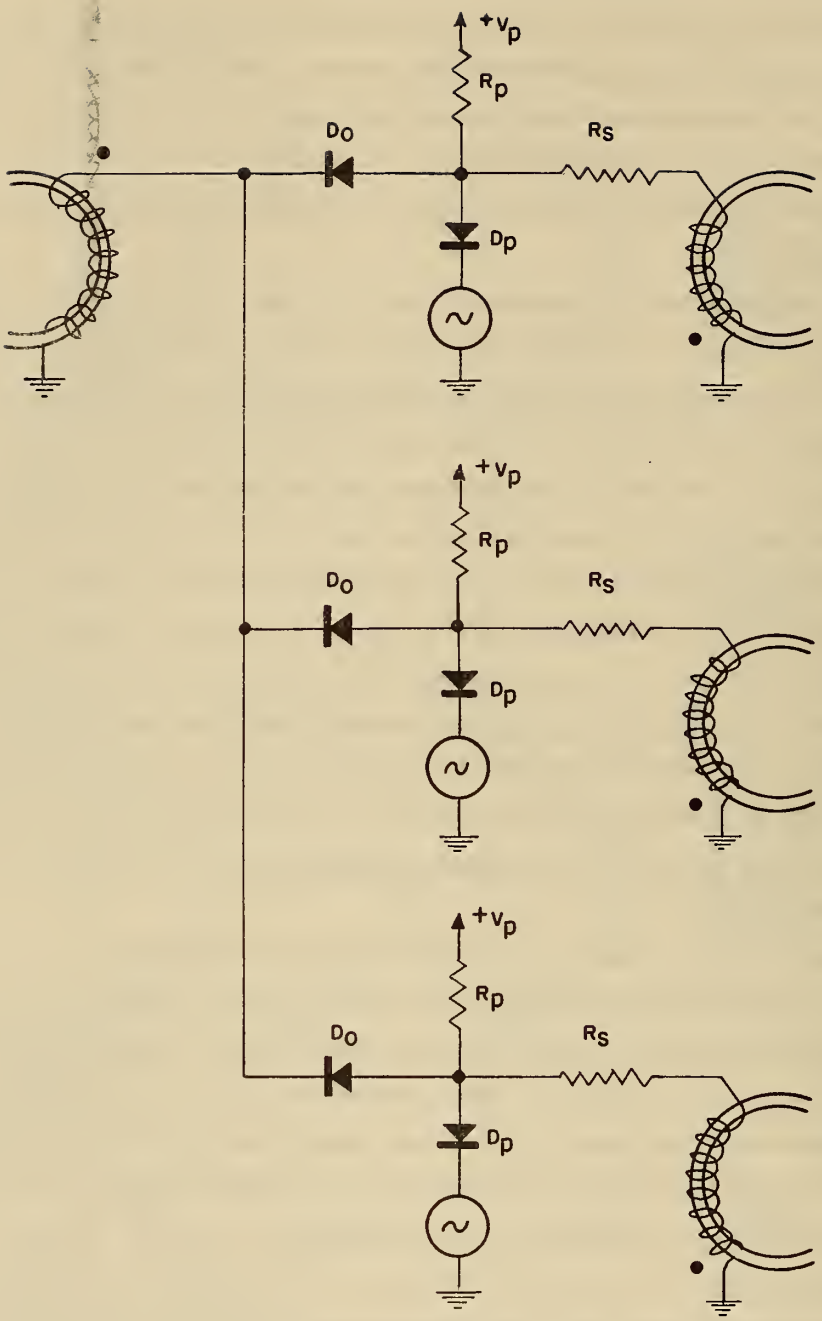


Figure 48. Signal branching from one core to three others

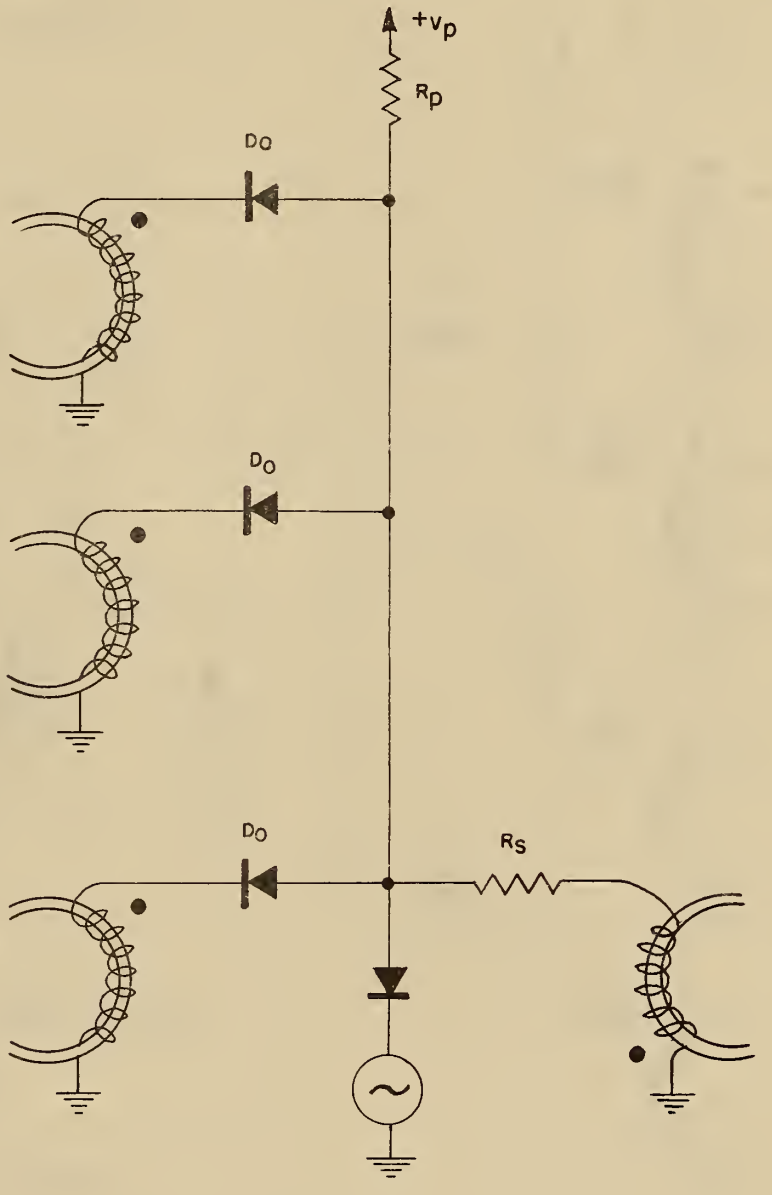


Figure 49. The inter-element coupling network as an AND-gate

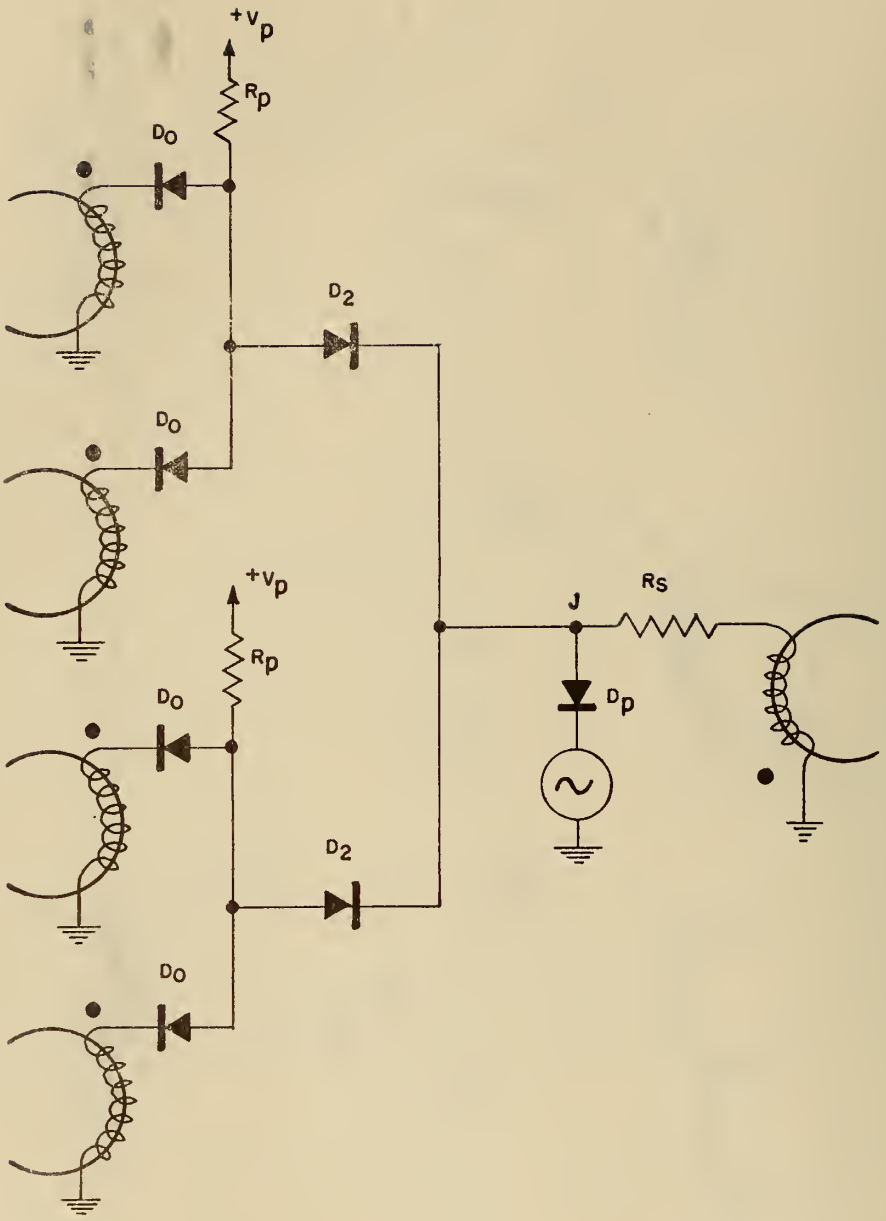


Figure 50. The inter-element AND-OR network

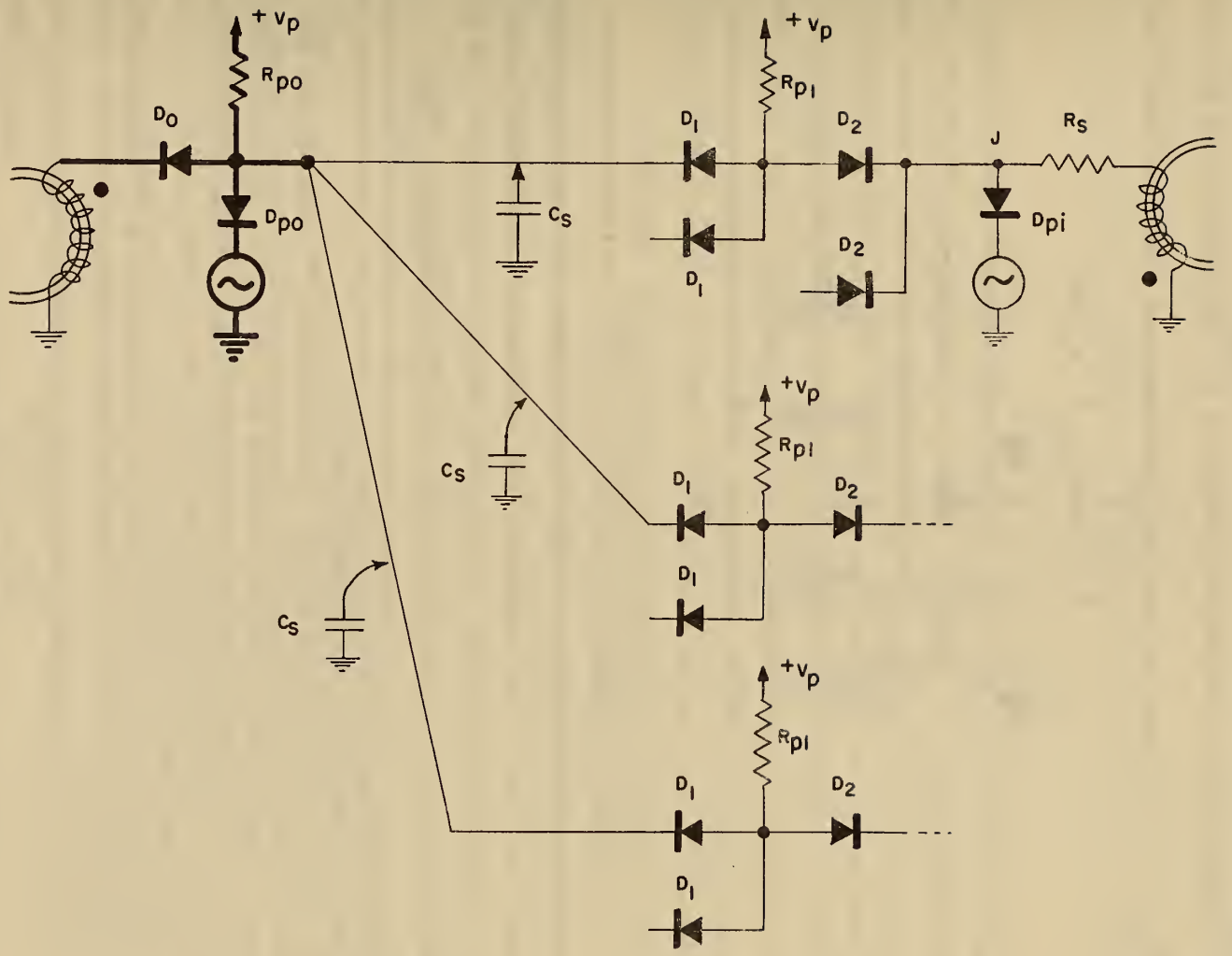


Figure 51. Inter-element logic network and the output (degenerate) and-gate

During the coupling half-cycle the signal input to the resistor-core computer element is simply $\int_o^{T/2} v_J\,(t)\,dt$, and the output of the preceding core is $\int_o^{T/2} v_K(t)\,dt$. Even for the case in which $\frac{n_2}{n_1}\frac{R_c}{R_s+R_c}\,v_o > v_o$, we have seen that $v_J(t) = v_K(t)$ throughout the coupling half-cycle. Therefore

$$\int_o^{T/2} v_J\,(t)\,dt = \int_o^{T/2} v_K\,(t)\,dt$$

during this half-cycle; or, in other words, the signal parameter transfer-function of the inter-element coupling circuit is $y = f(x) = x$. Therefore the signal propagation function for a cascade or a ring of resistor-core computer elements coupled by this circuit as shown in Fig. 46, depends solely on the transfer function of the elements themselves. This is also true for sequences in which the elements are connected by the logical networks developed from the basic coupling circuit. From this we may conclude that a working computer circuit has not yet been achieved, because, owing to the restriction (36) imposed by the coupling circuit, the resistor-core transfer characteristic cannot cross the unity gain line. The propagation function is ZERO-stable only, and ONES will not be preserved.

6. AN ATTEMPT TO ACHIEVE A SATISFACTORY ELEMENT TRANSFER-FUNCTION

Two ways out of this difficulty were tried. The first of these, which was only moderately successful, was to effect a slight improvement in the resistor-core transfer-function by increasing n_2/n_1 in violation of restriction (36). The second way, which proved very successful, but at the cost of an additional active component, made use of the fact that element groups that have satisfactory transfer functions can sometimes be formed from elements whose transfer-functions individually are inadequate for binary signal propagation.

The results of the first attempt have been reported elsewhere.[4] A three-bit ring was constructed of magnetic digital amplifiers resembling those in Figure 46, but with the addition of a small (approx. 1v.) low-impedance positive d-c supply $+B_1$ to which the lower terminal of each output winding was connected. See Fig. 52.

Instead of restriction (36) we have for this case, in order to prevent D_o from conducting during the negative half-cycle,

$$\frac{n_2}{n_1} \leq \frac{v_o + B_1}{v_{co}} \tag{52}$$

since $+B_1$ must be overcome before D_o can be forward-biased. Now, in general, the maximum slope of the resistor-core transfer function is

$$\left.\frac{dy}{dx}\right|_{T/4} = \frac{n_2}{n_1}\,\frac{v_{co}}{v_o}, \tag{53}$$

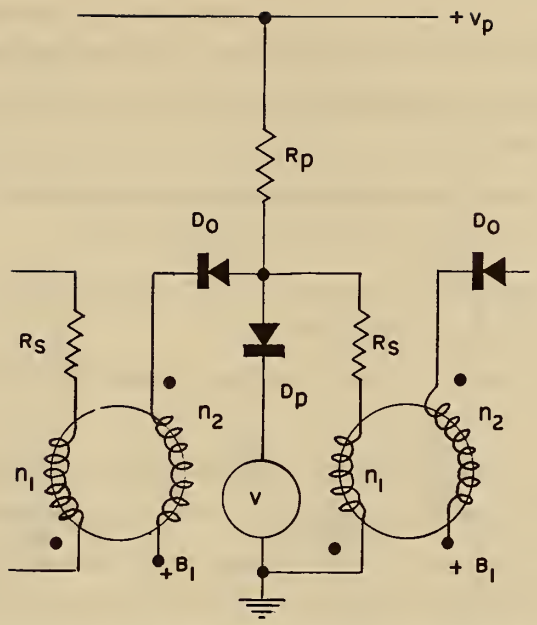


Figure 52. The use of a small series voltage source in an attempt to improve the magnetic element transfer-function

and this is equal to unity when restriction (36) is imposed. However, in the present case we impose (52) instead, with the result that the largest value for dy/dx is

$$\left.\frac{dy}{dx}\right|_{T/4} = \frac{v_o + B_1}{v_{co}} \cdot \frac{v_{co}}{v_o} = 1 + \frac{B_1}{v_o} > 1. \qquad (54)$$

In the experimental ring of amplifiers B_1/v_o could not much exceed 0.1, but results showed that $\frac{n_2}{n_1} \frac{v_{co}}{v_o}$ for this value could be as large as 1.2. This can be accounted for by the fact that approximately a volt of forward bias can be applied to D_o before appreciable current flows in it.

Because of their marginal volt-second transfer-characteristic these amplifiers could not tolerate much loading. Little increase in signal gain (transfer-function slope g) can be obtained by the use of $+B_1$ because it adds to v_K during the coupling half-cycle also, and reduces ZERO stability. This difficulty might be overcome by replacing $+B_1$ with a positive voltage half sine-wave occurring only during the decoupling half-cycle; but a low impedance source of this nature is difficult to realize.

7. THE ADDITION OF THE PEAK-SATURATING EMITTER-FOLLOWER PRODUCES A SATISFACTORY ELEMENT-GROUP TRANSFER-FUNCTION

We now turn to the second attempt to get a satisfactory signal propagation function. The solution occurred experimentally as the result of an attempt to get increased power gain through the inclusion of a transistor emitter-follower in the magnetic digital amplifier circuit already described. In addition to the possibility which it offers of improving the signal propagation function,

the emitter follower,

1. Provides power gain as current gain only, with a voltage gain near unity. This property makes it directly compatible with the resistor-core element which also amplifies solely through current gain.
2. Reduces the current required in the extensive inter-element diode logic network by providing current gain at a low input current level.
3. Reduces the proportion of a-c power to d-c power consumed by the circuit. d-c power is easier to generate and distribute.
4. Permits the design of a simple, economical negating amplifier having a delay of only 1/2 cycle.
5. Serves as a unilateral buffer to provide further isolation between the magnetic elements. It does this through its impedance transforming action whereby a high impedance is presented to the signal from the previous core and a low impedance is presented to the following core-resistor element. The emitter-follower is effectively unilateral when working, as it does in the Transmag circuit, between a signal source of low impedance relative to its own input impedance, and a load impedance which high relative to its own output impedance. (See the section on gain.)

All these advantages are purchased at the small price of one transistor and one (emitter-) resistor plus two additional d-c supply taps.* The price looks even smaller when it is realized that, with the relatively low source impedance and high load impedance presented to it, the emitter-follower has the following properties:

1. It is uncritical of transistor parameters (β, f_{ab})
2. It has a wide frequency range relative to f_{ab}
3. It is free from thermal drift.

Referring to Fig. 51 the emitter-follower was inserted into the circuit at the point J, just ahead of R_s. Figure 53 shows the resulting Transmag digital amplifier as it would be used in a simple cascade or ring, without inter-element logic. Notice that the input AND-gate (R_{p1}, D_1) has been omitted, but that the OR-gate D_2 (here degenerate) has been retained. The latter was found essential to the stable propagation of binary signals. D_2 permits the emitter follower to be operated in a manner such that it will produce satisfactory element-group transfer-functions when grouped with the resistor-core element. Here it should be pointed out that, when operated conventionally, the emitter-follower has a volt-second transfer function which is simply $y = x$. Therefore, in this mode of operation, it would be of no help in securing a satisfactory group transfer function.

In the mode of operation that proved successful, the transistor was driven into saturation momentarily at the peak of the ONE signal. The resulting base charge storage gave rise to signal

* And one more diode, in the case of the negating amplifier.

stretching, and this compensated for the signal curtailment caused by the core. Figure 54 shows the voltage-selective pulse-time stretching of the OR-diode driven emitter-follower in an experimental setup using a variable-amplitude input pulse from the low-impedance-generator G. A single-input AND-gate with an adjustable pull-up resistor R_p was used to provide a controlled limit to the current that could be delivered to the transistor base by the pulse. Short input pulses of

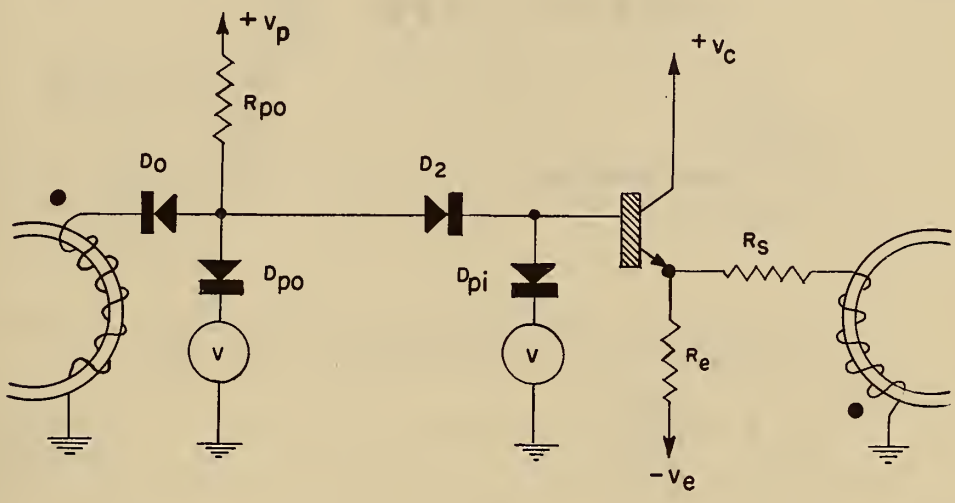


Figure 53. The transistor-magnetic core digital amplifier (Transmag)

fixed duration (between 0.1 and 0.2 μsec) but having the different amplitudes shown by 1, 2, 3 and 4, resulted in the outputs 1, 2, 3 and 4 shown. Longer input pulses resulted in roughly proportionately longer storage times. The pulse stretching factor depended upon the type of transistor used; and increased with the magnitude of the current in the AND-gate, and with the magnitude of R_c. High performance transistors (high β and f_{ab}) gave the greatest stretching factors. Values ranging from 3 to 10 were observed.

The amount by which a pulse was stretched was proportional to the voltage-time area of that portion of the input pulse that exceeded the collector potential. With the collector held at 10 volts the ratio between the input area increment, above 10 volts, and the output area increment could be as high as 50. This is shown in Fig. 55, in which the ratio of the shaded area to the dark area is 50:1. A plot of the voltage-time area of the output of the emitter follower as a function of that of a 0.2 μsec input pulse, whose height is varied, is shown in Fig. 56. Observe that the vertical scale is ten times that of the horizontal scale. The plot shows a volt-second gain of unity until the input pulse height reaches the collector voltage (10v). The slope of the curve from 2 volt-μsec to 2.4 volt-μsec is 50. Above this it drops rapidly to zero corresponding to a maximum possible base charge storage for the particular value of pull-up current used.

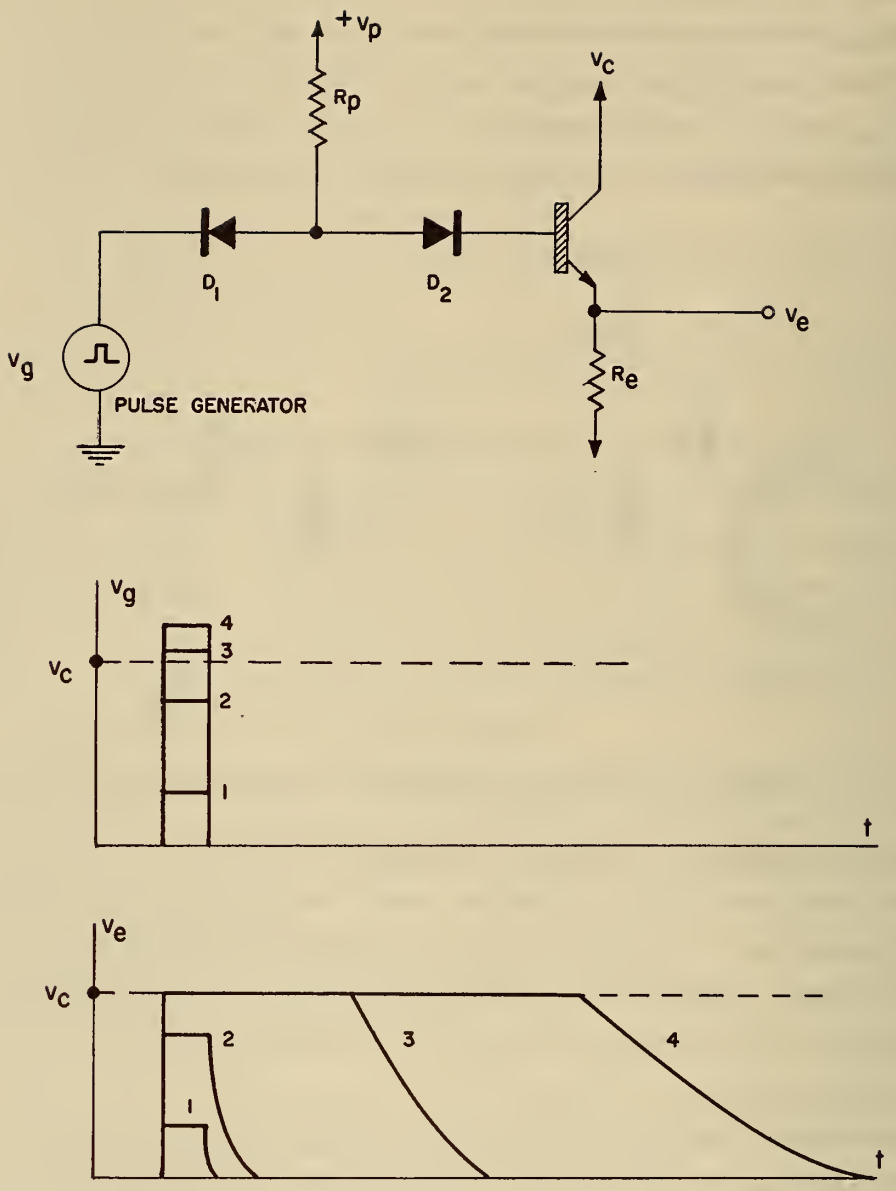


Figure 54. The pulse stretching property of the OR-diode coupled-, peak-saturating emitter follower

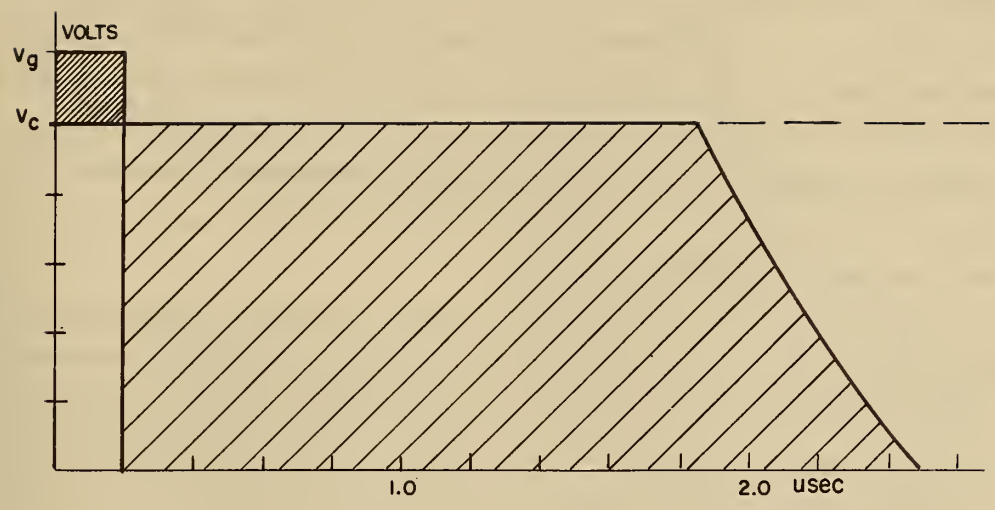


Figure 55. Large ratio of pulse output area-increment (shaded) to pulse input area-increment (dark) above collector-voltage V_c

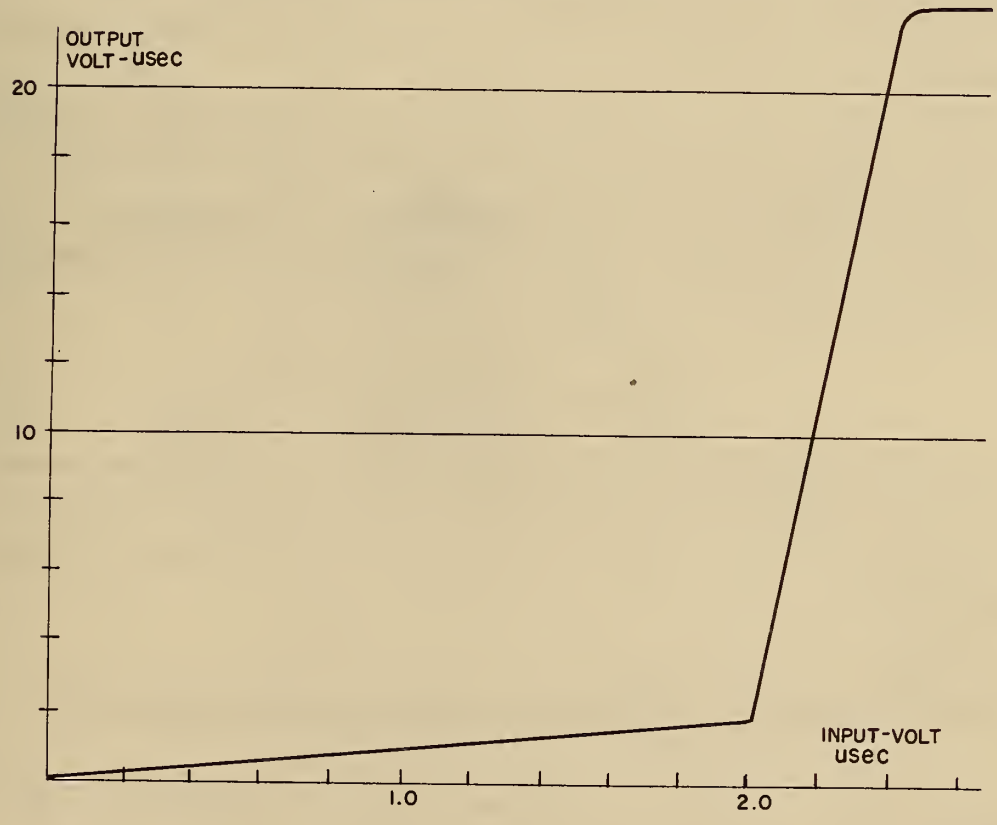


Figure 56. Voltage-time-area of the emitter-follower output pulse versus the area of a 0.2 μsec input pulse of variable height. $V_c = 10_v$

The explanation of this voltage-amplitude-selective pulse stretching is that, for base potentials below that of the collector, few if any minority carriers are stored in the base, and the transistor behaves in the normal manner. But the moment the base potential exceeds that of the collector the base-collector junction is forward-biased and the base soon draws the full pull-up current in R_p. The transistor is said to be saturated. During saturation the base accumulates charge carriers, which remain trapped in it when the input pulse returns to zero, opening D_2. The transistor then continues to conduct until these carriers have been dissipated.

The signal stretching of the circuit in Fig. 53 is accomplished in similar fashion. In the latter case the input signal is either a large or a small portion of the clock half-sine wave, depending upon whether a ONE or a ZERO is received. The collector supply voltage V_c is made somewhat less than $+v_o$. As a result, signals that terminate before the sine wave has reached the value $v = V_c$ are transmitted nearly unchanged by the emitter follower. But signals that permit the base potential to exceed V_c, even momentarily, are stretched in time. In this circuit these signals are transmitted by the emitter-follower as a full half sine wave, the trailing edge being shaped by the clock through the input power-diode D_{pi}. Fig. 57 shows the selective reshaping produced by the clocked saturating diode-driven emitter follower. The trailing edge of the ONE, if "unclocked", is shown by the dashed line.

We now wish to derive the volt-second transfer function for the clocked saturating diode-driven emitter-follower. Referring to Fig. 58 in which the partial sine-wave shown by the solid line represents a typical ONE signal voltage at the input to the OR-diode, it is seen that for $o < t < t_o$ the emitter-follower transfer-function is simply $y = x$ because the base potential in this range is less than V_c. Then, to find $y = f(x)$ for $t > t_o$, where

$$\frac{2\pi t_o}{T} = \arcsin \frac{V_c}{v_o} , \tag{55}$$

we observe that during the early part of this interval, when $(t - t_o)/T$ is small, the base potential exceeds V_c, and carrier storage proportional to the black area $\Delta_2 x$ takes place. To calculate the effect of this storage on the transfer-function $x(t)$ is expanded in a power series in $t - t_o$, by means of the Taylor expansion,

$$x(t) = x(t_o) + \dot{x}(t_o)(t - t_o) + \frac{1}{2!}\ddot{x}(t_o)(t - t_o)^2 + \frac{1}{3!}\dddot{x}(t_o)(t - t_o)^3 + \text{etc.}$$

$$= x_o + v_o (t - t_o) \sin 2\pi \frac{t_o}{T} + v_o \left(\frac{\pi}{T}\right)(t - t_o)^2 \cos 2\pi \frac{t_o}{T} - 2/3\, v_o \left(\frac{\pi}{T}\right)^2 (t - t_o)^3 \sin 2\pi \frac{t_o}{T} + \text{etc.} \tag{56}$$

where $v_o (t - t_o) \sin 2\pi \frac{t_o}{T} = \Delta_1 x$ in Figure 58, and where the sum of the remaining terms equals $\Delta_2 x$. Dividing by $v_o T/\pi$, the area of the half sine wave, we have

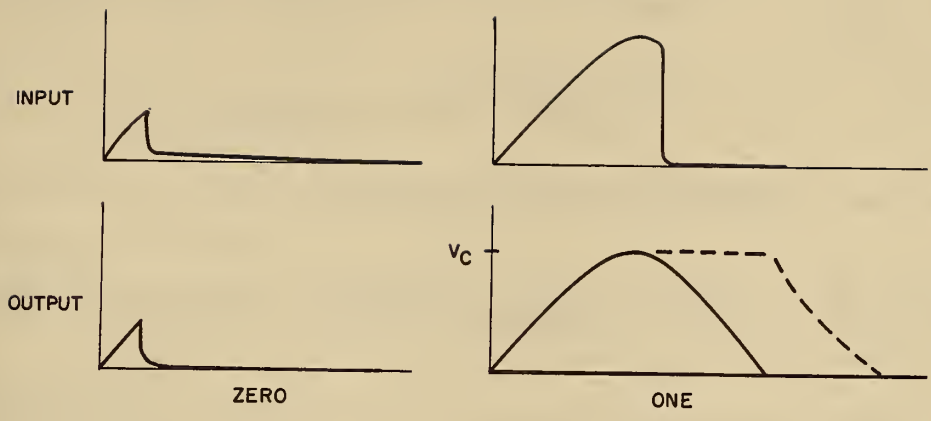


Figure 57. Selective signal reshaping produced by the clocked saturating diode-driven emitter-follower

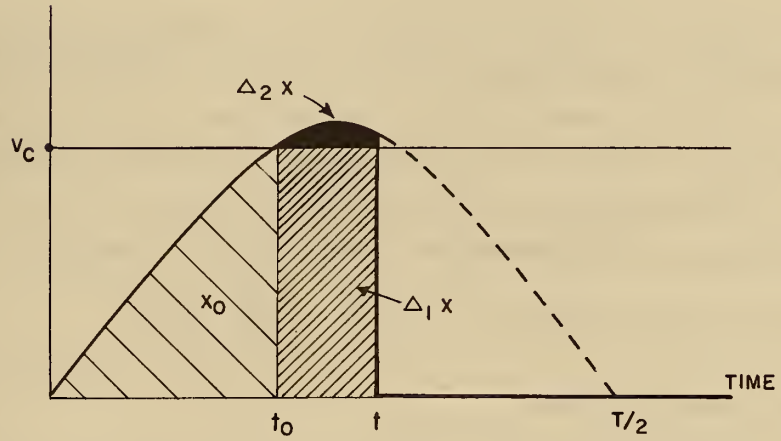


Figure 58. Diagram used in deriving the volt-second transfer function of the diode-driven, saturating emitter-follower

$$\frac{x}{v_o\, T/\pi} = \frac{x_o}{v_o\, T/\pi} + \frac{v_o(\sin 2\pi\, t_o/T)(t - t_o)}{v_o\, T/\pi} + \frac{v_o^2\,(\sin 2\pi\, t_o/T)^2\,(t - t_o)^2}{(v_o T/\pi)^2} \cdot \frac{\cos 2\pi\, t_o/T}{\sin^2 2\pi\, t_o/T}$$

$$- 2/3\, \frac{v_o^3\,(\sin 2\pi\, t_o/T)^3\,(t - t_o)^3}{(v_o T/\pi)^3} \cdot \frac{1}{\sin^2 2\pi\, t_o/T} + \text{etc.} \qquad (57)$$

Or, in terms of $\Delta_1 x$, and dropping all terms after the fourth,

$$\frac{x}{v_o\, T/\pi} \simeq \frac{x_o}{v_o\, T/\pi} + \frac{\Delta_1 x}{v_o\, T/\pi} + \frac{1}{\sin^2 2\pi\, t_o/T}\left[\left(\frac{\Delta_1 x}{v_o\, T/\pi}\right)^2 \cos 2\pi\, t_o/T - 2/3\left(\frac{\Delta_1 x}{v_o\, T/\pi}\right)^3\right] \qquad (58)$$

For simplicity, if we measure the signal parameters in units of $v_o\, T/\pi$ and denote these numbers by X and Y to indicate that fact, then

$$X = \frac{x}{v_o\, T/\pi} \qquad (59a)$$

$$Y = \frac{y}{v_o\, T/\pi}\,, \qquad (59b)$$

and

$$X = X_o + \Delta_1 X + \frac{1}{\sin^2 2\pi\, t_o/T}\left[(\Delta_1 X)^2 \cos 2\pi\, t_o/T - 2/3\,(\Delta_1 X)^3\right] = X_o + \Delta_1 X + \Delta_2 X \qquad (60)$$

If we now identify $\Delta_2 x$, and therefore $\Delta_2 X$, with the dark area of Fig. 55, then the constant of proportionality G, which gives the ratio of the shaded area to the dark area in Fig. 55, multiplied by $\Delta_2 X$, gives the increase in the emitter-follower output voltage-time integral $\int_o^{T/2} v_{E.F}(t)\, dt$ over its input voltage-time integral $\int_o^{T/2} \frac{n_2}{n_1} v_c(t)\, dt$ received from the previous core. Thus

$$Y = X_o + \Delta_1 X + G\Delta_2 X = X_o + \Delta_1 X + \frac{G}{\sin^2 2\pi\, t_o/T}\left[(\Delta_1 X)^2 \cos 2\pi\, t_o/T - 2/3\,(\Delta_1 X)^3\right] \qquad (61)$$

Then starting at the point $X = X_o$, $Y = X_o$, we may plot $\Delta Y = Y - X_o$ as a function of $\Delta X = X - X_o = \Delta_1 X + \Delta_2 X$. This is simplified by the fact that for small $\Delta_1 X$ and for t_o near T/4, the region of interest, $\Delta_2 X$ is small compared with $\Delta_1 X$.

Therefore we may instead plot

$$\Delta Y = \Delta_1 X + \frac{G}{\sin^2 2\pi t_o/T} \left[(\Delta_1 X)^2 \cos 2\pi t_o/T - 2/3 (\Delta_1 X)^3 \right]$$

$$\simeq \Delta X + \frac{G}{\sin^2 2\pi t_o/T} \left[(\Delta X)^2 \cos 2\pi t_o/T - 2/3 (\Delta X)^3 \right] \quad (62)$$

and add it to the portion $Y = X$ for $0 \leq X \leq X_o$ to get graph which represents

$$Y = \begin{cases} X, \text{ for } 0 \leq X \leq X_o \\ X + \dfrac{G}{\sin^2 2\pi t_o/T} \left[(X - X_o)^2 \cos 2\pi t_o/T - 2/3 (X - X_o)^3 \right] \end{cases} \quad (63a)$$

for positive small $X - X_o$.

This graph is shown by curve 2 in Fig. 59 for $G = 50$, and for

$$\frac{V_c}{v_o} = \sin 2\pi t_o/T = .90.$$

Because of the reshaping provided through D_{pi}, Y cannot exceed unity. (y cannot exceed $v_o T/\pi$). Therefore the true transfer functions, as shown by the solid curves, include the line $Y = 1$. Acceptable values of G will produce curves of sufficient slope that $Y = 1$ for small $X - X_o$. Therefore equation (63a), with the restriction $Y \leq 1$, is a good approximation to the transfer-function of the clocked saturating diode-driven emitter-follower. It may be written alternatively as,

$$Y = \left\{ \begin{cases} X, \text{ for } 0 \leq X \leq X_o \\ X + \dfrac{G}{V_c^2/v_o^2} \left[(X - X_o)^2 \sqrt{1 - \dfrac{V_c^2}{v_o^2}} - 2/3 (X - X_o)^3 \right] \end{cases} \right\} \leq 1, \quad (63b)$$

$$\text{where } X_o = 1/2 \left[1 - \sqrt{1 - \frac{V_c^2}{v_o^2}} \right] \quad (64)$$

Curve 1 in Figure 59 is the transfer-function of the resistor-core element actually used in the experimental Transmag circuit. It is seen that neither curve 1 nor curve 2 crosses the unity gain line in the required three points O, R and S. Therefore we wish to know whether their group transfer functions satisfy this requirement. Calling the resistor-core transfer function $f_1(X)$ and the emitter follower transfer function $f_2(X)$ we can obtain $f_{12}(X)$, $f_{21}(X)$, r_{12}, s_{12}, r_{21}, and s_{21} by superimposing the graphs of $f_1(X)$ and $f_2(X)$ as was done for the vacuum tube flip-flop. See Figure 21. In Figure 60 the dashed curves show two possible functions $f_1(X)$, corresponding to two different values of core turns ratio n_2/n_1, superimposed in the manner of Figure 21 upon four solid curves representing possible emitter-follower functions $f_2(X)$ resulting from different values of V_c/v_o and G. Two group transfer-functions, $f_{12}(X)$ and $f_{21}(X)$, can be

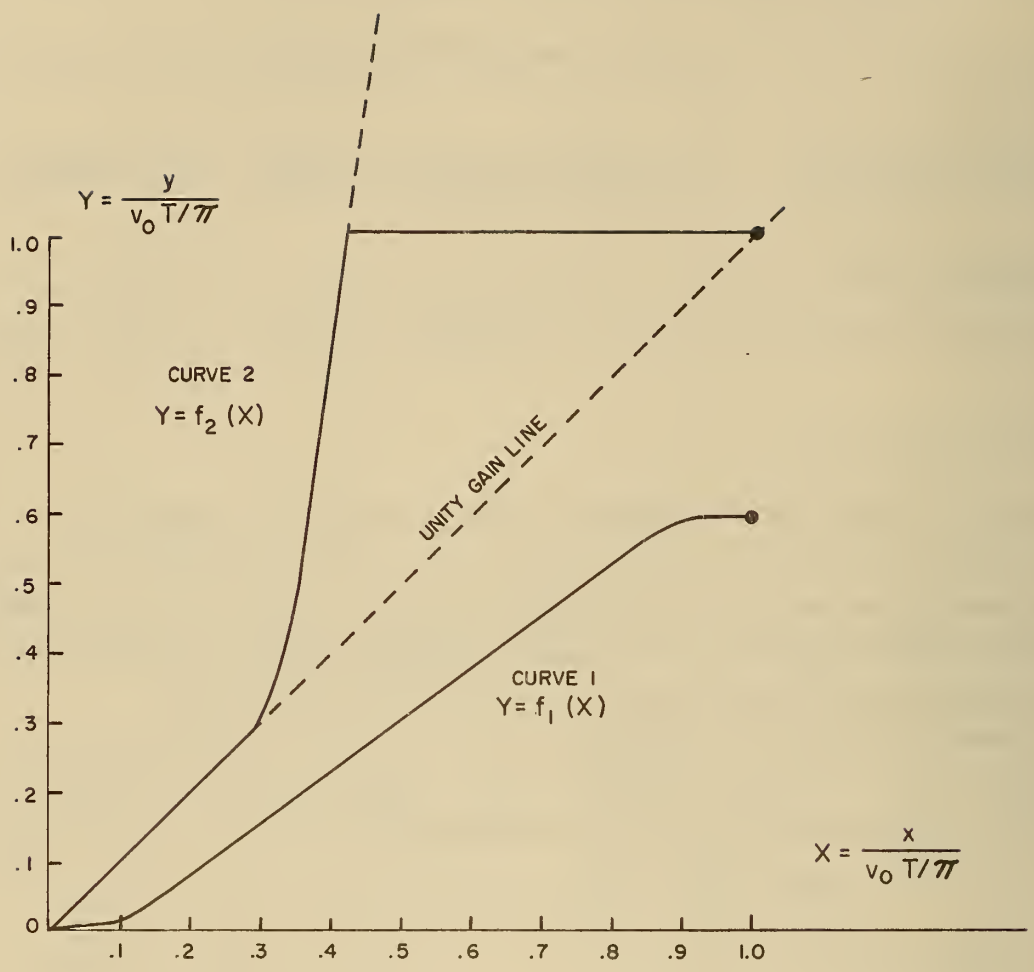


Figure 59. Volt-second transfer-function of the resistor-core element (curve 1) and of the peak-saturating emitter-follower (curve 2)

plotted for each intersecting pair of curves using values easily obtained graphically from the figure. The coordinates of the points of second intersection of $f_1(X)$ and $f_2(X)$ give $r_{12}/\frac{v_o T}{\pi}$ and $r_{21}/\frac{v_o T}{\pi}$ directly, the former being the ordinate and the latter being the abscissa. Similarly, $s_{12}/\frac{v_o T}{\pi}$ and $s_{21}/\frac{v_o T}{\pi}$ are given by the coordinates of the points of third intersection of these functions, shown by the small circles.

For example, if $V_c/v_o = 0.90$ and $G = 25$; and if $n_2/n_1 = 2$, $R_c = 750$ ohms, $R_s = 470$ ohms, and $m = 0.36$, then

$$r_{12} = 0.67\ (v_o T/\pi)$$
$$r_{21} = 0.42\ \text{"}$$
$$s_{12} = 1.00\ \text{"}$$
$$s_{21} = 0.60\ \text{"}$$

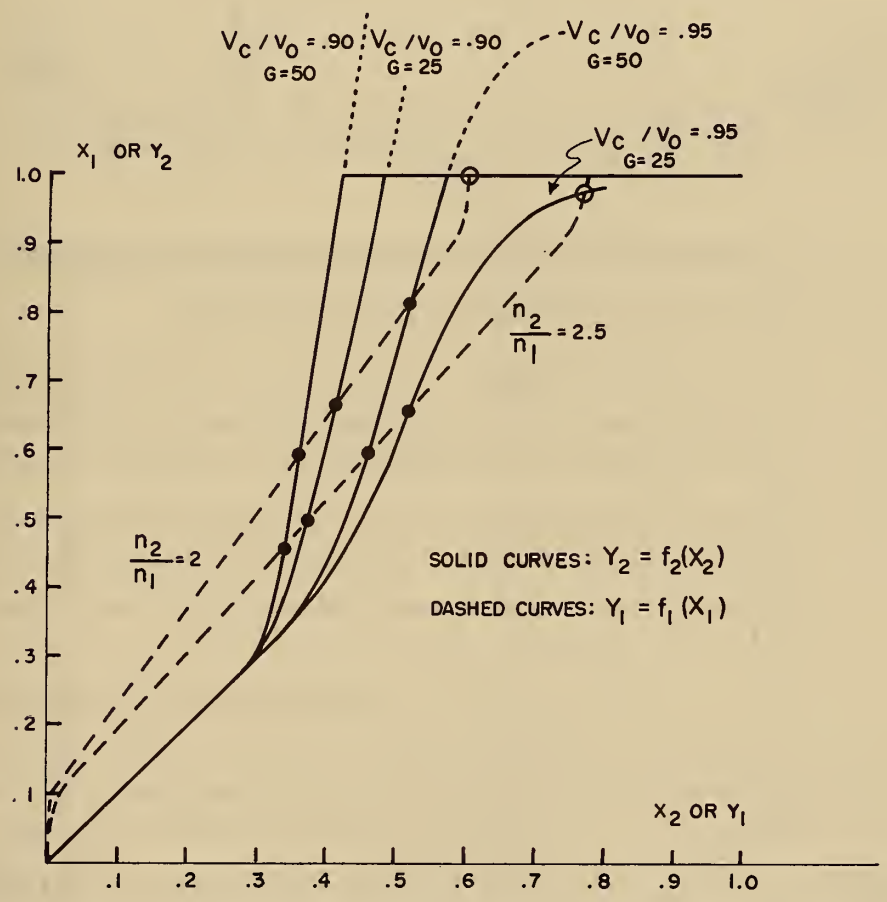


Figure 60. Superposition of magnetic-element and transistor-element transfer-functions to obtain values of r and s for the element-group transfer functions

This case is typical of the Transmag circuit that was experimentally arrived at. Its steady-state total propagation function $\phi^{\infty}(X)$ is shown in Figure 61 and its element-group transfer functions $f_{12}(X)$ and $f_{21}(X)$ are shown in Figure 62.

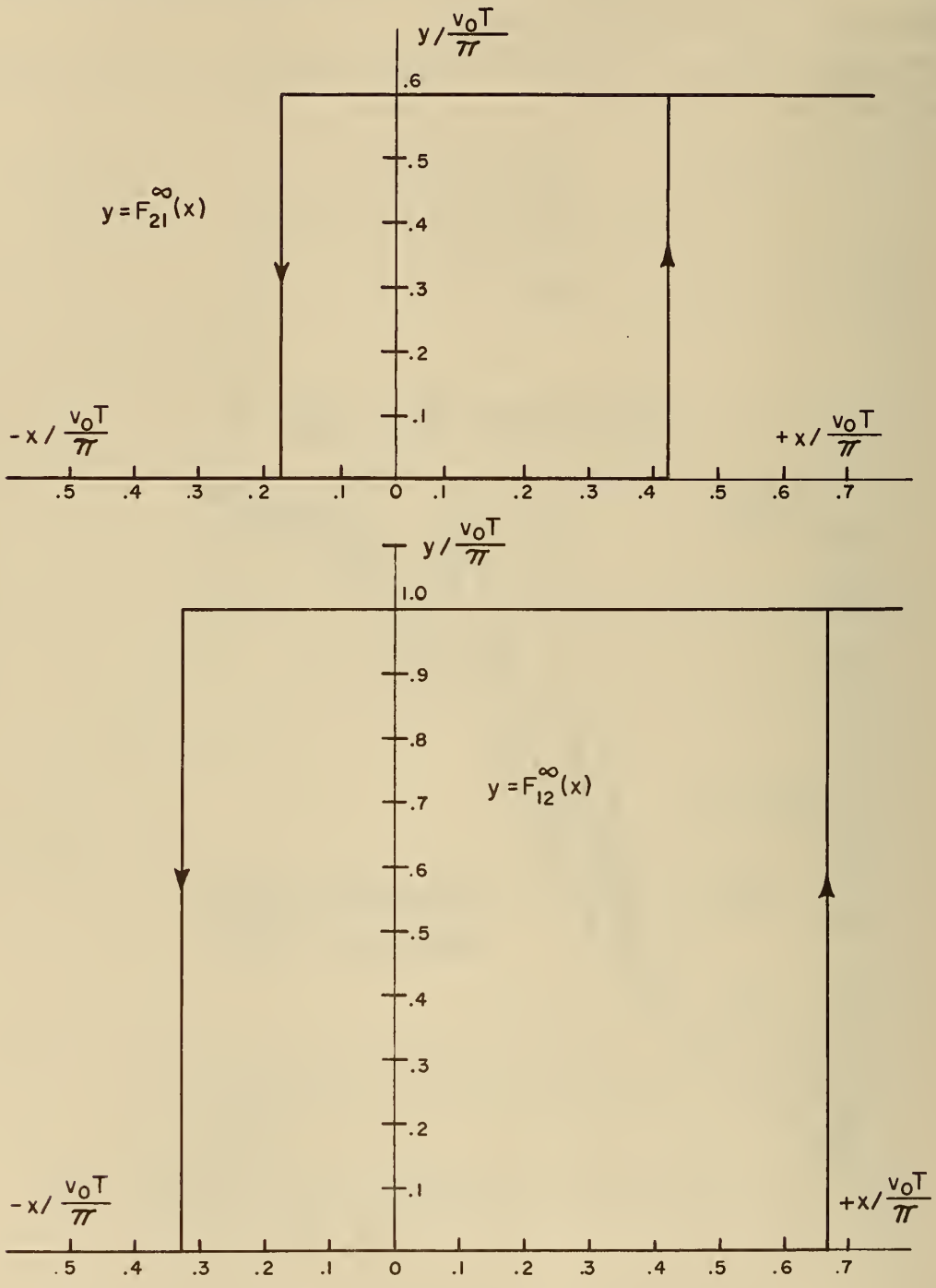


Figure 61. a. The steady-state propagation function for the transistor-core element-group, and
b. For the core-transistor element-group

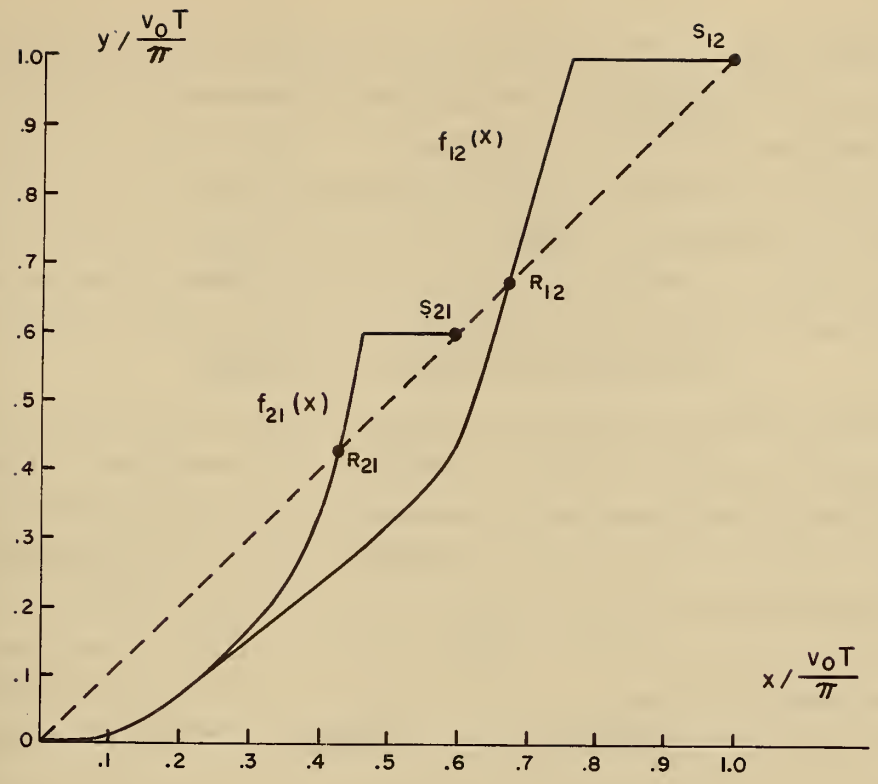


Figure 62. Transistor-core transfer-function $f_{21}(x)$, and core-transistor transfer-function $f_{12}(x)$ constructed graphically from Figure 60

We know that stable binary signal propagation results for this case because the group transfer functions intersect the unity gain line at O, R and S. In the case of the curves corresponding to $V_c/v_o = 0.95$, $G = 25$ and $n_2/n_1 = 2$, $f_1(X)$ and $f_2(X)$ intersect only at the origin, therefore the resulting group transfer functions fail to intersect the unity-gain line anywhere except at O, and stable binary signal propagation is impossible. However, with the same emitter-follower transfer-function (which is poor in this case) stable signal propagation can be restored by increasing the core turns-ratio to 2.5, as is shown in Figure 60. $n_2/n_1 = 2.5$ is the largest turns-ratio permitted by restriction (36) for the particular values of R_s, R_c, and m used.

For maximum stability against extraneous noise s_{12} and s_{21} should be as large as possible, and r_{12}/s_{12} and r_{21}/s_{21} should equal 1/2. In terms of Figure 60, this means that the points of third intersection (the small circles) should come as close to X = 1, Y = 1 as possible, and that the points of second intersection (black dots) should come close to $X = 1/2\,(s_{21}/\frac{v_o T}{\pi})$, $Y = 1/2\,(s_{12}/\frac{v_o T}{\pi})$. It is seen that these conditions are pretty well fulfilled for the cases $V_c/v_o = 0.90$; $25 \leq G \leq 50$; $n_2/n_1 = 2$, which approximate the experimentally achieved parameters. Some improvement could have been made by increasing the turns-ratio to 2.5.

Stability against changes in $f_1(X)$ and $f_2(X)$ is best when these curves intersect each other at the largest possible angle when superimposed. This minimizes the dislocation of the intersection points with changes in the transfer-functions. Thus the ideal form for $f_1(X)$ and $f_2(X)$ from the point of view of stability to changes in $f_1(X)$ and $f_2(X)$, and for maximum noise thresholds, is the unit-step at $X = 1/2$. This is also the ideal form for binary signal propagation. However, a transfer-function approximating this shape is so difficult to achieve in practice that it is useful to know that functions that depart widely from it, such as those in Figure 59, can provide good signal propagation.

8. THE EXCLUSION OF MARGINAL SIGNALS

The chief difficulty with non-ideal element transfer functions lies in the low value of signal gain g, which the group transfer-functions may have. In Section 2.2 it was shown that, if the propagation function figure of merit g^m is not large, then, in the presence of noise, the clearly-defined steady-state propagation function $F^\infty(x)$, having the full thresholds r and -(s-r), is replaced by the random collection of propagation functions shown in Figure 14, which represents $y = f^\infty\left[f^m(\xi) + x \right]$ for equally likely values of ξ between 0 and s. For equally probable values of ξ between 0 and s noise thresholds of any magnitude from zero up to, but not including, r and s-r are equally likely; and the probability that a threshold will differ from r and -(s-r) increases as g^m decreases. This arises from the fact that $f^m(\xi)$ has the form shown in Figure 12a for $f^n(x)$, from which it is seen that, for equally likely ξ, the ratio of the number of signals that can result in values of $f^m(\xi)$ that are different from 0 or s, to the totality of signals lying between 0 and s is $1/g^m$. Furthermore, it is evident that all values of $f^m(\xi)$ resulting from these signals are equally likely.

However, if we change the amplitude distribution of signals only so as to exclude those having values within the range $r - \gamma < \xi < r + \sigma$, in Figure 63, then $f^m(\xi)$ may have values only outside the range $r - \gamma g^m < f^m(\xi) < r + \sigma g^m$, and the probability that $f^m(\xi)$ will have a value different from 0 or s becomes

$$\frac{\frac{s}{g^m} - (\gamma + \sigma)}{s - (\gamma + \sigma)} \tag{65}$$

which can even be made zero if $\gamma + \sigma \geq \frac{s}{g^m}$.

This shows that even though g^m may not be large, it is possible to achieve the ideal steady state propagation function $F^\infty(x)$ for a system of non-ideal computer elements by the proper choice of γ and σ --- in other words by the exclusion of a sufficient range of signal amplitudes in the neighborhood of r.

But even if a smaller range $\gamma + \sigma$ is chosen, signals within this range are forbidden, so that the thresholds in $y = f^\infty\left[f^m(\xi) + x \right]$ can never be zero. Thus this function might appear as in Figure 64 rather than as in Figure 14. The probability density within the uncertain regions in Figure 64 is given by (65).

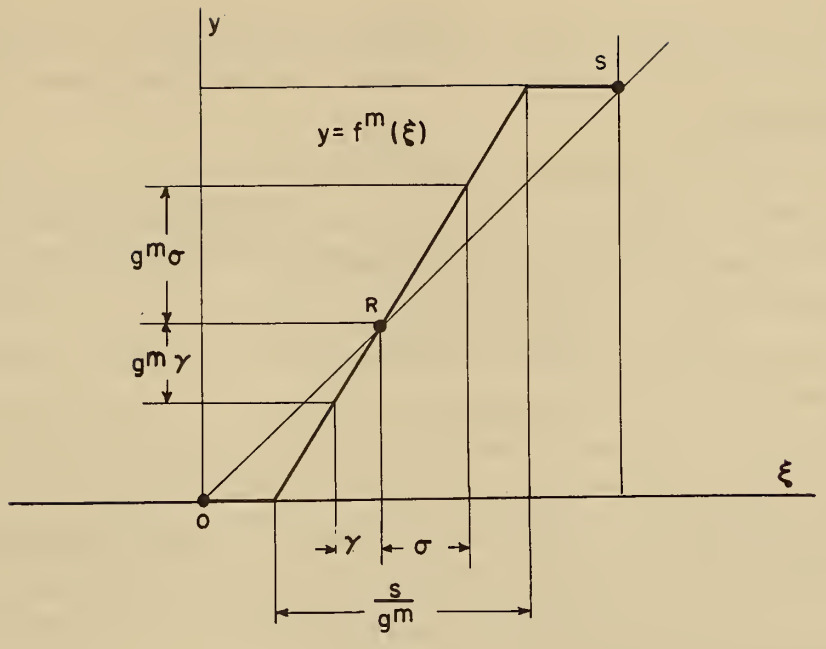


Figure 63. Ranges γ, σ of signal amplitudes to be excluded from the computer network

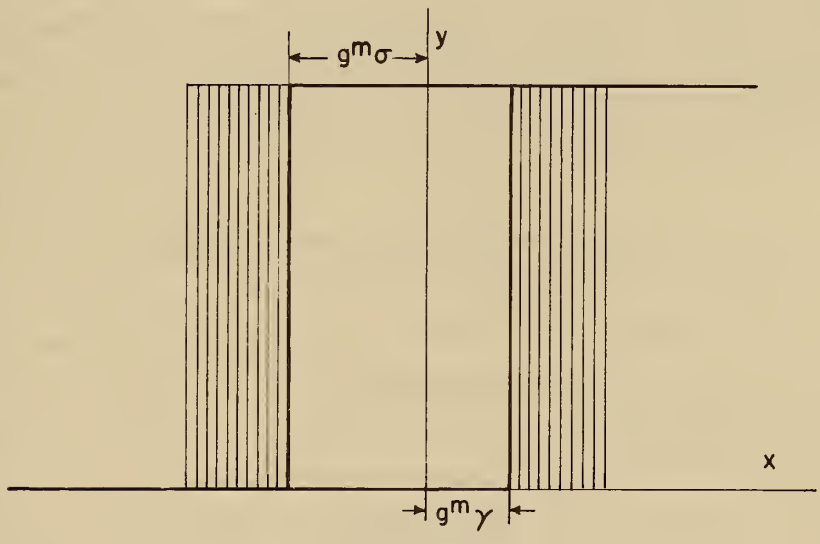


Figure 64. $Y = f^{\infty}\left[f^m(\xi) + X\right]$ when $g^m\gamma$ and $g^m\sigma$ do not include all imperfect signals

The above reasoning has been based on an assumed ideal form for $f^m(\xi)$ such as is shown for $f^n(x)$ in Fig. 12a. This assumption is reasonable, even for a poorly shaped $f(\xi)$, if $m \geq 3$.

8.1 The Synchronizer

In practice the task of prohibiting signals in the unwanted range $r - \gamma < \xi < r + \sigma$ is given to the input buffer or synchronizer. The basic problem in the design of this device centers around the fact that no value of ξ may be excluded, and therefore g^m must be extremely large to guarantee that a propagation function other than $F^\infty(x)$ will be sufficiently improbable. In the synchronizer a signal, which may have any amplitude ξ, is introduced into a storage and regeneration device coincident with a fully synchronized timing signal. Subsequent to this event the signal is allowed to propagate undisturbed in the regeneration device, which is a ring of element groups, until a second timing signal releases it to the computer. The probability that this signal will have a magnitude different from zero or s upon its release is $1/g^m$ where g is the signal gain (slope of the transfer function at R) of each element-group in the ring, and m is the number of transmissions the signal has experienced in the ring before being released to the computer. See Appendix V.

8.2 The Maximum Acceptable Signal Input Frequency $\hat{f}_i$

If a maximum value of $1/g^m$ is decided upon, then g and the element-group delay time t_d* determine the maximum rate at which unsynchronized signals may be accepted. The shortest permissible time between incoming signals obviously cannot be less than the storage time mt_d in the regeneration ring, and is in fact $2\,mt_d$ in a conventional synchronizer. The maximum acceptable signal input frequency is therefore

$$\hat{f}_i = \frac{1}{2mt_d} \tag{66}$$

Then letting p be the maximum acceptable synchronizer failure probability, we set

$$p = 1/g^m \tag{67a}$$

from which

$$m = -\log p/\log g, \tag{67b}$$

and the maximum signal input frequency is then

$$\hat{f}_i = \frac{1}{2(-\log p/\log g)t_d}$$

$$= \frac{\log g}{-2t_d \log p} \tag{68a}$$

In an n-phase system $t_d = T/n$, where T is the element-group cycle time; therefore in terms of the cycle time,

* t_d is the time between the reception of the signal by an element-group and its reception by the next group in the sequence. Thus it includes the time spent by the signal in delay lines inserted between the groups in some circuits.

$$\hat{f}_i = \frac{n \log g}{-2T \log p} \tag{68b}$$

or

$$\hat{f}_i = \frac{n f_c \log g}{-2 \log p} \tag{68c}$$

where f_c is the system "clock" frequency.

In the case of the experimental Transmag circuit n = 2, $g \simeq 3$, and f_c = 300 kc. $\hat{f}_i$ for this system is therefore

$$\hat{f}_i = \frac{2 \times 3 \times 10^5 \times (.47)}{-2 \log p}$$

$$= 1.4 \times 10^5 \text{ cps}/-\log p \tag{69}$$

Then if we choose $p = 10^{-10}$, $\hat{f}_i$ becomes 14 kc.

To achieve the error probability of 10^{-10}, equation (67b) shows that 20 transmissions of the signal by the element groups in the regeneration ring are needed. The product $p\hat{f}_i$ gives the probable maximum synchronizer error-rate to be one error every eight (24 hr.) days.

In the small computer built to test the performance of the Transmag circuit the synchronizer was timed to give m = 8. Therefore, for this synchronizer, $p = 10^{-4}$, by equation (67a) or (67b) with $g \simeq 3$. When unsynchronized start pulses were fed to the synchronizer at a rate of 10 kc, the computer made 80 errors during an 80-second interval, and 80 errors during another interval of 85 seconds. This compares well with the theoretical error-rate $pf_i = (10^{-4})(10^4 \text{ cps}) = 1$ error per second. That these errors originated in the synchronization process was demonstrated by the fact that when the computer was self-triggered at a rate of approximately 30 kc, no errors occurred during a 3-hour interval of observation.

9. THE TRANSMAG NEGATING AMPLIFIER

In the Transmag circuit, the logical operations AND and OR are performed conventionally by diode switching ahead of the emitter-follower. The NOT function is achieved by an almost trivial modification of the core input circuit. The Transmag NOT amplifier is shown in Figure 65 (Compare it with Figure 53). In this amplifier the "clock" is connected to one terminal of the core input winding so as to set the core in the ONE state during each receive-interval. The other terminal of the input winding is connected through R_s to the emitter. A diode clamp D_c holds the emitter at ground when ZEROs are present at the emitter follower input because R_e has been made low enough to provide a clamping current which exceeds the largest value of current drawn by the core during the receive-interval. The core then, being continually set by the "clock", transmits ONEs. But, upon the arrival of a ONE at its input, the emitter-follower generates sufficient current to open the diode clamp, and the resulting emitter signal opposes the "clock" voltage, leaving the core in the ZERO state. The core then transmits a ZERO.

In case both the negation and the assertion of the same signal are desired, a NOT-amplifier and an assertive amplifier can be connected in parallel as is shown in Figure 66. Or, a saving in components and a reduced collector dissipation results from the connection shown in Figure 67.*

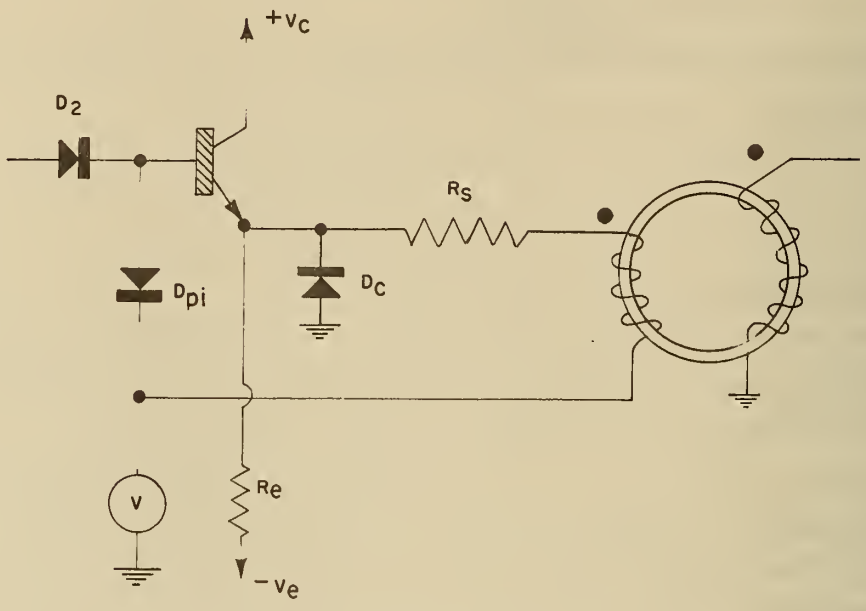


Figure 65. The negating amplifier

To get the volt-second transfer-function of the NOT-amplifier we first observe that the transfer-function of the saturating emitter-follower remains unchanged. It is therefore only necessary to get the transfer-function of the negating resistor-core element. In Figure 68 the negative waveform shown by the heavy line represents the signal voltage at the emitter during the receive-interval. The polarities of the voltages shown indicate the polarity of the flux change they tend to produce in the core, and are not the polarities with respect to ground. The voltage-time-area x of the emitter wave is the input signal to the negating resistor-core element. The full positive half-sine wave shown is the clock voltage which is applied to the un-dotted input terminal of the core. The positive waveform shown by the upper heavy line in Figure 68 represents the voltage applied to the resistor-core element during the receive-interval. It is the difference between the clock wave and the emitter wave. v_c is the voltage applied to the core input winding during the receive-interval, and the resultant volt-second output of the negating core during the ensuing transmit interval is given by

$$\frac{n_2}{n_1} \int_0^{T/2} v_c \, dt = \frac{n_2}{n_1} A_2 = y_n \qquad (70)$$

* See Appendix VIII.

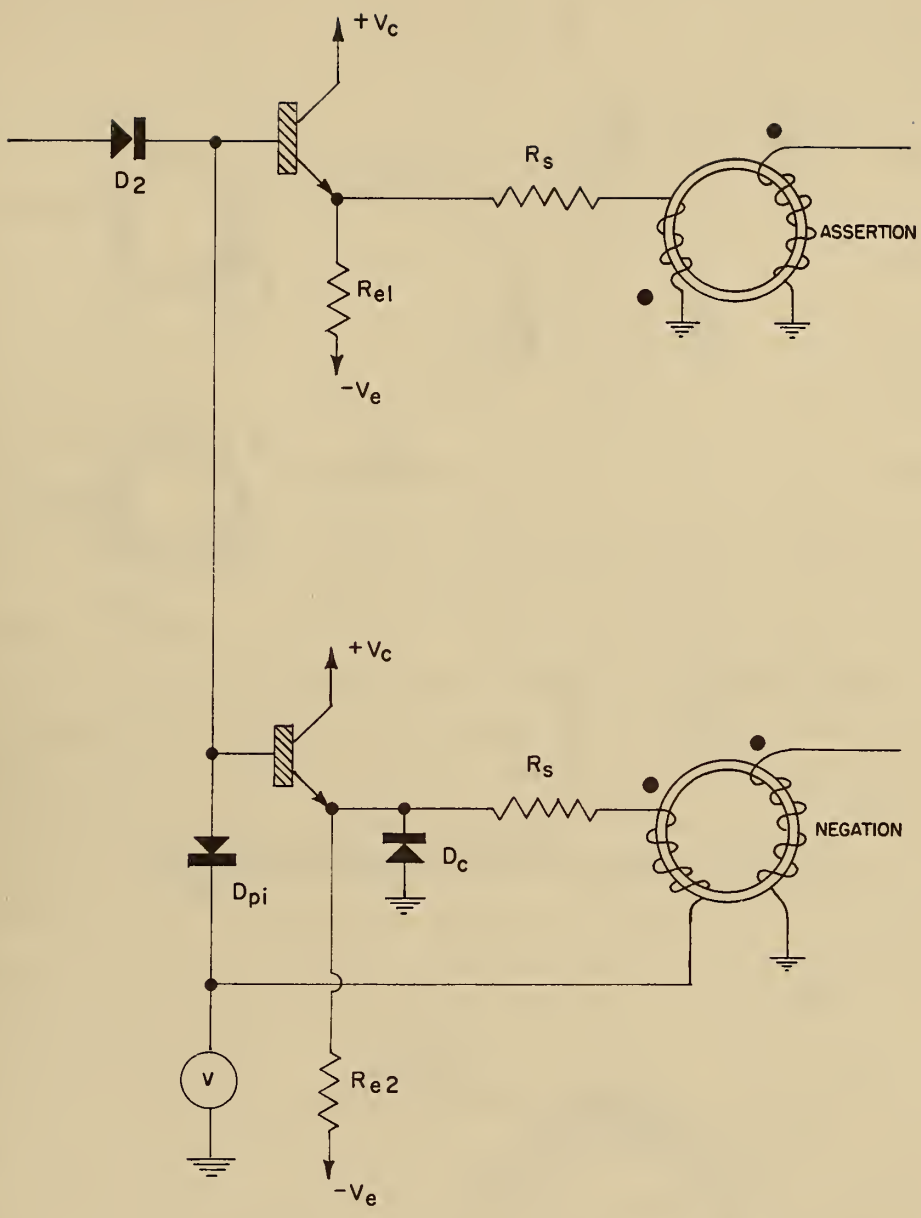


Figure 66. Separate assertive-, and negating amplifiers driven in parallel

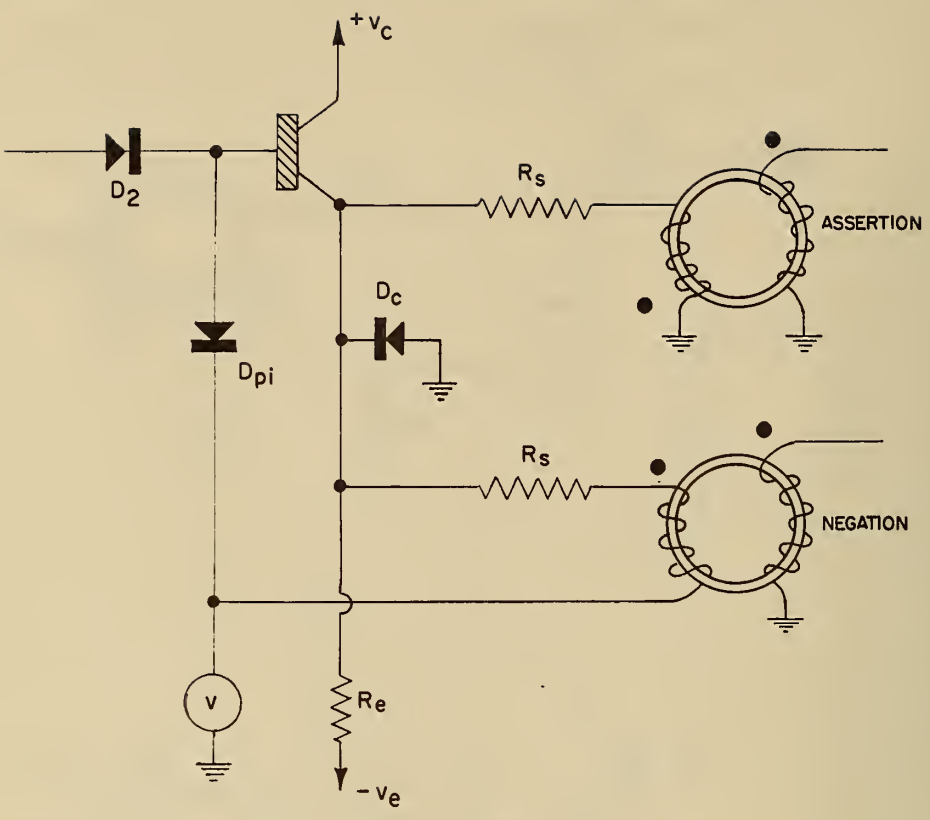


Figure 67. Combined assertive-, and negating amplifiers

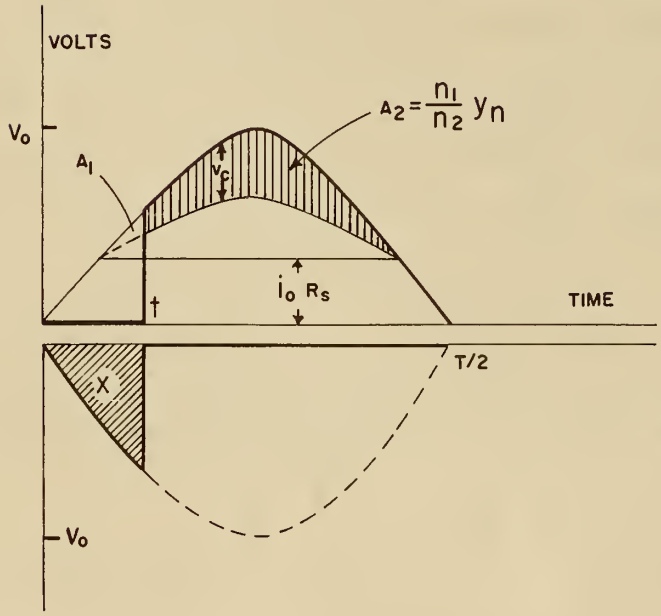


Figure 68. Explanation of the negating amplifier

Now in the case of the assertive core, the output $y_a(x)$ is given by curve 2 in Figure 33; and referring to Figure 68,

$$y_a = \frac{n_2}{n_1} \quad A_1(x) \tag{71}$$

Furthermore,

$$A_1 + A_2 = \frac{n_1}{n_2} \quad y_a \left(\frac{v_o T}{\pi}\right) \tag{72}$$

Therefore

$$y_n(x) = \frac{n_2}{n_1} \quad A_2 = y_a \left(\frac{v_o T}{\pi}\right) - \frac{n_2}{n_1} \quad A_1(x) \tag{73}$$

and

$$y_n(x) = y_a \left(\frac{v_o T}{\pi}\right) - y_a(x) \tag{74}$$

Then, since

$$y_a \left(\frac{v_o T}{\pi}\right) = s_{21} \tag{75}$$

from Figures 60 and 62, the transfer-function of the negating resistor-core element is

$$y_n(x) = s_{21} - y_a(x) \tag{76}$$

$y_n(x)$ is simply the reflection of $y_a(x)$ in the line $y = s_{21}/2$, and is shown in Figure 69 as $y_n = \overline{f}_1(x)$.

10. THE PROPAGATION FUNCTION FOR NEGATING AMPLIFIERS ONLY

To get the element-group transfer-functions resulting from combining the saturating emitter-follower and the negating resistor-core element, we superimpose their graphs in the manner of Figures 21 and 60.* Figure 70 shows the emitter-follower transfer-function $y_2 = f_2(x)$ plotted for $V_c/v_o = .90$ and $G = 25$, together with the reflection in the line $y = x$ of the negating resistor-core transfer-function $y_n = \overline{f}_1(x)$. The curves for $y = \overline{f}_{21}(x) = \overline{f}_1\left[f_2(x)\right]$ and $y = \overline{f}_{12}(x) = f_2\left[\overline{f}_1(x)\right]$, and the values for $\overline{r}_{21}$ and $\overline{r}_{12}$ are available directly from this plot, as r_{21} and r_{12} were obtained in Figure 21, and are shown in Figure 71. The values for $\overline{s}_{21}$ and $\overline{s}_{12}$ are seen to be equal to s_{21} and s_{12} for the assertive amplifier.

We now wish to obtain the total steady-state propagation function $\phi^{\infty}(x)$ for a signal travelling in rings or cascades of saturating emitter-follower elements and negating resistor-core elements in alternating sequence. $\phi^{\infty}(x)$ will consist of two propagation functions $\overline{F}_{12}^{\infty}(x)$ and $\overline{F}_{21}^{\infty}(x)$ arising from the association of the elements into two possible minimum element-groups having the group transfer-functions $\overline{f}_{12}(x)$ and $\overline{f}_{21}(x)$ respectively. In accordance with equation (13) we can write

$$\overline{F}_{12}^{\infty}(x) = \lim_{n \to \infty} \overline{F}^n(x) = \lim_{n \to \infty} \begin{cases} \overline{f}^n(s + x) \\ \overline{f}^n(0 + x) \end{cases} \tag{77}$$

* See, however, Appendix IX, which shows a shorter method applicable here.

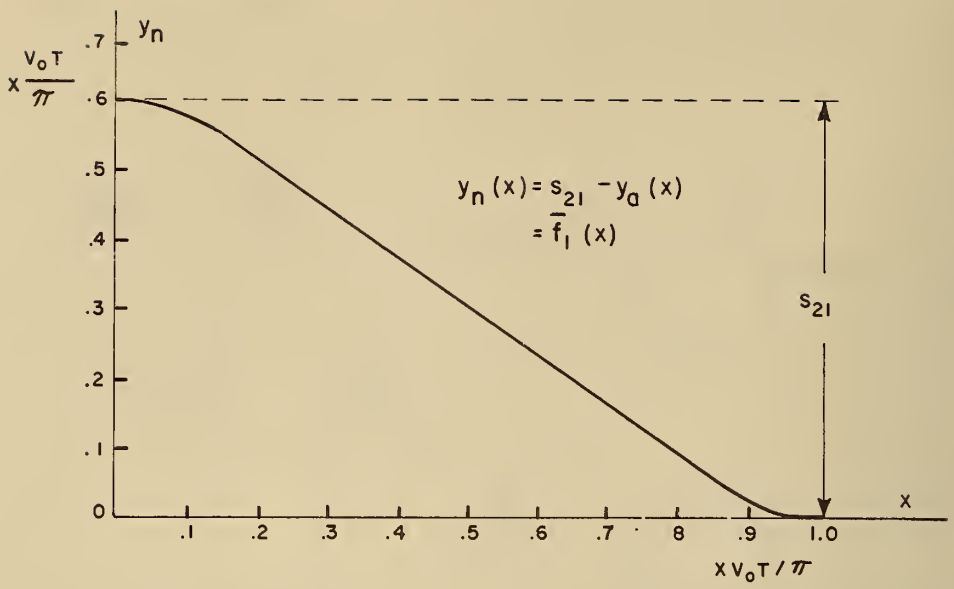


Figure 69. Volt-second transfer-function of the negating resistor-core element

for which, because $\overline{f}_{12}(x)$ has a negative slope, we must distinguish two cases: n even, and n odd. When n is even we may think of the sequence as made up of n/2 identical element groups $\overline{1}2\overline{1}2$, each having the transfer function $f_{\overline{1}2\overline{1}2}(x) = f_2\left[\overline{f}_1\left\{f_2\left[\overline{f}_1(x)\right]\right\}\right]$. But this transfer-function has a positive slope; therefore

$f^{\infty/2}_{\overline{1}2\overline{1}2}(x) = \overline{f}^{\infty}_{12}(x)$ has a positive slope also, and

resembles $f^{\infty}(x)$ shown in Figure 13a. Then, for n even, $\overline{F}^{\infty}_{12}(x)$ resembles Figure 13b.

When n is odd, we may write

$$\underset{\text{n-odd}}{\overline{f}^{\infty}_{12}(x)} = \overline{f}_{12}\left[\underset{\text{n-even}}{\overline{f}^{\infty}_{12}(x)}\right]$$ and the operations indicated on the

right, when carried out on the superimposed graphs of Figure 71, show that $\underset{\text{n-odd}}{\overline{f}^{\infty}(x)}$ is as shown in Figure 72a. Then by (77), $\overline{F}^{\infty}_{12}(x)$ for n odd has the form shown in Figure 72b. Thus it is seen that $\overline{F}^{\infty}_{12}(x)$ has two solutions, and by similar reasoning, $\overline{F}^{\infty}_{21}(x)$ also has two solutions. The graph of the complete propagation function $\phi^{\infty}(x)$ therefore includes the four square-loop graphs shown in Figure 73.

To interpret these graphs, we observe that $\underset{\text{n-even}}{\overline{F}^{\infty}_{12}(x)}$ gives the limiting or steady-state response at

all the even-numbered 2, 1 junctions in a sequence to a disturbance introduced at the zero-th 2, 1 junction $\underset{\text{n-odd}}{\overline{F}^{\infty}_{12}(x)}$ gives the response at all the odd-numbered 2, 1 junctions to a disturbance at the zero-th 2, 1 junction. A comparison of Figure 73b with Figure 73a shows that the signals at the odd

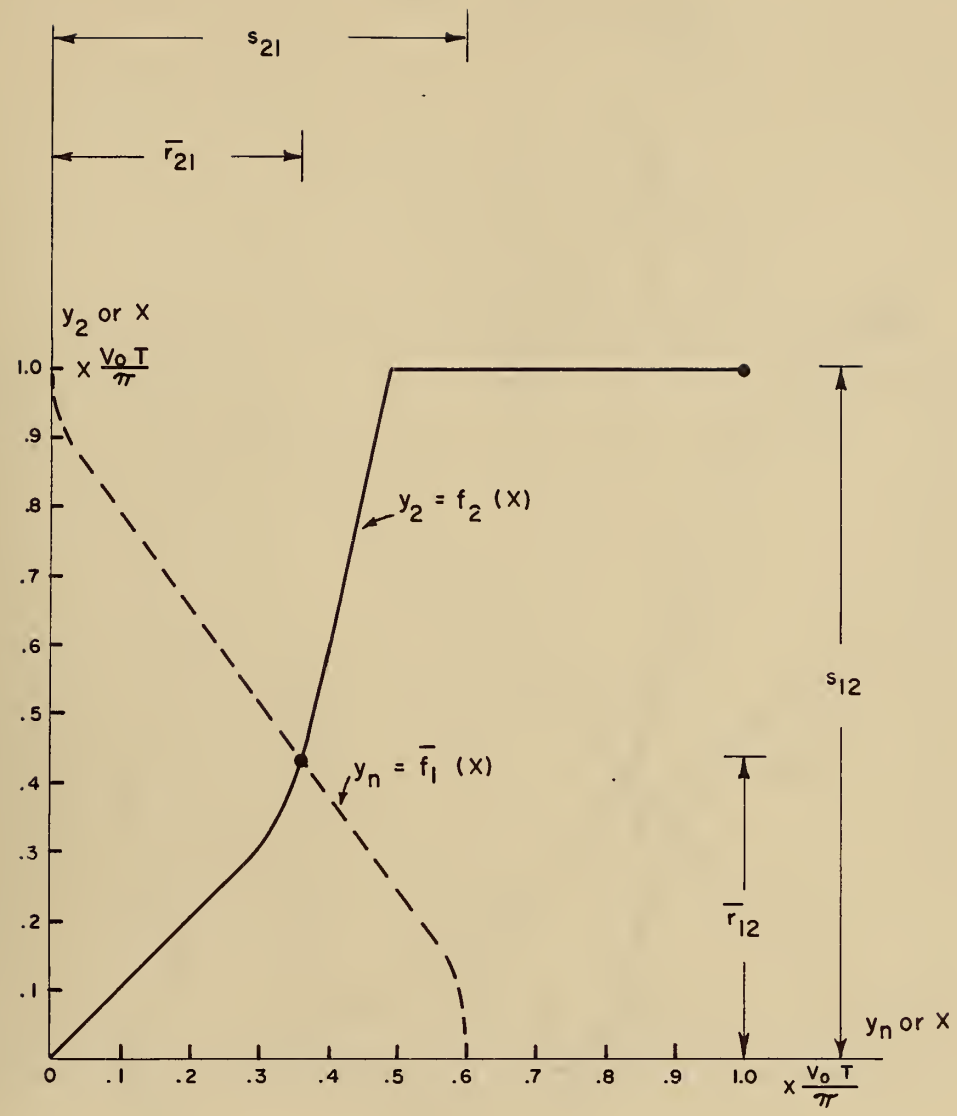


Figure 70. Evaluation of r and s for the transistor-negating core element group and for the negating core-transistor element group by super-position of the element transfer-functions

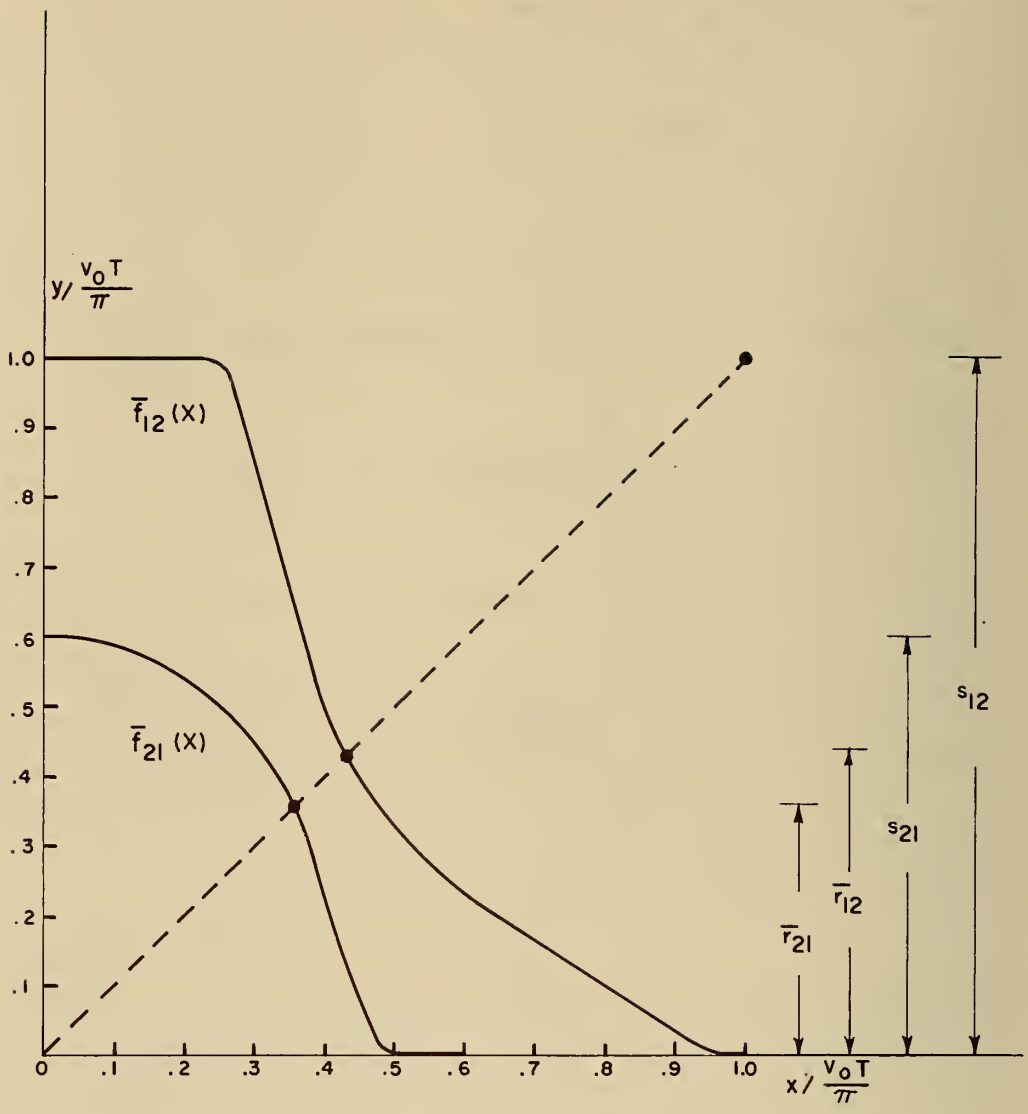
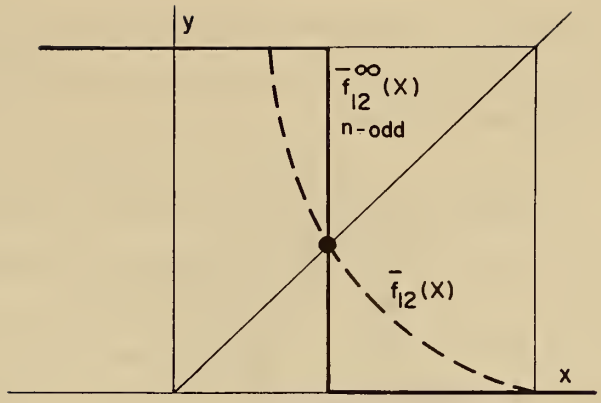
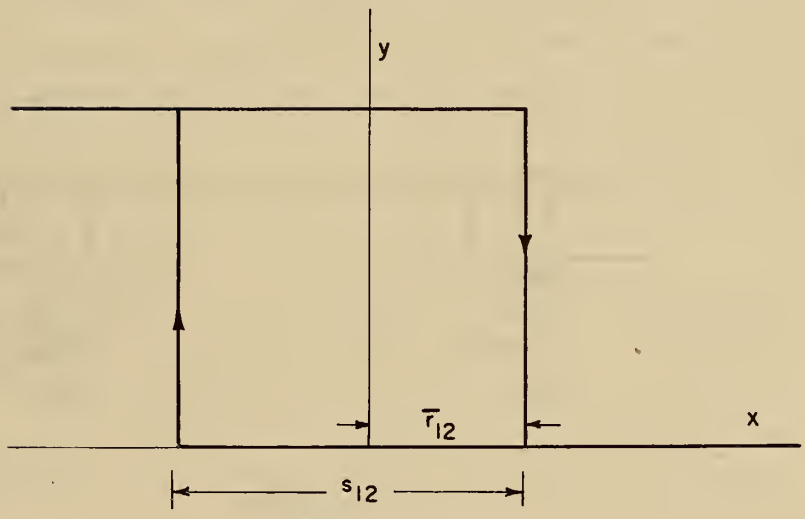


Figure 71. The transistor-negating core transfer-function $\bar{f}_{21}(X)$, and the negating core-transistor transfer-function $\bar{f}_{12}(X)$ constructed graphically from Figure 70



(a)



(b)

Figure 72. a. $\bar{f}_{12}^{\infty}(X)$ derived from $\bar{f}_{12}(X)$; n-odd

b. $\bar{F}_{12}^{\infty}(X)$; n-odd

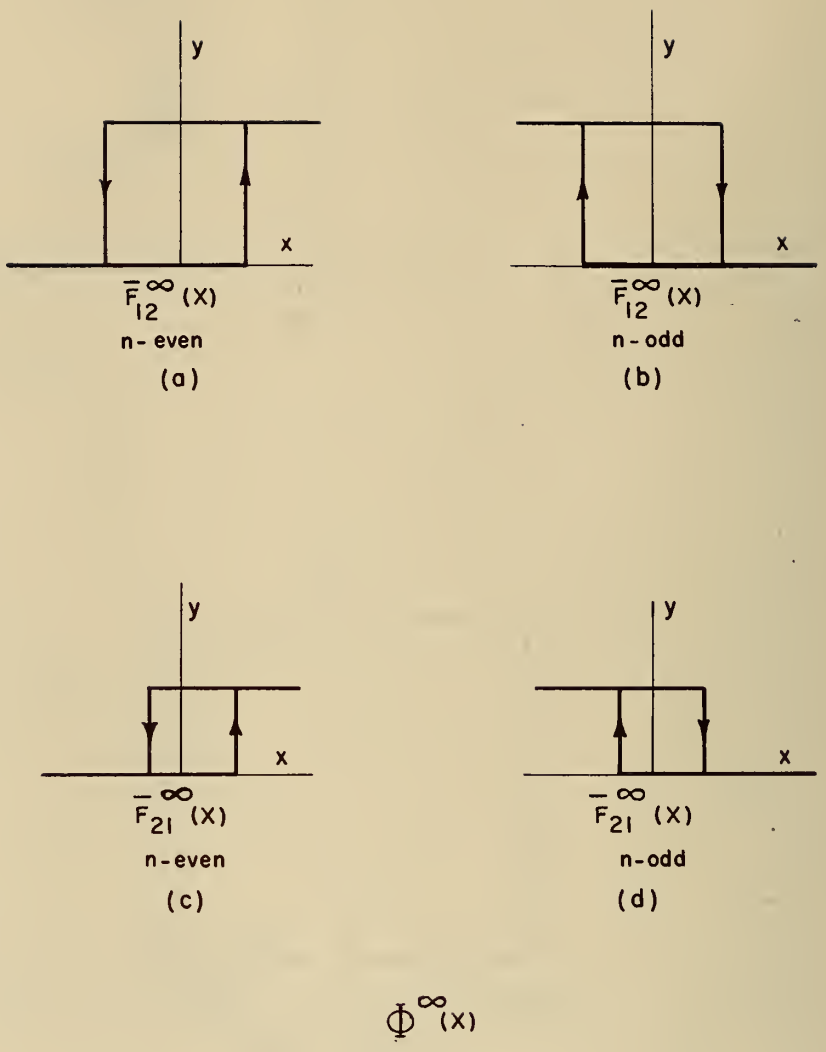


Figure 73. The complete steady-state propagation-function for a sequence of negating amplifiers

numbered 2, 1 junctions are the complements of those at the even-numbered 2, 1 junctions. For example, observe that a positive disturbance, say, at the zero-th junction affects a full ONE observed at the even junctions in the same way that it affects a full ZERO observed at the odd junctions. $\overline{F}^{\infty}_{21}(X)$ is similarly interpreted for the 1, 2 junctions.

11. STABILITY MARGINS OF MIXED ELEMENT-GROUPS

In the unlikely event that rings and long cascades of negating element-groups are to be associated with rings and cascades of assertive element-groups, attention must be given to the fact that $\overline{r}_{21}$ may not be equal to r_{21}, and $\overline{r}_{12}$ may not be equal to r_{12}. When these quantities differ, the signal stability margins are reduced because an ambiguity of circuit response to substandard signals is introduced.

The nature of this difficulty is illustrated for the very important practical case in which isolated negating element-groups form links in rings and cascades of assertive groups. Figure 74 shows the severest example of this, in which negating element-groups alternate with assertive element-groups. In such a sequence, four kinds of identical inclusive element-groups can be formed, as shown by a, b, c and d of Figure 74; each with a different transfer-function derived, as indicated, from the sub-group transfer-functions $f_{12}(X)$, $f_{21}(X)$, $\overline{f}_{12}(X)$ and $\overline{f}_{21}(X)$, whose graphs are shown in Figure 62 and Figure 71.

Recalling Figure 73, we see that the total steady-state propagation function $\phi^{\infty}(X)$ includes, in the present case:

1) $F^{\infty}_{2\overline{1},21}(X)$ (n-even) and $F^{\infty}_{2\overline{1},21}(X)$ (n-odd)

2) $F^{\infty}_{21,2\overline{1}}(X)$ (n-even) and $F^{\infty}_{21,2\overline{1}}(X)$ (n-odd)

3) $F^{\infty}_{\overline{1}2,12}(X)$ (n-even) and $F^{\infty}_{\overline{1}2,12}(X)$ (n-odd)

4) $F^{\infty}_{12,\overline{1}2}(X)$ (n-even) and $F^{\infty}_{12,\overline{1}2}(X)$ (n-odd)

In these four pairs of steady-state propagation functions are included two values of s, s_{12} and s_{21}; and, in general, 4 values of r: $r_{2\overline{1},21}$, $r_{21,2\overline{1}}$, $r_{\overline{1}2,12}$ and $r_{12,\overline{1}2}$. Figure 75 shows $\phi^{\infty}(X)$ in terms of eight square-loop graphs. The values of r and s in these graphs were obtained, as shown in Figure 76, in the manner of Figure 21. The negating transfer-functions have been reflected in the line y = x in Figure 76.

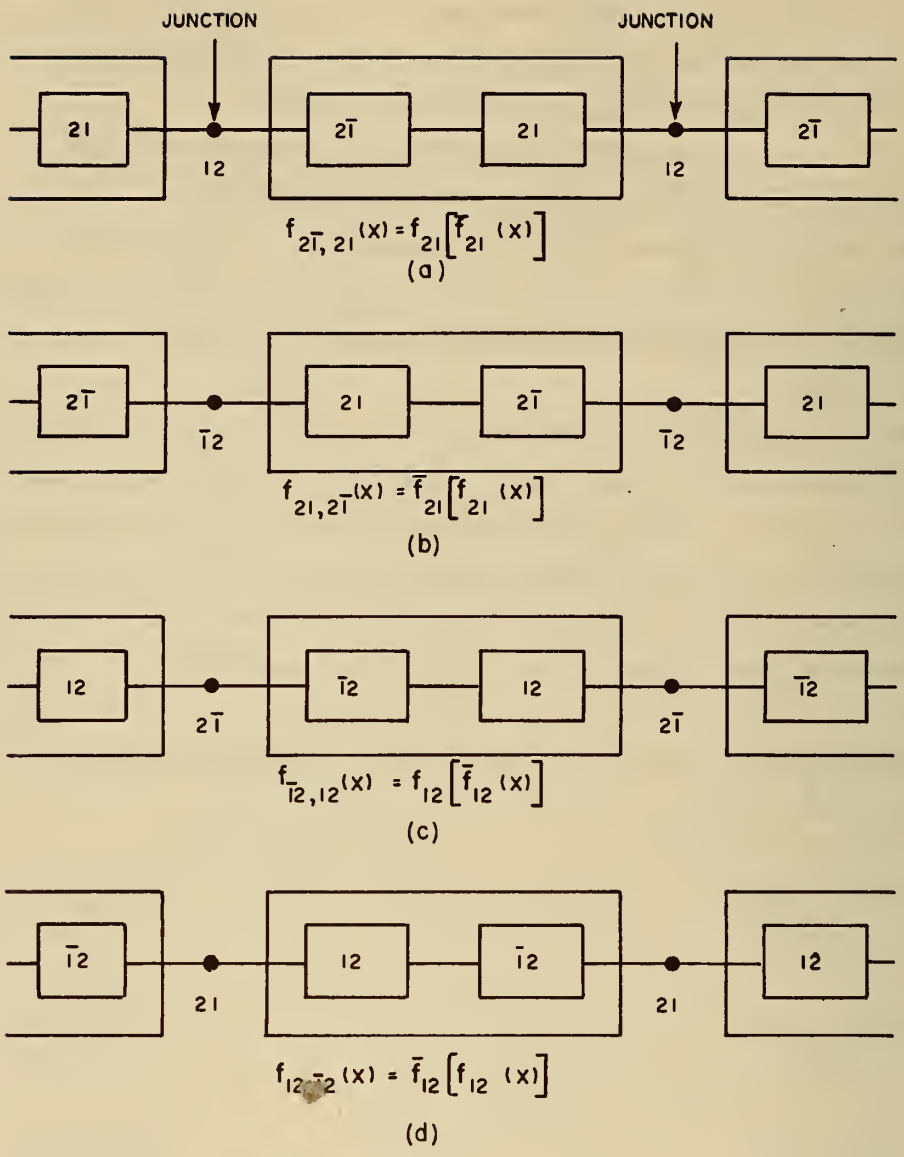


Figure 74. The four kinds of element-group groups that can be formed in an alternating sequence of assertive element-groups and negating element-groups

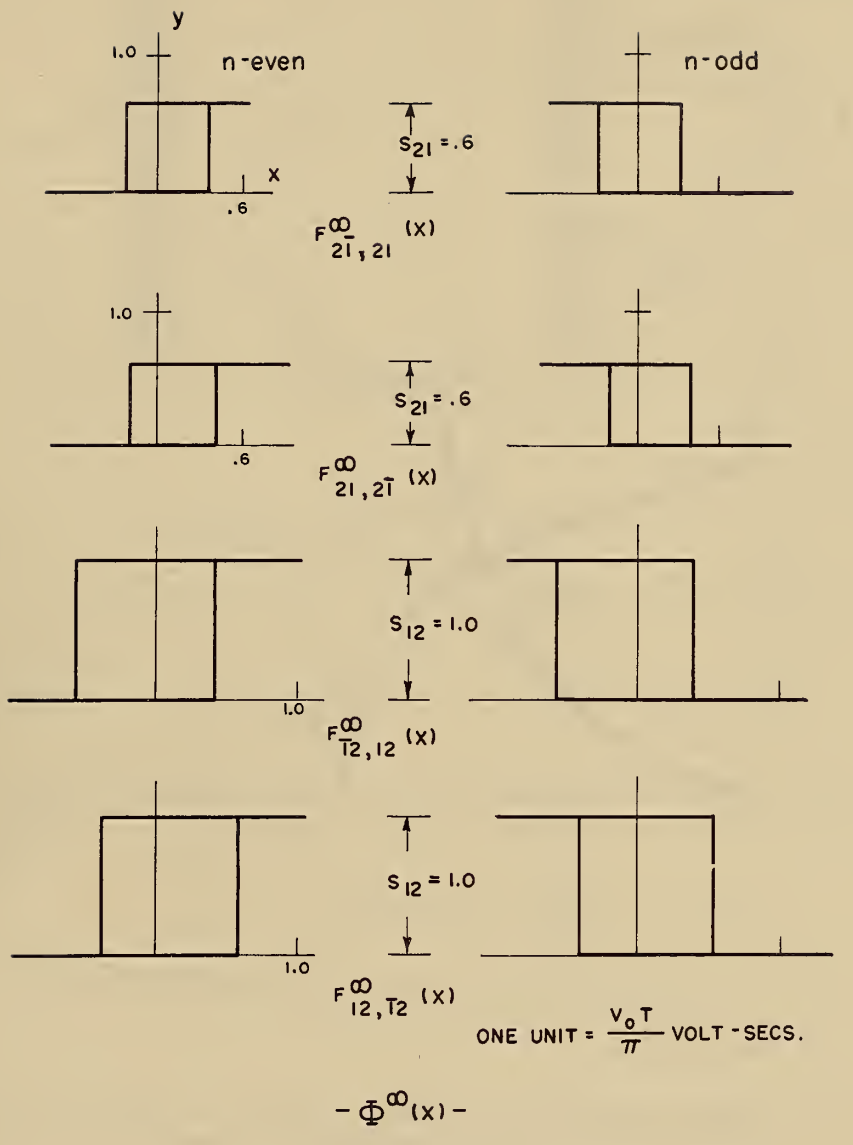


Figure 75. The complete steady-state propagation function for alternating assertive and negating element-groups

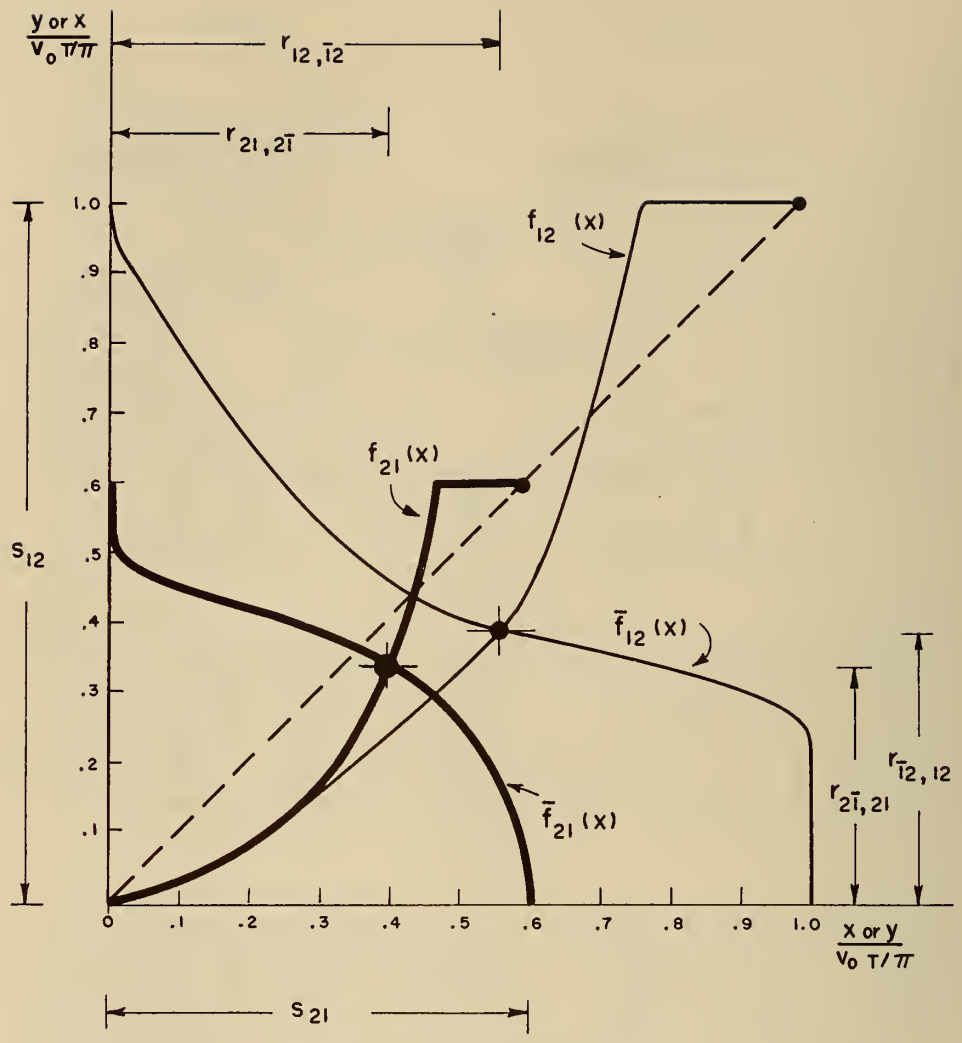


Figure 76. Determination of the four values of r and the two values of s associated with the alternating sequence of assertive and negating element-groups

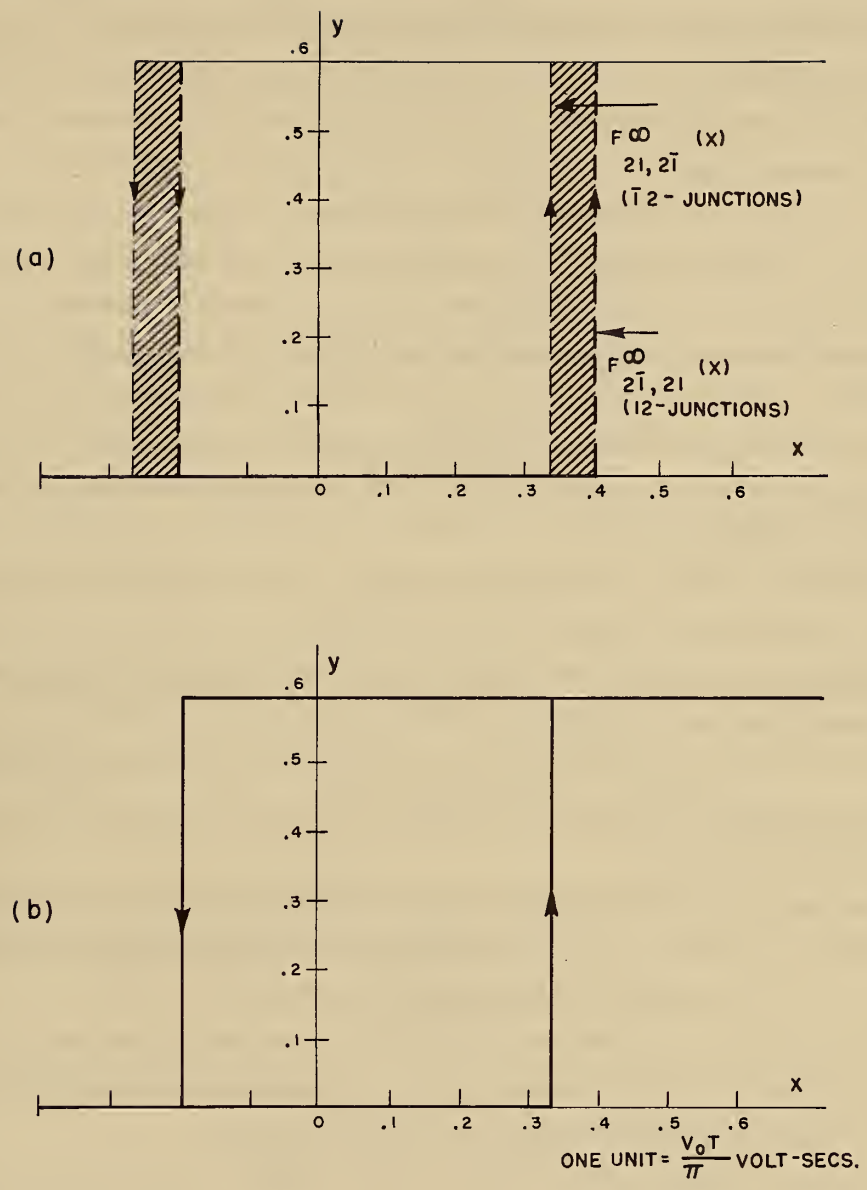


Figure 77. a. Non-coincidence of $F^{\infty}_{21,2\bar{1}}(x)$ and $F^{\infty}_{2\bar{1},21}(x)$ produces regions (shaded) of ambiguous response to signals that can enter the sequence of Figure 74 at $\bar{1}, 2$ junctions or at $1, 2$ junctions

b. Resultant effective propagation function for signals that can enter at $\bar{1}, 2$ junctions or at $1, 2$ junctions

In Figure 77a the n-even graphs of $F^{\infty}_{2\bar{1},\,21}(X)$ and $F^{\infty}_{21,\,2\bar{1}}(X)$ are shown superimposed. These are the steady-state functions for the inclusive element-groups that lie between the 12-junctions, and between the $\bar{1}2$-junctions respectively. If a ring of the kind being considered here is embedded in a logic net, the signals and disturbances from the net may enter the ring equally well at the 12-junctions, and at the $\bar{1}2$-junctions. Figure 77a shows that a disturbance whose value lies within the shaded ranges grows to full signal magnitude s_{21} if it enters the ring at $\bar{1}2$-junctions; or, it diminishes to zero magnitude if it enters at 12-junctions. Because the shaded ranges of ambiguity must be excluded, practical stability margins for disturbances introduced into the ring at $\bar{1}2$-junctions, or at 12-junctions are shown in the composite graph of Figure 77b to be the least thresholds of $F^{\infty}_{2\bar{1},\,21}(X)$ and $F^{\infty}_{21,\,2\bar{1}}(X)$. To maximize the practical stability margins by eliminating response ambiguity, the functions $f_{21}(X)$ and $\bar{f}_{21}(X)$ should cross the unity-gain line at the same point. This makes $r_{2\bar{1},21} = r_{21,2\bar{1}}$ so that the square-loop graphs coincide. The graph intersection point then lies on the unity-gain line in Figure 76.

The foregoing discussion can be repeated, in general, for the element-groups lying between the $2,\bar{1}$ junctions, and between the 21-junctions. But, in the practical case of the Transmag circuit, no logic interconnections are made at these junctions because they lie within the digital amplifiers. Therefore, there is less need to minimize the difference between $r_{\bar{1}2,\,12}$ and $r_{12,\,\bar{1}2}$.

In any case, a properly designed input buffer or synchronizer will not (except to within the specified error probability p) introduce, into the logic net, signals that lie within the ranges of ambiguity for 12 and $\bar{1}2$-junctions.

In the more general case of a sequence having one negating amplifier for every n identical assertive amplifiers, the values of s and r are the same as for the worst case just considered.

12. FACTORS AFFECTING POWER GAIN AND FAN-OUT

In this section we wish to consider the important factors affecting the maximum power gain [= current gain] G and the logical fan-out N achievable by the Transmag amplifier. The overall gain is simply the product of the gains of the individual stages.

Because the output stage handles the greatest amount of power, and, in Transmag, also provides most of the gain, its design, from the standpoint of maximum achievable gain is considered first. This order is customary in the design of multistage power amplifiers.

12.1 The Gain of the Magnetic Amplifier

The core is, in a sense, a passive amplifier since it behaves as a load-current sink, rather than as a load-current source. Referring to Figure 51, at the beginning of the transmission of a ZERO, the sum of the currents flowing in the output AND-gate pull-up R_{po} and in the pull-ups R_{p1} of all the driven AND-gates, which are not otherwise held down, is suddenly switched into the output winding of the (near) saturated core. As this takes place, a voltage is developed across the winding whose time-integral is given by the product of its self-inductance times the total current.

From Section 2 we know that if this voltage-time integral exceeds r_{21}, a false ONE will be transmitted to the driven AND-gates. Therefore, if i_{max} is the largest permissible value for the sum of these currents, and if L_{co} is the saturation inductance of the output winding, then

$$L_{co}\, i_{max} = r_{21}. \quad * \tag{78}$$

Now

$$s_{21} = n_2(2\,\phi_r) \tag{79}$$

is the maximum ONE signal output obtainable from the core, and we can write

$$i_{max}\, L_{co} = \frac{r_{21}}{s_{21}}\; n_2\,(2\,\phi_r). \tag{80}$$

Then, we define the effective full-switching inductance of the core output winding to be

$$L_{c1} = \frac{n_2(2\,\phi_r)}{\hat{i}\, n_1/n_2} \tag{81}$$

where $\hat{i}$ is the peak value of the total current drawn by the input winding of the core, and is given by

$$\hat{i} = \hat{\underline{i}} + i'_0 = \hat{\underline{i}} + (i_0 + i_{bias}), \tag{82}$$

in which $\hat{\underline{i}}$ is the peak value of the core excess current $\underline{i}$. $\underline{i}$ satisfies the Manyuk-Goodenough switching equation

$$\frac{n_1 \underline{i}}{l} = \frac{n_1}{l}\,(i - i'_o)\,\tau = (H - H'_o)\,\tau = S_w, \tag{21c}$$

where i'_o and H'_o are the core switching thresholds, including external bias.

We now define the core maximum current gain G_c by

$$G_c = \frac{i_{max}}{\hat{i}} \tag{83}$$

and get, from equations (80) and (81),

$$L_{co}\; G_c\; \hat{i} = \frac{r_{21}}{s_{21}}\; n_2\; (2\,\phi_r) = \frac{r_{21}}{s_{21}}\; L_{c1}\; \hat{i}\; n_1/n_2$$

or

$$G_c = \frac{r_{21}}{s_{21}}\;\; \frac{n_1}{n_2}\;\; \frac{L_{c1}}{L_{co}} \tag{84}$$

Now if we assume the output winding to be a complete toroid, its inductance can be written as

$$L_c = \frac{n_2^2\, \mu\, A}{l} \tag{85}$$

---

* Here we are neglecting the forward drop across D_o, and are assuming that $B_r/B_s = 1$.

where A is the winding cross-section, l is the mean magnetic path length, and μ is the average permeability of the volume within the winding.

In magnetic amplifiers constructed for high switching rates, a large fraction of this volume is unfilled by the magnetic material. See Figure 78, in which A_m is the cross-section of the magnetic material, μ_m is its permeability, and μ_o is the permeability of free space.

Thus,

$$\mu A = \mu_m A_m + \mu_o (A - A_m) \simeq \mu_m A_m + \mu_o A \qquad (86)$$

and

$$\frac{\mu}{\mu_o} = \frac{\mu_m}{\mu_o} \left(\frac{A_m}{A} \right) + 1$$

$$= \frac{\mu_m}{\mu_o} F_s + 1 \qquad (87)$$

where F_s is called the space factor.

Then, from (85), and because n_2, A and l do not change, (84) can be written as

$$G_c = \frac{r_{21}}{s_{21}} \frac{n_1}{n_2} \frac{\mu}{\mu_o}$$

$$= \frac{r_{21}}{s_{21}} \frac{n_1}{n_2} \left(\frac{\mu_m}{\mu_o} F_s + 1 \right)$$

$$= \frac{r_{21}}{s_{21}} \frac{n_1}{n_2} (k_m F_s + 1) \qquad (88)$$

in which k_m is the effective switching relative permeability of the core material.

We now wish to evaluate k_m. Making use of the flux equation

$$L_{c1} \frac{n_1}{n_2} \hat{i} = \left(\frac{n_2^2 \mu_m A_m}{l} + L_{co} \right) \frac{n_1}{n_2} \hat{i} = n_2 (2 \phi_r) + L_{co} \frac{n_1}{n_2} \hat{i},$$

we have

$$\frac{\mu_m A_m}{l} = \frac{2 \phi_r}{n_1 \hat{i}} \qquad (89)$$

Then, in the optimum case, (see Fig. 37) for which m = 0.33 and $R_s = R_c$, $\hat{i}$ equals $2 \underline{\hat{i}}$.

Now $$\underline{\hat{i}} = \hat{i} - i_o' = \frac{v_{co}}{R_c} \qquad (90)$$

Combining this with the following two relations:

$$R_c = \frac{n_1^2 (2 \phi_r)}{S_w l} \qquad (24)$$

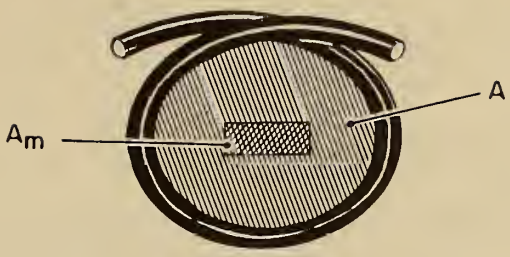


Figure 78. Diagram illustrating the total winding-enclosed area A, and the magnetic material cross-section A_m

and

$$\frac{v_{co} T}{\pi} = n_1 (2 \phi_r), * \tag{91}$$

we get

$$\hat{i} = 2 \underline{\hat{i}} = \frac{2\pi S_w l}{n_1 T} \tag{92}$$

Using this value for $\hat{i}$ in (89) gives

$$\mu_m = \frac{(\phi_r / A_m) T}{\pi S_w} = \frac{B_r T}{\pi S_w} = \frac{B_r}{\pi S_w f_c} \tag{93}$$

and

$$k_m = \frac{\mu_m}{\mu_o} = \frac{B_r}{\pi \mu_o S_w f_c}, \tag{94}$$

where f_c is the "clock" frequency. This is a working definition of k_m under the constraint $\hat{i} = 2 \underline{\hat{i}}$. It is applicable only at high switching rates for which $\underline{\hat{i}} \geq i_o$, where i_o is the switching threshold current, and has as its lower limit the coercive current i_c.

At low frequencies k_m approaches its dc value $2 B_r / \mu_o H_c$.

Putting the value for k_m given in (94) into the gain equation (88) gives

$$G_c = \frac{r_{21}}{s_{21}} \frac{n_1}{n_2} \left(\frac{B_r F_s}{\pi \mu_o S_w f_c} + 1 \right) \tag{95}$$

as the magnetic amplifier current gain for the optimum case shown in Figure 37. This is also the power gain, since the signal voltage amplitude remains unchanged.

Observe that (95) does not directly contain core geometry and the number of turns in the windings. These quantities do affect the space factor F_s, however; and they enter directly into the core effective input resistance R_c.

---

* See Appendix III.

$$R_c = \frac{n_1^2 \Delta \phi}{S_w l}$$

$$= \frac{2n_1^2 \phi_r}{S_w l}$$

$$= \frac{2n_1^2 B_r A_m}{S_w l} \qquad (96)$$

$$= \frac{2n_1^2 B_r F_s A}{S_w l}$$

R_c must be kept as large as possible, for any given "clock" voltage v_o in order to minimize the power required to drive the core.

In the optimum case of Figure 37 the impedance presented to the emitter-follower by the core and R_s in series is

$$\frac{v_{co}}{\hat{i}} = \frac{1}{\hat{i}} \left[R_s \hat{i} + R_c (\hat{i} - i_o') \right]$$

$$= \frac{1}{\hat{i}} \left[R_c \hat{i} + R_c (\hat{i} - i / 2) \right]$$

$$= 3 R_c / 2 \qquad (97)$$

and the power absorbed by the core-resistor combination is

$$1/2 \quad \frac{v_o^2}{3 R_c / 2} = \frac{v_o^2 / R_c}{3} \qquad (98)$$

To minimize this power, one would like to keep v_o small, yet it must be kept at least several times greater than the forward threshold of the circuit diodes. The minimum value of v_o consistent with good operation of the diodes thus becomes a more-or-less fixed design parameter of about 10 volts.

Then, at a given frequency f_c, with v_o fixed, we have, for the case of full core switching, that

$$2n_1 \phi_r = 2n_1 B_r F_s A \simeq 1/3 \frac{v_o T^*}{\pi} = 1/3 \frac{\left[v_o\right]}{\pi f_c} \qquad (99)$$

which is a fixed quantity. This leaves R_c to be maximized through n_1 and l, since S_w is a constant of the magnetic material.

---

* Assuming $m \simeq 0.3$.

Writing

$$R_c = \frac{n_1}{l}\left[\frac{2n_1 B_r F_s A}{S_w}\right]$$

$$= F_{w1}\left[\frac{2n_1 B_r F_s A}{S_w}\right] \qquad (100)$$

where the bracketed quantity is held constant, we see that R_c is proportional to F_{w1}, the winding factor of the input winding. F_{w1} is related to the output winding factor F_{w2} by

$$F_{w1} = \frac{n_1}{n_2} F_{w2} \qquad (101)$$

The output winding is put on the core first to keep its cross-sectional area A as small as possible. Then the input winding is added.

The practical limitations of toroidal core winding procedures, wire size, and toroidal geometry result in a reduction of the maximum attainable value for F_{w2} as l is reduced. The maximum value for F_{w2} is obtained by putting on layers of winding until the remaining toroid aperture cannot be made smaller.

For any given l, as n_1 is increased, n_2 increases, (keeping n_2/n_1 constant) and, beyond one layer of winding, A increases. As a result F_s inevitably decreases. The increase in n_1 raises R_c, provided the bracketed quantity is not reduced, but the price is now paid as a loss in core gain G_c, proportional to the reduction of F_s, as is shown by equation (95).

In designing the magnetic amplifier, both equations (95) and (100) must be used to arrive at the desired compromise between power expended and gain capability achieved.

Combining equations (96) and (99) we can write

$$R_c f_c = \frac{\left[v_o\right]}{3\pi S_w} F_{w1} \qquad (102)$$

which, subject to the restriction (indicated by brackets) that v_o remain fixed, expresses a $(\text{power})^{-1}$ - frequency figure of merit for the magnetic amplifier in the form of the resistance-frequency product as a function of F_{w1} and S_w.

Then observing that for G_c in (95) to be greater than 4, with $r_{21}\, n_1/s_{21}\, n_2 \leq 1/4$, it is necessary for $B_r F_s/\pi \mu_o S_w f_c$ to exceed 16, we may conveniently drop the unit quantity from the parenthesis and write:

$$G_c f_c \simeq \frac{r_{21}}{s_{21}} \frac{n_1}{n_2} \frac{B_r F_s}{\pi \mu_o S_w}$$

$$\simeq \frac{r_{21}}{s_{21}} \frac{n_1}{n_2} \frac{B_r A_m}{\pi \mu_o S_w A} = \frac{r_{21}}{s_{21}} \frac{n_1}{n_2} \frac{\phi_r}{\pi \mu_o S_w A}$$

Combining this with (99) gives

$$G_c f_c^2 = \frac{r_{21}}{s_{21}} \frac{1}{n_2} \frac{\left[v_o\right]}{6\pi^2 \mu_o S_w A}; \quad G_c \geq 4. \tag{103}$$

This equation gives a unique value for the gain - (frequency)^2 product which is independent of frequency if $2n_1 \phi_r = 2n_1 B_r F_s A$ is kept inversely proportional to f_c, as required by (99). Now, if the turns-ratio is to be preserved, n_1 must be kept constant since n_2 appears in (103a). A also appears in (103), and B_r is a constant of the core material. This leaves F_s which must be varied inversely with f_c. For a <u>given wound core</u> we see that (103) can hold only at the one frequency that satisfies (99).

But equation (99) applies only when the core is <u>fully</u> switched. If the alternative of <u>partial</u> switching is to be included, the more general equation

$$n_1 \Delta \phi f_c = n_1 \Delta B F_s A f_c = \frac{\left[v_o\right]}{3\pi} \tag{104a}$$

replaces (99). $\Delta \phi$ is illustrated in Figure 28 a.

Then if we define the fractional-switching variable Z by

$$Z = \frac{\Delta B}{2B_r} \tag{105}$$

equation (104a) can be written in the form:

$$Z F_s f_c = \frac{\left[v_o\right]}{6\pi n_1 B_r A} \tag{104b}$$

or, alternatively as

$$Z A_m f_c = \frac{\left[v_o\right]}{6\pi n_1 B_r} \tag{104c}$$

in which the variables are shown on the left. Thus the core gain G_c can be found from the $G_c f_c^2$ product, given by (103), at any frequency for which the product $Z A_m f_c$ satisfies (104c).

We note that (104 a, b, c) holds, in principle, at any frequency above the lowest needed to produce full switching, even for a given wound core, for which A_m is fixed, because Z automatically adjusts itself, varying inversely with f_c. But in practice, if Z falls too low, the effective value of S_w is materially increased; and this, by (103), lowers Gf_c^2. By reason of the higher power of its frequency term, (103) tends to set the maximum practical value for f_c, in any case.

If we also allow B_r as a design variable (104c) can be written as

$$Z \phi_r f_c = \frac{\left[v_o\right]}{6\pi n_1}, \tag{104d}$$

which is simpler and more general. The three design equations then are:

$$R_c f_c = \frac{\left[v_o\right] F_{w1}}{3\pi S_w} \tag{102}$$

$$G_c f_c^2 = \frac{r_{21}}{s_{21}} \frac{\left[v_o\right]}{6\pi^2 \mu_o S_w n_2 A}; \quad G_c \geq 4 \tag{103}$$

$$Z \phi_r f_c = \frac{\left[v_o\right]}{6\pi n_1} \tag{104d}$$

The design equations (102), (103) and (104d) were derived for the optimum case, illustrated in Figure 37, for which $R_s = R_c$, $m = 0.33$ and $n_2/n_1 \leq 3$. We make the core turns-ratio equal to 2 so that the core-transistor element-group transfer-function for this case will approximate those already derived for the experimental circuit. Now, generally speaking, it would be desirable to maximize both the $R_c f_c$ and the $G_c f_c^2$ products; and this could be done provided S_w, or A, or l could be made as small as we please. However, S_w is limited by the choice of core materials available; and, for the 1/8-mil. 4-79 Mo.-Permalloy tape used, it was around 0.33×10^{-6} oersted-seconds. Furthermore, as has already been pointed out, the practical limitations of core winding procedures, wire size, and toroidal geometry result in a reduction of the maximum attainable values for F_{w1} and F_{w2} as l and A are reduced. But, from (102), a reduction of F_{w1} reduces the achievable $R_c f_c$ product so that at high frequencies R_c falls too low to be compatible with the semiconductor components in the circuit, and excessive power is required to drive the core.

On the other hand, the attainment of an arbitrarily large winding factor by using a larger core and many more turns (by means of many layers of winding) is not permissible by reason of equation (103) which shows that the $G_c f_c^2$ - product varies inversely with the number of output winding turns n_2 and the winding cross-section A. An excellent compromise of the conflicting goals of low power and high gain, in the multi-hundred kilocycle-per-second range, is provided by commercially available cores of 1/32-inch wide, 1/8-mil tape wrapped on stainless steel bobbins having a diameter of 0.150 inches. These can be supplied with windings totaling 300 turns of No. 43 wire.

In the case of a 10-wrap core carrying a single 300-turn winding, the manufacturer gives the following data:

$$F_s = 0.04$$

$$A_m = 2.5 \times 10^{-4} \text{ cm}^2$$

$$l = 1.3 \text{ cm}$$

$$\phi_r = 1.8 \text{ maxwells}$$

From this we calculate that

$$A = 6.2 \times 10^{-3} \text{ cm}^2;$$

and taking $n_1 = 100$ and $n_2 = 200$,

F_{w1} = 77 turns/cm

Then, using v_o = 10 volts, and S_w = 0.33×10^{-6} oerst-sec., the resistance-frequency product for this magnetic amplifier is

$$R_c f_c = \frac{10v.}{3\pi} \frac{77 \times 10^2 \text{ turns/meter}}{0.33 \times 10^{-6} \text{ oerst-sec } (10^3/4\pi) \text{ amp-turns-sec/meter}}$$

$$= 3 \times 10^8 \text{ ohms-sec}^{-1}$$

From this we may, in principle, calculate R_c for this amplifier for any frequency that makes $Z \leq 1$ in equation (104d).* Using (104d) we calculate Z for f_c = 300 kc.

$$Z = \frac{\left[v_o\right]}{\phi_r \, 6\pi \, n_1 \, f_c} = \frac{10^9 \text{magvolts}}{(1.8 \text{ mxwls})(6\pi)(100)(3 \times 10^5 \text{ cps})}$$

$$= 0.98 < 1$$

Therefore R_c at 300 kc is $3 \times 10^8 / 3 \times 10^5$ = 1000 ohms

Now to get the $G_c f_c^2$ - product from (103), using r_{21}/s_{21} = 1/2,

$$G_c f_c^2 = 1/2 \times 1/200 \frac{10^9 \text{ magvolts}}{6\pi^2 \, (1)(0.33 \times 10^{-6} \text{ oerst-sec})(6.2 \times 10^{-3} \text{ cm}^2)}$$

$$= 2 \times 10^{13} \text{ sec}^{-2}$$

Therefore the theoretical gain of this amplifier at 300 kc has the very large value of 200.

At the top of the multi-hundred kilocycle-per-second range

R_c = 300 ohms (at 1 mc), and

G_c = 20

From equation (98), the power required to drive the resistor-core combination is 33 milliwatts at 300 kc; and 100 milliwatts at 1 megacycle. Then, if we assume that the power dissipated by the collector is equal to twice** that consumed by $R_s + R_c$, we see that at 300 kc the transistor must dissipate 66 milliwatts, and, at 1 megacycle, 200 milliwatts. The need for a power transistor is indicated above 300 kc.

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* Z should be kept near to the value for which S_w has been evaluated.

** See Appendix VIII.

The foregoing discussion has shown that the gain capability of the 0.150 inch core is more than adequate for frequencies below one megacycle, and that, in the hundred-kilocycle range, the transistor output power capability is the chief consideration. Smaller wound cores, having diameters of 0.100 inch and 0.050 inch, are produced commercially, but these are less desirable in the hundred-kilocycle range because their best winding factor is less than for the 0.150 inch core. However, if we try to enter the megacycle range, the $G_c f_c^2$ - product just calculated for the 0.150 inch core shows that at 2 megacycles $G_c = 5$, which is about the lower limit of useful gain.

The solution is to use smaller cores with fewer turns and smaller winding cross-sections in order to get larger values for the $G_c f_c^2$ - product. But a heavy price is paid in terms of the increased power output demanded of the transistor arising, both from the reduced $R_c f_c$ product of the smaller cores, and from the increased f_c within this product.

12.1a How Scaling Affects the Relationship Between R_c, G_c and f_c

In the case of a given wound core, equations (102) and (103) give the relationship between G, R and f (dropping the subscripts) in terms of two constants, the Rf-product, and the Gf^2-product, provided that $Z \phi_r$ satisfied equation (104d). We now wish to determine how core size affects the gain-resistance-frequency relationship. Taking the mean magnetic path length l to be the measure of core size, and representing the Rf-product by P_R and the Gf^2-product by P_G we see from equations (102) and (103) that core size can affect $P_R(l)$ and $P_G(l)$ through the winding parameters F_{wl}, n_2 and A.

We now make the physically appropriate assumption that, regardless of size, the core is always wound to the same fraction of its window area with wire of the same size. We further assume n_2/n_1 to be held constant. As a result of these assumptions the core scaling law is expressed by:

$$\begin{aligned} F_{wl} &\sim 1 \\ n_1 \sim n_2 &\sim l^2 \\ A &\sim l^2 \end{aligned}$$

or

$$\left.\begin{aligned} F_{wl}(l) &= F_{wl}(l_o)(l/l_o) \\ n_1(l) &= n_1(l_o)(l/l_o)^2 \\ n_2(l) &= n_2(l_o)(l/l_o)^2 \\ A(l) &= A(l_o)(l/l_o)^2 \end{aligned}\right\} \qquad (105)$$

where l_o is the core scaling reference size.

Under this scaling law equations (102) and (103) show that:

$$P_R(l) = P_R(l_o)(l/l_o) \qquad (106a)$$

$$P_G(l) = P_G(l_o)(l/l_o)^{-4} \qquad (107a)$$

Furthermore, letting P_s represent the spacefactor-frequency product $F_s f$, we have from equation (104b) that

$$P_s(l) = P_s(l_o)(l/l_o)^{-4} \tag{108a}$$

The three quantities

$$P_R(l_o) = \frac{\left[v_o\right]}{3\pi S_w} F_{w1}(l_o) \tag{109}$$

$$P_G(l_o) = \frac{r_{21}}{s_{21}} \cdot \frac{\left[v_o\right]}{6\pi^2 \mu_o S_w n_2(l_o) A(l_o)} \tag{110}$$

$$P_s(l_o) = \frac{\left[v_o\right]}{6\pi B_r n_1(l_o) A(l_o) Z} * \tag{111}$$

are constants fixed by the windings of the reference core.* Thus the performance of a core of reference size l_o is given by the three simultaneous equations

$$Rf = P_R(l_o) \tag{112}$$

$$Gf^2 = P_G(l_o) \tag{113}$$

$$F_s f = P_s(l_o) \; ; \; 0 < F_s \leq \hat{F}_s < 1 \tag{114}$$

in terms of the winding constants $P_R(l_o)$, $P_G(l_o)$, $P_s(l_o)$ and the design variable F_s. $\hat{F}_s$ represents the maximum space-factor that can be achieved with a given output winding. Over the range of values permitted for F_s, R and G are unique functions of f.

In the case of a core of size l scaled from the reference core in accordance with (105), we have from (106a), (107a) and (108a)

$$Rf = P_R(l_o)(l/l_o) \tag{106b}$$

$$Gf^2 = P_G(l_o)(l/l_o)^{-4} \tag{107b}$$

$$F_s f = P_s(l_o)(l/l_o)^{-4} \tag{108b}$$

The presence of the quantity F_s in the left member of (108b) implies that it is independent of l. This is so because F_s is invariant to the scaling process defined by (105). To show this we refer to Fig. 79 in which the shaded area A_w shows the portion of the total cross-section of the output winding that is taken up by wire, and is therefore not available to core material. Then, if we make the assumption that the area available to the core material is some constant fraction of $A - A_w$, we have

$$F_s = \frac{A_m}{A} \sim \frac{A - A_w}{A} \sim \frac{l^2}{l^2} = \text{constant} \tag{109}$$

It is now possible to solve (106b), (107b) and (108b) for three design constants which, for a

* Z is given the value for which S_w has been evaluated.

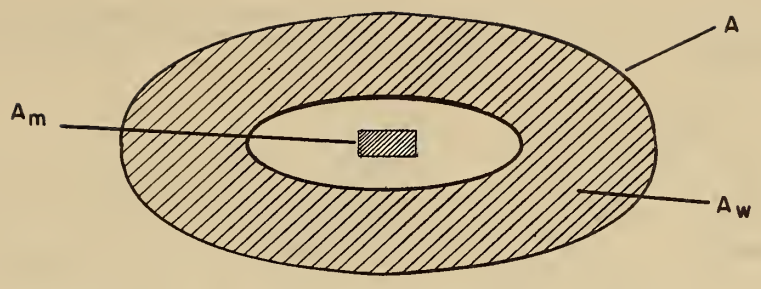


Figure 79. Core cross-section showing total winding-enclosed area A; winding-filled area A_w; and magnetic material cross-sectional area A_m

given F_s, will determine G, R, and $1/l_o$ as functions of f for members of the class of cores obtainable by scaling from the reference core. Multiplying (106b) by the fourth-root of (108b) gives the first constant, called the resistance-frequency constant:

$$p_R = Rf^{5/4} = P_R(l_o)\left[P_s(l_o)/F_s\right]^{1/4} \tag{115}$$

Dividing (107b) by (108b) gives the second design constant, called the gain-frequency constant:

$$p_G = Gf = \frac{P_G(l_o)}{P_s(l_o)/F_s} \tag{116}$$

p_G resembles the common "gain-bandwidth product" in that all sub-harmonics of f are transmitted, and constitute a "band" of discrete frequencies from zero to f. The third design constant, the size-frequency constant, is obtained directly from (108a):

$$p_l = (1/l_o)f^{1/4} = \left[P_s(l_o)/F_s\right]^{1/4} \tag{117}$$

Once the reference-core design constants $P_R(l_o)$, $P_G(l_o)$, $P_s(l_o)$, l_o and the spacefactor F_s have been fixed, it is seen that G, R and l are uniquely determined by f. The curves in Figure 80 show how R, G and $1/l_o$ vary with frequency, subject to scaling in accordance with equations (105), taking as the reference design the 10-wrap-, 0.150 inch diameter core having n_1 = 100 turns and n_2 = 200 turns. The design constants used in plotting these curves were calculated as follows:

From an earlier section

$P_R(l_o) = 3 \times 10^8$ ohms-sec^{-1}

$P_G(l_o) = 2 \times 10^{13}$ sec^{-2}

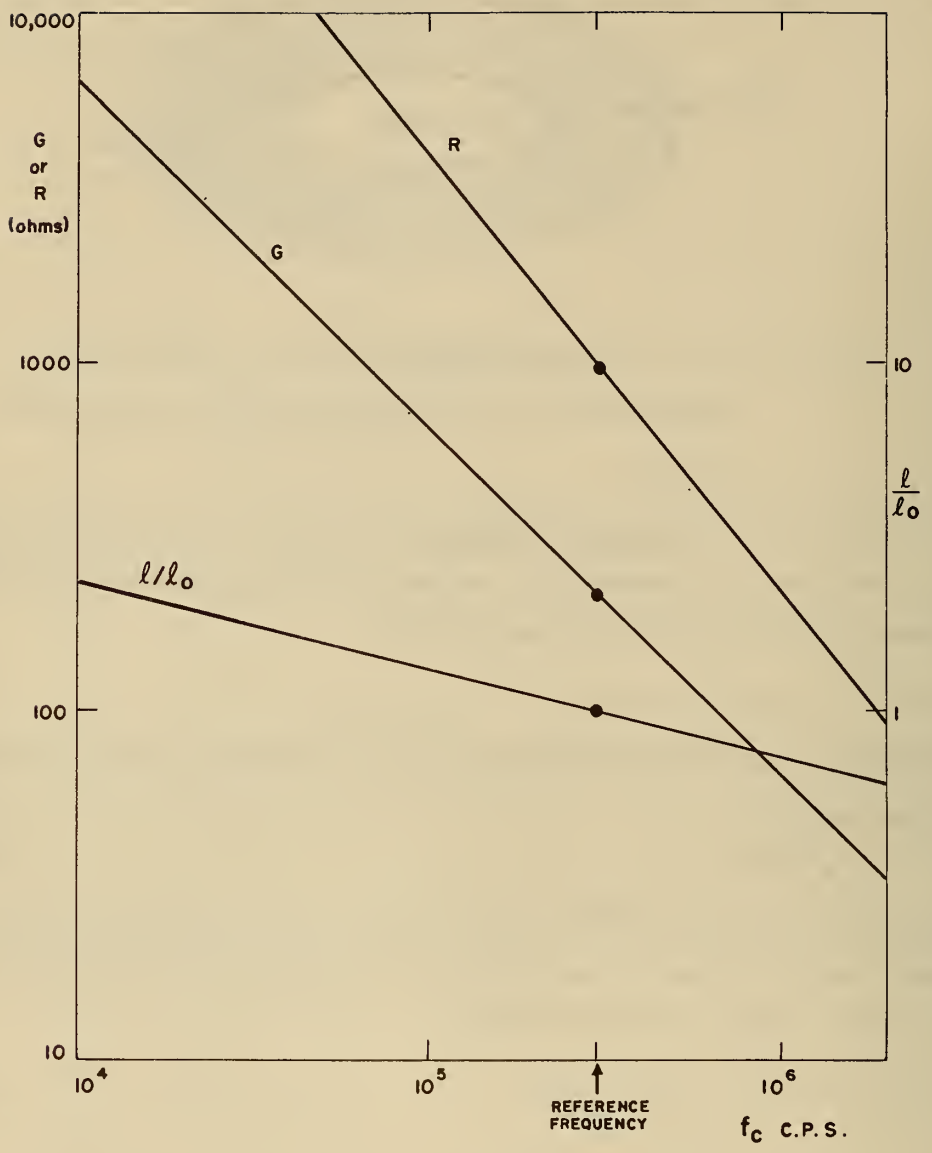


Figure 80. Magnetic amplifier core switching resistance R. current-gain G, and relative size $1/1_o$, versus frequency when the design is scaled in accordance with equations (105). 1_o = 0.150 inch.

F_s = 0.04, and from (111) setting Z = 1,

$P_s(l_o)$ = 1.22×10^4 sec^{-1}

Using these values,

$$p_R = (3 \times 10^8) \left[1.22 \times 10^4/.04\right]^{1/4}$$

$$= (3 \times 10^8)(23.6) = 71 \times 10^8 \text{ ohms-sec}^{-5/4}$$

$$p_G = 2 \times 10^{13}/30.5 \times 10^4$$

= 65 megacycles per second

$$p_l = \left[1.22 \times 10^4/.04\right]^{1/4}$$

$$= 23.6 \text{ sec}^{-1/4}$$

12.2 The Gain of the Input Circuit

Having found expressions for the gain and input resistance of the magnetic output stage, we now wish to determine the current gain of the Transmag input circuit. This portion includes the input power-diode D_{pi}, and the peak-saturating emitter follower.

We define the gain of this circuit to be

$$G_i = \hat{i}_c/i_p, \tag{118a}$$

where $\hat{i}_c$ is the core input peak current, and i_p is the least value of the current that must flow in one input AND-gate in order to properly transmit a ONE to the input circuit. We first consider the case for which i_p is constant* throughout the clock cycle.

Figure 81 shows the Transmag amplifier driven by one AND-gate through the essential OR-diode D_2. From the figure,

$$i_p = i_b + i_D, \tag{119}$$

where i_b is the transistor base current, and i_D is the current in the input power diode D_{pi}. More particularly, since i_p is constant, we require that

$$i_p = \hat{i}_b + I_D \tag{120}$$

where $\hat{i}_b$ is the maximum value of i_b, and I_D is the minimum permissible value of i_D. In evaluating i_b and I_D two cases must be considered:

1. During the rise of the clock wave, for $v < V_p$, and
2. Around the peak of the clock wave, when $v > V_p$.

We first find $\hat{i}_b = \hat{i}_{b1}$ for case 1. To do this we make use of an equivalent circuit for the input impedance of an emitter-follower derived in Appendix VI.

The circuit is shown in Figure VI-3, in which r_b is the transistor base resistance, R_L is the complete emitter-follower load, ω_{ab} is the radian alpha-cutoff (0.707) frequency of the transistor,

* i_p is effectively constant if V_p is much larger than v_o.

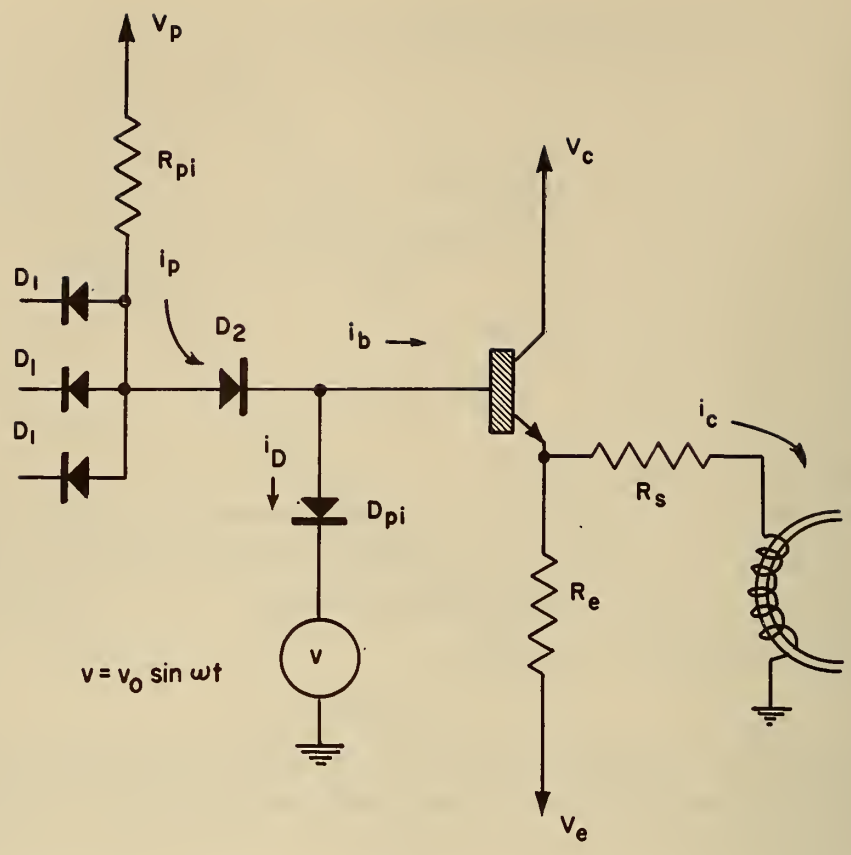


Figure 81. Important currents in the Transmag digital amplifier

and β_o is its low-frequency small-signal "beta". The reactance of the virtual capacitance C_i is

$$X_i = -jR_L \omega_{ab}/\omega \tag{121}$$

and r_b is normally under 100 ohms. Therefore, at very low frequencies for which $\omega_{ab}/\omega \gg 1 + \beta_o$, the input impedance of the emitter-follower is effectively $(1 + \beta_o) R_L$. But we are principally concerned with the reverse case, for which $\omega_{ab}/\omega < 1 + \beta_o$. In this case the $(1 + \beta_o)R_L$ branch can be ignored. Then, neglecting r_b in comparison with R_L, the transistor input impedance is as shown in Figure 82, driven by a voltage $v_b = v_o \sin \omega t$. Therefore, the peak value of i_{b1} is

$$\hat{i}_{b1} = \frac{v_o}{\sqrt{R_L^2 + X_i^2}} = \frac{v_o}{R_L\sqrt{1 + (\omega_{ab}/\omega)^2}}$$

$$\simeq \frac{\omega}{\omega_{ab}} \cdot \frac{v_o}{R_L}, \quad \text{for } \omega/\omega_{ab} \leq 1/2 \tag{122}$$

Thus $\hat{i}_{b1}$ is given by (122) over the range of ω/ω_{ab} indicated. Then, since the emitter-follower peak output current equals v_o/R_L, the current-gain of the emitter follower itself is

$$G_F = \frac{v_o/R_L}{\hat{i}_{b1}}$$

$$= \omega_{ab}/\omega, \text{ for } (1+\beta_o)^{-1} < \omega/\omega_{ab} < 1/2 \qquad (123)$$

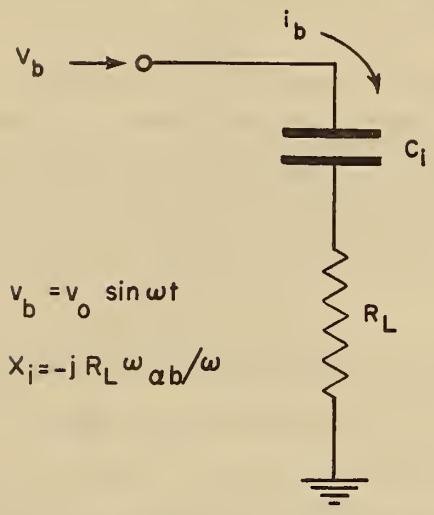


Figure 82. Approximate equivalent circuit for the emitter-follower input impedance

However, to get G_i we must still evaluate I_D and $\hat{i}_c$. Using equation (97)

$$\hat{i}_c = 2 v_o/3R_c \qquad (124)$$

Then, if R_e is set equal to $3R_c/2$, R_L equals $(1/2)(3R_c/2)$, and

$$v_o/R_L = 2(2v_o/3R_c) = 2\hat{i}_c \qquad (125)$$

Making use of (125), (122) and (119), equation (118a) becomes

$$G_i = \frac{1}{2\frac{\omega}{\omega_{ab}} + \frac{I_D}{\hat{i}_c}}; \qquad (118b)$$

and from (124),

$$G_i = \frac{1}{\frac{2\omega}{\omega_{ab}} + \frac{3R_c I_D}{2 v_o}}, \text{ for } (1+\beta_o)^{-1} < \omega/\omega_{ab} < 1/2 \qquad (118c)$$

So far as case 1 is concerned, the value chosen for I_D is governed by the desirability of keeping the impedance of the source that drives the emitter-follower low in comparison with the

emitter-follower input impedance. This source impedance is essentially the forward resistance of D_{pi}. I_D should equal or exceed the value I_{Do}, where I_{Do} is the current at which the slope of the diode forward volt-ampere characteristic is 100 ohms, say. An I_D of 1 or 2 milliamperes is ordinarily sufficient for this purpose, but when case 2 is considered, it may happen that I_D must be given a larger value.

Under case 2, D_{pi} is back-biased, and $\dot{v}_b = 0$; therefore $i_D = 0$, and there is no charging current needed for C_i. But the base-collector junction is forward-biased with the result that $i_p \left[= i_{b2}\right]$ flows into the base, and gives rise to the stored charge carriers that produce the desired emitter-follower volt-second transfer function. To produce enough of these carriers i_p must not fall below some value I_p. Thus from case 2 we have the requirement that

$$i_p = \hat{i}_{b1} + I_D \geq I_p \tag{126a}$$

When the requirement of case 1, is added to (126a) we have finally that

$$I_p - \hat{i}_{b1} \leq I_D \geq I_{Do} \tag{126b}$$

Ordinarily I_p will determine the value of I_D, because $I_p - \hat{i}_{b1}$ is likely to exceed the value I_{Do} required to keep the forward resistance of D_{pi} equal to 100 ohms. In this case G_i is obtained simply by setting $i_p = I_p$ in (118a),

whence

$$G_i = \frac{\hat{i}_c}{I_p} = \frac{2v_o}{3R_c I_p}, \quad \text{for } I_p - \hat{i}_{b1} > I_{Do} \tag{127a}$$

Otherwise, $I_D = I_{Do}$ and (118c) gives

$$G_i = \frac{1}{\frac{2\omega}{\omega_{ab}} + \frac{3R_c I_{Do}}{2v_o}}, \quad \text{for } I_p - \hat{i}_{b1} \leq I_{Do} \tag{127b}$$

In the unlikely case that $I_p - \hat{i}_{b1}$ is less than I_{Do}, (127b) still applies, because I_D must not be less than I_{Do}.

12.2a Restrictions on ω / ω_{ab}

In general, we require that

$$I_D = i_p - \hat{i}_{b1} \geq I_{Do} \tag{128}$$

From this, using (122) and (125) we get

$$\frac{\omega}{\omega_{ab}} \leq \frac{i_p - I_{Do}}{2\hat{i}_c} \tag{129a}$$

Equation (129a) shows that any value for ω / ω_{ab} is permissible provided i_p is made large enough. But from (123), $(\omega / \omega_{ab})^{-1} = G_F$, so that only fractional values for ω / ω_{ab} need be considered. Furthermore, for simplicity we require that $\omega / \omega_{ab} \leq 1/2$, which is the range of validity of (122).

Ordinarily $I_p - \hat{i}_{b1} > I_{Do}$, and i_p is set equal to I_p. In this case the range of ω / ω_{ab} is given by

$$\frac{\omega}{\omega_{ab}} \leq \frac{I_p - I_{Do}}{2\hat{i}_c} \tag{129b}$$

or by

$$\frac{\omega}{\omega_{ab}} \leq \frac{I_p - I_{Do}}{4v_o / 3R_c} \tag{129c}$$

When ω/ω_{ab} satisfies (129b, c) the gain of the Transmag input circuit is said to be limited by the transistor storage-requirements. Conversely, when $\hat{i}_{b1}$ is so large that $I_p - \hat{i}_{b1} < I_{Do}$, that is to say when $I_p < I_{Do} + \hat{i}_{b1}$ so that i_p must be made greater than I_p in order to satisfy (128), then the gain of the input circuit is said to be alpha-cutoff limited.

12.2b The Case in Which V_p is only a Few Times Larger than v_o

The foregoing derivations have been based on the assumption that i_p remains constant throughout the clock cycle. In practice, unless a nonlinear R_{p1} is used, i_p is kept constant by making V_p large compared with v_o.*

However, at the price of a small loss in current-gain, a smaller V_p can be used. i_p is then no longer constant, but varies in accordance with

$$i_p = \frac{V_p - v_o \sin \omega t}{R_{p1}} \tag{130}$$

Now for the propagation of information we are concerned only with the value of i_p during the positive half cycle of the clock, i.e., for $\sin \omega t \geq 0$. More particularly, we need to know its value at $\omega t = 0$; and at $\omega t = \pi/2$. Furthermore, for each AND-gate that a core must "hold down" it must absorb a current i_{po} equal to the value of i_p at $\omega t = 0$. Then, for the sake of simplicity, if we assume the case of relatively high emitter-follower gain, $G_F = \omega_{ab}/\omega \geq 4$, we can take the phase angle of $R_L + X_i$ to be nearly $\pi/2$, with the result that i_{b1} assumes its maximum value $\hat{i}_{b1}$ near $\omega t = 0$. Thus, paralleling (128), we require that

$$I_D = i_{po} - \hat{i}_{b1} \geq I_{Do} \tag{131}$$

But in addition, we must require that i_p at $\omega t = \pi/2$ be at least equal to I_p. Now at $\omega t = \pi/2$, using (130), we have

---

* i_p may also be kept constant by superimposing the voltage $v = v_o \sin \omega t$ upon a d-c component, giving a varying V_p.

$$i_p(\pi/2) = \frac{V_p}{R_{p1}}\left(1 - \frac{v_o}{V_p}\right) = i_{po}\left(1 - \frac{v_o}{V_p}\right) \tag{132}$$

Then if we set $i_p(\pi/2) = I_p$, and assume the circuit gain to be storage-requirement limited (since we have assumed $\omega_{ab}/\omega \geqq 4$), we may write

$$i_{po} = I_p\left(1 - v_o/V_p\right)^{-1} \tag{133}$$

From this, using

$$G_i = \hat{i}_c/i_{po} \tag{134}$$

which parallels (118a), we have

$$G_i = \frac{\hat{i}_c}{I_p\left(1 - v_o/V_p\right)^{-1}} = \frac{2v_o\left(1 - v_o/V_p\right)}{3R_c I_p} \tag{135}$$

$$\text{for } I_p\left(1 - v_o/V_p\right)^{-1} - \hat{i}_{b1} > I_{Do},$$

which parallels (127a).

Finally, for this case, the range of ω/ω_{ab} is given by

$$1/4 \geqq \omega/\omega_{ab} \leqq \frac{I_p\left(1 - v_o/V_p\right)^{-1} - I_{Do}}{4v_o/3R_c} \tag{136}$$

This parallels (129c), but is a little less restrictive on ω/ω_{ab}, by reason of the factor $\left(1 - v_o/V_p\right)^{-1}$.

In no case, however, should ω/ω_{ab} exceed values for which the emitter-follower is unilateral. In an enumeration of some of the benefits acquired through the use of an emitter follower, point five in Section 7 states that the emitter-follower serves as a unilateral buffer to provide further isolation between the magnetic elements. The emitter-follower is unilateral when working between a signal source of low impedance, relative to its own input impedance, and a load impedance which is high relative to its own output impedance. Because the source impedance is effectively equal to the forward resistance r_D of the input power diode D_{pi}, the requirements for unilateral signal transmission by the emitter-follower are:

$$r_{Do} << Z_{input} \tag{137a}$$

$$R_L >> Z_{output}, \tag{138a}$$

where r_{Do} is the value of r_D at the forward current I_{Do}.

Then, confining ω/ω_{ab} to the range $(\omega + \beta_o)^{-1} < \omega/\omega_{ab} \leqq 1/4$, and neglecting r_b, (137a) may be written

$$r_{Do} << \left| -jR_L \right| \omega_{ab}/\omega \tag{137b}$$

And, making use of the output equivalent circuit of the emitter-follower derived in Appendix VII, (138a) may be written

$$R_L >> \left| j\left(r_{Do} + r_b\right) \right| \omega/\omega_{ab}. \tag{138b}$$

Finally, combining (137b) and (138b), the requirements for unilateral signal transmission are

$$\frac{R_L}{r_b + r_{Do}} >> \frac{\omega}{\omega_{ab}} << \frac{R_L}{r_{Do}}$$

Or, equivalently

$$\omega/\omega_{ab} << R_L (r_b + r_{Do})^{-1} \tag{139}$$

in the range $(1 + \beta_o)^{-1} < \omega/\omega_{ab} \leq 1/4$.

Practically speaking (139) may then be written as

$$\omega/\omega_{ab} \leq R_L/10(r_b + r_{Do}) \tag{140a}$$

or, when $R_L = 3R_c/4$, as

$$\omega/\omega_{ab} \leq R_c/13 (r_b + r_{Do}) \tag{140b}$$

Then, using $r_b = 100$ ohms, $r_{Do} = 100$ ohms and $R_c = 1000$ ohms at 300 kc, (See Figure 80) gives $R_c/13(r_b + r_{Do}) \simeq 2/5 > 1/4$. Therefore, for these values, (139) is satisfied throughout its range, and the emitter-follower is unilateral at least for $\omega/\omega_{ab} \leq 1/4$; that is to say, for $G_F = \omega_{ab}/\omega \geq 4$.

When the gain of the input circuit is storage-requirement limited, the maximum acceptable value for ω/ω_{ab} can easily be less than 1/4, however, depending upon R_L and I_p. In the experimental Transmag circuit it was found that good signal transmission was obtained using a CK760A transistor with $V_p = 25$ v., $R_{p1} = 5600$ ohms, $R_e = 680$ ohms, $v_o = 10$ volts, and $R_s = 470$ ohms, with a core for which $R_c = 750$ ohms and $i'_o = 1/2\ \hat{i}_c$.

In this case the range of ω/ω_{ab} can be calculated from

$$1/4 \geq \omega/\omega_{ab} \leq \frac{i_{po} - I_{Do}}{v_o / R_L}$$

in which $I_{Do} = 2$ ma. (for the diode used); $i_{po} = V_p/R_{p1} = 4.5$ ma.; and R_L is the resistance of R_e in parallel with the effective resistance of the branch containing R_s and the core. The resistance of this branch is, in the manner of (97)

$$\frac{1}{\hat{i}_c} \left[R_s \hat{i}_c + R_c (\hat{i}_c - i'_o) \right]$$

$$= \frac{1}{\hat{i}_c} \left[R_s \hat{i}_c + R_c (\hat{i}_c - \frac{1}{2} \hat{i}_c) \right]$$

$$= R_s + R_c/2 = 840 \text{ ohms.}$$

Then

$$R_L = \frac{(840)(680)}{840+680} = 375 \text{ ohms.}$$

and

$$1/4 \geq\!\!= \omega/\omega_{ab} \leq\!\!= \frac{4.5 \text{ ma.} - 2 \text{ ma.}}{27.5 \text{ ma.}}$$

$$\leq\!\!= 1/11.$$

This circuit functioned at a clock frequency of 300 kc; therefore the required range for

$f_{ab} \geq\!\!= 11(300 \text{ kc})$

$\geq\!\!= 3.3 \text{ mc.}$

The spread of f_{ab} for the CK760A is 3 to 5 mc.

Using (133) we calculate the minimum required storage current to be

$$I_p = i_{po}(1 - v_o/V_p)$$

$$= 4.5(1 - 10/25) = 2.7 \text{ ma.}$$

The gain of the emitter-follower was

$$G_F = \omega_{ab}/\omega = 11,$$

and the gain of the complete input circuit was

$$G_i = \frac{v_o/R_L}{i_{po}} = \frac{10/840}{4.5} = 2.6$$

For comparison we calculate the range of ω/ω_{ab} obtainable with $R_c = 1000$ ohms, $R_L = 3R_c/4$; and with all other parameters the same as before, including i_{po}. The lower limit on ω/ω_{ab} is given by

$$1/4 \geq\!\!= \omega/\omega_{ab} \leq\!\!= \frac{i_{po} - I_{Do}}{4 v_o 3 R_c}$$

$$\leq\!\!= \frac{4.5 - 2}{13} = 0.192;$$

or, since $0.192 < 1/4$, $\omega/\omega_{ab} \leq\!\!= 0.192$, and $f_{ab} \geq\!\!= 1.56$ mc,

$$G_F = \omega_{ab}/\omega \geq\!\!= 5.2, \text{ and}$$

$$G_i = \frac{2v_o/3R_c}{i_{po}} = \frac{6.6 \text{ ma}}{4.5 \text{ ma}} = 1.46$$

The assumed I_p of 2.7 ma for this case is probably larger than would actually be required. If a smaller value for I_p is allowed, a reduction in AND-gate power can be affected by using a faster transistor (to give more current gain) and reducing V_p or increasing R_{p1}.

12.2c The Dependence of Transistor Speed and Power Requirements upon Clock Frequency

It is useful to know how the minimum required alpha cut-off frequency $f_{\alpha bo}$ and the collector dissipation h must vary with clock frequency when the design of the core to be driven is scaled in accordance with equations (105) from the core for which the curves of Figure 80 were plotted. We assume fixed values for v_o, V_p, R_p, and, without justification other than that it seems possible, for I_p. Under these assumptions the power dissipated in the logic AND-gates is constant, and for the storage-limited case we have that

$$\hat{i}_{b1} = I_p (1 - v_o/V_p)^{-1} - I_{Do} = \text{constant.}$$

Then, from

$$G_F \hat{i}_{b1} = v_o/R_L = 4 v_o/ 3 R_c,$$

using (123),

$$\frac{\omega_{\alpha bo}}{\omega} = \frac{f_{\alpha bo}}{f} = \frac{4v_o}{3\hat{i}_{b1} R_c}$$

or,

$$f_{\alpha bo} = \frac{4v_o}{3 \hat{i}_{b1}} \frac{f}{R_c} \qquad (141)$$

Then, using (115),

$$f_{\alpha bo} = \frac{4v_o}{3 \hat{i}_{b1} p_R} f^{9/4} \qquad (142a)$$

for $f_{\alpha bo} \geq 2f$.

If we let v_o = 10 volts, V_p = 25 volts, I_{Do} = 2 ma., and I_p = 2.7 ma.

$$\hat{i}_{b1} = 2.7 (1 - 10/25)^{-1} - 2$$

$$= 4.5 \text{ ma.} - 2 \text{ ma.} = 2.5 \text{ ma.};$$

and, for the core design we are using, $p_R = 71 \times 10^8$, so that

$$f_{\alpha bo} = \frac{4(10)}{3(2.5 \times 10^{-3})(71 \times 10^8)} f^{9/4} \qquad (142b)$$

This is represented by the curve for $f_{\alpha bo}$ in Figure 83, along with curves for h_{ao}, the collector dissipation for the (unclamped) assertive amplifier for all ZEROs; and for h_{c1}, the dissipation for the assert-negate amplifier for all ONEs. The functions represented by these curves were derived as follows: In Appendix VIII h_{ao} is conservatively estimated to be

$$h_{ao} = 2(v_o^2/3 R_c),$$

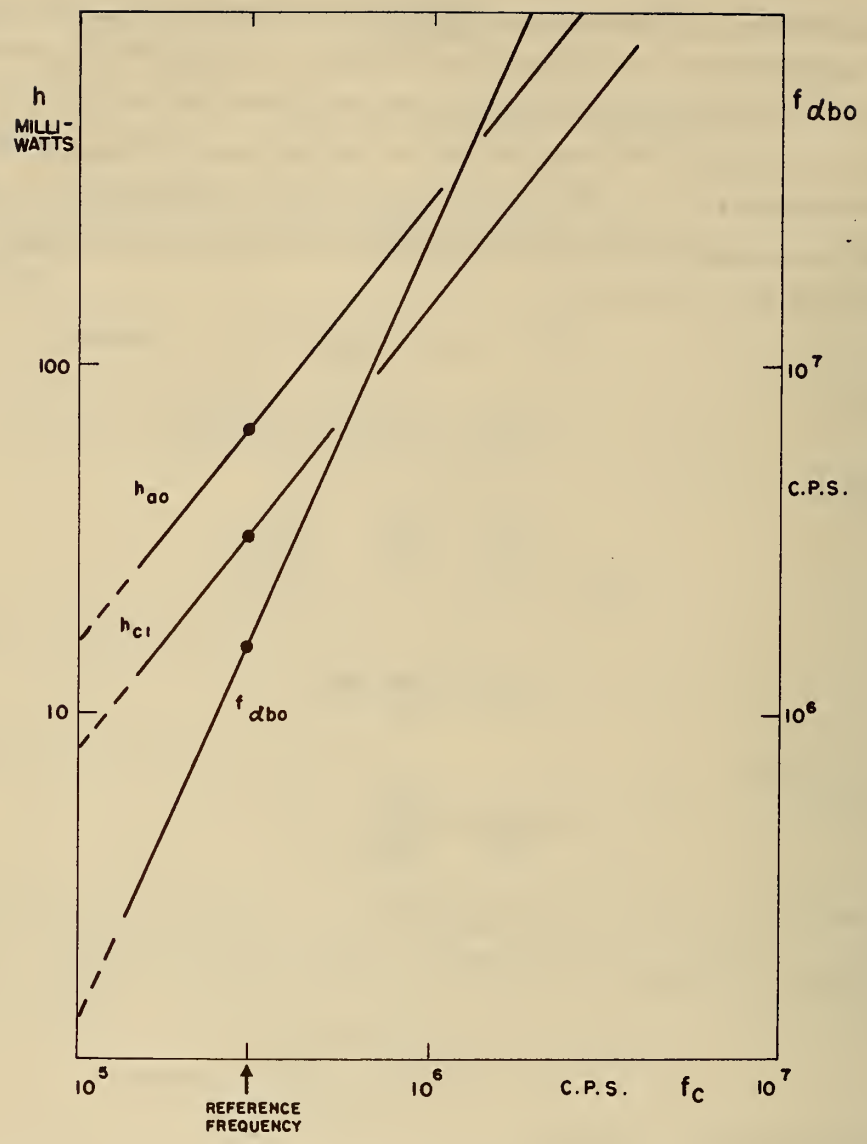


Figure 83. Transistor collector dissipations h_{ao} and h_{c1} versus clock frequency f_c, from Appendix VIII; and minimum-required alpha-cut-off $f_{\alpha bo}$ versus clock frequency for the core design used in Figure 80 and a nominal AND-gate current of 4.5 ma

from which, making use of (115),

$$h_{ao} = \frac{2v_o^2}{3 P_R} f^{5/4} \tag{143a}$$

$$= \frac{2(10)^2}{3(71 \times 10^8)} f^{5/4} \tag{143b}$$

h_{a1} is about one-half of h_{ao}.

Also in Appendix VIII h_{c1} is shown to be very nearly equal to $v_o^2/3\,R_c$, so that we may write

$$h_{c1} = \frac{v_o^2}{3\,p_R}\, f^{5/4} \qquad (144)$$

$$= h_{ao}/2$$

Furthermore $h_{co} \simeq 0$.

The low collector dissipation, the double output, and the economy of components of the assert-negate amplifier make it very attractive.

12.3 Additional Factors that Affect the Fan-Out N

Having gotten expressions for calculating the current gain of the Transmag digital amplifier, we wish to take up the remaining factors that affect the attainable fan-out.

In the first place we wish to point out that the kind of output branching shown in Figure 84 is ordinarily to be avoided,* particularly if many loads are to be driven. For, although it does minimize lead ground capacitance, this branching combines the load currents in a single long lead that may have a self-inductance greater than the core saturation inductance. During the transmission of a ZERO the volt-second signal developed across this inductance by the combined load currents may well exceed the threshold r_{21} and give rise to a false ONE at the load inputs.

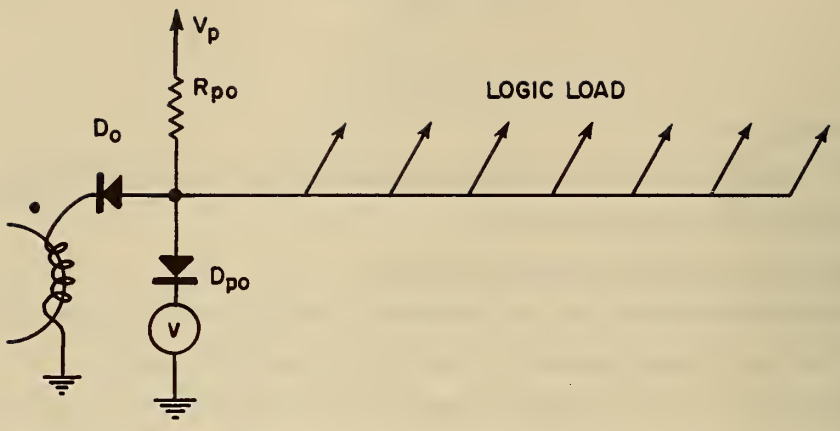
Figure 51 shows the proper manner of connecting the logic load to the Transmag amplifier. The output degenerate AND gate is located close to the core, and the signal is distributed through separate leads to the remote logic gates. The output gate provides the power to maintain the ONE signal across the combined lead ground capacitance ΣC_s. As was stated earlier, the insertion of the output gate is necessary because the magnetic element has a high impedance during the transmission of a ONE, and is therefore incapable of developing an acceptable signal across the lead ground capacitance. The output gate also serves to ZERO the core during the transmit half-cycle.

The branching shown in Figure 51 maximizes the lead capacitance that must be driven. Therefore the output gate pull-up resistor R_{po} must carry a current considerably larger than is required of the logic gate pull-ups R_{p1}. In fact the current in R_{po} must equal or exceed the value

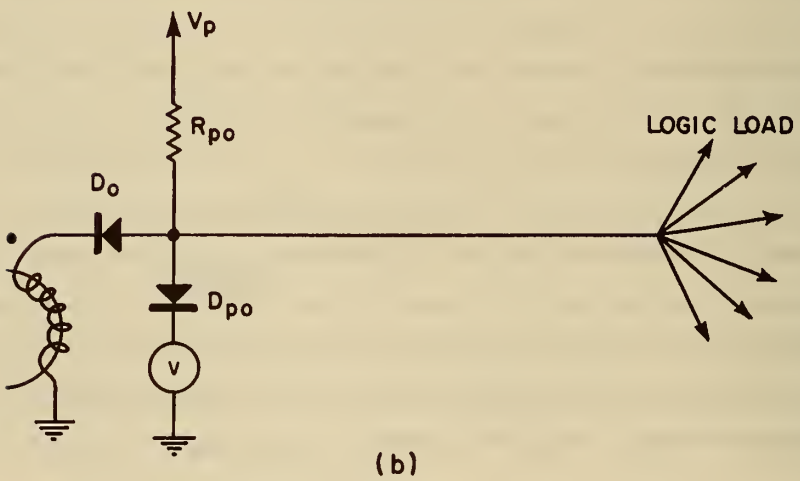
$$(\Sigma C_s)\left[\dot{v}\right]_{\text{maximum}} + I_o = \omega v_o \Sigma C_s + I_o$$

where I_o is the minimum current required to keep D_{po} conducting and to ZERO the core through its output winding.

* Unless a low-impedance line is used. Furthermore, the delay in this, or any other lead, should be small compared with $T/2$.



(a)



(b)

Figure 84. Ordinarily undesirable output branching

The attainable logical fan-out for the Transmag digital amplifier is than

$$N = \frac{Gi_{po} - (\omega v_o \Sigma C_s + I_o)}{i_{po}}$$

$$= G - \frac{\omega v_o \Sigma C_s + I_o}{i_{po}} \qquad (145)$$

where i_{po} is the minimum required value of the current in R_{pl} when sin $\omega t = 0$. C_s is the ground capacitance of a fan-out branch, and G is the current gain of the amplifier.

It might be thought that the output gate could be eliminated by increasing the currents in the logic gate pull-ups R_{pl}. This could be done provided the current in each logic pull-up were made large enough to drive all the lead capacitance ΣC_s. But if the number of branches is large, or if the branches are long, the current needed to drive ΣC_s may be much larger than the minimum required logic gate current i_{po}. In this case the number of such gates that can be driven by the amplifier is drastically reduced, i.e., the fan-out N is much smaller than the amplifier current gain G. It is not sufficient to make each logic gate capable of driving only its own input leads, because it may happen, in the logical functioning of the circuit, that all gates in the logic load, except one, simultaneously receive ZEROs on one or more of their inputs. These gates are therefore held at ground potential. Then, if a ONE is to be transmitted to the remaining gate, that gate must drive the total capacitance ΣC_s.

Figure 85 shows an alternative scheme of interconnection that eliminates the output gate without such a drastic reduction of fan-out. In this scheme, the diodes of the logic gates are located at the transmitting amplifier instead of with the pull-up resistors R_{pl}. Inspection of the diagram shows that the current in each logic AND-gate must be made large enough to drive $C_s + \Sigma C'_s$, the stray capacitance to ground associated with all its own input leads. But no gate need be capable of driving ΣC_s.

In the design of the logic gates in this scheme there are two possibilities:

1. An advance knowledge of the ground capacitance of each input lead is obtained, and the pull-up R_{pl} of each gate is given the proper value to drive the total input lead capacitance for that gate.
2. A maximum possible lead-capacitance for each gate is assumed, and the gate is designed for this. There are two possibilities for this procedure:
   a. A maximum capacitance for each gate based on the number of input leads to that gate is assumed, or
   b. A maximum capacitance, disregarding the number of inputs, is assumed for all gates.

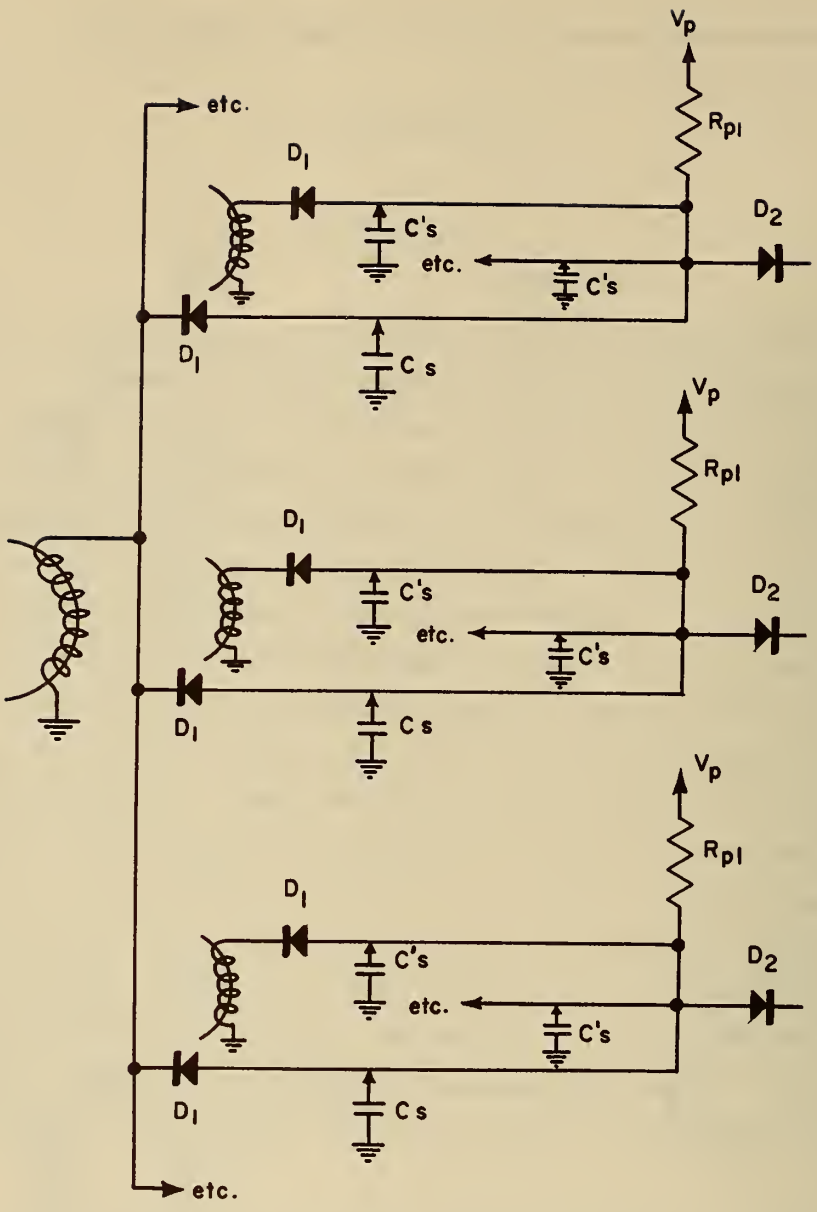


Figure 85. Lead capacitances involved when no output AND-gate is used

Procedure 2b requires the least computation in assembling digital circuits from packaged gating assemblies; but it gives the smallest fan-out because of the conservatively large value of current carried in each logic pull-up. If the maximum number of AND-gate inputs is 10 or more, N will be appreciably smaller than G.

Procedure 1 requires the greatest amount of computation, and results in the least uniformity and interchangeability of packaged assemblies. The design of each gate is tailored to fit its particular location in the logic net. The ratio of N to G for this method, while greater than for

2a and 2b, will generally be smaller than for the scheme of Figure 51. The reason for this can be seen from Figure 85, where the transmitting amplifier must be able to handle a total logic-gate pull-up current sufficient to drive, not only ΣC_s, but also $\Sigma\Sigma C'_s$. The fan-out reduction becomes significant when the additional current required in each logic-gate to drive its total input lead capacitance $C_s + \Sigma C'_s$ equals or exceeds the current i_{po} required to drive the following amplifier. The inferiority of the method of Figure 85 to that of Figure 51 becomes more pronounced as the number of inputs per logic AND-gate increases.

Although it requires the addition of an output AND gate that performs no logical function, the method of Figure 51 is superior to that of Figure 85 because:

1. All the logic-gate pull-ups R_{pl} carry the same current.
2. This current need be no greater than is required to drive the digital amplifier.
3. The difference between G and N, resulting from the need to spend amplifier power in driving lead ground capacitance, is less.

13. THE TEST COMPUTER

The test computer was constructed in modularized bread-board form using the basic circuits shown in Figure 86a, and diagrammed in Figure 86b. In tests of these circuits, an OR-gate fan-in of 4 with AND-gate fan-ins of over 5 each were easily obtained. A conservative fan-out figure was 30. The total power consumption of an amplifier was around 0.5 watt, and the power per singly-loaded logic AND-gate was 0.15 watt. Over 80 digital amplifiers were used.

The organization of the machine, shown in Figure 87, was suggested by S. Greenwald. Figures 88, 89, 90 and 91 show the details of the blocks in Figure 87.

An over-size central clock source generated 24 watts of 300 kc, amplitude-regulated power at a level of 20 volts rms. Approximately 4 watts of this were distributed to the computer through nine ferrite-core transformers whose center-tapped secondaries provided the two-phase, 7 volt clock for each of nine racks of up to 16 amplifiers each. An attractive alternative to this system would be the use of small local transistor clock power amplifiers driven by a central low-power clock.

In operation the computer, upon receiving start pulses, alternately adds two six-bit binary numbers entered by means of toggle switches on the control panel; and compares the sum, bit-by-bit, with a check-word, also inserted manually. The operations are serial. Errors revealed in the compare operation are counted by a three-stage binary counter included in the computer. A seven-stage shift register using dynamic flip-flops serves as the machine's internal store.

Figure 92 is a front view of the computer. Figure 93 is a close view showing the control panel and the modularized bread-board construction. The small white "buttons" contain the potted cores.

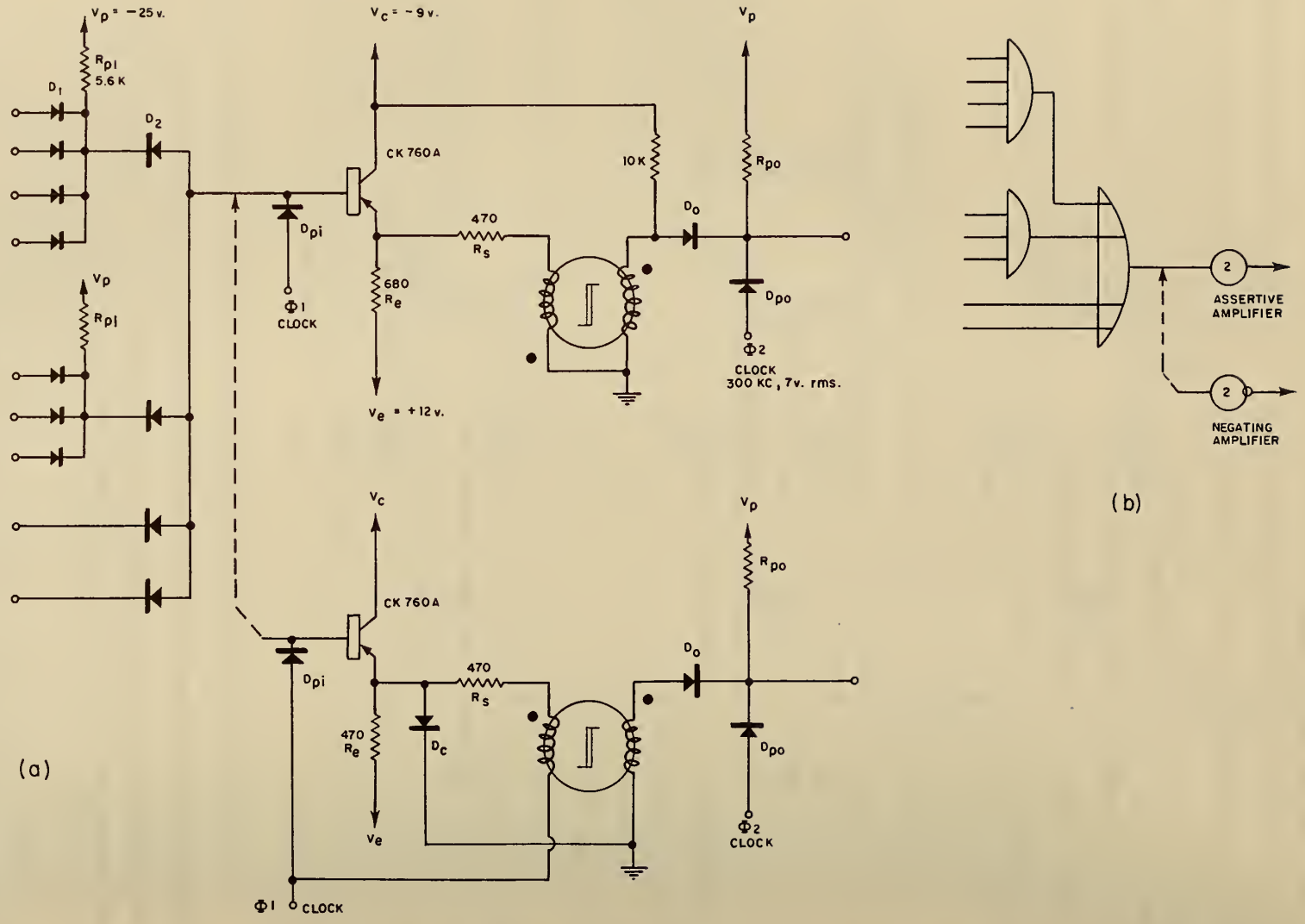


FIGURE 86. (a) TRANSMAG DIGITAL AMPLIFIERS AND TYPICAL GATING USED IN THE TEST COMPUTER. (b) LOGICAL SYMBOL FOR a.

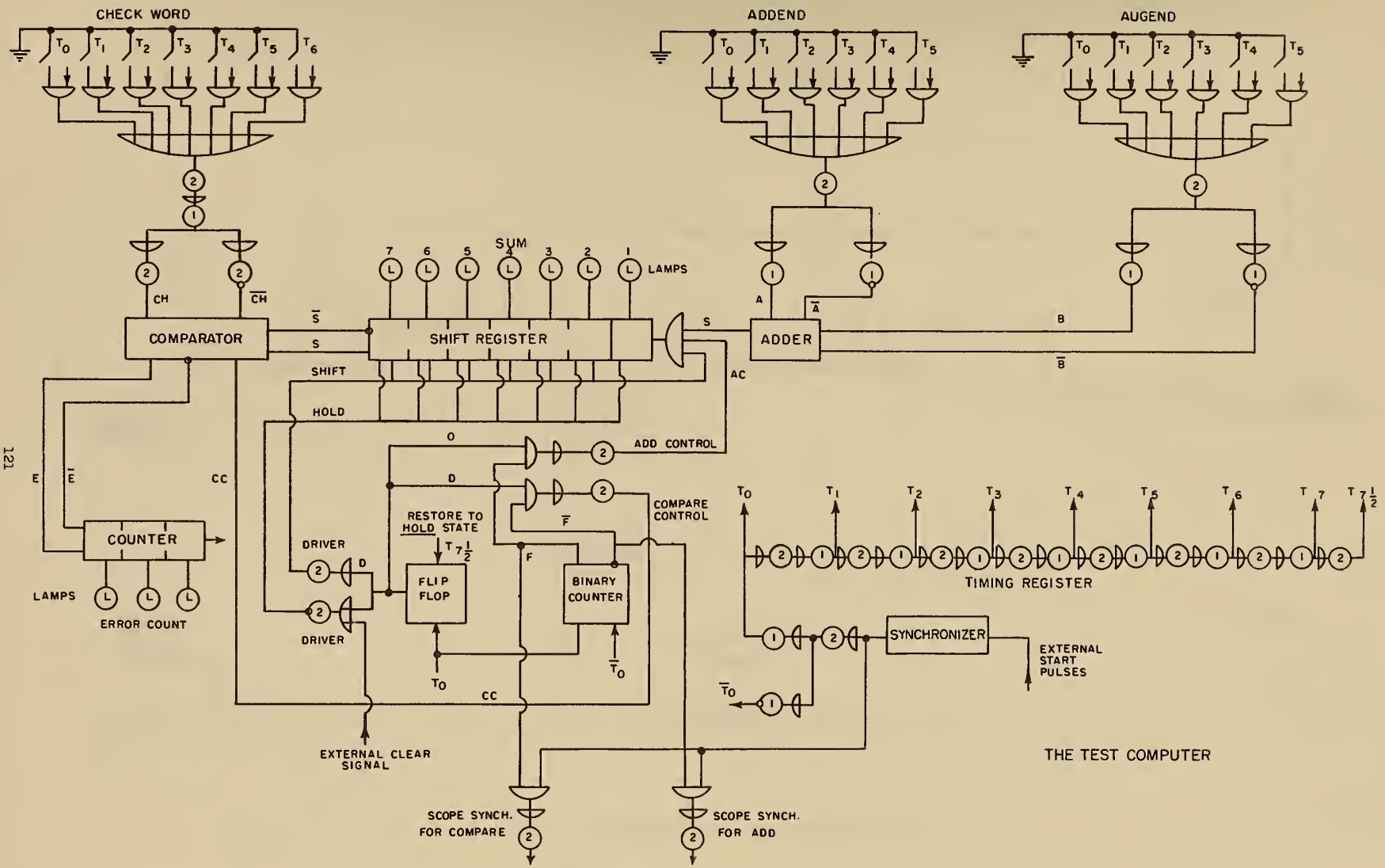


FIGURE 87. ORGANIZATION OF THE TEST COMPUTER

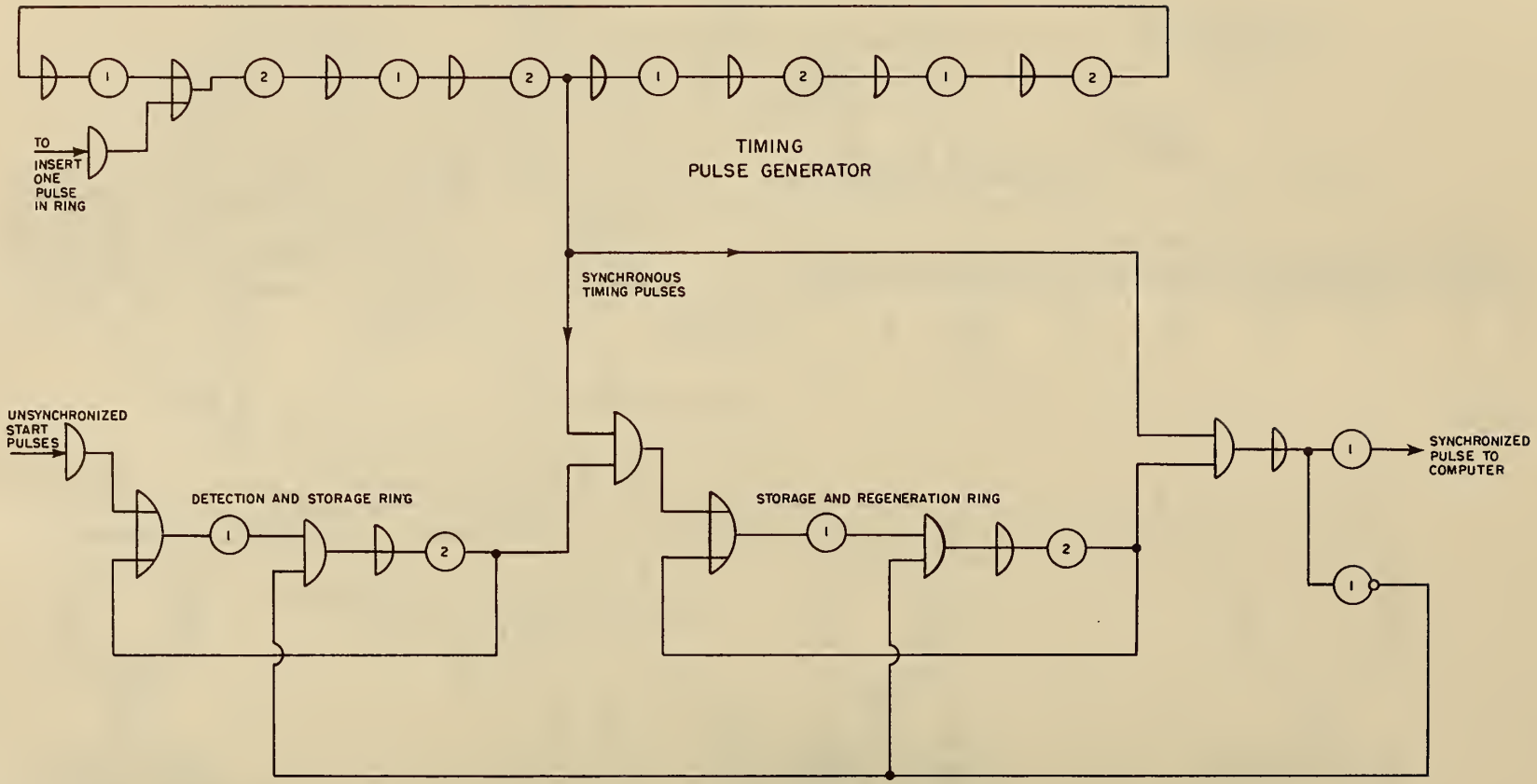


FIGURE 88. THE SYNCHRONIZER

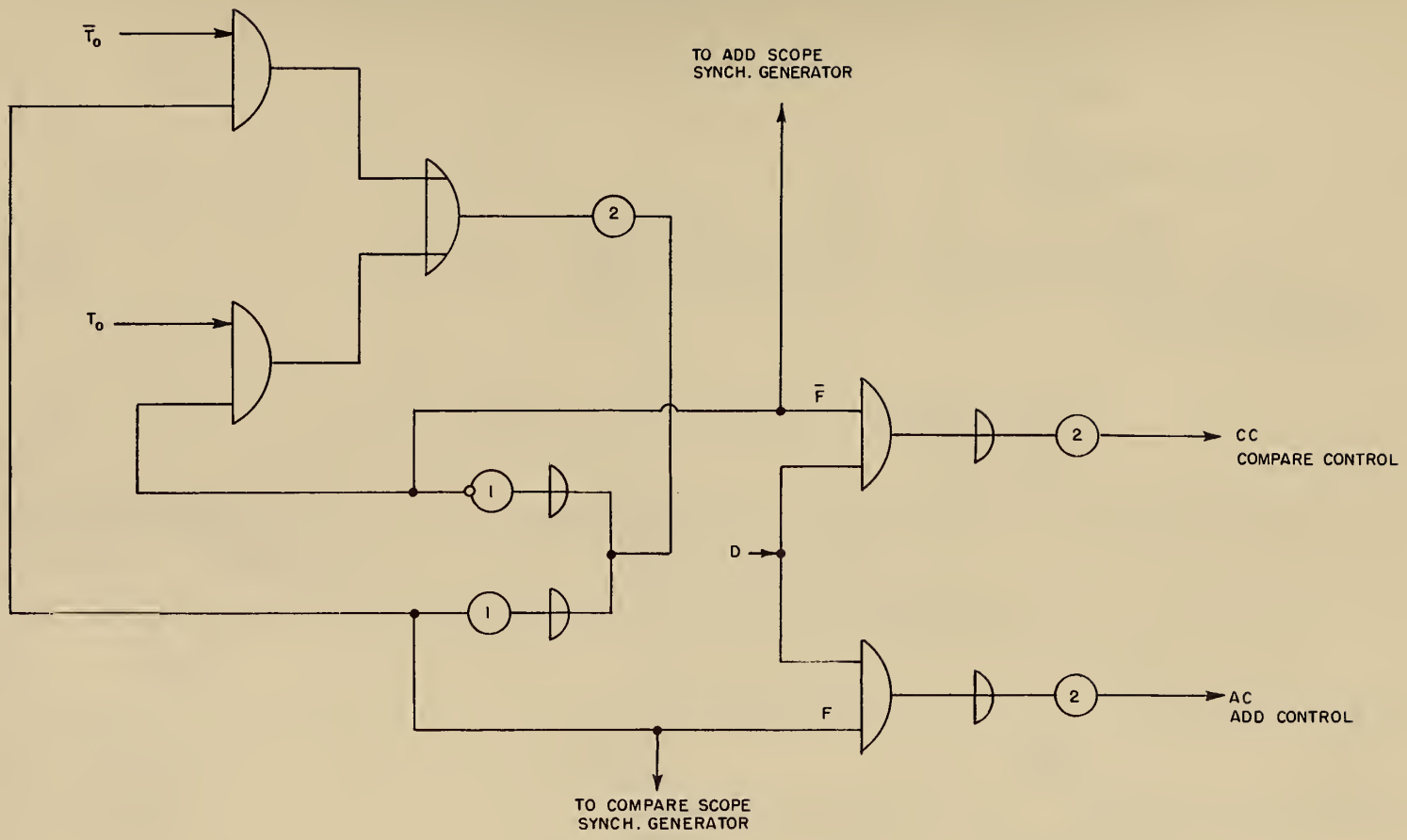


FIGURE 89. BINARY CYCLE-COUNTER AND OPERATION CONTROL GENERATOR

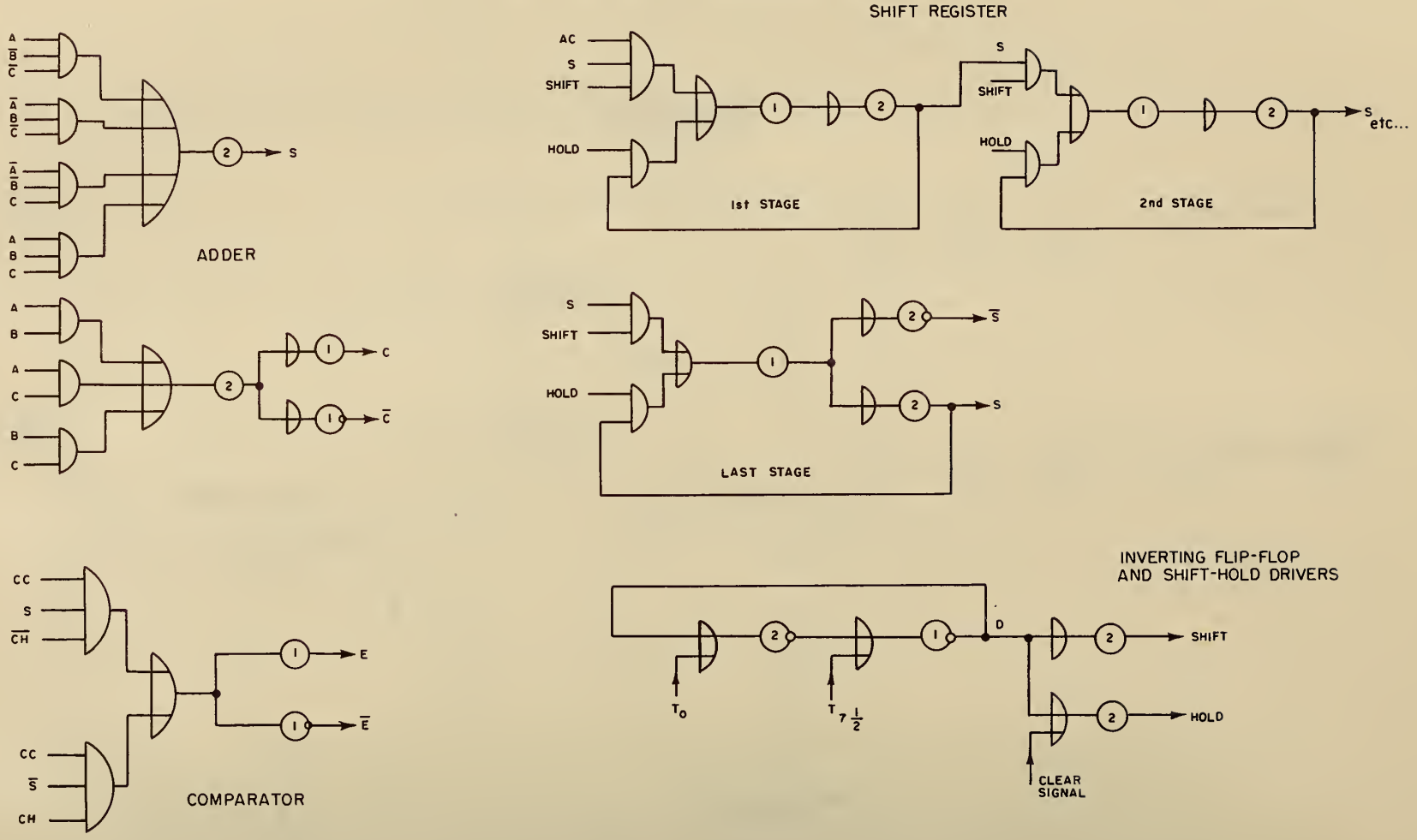


FIGURE 90. ADDER, COMPARATOR, SHIFT-REGISTER STAGES, AND SHIFT-HOLD CIRCUIT

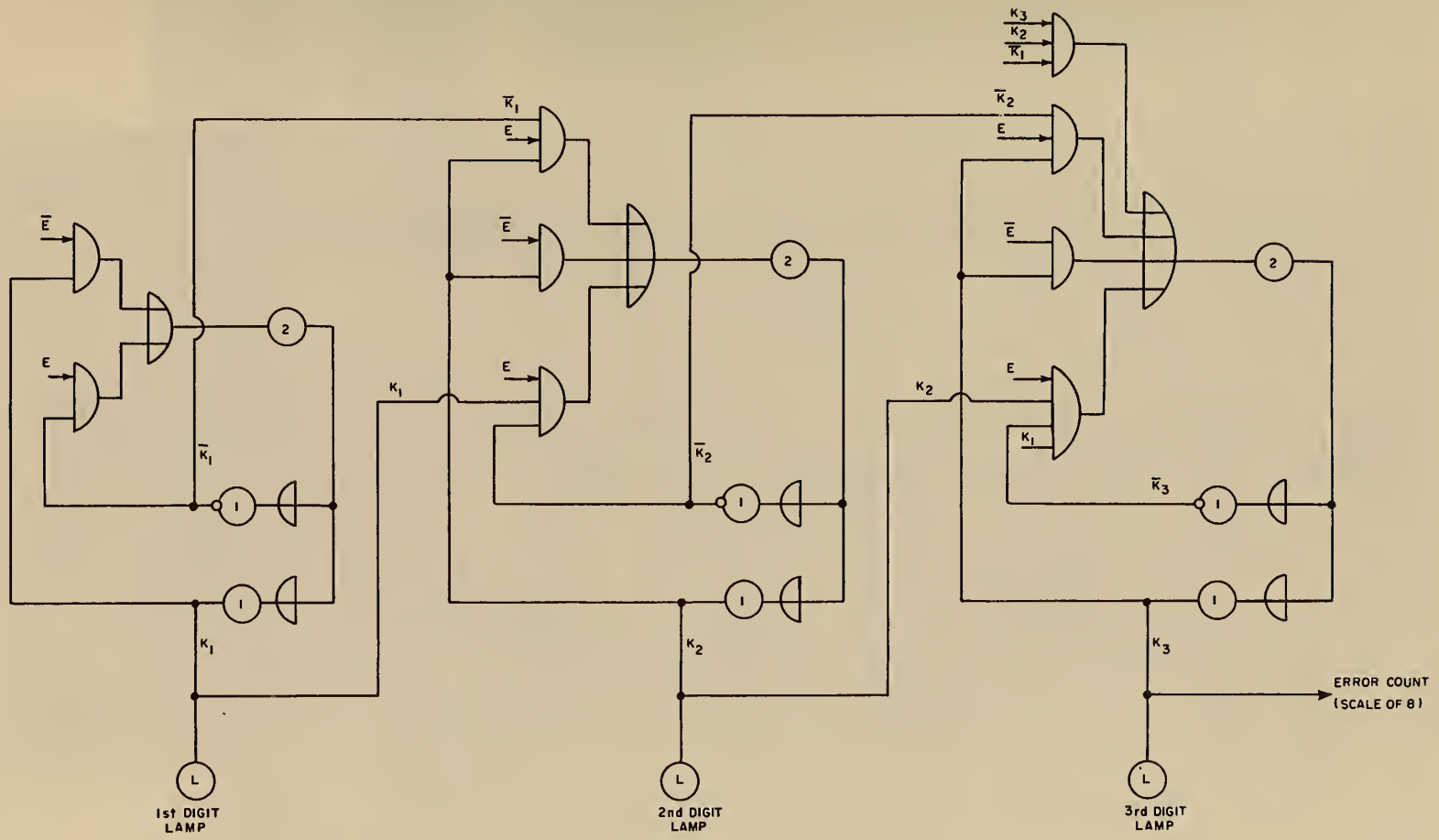


FIGURE 91. THE ERROR COUNTER

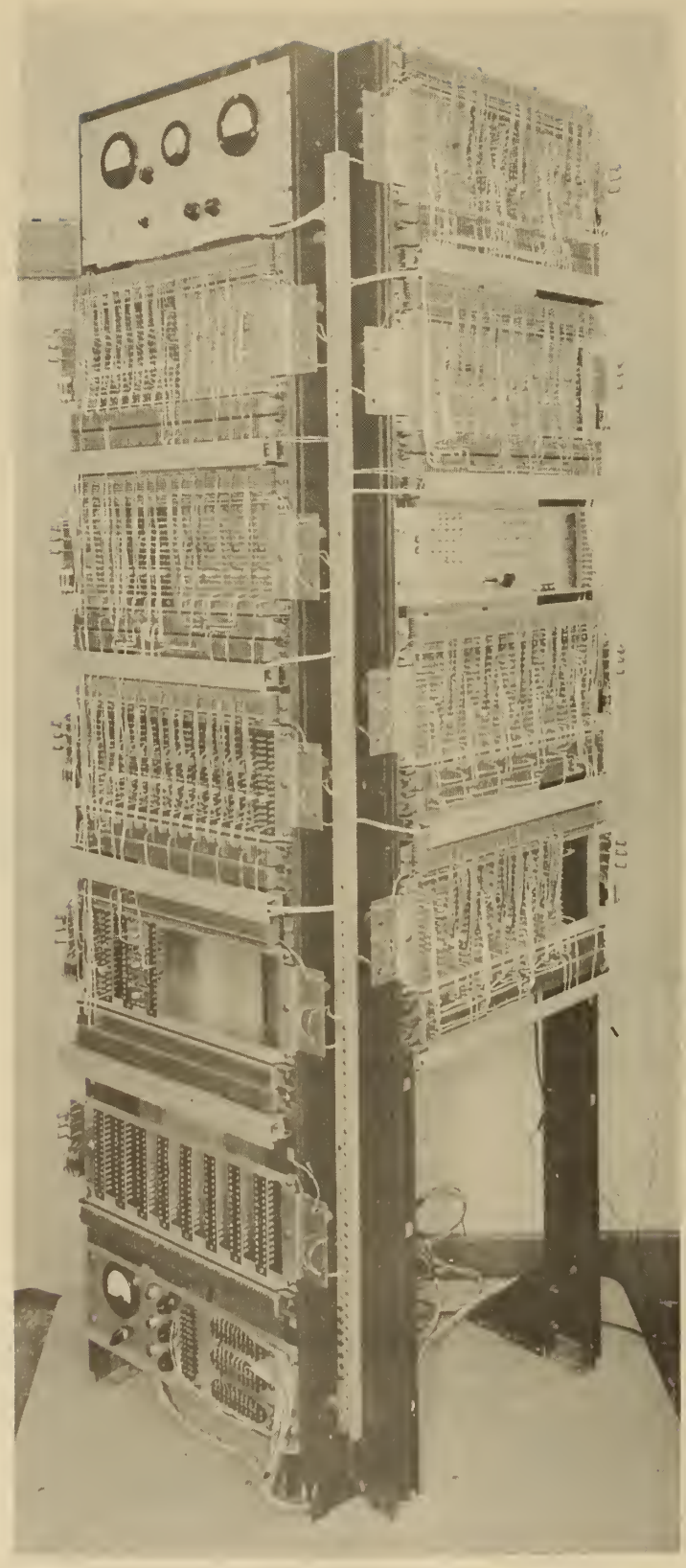


Figure 92. Front View of the Test Computer

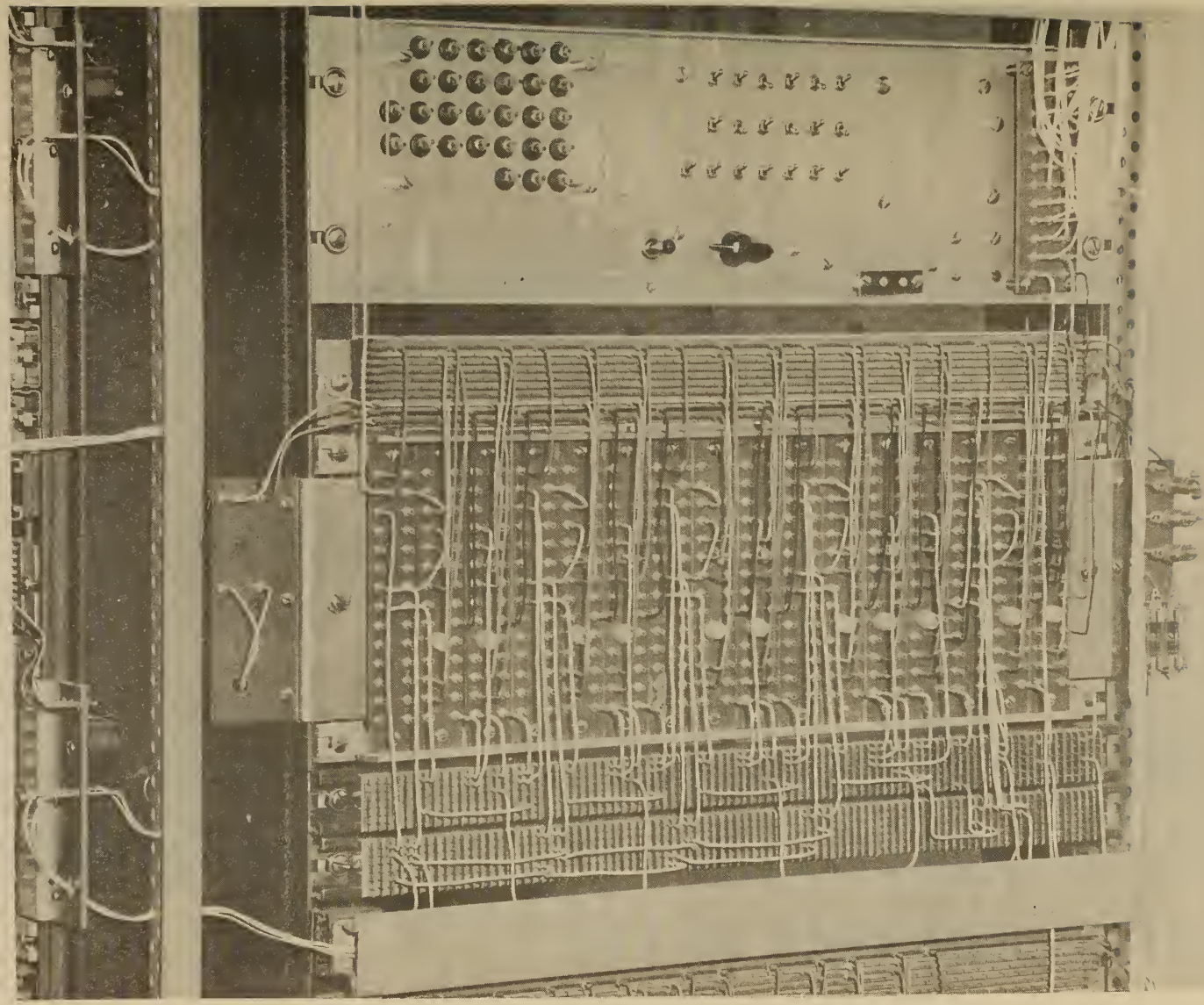


Figure 93. Close View of the Test Computer Showing the Control Panel and the Modularized Bread-Board Construction

Two ferrite clock transformers appear on the left. Figure 94 is a rear view showing the 24-watt clock generator at the top.

Valuable assistance in testing the circuits, and in assembling the computer, was contributed by G. Reimherr, L. Liebschutz and O. Hall.

SUMMARY

Because it lacks the inherent instability of majority logic, and because it is economical of components, diode switching is an attractive way to implement computer logical functions. The drawbacks of diode switching are that it does not provide the essential NOT function; it lacks power amplification, which is necessary for signal propagation and for logical branching; and it provides no signal regeneration. To make up for these deficiencies it is necessary to insert amplifiers at intervals within the switching network.

This note describes a solid-state amplifier and a solid-state ONES-complementer amplifier designed to receive, either individually or together, the signal from an AND-OR sequence of diode logic. Each amplifier consists of three principal parts: an emitter-follower input stage; a square loop-core magnetic amplifier output-stage; and finally an output degenerate AND-gate. Power amplification is entirely in the form of current amplification with the core providing most of the gain. The emitter-follower is particularly well suited as an input stage because is provides gain at low current levels. This lowers the current requirements in the extensive diode gating structure, with a considerable saving in power. The core, on the other hand, requires more input current than the emitter-follower and is capable of handling very large output currents. It is therefore most suitable as an output stage. The emitter-follower and the core complement each other also in another very important way. Because of the manner of operation of a magnetic amplifier, the signal-carrying parameter, which must be amplified and propagated, is measured in volt-seconds ($\int$ vdt). This quantity tends to be dissipated in passage through successive magnetic amplifiers. The emitter-follower, however, is made to replenish the signal by pulse-stretching through base-charge storage produced by driving the base-emitter junction into forward conduction momentarily at the peak of the signal.

The operating cycle of the core, and therefore of the entire amplifier, consists of two parts: a receive operation followed by a transmit-recover operation. At the end of every transmit-recover interval the core is left in the state of negative remanence, called the ZERO state. Then, during its receive-interval, the occurrence of a ONE at the emitter-follower input carries the core to a state of positive remanence near saturation, called the ONE state; or, the occurrence of a ZERO, which is the absence of a ONE, leaves the core in the ZERO state. During the transmit-recover interval current from the driven AND-gates (the logic-load), plus the current from the degenerate AND-gate through which the driven gates are connected to the core, passes through the

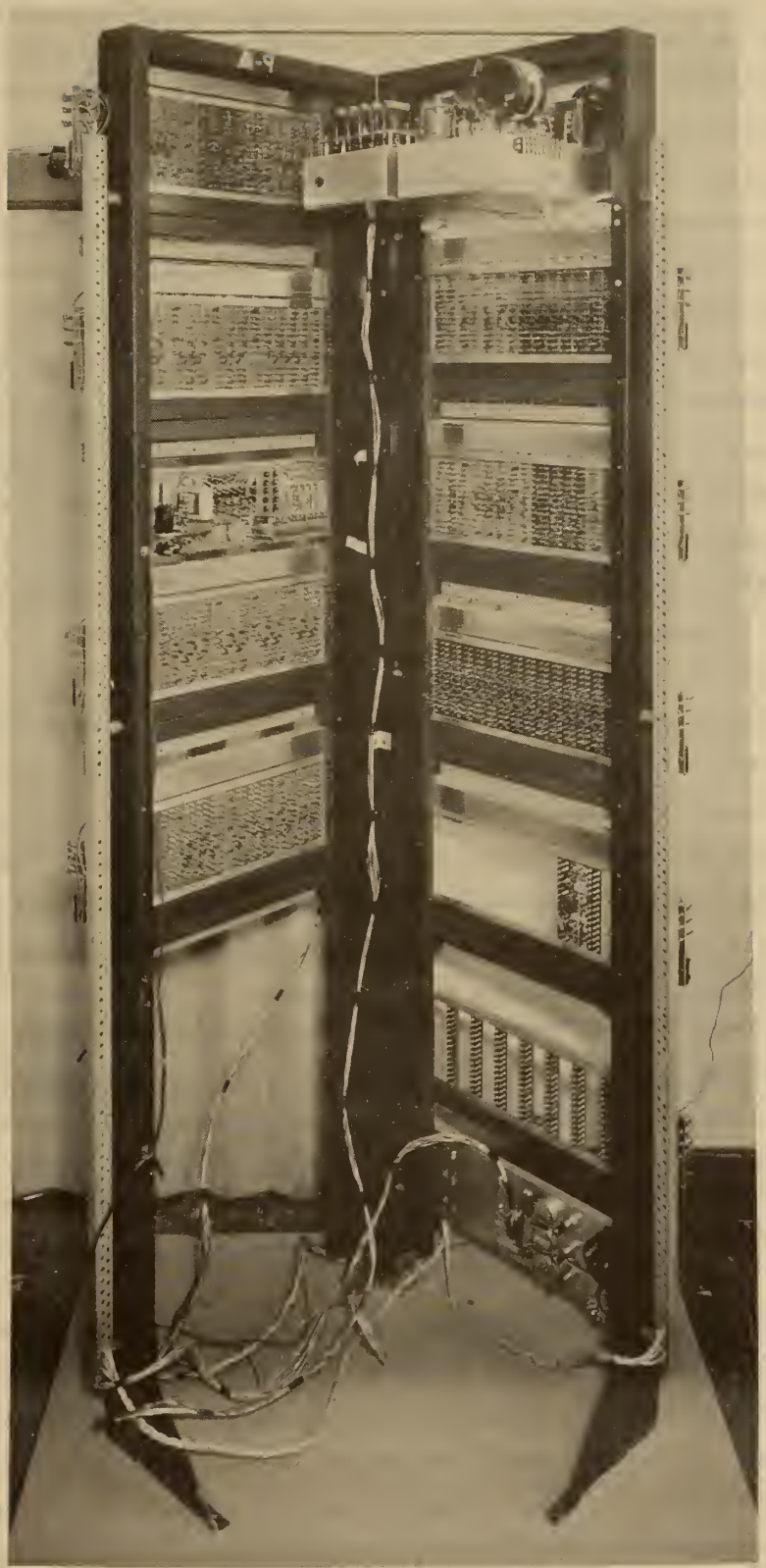


Figure 94. Rear View of the Test Computer Showing the Clock Generator at Top

output winding in such a sense as to restore the core to negative remanence. The time integral of the c.e.m.f. across the output winding during this time constitutes the output signal of the amplifier, and is large or small depending upon whether the core was in the ONE or the ZERO state at the outset of the transmit-recover integral. Signal timing and shaping, and some of the power used to cycle the core are supplied by a sine-wave voltage-source clock connected to the amplifiers. A two-phase clock is required because the receive and transmit intervals are sequential, so that for every amplifier which is in the transmitting phase, there is one which is simultaneously in the receiving phase. It also follows that there must be two amplifiers for each bit of information transmitted.

The output degenerate AND-gate supplies current to restore the core in case none is available from the logic gates at any time; and it also supplies current to charge the fan-out lead capacitance. The pull-up resistor in this gate may be adjusted to a few alternate values depending upon the rough magnitude of capacitance to be driven by the particular amplifier. The use of the degenerate AND-gate for this purpose allows all the logic gates to have identical pull-up currents of minimum value. The use of a square-loop core as a saturable reactor to "hold down" logical gates is particularly attractive in that continuous standby power is not necessary, as it is when they are held down by a clamped OR-gate in the conventional manner.

In the complementing amplifier the clock is connected to one terminal of the input winding of the core so as to set the core in the ONE state during each receive-internal. The other terminal of the input winding is connected through a resistor to the emitter. A diode clamp holds the emitter at ground when ZEROS are present at the emitter-follower input. The core then, being continually set by the clock, transmits ONES. But upon the arrival of a ONE at its input the emitter-follower generates sufficient current to open the diode clamp and the resulting emitter signal opposes the clock, leaving the core in the ZERO state. The core then transmits a ZERO.

The gating structure requires one d-c supply of -25 volts, 5 ma per AND-gate. The amplifiers require d-c supplies of -9 volts and +12 volts, supplying a power of approximately 0.5 watt. The clock frequency is 300 kc. Its amplitude is 7 volts (rms), and it supplies about 50 mw of power to each amplifier. A logical fan-in of 20 and fan-out of 30 is achieved.

The volt-second transfer characteristic of the amplifier critically determines the stability of propagation of binary signals. Factors governing the required shape of this characteristic are discussed.

A test computer using 81 magnetic cores was built to demonstrate the operation of the circuit. It alternately adds 2 six-bit binary numbers and compares the sum with an inserted seven-bit check word. The operations are serial. Errors revealed in the compare operation are counted by a three-stage binary counter, which is also part of the computer. A seven-place shift register using dynamic flip-flops, also constructed from the same circuitry, serves as the machine's internal storage. The machine may be run self synchronously, or may be externally triggered through a synchronizer.

APPENDIX I

Derivation of

$$m = \frac{i_o R_s}{v_o} = \frac{1 - v_{co}/v_o}{1 + v_{co}/i_o R_c}$$

Starting with

$$\frac{R_c}{R_s + R_c}\left(1 - \frac{i_o R_s}{v_o}\right) = \frac{v_{co}}{v_o},$$

$$1 - \frac{i_o R_s}{v_o} = \frac{v_{co}}{v_o}\left(1 + \frac{R_s}{R_c}\right)$$

$$\frac{i_o R_s}{v_o} - 1 = -\frac{v_{co} R_s}{v_o R_c} - \frac{v_{co}}{v_o}$$

$$\frac{i_o R_s}{v_o} + \frac{v_{co} R_s}{v_o R_c} = 1 - \frac{v_{co}}{v_o}$$

$$\frac{i_o R_s}{v_o} + \frac{v_{co} R_s i_o}{v_o R_c i_o} = 1 - \frac{v_{co}}{v_o}, \text{ whence}$$

$$\frac{i_o R_s}{v_o}\left(1 + \frac{v_{co}}{i_o R_c}\right) = 1 - \frac{v_{co}}{v_o}$$

$$m = \frac{i_o R_s}{v_o} = \frac{1 - v_{co}/v_o}{1 + v_{co}/i_o R_c}$$

APPENDIX II

Derivation of $m = (1 + v_{co}/i_o R_p)^{-1}$,

where

$$R_p^{-1} = R_s^{-1} + R_c^{-1}.$$

Starting with

$$m = \frac{1 - v_{co}/v_o}{1 + v_{co}/i_o R_c},$$

make the substitution

$$\frac{v_{co}}{v_o} = \frac{R_c}{R_s + R_c}\left(1 - \frac{i_o R_s}{v_o}\right) = \frac{R_c}{R_s + R_c}(1 - m)$$

then

$$m \doteq \frac{1 - \frac{R_c}{R_s + R_c}(1 - m)}{1 + v_{co}/i_o R_c}$$

$$m\left(1 + v_{co}/i_o R_c\right) = 1 - \frac{R_c}{R_s + R_c} + m\frac{R_c}{R_s + R_c}$$

$$m\left(1 + \frac{v_{co}}{i_o R_c} - \frac{R_c}{R_s + R_c}\right) = 1 - \frac{R_c}{R_s + R_c}$$

$$m\left[\frac{v_{co}}{i_o R_c} + \left(1 - \frac{R_c}{R_s + R_c}\right)\right] = 1 - \frac{R_c}{R_s + R_c}$$

$$m\left(\frac{v_{co}}{i_o R_c} + \frac{R_s}{R_s + R_c}\right) = \frac{R_s}{R_s + R_c}$$

$$m = \frac{R_s}{R_s + R_c}\left(\frac{R_s}{R_s + R_c} + \frac{v_{co}}{i_o R_c}\right)^{-1}$$

$$= \left(1 + \frac{v_{co}}{i_o} \cdot \frac{R_s + R_c}{R_s R_c}\right)^{-1}$$

$$= \left(1 + v_{co}/i_o R_p\right)^{-1}$$

APPENDIX III

Derivation of the exact and approximate formulas for

$$x_c\,(T/2) = \int_o^{T/2} v_c\,dt = \int_{t_o}^{(T/2 - t_o)} v_c\,dt \qquad \text{(III-1)}$$

$x_c\,(T/2)$ is the maximum voltage-time integral impressed upon the input winding during the receive half-cycle. It is represented by the shaded area in Figure III-1.

From equation (29), which gives $y\,(t) = \int_{t_o}^{t} \frac{n_2}{n_1} v_c\,dt$,

we have, setting $t = t_1 \left[= T/2 - t_o\right]$

$$x_c\,(T/2) = \frac{n_1}{n_2}\, y\,(T/2)$$

$$= \frac{R_c}{R_s + R_c} \left[\left(\cos 2\pi \frac{t_o}{T} + 2\pi \frac{i_o R_s}{v_o} \frac{t_o}{T}\right) - \left(\cos 2\pi \frac{t_1}{T} + 2\pi \frac{i_o R_s}{v_o} \frac{t_1}{T}\right) \right] \frac{v_o T}{2\pi}$$

and, since $\cos 2\pi\, t_1/T = -\cos 2\pi\, t_o/T$,

$$x_c\,(T/2) = \frac{R_s}{R_s + R_c} \left[2\cos \frac{t_o}{T} - 2\pi \frac{i_o R_s}{v_o} \left(\frac{t_1 - t_o}{T}\right) \right] \frac{v_o T}{2\pi}$$

$$= \frac{R_s}{R_s + R_c} \left[\cos 2\pi \frac{t_o}{T} - \frac{\pi(t_1 - t_o)}{T} \cdot \frac{i_o R_s}{v_o} \right] \frac{v_o T}{\pi}$$

Then using $t_1 - t_o = T/2 - 2\,t_o$,

$$x_c\,(T/2) = \frac{R_s}{R_s + R_c} \left[\cos 2\pi \frac{t_o}{T} - \frac{\pi}{2}\left(1 - \frac{4t_o}{T}\right) \frac{i_o R_s}{v_o} \right] \frac{v_o T}{\pi} \qquad \text{(III-2)}$$

$$= \frac{v'_{co}\, T}{\pi}, \text{ which defines an effective core input peak voltage}$$

$$v'_{co} = \frac{R_c}{R_s + R_c} \left[\cos 2\pi \frac{t_o}{T} - \frac{\pi}{2}\left(1 - \frac{4t_o}{T}\right) \frac{i_o R_s}{v_o} \right] v_o \qquad \text{(III-3)}$$

We compare v'_{co} with v_{co}, the latter being given by

$$v_{co} = \frac{R_s}{R_s + R_c} \left(1 - \frac{i_o R_s}{v_o}\right) v_o, \qquad \text{(III-4)}$$

and observe that as t_o/T and hence $i_o R_s/v_o = m$ approach zero

$$v'_{co} \longrightarrow v_{co} \longrightarrow \frac{R_c}{R_s + R_c} v_o \qquad \text{(III-5)}$$

If we let $t_o/T = 1/12$, then $i_o R_s/v_o = \sin 2\pi t_o/T = \sin 30^o = 0.5 = m$, a very large value. For this value of m

$$v'_{co} = \frac{R_s}{R_s + R_c}\left[\cos\frac{2\pi}{12} - \frac{\pi}{2}\left(1 - \frac{4}{12}\right)\frac{i_o R_s}{v_o}\right] v_o = \frac{R_c}{R_s + R_c}\left[0.866 - 1.05\frac{i_o R_s}{v_o}\right] v_o \qquad \text{(III-6)}$$

Comparison of (III-6) with (III-4) shows that, for values of $m \leq 0.5$, $v'_{co} \simeq v_{co}$, and

$$x_c\,(T/2) = \frac{v'_{co}\,T}{\pi} \simeq \frac{v_{co}\,T}{\pi}$$

Specifically, for m = 0.5

$$v'_{co} = \frac{0.866 - 1.05\,(5)}{1 - 0.5} = 0.73\,v_{co}$$

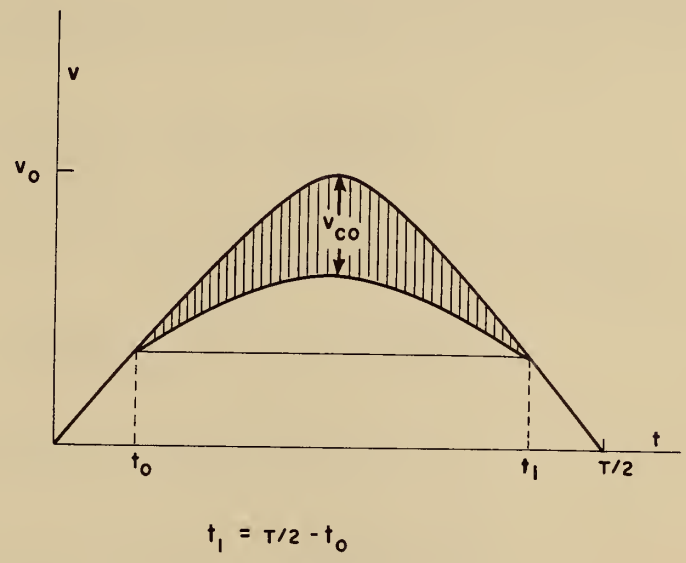


Figure III-1. Maximum voltage-time integral received by the core

APPENDIX IV

The curves in Figure 39 were not plotted, but were sketched, assuming $dy/dx = 1$ at $t = T/4$, and using the values for $y\,(T/2)$ calculated for different values of m, using the formula

$$y(T/2) = \left[\sqrt{\frac{1+m}{1-m}} - \left(\frac{\pi}{2} - \sin^{-1} m\right)\frac{m}{1-m}\right]\frac{v_o T}{\pi} \qquad \text{(IV-1)}$$

obtained by setting $t = T/2$, $m = i_o R_s / v_o$, and

$$\frac{n_2}{n_1}\,\frac{R_c}{R_s + R_c} = \frac{1}{1 - m} \quad \text{in (29).}$$

The following table gives $y(T/2)$ for three values of m.

m	y (T/2)	
0.36	0.78	$v_o T/\pi$
0.50	0.73	"
0.80	0.50	"

APPENDIX V

The synchronizer used in the Transmag test computer is diagrammed in Figure 88. It is the kind described and shown in Figure 1 of the paper "Buffering Between Input-Output and the Computer" by A. L. Leiner. [5] The storage and regeneration device is a ring of two element-groups. The probability p that this ring will emit an imperfect signal to the computer is practically equal to g^{-m} if the transfer-functions of its element-groups are always nearly alike, and if high frequency noise is excluded from it.

APPENDIX VI

INPUT IMPEDANCE OF THE EMITTER-FOLLOWER

Here is a derivation of the input impedance and input equivalent circuit of the emitter follower based on the assumption that the time response of the transistor is that of a single-section low-pass RC filter.

From Shea, equation (10.67),[6] the input impedance for the common-collector connection is

$$Z_i = r_b + (1 + \beta) R_L$$

or

$$Z_i - r_b = (1 + \beta) R_L$$

where β is a complex function of frequency and R_L is the emitter-follower load resistance. See Figure VI-1.

In terms of α, also a complex function of frequency,

$$Z_i - r_b = \left(\frac{1}{1 - \alpha}\right) R_L$$

we now assume

$$\alpha = \frac{\alpha_o}{1 + j\omega\tau}$$

where α_o is the real low-frequency common-base current gain of the transistor; and where $\tau = 1/\omega_{ab}$ equals the response time constant of the transistor. The above single-pole expression for α defines its frequency response to be that of a single section low-pass RC-filter. Then

$$Z_i - r_b = R_L \frac{1}{1 - \frac{\alpha_o}{\omega + j\omega\tau}} = R_L \frac{1 + j\omega\tau}{(1 - \alpha_o) + j\omega\tau}$$

and, since $(1 - \alpha_o) = (1 + \beta_o)^{-1}$, where β_o is the real low frequency common emitter current gain,

$$Z_i - r_b = R_L \frac{1 + j\omega\tau}{(1 + \beta_o)^{-1} + j\omega\tau} = R_L (1 + \beta_o) \frac{1 + j\omega\tau}{1 + j\omega\tau(1 + \beta_o)}$$

Consider now the impedance Z of the network in Figure VI-2.

$$(Z - r_b)^{-1} = R^{-1} + \left[r + 1/j\omega C_i\right]^{-1} = \frac{1 + j\omega r C_i + j\omega R C_i}{R(1 + j\omega r C_i)}$$

or

$$Z - r_b = R \frac{1 + j\omega r C_i}{1 + j\omega(R + r)C_i}$$

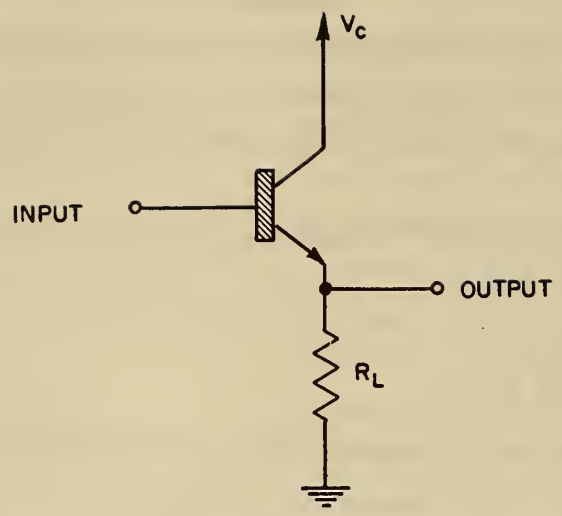


Figure VI-1. Emitter-follower

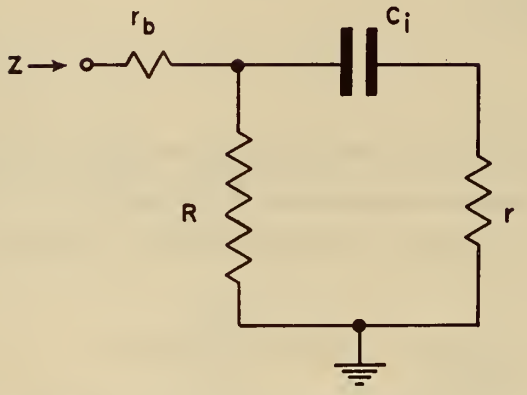


Figure VI-2. Diagram used in deriving the emitter-follower input equivalent circuit

A formal substitution of

$$r = R_L$$

$$C_i = \tau/r = \tau/R_L, \text{ and}$$

$$R = R_L (1 + \beta_o)$$

gives

$$Z - r_b = R_L (1 + \beta_o) \frac{1 + j\omega\tau}{1 + j\omega\tau (1 + 1 + \beta_o)}$$

which is very nearly the same as the expression for $Z_i - r_b$. In any practical case $1 + \beta_o$ is enough greater than unity that

$$1 + 1 + \beta_o \simeq 1 + \beta_o,$$

and the circuit in Figure VI-3 is the practical equivalent circuit for the input impedance of the emitter-follower.

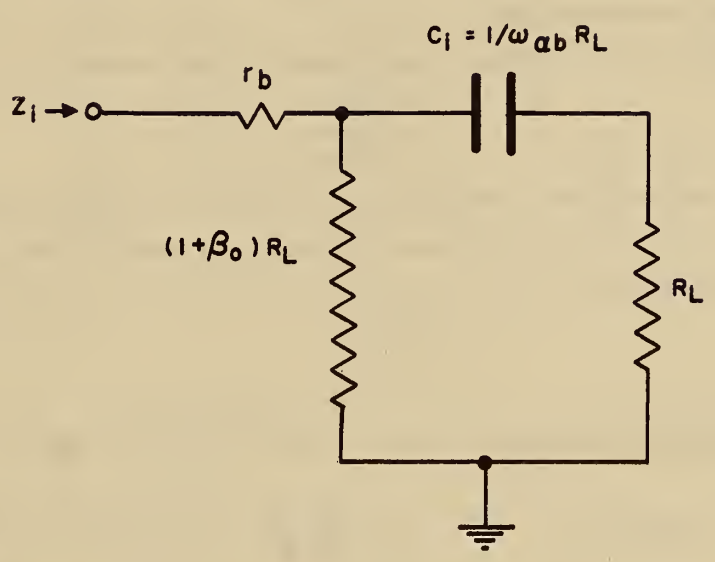


Figure VI-3. Emitter-follower input equivalent circuit

APPENDIX VII

EMITTER-FOLLOWER OUTPUT IMPEDANCE AND OUTPUT EQUIVALENT CIRCUIT

This derivation is based on the assumption that the time-response of the transistor is that of a single-section, low-pass RC-filter.

Omitting the emitter resistance from equation (10.69) of Shea,[6]

$$Z_o = \frac{r_b + Z_g}{1 + \beta} = (1 - \alpha)(r_b + Z_g)$$

where Z_o is the output internal impedance of the emitter-follower, Z_g is the internal impedance of the signal generator that drives the base, r_b is the base resistance, and α and β have their usual meaning. We let

$$\alpha = \frac{\alpha_o}{1 + j\omega\tau}$$

where α_o is the real, low-frequency value of α, and $\tau = 1/\omega_{\alpha b}$. Then

$$1 - \alpha = 1 - \frac{\alpha_o}{1 + j\omega\tau} = \frac{(1 - \alpha_o) + j\omega\tau}{1 + j\omega\tau} = (1 + \beta_o)^{-1} \frac{1}{1 + j\omega\tau} + \frac{j\omega\tau}{1 + j\omega\tau};$$

and, setting Z_g equal to r_D, the forward resistance of D_{pi},

$$Z_o = \frac{r_b + r_D}{1 + \beta_o} \frac{1}{1 + j\omega\tau} + (r_b + r_D) \frac{j\omega\tau}{1 + j\omega\tau}$$

Consider now the impedance Z of the network in Figure VII-1.

$$Z = r_1 \frac{1}{1 + j\omega r_1 C_o} + r_2 \frac{j\omega L_o / r_2}{1 + j\omega L_o / r_2}$$

A formal substitution:

$$r_1 = \frac{r_b + r_D}{1 + \beta_o}$$

$$C_o = \frac{\tau}{r_1} = \frac{\tau(1 + \beta_o)}{(r_b + r_D)}$$

$$r_2 = r_b + r_D, \text{ and}$$

$$L_o = \tau r_2 = \tau (r_b + r_D)$$

makes $Z = Z_o$, and Figure VII-1 becomes the equivalent circuit for the output internal impedance of the emitter follower.

Figure VII-2 shows the impedances of the branches of the network.

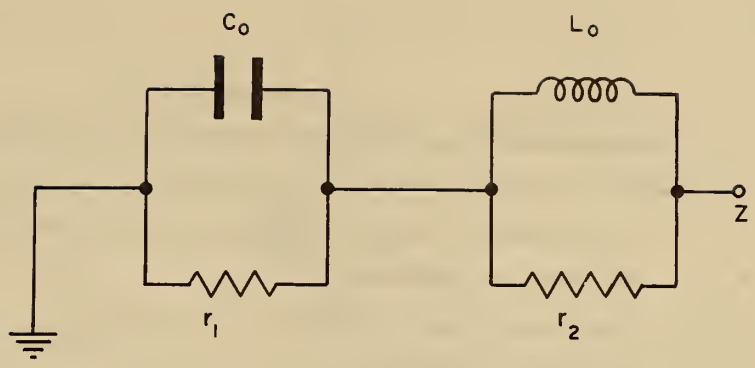


Figure VII-1. Diagram used in deriving the emitter-follower output equivalent circuit

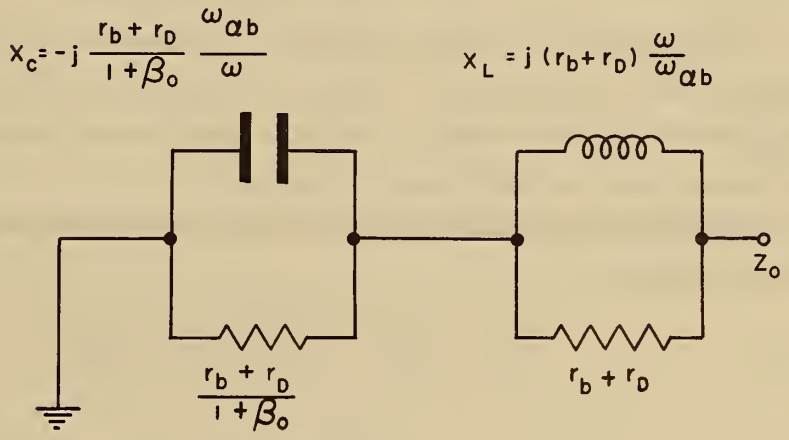


Figure VII-2. Emitter-follower output equivalent circuit

In the frequency range

$$(1 + \beta)^{-1} << \omega/\omega_{ab} \leq 1/4$$

Z_o is principally inductive, and simplies to

$$Z_o \simeq j (r_b + r_D) \omega/\omega_{ab}$$

APPENDIX VIII

THE DEPENDENCE OF COLLECTOR DISSIPATION UPON CORE RESISTANCE

The collector dissipation h needs to be considered for each of six cases:

h_{a1} For the assertive amplifier of Figure 53 for all ONEs received.

h_{a0} The same, for all ZEROs.

h_{b1} For the NOT-amplifier of Figure 65 for all ONEs.

h_{b0} The same, for all ZEROs.

h_{c1} For the assert-negate amplifier of Figure 67.

h_{c0} The same, for all ZEROs.

The Assertive Amplifier

In actual practice the collector dissipation is lower than for the worst-case version of Figure 53, shown in Figure VIII-1. But we first calculate h'_{a1} and h'_{a0} for this version. In Figure VIII-1, the emitter supply is made large enough to allow the emitter-follower to reproduce the full clock sine wave without negative clipping.

When ONEs are being transmitted, the average collector dissipation for this version of the assertive amplifier is

$$h'_{a1} = \frac{1}{2\pi} \int_0^{2\pi} (V_c - v)\, i_{cb}\, d(\omega t)$$

$$= \frac{1}{2\pi} \int_0^{2\pi} (v_o - v_o \sin \omega t)\, i_{cb}\, d(\omega t) \qquad \text{(VIII-1)}$$

Now

$$i_{cb} = i_1 + i_2, \qquad \text{(VIII-2)}$$

where

$$i_2 = \frac{v_o \sin \omega t}{3R_c/2} \qquad \text{(VIII-3)}$$

and

$$i_1 = \frac{v - V_e}{3\, R_c/2}$$

$$= \frac{v_o \sin \omega t + 2\, v_o}{3\, R_c/2}\,; \qquad \text{(VIII-4)}$$

so that

$$i_{cb} = \frac{2\, v_o + 2\, v_o \sin \omega t}{3\, R_c/2}$$

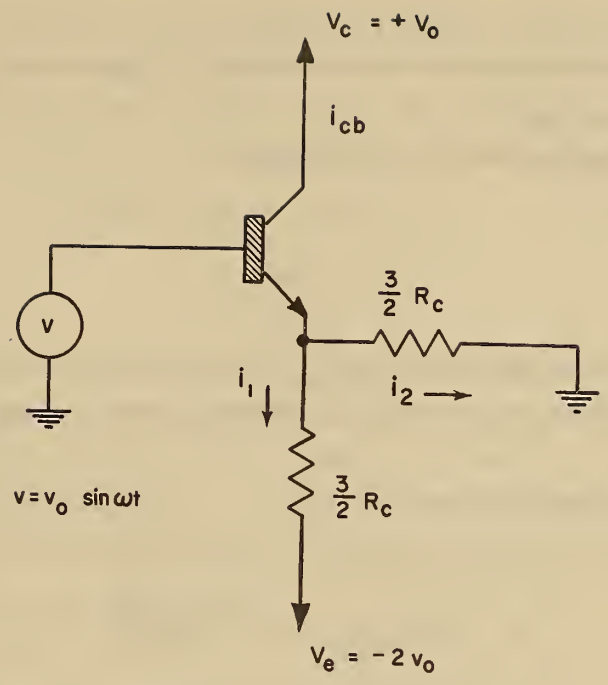


Figure VIII-1. Diagram used in calculating worst-case collector dissipation

Then

$$h'_{a1} = \frac{1}{2\pi} \int_o^{2\pi} \frac{(v_o - v_o \sin \omega t)(2 v_o + 2 v_o \sin \omega t)}{3 R_c/2} \, d(\omega t)$$

$$= \frac{2v_o^2}{3\pi R_c} \int_o^{2\pi} \cos^2 \omega t \, d(\omega t) = \frac{2 v_o^2}{3 R_c} \qquad \text{(VIII-6)}$$

In the case of all ZEROs,

$$h'_{ao} = \frac{1}{2} \left[\frac{1}{\pi} \int_o^{\pi} v_o \left(\frac{v_o}{3R_c / 2} \right) d(\omega t) + \frac{2 v_o^2}{3 R_c} \right]$$

$$= \frac{1}{2} \left[\frac{4 v_o^2}{3 R_c} + \frac{2 v_o^2}{3 R_c} \right] = \frac{v_o^2}{R_c} \qquad \text{(VIII-7)}$$

The NOT-Amplifier

No power is dissipated in the collector of the NOT-amplifier during the negative half cycle of the clock because no collector current flows. This is also (almost) true during the positive half cycle for all ZEROs received, so we may assume

$$h_{bo} \simeq 0 \qquad \text{(VIII-8)}$$

But during the reception of ONEs, the clamping diode D_c, in Figure 65, is open, and the collector current i_{cb} equals the sum of the constant current I_e, which formerly had been present in R_e, plus a varying component equal to $v_o \sin \omega t/R_e$. No current flows in the core branch during this time because of the opposing clock e.m.f. Therefore

$$i_{cb} = v_o \sin \omega t/R_e + I_e \qquad \text{(VIII-9)}$$

in which

$$I_e = \hat{i}_c + I_{co} \qquad \text{(VIII-10)}$$

where $\hat{i}_c$ is the core peak current, and I_{co} is the value of the current through D_c for which its forward resistance equals the largest permissible clamping resistance r_{co}. (r_{co} should be 50 ohms or less.)

For the NOT-amplifier then

$$\begin{aligned} h_{b1} &= \frac{1}{2\pi} \int_o^\pi (V_c - v)\, i_{cb}\, d(\omega t) \\ &= \frac{1}{2\pi} \int_o^\pi (v_o - v_o \sin \omega t)(I_e + v_o \sin \omega t/R_e)\, d(\omega t) \\ &= \frac{1}{2\pi} \int_o^\pi \left[v_o I_e - v_o I_e \sin \omega t + v_o^2 \sin \omega t/R_e - v_o^2 \sin \omega t/R_e \right] d(\omega t) \\ &= v_o I_e (1/2 - 1/\pi) + \frac{v_o^2}{R_e} (1/\pi - 1/4). \end{aligned} \qquad \text{(VIII-11)}$$

The Assert-Negate Amplifier

As far as the transistor is concerned, the only difference between the circuit of Figure 67 and that of Figure 65 is the additional collector current $i_c \sin \omega t$ drawn, during the positive half-cycle, by the assertive core. The extra collector dissipation due to this current is given by

$$\begin{aligned} & 1/2\pi \int_o^\pi (V_c - v)(\hat{i}_c \sin \omega t)\, d(\omega t) \\ &= 1/2\pi \int_o^\pi v_o (1 - \sin \omega t)(2v_o \sin \omega t/R_c)\, d(\omega t) \\ &= \frac{v_o^2}{3\pi R_c} \int_o^\pi (\sin \omega t - \sin^2 \omega t)\, d(\omega t) \\ &= \frac{v_o^2}{3R_c} (2/\pi - 1/2) \end{aligned} \qquad \text{(VIII-12)}$$

Therefore

$$h_{c1} = h_{b1} + \frac{v_o^2}{3R_c}(2/\pi - 1/2)$$

$$= v_o I_e (1/2 - 1/\pi) + \frac{v_o^2}{R_e}(1/\pi - 1/4) + \frac{v_o^2}{3R_c}(2/\pi - 1/2). \quad \text{(VIII-13)}$$

Finally

$$h_{co} = h_{bo} \simeq 0. \quad \text{(VIII-14}$$

We now wish to evaluate the collector dissipation for each of the six cases using $R_c = 1000$ ohms obtained from Figure 76 at $f_c = 300$ kc. With $v_o = 10$ volts, $\hat{i}_c = 2\, v_o/3\, R_c = 7$ ma. Then, letting $I_{co} = 5_{ma}$, $I_e = 12$ ma; and using $V_e = -12$ volts makes $R_e = R_c = 1000$ ohms.

We wish to compare the collector dissipation figures obtained with $v_o^2/3\, R_c = 33$ milliwatts, which is the power required to drive R_s and the core.

$$h'_{a1} = 2(v_o^2/3\, R_c) = 67 \text{ milliwatts}$$

$$h'_{ao} = 3(v_o^2/3\, R_c) = 100 \text{ milliwatts}$$

$$h_{b1} = 10(.012)(.5-.32) + (100/1000)(.32-.25)$$

$$= (.12)(.18) + (.1)(.07) = 29 \text{ milliwatts}$$

$$h_{bo} \simeq 0$$

$$h_{c1} = 0.029 + .033\,(.14) \text{ watts}$$

$$= 29 + 4.6 = 34 \text{ milliwatts}$$

$$h_{co} \simeq 0$$

It is apparent that the version of the assertive amplifier of Figure VIII-1, for which h'_{a1} and h'_{ao} were calculated, produces excessive collector dissipation when compared with the remaining two circuits. These circuits owe their low dissipation to the transfer of current from the transistor to the clamping diode D_c during the negative half clock cycle. The use of a clamping diode would also greatly lower the collector dissipation in the assertive amplifier. But there is no need for the negative half clock wave to be reproduced because the core is ZEROed by its output AND-gate. V

can therefore be reduced in magnitude from 2 v_o to v_o or even less with a consequent large reduction in collector dissipation without the use of D_c. A conservative estimate of collector dissipation when this is done is

$$h_{a1} \simeq 33 \text{ milliwatts} = v_o^2/3\,R_c$$

$$h_{ao} \simeq 67 \text{ milliwatts} = 2\,(v_o^2/3\,R_c)$$

The assert-negate amplifier looks most attractive from the point of view of collector dissipation for it provides both assertion and negation, in an economical circuit, with a collector dissipation of only 16% more than for negation alone.

APPENDIX IX

NEGATING TRANSFER-FUNCTION

To obtain $y = \overline{f}_{21}(x)$ we first observe that $y_n = \overline{f}_1(x) = s_{21} - f_1(x)$.

Then $\overline{f}_{21}(x) = \overline{f}_1\left[f_2(x)\right]$

$= s_{21} - f_1\left[f_2(x)\right]$;

which is simply the reflection of $f_{21}(x)$ in the line $y = s_{21}/2$.. Compare $y = \overline{f}_{21}(x)$ in Figure 71 with $y = f_{21}(x)$ in Figure 62.

To obtain $y = \overline{f}_{12}(x)$ we can write

$\overline{f}_{12}(x) = f_2\left[\overline{f}_1(x)\right]$

$= f_2\left[s_{21} - f_1(x)\right]$;

and because, in this case, $f_1(x)$ is symmetrical about the point $x = s_{12}/2$, $y = s_{21}/2$, $s_{21} - f_1(x) = f_1(s_{12} - x)$. See Figure IX-1.

Therefore

$\overline{f}_{12}(x) = f_2\left[s_{21} - f_1(x)\right] = f_2\left[f_1(s_{12} - x)\right]$, which is the reflection of $f_{12}(x)$ in the line $x = s_{12}/2$. Compare $y = \overline{f}_{12}(x)$ in Figure 71 with $y = f_{12}(x)$ in Figure 62.

If the nonlinearity of a transfer-function is such as to provide stable propagation of ONEs and ZEROs, that transfer-function is said to be <u>properly nonlinear,</u> or p.n.l. In general it can be said that if an element-group transfer-function is p.n.l. then its reflection in the line $x = s/2$ or in the line $y = s/2$ is also p.n.l. Therefore, if $y = f_{21}(x) = f_1\left[f_2(x)\right]$ is p.n.l., then $y = \overline{f}_{21}(x) = s_{21} - f_1\left[f_2(x)\right]$ is p.n.l.

And if

$y = f_{12}(x) = f_2\left[f_1(x)\right]$ is p.n.l., then

$y = \overline{f}_{12}(x) = f_2\left[f_1(s_{12} - x)\right]$ is p.n.l. $|g| > 1$ for any p.n.l. transfer-function.

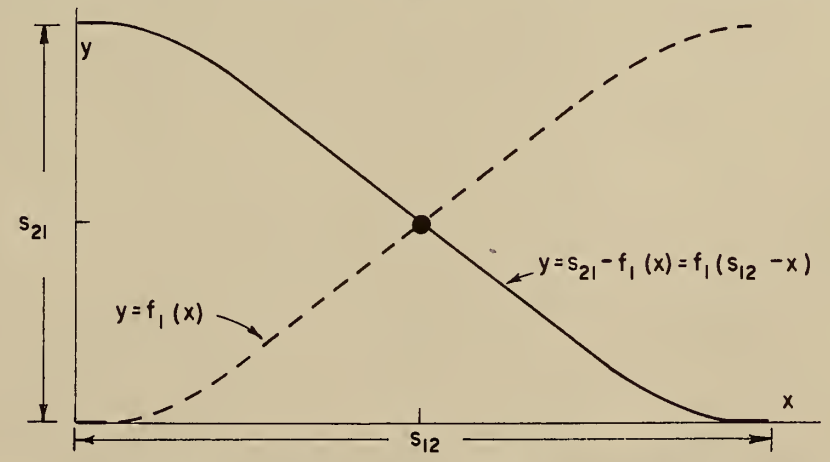


Figure IX-1. Diagram showing that $s_{21} - f_1(x) = f_1(s_{12} - x)$ when $f_1(x)$ is symmetrical about the point $x = 1/2\ s_{12}$, $y = 1/2\ s_{21}$

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