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U.S. DEPARTMENT OF COMMERCE / National Bureau of Standards

A Schottky Diode Bridge Sampling Gate

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Arnold G. Perrey
Howard K. Schoenwetter

Electrosystems Division
Center for Electronics and Electrical Engineering
National Bureau of Standards
Washington, D.C. 20234

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A SCHOTTKY DIODE BRIDGE SAMPLING GATE

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A Schottky diode bridge and associated gating and delay circuits have been designed to facilitate the measurement of low level signals preceded by large signals without overdriving the measuring instrument. This measurement problem occurs in testing or evaluating operational amplifiers, digital-to-analog converters, sample/hold amplifiers and other similar active circuits.

Key Words: Diode bridge sampling gates; diode bridge switches; diode clipping circuits; diode shunt limiters; Schottky diode bridge; time controlled sampling.

1. Introduction

To determine the performance of operational amplifiers, sample/hold amplifiers, digital-to-analog converters and other active circuits, it is often necessary to measure low level voltages in the range of 10 - 1000 μV, preceded by larger signals in the 0.1 - 10 volt range. Amplifiers with high gains must be employed in the instruments (oscilloscope, A/D converter, etc.) used for these measurements. However, the large signals overdrive ("over-load") the amplifier, causing voltage offsets of varying magnitude and duration in the amplifier output. If these offsets have not decayed to negligible levels when the low level signals are measured, erroneous measurements result.

An application which illustrates this measurement problem is the determination of D/A converter (DAC) settling times, using a sensitive direct-coupled oscilloscope. In Fig. 1, V(t) represents the transition between two successive output voltages V_1 and V_2 from the converter. The settling of V(t) to the new level V_2 can be examined in considerable detail if voltage v_p is shifted to approach zero after the transition at time t_1, using a precision resistive divider and a reference supply V_R approximately equal to $-V_2$. However, since $v_p = 1/2\ (V_R + V(t))$, v_p is very large prior to t_1 and is likely to overdrive the oscilloscope's input amplifier.

Diode clipping circuits, various active circuits, and sampling switches may be used to prevent overdrive of a measuring instrument. An example of each type is shown in Fig. 1. If nodes p and a are connected, Schottky diodes D1 and D2 limit v_p to less than approximately ±0.6V (i.e., $|v_p|<0.6$) but have negligible effect on signals smaller than approximately ±20 mV. Since the diodes have picosecond switching speed and approximately 1 pF capacitance per diode at zero voltage, no serious recovery or bandwidth problems are inherent in the circuit. If nodes p and b are connected (instead of p and a), the maximum signal applied to the oscilloscope is still ±0.6V; however, if the open circuit voltage v_p is small, it is amplified by a factor $-2R_1/R$. Thus, a less sensitive range of the oscilloscope may be used and overdrive is less likely. The sampling switch (Circuit C) prevents overdrive of the oscilloscope through proper timing of the gate pulse which closes the switch. Since commercial analog switches are capable of holding off input voltages up to approximately ±10V, the gating voltages generated within the switch package are necessarily large causing voltage spikes of ~0.5V amplitude to feed through to the output circuit. Depending upon the oscilloscope sensitivity and repetition rate, oscilloscope overdrive may result. A second disadvantage of some sampling switches, such as CMOS types, is the turn-on and turn-off delays ranging up to approximately 1 μs. The switch shown in Circuit C can also be used as a shunt switch, connected between node c and ground. Node c is connected directly to the oscilloscope. This mode of operation has most of the disadvantages of a series switch as well as requiring a closed (on) resistance which is very much less than R.

The disadvantage of Circuit A is the small degree of voltage limiting provided. The chief disadvantage of Circuit B and other active voltage limiting circuits is their relatively long recovery or response time: typically 2 to 5 μs. The advantage of these circuits over Circuit C is that they require no gating or timing pulses for their operation.

A fast response circuit was sought to facilitate the measurement of low level signals preceded by very large signals. The approach used and described in the following sections is a combination of circuits A and C. Input signals are limited to ±0.6V using clipping diodes and then applied to a sampling switch operable from gating voltages just large enough to hold off input signals of this magnitude. A gated diode bridge using Schottky diodes was used for the sampling switch for two reasons: (1) The switch has high speed; and (2) The complementary gating voltages needed to gate the bridge are small and cause only small turn-on and turn-off transients in the bridge output.

2. Diode Bridge

The diode bridge and associated circuits are shown in Fig. 2. The general theory of operation of these circuits is presented elsewhere [1,2], so the discussion here will be limited to a brief description of the actual circuits used, and their adjustments.

Clipping diodes D1 and D2 limit the signal applied to the bridge to ±0.6V for input voltages up to ±10V and source resistances greater than 500 ohms. The diode bridge consists of diodes D3, D4, D5 and D6 gated on and off by complementary pulses received through gating diodes D7 and D8. When D7 and D8 are reverse biased, the bridge is biased "on" by a constant current through transistors Q1 and Q2. Constant current sources are used instead of resistors to minimize loading of the input circuit from dc to 50 kHz, the frequency range of immediate interest. When D7 and D8 are forward biased, the constant currents flow through these diodes, and the bridge diodes are reverse biased (cut off). When the bridge is cut off, the signal voltage fed through from node f to g is negligible at low frequencies. Above 50 kHz it is largely determined by the capacitance between these nodes (~1 pF) and the load capacitance between node g and ground. Schottky type diodes D1-D8 are used to ensure maximum switching speeds. The capacitance match for the diodes in the encapsulated matched quad D3-D6 is 0.2 pF.[1] Diodes D7 and D8 have the same degree of matching. The forward voltage drops of the diodes in the matched quad are the same to the extent that the voltage offset at node g ranges up to about 2 mV when node f is grounded. Because of the capacitance and forward drop matching of diodes D3-D8, the spikes fed through to node g will largely cancel each other, if the gate pulses applied to D7 are the mirror images of those applied to D8. The means for developing these complementary gate pulses will be described in the next section. The voltage offset of the bridge can be compensated by adjusting R_2 so that a small current flows into the source resistance. Since a source resistance less than 500 ohms is impractical (i.e., $R \geq 1000$ ohms in Fig. 1), a current of less than 4 μA from the bridge into the source develops a voltage sufficient to compensate for the bridge offset.

3. Gate Pulse Circuit

The purpose of the gate pulse circuit (Fig. 3) is to convert unipolar rectangular input pulses (such as TTL logic) into complementary gate pulses suitable for gating the diode bridge on and off. It consists of two cascaded, inverting wide band amplifiers driven through an optically isolated gate. The open collector of the output transistor of this gate (node d) is loaded with a 1 kΩ resistor.

The offset adjustments of AR1 and AR2 are made as follows: (1) ground nodes d and e, adjust R4 for zero output voltage from AR1, and adjust R5 for zero output from AR2. (2) Unground nodes d and e. Then, apply a positive dc voltage of about 4V to the input of the optically isolated gate and adjust R3 for an output voltage of +0.35V from AR1. (The output from AR2 should be -0.35V). With positive input gate pulses of 3.5V to 5V, the output voltage excursions from AR1 should be between +0.35V and -0.95V, approximately. The output of AR2 will be the complement of these values. These drive voltages to the diode bridge are the minimum excursions that may be used if the input is limited to

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[1] Manufacturer's specifications.

±0.60V during non-viewing periods (diode bridge reverse biased) and is no larger than 100 mV during the viewing periods.[2] The specified unity gain settling time to 0.1 percent is 200 ns and 100 ns, respectively, for AR1 and AR2. As configured, the bandwidth is much wider for AR2 than for AR1 so that amplifier AR2 faithfully amplifies the output of AR1 by a factor of -1. Thus, the gate pulses applied to D8 from AR2 are the mirror images of those applied to D7 from AR1. Also, these gating pulses are the smallest that can be used for proper operation of the bridge. As mentioned previously, the bridge diodes and gating diodes (D7 and D8) are matched for forward voltage drop and shunt capacitance. Therefore, all basic conditions have been met for minimal switching transients at the bridge output.

The voltage transitions at the output of AR1 and AR2, corresponding to the leading edge of a rectangular voltage pulse applied to the optically isolated gate, are shown in the lower oscilloscope traces of Fig. 4A. The diode bridge is turned "on" during these transitions and the switching transient appearing in the bridge output (upper trace) decays to a 200 μV amplitude within 350 ns after the start of these transitions. The oscilloscope bandwidth for the lower traces is 200 MHz and is 105 MHz for the upper trace. Since the measured differential delay for these two oscilloscope channels is 20 ns, the transient decay time is somewhat less than shown. Figure 4B is similar to 4A except that the oscilloscope sensitivity has been reduced for the upper trace. The signal input to the bridge is zero for each of these photographs. The response of the bridge to input voltage steps such as V(t) of Fig. 1 is illustrated in Fig. 4C. The first transient in the bridge output (upper trace) is caused by capacitive feedthrough from a 0 to -5V transition (lower trace), applied when the bridge is off. The second transient is caused mostly by the gating voltages which turn the bridge on; however the length of this transient is increased slightly (to about 400 ns) by the -5V pulse, whose trailing edge approximately coincides with the time of bridge turn-on.

After the bridge has been gated on, its response to rapid input voltage changes is determined by the RC time constant of the overall bridge circuit and is typically around 45 ns: 60 pF load capacitance (oscilloscope, cable and bridge capacitance to ground) and 750 Ω series resistance, including a bridge resistance of ~200 Ω. The measured temperature coefficient of bridge offset is less than 20 μV/°C.

As indicated previously, the capacitance between nodes f and g is ~1 pF when the bridge diodes are cut off. If 60 pF is assumed to be the load capacitance, the maximum high frequency signal that can feed

[2] These values are based on nominal forward drops of 0.25V for diodes D3-D6 when the bridge is gated on, and 0.35V for diodes D7 and D8 when the bridge is gated off.

through to the oscilloscope is the clipping voltage level (600 mV) multiplied by the 1/60 capacitance divider ratio, which is 10 mV. This feedthrough level is too small to overdrive the oscilloscope in most practical applications of the bridge.

The diode bridge and gate pulse circuit were first operated with a delayable gate pulse generator designed at NBS and briefly described in the next section. This circuit is inexpensive to construct and satisfactory for many applications. Later, for convenience and general utility, the diode and gate pulse circuit were packaged in a module that plugs into a commercial mainframe containing a triggerable pulse generator. The commercial pulse generator has characteristics similar to the NBS delayable gate pulse generator. Figure 5 shows the module and the mainframe in which it is used. The gate pulse circuit is driven from the triggerable pulse generator, shown mounted in the mainframe.

4. Delayable Gate Pulse Generator

This circuit (Fig. 6) generates rectangular pulses which are applied to the gate pulse circuit and are delayed relative to the synchronization pulses used to trigger the oscilloscope. The delays and widths ("window" size) of the gate pulses are essentially continuously adjustable to facilitate use of oscilloscope sweep speeds ranging approximately from 10 ns/division to 1 ms/division.

The delay circuit consists of short, medium and long time delay function blocks. A simplified schematic diagram of the delay and window circuits is shown in Fig. 7. The short time delay utilizes the propagation delay of integrated logic gates and employs cascaded NOR gates to develop up to 200 ns delay in increments of 20 ns. The medium time delay is a monostable multivibrator whose output pulse length (delay) is adjustable by means of R1 from 100 ns to 1.5 μs. The long time delay circuit employs a 555 type of integrated circuit timer and has a pulse length (delay) adjustable by means of R2 from 1 μs to 10 μs. The long time delay circuit is driven from the medium delay circuit via a monostable multivibrator with fixed pulse length.

The circuit which determines the window size is similar to the long time delay circuit and its drive circuit, except that the pulse width (window size) is adjustable from 5 μs to 5 ms in 3 ranges using capacitors C1 through C3 in conjunction with R3.

5. Conclusion

A Schottky diode bridge and associated gating and delay circuits have been described which facilitate the measurement of low level signals preceded by large signals without overdriving the measuring instrument.

The diode bridge is well suited for making measurements using a wideband oscilloscope with vertical deflection sensitivities as high as 1 mV/cm. Therefore, the amplitude of rapidly varying signals can be measured to within 100 μV. When the bridge is gated on, the transient at its output is less than 8 mV and decays to 200 μV in less than 400 ns. When the bridge is gated off, high frequency feedthrough is less than 10 mV. This is too small to overdrive the oscilloscope in most practical applications of the bridge. The measured temperature offset of the bridge is less than 20 μV/°C.

6. References

[1] G. A. Korn and Theresa M. K. Korn, Electronic Analog Computers, McGraw-Hill, Inc., 1964.

[2] Analog Devices, Inc., Norwood, Mass., Nonlinear Circuits Handbook, 1976.

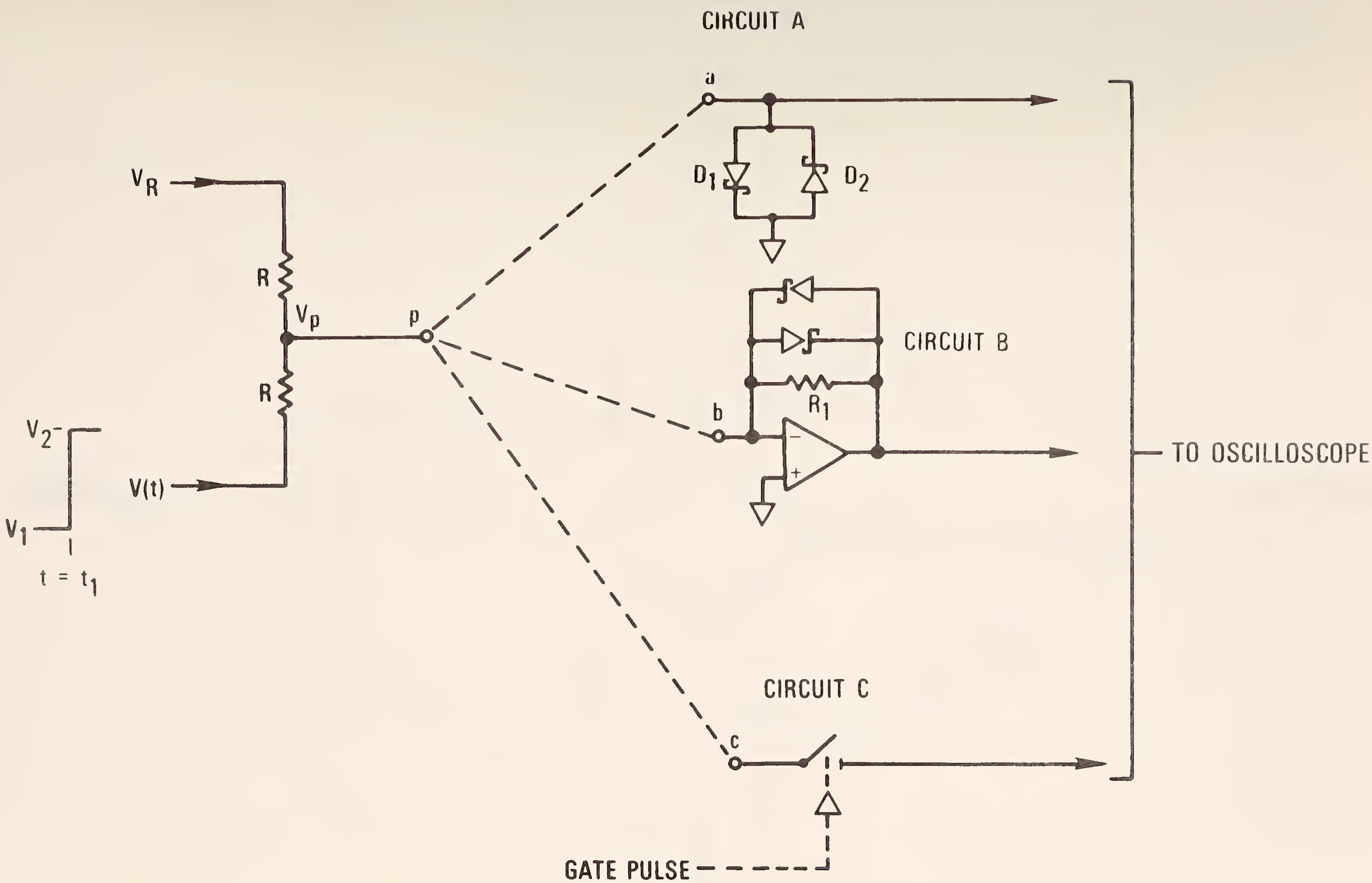

Figure 1. Settling time measurements

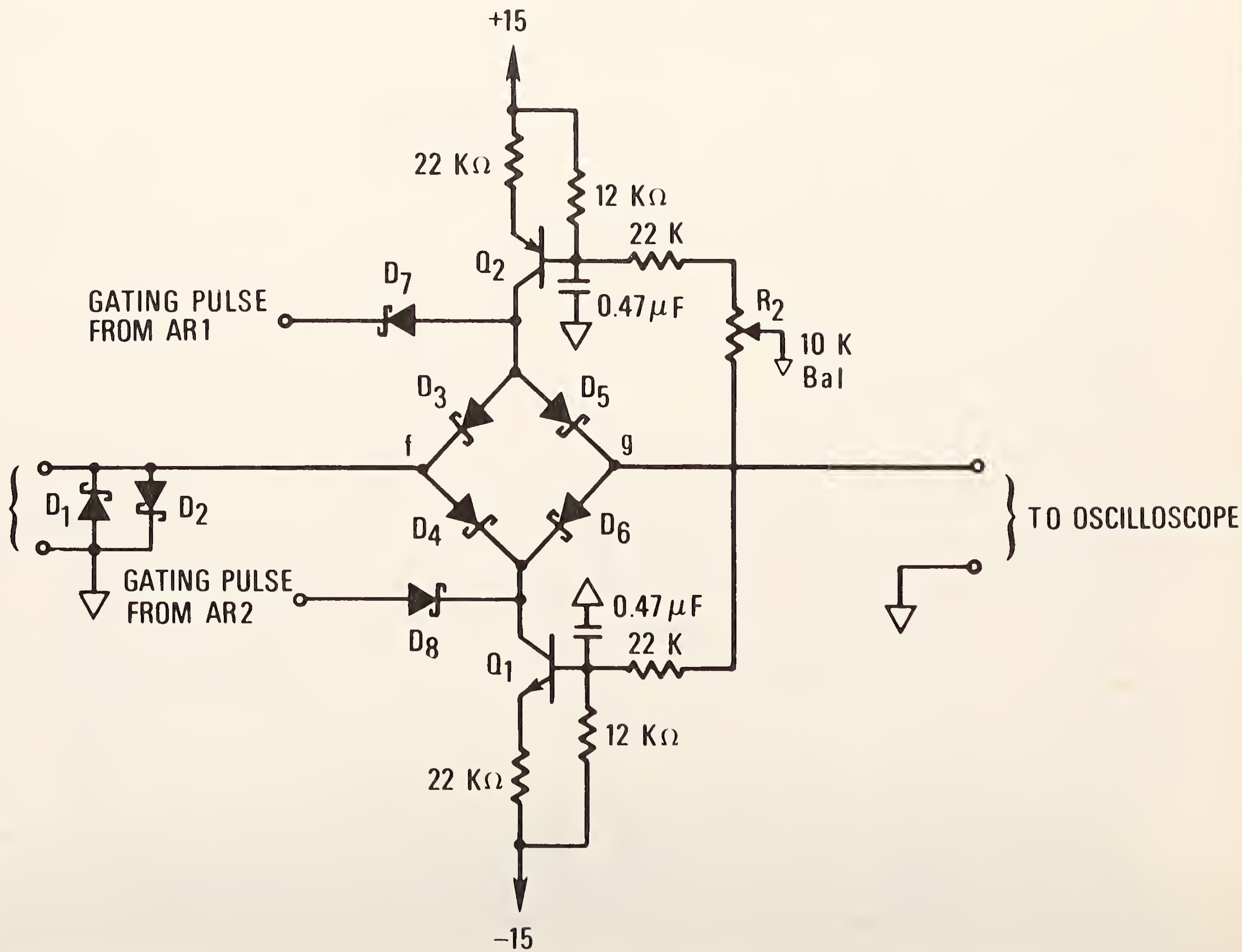

Figure 2. Diode bridge and associated circuits

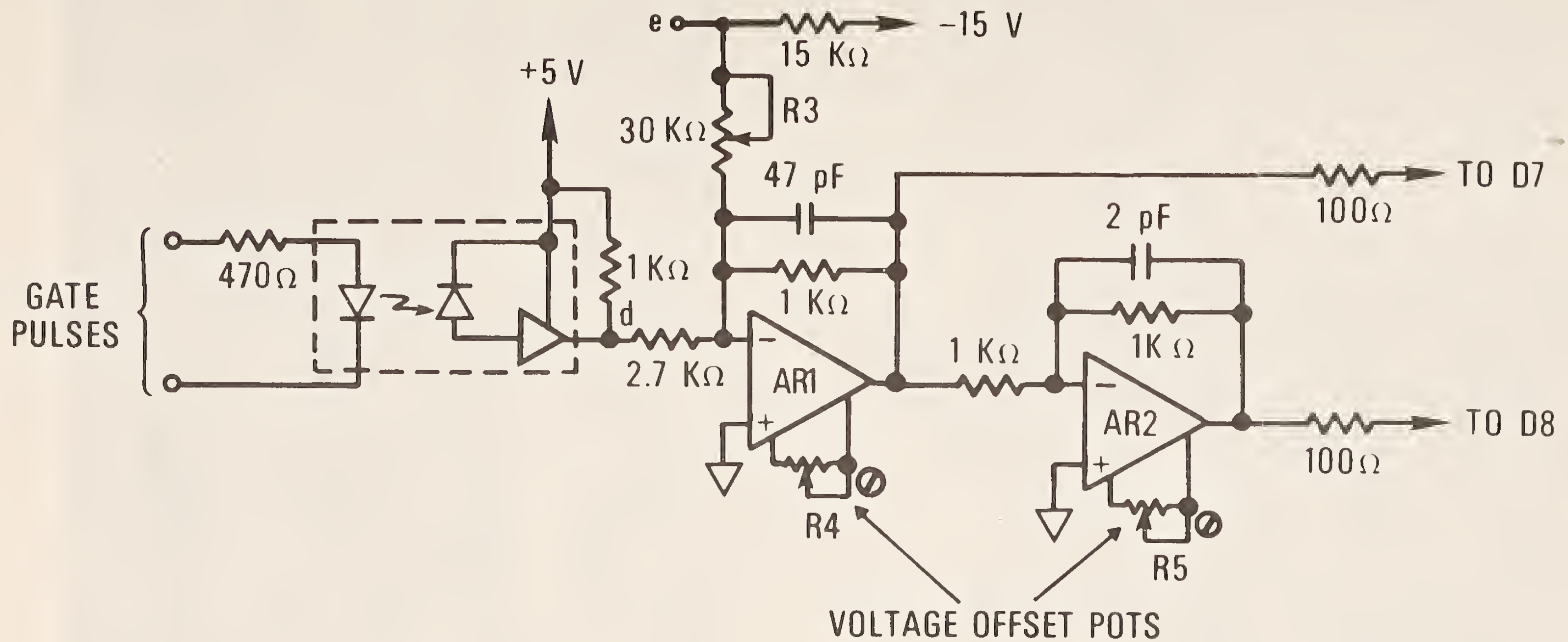

Figure 3. Gate pulse circuit

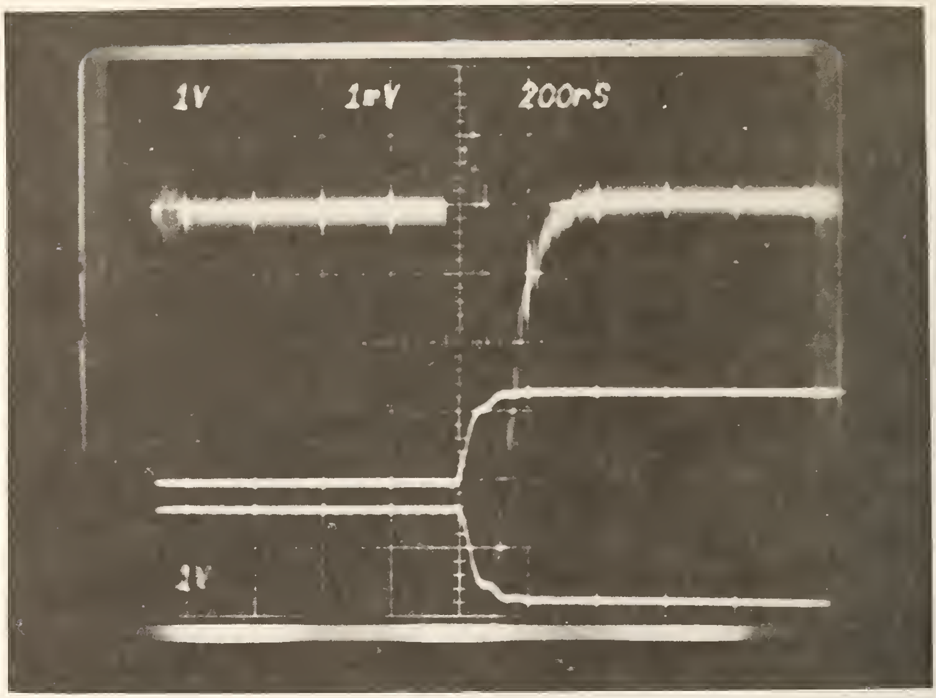

Figure 4(a)

The switching transient (upper trace) at output of diode bridge when it is turned "on" by the gating voltages (lower traces).

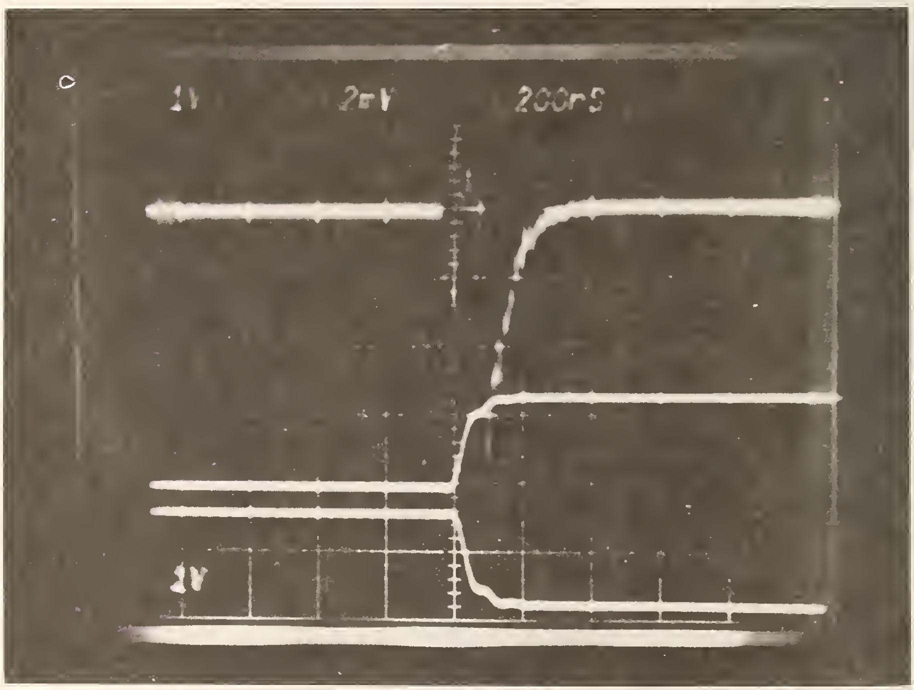

Figure 4(b)

Same as 4(a) except for lower scope sensitivity on upper trace.

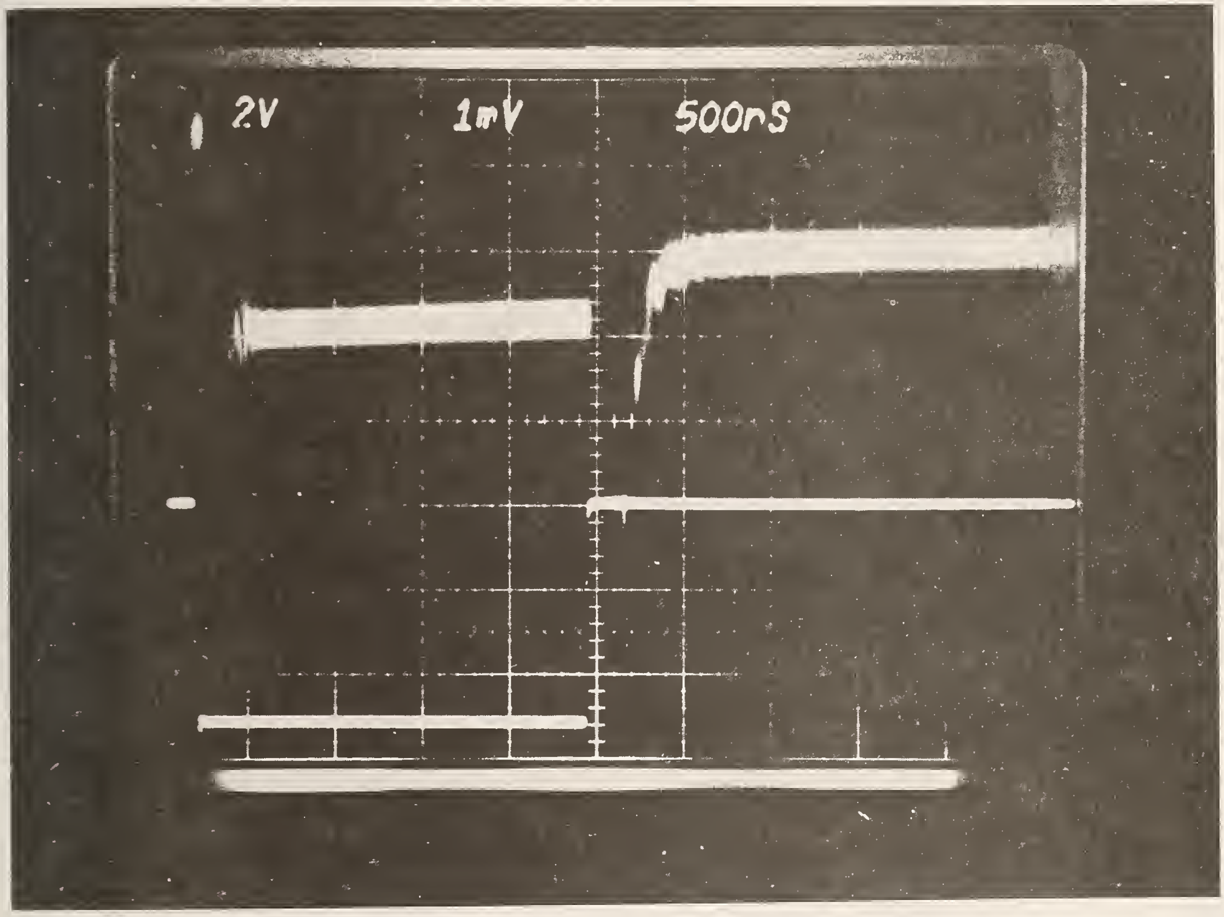

Figure 4 (c)

Bridge output response (upper trace) to -5V input pulse (lower trace). Bridge turn-on coincides approximately with the -5V to 0V transition.

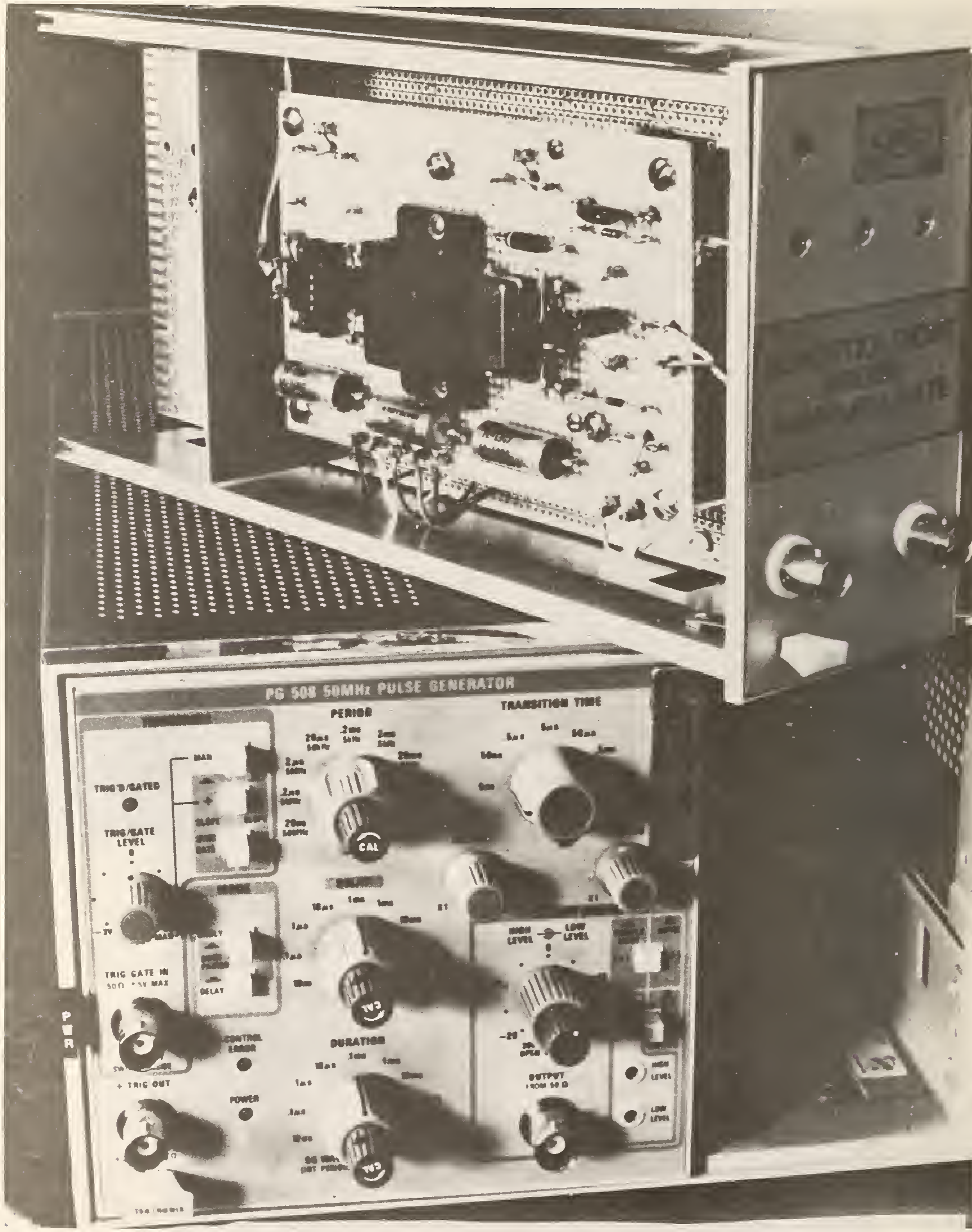

Figure 5. Module of diode bridge and gate pulse circuits and the mainframe in which it is used.

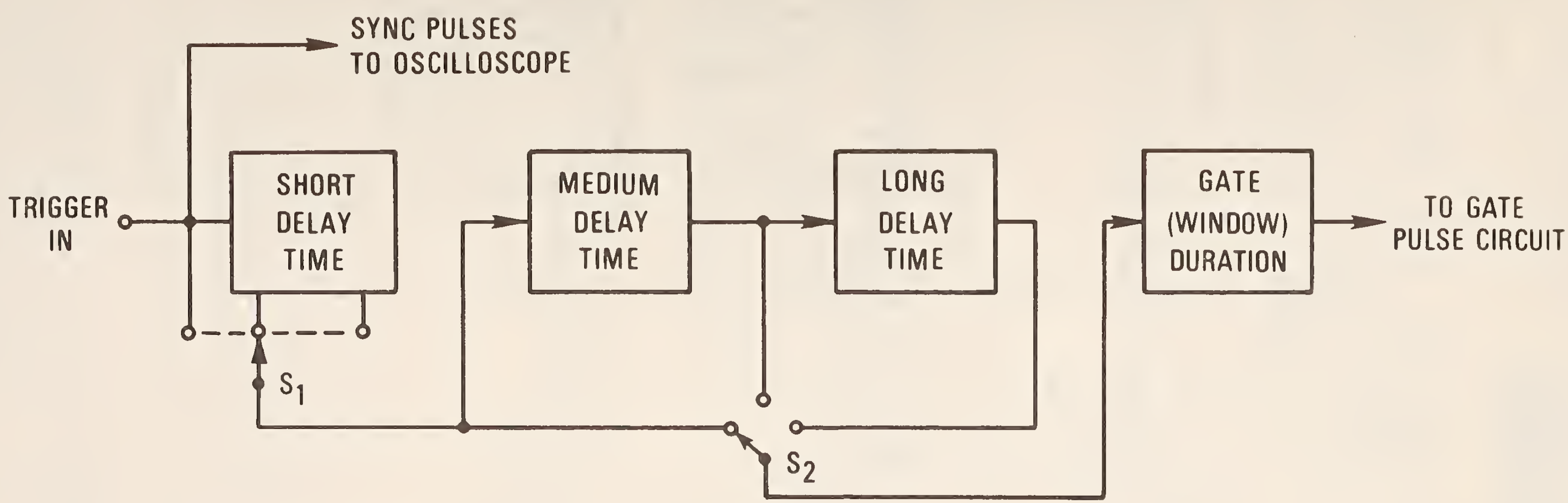

Figure 6. Block diagram of delay and window circuits

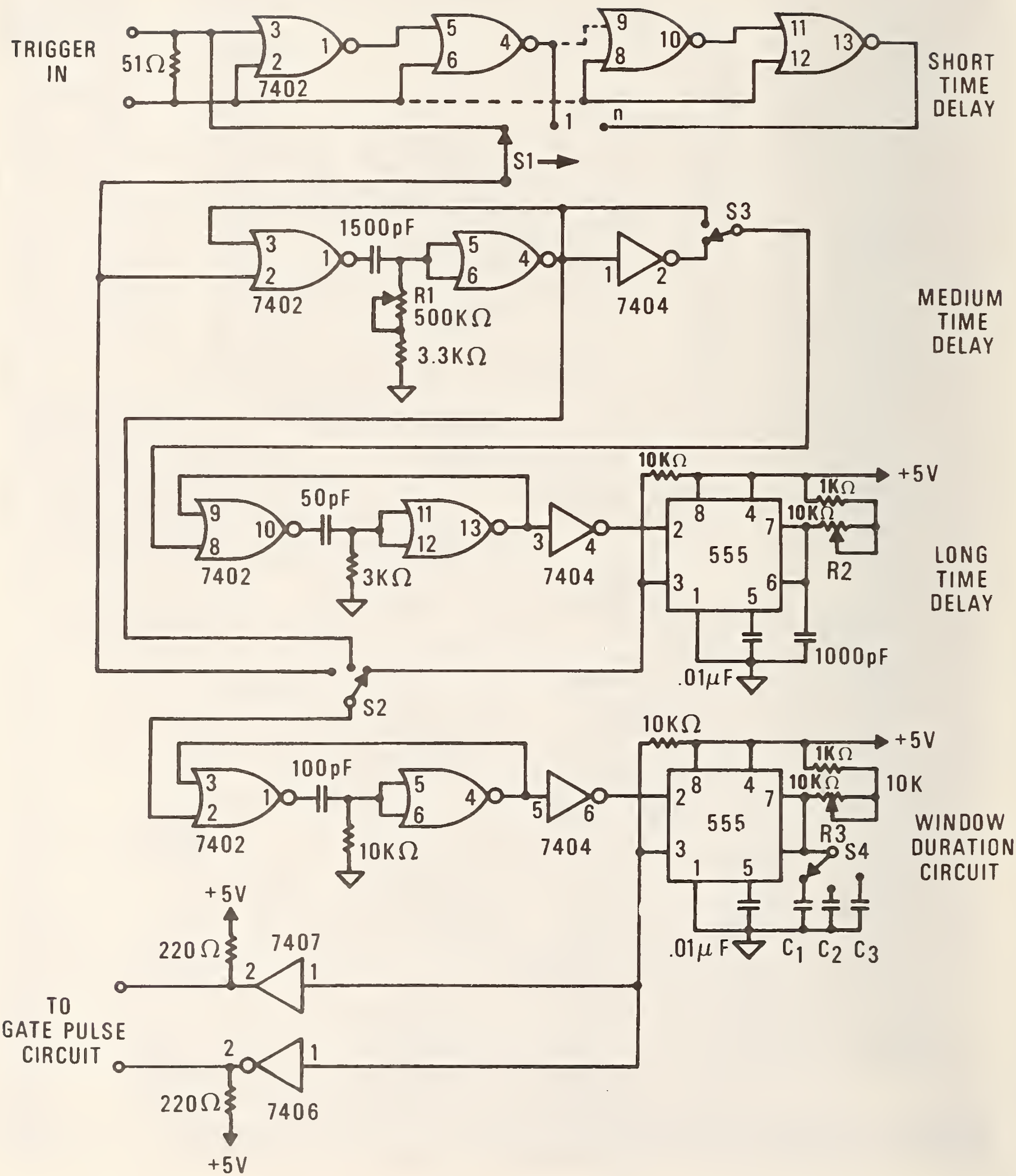

Figure 7 Schematic diagram of delay and window circuits

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15. SUPPLEMENTARY NOTES

☐ Document describes a computer program; SF-185, FIPS Software Summary, is attached.

16. ABSTRACT *(A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.)*

A Schottky diode bridge and associated gating and delay circuits have been designed to facilitate the measurement of low level signals preceded by large signals without overdriving the measuring instrument. This measurement problem occurs in testing or evaluating operational amplifiers, digital-to-analog converters, sample/hold amplifiers and other similar active circuits.

17. KEY WORDS *(six to twelve entries; alphabetical order; capitalize only the first letter of the first key word unless a proper name; separated by semicolons)*

Diode bridge sampling gates; diode bridge switches; diode clipping circuits; diode shunt limiters; Schottky diode bridge; time controlled sampling

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