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Large Scale Integration Digital Testing— Annotated Bibliography, 1969-1978

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Table of Contents

LARGE SCALE INTEGRATION DIGITAL TESTING — ANNOTATED BIBLIOGRAPHY, 1969 - 1978

T. F. Leedy

This annotated bibliography covers articles published in the field of semiconductor device testing. The bibliography contains (1) entries divided into six economics of testing, (2) monolithic circuit testing, (3) the testing of subsystems of large scale integrated circuits such as microcomputer boards and memory arrays, (4) various test strategies used to locate a defective LSI circuit, (5) test equipment available for LSI testing, and (6) various measurement methods that may be of interest to the test engineer.

Key Words: Electronics; integrated circuit; large scale integration; memory; microprocessor; testing.

1. INTRODUCTION

The testing of digital semiconductor devices, especially complex integrated circuits, is a difficult task that must be performed to assure their proper electrical operation. Over the past decade, small- and medium-scale integrated circuits have had a profound influence on electronic circuit design. This trend is likely to be overshadowed by large scale integrated (LSI) circuits in the next decade. The two main production considerations of LSI circuits are efficient processing and cost-effective testing. This bibliography is primarily concerned with the engineering methods and equipment for testing these complex devices and their associated systems. This bibliography does not purport to be an exhaustive search of the literature. Rather, it is a listing of references that cover the many diverse techniques to assure proper performance of LSI devices and systems. As such, this bibliography may serve as an introduction to the literature of LSI testing for those not familiar with the techniques. In general, papers dealing with the reliability and failure analysis of semiconductor devices have not been included although device testing is an integral part of this discipline.

The bibliography is divided into six sections. The first section deals with the necessity for testing LSI devices and systems and the resultant economic benefit for both the vendor and consumer. The next section considers those test methods that may be applied to monolithic LSI circuits where the level of diagnosis and repair is the IC itself. The third section contains references to logic boards and to small systems that contain LSI parts. The testing techniques at this level are different from those for testing monolithic units since the interconnections between LSICs may be faulty and the defective parts must be identified in order for the system to be repaired. In the next section are found references to articles on the strategies employed in either the design or testing of LSI circuits and systems. The fifth section covers various

aspects of testing equipment that is commercially produced or designed for specialized applications. The last section is concerned with the measurements of the electrical signals in LSI testing.

Sources for the bibliography were personal files, literature citations in papers collected, and manufacturer's technical notes. Additionally, computer searches of the *Electronics and Computer Abstracts* of INSPEC from 1969 to 1977, the NTIS Abstracts from 1964 to 1977, and the COMPENDEX from 1970 to 1977 were made.

2. NEED AND ECONOMICS OF TESTING

1. Anderson, R. E., Test Methods Change to Meet Complex Demands, *Electronics* 49, No. 8, 125-128 (April 15, 1976).

   Several factors affect the ability of a microprocessor to be tested. Unique failure modes, the inability to gain access to internal logic, and high test speeds make testing devices difficult. Thus, extra testing at the board level is also needed.

2. Anon., Demand for LSI Brings Test Crunch, *Electronics* 51, No. 18, 46 ff (August 31, 1978).

   This note describes the need for test methods for the automotive, computer, instrument, and telecommunications markets.

3. Anon., Military Too Strict on Microprocessors, *Electronics* 49, No. 5, 38 ff (March 4, 1976).

   The claim is made that the specifications on which the military rely are outmoded and call for too many screening and test steps.

4. Anon., Semiconductor Testing: So Who Needs It? (Fairchild Systems Technology, San Jose, California).

   A transcript of a discussion among eight persons on the various aspects of testing philosophies, available test equipment, and the management issues that are associated with semiconductor testing.

5. Boudreault, A. L., Automatic Test Equipment in the Production Process, *IEEE Trans. Manufacturing Technology* MFT-4, No. 2, 48-52 (December 1975).

   A cost analysis of testing is important prior to the purchase of test equipment. Such an analysis must include the cost of both testing incoming components and the cost of not testing them.

6. Boudrealt, A. L., Quality Control ... A Savings Center, *Quality* 16, No. 9, 20-21 (September 1977).

   The testing of printed circuit board assemblies is necessary for an electronic equipment manufacturer to be cost effective.

7. Chrones, C., Calculating the Cost of Testing LSI Chips, *Electronics* 51, No. 1, 171-173 (January 5, 1978).

This is an analysis of how much it will cost to test an LSI chip on a cost-per-unit basis.

8. Chrones, C., Testing LSI: An Independent Viewpoint, *Electronic Products* 20, No. 10, 65-68 (March 1978).

This article alerts the user to the crucial need to test LSI, explains why this is not a trivial task, and outlines how it may be done.

9. Egan, F., and Speer, R., Eds., IC Testing — A Special Report, *Electronic Design* 16, No. 18, 50-71, 74-76 (September 1, 1968).

This report, in six sections, considers IC testing from the viewpoint of the manufacturer, aerospace and industrial users, and the test equipment manufacturer.

10. Grossman, S. E., Automated Testing Pays Off for Electronic System Makers, *Electronics* 47, No. 19, 95-109 (September 19, 1974).

This article is a review of the test equipment available along with an economic analysis of testing both components and boards.

11. Hnatek, E. R., High-Reliability Semiconductors: Paying More Doesn't Always Pay Off, *Electronics* 50, No. 3 (February 3, 1977).

The premium paid for high reliability is more important for discretes than for integrated circuits. The study is based on the data from approximately 190,000 high-reliability semiconductor devices over an 18-month period.

12. Hodges, D. A., A Review and Projection of Semiconductor Components for Digital Storage, *Proc. IEEE* 63, No. 8, 1136-1147 (August 1975).

This paper considers the use of MOS, MNOS, CCD, and bipolar technologies as alternatives to moving-surface memories. Other device technologies and circuit designs are also examined.

13. Johnson, R., User Experiences in Testing Microprocessors, *Proc. Technical Program, International Microelectronic Conference,* Anaheim, California, February 24-26, 1976 and New York, New York,

June 8-10, 1976, pp. 68-73 (Industrial and Scientific Management, Inc., Chicago, 1976).

This paper describes the economic justification for in-house microprocessor testing, presents a description of a tester developed by a user, and concludes with observations regarding the cost savings which have been realized.

14. Koppel, R. J., and Maltz, I. R., Cost, Performance, and Reliability Tradeoffs in Semiconductor Memory Systems, *13th IEEE Computer Soc. Int. Conf.*, September 7-10, 1976, Washington, D.C., pp. 218-222.

This paper reviews the several aspects of system organization and the resulting performance tradeoffs. It is followed by a review of reliability considerations including the use of error-correcting techniques.

15. LeBoss, B., LSI: The Testing Nightmare, *Electronics* 50, No. 25, 65-66 (December 8, 1977).

Increased device and testing complexity along with high test system cost provides a bad situation which will probably get worse in the future.

16. Loranger, J. A., Jr., The Case for Component Burn-In: The Gain is Well Worth the Price, *Electronics* 48, No. 2, 73-78 (January 23, 1975).

The system designer can calculate what component burn-in will save in overall cost. Several authorities testify that burn-in is both an economical and effective way to reduce field failures.

17. Melgaard, H., Reducing Burn-In Operating Costs, *Circuits Manufacturing* 18, No. 6, 36-37 (June 1978).

The author states that a semiconductor burn-in oven may be operated more economically by taking measures to reduce wasted heat and by using higher temperature for shorter times.

18. Mow, W. C. W., Zero Overhead Testing for LSI, *Proc. Technical Program, Semiconductor/IC Processing and Production Conf.*, Anaheim, California, February 8-10, 1972, pp. 25-28 (Industrial and Scientific Conference Management, Inc., Chicago, 1972).

A new concept for the testing of large scale integration is described that requires no user software and lends itself to a com-

pletely modular approach for total system integration. The new concept consists of interdisciplinary areas such as software requirements, dynamic accuracies of testing, LSI product types, and function and parametric speeds related to various product lines.

19. Rubinstein, E., Independent Test Labs: Caveat Emptor, *IEEE Spectrum* 14, No. 6, 44-50 (June 1977).

This article provides an overview of what services are performed by the independent test laboratories. Additionally, it gives the advantages and disadvantages of using an independent test laboratory.

20. Runyon, S., How to Test Those LSI Chips: Watch out for 'Ifs' and 'Buts,' *Electronic Design* 23, No. 22, 74-78 (November 22, 1975).

A general review of the problems that plague the testing of large scale integration from various points of view is presented.

21. Salvador, J., Today's Dynamic IC Tests Won't Work Without Meaningful Specs, *Electronics* 44, No. 23, 91-94 (November 8, 1971).

The necessity of correctly defining logic levels, pulse shapes, and timing intervals is stressed.

22. Seltzer, R., Future Test: How to Cope With the Changing World of LSI, *Circuits Manufacturing* 17, No. 12, 33 ff (December 1977).

A review of the major developments presented at the IEEE Semiconductor Test Symposium, Cherry Hill, New Jersey, in 1977.

23. Taren, W., Semiconductor Memory Systems: How Much Do They Really Cost? *Electronics* 43, No. 21, 94-97 (October 12, 1970).

System builders often find that the cost advantage of their custom-designed memories is much reduced after consideration is given to testing.

24. Van Veen, F., An Introduction to IC Testing, *IEEE Spectrum* 8, No. 12, 28-37 (December 1971).

This article focuses on problems encountered and techniques employed in testing both digital and linear ICs.

25. Waller, L., Testing for Others Means Business, *Electronics* 51, No. 6, 92-94 (March 16, 1978).

Macrodata, a manufacturer of test equipment, is now performing IC tests for others. This is not only profitable, but also allows the building of a library of test programs.

26. Waller, L., Tests Show Spotty LSI Record, *Electronics* 51, No. 3, 78-80 (February 2, 1978).

A three-year program at the Jet Propulsion Laboratory to find LSI devices for unmanned space applications pinpoints faults in specifications, performance and testing.

3. INTEGRATED CIRCUIT TESTING

27. Anderson, R. E., How to Approach the Microprocessor Testing Problem - Some Guidelines, *Proc. Technical Program, International Microelectronics Conference*, Anaheim, California, February 24-26, 1976, and New York, New York, June 8-10, 1976, pp. 77-81 (Industrial and Scientific Management, Inc., Chicago, 1976).

The testing of microprocessors requires the use of different test equipment than used for integrated circuits and logic boards. Often, the task of microprocessor testing is more difficult, and the test equipment more expensive; there are some techniques that enable cost-effective testing for low-volume users of microprocessors.

28. Barraclough, W., Chiang, A. C. L., and Sohl, W., Techniques for Testing the Microcomputer Family, *Proc. IEEE* 64, No. 6, 943-950 (June 1976).

The microcomputer family is defined as consisting of microprocessor units and random-access memories. Equipment necessary to test these components is described along with a new testing approach called modular sensorialization.

29. Beaumont, J., Performance Evaluation of the CCD450 Digital Memory, Master's thesis, Air Force Institute of Technology, Wright-Patterson Air Force Base, Ohio School of Engineering (1975). (NTIS Accession No. AD/A 019810/ST.)

The Fairchild CCD450 9216-bit CCD memory was dynamically tested using a commercial tester and an interface designed by the author. Comparisons were made of the performance of the memory to that specified by the manufacturer.

30. Beck, R., Functional Testing an IC Memory, Application Report 105 (Teradyne, Inc., Boston, Massachusetts, 1970).

It is often impractical to perform exhaustive tests on IC memories for all possible combinations of inputs. This report states that savings in time can be achieved by isolating the possible fault modes of the device and then establishing a test sequence designed to detect those particular faults.

31. Borne, R. B., Jr., Fault Detection in Bipolar Integrated Circuit Outputs, Application Report 113 (Teradyne, Inc., Boston, Massachusetts, 1973).

The testing of output characteristics of bipolar digital integrated circuits is described using a commercial tester. Both functional and parametric tests are considered for various devices including multiple output types and those with open collector and high voltage outputs.

32. Carroll, B. D., Development of Automated Test Procedures and Techniques for LSI Circuits, Final Report, Contract No. NAS8-31190 (Department of Electrical Engineering, Auburn University, Alabama, September 4, 1975). (NTIS Accession No. NASA-CR-143951.)

The use of automatic test pattern generation is applied to testing large scale integrated logic circuits. An algorithm is presented that can be applied to test both combinational and sequential logic circuits.

33. Chiang, A. C. L., Reliability Evaluation of Semiconductor Memories, Final Report, Contract No. F30602-74-C-0093 (Macrodata Corporation, Woodland Hills, California, February 1976). (NTIS Accession No. AD/A 021421/3ST.)

This report investigated the parametric and functional tests of high usage memories which are required for military specifications. Special attention was given to the application of functional tests to determine if a memory suffers from pattern sensitivity.

34. Chiang, A. C. L., and Sandridge, R., Pattern Sensitivity on 4K Devices, *Computer Design* 14, No. 2, 88-90 (February 1975).

Detailed here are test programs that allow characterization of address access time with respect to device power supply, thereby permitting effective screening and aiding in evaluation of vendor specifications.

35. Chrones, C., Testing Microprocessor Chips: A Large-Scale Challenge, *Electronic Packaging and Production* 15, No. 4, 35 ff (April 1975).

This article describes the various philosophies used to test microprocessors such as testing its various component parts and the testing of the whole chip by execution of a worse-case program. A description of commercial testing equipment is also presented.

36. Colbourne, E. D., Coverly, G. P., and Behera, S. K., Reliability of MOS LSI Circuits, *Proc. IEEE* 62, No. 2, 244-259 (February 1974).

MOS LSI circuits possess many of the reliability problems associated with discrete semiconductors and MSI circuits. Their complexity requires that different methods are used to assure their reliability. Specific areas considered are pattern sensitivity, manufacturing controls, assembly, packaging, and electrical testing.

37. Colasanti, L., Burn-in for Device Screening, *Circuits Manufacturing* 18, No. 7, 42 ff (July 1978).

A review of the various burn-in tests for the detection of infant-mortality type failures. Also covered are the various physical configurations of high-temperature testing equipment available for both static and exercised operation of devices. Following this article is a list of vendors of testing equipment and services.

38. Fischer, J. E., 4K RAMs: Increased Densities Bring Difficult Testing Problems, *EDN* 19, No. 22, 47-51 (November 20, 1974).

Several test patterns that can be effective tools in the search for the ideal pattern are proposed.

39. Foss, R. C., Harland, R., and Roberts, J. A., Check List for 4096-Bit RAMs Flags Potential Problems in Memory Design, *Electronics* 49, No. 18, 103 (September 2, 1976).

Consideration should be given to at least ten requirements for 4K RAM systems to assure reliable system operation. The article also suggests procurement strategies for the purchase of RAM devices.

40. Foster, R. C., Goldberg, J., Levitt, K. N., and Wensley, J., H., An Organization for a Highly Survivable Memory, *IEEE Trans. Computers* C-23, No. 7, 693-705 (July 1974).

A memory organization is considered for which a large number of faults can be tolerated at a low cost in redundancy. The primary element in the system is an LSI chip that realizes a section of the memory. The chips are connected via a switching network so that the memory can be reconfigured effectively in the presence of chip failures.

41. Greenwood, W. T., Jr., Reliability Testing for Industrial Use, *Computer* 10, No. 7, 26-30 (July 1977).

The uses of IC burn-in are discussed as an important test technique to assure reliable devices. Burn-in will increase in importance as devices become more complex.

42. Grooms, D. W., Ed., Random Access Memories: Citations From the Engineering Index Data Base, NTISearch NTIS/PSA-76/0998/5EES (December 1976). (Available from the National Technical Information Service, Springfield, VA 22161).

Research on the design, testing, and application of random access computer storage devices is cited in this bibliography of world wide journal literature. This bibliography was prepared by searching the 1974 to 1976 data base of Engineering Index. It contains 178 abstracts.

43. Hnatek, E. R., An Introduction to Microprocessor Testing — Problems and Test Methods, *Proc. Technical Program, Int. Microelectronics Conf.*, Anaheim, California, February 24-26, 1976, and New York, New York, June 8-10, 1976, pp. 59-67 (Industrial and Scientific Management, Inc., Chicago, 1976).

Designers should modify traditional component testing concepts and restructure their thinking to treat the CPU as a system rather than an assembly of components. The point is made that testing a CPU is at best a trial-and-error procedure. More effective and efficient means of testing a CPU must developed.

44. Hnatek, E. R., Checking Microprocessors? *Electronic Design* 23, No. 22, 102-105 (October 25, 1975).

Four methods are discussed which may be used to test microprocessor systems. These are the self-diagnostic type of test, the comparison approach, using algorithmic pattern generation, and the stored response type of testing.

45. Hnatek, E. R., User's Tests, Not Data Sheets, Assure IC Performance, *Electronics* 48, No. 24, 108-113 (November 27, 1975).

Designers should do their own characterization of LSI devices to assure performance in each application. Examples are given on characterizing a NAND gate and comparing two different RAM types.

46. Huston, R., Microprocessor Function Test Generation on the Sentry 600, Technical Bulletin 4 (Fairchild Systems Technology, San Jose, California, 1974).

The test generation technique described uses a known good microprocessor and the Sentry 600 to develop the truth table from a user's diagnostic written in the microprocessor's own machine code or assembly language. The generation program can be composed without having to know the internal architecture of the microprocessor.

47. Huston, R. E., Testing Semiconductor Memories, *Digest of Papers, IEEE Symp. Semiconductor Memory Testing*, Cherry Hill, New Jersey, October 2-3, 1973, pp. 27-62. [Available from IEEE (73 CH0827-6C), New York, New York.]

Various test patterns for random access memories are described and their applications are discussed. Analysis techniques for random access memory characterization are presented.

48. Jones, D., and Cheek, T., Error Correction Strategies Safeguard Control Hardware, *EDN* 22, No. 17, 109-111 (September 20, 1977).

This article is a discussion of methods to modify microprocessor software to avoid having to remask ROMs if errors are detected.

49. Keonjian, E., and Mizell, L., Establishing an Electrical Test Philosophy for LSI Microcircuits, Volume 1, Final Report, Contract No. NAS8-25832 (Grumman Aerospace Corporation, Bethpage, New York, February 1971). (NTIS Accession No. N71-26703.)

A preliminary study on various contemporary LSI testing techniques was conducted. The techniques were categorized into logic type (combinatorial and sequential) and the type of electrical testing (functional and parametric). Electrical parameters specified on each type of LSI device were listed and the parameters specified by each manufacturer were tabulated. A study was also made of available LSI test equipment.

50. Keonjian, E., and Mizell, L., Establishing an Electrical Test Philosophy for LSI Microcircuits, Volume 2, Final Report, Contract NAS8-25835 (Grumman Aerospace Corporation, Bethpage, New York, February 1971). (NTIS Accession No. N71-26704.)

Specific guidelines are developed for high-reliability testing at the wafers and package levels. Functional and parametric testing

is discussed and recommendations are made for MOS and bipolar devices. Specifications for an LSI test system are outlined.

51. Kravtsov, A. D., Kryukov, V. P., Zolotarev, T. V., Ivannikov, A. Z., and Toropov, A. D., Testing and Diagnostic Methods for Semiconductor Integrated Memory Devices, *Izv. Vyssh. Uchebn. Zaved. Radioelectron.* 20, No. 1, 41-44 (January 1977).

A procedure for testing memories employing a computer-controlled tester is presented. The instrumentation used in the automated performance tests and in fault diagnosis of the memory devices is discussed. (In Russian.)

52. Kreuwels, W. G. J., Structural Testing of Digital Circuits, *Philips Technical Review* 35, No. 10, 261-270 (January 28, 1976).

The article begins with a review of faults in a digital network. It describes two programs, TESTCC and TESTSC, for testing combinational and sequential networks, respectively. Networks with a maximum of 1000 gates can be processed.

53. Levine, L., and Myers, W., Timing: A Crucial Factor in LSI-MOS Main-Memory Design, *Electronics* 48, No. 14, 107-111 (July 10, 1975).

Guidelines are provided that designers can follow to assure proper timing in a semiconductor memory system. Careful timing is essential to avoid bit errors.

54. Levitz, P. J., and Luce, A. N., Automated Testing for Electronics Manufacturing - LSI Testing for Reliability Assurance, *Circuits Manufacturing* 18, No. 3, 42-44 (March 1978).

To qualify LSI products made with new processes, engineers have developed a test chip to facilitate accelerated stress testing of particular devices. The final product is then stressed and the failure modes compared with the failure modes and the device performed within the expected reliability objectives.

55. Lindwedel, J. H., Reliability Evaluation of LSI Microcircuits, Final Report, Contract No. C72-032/201 (Autonetics Division, Rockwell International Corporation, Anahelm, California, April 1971 - October 1972). (NTIS Accession No. AD 911826/6ST.)

This study was performed to document the common failure modes of LSI devices and to find methods of electrical stress testing of

these components. A wide varity of device technologies were evaluated in the study.

56. Lo, T. C., and Guidry, M. R., An Integrated Test Concept for Switched-Capacitor Dynamic MOS RAMs, *IEEE J. Solid-State Circuits* SC-12, No. 6, 693-703 (December 1977).

Test procedures are developed from an understanding of the fabrication technology used in their construction. The associated design weaknesses are reviewed, and test programs for the detection of pattern sensitivity are presented.

57. Luciw, W., Can a User Test LSI Microprocessors Effectively? *Proc. Technical Program, Int. Microelectronics Conf.*, Anaheim, California, February 24-26, 1976, and New York, New York, June 8-10, 1976, pp. 74-76 (Industrial and Scientific Management, Inc., Chicago, 1976).

This article describes a testing system and philosophy for testing 8080 microprocessors. The basic test philosophy is to execute "random" instructions on "random" data. This approach is feasible because the execution of each instruction is largely independent of previous instructions.

58. Maluda, S., Production Test Routines for Minicomputers, *Quality* 17, No. 2, 12-15 (February 1978).

The strategy of a minicomputer manufacturer to provide a reliable product is discussed. Consideration is given to both the testing and management of a quality control program.

59. Mattera, L., Component Reliability, Part 1: Failure Data Bears Watching, *Electronics* 48, No. 20, 91-98 (October 2, 1975).

This first of a two-part review discusses many electronic components and their failure rates. Emphasis is placed on the failure of integrated circuits of all types.

60. Mattera, L., Component Reliability, Part 2: Hearing From the Users and Vendors, *Electronics* 48, No. 22, 87-94 (October 30, 1975).

This second of a two-part review gives information on how original equipment manufacturers and component vendors test electronic components, especially integrated circuits.

61. McDonald, J. C., Testing for High Reliability: A Case Study, *Computer* 9, No. 2, 18-21 (February 1976).

A testing approach used by a manufacturer of communications equipment to assure a reliable system is described. Epoxy-encapsulated TTL and ceramic MOS LSI devices were used in the study.

62. Mitchell, T., and Kane, G., Bipolar Control Storage Memory-Design Considerations and Test Problems, *Solid State Technology* 16, No. 3, 41-44 (March 1973).

A bipolar memory device used in the UNIVAC 9700 computer is discussed from the viewpoint of both system reliability and design as well as the philosophy of its incoming testing.

63. Muller, K., Zur Strategie der Elektrischen Funktionspruefung an Integrierten Halbleiterspeichern (Strategy of Electric Functional Testing of Integrated Semiconductor Memories), *Z. Elektr. Inf. Energietech.* 5, No. 2, 137-143 (1975).

The use of computer-aided testing system for memories is presented with emphasis on the peculiarities of MOS memories and the saving of testing time. (In German.)

64. Nelson, G. P., and King, E. E., Methods for Radiation Testing Random Access Memories and LSI Circuits, *IEEE Trans. Nucl. Sci.* NS-24, No. 6, 2341-2346 (December 1977).

A review of many approaches to testing LSI devices is presented. Additionally, methods are described to obtain the radiation response of CMOS RAMs to ionizing radiation.

65. Nelson, G. P., and Boggs, W. F., Parametric Tests Meet the Challenge of High-Density ICs, *Electronics* 48, No. 25, 108-111 (December 11, 1975).

A discussion of parametric tests which, in tandem with more common methods, can push minimum IC acceptability standards close to 99.99 percent level.

66. Padwick, G. B., Dynamic IC Testing Made Easy, *Electronics* 41, No. 20, 74-80 (September 30, 1968).

The importance of testing ICs at the speeds at which they are intended to operate is stressed. The basic concept of propagation

time and its measurement is essential to understanding the speed limitation of ICs.

67. Puri, Y., Stress Testing FET Gates Without the Use of Test Patterns, *IEEE J. Solid State Circuits* SC-10, No. 5, 294-298 (October 1975).

This gate stressing technique essentially results from sequencing the clock signals in a multiphase circuit in reverse order. Stressing by this method helps guarantee that devices with mobile ion contamination and/or gate breakdown will be found.

68. Richardson, W. S., Diagnostic Testing of MOS Random Access Memories, *Digest of Papers, IEEE Symp. Semiconductor Memory Testing*, October 2-3, 1973, Cherry Hill, New Jersey, pp. 7-20 (1973). [Available from IEEE (73 CH0827-6C), New York, New York.]

The problems of assembling the right testing equipment and utilizing the proper techniques and test sequences for diagnostic testing are discussed. An example is given to illustrate the difficulty of identifying trouble areas of an MOS memory.

69. Richardson, W. S., Diagnostic Testing of Random Access Memories, *Solid State Technology* 18, No. 3, 31-34 (March 1975).

The specific requirements of a memory test system and the hardware necessary to support the system are discussed. An example of a memory disturb problem is explained in detail.

70. Rickers, H. C., Microcircuit Device Reliability: LSI Data, Contract No. F30602-73-0065 (Reliability Analysis Center, Griffiss Air Force Base, New York, 1976). (NTIS Accession No. AD/A 023277/2ST.)

The compendium of Microcircuit Reliability data is separated into two parts. The General LSI Technology Summaries presents descriptions of the fabrication processes of LSI technologies. The Detailed Data Sections is arranged with each section devoted to a particular memory/LSI device function. Each section contains a detailed breakdown of part level life and environmental and screening tests arranged by part manufacturer and part number.

71. Schneider, B., Problemer Ved Test AF Komplekse IC. En Gennemgang AF en Del Specielle Problemer Ved Test AF MSI Og LSI Kredse Som F. Eks. RAM, ROM, Og CPU (Testing Problems of Complex Integrated Circuits. A Consideration of Special Testing Problems of MSI and

LSI Circuits Also of Random Access Memories, Read Only Memories and Central Processor Units), Report No. ECR-52 (Elektronikcentralen, Hoersholm, Denmark, May 1975).

A review of the problems associated with the purchase of automatic test equipment. Included are some special measurement problems and limitations of equipment to meet various measurement challenges. (In Danish with English summary.)

72. Schusheim, B., A Flexible Approach to Microprocessor Testing, *Computer Design* 15, No. 3, 67-72 (March 1976).

This paper describes the LEAD (Learn, Execute, and Diagnose) strategy of microprocessor testing. In this system, the microprocessor executes its own instructions and relies on the tester only for memory and peripherals.

73. Scrupski, S., Why and How Users Test Microprocessors, *Electronics* 51, No. 5, 97-104 (March 2, 1978).

This article is a review of various types of microprocessor test equipment from small to large systems. In addition, the types of testers used by the manufacturers of ICs are presented.

74. Smith, D. H., Exercising the Functional Structure Gives Microprocessors a Real Workout, *Electronics* 50, No. 4, 109-112 (February 17, 1977).

A new test method, Wisest, overcomes the deficiencies of older methods. In effect, the test computer builds a pattern of variables from the instruction set of the device under test and then checks the pattern for conditions defined by the user.

75. Smith, J. G., and Oldham, H. E., Laser Testing of Integrated Circuits, *IEEE J. Solid-State Circuits* SC-12, No. 3, 247-252 (June 1977).

Data may be injected directly into the internal circuitry of an integrated circuit by a finely focused laser beam, at rates over 1 MHz, using an electro-optic modulator. Large savings in time and ease of fault detection are envisioned by this test method.

76. Srini, V. P., API Tests for RAM Chips, *Computer* 10, No. 7, 32-35 (July 1977).

A test vector designed to efficiently detect adjacent-pattern-interference faults is described. Elements to the top, bottom, left, and right of the base storage element are altered to detect pattern sensitivity.

77. Srini, V. P., Fault Diagnosis of Microcomputer Systems, *Computer* 10, No. 1, 60-65 (January 1977).

A diagnostic system for a microcomputer and associated RAM chips is described. The system consists of both resident and nonresident diagnostic programs along with a diagnostic supervisor for controlling the execution of the programs.

78. Tarui, Y., Hayashi, Y., Narukami, N., and Ishii, K., Reliability Test to Improve the Fabrication Technique for MOS-LSI Memories, *Electronics and Communications in Japan* 55, No. 2, 97-104 (February 1972).

This paper describes the reliability aspects of the evaluation and improvement of the fabrication techniques for an *n*-channel MOS-LSI memory. The reliability tests included the measurement of the frequency of a ring counter constructed from the test specimens.

79. Wadsack, R. L., Fault Coverage in Digital Integrated Circuits, *Bell Syst. Tech. J.* 57, No. 5, 1475-1488 (June 1978).

This paper addresses the relation between the fault coverage and measured yield in CMOS integrated circuit chips. A type-D flip-flop, a multivibrator, and a multiplexer are analyzed.

80. Wadsack, R. L., Fault Modeling and Logic Simulation of CMOS and MOS Integrated Circuits, *Bell Syst. Tech. J.* 57, No. 5, 1449-1474 (June 1978).

The fault modeling of CMOS devices is considered since they are inherently tri-state devices, and new test techniques must be employed to test for a "stuck-open" condition. The paper describes methods for creating simulator models for tri-state circuit elements.

81. Zirphile, J., Tulloue, R., and Caillat, J., TAU 1: Un Outil pour le Test des Circuits Intégrés Logiques (TAU 1: A Tool for Testing Logic Integrated Circuits), *Revue Technique Thomson-CSF* 9, No. 1, 127-148 (March 1977).

A test program simulator is described which models the possible faults of integrated circuits. Examples are given ranging from a D-type flip-flop to a microprocessor. The program is written in FORTRAN IV.

4. BOARD AND SYSTEM TESTING

82. Agrawal, V. D., and Agrawal, P., An Automatic Test Generation System for Illiac IV Logic Boards, *IEEE Trans. Computers* C-21, No. 9, 1015-1017 (September, 1972).

Experience testing logic boards has shown that random patterns are most efficient for less than seven levels of logic, and the D-algorithm is necessary for more than seven levels. The random pattern generator employed is based on the TEST-DETECT program.

83. Alonzo, R. L., Testing RAMs for the User - Devices, Boards and Systems, *Proc. Technical Program, National Electronic Packaging and Production Conf., Session Pap*, Anaheim, California, February 26-28, 1974, and New York, New York, June 18-20, 1974, pp. 38-44 (Industrial and Scientific Management, Inc., Chicago, 1974).

Testing RAMs focused for a long time on testing devices rather than boards or systems. The reasons for the shift to board testing and two possible testing structures are explained.

84. Anon., McCook of Fluke Trendar Asks Designers to Help Out, *Electronics* 51, No. 18, 14 (August 31, 1978).

A discussion of the possibility of using the microprocessor on a board to augment the test equipment in locating defects.

85. Calebotta, S., System Design with Dynamic Memories Takes Attention to Detail, *Electronics* 51, No. 3, 109-113 (February 2, 1978).

The timing problems of designing a dynamic RAM board are reviewed from the points of view of proper timing of address, data, and control signals. Attention is given to power distribution and clock line efficiency as implemented in the board design.

86. Chang, H. Y., Smith, G. W., Jr., and Walford, R. B., LAMP: System Description, *Bell Syst. Tech. J.* 53, No. 8, 1431-1449 (October 1974).

A general description of the Logic Analyzer for Maintenance Planning (LAMP) used for logic-design verification, generation of fault-detection data, and the production of a fault dictionary. LAMP has been used in the development of electronic switching systems, integrated circuits, and communication equipment.

87. Clark, T., Trouble Shooting Microprocessor-Based Systems, *Digital Design* 8, No. 2, 56-66 (February 1978).

A step-by-step procedure for debugging software and hardware, checking memories, and solving timing problems in microprocessor systems. Consideration is given to the manufacture and field service of the final system.

88. Heavey, P. P., and Simpson, V. E., Functional and Level Fail Detection for Register Array Testing, *IBM Technical Disclosure Bulletin* 15, No. 4, 1135-1136 (September 1972).

The operation of register arrays are checked by a self-programming detector technique. Testing is performed for level and functional failures.

89. Hilsinger, H. A., Mozingo, K. D., Starnes, C. F., and Van Dine, G. A., 1A Processor: Testing and Integration, *Bell Syst. Tech. J.* 56, No. 2, 289-312 (February 1977).

This article describes the complete testing philosophy as applied to the 1A communications processor. The three levels of testing and verification considered were circuit-pack, the frame, and the system.

90. Goldblatt, R. C., How Computers Can Test Their Own Memories, *Computer Design* 15, No. 7, 69-75 (July 1976).

A semiconductor memory, after it has been installed in a computer, can be tested in only a limited way since it must store its own test program.

91. Kubert, V., and Seuffert, P., Test Fixture Selection Criteria, *Electronics Test*, Introductory Issue, 4-5 (1978).

A review of the types of probes necessary for contacting printed circuit boards for testing purposes.

92. Leatherman, J., and Burger, P., System Integration and Testing with Microprocessors-Hardware Aspects, *IEEE Trans. Industrial Electronics and Control Instrumentation* IECI-22, No. 3, 360-363 (August 1975).

Functional checks of microprocessor hardware is made by a minicomputer. The hardware system integration between the minicomputer and the microprocessor can then be made on a variety of levels.

93. Lilley, R. W., Test Program for 4-K Memory Card, JOLT Microcomputer, Contract No. NGR-36-009-017 (Department of Electrical Engineering, Ohio University, Athens, Ohio, August 1976). (NTIS Accession No. N76-30845/1ST.)

A test program is described for use with the 4096-word JOLT microcomputer incorporated in navigational equipment. The program exercises the memory by cycling through all possible combinations of bits for all words.

94. Lyman, J., Automated Circuit Testers Lead the Way Out of Continuity Maze, *Electronics* 48, No. 16, 87-95 (August 7, 1975).

A discussion of testing techniques related to printed circuit boards, cables, harnesses, and hybrid substrates.

95. Ostrego, M. A., Diagnosing Defects in Complex Digital Circuit Packs, *The Western Electric Engineer* 20, No. 4, 2-7 (October 1976).

The description of a software package for the detection of faults in complex digital circuitry by directing an operator to probe internal nodes. Multiple faults are handled one at a time.

96. Petschauer, R. J., Error Logging in Semiconductor Storage Units, U.S. Patent 3,906,200, July 5, 1974.

In a procedure for scheduling preventive maintenance in a memory system, a method is described which consists of an array of registers which store the location of errors detected from the memory. Additionally, the system may be used when the error rate of the memory exceeds a predetermined magnitude.

97. Schneider, D., Designing Logic Boards for Automatic Testing, *Electronics* 47, No. 15, 100-104 (July 25, 1974).

The emphasis is on placing test points on logic boards in such a way as to allow identification of faults during the test.

98. Scola, P., An Annotated Biblography of Tests and Diagnostics, *Honeywell Computer Journal* 6, No. 2, 105-161 (1972).

An extensive bibliography of 1300 entries dealing with test and diagnostics for computer applications is presented. It contains numerous entries from foreign sources.

99. de Souza, J. M., and Paz, P. E., Fault-Tolerant Digital Clocking System, *Electron. Lett.* 11, No. 18, 433-434 (September 4, 1975).

A fault-tolerant clock has advantages that are important in reliable structures. An example is given of a clock circuit which may be incorporated in a redundant manner for high system reliability.

100. Srini, V. P., Fault Location in a Semiconductor Random-Access Memory Unit, *IEEE Trans. Computers* C-27, No. 4, 349-358 (April 1978).

The location of faults of RAM systems, including interconnection wiring, is provided by six tests. The tests are shown to be of minimal length with respect to symmetric array organization of RAM chips.

5. TESTING STRATEGIES

101. Akers, S. B., Jr., Universal Test Sets for Logic Networks, *IEEE Trans. Computers* C-22, No. 9, 835-839 (September 1973).

This paper considers how to test a network of monotonic elements given its functional description rather than its implementation. The universal test sets described are easily generated, detect multiple faults, and can be derived for both complete and incomplete functions.

102. Aleksander, I., and Al-Bandar, Z., Adaptively Designed Test Logic for Digital Circuits, *Electron. Lett.* 13, No. 16, 466-467 (August 4, 1977).

Adaptive pattern-recognition technique is used to detect faults in a logic system. A hardware implementation of the technique is described.

103. Anon., Memory-board Tests are Fast, *Electronics* 48, No. 21, 175-176 (October 16, 1975).

The Adar DR12/20 memory board testing system that is built around a high speed RAM records the location of defective chips in a scheme called memory-board error-mapping.

104. Anon., With LSI Outdistancing Tester Makers, Chip Inside Must be Guessed At, *Electronics* 50, No. 19, 46 ff (September 15, 1977).

Manufacturers of test equipment find it difficult to obtain detailed information on LSI parts. As a consequence, emulation of the part is the only way known how to test it.

105. Barrett, W. A., Information Management System for Integrated Circuit Devices, *IEEE Trans. Engineering Management* EM-23, No. 4, 147-152 (November 1976).

Data-base management techniques have been used to provide rapid information on the test results in the development of an IC memory. Both parametric and go-no go test sequences can be maintained simultaneously.

106. Batni, R. P., and Kime, C. R., A Module-Level Testing Approach for Combinational Networks, *IEEE Trans. Computers* C-25, No. 6, 594-604 (June 1976).

A method based on a directed graph model is used to modify the hardware of a combinational network for simplified test generation. Networks with one output are considered first and the method expanded to cover multiple outputs.

107. Bennetts, R. G., and Scott, R. V., Recent Developments in the Theory and Practice of Testable Logic Design, *Computer* 9, No. 6, 47-63 (June 1976).

This article is a survey paper on the properties of "easily testable" logic networks. Guidelines are given for some practical aspects of testable logic arrays.

108. Breuer, M. A., Chang, S., and Su, S. Y. H., Identification of Multiple Stuck-Type Faults in Combinational Networks, *IEEE Trans. Computers* C-25, No. 1, 44-54 (January 1976).

This paper addresses the problems of multiple stuck-type failures in combinational networks. The use of a cause-effect equation allows the determination of multiple faults. A procedure for the elimination of a fault dictionary is described.

109. Chang, H. Y., and Heimbigner, G. W., LAMP: Controllability, Observability, and Maintenance Engineering Technique (COMET), *Bell Syst. Tech. J.* 53, No. 8, 1505-1534 (October 1974).

This article describes a new method based on graph theory. The method provides an orderly basis to locate test points in a digital system.

110. Chappell, S. G., Automatic Test Generation for Asynchronous Digital Circuits, *Bell Syst. Tech. J.* 53, No. 8, 1477-1503 (October 1974).

A description of an automatic test generation system for the detection of faults using unit- and zero-time-delay gates. Two different strategies are described. One provides for a maximum coverage of potential faults, while the other provides a method for detecting individual faults.

111. Chappell, S. G., Elmendorf, C. H., and Schmidt, L. D., LAMP: Logic-Circuit Simulators, *Bell Syst. Tech. J.* 53, No. 8, 1451-1576 (October 1974).

The description of a logic circuit simulator which can simulate fault-free logic, stuck-at faults, and shorted-gate-output faults.

In addition, a new phenomenon, called hyperactive faults, which requires an inordinate amount of simulation time, is described.

112. Chiang, A. C. L., and McCaskill, R., Two New Approaches Simplify Testing of Microprocessors, *Electronics* 49, No. 2, 100 (January 22, 1976).

A concept is proposed to subdivide the circuitry into functional modules and test each module. Then algorithmic pattern generation may be applied to enhance testing efficiency.

113. Chiang, A. C. L., Reed, I. S., and Banes, A. V., Path Sensitization, Partial Boolean Difference, and Automated Fault Diagnosis, *IEEE Trans. Computers* C-21, No. 2, 189-195 (February 1972).

This note describes a method of fault diagnosis using a new theorem on the partial Boolean difference. The algorithm is presented, along with an application, for fault diagnosis of a combinational circuit.

114. Cocke, J., Read-and-Test to Reduce Redundancy Requirements in Memories, *IBM Technical Disclosure Bulletin* 15, No. 3, 885-886 (August 1976).

A technique is presented for determining error conditions in a memory which relies on treating the memory as a binary erasure channel. After each read operation, the data are complemented, written into the same address and reread. If any corresponding bits have the same value, the location read has a storage error.

115. de Jonge, J. H., and Smulders, A. J., Moving Inversions Test Pattern is Thorough, Yet Speedy, *Computer Design* 15, No. 5, 169-173 (May 1976).

A test pattern is described which is especially useful for static MOS and bipolar memories. Dynamic memories can also use the technique in conjunction with other test methods. This method is especially useful for larger memories.

116. Dias, F. J. O., Fault Masking in Combinational Logic Circuits, *IEEE Trans. Computers* C-24, No. 5, 476-482 (May 1975).

This paper considers an algebraic technique employing fault equivalence and fault dominance to simplify the detection of multiple faults. The technique is demonstrated for a single-output network but may be extended to multiple-output circuits.

117. Dirilten, H., On the Mathematical Characterizing Faulty Four-Phase MOS Logic Arrays, *IEEE Trans. Computers* C-21, No. 3, 301-305 (March 1972).

This short note analyzes the models of a single faulty load or sampling transistor in a MOS circuit. It has application for both combinatorial or sequential circuits.

118. Dorr, R. C., Self-Checking Combinational Logic Binary Counters, *IEEE Trans. Computers* C-21, No. 12, 1426-1430 (December 1972).

This method of self-checking the states of a binary counter uses parity prediction. The method was found to be at least 98 percent effective for an n-bit counter.

119. Flaningam, D., Testing Large Dynamic Memories, *Proc. Internepcon (Microelectronics)*, October 19-21, 1976, p. 181.

The paper discussed the most useful test patterns for checking large memories, the inclusion of a refresh cycle into the test sequence, and the temperature at which the test should be performed. Some guidelines on the purchase of memory chips are also given.

120. Foster, R. C., How to Avoid Getting Burned with Burn-in, *Circuits Manufacturing* 16, No. 8, 56-61 (August 1976).

To ensure product reliability, the users of plastic encapsulated semiconductors can opt for incoming screening, burn-in, and/or testing. This article examines the pros, cons, and costs of these approaches.

121. Friedman, A. D., Diagnosis of Short-Circuit Faults in Combinational Circuits, *IEEE Trans. Computers* C-23, No. 7, 746-752 (July 1974).

This paper considers the diagnosis of shorted diodes, faults on input lines, and other nonclassical short-circuit faults. The technique employs adding constraints to a path sensitization test generation process.

122. Fujiwara, H., Nagao, T., Sasao, T., and Kinoshita, K., Easily Testable Sequential Machines with Extra Inputs, *IEEE Trans. Computers* C-24, No. 8, 821-826 (August 1975).

It is shown that a machine may be made easily testable with the addition of two extra input symbols. Also presented is a design of a checking experiment for easily testable machines.

123. Gault, J. W., Robinson, J. P., and Reddy, S. M., Multiple Fault Detection in Combinational Networks, *IEEE Trans. Computers* C-21, No. 1, 31-36 (January 1972).

The increase in the efficiency of detection of multiple faults in combinational networks by adding extra input and outputs is discussed. Sections cover an analysis of multiple faults, the bounds for the number of detection tests, and a method for the test generation.

124. Gibson, J. M., Digital Logic Design for Testability, *Circuits Manufacturing* 18, No. 6, 42-43 (June 1978).

This article is a result of lectures covering the topics of test cost, testing during the manufacturing process, logic simulation, and the methods of design for testability. Ten examples of how to improve logic testability are given.

125. Girard, E., Lusinchi, J. P., Rault, J. C., and Tulloue, R., Functional Memory Testing. A Review of Fault Detection and Location, *Revue Technique Thomson-CSF* 6, No. 1, 217-227 (March 1974).

The authors point out the peculiarities of memory testing, along with the tests necessary to locate the faults and their associated effects. The main algorithms for fault detection are briefly described, and the authors finally propose a two-stage testing strategy that utilizes several of these algorithms. An extensive bibliography on memory testing is also included.

126. Girard, E., Rault, J. C., and Tulloue, R., Outil Pour la Simulation et le Test des Circuits Intégrés à Grande Echelle, lere Partie (Test and Simulation of Large Scale Integrated Circuits, Part 1), Contract No. DGRST-73-7-1392 (Thomson-CSF, Paris, France, July, 1974). (NTIS Accession No. N76-20859.)

Various computer programs are described to show the response to a given input sequence as applied to large scale integrated logic circuits. The circuit may be synchronous or asynchronous, and simple detectable faults such as short circuits, open circuits, and stuck gates are listed. A detailed bibliography containing over 1,180 items is given.

127. Gordon, G., and Nadig, H., Hexadecimal Signatures Identify Troublespots in Microprocessor Systems, *Electronics* 50, No. 5, 89-96 (March 3, 1977).

Signature analysis is a useful diagnostic technique to trace a digital signal through a system. A new test instrument is described which can map lengthy bit streams from the unit under test into four-digit hexadecimal "signatures." These signatures can be compared with those of a known good unit to determine if the unit under test is operating properly.

128. Hayes, J. P., A NAND Model for Fault Diagnosis in Combinational Logic Networks, *IEEE Trans. Computers* C-20, No. 12, 1496-1506 (December 1971).

A network model called the normal NAND model is described for fault diagnosis in combinational logic circuits. Every network can be transformed into an equivalent normal NAND network. Furthermore, the use of this model greatly simplifies test generation.

129. Hayes, J. P., Detection of Pattern-Sensitive Faults in Random-Access Memories, *IEEE Trans. Computers* C-24, No. 2, 150-157 (February 1975).

An efficient procedure for constructing a memory checking sequence for the detection of unrestricted pattern-sensitive faults is presented. Test generation methods are described for local pattern-sensitive faults defined on both open and closed neighborhoods.

130. Hayes, J. P., On Modifying Logic Networks to Improve Their Diagnosability, *IEEE Trans. Computers* C-23, No. 1, 56-62 (January 1974).

This paper considers the use of exclusive-or elements as control logic to reduce the number of tests required by a logic network and to facilitate test generation. This approach allows the introduction of signal into the network and permits the internal signals to be observed.

131. Hayes, J. P., and Friedman, A.D., Test Point Placement to Simplify Fault Detection, *IEEE Trans. Computers* C-23, No. 7, 727-375 (July 1974).

The selection of test points to facilitate testing for fault detection in combinational logic networks is discussed. The methods

presented can produce an optimal (or near-optimal) set of tests in fanout-free networks.

132. Hill, F. J., and Huey, B., A Design Language Based Approach to Test Sequence Generation, *Computer* 10, No. 6, 28-33 (June 1977).

The Sequential Circuit Test Search System (SCIRTSS) is described. The system performs a sensitization search which finds an input vector which causes a network fault to be driven to a flip-flop or output. The propagation search causes a fault, internal to the network, to be propagated to an output.

133. Hill, F. J., and Huey, B., SCIRTSS: A Search System for Sequential Circuit Test Sequences, *IEEE Trans. Computers* C-26, No. 5, 490-502 (May 1977).

A tree search formulation of a test system for sequential circuits is given. Eight circuits of various complexity were analyzed with SCIRTSS with a fault detection sequence found for least 98 percent of the faults.

134. Landgraff, R. W., Design of Diagnosable Iterative Arrays, *IEEE Trans. Computers* C-20, No. 8, 867-877 (August 1971).

One- and two-dimensional arrays of combinational logic are considered with, at most, one faulty cell. A procedure is described to make the arrays diagnosable.

135. Levin, H., A Mathematical Model of a Parallel Tester, Memory Testing Applications Report 105, (Teradyne, Inc., Chatsworth, California, 1977).

This applications report describes the use of a mathematical model which takes into account the user's and producer's requirements, the test formulating requirements such as binning, test duration, yield, etc., and the use of a computer program to analyze the data.

136. Losq, J., Efficiency of Random Compact Testing, *IEEE Trans. Computers* C-27, No. 6, 516-525 (June 1978).

The use of random inputs to a circuit is used to elicit a statistically meaningful output sequence. The testing equipment is simple; however, complete confidence of the network perfection is not guaranteed.

137. Mei, K. C. Y., Bridging and Stuck-At Faults, *IEEE Trans. Computers* C-23, No. 7, 720-727 (July 1974).

A model is presented which is based on wired logic commonly found in emitter-coupled and diode transistor logic families. Four classes of faults are investigated and the methods used to generate tests to determine fault conditions.

138. Menon, P. R., and Chappell, S. G., Deductive Fault Simulation with Functional Blocks, *IEEE Trans. Computers* C-27, No. 8, 689-695 (August 1978).

A way of propagating faults through functions using the deductive fault logic simulation technique is presented. This system is used in the Bell Laboratory Logic Analysis for Maintenance Planning (LAMP) System.

139. Mercier, J. J., Self-Testing Comparator, *Electron. Lett.* 12, No. 19, 489-490 (September 16, 1976).

The letter describes a "self-testing comparator" for use in detecting errors in data streams.

140. Morgan, M. K. M., A New Approach to Memory Testing, *Microelectronics and Reliability* 15, No. 4, 351-353 (1976).

Various presently used programs are evaluated and a new way to look at testing the new generation of RAMs is discussed by applying n- (rather than n-squared) patterns that will test different parts of the circuit for faults.

141. Muehldorf, E. I., A Quality Measure for LSI Components, *IEEE J. Solid-State Circuits* SC-9, No. 5, 291-297 (October 1974).

The LSI quality measure can be related to component yield and is based on the stuck fault testing coverage, the physical circuit design layout, and the rate of faults occurring on elemental circuit geometries. An example of the technique is presented.

142. Nair, R., Thatte, S. M., and Abraham, J. A., Efficient Algorithms for Testing Semiconductor Random-Access Memories, *IEEE Trans. Computers* C-27, No. 6, 572-576 (June 1978).

Two algorithms are presented which test faults in logic memories. One method will detect all two-coupled faults and a restricted number of three-coupled faults.

143. Owens, J. K., Enhancing the Testability of Synchronous Sequential Machines with Emphasis on Large Scale Integrated Circuits, Ph.D. thesis, Mississippi State University, State College, Mississippi (1974). (Available from University Microfilms, Order No. 74-24217.)

A determination was made to identify the most important aspects of fault detection. A scheme is presented whereby a digital-to-analog converter and an additional output terminal are added to the basic machine. The output terminal provides a signal from the converter that completely specifies the state of the machine.

144. Robach, C., and Saucier, G., Dynamic Testing of Control Units, *IEEE Trans. Computers* C-27, No. 7, 617-623 (July 1978).

A method is presented of testing hard-wired or microprogrammed control units through the application for which the system has been designed. The location of the fault is not determined by the technique; however, special test facilities and outputs are not needed.

145. Schertz, D. R., Fault-Tolerant Computing: An Introduction, *IEEE Trans. Computers* C-23, No. 7, 649-650 (July 1974).

This article provides an introduction to some of the literature and concepts of fault-tolerant computing.

146. Schnurmann, D. H., Lindbloom, E., and Carpenter, R. G., The Weighted Random Test-Pattern Generator, *IEEE Trans. Computers* C-24, No. 7, 695-700 (July 1975).

A weighted random test-pattern generator is described which may be implemented in either hardware or software. This approach has the advantage that the test generation time is nearly independent of the number of gates or primary inputs to be tested.

147. Su, S. Y. H., and Cho, Y., A New Approach to the Fault Location of Combinational Circuits, *IEEE Trans. Computers* C-21, No. 1, 21-30 (January 1972).

A method for the location of a single fault in a combinational logic network is presented. The method uses the technique of sequential diagnostic tests rather than a fault table approach.

148. Sundberg, C. W., Erasure and Error Decoding for Semiconductor Memories, *IEEE Trans. Computers* C-27, No. 8, 696-705 (August 1978).

The properties of faults, errors, and erasures as applied to semiconductor memories are given. The technique involves increased decoder complexity to achieve high reliability.

149. Sung, C., Testable Sequential Cellular Arrays, *IEEE Trans. Computers* C-25, No. 1, 11-18 (January 1976).

Presented are some of the sufficient conditions for the detection and location of a fault in a two-dimensional cellular array.

150. Susskind, A. K., Diagnostics for Logic Networks, *IEEE Spectrum* 10, No. 10, 40-47 (October 1973).

This paper reviews four techniques for the testing of logical networks. The techniques are applicable to both sequential and combinational logic.

151. Williams, M. J. Y., and Angell, J. B., Enhancing Testability of Large-Scale Integrated Circuits via Test Points and Additional Logic, *IEEE Trans. Computers* C-22, No. 1, 46-60 (January 1973).

By adding logic to LSI chips, the internal flip-flops can be reconnected to form a shift register so their performance may be checked and their internal states examined.

152. Yau, S. S., and Yang, S., Multiple Fault Detection for Combinational Logic Circuits, *IEEE Trans. Computers* C-24, No. 3, 233-242 (March 1975).

This presents a method for generating a nearly optimum test sequence to detect all multiple stuck-at faults for a combinational network using the concept of representative functions. Two methods of producing representative functions are discussed.

6. TESTING EQUIPMENT

153. Alvarez, D., Considerations in Semiconductor Tester Selection, *Computer Design* 16, No. 12, 69-74 (December 1976).

The key issue of tester selection is cost effectiveness over the life of the tester. Evaluation criteria include versatility, reliability, and efficiency.

154. Anon., Dynamic Testing for the Price of Static, *Electronics* 49, No. 4, 30-31 (February 19, 1976).

A description of an addition to a computer-controlled static test system to permit dynamic measurements on as many as 480 test pins is described. The add-on unit is a 10-MHz digital word generator that produces digital stimuli and receives responses from a printed circuit board or other unit under test.

155. Anon., Low Cost Semiconductor Memory Exerciser Provides Speed and Flexibility, *Evaluation Engineering* 11, No. 1, 30 (January 1972).

The article describes a newly developed programmable exerciser. The equipment permits testing of the majority of existing and future semiconductor memory chips or systems.

156. Anon., With LSI Outdistancing Tester Makers, Chip Inside Must be Guessed At, *Electronics* 50, No. 19, 46 ff (September 15, 1977).

Manufacturers of test equipment find it difficult to obtain detailed information on LSI parts. As a consequence, emulation of the part is the only way known how to test it.

157. Barnes, J., and Gregory, V., Basic μP Test Tool: The Portable Debugger, *EDN* 20, No. 15, 51-56 (August 20, 1975).

A "micro-control panel" type of tester is described that may be used to test microprocessor type systems. It may be used to examine the contents of a memory or to take snapshots of the operations of the system.

158. Barroeta, J. J., Camps, S., Suárez, R. E., Cañas, M. A., and Amaya, R. A., A Fault Detection System for Digital Integrated Circuits, *IEEE Trans. Instrumentation and Measurement* IM-26, No. 3, 246-251 (September 1977).

A system is described for the detection of the most commonly occurring faults in digital ICs. Both the input and output terminals are simultaneously analyzed under quasi-optimum test patterns.

159. Bush, T. S., Local Memory for a High-Speed Digital Test System, *IEEE Trans. Instrumentation and Measurement* IM-26, No. 3, 217-220 (September 1977).

The use of either random access memory or a shift register as a memory dictates many of the characteristics of a test system. The effects of this choice on the test program efficiency, test speed, and system cost are examined.

160. Campbell, J. F., Jr., A New Real-Time Function Test Generation System for Complex LSI Testing, *IEEE Trans. Manufacturing Technology* MFT-4, No. 2, 52-55 (December 1975).

This paper discusses the features of a 10-MHz sequential pattern generator designed for a general-purpose high-speed large-scale integration test system. The system has an 80-bit word size, real-time control of input-output definition, and data masking ability.

161. Chiang, A., Ferraro, E., and Liu, B., Micro-processor Unit Chip Testing Using Low Cost Tester. (Available from Macrodata Corporation, Woodland Hills, California.)

This article delineates a low-cost tester dedicated to testing micro-processor chip units. The testing is executed on instruction by instruction basis. As a result, any faulty instruction can be isolated. A high speed pattern generator is used as the core of this tester. As an illustration, the testing scheme on the 8008 is presented.

162. Cohen, C., Test System Check Microprocessors and LSI Modules, *Electronics (Intl. Ed.)* 49, No. 14, 17E (July 8, 1976).

A modular test system which can accommodate memories as large as 65K, 18-bit words was built incorporating a micropattern generator. The system performs dynamic functional tests on both microprocessors and memories.

163. Cole, B., IC Tester Aims at Small User, *Electronics* 47, No. 11, 128 (May 30, 1974).

This note describes Fairchild's low-cost Quantifier model 901. It features self-test capability, can accommodate 24-pin packages, and can test DTL, TTL, and C-MOS families.

164. Cole, B., Testing Entire Microcomputer Board, *Electronics* 50, No. 4, 123-124 (February 17, 1977).

Described is a low-cost system from Fluke Trendar which tests microprocessor and peripheral logic at their normal speed.

165. Connelly, R. N., A Tester for MOS Integrated Circuits, *Syst. Technol.* 15, No. 15, 6-8 (August 1972).

A description of the development of an automatic machine suitable for testing individual custom-designed MOS integrated circuits with up to 40 leads. A tester which is suitable for either production or laboratory work is explained.

166. Curran, L., Meeting the MOS/LSI Challenge: A Special Report on Testers, *Electronics* 44, No. 10, 68-76 (May 10, 1971).

Testing equipment manufacturers and the MOS/LSI vendors are starting to resolve differences in testing philosophies. The consensus is that universal systems are impractical. A trend is seen to more specialized equipment for specific devices.

167. Farnsbach, W. A., Logic State Analyzers — A New Instrument for Analyzing Sequential Digital Processes, *IEEE Trans. Instrumentation and Measurement* IM-24, No. 4, 353-356 (December 1975).

Logic state analyzers may be used to monitor the sequence of program and data flow in sequential processors. The application of this technique to debugging and troubleshooting is described.

168. Fitzpatrick, J. F., Today's Three Test Environments, *Digest of Papers, Semiconductor Memory Test Symposium*, October 4, 1972, Cherry Hill, New Jersey, pp. 47-59 (1973).

This article discusses the criteria to be considered when specifying semiconductor memory test equipment. Three major topics of concern are the performance of the tester for quality assurance, evaluation engineering, and production.

169. Franson, P., Portable Tester Checks Complex Logic, *Electronics* 47, No. 14, 125-126 (July 11, 1974).

A low-cost testing unit with the capabilities of a minicomputer-controlled system is described. The unit features both programmed and pseudorandom test patterns.

170. Green, C. W., Checking Out Semiconductor Memories for Electronic Switching Systems, *Bell Laboratories Record* 55, No. 5, 131-136 (May 1977).

The findings indicate that the investment in sophisticated test equipment is essential to characterizing communications circuits and to assure reliable system operation.

171. Hemmer, N., Prüefeinrichtungen des Systems Computest (COMPUTEST System), *Siemens-Zeitschrift* 48, No. 9, 608-610 (September 1974).

This article describes the COMPUTEST computer system for testing integrated circuits and memory devices. Additionally, the system may be used to test moving media and magnetic storage sytems. (In German with English abstract.)

172. King, G., Selecting a Tester to Meet 4K RAM Incoming Inspection Needs, *Electronic Packaging and Production* 16, No. 8, T7-T13 (August 1976).

A review of three types of memory testers: The functional exerciser, the dedicated tester and the computer-controlled systems. Consideration is given to the testing of 16K RAMs.

173. Kubinec, J. J., Build a Programmable Word Generator, *Electronic Design* 17, No. 2, 62-67 (January 18, 1969).

Details are presented for the construction of a programmable 100-bit word generator. Addresses are programmed into the generator by means of switches and then read into memory at a 1-MHz bit rate.

174. Laliotis, T. A., and Brumett, T. D., A Microprocessor-Controlled DIC Test System, *Computer* 8, No. 10, 60-67 (October 1975).

This paper describes the benefits of a microprocessor-based digital integrated circuit test system, the Quantifier 901.

175. Legnard, E., Moore, M., and Tomko, J., Pattern Generating System, *IBM Technical Disclosure Bulletin* 14, No. 2, 482-484 (July 1971).

A pattern generator is described which provides outputs of write, read, and data at speeds of up to 10 MHz.

176. Marshall, M., Logic Scopes Speeds Diagnosis of Faults in Digital Circuits, *Electronics* 47, No. 20, 119 (October 3, 1974).

As digital systems become more complex, errors such as glitches and ringing on interconnection lines becomes more prevalent. Digital oscilloscopes have the ability to display events that could cause system failure.

177. Malkiel, C., ATE Workshop Reports from the ATE Seminar Exhibit - Make or Buy ATE? *Circuits Manufacturing* 18, No. 4, 61-66 (April 1978).

Four panelists at a workshop discussed the liabilities and benefits of building or buying automatic test equipment.

178. Neese, J. W., Microprocessor System Validation and Failure Isolation with Portable Tester, *Computer Design* 16, No. 11, 105-111 (September 1977).

The system described is a diagnostic tester for a microprocessor system. With the unit, memory test can be run that will determine and print out the location of the faulty IC.

179. Perlmutter, D., Handle Complex Testing with Word Generators, *Electronic Products* 17, No. 12, 51 ff (May 26, 1975).

The use of word generators to produce data in both serial and parallel forms is explored. For example, in serial form, the data may be used to test communication networks, and in parallel form they may be used to verify the operation of semiconductor memory stacks.

180. Pulyer, R. C., and Swaney, C. B., Dynamically Controlling the Testing of Stored Information in a Monolithic Memory, *IBM Technical Disclosure Bulletin* 14, No. 10, 2888-2891 (March 1972).

The article describes a computer-controlled testing system which will conventionally apply the addresses of the storage locations to the memory and will sense the resulting output. In addition, the computer can be used to determine characteristics of ROMs.

181. Runyon, S., Focus on IC Testers, *Electronic Design* 24, No. 9, 48-55 (April 26, 1976).

A review of the testers on the market, with a general summary of the characteristics of each.

182. Santoni, A., Needed for Logic Testing: A New Breed of Instruments, *Electronics* 48, No. 19, 88-93 (September 18, 1975).

A review article of small-scale instruments for logic and fault analysis. This includes such items as logic probes, pulsers, state analyzers, and oscilloscopes.

183. Santoni, A., Testers Are Getting Better at Finding Microprocessor Flaws, *Electronics* 50, No. 26, 57-66 (December 23, 1976).

Instruments for the examination of microprocessor busses are the logic analyzers and the microprocessor analyzers. This article provides information on the commercial types of these devices available and their capabilities.

184. Shoemaker, W. E., and Wilson, D. W., Digital Testing Oscilloscope Cushions Against Mounting Costs of Troubleshooting, *Electronics* 51, No. 6, 105-112 (March 16, 1978).

The Biomation DTO-1 test instrument is described. It combines the capabilities of a go/no-go comparison tester, a time-domain logic analyzer, and a storage oscilloscope.

185. Showers, J. L., Dynamic Analysis of MNOS Memories, Master's thesis, Air Force Institute of Technology, Wright-Patterson Air Force Base, Ohio School of Engineering (1974). (NTIS Accession No. AD-785126.)

The study determines and demonstrates the feasibility of using the Macrodata MD-104 test system for the analysis of MNOS memory devices. A personality board was designed for the National Cash Register 1105 EROM and the unit was tested in both dc and ac modes.

186. Vodovoz, E., Testing Microprocessors is a Gamble, *Electronic Products* 17, No. 11, 27-29, 146-147 (November 1975).

A review of the test equipment available to test microprocessor memories and the functions of the arithmetic logic unit.

187. Anon., Fast Pulse Test Fixtures, (E-H Research Laboratories, Inc., Oakland, California, 1969).

A manual concerned with the design and construction of test fixtures for use with the E-H 4000 series dynamic test systems. There are sections on measurement concepts, constructional techniques, and sources of measurement error.

188. Dreher, T., Fast Pulse Techniques (E-H Research Laboratories, Inc., Oakland, California, 1968).

This manual is concerned with the use of fast pulses for testing in the time domain. It covers the theoretical basis of pulse testing, time-domain instrumentation, and applications of pulse testing.

189. Hubbs, J. C., The New Pulse: A Glossary of Proposed Standard Pulse Definitions, (E-H Research Laboratories, Inc., Oakland, California, 1966).

The definitions of pulse parameters are based upon the measurement of the peak amplitude of the pulse. These definitions are based upon the geometry of the individual static pulse and are frequency and application independent.

190. Marshall, M., and Nyder, R., Which Method Should be Used to Measure Fast Pulses? *Electronics* 47, No. 2, 94-97 (January 24, 1974).

This article discusses the three most popular types of oscilloscopes that engineers use to capture and analyze fast pulses. Sampling oscilloscopes are best for high speeds, single-shot oscilloscopes are used at low repetition rates, and real-time oscilloscopes are the least expensive.

191. Wolfe, G., Scaling the Mountains of Data, *Circuits Manufacturing* 16, No. 4, 48 ff (April 1976).

Graphical plots present an attractive way to display the results of IC test computer output. This is very economical and efficient with the use of a graphic display terminal.

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☐ Document describes a computer program; SF-185, FIPS Software Summary, is attached.

16. ABSTRACT *(A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.)*

This annotated bibliography covers articles published in the field of semiconductor device testing. The bibliography contains (1) entries divided into six economics of testing, (2) monolithic circuit testing, (3) the testing of subsystems of large scale integrated circuits such as microcomputer boards and memory arrays, (4) various test strategies used to locate a defective LSI circuit, (5) test equipment available for LSI testing, and (6) various measurement methods that may be of interest to the test engineer.

17. KEY WORDS *(six to twelve entries; alphabetical order; capitalize only the first letter of the first key word unless a proper name; separated by semicolons)*

Electronics; integrated circuit; large scale integration; memory; microprocessor; testing.

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