Large Scale Integration Digital Testing—Annotated Bibliography, 1969-1978
Large Scale Integration

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LARGE SCALE INTEGRATION DIGITAL TESTING —
ANNOTATED BIBLIOGRAPHY, 1969 - 1978

T. F. Leedy

This annotated bibliography covers articles published in the field of semiconductor device testing. The bibliography contains (1) entries divided into six economics of testing, (2) monolithic circuit testing, (3) the testing of subsystems of large scale integrated circuits such as microcomputer boards and memory arrays, (4) various test strategies used to locate a defective LSI circuit, (5) test equipment available for LSI testing, and (6) various measurement methods that may be of interest to the test engineer.

Key Words: Electronics; integrated circuit; large scale integration; memory; microprocessor; testing.

1. INTRODUCTION

The testing of digital semiconductor devices, especially complex integrated circuits, is a difficult task that must be performed to assure their proper electrical operation. Over the past decade, small- and medium-scale integrated circuits have had a profound influence on electronic circuit design. This trend is likely to be overshadowed by large scale integrated (LSI) circuits in the next decade. The two main production considerations of LSI circuits are efficient processing and cost-effective testing. This bibliography is primarily concerned with the engineering methods and equipment for testing these complex devices and their associated systems. This bibliography does not purport to be an exhaustive search of the literature. Rather, it is a listing of references that cover the many diverse techniques to assure proper performance of LSI devices and systems. As such, this bibliography may serve as an introduction to the literature of LSI testing for those not familiar with the techniques. In general, papers dealing with the reliability and failure analysis of semiconductor devices have not been included although device testing is an integral part of this discipline.

The bibliography is divided into six sections. The first section deals with the necessity for testing LSI devices and systems and the resultant economic benefit for both the vendor and consumer. The next section considers those test methods that may be applied to monolithic LSI circuits where the level of diagnosis and repair is the IC itself. The third section contains references to logic boards and to small systems that contain LSI parts. The testing techniques at this level are different from those for testing monolithic units since the interconnections between LSICs may be faulty and the defective parts must be identified in order for the system to be repaired. In the next section are found references to articles on the strategies employed in either the design or testing of LSI circuits and systems. The fifth section covers various
aspects of testing equipment that is commercially produced or designed for specialized applications. The last section is concerned with the measurements of the electrical signals in LSI testing.

Sources for the bibliography were personal files, literature citations in papers collected, and manufacturer's technical notes. Additionally, computer searches of the *Electronics and Computer Abstracts* of INSPEC from 1969 to 1977, the NTIS Abstracts from 1964 to 1977, and the COMPENDEX from 1970 to 1977 were made.
2. NEED AND ECONOMICS OF TESTING


Several factors affect the ability of a microprocessor to be tested. Unique failure modes, the inability to gain access to internal logic, and high test speeds make testing devices difficult. Thus, extra testing at the board level is also needed.


This note describes the need for test methods for the automotive, computer, instrument, and telecommunications markets.


The claim is made that the specifications on which the military rely are outmoded and call for too many screening and test steps.


A transcript of a discussion among eight persons on the various aspects of testing philosophies, available test equipment, and the management issues that are associated with semiconductor testing.


A cost analysis of testing is important prior to the purchase of test equipment. Such an analysis must include the cost of both testing incoming components and the cost of not testing them.


The testing of printed circuit board assemblies is necessary for an electronic equipment manufacturer to be cost effective.

This is an analysis of how much it will cost to test an LSI chip on a cost-per-unit basis.


This article alerts the user to the crucial need to test LSI, explains why this is not a trivial task, and outlines how it may be done.


This report, in six sections, considers IC testing from the viewpoint of the manufacturer, aerospace and industrial users, and the test equipment manufacturer.


This article is a review of the test equipment available along with an economic analysis of testing both components and boards.


The premium paid for high reliability is more important for discretes than for integrated circuits. The study is based on the data from approximately 190,000 high-reliability semiconductor devices over an 18-month period.


This paper considers the use of MOS, MNOS, CCD, and bipolar technologies as alternatives to moving-surface memories. Other device technologies and circuit designs are also examined.


This paper describes the economic justification for in-house microprocessor testing, presents a description of a tester developed by a user, and concludes with observations regarding the cost savings which have been realized.


This paper reviews the several aspects of system organization and the resulting performance tradeoffs. It is followed by a review of reliability considerations including the use of error-correcting techniques.


Increased device and testing complexity along with high test system cost provides a bad situation which will probably get worse in the future.


The system designer can calculate what component burn-in will save in overall cost. Several authorities testify that burn-in is both an economical and effective way to reduce field failures.

17. Melgaard, H., Reducing Burn-In Operating Costs, *Circuits Manufacturing* 18, No. 6, 36-37 (June 1978).

The author states that a semiconductor burn-in oven may be operated more economically by taking measures to reduce wasted heat and by using higher temperature for shorter times.


A new concept for the testing of large scale integration is described that requires no user software and lends itself to a com-
pletely modular approach for total system integration. The new concept consists of interdisciplinary areas such as software requirements, dynamic accuracies of testing, LSI product types, and function and parametric speeds related to various product lines.


This article provides an overview of what services are performed by the independent test laboratories. Additionally, it gives the advantages and disadvantages of using an independent test laboratory.


A general review of the problems that plague the testing of large scale integration from various points of view is presented.


The necessity of correctly defining logic levels, pulse shapes, and timing intervals is stressed.


System builders often find that the cost advantage of their custom-designed memories is much reduced after consideration is given to testing.


This article focuses on problems encountered and techniques employed in testing both digital and linear ICs.

Macrowdata, a manufacturer of test equipment, is now performing IC tests for others. This is not only profitable, but also allows the building of a library of test programs.


A three-year program at the Jet Propulsion Laboratory to find LSI devices for unmanned space applications pinpoints faults in specifications, performance and testing.
3. INTEGRATED CIRCUIT TESTING


The testing of microprocessors requires the use of different test equipment than used for integrated circuits and logic boards. Often, the task of microprocessor testing is more difficult, and the test equipment more expensive; there are some techniques that enable cost-effective testing for low-volume users of microprocessors.


The microcomputer family is defined as consisting of microprocessor units and random-access memories. Equipment necessary to test these components is described along with a new testing approach called modular sensorialization.


The Fairchild CCD450 9216-bit CCD memory was dynamically tested using a commercial tester and an interface designed by the author. Comparisons were made of the performance of the memory to that specified by the manufacturer.


It is often impractical to perform exhaustive tests on IC memories for all possible combinations of inputs. This report states that savings in time can be achieved by isolating the possible fault modes of the device and then establishing a test sequence designed to detect those particular faults.

The testing of output characteristics of bipolar digital integrated circuits is described using a commercial tester. Both functional and parametric tests are considered for various devices including multiple output types and those with open collector and high voltage outputs.


The use of automatic test pattern generation is applied to testing large scale integrated logic circuits. An algorithm is presented that can be applied to test both combinational and sequential logic circuits.


This report investigated the parametric and functional tests of high usage memories which are required for military specifications. Special attention was given to the application of functional tests to determine if a memory suffers from pattern sensitivity.


Detailed here are test programs that allow characterization of address access time with respect to device power supply, thereby permitting effective screening and aiding in evaluation of vendor specifications.


This article describes the various philosophies used to test microprocessors such as testing its various component parts and the testing of the whole chip by execution of a worse-case program. A description of commercial testing equipment is also presented.

MOS LSI circuits possess many of the reliability problems associated with discrete semiconductors and MSI circuits. Their complexity requires that different methods are used to assure their reliability. Specific areas considered are pattern sensitivity, manufacturing controls, assembly, packaging, and electrical testing.


A review of the various burn-in tests for the detection of infant-mortality type failures. Also covered are the various physical configurations of high-temperature testing equipment available for both static and exercised operation of devices. Following this article is a list of vendors of testing equipment and services.


Several test patterns that can be effective tools in the search for the ideal pattern are proposed.


Consideration should be given to at least ten requirements for 4K RAM systems to assure reliable system operation. The article also suggests procurement strategies for the purchase of RAM devices.


A memory organization is considered for which a large number of faults can be tolerated at a low cost in redundancy. The primary element in the system is an LSI chip that realizes a section of the memory. The chips are connected via a switching network so that the memory can be reconfigured effectively in the presence of chip failures.

The uses of IC burn-in are discussed as an important test technique to assure reliable devices. Burn-in will increase in importance as devices become more complex.


Research on the design, testing, and application of random access computer storage devices is cited in this bibliography of worldwide journal literature. This bibliography was prepared by searching the 1974 to 1976 data base of Engineering Index. It contains 178 abstracts.


Designers should modify traditional component testing concepts and restructure their thinking to treat the CPU as a system rather than an assembly of components. The point is made that testing a CPU is at best a trial-and-error procedure. More effective and efficient means of testing a CPU must developed.


Four methods are discussed which may be used to test microprocessor systems. These are the self-diagnostic type of test, the comparison approach, using algorithmic pattern generation, and the stored response type of testing.


Designers should do their own characterization of LSI devices to assure performance in each application. Examples are given on characterizing a NAND gate and comparing two different RAM types.

The test generation technique described uses a known good microprocessor and the Sentry 600 to develop the truth table from a user's diagnostic written in the microprocessor's own machine code or assembly language. The generation program can be composed without having to know the internal architecture of the microprocessor.


Various test patterns for random access memories are described and their applications are discussed. Analysis techniques for random access memory characterization are presented.


This article is a discussion of methods to modify microprocessor software to avoid having to remask ROMs if errors are detected.


A preliminary study on various contemporary LSI testing techniques was conducted. The techniques were categorized into logic type (combinatorial and sequential) and the type of electrical testing (functional and parametric). Electrical parameters specified on each type of LSI device were listed and the parameters specified by each manufacturer were tabulated. A study was also made of available LSI test equipment.


Specific guidelines are developed for high-reliability testing at the wafers and package levels. Functional and parametric testing
is discussed and recommendations are made for MOS and bipolar devices. Specifications for an LSI test system are outlined.


A procedure for testing memories employing a computer-controlled tester is presented. The instrumentation used in the automated performance tests and in fault diagnosis of the memory devices is discussed. (In Russian.)


The article begins with a review of faults in a digital network. It describes two programs, TESTCC and TESTSC, for testing combinational and sequential networks, respectively. Networks with a maximum of 1000 gates can be processed.


Guidelines are provided that designers can follow to assure proper timing in a semiconductor memory system. Careful timing is essential to avoid bit errors.


To qualify LSI products made with new processes, engineers have developed a test chip to facilitate accelerated stress testing of particular devices. The final product is then stressed and the failure modes compared with the failure modes and the device performed within the expected reliability objectives.


This study was performed to document the common failure modes of LSI devices and to find methods of electrical stress testing of
these components. A wide variety of device technologies were evaluated in the study.


Test procedures are developed from an understanding of the fabrication technology used in their construction. The associated design weaknesses are reviewed, and test programs for the detection of pattern sensitivity are presented.


This article describes a testing system and philosophy for testing 8080 microprocessors. The basic test philosophy is to execute "random" instructions on "random" data. This approach is feasible because the execution of each instruction is largely independent of previous instructions.


The strategy of a minicomputer manufacturer to provide a reliable product is discussed. Consideration is given to both the testing and management of a quality control program.


This first of a two-part review discusses many electronic components and their failure rates. Emphasis is placed on the failure of integrated circuits of all types.


This second of a two-part review gives information on how original equipment manufacturers and component vendors test electronic components, especially integrated circuits.

A testing approach used by a manufacturer of communications equipment to assure a reliable system is described. Epoxy-encapsulated TTL and ceramic MOS LSI devices were used in the study.


A bipolar memory device used in the UNIVAC 9700 computer is discussed from the viewpoint of both system reliability and design as well as the philosophy of its incoming testing.


The use of computer-aided testing system for memories is presented with emphasis on the peculiarities of MOS memories and the saving of testing time. (In German.)


A review of many approaches to testing LSI devices is presented. Additionally, methods are described to obtain the radiation response of CMOS RAMs to ionizing radiation.


A discussion of parametric tests which, in tandem with more common methods, can push minimum IC acceptability standards close to 99.99 percent level.


The importance of testing ICs at the speeds at which they are intended to operate is stressed. The basic concept of propagation
time and its measurement is essential to understanding the speed limitation of ICs.


This gate stressing technique essentially results from sequencing the clock signals in a multiphase circuit in reverse order. Stressing by this method helps guarantee that devices with mobile ion contamination and/or gate breakdown will be found.


The problems of assembling the right testing equipment and utilizing the proper techniques and test sequences for diagnostic testing are discussed. An example is given to illustrate the difficulty of identifying trouble areas of an MOS memory.


The specific requirements of a memory test system and the hardware necessary to support the system are discussed. An example of a memory disturb problem is explained in detail.


The compendium of Microcircuit Reliability data is separated into two parts. The General LSI Technology Summaries presents descriptions of the fabrication processes of LSI technologies. The Detailed Data Sections is arranged with each section devoted to a particular memory/LSI device function. Each section contains a detailed breakdown of part level life and environmental and screening tests arranged by part manufacturer and part number.

71. Schneider, B., Problemer Ved Test AF Komplekse IC. En Gennemgang AF en Del Specielle Problemer Ved Test AF MSI Og LSI Kredse Som F. Eks. RAM, ROM, Og CPU (Testing Problems of Complex Integrated Circuits. A Consideration of Special Testing Problems of MSI and
LSI Circuits Also of Random Access Memories, Read Only Memories and Central Processor Units), Report No. ECR-52 (Elektronikcentralen, Hoersholm, Denmark, May 1975).

A review of the problems associated with the purchase of automatic test equipment. Included are some special measurement problems and limitations of equipment to meet various measurement challenges. (In Danish with English summary.)


This paper describes the LEAD (Learn, Execute, and Diagnose) strategy of microprocessor testing. In this system, the microprocessor executes its own instructions and relies on the tester only for memory and peripherals.


This article is a review of various types of microprocessor test equipment from small to large systems. In addition, the types of testers used by the manufacturers of ICs are presented.


A new test method, Wisest, overcomes the deficiencies of older methods. In effect, the test computer builds a pattern of variables from the instruction set of the device under test and then checks the pattern for conditions defined by the user.


Data may be injected directly into the internal circuitry of an integrated circuit by a finely focused laser beam, at rates over 1 MHz, using an electro-optic modulator. Large savings in time and ease of fault detection are envisioned by this test method.

A test vector designed to efficiently detect adjacent-pattern-interference faults is described. Elements to the top, bottom, left, and right of the base storage element are altered to detect pattern sensitivity.


A diagnostic system for a microcomputer and associated RAM chips is described. The system consists of both resident and nonresident diagnostic programs along with a diagnostic supervisor for controlling the execution of the programs.

78. Tarui, Y., Hayashi, Y., Narukami, N., and Ishii, K., Reliability Test to Improve the Fabrication Technique for MOS-LSI Memories, Electronics and Communications in Japan 55, No. 2, 97-104 (February 1972).

This paper describes the reliability aspects of the evaluation and improvement of the fabrication techniques for an n-channel MOS-LSI memory. The reliability tests included the measurement of the frequency of a ring counter constructed from the test specimens.


This paper addresses the relation between the fault coverage and measured yield in CMOS integrated circuit chips. A type-D flip-flop, a multivibrator, and a multiplexer are analyzed.


The fault modeling of CMOS devices is considered since they are inherently tri-state devices, and new test techniques must be employed to test for a "stuck-open" condition. The paper describes methods for creating simulator models for tri-state circuit elements.

A test program simulator is described which models the possible faults of integrated circuits. Examples are given ranging from a D-type flip-flop to a microprocessor. The program is written in FORTRAN IV.
4. BOARD AND SYSTEM TESTING


Experience testing logic boards has shown that random patterns are most efficient for less than seven levels of logic, and the D-algorithm is necessary for more than seven levels. The random pattern generator employed is based on the TEST-DETECT program.


Testing RAMs focused for a long time on testing devices rather than boards or systems. The reasons for the shift to board testing and two possible testing structures are explained.


A discussion of the possibility of using the microprocessor on a board to augment the test equipment in locating defects.


The timing problems of designing a dynamic RAM board are reviewed from the points of view of proper timing of address, data, and control signals. Attention is given to power distribution and clock line efficiency as implemented in the board design.


A general description of the Logic Analyzer for Maintenance Planning (LAMP) used for logic-design verification, generation of fault-detection data, and the production of a fault dictionary. LAMP has been used in the development of electronic switching systems, integrated circuits, and communication equipment.

A step-by-step procedure for debugging software and hardware, checking memories, and solving timing problems in microprocessor systems. Consideration is given to the manufacture and field service of the final system.


The operation of register arrays are checked by a self-programming detector technique. Testing is performed for level and functional failures.


This article describes the complete testing philosophy as applied to the 1A communications processor. The three levels of testing and verification considered were circuit-pack, the frame, and the system.


A semiconductor memory, after it has been installed in a computer, can be tested in only a limited way since it must store its own test program.


A review of the types of probes necessary for contacting printed circuit boards for testing purposes.


Functional checks of microprocessor hardware is made by a minicomputer. The hardware system integration between the minicomputer and the microprocessor can then be made on a variety of levels.
93. Lilley, R. W., Test Program for 4-K Memory Card, JOLT Microcomputer, Contract No. NGR-36-009-017 (Department of Electrical Engineering, Ohio University, Athens, Ohio, August 1976). (NTIS Accession No. N76-30845/1ST.)

A test program is described for use with the 4096-word JOLT microcomputer incorporated in navigational equipment. The program exercises the memory by cycling through all possible combinations of bits for all words.


A discussion of testing techniques related to printed circuit boards, cables, harnesses, and hybrid substrates.


The description of a software package for the detection of faults in complex digital circuitry by directing an operator to probe internal nodes. Multiple faults are handled one at a time.


In a procedure for scheduling preventive maintenance in a memory system, a method is described which consists of an array of registers which store the location of errors detected from the memory. Additionally, the system may be used when the error rate of the memory exceeds a predetermined magnitude.


The emphasis is on placing test points on logic boards in such a way as to allow identification of faults during the test.


An extensive bibliography of 1300 entries dealing with test and diagnostics for computer applications is presented. It contains numerous entries from foreign sources.

A fault-tolerant clock has advantages that are important in reliable structures. An example is given of a clock circuit which may be incorporated in a redundant manner for high system reliability.


The location of faults of RAM systems, including interconnection wiring, is provided by six tests. The tests are shown to be of minimal length with respect to symmetric array organization of RAM chips.
5. TESTING STRATEGIES


This paper considers how to test a network of monotonic elements given its functional description rather than its implementation. The universal test sets described are easily generated, detect multiple faults, and can be derived for both complete and incomplete functions.


Adaptive pattern-recognition technique is used to detect faults in a logic system. A hardware implementation of the technique is described.


The Adar DR12/20 memory board testing system that is built around a high speed RAM records the location of defective chips in a scheme called memory-board error-mapping.

104. Anon., With LSI Outdistancing Tester Makers, Chip Inside Must be Guessed At, Electronics 50, No. 19, 46 ff (September 15, 1977).

Manufacturers of test equipment find it difficult to obtain detailed information on LSI parts. As a consequence, emulation of the part is the only way known how to test it.


Data-base management techniques have been used to provide rapid information on the test results in the development of an IC memory. Both parametric and go-no go test sequences can be maintained simultaneously.

A method based on a directed graph model is used to modify the hardware of a combinational network for simplified test generation. Networks with one output are considered first and the method expanded to cover multiple outputs.


This article is a survey paper on the properties of "easily testable" logic networks. Guidelines are given for some practical aspects of testable logic arrays.


This paper addresses the problems of multiple stuck-type failures in combinational networks. The use of a cause-effect equation allows the determination of multiple faults. A procedure for the elimination of a fault dictionary is described.


This article describes a new method based on graph theory. The method provides an orderly basis to locate test points in a digital system.


A description of an automatic test generation system for the detection of faults using unit- and zero-time-delay gates. Two different strategies are described. One provides for a maximum coverage of potential faults, while the other provides a method for detecting individual faults.


The description of a logic circuit simulator which can simulate fault-free logic, stuck-at faults, and shorted-gate-output faults.
In addition, a new phenomenon, called hyperactive faults, which requires an inordinate amount of simulation time, is described.


A concept is proposed to subdivide the circuitry into functional modules and test each module. Then algorithmic pattern generation may be applied to enhance testing efficiency.


This note describes a method of fault diagnosis using a new theorem on the partial Boolean difference. The algorithm is presented, along with an application, for fault diagnosis of a combinational circuit.


A technique is presented for determining error conditions in a memory which relies on treating the memory as a binary erasure channel. After each read operation, the data are complemented, written into the same address and reread. If any corresponding bits have the same value, the location read has a storage error.


A test pattern is described which is especially useful for static MOS and bipolar memories. Dynamic memories can also use the technique in conjunction with other test methods. This method is especially useful for larger memories.


This paper considers an algebraic technique employing fault equivalence and fault dominance to simplify the detection of multiple faults. The technique is demonstrated for a single-output network but may be extended to multiple-output circuits.

This short note analyzes the models of a single faulty load or sampling transistor in a MOS circuit. It has application for both combinatorial or sequential circuits.


This method of self-checking the states of a binary counter uses parity prediction. The method was found to be at least 98 percent effective for an n-bit counter.


The paper discussed the most useful test patterns for checking large memories, the inclusion of a refresh cycle into the test sequence, and the temperature at which the test should be performed. Some guidelines on the purchase of memory chips are also given.

120. Foster, R. C., How to Avoid Getting Burned with Burn-in, Circuits Manufacturing 16, No. 8, 56-61 (August 1976).

To ensure product reliability, the users of plastic encapsulated semiconductors can opt for incoming screening, burn-in, and/or testing. This article examines the pros, cons, and costs of these approaches.


This paper considers the diagnosis of shorted diodes, faults on input lines, and other nonclassical short-circuit faults. The technique employs adding constraints to a path sensitization test generation process.

It is shown that a machine may be made easily testable with the addition of two extra input symbols. Also presented is a design of a checking experiment for easily testable machines.


The increase in the efficiency of detection of multiple faults in combinational networks by adding extra input and outputs is discussed. Sections cover an analysis of multiple faults, the bounds for the number of detection tests, and a method for the test generation.


This article is a result of lectures covering the topics of test cost, testing during the manufacturing process, logic simulation, and the methods of design for testability. Ten examples of how to improve logic testability are given.


The authors point out the peculiarities of memory testing, along with the tests necessary to locate the faults and their associated effects. The main algorithms for fault detection are briefly described, and the authors finally propose a two-stage testing strategy that utilizes several of these algorithms. An extensive bibliography on memory testing is also included.


Various computer programs are described to show the response to a given input sequence as applied to large scale integrated logic circuits. The circuit may be synchronous or asynchronous, and simple detectable faults such as short circuits, open circuits, and stuck gates are listed. A detailed bibliography containing over 1,180 items is given.

Signature analysis is a useful diagnostic technique to trace a digital signal through a system. A new test instrument is described which can map lengthy bit streams from the unit under test into four-digit hexadecimal "signatures." These signatures can be compared with those of a known good unit to determine if the unit under test is operating properly.


A network model called the normal NAND model is described for fault diagnosis in combinational logic circuits. Every network can be transformed into an equivalent normal NAND network. Furthermore, the use of this model greatly simplifies test generation.


An efficient procedure for constructing a memory checking sequence for the detection of unrestricted pattern-sensitive faults is presented. Test generation methods are described for local pattern-sensitive faults defined on both open and closed neighborhoods.


This paper considers the use of exclusive-or elements as control logic to reduce the number of tests required by a logic network and to facilitate test generation. This approach allows the introduction of signal into the network and permits the internal signals to be observed.


The selection of test points to facilitate testing for fault detection in combinational logic networks is discussed. The methods
presented can produce an optimal (or near-optimal) set of tests in fanout-free networks.


The Sequential Circuit Test Search System (SCIRTSS) is described. The system performs a sensitization search which finds an input vector which causes a network fault to be driven to a flip-flop or output. The propagation search causes a fault, internal to the network, to be propagated to an output.


A tree search formulation of a test system for sequential circuits is given. Eight circuits of various complexity were analyzed with SCIRTSS with a fault detection sequence found for least 98 percent of the faults.


One- and two-dimensional arrays of combinational logic are considered with, at most, one faulty cell. A procedure is described to make the arrays diagnosable.


This applications report describes the use of a mathematical model which takes into account the user's and producer's requirements, the test formulating requirements such as binning, test duration, yield, etc., and the use of a computer program to analyze the data.


The use of random inputs to a circuit is used to elicit a statistically meaningful output sequence. The testing equipment is simple; however, complete confidence of the network perfection is not guaranteed.

A model is presented which is based on wired logic commonly found in emitter-coupled and diode transistor logic families. Four classes of faults are investigated and the methods used to generate tests to determine fault conditions.


A way of propagating faults through functions using the deductive fault logic simulation technique is presented. This system is used in the Bell Laboratory Logic Analysis for Maintenance Planning (LAMP) System.


The letter describes a "self-testing comparator" for use in detecting errors in data streams.


Various presently used programs are evaluated and a new way to look at testing the new generation of RAMs is discussed by applying $n$- (rather than $n$-squared) patterns that will test different parts of the circuit for faults.


The LSI quality measure can be related to component yield and is based on the stuck fault testing coverage, the physical circuit design layout, and the rate of faults occurring on elemental circuit geometries. An example of the technique is presented.


Two algorithms are presented which test faults in logic memories. One method will detect all two-coupled faults and a restricted number of three-coupled faults.

A determination was made to identify the most important aspects of fault detection. A scheme is presented whereby a digital-to-analog converter and an additional output terminal are added to the basic machine. The output terminal provides a signal from the converter that completely specifies the state of the machine.


A method is presented of testing hard-wired or microprogrammed control units through the application for which the system has been designed. The location of the fault is not determined by the technique; however, special test facilities and outputs are not needed.


This article provides an introduction to some of the literature and concepts of fault-tolerant computing.


A weighted random test-pattern generator is described which may be implemented in either hardware or software. This approach has the advantage that the test generation time is nearly independent of the number of gates or primary inputs to be tested.


A method for the location of a single fault in a combinational logic network is presented. The method uses the technique of sequential diagnostic tests rather than a fault table approach.

The properties of faults, errors, and erasures as applied to semiconductor memories are given. The technique involves increased decoder complexity to achieve high reliability.


Presented are some of the sufficient conditions for the detection and location of a fault in a two-dimensional cellular array.


This paper reviews four techniques for the testing of logical networks. The techniques are applicable to both sequential and combinational logic.


By adding logic to LSI chips, the internal flip-flops can be re-connected to form a shift register so their performance may be checked and their internal states examined.


This presents a method for generating a nearly optimum test sequence to detect all multiple stuck-at faults for a combinational network using the concept of representative functions. Two methods of producing representative functions are discussed.
6. TESTING EQUIPMENT


The key issue of tester selection is cost effectiveness over the life of the tester. Evaluation criteria include versatility, reliability, and efficiency.


A description of an addition to a computer-controlled static test system to permit dynamic measurements on as many as 480 test pins is described. The add-on unit is a 10-MHz digital word generator that produces digital stimuli and receives responses from a printed circuit board or other unit under test.


The article describes a newly developed programmable exerciser. The equipment permits testing of the majority of existing and future semiconductor memory chips or systems.

156. Anon., With LSI Outdistancing Tester Makers, Chip Inside Must be Guessed At, *Electronics* 50, No. 19, 46 ff (September 15, 1977).

Manufacturers of test equipment find it difficult to obtain detailed information on LSI parts. As a consequence, emulation of the part is the only way known how to test it.


A "micro-control panel" type of tester is described that may be used to test microprocessor type systems. It may be used to examine the contents of a memory or to take snapshots of the operations of the system.

A system is described for the detection of the most commonly occurring faults in digital ICs. Both the input and output terminals are simultaneously analyzed under quasi-optimum test patterns.


The use of either random access memory or a shift register as a memory dictates many of the characteristics of a test system. The effects of this choice on the test program efficiency, test speed, and system cost are examined.


This paper discusses the features of a 10-MHz sequential pattern generator designed for a general-purpose high-speed large-scale integration test system. The system has an 80-bit word size, real-time control of input-output definition, and data masking ability.


This article delineates a low-cost tester dedicated to testing micro-processor chip units. The testing is executed on instruction by instruction basis. As a result, any faulty instruction can be isolated. A high speed pattern generator is used as the core of this tester. As an illustration, the testing scheme on the 8008 is presented.


A modular test system which can accommodate memories as large as 65K, 18-bit words was built incorporating a micropattern generator. The system performs dynamic functional tests on both microprocessors and memories.

This note describes Fairchild's low-cost Quantifier model 901. It features self-test capability, can accommodate 24-pin packages, and can test DTL, TTL, and C-MOS families.


Described is a low-cost system from Fluke Trendar which tests microprocessor and peripheral logic at their normal speed.


A description of the development of an automatic machine suitable for testing individual custom-designed MOS integrated circuits with up to 40 leads. A tester which is suitable for either production or laboratory work is explained.


Testing equipment manufacturers and the MOS/LSI vendors are starting to resolve differences in testing philosophies. The consensus is that universal systems are impractical. A trend is seen to more specialized equipment for specific devices.


Logic state analyzers may be used to monitor the sequence of program and data flow in sequential processors. The application of this technique to debugging and troubleshooting is described.


This article discusses the criteria to be considered when specifying semiconductor memory test equipment. Three major topics of concern are the performance of the tester for quality assurance, evaluation engineering, and production.

A low-cost testing unit with the capabilities of a minicomputer-controlled system is described. The unit features both programmed and pseudorandom test patterns.


The findings indicate that the investment in sophisticated test equipment is essential to characterizing communications circuits and to assure reliable system operation.


This article describes the COMPUTEST computer system for testing integrated circuits and memory devices. Additionally, the system may be used to test moving media and magnetic storage systems. (In German with English abstract.)


A review of three types of memory testers: The functional exerciser, the dedicated tester and the computer-controlled systems. Consideration is given to the testing of 16K RAMs.


Details are presented for the construction of a programmable 100-bit word generator. Addresses are programmed into the generator by means of switches and then read into memory at a 1-MHz bit rate.


This paper describes the benefits of a microprocessor-based digital integrated circuit test system, the Quantifier 901.

A pattern generator is described which provides outputs of write, read, and data at speeds of up to 10 MHz.


As digital systems become more complex, errors such as glitches and ringing on interconnection lines becomes more prevalent. Digital oscilloscopes have the ability to display events that could cause system failure.


Four panelists at a workshop discussed the liabilities and benefits of building or buying automatic test equipment.


The system described is a diagnostic tester for a microprocessor system. With the unit, memory test can be run that will determine and print out the location of the faulty IC.


The use of word generators to produce data in both serial and parallel forms is explored. For example, in serial form, the data may be used to test communication networks, and in parallel form they may be used to verify the operation of semiconductor memory stacks.


The article describes a computer-controlled testing system which will conventionally apply the addresses of the storage locations to the memory and will sense the resulting output. In addition, the computer can be used to determine characteristics of ROMs.

A review of the testers on the market, with a general summary of the characteristics of each.


A review article of small-scale instruments for logic and fault analysis. This includes such items as logic probes, pulser, state analyzers, and oscilloscopes.


Instruments for the examination of microprocessor busses are the logic analyzers and the microprocessor analyzers. This article provides information on the commercial types of these devices available and their capabilities.


The Biomation DTO-1 test instrument is described. It combines the capabilities of a go/no-go comparison tester, a time-domain logic analyzer, and a storage oscilloscope.


The study determines and demonstrates the feasibility of using the Macrodata MD-104 test system for the analysis of MNOS memory devices. A personality board was designed for the National Cash Register 1105 EROM and the unit was tested in both dc and ac modes.


A review of the test equipment available to test microprocessor memories and the functions of the arithmetic logic unit.
7. MEASUREMENT METHODS


A manual concerned with the design and construction of test fixtures for use with the E-H 4000 series dynamic test systems. There are sections on measurement concepts, constructional techniques, and sources of measurement error.


This manual is concerned with the use of fast pulses for testing in the time domain. It covers the theoretical basis of pulse testing, time-domain instrumentation, and applications of pulse testing.


The definitions of pulse parameters are based upon the measurement of the peak amplitude of the pulse. These definitions are based upon the geometry of the individual static pulse and are frequency and application independent.


This article discusses the three most popular types of oscilloscopes that engineers use to capture and analyze fast pulses. Sampling oscilloscopes are best for high speeds, single-shot oscilloscopes are used at low repetition rates, and real-time oscilloscopes are the least expensive.


Graphical plots present an attractive way to display the results of IC test computer output. This is very economical and efficient with the use of a graphic display terminal.
This annotated bibliography covers articles published in the field of semiconductor device testing. The bibliography contains (1) entries divided into six economics of testing, (2) monolithic circuit testing, (3) the testing of subsystems of large scale integrated circuits such as microcomputer boards and memory arrays, (4) various test strategies used to locate a defective LSI circuit, (5) test equipment available for LSI testing, and (6) various measurement methods that may be of interest to the test engineer.

**Key Words:** Electronics; integrated circuit; large scale integration; memory; microprocessor; testing.

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**ABSTRACT:**
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**Subject Keywords:**
- Electronics
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