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Reference Flat Pulse Generator

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J. R. Andrews
B. A. Bell
E. E. Baldwin

Electromagnetic Fields Division
National Engineering Laboratory
National Bureau of Standards
Boulder, Colorado 80303



U.S. DEPARTMENT OF COMMERCE, Malcolm Baldrige, Secretary

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Reference Flat Pulse Generator

J. R. Andrews,* B. A. Bell,** and E. E. Baldwin†

National Bureau of Standards
Boulder, Colorado 80303

A reference step-like pulse generator is described which has been developed at NBS. This generator can be used for accurately characterizing the step response of various kinds of transient recording equipment (oscilloscopes, waveform recorders, transient digitizers, etc.).^{††} Basic design principles are given as well as complete circuit diagrams and descriptions. An analysis of the output stage of the generator is presented together with the circuit models for developing a time-domain computer simulation program using extended-SCEPTRE. Preliminary specifications indicate that the NBS Reference Flat Pulse Generator provides a negative-going reference transition duration (90 to 10 percent) of 600 ps, ± 20 percent with baseline perturbations of less than ± 2 percent for less than 5 ns.

Key words: available waveform; baseline; circuit analysis; flat pulse generator; modeling; pulse delay; step response; topline; transfer standard; transition duration.

1. Introduction

1.1 Background

The need for a reference step-like waveform generator has become increasingly important for accurately characterizing the step response of oscilloscopes, transient recorders, and fast sampling channels of digital measurement instruments and automatic test equipment (ATE). The measurement system response can be subtracted from the reference waveform to give the measurement system distortion explicitly as a function of time (dynamic performance error). Equivalently, the reference waveform can be deconvolved from the response of the measurement system (to the reference waveform) in order to obtain the system impulse response. Here and in the remainder of this technical note a nominal load impedance of 50Ω has been assumed. When the load impedance is not 50Ω , additional analysis is required (see, for example, ref. 1). By comparing the measurement waveforms and/or data with that of a reference waveform, the fidelity with which the measurement system can acquire the waveform can be determined. The dynamic performance of a measurement system is often desired, together with its ability to measure dc or steady-state quantities.

For example, it is well known that skin effect losses in shielded conductors and coaxial cables cause their step response to approach a final dc level asymptotically [2,3]. Since all physically realizable measuring devices require connectors, cables, wires, etc., transmission line effects on fast input signals are bound to occur. Hence, any measurement system will cause a certain amount of distortion to an applied signal which causes the acquired waveform to differ.

From a practical point of view, it is often desirable to be able to calibrate the dc voltage levels of the measurement system, as well as any time-dependent parameters. For this reason a voltage

* Presently with Picosecond Pulse Labs, Inc., P.O. Box 44, Boulder, Colorado.

**Electrosystems Division, National Engineering Laboratory.

† Formerly with the Electromagnetic Technology Division, National Engineering Laboratory.

†† Certain commercial equipment, instruments, or materials are identified in this paper in order to adequately specify the experimental procedure. Such identification does not imply recommendation or endorsement by the National Bureau of Standards, nor does it imply that the materials or equipment identified are necessarily the best available for the purpose.

step function, whose beginning and ending dc levels are calibratable, has considerable merit as a reference standard, particularly if the transition between these two levels is also well-behaved and predictable. Such was the purpose for developing a Reference Flat Pulse Generator (RFPG) in the Electromagnetic Waveform Metrology Group at NBS [4].

1.2 Objectives

The main objective of developing an RFPG was to design, build, and model a pulse generator standard which can provide a step-like pulse waveform of known amplitude and flatness, together with a predictable transition duration between levels. Such a standard can then be used for the alignment and calibration of pulse waveform measuring instrumentation.

As shown in figure 1-1, the step response of, say, an oscilloscope typically contains three regions of interest in specifying its dynamic accuracy. The first one is the transition region in which the important parameter is the transition duration, t_r (often referred to as rise time), which is the time required for the response to pass from the proximal (or 10 percent) level to the distal (or 90 percent) level [5]. It is oftentimes difficult to ascertain the 10 and 90 percent levels of input waveforms with sloping baselines and topline. The calibratable beginning and ending levels (topline and baseline, respectively) of the RFPG avoids this difficulty.

The second region of interest is the perturbation region immediately following the transition. Ideally, the step response should smoothly and monotonically rise to the final dc (100 percent) level and remain there. In practice, there are usually some small bumps, wiggles, overshoot, ringing, etc. This region is usually described by the peak-to-peak amplitude, V_p , of the ringing (as a percentage of the full-scale step), and the time interval, t_p , required for the perturbations to disappear.

The third region of interest typically lasts over a relatively long settling time, t_s , wherein the response converges to (and stays within) a specified accuracy of the final dc value. Depending on charge storage and nonlinear saturation effects in the measurement and display circuits, and on the closeness to the final dc level, this parameter can be difficult to determine [6]. As shown in figure 1-1, t_p and t_s are both usually measured starting at the mesial (or 50 percent) level of the step response.

1.3 Report Organization

This report is divided into six sections and four appendices. Following this introductory section, sections 2 and 3 describe the design techniques, circuit details, and preliminary specifications of the RFPG. Section 4 contains the circuit modeling, selected program listings, and computer-simulated waveforms for analyzing the subject generator using SCEPTRE [7]. Appendix A contains the list of parts used in the RFPG module. Appendix B provides the alignment procedure for making adjustments to the generator as a source for calibration purposes. Appendix C describes time constant measurements taken on rf switching transistors. Appendix D gives an analysis for approximating equivalent capacitors.

2. Basic Design Techniques

2.1 Prior Methods

To date, there has not been available a flat pulse generation method which allows accurate determination (on a stable dc basis) of both the baseline and topline levels and well-characterized transition and perturbation regions (see fig. 1-1). Manufacturers in the past have built step generators

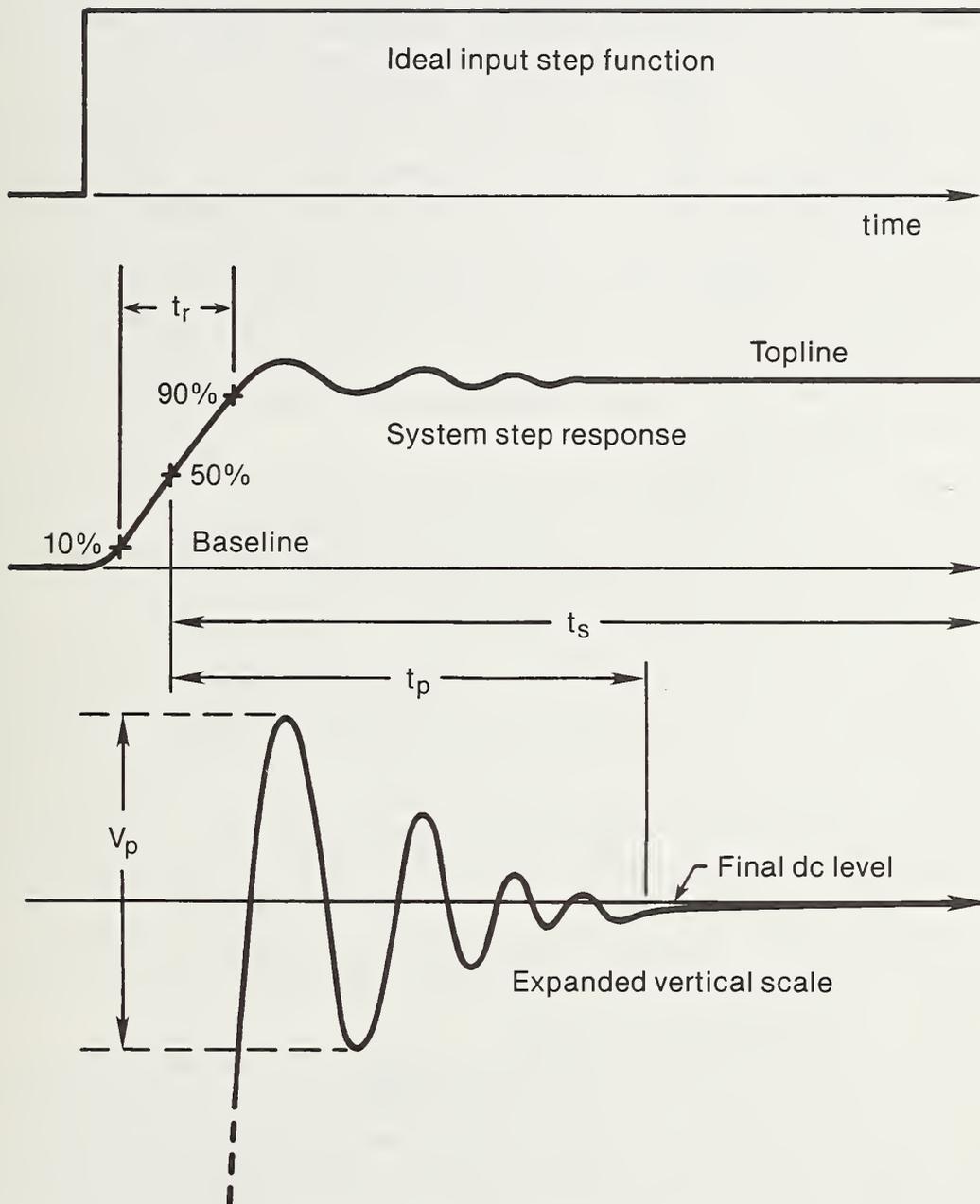


Figure 1-1. Anatomy of a step-like pulse.

with varying success. In the subnanosecond region, tunnel diodes [8] or mercury wetted mechanical switches [9] have typically been used. Tunnel diodes provide the fastest switching times, with 20 ps being typical. Such diodes provide low-level pulses of the order of 1/4 V. Their major limitation is the long-term sag in their output voltage due to internal heating of the junction. Thus, they cannot be used for accurate calibration transfer from dc.

High voltage (tens to hundreds of volts) pulses can be generated using mercury switches. Transition durations as short as 39 ps have been obtained [10]. Disadvantages of mercury switches are: low repetition rates, typically line frequency (60 Hz), limited life times, and pulse amplitude instabilities of the order of a percent. Another more subtle problem stems from the use of transmission lines in the pulse generator design. A typical mercury switch pulse generator, figure 2-1, consists of a dc power supply, a charging resistor R_C , a coaxial cable of impedance R_0 with electrical delay length T_D and the switch [$T_D = 2\ell / (V_p \cdot C)$ where ℓ is the cable length in meters, V_p is the propagation factor in percent, and C is the speed of light in meters per second]. The cable is initially charged to the voltage V_{bb} . When the switch is closed the line is discharged into the load resistor R_L . Ideally, if $R_L = R_0$ then a rectangular output pulse will be produced [11]. The amplitude would be $1/2 V_{bb}$ and the duration would be $2T_D$. This concept should produce an ideal pulse amplitude standard related precisely to a dc measurement of V_{bb} . In practice, there are problems. First, R_0 is usually not well known, closer than perhaps one percent. Second, owing to skin effect and dielectric losses, real cables introduce significant pulse distortion which alters the waveshape from the ideal rectangular pulse and reduces the amplitude.

Earlier work at NBS addressed the problems of sag and distortion [10]. One of the common design defects with conventional pulse generators is the varying load on the generator's power supplies as the output pulse changes state. Depending on the dynamic regulation of the power supply, aberration in the form of sag may appear in the generated topline and/or baseline.

One technique used by Andrews [10,12] to obtain a flat pulse consisted of a simple diode switch (fig. 2-2). Initially, the switch S_1 (in reality a PNP transistor operated in saturation or cutoff) is open. The constant current I_0 passes through the diode and R_1 , producing the generator baseline voltage $-I_0 R_1$. When the switch S_1 is closed, the diode becomes reverse biased, thus disconnecting I_0 from R_1 . The output voltage thus changes rapidly to its topline value of zero volts. The pulse generator system has a source resistance equal to R_1 . A constant current I_0 is always drawn from the independent power supply $-V$. Thus, the topline and baseline determining elements are completely free from power supply dynamic regulation problems. The only uncertainty in this circuit is in the transition region due to the switching transients of S_1 and the charge storage time in the diode. By using a Schottky diode, the charge storage time may be minimized. With this circuit very flat pulses were obtained 20 ns after the positive-going transition.

To extend the flat pulse concept to the subnanosecond region, the mercury wetted switch was attractive [11]. Figure 2-3 shows such a flat pulse generator. Again, the power supply (+V) provides a constant current I_0 , regardless of the switch condition (open or closed). With the switch open, the baseline is zero volts. When the switch closes, the generator topline is $I_0 R_1$. The equivalent generator source resistance is R_1 . Unfortunately, the disadvantages of the mercury switches, as mentioned earlier, limited this approach.

Both of the above flat pulse generators also avoided the use of coaxial cables and their attendant distortion problems. Instead, the principle of design is the use of constant current sources steered to and away from the output load terminal via high-speed switching. The use of this technique

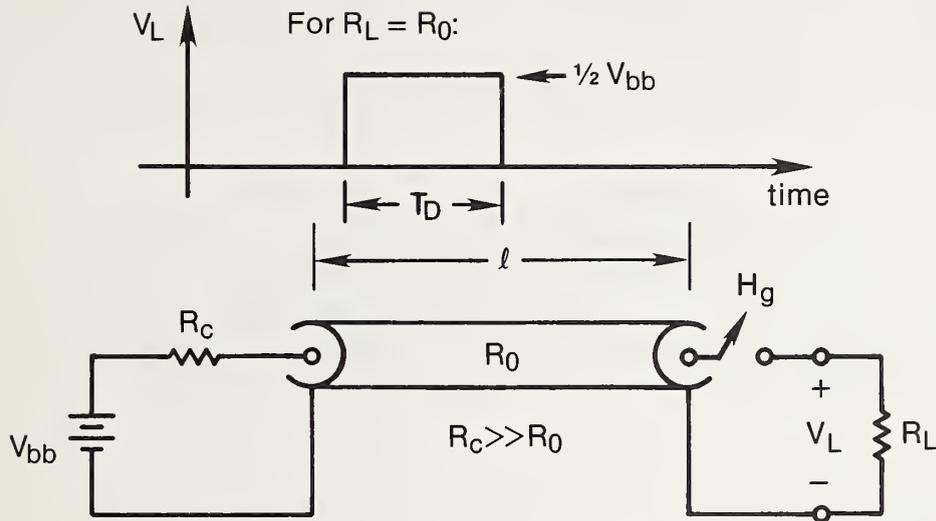


Figure 2-1. Typical mercury switch pulse generator.

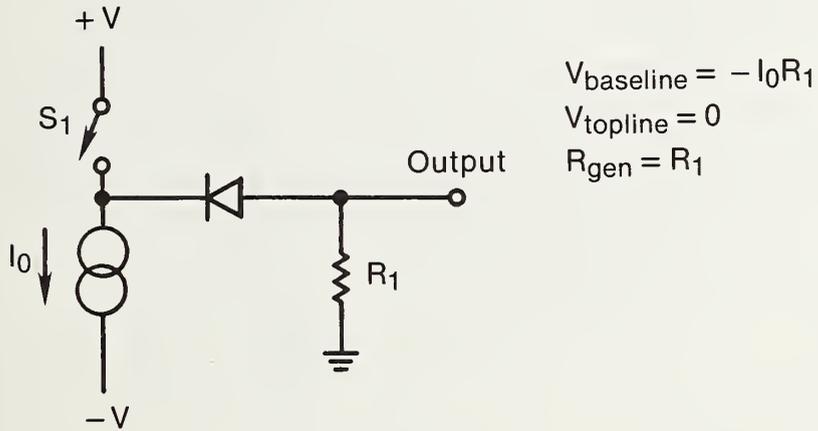


Figure 2-2. Diode switch flat pulse generator.

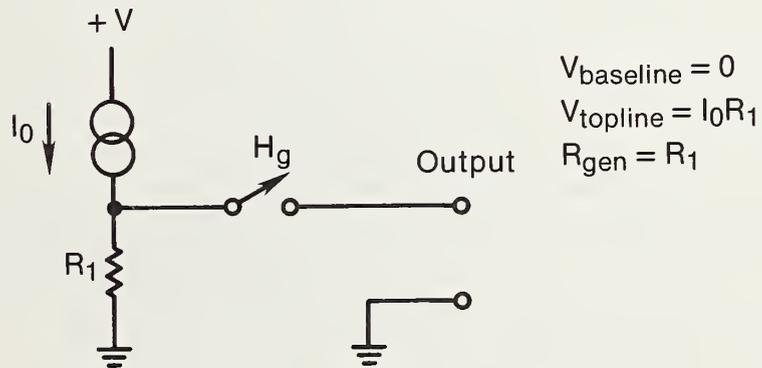


Figure 2-3. Mercury switch flat pulse generator.

was recognized and implemented by Andrews in 1970 [12]. Figure 2-4 shows the basic design of the generator consisting of a constant current source I_1 feeding the R_1 resistor having a typical value of 50.0Ω . The I_2 current source is turned off by means of the control gate so that a stable topline on the voltage output pulse is formed by I_1 through R_1 . When the control pulse turns on current source I_2 such that

$$I_1 = I_2 = I_0,$$

then the current flow to R_1 is zero, so that the baseline voltage is (ideally) zero. By using the turn-off of an active device (I_2), the transition in the output waveform is limited by the inherent device switching speed and output capacitance. Flat-top pulses having a transition duration (10 percent to 90 percent) of about 2 ns with around 5 percent to 10 percent aberrations were obtained by this method.

2.2 Present Approach

The present design approach used in the RFPG is shown in figure 2-5. The technique is very similar to the earlier concepts, particularly the one shown in figure 2-4. Two major improvements are provided, however, by the present approach with (1) inclusion of the output diode, and (2) control of the negative current source by means of switches S1 and S2. The switching at $t = t_0$ causes rapid turn off of the output diode by steering I_0 down through switch S2. A stable baseline voltage of essentially zero volts is produced equal to the leakage current of the diode through R_1 in parallel with R_L (typically, $-100 \text{ nA} \cdot 25 \Omega = -2.5 \mu\text{V}$). With switch S1 closed and S2 open, the upper positive constant current source is steered through the output diode providing a constant, and therefore calibratable, topline voltage of I_0 through R_1 in parallel with R_L (typically, $+20 \text{ mA} \cdot 25 \Omega = +500 \text{ mV}$). The rapid transition from the topline to the baseline (less than 1 ns in the present RFPG), is caused by both the use of fast, rf-switching transistors for S1 and S2 and the sudden reverse bias seen by the output diode. For best results, the diode is a passivated, Schottky barrier type having low turn-on voltage and fast, charge-storage recovery time. Thus, this basic approach produces a fast step-like waveform generator having two known output levels with a constant output impedance R_1 .

The actual electronic circuit used to implement this approach is shown symbolically in figure 2-6. Q8 functions as the dc current source I_{dc} . Q1 and Q2 are the switches S1 and S2. Q1 and Q2 form an emitter-coupled differential-switch pair. They are driven in push-pull by the complementary outputs of an ECL logic OR gate U13. Q3 is the current source for the emitters of Q1 and Q2. I_e must be greater than I_{dc} . Initially, the base of Q1 is an ECL "1" (-0.9 V) and the base of Q2 is an ECL "0" (-1.7 V). Thus, Q2 is off and Q1 is on, conducting all the emitter current I_e to ground. The current I_{dc} from Q8 all passes through CR3 to R_g creating an open circuit output of 1.00 V ($20 \text{ mA} \times 50 \Omega$). CR3 is conducting while CR2 is reverse biased and nonconducting. At $t = t_0$ U13 receives a pulse. The complementary outputs from U13 rapidly switch Q1 off and Q2 on. Q2 now conducts all of the 30 mA emitter current I_e . Thus, the collector of Q2 tries to pull 30 mA from the node connecting CR3, CR2, and Q8. The only way for the nodal currents to balance is for Q8 to supply 20 mA , CR3 to become nonconducting, and CR2 to turn on and supply 10 mA . Thus, the desired function of turning off CR3 and disconnecting I_{dc} from the output is accomplished.

In actual practice, only the negative-going transition from 500 mV to $-2.5 \mu\text{V}$ is considered as the reference step transition. It is far easier to control the transient behavior of CR3 turning off than when it is turning back on. Figure 2-7 is a pair of photos taken of the main output pulse from the RFPG.

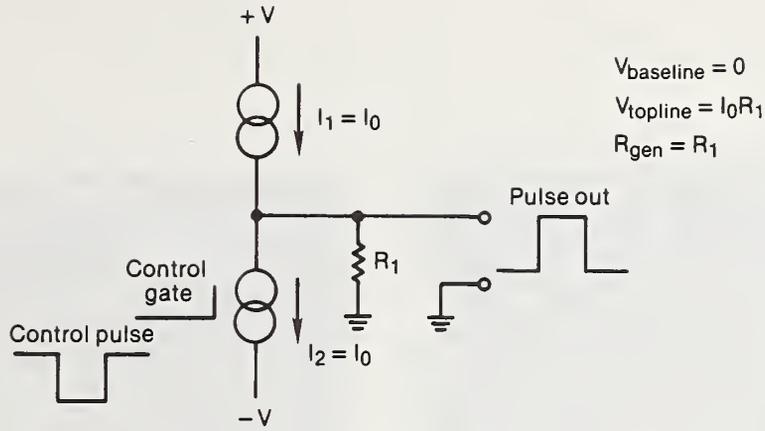


Figure 2-4. Stable reference flat top pulse generator.

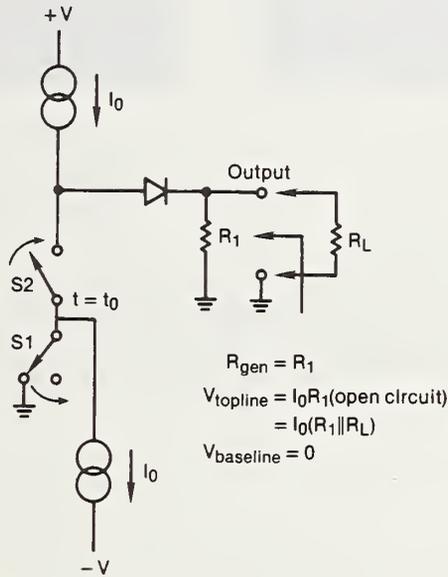


Figure 2-5. Present RFPG switching technique.

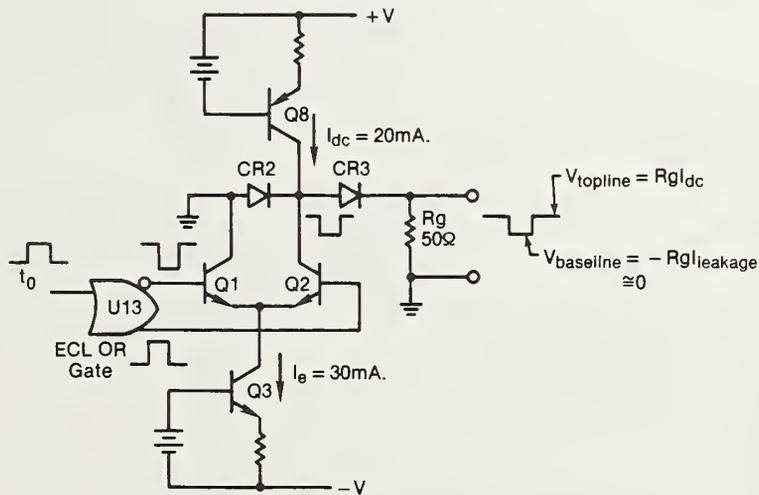
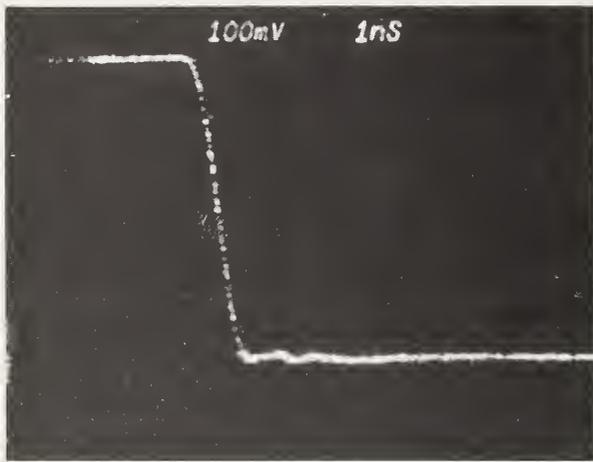
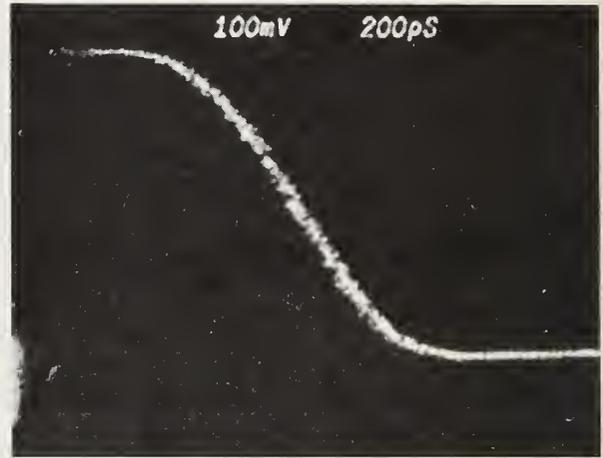


Figure 2-6. Output stage of the RFPG.



(a)



(b)

Figure 2-7. Photos of the main PULSE output from the prototype RFG.
 (a) 100 mV/cm--vertical sensitivity; 1 ns/cm--horizontal time base.
 (b) Same vertical sensitivity with expanded 200 ps/cm time base.

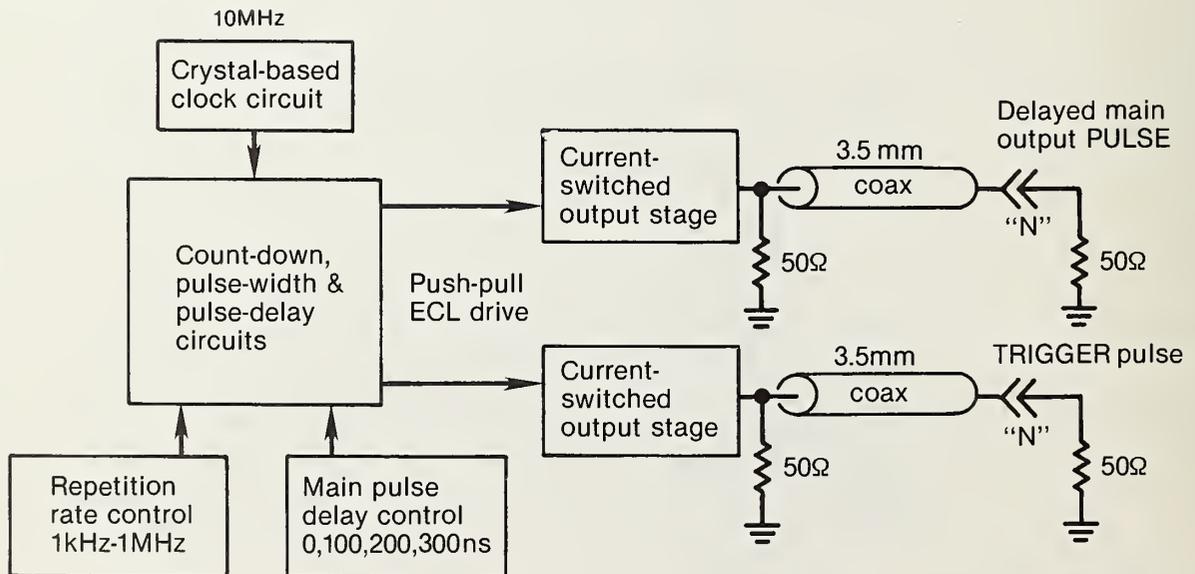


Figure 2-8. Block diagram of complete RFG.

A block diagram showing the complete RFPG is given in figure 2-8. The current-switched output stage, of course, is critical in producing the reference step-like output waveform, and has been briefly described above. The output pulse across the 50 Ω generator source resistor is coupled to the front panel N type connectors via nominal 50 Ω , 3.5 mm rigid coaxial lines. A trigger output pulse is also provided from an identical output stage. It has the same specifications as the delayed main output pulse, except for a 50 percent duty cycle (10 percent duty cycle for the main pulse). A 10 MHz crystal-based clock circuit is counted down to provide for selectable pulse repetition rates with appropriate pulse-durations and selectable pulse delays for the main output pulse. The rep. rates, delays, and duty cycles are all determined by digitally counting the 10 MHz (100 ns) clock pulses. These circuits are implemented in emitter-coupled logic (ECL) to provide fast transition edges with minimum jitter, particularly between the push-pull ECL drive to the current-switched output stages. Figure 2-9 above shows the front panel of the NBS Reference Flat Pulse Generator.

2.3 Preliminary Specifications

Specifications are common to the pulse output and the trigger output unless noted otherwise.

Baseline: 0.00 V \pm 10 μ V

Topline: 1.00 V open circuit, \pm 0.1 percent

Source impedance: 50.0 Ω , \pm 0.5 percent

Reference transition: negative-going

Reference transition duration: 600 ps (90 percent to 10 percent), \pm 20 percent

Perturbations: Less than \pm 2 percent lasting for 5 ns or less

Second transition duration: 2 ns (10 percent to 90 percent), \pm 20 percent

Trigger to pulse delay: Selectable 0 ns, 100 ns, 200 ns, or 300 ns, \pm 1/2 ns

Jitter: 25 ps or less

Repetition rate: Selectable 1 MHz, 100 kHz, 10 kHz, or 1 kHz, \pm 0.01 percent

Duty cycle: 10 percent for pulse

50 percent for trigger

Internal working standards: 10 MHz crystal oscillator for time base

LM399H active zener for dc voltage

Selected 50 Ω , SMA, microwave termination

Connectors: Type N female

Controls: Mode 0V, dc (1 V O.C.), or pulse

Construction: TEK TM500 single-wide plug-in kit

Power requirements: Supplied by TM500 main frame

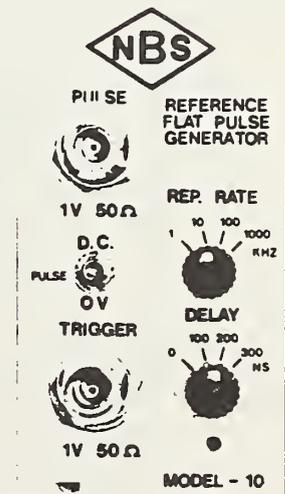


Figure 2-9. Front panel of the NBS Reference Flat Pulse Generator.

3. Circuit Diagrams and Description

3.1 Clock, Delay, and Pulse Duration Circuits

Figure 3-1 is the circuit diagram for the clock, delay, and duration circuits. Figures 3-2 through 3-5 are the timing diagrams. The internal time standard for the generator is a 10 MHz crystal oscillator U1. The first section U1a provides a dc reference voltage to bias the second section U1b as a linear amplifier. The second section is a modified form of Colpitts crystal oscillator. The third section U1c provides squaring and buffering.

The 10 MHz clock is used to toggle a chain of 95H90 divided by 10 ICs, U2-U5. These counters provide the basic repetition rates of the generator. S1a is used to select either 1 MHz, 100 kHz, 10 kHz, or 1 kHz. The output from S1a is labeled RESET. All the remaining logic functions are initiated by the negative going transition of the RESET square wave.

RESET and $\overline{\text{CLK}}$ are applied to the NOR gate U6a. When RESET goes to a "0", U6a then passes the 10 MHz $\overline{\text{CLK}}$ pulses creating the GATED CLK signal. The first GATED CLK pulse toggles a "1" into the Trigger D flip-flop U7a. The $\overline{\text{Q}}$ output is the $\overline{\text{TRIG}}$ signal.

The pulse delay function is obtained by successively dividing the GATED CLK pulses using divide by 2 flip-flops U7b and U8. The appropriate positive transition for 0 ns, 100 ns, 200 ns, or 300 ns delay is selected via S2 and used to toggle a "1" into U9a, a D flip-flop. The Q output is the DELAYED PULSE. The R-C networks (R1, C6, and C7; R2 and C8; and R3, C9, and C10) are adjustable delay networks used to compensate for the propagation delays in the various delay ICs.

The specifications call for a 10 percent duty cycle for the pulse output. Thus, the duration of the DELAYED PULSE is to be 100 ns, 1 μs , 10 μs , or 100 μs , depending upon the repetition rate selected. This duration is accomplished by counting the appropriate number of 10 MHz clock pulses and then clearing (pin 1) flip-flop U9a. When $\overline{\text{DELAYED PULSE}}$ goes to a "0", gate U6c then passes the GATED CLK pulses to a chain of divide by 10 dividers, U10 to U12. The output of the appropriate divider is selected by S1b and used to toggle a "1" into flip-flop U9b. The Q output from U9b clears U9a and also U7b and U8 through the OR gate U6b. U7a and U9b are cleared by the positive transition of the RESET square wave. Incidentally, this action causes the duty cycle of the trigger pulse to be 50 percent. RESET is also passed through U6b to ensure that U7b and U8 are reset properly at initial power-on.

The $\overline{\text{TRIG}}$ and DELAYED PULSE signals are passed through separate buffers U13 and U14 to provide complementary, push-pull ECL drive to the trigger and pulse output stages. The operating states of these buffers are controlled by the MODE switch S3.

3.2 Current-Switching Output Stages

Figure 3-6 is the schematic diagram of the output stages. These stages are identical; therefore, we will only discuss the trigger output stage. Section 2.2 described in detail the operation of this particular circuit using the symbolic diagram in figure 2-6.

U15 is the internal dc voltage working standard. It is a temperature-controlled, active zener voltage reference. U16, Q7, and Q8 function as the 20 mA dc current source. A dc voltage differential of 2 V between the +12 V bus and the (+) input to U16 is set by potentiometer R17. U16 forces the potential across R20 to also be 2 V, thus establishing the emitter current of Q8 to be 20 mA. Due to the high β (300 x 200) of the Darlington pair, Q7 and Q8, the composite collector current is almost identically the same as the 20 mA emitter current.

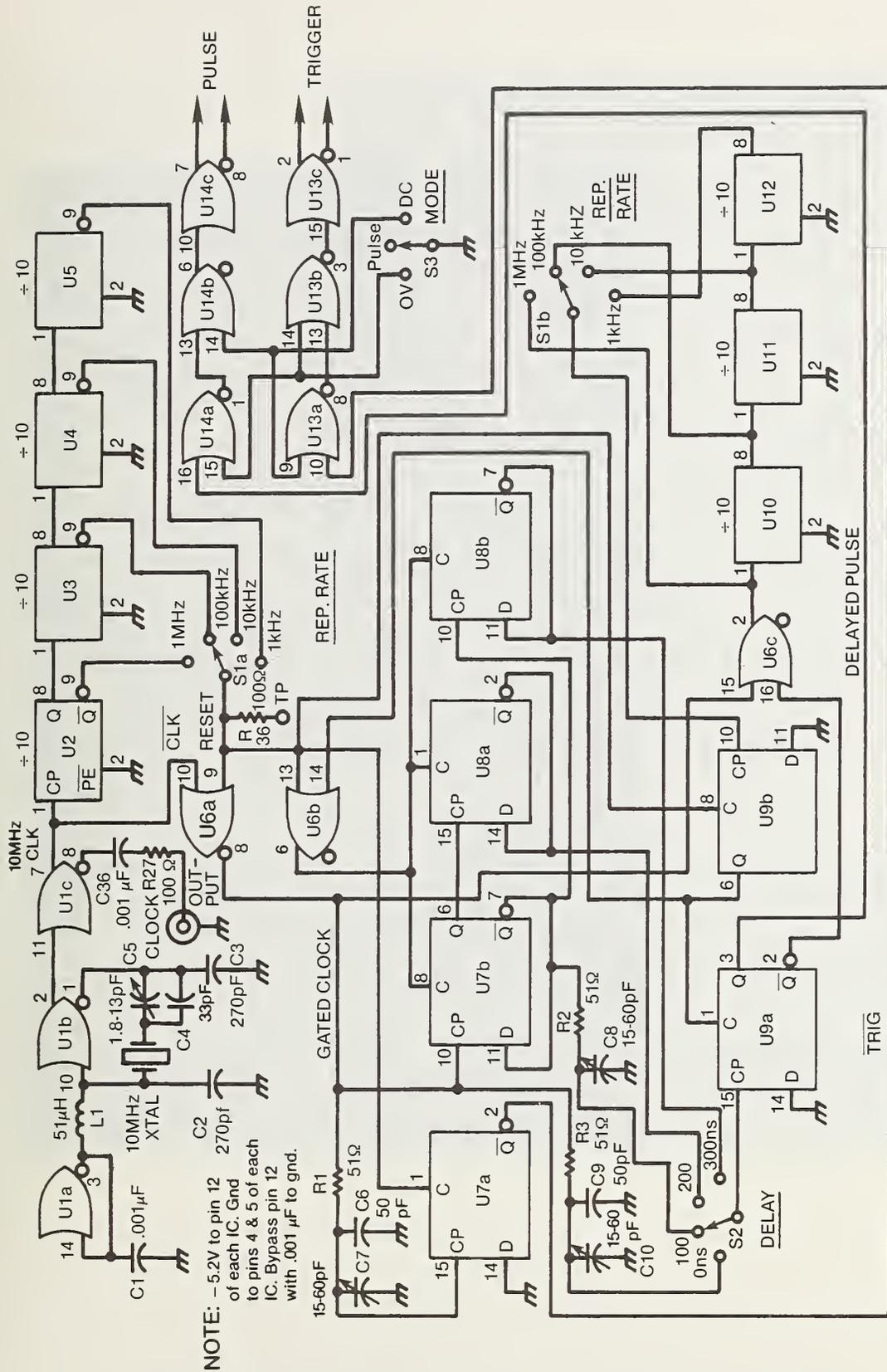


Figure 3-1. Schematic diagram of the clock, pulse duration, and pulse delay circuits.

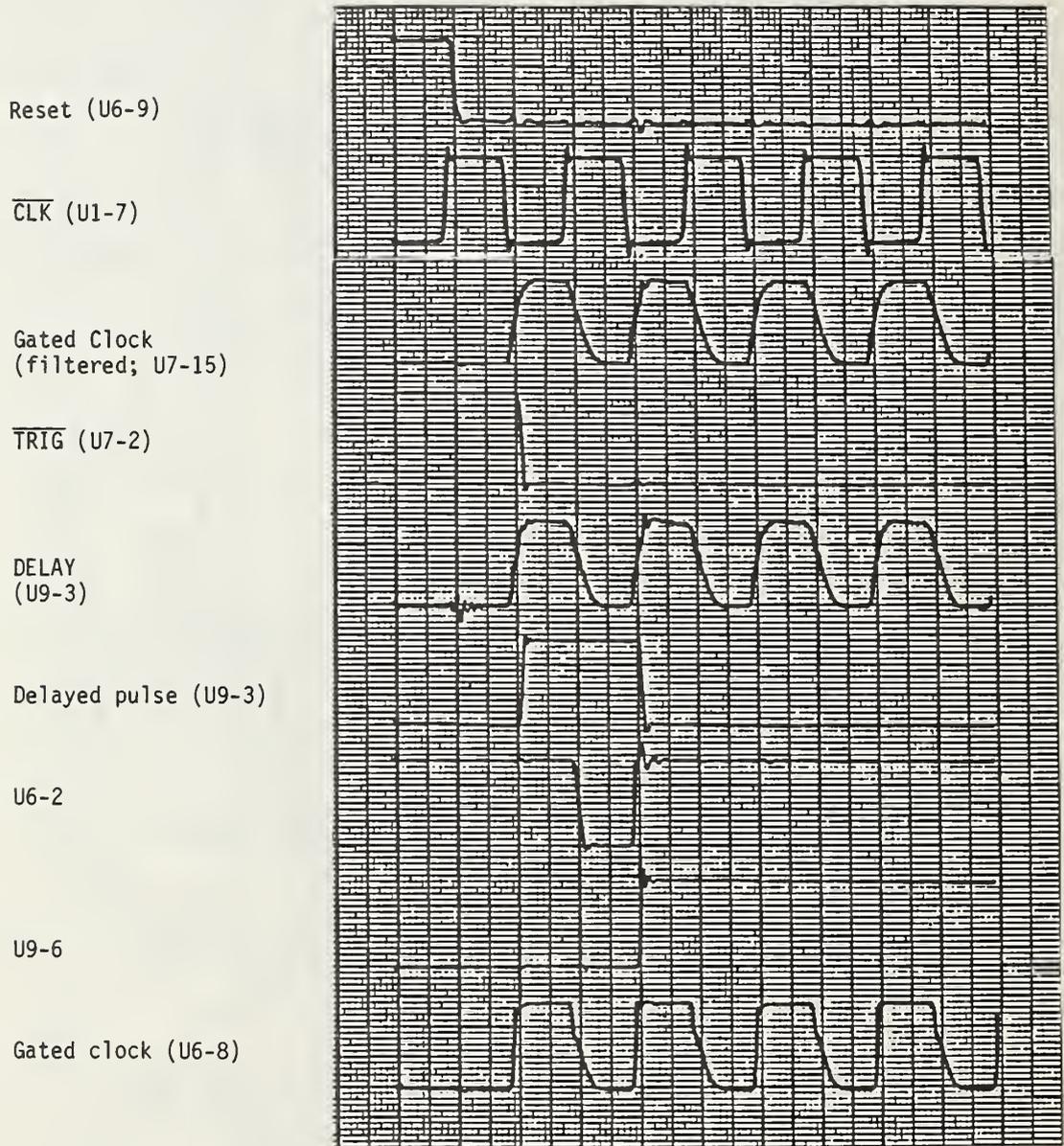


Figure 3-2. Timing diagrams for 1 MHz repetition rate, 0 ns delay.

Reset (U6-9)

Gated clock (U6-8)

$\overline{\text{TRIG}}$ (U7-2)

U7-6

U8-2

Delay (U9-15)

Delayed pulse (U9-3)

U6-2

U9-6

U6-6

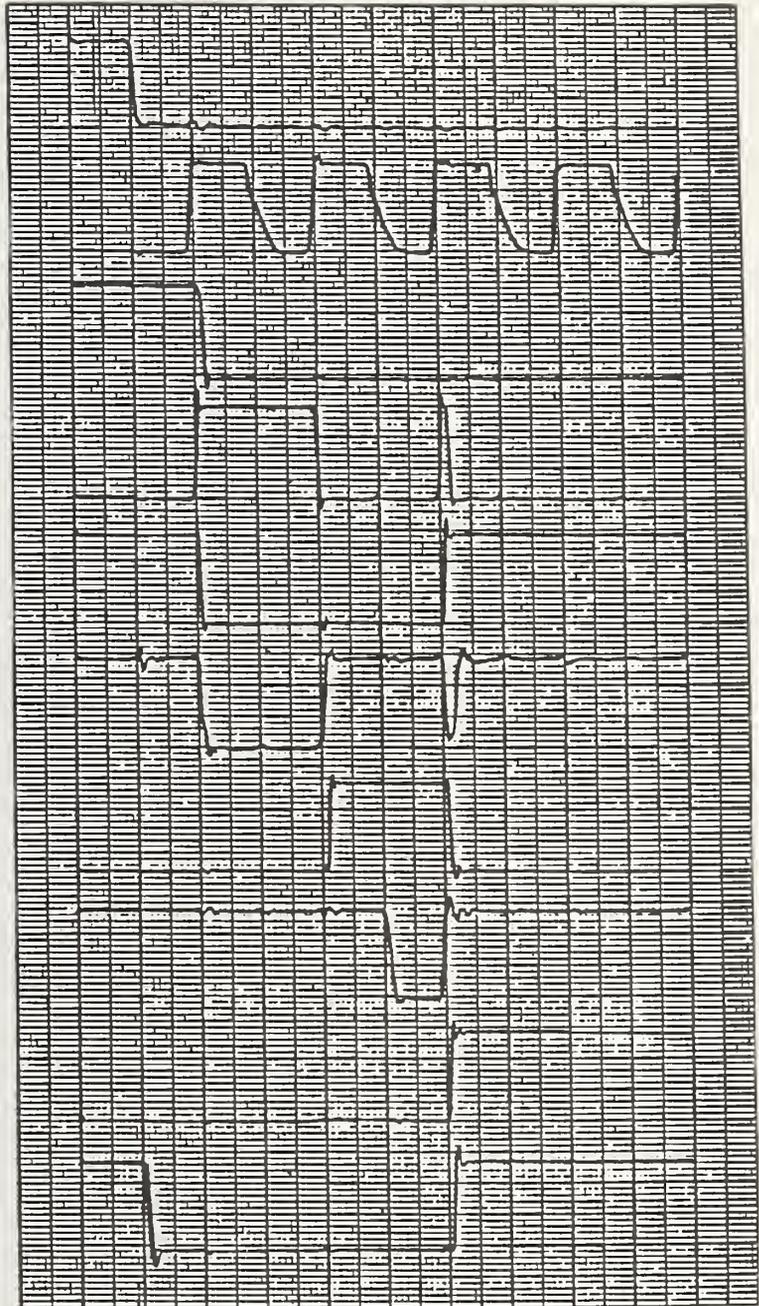


Figure 3-3. Timing diagrams for 1 MHz repetition rate, 100 ns delay.

Reset (U6-9)

Gated clock (U6-8)

$\overline{\text{TRIG}}$ (U7-2)

U7-6

U8-2

Delay (U9-15)

Delayed Pulse (U9-3)

U6-2

U9-6

U6-6

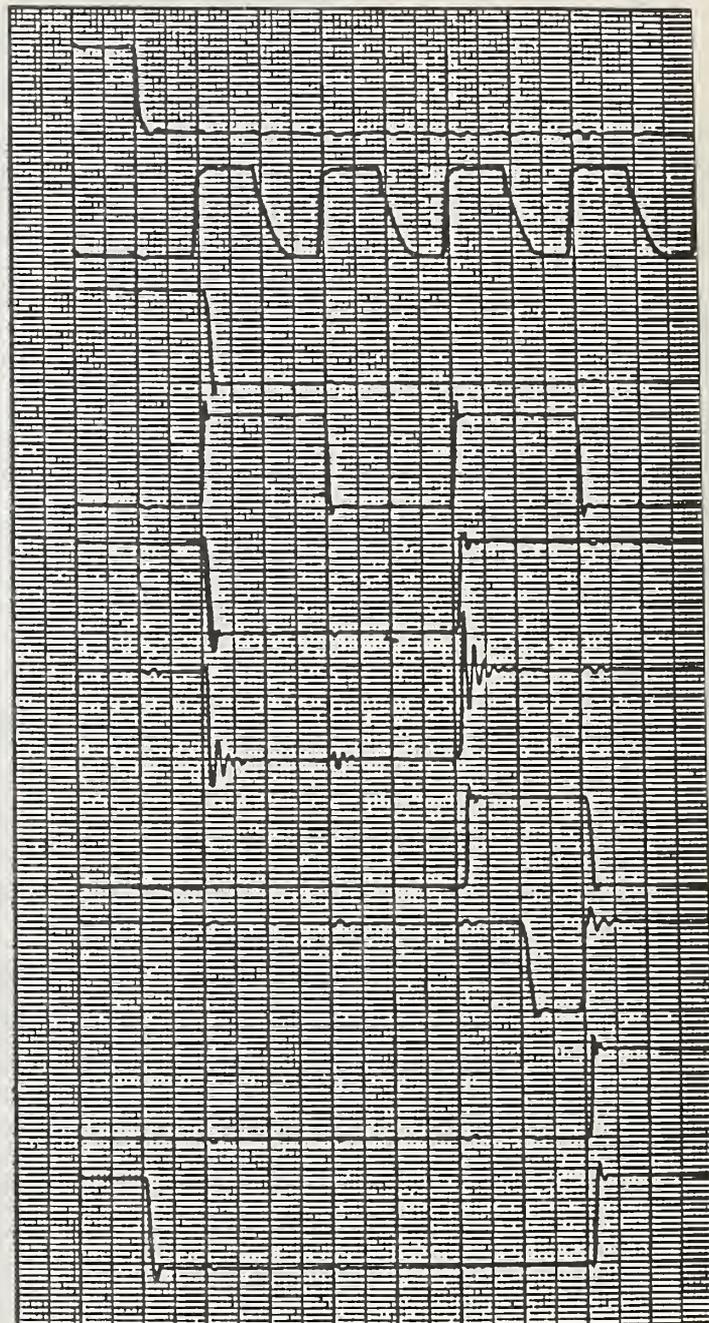


Figure 3-4. Timing diagrams for 1 MHz repetition rate, 200 ns delay.

Reset (U6-9)

Gated clock (U6-8)

$\overline{\text{TRIG}}$ (U7-2)

U7-7

U8-7

Delayed pulse (U9-3)

U6-2

U9-6

U6-6

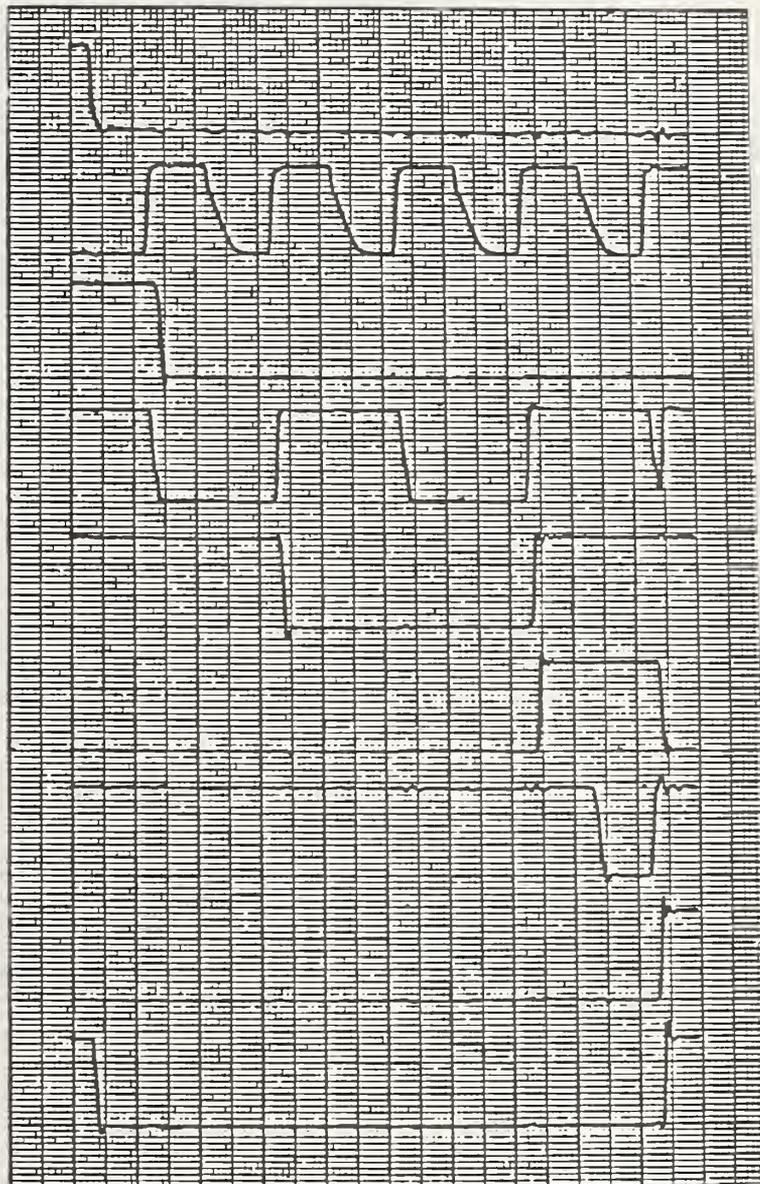


Figure 3-5. Timing diagrams for 1 MHz repetition rate, 300 ns delay.

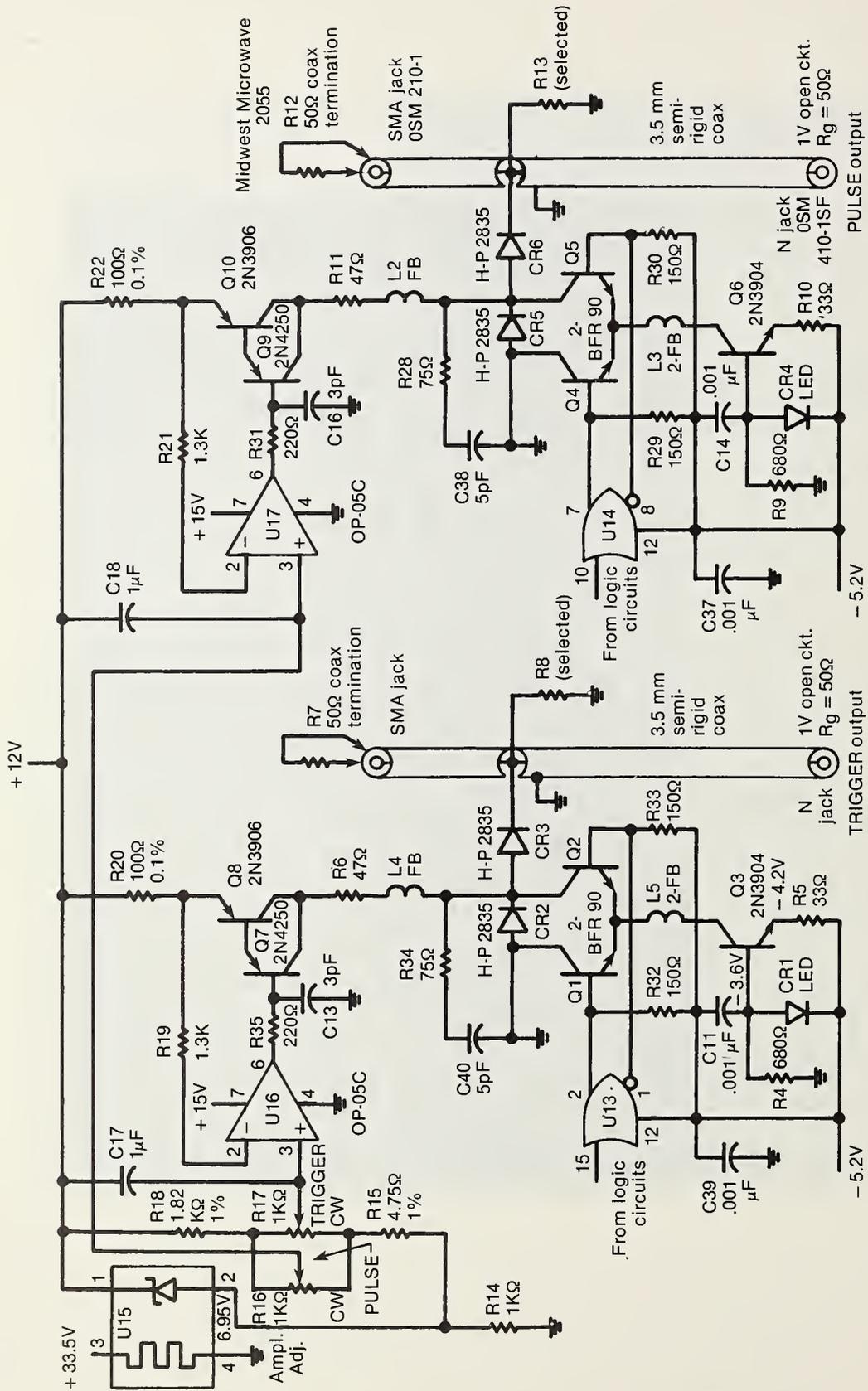


Figure 3-6. Schematic diagram of RFPG output stages.

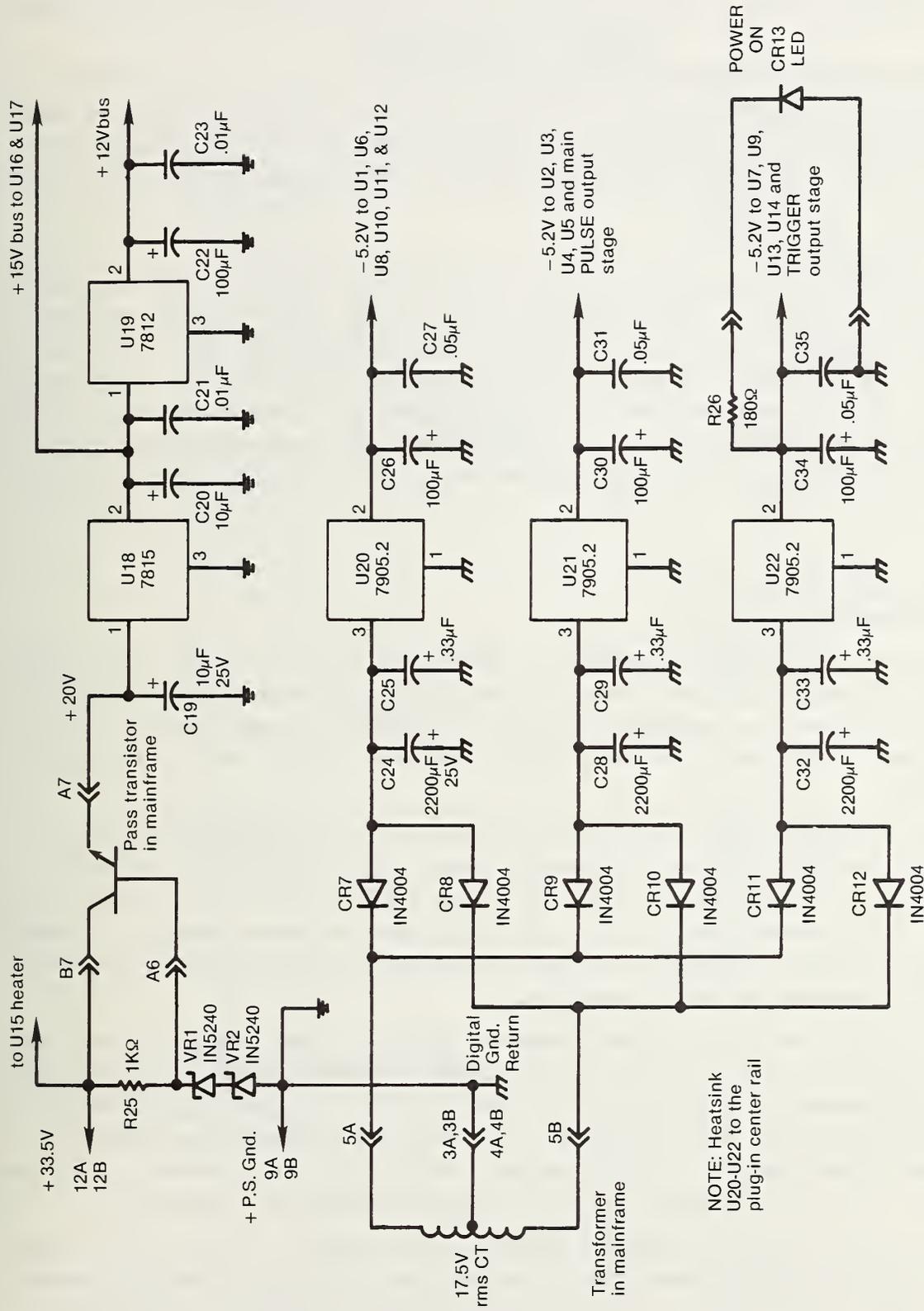


Figure 3-7. Power supplies for RFGG.

A less complex current source is used for the 30 mA emitter current for the differential switches Q1 and Q2. Q3 is the current source. CR1 is an LED which provides a 1.6 V reference voltage. This reference, minus Q3's base-emitter drop of 0.6 V sets the voltage across R5 at 1 V. This voltage in turn forces the emitter current of Q3 to be 30 mA. The collector current of Q3 is also approximately 30 mA.

The other miscellaneous components are used primarily to control the switching transition. R32 and R33 improve the switching times of U13. L5 increases the output impedance of Q3 at high frequencies. R6 and L4 perform a similar function for Q7 and Q8. R35 and C13 eliminate a small amount of damped ringing present in Q7 and Q8. R34 and C40 eliminate a minor overshoot in the output waveform.

3.3 Power Supplies

Figure 3-7 is the schematic diagram of the power supplies for the generator. The requirements are: +12 V at 45 mA, +15 V at 55 mA, and -5.2 V at 1 A (1.4 A worst case). The TM-500 mainframe is used to supply raw dc and ac power. The +33 V supply is first preregulated to +20 V using VR1, VR2, and a mainframe pass transistor. The +20 V is then dropped to +15 V using U18. U19 further drops the +15 V to +12 V. -5.2 V is supplied by three separate IC regulators, U20 through U22. The connections to the output stages and various ECL circuits are such as to evenly distribute the load currents. The top and bottom rails of the plug-in module housing the RFPG circuit card are used as heat sinks for U18 through U22.

4. Modeling and Computer Simulation

4.1 Use of Extended-SCEPTRE

The motivation for doing computer analysis and simulation of the RFPG is that in order to have a waveform generator standard, one needs a theoretical basis for how the electronics generate the various electrical waveshapes. Circuit modeling, using known or measured parameters for the circuit model, allows one to approximate the actual results and thereby predict the circuit performance from basic principles.

The circuit analysis programs developed for the RFPG were written using extended-SCEPTRE. The host computer for the extended-SCEPTRE software was a Control Data Corporation CYBER 170, model 750 system. Waveshape generation by computer simulation of the RFPG was conveniently obtained by accessing the CYBER 170 via a graphics terminal over a multiplexed hardwired link at 9600 baud. A FORTRAN 66 program known as DISSPLA, available on the CYBER 170, provided the capability for plotting the transient analysis data obtained from a SCEPTRE run.

Besides the SCEPTRE application programs themselves, described in detail in the following sections, other procedural programs were utilized. For example, a FORTRAN program was available, known as PLOTSCP, which accessed the tape containing data from a SCEPTRE run, as well as the DISSPLA program, and provided options for title on graph, start and stop times, independent and dependent variables, number of available points, running average, vertical scaling, etc. Another program, similar to PLOTSCP, was utilized for outputting data via a terminal having a paper tape punch.

Figure 4-1 shows the outline of a typical SCEPTRE program. Between the /JOB and /EOR statements are typically a number of FORTRAN command instructions which set up the batch processing procedures needed by the CYBER 170/750 system. The remainder of the program has somewhat of a fixed format with the various headings shown. Getting the proper entries under each of these headings is the main problem towards generating a successful SCEPTRE program.

PROGRAM NAME

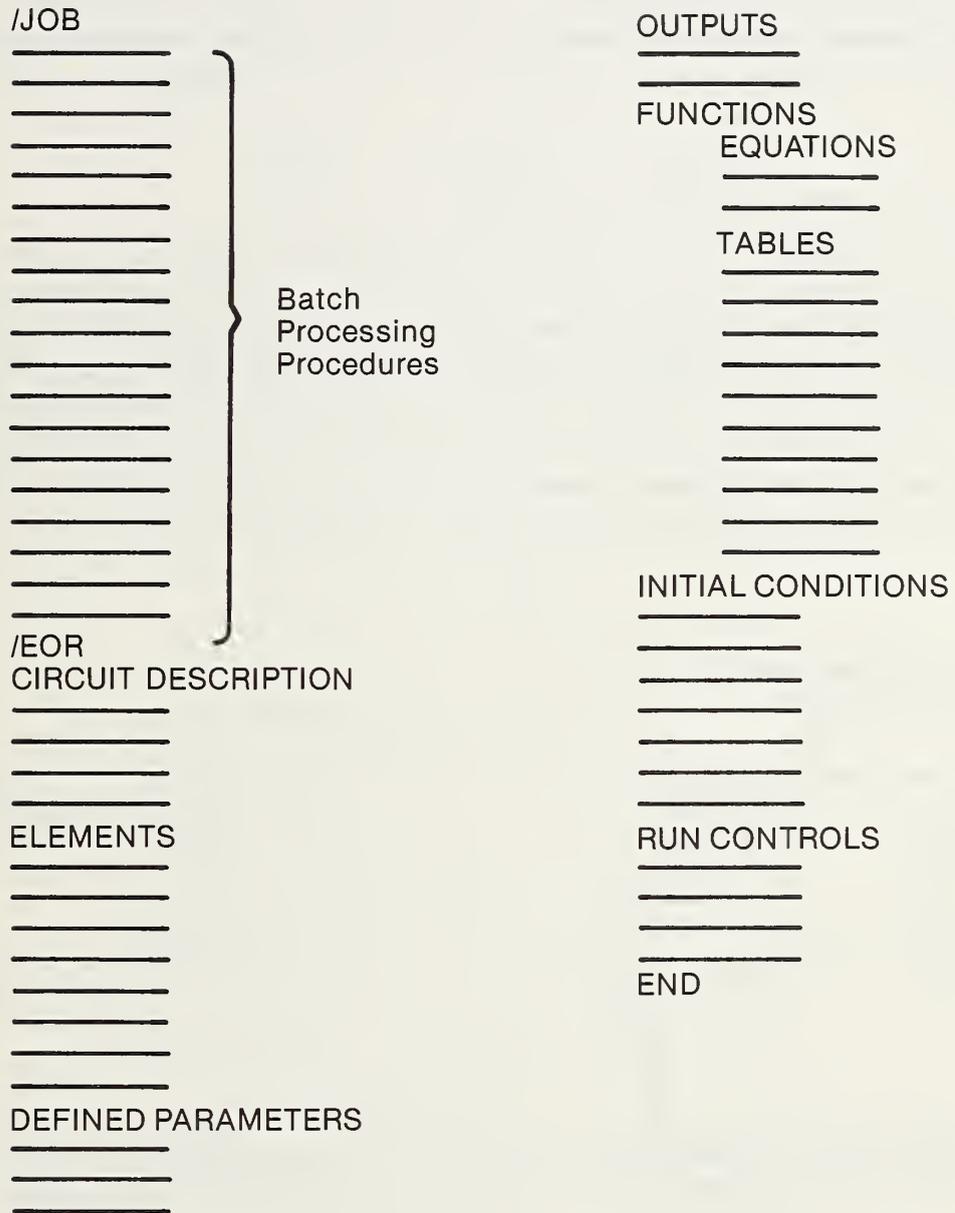


Figure 4-1. Typical SCEPTRE program.

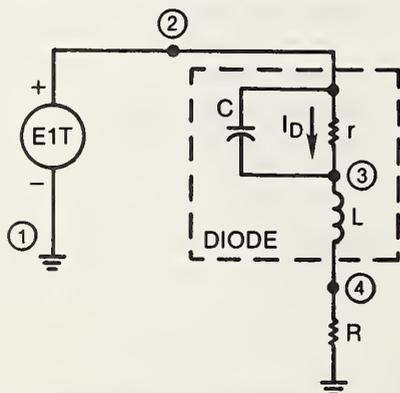
For the purpose of modeling the RFPG, the ability to utilize time-dependent, nonlinear circuit elements provided for in SCEPTRE was essential [13]. In particular, primary dependent current sources for ideal diodes proved to be especially convenient when combined with voltage or current dependent capacitors. Secondary dependent current sources with nonlinear, table-entered, dependencies permitted the development of an accurate model for the rf-switching transistors used in the output stage of the RFPG.

Run controls for the SCEPTRE programs were relatively simple in that transient solutions were the only mode of analysis desired. Consequently, a stop time is the only required entry to specify the desired time interval for analysis. However, because the Runge-Kutta integration method was found to typically give the best results, this routine was also called for under the run controls section of the programs.

4.2 Simple Diode Circuit Analysis via Program TEST

As a simple example of using SCEPTRE for modeling transient response, figure 4-2 shows the SCEPTRE circuit for a diode in series with a load resistor, R. The diode is first modeled by its dynamic forward resistance, r, junction capacitance, C, and package inductance, L. E1 is the driving node voltage which is a time function, entered in the program by means of a table. By analogy to the RFPG output stage, this is a very simple model of the switching mode for the current sources and the output diode in series with the generator source resistor (in parallel with the output load resistor). Hence, by assuming appropriate initial conditions (voltage on C and current through L), we can simulate the output voltage across R for various input time functions of E1.

E1T is the driving node voltage time function



$$\text{When using } I_D = I_0(\exp^{\theta V_D} - 1)$$

$$r = [\theta(I_D + I_0)]^{-1}$$

$$\approx \frac{1}{\theta I_D}$$

Transfer function:

$$\frac{V_R}{E1} = \frac{\left(\frac{R}{R+r}\right)(rCs + 1)}{\left(\frac{r}{R+r}\right)LCs^2 + \left(\frac{L+RrC}{R+r}\right)s + 1}$$

Critical Damping:

$$r_c = \frac{L}{RC \pm 2\sqrt{LC}}$$

or,

$$R_c = \frac{L}{rC} \pm 2\sqrt{L/C}$$

For R = 0:

$$r_c = \frac{1}{2}\sqrt{L/C}$$

For r = ∞

$$R_c = 2\sqrt{L/C}$$

Figure 4-2. Simple diode model for TEST program.

Straightforward Laplace transform analysis of this circuit (assuming zero initial conditions) gives the transfer function,

$$\frac{V_R}{E1} = \frac{\left(\frac{R}{R+r}\right) (rCs + 1)}{\left(\frac{r}{R+r}\right) LCs^2 + \left(\frac{L + RrC}{R+r}\right) s + 1}, \quad (1)$$

where V_R is the voltage across R . For $E1$ a step function, it is well-known that the step response for such a second-order system will depend on the roots or pole locations of the denominator polynomial. These roots can, in general, be complex and are given by

$$s_1, s_2 = \frac{-\left(\frac{L + RrC}{R+r}\right) \pm \sqrt{\left(\frac{L + RrC}{R+r}\right)^2 - 4\left(\frac{r}{R+r}\right) LC}}{2\left(\frac{r}{R+r}\right) LC}. \quad (2)$$

Critical damping occurs when the square root term is zero (equal real roots). Underdamping occurs when the quantity under the square root is negative (complex roots with both real and imaginary parts), and an overdamped response occurs when this quantity is positive (both roots real and unequal).

Further algebraic manipulations for the critically damped case provide the critical value for r ,

$$r_c = \frac{L}{RC \pm 2\sqrt{LC}} \quad (3)$$

or, for R ,

$$R_c = \frac{L}{rC} \pm 2\sqrt{\frac{L}{C}}. \quad (4)$$

For the extreme case where $R \rightarrow 0$,

$$r_c = \frac{1}{2}\sqrt{\frac{L}{C}}, \quad (5)$$

which is the well-known critical resistance of a parallel-tuned rLC circuit. Similarly, for the extreme case where $r \rightarrow \infty$,

$$R_c = 2\sqrt{\frac{L}{C}}, \quad (6)$$

which is the well-known critical resistance for a series-tuned RLC circuit. Letting $R = 3r_c$ in eq (3), so that $r_c/(R + r_c) = 1/4$ in eq (2),

$$r_{c1}, r_{c2} = \sqrt{\frac{L}{C}}, \frac{1}{3}\sqrt{\frac{L}{C}}.$$

Typical values of L and C for the Schottky diodes used in the RFPG are 2 nH and 1 pF, respectively. Then,

$$\begin{aligned}
r_{c1}, r_{c2} &= \sqrt{\frac{2 \times 10^{-9}}{10^{-12}}}, \frac{1}{3} \sqrt{\frac{2 \times 10^{-9}}{10^{-12}}} \\
&= 10\sqrt{20}, \frac{10}{3}\sqrt{20} \\
&= 44.72 \, \Omega, 14.91 \, \Omega.
\end{aligned}$$

Corresponding R values are 134.2 Ω and 44.72 Ω .

Figure 4-3 shows the SCEPTRE program, TEST1, for analyzing the step response of the diode-load resistor circuit. As shown, E1 as a function of time is provided by table 1 which has five entries. By applying a negative 1 V step, the program thus simulates the output branch circuit of the RFPG (assuming negligible effects due to the 3.5 mm coaxial line). Because of the critical values chosen for r (designated RS) and R (designated RL), the initial conditions for the capacitor voltage and inductor current are the values given as 0.25 V and 0.01677 A, respectively.

Figure 4-4 is a plot of the waveforms generated by program TEST1. As expected, these responses show critical damping of the R-r, L, C circuit described above. VRL, VRS, and VL are the voltage waveforms across RL, RS, and L, respectively. For the typical values used, it can be seen that the step response has died out in approximately 200 ps. Figure 4-5 shows that with RL = 25 Ω (the nominal value), the response is overdamped, settling in about 300 ps. With RL again at 44.72 Ω , but with a larger RS of 50 Ω , figure 4-6 displays the resulting underdamped waveforms.

The nonlinear I-V characteristic of the diode, where its dynamic forward resistance varies inversely with the diode current, was then added to create the TEST2 program. Figures 4-7 and 4-8 show the typical characteristic for the particular Schottky barrier diode used in the RFPG [14]. Figure 4-9 is a listing of the TEST2 program which indicates how SCEPTRE allows the simple entry for the diode under ELEMENTS. The first argument inside the parenthesis is the value for I_0 , the reverse "leakage" current, typically 100 nA. The second argument is the value for $\theta = e/kT$ which at room temperature (300 K) is the value 38.7. Note also the different initial conditions which must be satisfied in this case.

Figure 4-10 shows the resultant circuit waveforms with r replaced by the diode equation. Since figure 4-5 shows an overdamped response for r = RS \cong 15 Ω , figure 4-10 is somewhat startling at first. With a starting forward current of 0.0274 A (27.4 mA), one would expect from figure 4-8 a more damped response since r is typically less than 15 Ω for diode currents of about 2 to 3 mA or more. However, figure 4-6 also supports the analysis that as r increases, the response grows underdamped. Thus we see that the time-dependent variation of r in the case of the actual diode is such as to cause an undershoot in the negative step response, as the diode current cuts off.

Further investigation into the nonlinear effects of the Schottky diode used in the RFPG were pursued, as will be described in the following sections. As a final example of modeling the diode-load resistor output branch, however, figure 4-11 shows the listing for program TEST3 in which E1, the driving node voltage, is set up via table 1 to approximate the "double ramp" type of voltage waveform actually observed in the RFPG. Figure 4-12 gives a plot of the resultant waveforms generated by program TEST3. The time base is five times longer than before for TEST2 and the values for C and L changed by a factor of four. Nevertheless, the undershoot in the response (VRL) of the simulated waveform is seen to much more clearly approximate the actual observed output waveform (see fig. 2-7).

TEST1

```

/JOB
SCEPTRE (T200)
READ,USERFIL
HEADING,B10AUSCPTTR
PURGE,TAPEBEL.
GOTO,1.
EXIT.
1. PURGE,TAPE2.
GOTO,2.
EXIT.
2. ATTACH, SUPER/UM-LIB,NA.
RETURN, SUPER.
ATTACH, SCEPTR/UM-LIB,NA.
SCEPTR.
RETURN, SCEPTR.
FTN, 1-TAPEB, A, L-ZBELL.
GET, SCPT2B/UM-LIB,NA.
REWIND,TAPEB.
SKIPFF,TAPEB.
RETURN,TAPE14,TAPE3,TAPE1,TAPE2,TAPE13,TAPE16,TAPE15.
DEFINE,TAPEB.
MAP,OFF.
LOAD,SCPT2B.
LGO.
GOTO,3.
EXIT.
3. REWIND,TAPE2.
RETURN,TAPE1,TAPE3.
DEFINE(TAPE14,TAPEBEL)
REWIND,TAPE14.
GET, SCPTA3/UM-BLP.
ATTACH(LIB/UM-LIB)
LDSET(LIB-LIB)
SCPTA3B.
PURGE,TAPE2.
/EOB
CIRCUIT DESCRIPTION
RLC TEST PROGRAM 1(11/14/B1)
E IN VOLTS
R IN OHMS
C IN FARADS
J IN AMPERES
L IN HENRYS
TIME IN SECONDS
ELEMENTS
E1, 1-2 - TABLE 1 (TIME)
R5, 2-3 - 14.007
C, 2-3 - 1.0E-12
L, 3-4 - 2.0E-9
RL, 4-1 - 44.72
OUTPUTS
URL,UL,VRS,PLOT
FUNCTIONS
TABLE 1
0.E-12, 1.0
100.E-12, 1.0
150.E-12, 0.0
200.E-12, 0.0
1000.E-12, 0.0
INITIAL CONDITIONS
UC - 0.E5

```

```

IL - 0.01877
RUN CONTROLS
INTEGRATION ROUTINE - RUK
STOP TIME - 1000.E-12
PLOT INTERVAL - 5
END OF FILE
?? END, TEST2,RL
TEST2 REPLACED
TEST2 IS A LOCAL FILE
/SUBMIT,TEST2
11.51.45. SUBMIT COMPLETE. JOBNAME IS ACKIIE
/ENQUIRE,JN-IJE
/ACKIIE, EXECUTING.
/ENQUIRE,JN-IJE
/ACKIIE, NOT FOUND.
/CATALOG
CATALOG OF BABELL
FR/NOAA 81/11/14. 11.52.39.
INDIRECT ACCESS FILE(S)
3 GOSCEP PHOT02A RFP010C RFP011 TEST1 TRANGE TRFPG
IL GOUIEU PHOT02B RFP010D RFP011B TEST2 TRFPG1 USERF
IL MAKOO RFP010B
DIRECT ACCESS FILE(S)
TAPEBEL
16 INDIRECT ACCESS FILE(S), TOTAL PRUS - 58.
1 DIRECT ACCESS FILE(S), TOTAL PRUS - 9.
/CALL,GOSCEP

```

Figure 4-3. Listing for SCEPTRE program TEST1.

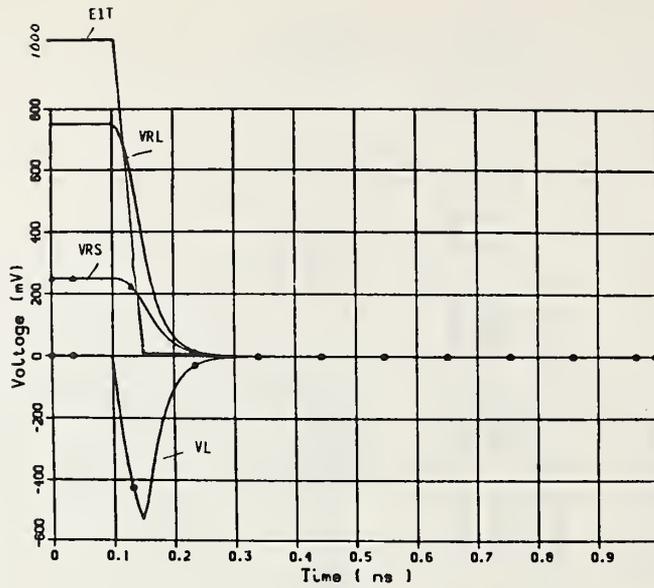


Figure 4-4. Step response from TEST1 program. Critical damping with $R_S = 14.91 \Omega$ and $R_L = 44.72 \Omega$.

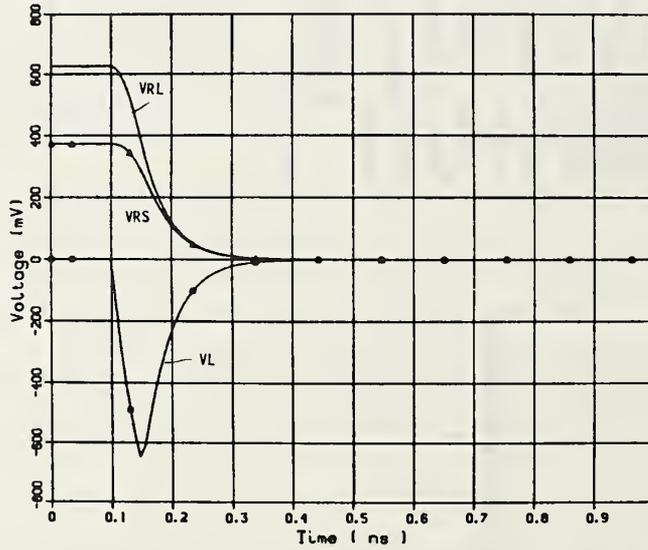


Figure 4-5. Step response from TEST1 program. Overdamping with $R_S = 14.91 \Omega$ and $R_L = 25.0 \Omega$.

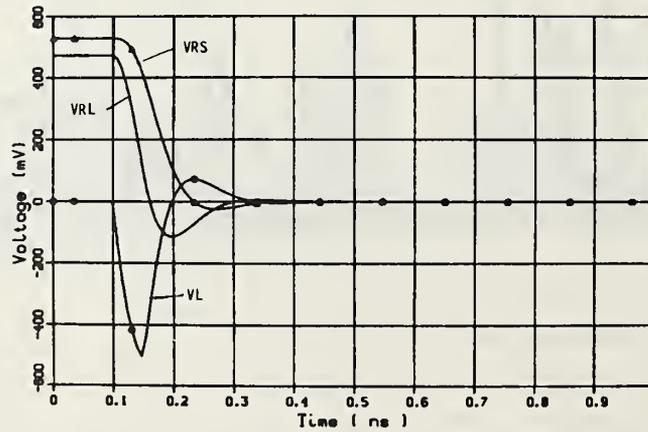


Figure 4-6. Step response from TEST1 program. Underdamping with $R_S = 50.0 \Omega$ and $R_L = 44.72 \Omega$.

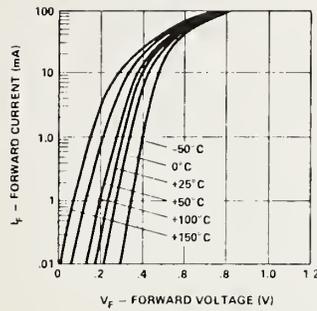


Figure 4-7. I-V curve showing typical temperature variations for 5082-2835 Schottky diode.

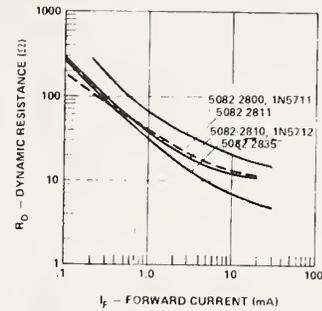


Figure 4-8. Typical dynamic resistance (R_D) versus forward current (I_F).

Thus it is that further modeling of the nonlinear RFPG output stage components was felt to be needed in order to derive the approximate driving node voltage waveform.

4.3 Initial Modeling via Program RFPG

As described in sections 2.2 and 3.2, the output stage of the RFPG consists of positive and negative current sources that are steered by means of transistor switches (see figs. 2-5, 2-6, and 3-6). An initial model that was used for simulating the output stage is shown in figure 4-13. Ideal diode current JD1 and associated components C1, L1, and C4, together with R3, form the output branch of the generator circuit. Similarly, JD2, C2, L2, and C5 represent the CR2 diode of figure 2-6 (CR2 and CR5 of fig. 3-6). C1 and C2 are the voltage dependent junction capacitance, L1 and L2 are the package inductance, and C4 and C5 are the package capacitance of the diodes [14]. R2 and C3 are the filter components for controlling part of the undershoot in the output waveform. J1 and J2 are the nominal 20 mA and 30 mA positive and negative constant current sources (33 mA value used in SCEPTRE program for J2). To simulate the action of the switching transistors time-dependent resistors R1T and R2T are utilized.

Several versions of the program for this model were developed in the process of experimenting with component values, appropriate initial conditions, and the switching times/resistance levels of the R1T and R2T resistors. Figure 4-14 shows the SCEPTRE program, RFPG10, which yielded fairly useful results. In the topological listing under ELEMENTS, the voltage dependence of C1 and C2 is provided by table 2 which uses typical values provided by the manufacturer's data sheet [14]. Tables 1 and 3 provide the resistance versus time dependence of R1T and R2T, approximating the complementary switching action of the BFR 90 rf switching transistors. These devices are rated for a current gain-bandwidth product, $f_T = 5$ GHz (typical) at $I_C = 14$ mA. Under INITIAL CONDITIONS are shown the two initial inductor currents and five initial capacitor voltages.

Figure 4-15 gives the resultant plots of the transient step-like output voltage across R3 and driving node voltage across C5 for the RFPG10 program. The flatness of the waveforms at $t = 0_+$ indicates that the assumed values of the initial conditions is good. The wrinkle in the transition region at about 0.45 ns is for the VC5 waveform which is identified by the black dots. There is a considerable (on the order of 20 percent) undershoot in the VR3 waveform which does not approximate reality very well. However, as demonstrated in section 4.2, this difference is probably due to lack of the

TEST2

```

/JOB
SCEPTRE(1200)
/READ.USERFIL
HEADING.BIBABSCPTR
/NOSEQ
PURGE.TAPEBEL.
GOTO,1.
EXIT.
1.PURGE.TAPE2.
GOTO,2.
EXIT.
2.ATTACH.SUPER/UN-LIB,NA.
SUPER.
RETURN,SUPER.
ATTACH,SCEPTR/UN-LIB,NA.
SCEPTR.
RETURN,SCEPTR.
ATTACH,SCPTK2B/UN-LIB,NA.
GET,SCPTK2B/UN-LIB,NA.
REWIND,TAPE8.
SKIP,TAPE8.
RETURN,TAPE14,TAPE3,TAPE1,TAPE2,TAPE13,TAPE15,TAPE16.
RECINE,TAPE2.
/NO,OFF.
LOAD,SCPTR2B.
GGO.
GOTO,3.
EXIT.
3.REWIND,TAPE2.
RETURN,TAPE1,TAPE3.
REWIND,TAPE14,TAPEBEL)
REWIND,TAPE14.
ATT,SCPTAP3/UN-BLP.
LDSCR(LIB/UN-LIB)
SCPTAP3.
PURGE,TAPE2.
/NO.
CIRCUIT DESCRIPTION
RLC TEST PROGRAM 2(11/14/81)
R IN VOLTS
R IN OHMS
C IN FARADS
J IN AMPERES
L IN HENRIES
TIME IN SECONDS
ELEMENTS
E1, 2-5 * TABLE 1 (TIME)
J0, 2-5 * DODE EQUATION(1.E-7,38.7)
C, 2-3 * 1.0E-2
L, 3-4 * 2.0E-9
RL, 4-1 * 25.
OUTPUTS
URL,VL,UC,PLOT
FUNCTIONS
TABLE 1
0.E-12, 1.0
100.E-12, 1.0
150.E-12, 0.0
200.E-12, 0.0
1000.E-12, 0.0
INITIAL CONDITIONS
UC = 0.315

```

```

IL = 0.0274
RUN CONTROLS
INTEGRATION ROUTINE = RUK
STOP TIME = 1000.E-12
PLOT INTERVAL = S
END
END OF FILE
77 END, TEST2, RL
TEST2 IS A LOCAL FILE
/SUBMIT, TEST2
13.15.08. SUMMIT COMPLETE. JOBNAME IS AKKI10T
/ENQUIRE, JN=10T
AKKI10T EXECUTING.
/ENQUIRE, JN=10T
AKKI10T NOT FOUND.
/CATLIST
CATALOG OF BABELL FM/NOAAA 81/11/14. 13.16.06.
INDIRECT ACCESS FILE(S)
3 GOSCEP PHOTO2A RFPG10C RFPG11 TEST1 TRANGE TRFPG
IL GOUIEU PHOTO2B RFPG10D RFPG11B TEST2 TRFPG1 USER
MAKGO RFPG10B
DIRECT ACCESS FILE(S)
TAPEBEL
16 INDIRECT ACCESS FILE(S), TOTAL PRUS = 50.
1 DIRECT ACCESS FILE(S), TOTAL PRUS = 12.
/CALL, GOSCEP

```

Figure 4-9. Listing of SCEPTRE program TEST2.

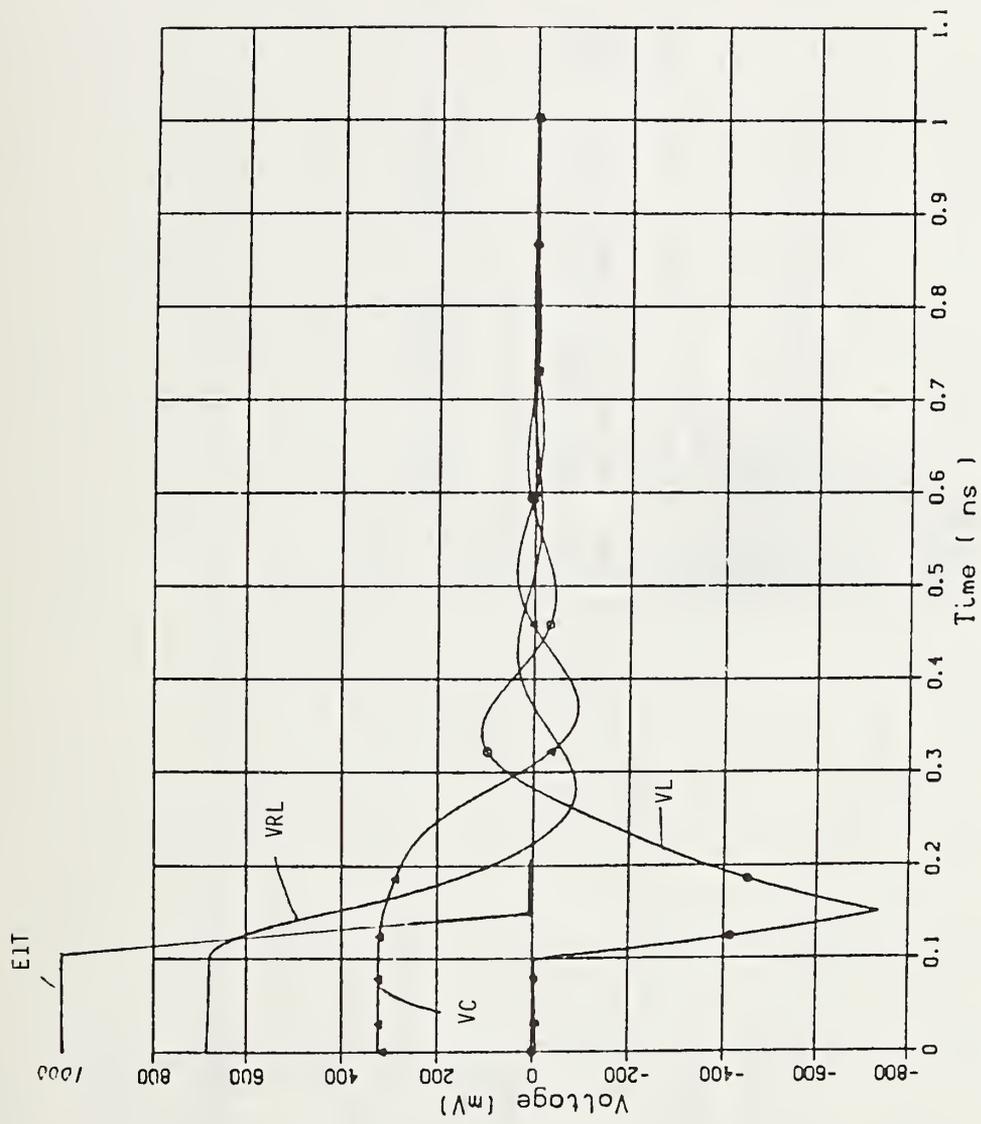


Figure 4-10. Step response from TEST2 program. Underdamping of VRL waveform with r replaced by diode equation.

TEST3

```

/JOB
SCEPTRE(T300)
/READ,USERILL
/HEADING,LIBABSCPTR
/NOSED
PURGE,TAPEBEL.
GOTO,1.
EXIT.
1. PURGE,TAPE2.
GOTO,2.
EXIT.
2. ATTACH, SUPER/UM=LIB,NA.
RETURN,SUPER.
ATTACH,SCEPTR/UN=LIB,NA.
SCEPTR.
RETURN,SCEPTR.
FTN,1=TAPE3,A,1=ZBELL.
GET,SCPTR2B/UM=LIB,NA.
REWIND,TAPE3.
SKIPF,TAPE3.
RETURN,TAPE14,TAPE3,TAPE1,TAPE2,TAPE13,TAPE15,TAPE16.
DEFINE,TAPE2.
MAP,OFF.
LOAD,SCPTR2B.
LGO.
GOTO,3.
EXIT.
3. REWIND,TAPE2.
RETURN,TAPE1,TAPE3.
DEFINE(TAPE14=TAPEBEL)
REWIND,TAPE14.
GET,SCPTAPB/UM=BLP.
ATTACH(LIB=LIB)
LDSET(LIB=LIB)
SCPTAPB.
PURGE,TAPE2.
/EOB
CIRCUIT DESCRIPTION
RLC TEST PROGRAM 3(11/17/81)
R IN VOLTS
C IN OHMS
C IN FARADS
J IN AMPERES
L IN HENRYS
TIME IN SECONDS
ELEMENTS
E1, 1-2 - TABLE 1 (TIME)
JD, 2-3 - DIODE EQUATION(1.E-7,38.7)
C, 3-4 - 8.0E-9
L, 4-1 - 25.
OUTPUTS
URL,UL,VC,JD,IC,IRL,PLOT
FUNCTIONS
TABLE 1
0.E-9, 1.0
1.E-9, 1.0
2.E-9, 0.25
3.E-9, 0.0
4.E-9, 0.0
5.E-9, 0.0
INITIAL CONDITIONS
VC = 0.315
IL = 0.0274
RUN CONTROLS
INTEGRATION ROUTINE = RUK
STOP TIME = 5.0E-9
PLOT INTERVAL = 5
END
END OF FILE
/END,TEST3,RL
TEST3 REPLACED
TEST3 IS A LOCAL FILE
/submit TEST3
/submit,submit complete. JOBNAME IS ACKIFEC
/ACKIFEC,JEMECUTTING.
/ACKIFEC,JEMECUTTING.
/ACKIFEC,JEMECUTTING.
/ACKIFEC,JEMECUTTING.
/ACKIFEC,NOT FOUND.
/CATALOG
CATALOG OF BABELL
FR/NORA 81/11/17. 14.44.23.
INDIRECT ACCESS FILE(S)
3 GOSCEP PHOT02A RFPG10C RFPG11 TEST2 TRANGE TRFPG
IL GOUIEU PHOT02B RFPG10D RFPG11B TEST3 TRFPG1 USER
IL MAK00 RFPG10B
DIRECT ACCESS FILE(S)
TAPEBEL
16 INDIRECT ACCESS FILE(S), TOTAL PRUS = 50.
1 DIRECT ACCESS FILE(S), TOTAL PRUS = 156.
/CALL,GOSCEP

```

Figure 4-11. Listing of SCEPTRE program TEST3.

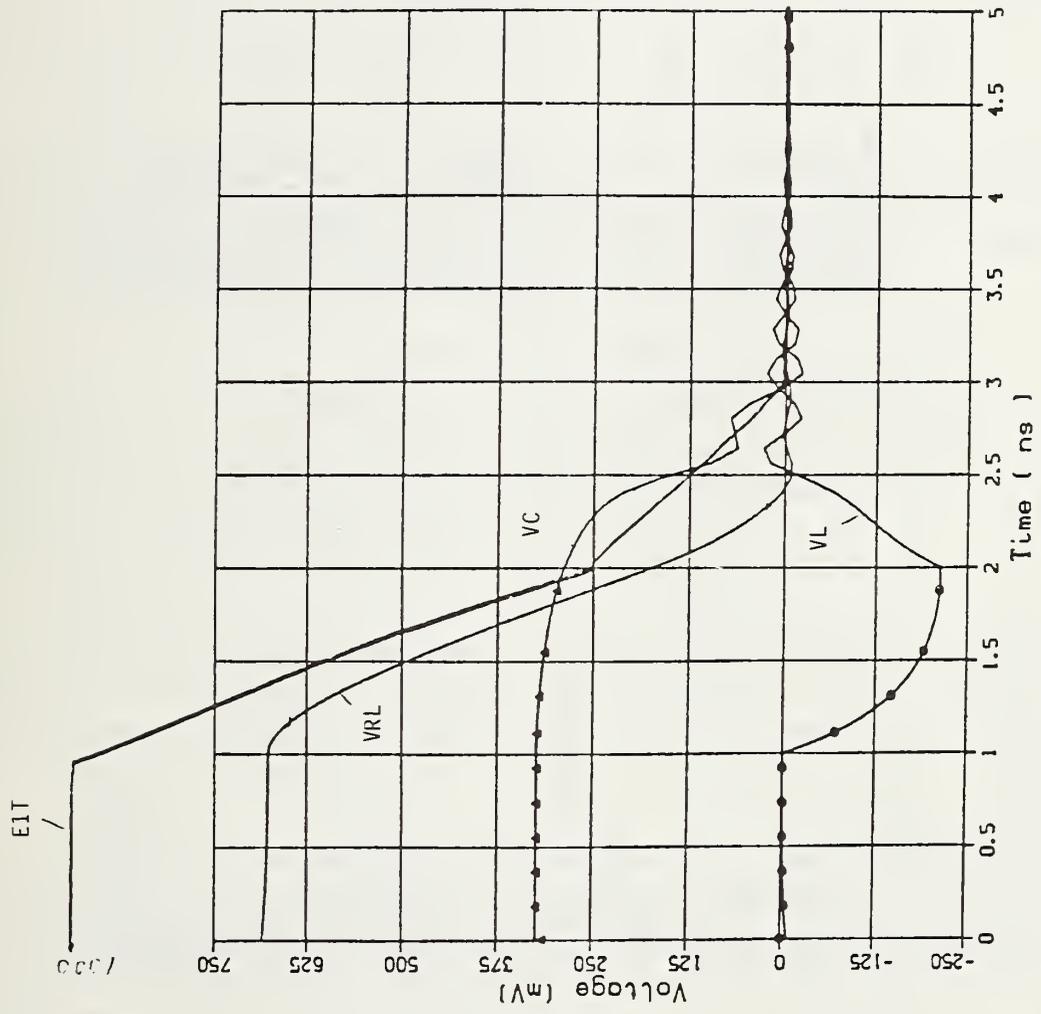


Figure 4-12. "Double ramp" response of RLC circuit from TEST3 program.

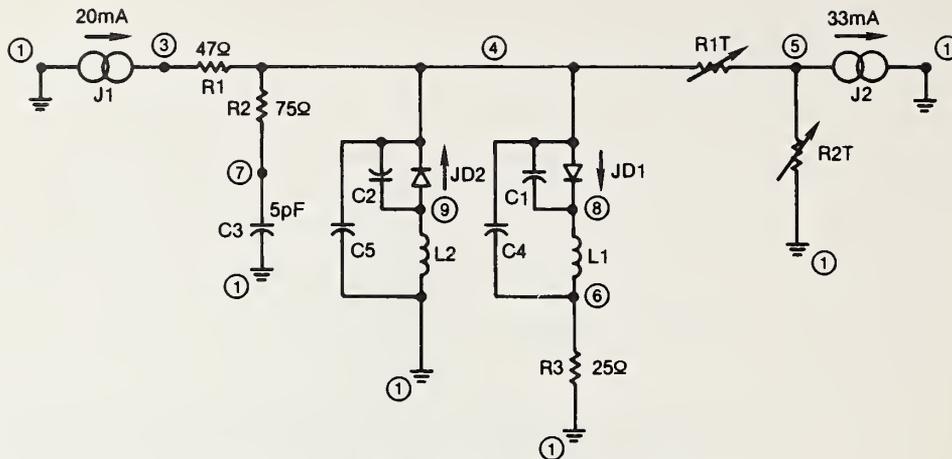


Figure 4-13. An initial RFGP program model.

proper waveform for VC5. This poor approximation of the actual driving node voltage in turn is due to the 300 ps switching from 100 k Ω (100 Ω) to 100 Ω (100 k Ω) for R1T (R2T). Nevertheless, the simulation does show that with such switching speed, a faster transition fall time than 600 ps could be realized.

4.4 ECL Drive and Transistor Switching Model via Program TRAN

Simple circuit modeling of the RFGP output stage, as described briefly in sections 4.2 and 4.3, reveals that the 600 ps transition duration observed in the actual step-like output waveform is limited by the speed of the switching elements more than by the properties of the output current-steering diodes. Consequently, work was undertaken to develop a model for the rf switching transistors used in the design of the RFGP and their associated complementary ECL input drive signals.

Figure 4-16 shows the schematic diagram of the SCEPTRE circuit used for this purpose. Node 14 corresponds to node 4 of the RFGP program with R9 at the collector of Q2 representing the load of the RFGP output network. The rf switching transistors, Q1 and Q2, are simulated by using a modified Geller, Mantek, and Boyle (GMB) model for large-signal switching [15]. The J3 constant current source corresponds to J2 in the RFGP program. The remaining components provide the simulation of the ECL OR gate drive of the actual RFGP circuit.

Regarding the model used for the individual transistors, figure 4-17 shows a simple common-emitter equivalent circuit that was developed for the BFR 90 transistors. The primary difficulty overcome with the use of this model is the effect of the nonlinear base-to-emitter characteristics of the transistor when driven with low driving source impedances. The basic GMB model represents the B-E junction, from charge control theory, as the nonlinear forward resistance of the base-emitter junction $r_{B'E}$ (as employed in section 4.2 for the Schottky barrier diode analysis), in parallel with two capacitors. One capacitor is the usual diffusion capacitance of the forward-biased base-emitter junction. The other capacitor is a feedback capacitance due to the component of base current that appears when the collector-to-base depletion layer varies as a function of collector base voltage. The feedback effects of the collector-to-base space charge capacitance are then directly contained in the solution of base current versus time when a finite load resistance (R3 in fig. 4-17) exists. An analysis to support this modified GMB model can be made by noting that for the forward biased base-emitter junction,

RFPG10

```

/JOB
SCEPTRE (TR00)
ACCOUNT (BARRELL, BARRELL)
CHARGE, TR4, 78444501.
HEADING, B1BABSCTR
/PROSD
PURGE, TAPEBEL.
GOTO, 1.
EXIT.
GOTO, 8.
1, PURGE, TAPEB.
EXIT.
2, ATTACH, SUPER/UN=LIB, NA.
RETURN, SUPER.
ATTACH, SCTR/UN=LIB, NA.
SCEPTR.
RETURN, SCEPTR.
FTN, I=TAPEB, A, L, ZBELL.
GET, SCTR/UN=LIB, NA.
REIND, TAPEB.
SKIPF, TAPEB.
RETURN, TAPE14, TAPE3, TAPE1, TAPE2, TAPE13, TAPE15, TAPE16.
DEFINE, TAPE2.
MAP, OFF.
LOAD, SCTR23.
LGO.
GOTO, 3.
EXIT.
3, REIND, TAPE2.
RETURN, TAPE1, TAPE3.
DEFINE (TAPE14=TAPEBEL)
REIND, TAPE14.
GET, SCTR/UN=BLP.
ATTACH (LIB=UN=LIB)
SCTR/TAPEB.
PURGE, TAPE2.
ZEOR.
CIRCUIT DESCRIPTION
REFERENCE FLAT PULSE GENERATOR-NETWORK 10(8/14/81)
R IN VOLTS
C IN FARADS
J IN HERTZES
I IN AMPS
TIME IN SECONDS
ELEMENTS
R2, 5-1 = 0.033
R1, 3-1 = 47.
R3, 4-7 = 75.
R3, 6-1 = 25.
C1, 4-8 = TABLE 2 (UC1)
C3, 9-4 = TABLE 2 (UC2)
C3, 7-1 = 5.E-12
C4, 4-8 = 0.2E-12
C5, 4-1 = 0.2E-12
L1, 8-6 = 2.E-9
L3, 9-1 = 2.E-9
J1, 1-3 = 0.09
JDI, 4-8 = DIODE EQUATION(1.E-7, 38.7)
JDB, 9-4 = DIODE EQUATION(1.E-7, 38.7)
RTI, 4-8 = TABLE 1 (TIME)
RTB, 5-1 = TABLE 3 (TIME)
OUTPUTS
UCJ, RTI, JDI, UC2, UCS, PLOT
FUNCTIONS
TABLE 1
0.E-12, 100.E3
100.E-12, 100.E3
200.E-12, 100.E3
300.E-12, 10.E3
400.E-12, 1000.
500.E-12, 100.
600.E-12, 100.
1000.E-12, 100.
TABLE 2
-4.0, 0.5E-12
-2.0, 0.5E-12
-1.0, 0.6E-12
-0.5, 0.7E-12
0.0, 0.85E-12
0.5, 0.85E-12
TABLE 3
0.E-12, 100.
100.E-12, 100.
200.E-12, 100.
300.E-12, 1000.
400.E-12, 10.E3
500.E-12, 100.E3
600.E-12, 100.E3
INITIAL CONDITIONS
I12 = 1.E57
I13 = 1.E17
UC2 = 0.315
UC3 = 0.815
UC4 = 0.315
UC5 = 0.815
RUN CONTROLS
INTEGRATION ROUTINE = RUK
STOP TIME = 1000.E-12
PLOT INTERVAL = 5
END
END OF FILE
77 END, RFPG10B, RL
RFPG10B REPLACED
RFPG10B IS A LOCAL FILE
/SUBMIT, RFPG10B
12.06.04, ASKICKO
/ENQUIRE, JIN=CKO
/ASKICKO EXECUTING.
/ENQUIRE, JIN=CKO
/ASKICKO NOT FOUND.

```

Figure 4-14. Listing of SCEPTRE program RFPG10.

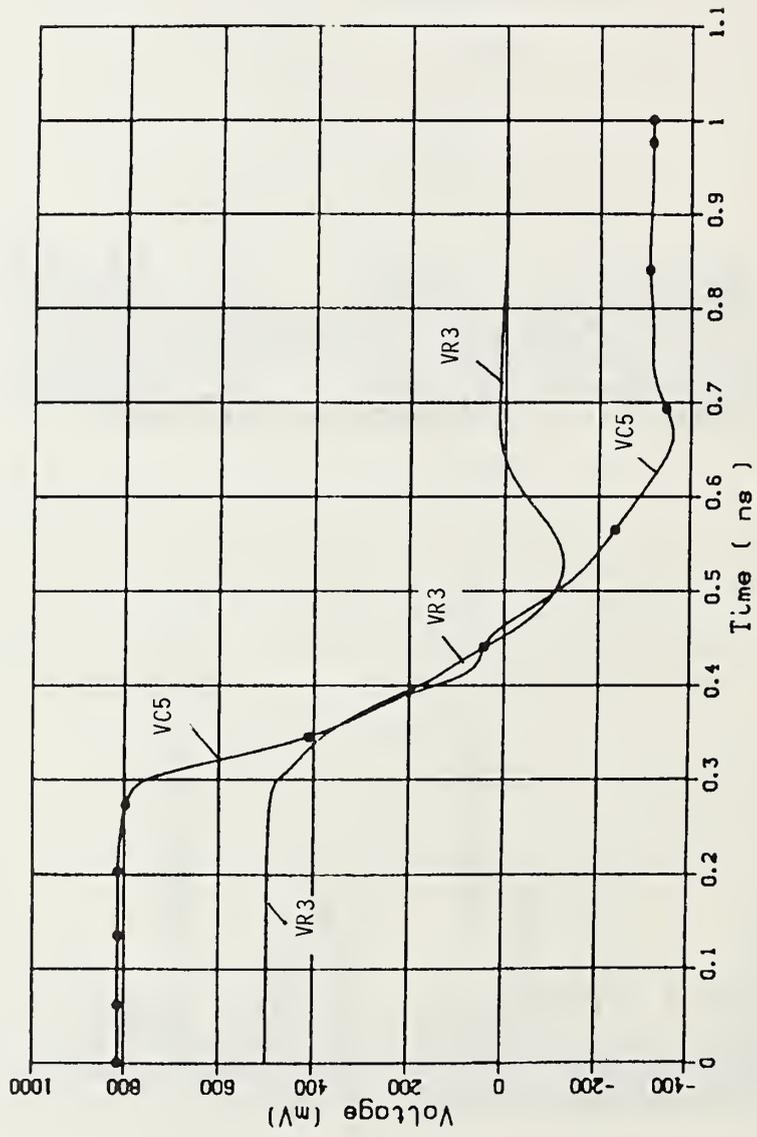


Figure 4-15. Output voltage (VR3) and driving node voltage (VC5) from RFP610 program.

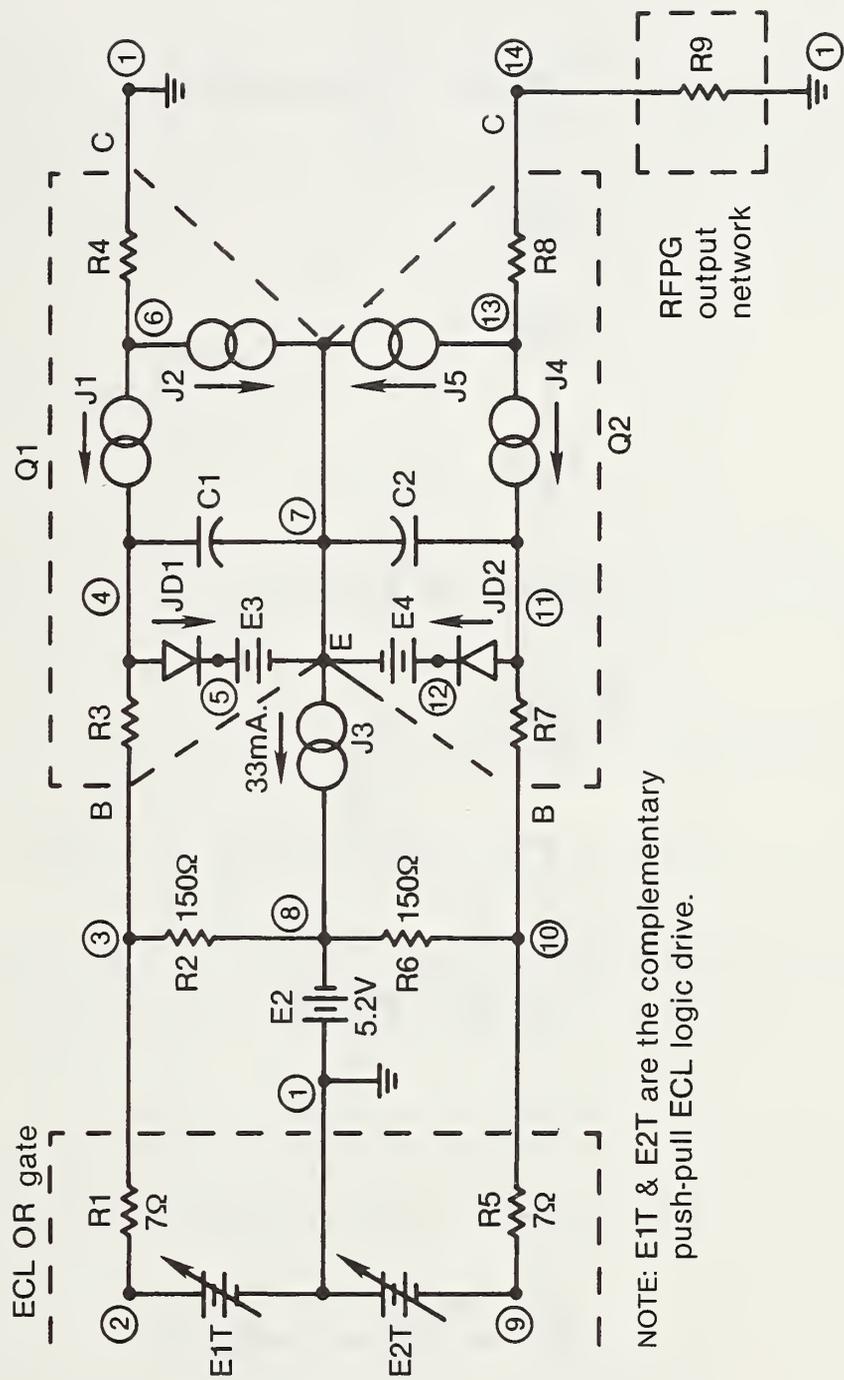


Figure 4-16. TRANG program model for $Q_1 - Q_2$ switching simulation.

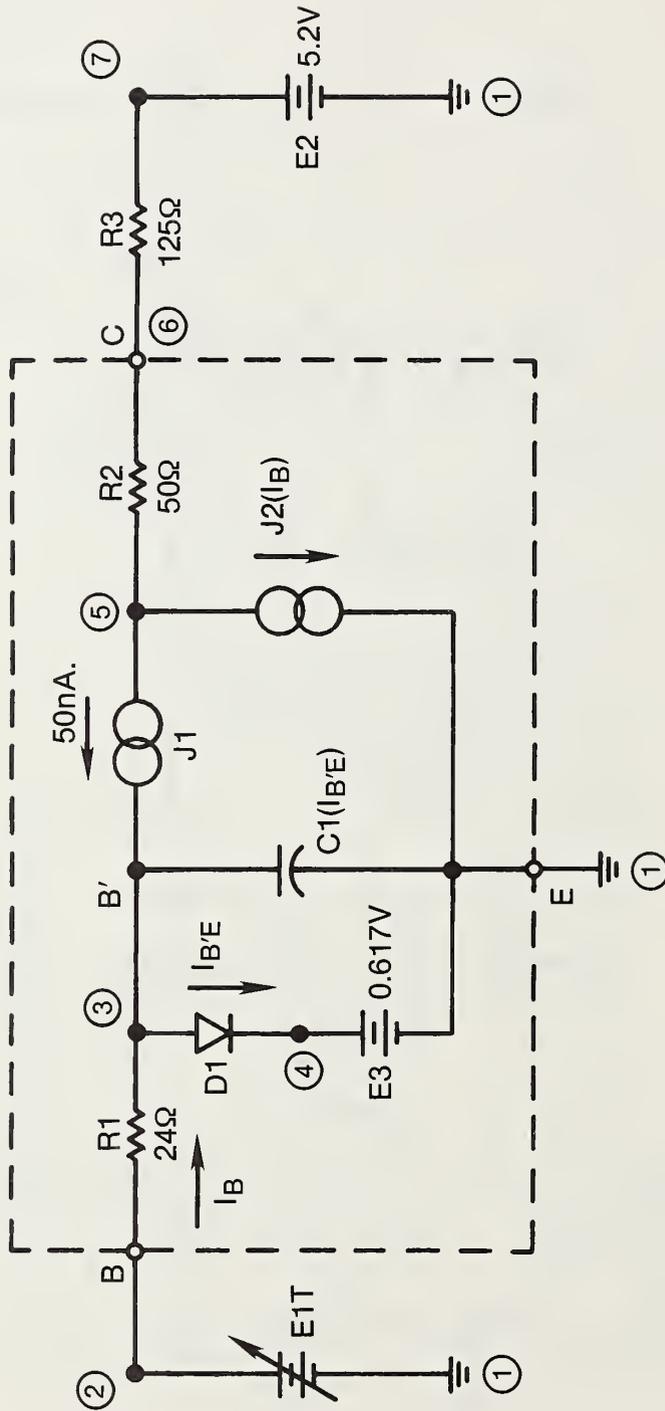


Figure 4-17. Modified Geller, Mantek, and Boyle (GMB) model for the BFR 90 rf transistor.

$$I_{B'E} = I_0 \left[\exp^{\theta(V_{B'E} - E3)} - 1 \right] \quad (8)$$

so that

$$\frac{1}{r_{B'E}} = \frac{dI_{B'E}}{dV_{B'E}} = \theta(I_{B'E} + I_0), \quad (9)$$

where $\theta = e/kT = 38.7$ at $T = 300$ K, I_0 is the base-emitter reverse saturation current, and $E3$ is an offset voltage described below. It is well known that when the junction transistor is switched by means of a large step of base-current, but does not saturate, the collector current is approximately an exponential function of time [16]. The nonlinear GMB model shown in figure 4-17 simulates this type of response by means of the time constant,

$$\tau_{B'} = r_{B'E} C1 \quad (10)$$

which is considered to be invariant over the entire base current excursion. Consequently, $C1$ is seen to be a function of the nonlinear base-emitter current, since

$$C1 = \frac{\tau_{B'}}{r_{B'E}} = \theta \tau_{B'} (I_{B'E} + I_0). \quad (11)$$

Although the nonlinear network elements are constrained to maintain $\tau_{B'}$ invariant, the dynamic impedance seen looking into the base-emitter terminals is continuously variable during the resulting transient, as described in reference 15. Appendix C describes the measurement set-up and data taken for determining an estimated value of $\tau_{B'}$ for the BFR 90 transistor.

The forward-biased, base-emitter diode is thus modeled as before, except for an offset voltage $E3 = 0.617$ V, which was determined by measurement of the BFR 90 base-emitter I-V characteristics, as shown in figure 4-18. For the ideal diode (see fig. 4-2),

$$V_D = \frac{1}{\theta} \ln \left[\frac{I_D}{I_0} + 1 \right]. \quad (12)$$

Increasing the vertical scale (current sensitivity) in figure 4-18 shows that at $I_B = 10 \mu\text{A}$, $V_{BE} \cong 730$ mV. Using $\theta = 38.7$ as before and $I_0 = 126$ mA (average of reverse saturation current readings taken with Keithley Model 150A nanoammeter), then

$$V_D = \frac{1}{38.7} \ln \left[\frac{10,000}{126} + 1 \right] \cong 113 \text{ mV}.$$

By neglecting the voltage drop of I_B through the bulk resistance $r_{BB'}$ at the $10 \mu\text{A}$ level (see fig. 4-19), then

$$E3 = E_{\text{OFFSET}} = V_{BE} - V_D = 730 - 113 = 617 \text{ mV}.$$

The general expression for the static base-emitter I-V characteristic is given by

$$V_{BE} = I_b r_{BB'} + V_D + E_{\text{OFFSET}} \quad (13)$$

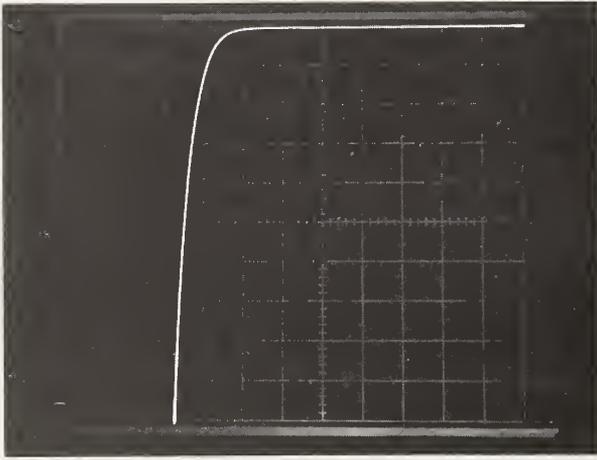


Figure 4-18. Typical BFR 90 base-emitter I-V characteristic.
 Vertical: 100 $\mu\text{A}/\text{div}$.
 Horizontal: 100 mV/div.
 Collector circuit: $V_{CC} = 4.97 \text{ V}$,
 $R_L = 150 \Omega$.

so that $r_{BB'}$ can be found from rearranging eq (13) and using eq (12) to give

$$r_{BB'} = \frac{V_{BE} - E_{\text{OFFSET}} - V_D}{I_B} = \frac{V_{BE} - E_{\text{OFFSET}} - \frac{1}{\theta} \ln \left[\frac{I_B}{I_0} + 1 \right]}{I_B} \quad (14)$$

At $I_B = 600 \mu\text{A}$, $V_{BE} \cong 850 \text{ mV}$. Hence, for the BFR 90 model,

$$R1 = r_{BB'} = \frac{0.850 - 0.617 - \frac{1}{38.7} \ln \left[\frac{600,000}{126} + 1 \right]}{600 \times 10^{-6}} = 23.6 \Omega.$$

The constant current source J1 in the GMB model is the leakage current of the back-biased collector-base junction, or the collector cutoff current I_{CB0} given as 50 nA in the device specifications [17]. J2 is a secondary dependent current source which is a nonlinear function of the base current I_B . Figure 4-20 shows the common-emitter collector characteristic for typical BFR 90 transistors. For the 100 μA incremental steps of base current, a decreasing increment of collector current is observed. Thus, the I_C/I_B ratio (α_{FE} , or β) depends on current level and is best modeled by means of a typical tabular relationship, as shown below. Finally, R2 in the model is the saturation resistance of the collector characteristic, nominally of value 50 Ω . The saturation and storage time simulation capabilities of the GMB model were not utilized in this development.

Figure 4-21 shows a listing of the TRAN6E program used in conjunction with the SCEPTRE circuit for the ECL drive and transistor switching simulation given in figure 4-16. The approximate ECL voltage drive waveforms for E1T and E2T, as reflected in tables 1 and 3, were determined by observing nodes 3 and 10 with a sampling oscilloscope. Capacitors C1 and C2 are dependent on their respective base-emitter diode currents via eq (11) using $\theta = 38.7$ and $\tau_{B1} = 5 \text{ ns}$. J2 and J5 are the secondary current sources dependent on base currents JD1 and JD2, respectively. The values used in table 2 approximate the I_C/I_B relationship and were taken from corresponding I_B - I_C current values on a 5.2 V, 125 Ω load line drawn on the collector characteristics shown in figure 4-20.

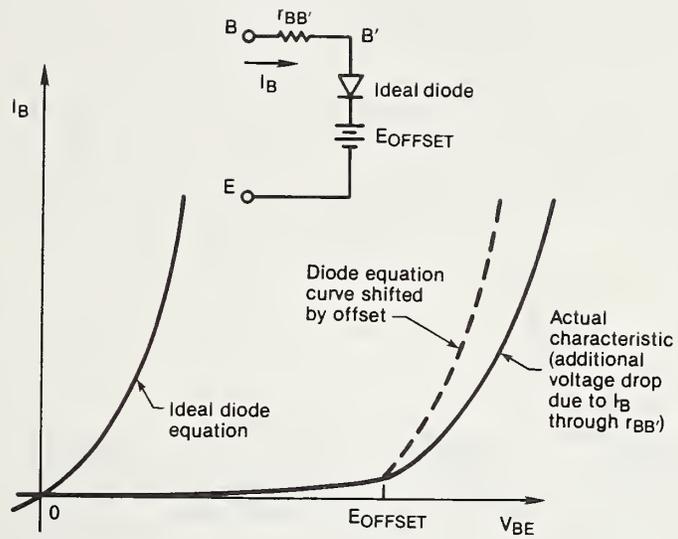


Figure 4-19. Analysis of base-emitter characteristic.

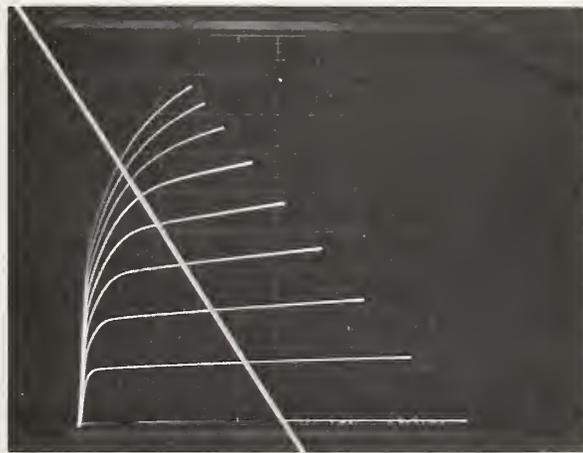


Figure 4-20. Typical BFR 90 common-emitter collector characteristics. Vertical: 5 mA/div. Horizontal: 1 V/div. Base current: 100 μ A/step.

```

TYPE
/108
SCEPTRE(1200)
/READ,USERFIL
/HEADNG,BIBASBCTR
/INSE0
PURGE,TAPEBEL.
GOTO,1.
EXIT.
1,PURGE,TAPE2.
GOTO,2.
EXIT.
2,ATTACH,SUPER/UN=L,LIB,NA.
SUPER.
RETURN,SUPER.
ATTACH,SCEPTR/UN=L,LIB,NA.
SCEPTR.
RETURN,SCEPTR.
FTN,J=TAPEB,A,L=ZBELL.
GET,SCPTR28/UN=L,LIB,NA.
REVIND,TAPEB.
SLIPE,TAPEB.
RETURN,TAPE14,TAPE3,TAPE1,TAPE2,TAPE13,TAPE15,TAPE16.
DEFJNE,TAPE2.
MAP,OFF.
LOAD,SCPTR2B.
LGO.
GOTO,3.
EXIT.
3,REVIND,TAPE2.
RETURN,TAPE1,TAPE3.
DEFJNE,TAPE14=TAPEBEL)
REVIND,TAPE14.
GET,SCPTAPB/UN=BLP.
ATTACH,LIB/UN=L,LIB)
LDSET,LIB=L,LIB)
SCPTAPB.
PURGE,TAPE2.
/EDR
CIRCUIT DESCRIPTION
BFR 88 TRANSISTOR SIMULATION-NETWORK 6E(10/1/81)
E IN VOLTS
R IN OHMS
C IN FARADS
J IN AMPERES
L IN HENRYS
TIME IN SECONDS
ELEMENTS
E1T, 1-2 = TABLE 1 (TIME)
E2T, 1-0 = TABLE 3 (TIME)
E3, 9-1 = 5.2
E4, 7-5 = 0.617
R1, 2-3 = 7
R2, 3-8 = 100.
R3, 3-4 = 24.
R4, 1-6 = 50.
R5, 9-10 = 7.
R6, 10-0 = 100.
R7, 10-11 = 24.
R8, 14-13 = 50.
R0, 1-14 = 130.
R10, 15-8 = 30.3
C1, 4-7 = EQUATION 1 (JD1)
C2, 11-7 = EQUATION 1 (JD2)
C3, 7-10 = 3 E-12
JD1, 4-6 = DIODE EQUATION(126.E-9,36.7)
JD2, 11-12 = DIODE EQUATION(126.E-9,36.7)
J1, 6-4 = 50.E-9
J2, 6-7 = TABLE 2 (JD1)
J3, 7-10 = 0.833
J4, 13-11 = 50.E-9
J5, 13-7 = TABLE 2 (JD2)
OUTPUTS
VC1,VC2,JD1,JD2,J5,VJ3,VR9,PLOT
FUNCTIONS
EQUATION 1 (A) = (193.5E-0*ABS(A))
TABLE 1
0.E-12, -0.850
1000.E-12, -0.850
2000.E-12, -1.276
3000.E-12, -1.503
4000.E-12, -1.503
5000.E-12, -1.503
TABLE 2
-100.E-9, 0.E-6
0.E-6, 0.E-6
1.E-6, 500.E-6
100.E-6, 8.E-3
200.E-6, 14.6E-3
300.E-6, 20.0E-3
400.E-6, 26.E-3
500.E-6, 28.E-3
600.E-6, 32.5E-3
700.E-6, 35.E-3
800.E-6, 35.E-3
900.E-6, 35.E-3
TABLE 3
0.E-12, -1.700
1000.E-12, -1.700
2000.E-12, -1.276
3000.E-12, -0.657
4000.E-12, -0.657
5000.E-12, -0.657
INITIAL CONDITIONS
VC1 = 0.840
VC2 = 0.100
VC3 = 2.45
RUN CONTROLS
INTEGRATION ROUTINE = RUK
STOP TIME = 6000.E-12
PLOT INTERVAL = 5
END OF FILE
??

```

Figure 4-21. Listing of SCEPTRE program TRAN6E.

Figures 4-22, 4-23, 4-24, and 4-25 show the results obtained via program TRAN6E for the ECL drive and transistor switching simulation of figure 4-16. The ECL drive waveform in figure 4-22 approximates the ~ 2 ns logic swing from around -1.7 V to -0.957 V observed for E2T. It can be seen in figure 4-23 that by 2 ns (1 ns after E2T begins to change), the voltage across the base-emitter capacitor, C2, of transistor Q2 has risen up to the 750 mV level. As previously determined from the base-emitter characteristics (see fig. 4-18), appreciable base current now begins to build up in Q2. Figure 4-24 shows the JD2 waveform which peaks at ~ 0.67 mA a little after 3 ns. The corresponding rise in collector current J5 is seen in figure 4-25. Due to the saturation characteristic, J5 flattens out upon reaching the 33 mA level at about 2.8 ns. Thus, as anticipated, the switching action of the BFR 90 transistors (and their associated complementary ECL input drive signals) is to produce a current step-like waveform which has a transition time on the order of 600 ps.

4.5 The Total Model via Program TRFPG

As shown in section 4.3, simple modeling of the output stage of the RFPG produces a simulated output waveform with a much faster transition time and larger undershoot than observed on the actual waveform. Lack of the proper driving node voltage waveform and a slower switching speed on the part of the rf transistors/ECL input drive were likely causes. Section 4.4 above describes the development of a model for the ECL drive and transistor switches (via program TRAN) which confirms the switching speed supposition. To confirm the total model, then, R9 of figure 4-16 is replaced by the initial output stage model of figure 4-13.

Figure 4-26 shows the merging of figures 4-13 and 4-16 used for programs RFPG and TRAN, respectively. Node 15 at the collector of Q2 is now the driving node for the output stage, corresponding to node 4 of figure 4-13. The output diode and load resistor branch is designated by nodes 19 and 20.

Figures 4-27, 4-28, 4-29, and 4-30 show the results of SCEPTRE program TRFPG1, simulating the total RFPG model using the same ECL drive signals as in figure 4-22. Figure 4-27 shows that the collector current J5 is maintained as before in figure 4-25. The voltage produced at node 15 (VC5) is shown in figure 4-28. The output diode current, JD4 is plotted in figure 4-29. The output voltage waveform across R13 is given in figure 4-30, and can be seen to begin now to approximate reality. The step-like output waveform is flat until the driving voltage at node 15 begins to fall at ~ 1.75 ns, which is where J5 begins to turn on. VC5 then decreases at a rate comensurate with the increase of J5. Consequently, as analyzed in section 4.2, diode current JD4 decreases even more rapidly as the output diode becomes reverse-biased into cutoff. As seen in the earlier analysis of the diode-load resistor step response, however, the undershoot observed in the output waveform is highly dependent on the driving node voltage waveform, due to the parasitic reactances and nonlinear properties of the diode.

Modifying the essential parts of the model for the RFPG shown in figure 4-26 so that the simulated waveforms better match the actual waveforms observed, therefore, is a matter of accounting for various parasitic and distributed inductances and capacitances in the circuit which help to shape the driving node voltage waveform. Small lead inductances (in the output circuit diodes and in the connections to the driving node) and small capacitances, particularly associated with the driving point node (node 15 in figure 4-26), have a very pronounced effect. Figure 4-31 shows a model, modified from figure 4-26, which gives a reasonably close approximation to the actual observed waveforms of the RFPG. The additional inductances and capacitances (and their associated values) can be attributed to the actual physical devices and structure used in the construction of the RFPG. For example, appendix D describes an analysis for approximating the value of C9 by knowing the typical value of the

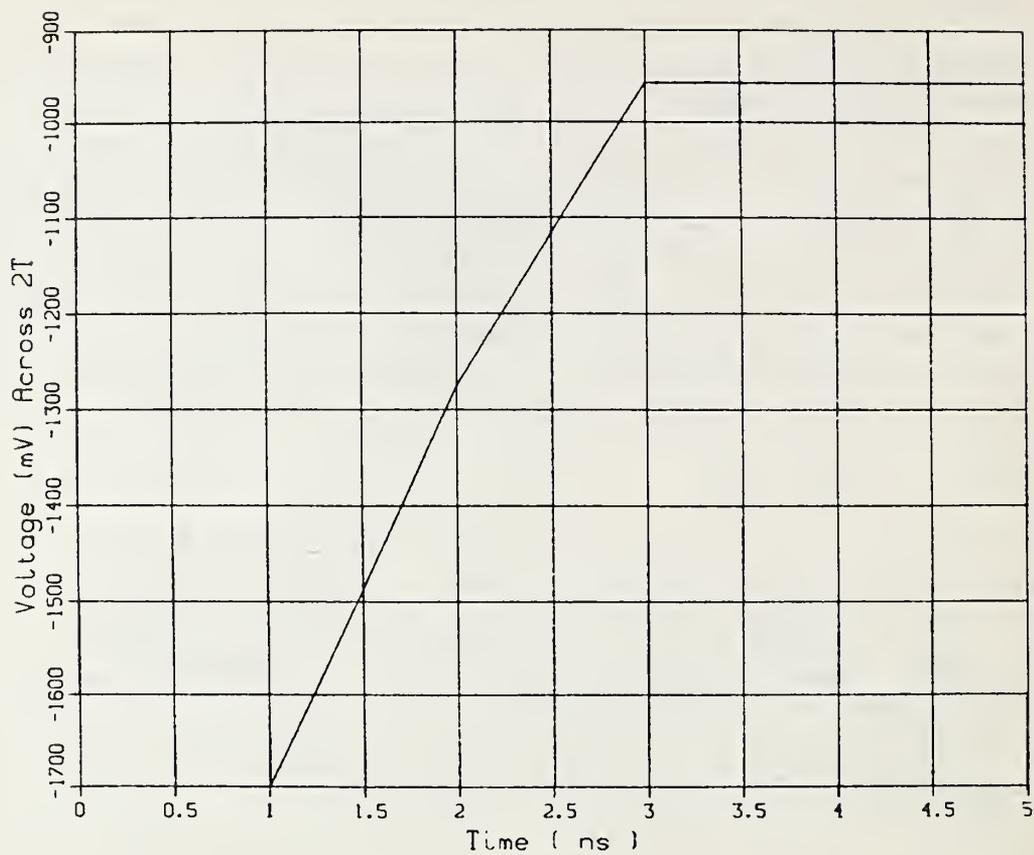


Figure 4-22. ECL drive waveform E2T from TRAN6E program.

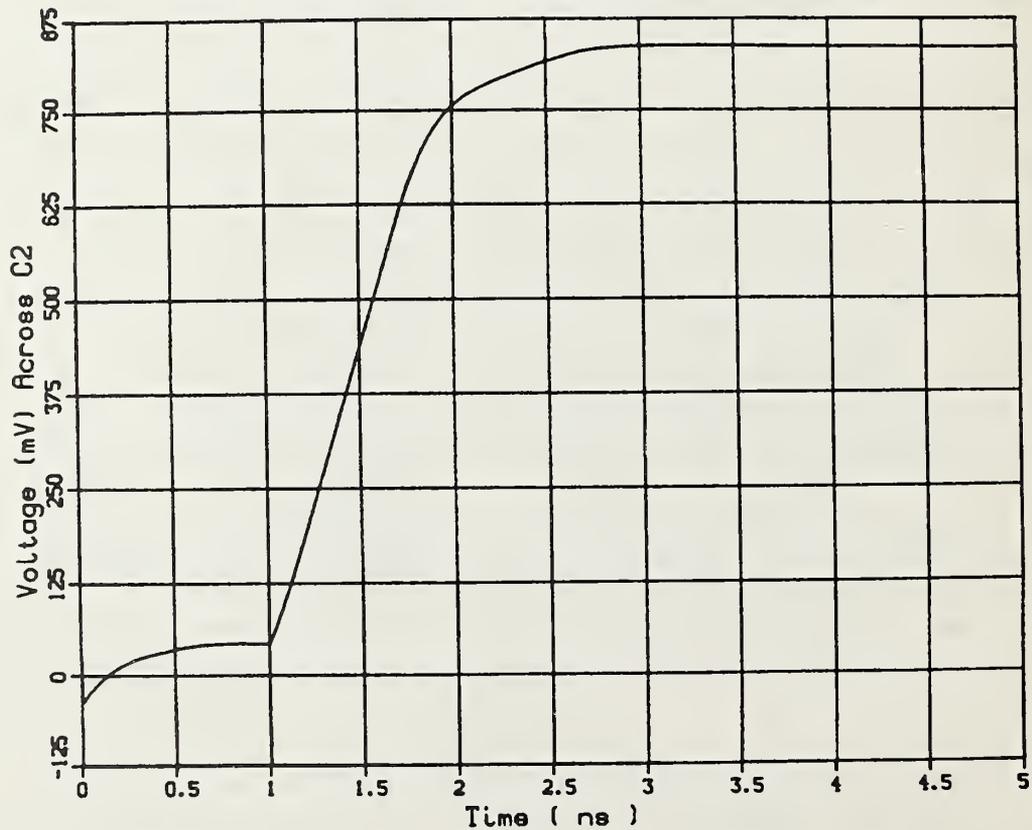


Figure 4-23. Voltage across capacitor C2 in response to E2T (ECL drive waveform of fig. 4-22) from TRAN6E program.

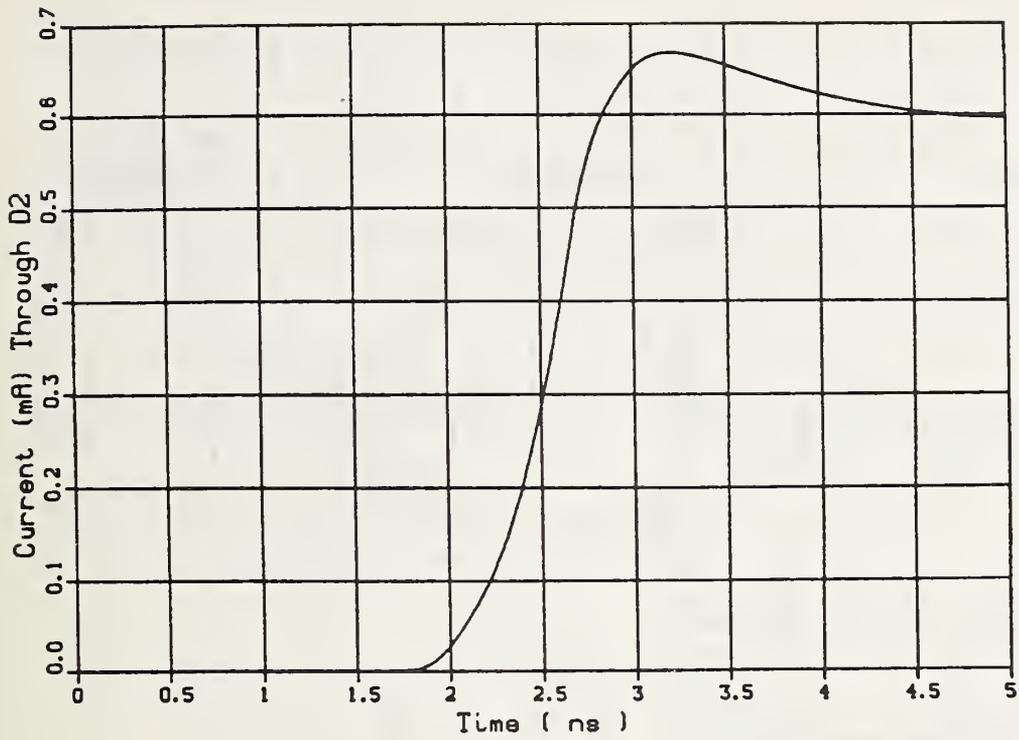


Figure 4-24. Transient current JD2 in response to ECL base drive from TRAN6E program.

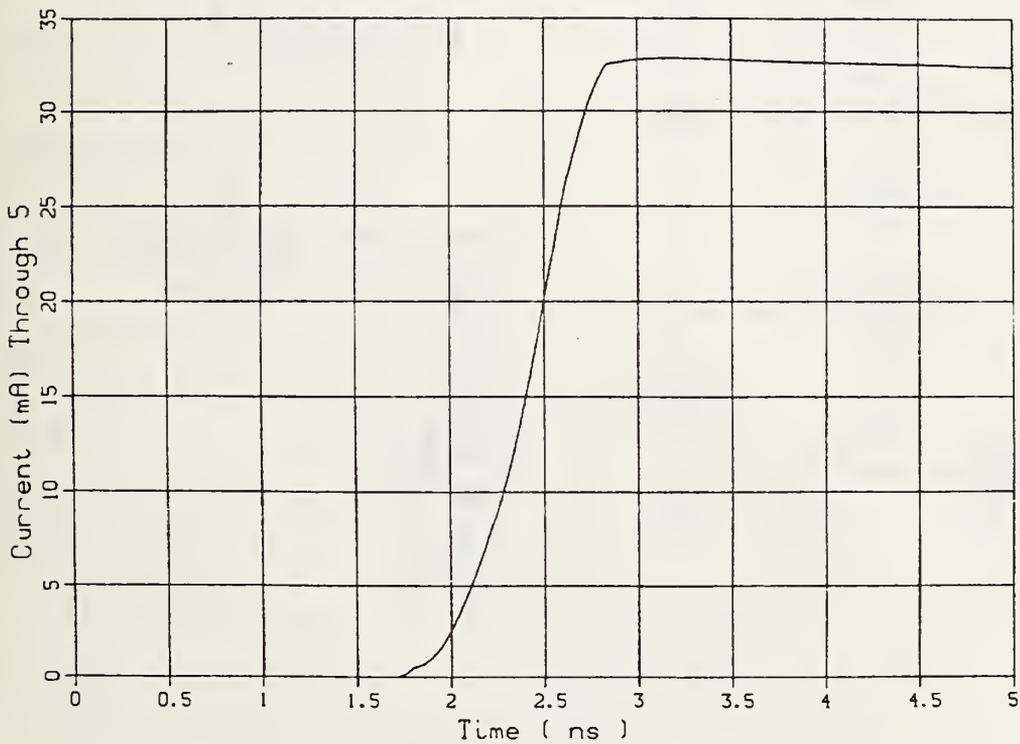


Figure 4-25. Collector current J5 of Q2 from TRAN6E program.

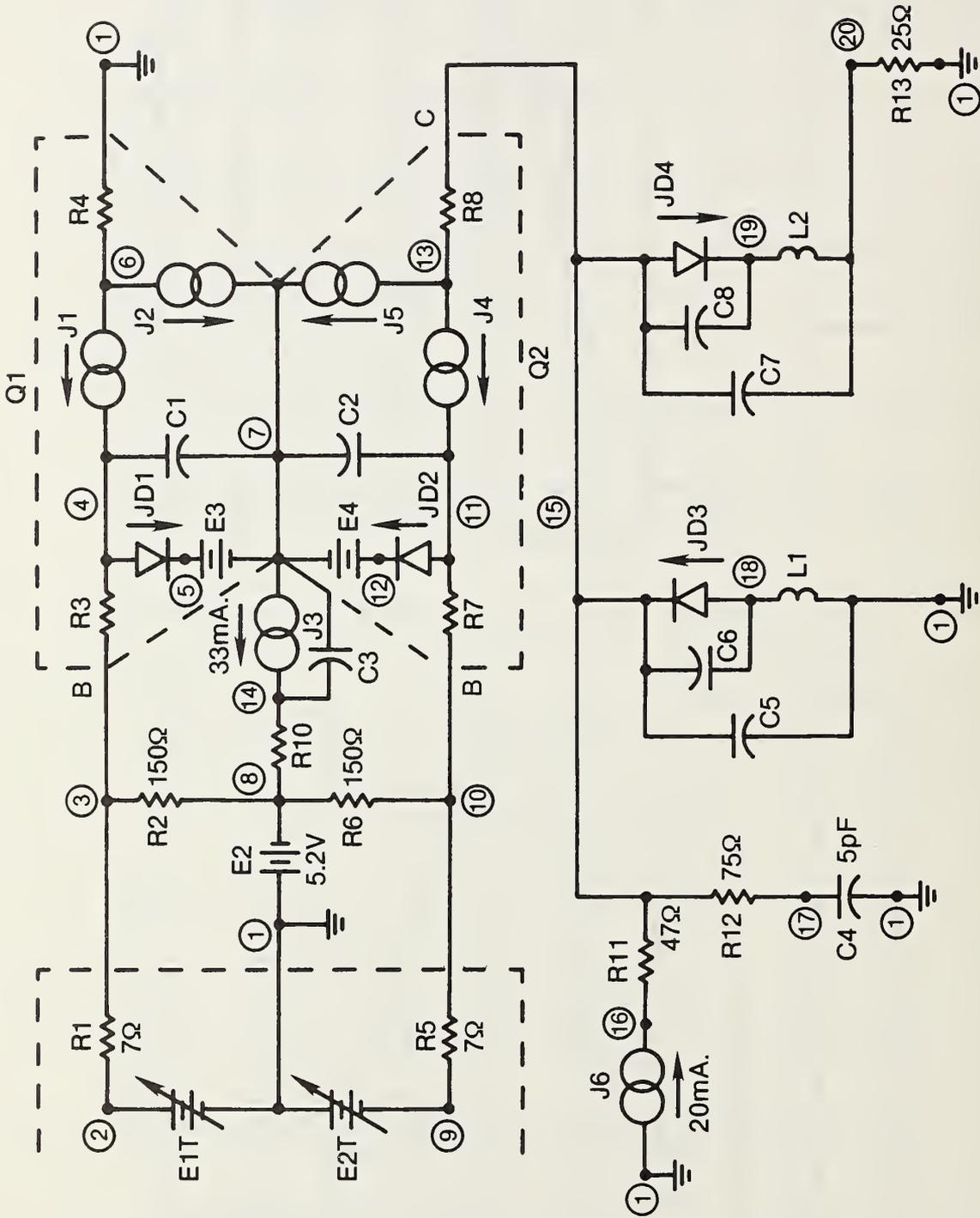


Figure 4-26. TRFPG1 program model.

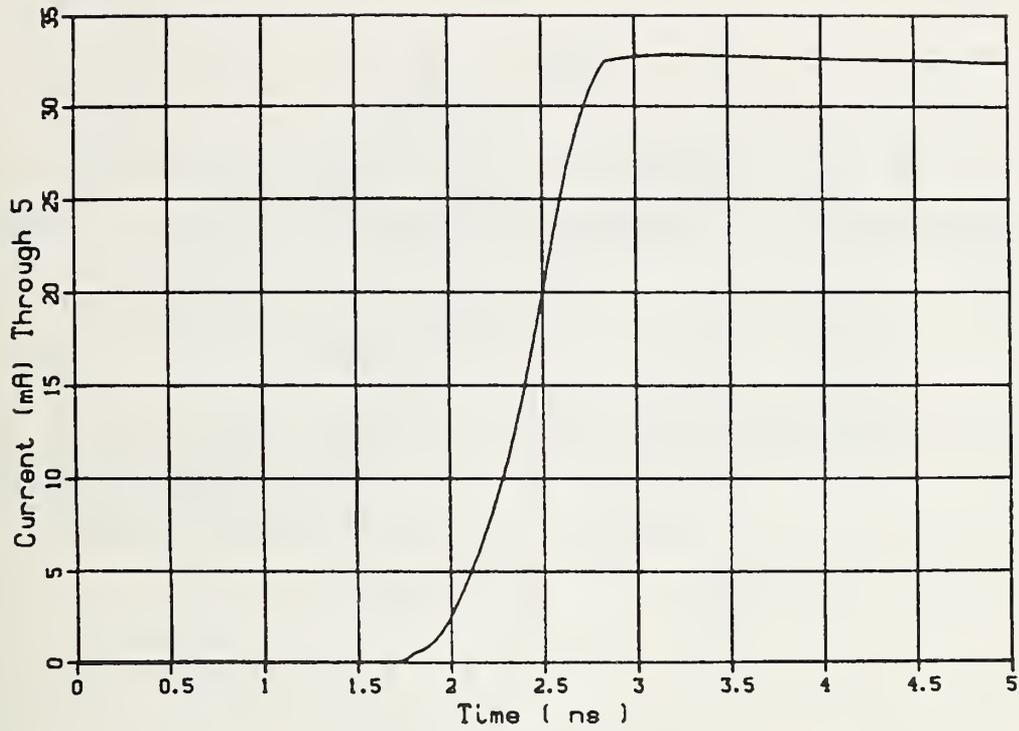


Figure 4-27. Collector current J5 of Q2 from TRFPG1 program.

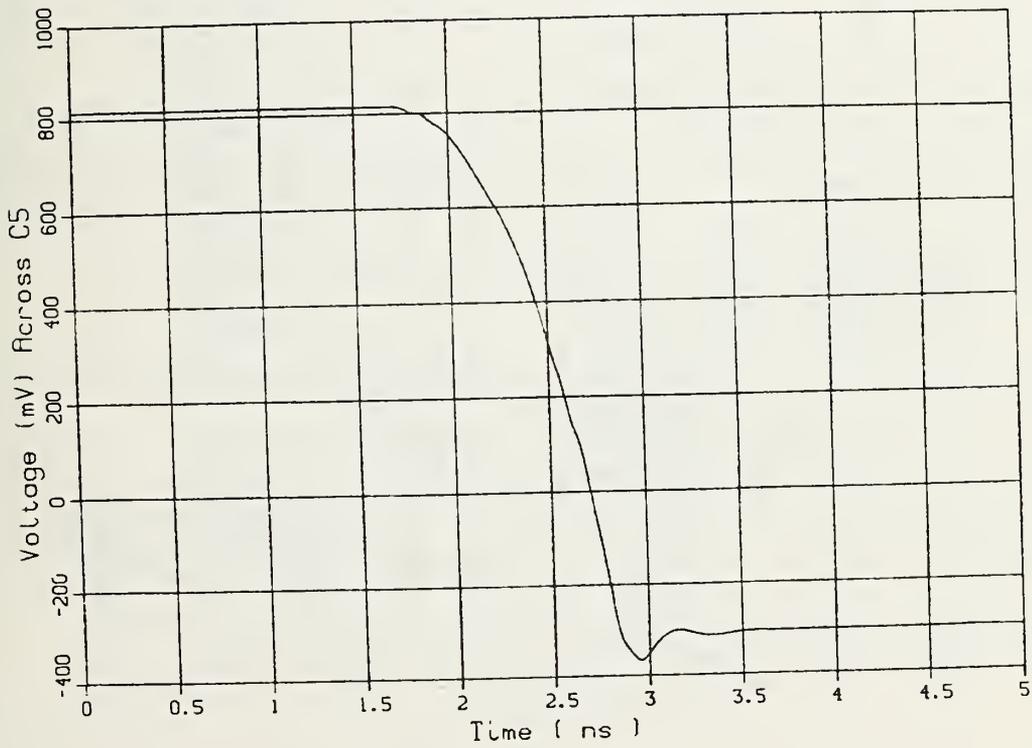


Figure 4-28. Driving node voltage VC5 from TRFPG1 program.

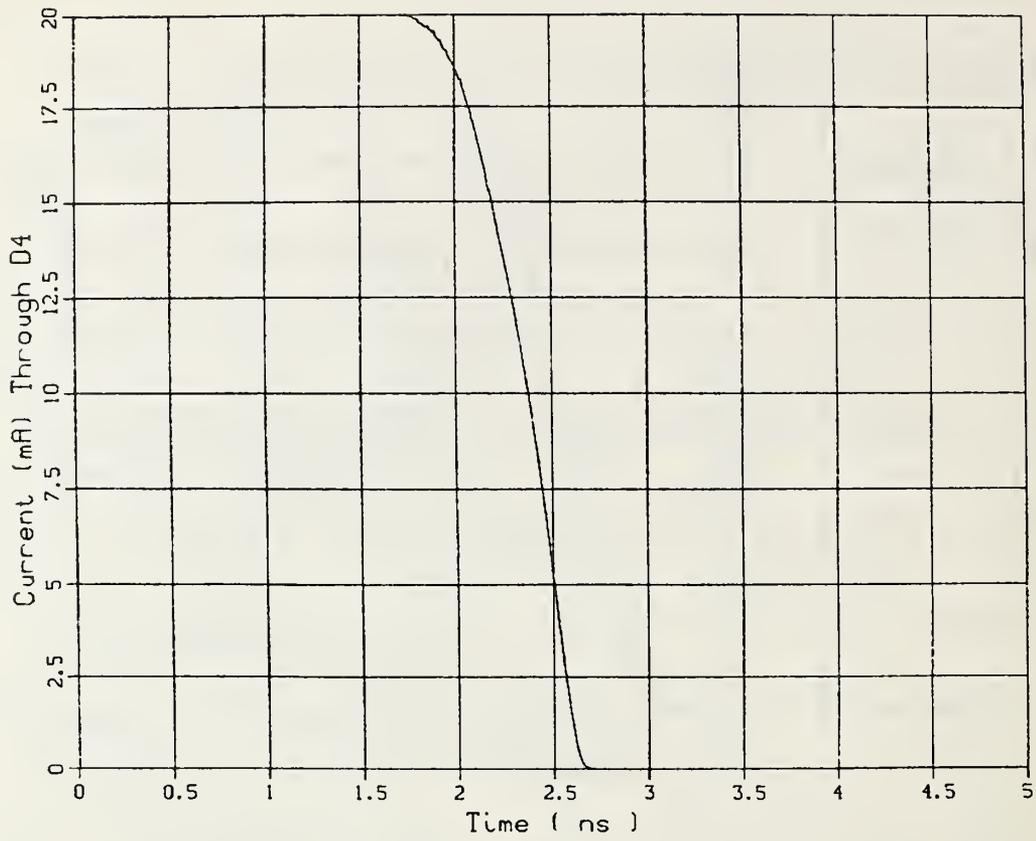


Figure 4-29. Output diode current JD4 from TRFPG1 program.

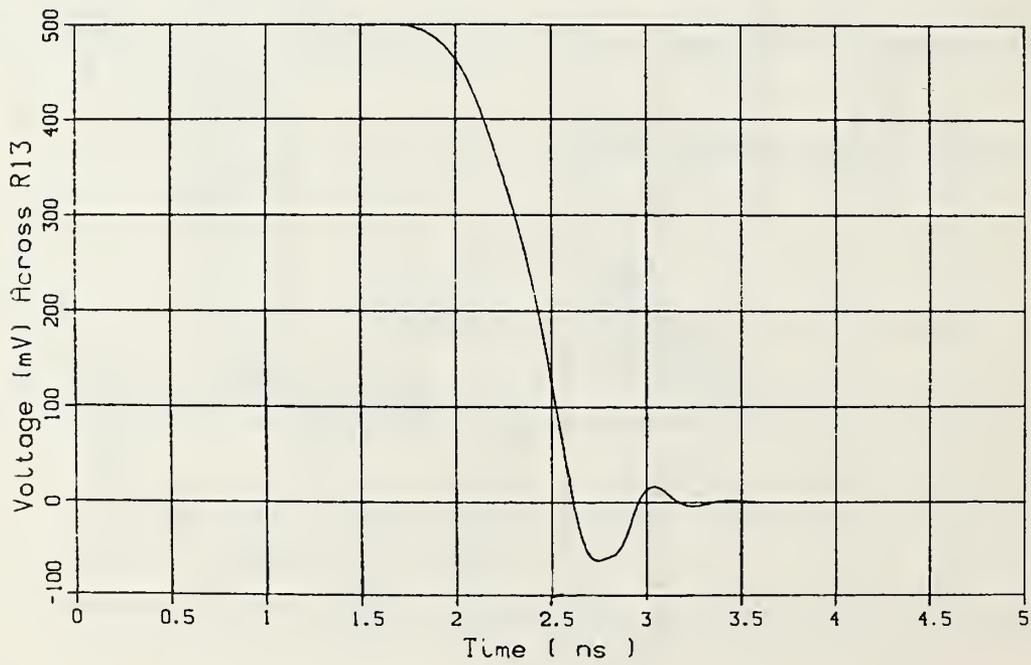


Figure 4-30. Resultant step-like output voltage waveform VR13 from TRFPG1 program.

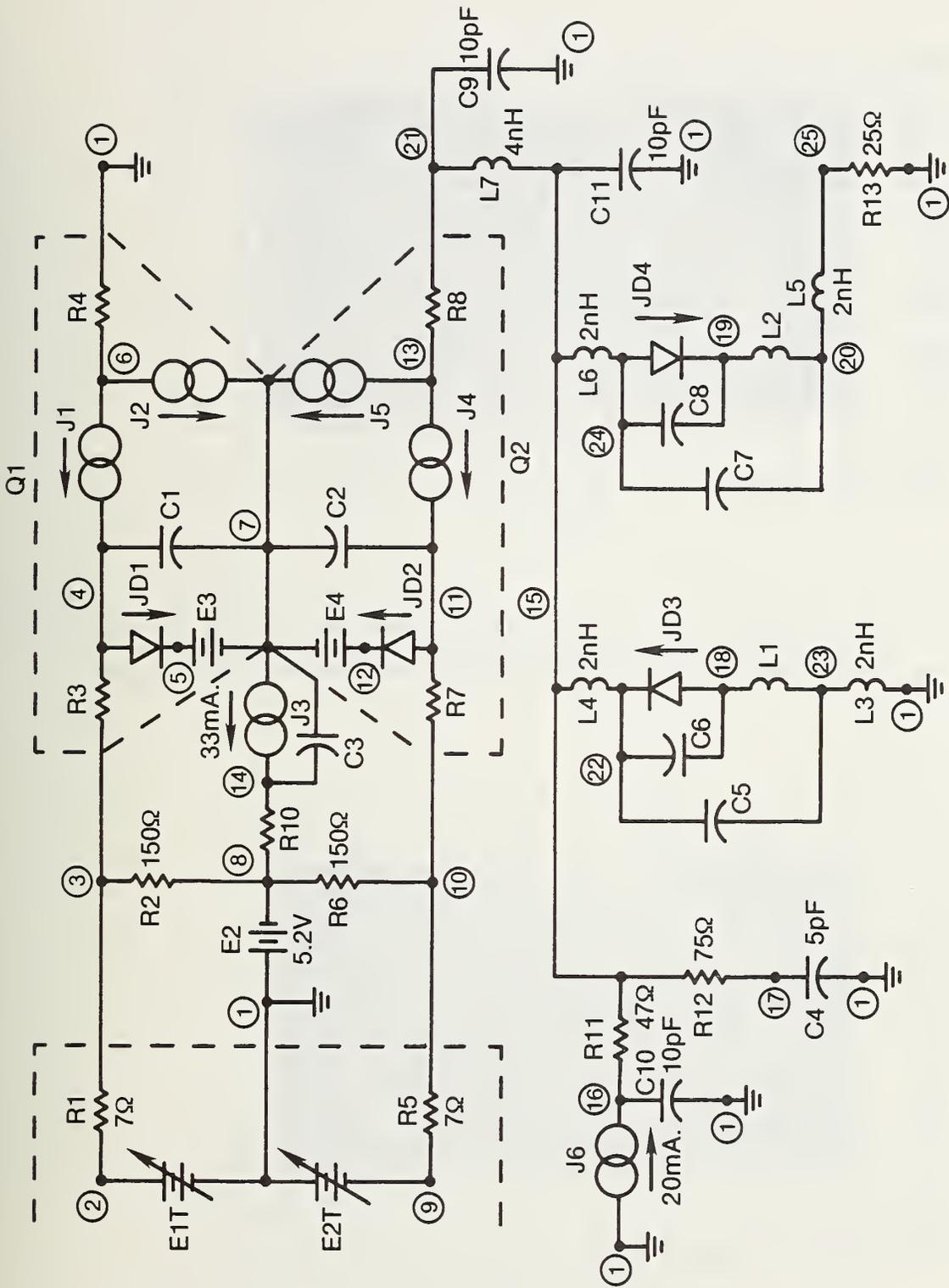


Figure 4-31. TRFPG3 program model.

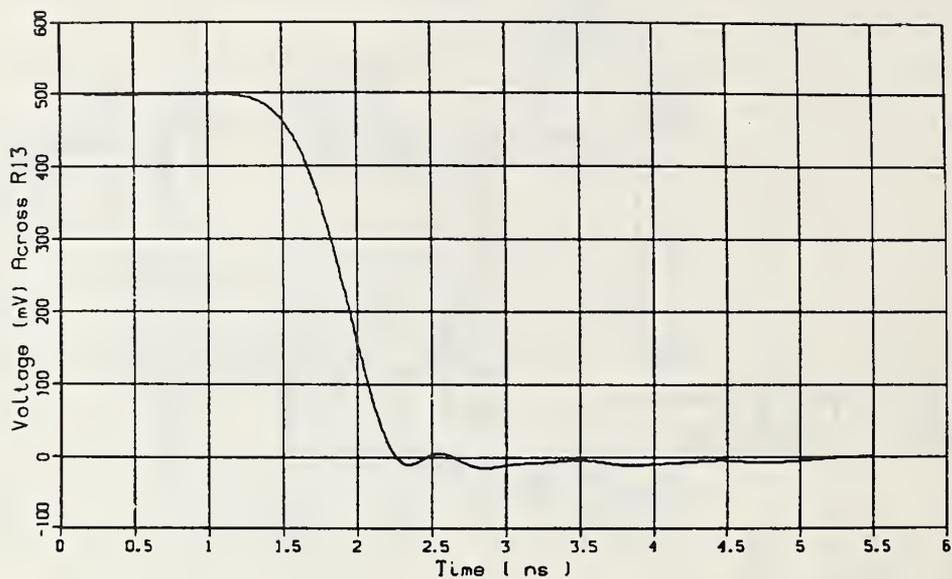


Figure 4-32. Example of predicted available transition waveform from TRFPG3 program.

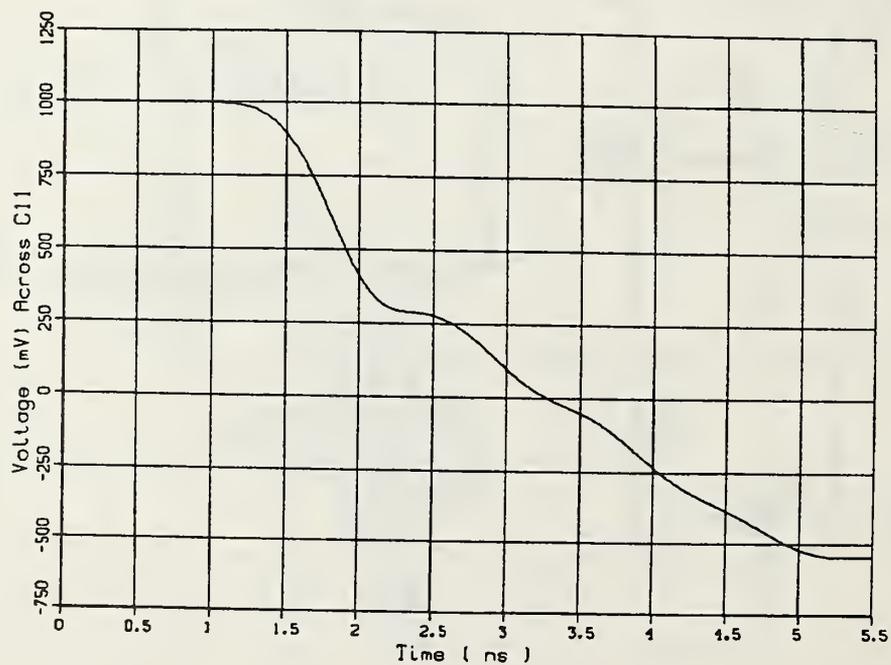


Figure 4-33. Example of corresponding driving node voltage from TRFPG3 program.

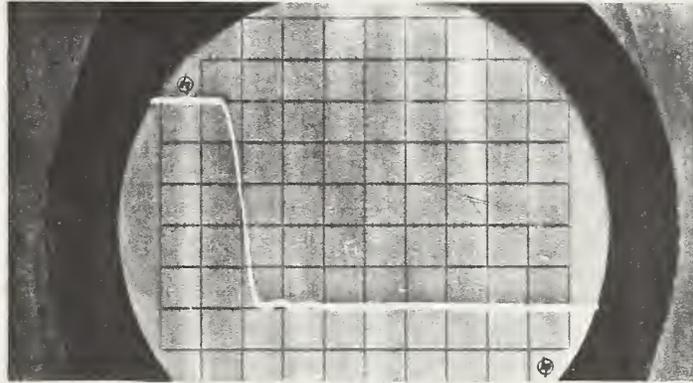


Figure 4-34. Actual output waveform from the RFPG observed with a sampling oscilloscope. Vertical: 100 mV/div. Horizontal: 1 ns/div.

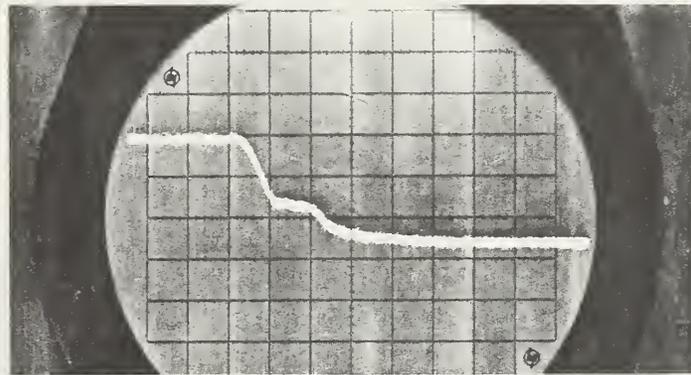


Figure 4-35. Actual driving node voltage waveform from the RFPG observed with a sampling oscilloscope. Vertical: 500 mV/div. Horizontal: 2 ns/div.

TRFPG3

```

/JOBS
SCEPTRE(IT200)
/READ,USERFIL
/HEAD,818ABSCPTR
/NOSED
PURGE,TAPEBEL.
GOTO,1.
EXIT
1.PURGE,TAPE2.
GOTO,2.
EXIT
2.ATTACH,SUPER/UN=LJB,NA.
SUPER
RETURN,SUPER
ATTACH,SCEPTR/UN=LJB,NA.
SCEPTR.
RETURN,SCEPTR.
FTN,J=TAPE6,A,L=ZBELL.
GET,SCPTR2B/UN=LJB,NA
REVIND,TAPE8.
SKIPF,TAPE8.
RETURN,TAPE14,TAPE3,TAPE1,TAPE2,TAPE13,TAPE15,TAPE16
DEFINE,TAPE2.
MAP,OFF.
LOAD,SCPTR2B.
LGO.
GOTO,3.
EXIT
3.REVIND,TAPE2
RETURN,TAPE1,TAPE3
DEFINE(TAPE14=TAPEBEL)
REVIND,TAPE14
GET,SCPTAB/UN=BLP
ATTACH(LIB=LIB)
LDSET(LIB=LJB)
SCPTAB
PURGE,TAPE2
/EOB
CIRCUIT DESCRIPTION
TOTAL REF FLAT PULSE GENERATOR-NETWORK 3(11/24/81)
E IN VOLTS
R IN OHMS
C IN FARADS
J IN AMPERES
L IN HENRYS
TIME IN SECONDS
ELEMENTS
E11, 1-2 = TABLE 1 (TIME)
E21, 1-0 = TABLE 3 (TIME)
E3, 7-5 = 0.617
E4, 7-12 = 0.617
R1, 2-3 = 7
R2, 3-8 = 150.
R3, 3-4 = 24.
R4, 1-6 = 50.
R5, 9-10 = 7
R6, 10-0 = 150.
R7, 10-11 = 24.
R8, 21-13 = 50.
R9, 1-14 = 130.
R10, 14-8 = 30.3
R11, 16-15 = 47.
R12, 15-17 = 75.
R13, 25-1 = 25.
C1, 4-7 = EQUATION 1(JD11)
C2, 11-7 = EQUATION 1(JD2)
C3, 7-14 = 3.E-12
C4, 17-1 = 5.E-12
C5, 22-23 = 0.2E-12
C6, 18-22 = TABLE 4(VC6)
C7, 24-20 = 0.2E-12
C8, 24-10 = TABLE 4(VC8)
C9, 21-1 = 10.E-12
C10, 16-1 = 10.E-12
C11, 15-1 = 10.E-12
L1, 10-20 = 2.0E-9
L2, 10-20 = 2.0E-9
L3, 23-1 = 2.0E-9
L4, 15-22 = 2.0E-9
L5, 20-25 = 2.0E-9
L6, 15-24 = 2.0E-9
L7, 15-21 = 4.0E-9
JD1, 4-5 = D10DE EQUATION(126,E-9,38.7)
JD2, 11-12 = D10DE EQUATION(126,E-9,38.7)
JD3, 18-22 = D10DE EQUATION(126,E-9,38.7)
JD4, 24-10 = D10DE EQUATION(11,E-7,24.4)
J1, 6-4 = 50.E-9
J2, 6-7 = TABLE 2 (JD1)
J3, 7-14 = 0.033
J4, 13-11 = 50.E-9
J5, 13-7 = TABLE 2 (J02)
J6, 1-16 = 0.02
OUTPUTS
YR13,VC11,JD4,IL2,IC8,PLOT
FUNCTIONS
EQUATION 1(A) = ((116.1E-9*ABS(A)))
TABLE 1
0.E-12, -0.850
100.E-12, -0.850
1100.E-12, -1.275
2100.E-12, -1.503
4000.E-12, -1.503
5000.E-12, -1.503
TABLE 2
-150.E-9, 0.E-6
0.E-6, 0.E-6
1.E-6, 500.E-6
100.E-6, 8.E-3
200.E-6, 14.6E-3
300.E-6, 20.0E-3
400.E-6, 26.E-3
500.E-6, 20.E-3
600.E-6, 32.5E-3
700.E-6, 33.E-3
800.E-6, 33.E-3
TABLE 3
0.E-12, -1.700
1100.E-12, -1.275
2100.E-12, -0.657
4000.E-12, -0.657
5000.E-12, -0.957
TABLE 4
-4.0, 0.5E-12
-2.0, 0.55E-12
-1.0, 0.6E-12
-0.5, 0.7E-12
0.0, 0.85E-12
0.5, 0.85E-12
INITIAL CONDITIONS
VC1 = 0.840
VC2 = 2.45
VC3 = 2.45
VC4 = 1.0
VC5 = 1.0
VC6 = -1.0
VC7 = 0.50
VC8 = 0.50
VC9 = 1.0
VC10 = 1.940
VC11 = 1.E-7
IL1 = 1.E-7
IL2 = 0.02
IL3 = 1.E-7
IL4 = 1.E-7
IL5 = 0.02
IL6 = 0.02
IL7 = 1.E-7
RUN CONTROLS
INTEGRATION ROUTINE = RUK
STOP TIME = 10500.E-12
PLOT INTERVAL = 5.
END OF FILE
??

```

Figure 4-36. Listing of SCEPTRE program TRFPG3.

collector-base capacitance of the BFR 90 transistor. The value of C11, on the other hand, is an approximation of the effective capacitance to ground at the driving point node where the leads of Q2, R11, R12, and the two current steering diodes are all connected together in a relatively large solder joint. The nanohenry values for L3-L7 are best estimates. Obviously, the better these parasitic and distributed L-C values can be determined (by measurements or by calculations), the more exactly this model can be made to approximate the actual waveforms of the RFPG.

Figure 4-32 shows an example of the predicted available transition waveform of the RFPG produced by SCEPTRE program TRFPG3 in which the estimates of the above parasitic elements have been included. Figure 4-33 is an example of the corresponding driving node voltage produced by the same program. These simulated waveforms can be compared with the actual corresponding waveforms shown in figures 4-34 and 4-35, measured with a commercial sampling oscilloscope. The similarities between the simulated and observed waveforms are quite apparent, taking the different vertical and horizontal scales into account. However, additional work remains to determine the exact error function between the simulated and observed available transition waveforms, and thereby to improve the present model for the RFPG. Figure 4-36 gives the listing of the SCEPTRE program TRFPG3.

5. Summary

This technical note contains the theory, circuit design, performance specifications, modeling, and computer simulations which describe the NBS Reference Flat Pulse Generator (RFPG). Prior methods used for generating flat baseline and topline pulse generators are discussed, together with their limitations. The present approach used in the RFPG, i.e., steering constant current sources to the load via a fast Schottky barrier diode, is thoroughly described. A complete circuit diagram and description is given for the clock, delay, and pulse duration logic, the current-switching output stages, and the regulated power supplies.

A considerable portion of the report is used to present the development of the circuit analysis programs for the RFPG, written using extended-SCEPTRE hosted on a large computer system. The circuit analysis of the nonlinear step response of a simple diode and series load resistor is used as the basis for examining and evaluating the results obtained for the more complex switching structure of the RFPG. These analyses show that the available transition waveform from the RFPG is also highly dependent on the characteristics of the rf switching transistors used and the associated ECL logic drive, as well as parasitic and distributed inductances and capacitances in the output stage of the RFPG.

Finally, it is recommended that the efforts needed to determine a more exact error function between the simulated and observed waveforms be pursued. This work can provide the basis for an improved model of the NBS RFPG by which to predict its performance when used as a pulse waveform generator standard in either the laboratory or as a dynamic transport standard for field testing purposes.

The authors would like to acknowledge the helpful comments and guidance provided by other members of the NBS technical staff in the development and modeling of the Reference Flat Pulse Generator, including N. S. Nahman, R. A. Lawton, and R. L. Peterson. The efforts of the NBS clerical staff in preparing this report are also gratefully acknowledged, including M. E. DeWeese and P. J. Rice.

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b. IEEE standard, IEEE std. 181-
c. International Electrotechnical Commission publication 469-1 and 2, 1974. Part 1: Pulse terms and definitions. Part 2: Pulse measurement and analysis, general consideration.
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Appendix A. Flat Pulse Generator Parts List

Integrated Circuits

IC1	E.C.L.	NOR gate	95H03
IC2	"	divider	95H90
IC3	"	"	95H90
IC4	"	"	95H90
IC5	"	"	95H90
IC6	"	NOR gate	95H03
IC7	"	Flip-flop	95H28
IC8	"	"	95H28
IC9	"	"	95H28
IC10	"	Divider	95H90
IC11	"	"	95H90
IC12	"	"	95H90
IC13	"	NOR gate	95H03
IC14	"	"	95H03
IC15	Reference voltage source		LM-399H
IC16	Precision op-amp		OP-05C
IC17	"		OP-05C
IC18	Voltage regulator +15 V		7815
IC19	"	" +12 V	7812
IC20	"	" -5 V	7905
IC21	"	" -5 V	7905
IC22	"	" -5 V	7905

Transistors

Q1	BFR90
Q2	BFR90
Q3	2N3904
Q4	BFR90
Q5	BFR90
Q6	2N3904
Q7	2N4250
Q8	2N3906
Q9	2N4250
Q10	2N3906

Diodes

CR1	Light emitting	HP-5082-4484
CR2	Schottky diode	HP-2835
CR3	" "	HP-2835
CR4	Light emitting	HP-5082-4484
CR5	Schottky diode	HP-2835
CR6	" "	HP-2835
CR7	Rectifier, General-Purpose	IN4004

Diodes, cont.	CR8	Rectifier, General-Purpose	IN4004
	CR9	" "	"
	CR10	" "	"
	CR11	" "	"
	CR12	" "	"
	CR13	Zener diode	IN5240
	CR14	Zener "	IN5240
	CR15	Light emitting	HP-5082-4484

Resistors--±5% tolerance unless noted otherwise

R1	Composition	51 Ω 1/4 W
R2	"	51 Ω 1/4 W
R3	"	51 Ω 1/4 W
R4	"	680 Ω 1/4 W
R5	"	33 Ω 1/4 W
R6	"	47 Ω 1/4 W
R7	OSM termination	50 Ω
R8	Selected, used only if needed	
R9	Composition	680 Ω 1/4 W
R10	"	33 Ω 1/4 W
R11	"	47 Ω 1/4 W
R12	OSM termination	50 Ω
R13	Selected, used only if needed	
R14	Composition	1 KΩ
R15	Glass film	4.75 K 1%
R16	Trimmer, multi-turn	1 KΩ
R17	"	1 KΩ
R18	Carbon film	1.82 KΩ 1%
R19	Composition	1.3 KΩ 1/4 W
R20	Precision, wire wound	100 Ω 0.1%
R21	Composition	1.3 KΩ 1/4 W
R22	Precision, wire wound	100 Ω 0.1%
R23	Not assigned	
R24	" "	
R25	Wire wound	1 KΩ 2 W
R26	Composition	180 Ω 1/4 W
R27	"	100 Ω 1/4 W
R28	"	75 Ω 1/8 W
R29	"	150 Ω 1/4 W
R30	"	150 Ω 1/4 W
R31	"	220 Ω 1/4 W
R32	"	150 Ω 1/4 W
R33	"	150 Ω 1/4 W
R34	"	75 Ω 1/8 W
R35	"	220 Ω 1/4 W
R36	"	100 Ω 1/4 W

Capacitors

C1	Disk ceramic	0.001 μ F
C2	Silver mica	270 pF
C3	Silver mica	270 pF
C4	Silver mica	33 pF
C5	Trimmer	1.8-13 pF
C6	Silver mica	50 pF
C7	Trimmer	15-60 pF
C8	"	15-60 pF
C9	Silver mica	50 pF
C10	Trimmer	15-60 pF
C11	Disk ceramic	0.001 μ F
C12	Unassigned	
C13	Silver mica	3 pF
C14	Disk ceramic	0.001 μ F
C15	Unassigned	
C16	Silver mica	3 pF
C17	Ceramic	1 μ F, 25 V
C18	"	1 μ F, 25 V
C19	Electrolytic	100 μ F, 25 V
C20	"	100 μ F, 25 V
C21	Disk ceramic	0.01 μ F, 100 V
C22	Electrolytic	100 μ F, 25 V
C23	Disk ceramic	0.01 μ F, 100 V
C24	Electrolytic	(2) 1000 μ F, 25 V
C25	Tantalum	1 μ F, 35 V
C26	Electrolytic	100 μ F, 25 V
C27	Disk ceramic	0.05 μ F
C28	Electrolytic	(2) 1000 μ F, 25 V
C29	Tantalum	1 μ F, 35 V
C30	Electrolytic	100 μ F, 25 V
C31	Disk ceramic	0.05 μ F
C32	Electrolytic	(2) 1000 μ F, 25 V
C33	Tantalum	1 μ F, 35 V
C34	Electrolytic	100 μ F, 25 V
C35	Disk ceramic	0.05 μ F
C36	" "	0.001 μ F
C37	" "	0.01 μ F, 25 V
C38	Silver mica	5 pF
C39	Disk ceramic	0.01 μ F, 25 V
C40	Silver mica	5 pF
C41-59	Disk ceramic	0.01 μ F, 100 V

(Not shown on schematic, these are
bypass capacitors near each I.C. socket.)

Inductors

L1 rf choke, miniature 51 μ Hy
L2-4 Ferrite beads

Connectors

Output, Type N, OSN 410-101 or equal, 2 ea.
Terminator, Type OSM, OSM-210-1 or equal, 2 ea.
(Shoulder turned down to reduce size)

Switches

S1 Rep. rate, 2 pole, 4 position miniature,
Alco switch MRB-2-5 or equal
S2 Delay, 2 pole, 4 position miniature,
Alco switch MRB-2-5 or equal
S3 Mode, 1 pole, 3 position center off toggle
Alco MTA 10SE or equal

Knobs

Miniature, 1/8" for S1 and S2, 2 ea.

Miscellaneous

Y1 Crystal, 10 MHz, FM-2 case
Socket, crystal, type FM-2
" , I.C., low profile 16 pin D.I.P., 14 ea.
" , I.C., 8 pin, Augat 8059-2G5 or equal, 2 ea.
" , I.C., 4 pin, Augat 8059-4G4 or equal, 1 ea.
Heat sink pads, 4 ea.
Blank plug-in, Tektronix 040-0652-05
Coax line, semi-rigid, 3.5 mm, TFE, approx. 2 ft length
Printed circuit board, 1/16" thick G-10, double-sided foil pattern per
figure A-1.

Appendix B. Alignment/Calibration Procedures

There are a minimal number of adjustments needed for maintaining the proper operation of this generator. These involve the output resistance, dc output voltage levels, trigger repetition rate, and delay (Trigger-to-Pulse) time.

A. Output Impedance Adjustments (Trigger and Pulse outputs)

1. Set the mode switch to 0 V.
2. Connect an accurate ohmmeter to the type-N output connector. Be sure that the ohmmeter test voltage on the center conductor is positive.
3. Measure the dc resistance. If it is not $50.00 \Omega \pm 0.5$ percent (may use a tighter specification if desired), then continue to step 4.
4. Select an SMA, microwave, 50Ω termination, R7 (R12), whose dc resistance is very close to, but slightly greater than, 50.00Ω .
5. Compute the required shunt resistor, R8 (R13), using $R8 = 50 \times R7 / (R7 + 50)$.
6. Select the nearest standard value 1/4W, carbon composition resistor for R8 (R13) and install it with very short leads to the connection point of CR3 (CR6) and the 3.5 mm coax. Use adequate heat sinking on the resistor during soldering.
7. Repeat steps 1 through 3.

B. Output Voltage Adjustment

1. Connect an accurate DVM to the type N output connector.
2. Set the DVM to the 1 V range.
3. Set the mode switch to 0 V.
4. Check that the output voltage is $0.0 \text{ V} \pm 10 \mu\text{V}$. If OK, go to step 6.
5. If the output is greater than $\pm 10 \mu\text{V}$, then CR3 (CR6) has excessive leakage current and must be replaced.
6. Set the mode switch to DC.
7. Adjust R17 (R16) for a reading of $1.000 \text{ V} \pm 1 \text{ mV}$ on the DVM (a tighter specification may be used if desired).

C. Repetition Rate Adjustment

1. Connect an accurate frequency counter to the Trigger output.
2. Set the repetition rate switch to 1000 kHz.
3. Set the mode switch to Pulse.
4. Adjust C5 to set the repetition rate to precisely $1.00 \text{ MHz} \pm 0.01$ percent ($\pm 100 \text{ Hz}$).

D. Delay Adjustment

1. Use a dual channel, random sampling oscilloscope for these adjustments.
2. Remove the internal reverse termination, R7, on the Trigger channel. Connect an SMA, 10 dB pad and coaxial cable to this point. Connect the other end of the cable to the scope trigger input.
3. Connect the ChA sampler to the SMA CLK (clock) output on PC board.
4. Connect the ChB sampler to the Pulse output.
5. Connect a 50Ω termination to the Trigger output.
6. Set the generator controls as follows:
Mode: Pulse, Repetition Rate: 1 MHz, and Delay: 200 ns.

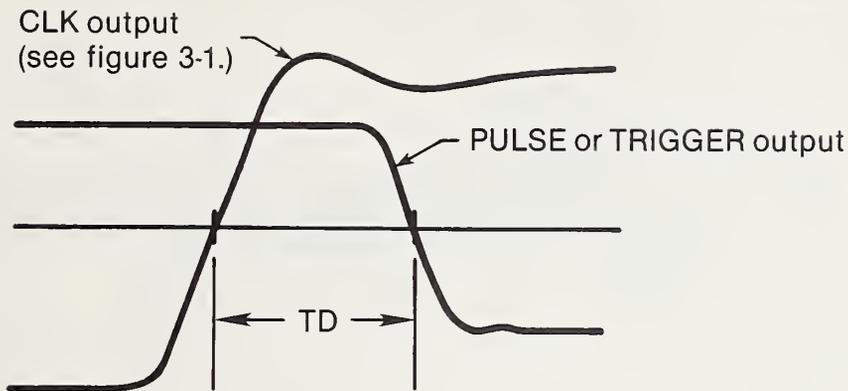


Figure B-1. Time delay adjustment waveforms. Vertical: 100 mV/div.
Horizontal: 2 ns/div. (or faster).

7. Set the sampling scope controls as follows:
Mode: Random sampling, Dual Trace, 2 ns/cm, Trigger: as needed for stable display.
8. Adjust the time position control for a display similar to that shown in figure B-1.
Adjust the individual vertical channel delay controls to minimize the time TD between transitions.
9. Measure and record $TD_1 = \text{--- ns}$.
10. Connect the ChB sampler to Trigger output and the 50 Ω termination to Pulse output.
11. Adjust the scope time position control for the figure B-1 display again.
12. Adjust C7 to set TD to precisely the value measured in step 9.
13. Set the delay to 0 ns.
14. Connect the ChB sampler to Pulse output and the 50 Ω termination to the Trigger output.
15. Adjust the time position control for the figure B-1 display again.
16. Adjust C10 to set TD to precisely the value measured in step 9.
17. Set the delay to 100 ns.
18. Adjust the time position control for the figure B-1 display again.
19. Adjust C8 to set TD to precisely the value measured in step 9.
20. Set the delay to 300 ns.
21. Adjust the time position control for the figure B-1 display again.
22. Measure and record TD_3 . TD_3 should equal TD_1 , from step 9, $\pm 1/2$ ns.
23. Remove the 10 dB pad and replace the internal 50 Ω termination for the Trigger output.

Appendix C. Measurements of the Effective Time Constant ($\tau_{B'}$)
for the BFR 90 Transistor

Besides the parameters that can be obtained from the base-emitter and collector-emitter characteristics, modeling of the BFR 90 transistor using the nonlinear GMB model [15] requires knowledge of the effective collector current exponential response to a step of base current (common-emitter configuration). As described in reference 15, a charge-controlled model of the base-emitter junction (and the associated differential equations) can be used to develop the following common-emitter equivalent circuit for simulation purposes:

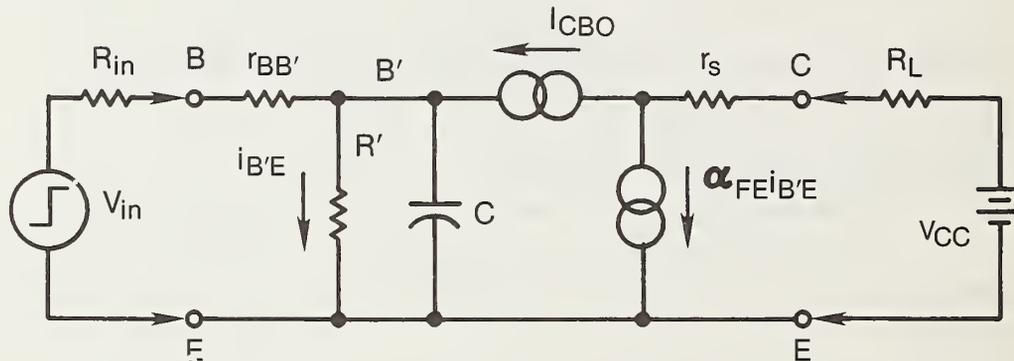


Figure C-1. Common-emitter equivalent circuit (GMB model).

- where:
- $r_{BB'}$ = bulk or extrinsic base-emitter resistance
 - R' = current-dependent base-emitter diode resistance, $r_{B'E}$
 - C = sum of the base-emitter diffusion capacitance ($C_{B'E}$) and a feedback capacitance (C_f) representative of the collector-base depletion capacitance
 - I_{CBO} = leakage (cutoff) current of the collector-base junction
 - α_{FE} = $i_C/i_{B'E}$, the common-emitter base to collector current gain, or beta (β)
 - r_s = collector saturation resistance

Although this equivalent circuit is useful for large signal switching analysis, operation in the saturation region where storage time effects must be accounted for is not inherent to the use of the BFR 90 switches used in the RFPG. Therefore, the saturation sensing diode and storage time circuit of the complete GMB model is not included in figure C-1.

The $R'C$ time constant is denoted as $\tau_{B'}$ where $\tau_{B'} = (C_{B'E} + C_f) r_{B'E}$. This time constant is considered to be constant over the entire base current excursion even though the dynamic impedance between the $B'-E$ terminals is continuously variable during the transient step. As pointed out in reference 15, this variation is important when source impedances (R_{in}) are of low value since then the input impedance affects the level of current from the driving source. For the RFPG, the driving source to the BFR 90 transistors is the low impedance ($\sim 7 \Omega$) output from an ECL logic OR gate. A measure of $\tau_{B'}$ then allows for a calculation of C since R' is determined from the base-emitter characteristics.

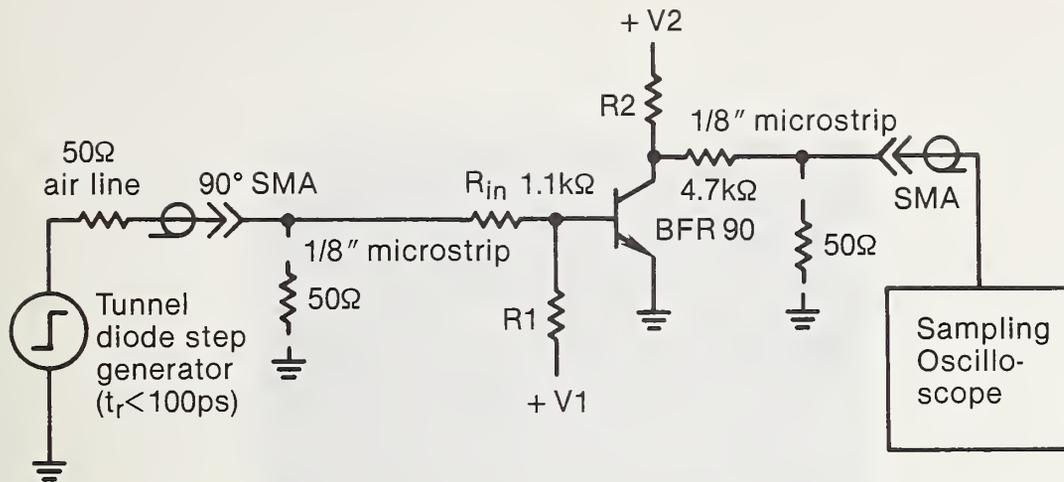


Figure C-2. BFR 90 time constant measurement circuit.

With a large value of R_{in} (so that $I_{in} = V_{in}/R_{in} = \text{constant}$) and ignoring the second-order effect of I_{CBO} , the instantaneous collector current can be expressed as

$$i_C(t) \cong \alpha_{FE} I_{in} [1 - \exp(-t/\tau_B)] \quad (C-1)$$

Time constant τ_B is equal in value to the ~63 percent point of the collector current response to a base current step, measured with i_C ranging from cutoff to just saturation (with the desired value of load resistor R_L in the collector circuit).

A test board using microstrip lines and miniature connectors for a broadband 50 Ω environment (developed for time domain reflectometry testing purposes) was used to make the τ_B measurements. The circuit board and test setups are shown in figure C-2.

The bias supplies V1 and V2 were provided by a bank of NiCad batteries. R2 is the effective load resistor (R_L) as indicated in figure C-1. Using 50 Ω microstrip lines with 1/8 inch wide copper foil on glass-epoxy printed circuit board, the step generator and sampling oscilloscope were connected via miniature high-frequency connectors. Observation of the tunnel diode step generator with the sampling scope output of the standard 50 Ω air dielectric line indicated a step transition duration (t_r) of less than 100 ps.

Photographs taken of the step response of a typical BFR 90 transistor in the test circuit given in figure C-2 are shown on figures C-3 and C-4.

The results of the step response tests run on three BFR 90 transistors are tabulated in the table C.1. The data from this table are plotted in figure C-5 showing that for large signal collector current swings up to approximately 30 ma (corresponding to load resistance of about 200 Ω), the effective τ_B is around 3 ns.

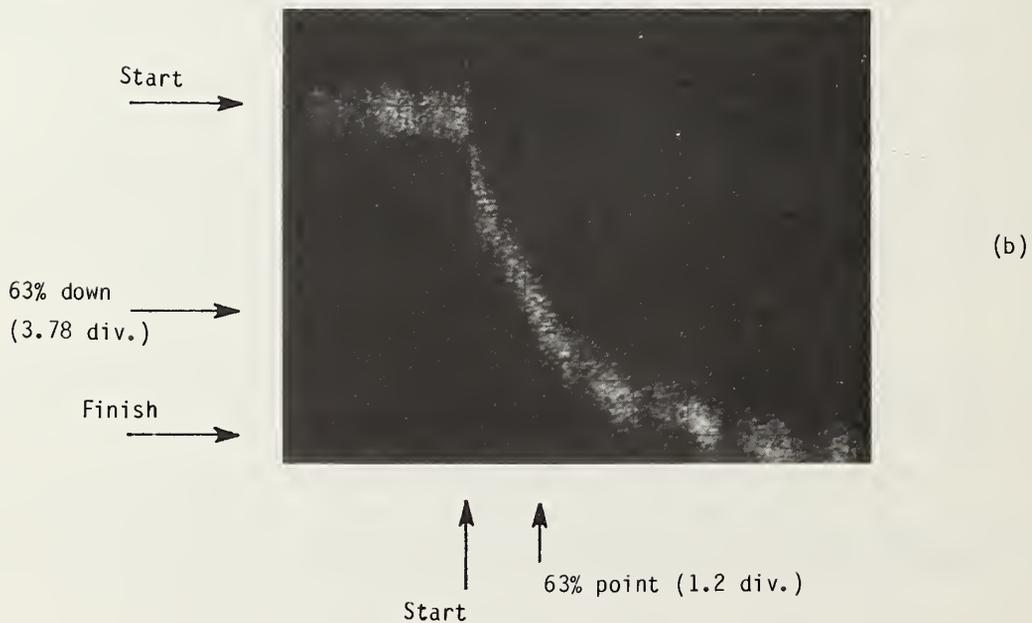
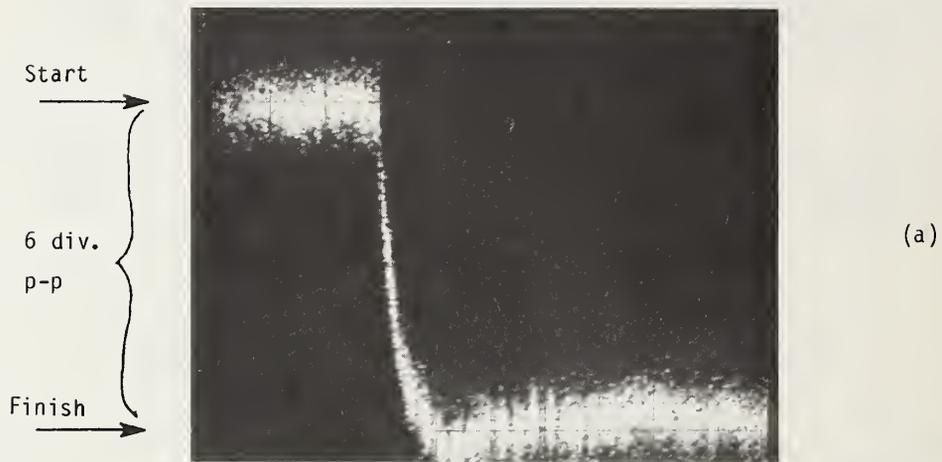


Figure C-3. Step response (τ_b measurement) photos of a typical BFR 90 transistor (150 Ω load resistance).
 (a) Vertical: 5 mV/div. Horizontal: 10 ns/div. Test conditions: $V_1 = V_2 = 6.3$ V, $R_1 = 6.2$ k Ω , $R_2 = 150$ Ω . V_{CE} swing: 6 div p-p; +1.5 V (saturation), +4.9 V (cutoff).
 (b) Vertical: 5 mV/div. Horizontal: 2 ns/div. Test conditions: same as above. 63% x 6 div. = 3.78 div. $\tau_b \cong 1.2$ div. x 2 ns/div. $\cong 2.4$ ns.

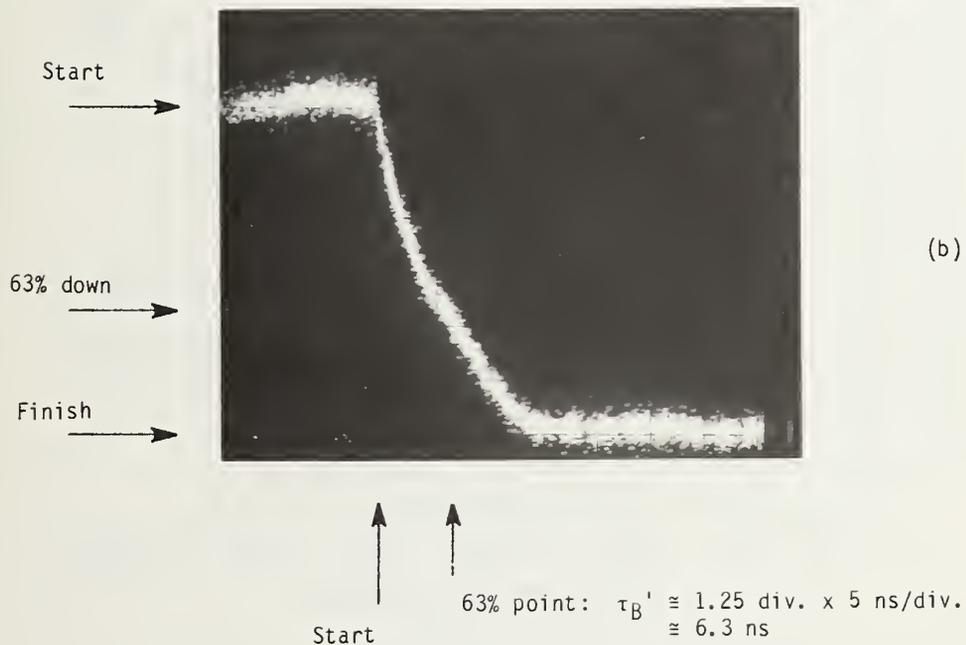
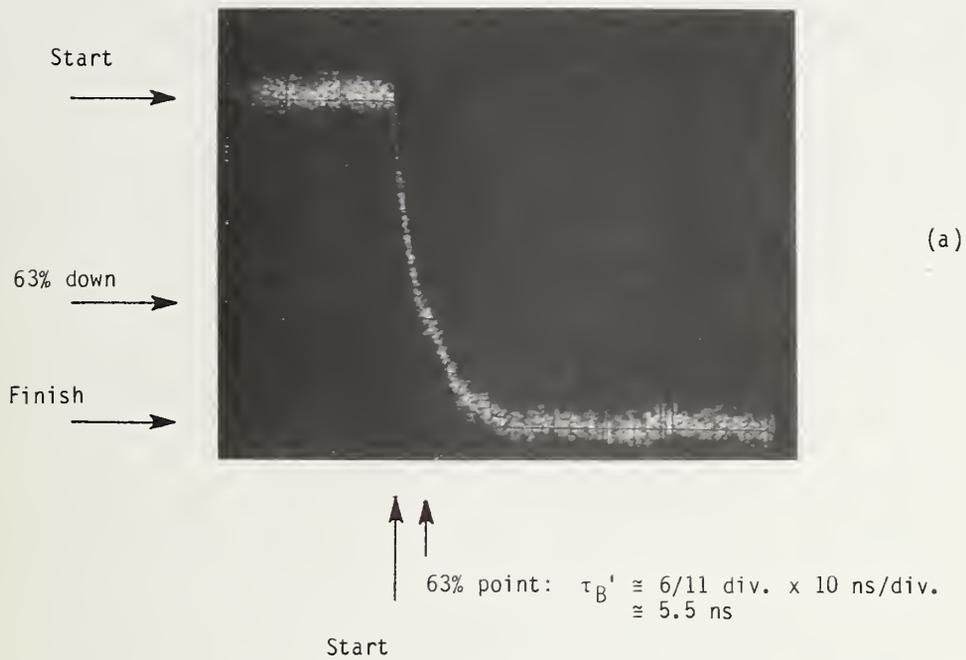


Figure C-4. Step response (τ_B' measurement) of a typical BFR 90 transistor (300 Ω and 620 Ω load resistance).

(a) Vertical: 6 div. p-p. Horizontal: 10 ns/div. Test conditions: $V_1 = 5.02 \text{ V}$, $V_2 = 6.3 \text{ V}$, $R_1 = 6.2 \text{ k}\Omega$, $R_2 = 300 \Omega$. V_{CE} swing: +0.6 V (saturation), +5.8 V (cutoff).

(b) Vertical: 6 div. p-p. Horizontal: 5 ns/div. Test conditions: same as above except $R_2 = 620 \Omega$. V_{CE} swing: +0.6 V (saturation), +5.6 V (cutoff).

Table C.1. Summary

Transistor number		$R_2 = 150 \Omega$ (ns)	$R_2 = 300 \Omega$ (ns)	$R_2 = 620 \Omega$ (ns)
5	2.4	5.45	6.25	
6	2.0	5.2	8.4	
3	1.8	5.0	7.9	
	Ave.	2.07	5.22	7.52

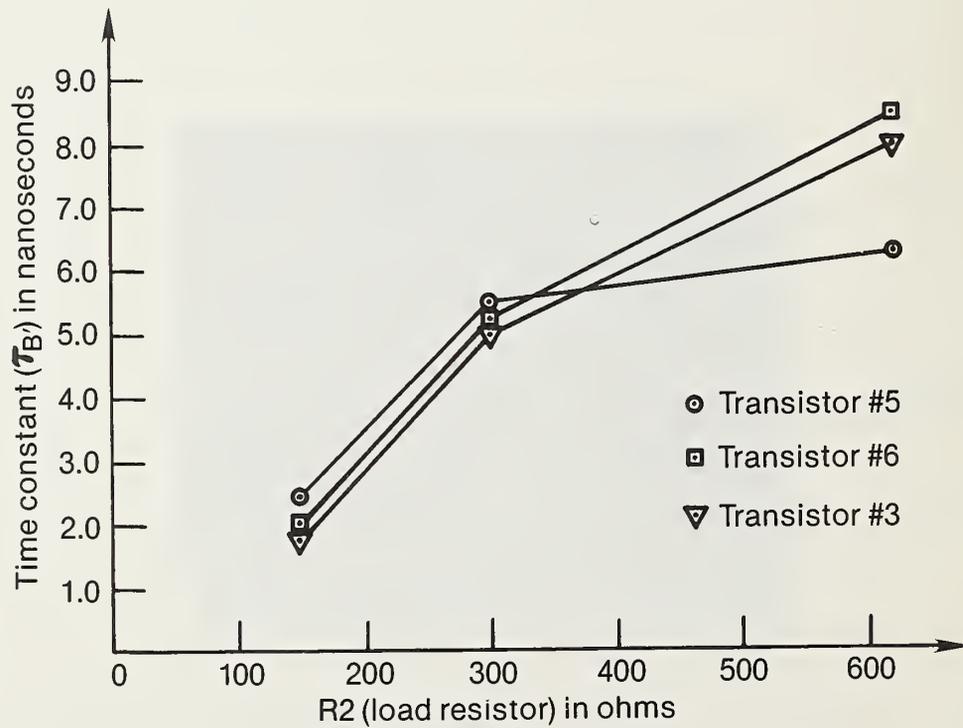


Figure C-5. Plot of τ_B data on BFR 90 transistors.

Appendix D. Collector Capacitance Equivalency

Given the circuits shown in figures D-1 and D-2 on the following page, it is desired to determine the step response voltage at the collector node due to either the known collector-base capacitance or an equivalent capacitance between collector and circuit common. Letting $X(s) = \mathcal{L}[x(t)]$ denote the Laplace transform representation of the instantaneous value of the circuit variables for figure D-1, then

$$I_b(s) = I_{b'e}(s) + I_f(s), \quad (D-1)$$

where, assuming zero initial conditions,

$$I_f(s) = sC_f V_{b'e}(s). \quad (D-2)$$

The collector-base voltage $V_{b'e}(s)$ is determined by

$$V_{b'e}(s) = I_{b'e}(s)R_2 + V_o(s), \quad (D-3)$$

where $V_o(s) = I_\ell(s)R_\ell$ is the collector output node voltage. Since

$$I_\ell(s) = \beta I_{b'e}(s) - I_f(s) \quad (D-4)$$

then

$$V_o(s) = [\beta I_{b'e}(s) - I_f(s)]R_\ell \quad (D-5)$$

or, by substituting for $I_f(s)$, using eq (D-1),

$$V_o(s) = [I_{b'e}(s)(1 + \beta) - I_b(s)]R_\ell. \quad (D-6)$$

By solving for $V_{b'e}(s)$ in eq (D-2), and using eq (D-3),

$$I_{b'e}(s)R_2 + V_o(s) = I_f(s)/sC_f \quad (D-7)$$

or,

$$R_2 C_f s I_{b'e}(s) + C_f s V_o(s) = I_f(s) = I_b(s) - I_{b'e}(s). \quad (D-8)$$

Solving for $I_{b'e}(s)$ gives

$$I_{b'e}(s) = \frac{I_b(s) - C_f s V_o(s)}{1 + R_2 C_f s}. \quad (D-9)$$

Substituting for $I_{b'e}(s)$ in eq (D-6),

$$V_o(s) = \left[\left(\frac{I_b(s) - C_f s V_o(s)}{1 + R_2 C_f s} \right) (1 + \beta) - I_b(s) \right] R_\ell. \quad (D-10)$$

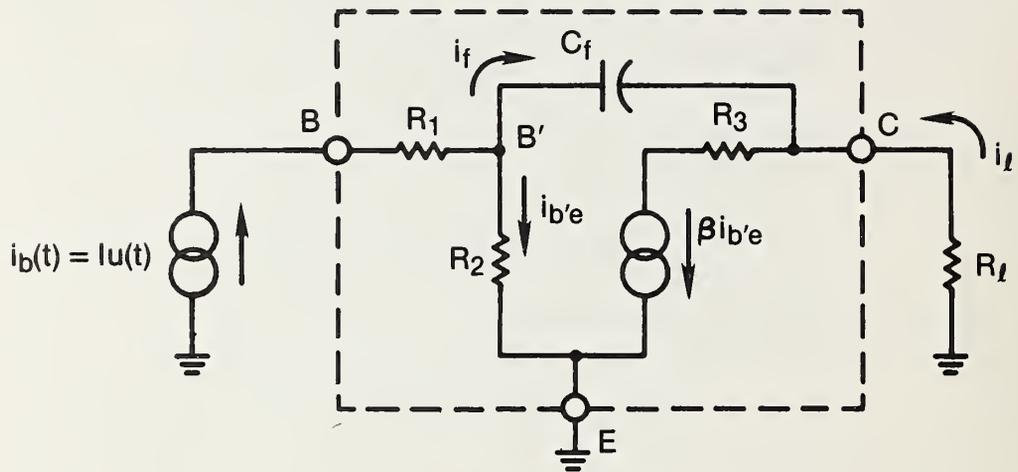


Figure D-1. Simplified transistor model using collector-base capacitance for step response.

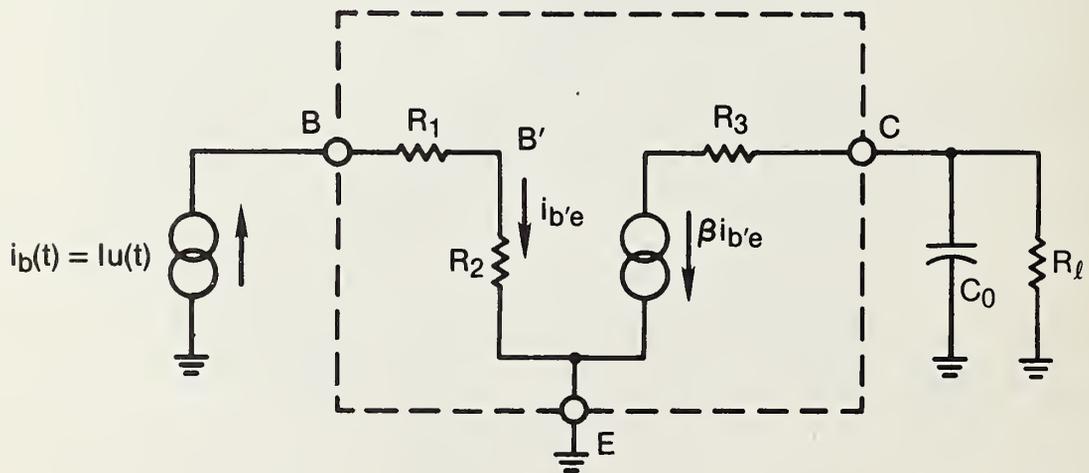


Figure D-2. Simplified transistor model using equivalent common-collector capacitance for step response.

With appropriate rearrangement,

$$V_o(s) = \frac{(\beta - R_2 C_f s) R_\ell I_b(s)}{1 + [R_2 + (1 + \beta) R_\ell] C_f s} \quad (D-11)$$

For $i_b(t) = Iu(t)$, an input step of base current of I amperes, so that $I_b(s) = I/s$,

$$V_o(s) = \frac{(\beta - R_2 C_f s) R_\ell I}{s \{1 + [R_2 + (1 + \beta) R_\ell] C_f s\}} \quad (D-12)$$

or,

$$V_o(s) = \frac{\beta R_\ell I}{s \{1 + [R_2 + (1 + \beta) R_\ell] C_f s\}} - \frac{R_2 C_f R_\ell I}{1 + [R_2 + (1 + \beta) R_\ell] C_f s} \quad (D-13)$$

By using partial fraction expansion,

$$V_o(s) = \frac{\beta R_\ell I}{s} - \frac{\beta R_\ell I}{s + \frac{1}{[R_2 + (1 + \beta) R_\ell] C_f}}$$

$$- \frac{\left(\frac{R_2 R_\ell}{R_2 + (1 + \beta) R_\ell}\right) I}{s + \frac{1}{[R_2 + (1 + \beta) R_\ell] C_f}} \quad (D-14)$$

or,

$$V_o(s) = \beta R_\ell I \left[\frac{1}{s} - \frac{1}{s + 1/\tau_1} \right] - \frac{R_p I}{s + 1/\tau_1} \quad (D-15)$$

where: $\tau_1 = [R_2 + (1 + \beta) R_\ell] C_f$

$$R_p = \frac{R_2 R_\ell}{R_2 + (1 + \beta) R_\ell}$$

The step response voltage at the collector node is thus

$$V_o(t) = \beta R_\ell I [1 - \exp(-t/\tau_1)] - R_p I \exp(-t/\tau_1) \quad (D-16)$$

For figure D-2,

$$\beta I_{b,e}(s) = \beta I_b(s) \quad (D-17)$$

The load impedance at the collector node is

$$Z_\ell(s) = \frac{R_\ell}{1 + R_\ell C_o s} \quad (D-18)$$

so that the collector output node voltage is

$$V_o(s) = \beta I_b(s) Z_\ell(s) \quad (D-19)$$

or,

$$V_o(s) = \frac{\beta R_\ell I_b(s)}{1 + R_\ell C_o s} \quad (D-20)$$

which corresponds to eq (D-11) for figure D-1. Again, for $I_b(s) = I/s$, corresponding to an input step of base current of I amperes,

$$V_o(s) = \frac{\beta R_\ell I}{s[1 + R_\ell C_o s]} \quad (D-21)$$

By partial fraction expansion,

$$V_o(s) = \frac{\beta R_\ell I}{s} - \frac{\beta R_\ell I}{s + \frac{1}{R_\ell C_o}}, \quad (D-22)$$

or,

$$V_o(s) = \beta R_\ell I \left[\frac{1}{s} - \frac{1}{s + 1/\tau_2} \right], \quad (D-23)$$

where $\tau_2 = R_\ell C_o$. The step response voltage is then

$$V_o(t) = \beta R_\ell I [1 - \exp(-t/\tau_2)]. \quad (D-24)$$

For equivalent response times,

$$\tau_1 = [R_2 + (1 + \beta)R_\ell]C_f = \tau_2 = R_\ell C_o. \quad (D-25)$$

For typical values, $(1 + \beta)R_\ell \gg R_2$. Hence,

$$(1 + \beta)R_\ell C_f \cong R_\ell C_o, \quad (D-26)$$

or,

$$C_o = (1 + \beta)C_f. \quad (D-27)$$

In the case for a BFR 90 transistor, from reference 17, typically

$$\begin{aligned} C_f &= C_{cb} = 0.5 \text{ pF} \\ \beta &= h_{FE} = 25_{\min} \text{ to } 250_{\max}. \end{aligned} \quad (D-28)$$

From actual observed collector characteristics (see fig. 4-20), typical β values are 40 to 80. Using $\beta = 60$ and $C_f = 0.5 \text{ pF}$ in eq (D-27),

$$C_o(\text{typical}) \cong (61) 0.5 \text{ pF} = 30.5 \text{ pF}. \quad (D-29)$$

A value of $C_o = C_g = 10 \text{ pF}$ was found to produce good results in the TRFPG program model shown in figure 4-31.

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6. PERFORMING ORGANIZATION (If joint or other than NBS, see instructions) NATIONAL BUREAU OF STANDARDS DEPARTMENT OF COMMERCE WASHINGTON, D.C. 20234		7. Contract/Grant No.	8. Type of Report & Period Covered
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11. ABSTRACT (A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here) <p>A reference step-like pulse generator is described which has been developed at NBS. This generator can be used for accurately characterizing the step response of various kinds of transient recording equipment (oscilloscopes, waveform recorders, transient digitizers, etc.). Basic design principles are given as well as complete circuit diagrams and descriptions. An analysis of the output stage of the generator is presented together with the circuit models for developing a time-domain computer simulation program using extended-SCEPTRE. Preliminary specifications indicate that the NBS Reference Flat Pulse Generator provides a negative-going reference transition duration (90 to 10 percent) of 600 ps, ± 2 percent after 5 ns.</p>			
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