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Semiconductor Measurement Technology:

INSTANT – IGBT Network Simulation and Transient ANalysis Tool

A. R. Hefner, Jr.

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Abstract

The IGBT (Insulated Gate Bipolar Transistor) is a power semiconductor device that has gained acceptance among power electronic circuit design engineers for motor drive and power converter applications. These devices have the best features of both power MOSFETs and power bipolar transistors, i.e., efficient voltage gate drive requirements and high current density capability. When designing circuits and systems that utilize IGBTs or other power semiconductor devices, circuit simulations are needed to examine how the devices affect the behavior of the circuit. However, the semiconductor device models available in most circuit simulators were originally intended to describe microelectronic devices and cannot adequately describe the characteristics of power devices.

In this publication, a compact IGBT model suitable for incorporation in circuit simulators is described, and a circuit simulation program called INSTANT is presented that simulates the dynamic behavior of IGBTs within any external drive, load, and feedback circuit configuration. The INSTANT simulator solves the systems of differential equations (state equations) that describe each component of the circuit, where the equations for the individual components are coupled by the circuit configuration. The INSTANT software package is designed to provide the flexibility to change the external circuit configuration and model equations. The device and circuit parameters are also readily accessible, and the graphics output provides a real-time display of the waveforms as they are calculated.

This publication also describes the automated measurement methods developed to extract the IGBT device model parameters from terminal electrical measurements. It is shown that unlike parameter extraction for microelectronic devices, the dynamic characteristics must be used to characterize IGBTs and to extract the model parameters. This occurs because the devices exhibit non-quasi-static behavior and because the dynamic waveforms contain many features that isolate different physical mechanisms, whereas the physical mechanisms are convoluted in the relatively simple steady-state characteristics. The unique features

of the IGBT electrical characteristics are explained using the model, and the procedures used to verify the IGBT model are given.

Key words: circuit simulator; dynamic model; FORTRAN; power transistor; software.

I. INTRODUCTION

The Insulated Gate Bipolar Transistor (IGBT) is a relatively new power device with an insulated gate input like that of a power MOSFET but with the low on-state resistance of a power bipolar transistor. A schematic of the structure of two of the many thousand cells of an n-channel IGBT is shown in figure 1. The IGBT functions as a bipolar transistor that is supplied base current by the drain of a MOSFET where the source of the MOSFET is shorted to the collector of the bipolar transistor (fig. 2). The regions of each of these components are labeled on the right half of figure 1.

The bipolar transistor of the IGBT consists of a lightly doped wide base with the base virtual contact (MOSFET drains) near the collector end of the base. This bipolar transistor has a low gain and is in the high-level injection condition for the practical current density range of the IGBT. Consequently, the IGBT bipolar transistor cannot be described in traditional ways [1,2]. The MOSFET portion of the IGBT behaves similarly to the structurally equivalent power VDMOSFET (Vertical double Diffused MOSFET), with the exception that the resistance of the lightly doped epitaxial layer is replaced by the conductivity-modulated base resistance of the bipolar transistor.

An analytical model has been developed for the IGBT that is applicable for general external circuit conditions [3,4]. The analytical model for the IGBT is based upon ambipolar transport theory and accurately describes the IGBT steady-state current-voltage characteristics [1-7]. The IGBT model does not assume the quasi-static condition for the transient analysis and accurately describes the output current and voltage turn-off switching waveform for general loading conditions [1-5]. It was shown in reference [2] that the traditional quasi-static approach of modeling bipolar transistors is not adequate for the low-gain, high-level injection bipolar transistor of the IGBT. An analytical model for the VDMOSFET characteristics has also been included in the non-quasi-static IGBT model, and this model accurately describes the input and output, current and voltage, turn-on and turn-off switching waveforms for general external drive, load, and feedback circuit conditions [3].

The standard models available in most commercial circuit simulators (e.g., SPICE) were originally intended to describe microelectronic devices and cannot readily be used to describe the internal bipolar transistors or internal MOSFETs of power devices such as the IGBT [8-10]. The purpose of this publication is to describe the circuit simulation program developed to simulate the behavior of IGBTs within the circuit [4], to present the complete IGBT model in a form that is suitable for implementation in commercial circuit simulators [8,9], and to describe the procedures used to extract the IGBT model parameters from terminal electrical measurements [4,10]. The circuit simulation program described in this

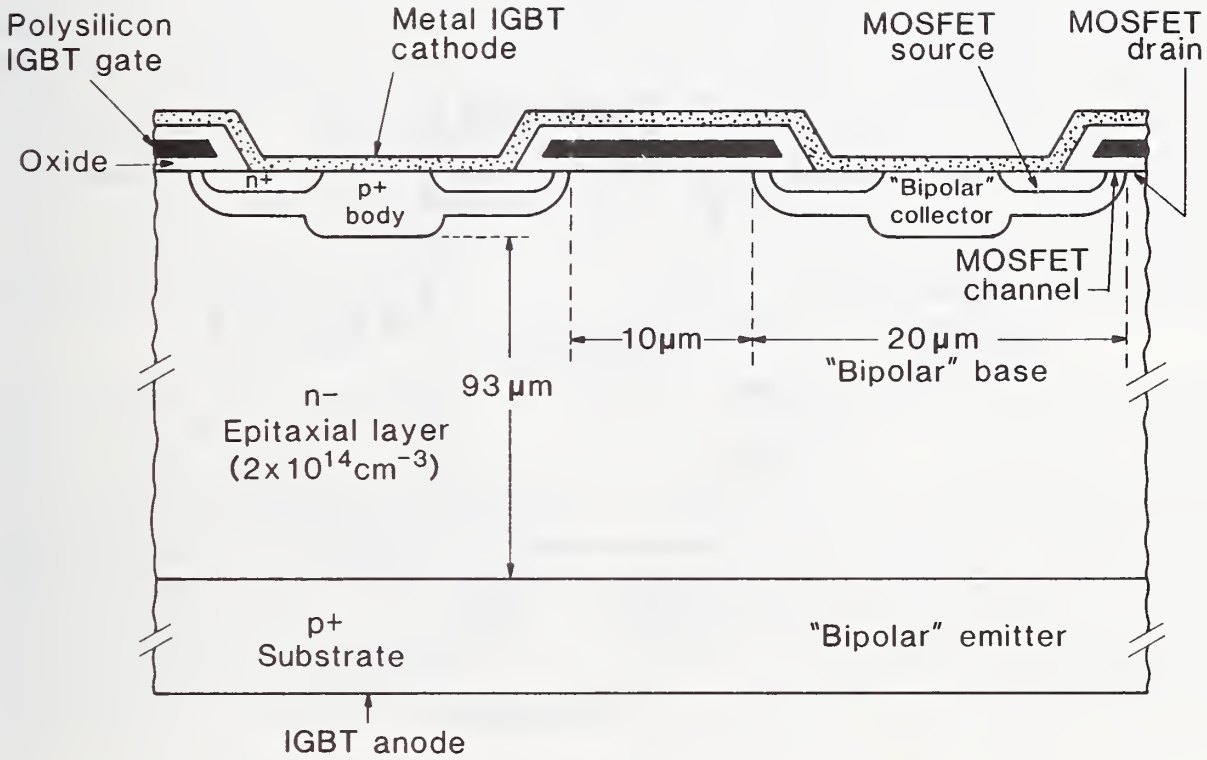

Figure 1. A diagram of two of the diffused cells of an n-channel IGBT.

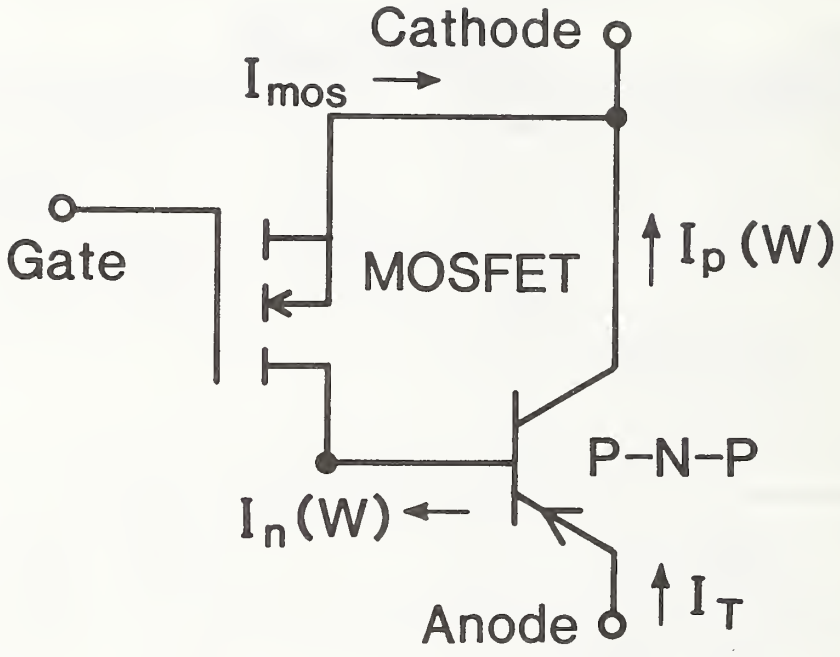

Figure 2. The basic equivalent circuit model of the IGBT.

publication is called INSTANT [4]: IGBT Network Simulation and Transient ANalysis Tool. INSTANT* is written in generally portable FORTRAN code and is available with graphics libraries for various PC, VAX,** and Sun** FORTRAN compilers and graphics Windows environments [11].

II. IGBT DYNAMIC MODEL

In this section, an analytical model is presented that describes the dynamic behavior of the IGBT including the drive circuit dependence and the load circuit dependence. The IGBT model is formulated as the three state equations given in table 1 that describe the evolution of the state of the base-collector voltage V_{bc}, the base charge Q, and the gate-source voltage V_{gs}, where the symbols are defined in the nomenclature. These state equations are expressed in terms of functions of the instantaneous values of the state variables of the IGBT and the external circuit. The functions of the IGBT state variables are listed in table 2, and the functions of the external circuit state variables, I_T and I_g, depend upon the external circuit configuration as described below. To describe the interaction of the IGBT with the external circuit, the IGBT state equations are integrated simultaneously with the state equations of the external circuit. The circuit state equations are expressed in terms of the IGBT state variables as well as the circuit state variables using the expressions in table 3 to calculate the IGBT anode terminal voltage.

Figure 3 shows the configuration of the MOSFET and bipolar equivalent circuit components of the IGBT superimposed on a schematic of one-half of the symmetric diffused IGBT cell. The MOSFET portion of the IGBT studied in this work behaves similarly to the power VDMOSFET [12-15], with the exception that the resistance of the lightly doped epitaxial layer is accounted for as the conductivity-modulated base resistance of the bipolar transistor, R_b. In addition, the drain-source and gate-drain depletion capacitances coincide with the base-collector depletion capacitance of the bipolar transistor and hence are only included in the MOSFET. In the remainder of this section, the mathematical model for these internal components is described and is used to derive the IGBT state equations.

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* The INSTANT software package can be obtained by sending a letter of request along with a blank floppy disk(s) (total of at least 1 Mb) to the author of this publication, or by sending an e-mail message requesting the software with a return address to: hefner@sed.eeel.nist.gov. The INSTANT software package contains the complete IGBT modeling source code, a graphics library for the specified FORTRAN compiler, example model parameter sets for several commercially available IGBT part numbers, and example input files for several external circuit configurations.

** Certain commercial equipment, instruments, or materials are identified in this paper in order to specify adequately the experimental procedure. Such identification does not imply recommendation or endorsement by the National Institute of Standards and Technology, nor does it imply that the materials or equipment identified are necessarily the best available for the purpose.

Table 1. IGBT State Equations

$$\frac{\mathrm{d}V_{gs}}{\mathrm{d}t} = \frac{I_g}{C_{gs}+C_{gd}} + \frac{C_{gd}}{C_{gs}+C_{gd}} \cdot \frac{\mathrm{d}V_{bc}}{\mathrm{d}t} \tag{T1.1}$$

$$\frac{\mathrm{d}V_{bc}}{\mathrm{d}t} = \frac{I_T - M \cdot \left[\frac{\gamma I_T}{1+b} + \frac{2D}{W^2}Q + I_{mos} + I_{gen}\right] + \frac{C_{gd}}{C_{gs}+C_{gd}} I_g}{\left[C_{dsj} + \frac{C_{gs}C_{gd}}{C_{gs}+C_{gd}} + M \cdot \frac{C_{bcj}}{3} \cdot \frac{Q}{Q_B}\right]} \tag{T1.2}$$

$$\begin{aligned}\frac{\mathrm{d}Q}{\mathrm{d}t} =& M \cdot (I_{mos} + I_{gen}) + (M-1) \cdot I_p(W) + (C_{dsj} + C_{gd})\frac{\mathrm{d}V_{bc}}{\mathrm{d}t} - C_{gd}\frac{\mathrm{d}V_{gs}}{\mathrm{d}t} \\ & - \frac{Q}{\tau_{HL}} - \frac{Q^2}{Q_B^2} \cdot \frac{4N_{scl}^2}{n_i^2} I_{sne},\end{aligned} \tag{T1.3}$$

Table 2. Functions of IGBT State Variables

$$W_{gdj} = \sqrt{2\epsilon_{si}(V_{ds} - V_{gs} + V_{Td})/qN_{scl}} \tag{T2.1}$$

$$W_{dsj} = \sqrt{2\epsilon_{si}(V_{ds} + V_{bi})/qN_{scl}} \tag{T2.2}$$

$$W_{bcj} = \sqrt{2\epsilon_{si}(V_{bc} + V_{bi})/qN_{scl}} \tag{T2.3}$$

$$W = W_B - W_{bcj} \tag{T2.4}$$

$$Q_B = qAWN_{scl} \tag{T2.5}$$

$$\gamma = Q/(Q + Q_B) \tag{T2.6}$$

$$D = D_n D_p(2Q + Q_B)/[D_n(Q + Q_B) + QD_p] \tag{T2.7}$$

$$C_{bcj} \equiv A\epsilon_{si}/W_{bcj} \tag{T2.8}$$

$$C_{dsj} = (A - A_{gd})\epsilon_{si}/W_{dsj} \tag{T2.9}$$

$$C_{gdj} = A_{gd}\epsilon_{si}/W_{gdj} \tag{T2.10}$$

$$C_{gd} = \begin{cases} C_{ozd} & \text{for} \quad V_{ds} \le V_{gs} - V_{Td} \\ C_{ozd}C_{gdj}/(C_{ozd} + C_{gdj}) & \text{for} \quad V_{ds} > V_{gs} - V_{Td} \end{cases} \tag{T2.11}$$

$$BV_{cbo} = BV_f \cdot 5.34 \times 10^{13} \cdot N_{scl}^{-0.75} \tag{T2.12}$$

$$M = 1/[1 - (V_{cb}/BV_{cbo})^{BV_n}] \tag{T2.13}$$

$$I_{gen} = \left(qn_i A\sqrt{2\epsilon_{si}V_{bc}/qN_{scl}}\right)/\tau_{HL} \tag{T2.14}$$

$$I_{mos} = \begin{cases} 0 & \text{for } V_{gs} < V_T \\ \dfrac{K_{Plin}\left[(V_{gs} - V_T)V_{ds} - \dfrac{K_{Plin}V_{ds}^2}{2K_{Psat}}\right]}{[1 + \theta(V_{gs} - V_T)]} & \text{for } V_{ds} \le (V_{gs} - V_T)\dfrac{K_{Psat}}{K_{Plin}} \\ \dfrac{K_{Psat}(V_{gs} - V_T)^2}{2[1 + \theta(V_{gs} - V_T)]} & \text{for } V_{ds} > (V_{gs} - V_T)\dfrac{K_{Psat}}{K_{Plin}} \end{cases} \tag{T2.15}$$

Table 3. Anode Terminal Voltage

$$\mu_{nc} = 1/(1/\mu_n + 1/\mu_c) \tag{T3.1}$$

$$\mu_{pc} = 1/(1/\mu_p + 1/\mu_c) \tag{T3.2}$$

$$\mu_{eff} = \mu_{nc} + \mu_{pc}Q/(Q + Q_B) \tag{T3.3}$$

$$D_{ccs} = (kT/q)\mu_{nc}\mu_{pc}/(\mu_{nc} + \mu_{pc}) \tag{T3.4}$$

$$L = \sqrt{D_{ccs}\tau_{HL}} \tag{T3.5}$$

$$P_0 = Q/(qAL \tanh \frac{W}{2L}) \tag{T3.6}$$

$$\overline{\delta p} \equiv P_0 \sinh(W/2L)/\sinh(W/L) \tag{T3.7}$$

$$Q_0 = A\sqrt{2\epsilon_{si}qN_BV_{bi}} \tag{T3.8}$$

$$n_{eff} \equiv \frac{\frac{W}{2L}\sqrt{N_B^2 + P_0^2\,\mathrm{csch}^2(\frac{W}{L})}}{\operatorname{arctanh}\left[\dfrac{\sqrt{N_B^2 + P_0^2\,\mathrm{csch}^2(\frac{W}{L})}\cdot\tanh(\frac{W}{2L})}{N_B + P_0\,\mathrm{csch}(\frac{W}{L})\tanh(\frac{W}{2L})}\right]} \tag{T3.9}$$

$$R_b = \begin{cases} W/(q\mu_{nc}AN_B) & \text{for} \quad Q < 0 \\ W/(q\mu_{eff}An_{eff}) & \text{for} \quad Q \geq 0 \end{cases} \tag{T3.10}$$

$$V_{ebj} = V_{bi} - (Q - Q_0)^2/(2qN_B\epsilon_{si}A^2) \tag{T3.11}$$

$$V_{ebd} = \frac{kT}{q}\ln\left[\left(\frac{P_0}{n_i^2} + \frac{1}{N_B}\right)\left(N_B + P_0\right)\right] - \frac{D_{ccs}}{\mu_{nc}}\ln\frac{P_0 + N_B}{N_B} \tag{T3.12}$$

$$V_{ebq} = \begin{cases} V_{ebj} & \text{for} \quad Q < 0 \\ \min(V_{ebj}, V_{ebd}) & \text{for} \quad Q_0 > Q \geq 0 \\ V_{ebd} & \text{for} \quad Q \geq Q_0 \end{cases} \tag{T3.13}$$

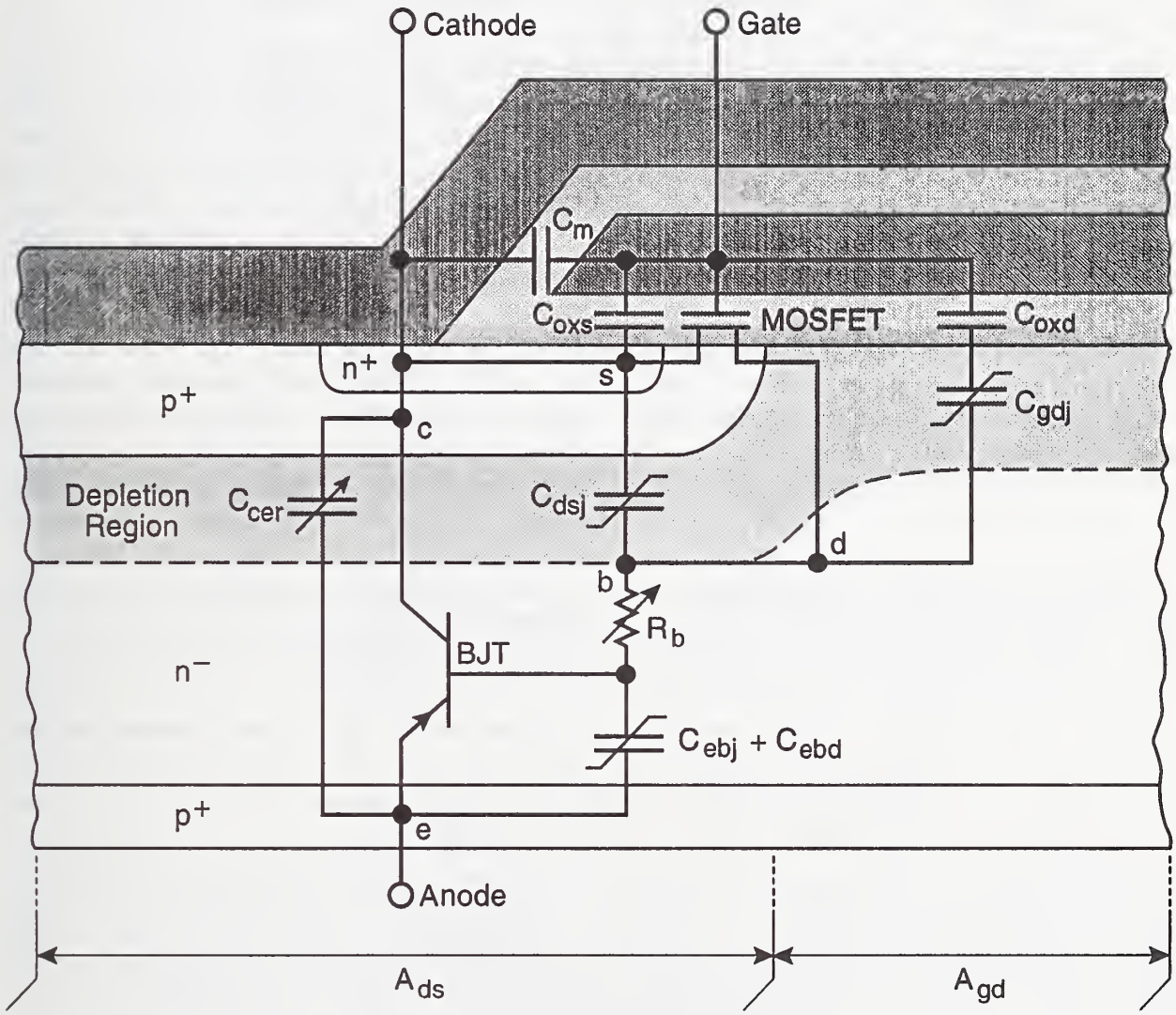


Figure 3. The configuration of the MOSFET and bipolar equivalent circuit components superimposed on a schematic of one-half of the symmetric IGBT cell.

MOSFET Input Characteristics

The basic expressions describing the equivalent circuit MOSFET of the IGBT are listed among the functions of the IGBT state variables in table 2. To describe IGBTs made with power MOSFET structures other than the VDMOSFET structure, the expressions in table 2 can be replaced with the expressions for the appropriate structurally equivalent power MOSFET. The MOSFET channel current consists of the linear and saturation regions, where the linear region transconductance parameter K_{Plin} is different from the saturation region transconductance parameter K_{Psat} due to the graded channel dopant density for the diffused channel MOSFET [8,13]. This difference exists for all VDMOSFET structures, but the linear region transconductance is not as important for the high-voltage power VDMOSFETs due to the high series resistance of the thick, lightly doped epitaxial layer. The MOSFET channel current expression also includes the reduction in channel mobility due to high transverse electric fields using the parameter θ [13,16].

The dominant components of the VDMOSFET gate-source capacitance C_{gs} are due to the gate oxide capacitance of the source overlap C_{oxs} and the source metallization capacitance C_m indicated on figure 3. The dominant component of the MOSFET gate-drain capacitance C_{gd} is the gate oxide capacitance of the drain overlap C_{oxd} for $V_{ds} \leq V_{gs} - V_{Td}$ or the series combination of the gate-drain overlap oxide capacitance and the gate-drain overlap depletion capacitance C_{gdj} for $V_{ds} > V_{gs} - V_{Td}$. The gate-to-channel and gate-to-body capacitances are neglected in this publication for simplicity [15]. The effect of the inversion of the silicon beneath the gate-drain overlap on the gate-drain capacitance for negative gate voltages is also neglected. However, the simplified expressions for the capacitances in table 2 can readily be changed to include these effects, if necessary.

The gate-drain overlap depletion capacitance C_{gdj} and the drain-source depletion capacitance C_{dsj} are voltage dependent due to the voltage dependencies of the respective depletion widths. The drain-source depletion width W_{dsj} is proportional to the square-root of the drain-source voltage plus the built-in potential of the junction $V_{bi} \approx 0.6$ V. The gate-drain depletion width W_{gdj} is proportional to the square-root of the gate-drain voltage where the threshold voltage for the depletion of the epitaxial layer V_{Td} is approximately zero for most devices due to the low doping concentration of the epitaxial layer. The gate-drain capacitance is also proportional to the area of the gate-drain overlap A_{gd}. The drain-source capacitance is proportional to the area of the body region A_{ds} (fig. 3), where the sum of A_{gd} and A_{ds} is the active area of the chip A.

The depletion widths in table 2 and the corresponding capacitances are obtained by solving Poisson's equation, assuming a one-sided step junction with the space charge concentration N_{scl}. The expression for the space charge concentration,

$$N_{scl} = N_B + \frac{I_p(W)}{qAv_{psat}} - \frac{I_{mos}}{qAv_{nsat}}, \tag{1}$$

is used to evaluate the equations in table 1 [1]. This expression consists of the sum of the uncompensated dopant concentration N_B and the mobile carriers in the depletion region

due to the saturated velocity of holes and electrons in silicon v_{psat} and v_{nsat}, respectively. In general, the expression for N_{scl} must be solved implicitly during simulations because it depends upon the values of $I_p(W)$ (described below) and I_{mos} which are calculated using the value of N_{scl}.

Bipolar Output Characteristics

The transient behavior of the lightly doped wide base bipolar transistor of the IGBT (and other conductivity-modulated devices) was analyzed in references [1,2]. The transient carrier distribution and currents in the base are obtained by solving the ambipolar transport equations and charge continuity equations given in appendix 1 for the boundary conditions of the bipolar transistor. Figure 4 shows the coordinate system used to develop the IGBT bipolar transistor model. Because the base-collector voltage changes with time during transient conditions, the base-collector depletion width changes with time and the excess carrier charge stored in the base is swept into a neutral base width W that changes with time. It is shown in appendix 2 that the ambipolar diffusion equation must be solved for the moving boundary condition to obtain the non-quasi-static transient carrier distribution and collector current when the base width changes faster than the base transit speed for excess carriers. It is also shown below that this condition exists during typical IGBT transient operation and that the moving boundary redistribution effect dominates the transient behavior.

The hole current at the collector edge of the neutral base (collector current of fig. 2 except for the multiplication current) for the moving boundary condition is derived in appendix 2. The expression for the collector current is given in terms of the functions of the state variables in table 2 by substituting eq (A2.3) into eq (A2.6) and using the expression for the background base charge Q_B in table 2:

$$I_p(W) = \left(\frac{\gamma}{1+b}\right) I_T \; + \; \frac{2D}{W^2} Q \; + \; \frac{C_{bcj}}{3} \cdot \frac{Q}{Q_B} \cdot \frac{\mathrm{d}V_{bc}}{\mathrm{d}t} \; , \tag{2}$$

where the expressions in table 2 for γ and D are used so that the expression for the collector current also describes the low-level injection condition. It is shown in appendix 2 that the redistribution current (third term on the right-hand side of eq (2)) becomes larger than the charge control current (second term) when the base width changes faster than the base transit speed. Because the third term as expressed in eq (2) is proportional to the time rate-of-change of base-collector voltage, it can be construed as a capacitive term where the capacitance is proportional to the instantaneous charge in the base Q [1-3,7]. This is indicated by the charge-dependent collector-emitter redistribution capacitance C_{cer} in figure 3. Because the ratio Q/Q_B is much larger that unity for high level injection, the redistribution capacitance is much larger than the depletion capacitances and dominates the output capacitance of the IGBT.

In addition to the components of current indicated on figure 3, a component of current:

$$I_{mult} = M \cdot I_{gen} + (M-1) \cdot (I_{mos} + I_p(W)) \tag{3}$$

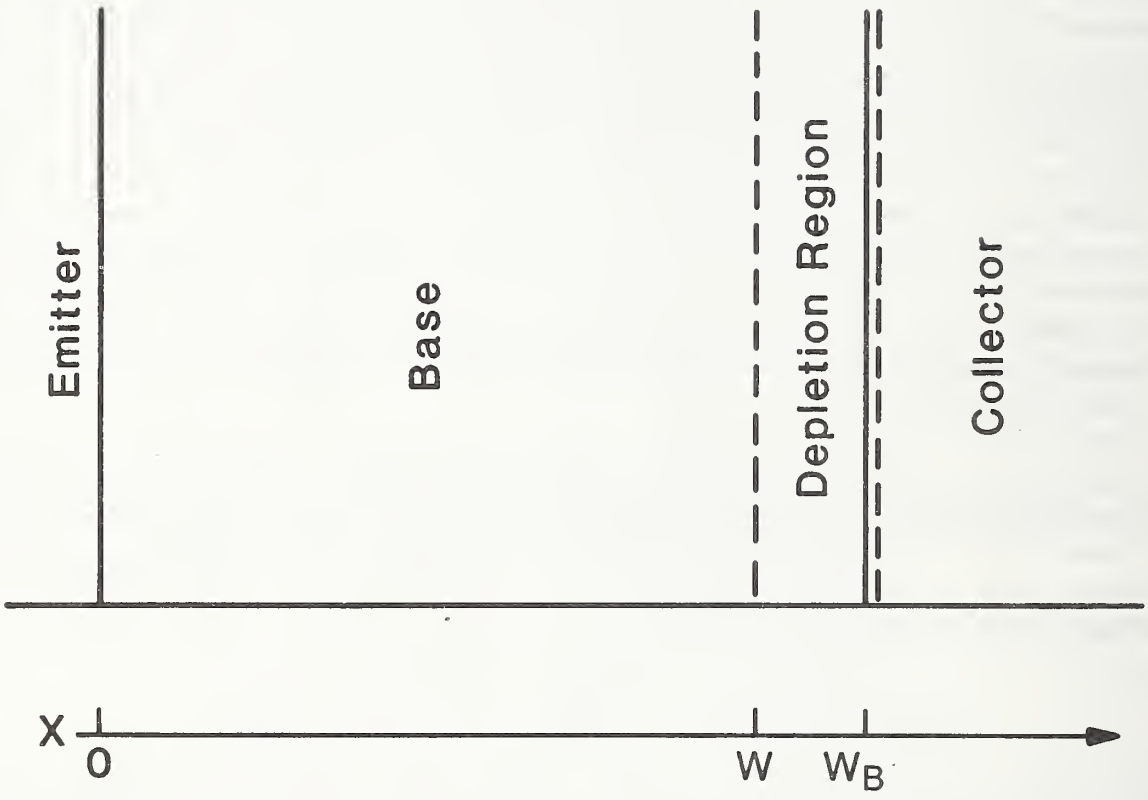


Figure 4. The coordinate system used to develop the IGBT bipolar transistor model. The emitter, base, and collector regions correspond to those indicated on the right half of figure 1.

flows between the collector and base regions due to carrier multiplication and thermal generation within the base-collector depletion region. The holes generated within the base-collector depletion region drift toward the collector edge of the depletion region $x = W_B$, and the electrons drift toward the base edge of the depletion region $x = W$. Therefore, the electron-hole pairs generated within the depletion region constitute a component of base current that flows from the collector. The electron current at the collector edge of the neutral base $x = W$ (base current of fig. 2) is equal to the sum of 1) the MOSFET channel current multiplied by the multiplication factor M, 2) the current due to thermal generation of carriers within the base-collector depletion region I_{gen} multiplied by M, 3) the component of multiplication current due to the hole current entering the depletion region $I_p(W)$, and 4) the displacement currents from the drain-source and gate-drain capacitances:

$$I_n(W) = M \cdot (I_{mos} + I_{gen}) + (M-1) \cdot I_p(W) + (C_{dsj} + C_{gd})\frac{\mathrm{d}V_{ds}}{\mathrm{d}t} - C_{gd}\frac{\mathrm{d}V_{gs}}{\mathrm{d}t}, \qquad (4)$$

where I_{mos}, I_{gen}, and M are given in terms of the state variables of the IGBT (e.g., see table 2).

IGBT State Equations

In this subsection, the expressions for the individual components of currents described above are combined to form the IGBT state equations in table 1. These state equations are expressed in terms of the instantaneous values of the state variables of the IGBT (through the expressions in table 2) and in terms of the instantaneous values of the state variables of the external circuit (through the expressions for I_g and I_T described below). Thus the IGBT state equations are integrated simultaneously with the state equations of the external circuit to simulate the transient waveforms of the IGBT including the interaction with the external circuit. In the next subsection, it is shown how the external circuit state equations are expressed in terms of the state variables of the IGBT and those of the external circuit.

The state equation for the IGBT gate-source voltage, eq (T1.1), is obtained by equating the gate current I_g to the sum of the gate-source and gate-drain displacement currents, and by then solving the resulting expressions for the time rate-of-change of the gate-source voltage where $V_{ds} = V_{bc}$ is used (see fig. 3). The state equation for the base-collector voltage T1.2 is obtained by equating the total anode current I_T to the sum of the electron and hole components at $x = W$ (eqs (2) and (4)), by substituting eq (T1.1) for $\mathrm{d}V_{gs}/\mathrm{d}t$, and by then solving for the time rate-of-change of base-collector voltage where $V_{ds} = V_{bc}$. In integrating the IGBT state equations, eq (T1.2) is evaluated first so that the value of $\mathrm{d}V_{bc}/\mathrm{d}t$ can be used to evaluate eq T1.1.

The state equation eq (T1.3) is obtained from the conservation of total base charge Q. The conservation relation is obtained by integrating the continuity equation, eq (A1.6), across the bipolar neutral base (between $x = 0$ and $x = W$):

$$\frac{\mathrm{d}Q}{\mathrm{d}t} = I_n(W) - \frac{Q}{\tau_{HL}} - I_n(0), \qquad (5)$$

where Q is the integrated excess carrier electron charge in the bipolar transistor base which is required to be equal to the excess hole charge in the bipolar transistor base to maintain the quasi-neutrality condition. This expression indicates that the excess carrier electron charge in the bipolar base is supplied by the electron current entering the base at ($x = W$), and is depleted by the electron current leaving the base at $x = 0$ and by recombination of electrons with holes in the base Q/τ_{HL}. Equation (T1.3) is then obtained using the expression for the base current $I_n(W)$ given by eq (4) and the expression for the boundary condition of the electron current at the emitter edge of the base $I_n(0)$ given in eq (A1.9) where eq (A2.5) is used to express P_0 in terms of the total integrated charge Q.

To analyze the behavior of the IGBT state equations, first consider the stiff gate drive conditions in which the gate voltage is switched rapidly and the switching characteristics are determined by the output characteristics of the power switching device [1,2,7]. For the IGBT, the output capacitance and thus the anode voltage rate-of-rise at turn-off is dominated by the moving boundary redistribution capacitance (last term in the denominator in eq (T1.2)). The redistribution capacitance dominates at turn-off because the ratio of the excess carrier charge to the background mobile carrier charge in the base, Q/Q_B, is much larger than unity for high-level injection (this capacitance also varies with device base lifetime because Q varies with bas lifetime). However, because the base charge Q is zero at the initialization of turn-on, the redistribution capacitance is negligible, and the IGBT can be turned on as rapidly as the structurally equivalent power MOSFET.

Next, consider the dependency of the IGBT switching waveforms upon the gate drive conditions [3]. For gate currents below a critical value, the anode voltage turn-off switching waveforms of the IGBT are determined by the gate current that charges the gate-drain feedback capacitance. Otherwise, for gate current above the critical value determined by $I_g/C_{gd} > I_T/C_{out}$, the anode voltage switching waveforms are determined by the IGBT output capacitance C_{out}. Because the output capacitance of the IGBT is several orders of magnitude larger than that of the MOSFET, the gate current that begins to influence the voltage rate-of-rise at turn-off is several orders of magnitude smaller than that for the MOSFET. This critical value of gate current depends upon the value of base lifetime because the output capacitance depends upon the IGBT base lifetime.

Equations (T1.1) and (T1.2) reduce to those for the structurally equivalent power MOSFET for $Q = 0$ (i.e., for τ_{HL} sufficiently small that Q remains zero). In the INSTANT program described in section IV, the IGBT state equations can be used to describe the structurally equivalent power MOSFET by assigning $\tau_{HL} < 0$. This option sets $Q = 0$ and does not evaluate eq (T1.3). In addition, the emitter-base diffusion potential described below is set to zero for the MOSFET. Although the IGBT model equations mathematically reduce to those for the MOSFET at arbitrarily small τ_{HL}, the MOSFET option of INSTANT prevents the overflows that would occur in the numerical calculations if the lifetime were set to zero to describe the MOSFET.

Conductivity–Modulated Base Resistance

In order to express the external circuit state equations in terms of the IGBT state variables and the external circuit state variables, the IGBT anode-cathode terminal voltage V_A must be expressed in terms of the internal IGBT state variables. The anode-cathode voltage of the IGBT is given by the sum of the emitter-base voltage, the MOSFET drain-source voltage (equal to the base-collector voltage), and a series resistive drop due to the resistance of the bond wire, the spreading resistance at the bond, and metallization resistance:

$$V_A = V_{eb} + V_{bc} + I_T \, R_s. \tag{6}$$

The base-collector voltage is an IGBT state variable and the series resistive drop is calculated from the anode current I_T which is determined by the external circuit. The IGBT emitter-base voltage is analyzed in appendix 3 using the ambipolar transport equations of appendix 1 [1,7].

The emitter-base voltage consists of three components as indicated in figure 3: the potential drop across the conductivity-modulated base resistance, the diffusion capacitance potential, and the depletion capacitance potential, which is important for reverse blocking. The emitter-base voltage can be expressed in the form:

$$V_{eb} = V_{ebq}(V_{bc}, Q) + I_T \cdot R_b(V_{bc}, Q), \tag{7}$$

where the conductivity-modulated base resistance R_b and the potential drop across the emitter-base capacitance V_{ebq} are functions of the instantaneous values of V_{bc} and Q [3,4]. The expression given in table 3 for R_b in the forward bias case ($Q > 0$) is obtained by identifying the second term in eq (7) as the first term in eq (A3.4), where the expression for μ_{eff} is used so that R_b reduces to the low-level injection, non-conductivity-modulated base resistance for small values of Q. The expression for the emitter-base diffusion potential V_{ebd} (equal to V_{ebq} in the forward bias injection regime $Q \gg 0$) is obtained by identifying the first term in eq 7 as the sum of eq (A3.2) and the second term in eq (A3.4). In the INSTANT program, the series resistance R_s of eq (6) is included in the evaluation of R_b for simplicity.

The values of electron and hole mobilities used for the forward-bias emitter-base voltage μ_{nc} and μ_{pc} are functions of bias due to the carrier-carrier scattering effect [17]. The carrier-carrier scattering component of mobility is accounted for by adding the scattering frequencies (or equivalently inverse mobilities) due to carrier-carrier scattering μ_c and due to ionized impurity scattering and lattice μ_n and μ_p. The inverse mobility due to carrier-carrier scattering is given in terms of the free carrier level by [17]:

$$1/\mu_c = [\overline{\delta p} \ln(1 + \alpha_2(\overline{\delta p})^{-2/3})]/\alpha_1, \tag{8}$$

where the excess carrier concentration at the center of the base $\overline{\delta p}$ is used to represent the average free carrier density in the base. In general, the expression for μ_c must be solved

implicitly during simulations because it depends upon the value of $\overline{\delta p}$ which is calculated using the value of μ_c.

In the dynamic model, the expression for V_{eb} (eq (7)) depends upon the instantaneous values of both Q and I_T independently of each another. This becomes important for rapid turn-on conditions where the MOSFET portion of the device is switched on rapidly and the total load current I_T flows through the base before sufficient excess carrier charge Q is present to modulate the conductivity of the base. The emitter-base voltage at turn-on may be as large as the on-state voltage of the structurally equivalent power MOSFET, because Q is zero at the initiation of the turn-on and R_b is equal to the non-conductivity-modulated epitaxial layer resistance for $Q < Q_B$. However, Q rapidly approaches a value that is sufficient to modulate the resistance, because the steady-state charge is typically several orders of magnitude larger than the background concentration.

The emitter-base junction depletion capacitance C_{ebj} indicated on figure 3 is important when the emitter-base junction is reverse biased or has a small forward bias, but for larger forward biases, the emitter-base diffusion capacitance C_{ebd} is dominant. In the model, C_{ebj} is accounted for using the same state variable Q that accounts for C_{ebd}. For negative values of Q, the emitter-base junction is reverse biased (reverse blocking) and the state variable Q describes the space charge of the emitter-base depletion region. For this case, V_{eb} is given by the sum of the potential across the non-conductivity-modulated epitaxial layer resistance and the potential across the emitter-base junction depletion capacitance. A continuous transition between C_{ebj} and C_{ebd} is imposed by using the larger of the two capacitances (or equivalently the minimum of the capacitor voltages) for small forward biases. The base and collector current expressions also differ for reverse blocking (not indicated in the state equations of table 1).

III. INTERACTION WITH EXTERNAL CIRCUITS

To describe the dynamic behavior of IGBTs in different circuits, the IGBT state equations are combined with the state equations of the external circuit. To evaluate the IGBT state equations, the anode current and the gate current must be expressed in terms of the state variables of the system. The state variables of the system consist of the state variables of each IGBT (Q, V_{gs}, V_{bc}) and the state variables of the external circuit (inductor currents and capacitor voltages). The external circuit state equations are obtained by expressing the inductor voltages and the capacitor currents in terms of the state variables of the system. The inductor voltages are used to form the state equations for the inductor currents using $\mathrm{d}I_L/\mathrm{d}t = V_L/L$, and the capacitor currents are used to form the state equations for the capacitor voltages using $\mathrm{d}V_C/\mathrm{d}t = I_C/C$. In general, the expressions for the gate and anode currents of the IGBTs, the external circuit inductor voltages, and the external circuit capacitor currents are obtained by applying Kirchhoff's current and voltage laws assuming that the state variables of the system are known.

To simplify this process, the circuit can be represented schematically using the simplified elements shown in figure 5. In this representation, the IGBTs within the circuit are

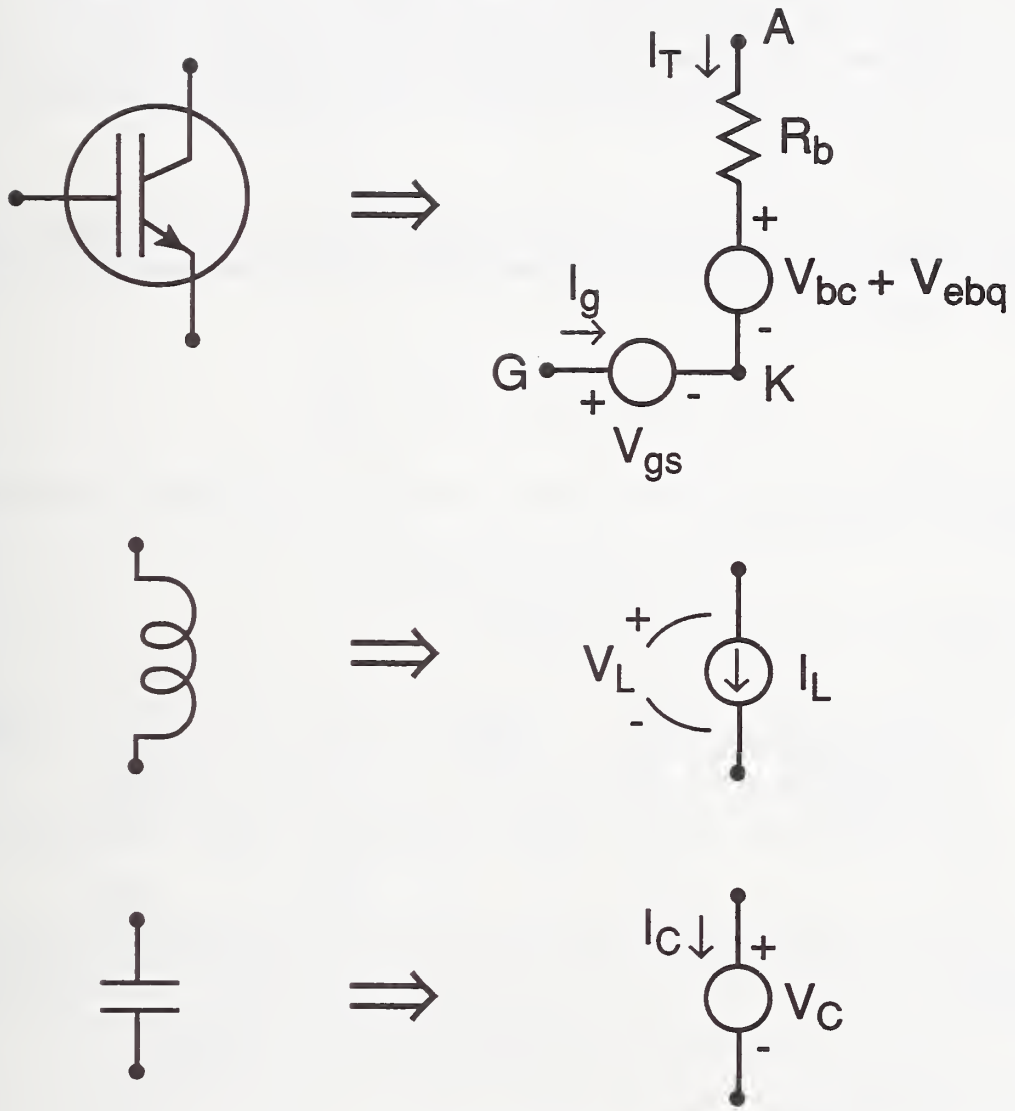


Figure 5. Simplified circuit element transformations for use in deriving external circuit state equations from Kirchhoff's laws.

replaced by a known voltage source between the gate and cathode terminals and a known voltage source in series with a known resistor between the anode and cathode terminals. The values of V_{bc} and V_{gs} are assumed to be known because they are state variables, and the values of R_b and V_{ebq} are assumed to be known because they are evaluated directly in term of the IGBT state variables, using the expressions in table 3. In addition, the external circuit capacitors are replaced by a known voltage source, and the external circuit inductors are replaced by known current source. Using the resulting simplified circuit, Kirchhoff's current and voltage laws are then applied to obtain the expressions needed to evaluate the IGBT state equations and to form the external circuit state equations.

Series Resistor-Inductor Load

As an example, consider the dynamic behavior of the IGBT for the series resistor-inductor load circuit and the resistive drive circuit shown in figure 6. The load circuit state equation for the circuit of figure 6 is:

$$\frac{\mathrm{d}I_L}{\mathrm{d}t} = \frac{1}{L_L}(V_{AA} - R_L \cdot I_L - V_A), \tag{9}$$

where $I_T = I_L$ for this circuit and V_A is given by eqs (6) and (7). The gate current for the circuit of figure 6 is given by:

$$I_g = (V_{gg} - V_{gs})/R_g, \tag{10}$$

where the gate pulse generator voltage is given by:

$$V_{gg} = \begin{cases} 0 & \text{for} \quad t \le t_{on} \\ V_{gon}(t - t_{on})/t_{rise} & \text{for} \quad t_{on} < t < t_{on} + t_{rise} \\ V_{gon} & \text{for} \quad t_{on} + t_{rise} < t < t_{off} \\ V_{gon}(t_{off} + t_{fall} - t)/t_{fall} & \text{for} \quad t_{off} < t < t_{off} + t_{fall} \\ 0 & \text{for} \quad t \ge t_{off} + t_{fall} \end{cases} . \tag{11}$$

The pulse generator rise and fall times are described by the second and fourth cases in eq (11). The initial conditions of the state variables before the initiation of the gate pulse are $V_{gs} = 0$, $Q = 0$, $V_{bc} = V_{AA}$, and $I_L = 0$. To simulate the dynamic operation of the IGBT in different circuits, only the circuit state equations need to be changed.

Polarized Turn-Off Snubber

To include the protection circuit shown in figure 7, the state equation

$$\frac{\mathrm{d}V_S}{\mathrm{d}t} = \begin{cases} -\dfrac{V_S - V_{SS}}{R_B C_S} & \text{for} \quad V_A \le V_S + V_{bi} \\ \dfrac{V_A - V_S - V_{bi}}{C_S R_D} - \dfrac{V_S - V_{SS}}{R_B C_S} & \text{for} \quad V_A > V_S + V_{bi} \end{cases} \tag{12}$$

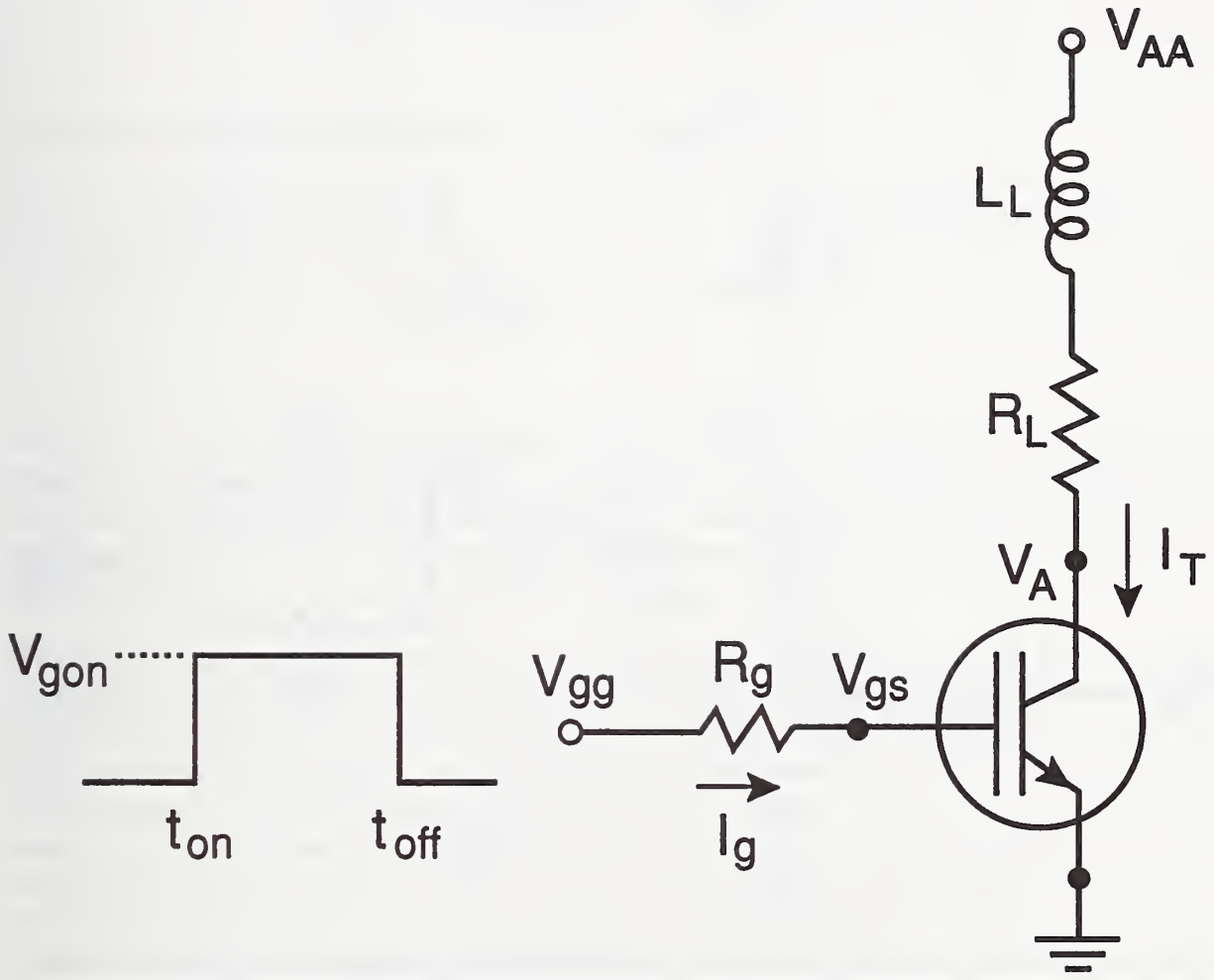


Figure 6. The circuit configuration of an IGBT with a series resistor-inductor load and a resistive gate drive.

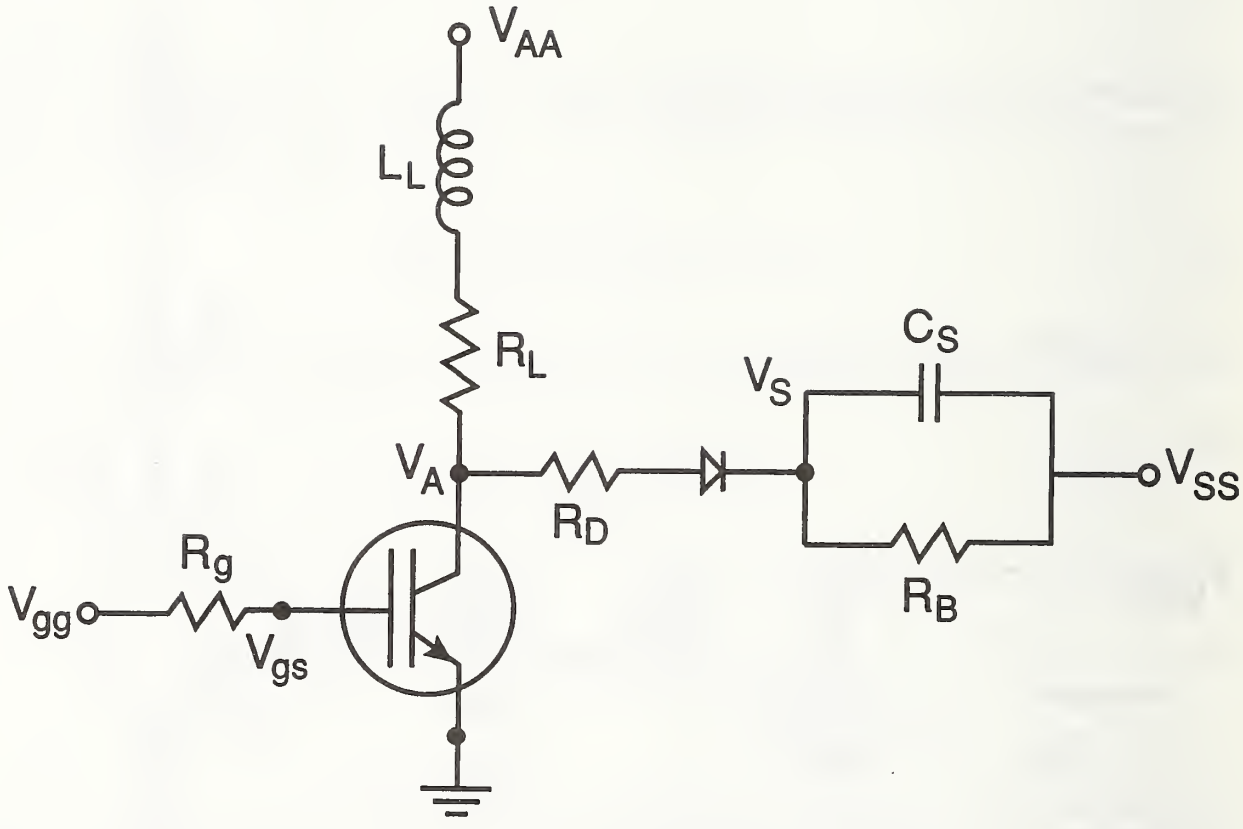


Figure 7. The circuit configuration of an IGBT with a series resistor-inductor load, a resistive gate drive, and a polarized turn-off snubber or soft clamp protection circuit.

is added. The anode current for this loading condition is given in terms of the state variables I_L, V_A, and V_S by

$$I_T = \begin{cases} I_L & \text{for} \quad V_A \leq V_S + V_{bi} \\ I_L - \dfrac{V_A - V_S - V_{bi}}{R_D} & \text{for} \quad V_A > V_S + V_{bi} \end{cases}, \tag{13a}$$

and the anode voltage is given by

$$V_A = \begin{cases} V_{ebq} + V_{bc} + I_L \cdot R_b & \text{for} \quad V_A \leq V_S + V_{bi} \\ \dfrac{I_L R_b R_D + (V_S + V_{bi}) R_b + (V_{ebq} + V_{bc}) R_D}{R_b + R_D} & \text{for} \quad V_A > V_S + V_{bi} \end{cases}, \tag{13b}$$

where R_b is the conductivity-modulated base resistance of the IGBT including the series resistance R_s (see eqs (6) and (7)). Because the diode is modeled by a voltage offset V_{bi} and a small resistance R_D for the forward-bias condition and by an open circuit for the reverse-bias condition, the two cases require the two different expressions in both eq (12) and eq (13).

The bleeder resistor R_B is used to determine the initial condition of the snubber voltage at the time the turn-off transient is initiated. If the bleeder resistor is connected to V_A instead of to the constant voltage supply, the protection circuit is commonly referred to as a polarized turn-off snubber (or shunt snubber) [18,19]. In this case, the initial condition of V_S depends on the frequency and the duty cycle for a given R_B, but for long on-state times, it approaches the IGBT on-state voltage. If the snubber supply voltage is connected as shown in figure 7, the protection circuit reduces to a voltage clamping circuit [20]. For this configuration, the initial condition of V_S depends on the frequency for a given bleeder resistor, but it approaches V_{SS} for single pulses (low frequencies) and $V_{SS} \geq V_{AA}$. For a repetitive waveform, the initial condition is obtained by iterating the solution until $V_S(t+T) = V_S(t)$ where T is the period of the repetitive waveform.

Polarized Active Feedback Snubber

Figure 8 shows the circuit configuration for the IGBT with a series resistor-inductor load, a polarized gate drive resistance, and a series resistor-capacitor external feedback circuit. For this protection circuit, an additional state equation for the potential across the external feedback capacitor V_{cf} is necessary:

$$\frac{\mathrm{d}V_{cf}}{\mathrm{d}t} = \frac{I_f}{C_f}, \tag{14}$$

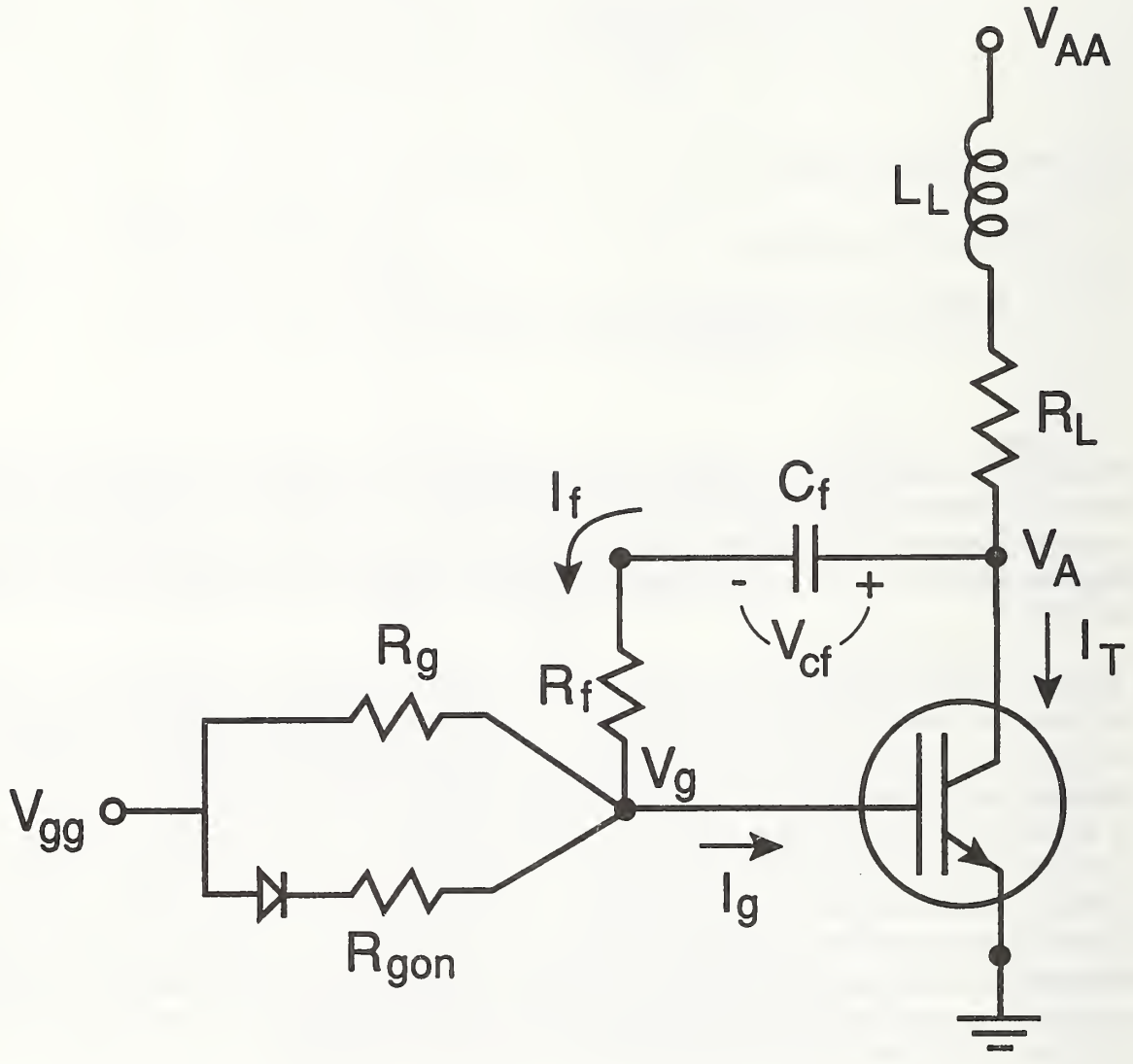


Figure 8. The circuit configuration of an IGBT with a series resistor-inductor load, a polarized gate drive resistance, and a series resistor-capacitor feedback circuit.

where the feedback current is given by:

$$I_f = (V_A - V_{cf} - V_{gs})/R_f. \tag{15}$$

For this circuit, the IGBT anode current is given by $I_T = I_L - I_f$, and the anode voltage is obtained in terms of the state variables by combining this expression with eqs (6) and (7). The expression for the gate current of eq (10) is replaced by:

$$I_g = \begin{cases} I_f + (V_{gg} - V_{gs})/R_g & \text{for} \quad V_{gg} < V_{gs} + V_{bi} \\ I_f + (V_{gg} - V_{gs})/R_g & \\ \quad +(V_{gg} - V_{gs} - V_{bi})/R_{gon} & \text{for} \quad V_{gg} \geq V_{gs} + V_{bi} \end{cases}, \tag{16}$$

where the diode is modeled as a voltage offset V_{bi} and a 1-Ω effective series resistance that is included in R_{gon}. The initial condition for the feedback capacitor voltage before the initiation of the gate voltage pulse is $V_{cf} = V_{AA}$.

Paralleled IGBT Operation

Finally, the circuit configuration of two paralleled IGBTs is shown in figure 9, where the lead inductances are not considered in this particular example. A simplified schematic representation of figure 9 is shown in figure 10 using the element transformations indicated in figure 5. By applying Kirchhoff's current and voltage laws to the circuit of figure 10, the necessary expressions are obtained for the inductor voltage and the gate and anode currents for the two IGBTs. The anode voltage of the IGBTs is given by:

$$V_A = \left(I_L + \frac{V_{bc1} + V_{ebq1}}{R_{b1}} + \frac{V_{bc2} + V_{ebq2}}{R_{b2}} \right) \frac{R_{b1} R_{b2}}{R_{b1} + R_{b2}}. \tag{17}$$

The IGBT anode currents for this circuit are given by:

$$I_{T1} = \frac{V_A - V_{bc1} - V_{ebq1}}{R_{b1}} \quad \text{and} \quad I_{T2} = \frac{V_A - V_{bc2} - V_{ebq2}}{R_{b2}}. \tag{18}$$

The IGBT gate currents are given by:

$$I_{g1} = \frac{V_{gg} - V_{gs1}}{R_{g1}} \quad \text{and} \quad I_{g2} = \frac{V_{gg} - V_{gs2}}{R_{g2}}. \tag{19}$$

These equations in conjunction with eqs (9) and (11) form the state equations for the circuit of figure 10, where each IGBT contributes three state equations. The initial conditions for each of the IGBTs are the same as for the single IGBT described above.

IV. INSTANT - IGBT NETWORK SIMULATION AND TRANSIENT ANALYSIS TOOL

In this section, a general overview of the operation and use of the INSTANT software package is given. The INSTANT program is based upon the IGBT device model presented

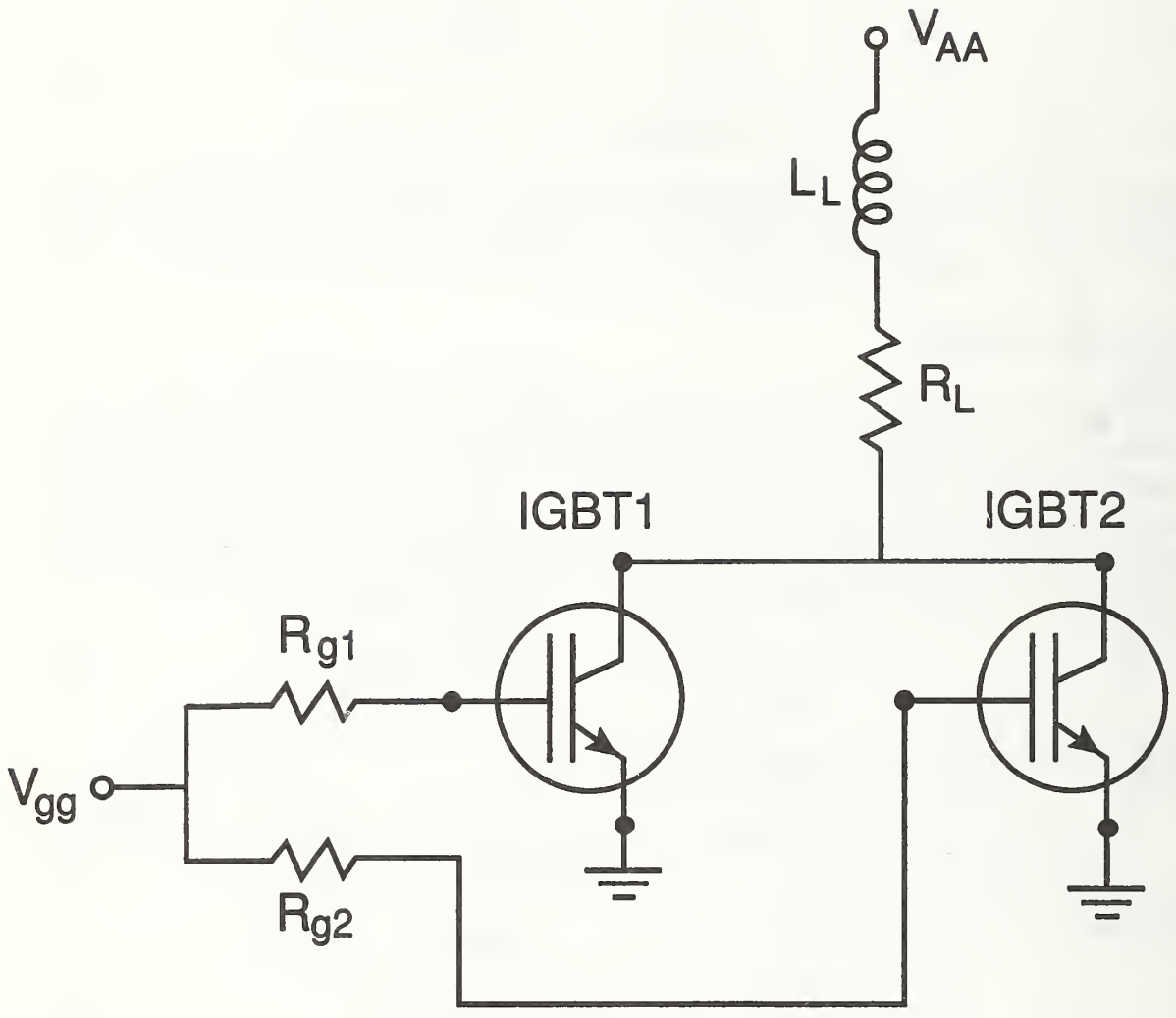


Figure 9. The circuit configuration of two paralleled IGBTs, with a common series resistor-inductor load, and separate resistive gate drive circuits.

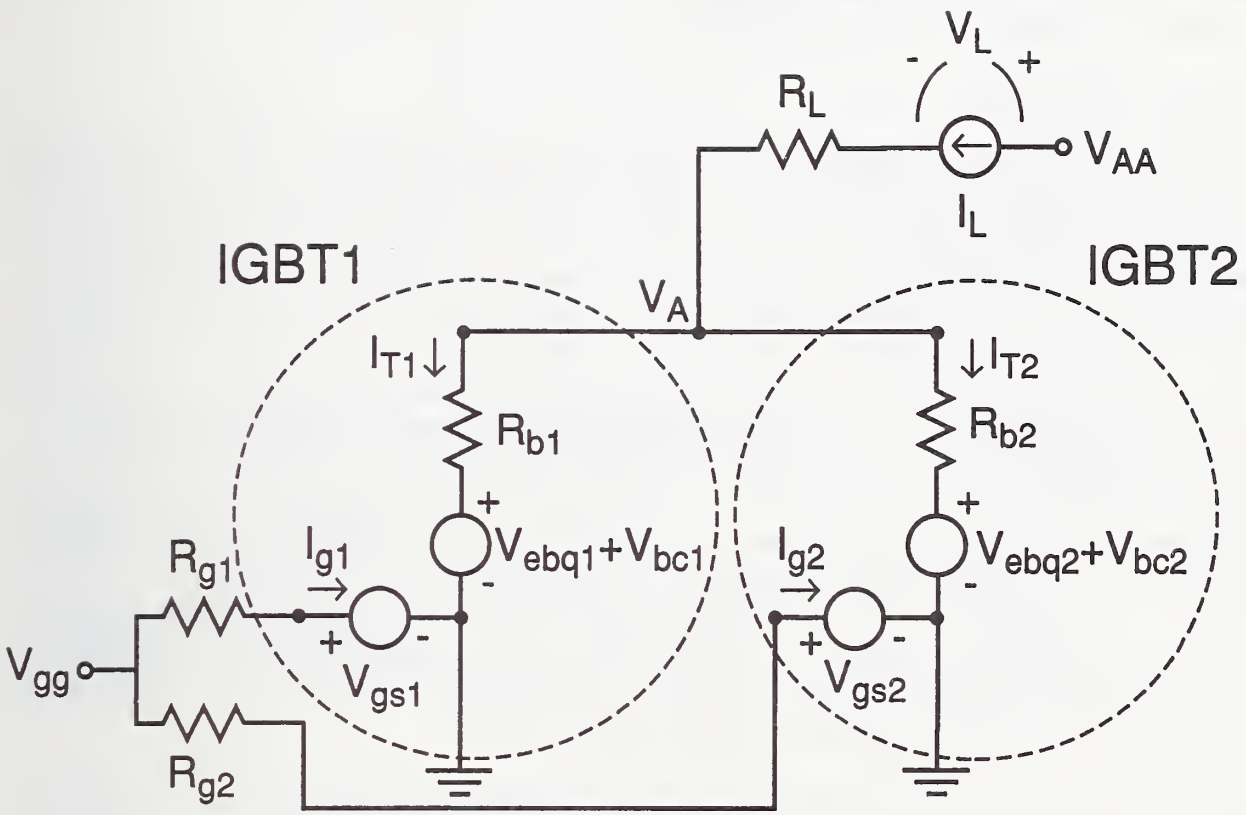


Figure 10. A simplified schematic representation of figure 9 obtained using the element transformations indicated in figure 5. This schematic is used to obtain the external circuit state equations.

in section II and is applicable to general external circuits as described in section III. INSTANT is written in generally portable FORTRAN code and is available with graphics libraries for various PC, VAX, and Sun FORTRAN compilers and graphics Windows environments [11]. The INSTANT software package contains the complete software source code, a graphics library for the specified FORTRAN compiler, and executable programs for the example circuits described in section III along with example input files for the device and circuit parameters. The INSTANT software package also contains the document file given in appendix 4 that describes each of the files on the disk, the variable names used in the source code, and the procedure used to execute the programs and to generate executable programs for different circuits.

INSTANT Operation

The INSTANT program (appendices 5-10) simulates the interaction of the IGBT with the external drive, load, and feedback circuits. This is accomplished by simultaneously integrating the state equations of the IGBT with those of the external circuit, where the expressions for the IGBT anode current I_T and gate current I_g are determined by the external circuit configuration and where the expression for the IGBT anode-cathode terminal voltage V_A is obtained in terms of the state variables using eqs (6) and (7) (e.g., see sec. III). The simultaneous integration of the state equations is performed using the readily available RKF45 subroutine [21] where the initial conditions are obtained from a known steady-state condition. The RKF45 subroutine uses an automatic Runge-Kutta-Fehlberg method to evaluate iteratively a user-defined subroutine that contains the state equations. To simplify the implementation of different circuits and circuits with multiple IGBTs, the IGBT model within INSTANT is implemented in two subroutines [4]; the first subroutine IGBTSEQ† is given in appendix 6 and evaluates the IGBT state equations (tables 1 and 2), and the second subroutine IGBTVeb is given in appendix 7 and evaluates the emitter-base capacitor voltage V_{ebq} and the conductivity-modulated base resistance R_b (tables 2 and 3) which includes the series resistance R_s.

Figure 11 shows the simplified flowchart for the INSTANT program where the user-defined subroutines for a given circuit are explained on the right. The INSTANT main program is also given appendix 5. To simulate a given circuit, the user needs only to create the three user-defined subroutines and to link them with the INSTANT software package as described below. The program begins by calling the user-defined subroutine INPUT. This subroutine reads the IGBT parameters from a parameter input file by calling the subroutine IGBTINP provided within the INSTANT software package, and reads the circuit parameters for the given circuit from the circuit parameter input file. Subroutine INPUT then sets the initial conditions for the state variables and sets the output and plotting parameters to be used by subroutine OUTPUT. The parameters initialized within subroutine INPUT are passed to the other user-defined subroutines using the common blocks /IOpar/, /CIRCpar/, and /IGBTpar/. If circuits contain multiple IGBTs with different parameters, each parameter set that is read from disk with IGBTINP can be stored in a different model parameter

† The "sans serif" symbols throughout the text represent computer mnemonics.

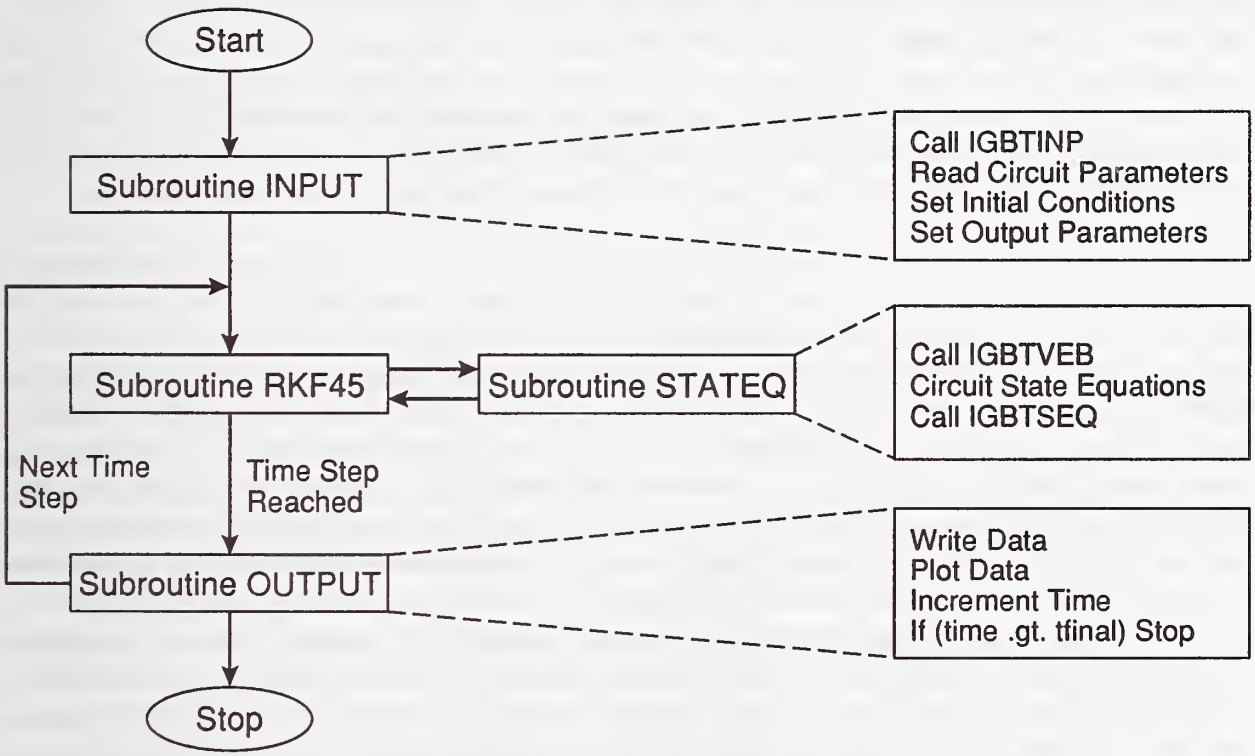


Figure 11. Simplified flowchart of the INSTANT circuit simulation program where the three user-defined subroutines are explained on the right.

array using subroutine IGBTSTO, and the parameters can be recalled to the common block /IGBTpar/ when the IGBT model is evaluated for each device using IGBTREC. Subroutines IGBTINP, IGBTSTO and IGBTREC are given in appendix 8.

After returning from subroutine INPUT, INSTANT calls subroutine RKF45 which repetitively evaluates the user-defined subroutine STATEQ to advance the system state variables to the next time step within the specified precision. The user-defined subroutine STATEQ evaluates the device and circuit state equations for the given circuit. This subroutine first calls the subroutine IGBTVeb supplied within the INSTANT software package to evaluate the emitter-base capacitor voltage and the base resistance for each IGBT in terms of the instantaneous values of the state variables of each IGBT. These values are used to evaluate the circuit expressions for the gate currents, the anode currents, the capacitor currents, and the inductor voltages, so that the state equations of the external circuit and the state equations of the IGBTs can be evaluated, as described in section III. The IGBT state equations are evaluated by calling IGBTSEQ which requires as its input the gate and anode currents as well as the instantaneous values of the IGBT state variables.

As previously mentioned, the model equations that describe carrier-carrier scattering in the neutral base and velocity saturation in the collector base depletion region must be solved implicitly. The mobility reduction due to high free-carrier levels has a second-order effect on the on-state emitter-base voltage [1] and is implemented iteratively within the IGBTVeb subroutine [4]. The implicit equation is evaluated using the readily available function ROOT (subroutine ZEROIN in ref. [21]) which iteratively evaluates the function Dccs given in appendix 9 to calculate the value of diffusivity including the carrier-carrier effect. Using the parameter ccsflg in the device input parameter list, the carrier-carrier scattering effect can be neglected (ccsflg < 0) for faster computation speed, or included for more accuracy of on-state voltage (ccsflg > 0). The space charge concentration due to velocity saturation within the base-collector depletion region has a second-order effect on the time rate-of-change of the base-collector voltage [1] and is implemented iteratively within IGBTSEQ [4]. This implicit equation is evaluated using the function ROOT which evaluates iteratively the function spachg given in appendix 10 to calculate the base-collector space charge density including the velocity saturation. The effect of the velocity saturation in the base-collector depletion region can be included or neglected using the parameter sclflg.

Once RKF45 has reached the next time step, subroutine OUTPUT is called (see fig. 11). This subroutine writes and plots the data at that time step. The time step is then incremented within subroutine OUTPUT, and control is returned to the INSTANT main program which continues the process of alternately calling subroutines RKF45 and OUTPUT until subroutine OUTPUT detects that the final time step has been reached. For the given circuit to be simulated, the user must supply a file containing subroutines INPUT, STATEQ, and OUTPUT which in turn reference the INSTANT-supplied subroutines IGBTINP, IGBTVeb, and IGBTSEQ to describe the IGBTs. In effect, the three user-defined subroutines completely describe the device and circuit equations, the model parameters, and the program control for the simulation, where the IGBT equations are implemented

by simply calling subroutines.

Using INSTANT

Figure 12 shows an example of subroutine STATEQ for the circuit of figure 6. The inputs from RKF45 are the time and the instantaneous values of the system state variables (**Y**), and the outputs are the time rate-of-change of the state variables (**YP**) as evaluated by the system state equations. This example has four state variables: one for the inductor current and the three IGBT state variables. The circuit parameters that are designated within subroutine INPUT are obtained through the common block /CIRCpar/, but the IGBT parameters are not needed in this subroutine because they are passed directly from subroutine IGBTINP to subroutines IGBTVeb and IGBTSEQ through the common block /IGBTpar/. In the "Evaluate functions of state variables" segment of the subroutine in figure 12, IGBTVeb is called to evaluate R_b and V_{ebq} so that the values of V_A, I_g, and I_T can be evaluated in terms of the instantaneous values of the state variables using the circuit equations. These values are used in the "Evaluate state equations" segment to evaluate the state equations for the inductor current and to evaluate the IGBT state equations using IGBTSEQ.

Figure 13 shows the file organization of the INSTANT software package. For a given circuit the user must create the file called, for example, Circuit.for that contains the three user-defined subroutines: INPUT, STATEQ, and OUTPUT. Appendices 11 through 14 contain user-defined circuit source code files for the example circuits discussed in section III, figures 6 through 9, respectively. The user then executes the batch file Linkcirc.bat with the circuit source code file name (e.g., Circuit in this example) as a batch file parameter to create an executable program called in this example Circuit.exe. The Linkcirc.bat batch file compiles the user-defined circuit subroutines and links them with the INSTANT-supplied subroutines and the graphics library. Finally, the user executes the circuit program and enters the names of the device parameter input file, the circuit parameter input file, and the output data file. Figure 14 shows typical device and circuit input files for a 7.1-μs base lifetime IGBT, a 30-Ω, 80-μH load, and a 500-Ω gate resistance. These parameters can be changed with an ASCII text editor without recompiling the circuit routines.

As an example, figure 15 demonstrates the typical user input (a) and real-time graphics output (b) of INSTANT for an IGBT being switched on and off for the circuit of figure 6. When the circuit program name is entered (e.g., Circuit.exe), the program first requests the names of the input and output files. After the file names are entered by the user (e.g., Device.IGT, Circuit.inp, and Output.dat), the plot of figure 15b appears on the computer graphics screen and the curves are drawn as they are computed at each time step of the integration. The curves of figure 15b are scaled in subroutine output so that the expected range of the curves will fit on the plot, and the gate current is offset to the center of the vertical axis because it is negative at turn-off. This simulation takes about 30 s on a 12-MHz, 386 microcomputer and takes about 2 s on a Sun SPARC station 2. Because the waveforms are drawn as they are calculated, the simulations can be interrupted at any point of the integration to speed the design process. When the simulation is complete,

```
C ***************************************************************************
C
C *** Subroutine to evaluate the state equations of the device and circuit.
C
      SUBROUTINE STATEQ (Time, Y, YP)
C
C *** Designate the number of state equations and declare the calling
C     arrays for the state variables and their time derivatives.
C
      INTEGER NEQN
      PARAMETER (NEQN=4)
      REAL Y(NEQN),YP(NEQN),time
C
C *** Designate external functions.
C
      REAL Pulsgen
      EXTERNAL Pulsgen
C
C *** Declare labeled common block for circuit parameters.
C
      REAL             LL,RL,Vaa,Rg,Vggon,ton,toff,trise
      COMMON /CIRCpar/ LL,RL,Vaa,Rg,Vggon,ton,toff,trise
C
C *** Declare names for state variables and their time derivatives.
C
      REAL Vcb,Qte6,IL,Vgs
      REAL DVcb,DQte6,DIL,DVgs
C
C *** Declare names for functions of state variables.
C
      REAL Va,Ig,Vgg,It,Rb,Vebq
C
C *** Define names for state variables in terms of the calling array.
C
      Vcb   =Y(1)
      Qte6  =Y(2)
      IL    =Y(3)
      Vgs   =Y(4)
C
C *** Evaluate functions of state variables.
C
      call IGBTVeb (Qte6,Vcb,Rb,Vebq)
      Va= IL*Rb + Vcb + Vebq
C
      It=IL
      Vgg=Pulsgen(time,ton,toff,trise,trise,Vggon)
      Ig=(Vgg-Vgs)/Rg
C
C *** Evaluate the state equations.
C
      call IGBTSEQ(Vgs,Vcb,Qte6,Ig,It,DVgs,DVcb,DQte6)
      DIL=1.0/LL*(-IL*RL-Va+VAA)
C
C *** Define return array for time derivatives of state variables.
C
      YP(1)=DVcb
      YP(2)=DQte6
      YP(3)=DIL
      YP(4)=DVgs
C
      RETURN
      END
C
C ***************************************************************************
```

Figure 12. An example of the user-defined subroutine STATEQ for the circuit of figure 6.

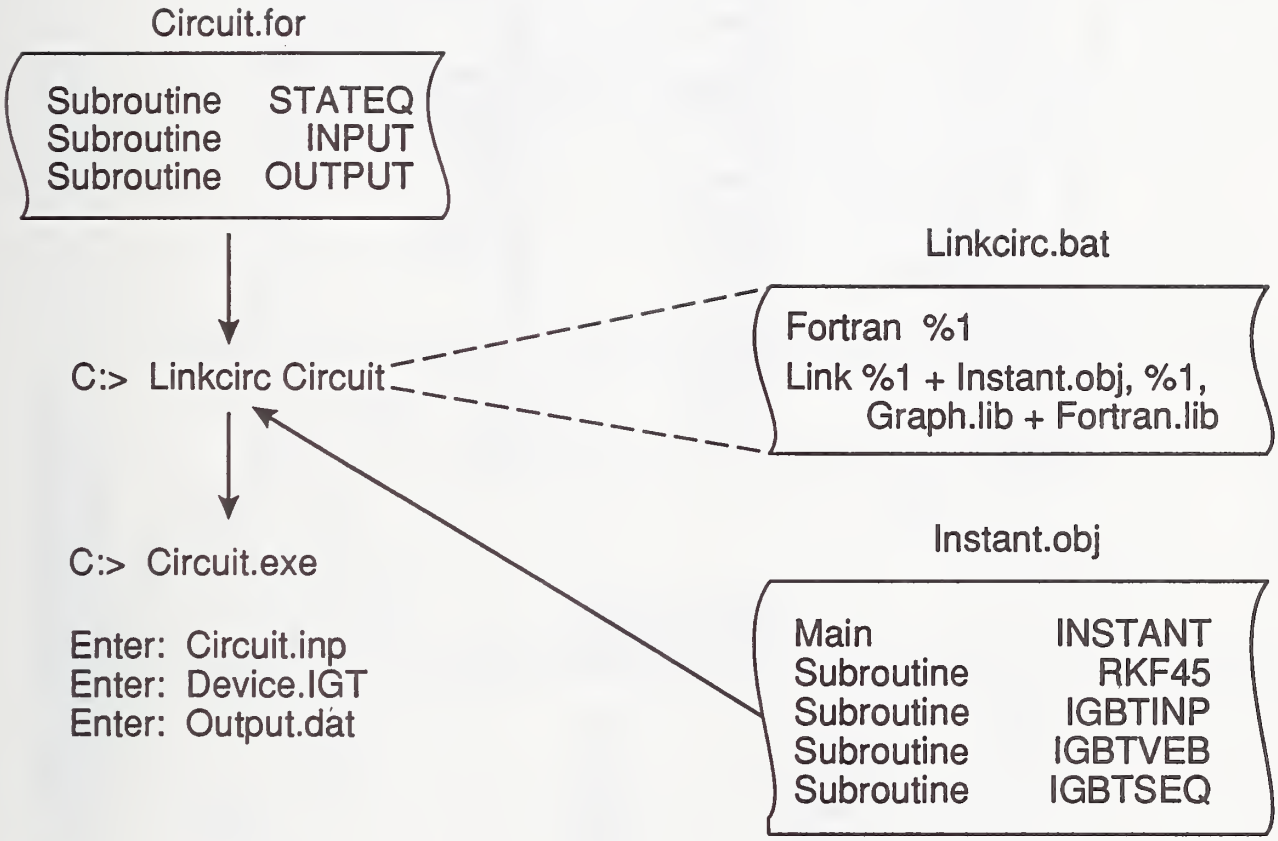


Figure 13. File organization of the INSTANT software package indicating the use of Linkcirc.bat to create a circuit simulation program from the three user-defined subroutines.

Device.IGT

7.1e-6	t_HL	(s)
0.0093	w_B	(cm)
2.0e4	N_B	(cm**-3 * E-10)
0.1	A	(cm**2)
6.5e-14	Isne	(A)
4.7	Vt	(V)
0.38	Kpsat	(A/V**2)
0.7	Kplin	(A/V**2)
0.02	Rs	(ohm)
0.01	theta	(1/V)
0.62e-9	Cgs	(F)
0.05	Agd	(cm**2)
1.75e-9	Coxd	(F)
0.0	Vtd	(V)
4.0	BVn	
2.0	BVf	
-1.0	ccsflg	(+/-)
-1.0	sclflg	(+/-)

Circuit.inp

30.0	RL
80.e-6	LL
300.0	Vaa
500.0	Rg
20.0	Vgon
1.0e-6	ton
20.0e-6	toff
0.1e-6	trise
30.0e-6	tfinal
0.0e-6	tplot

Figure 14. Example device and circuit input files for the series resistor-inductor load with a resistive gate drive.

C:> Circuit.exe

Enter file to read device input parameters from:

Device.IGT

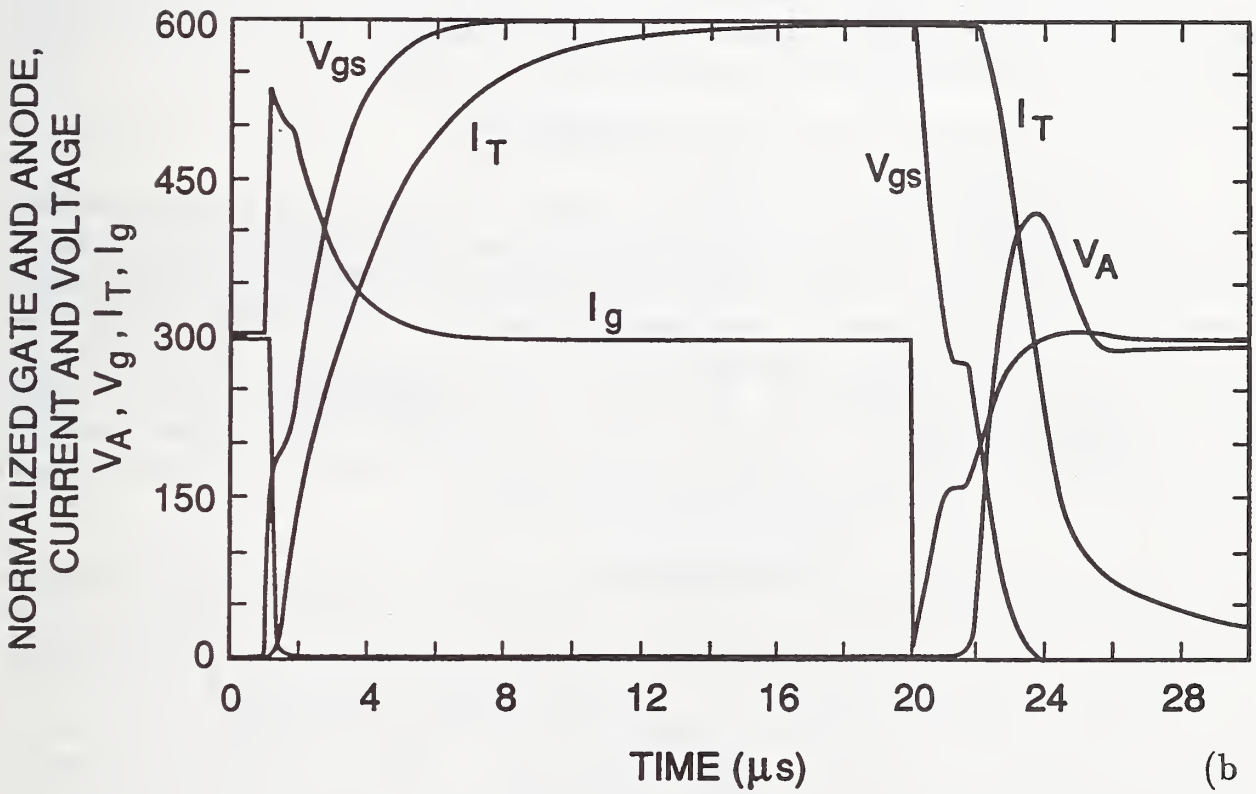
Enter file to read circuit input parameters from:

Circuit.inp

Enter file to write data to:

Output.dat

(a



(b

Figure 15. Example of the user input (a) and real-time graphics output (b) of the INSTANT software for the example of a series resistor-inductor load with a resistive gate drive.

the plot can be printed directly on a graphics-compatible dot-matrix printer or Postscript laser printer.

Initially at $t = 0$, the gate voltage is zero and the IGBT is in the off-state. Because the IGBT is in the off-state, the anode current is zero, and the anode voltage is equal to the anode supply voltage (300 V). At $t = 1$ μs, the pulse generator is switched on so gate current begins to flow into the gate and the gate voltage begins to rise. Once the gate voltage exceeds the threshold voltage, the anode voltage falls rapidly to near its on-state value, and the anode current begins to rise at a rate that is determined by the load inductance. At $t = 20$ μs, the device and circuit have nearly reached the steady-state condition. At this point, the gate voltage pulse generator is switched off so current begins to flow out of the gate, and the gate voltage begins to fall. Once the gate voltage has fallen to the value where the MOSFET enters the saturation region, the anode voltage begins to rise slowly, and the gate voltage remains constant as the gate-drain overlap oxide capacitance is discharged. Once the gate-drain overlap becomes depleted, the gate-drain capacitance is reduced by about two orders of magnitude, and the anode voltage rises at a rate that is determined by the IGBT effective output capacitance. The anode voltage overshoots the supply voltage due to the large load inductance. The anode current initially falls at a rate that is determined by the load inductance and then tails off at a slower decay rate due to the slowly decaying excess carrier charge in the base.

V. PARAMETER EXTRACTION ALGORITHMS

In this section, the algorithms that have been developed to extract the IGBT model parameters from computer-controlled measurements are discussed. Because the characteristics of the internal MOSFETs and bipolar transistors are convoluted in the steady-state terminal characteristics of merged power devices such as the IGBT, and because the conductivity-modulated devices exhibit non-quasi-static behavior, the dynamic characteristics must in general be examined to characterize the devices and to extract model parameters. This is in contrast to microelectronic devices where the steady-state current-voltage terminal characteristics in conjunction with interelectrode capacitance-voltage characteristics are sufficient to extract most of the device model parameters.

The dynamic measurements require high precision and the ability to make calculations on waveforms obtained from computer-controlled measurements. In addition, calculations are required to separate the measured characteristics into the characteristics of the internal MOSFETs and bipolar transistors. The basic measurement system used to do this is shown in figure 16a and consists of a computer that controls power supplies, a waveform digitizer, a temperature controller, and a curve tracer. Figure 16b shows an example of a circuit configuration used to measure the high-voltage and high-current steady-state characteristics which require a pulsing capability to avoid excess heating for the high-power measurements. Figure 16c shows an example of a circuit configuration used to measure the dynamic characteristics which require a high current gate pulse generator, a high-resolution single event transient digitizer, and a low-inductance bypass capacitor for the anode power supply. Various software tools and programmable electronic instruments are

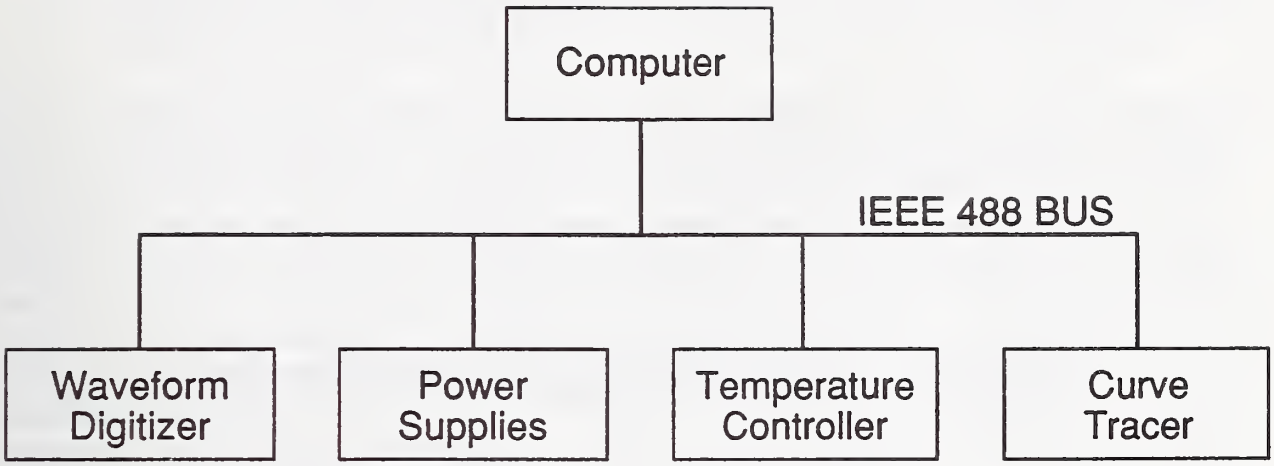


Figure 16 (a). Configuration of laboratory equipment necessary to extract the IGBT model parameters.

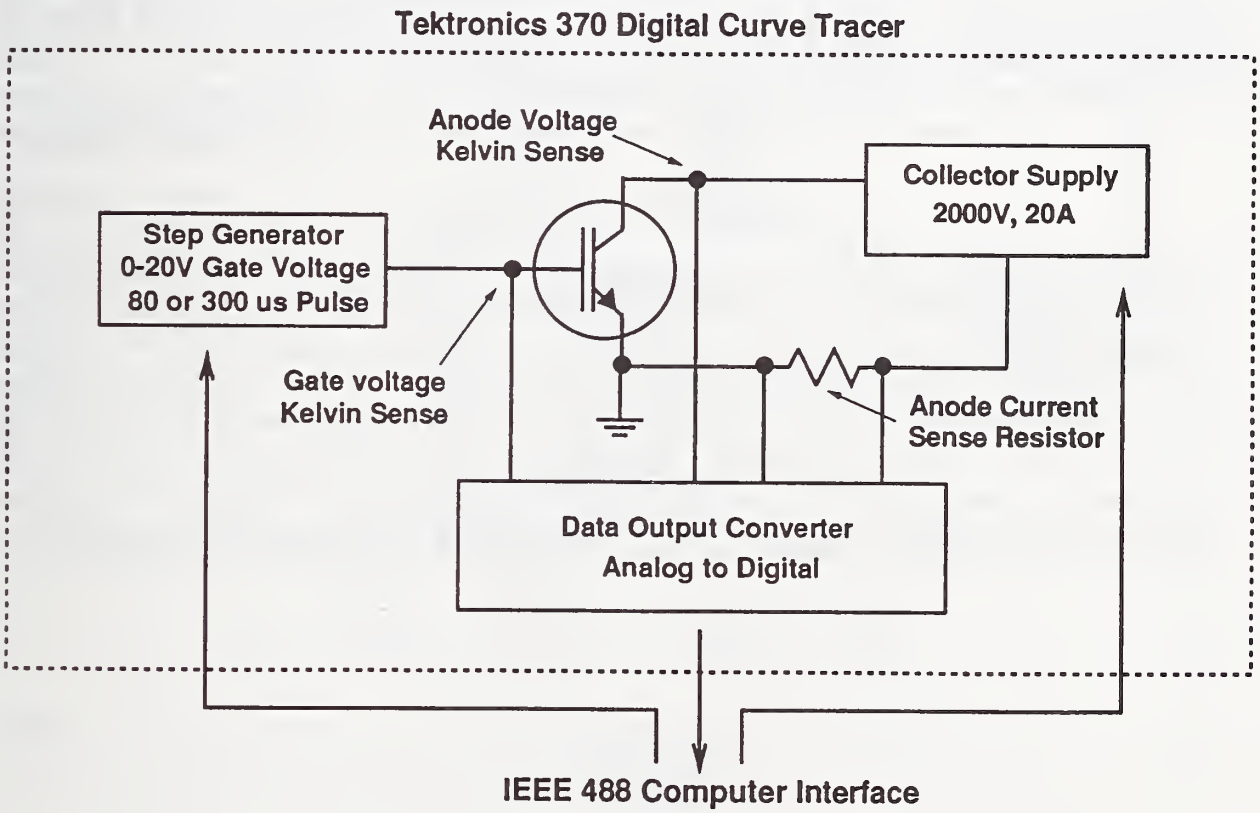


Figure 16 (b). Circuit configuration used to measure the high voltage and high current steady-state characteristics.

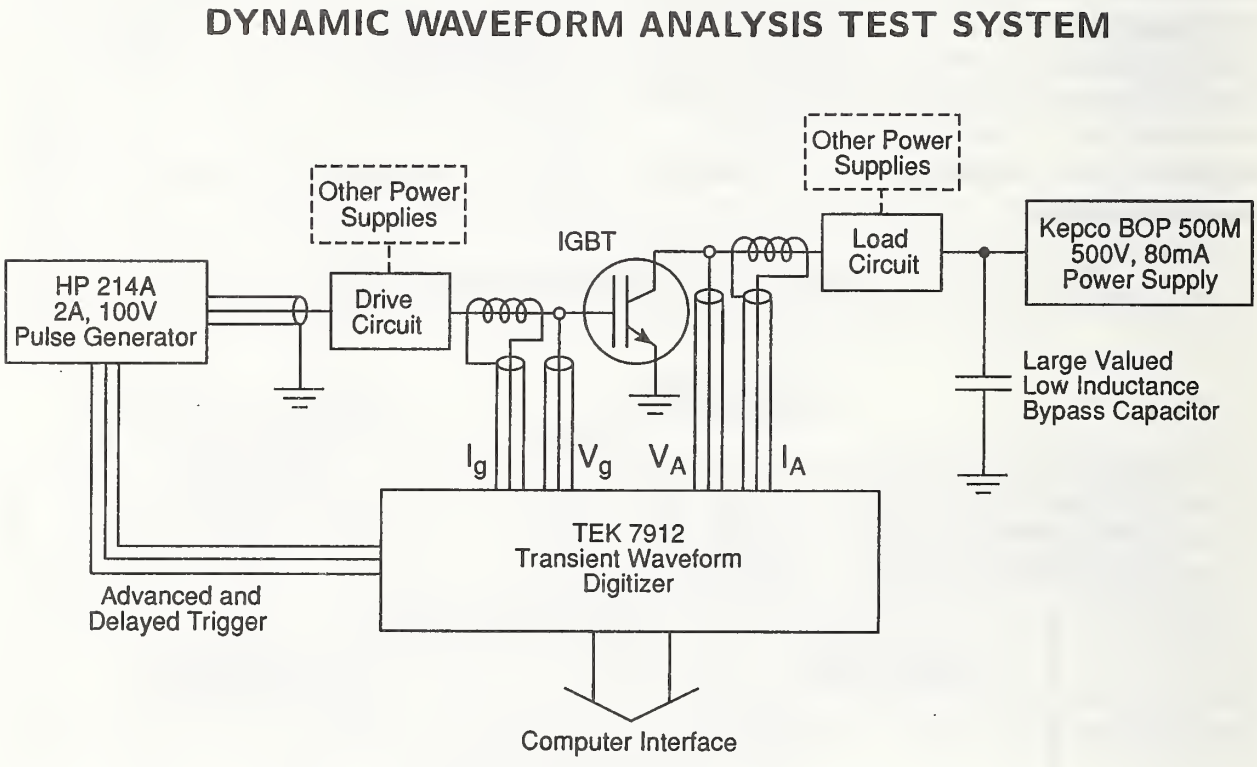


Figure 16 (c). Circuit configuration used to measure the dynamic characteristics.

available to facilitate the development of automated parameter extraction procedures [10]. In this publication, the basic IGBT parameter extraction sequence is discussed, but the specific hardware and programming details will be the topic of a future publication.

Table 4 gives a list of the IGBT model parameters indicating their nominal values and the device characteristics that are used to extract each parameter. The physical constants of silicon listed in table 5 are not expected to change from one IGBT device to another. The device active area is extracted by decapsulation and visual inspection of the active chip size. Five basic types of electrical measurements are used to extract the remaining model parameters: 1) The turn-off current tail decay rate versus anode current is used to extract the base lifetime τ_{HL}. 2) The relative size of the turn-off current tail versus anode current, and anode voltage is used to extract the emitter electron saturation current I_{sne}, the metallurgical base width W_B, and the base doping concentration N_B. 3) The saturation current versus gate voltage is used to extract the MOSFET channel saturation region transconductance parameter K_{psat} and the MOSFET channel threshold voltage V_T. 4) The on-state voltage versus gate voltage at a constant anode current is used to extract the MOSFET channel linear region transconductance parameter K_{plin} and the series resistance R_s. 5) The gate charge and the gate-drain charge characteristics are used to extract the gate-source capacitance, the gate-drain overlap oxide capacitance, and the gate-drain overlap area. The five measurements are performed in the indicated sequence because the calculations made using measured data to extract the parameters require the values of the parameters extracted from the preceding extraction steps.

Tail Decay Rate

The constant anode voltage turn-off current tail decay rate can be measured using either the clamped large inductive load (1-mH) test circuit (fig. 17a) or the constant anode supply voltage test circuit (fig. 17b). The clamped inductive load technique is most suitable for small base lifetimes because it results in a larger tail size. When the gate voltage is turned off or when the anode clamp voltage is reached for the clamped inductive load case, the anode current initially falls rapidly and then tails off slowly as the anode voltage remains constant. It is shown theoretically in reference [1] that the decay time constant of the slowly decaying portion of the current waveform for a constant anode voltage is given by:

$$\frac{\mathrm{d}\ln I_T}{\mathrm{d}t} \equiv \frac{\mathrm{d}I_T/\mathrm{d}t}{I_T} = -\frac{1}{\tau_{HL}}\left(1+\frac{I_T}{I_k^\tau}\right) \tag{20}$$

where

$$I_{sne} \equiv \frac{q^2 A^2 D_p n_i^2}{I_k^\tau \tau_{HL}}. \tag{21}$$

Figure 18 shows the measured current decay time constant versus instantaneous tail current for devices with five different base lifetimes. Each curve is composed of several segments measured at different initial currents because the current scales of the measurement equipment need to be changed to maintain adequate precision. The measured values of the

Table 4. Characteristics Used to Extract Device Model Parameters

A	0.1 cm^2	Chip size
τ_{HL}	0.3 – 8.0 μs	Tail decay rate
I_{sne}	6.0×10^{-14} A	Tail size vs. current
W_B	93 μm	Tail size vs. V_A
N_B	2×10^{14} cm^{-3}	Tail size vs. V_A
V_T	5.0 V	Saturation current vs. V_{gs}
K_{Psat}	0.4 A/V^2	Saturation current vs. V_{gs}
θ	0.01 V^{-1}	Saturation current vs. V_{gs}
K_{Plin}	0.75 A/V^2	On-state voltage vs. V_{gs}
R_s	30 mΩ	On-state voltage vs. V_{gs}
C_{gs}	0.6 nF	Gate charge
C_{ozd}	1.6 nF	Gate charge
A_{gd}	0.05 cm^2	Gate-drain charge
V_{Td}	0.0 V	Gate-drain charge

Table 5. Physical Constants of Si at $T = 25$ °C

n_i	1.45×10^{10} cm^{-3}
μ_n	1500 $cm^2/V{\cdot}s$
μ_p	450 $cm^2/V{\cdot}s$
ϵ_{si}	1.05×10^{-12} F/cm
α_1	1.428×10^{20} $(cm{\cdot}V{\cdot}s)^{-1}$
α_2	4.54×10^{11} cm^{-2}
v_{nsat}	1.1×10^7 cm/s
v_{psat}	0.95×10^7 cm/s

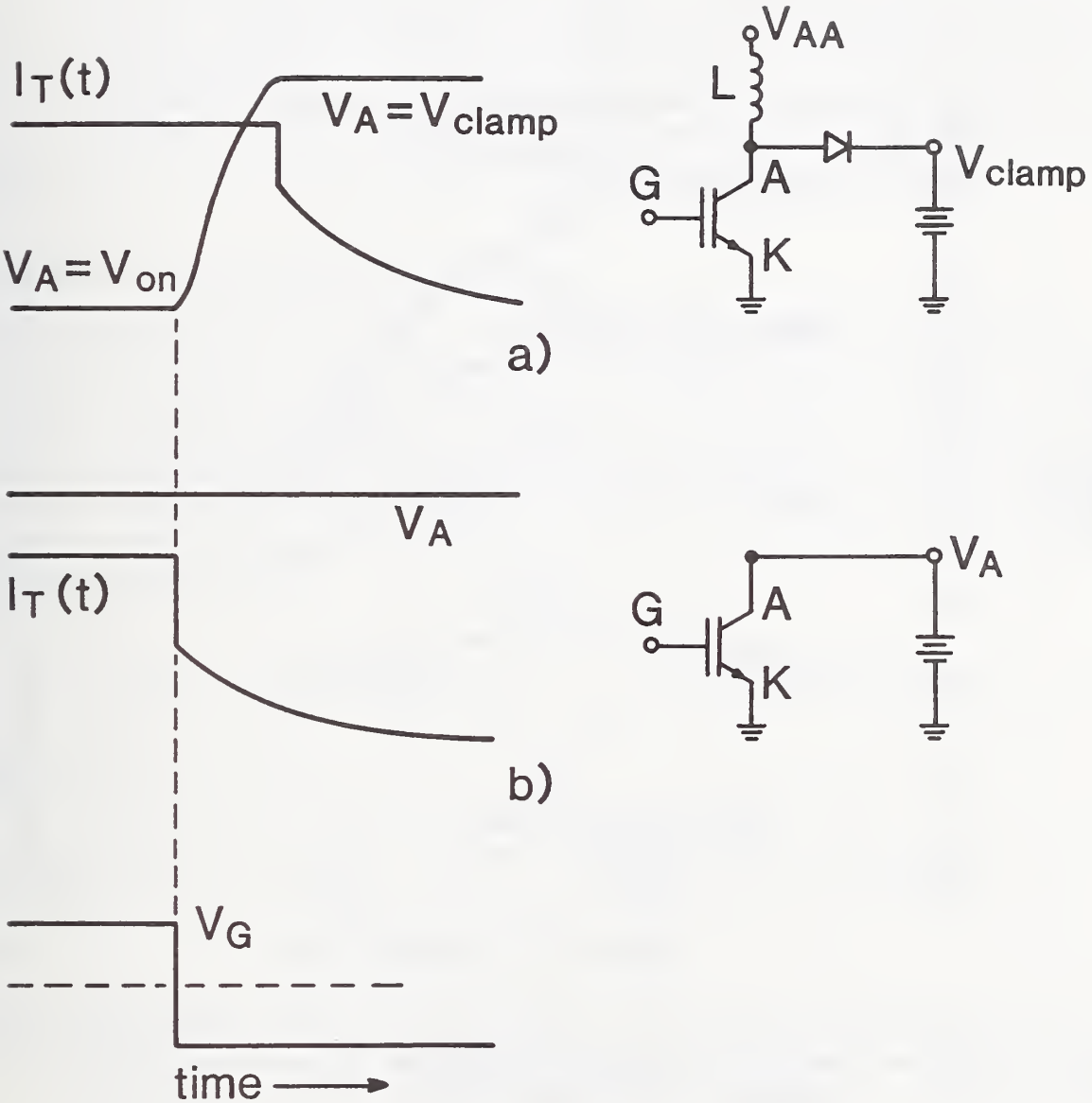


Figure 17. Circuit configuration and example turn-off switching waveforms for (a) the clamped large inductive load, and (b) the constant anode supply voltage.

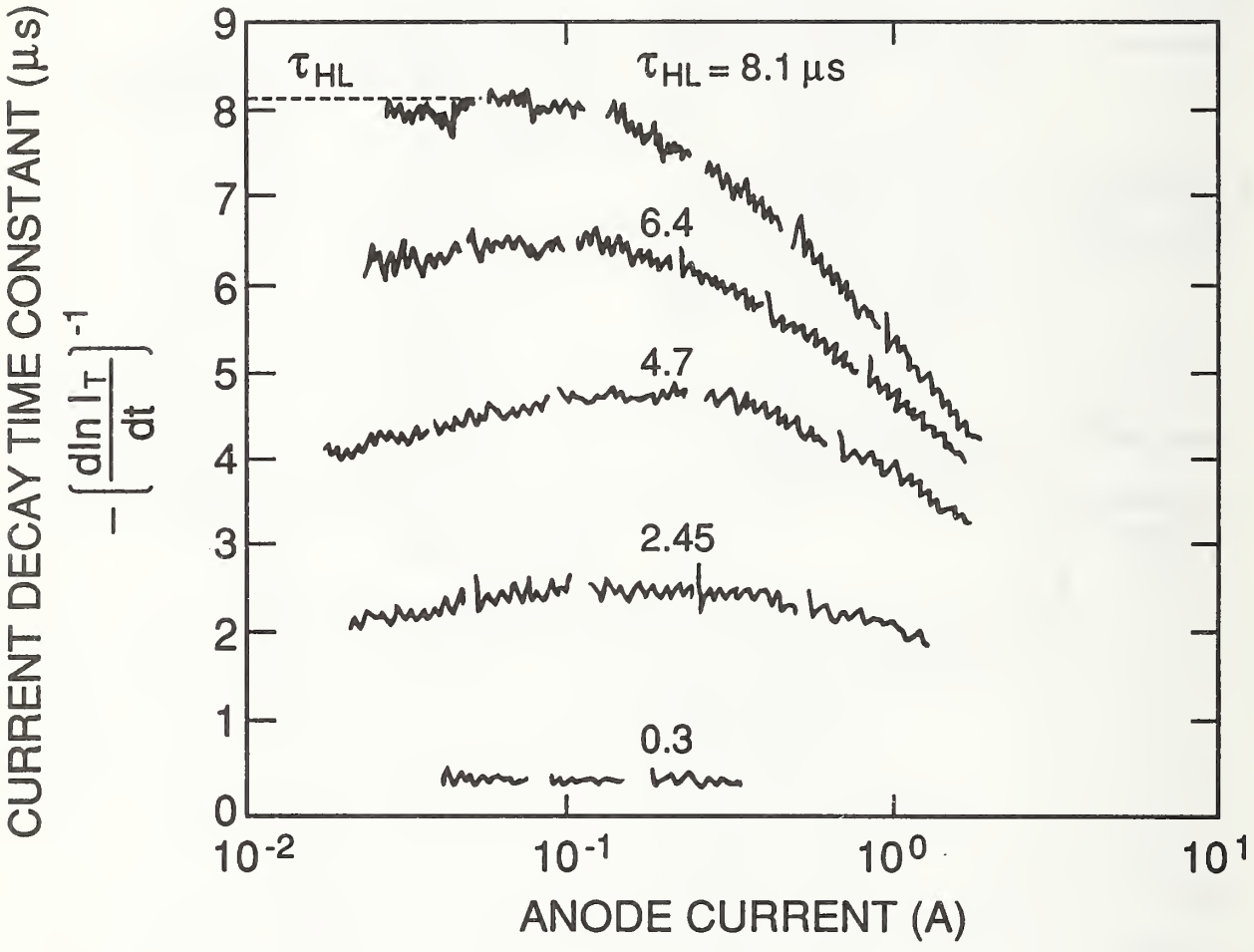


Figure 18. Experimental values of the current decay time constant versus current, calculated from digitized waveforms for different device base lifetimes and different initial currents. The value of base lifetime extracted for the 8.1-μs device is indicated.

current decay time constant are obtained by taking the negative time derivative of the log of the digitized current waveforms as indicated on figure 18. From eq (20), it is expected that the maximum value of this decay rate is equal to the device base lifetime as indicated on figure 18. However, the decay time constant decreases at low currents due to recombination in the emitter-base junction, due to surface recombination, and because the base enters the low-level injection condition. Therefore, the value of base lifetime is extracted from the least-squares fit of eq 20 to the measured values of the inverse current decay time constant versus current. The graphics output of this automated extraction routine is shown in figure 19, where it is indicated that the extrapolated zero current intercept is equal to the $1/\tau_{HL}$ and that the slope can be used to extract the value of I_{sne} using eq (21).

Tail Size Versus Anode Current and Voltage

Figure 20a shows a typical constant anode voltage turn-off current waveform, which consists of an initial rapid fall followed by a slowly decaying current tail. It was shown in reference [1] that a finite time is required after the initial rapid fall in current for the excess carriers to assume a distribution that can be described by a simple model. However, if the current tail is extrapolated back past the redistribution phase to the time of the initial rapid fall in current using the current tail of a larger initial current waveform, as shown in figure 20b, then the relative size of the extrapolated current tail for constant anode supply voltage switching is given by [1]:

$$\beta_{tr,V} \equiv \left.\frac{I_T(0^+)}{I_T(0^-) - I_T(0^+)}\right|_{V_A = \text{const.}} = \beta_{tr,V}^{max}\left(1 + \frac{I_T(0^+)}{I_k}\right)^{-1} \qquad (22)$$

where

$$\beta_{tr,V}^{max} = \left(\left(\frac{W}{L}\right)^2 \frac{\coth(\frac{W}{L})}{2\tanh(\frac{W}{2L})} - 1\right)^{-1} \qquad \cdot (23)$$

and

$$I_{sne} \equiv \frac{\tanh^2(\frac{W}{2L})}{(\frac{W}{L})^4}\left(\frac{(4qn_iAD_p)^2}{L^2(1+\frac{1}{b})}\right) \cdot \frac{1}{\beta_{tr,V}^{max} I_k}. \qquad (24)$$

The current tail of the larger current waveform is used for the extrapolation because the current decay rate is a function of the instantaneous tail current, and the model parameters that describe the tail are not known at this point in the extraction sequence.

Figure 21 shows the measured values of the relative size of the extrapolated current tail $\beta_{tr,V}$ for two different values of constant anode supply voltage. The extrapolations are performed using a larger initial current waveform which is automatically aligned with the

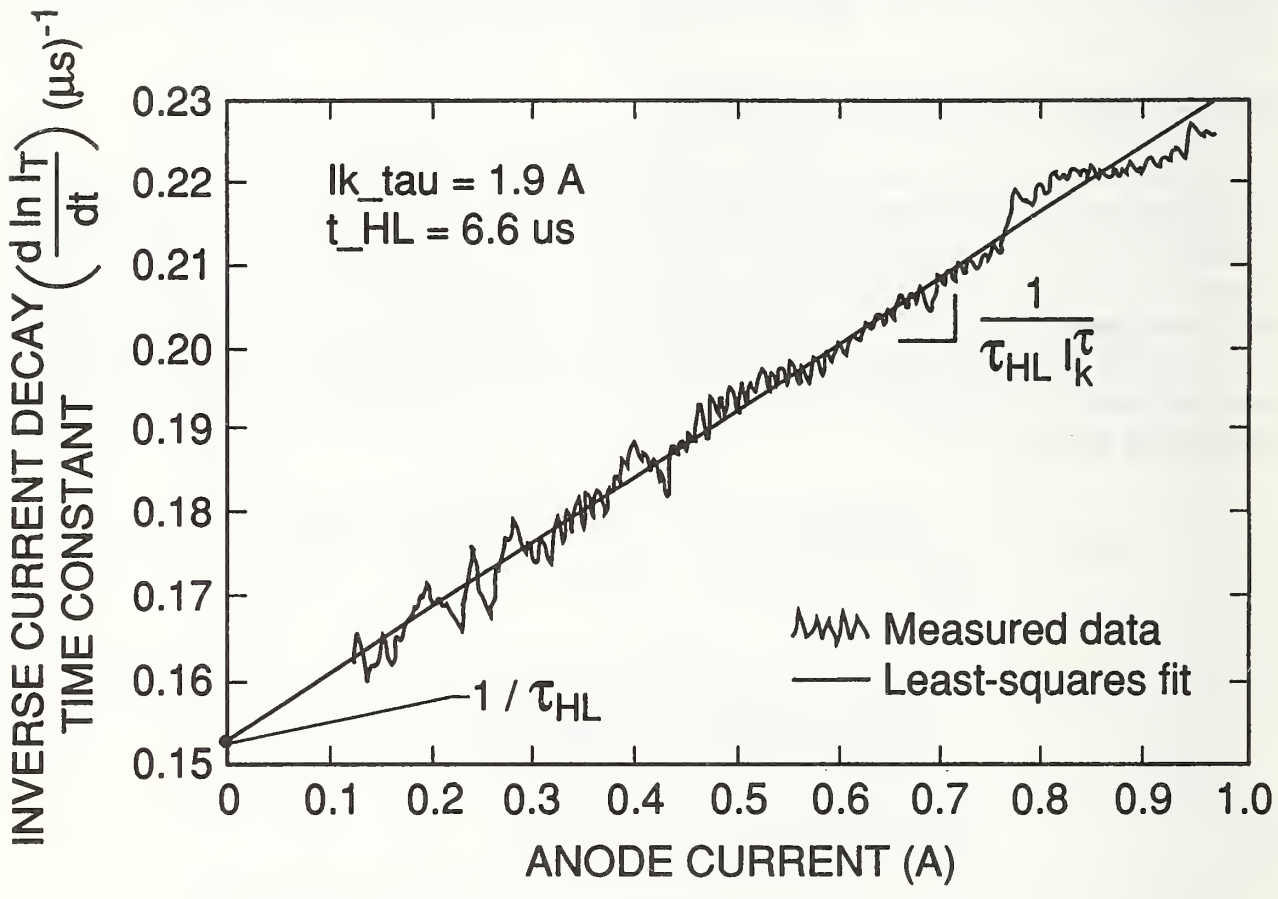
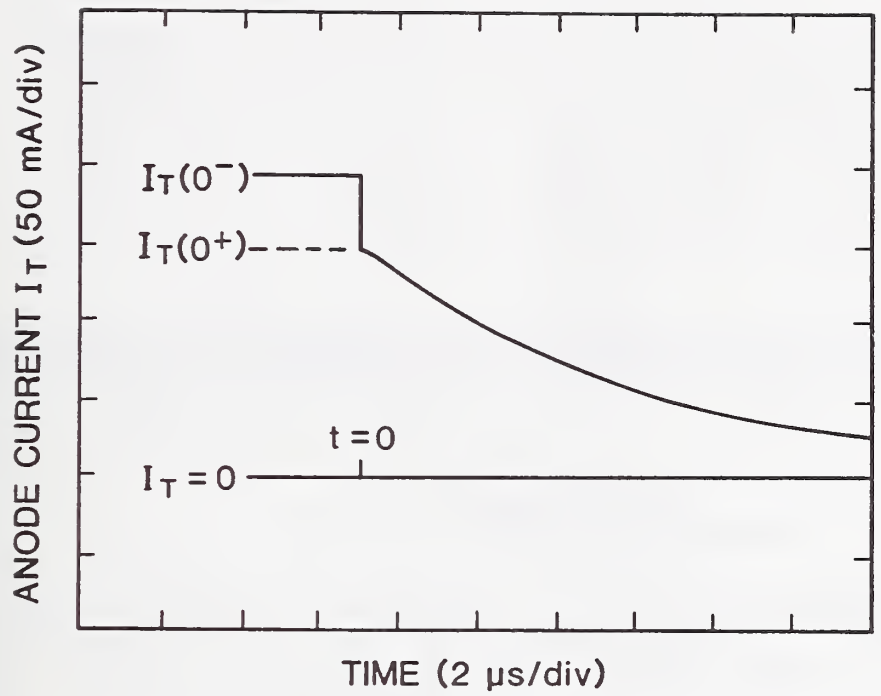
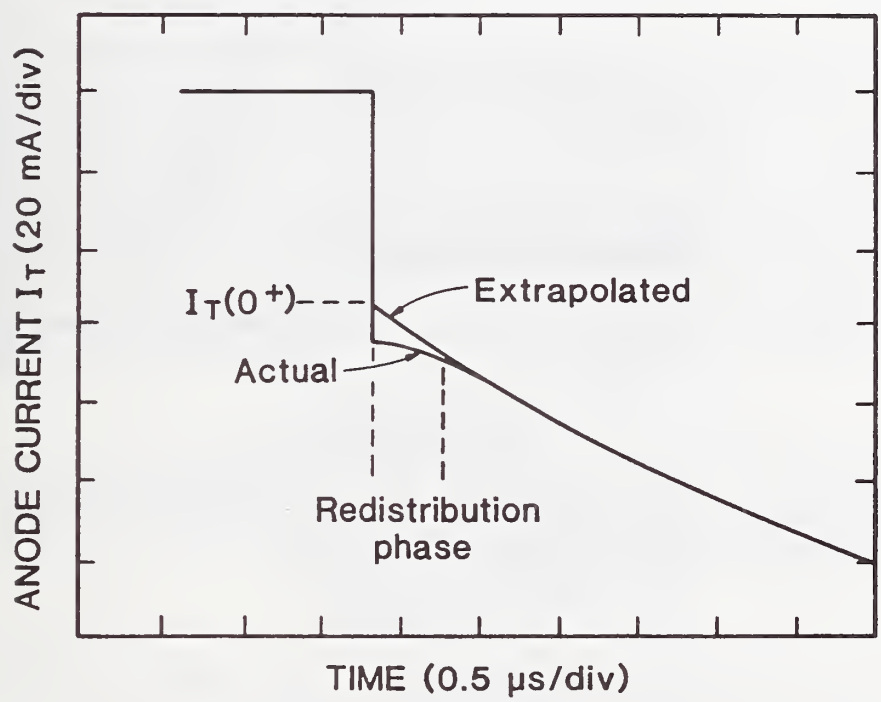


Figure 19. The graphics output of the tail decay rate automated extraction routine indicating that the extrapolated zero current intercept is equal to the $1/\tau_{HL}$.



(a



(b

Figure 20. (a) Constant anode voltage turn-off current waveform, indicating the current before and after the initial rapid fall, and (b) a diagram of the redistribution phase on an expanded scale, showing the extrapolated value of $I_T(0^+)$.

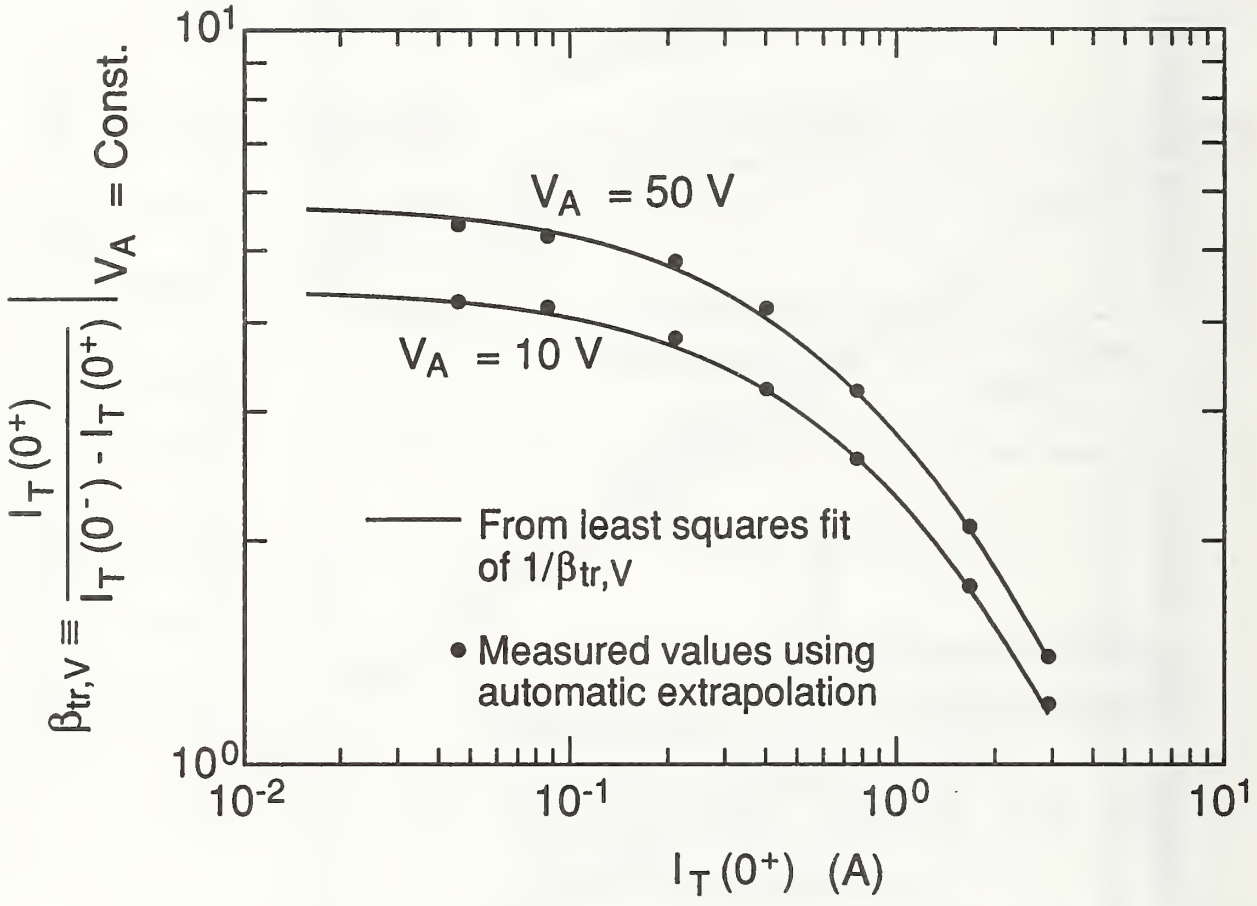


Figure 21. Measured values of the relative size of the extrapolated current decay tail $\beta_{tr,V}$ versus current for two different values of constant anode voltage.

current tail by a computer-fitting algorithm. Figure 22 shows the measured values of $1/\beta_{tr,V}$ versus the initial tail current, which is expected from eq (22) to be linear with a slope of $1/(\beta_{tr,V}^{max} I_k)$ and with a zero current intercept of $1/\beta_{tr,V}^{max}$. The solid curves in figures 21 and 22 are obtained from a least-squares linear fit to the $1/\beta_{tr,V}$ data. The slope of the least-squares fit is used with eq (24) to extract the parameter I_{sne}, and the zero current intercept is used to obtain the value of W at the given anode voltage from eq (23). The method of using the slope of figure 22 to extract I_{sne} is preferred over using the slope of figure 19, because the variation of $\beta_{tr,V}$ with current is larger than that of τ_{HL}.

The inputs to this automated extraction routine are the values of τ_{HL} and A obtained from the previous extraction steps, and the outputs are the values of I_{sne} and the value of W for the voltage at which the measurement was made. Because the base width W is expected to be given in terms of anode voltage by [1]:

$$W \approx W_B - \sqrt{2\epsilon_{si} V_A / q N_B}, \tag{25}$$

the values of W versus the square root of anode voltage can be used to extract the values of W_B and N_B. The values of W_B and N_B obtained using the extraction algorithms are consistent with the values previously obtained from spreading resistance measurements [1].

Saturation Current Versus Gate Voltage

Figure 23 defines the IGBT saturation current at a given gate voltage. The IGBT anode current saturates because the internal MOSFET channel current saturates where the MOSFET saturation current is magnified (gain enhancement) by the steady-state common collector current gain of the bipolar transistor $(1 + \beta_{ss})$. Figure 24 shows the bipolar transistor common collector current gain versus anode current predicted using the bipolar transistor parameters that were isolated and extracted from the dynamic characteristics described in the previous paragraphs. Hence, the saturation characteristics of the internal MOSFET are obtained from IGBT saturation characteristics by dividing out the bipolar transistor current gain [1]:

$$I_{mos}^{sat} = I_T^{sat} / (1 + \beta_{ss}). \tag{26}$$

For $V_{gs} - V_T \ll 1/\theta$, the square root of the saturation current is linearly related to the gate voltage with a zero current intercept of V_T and with a slope of $\sqrt{K_{psat}/2}$ (see eq (T2.15)):

$$\sqrt{I_{mos}^{sat}} = \sqrt{\frac{K_{psat}}{2}} (V_{gs} - V_T). \tag{27}$$

The value of $\theta \approx 0.01$ V^{-1} can be extracted from the saturation current at high gate voltages.

Figure 25 shows the square root of the MOSFET saturation current versus gate-source voltage obtained by dividing the measured IGBT saturation current by the common collector current gain for devices with different base lifetimes. The values of K_{psat} and V_T are extracted from the slope and the zero-current intercept of these curves. This method

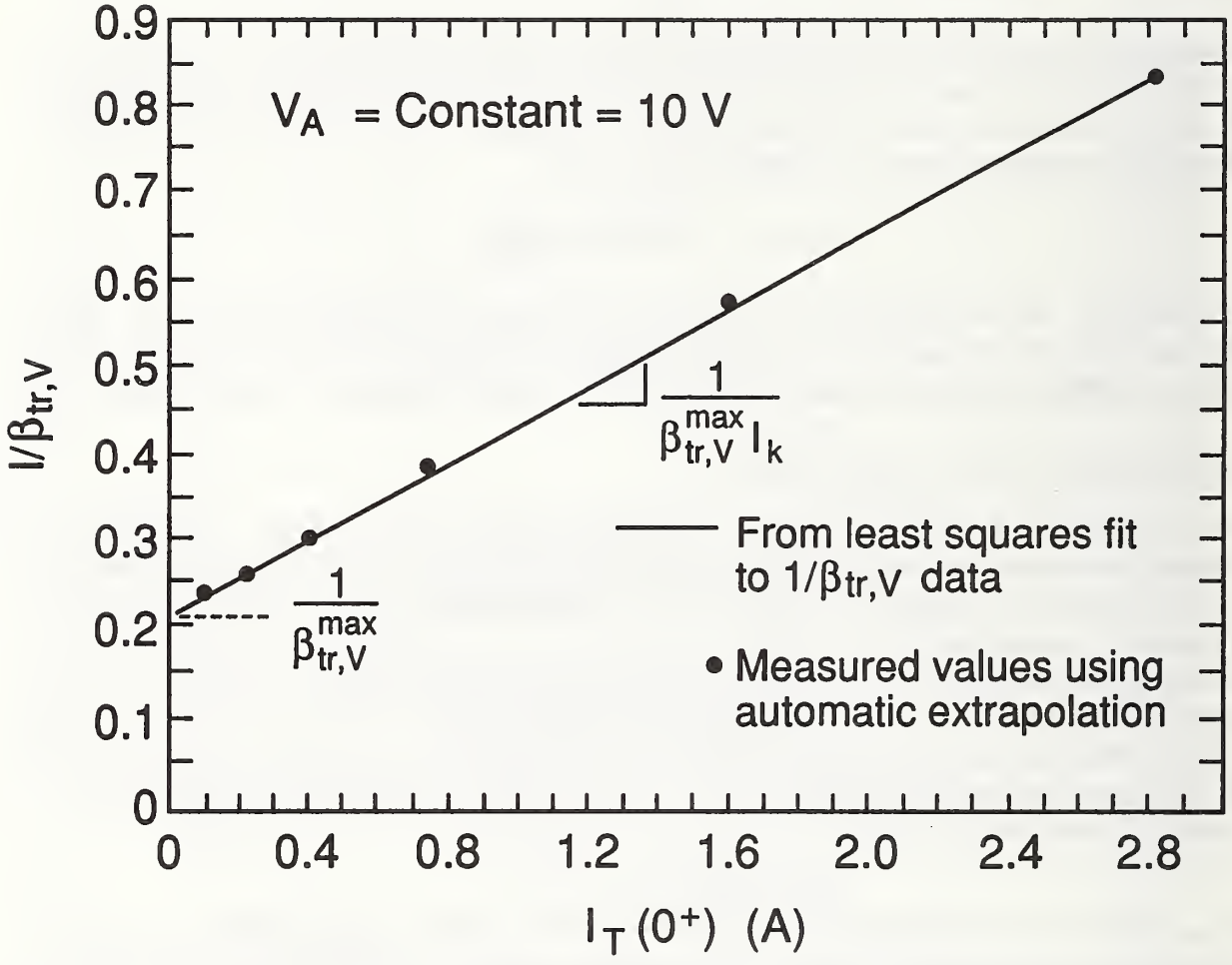


Figure 22. Measured values and linear least-squares fit to $1/\beta_{tr,V}$ versus $I_T(0^+)$, indicating quantities obtained from slope and intercept.

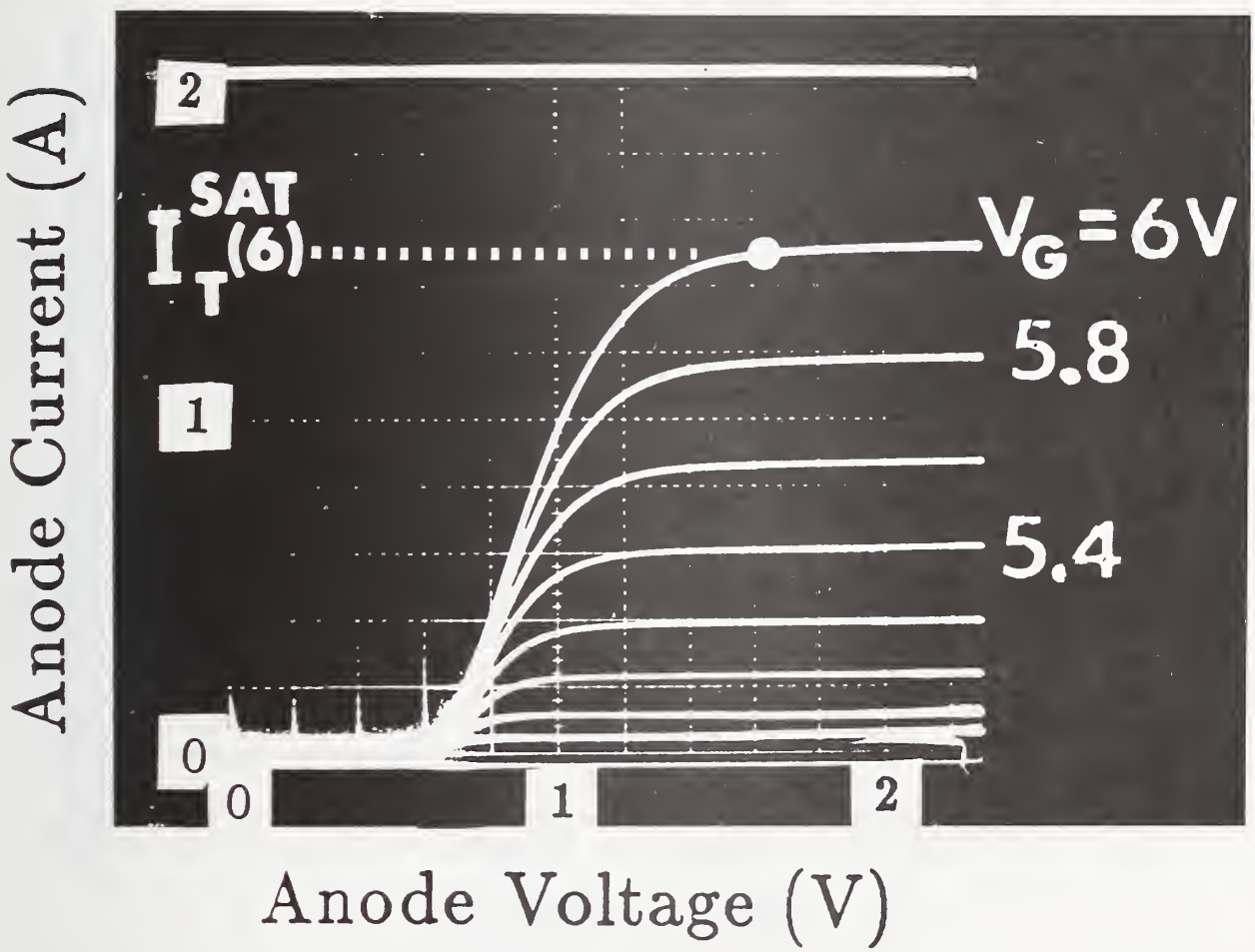


Figure 23. An oscillogram of the steady-state characteristics of the IGBT, defining the value of the IGBT saturation current at a given gate voltage.

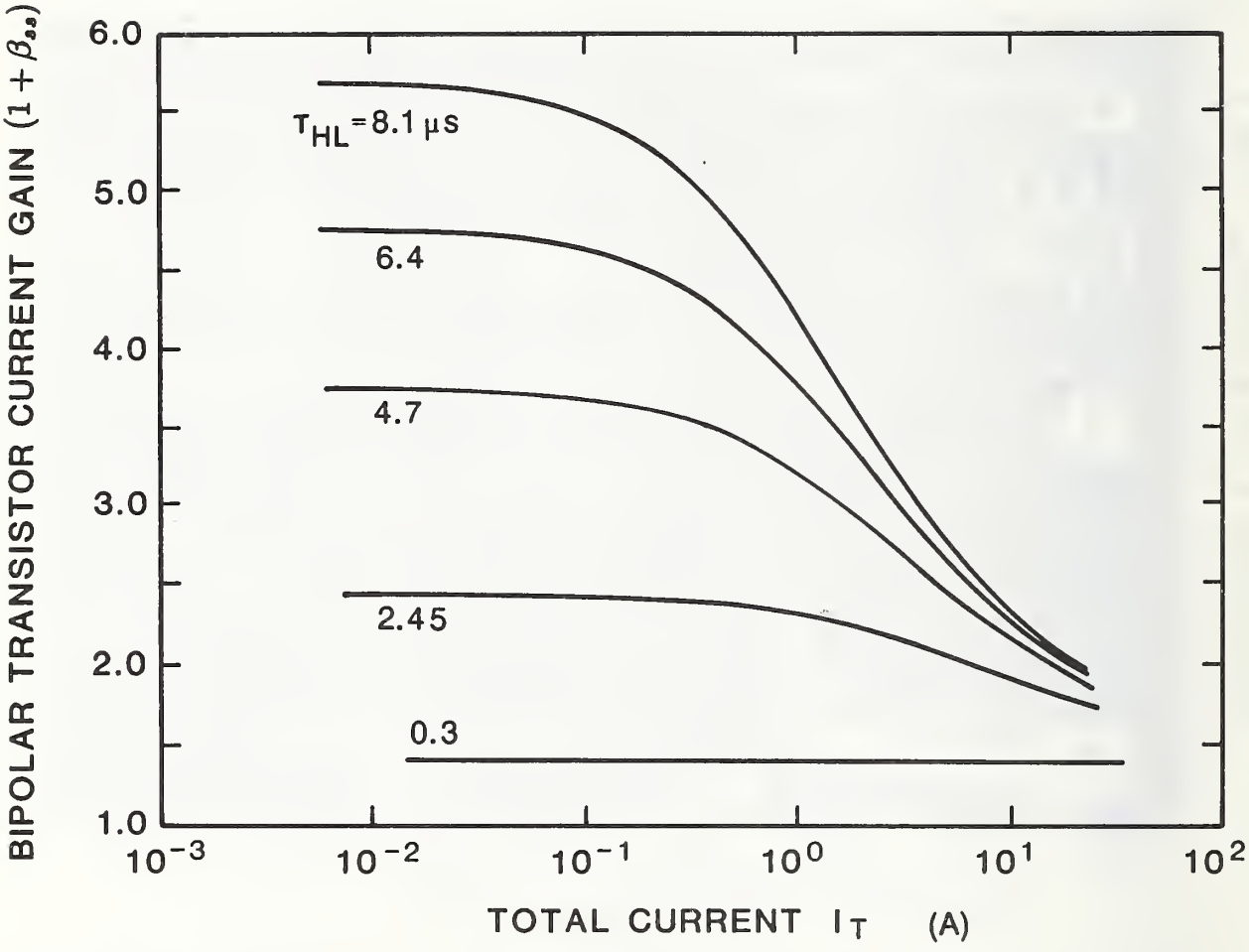


Figure 24. The steady-state common collector current gain versus anode current for the bipolar transistor of IGBTs with different base lifetimes.

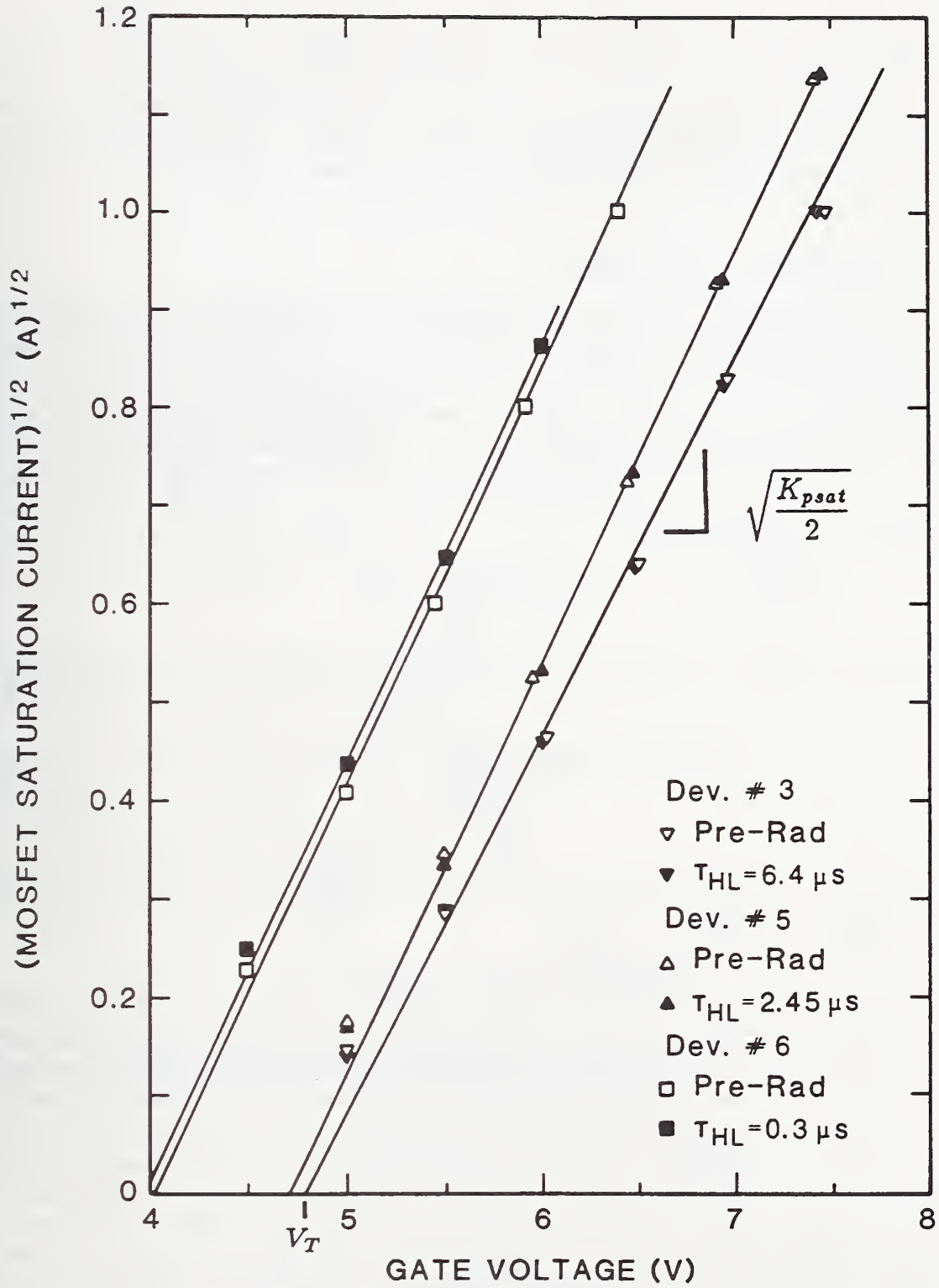


Figure 25. The square root of the MOSFET saturation current indicating that the slope is used to extract K_{psat} and the zero current intercept is used to extract V_T.

results in similar values of K_{psat} and V_T before and after the bipolar transistor current gain of each device is reduced by neutron exposure, which is not expected to change the values of the MOSFET parameters [6]. Figure 26 shows the graphics output of this automated parameter extraction procedure indicating the measured IGBT saturation current, the MOSFET saturation current calculated from the measured data using the parameters obtained from the previous extraction steps, and the least-squares fit to the MOSFET saturation current.

On-State Voltage Versus Gate Voltage

Figure 27 is an oscillogram of the output characteristics of the IGBT, indicating the on-state voltage for different gate voltages at a constant anode current. As indicated in eq (6), the IGBT anode-cathode voltage consists of the sum of the bipolar emitter-base voltage (due to conductivity-modulated base resistance and the emitter-base junction voltage), the voltage drop across the series resistance R_s, and the voltage across the MOSFET channel. For the IGBT on-state, the MOSFET channel current is in the linear region, and this MOSFET channel current is magnified by the steady-state common collector current gain of the bipolar transistor (fig. 24):

$$I_T^{lin} = (1 + \beta_{ss}) I_{mos}^{lin}. \tag{28}$$

Using eqs (6) and (28), and assuming that the MOSFET channel current is given by the first term in the linear region expression of eq (T2.15), the IGBT on-state voltage is given by:

$$V_{on} = V_r + \frac{I_T}{(1 + \beta_{ss}) K_{Plin}} \left(\frac{1}{V_{gs} - V_T} \right), \tag{29}$$

where

$$V_r \equiv V_{eb} + R_s \cdot I_T + \frac{I_T \theta}{(1 + \beta_{ss}) K_{Plin}} \tag{30}$$

and $V_{bc} = V_{ds}$ has been used (see fig. 3).

From eq (29), it is expected that the on-state voltage versus $1/(V_{gs} - V_T)$ at a constant anode current is linear with a slope of $I_T / K_{Plin}(1 + \beta_{ss})$ and with an infinite gate voltage intercept of V_r given by eq (30). Figure 28 shows the graphics output of the automated extraction procedure used to extract the MOSFET linear region transconductance and series resistance. As indicated on figure 28, the values of V_r and K_{plin} are obtained from the slope and intercept of the least-squares fit to the measured on-state voltage versus $1/(V_{gs} - V_T)$ at a constant anode current over the range of gate voltages where the MOSFET channel current is given by the first term in the linear region expression of eq (T2.15). The values of K_{plin} and R_s are thus obtained from this extraction step using the values of V_T, β_{ss}, V_{eb}, K_{Plin}, and θ calculated from model parameters obtained in previous extraction steps.

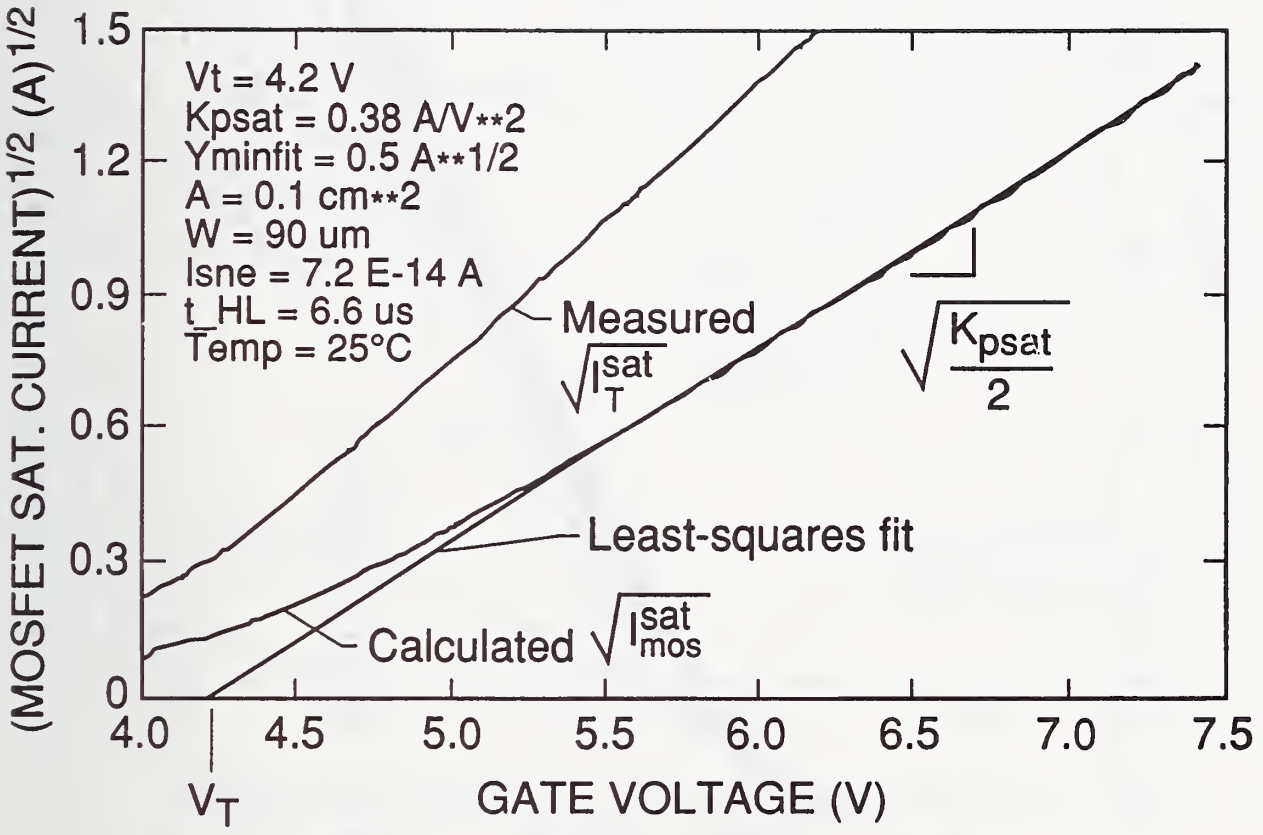


Figure 26. Graphics output of the automated extraction procedure used to extract the MOSFET threshold voltage and saturation transconductance.

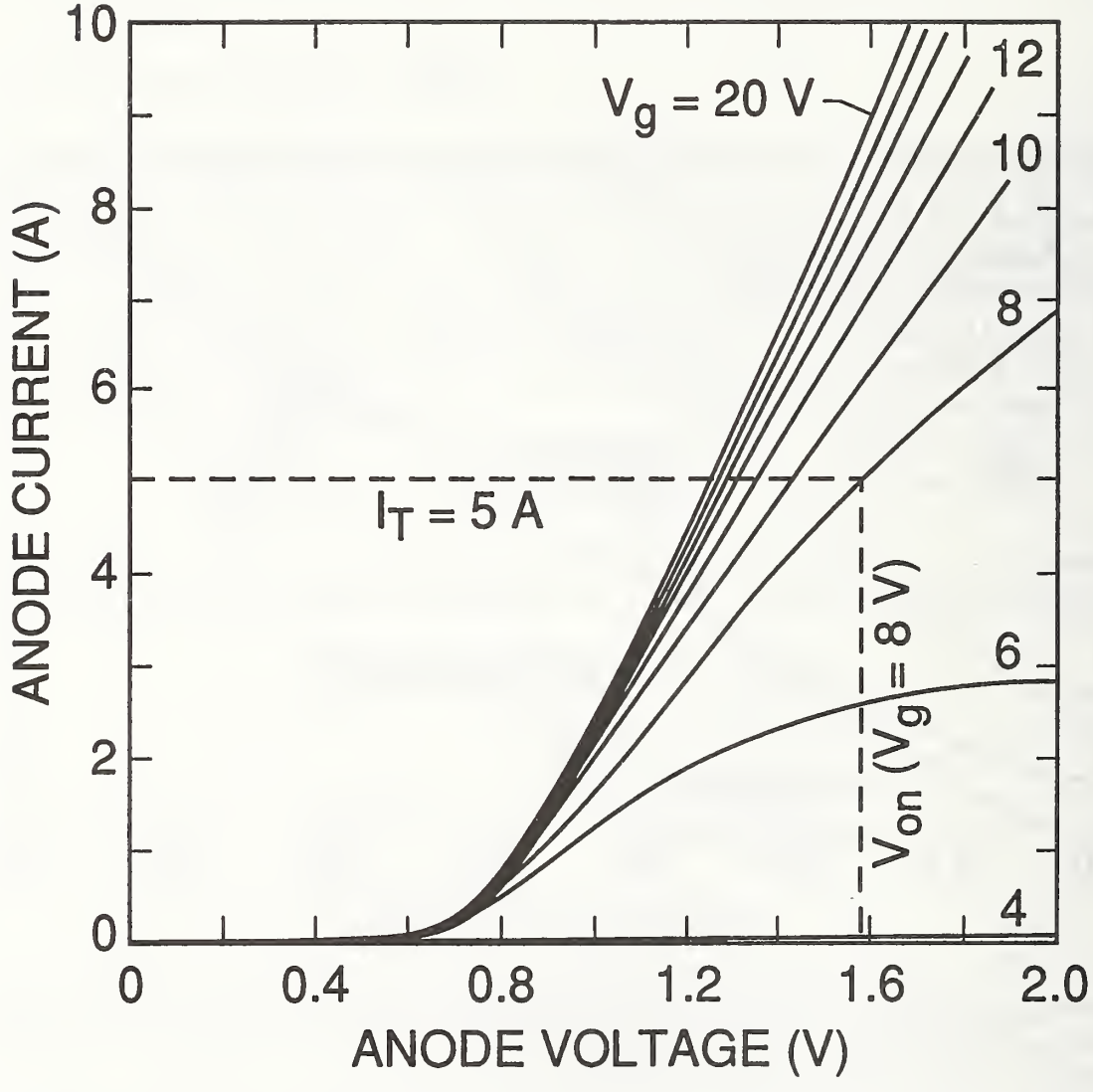


Figure 27. An oscillogram of the on-state characteristics of the IGBT, indicating the on-state voltages versus gate voltage for a constant current.

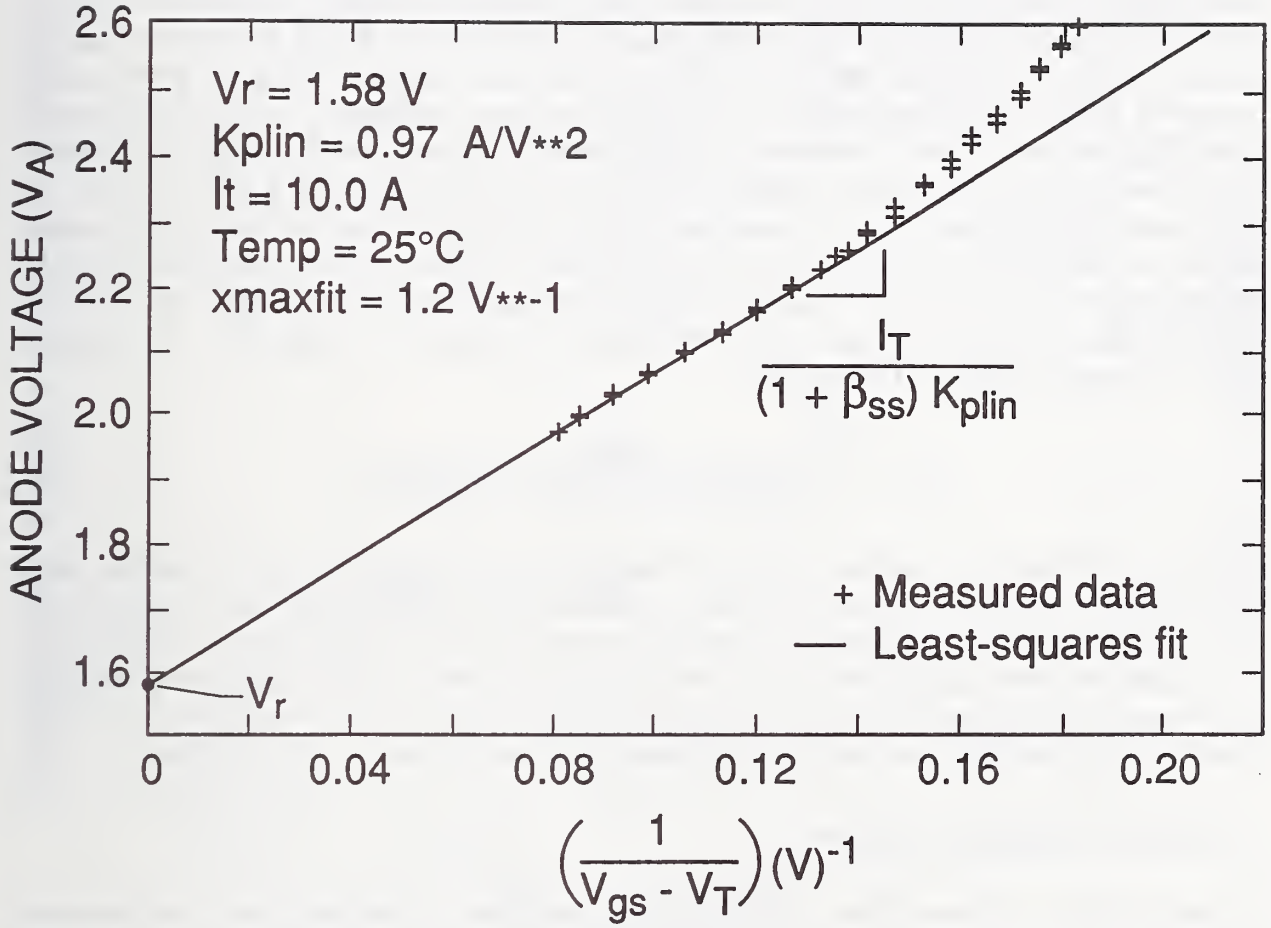


Figure 28. Graphics output of the automated extraction procedure used to extract the MOSFET linear region transconductance and series resistance.

Gate and Gate-Drain Charge

Figure 29 shows typical IGBT turn-on gate and anode voltage waveforms for a nearly constant gate current and for a load that results in a low anode current. These waveforms are used to examine the gate and gate-drain charge characteristics [3]. For the low anode current, $Q \approx 0$ and the gate charge characteristics are similar to those of the structurally equivalent power MOSFET [12,13]. The gate voltage waveform consists of three phases, as indicated in figure 29. During the first phase, V_{gs} rises with a constant slope as the constant gate current charges the constant gate-source capacitance. Therefore, the gate-source capacitance is extracted from this phase, as indicated in figure 30, by dividing the digitized values of the gate current waveform by the time rate-of-change of gate voltage computed from the digitized values of the gate voltage waveform. During the second phase, V_{gs} remains virtually constant, and V_A falls as the gate current charges the voltage-dependent gate-drain feedback capacitance. Therefore, the voltage dependence of the gate-drain depletion capacitance is ascertained by dividing the digitized values of the gate current waveform by the time rate-of-change of gate-to-anode voltage computed from the digitized values of the gate and anode voltage waveforms as shown on figure 31. For the VDMOSFET structure, the gate-drain depletion capacitance is expected to be given in terms of gate-to-anode voltage by [3]:

$$C_{gdj} \approx \frac{A_{gd}\epsilon_{si}}{\sqrt{2\epsilon_{si}(V_A - V_{bi} - V_{gs} + V_{Td})/qN_B}}. \tag{29}$$

Therefore, the measured values of C_{gdj} for high anode voltages are used to extract A_{gd}, and $1/C_{gdj}^2$ versus $V_A - V_{gs}$ can be used to extract V_{Td}. During the third phase of the gate voltage waveform, V_A remains relatively constant, and the gate-source voltage rises as the gate current charges the sum of the gate-drain overlap oxide capacitance and the gate-source capacitance. Therefore, the value of C_{oxd} is extracted by subtracting the value of the input capacitance during the first phase from that during the third phase.

VI. MODEL VERIFICATION

In this section, it is shown that the IGBT model presented in section II and implemented in INSTANT gives accurate results when the parameters are extracted as described in section V. Results are shown for IGBTs with the parameters listed in tables 4 and 5 and for devices with different base lifetimes (an exception to table 4 is that the base width of the 0.3-μs device is 110 μm). Comparisons of the IGBT model with experiments are made for different device base lifetimes, different external circuit configurations, and different circuit component values.

The validity of the model for both steady-state and transient conditions is examined. The dynamic model is first examined for the constant gate current condition, the constant anode current condition, and the constant anode voltage condition to verify each of the IGBT state equations independently. The model is then verified for external circuit operating conditions representative of those for which the device is intended to be operated. It

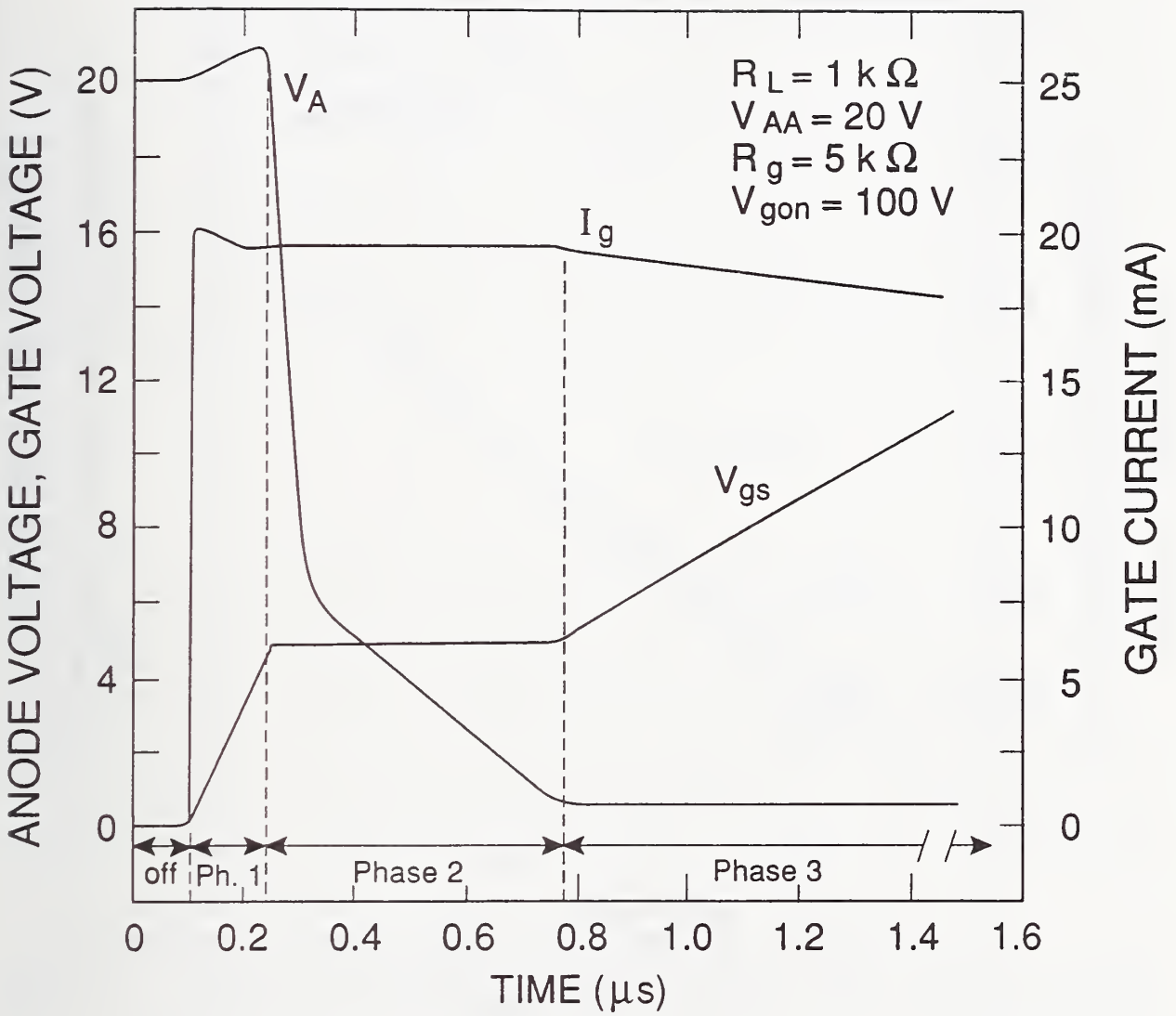


Figure 29. Measured gate and gate-drain charging characteristics for a low anode current and a relatively constant ~ 20-mA gate current pulse.

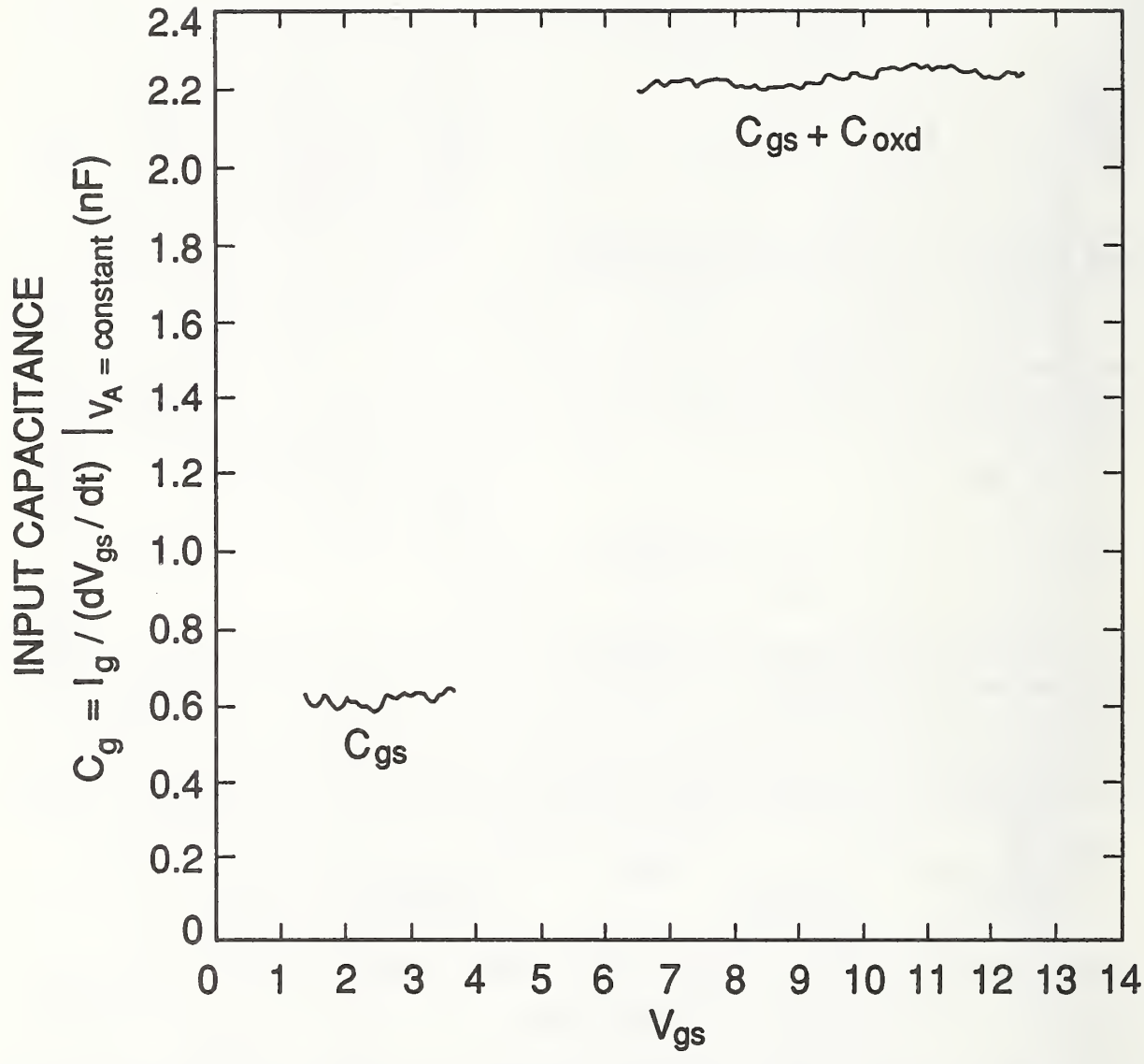


Figure 30. The measured input capacitance versus gate voltage characteristics for V_{AA} = 300 V obtained from digitized gate current and gate voltage waveforms similar to those in figure 29.

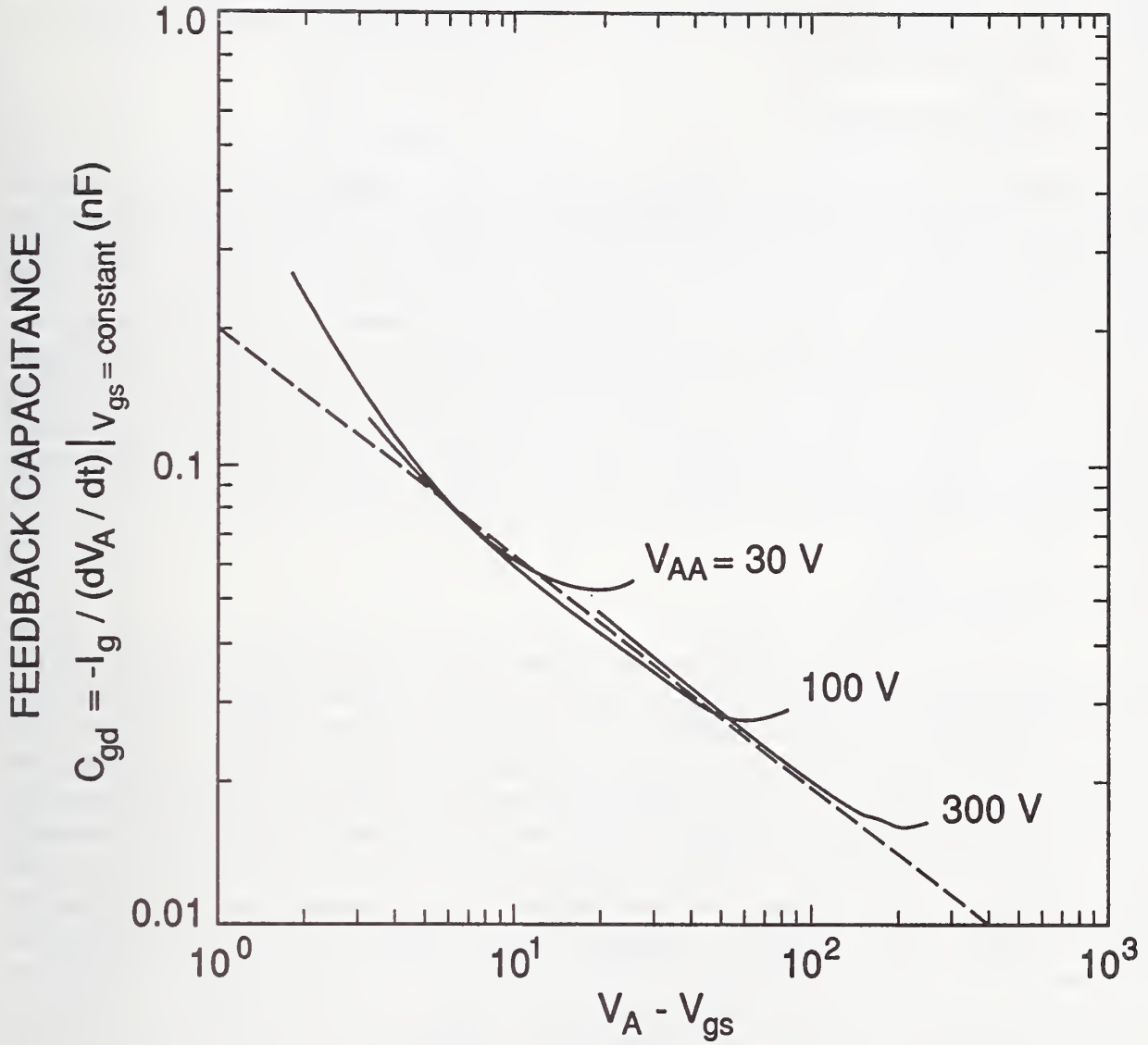


Figure 31. The measured gate-drain feedback capacitance versus anode-gate voltage obtained from digitized gate current, gate voltage, and anode voltage waveforms similar to those in figure 29. The data is obtained from waveforms with several different anode supply voltages, 30 V, 100 V, and 300 V, to maintain adequate precision over the voltage range of the measurements. The beginning of each waveform is evident by the high-voltage portion that does not lie along the dashed line due to the increasing gate voltage before phase 2 of figure 29 is reached. The low-voltage portion does not lie on the dashed line because of the voltage offset of V_{bi} and V_{Td}.

is shown that the model accurately describes the turn-on and turn-off waveforms for a series resistor-inductor load both with and without snubber capacitors and active feedback circuits. The performance of the model is evaluated for different load resistances, load inductances, gate resistances, snubber capacitances, feedback snubber capacitances, and series feedback resistances.

Steady-State Characteristics

The saturation characteristics as defined in figure 23 are shown in figure 32 versus gate voltage for devices with different base lifetimes. The saturation current versus gate voltage is important during transient conditions when both a high anode current and a high anode voltage occur at the same time. The steady-state value of the IGBT anode voltage for a high gate voltage is important in determining the energy losses in the IGBT during the on-state. The on-state characteristics of the IGBT were measured for gate drive voltages from 10 V to 40 V. The on-state voltage has a significant gate drive voltage dependence for on-state currents above 1 A due to the finite value of the MOSFET channel resistance. Therefore, to demonstrate the accuracy of the wide base bipolar transistor model, the theoretical and experimental values of the on-state voltage versus current at $V_{gs} - V_T = 35$ V are shown in figure 33.

Dynamic Characteristics

The behavior of the gate charge and gate-drain charge characteristics of figure 29 are determined by eq (T1.1) and are independent of eq (T1.2) and eq (T1.3), because the MOSFET channel current and bipolar transistor base charge are small for the low anode current conditions. Therefore, eq (T1.1) is independently verified by the good correspondence between the voltage dependencies of the measured capacitances of figures 30 and 31 and the theoretical expressions in table 2. To verify the remainder of the IGBT dynamic model, both constant anode voltage and constant anode current turn-off conditions are examined for a rapid gate voltage transition. Because the gate voltage is switched off rapidly and then remains zero during the remainder of the transient, the IGBT state equations T1.2 and T1.3 are verified independently of eq (T1.1). The constant current condition is obtained by using a clamped inductive load with a large ($\sim$ 1-mH) inductance. Before the clamp voltage is reached, the large inductance requires the anode current to remain constant at the initial value determined by the steady-state conditions. The constant anode voltage condition is obtained for two different load circuits: 1) For clamped inductive load switching with a large clamp capacitor, the voltage remains constant after the clamp voltage is reached. 2) For constant anode supply voltage switching ($R = 0$ and $L = 0$), the anode voltage is held constant with a large-valued, low-inductance capacitor connected to the anode, and the current is determined by varying the steady-state gate voltage.

Constant Voltage Current Decay: First consider the current waveform for constant anode supply voltage switching which is shown in figure 20. The current waveform consists of an initial rapid fall due to (but not equal to) the removal of the MOSFET current, followed by a slowly decaying phase due to the remaining slowly decaying excess carriers in the

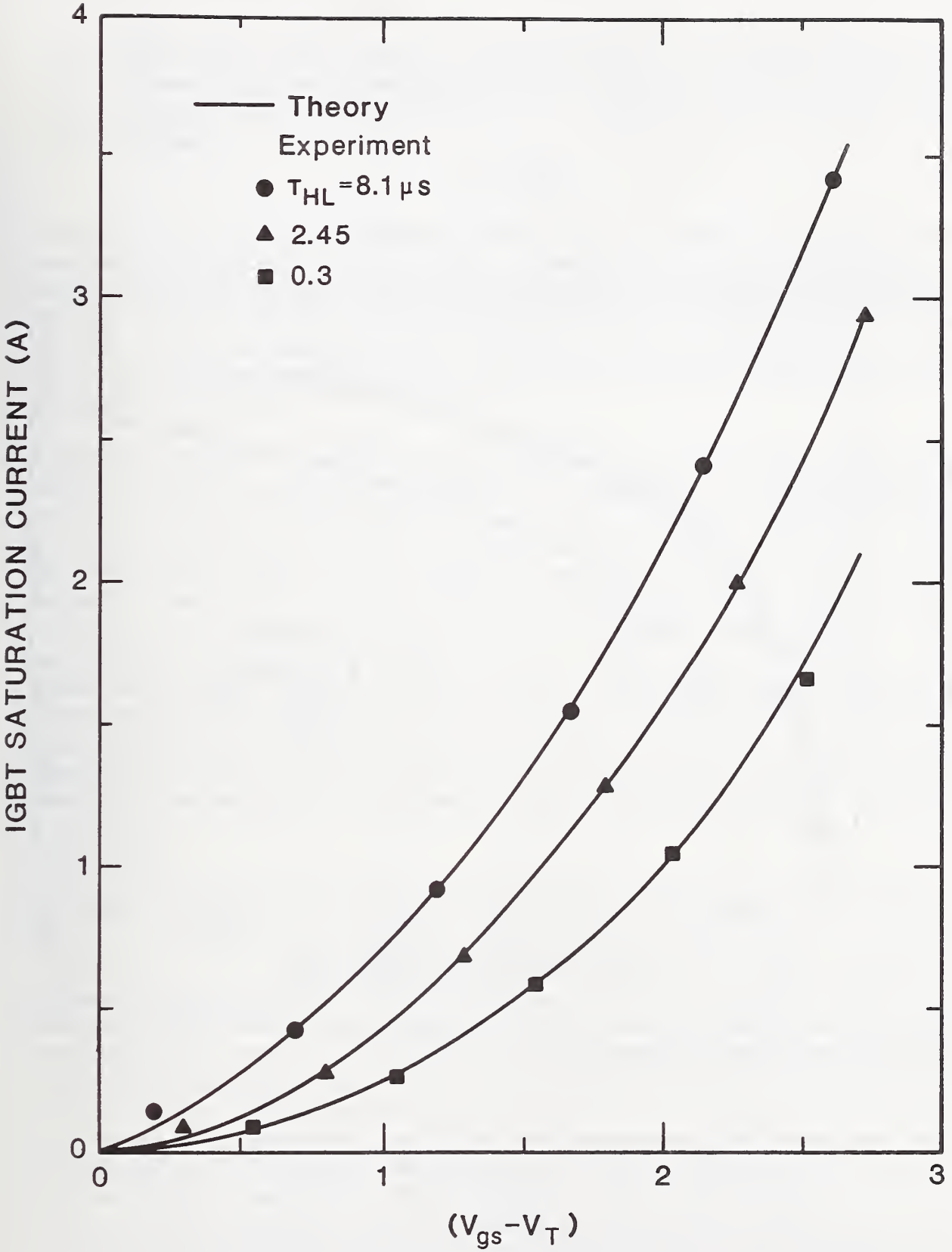


Figure 32. The measured and predicted values of the IGBT saturation current versus gate voltage for IGBTs with different lifetimes.

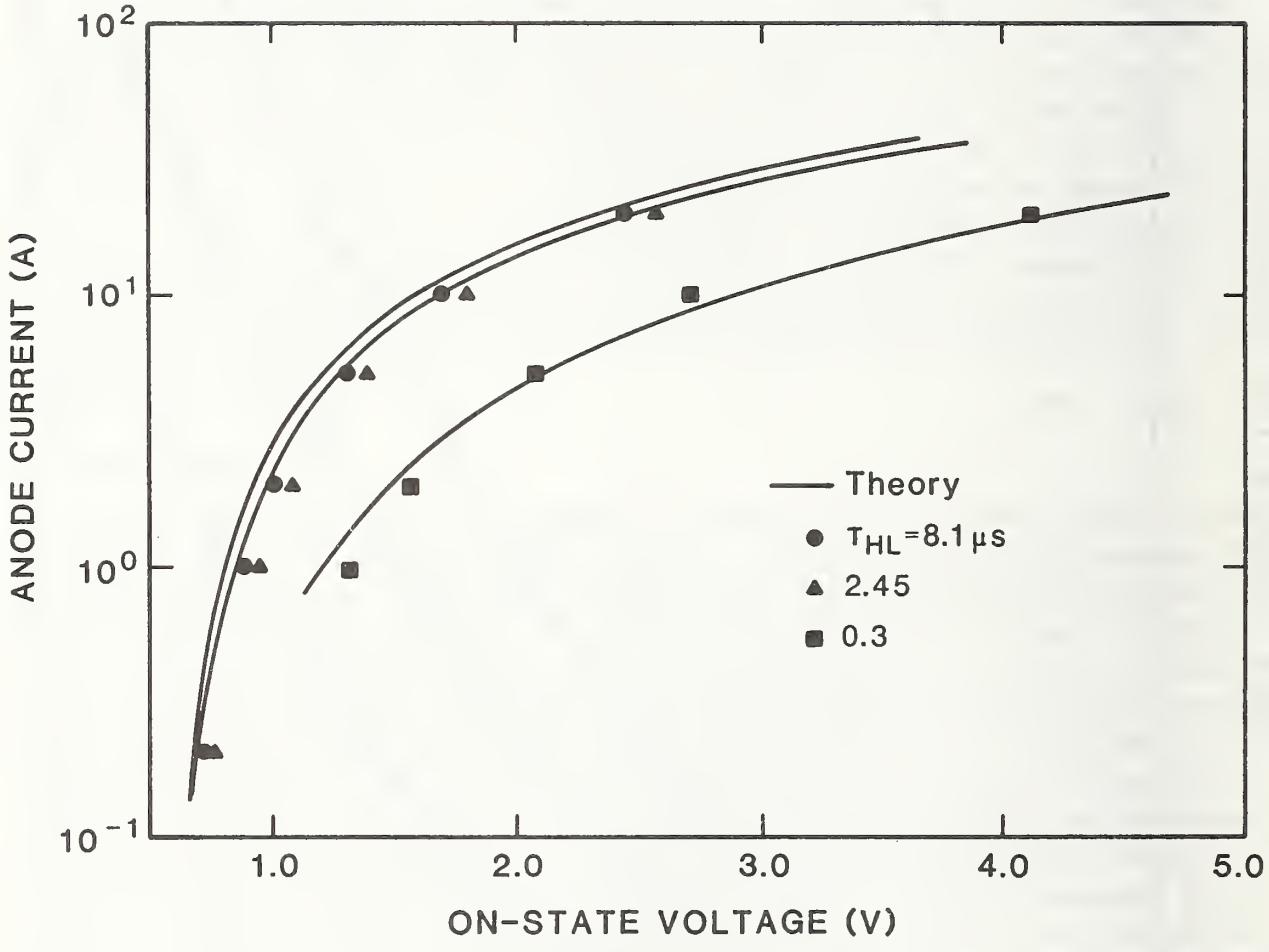


Figure 33. Predicted and measured on-state voltage versus current at $V_{gs} - V_T = 35$ V for devices with different base lifetimes.

base. After the gate voltage reaches its off-state value and the MOSFET portion of the current is removed, the current waveform is described by eq (T1.2) and eq (T1.3). For the constant voltage condition, eq (T1.2) reduces to an algebraic equation for the current in terms of charge

$$I_T \approx \frac{4D_p}{W^2} Q, \tag{30}$$

where W is constant for constant anode voltages which are much larger than the emitter-base voltage, neglecting the effect of mobile carriers on the depletion region space charge concentration. The current versus time is then obtained by integrating eq (T1.3) where only the last two terms are non-zero. Because the current is equal to a constant times the charge, eq (T1.3) indicates that the current decays exponentially with a time constant of τ_{HL} at low currents and that at high currents the rate is increased due to injection of electrons into the emitter.

Figure 34 shows the measured slowly decaying portion of the current decay waveform over several decades on a semi-log scale. This figure was obtained by overlapping the current decay waveforms with different values of initial currents. After a short redistribution phase ($t > 0.5\mu$s), the current decay waveform follows a path independent of the initial current. The redistribution portion of the waveform at each initial current is evident from the beginning of each waveform, which does not lie on the continuous curve. The independence of the decay rate on the initial current after the redistribution phase means that the decay rate depends only on the instantaneous value of current and can be described by the charge control model. Notice that the charge control current decay rate is nearly constant in the intermediate current range and that it increases at both low and high currents. The increased decay rate at high currents is due to injection of electrons into the emitter. The linearity of the data of figure 19 verifies that the model accurately describes the charge decay rate over the practical current range of the IGBT and thus verifies eq (T1.3). The increased decay rate for current below the practical current density range is not included in the model.

Constant Current Voltage Rise: Next, consider the clamped inductive load with a large inductor (~1 mH) and a large clamp capacitor. As an example, figure 35 shows the predicted $I_T = 10$ A, large inductive load, turn-off current and voltage waveforms at different clamp voltages for a device with the parameters listed in tables 4 and 5, and a base lifetime of 7.1 μs. Before the clamp voltage is reached, the large inductance keeps the anode current constant at the initial value determined by the steady-state conditions. Measured and simulated voltage waveforms for a large inductor load are compared in figure 36 for devices with different base lifetimes at a current of 10 A. The simulated voltage rate-of-rise is primarily determined by eq (T1.2), and the agreement with experiment verifies this expression. Notice that the voltage rate of rise varies significantly with device base lifetime. This is caused by the effective increase in the output capacitance due to the moving boundary redistribution current. Because the depletion layer width is large for the voltages in the curves in figure 36, the effect of mobile carrier charge on the depletion layer space charge concentration is significant. For example, figure 37 shows the measured and simulated large inductor voltage waveforms for two values of initial anode current and a

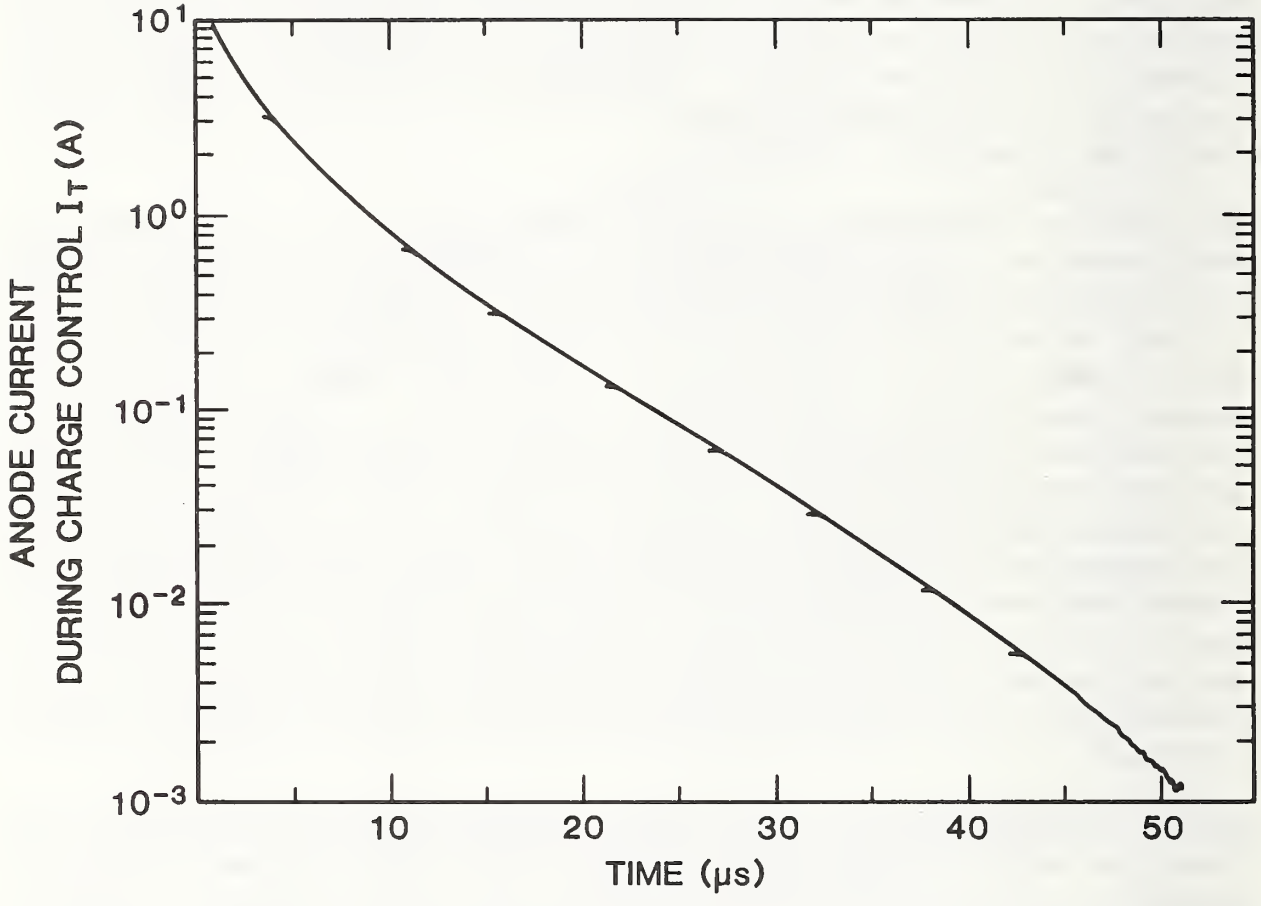


Figure 34. The charge control current decay path obtained by superimposing nine digitized current decay waveforms taken at different initial currents.

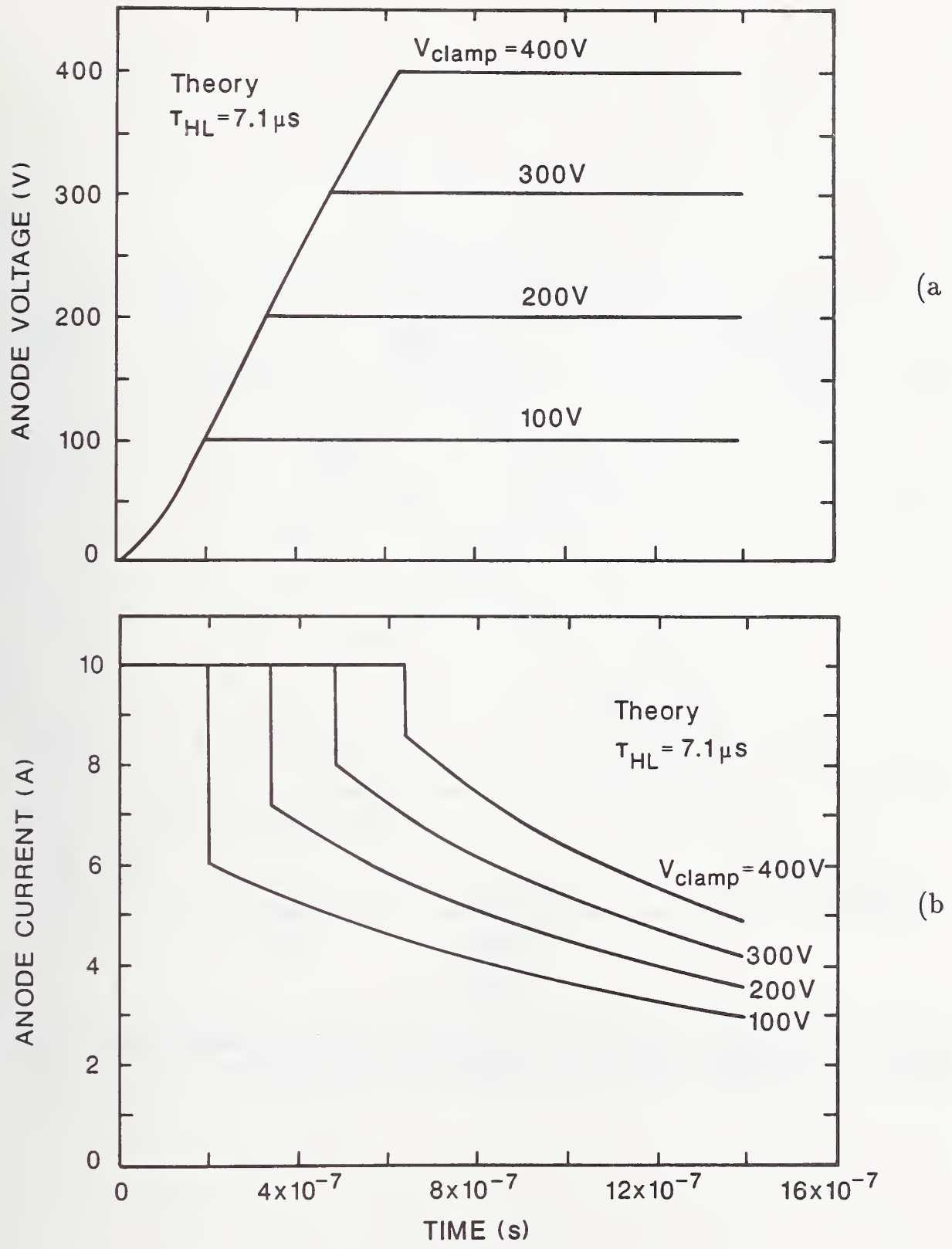


Figure 35. Predicted infinite inductive load switching voltage (a) and current (b) waveforms for a 7.1-μs device at different clamp voltages.

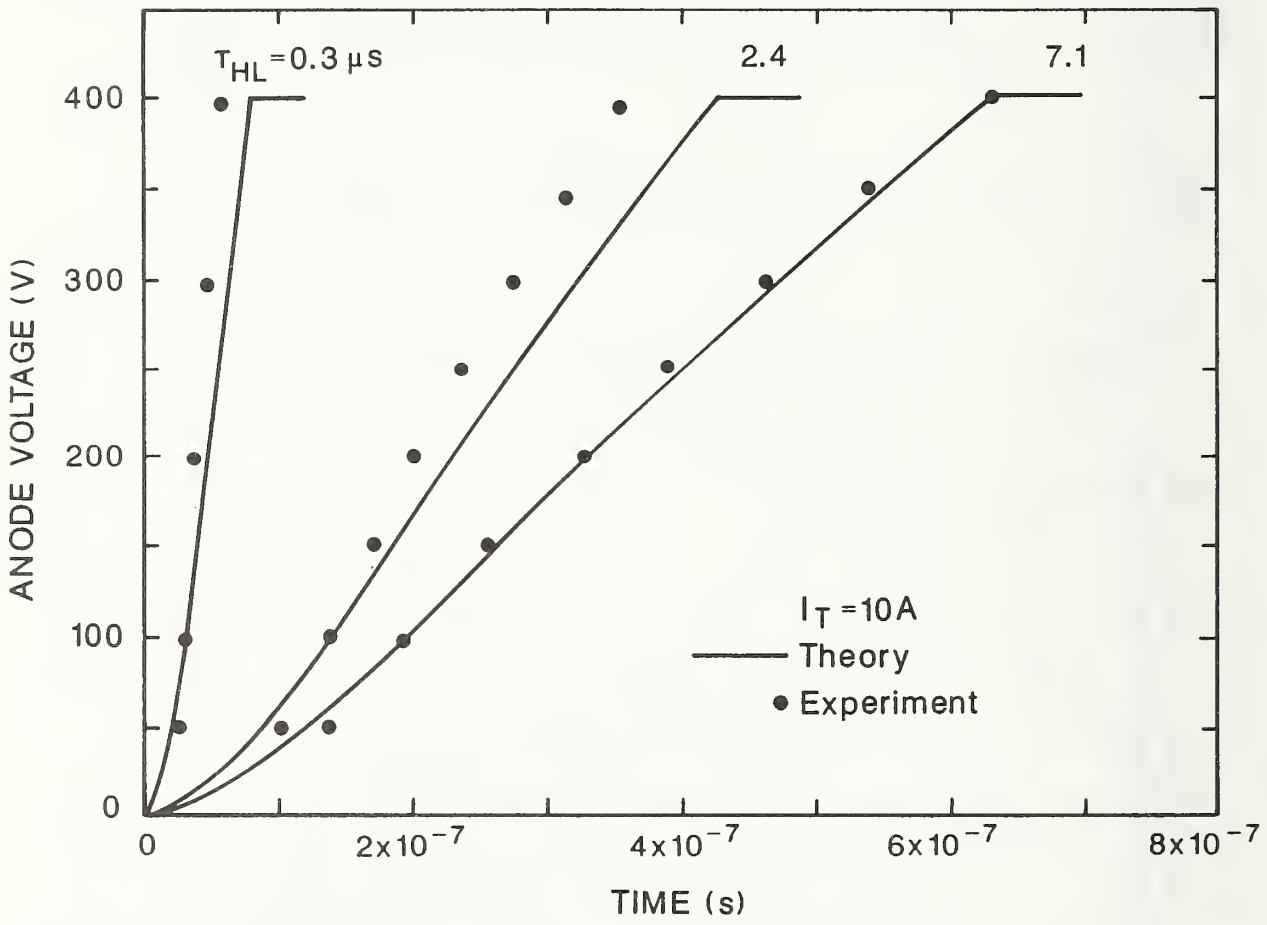


Figure 36. A comparison of the theoretical and measured 10-A infinite inductive load switching voltage waveforms for devices with different base lifetimes.

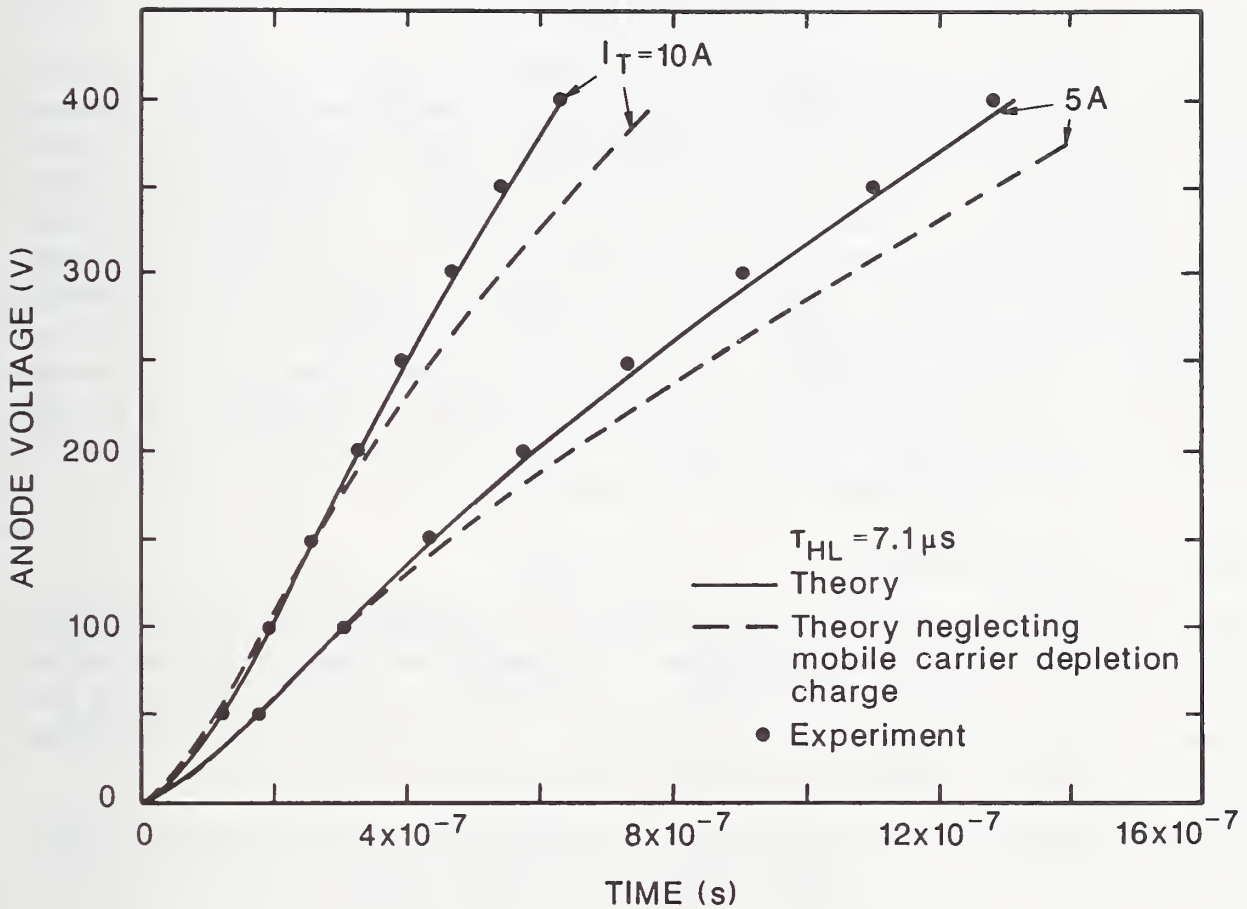


Figure 37. A comparison of the theoretical and measured infinite inductive load switching voltage waveforms for a 7.1-μs device at 5 A and 10 A. The dashed lines indicate the theoretical values neglecting the effect of mobile carriers on the collector-base space charge concentration.

device base lifetime of 7.1 μs. The dashed curves show the calculated values neglecting this effect, and the solid curves account for this effect using eq (1).

Relative Size of the Current Tail: The ratio of the initial value of the slowly decaying portion of the current decay waveform to the magnitude of the initial rapid fall in current is defined as:

$$\beta_{tr} = \frac{I_T(0^+)}{I_T(0^-) - I_T(0^+)}, \tag{31}$$

where $I_T(0^-)$ is the steady-state anode current, and $I_T(0^+)$ is the initial value of the slowly decaying portion (see fig. 20). Figure 38 compares the measured and calculated values of β_{tr} for constant anode supply voltage switching ($\beta_{tr,V}$) and β_{tr} for large inductor load switching ($\beta_{tr,L}$) versus current, both at two different voltages. The values of $\beta_{tr,L}$ differ from the values of $\beta_{tr,V}$ because the excess carrier base charge is swept into a narrower base (narrower than for steady-state) during the voltage rise, and because some of the charge decays during the voltage rise. The dashed curves in figure 38 show the effects of neglecting this decay by using the steady-state charge in calculating $I_T(0^+)$. The agreement between the model and the experiment for $\beta_{tr,V}$ indicates that the value of steady-state charge used by the model is adequate for an initial condition of the transient. The agreement between the theory and experiment for $\beta_{tr,L}$ at different voltages indicates that the charge decay is properly accounted for during anode voltage transitions.

Interaction With Load Circuit

In this subsection, the interaction of the IGBT with external loading circuits is examined by considering the turn-off anode voltage and anode current waveforms for various loading conditions and for a stiff gate drive condition. For the stiff gate drive condition, the gate voltage is rapidly switched to its off-state value so that the drive circuit has negligible influence on the anode current and voltage switching behavior.

Series Resistor-Inductor Load: Figure 39a shows the measured current and voltage-switching waveforms for a series resistor-inductor load circuit of figure 6 with $R = 31\ \Omega$, $L_L = 5.5\ \mu$H, and $V_{AA} = 150$ V. A stiff gate drive circuit is used so that the drive circuit parameters do not influence the output waveforms. Figure 39b shows the simulated results for the same conditions as the measurements of figure 39a. The theoretical and experimental waveforms are in good quantitative agreement with the exception that the ringing is damped more in the experiment. Notice in figures 39a and 39b that the voltage overshoots more and that the current approaches zero faster for the lower lifetime devices. The overshoot results from the stored energy in the inductor which is transferred to the effective output capacitance of the IGBT. It is evident from figure 36 that the effective output capacitance of the IGBT (proportional to the time rate-of-change of anode voltage) varies significantly with lifetime and that it is well described by the model.

The combinations of values of R, L_L, V_{AA}, and τ_{HL} which are suitable for unprotected series resistor-inductor load switching with a fast gate voltage transition are limited. For example, figures 40 through 42 show the simulated and measured series resistor-inductor

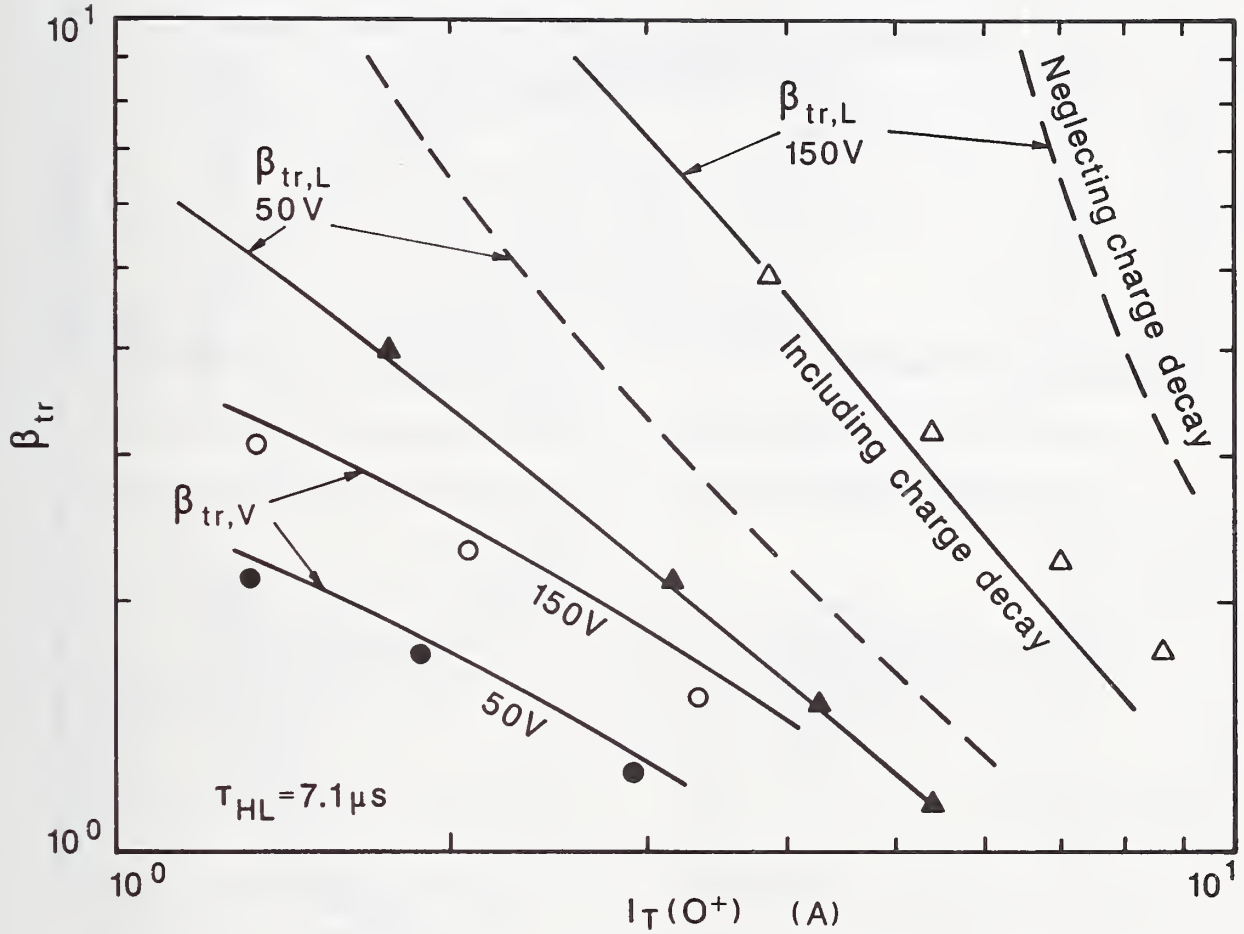


Figure 38. A comparison of the theoretical (solid curves) and measured values (symbols) of β_{tr} versus current for both constant anode supply voltage switching (circles) and clamped inductive load switching (triangles) at 50 V (solid symbols) and 150 V (open symbols) for a 7.1-μs device. The dashed curves are the calculated values of $\beta_{tr,L}$ neglecting the loss of charge during the voltage transition.

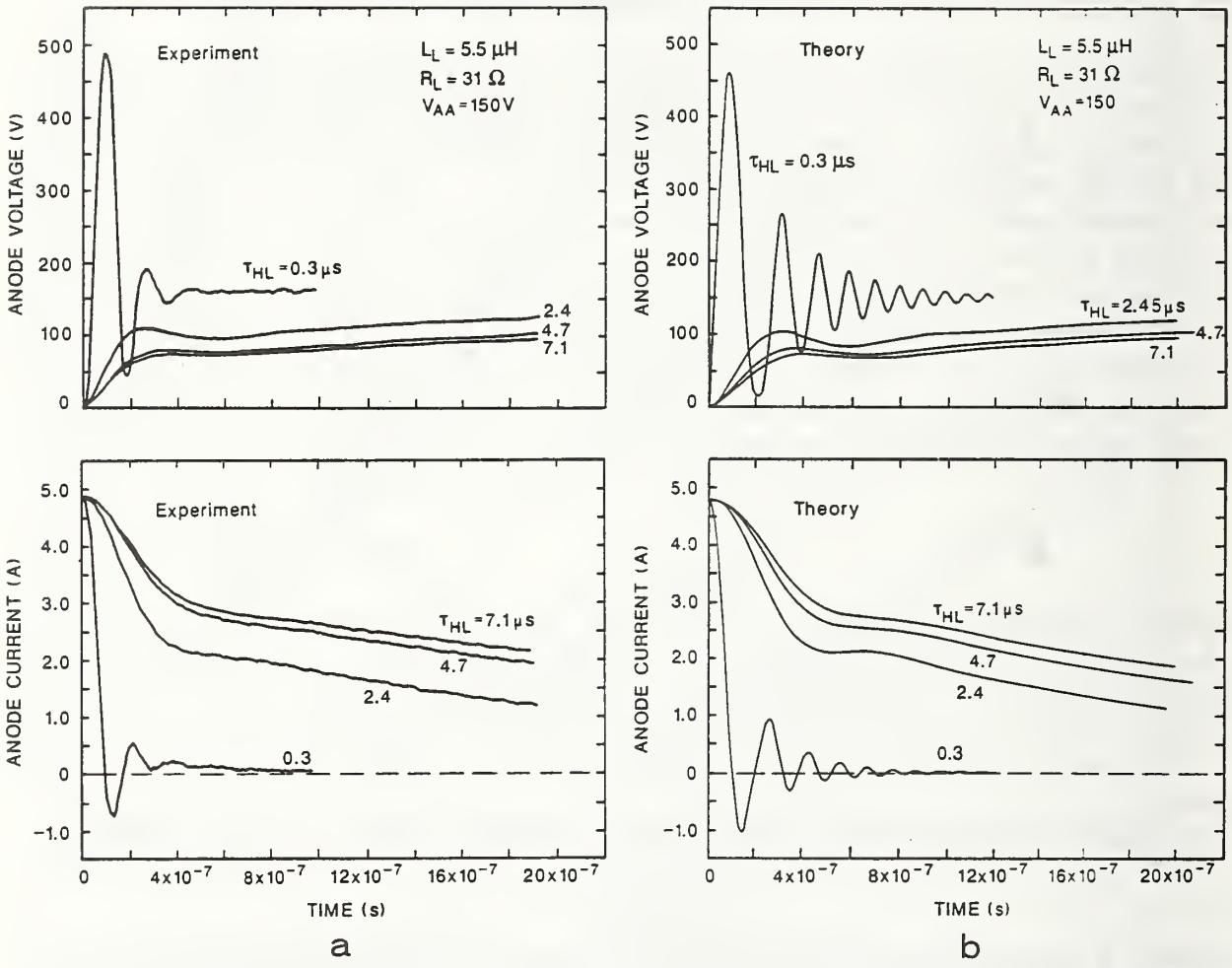


Figure 39. The measured (a) and simulated (b) series 31-Ω resistor, 5.5-μH inductor load current and voltage waveforms for devices with different lifetimes.

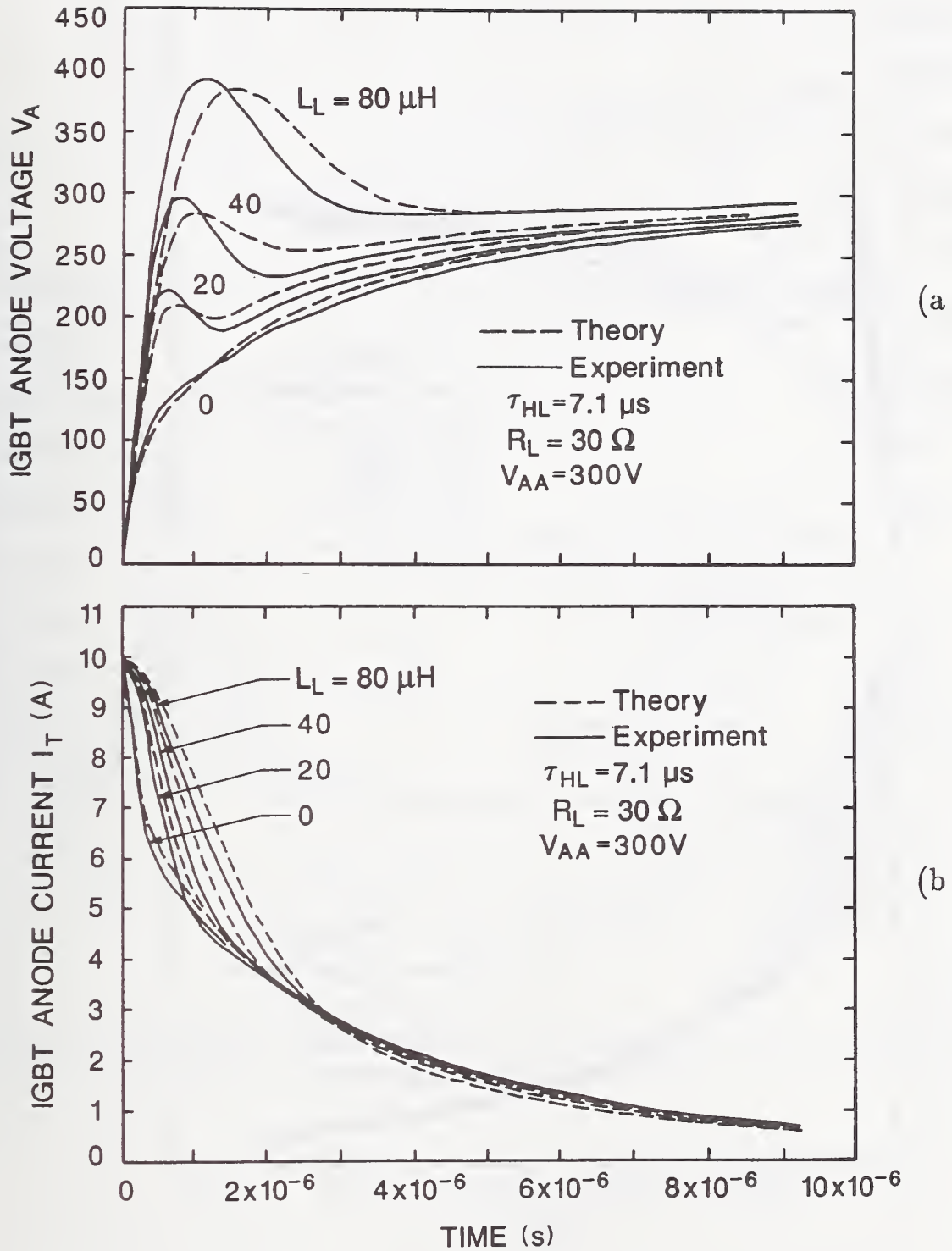


Figure 40. The measured and simulated series resistor-inductor load voltage (a) and current (b) waveforms for a 7.1-μs device and inductances from 0 to 80 μH.

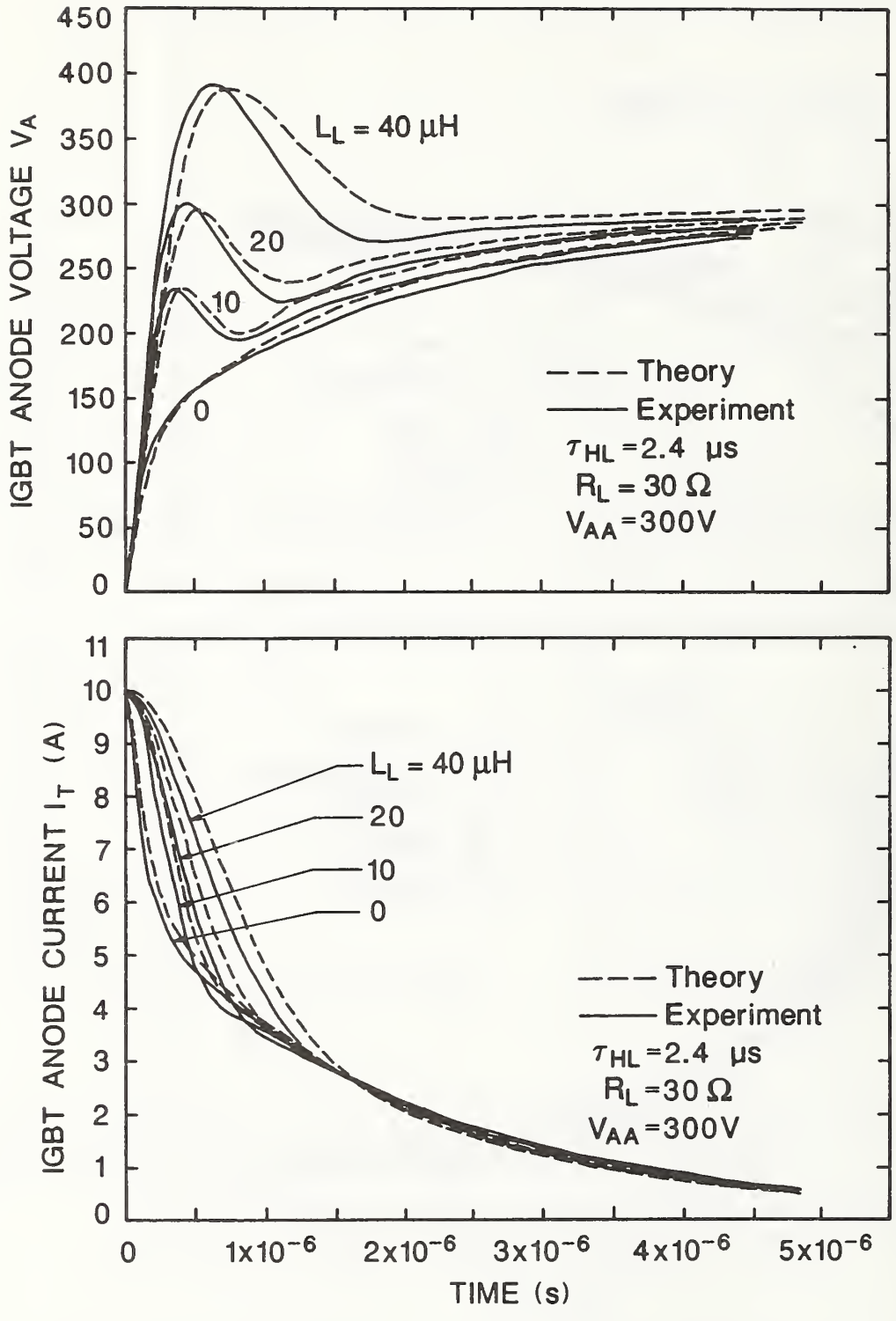


Figure 41. The measured and simulated series resistor-inductor load voltage (a) and current (b) waveforms for a 2.4-μs device and inductances from 0 to 40 μH.

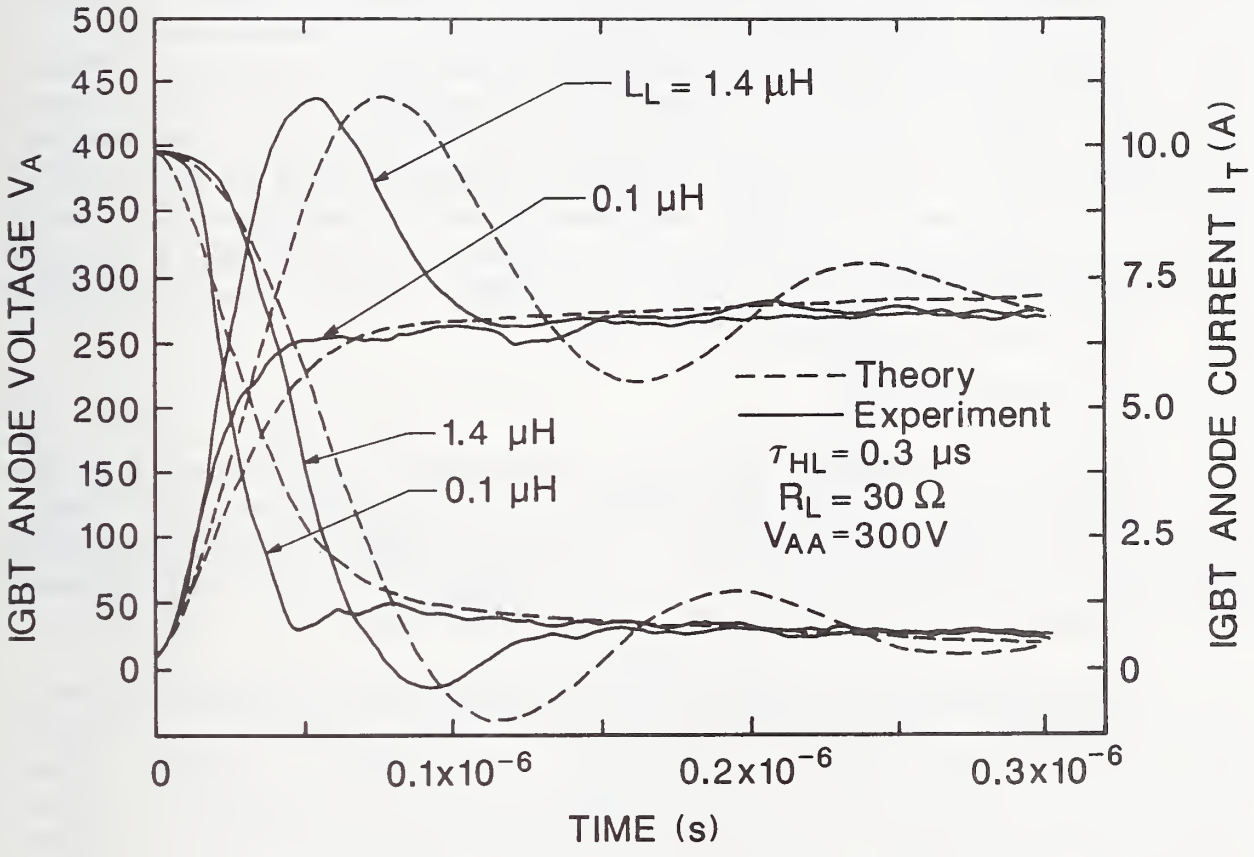


Figure 42. The measured and simulated series resistor-inductor load current and voltage waveforms for a 0.3-μs device and inductances of 0.1 to 1.4 μH.

load current and voltage-switching waveforms for values of inductance that can be safely switched. Each figure is for a different device lifetime. For inductances larger than 40 μH, the peak overshoot voltage for the 2.4-μs device (fig. 41) approaches the BV_{CEO} of the IGBT (500 V), and the voltage will be clamped by the avalanche current. This is potentially destructive, so a protection circuit must be added to the 2.4-μs device for load inductances larger than 40 μH. For otherwise identical conditions, the 7.1-μs device can switch 80 μH (fig. 40) and the 0.3-μs device can switch 1 μH (fig. 42) without excessive voltage overshoot.

Polarized Turn-off Snubber: The simulated and measured series resistor-inductor load current and voltage waveforms including the protection circuit of figure 7 are shown in figures 43 through 45 for inductances which are too large to be switched without a protection circuit. The simulations are performed using eqs (9), (15), and (16) to describe the external circuit. Each figure is for a different device lifetime and load inductance. Figures 43 and 44 include two different values of C_S. For lower values of C_S or larger L_L, the overshoot approaches the device voltage rating. These figures demonstrate that the IGBT model in INSTANT can be used to determine the values of the protection circuit components needed for a given load circuit inductance. The simulations can also be used to examine other quantities of importance in the design of a snubber circuit, such as the switching energy of the device and the efficiency of the circuit.

Interaction With Drive Circuit

In this subsection, the interaction of the IGBT with external drive, load, and feedback circuits is examined. For small gate drive currents, a significant time is required to charge the gate-source and gate-drain capacitances. This results in a switching delay time and a reduced time rate-of-change of anode voltage. The small gate currents occur for large gate drive resistances and for external gate-drain feedback capacitors.

Turn–Off Transient: Figures 46a through 46c show the measured and simulated, gate and anode, current and voltage turn-off waveforms for the circuit of figure 6 with different values of gate resistance, where figures 46a, 46b, and 46c are each for a different device base lifetime and load inductance. The load inductances are chosen for each device so that the anode voltage overshoot will not exceed the device voltage rating of 500 V. The gate voltage pulse amplitude of $V_{gon} = 20$ V is chosen so that the plateau in gate current occurs at approximately the same magnitude for turn-on as for turn-off. The 15-ns fall time of the gate pulse generator is also included in the simulations. The gate voltage pulse widths for the simulations and measurements are chosen so that a steady-state condition is reached before the devices are switched off. The load resistance of 30 Ω results in a steady-state current of 10 A for the anode supply voltage of 300 V.

The turn-off sequence of figures 46a through 46c begins when V_{gg} is switched rapidly to zero. Initially, V_{gs} begins to fall as the gate capacitance is discharged through the gate resistance, and V_{ds} rises a few volts so that the current through the MOSFET channel (linear region of eq (T2.15)) remains relatively constant. Once V_{gs} has fallen and V_{ds} has risen to the point where the MOSFET enters the current saturation region $V_{ds} \geq V_{gs} - V_T$,

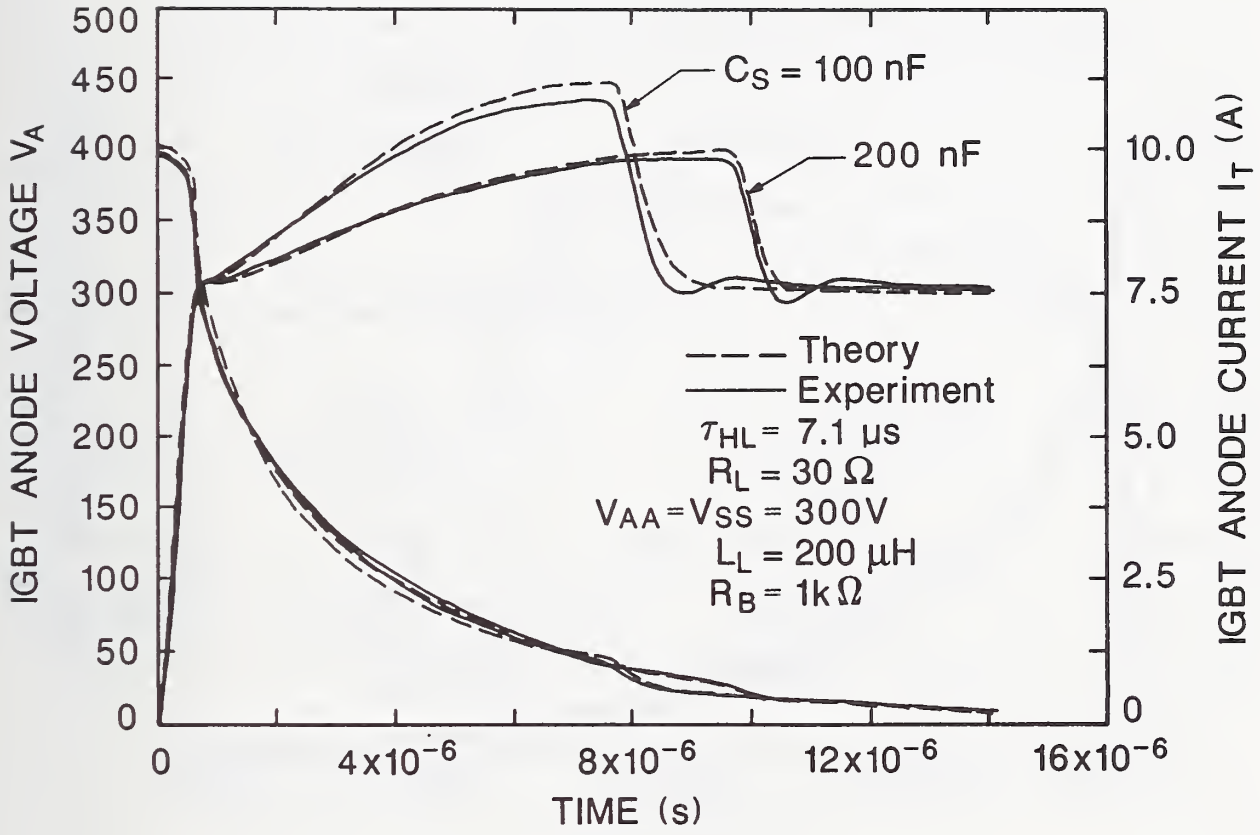


Figure 43. The simulated and measured snubbed series resistor-inductor load current and voltage waveforms for a 7.1-μs device, a 200-μH inductance, and two different snubber capacitances.

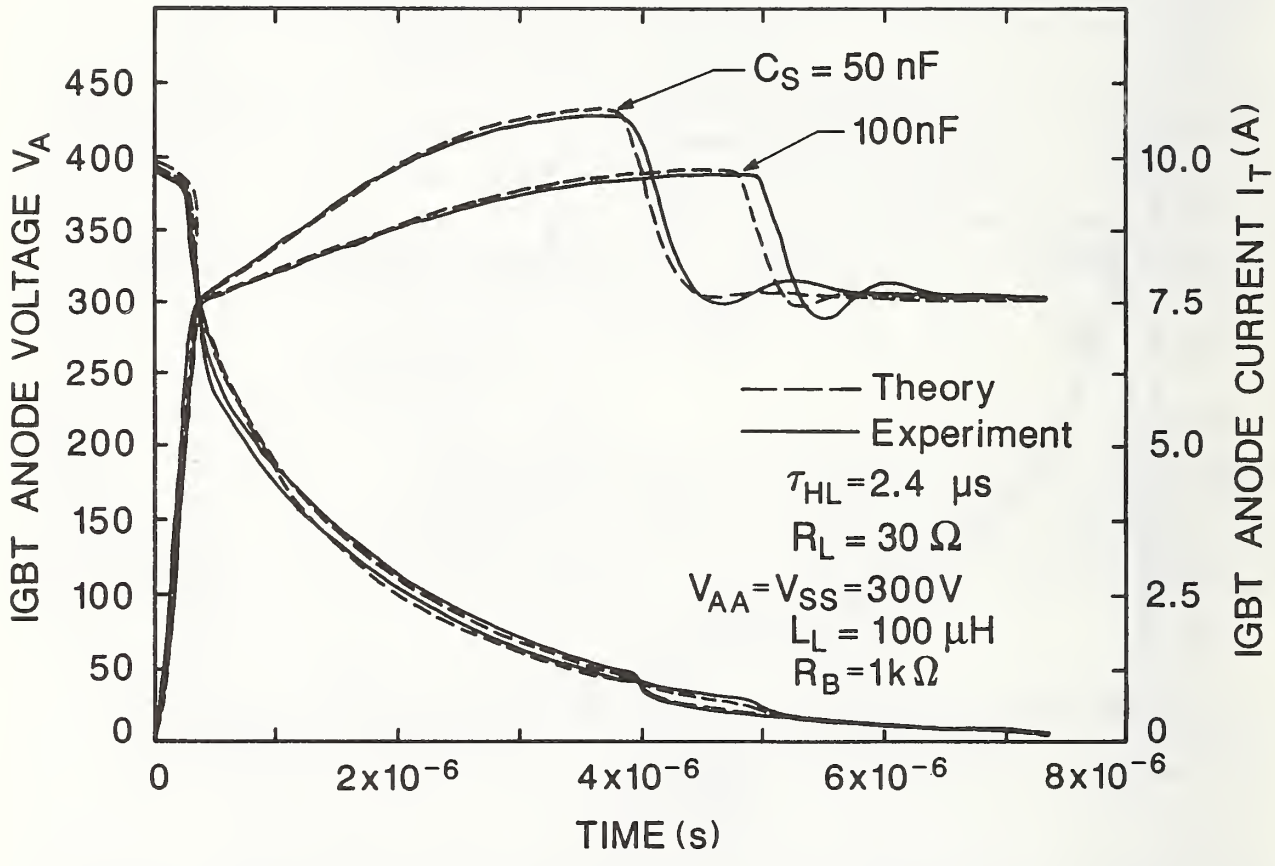


Figure 44. The simulated and measured snubbed series resistor-inductor load current and voltage waveforms for a 2.4-μs device, a 100-μH inductance, and two different snubber capacitances.

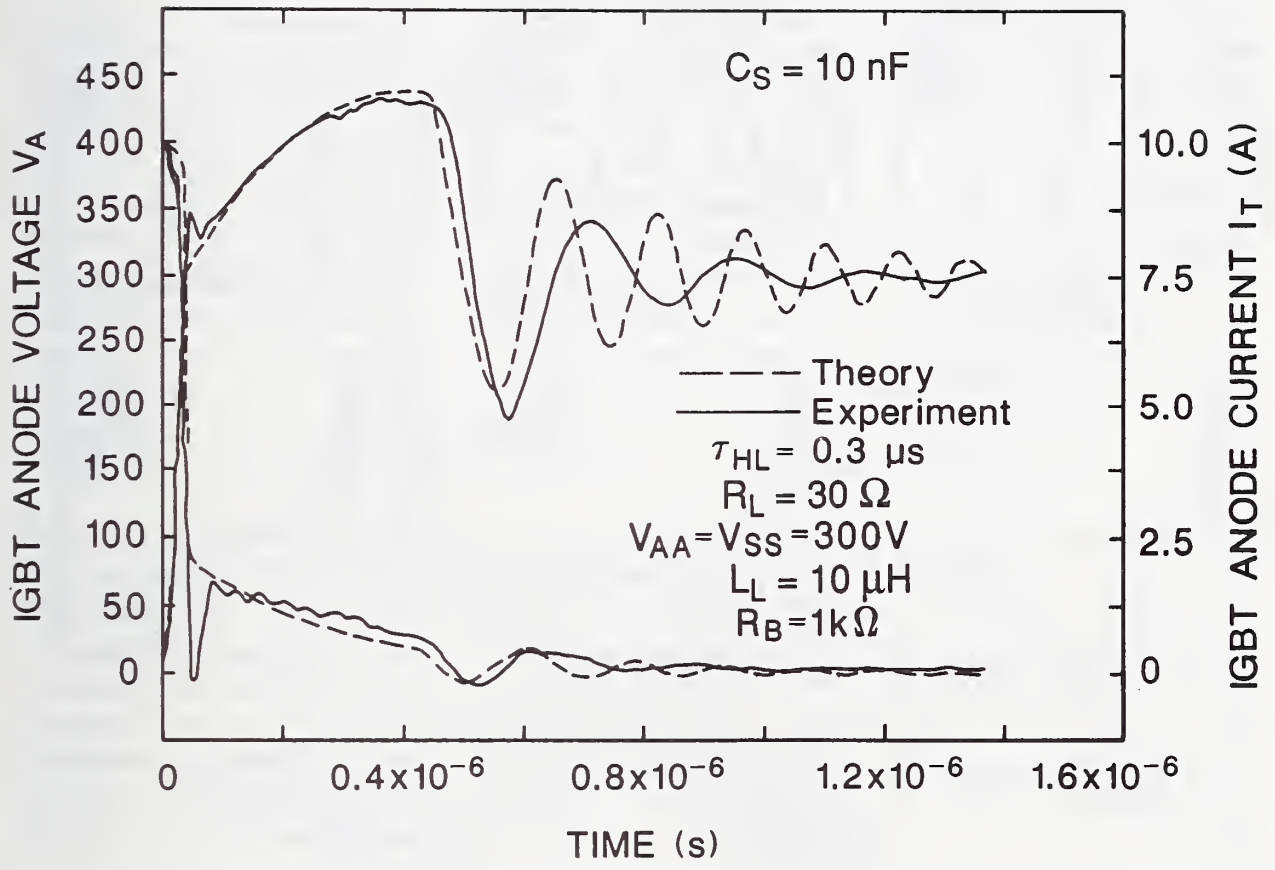


Figure 45. The simulated and measured snubbed series resistor-inductor load current and voltage waveforms for a 0.3-μs device and a 10-μH inductance.

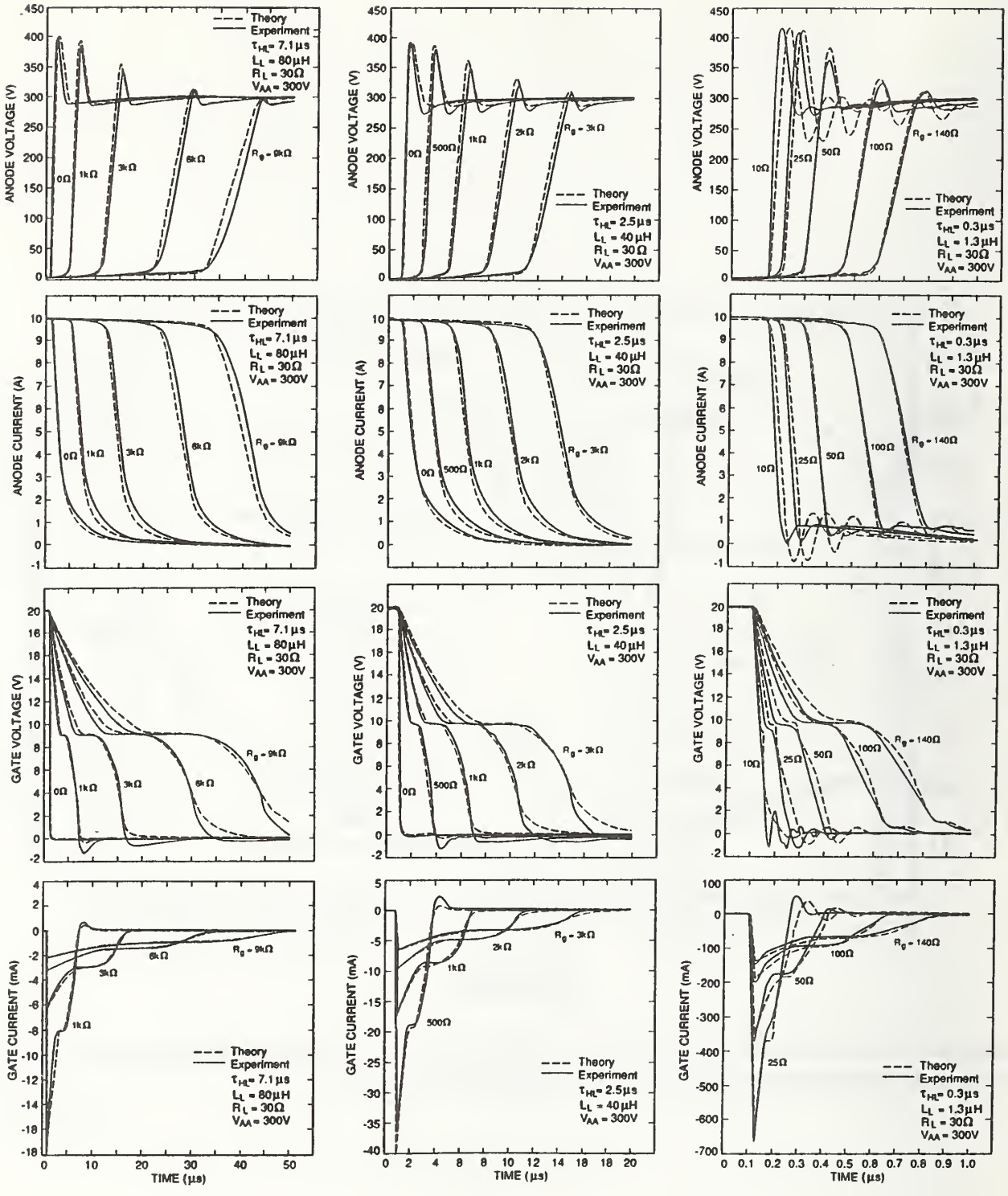


Figure 46. Comparison of the measured and simulated, gate and anode, current and voltage turn-off waveforms for the circuit of figure 6 with different values of gate resistance, where (a) is for a 7.1-μs device, (b) is for a 2.5-μs device, and (c) is for a 0.3-μs device.

the gate voltage remains constant at $V_{gs} = V_T + \sqrt{2I_{mos}/K_{psat}}$ and the gate current charges the large gate-drain overlap oxide capacitance as V_{ds} rises slightly faster. This plateau in V_{gs} continues until V_{ds} rises to the point where the gate-drain overlap capacitance becomes depleted, $V_{ds} \geq V_{gs} - V_{Td}$. Beyond this point, the gate-drain feedback capacitance is reduced by about two orders of magnitude and the anode voltage rate-of-rise increases sharply. Because V_A rises only slightly during the first two phases (from the on-state voltage to about 10 V), they are perceived as a delay in the turn-off where the delay time is nearly proportional to the gate resistance.

After the turn-off delay, the anode voltage rate-of-rise is determined by the effective output capacitance C_{out} (denominator of eq (T1.2)) if $I_g/C_{gdj} \gg I_T/C_{out}$; otherwise, the anode voltage rate-of-rise is limited by the gate current that charges the high-voltage gate-drain feedback capacitance C_{gdj}. For a power MOSFET with a structure similar to that of the IGBT in figure 1, C_{out} is on the same order of magnitude as C_{gdj} because $A_{gd} \approx A_{ds}$ and the gate current limits the anode voltage rate-of-rise for $I_g < I_T$, i.e., for $R_g > 2\ \Omega$. However, as mentioned above, the effective output capacitance of the IGBT is several orders of magnitude larger than that of the structurally equivalent power MOSFET and depends upon the device base lifetime. Thus, the rate-of-rise of anode voltage and the anode voltage overshoot are not affected by gate resistances below 1 kΩ for the 7.1-μs IGBT of figure 46a, below 500 Ω for the 2.5-μs IGBT of figure 46b, or below 25 Ω for the 0.3-μs IGBT of figure 46c. For gate resistances larger than these values, though, the anode voltage rate-of-rise and the voltage overshoot are reduced (active snubbing).

Turn-On Transient: Figure 47 shows the measured and simulated, gate and anode, current and voltage turn-on waveforms for the circuit of figure 6 with different values of gate resistance. The disagreement between the simulated and measured gate current and gate voltage waveforms is due to the source lead inductance which is not included in the simulations for simplicity. The small value of load inductances is chosen for this example to show that both the anode current and anode voltage can change rapidly at turn-on. Because the turn-on waveforms are relatively independent of device base lifetime, they are only shown for the 2.5-μs device. The gate voltage pulse amplitude of $V_{gon} = 20$ V is the same as for the turn-off results, and the rise time of the gate pulse generator is also 15 ns.

The turn-on sequence of figure 47 begins when V_{gg} is switched rapidly to V_{gon}. Initially, V_{gs} rises as the gate capacitance is charged through the gate resistance, and V_A remains relatively constant at V_{AA} while $V_{gs} < V_T$. This phase appears as a short turn-on delay that is proportional to the gate resistance. Once V_{gs} exceeds V_T, the MOSFET enters its saturation region and the anode current increases as V_{gs} continues to increase. During this phase, the gate current charges the gate-source capacitance and discharges the gate-drain capacitance as V_A decreases rapidly. Once V_{gs} has risen and V_{ds} has fallen to the point where the gate-drain overlap depletion region vanishes, $V_{ds} \leq V_{gs} - V_{Td}$, the gate-drain capacitance increases by approximately two orders of magnitude, so V_{gs} remains relatively constant at $V_{gs} = V_T + \sqrt{2I_{mos}/K_{psat}}$ and the gate current charges the large gate-drain overlap oxide capacitance as V_A falls slowly. Once V_{ds} is reduced to the point where the MOSFET enters the linear region $V_{ds} \leq V_{gs} - V_T$, the gate voltage begins to rise again

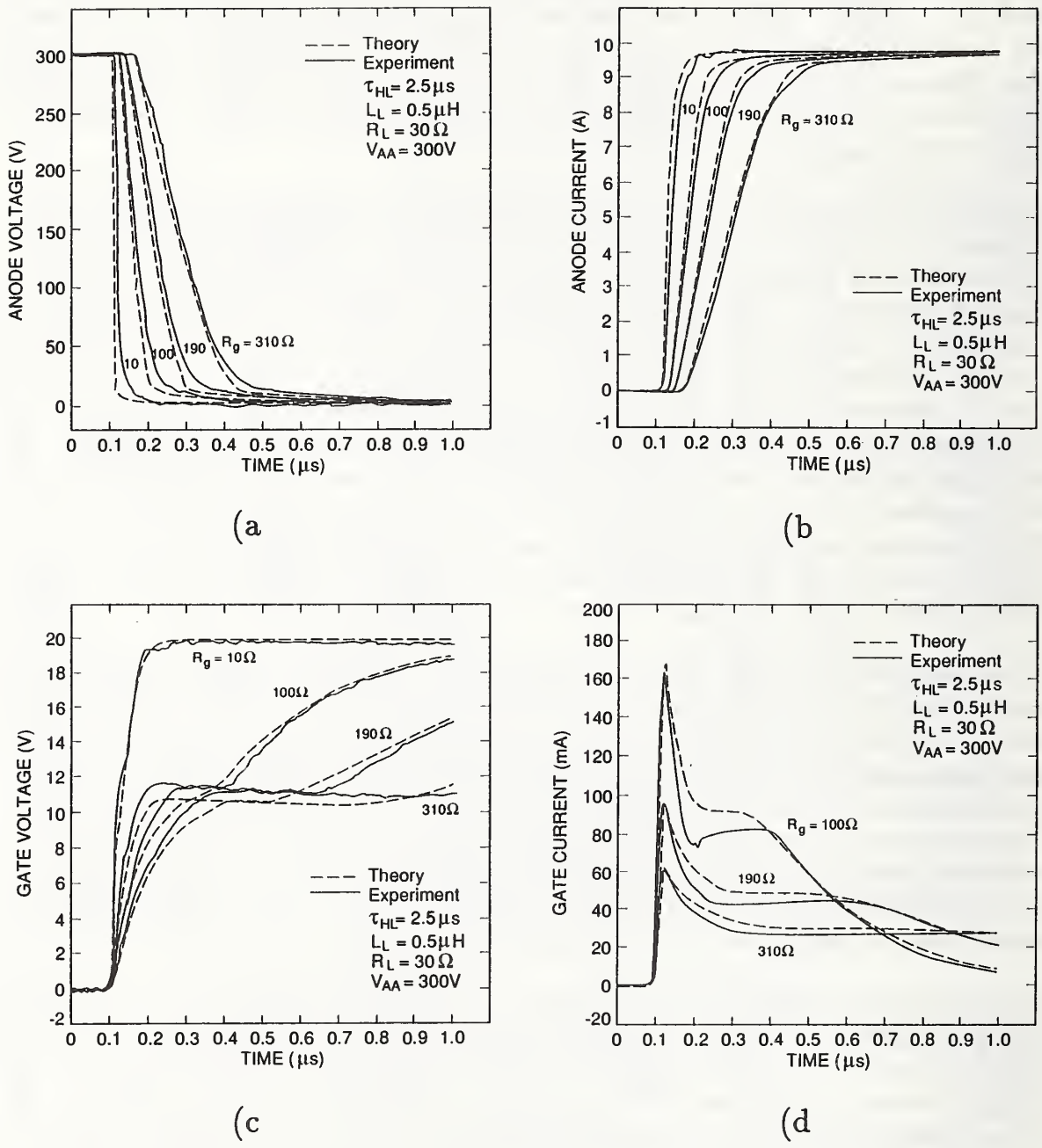


Figure 47. Comparison of the measured and simulated anode voltage (a), anode current (b), gate voltage (c), and gate current (d) turn-on waveforms for the circuit of figure 6 with different values of gate resistance.

and V_{ds} continues to fall slowly so that the current through the MOSFET channel (linear region of I_{mos} in table 1) remains relatively constant.

Comparing figures 46 and 47, it is evident that the anode voltage rate-of-fall at turn-on is influenced by much smaller gate resistances than those that influence the anode voltage rate-of-rise at turn-off. This occurs because Q is zero at the beginning of the turn-on sequence and the effective output capacitance depends upon Q (denominator of eq (T1.2)). Thus, the anode voltage rate-of-fall at turn-on is as rapid for the IGBT as it is for the structurally equivalent power MOSFET. The speed of the low anode voltage portion of the IGBT turn-on waveform (lower than the MOSFET on-state voltage) is limited, though, for $R_g < 30\ \Omega$ by the finite time required to supply the base charge that modulates the base resistance (dynamic saturation). For $R_g > 30\ \Omega$, the turn-on speed at low anode voltages is limited by the time required for the gate current to discharge the gate-drain overlap oxide capacitance.

Figure 48 shows the instantaneous emitter-base voltage and base charge for the same turn-on conditions as the $R_g = 10\ \Omega$ waveform of figure 47 and for two different device base lifetimes. For small load inductances and small gate resistances, the anode current can rise much faster than the base charge so that the base resistance is not conductivity-modulated and the potential across the base resistance may initially be as large as the potential across the nonconductivity-modulated epitaxial layer resistance of the structurally equivalent power MOSFET ($\sim$ 15 V). But, the base resistance rapidly becomes modulated, because I_{mos} is initially nearly as large as the total current (10 A), and Q approaches ten times the background base charge ($Q_B \sim 30$ nC) in approximately 30 ns (see eq (T1.3) and the time rate-of-change of Q on fig. 48). The turn-on speed is relatively independent of the device base lifetime because the time required to modulate the base resistance depends primarily upon the MOSFET current and the base transit time.

Active Snubbing: It has been proposed by others (e.g., ref. [22]) that the gate resistance can be used to control the voltage rate-of-rise at turn-off for the IGBT (active snubbing). However, as can be seen from figure 46, a large value of gate resistance is required to have an influence on the voltage rate-of-rise at turn-off for the IGBTs. Therefore, it is beneficial to use a polarized gate drive resistance in this instance so that the turn-on time is not also increased. In addition, a very long, possibly unacceptable turn-off delay time results for gate resistances large enough to have an influence on the IGBT anode voltage rate-of-rise at turn-off (e.g., 30-μs turn-off delay for the $R_g = 9\ \text{k}\Omega$ waveform in fig. 46a). This occurs because the gate-drain overlap oxide capacitance is much larger than the high-voltage gate-drain overlap depletion capacitance.

It has been suggested by others [23], though, that the time rate-of-change of drain voltage for power VDMOSFETs can be controlled independently of the delay time by inserting a small capacitor from gate-to-drain. This occurs because the ratio of the net gate-to-drain feedback capacitance at high voltages to that at low voltages is increased by inserting the external feedback capacitor. This technique is especially beneficial for the IGBT due to the excessively long delay times incurred [3]. It is proposed by Hefner [3] that a large

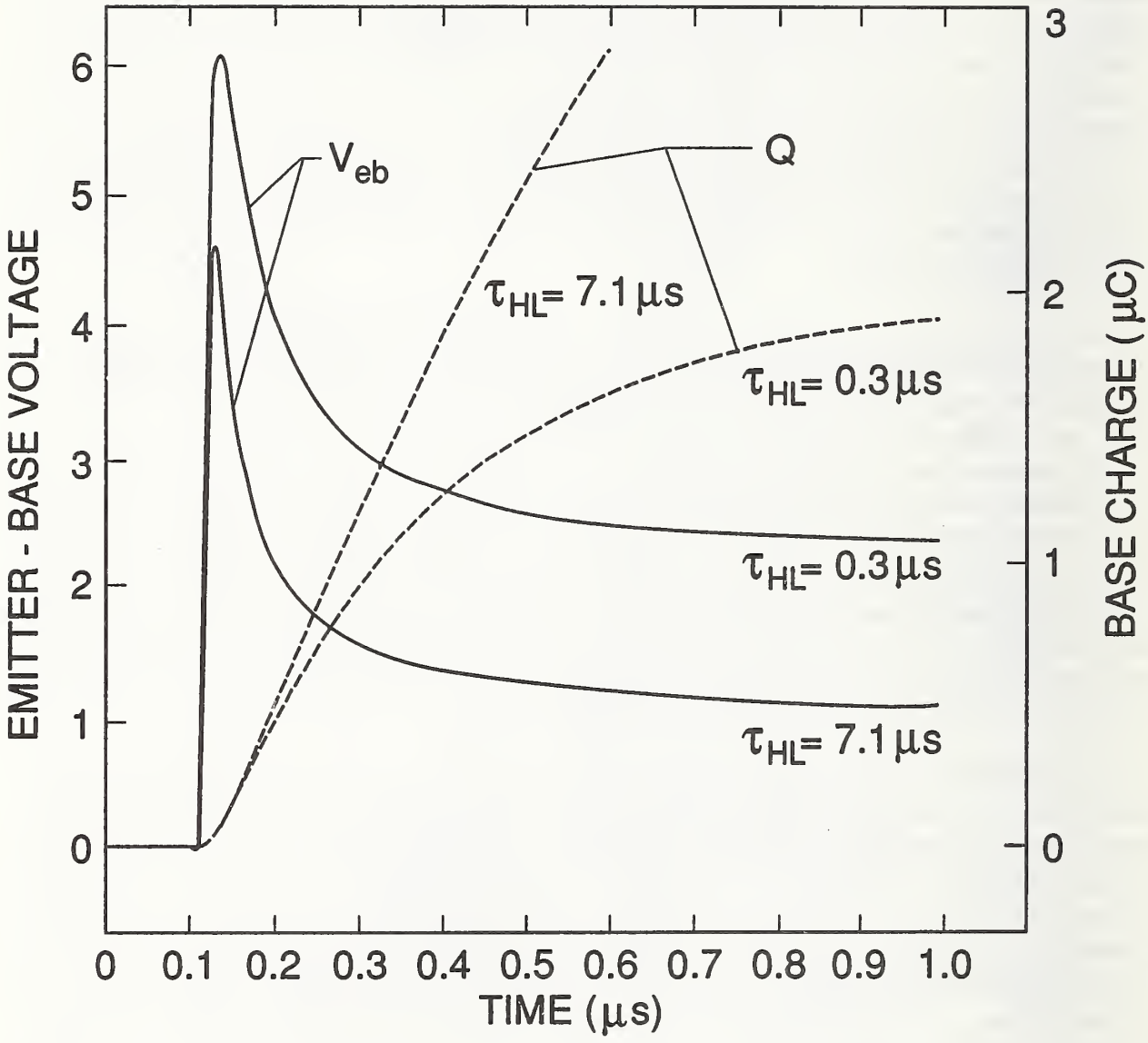


Figure 48. The emitter-base voltage and base charge for the same turn-on conditions as the $R_g = 10\ \Omega$ waveform of figure 47 and for two different device base lifetimes.

gate-to-anode feedback resistor be placed in series with the external gate-to-anode feedback capacitor when used with the polarized gate resistance, so that the turn-on speed is not significantly reduced by the feedback network for a given turn-on gate resistance. A minimal value of series feedback resistance is also necessary to suppress high frequency oscillations [24]. The circuit configuration of the IGBT with this polarized active feedback snubber and a series resistor-inductor load is shown in figure 8 and the external circuit equations are given by eqs (9), (11), (14), (15) and (16).

As an example, figure 49 compares the simulated and measured turn-off anode voltage waveforms for circuit conditions similar to those of figure 46a with the exception that the external feedback circuit components of figure 49 are included in two of the waveforms. The R_g = 1-kΩ and 9-kΩ waveforms of figure 46a (i.e., $C_f = 0$) are repeated on figure 49 for comparison. It is evident from this figure that if a 0.2-nF external gate-to-anode capacitor is inserted, the 1-kΩ gate resistor results in a time rate-of-change of anode voltage and voltage overshoot similar to the 9-kΩ waveform of figure 46a, but with a turn-off delay similar to that of the 1-kΩ waveform of figure 46a. It is also evident from figure 49 that values of series feedback resistance as large as R_f = 10 kΩ do not diminish the effect of the feedback capacitor for the 1-kΩ gate resistor.

However, the effect of the feedback capacitor at turn-on is diminished by a series feedback resistance of 10 kΩ, because the turn-on gate current is larger than the turn-off gate current for the polarized gate resistance, and the feedback current becomes negligible if V_A/R_f is much less than the gate current. For example, figure 50 compares the simulated and measured turn-on anode voltage waveforms for the same circuit conditions as for figure 49 and for a turn-on gate resistance of R_{gon} = 100 Ω. For $R_f \leq 100\ \Omega$, the anode voltage rate-of-fall is determined by the gate current charging the external gate-to-anode feedback capacitor. However, for $R_f \geq 10$ kΩ, the turn-on anode voltage waveform is similar to the R_g = 100 Ω waveform of figure 47 (i.e., $C_f = 0$). Thus, the rate-of-rise of anode voltage at turn-off is controlled independently of the turn-off delay time and independently of the rate-of-fall of anode voltage at turn-on without increasing the drive circuit current requirements; i.e., it is not necessary to reduce R_{gon} to compensate for the addition of the external gate-to-anode feedback capacitor.

VII. CONCLUSIONS

An analytical model has been developed for the IGBT that is applicable for general external circuit conditions and is suitable for incorporation into circuit simulators. The analytical model is based upon ambipolar transport theory and does not assume the quasi-static condition for the transient analysis. To implement the IGBT model in the INSTANT circuit simulator described in this publication, the model is formulated as three state equations that describe the state of the base-collector voltage, the gate-source voltage, and the excess carrier base charge. The INSTANT program simulates the interaction of the IGBT with the external circuit by simultaneously integrating the IGBT state equations with those of the external circuit. A simplified procedure has been described for deriving the external circuit state equations by applying Kirchhoff's current and voltage laws to a

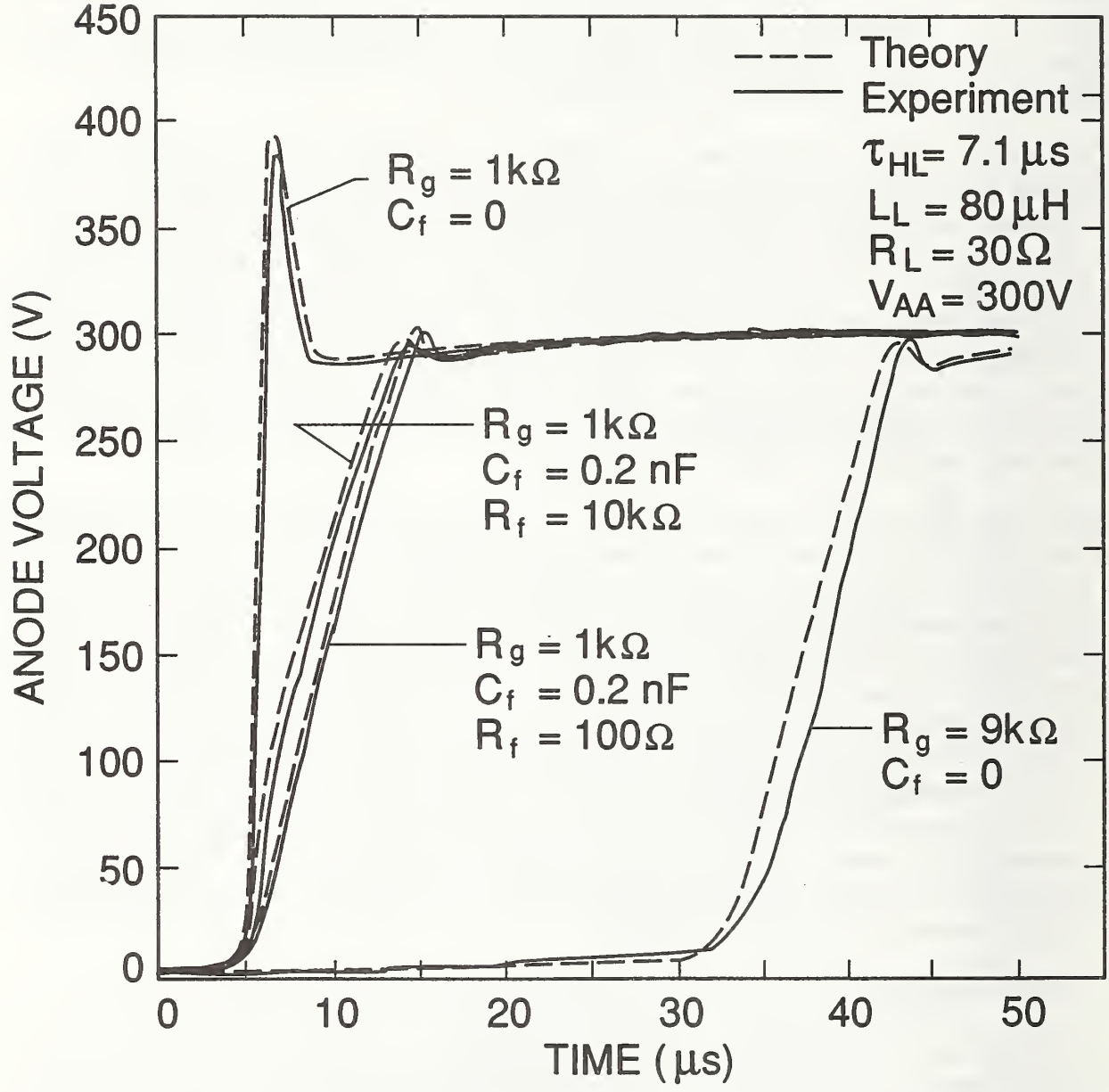


Figure 49. Comparison of the measured and simulated, anode voltage turn-off waveforms for the circuit of figure 8 with different values of gate resistance, external gate-to-anode feedback capacitances, and different series feedback resistances.

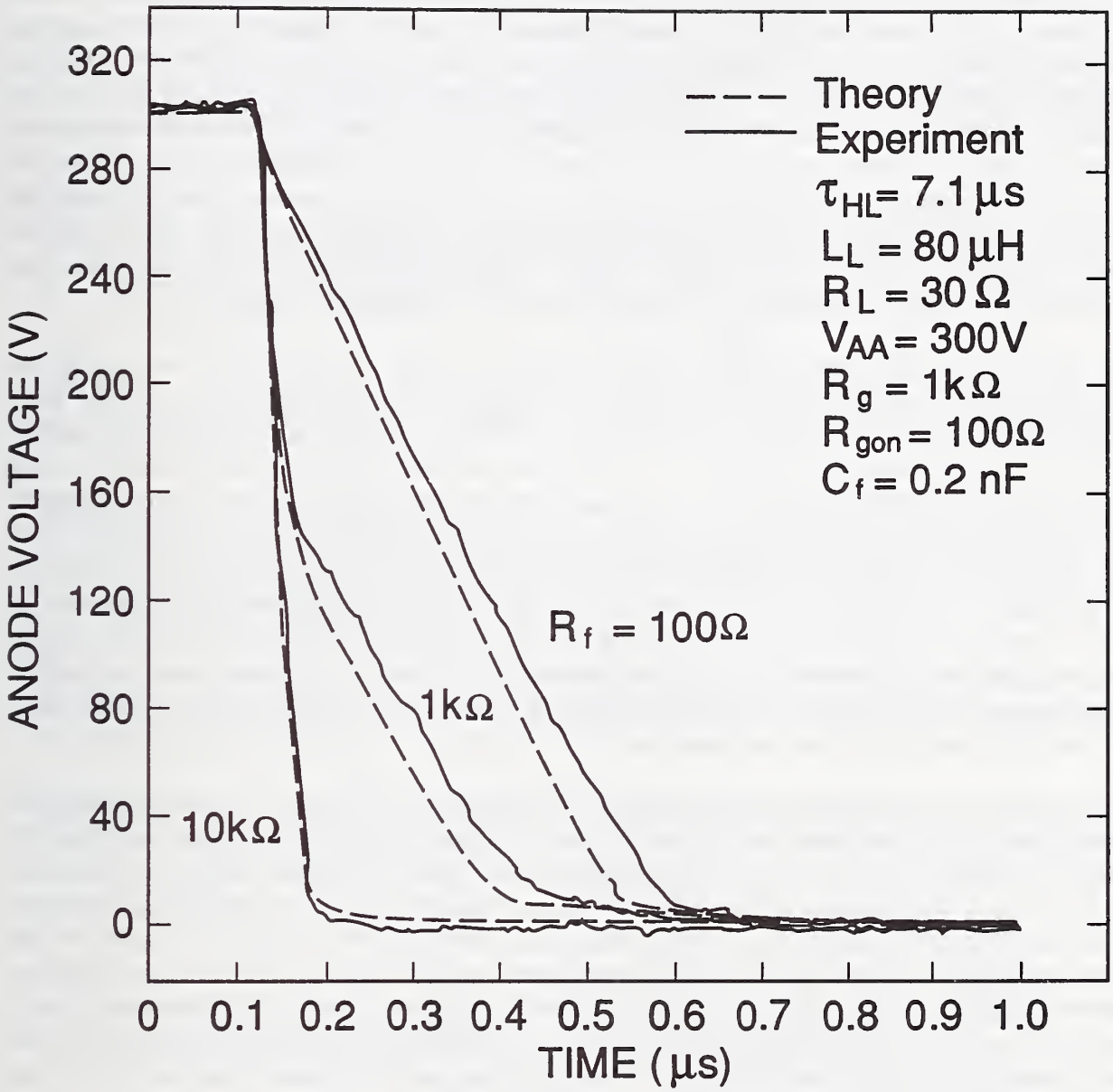


Figure 50. Comparison of the measured and simulated, anode voltage turn-on waveforms for the circuit of figure 8 with different values of series feedback resistances.

simplified schematic representation of the IGBTs and the external circuit.

A general overview of the operation and use of the INSTANT software package has been given, and the INSTANT source code has been described. The INSTANT software package is designed to provide the flexibility to change the external circuit configuration and model equations. The device and circuit parameters are also readily accessible, and the graphics output provides a real-time display of the waveforms as they are calculated. INSTANT is written in generally portable FORTRAN code and is available with graphics libraries for various PC, VAX, and Sun FORTRAN compilers and graphics Windows environments. The INSTANT software package contains the complete software source code, a graphics library for the specified FORTRAN compiler, and executable programs for several example circuits. The INSTANT software package also contains the document file that describes each of the files in the software package, the variable names used in the source code, and the procedure used to generate executable programs for different circuits.

The automated measurement methods developed to extract the IGBT device model parameters from terminal electrical measurements have also been described. It has been shown that unlike parameter extraction for microelectronic devices, the dynamic characteristics must be used to characterize the IGBTs and to extract the model parameters. The dynamic characteristics must be used because the conductivity-modulated power devices such as the IGBT exhibit non-quasi-static behavior, and because the characteristics of the internal MOSFETs and bipolar transistors are convoluted in the steady-state terminal characteristics of merged power devices such as the IGBT, whereas the dynamic waveforms contain many features that isolate different model parameters. The device model parameters are obtained sequentially by selecting features of the device characteristics that isolate parameters, and using the parameters obtained from previous extraction steps to calculate the model parameters from the measured characteristics.

The unique features of the IGBT electrical characteristics have been explained using the model, and the procedures used to verify the IGBT model have been given. The effective output capacitance of the IGBT at turn-off is several orders of magnitude larger than that of the structurally equivalent power MOSFET and depends upon the device base lifetime, because the base charge at turn-off depends upon the device base lifetime. However, the gate-drain feedback capacitance is unchanged from the value for the structurally equivalent power MOSFET. Thus, the load inductance that results in excessive voltage overshoot is several orders of magnitude larger than that for the structurally equivalent power MOSFET and varies with device base lifetime. The minimum gate resistance that influences the anode voltage rate-of-rise at turn-off is also several orders of magnitude larger than that for the power MOSFET and varies with device base lifetime. However, the anode voltage rate-of-fall at turn-on is influenced by gate resistance as small as those that influence the structurally equivalent power MOSFET, because the base charge is zero at the initiation of turn-on.

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Appendix 1
Ambipolar Transport

Because the base is wide and the base doping concentration is low for the bipolar transistor of the IGBT, the concentration of injected carriers in most of the base becomes larger than the base background doping concentration at a small current density. When the excess carrier concentration is greater than the background doping concentration, the transport of electrons and the transport of holes are coupled by the electric field in the drift terms of the respective transport equations, and they cannot be treated separately. In this appendix, it is shown that the transport of electrons and holes in the base of the bipolar transistor of the IGBT must be described by ambipolar transport and cannot be described by the traditional approach of decoupling the transport equations for electrons and holes.

In general, the electron and hole currents are given by:

$$I_n = nqA\mu_n E + qAD_n \frac{\partial n}{\partial x} \qquad (A1.1)$$

$$I_p = pqA\mu_p E - qAD_p \frac{\partial p}{\partial x}. \qquad (A1.2)$$

The first terms in eqs (A1.1) and (A1.2) are due to drift, and the second terms are due to diffusion. Under the high-gain conditions of the traditional bipolar transistor analysis, these equations can be decoupled, and the transport of minority carriers in the base is described by a simple expression for both high- and low-level injection conditions. For a high-gain *pnp* transistor in low-level injection ($p \ll n$ in the base), the high-gain condition requires a negligible hole drift current, and the transport of holes is by diffusion only (second term in eq (A1.2)). For a high-gain *pnp* transistor in high-level injection, quasi-neutrality gives $n \approx p$, and the high-gain condition requires that the drift of electrons is approximately that required to cancel the electron diffusion so the electric field is obtained approximately by setting $I_n = 0$. Using this electric field and the Einstein relation, $D_{n,p} = (kT/q)\mu_{n,p}$, an expression is obtained for the hole current which resembles low-level injection diffusion except with D_p replaced by $2D_p$ [A1.1].

However, for the low-gain, high-level injection conditions of the bipolar transistor of the IGBT, the difference between the electron drift and diffusion currents is significant, and the net electron current cannot be set to zero to approximate the electric field. In this case, the net electron current has a significant effect on the hole drift current, and the electron and hole transport equations cannot be decoupled. Assuming quasi-neutrality (i.e., $\delta n = \delta p$) and a high excess carrier level (i.e., $\delta n \gg N_B$), the ambipolar electron and hole transport equations are obtained by eliminating the electric field between eqs (A1.1) and (A1.2) [A1.2,A1.3]:

$$I_n = \frac{b}{1+b} I_T + qAD \frac{\partial n}{\partial x} \qquad (A1.3)$$

$$I_p = \frac{1}{1+b} I_T - qAD \frac{\partial p}{\partial x}. \qquad (A1.4)$$

Notice that both of these expressions depend on the total current so that the transport of electrons and holes are coupled. For negligible electron current (high-gain case), the total current is approximately equal to the hole current, and eq (A1.4) reduces to the traditional high-gain, high-injection model described above.

The hole and electron continuity equations are given by:

$$\frac{\partial \delta p}{\partial t} = -\frac{\delta p}{\tau_{HL}} - \frac{1}{qA}\frac{\partial I_p}{\partial x} \qquad (A1.5)$$

$$\frac{\partial \delta n}{\partial t} = -\frac{\delta n}{\tau_{HL}} + \frac{1}{qA}\frac{\partial I_n}{\partial x}. \qquad (A1.6)$$

From eqs (A1.5) and (A1.4), the time-dependent ambipolar diffusion equation is obtained:

$$\frac{\partial^2 \delta p}{\partial x^2} = \frac{\delta p}{L^2} + \frac{1}{D}\frac{\partial \delta p}{\partial t}. \qquad (A1.7)$$

A requirement in deriving this expression is that the total current (I_T) is independent of position in the base. This is satisfied in the IGBT because the base current (electrons) flows from the collector through the base in the same direction as the injected hole current. Equation (A1.7) does not hold for the traditional bipolar transistor for which the base current enters from the side in the middle of the base.

To determine the distribution of excess carriers in the base of the bipolar transistor of the IGBT, eq (A1.7) is solved for the boundary conditions and initial condition of the bipolar transistor. This distribution is then used in eqs (A1.3) and (A1.4) to express the electron and hole currents in terms of the total current and the carrier concentration. The boundary condition for the excess carrier concentration at the emitter edge of the quasi-neutral base ($x = 0$) is

$$\delta p(x = 0) \equiv P_0, \qquad (A1.8a)$$

where P_0 is used as a parameter for the development of the model, and at the collector edge of the quasi-neutral base ($x = W$), the boundary condition is

$$\delta p(x = W) = 0 \qquad (A1.8b)$$

because the collector-base junction is reverse biased for forward operation of the IGBT (anode positive).

The component of bipolar transistor base current that is injected into the emitter is determined by the boundary condition for the electron current at the emitter-base junction ($I_n(x = 0)$). The electron current injected into the emitter is given in terms of P_0 by:

$$I_n(0) = \frac{\delta n_{e0} N_E}{n_{ie}^2} I_{sne} = \frac{P_0^2}{n_i^2} I_{sne}, \qquad (A1.9)$$

where δn_{e0} is the excess electron concentration at the emitter edge of the emitter-base junction, N_E is the doping concentration in the emitter, and n_{ie} is the intrinsic carrier concentration in the emitter. The first equality represents a solution to the low-level injection semiconductor transport and conductivity equations in the emitter where I_{sne} is the measured emitter electron saturation current which accounts for the emitter parameters (similar to the emitter Gummel number). The second equality is obtained using the quasi-equilibrium simplification for the high-level injection condition to relate the excess carrier concentrations on both sides of the emitter-base junction.

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Appendix 2
Transient Bipolar Collector Current

The analysis of the bipolar transistor portion of the IGBT is described using the coordinate system defined in figure 4 and the symbols defined in the nomenclature. The collector-base junction of the bipolar transistor of the IGBT is reverse biased for forward conduction, and the depletion region of the collector-base junction extends into the base. The collector-base junction depletion width is given by

$$W_{bcj} = \sqrt{\frac{2\epsilon_{si}(V_{bc} + V_{bi})}{qN_{scl}}}, \qquad (A2.1)$$

and the width of the quasi-neutral base is given by

$$W = W_B - W_{bcj}. \qquad (A2.2)$$

Because of the IGBT structure (fig. 1), the bipolar transistor base current (electrons) supplied by the MOSFET is introduced at the collector end of the base. In the model, the region of the device at the epitaxial layer edge of the reverse-biased epitaxial layer-body junction ($x = W$) is designated as the contact between the bipolar transistor base and the MOSFET drain. The electron current that enters this region $I_n(W)$ is the bipolar transistor base current which is supplied by the MOSFET drain, and the hole current there $I_p(W)$ is the collector current of the bipolar transistor (see fig. 2).

For the voltage transitions of typical IGBT transient operation, the quasi-neutral base width (W of eq (A2.2)) changes in a time on the order of the base transit time, and the solution to eq (A1.7) must account for the moving boundary condition. From eq (A2.1), the time rate-of-change of quasi-neutral base width is given in terms of the time rate-of-change of collector-base voltage by:

$$\frac{dW}{dt} = \frac{-C_{bcj}}{qN_{scl}A} \cdot \frac{dV_{bc}}{dt}, \qquad (A2.3)$$

where $C_{bcj} \equiv A\epsilon_{si}/W_{bcj}$ is the collector-base depletion capacitance. This moving quasi-neutral base width boundary condition results in an additional component of non-quasi-static collector current. This component of current is larger than the displacement current through the collector-base junction depletion-capacitance for the high-level injection condition, and is a significant component of the total collector current for the low-gain condition. This non-quasi-static effect is unimportant, though, for the low-level injection or high-gain conditions of "signal" transistors.

It is assumed in the quasi-static approach that the collector current, during the transient, is determined exclusively by the instantaneous base charge and terminal voltages using the steady-state relationships. However, for the bipolar transistor of the IGBT, the collector current during the transient also depends upon 1) the instantaneous total current, because the transport of electrons and holes are coupled, and 2) the time rate-of-change of the quasi-neutral base width because it changes faster than the base transit speed. In the

following analysis, expressions are presented for the non-quasi-static transient excess carrier distribution and collector current.

Because the quasi-neutral base width changes with the changing collector-base voltage, eq (A2.3), the excess carrier base charge Q is swept into a quasi-neutral base that becomes narrower as the voltage is increased. This is illustrated in figure A2.1 for a simplified excess carrier distribution where the change in local excess carrier concentration Δp that results throughout the base for a change in base width ΔW is indicated. For comparison, figure A2.2 shows the change in local excess carrier concentration that results for a change in total base charge ΔQ which is important for high-speed operation of "signal" transistors [A2.1, pp. 222]. It is clear from figure A2.1 that the time rate-of-change of local excess carrier concentration $\partial \delta p / \partial t$ depends upon the quasi-neutral base width boundary velocity $\mathrm{d}W/\mathrm{d}t$. Therefore, because $\partial \delta p / \partial t$ appears in the second term on the right-hand side of eq (A1.7), a curvature in the carrier distribution given by the left-hand side of eq (A1.7) is required to bring about the redistribution of carriers for the moving boundary condition.

Thus, in general, eq (A1.7) must be solved for the conditions of a moving boundary to describe the non-quasi-static transient carrier distribution and collector current. A first-order solution to eq (A1.7) for the moving quasi-neutral base width boundary condition is given by [1]:

$$\delta p(x) = P_0 \left[1 - \frac{x}{W}\right] - \frac{P_0}{WD}\left[\frac{x^2}{2} - \frac{Wx}{6} - \frac{x^3}{3W}\right] \cdot \frac{\mathrm{d}W}{\mathrm{d}t}. \qquad (A2.4)$$

This carrier distribution is shown in figure A2.3 and consists of a linear component (first term) and a moving boundary redistribution component (second term). For a constant anode voltage, only the first term on the right-hand side of eq (A2.4) remains. The second term provides the curvature in the carrier distribution necessary to redistribute the excess carriers for a given quasi-neutral base width boundary velocity $\mathrm{d}W/\mathrm{d}t$.

By integrating eq (A2.4) through the base, the total base charge is given in terms of P_0 for the transient conditions by:

$$Q = \frac{qP_0AW}{2}. \qquad (A2.5)$$

The non-quasi-static transient collector current is then obtained by evaluating eq (A1.4) at $x = W$ using the non-quasi-static carrier distribution of eq (A2.4):

$$I_p(W) = \left(\frac{1}{1+b}\right) I_T + \frac{2D}{W^2}Q - \frac{Q}{3W} \cdot \frac{\mathrm{d}W}{\mathrm{d}t}, \qquad (A2.6)$$

where the Einstein relations, $D_{n,p} = (kT/q)\mu_{n,p}$, and the expressions for b and D in the nomenclature have been used. The first term on the right-hand side of eq (A2.6) is a non-quasi-static term that shows the explicit dependence of the collector current upon the instantaneous total current due to the coupling between the transport of electrons and holes. The second term is a charge-control component of current (I_{CC}) because it is directly related to the charge that remains in the base and to the applied collector-base

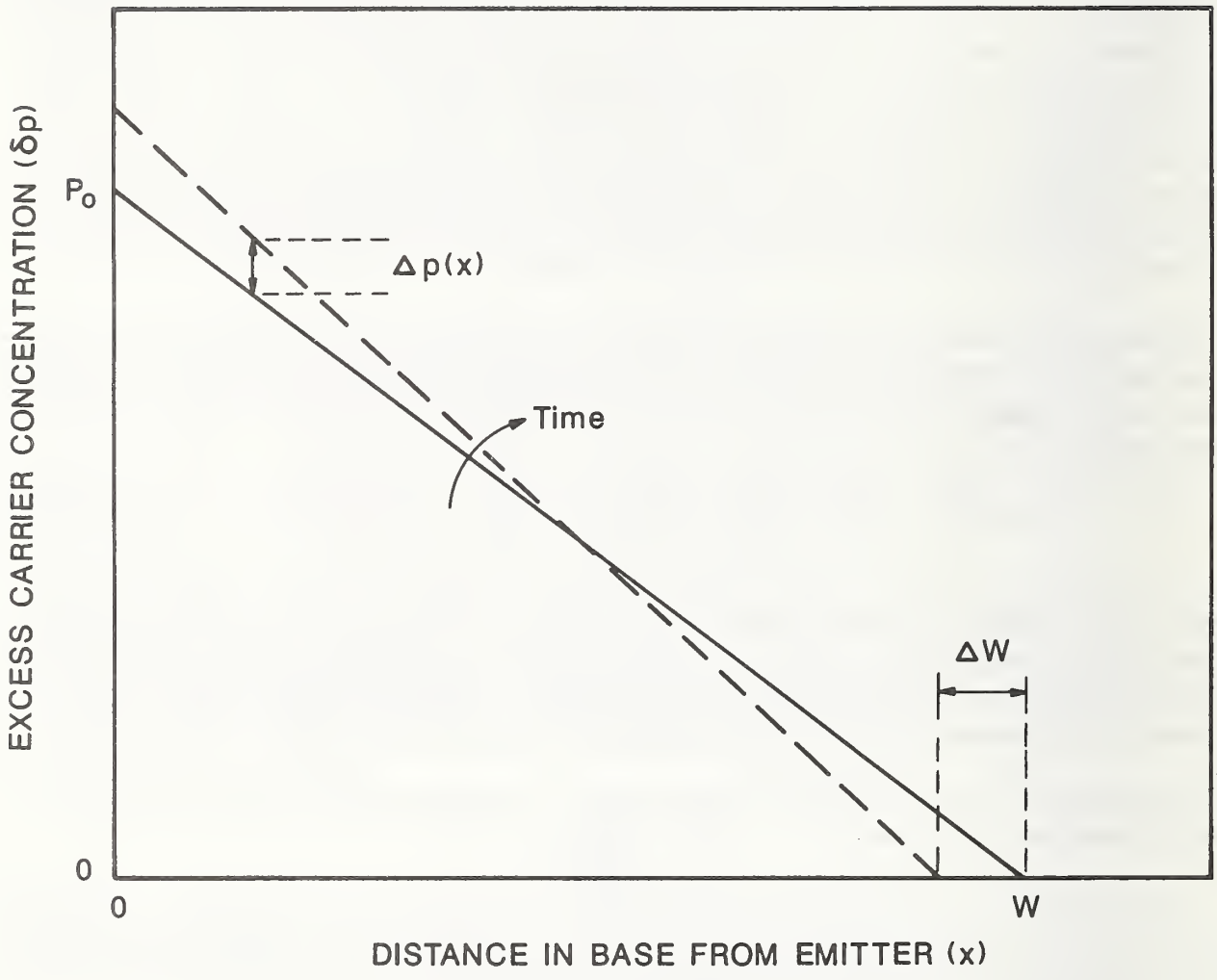

Figure A2.1. A simplified excess carrier distribution in the base indicating the change in local excess carrier concentration with time due to the moving quasi-neutral base width boundary.

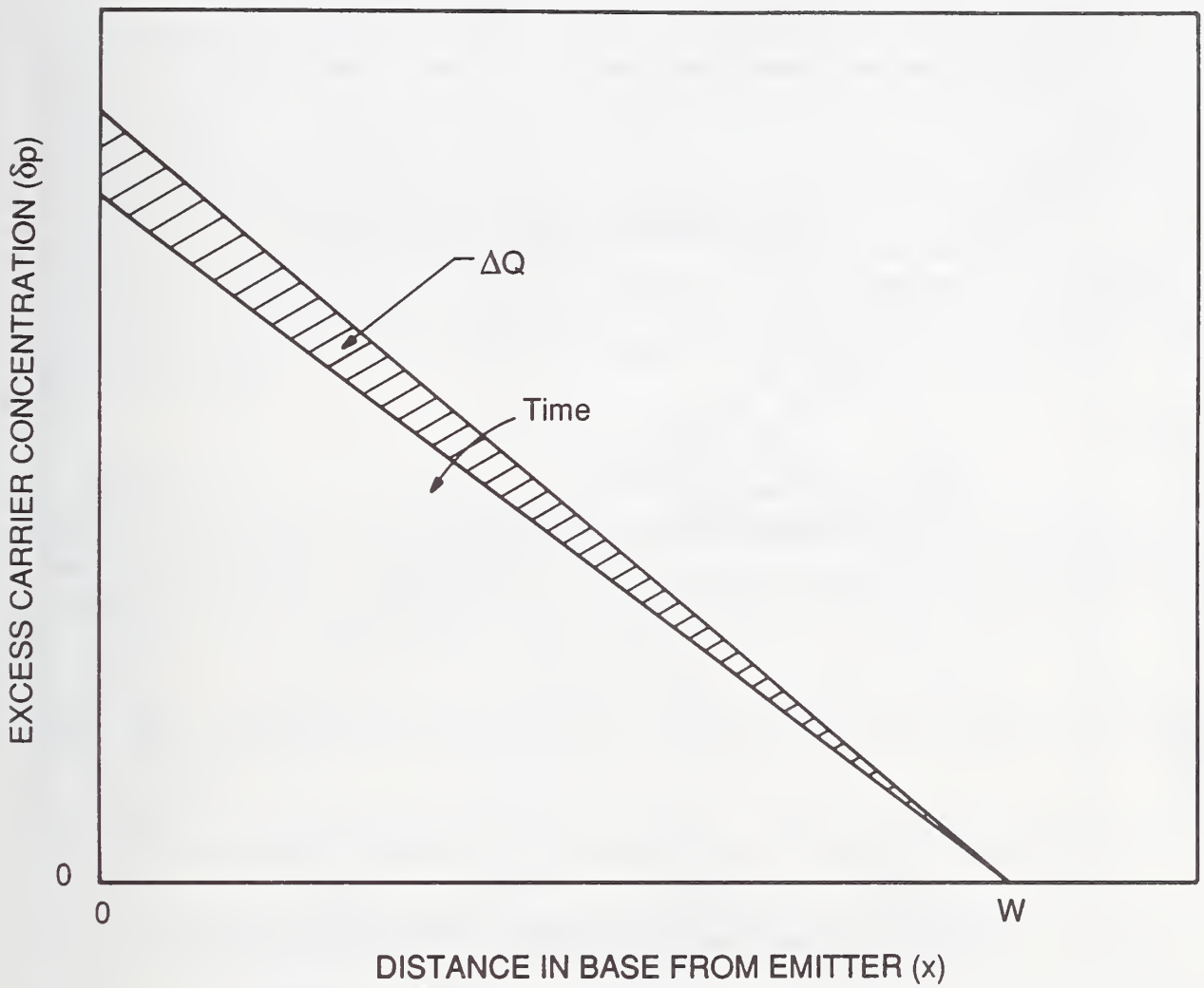

Figure A2.2. A simplified excess carrier distribution in the base indicating the change in local excess carrier concentration due to a change in total base charge.

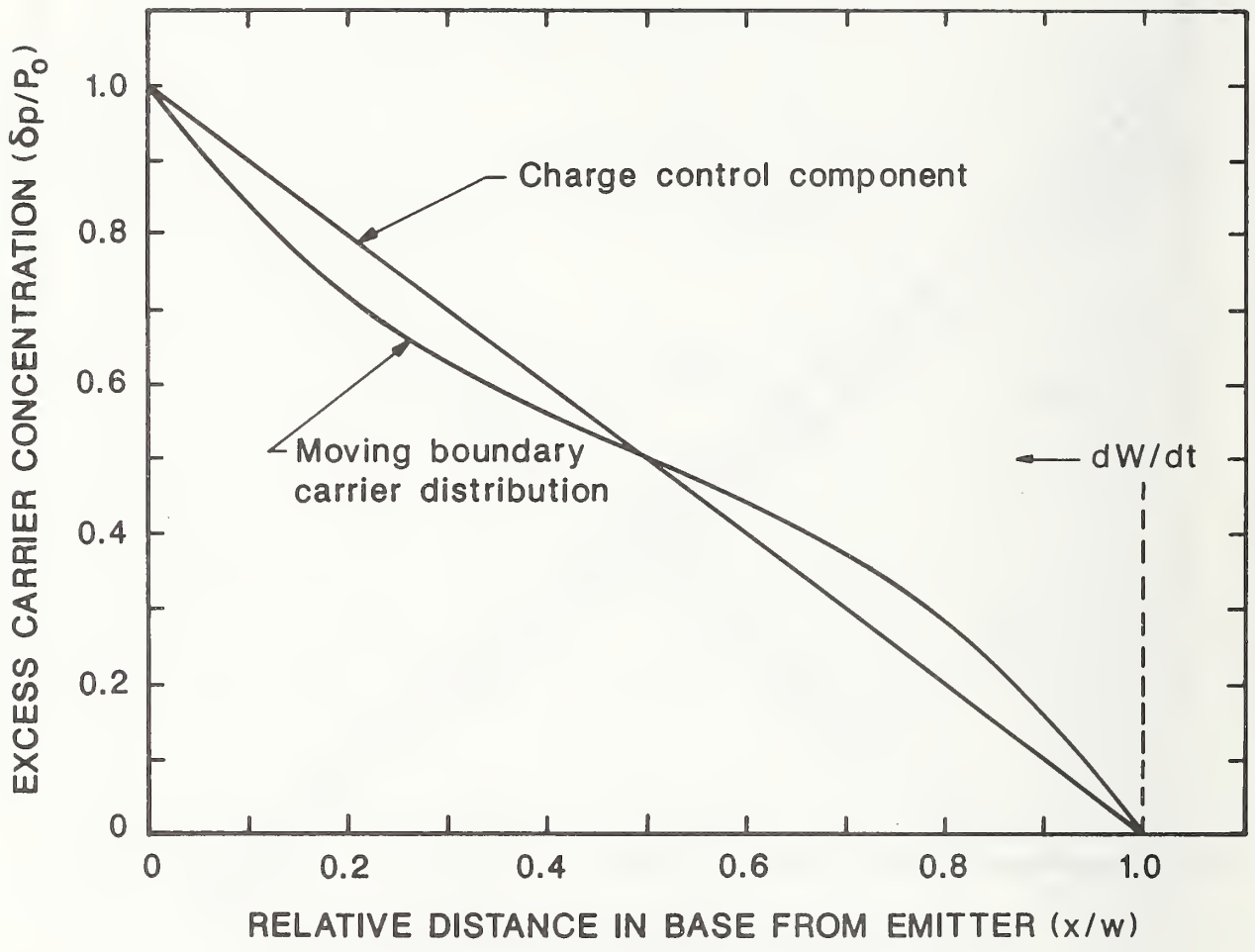

Figure A2.3. The excess carrier distribution in the base for a given quasi-neutral base width boundary velocity.

voltage using eqs (A2.1) and (A2.2). The third term is necessary to bring about the redistribution of carriers for the moving quasi-neutral base width boundary condition. This moving boundary redistribution component of current (I_R) is a non-quasi-static component because it depends upon the time rate-of-change of base width in addition to the instantaneous value of base width.

The non-quasi-static expression for collector current, eq (A2.6), differs substantially from the traditional quasi-static models, in that it depends upon 1) the instantaneous total current and 2) the time rate-of-change of the quasi-neutral base width. The explicit dependence upon the total current is important for the low-gain condition where the base current $I_n(W)$ is a significant component of the total current I_T, so that the collector current $I_p(W)$ is significantly affected by changes in instantaneous base current. Otherwise, for a high-gain condition, the total current is approximately equal to the collector current, and the first term can be combined with the left-hand side of eq (A2.6), resulting in the usual expression for the high-gain, high-level injection charge control component of collector current ($I_p(W) = 4D_pQ/W^2$). The physical significance of the redistribution component of current is ascertained by dividing the third term of eq (A2.6), I_R, by the second term, I_{CC}:

$$\frac{I_R}{I_{CC}} = \left(\frac{1+\frac{1}{b}}{3}\right) \cdot \frac{\tau_b}{W} \cdot \frac{\mathrm{d}W}{\mathrm{d}t}, \qquad (A2.7)$$

where $\tau_b \equiv W^2/4D_p$ is the high-gain, high-level injection base transit time. This indicates that the redistribution component of current becomes comparable to the charge control component when the base width changes as fast as the base transit speed W/τ_b .

References

[A2.1] Grove, A. S., Physics and Technology of Semiconductor Devices (Wiley, New York, 1967).

Appendix 3
Bipolar Emitter–Base Voltage

The base contact of the bipolar transistor of the IGBT is defined to be at the collector edge of the neutral base $x = W$, where the MOSFET channel current supplies electrons to the base (see fig. 2). Figure A3.1 shows the band diagram including quasi-fermi potentials from the emitter to base contacts. Because the excess carrier concentration is zero at the collector edge of the neutral base $x = W$ and at the emitter contact, the electron quasi-fermi potential coincides with its charge-neutral, thermal-equilibrium value relative to the electrostatic potential at both the emitter and base contacts. Thus, the applied emitter-base voltage is equal to the electron quasi-fermi potential difference between the emitter and base contacts:

$$V_{eb} = (\phi_{pej} - \phi_{nej}) + (\phi_{nej} - \phi_{nb}), \qquad (A3.1)$$

where $(\phi_{pej} - \phi_{nej})$ is the electron quasi-fermi potential drop in the emitter (the hole quasi-fermi potential is constant in the heavily doped emitter and coincides with the electron quasi-fermi potential at the emitter contact) and $(\phi_{nej} - \phi_{nb})$ is the electron quasi-fermi potential drop across the quasi-neutral base.

Because the hole quasi-fermi potential is constant in the heavily doped emitter (i.e., the ohmic drop is negligible), the electron quasi-fermi potential drop in the emitter is equal to the difference between the electron and hole quasi-fermi potentials at the emitter-base junction. Using the quasi-equilibrium simplification [A1.2, pp. 184] (i.e., the difference between the electron and hole quasi-fermi potentials is the same on both sides of the forward biased emitter-base junction), this difference is given in terms of the excess carrier concentration at the emitter edge of the neutral base P_0 by

$$(\phi_{pej} - \phi_{nej}) = \frac{kT}{q} \ln \left[\left(\frac{P_0}{n_i^2} + \frac{1}{N_B} \right) \left(N_B + P_0 \right) \right] \qquad (A3.2)$$

from the definition of the electron and hole quasi-fermi potentials [A3.1].

The electron quasi-fermi potential drop across the conductivity-modulated base is a result of both drift and diffusion. In general, the electron quasi-fermi potential gradient is related to the electron current and the electron concentration by [A3.1,A3.2]:

$$\frac{\mathrm{d}\phi_n(x)}{\mathrm{d}x} = -\frac{I_n(x)}{qA\mu_n n(x)}. \qquad (A3.3)$$

The electron quasi-fermi potential drop across the quasi-neutral base is determined by integrating this equation between the emitter and the collector edges of the quasi-neutral base, $x = 0$ and $x = W$, respectively. In doing this, the electron current $I_n(x)$ is given by eq (A1.1), and the carrier concentration is given by $n(x) = N_B + \delta p(x)$, where $\delta p(x)$ is the excess carrier distribution in the base. The result of the integration of eq (A3.3) has the form:

$$\phi_{nej} - \phi_{nb} = \frac{I_T W}{(1 + \frac{1}{b})\mu_n A q n_{eff}} - \frac{D}{\mu_n} \ln \frac{P_0 + N_B}{N_B} \qquad (A3.4)$$

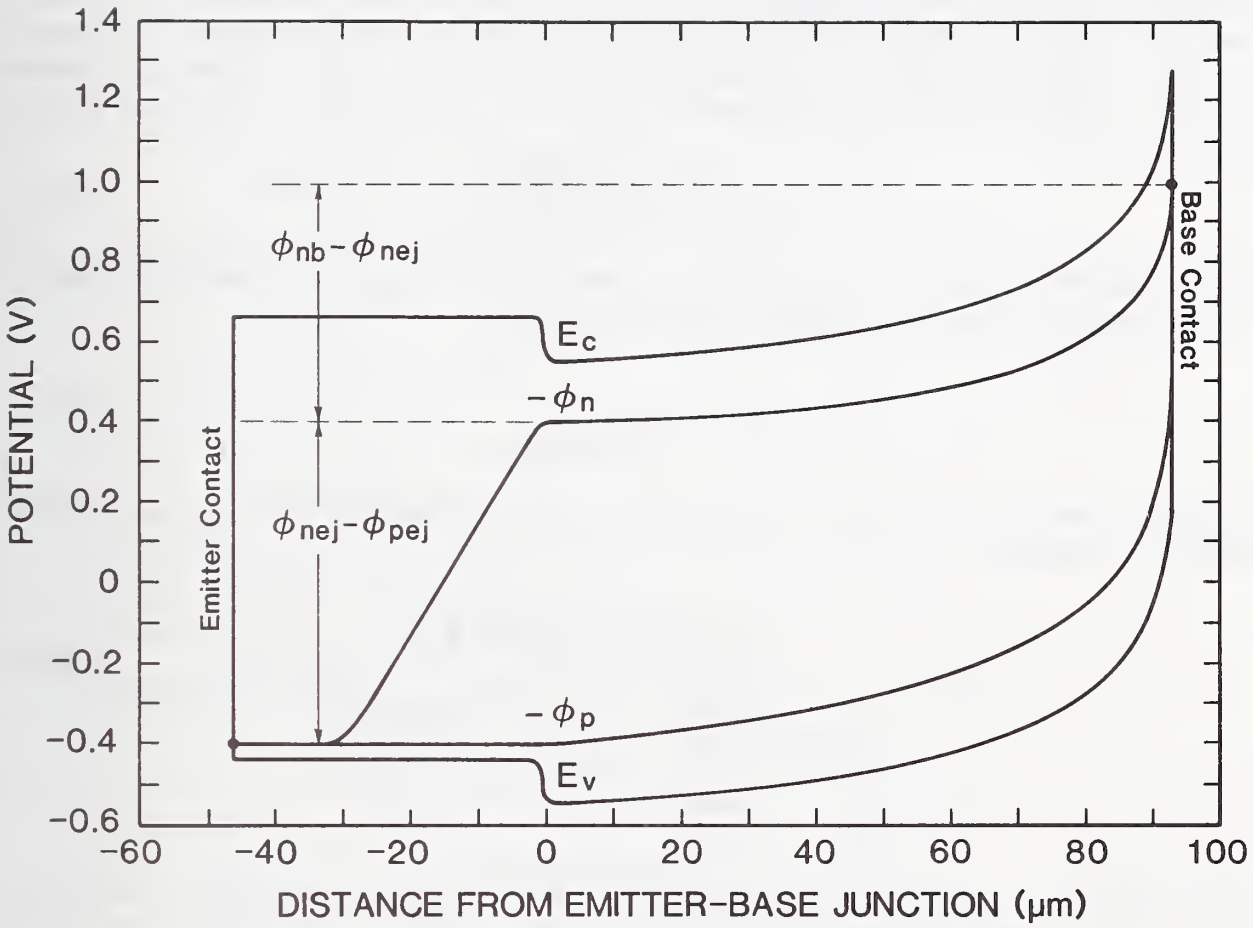

Figure A3.1. The band diagram from the emitter to base contacts for an IGBT with the physical parameters listed in tables 4 and 5, and a base lifetime of $\tau_B = 1$ μs, indicating the electron quasi-fermi potential drops in the emitter ($\phi_{nej} - \phi_{pej}$) and across the base ($\phi_{nb} - \phi_{nej}$).

where

$$\frac{1}{n_{eff}} \equiv \frac{1}{W}\int_0^W \frac{\mathrm{d}x}{N_B + \delta p(x)} \qquad (A3.5)$$

accounts for the conductivity-modulation in the base of the bipolar transistor and for the nonuniformity of the excess carrier distribution.

Because the emitter-base voltage is most important for on-state conditions, the steady-state shape of the carrier distribution for the instantaneous charge is used to integrate eq (A3.5). This distribution is obtained by solving the steady-state diffusion equation (eq (A1.7) with $\partial\delta p/\partial t$) for the boundary conditions of eq (A1.8). The excess carrier distribution is

$$\delta p(x) = P_0 \frac{\sinh(\frac{W-x}{L})}{\sinh(\frac{W}{L})}, \qquad (A3.6)$$

where P_0 is given in terms of the total excess carrier concentration in the base by integrating the carrier distribution of eq (A3.6) across the base:

$$P_0 = \frac{Q}{qAL\tanh\frac{W}{2L}}. \qquad (A3.7)$$

Using the carrier distribution of eq (A3.6) in the integral of eq (A3.5), n_{eff} has the analytical solution:

$$n_{eff} \equiv \frac{\frac{W}{2L}\sqrt{N_B^2 + P_0^2\mathrm{csch}^2(\frac{W}{L})}}{\operatorname{arctanh}\left[\dfrac{\sqrt{N_B^2 + P_0^2\mathrm{csch}^2(\frac{W}{L})}\,\tanh(\frac{W}{2L})}{N_B + P_0\mathrm{csch}(\frac{W}{L})\tanh(\frac{W}{2L})}\right]}. \qquad (A3.8)$$

For $P_0\mathrm{csch}(\frac{W}{L}) \ll N_B$, $n_{eff} \approx N_B$ and the first term in eq (A3.4) reduces to the resistance of the unmodulated epitaxial base times the current; and for $P_0\mathrm{csch}(\frac{W}{L}) \gg N_B$, the quantity n_{eff} increases approximately as $P_0/\ln(\frac{P_0}{N_B}\mathrm{csch}(\frac{W}{L}))$. Thus, the first term in eq (A3.4) describes the conductivity modulation of the epitaxial layer. The second term of eq (A3.4) is due to the majority carrier concentration difference between the emitter and collector edges of the quasi-neutral base and is zero for low-level injection. The first and second terms of eq (A3.4) cancel in a high-gain narrow base transistor, but the second term is always less than the first for the wide-base transistor.

References

[A3.1] Sze, S. M., Physics of Semiconductor Devices (Wiley, New Jersey, 1981), pp. 85.

[A3.2] Shockley, W., Electrons and Holes in Semiconductors (D. Van Nostrand, New York, 1956), pp. 302-308.

Appendix 4
INSTANT Document File

****

Software Documentation for the IGBT Circuit Simulation Software

I N S T A N T

IGBT Network Simulation and Transient ANalysis Tool.

Version 1.0
August 1991

by
Allen R. Hefner
National Institute of Standards and Technology
(301) 975-2071

****

CONTENTS

****

1) Introduction

The enclosed disk contains the IGBT simulation software (INSTANT). The source code: INSTANT.FOR contains the IGBT model subroutines IGBTVeb and IGBTSEQ, and the numerical routines to simulate transients. The disk also contains circuit file source code for several circuit configurations and executable programs for two example circuits 1) RLLOAD for figure 5 of reference [A4.1] and 2) ACTSNUB for figure 12 of reference [A4.1].

The theoretical IGBT model in the subroutines IGBTVeb and IGBTSEQ was derived and verified for several circuit configurations and for different device and circuit parameters in references [A4.1-A4.5]. The description of the INSTANT simulation software program flow and file organization is presented in references [A4.6,A4.7]. The purpose of this document is to orient the user with the software and to provide a description of the IGBT model routines.

****

2) Directory of the INSTANT Software Disk

The enclosed floppy disk contains the following files:

INSTANT.DOC	----	This document.
INSTANT.FOR	----	Source code for the IGBT circuit simulation software. This includes the main program that calls subroutines INPUT, OUTPUT, and RKF45, and the IGBT model subroutines IGBTVeb and IGBTSEQ.
INSTANT.OBJ	----	Object code compiled with the specific FORTRAN compiler.
LINKCIRC.BAT	----	Command file that compiles the circuit file source code and links it with the INSTANT object code to create the executable circuit simulation programs.
RGRAPH.LIB	----	Graphics library for specified FORTRAN compiler.
RLLOAD.FOR	----	Example circuit file source code for an IGBT with a series resistor-inductor load and a resistive gate drive (fig. 5 of reference [A4.1]).
RLLOAD.EXE	----	Executable circuit simulation program for the IGBT with a series resistor-inductor load and a resistive gate drive. This program was created from RLLOD.FOR using LINKCIRC.BAT.
RLLOAD.INP	----	Circuit parameter input file for RLLOAD.EXE. The circuit parameters can be changed by editing this file or by creating different input files without recompiling RLLOAD.FOR.
ACTSNUB.FOR ACTSNUB.EXE ACTSNUB.INP	----	Additional precompiled circuit example for the series resistor-inductor load with a series resistor-capacitor feedback and a polarized gate drive resistance.
CLAMP.FOR CLAMP.INP PARALEL.FOR PARALEL.INP	----	Additional circuit file source code examples and example circuit parameter input files for the circuits of figures 7 and 9 of reference [A4.7], respectively.
APT35g60BN.IGT IRGBC20S.IGT IRGBC20U.IGT IRGBC30U.IGT IRGBC40U.IGT IRGBC50U.IGT IXHS20n60A.IGT MGM20n50.IGT MPM6002.IGT	---	Example IGBT parameter input files. The device parameters can be changed by editing or creating new IGBT input files. These files can be used for any of the circuit simulation programs because the parameters are read using the IGBTINP subroutine provided in INSTANT.

T7.IGT
T7KP6.IGT
T2P5.IGT
TP3.IGT

****

3) Execution of Precompiled Examples

The disk contains two precompiled example circuit simulation programs: 1) RLLOAD for figure 5 in reference [A4.1] and 2) ACTSNUB for figure 12 in reference [A4.1]. When these programs are executed, they will ask for the device parameter input file, the circuit parameter input file, and the output file names. Example circuit parameter input files for the two programs are in the files RLLOAD.INP and ACTSNUB.INP, respectively. The disk also contains several example device parameter input files.

Upon execution of the example programs and entry of the input and output file names, the program will begin to simulate the transient. The gate current, gate voltage, anode current, and anode voltage waveforms will appear on the graphics computer screen as each time step is computed. When the waveforms reach the final time step, the graph of the waveforms remains on the screen as the program awaits further input from the user. At this point, the entry of a "P" will generate a Postscript file containing the graphics output, or the entry of a "D" will dump the graph to a graphics compatible dot matrix printer. Upon termination, the output file will contain the output quantities computed at each time step in subroutine OUTPUT.

The device and circuit parameters can be changed for the two example circuit simulation programs by editing or creating new device and circuit input files. For example, the circuit input file RLLOAD.INP contains the following list of input parameters:

```
30.0          RL      --- load resistance
80.e-6        LL      --- load inductance
300.0         Vaa     --- anode supply voltage
1000.0        RG      --- gate resistance
20.0          Vgon    --- gate pulse generator amplitude
1.0e-6        ton     --- time when gate pulse generator turns on
20.0e-6       toff    --- time when gate pulse generator turns off
0.1e-6        trise   --- rise/fall time of the pulse generator
30.0e-6       tfinal  --- final time step for the simulation
0.0e-6        tplot   --- starting time for the plot window
```

The first five (5) parameters are component values, the next three (3) parameters define the timing of the pulse generator, and the last two (2) parameters define the plot window and output time step resolution. For a description of the device parameters in the IGBT input files T7.IGT, T2p5.inp, etc., see section 5) below on Description of IGBT Model Routines.

****

4) Creating Your Own Circuit Files

You can change the input parameters without recompiling the program, but to change the external circuit, you must create a new FORTRAN circuit file similar to RLLOAD.FOR and ACTSNUB.FOR called, for example, CIRCUIT.FOR.

You then compile and link it with INSTANT using the command file LINKCIRC.BAT. For example, the command:

```
C:> LINKCIRC CIRCUIT
```

creates an executable program called CIRCUIT.EXE from the FORTRAN circuit file called CIRCUIT.FOR. The INSTANT.OBJ and RGRAPH.LIB on this disk are for a given FORTRAN compiler and Windows environment. You must also specify the paths to the FORTRAN and Windows libraries on your machine within LINKCIRC.BAT when first installed.

The FORTRAN circuit file CIRCUIT.FOR contains the circuit equations, the circuit parameter input read statements, the initial conditions of the device and circuit state variables, the graphics commands, and the program control tests. Essentially, the three routines within CIRCUIT.FOR: subroutine STATEQ, subroutine INPUT, and subroutine OUTPUT describe the entire circuit simulation using the subroutines within INSTANT.

To describe the operation of IGBTs within different circuits, the circuit state equations are combined with the IGBT state equations within the "Device and Circuit State Equations" segment of subroutine STATEQ. The IGBT state equations are evaluated using subroutine IGBTSEQ provided within INSTANT. This routine requires the input of the instantaneous gate and anode currents as well as the instantaneous values of the IGBT state variables. Thus, the anode and gate currents must be expressed in terms of the instantaneous values of the device and circuit state variables before subroutine IGBTSEQ is called. Likewise, the IGBT anode voltage must be expressed in terms of the instantaneous values of the state variables before the external load circuit state equations can be evaluated.

A general procedure is given in reference [A4.7] for expressing the IGBT anode voltage, anode current, and gate current in terms of the instantaneous values of the device and circuit state variables using Kirchhoff's voltage and current laws. These expressions are implemented into the "Functions of State Variables" segment of subroutine STATEQ, by first calling subroutine IGBTVeb to calculate the base resistance Rb and the emitter-base capacitor voltage Vebq in terms of the instantaneous values of the IGBT state variables. The expressions for the anode voltage Va=It*Rb+Vebq+Vcb, anode current, and gate current are then evaluated. The "Functions of State Variables" segment may also be included in subroutine OUTPUT to calculate output and plot quantities at each output time step.

Next, the parameters for the circuit equations that are to be read from the parameter file CIRCUIT.INP must be included in the labeled common statement: COMMON /CIRCpar/. This common statement should be included in the STATEQ, INPUT, and OUTPUT. The circuit parameter read statements are then entered into the respective segment of subroutine INPUT. The IGBT model parameters in the file DEVICE.IGT are read using subroutine IGBTINP provided within INSTANT, so the device parameter common statement, COMMON /IGBTpar/, need not be included in the CIRCUIT.FOR file. If multiple IGBTs with different model parameter sets are to be included in the circuit, subroutine IGBTSTO can be used to store the model parameters from the IGBTpar common block into an IGBT model parameter array, and subroutine IGBTREC can then be used to recall the parameters back into the IGBTpar common block before calling the IGBT model routines for each device.

Finally, the device and circuit state variable initial conditions are defined within subroutine INPUT at a known state, e.g., the off-state before the devices are switched on. All of the circuit and device

variables should be declared as to their variable type in each subroutine. The state variables and the time rate-of-change of the state variables are passed to and from the main program through the parameter list via Y and YP, so the names used for each of the state variables must be defined in terms of the array Y at the beginning of each subroutine, and the array YP must be defined in terms of the variables that represent the evaluated state equations at the end of subroutine STATEQ.

****

5) Description of IGBT Model Routines

The IGBT model within INSTANT is invoked by calling subroutine IGBTVeb and subroutine IGBTSEQ. The IGBT model parameters are passed to the IGBT model routines via the labeled common statement:

```
      COMMON /IGBTpar/ t,wb,nb,A,isne,Vt,Kpsat,Kplin,Rs,theta,
     &                 Cgs,Agd,Coxd,Vtd,BVn,BVf,
     &                 ccsflg,sclflg,vpsat,vnsat,
     &                 Un,Up,Ut,epsi,ni,q
```

Therefore, the model parameter values for the IGBT being modeled must be in the common block when the IGBT model routines IGBTVeb and IGBTSEQ are invoked. This common block does not need to be included in the circuit file source code, because subroutine IGBTINP reads the IGBT model parameters from the IGBT model parameter input file, and assigns the values to the common block variables. However, if multiple IGBTs with different parameter values are used, subroutine IGBTSTO can be used to store the parameters in a variable array for each IGBT after the model parameters are read by IGBTINP. Then the model parameters can be recalled to the common block using subroutine IGBTREC just before the IGBT model subroutines IGBTSEQ and IGBTVeb are called. Hence, the circuit file source code only needs to define a single variable array for each IGBT model parameter set.

5a) Subroutine IGBTINP

The first eighteen (18) parameters in the /IGBTpar/ common block are read from the device input file by IGBTINP and the remaining eight (8) physical constants of silicon are designated within subroutine IGBTINP. Several example IGBT model parameter input files are given on the INSTANT disk. For example, the File T7.IGT contains the following input:

```
  7.1e-6      t_HL     (s)              --- base high-level lifetime
  0.0093      W_B      (cm)             --- metallurgical base width
  2.0e4       N_B      (cm**-3 * E10)   --- base doping concentration
  0.1         A        (cm**2)          --- device active area
  6.5e-14     Isne     (A)              --- emitter electron saturation current
  4.7         Vt       (V)              --- MOSFET channel threshold
  0.38        Kpsat    (A/V**2)         --- MOSFET saturation transconductance
  0.7         Kplin    (A/V**2)         --- MOSFET linear transconductance
  0.02        Rs       (Ohm)            --- series anode resistance
  0.01        theta    (1/V)            --- transverse field mobility reduction
  0.62e-9     Cgs      (F)              --- gate-source capacitance
  0.05        Agd      (cm**2)          --- gate-drain overlap area
  1.75e-9     Coxd     (F)              --- gate-drain oxide capacitance
  0.0         Vtd      (V)              --- gate-drain depletion threshold
```

```
  4.0        BVn                    --- avalanche multiplication exponent
  0.9        BVf                    --- junction curvature factor
 -1.0        ccsflg  (+/-)          --- carrier-carrier scattering flag
 -1.0        sclflg  (+/-)          --- velocity saturation flag
```

which correspond to the first eighteen (18) device parameters in the common block /IGBTpar/. The remaining eight (8) physical constants of silicon are designated within IGBTINP as:

```
      Ut = 0.0259             --- thermal potential
      ni = 1.45               --- intrinsic carrier concentration
      Un = 1500.0             --- electron mobility
      Up = 450.0              --- hole mobility
      q = 1.6E-9              --- electronic charge
      epsi=8.854e-14*11.9     --- dielectric constant of silicon
      vpsat=0.95e7            --- hole saturation velocity
      vnsat=1.1e7             --- electron saturation velocity
```

where all of the densities are normalized to E-10 and the electronic charge is normalized to E10, to prevent overflows for single precision calculations.

5b) SUBROUTINE IGBTSEQ

The subroutine IGBTSEQ evaluates the IGBT state equations using the instantaneous values of the IGBT state variables and the gate and anode current and returns the values of the time rate-of-change of the state variables. This function is invoked by the command:

```
CALL IGBTSEQ(Vgs, Vcb, Qte6, Ig, It, DVgs, DVcb, DQte6)
```

where the parameter list is defined as follows:

```
Vgs     --- IGBT gate-source voltage
Vcb     --- IGBT collector-base voltage
Qte6    --- IGBT base charge * 1.0E6
Ig      --- IGBT gate current
It      --- IGBT anode current
DVgs    --- time rate-of-change of Vgs
DVcb    --- time rate-of-change of Vcb
DQte6   --- time rate-of-change of Qte6
```

The IGBT base charge is normalized to 1.0E6 so that all of the IGBT state variables will be of the same order of magnitude: Qt=Qte6*1.0e-6. The first five (5) parameters in this list are inputs from the calling routine, and the values of the remaining three (3) parameters in the list are calculated within IGBTSEQ and returned to the calling routine.

Subroutine IGBTSEQ also calculates values for the following variables which are functions of the parameter list and the IGBTpar common variables:

```
D      --- ambipolar diffusivity
b      --- ambipolar mobility ratio
W      --- quasi-neutral base width
Wcbj   --- collector-base depletion width
Wgdj   --- gate-drain overlap depletion width
Imos   --- MOSFET channel current
```

```
Ccbj   --- collector-base depletion capacitance
Cds    --- drain-source depletion capacitance
Cgd    --- gate-drain capacitance
Qb     --- background carrier charge in undepleted base
Ip     --- hole current at x=W
M      --- avalanche multiplication factor
BV     --- open emitter collector-base breakdown voltage
Igen   --- thermally generated collector-base current
gama   --- high-level injection coefficient
```

These functions are only used locally within IGBTSEQ to express the IGBT state equations. The IGBT routine also contains a few variables which are used to iterate the effective collector-base junction space charge concentration including the effect of the saturation velocity of mobile carriers:

```
ROOT    --- function that finds the root of the external
            function spachg(Nscl)
spachg  --- function that describes c-b space charge
Nscl    --- collector-base space charge density
sclmin  --- lower bound on Nscl
sclmax  --- upper bound on Nscl
TOL     --- tolerance for Nscl
sclvar  --- variables passed to the external function
            spachg through labeled common statvr
```

The iteration for the inclusion of the space charge due to saturation limited velocity in the collector-base depletion region is only carried out if sclflg is positive. Otherwise, if sclflg is negative, this effect is not included and Nscl=Nb.

5c) Subroutine IGBTVeb

The subroutine IGBTVeb evaluates the IGBT conductivity-modulated base resistance Rb and the emitter-base capacitor voltage Vebq using the instantaneous values of two of the IGBT state variables, Qte6 and Vcb, and the common IGBT model parameters. This subroutine is invoked by the command:

```
CALL IGBTVeb(Qte6, Vcb, Rb, Vebq)
```

where the parameter list is defined as follows:

```
Vcb     --- IGBT collector-base voltage
Qte6    --- IGBT base charge * 1.0E6
Rb      --- conductivity-modulated base resistance
Vebq    --- emitter-base capacitor voltage
```

The first two (2) parameters in this list are inputs from the calling routine, and the values of the remaining two parameters in the list are calculated in IGBTVeb and returned to the calling routine.

Subroutine IGBTVeb also calculates values for the following variables in addition to those for IGBTSEQ which are functions of the parameter list and the IGBTpar common variables:

```
W      --- quasi-neutral base width
Wcbj   --- collector-base depletion width
```

```
L       --- ambipolar diffusion length
P       --- carrier concentration at emitter edge of base
Pmid    --- carrier concentration in center of base
Unc     --- electron mobility including carrier-carrier
            scattering
Upc     --- hole mobility including carrier-carrier scattering
Ucinv   --- component of inverse mobility due to
            carrier-carrier scattering
wl      --- w/l
cosch   --- hyperbolic cosecant of w/l
tnh     --- hyperbolic tangent of w/l/2
cth     --- hyperbolic cotangent of w/l
Ueff    --- low-, high-level injection effective mobility
Navg    --- radical in the neff expression
x       --- used to evaluate arctnh using log identity
arctnh  --- inverse hyperbolic tangent in Neff expression
Vdep    --- emitter-base capacitance voltage for depletion
            capacitance dominant
Vdif    --- emitter-base capacitance voltage for diffusion
            capacitance dominant
Q0      --- equilibrium emitter-base junction depletion charge
neff    --- effective excess carrier concentration in base
```

These functions are only used locally within IGBTVeb to calculate the Rb and Vebq. The IGBTVeb routine also contains a few variables which are used to iterate the effective base mobility including the effect of carrier-carrier scattering for high free carrier levels:

```
ROOT    --- function that finds the root of the external
            function Dccs(D)
D       --- Ambipolar diffusivity including carrier-carrier
            scattering
Dhi     --- upper bound on Dccs
Dlo     --- lower bound on Dccs
TOL     --- tolerance for Dccs
ccsvar  --- variables passed to the external function
            Dccs through common block statvr
```

The iteration for the inclusion of carrier-carrier scattering is carried out if ccsflg is positive. Otherwise, if ccsflg is negative, this effect is not included and Unc=Un and Upc=Up.

****

6) References

[A4.1] Hefner, A. R., An Investigation of the Drive Circuit Requirements for the Power Insulated Gate Bipolar Transistor (IGBT), in Conf. Rec. IEEE Power Electronic Specialists Conf., 126-137, (1990); also in Special Issue of IEEE Trans. Power Electronics on Modeling Power Electronics Circuits and Systems PE-6, 208-219 (April 1991).

[A4.2] Hefner, A. R. and Blackburn, D. L., An Analytical Model for the Steady-State and Transient Characteristics of the Power Insulated Gate Bipolar Transistor, Solid-State Electronics 31, 1513-1532 (1988).

[A4.3] Hefner, A. R., Blackburn, D. L., and Galloway, K. F., The Effect of Neutrons on the Characteristics of the Insulated Gate Bipolar

Transistor (IGBT), IEEE Trans. Nucl. Sci. NS-33, 1428-1434 (1986).

[A4.4] Hefner, A. R., Analytical Modeling of Device-Circuit Interactions for the Power Insulated Gate Bipolar Transistor (IGBT), in Conf. Rec. IEEE Industry Applications Society Meet., 606-614 (1988); also in IEEE Trans. Industry Applications IA-26, 995-1005 (1990).

[A4.5] Hefner, A. R., An Improved Understanding for the Transient Operation of the Power Insulated Gate Bipolar Transistor (IGBT), in Conf. Rec. IEEE Power Electronics Specialists Conf., 303-313, (1989); also in IEEE Trans. Power Electronics PE-5, 459-468 (October 1990).

[A4.6] Hefner, A. R., Device Models, Circuit Simulation, and Computer Controlled Measurements for the IGBT, in Rec. of the 2nd IEEE Workshop on Computers in Power Electronics, (July 1990).

[A4.7] This paper, sections III and IV.

Appendix 5
INSTANT Main Program

```
C*****************************************************************************
C
C                              I N S T A N T
C
C         IGBT Network Simulation and Transient ANalysis Tool.
C
C                                Version 1.0
C                                August 1991
C
C                                    by
C                               Allen R. Hefner
C                 National Institute of Standards and Technology
C                               (301) 975-2071
C
C
C
C     The following code is part of the INSTANT (IGBT Network
C     Simulation and Transient ANalysis Tool) Software package.
C     The INSTANT software package is described in the INSTANT.doc
C     file and in the publication: NIST SP 400-88.
C
C
C
C *****************************************************************************
C
C
C
C
C     Program INSTANT
C
C
C     Program to integrate the device and circuit state equations
C     for external subroutine STATEQ.
C
C
      EXTERNAL STATEQ
      REAL Y(100),time,TOUT
      REAL RELERR,ABSERR,WORK(3+6*100)
      INTEGER IWORK(5), IFLAG, NEQN
C
C
C
      CALL INPUT(time,Y,NEQN,RELERR,ABSERR)
C
C
C
      IFLAG = 1
      TOUT = time
 10   continue
      CALL RKF45(STATEQ,NEQN,Y,time,TOUT,RELERR,ABSERR,IFLAG,WORK,IWORK)
      GO TO (80,20,30,40,50,60,70,80), IFLAG
 20   continue
C
C
C
```

```
      CALL OUTPUT(TOUT,Y)
      GO TO 10
C
C     Error messages from RKF45
C
   30 WRITE(99,31) RELERR,ABSERR
      GO TO 10
   40 WRITE(99,41)time
      GO TO 10
   50 ABSERR = 1.0E-9
      WRITE(99,31) RELERR,ABSERR
      GO TO 10
   60 RELERR = 10.0*RELERR
      WRITE(99,31) RELERR,ABSERR
      IFLAG = 2
      GO TO 10
   70 WRITE(99,71)time
      IFLAG = 2
      GO TO 10
   80 WRITE(99,81)
      STOP
C
   11 FORMAT(F5.1, 2F15.9)
   31 FORMAT(17H TOLERANCES RESET, 2E12.3)
   41 FORMAT(11H MANY STEPS,E12.3)
   71 FORMAT(12H MUCH OUTPUT,E12.3)
   81 FORMAT(14H IMPROPER CALL)
        end
C
C
C
C*******************************************************************************
```

Appendix 6
Subroutine IGBTSEQ

```
C*************************************************************************
C
C
C     Subroutine to evaluate the state equations for the IGBT
C
      Subroutine IGBTSEQ(Vgs,Vcb,Qte6,Ig,It,DVgs,DVcb,DQte6)
C
C *** Declare external function that evaluates collector-base
C     space charge due to velocity saturation.
C
      REAL spachg
      External spachg
C
C *** Declare common IGBT model parameters.
C
      REAL              t,wb,nb,A,isne,Vt,Kpsat,Kplin,Rs,theta,
     &                  Cgs,Agd,Coxd,Vtd,BVn,BVf,
     &                  ccsflg,sclflg,vpsat,vnsat,
     &                  Un,Up,Ut,epsi,ni,q
      COMMON /IGBTpar/ t,wb,nb,A,isne,Vt,Kpsat,Kplin,Rs,theta,
     &                  Cgs,Agd,Coxd,Vtd,BVn,BVf,
     &                  ccsflg,sclflg,vpsat,vnsat,
     &                  Un,Up,Ut,epsi,ni,q

C
C *** Declare parameter list variables and functions of model variables.
C
      REAL Vgs,Vcb,Qt,Ig,It,DVgs,DVcb,DQt,Qte6,DQte6
      REAL D,b,W,Wcbj,Wgdj,Imos,Ccbj,Cds,Cgd,Qb,Ip
      REAL gama,M,BV,Igen
C
C *** Declare common variables for space charge limited velocity routine.
C
      COMMON /Statvr/ sclvar
      REAL TOL,ROOT,Nscl,sclmin,sclmax,sclvar(5)
      Qt=Qte6*1.0e-6
      sclvar(1)=Vgs
      sclvar(2)=Vcb
      sclvar(3)=Qt
      sclvar(4)=It
      sclvar(5)=Ig
C
C *** Test flag for inclusion of effect of Scl velocity in c-b junction.
C
      If(sclflg .gt. 0.0) then
C
C ***** Call root to get the value of space charge in collector-base
C       depletion region including saturation limited velocity.
C
        nscl = Nb - spachg(Nb)
        TOL = 1.0E-4*Nb
        sclmin=min(nscl,nb)
        sclmax=max(nscl,nb)
        nscl=root(sclmin,sclmax,spachg,Tol)
```

```
C
      ELSE
        nscl=Nb
      ENDIF
C
C *** Evaluate functions of model variables:
C
C     breakdown voltage and multiplication coefficient,
C
      BV=BVf*5.34E13/(nscl*1.0E10)**(3.0/4.0)
      If(Vcb .gt. BV*0.999) then
          M=1.0/(1-0.999**BVn)
      else
         if(Vcb .lt. 0.0)  M=1.0      .
         if(Vcb .ge. 0.0)  M=1.0/(1-(Vcb/BV)**BVn)
      endif
      Igen=q/t*ni*A*sqrt(2.0*epsi*abs((Vcb)/q/Nscl))
         If (Vcb .lt. 0)Igen=0.0
C
C     depletion widths and capacitances,
C
      Wcbj=sqrt(2.0*epsi*abs((Vcb+0.6)/q/Nscl))
        if (Vcb .lt. -0.999*0.6)
     &     Wcbj=sqrt(2.0*epsi*abs(((1.0-0.999)*0.6)/q/Nscl))
      W=(Wb-Wcbj)
        if(W .lt. 0.05*Wb)W=0.05*Wb
      Ccbj=A*epsi/Wcbj
      Cds=(A-Agd)*epsi/Wcbj
      Cgd=Coxd
      If (Vcb .gt. Vgs-Vtd) then
         Wgdj=sqrt(2.0*epsi*abs((Vcb-Vgs+Vtd)/q/nscl))
         Cgd=Coxd/(1.0+Coxd/Agd/epsi*Wgdj)
      endif
C
C     diffusivity, mobility ratio, functions of charge
C
      Qb=Nscl*W*A*q
      gama=0.0
       If (Qt .gt. 0)gama=Qt/(Qt+Qb)
      D=Ut*Up
       If(Qt .ge. 0)D=Ut*Un*Up*(2*Qt+Qb)/(Un*(Qt+Qb)+Qt*Up)
      b = Un/Up
C
C     and MOSFET channel current.
C
      If(vgs .ge. Vt) then
        If (abs(Vcb) .le. (Vgs-Vt)*Kpsat/Kplin)
     &     Imos=Kplin*((Vgs-Vt)*Vcb-0.5*Kplin/Kpsat*abs(Vcb)*Vcb)
     &                /(1+theta*abs(Vgs-Vt))
        If (abs(Vcb) .gt. (Vgs-Vt)*Kpsat/Kplin)
     &     Imos=0.5*Kpsat*(Vgs-Vt)**2
     &                /(1+theta*abs(Vgs-Vt))
        If (abs(Vcb) .gt. (Vgs-Vt)*Kpsat/Kplin .and. Vcb .lt. 0.0)
     &     Imos=-Imos
       Else
        Imos=0.0
       Endif
C
C *** Evaluate the IGBT state equations.
C
```

```
      DVcb = ( It - M*(gama*It/(1+b) + 2.0*D*Qt/W**2 + Imos + Igen)
     &         + Cgd/(Cgs+Cgd)*Ig
     &       )/(  Cds + Cgs/(Cgs+Cgd)*Cgd + M*Ccbj/3.0*Qt/Qb  )
C
      DVgs = Ig/(Cgs+Cgd) + Cgd/(Cgs+Cgd)*DVcb
C
C *** Test if MOSFET, else evaluate IGBT base charge state equation.
C
      If(t .lt. 0.0) then
         DQt=0.0
      ELSE
        Ip=gama*It/(1+b) + 2.0*D/W**2*Qt + Ccbj/3.0*Qt/Qb*DVcb
        DQt= M*(Imos+Igen) + (M-1.0)*Ip + (Cds+Cgd)*Dvcb - Cgd*DVgs
     &       - Qt/t - 4.0*(Qt*Nscl/ni/Qb)**2*Isne
      ENDIF
C
      DQte6=DQt*1.0E6
      RETURN
      END
C
C
C
C*******************************************************************************
```

Appendix 7
Subroutine IGBTVeb

```
C ***************************************************************************
C
C
C
C   Function to evaluate the transient IGBT emitter-base voltage
C
      SUBROUTINE IGBTVeb(Qte6,Vcb,Rb,Vebq)
C
C
C
C *** Declare external function to iterate the high free carrier
C     level mobility.
C
      Real Dccs
      External Dccs
C
C *** Declare common IGBT model parameters.
C
      REAL              t,wb,nb,A,isne,Vt,Kpsat,Kplin,Rs,theta,
     &                  Cgs,Agd,Coxd,Vtd,BVn,BVf,
     &                  ccsflg,sclflg,vpsat,vnsat,
     &                  Un,Up,Ut,epsi,ni,q
      COMMON /IGBTpar/ t,wb,nb,A,isne,Vt,Kpsat,Kplin,Rs,theta,
     &                  Cgs,Agd,Coxd,Vtd,BVn,BVf,
     &                  ccsflg,sclflg,vpsat,vnsat,
     &                  Un,Up,Ut,epsi,ni,q

C
C *** Declare parameter list variables and functions of model variables.
C
      REAL Qte6,Qt,Vcb,Rb,Vebq,W,Wcbj,L,P,Pmid,Unc,Upc,Ucinv,wl
      REAL cosch,tnh,cth,Ueff,Navg,x,arctnh,Vdep,Vdif,Q0,neff
C
C *** Declare common variables for high free carrier level mobility routine.
C
      REAL ccsvar(5)
      COMMON /Statvr/ ccsvar
      REAL TOL,ROOT,D,Dhi,Dlo
      Qt=Qte6*1.0E-6
      ccsvar(2)=Vcb
      ccsvar(3)=Qt
C
C *** Evaluate functions of model variables.
C
      Wcbj=sqrt(2.0*epsi*abs((Vcb+0.6)/q/Nb))
        if (Vcb .lt. -0.999*0.6)
     &      Wcbj=sqrt(2.0*epsi*abs(((1-0.999)*0.6)/q/Nb))
      W=(Wb-Wcbj)
        if(W .lt. 0.05*Wb)W=0.05*Wb
      Q0=A*sqrt(epsi)*sqrt(2.0*q*Nb*0.6)
C
C *** Test if case of MOSFET.
C
      If(t .lt. 0.0) then
```

```
        Rb=W/Un/A/q/Nb + Rs
        Vebq=0.0
        return
      endif
C
C *** Test if case of emitter-base junction reverse biased (reverse blocking).
C
      If(Qt .lt. 0.0) then
        Rb=W/Un/A/q/Nb +Rs
        Vebq= -0.5*(Qt-Q0)/q/Nb/A**2/epsi*(Qt-Q0) + 0.6
        Return
      ENDIF
C
C *** ELSE: Emitter-base voltage for case of forward biased IGBT.
C
C *** Test if flag for carrier-carrier scattering is set.
C
      If (ccsflg .gt. 0.0) then
C
C ***** Call root to iterate the high free carrier level mobility.
C
        D = 2.0*Ut*Un*Up/(Un+Up)
        Dhi=D
        Dlo=D +Dccs(D)
        TOL = 1.0E-4*D
        D=root(Dlo,Dhi,Dccs,Tol)
C
C ***** Evaluate functions of the model variables.
C
        L = sqrt(t*D)
        wl=w/L
        cosch=1.0/sinh(wl)
        tnh=Tanh(wl/2.0)
        cth=1.0/tanh(wl)
        P=Qt/A/L/tnh/q
        pmid =P*sinh(wl/2.0)/sinh(wl)
C
C *****  1/Uc=Ucinv : the reciprocal component of mobility due to high
C                     free carrier level (carrier-carrier) scattering.
C
        Ucinv= sqrt(Pmid*(Pmid+Nb))*LOG(1.0+ 4.54E11/10.0**(20.0/3.0)
     &  /( (Pmid+Nb)*(Pmid+ni**2.0/Nb) )**(1.0/3.0) ) /1.428E10
C
C       Uc=1.428E10/(sqrt(Pmid*(Pmid+Nb))*LOG(1.0+ 4.54E11
C     &     /10.0**(20.0/3.0)/((Pmid+Nb)*Pmid)**(1.0/3.0)))
C
        Unc = 1.0/(1.0/Un+Ucinv)
        Upc = 1.0/(1.0/Up+Ucinv)
C
C ***** ELSE: case neglecting carrier-carrier scattering.
C
      else
        Unc=Un
        Upc=Up
        D = 2.0*Ut*Un*Up/(Un+Up)
C
C ***** Evaluate functions of model variables.
C
        L = sqrt(t*D)
        wl=w/L
```

```
        cosch=1.0/sinh(wl)
        tnh=Tanh(wl/2.0)
        cth=1.0/tanh(wl)
        P=Qt/A/L/tnh/q
      endif
C
C *** Evaluate the forward biased IGBT emitter base junction voltage.
C
      Ueff=Unc+Upc*Qt/(Qt+Nb)
      Navg=sqrt(Nb**2.0+P**2*cosch**2.0)
      x=(Navg*tnh/(Nb+P*cosch*tnh))
      ARCTNH=0.5*LOG((1.0+x)/(1.0-x))
      neff=wl/2.0*Navg/ARCTNH
      Rb=w/q/Ueff/neff/A + Rs
      Vdep= - 0.5*(Qt-Q0)/q/Nb/A**2/epsi*(Qt-Q0) + 0.6
      Vdif= Ut*LOG((P+Nb)*(P/ni**2+1.0/Nb)) - D/Unc*LOG((Nb+P)/Nb)
      If (Vdif .lt. Vdep .or. Qt .gt. Q0) then
        Vebq= Vdif
      else
        Vebq= Vdep
      endif
      return
      end
C
C
C
C*******************************************************************************
```

Appendix 8
Subroutines IGBTINP, IGBTSTO and IGBTREC

```
C*************************************************************************
C
C
C
C   Subroutine to input the IGBT model parameters from the input
C   File already opened under unit IUNIT.
C
C
      Subroutine IGBTINP(IUNIT)
C
C *** Declare common IGBT model parameters.
C
      REAL              t,wb,nb,A,isne,Vt,Kpsat,Kplin,Rs,theta,
     &                  Cgs,Agd,Coxd,Vtd,BVn,BVf,
     &                  ccsflg,sclflg,vpsat,vnsat,
     &                  Un,Up,Ut,epsi,ni,q
      COMMON /IGBTpar/ t,wb,nb,A,isne,Vt,Kpsat,Kplin,Rs,theta,
     &                  Cgs,Agd,Coxd,Vtd,BVn,BVf,
     &                  ccsflg,sclflg,vpsat,vnsat,
     &                  Un,Up,Ut,epsi,ni,q
      INTEGER IUNIT

C
C *** Read the device model parameters.
C
      read(iunit,*)t
      read(iunit,*)wb
      read(iunit,*)Nb
      read(iunit,*)A
      read(iunit,*)Isne
      read(iunit,*)Vt
      read(iunit,*)Kpsat
      read(iunit,*)Kplin
      read(iunit,*)Rs
      read(iunit,*)theta
      read(iunit,*)Cgs
      read(iunit,*)Agd
      read(iunit,*)Coxd
      read(iunit,*)Vtd
      read(iunit,*)BVn
      read(iunit,*)BVf
C
C *** Read the second order effect flags.
C
      read(iunit,*)ccsflg
      read(iunit,*)sclflg

C
C *** Designate the physical constants of silicon.
C
      Ut = 0.0259
      ni = 1.45
      Un = 1500.0
      Up = 450.0
```

```
      q = 1.6E-9
      epsi=8.854e-14*11.9
      vpsat=0.95e7
      vnsat=1.1e7
      Return
      End
C
C
C
C ***************************************************************************
C
C
C
C   Subroutine to store the IGBT model parameters from the labeled common
C   block IGBTpar into a device parameter array IGBTNAM.
C
C
      Subroutine IGBTSTO(IGBTNAM)
C
C *** Declare common IGBT model parameters.
C
      REAL IGBTNAM(20)
      REAL              t,wb,nb,A,isne,Vt,Kpsat,Kplin,Rs,theta,
     &                  Cgs,Agd,Coxd,Vtd,BVn,BVf,
     &                  ccsflg,sclflg,vpsat,vnsat,
     &                  Un,Up,Ut,epsi,ni,q
      COMMON /IGBTpar/ t,wb,nb,A,isne,Vt,Kpsat,Kplin,Rs,theta,
     &                  Cgs,Agd,Coxd,Vtd,BVn,BVf,
     &                  ccsflg,sclflg,vpsat,vnsat,
     &                  Un,Up,Ut,epsi,ni,q
C
C *** Read the device model parameters.
C
      IGBTNAM(1)=t
      IGBTNAM(2)=wb
      IGBTNAM(3)=Nb
      IGBTNAM(4)=A
      IGBTNAM(5)=Isne
      IGBTNAM(6)=Vt
      IGBTNAM(7)=Kpsat
      IGBTNAM(8)=Kplin
      IGBTNAM(9)=Rs
      IGBTNAM(10)=theta
      IGBTNAM(11)=Cgs
      IGBTNAM(12)=Agd
      IGBTNAM(13)=Coxd
      IGBTNAM(14)=Vtd
      IGBTNAM(15)=BVn
      IGBTNAM(16)=BVf
      IGBTNAM(17)=ccsflg
      IGBTNAM(18)=sclflg


C
      Return
      End
C
C
C
C ***************************************************************************
```

```
C
C
C
C   Subroutine to recall IGBT model parameters from a device parameter
C   array IGBTNAM into the labeled common block IGBTpar.
C
C
      Subroutine IGBTREC(IGBTNAM)
C
C *** Declare common IGBT model parameters.
C
      REAL IGBTNAM(20)
      REAL             t,wb,nb,A,isne,Vt,Kpsat,Kplin,Rs,theta,
     &                 Cgs,Agd,Coxd,Vtd,BVn,BVf,
     &                 ccsflg,sclflg,vpsat,vnsat,
     &                 Un,Up,Ut,epsi,ni,q
      COMMON /IGBTpar/ t,wb,nb,A,isne,Vt,Kpsat,Kplin,Rs,theta,
     &                 Cgs,Agd,Coxd,Vtd,BVn,BVf,
     &                 ccsflg,sclflg,vpsat,vnsat,
     &                 Un,Up,Ut,epsi,ni,q
C
C *** Read the device model parameters.
C
      t=IGBTNAM(1)
      wb=IGBTNAM(2)
      Nb=IGBTNAM(3)
      A=IGBTNAM(4)
      Isne=IGBTNAM(5)
      Vt=IGBTNAM(6)
      Kpsat=IGBTNAM(7)
      Kplin=IGBTNAM(8)
      Rs=IGBTNAM(9)
      theta=IGBTNAM(10)
      Cgs=IGBTNAM(11)
      Agd=IGBTNAM(12)
      Coxd=IGBTNAM(13)
      Vtd=IGBTNAM(14)
      BVn=IGBTNAM(15)
      BVf=IGBTNAM(16)
      ccsflg=IGBTNAM(17)
      sclflg=IGBTNAM(18)

C
      Return
      End
C
C
C
C ***************************************************************************
```

Appendix 9
Function Dccs

```
C ***************************************************************************
C
C
C
C     Function to iterate the ccs diffusivity.
C
      real function Dccs(D)
C
C *** Declare common IGBT model parameters.
C
      REAL              t,wb,nb,A,isne,Vt,Kpsat,Kp1in,Rs,theta,
     &                  Cgs,Agd,Coxd,Vtd,BVn,BVf,
     &                  ccsflg,sclflg,vpsat,vnsat,
     &                  Un,Up,Ut,epsi,ni,q
      COMMON /IGBTpar/ t,wb,nb,A,isne,Vt,Kpsat,Kplin,Rs,theta,
     &                  Cgs,Agd,Coxd,Vtd,BVn,BVf,
     &                  ccsflg,sclflg,vpsat,vnsat,
     &                  Un,Up,Ut,epsi,ni,q
C
C *** Declare common variables and functions of the variables.
C
      REAL Vgs,It,Qt,Vcb,Ig
      COMMON /Statvr/ Vgs,Vcb,Qt,It,Ig
      REAL W,Wcbj,D,L,P,Pmid,Unc,Upc,Ucinv,wl
C
C *** Evaluate functions of model variables.
C
      Wcbj=sqrt(2.0*epsi*abs((Vcb+0.6)/q/Nb))
        if (Vcb .lt. -0.999*0.6)
     &      Wcbj=sqrt(2.0*epsi*abs(((1-0.999)*0.6)/q/Nb))
      W=(Wb-Wcbj)
        if(W .lt. 0.05*Wb)W=0.05*Wb
      L = sqrt(t*D)
      wl=w/l
      P=Qt/A/L/Tanh(wl/2.0)/q
      pmid =P*sinh(wl/2.0)/sinh(wl)
C
C       1/Uc=Ucinv :  the reciprocal component of mobility due to high
C                     free carrier level (carrier-carrier) scattering.
C
      Ucinv= sqrt(Pmid*(Pmid+Nb))*LOG(1.0+ 4.54E11/10.0**(20.0/3.0)
     &  /( (Pmid+Nb)*(Pmid+ni**2.0/Nb) )**(1.0/3.0) ) /1.428E10
C
C       Uc=1.428E10/(sqrt(Pmid*(Pmid+Nb))*LOG(1.0+ 4.54E11
C     &     /10.0**(20.0/3.0)/((Pmid+Nb)*Pmid)**(1.0/3.0)))
C
      Unc = 1.0/(1.0/Un+Ucinv)
      Upc = 1.0/(1.0/Up+Ucinv)
C
C *** Calculate the next iteration carrier-carrier scattering diffusivity.
C
      Dccs =  2.0*Ut*Unc*Upc/(Unc+Upc) - D
      return
      end
```

```
C
C
C
C*************************************************************************
```

Appendix 10
Function Spachg

```
C ***************************************************************************
C
C
C
C  Function to iterate the effective space charge density in the
C  collector-base depletion region including the saturation limited velocity.
C
      REAL FUNCTION spachg(Nscl)
C
C *** Declare common IGBT model parameters.
C
      REAL              t,wb,nb,A,isne,Vt,Kpsat,Kplin,Rs,theta,
     &                  Cgs,Agd,Coxd,Vtd,BVn,BVf,
     &                  ccsflg,sclflg,vpsat,vnsat,
     &                  Un,Up,Ut,epsi,ni,q

      COMMON /IGBTpar/ t,wb,nb,A,isne,Vt,Kpsat,Kplin,Rs,theta,
     &                  Cgs,Agd,Coxd,Vtd,BVn,BVf,
     &                  ccsflg,sclflg,vpsat,vnsat,
     &                  Un,Up,Ut,epsi,ni,q

C
C *** Declare common variables for space charge limited velocity routine
C     and for functions of the model variables.
C
      REAL Vgs,Vcb,Qt,Ig,It,Nscl
      COMMON /Statvr/ Vgs,Vcb,Qt,It,Ig
      REAL D,b,W,Wcbj,Wgdj,Imos,Ccbj,Cds,Cgd,Qb
      REAL gama,M,BV,Igen
      REAL Ip,DVcb
C
C *** Evaluate functions of model variables.
C
C     breakdown voltage,
C
      BV=BVf*5.34E13/(abs(nscl)*1.0E10)**(3.0/4.0)
      If(Vcb .gt. BV*0.999) then
        M=1.0/(1-0.999**BVn)
      else
        if(Vcb .lt. 0.0) M=1.0
        if(Vcb .ge. 0.0)  M=1.0/(1-(Vcb/BV)**BVn)
      endif
      Igen=q/t*ni*A*sqrt(2.0*epsi*abs((Vcb)/q/Nscl))
        If (Vcb .lt. 0)Igen=0.0
C
C     depletion widths and capacitances,
C
      Wcbj=sqrt(2.0*epsi*abs((Vcb+0.6)/q/Nscl))
        if (Vcb .lt. -0.999*0.6)
     &    Wcbj=sqrt(2.0*epsi*abs(((1.0-0.999)*0.6)/q/Nscl))
      W=(Wb-Wcbj)
        if(W .lt. 0.05*Wb)W=0.05*Wb
      Ccbj=A*epsi/Wcbj
      Cds=(A-Agd)*epsi/Wcbj
```

```
      Cgd=Coxd
      If (Vcb .gt. Vgs-Vtd) then
         Wgdj=sqrt(2.0*epsi*abs((Vcb-Vgs+Vtd)/q/nscl))
         Cgd=Coxd/(1.0+Coxd/Agd/epsi*Wgdj)
      endif
C
C     diffusivity, mobility ratio, functions of charge
C
      Qb=Nscl*W*A*q
      gama=0.0
       If (Qt .gt. 0)gama=Qt/(Qt+Qb)
      D=Ut*Up
       If(Qt .ge. 0)D=Ut*Un*Up*(2*Qt+Qb)/(Un*(Qt+Qb)+Qt*Up)
      b = Un/Up
C
C    and MOSFET channel current.
C
      If(vgs .ge. Vt) then
        If (abs(Vcb) .le. (Vgs-Vt)*Kpsat/Kplin)
     &     Imos=Kplin*((Vgs-Vt)*Vcb-0.5*Kplin/Kpsat*abs(Vcb)*Vcb)
     &                 /(1+theta*abs(Vgs-Vt))
        If (abs(Vcb) .gt. (Vgs-Vt)*Kpsat/Kplin)
     &     Imos=0.5*Kpsat*(Vgs-Vt)**2
     &                 /(1+theta*abs(Vgs-Vt))
        If (abs(Vcb) .gt. (Vgs-Vt)*Kpsat/Kplin .and. Vcb .lt. 0.0)
     &     Imos=-Imos
      Else
        Imos=0.0
      Endif
C
C *** Evaluate the collector current.
C                                                                       q
      DVcb = ( It - M*(gama*It/(1+b) + 2.0*D*Qt/W**2 + Imos + Igen)
     &        + Cgd/(Cgs+Cgd)*Ig
     &       )/(  Cds + Cgs/(Cgs+Cgd)*Cgd + M*Ccbj/3.0*Qt/Qb  )
      Ip=gama*It/(1+b) + 2*D/W**2*Qt + Ccbj/3.0*Qt/Qb*DVcb
C
C *** Calculate the next iteration of space charge concentration
C
      spachg = Nscl-Nb-Ip/q/A/vpsat + Imos/q/A/vnsat
      RETURN
      END
C
C
C
C*************************************************************************
```

Appendix 11
Circuit File: Rlload.for

```
C ***************************************************************************
C
C  State Equations, Input Routine, and Output Routine
C  for the Series Resistor-Inductor Load with a Resistive
C  Gate Drive.
C
C ***************************************************************************
C
C
C *** Subroutine to evaluate the state equations of the device and circuit.
C
      SUBROUTINE STATEQ (Time, Y, YP)
C
C *** Designate the number of state equations and declare the calling
C     arrays for the state variables and their time derivatives.
C
      INTEGER NEQN
      PARAMETER (NEQN=4)
      REAL Y(NEQN),YP(NEQN),time
C
C *** Designate external functions.
C
      REAL Pulsgen
      EXTERNAL Pulsgen
C
C *** Declare labeled common block for circuit parameters.
C
      REAL             LL,RL,Vaa,Rg,Vggon,ton,toff,trise
      COMMON /CIRCpar/ LL,RL,Vaa,Rg,Vggon,ton,toff,trise
C
C *** Declare names for state variables and their time derivatives.
C
      REAL Vcb,Qte6,IL,Vgs
      REAL DVcb,DQte6,DIL,DVgs
C
C *** Declare names for functions of state variables.
C
      REAL Va,Ig,Vgg,It,Rb,Vebq
C
C *** Define names for state variables in terms of the calling array.
C
      Vcb   =Y(1)
      Qte6  =Y(2)
      IL    =Y(3)
      Vgs   =Y(4)
C
C *** Evaluate functions of state variables.
C
      call IGBTVeb (Qte6,Vcb,Rb,Vebq)
      Va= IL*Rb + Vcb + Vebq
C
      It=IL
      Vgg=Pulsgen(time,ton,toff,trise,trise,Vggon)
      Ig=(Vgg-Vgs)/Rg
C
```

```
C *** Evaluate the state equations.
C
      call IGBTSEQ(Vgs,Vcb,Qte6,Ig,It,DVgs,DVcb,DQte6)
      DIL=1.0/LL*(-IL*RL-Va+VAA)
C
C *** Define return array for time derivatives of state variables.
C
      YP(1)=DVcb
      YP(2)=DQte6
      YP(3)=DIL
      YP(4)=DVgs
C
      RETURN
      END
C
C
C
C
C
C ***************************************************************************
C
C
C *** Subroutine to input device and circuit parameters, initialize
C     state variables, and to set up the plot and the data file.
C
      SUBROUTINE INPUT (time,Y,NSTATE,ABSERR,RELERR)
C
C *** Designate the number of state variables and declare the
C     calling parameters.
C
      INTEGER NEQN
      PARAMETER (NEQN=4)
      REAL time,Y(NEQN),ABSERR,RELERR
      INTEGER NSTATE
C
C *** Declare labeled common block for circuit parameters.
C
      REAL              LL,RL,Vaa,Rg,Vggon,ton,toff,trise
      COMMON /CIRCpar/ LL,RL,Vaa,Rg,Vggon,ton,toff,trise
C
C *** Declare labeled common block for data output parameters
C     and plotting arrays.
C
      REAL              tplot,tfinal,dltat
      REAL  Xax(400),Y1ax(400),Y2ax(400),Y3ax(400),Y4ax(400)
      REAL  WX(400),WY(400)
      INTEGER           outunit,nout,iout
      COMMON /DATAOUT/ tplot,tfinal,dltat,
     &                  Xax,Y1ax,Y2ax,Y3ax,Y4ax,WX,WY,
     &                  outunit,nout,iout
C
      CHARACTER*40 tlable,vlable,right,head
C
C *** Declare variable for input file names and logical units.
C
      CHARACTER*40 filname
      INTEGER cirunit,devunit
C
C *** Open files to read parameter values from and write waveforms to.
C
```

```
      outunit=10
      devunit=11
      cirunit=12
  2   format(a)
C
  97  write(6,*)
     &    'Enter file to read device input parameters from:  '
      read(5,2) filname
      open(unit=devunit,file=filname,status='old',ERR=97)
C
  98  write(6,*)'Enter file to read circuit input parameters from:  '
      read(5,2) filname
      open(unit=cirunit,file=filname,status='old',ERR=98)
C
  99  write(6,*) 'Enter file to write data to: '
      read(5,2) filname
      open(unit=outunit,file=filname,status='new',ERR=99)
C
C *** Set Error Tolerances and number of state equations.
C
      NSTATE=NEQN
      ABSERR=1.0e-5
      RELERR =1.0e-5
C
C ***  Input device parameters.
C
      CALL IGBTINP(devunit)
C
C *** Input external circuit parameters;
C
C     load parameters,
C
      read(cirunit,*)RL
      read(cirunit,*)LL
      read(cirunit,*)Vaa
C
C     and drive parameters.
C
      read(cirunit,*)RG
      read(cirunit,*)Vggon
      read(cirunit,*)ton
      read(cirunit,*)toff
      read(cirunit,*)trise
C
C *** Also, input plotting parameters.
C
      read(cirunit,*)tfinal
      read(cirunit,*)tplot
C
C *** Initialize the state variables and time.
C
      time=0.0
      Y(1) = Vaa
      Y(2) = 0.0
      Y(3) = 0.0
      Y(4) = 0.0
C
C *** Write number of points at top of output file and calculate increment.
C
      iout=0
```

```
      nout=400
      write(outunit,*)nout
      dltat=(tfinal-tplot)/float(nout)
C
C ***  Set up graphics screen.
C
      tlable='  TIME (US) '
      vlable='VA * IA * VG * IG '
      head=' '
      right=' '
      call SIDTEX(head,0,tlable,1,vlable,1,RIGHT,0)
C                        top    bottom  left   right  0=color=default
C
C
      RETURN
      END
C
C
C
C
C ***************************************************************************
C
C
C *** Subroutine to write and plot the output quantities.
C
      SUBROUTINE OUTPUT(time, Y)
C
C *** Designate the number of state variables and declare the
C     calling parameters.
C
      INTEGER NEQN
      PARAMETER (NEQN=4)
      REAL Y(NEQN),time
C
C *** Designate external functions.
C
      REAL Pulsgen
      EXTERNAL Pulsgen
C
C *** Declare labeled common block for circuit parameters.
C
      REAL             LL,RL,Vaa,Rg,Vggon,ton,toff,trise
      COMMON /CIRCpar/ LL,RL,Vaa,Rg,Vggon,ton,toff,trise
C
C *** Declare labeled common block for data output parameters
C     and plotting arrays.
C
      REAL             tplot,tfinal,dltat
      REAL  Xax(400),Y1ax(400),Y2ax(400),Y3ax(400),Y4ax(400)
      REAL  WX(400),WY(400)
      INTEGER          outunit,nout,iout,nplt,loopin
      COMMON /DATAOUT/ tplot,tfinal,dltat,
     &                 Xax,Y1ax,Y2ax,Y3ax,Y4ax,WX,WY,
     &                 outunit,nout,iout
C
C *** Declare names for state variables.
C
      REAL Vcb,Qte6,IL,Vgs
C
C *** Declare names for functions of state variables.
```

```
C
      REAL Va,Ig,Vgg,It,Rb,Vebq,Qt
C
C
C *** If time is greater than or equal to tplot then:
C     Write out the anode voltage, gate voltage, anode current,
C     gate current, and charge at each time step, and plot
C     the device current and voltages. Otherwise, increment
C     the time and do another step.
C
      If(time .lt. tplot)then
      time=time+dltat
      return
      endif
C
C *** Define state variables.
C
      Vcb   =Y(1)
      Qte6  =Y(2)
      IL    =Y(3)
      Vgs   =Y(4)
C
C *** Calculate functions of state variables for output quantities.
C
      call IGBTVeb (Qte6,Vcb,Rb,Vebq)
      Va= IL*Rb + Vcb+Vebq
      It=IL
      Vgg=Pulsgen(time,ton,toff,trise,trise,Vggon)
      Ig=(Vgg-Vgs)/Rg
      Qt=Qte6*1.0E-6
C
C *** Write output quantities to logical unit.
C
      write(outunit,10)Time-tplot,
     &                 Va,It,Vgs,Ig,Qt,Vebq,rb
 10   format(8(1x,E10.4))
C
C *** Store normalized quantities for graphics output.
C
      iout=iout+1
      nplt=iout
      xax(iout)=time*1.0e6
      y1ax(iout)=Va
      y2ax(iout)=Vaa*2.0/Vggon*Vgs
      y3ax(iout)=Vaa+ Vaa/Vggon*Rg*Ig
      y4ax(iout)=It*2*RL

C
C *** Increment the integration time and decide if is final plot.
C
      time=time + dltat
      If (time .lt. tfinal)then
         return
      else
C
C *** Interactive graphics loop.
C
 99      continue
         call HOWPLT(0,1,1)
         call curv(nplt,xax,y1ax)
```

```
C
         call HOWPLT(0,1,3)
         call curv(nplt,xax,y2ax)
C
         call HOWPLT(0,1,7)
         call curv(nplt,xax,y3ax)
C
         call HOWPLT(0,1,4)
         call curv(nplt,xax,y4ax)
C
         call vg
         if(loopin().eq.1)goto 99
         stop
      endif
C
      END
C
C
C
C
C ***************************************************************************
C
C     Function to generate a single pulse.
C
C
      REAL function pulsgen(time,ton,toff,trise,tfall,Vggon)
C
      REAL Vgg,time,ton,toff,trise,tfall,Vggon
C
      Vgg=0.0
      If (time .gt. ton .and. time .lt. ton+trise)
     &     Vgg=Vggon*(time-ton)/trise
      If (time .ge. ton+trise .and. time .lt. toff)Vgg=Vggon
      If (time .ge. toff .and. time .lt. toff+tfall)
     &     Vgg=Vggon*(1.0-(time-toff)/tfall)
      pulsgen=Vgg
C
      RETURN
      END
```

Appendix 12
Circuit File: Clamp.for

```
C ***************************************************************************
C
C  State Equations, Input Routine, and Output Routine
C  for the Series Resistor-Inductor Load with a Resistive
C  Gate Drive, and a Soft Clamping Circuit.
C
C ***************************************************************************
C
C
C *** Subroutine to evaluate the state equations of the device and circuit.
C
      SUBROUTINE STATEQ (Time, Y, YP)
C
C *** Designate the number of state equations and declare the calling
C     arrays for the state variables and their time derivatives.
C
      INTEGER NEQN
      PARAMETER (NEQN=5)
      REAL Y(NEQN),YP(NEQN),time
C
C *** Designate external functions.
C
      REAL Pulsgen
      EXTERNAL Pulsgen
C
C *** Declare labeled common block for circuit parameters.
C
      REAL              LL,RL,Vaa,Rg,Vggon,ton,toff,trise,Rblead,
     &                  Cs,Rd,Vss
      COMMON /CIRCpar/ LL,RL,Vaa,Rg,Vggon,ton,toff,trise,Rblead,
     &                  Cs,Rd,Vss
C
C *** Declare names for state variables and their time derivatives.
C
      REAL Vcb,Qte6,IL,Vgs,Vs
      REAL DVcb,DQte6,DIL,DVgs,DVs
C
C *** Declare names for functions of state variables.
C
      REAL Va,Ig,Vgg,It,Rb,Vebq
C
C *** Define names for state variables in terms of the calling array.
C
      Vcb   =Y(1)
      Qte6  =Y(2)
      IL    =Y(3)
      Vgs   =Y(4)
      Vs    =Y(5)
C
C *** Evaluate functions of state variables.
C
      call IGBTVeb (Qte6,Vcb,Rb,Vebq)
      Va= IL*Rb + Vcb + Vebq
      if(Va .gt. Vs+0.6)Va=(IL*Rb*Rd+(Vs+0.6)*Rb+(Vcb+Vebq)*Rd)/(Rb+Rd)
C
```

```
      It=IL
      if (Va .gt. Vs + 0.6) It=IL-(Va-Vs-0.6)/Rd
C
      Vgg=Pulsgen(time,ton,toff,trise,trise,Vggon)
      Ig=(Vgg-Vgs)/Rg
C
C *** Evaluate the state equations.
C
      call IGBTSEQ(Vgs,Vcb,Qte6,Ig,It,DVgs,DVcb,DQte6)
      DIL=1.0/LL*(-IL*RL-Va+VAA)
      DVs=(Va-Vs-0.6)/Cs/Rd  - (Vs-Vss)/Rblead/Cs
      if(Va .lt. Vs +0.6)DVs=- (Vs-Vss)/Rblead/Cs
C
C *** Define return array for time derivatives of state variables.
C
      YP(1)=DVcb
      YP(2)=DQte6
      YP(3)=DIL
      YP(4)=DVgs
      YP(5)=DVs
C
      RETURN
      END
C
C
C
C
C
C ***************************************************************************
C
C
C *** Subroutine to input device and circuit parameters, initialize
C     state variables, and to set up the plot and the data file.
C
      SUBROUTINE INPUT (time,Y,NSTATE,ABSERR,RELERR)
C
C *** Designate the number of state variables and declare the
C     calling parameters.
C
      INTEGER NEQN
      PARAMETER (NEQN=5)
      REAL time,Y(NEQN),ABSERR,RELERR
      INTEGER NSTATE
C
C *** Declare labeled common block for circuit parameters.
C
      REAL              LL,RL,Vaa,Rg,Vggon,ton,toff,trise,Rblead,
     &                  Cs,Rd,Vss
      COMMON /CIRCpar/ LL,RL,Vaa,Rg,Vggon,ton,toff,trise,Rblead,
     &                  Cs,Rd,Vss
C
C *** Declare labeled common block for data output parameters
C     and plotting arrays.
C
      REAL              tplot,tfinal,dltat
      REAL  Xax(400),Y1ax(400),Y2ax(400),Y3ax(400),Y4ax(400)
      REAL  WX(400),WY(400)
      INTEGER           outunit,nout,iout
      COMMON /DATAOUT/ tplot,tfinal,dltat,
     &                  Xax,Y1ax,Y2ax,Y3ax,Y4ax,WX,WY,
```

```
     &                 outunit,nout,iout
C
      CHARACTER*40 tlable,vlable,right,head
C
C *** Declare variable for input file names and logical units.
C
      CHARACTER*40 filname
      INTEGER cirunit,devunit
C
C *** Open files to read parameter values from and write waveforms to.
C
      outunit=10
      devunit=11
      cirunit=12
  2   format(a)
C
  97  write(6,*)
     &    'Enter file to read device input parameters from:  '
      read(5,2) filname
      open(unit=devunit,file=filname,status='old',ERR=97)
C
  98  write(6,*)'Enter file to read circuit input parameters from:  '
      read(5,2) filname
      open(unit=cirunit,file=filname,status='old',ERR=98)
C
  99  write(6,*) 'Enter file to write data to: '
      read(5,2) filname
      open(unit=outunit,file=filname,status='new',ERR=99)
C
C *** Set Error Tolerances and number of state equations.
C
      NSTATE=NEQN
      ABSERR=1.0e-5
      RELERR =1.0e-5
C
C ***  Input device parameters.
C
      CALL IGBTINP(devunit)
C
C *** Input external circuit parameters;
C
C     load parameters,
C
      read(cirunit,*)RL
      read(cirunit,*)LL
      read(cirunit,*)Vaa
C
C *** snubber parameters,
C
      read(cirunit,*)Vss
      read(cirunit,*)Rblead
      read(cirunit,*)Cs
      read(cirunit,*)Rd
C
C     and drive parameters.
C
      read(cirunit,*)RG
      read(cirunit,*)Vggon
      read(cirunit,*)ton
      read(cirunit,*)toff
```

```
      read(cirunit,*)trise
C
C *** Also, input plotting parameters.
C
      read(cirunit,*)tfinal
      read(cirunit,*)tplot
C
C *** Initialize the state variables and time.
C
      time=0.0
      Y(1) = Vaa
      Y(2) = 0.0
      Y(3) = 0.0
      Y(4) = 0.0
      Y(5) = Vss
C
C *** Write number of points at top of output file and calculate increment.
C
      iout=0
      nout=400
      write(outunit,*)nout
      dltat=(tfinal-tplot)/float(nout)
C
C ***  Set up graphics screen.
C
      tlable='  TIME (US) '
      vlable='VA * IA * VG * IG '
      head=' '
      right=' '
      call SIDTEX(head,0,tlable,1,vlable,1,RIGHT,0)
C                       top    bottom  left   right  0=color=default
C
C
      RETURN
      END
C
C
C
C
C ***************************************************************************
C
C
C *** Subroutine to write and plot the output quantities.
C
      SUBROUTINE OUTPUT(time, Y)
C
C *** Designate the number of state variables and declare the
C     calling parameters.
C
      INTEGER NEQN
      PARAMETER (NEQN=5)
      REAL Y(NEQN),time
C
C *** Designate external functions.
C
      REAL Pulsgen
      EXTERNAL Pulsgen
C
C *** Declare labeled common block for circuit parameters.
```

```
C
      REAL              LL,RL,Vaa,Rg,Vggon,ton,toff,trise,Rblead,
     &                  Cs,Rd,Vss
      COMMON /CIRCpar/ LL,RL,Vaa,Rg,Vggon,ton,toff,trise,Rblead,
     &                  Cs,Rd,Vss
C
C *** Declare labeled common block for data output parameters
C     and plotting arrays.
C
      REAL              tplot,tfinal,dltat
      REAL  Xax(400),Y1ax(400),Y2ax(400),Y3ax(400),Y4ax(400)
      REAL  WX(400),WY(400)
      INTEGER           outunit,nout,iout,nplt,loopin
      COMMON /DATAOUT/ tplot,tfinal,dltat,
     &                  Xax,Y1ax,Y2ax,Y3ax,Y4ax,WX,WY,
     &                  outunit,nout,iout
C
C *** Declare names for state variables.
C
      REAL Vcb,Qte6,IL,Vgs,Vs
C
C *** Declare names for functions of state variables.
C
      REAL Va,Ig,Vgg,It,Rb,Vebq,Qt
C
C
C *** If time is greater than or equal to tplot then:
C     Write out the  anode voltage, gate voltage, anode current,
C     gate current, and charge at each time step, and plot
C     the device current and voltages. Otherwise, increment
C     the time and do another step.
C
      If(time .lt. tplot)then
      time=time+dltat
      return
      endif
C
C *** Define state variables.
C
      Vcb   =Y(1)
      Qte6  =Y(2)
      IL    =Y(3)
      Vgs   =Y(4)
      Vs    =Y(5)
C
C *** Calculate functions of state variables for output quantities.
C
      call IGBTVeb (Qte6,Vcb,Rb,Vebq)
      Va= IL*Rb + Vcb + Vebq
      if(Va .gt. Vs+0.6)Va=(IL*Rb*Rd+(Vs+0.6)*Rb+(Vcb+Vebq)*Rd)/(Rb+Rd)
C
      It=IL
      if (Va .gt. Vs + 0.6) It=IL-(Va-Vs-0.6)/Rd
C
      Vgg=Pulsgen(time,ton,toff,trise,trise,Vggon)
      Ig=(Vgg-Vgs)/Rg
      Qt=Qte6*1.0E-6
C
C *** Write output quantities to logical unit.
C
```

```
      write(outunit,10)Time-tplot,
     &                 Va,It,Vgs,Ig,Qt,Vebq,rb,Vs
 10   format(8(1x,E10.4))
C
C *** Store normalized quantities for graphics output.
C
      iout=iout+1
      nplt=iout
      xax(iout)=time*1.0e6
      y1ax(iout)=Va
      y2ax(iout)=Vaa*2.0/Vggon*Vgs
      y3ax(iout)=Vaa+ Vaa/Vggon*Rg*Ig
      y4ax(iout)=It*2*RL

C
C *** Increment the integration time and decide if is final plot.
C
      time=time + dltat

      If (time .lt. tfinal)then
         return
      else
C
C *** Interactive graphics loop.
C
 99      continue
         call HOWPLT(0,1,1)
         call curv(nplt,xax,y1ax)
C
         call HOWPLT(0,1,3)
         call curv(nplt,xax,y2ax)
C
         call HOWPLT(0,1,7)
         call curv(nplt,xax,y3ax)
C
         call HOWPLT(0,1,4)
         call curv(nplt,xax,y4ax)
C
         call vg
         if(loopin().eq.1)goto 99
         stop
      endif
C
      END
C
C
C
C
C ***********************************************************************
C
C     Function to generate a single pulse.
C
C
      REAL function pulsgen(time,ton,toff,trise,tfall,Vggon)
C
      REAL Vgg,time,ton,toff,trise,tfall,Vggon
C
      Vgg=0.0
      If (time .gt. ton .and. time .lt. ton+trise)
     &     Vgg=Vggon*(time-ton)/trise
```

```
      If (time .ge. ton+trise .and. time .lt. toff)Vgg=Vggon
      If (time .ge. toff .and. time .lt. toff+tfall)
     &     Vgg=Vggon*(1.0-(time-toff)/tfall)
      pulsgen=Vgg
C
      RETURN
      END
```

Appendix 13
Circuit File: Actsnub.for

```
C ***************************************************************************
C
C  State Equations, Input Routine, and Output Routine
C  for the Series Resistor-Inductor Load, a Polarized
C  Gate Resistance, and a series Resistor-Capacitor Feedback.
C
C ***************************************************************************
C
C
C *** Subroutine to evaluate the state equations of the device and circuit.
C
      SUBROUTINE STATEQ (Time, Y, YP)
C
C *** Designate the number of state equations and declare the calling
C     arrays for the state variables and their time derivatives.
C
      INTEGER NEQN
      PARAMETER (NEQN=5)
      REAL Y(NEQN),YP(NEQN),time
C
C *** Designate external functions.
C
      REAL Pulsgen
      EXTERNAL Pulsgen
C
C *** Declare labeled common block for circuit parameters.
C
      REAL             LL,RL,Vaa,Rg,Vggon,ton,toff,trise,Cf,Rf,rgon
      COMMON /CIRCpar/ LL,RL,Vaa,Rg,Vggon,ton,toff,trise,Cf,Rf,rgon
C
C *** Declare names for state variables and their time derivatives.
C
      REAL Vcb,Qte6,IL,Vgs,Vcf
      REAL DVcb,DQte6,DIL,DVgs,DVcf
C
C *** Declare names for functions of state variables.
C
      REAL Va,Ig,Vgg,It,Rb,Vebq
C
C *** Define names for state variables in terms of the calling array.
C
      Vcb   =Y(1)
      Qte6  =Y(2)
      IL    =Y(3)
      Vgs   =Y(4)
      Vcf   =Y(5)
C
C *** Evaluate functions of state variables.
C
      call IGBTVeb (Qte6,Vcb,Rb,Vebq)
      Va=( IL*Rb*Rf + (Vcb+Vebq)*Rf + (Vgs+Vcf)*Rb ) / (Rb+Rf)
      It=IL-(Va-Vgs-Vcf)/Rf
      Vgg=Pulsgen(time,ton,toff,trise,trise,Vggon)
      Ig=(Vgg-Vgs)/Rg+ (Va-Vcf-Vgs)/Rf
      If( Vgg .ge. (Vgs+0.6) )Ig=Ig + (Vgg-Vgs-0.6)/Rgon
```

```
C
C *** Evaluate the state equations.
C
      call IGBTSEQ(Vgs,Vcb,Qte6,Ig,It,DVgs,DVcb,DQte6)
      DIL=1.0/LL*(-IL*RL-Va+VAA)
      DVcf=1.0/(Rf*Cf)*(Va-Vgs-Vcf)
C
C *** Define return array for time derivatives of state variables.
C
      YP(1)=DVcb
      YP(2)=DQte6
      YP(3)=DIL
      YP(4)=DVgs
      YP(5)=DVcf
C
      RETURN
      END
C
C
C
C
C
C ***************************************************************************
C
C
C *** Subroutine to input device and circuit parameters, initialize
C     state variables, and to set up the plot and the data file.
C
      SUBROUTINE INPUT (time,Y,NSTATE,ABSERR,RELERR)
C
C *** Designate the number of state variables and declare the
C     calling parameters.
C
      INTEGER NEQN
      PARAMETER (NEQN=5)
      REAL time,Y(NEQN),ABSERR,RELERR
      INTEGER NSTATE
C
C *** Declare labeled common block for circuit parameters.
C
      REAL             LL,RL,Vaa,Rg,Vggon,ton,toff,trise,Cf,Rf,rgon
      COMMON /CIRCpar/ LL,RL,Vaa,Rg,Vggon,ton,toff,trise,Cf,Rf,rgon
C
C *** Declare labeled common block for data output parameters
C     and plotting arrays.
C
      REAL             tplot,tfinal,dltat
      REAL  Xax(400),Y1ax(400),Y2ax(400),Y3ax(400),Y4ax(400)
      REAL  WX(400),WY(400)
      INTEGER          outunit,nout,iout
      COMMON /DATAOUT/ tplot,tfinal,dltat,
     &                 Xax,Y1ax,Y2ax,Y3ax,Y4ax,WX,WY,
     &                 outunit,nout,iout
C
      CHARACTER*40 tlable,vlable,right,head
C
C *** Declare variable for input file name and logical units.
C
      CHARACTER*40 filname
      INTEGER cirunit,devunit
```

```
C
C *** Open files to read parameter values from and write waveforms to.
C
      outunit=10
      devunit=11
      cirunit=12
  2   format(a)
  97  write(6,*)
     &     'Enter file to read device input parameters from:  '
      read(5,2) filname
      open(unit=devunit,file=filname,status='old',ERR=97)
C
  98  write(6,*)
     &     'Enter file to read circuit input parameters from:  '
      read(5,2) filname
      open(unit=cirunit,file=filname,status='old',ERR=98)
C
  99  write(6,*) 'Enter file to write data to: '
      read(5,2) filname
      open(unit=outunit,file=filname,status='new',ERR=99)
C
C *** Set error tolerances and number of state equations.
C
      NSTATE=NEQN
      ABSERR=1.0e-5
      RELERR=1.0e-5
C
C ***  Input device parameters.
C
C Note: normalize all charges to 1.0E10 and distances are in cm
C
      CALL IGBTINP(devunit)
C
C *** Input external circuit parameters;
C
C     load parameters,
C
      read(cirunit,*)RL
      read(cirunit,*)LL
      read(cirunit,*)Vaa
C
C     drive parameters,
C
      read(cirunit,*)RG
      read(cirunit,*)Vggon
      read(cirunit,*)ton
      read(cirunit,*)toff
      read(cirunit,*)trise
C
C     and feedback parameters.
C
      read(cirunit,*)Cf
      read(cirunit,*)Rf
      read(cirunit,*)Rgon
C
C *** Also, input data and plotting parameters.
C
      read(cirunit,*)tfinal
      read(cirunit,*)tplot
C
```

```
C *** Initialize the state variables and time.
C
C
      time=0.0
      Y(1) = Vaa
      Y(2) = 0.0
      Y(3) = 0.0
      Y(4) = 0.0
      Y(5) = Vaa
C
C *** Write number of points at top of output file and calculate increment.
C
      iout=0
      nout=400
      write(outunit,*)nout
      dltat=(tfinal-tplot)/float(nout)
C
C ***  Set up graphics screen.
C
      tlable='  TIME (US) '
      vlable='VA * IA * VG * IG '
      head=' '
      right=' '
      call SIDTEX(head,0,tlable,1,vlable,1,RIGHT,0)
C                       top    bottom  left     right  0=color=default
C
C
      RETURN
      END
C
C
C
C
C
C ***************************************************************************
C
C
C *** Subroutine to write and plot the output quantities.
C
      SUBROUTINE OUTPUT(time, Y)
C
C *** Designate the number of state variables and declare the
C     calling parameters.
C
      INTEGER NEQN
      PARAMETER (NEQN=5)
      REAL Y(NEQN),time
C
C *** Designate external functions.
C
      REAL Pulsgen
      EXTERNAL Pulsgen
C
C *** Declare labeled common block for circuit parameters.
C
      REAL              LL,RL,Vaa,Rg,Vggon,ton,toff,trise,Cf,Rf,rgon
      COMMON /CIRCpar/ LL,RL,Vaa,Rg,Vggon,ton,toff,trise,Cf,Rf,rgon
C
C *** Declare labeled common block for data output parameters
C     and plotting arrays.
```

```
C
      REAL              tplot,tfinal,dltat
      REAL  Xax(400),Y1ax(400),Y2ax(400),Y3ax(400),Y4ax(400)
      REAL  WX(400),WY(400)
      INTEGER           outunit,nout,iout,nplt,loopin
      COMMON /DATAOUT/ tplot,tfinal,dltat,
     &                  Xax,Y1ax,Y2ax,Y3ax,Y4ax,WX,WY,
     &                  outunit,nout,iout
C
C *** Declare names for state variables.
C
      REAL Vcb,Qte6,IL,Vgs,Vcf
C
C *** Declare names for functions of state variables.
C
      REAL Va,Ig,Vgg,It,Rb,Vebq,Qt
C
C
C *** If time is greater than or equal to tplot then:
C     Write out the anode voltage, gate voltage, anode current,
C     gate current, and charge at each time step, and plot
C     the device current and voltages. Otherwise, increment
C     the time and do another step.
C
      If(time .lt. tplot)then
      time=time+dltat
      return
      endif
C
C *** Define state variables.
C
      Vcb   =Y(1)
      Qte6  =Y(2)
      IL    =Y(3)
      Vgs   =Y(4)
      Vcf   =Y(5)
C
C *** Calculate functions of state variables for output quantities.
C
      call IGBTVeb (Qte6,Vcb,Rb,Vebq)
      Va=( IL*Rb*Rf + (Vcb+Vebq)*Rf + (Vgs+Vcf)*Rb ) / (Rb+Rf)
      It=IL-(Va-Vgs-Vcf)/Rf
      Vgg=Pulsgen(time,ton,toff,trise,trise,Vggon)
      Ig=(Vgg-Vgs)/Rg+ (Va-Vcf-Vgs)/Rf
      If( Vgg .ge. (Vgs+0.6) )Ig=Ig + (Vgg-Vgs-0.6)/Rgon
      Qt=Qte6*1.0E-6
C
C *** Write output quantities to logical unit.
C
      write(outunit,10)Time-tplot,
     &                  Va,Vgs,IL,Ig,Vcf,(Va-Vgs-Vcf)/Rf
 10   format(7(1x,E10.4))
C
C ***  Store normalized quantities for graphics output.
C
      iout=iout+1
      nplt=iout
      xax(iout)=time*1.0e6
      y1ax(iout)=Va
      y2ax(iout)=Vaa*2.0/Vggon*Vgs
```

```
      y3ax(iout)=Vaa+ Vaa/Vggon*Rgon*Ig
      y4ax(iout)=It*2*RL
C
C *** Increment the integration time and decide if is final plot.
C
      time=time + dltat
      If (time .lt. tfinal)then
         return
      else
C
C *** Interactive graphics loop.
C
 99      continue
         call HOWPLT(0,1,1)
         call curv(nplt,xax,y1ax)
C
         call HOWPLT(0,1,3)
         call curv(nplt,xax,y2ax)
C
         call HOWPLT(0,1,7)
         call curv(nplt,xax,y3ax)
C
         call HOWPLT(0,1,4)
         call curv(nplt,xax,y4ax)
C
         call vg
         if(loopin().eq.1)goto 99
         stop
      endif
C
      END
C
C
C
C
C ***************************************************************************
C
C     Function to generate a single pulse.
C
C
      REAL function pulsgen(time,ton,toff,trise,tfall,Vggon)
C
      REAL Vgg,time,ton,toff,trise,tfall,Vggon
C
      Vgg=0.0
      If (time .gt. ton .and. time .lt. ton+trise)
     &     Vgg=Vggon*(time-ton)/trise
      If (time .ge. ton+trise .and. time .lt. toff)Vgg=Vggon
      If (time .ge. toff .and. time .lt. toff+tfall)
     &     Vgg=Vggon*(1.0-(time-toff)/tfall)
      pulsgen=Vgg
C
      RETURN
      END
```

Appendix 14
Circuit File: Paralel.for

```
C ***************************************************************************
C
C  State Equations, Input Routine, and Output Routine
C  for Paralleled IGBTs with a Series Resistor-Inductor Load and
C  a Resistive Gate Drive.
C
C ***************************************************************************
C
C
C *** Subroutine to evaluate the state equations of the device and circuit.
C
      SUBROUTINE STATEQ (Time, Y, YP)
C
C *** Designate the number of state equations and declare the calling
C     arrays for the state variables and their time derivatives.
C
      INTEGER NEQN
      PARAMETER (NEQN=7)
      REAL Y(NEQN),YP(NEQN),time
C
C *** Designate external functions.
C
      REAL Pulsgen
      EXTERNAL Pulsgen
C
C *** Declare labeled common block for circuit parameters.
C
      REAL              LL,RL,Vaa,Rg1,Rg2,Vggon,ton,toff,trise,
     &                  IGBT1(20),IGBT2(20)
      COMMON /CIRCpar/ LL,RL,Vaa,Rg1,Rg2,Vggon,ton,toff,trise,
     &                  IGBT1,IGBT2
C
C *** Declare names for state variables and their time derivatives.
C
      REAL Il,Vcb1,Qte61,Vg1,Vcb2,Qte62,Vg2
      REAL DIL,DVcb1,DQte61,DVg1,DVcb2,DQte62,DVg2
C
C *** Declare names for functions of state variables.
C
      REAL Vgg,Va,Ig1,It1,Rb1,Vebq1,Ig2,It2,Rb2,Vebq2
C
C *** Define names for state variables in terms of the calling array.
C
      IL     =Y(1)
      Vcb1   =Y(2)
      Qte61  =Y(3)
      Vg1    =Y(4)
      Vcb2   =Y(5)
      Qte62  =Y(6)
      Vg2    =Y(7)
C
C *** Evaluate functions of state variables.
C
      call IGBTREC(IGBT1)
      call IGBTVeb (Qte61,Vcb1,Rb1,Vebq1)
```

```
C
      call IGBTREC(IGBT2)
      call IGBTVeb (Qte62,Vcb2,Rb2,Vebq2)
C
      Va= ( IL + (Vcb1+Vebq1)/Rb1 + (Vcb2+Vebq2)/Rb2 )
     &    *  Rb1*Rb2/(Rb1+Rb2)
C
      It1=(Va-Vcb1-Vebq1)/Rb1
      It2=(Va-Vcb2-Vebq2)/Rb2
C
      Vgg=Pulsgen(time,ton,toff,trise,trise,Vggon)
      Ig1=(Vgg-Vg1)/Rg1
      Ig2=(Vgg-Vg2)/Rg2
C
C *** Evaluate the state equations.
C
      CALL IGBTREC(IGBT1)
      call IGBTSEQ(Vg1,Vcb1,Qte61,Ig1,It1,DVg1,DVcb1,DQte61)
C
      CALL IGBTREC(IGBT2)
      call IGBTSEQ(Vg2,Vcb2,Qte62,Ig2,It2,DVg2,DVcb2,DQte62)
C
      DIL=1.0/LL*(-IL*RL-Va+VAA)
C
C *** Define return array for time derivatives of state variables.
C
      YP(1)    =DIL
      YP(2)    =DVcb1
      YP(3)    =DQte61
      YP(4)    =DVg1
      YP(5)    =DVcb2
      YP(6)    =DQte62
      YP(7)    =DVg2
C
      RETURN
      END
C
C
C
C
C
C ***************************************************************************
C
C
C *** Subroutine to input device and circuit parameters, initialize
C     state variables, and to set up the plot and the data file.
C
      SUBROUTINE INPUT (time,Y,NSTATE,ABSERR,RELERR)
C
C *** Designate the number of state variables and declare the
C     calling parameters.
C
      INTEGER NEQN
      PARAMETER (NEQN=7)
      REAL time,Y(NEQN),ABSERR,RELERR
      INTEGER NSTATE
C
C *** Declare labeled common block for circuit parameters.
C
      REAL             LL,RL,Vaa,Rg1,Rg2,Vggon,ton,toff,trise,
```

```
     &                 IGBT1(20),IGBT2(20)
      COMMON /CIRCpar/ LL,RL,Vaa,Rg1,Rg2,Vggon,ton,toff,trise,
     &                 IGBT1,IGBT2
C
C *** Declare labeled common block for data output parameters
C     and plotting arrays.
C
      REAL             tplot,tfinal,dltat
      REAL  Xax(400),Y1ax(400),Y2ax(400),Y3ax(400),Y4ax(400)
      REAL  Y5ax(400),Y6ax(400),Y7ax(400)
      REAL  WX(400),WY(400)
      INTEGER          outunit,nout,iout
      COMMON /DATAOUT/ tplot,tfinal,dltat,
     &                 Xax,Y1ax,Y2ax,Y3ax,Y4ax,WX,WY,
     &                 Y5ax,Y6ax,Y7ax,
     &                 outunit,nout,iout
C
      CHARACTER*40 tlable,vlable,right,head
C
C *** Declare variable for input file names and logical units.
C
      CHARACTER*40 filname
      INTEGER cirunit,devunit
      outunit=10
      devunit=11
      cirunit=12
  2   format(a)
C
C *** Input device parameters and store in parameter arrays.
C
  96  write(6,*)
     &    'Enter file name of device parameters for IGBT #1:  '
      read(5,2) filname
      open(unit=devunit,file=filname,status='old',ERR=96)
      CALL IGBTINP(devunit)
      CALL IGBTSTO(IGBT1)
      close (devunit)
C
  97  write(6,*)
     &    'Enter file name of device parameters for IGBT #2:  '
      read(5,2) filname
      open(unit=devunit,file=filname,status='old',ERR=97)
      CALL IGBTINP(devunit)
      CALL IGBTSTO(IGBT2)
      close (devunit)
C
C *** Open files to read parameter values from and write waveforms to.
C
  98  write(6,*)'Enter file to read circuit input parameters from:  '
      read(5,2) filname
      open(unit=cirunit,file=filname,status='old',ERR=98)
C
  99  write(6,*) 'Enter file to write data to: '
      read(5,2) filname
      open(unit=outunit,file=filname,status='new',ERR=99)
C
C *** Set Error Tolerances and number of state equations.
C
      NSTATE=NEQN
      ABSERR=1.0e-4
```

```
      RELERR =1.0e-4
C
C *** Input external circuit parameters;
C
C     load parameters,
C
      read(cirunit,*)RL
      read(cirunit,*)LL
      read(cirunit,*)Vaa
C
C     and drive parameters.
C
      read(cirunit,*)Rg1
      read(cirunit,*)Rg2
      read(cirunit,*)Vggon
      read(cirunit,*)ton
      read(cirunit,*)toff
      read(cirunit,*)trise
C
C *** Also, input plotting parameters.
C
      read(cirunit,*)tfinal
      read(cirunit,*)tplot
C
C *** Initialize the state variables and time.
C
      time=0.0
      Y(1)   =0.0
      Y(2)   =Vaa
      Y(3)   =0.0
      Y(4)   =0.0
      Y(5)   =Vaa
      Y(6)   =0.0
      Y(7)   =0.0
C
C *** Write number of points at top of output file and calculate increment.
C
      iout=0
      nout=400
      write(outunit,*)nout
      dltat=(tfinal-tplot)/float(nout)
C
C ***  Set up graphics screen.
C
      tlable='  TIME (US) '
      vlable='VA * IA * VG * IG '
      head=' '
      right=' '
      call SIDTEX(head,0,tlable,1,vlable,1,RIGHT,0)
C                       top    bottom  left   right  0=color=default


C
      RETURN
      END
C
C
C
C
C ***************************************************************************
```

```
C
C
C *** Subroutine to write and plot the output quantities.
C
      SUBROUTINE OUTPUT(time, Y)
C
C *** Designate the number of state variables and declare the
C     calling parameters.
C
      INTEGER NEQN
      PARAMETER (NEQN=7)
      REAL Y(NEQN),time
C
C *** Designate external functions.
C
      REAL Pulsgen
      EXTERNAL Pulsgen
C
C *** Declare labeled common block for circuit parameters.
C
      REAL             LL,RL,Vaa,Rg1,Rg2,Vggon,ton,toff,trise,
     &                 IGBT1(20),IGBT2(20)
      COMMON /CIRCpar/ LL,RL,Vaa,Rg1,Rg2,Vggon,ton,toff,trise,
     &                 IGBT1,IGBT2
C
C *** Declare labeled common block for data output parameters
C     and plotting arrays.
C
      REAL             tplot,tfinal,dltat
      REAL  Xax(400),Y1ax(400),Y2ax(400),Y3ax(400),Y4ax(400)
      REAL  Y5ax(400),Y6ax(400),Y7ax(400)
      REAL  WX(400),WY(400)
      INTEGER          outunit,nout,iout,nplt
      COMMON /DATAOUT/ tplot,tfinal,dltat,
     &                 Xax,Y1ax,Y2ax,Y3ax,Y4ax,WX,WY,
     &                 Y5ax,Y6ax,Y7ax,
     &                 outunit,nout,iout

C
C *** Declare names for state variables and their time derivatives.
C
      REAL Il,Vcb1,Qte61,Vg1,Vcb2,Qte62,Vg2
C
C *** Declare names for functions of state variables.
C
      REAL Vgg,Va,Ig1,It1,Rb1,Vebq1,Ig2,It2,Rb2,Vebq2

C
C *** If time is greater than or equal to tplot then:
C     Write out the anode voltage, gate voltage, anode current,
C     gate current, and charge at each time step, and plot
C     the device current and voltages. Otherwise, increment
C     the time and do another step.
C
      If(time .lt. tplot)then
      time=time+dltat
      return
      endif
C
C *** Define names for state variables in terms of the calling array.
```

```
C
      IL     =Y(1)
      Vcb1   =Y(2)
      Qte61  =Y(3)
      Vg1   =Y(4)
      Vcb2   =Y(5)
      Qte62  =Y(6)
      Vg2   =Y(7)
C
C *** Calculate functions of state variables for output quantities.
C
      call IGBTREC(IGBT1)
      call IGBTVeb (Qte61,Vcb1,Rb1,Vebq1)
C
      call IGBTREC(IGBT2)
      call IGBTVeb (Qte62,Vcb2,Rb2,Vebq2)
C
      Va= ( IL + (Vcb1+Vebq1)/Rb1 + (Vcb2+Vebq2)/Rb2 )
     &    *  Rb1*Rb2/(Rb1+Rb2)
C
      It1=(Va-Vcb1-Vebq1)/Rb1
      It2=(Va-Vcb2-Vebq2)/Rb2
C
      Vgg=Pulsgen(time,ton,toff,trise,trise,Vggon)
      Ig1=(Vgg-Vg1)/Rg1
      Ig2=(Vgg-Vg2)/Rg2
C
C *** Write output quantities to logical unit.
C
      write(outunit,10)Time-tplot,
     &                 Va,It1,It2,Vg1,Vg2,Ig1,Ig2
 10   format(8(1x,E10.4))
C
C *** Store normalized quantities for graphics output.
C
      iout=iout+1
      nplt=iout
      xax(iout)=time*1.0e6
      y1ax(iout)=Va
      y2ax(iout)=Vaa*2.0/Vggon*Vg1
      y3ax(iout)=Vaa+ Vaa/Vggon*Rg1*Ig1
      y4ax(iout)=It1*2*RL
      y5ax(iout)=Vaa*2.0/Vggon*Vg2
      y6ax(iout)=Vaa+ Vaa/Vggon*Rg2*Ig2
      y7ax(iout)=It2*2*RL
C
C *** Increment the integration time and decide if is final plot.
C
      time=time + dltat

      If (time .lt. tfinal)then
         return
      else
C
C *** Interactive graphics loop.
C
 99      continue
C
         call HOWPLT(0,1,1)
         call curv(nplt,xax,y1ax)
```

```
C
         call HOWPLT(0,1,3)
         call curv(nplt,xax,y2ax)
         call curv(nplt,xax,y5ax)
C
         call HOWPLT(0,1,7)
         call curv(nplt,xax,y3ax)
         call curv(nplt,xax,y6ax)
C
         call HOWPLT(0,1,4)
         call curv(nplt,xax,y4ax)
         call curv(nplt,xax,y7ax)
C
         call vg
         if(loopin().eq.1)goto 99
         stop
      endif
C
      END
C
C
C
C
C ***************************************************************************
C
C     Function to generate a single pulse.
C
C
      REAL function pulsgen(time,ton,toff,trise,tfall,Vggon)
C
      REAL Vgg,time,ton,toff,trise,tfall,Vggon
C
      Vgg=0.0
      If (time .gt. ton .and. time .lt. ton+trise)
     &     Vgg=Vggon*(time-ton)/trise
      If (time .ge. ton+trise .and. time .lt. toff)Vgg=Vggon
      If (time .ge. toff .and. time .lt. toff+tfall)
     &     Vgg=Vggon*(1.0-(time-toff)/tfall)
      pulsgen=Vgg
C
      RETURN
      END
```

NOMENCLATURE

A	Device active area (cm^2)
$A_{ds} \equiv A - A_{gd}$	Body region area (cm^2)
A_{gd}	Gate-drain overlap area (cm^2)
$b \equiv \mu_n/\mu_p$	Ambipolar mobility ratio
C_{bcj}	Base-collector depletion capacitance (F)
C_{dsj}	Drain-source depletion capacitance (F)
C_{ebj}	Emitter-base depletion capacitance (F)
C_{ebd}	Emitter-base diffusion capacitance (F)
C_{ebq}	Emitter-base capacitance (F)
C_f	External feedback capacitor (F)
C_{gd}	Gate-drain capacitance (F)
C_{gdj}	Gate-drain overlap depletion capacitance (F)
C_{gs}	Gate-source capacitance (F)
C_{ozd}	Gate-drain overlap oxide capacitance (F)
C_S	Snubber capacitance (F)
$D \equiv 2D_nD_p/(D_n + D_p)$	Ambipolar diffusivity (cm^2/s)
D_{ccs}	Carrier-carrier scattering diffusivity (cm^2/s)
D_n, D_p	Electron, hole diffusivity (cm^2/s)
I_f	Feedback current (A)
I_g	Gate current (A)
I_k	Tail size knee current (A)
I_k^τ	Tail decay rate knee current (A)
I_L	Load inductor current (A)
I_{mos}	MOSFET channel current (A)
I_{mos}^{sat}	MOSFET channel saturation current (A)
I_n, I_p	Electron, hole current (A)
I_{sne}	Emitter electron saturation current (A)
I_T	IGBT anode current (A)
I_T^{sat}	IGBT anode saturation current (A)
K_{plin}	MOSFET linear transconductance (A/V^2)
K_{psat}	MOSFET saturation transconductance (A/V^2)
$L \equiv \sqrt{D\tau_{HL}}$	Ambipolar diffusion length (cm)
L_L	Series load inductance (H)

n, p	Electron, hole carrier concentration (cm^{-3})
$\delta n, \delta p$	Excess carrier concentrations (cm^{-3})
n_{eff}	Effective base carrier concentration (cm^{-3})
n_i	Intrinsic carrier concentration (cm^{-3})
N_{scl}	Collector-base space charge concentration (cm^{-3})
N_B	Base doping concentration (cm^{-3})
P_0	Excess carriers at emitter edge of base (cm^{-3})
q	Electronic charge (1.6×10^{-19} C)
Q	Instantaneous excess carrier base charge (C)
Q_B	Background mobile carrier base charge (C)
Q_0	Built-in emitter-base depletion charge (C)
R_b	Conductivity modulated base resistance (Ω)
R_B	Snubber bleeder resistance (Ω)
R_D	Diode resistance (Ω)
R_f	Series feedback resistance (Ω)
R_g	Gate drive resistance (Ω)
R_{gon}	Turn-on gate resistance (Ω)
R_L	Series load resistance (Ω)
R_s	Device series resistance (Ω)
V_A	Device anode voltage (V)
V_{AA}	Anode supply voltage (V)
V_{bc}	Applied base-collector voltage (V)
V_{bi}	Built-in junction potential (V)
V_{cf}	External feedback capacitor voltage (V)
$V_{ds} = V_{bc}$	Applied drain-source voltage (V)
V_{eb}	Applied emitter-base voltage (V)
V_{ebq}	Emitter-base capacitor voltage (V)
V_{ebd}	Emitter-base diffusion potential (V)
V_{ebj}	Emitter-base depletion potential (V)
V_{gg}	Gate pulse generator voltage (V)
V_{gon}	Gate pulse voltage amplitude (V)
V_{gs}	Gate-source voltage (V)
V_r	On-state voltage at high gate voltage (V)

V_S	Snubber voltage (V)
V_{SS}	Snubber supply voltage (V)
V_T	MOSFET channel threshold voltage (V)
V_{Td}	Gate-drain overlap depletion threshold (V)
v_{nsat}	Electron saturation velocity (cm/s)
v_{psat}	Hole saturation velocity (cm/s)
W	Quasi-neutral base width (cm)
W_B	Metallurgical base width (cm)
W_{bcj}	Base-collector depletion width (cm)
W_{dsj}	Drain-source depletion width (cm)
W_{gdj}	Gate-drain overlap depletion width (cm)
x	Distance in base from emitter (cm)
α_1	Carrier-carrier scattering coefficient ($(\text{cm}\cdot\text{V}\cdot\text{s})^{-1}$)
α_2	Carrier-carrier scattering coefficient (cm^{-2})
β_{ss}	Steady-state common emitter current gain
$\beta_{tr,L}$	Clamped inductive load tail size
$\beta_{tr,V}$	Constant anode supply voltage tail size
γ	High-level injection coeificent
ϵ_{si}	Dielectric constant of silicon (F/cm)
μ_{eff}	Effective ambipolar mobility ($\text{cm}^2/\text{V}\cdot\text{s}$)
μ_n, μ_p	Electron, hole mobility ($\text{cm}^2/\text{V}\cdot\text{s}$)
μ_{nc}, μ_{pc}	Carrier-carrier scattering mobilities ($\text{cm}^2/\text{V}\cdot\text{s}$)
ϕ_n, ϕ_p	Electron, hole quasi-fermi potential (V)
τ_{HL}	Base high-level lifetime (s)
$\tau_b \equiv W^2/4D_p$	High-gain, high-level injection base transit time (s)

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11. ABSTRACT (A 200-WORD OR LESS FACTUAL SUMMARY OF MOST SIGNIFICANT INFORMATION. IF DOCUMENT INCLUDES A SIGNIFICANT BIBLIOGRAPHY OR LITERATURE SURVEY, MENTION IT HERE.)

The IGBT (Insulated Gate Bipolar Transistor) is a power semiconductor device that has gained acceptance among power electronic circuit design engineers for motor drive and power converter applications. These devices have the best features of both power MOSFETs and power bipolar transistors, i.e., efficient voltage gate drive requirements and high current density capability. When designing the circuits and systems that utilize IGBTs or other power semiconductor devices, circuit simulations are needed to examine how the devices affect the behavior of the circuit. However, the semiconductor device models available in most circuit simulators were originally intended to describe microelectronic devices and cannot adequately describe the characteristics of power devices. In this publication, a compact IGBT model suitable for incorporation in circuit simulators is described, and a circuit simulation program called INSTANT is presented that simulates the dynamic behavior of IGBTs within any external drive, load, and feedback circuit configuration. The INSTANT simulator solves the systems of differential equations (state equations) that describe each component of the circuit, where the equations for the individual components are coupled by the circuit configuration. The INSTANT software package is designed to provide the flexibility to change the external circuit configuration and model equations. The device and circuit parameters are also readily accessible, and the graphics output provides a real-time display of the waveforms as they are calculated. This publication also describes the automated measurement methods developed to extract the IGBT device model parameters from terminal electrical measurements. It is shown that unlike parameter extraction for microelectronic devices, the dynamic characteristics must be used to characterize the IGBTs and to extract the model parameters. This occurs because the devices exhibit non-quasi-static behavior and because the dynamic waveforms contain many features that isolate different physical mechanisms, whereas the physical mechanisms are convoluted in the relatively simple steady-state characteristics. The unique features of the IGBT electrical characteristics are explained using the model, and the procedures used to verify the IGBT model are given.

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