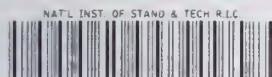NIST SPECIAL PUBLICATION **400-87**

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Semiconductor Measurement Technology:

A Programmable Reverse-Bias
Safe Operating Area
Transistor Tester

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A Programmable Reverse-Bias Safe Operating Area Transistor Tester

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Semiconductor Measurement Technology:
A Programmable Reverse-Bias Safe Operating Area Transistor Tester

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Abstract

The circuits and construction of a transistor turn-off breakdown tester are described. Principles of operation for various circuits in the tester are discussed, as well as those for the complete system. Construction notes are given with layout guidelines. Included are complete circuit schematics and details of construction of special parts used in the tester. Specifications and performance data are also given in this document.

Key words: Clamp circuits; converter circuits; drive circuits; fast-switching, high energy-circuits; inductive load switching; nondestructive measurements; power conversion; protection crowbar; reverse-bias breakdown; safe operating area; second breakdown; transistor; transistor-breakdown testing.

Disclaimer

1. INTRODUCTION

This Special Publication describes a tester that was built to address the need for testing the turn-off switching capability of power transistors. High-voltage power switching transistors are used in a wide variety of applications including such diverse fields as power conversion, motion control, and electronic ignition. A critical element for specifying the performance and reliability of these transistors is their turn-off capability. Most applications using high-voltage switching transistors require the transistor to turn off from a state of high-current conduction at low voltage with a load circuit that is at least somewhat inductive. Often the voltage rises to a high value before the current begins to fall, and there is a period of time when the transistor experiences a very high level of power dissipation. If a particular combination of current and voltage exceeds the switching capability of the transistor, it will break down and be destroyed. Furthermore, the switching capability of these transistors is a function of the drive conditions.

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This publication documents the plans and schematics for the National Institute of Standards and Technology's transistor turn-off tester, the RBSOA-2. This tester performs the same basic functions as an earlier tester built and documented in the late 1970s [1]. However, the new tester was developed to offer higher test currents and voltages, and it can be connected to a computer for making automated measurements. Some other important improvements over the older tester include voltage and current-breakdown sensing to greatly reduce susceptibility to false breakdown detections, a factor-of-three improvement over the old tester in the current removal rate for the protection circuit, and the addition of device test current as a settable parameter. Other testers have been built that incorporate somewhat different circuits and techniques for making transistor breakdown measurements [2,3].

Some experimental results obtained using the older tester developed at the National Institute of Standards and Technology are given in the literature [4,5].

2. SPECIFICATIONS

The following specifications describe the actual performance of the tester:

- Tests npn transistors, n-channel MOSFETs, and other devices that operate with a positive voltage applied to the output terminal that has higher impedance. (Opposite polarity devices can be tested with the addition of an appropriate inverting driver transformer referenced to the lower impedance output terminal. In this case, the lower impedance terminal is connected towards the positive voltage supply, and the output terminal that has higher impedance is connected to ground.)

- One-shot or repetitive test modes; 15-Hz test repetition rate in continuous repetitive mode, or 0.3-Hz maximum rate in the one-shot (manual or automated) mode

- Maximum test voltage: 2000 V

- Maximum test current: 100 A

- Peak test power: Up to 200,000 W

- Protection circuit:

    Current removal rate (averaged over 100 A): 2.5 A/ns

    Voltage slew rate: 200 V/ns

    Delay: 25 ns

    Time from transistor breakdown to remove 40 A: 30 ns

    Time from transistor breakdown to remove 100 A: 65 ns

    Technology: hybrid-vacuum tube/power MOSFET/SCR

- Base/Gate drive:

    Turn-on amplitude: 0 to 25.5 A in 0.1-A increments

    Turn-off amplitude: 0 to 25.5 A in 0.1-A increments or 0 to 2.55 A in 0.01-A increments

    On time: 0 to 255 μs in 1-μs increments

    Off time: 1 to 100 μs, 2-5-10 sequence

    Compliance voltage: ±4 to ±20 V

- Clamp voltage: 0 to 2000 V in 10-V increments

- Test device current: 0 to 100 A in 1-A increments

- Internal device supply voltage adjustable from 15 to 150 V

- Trigger outputs for both turn-on and turn-off pulses

3. PRINCIPLES OF OPERATION

This transistor turn-off tester was designed to make nondestructive breakdown measurements on npn high-voltage bipolar switching transistors and n-channel power MOSFETs. Some merged devices such as Insulated Gate Bipolar Transistors (IGBTs) can be measured also. These measurements are frequently called Reverse-Bias Safe-Operating-Area measurements (RBSOA). The RBSOA measurement is made by connecting the transistor under test in a common-emitter configuration with the collector connected to a voltage supply through a load inductor. The base is driven by a positive current source that turns the transistor on and causes current to build up in the load inductor. After a period of time, the forward base current is removed, and a reverse or turn-off base current is applied. After a storage time, the transistor begins to turn off, and the collector voltage rises as the load inductor continues to maintain a constant current. The collector voltage can either be clamped by a clamping circuit, or it can rise until the transistor breaks down. Sometimes the transistor will avalanche until the energy stored in the inductor is exhausted. Other times, the collector voltage will collapse with the transistor entering second breakdown, normally a destructive phenomenon. If the current and voltage can be removed fast enough after the voltage collapse, the transistor will not be destroyed or degraded. The most critical elements in a transistor RBSOA tester are the circuits that detect voltage collapse and remove current and voltage once the collapse is detected.

3.1 Block Diagram

Figure 1 is a block diagram of the tester. The device under test is connected to a voltage supply through load inductors. This connection is made to the high-impedance output terminal of the device under test, i.e., the collector of a bipolar transistor or the drain of a MOSFET. The base or gate of the device under test is driven by driver circuits that turn the device on and off with controlled levels of current that are adjustable in both duration
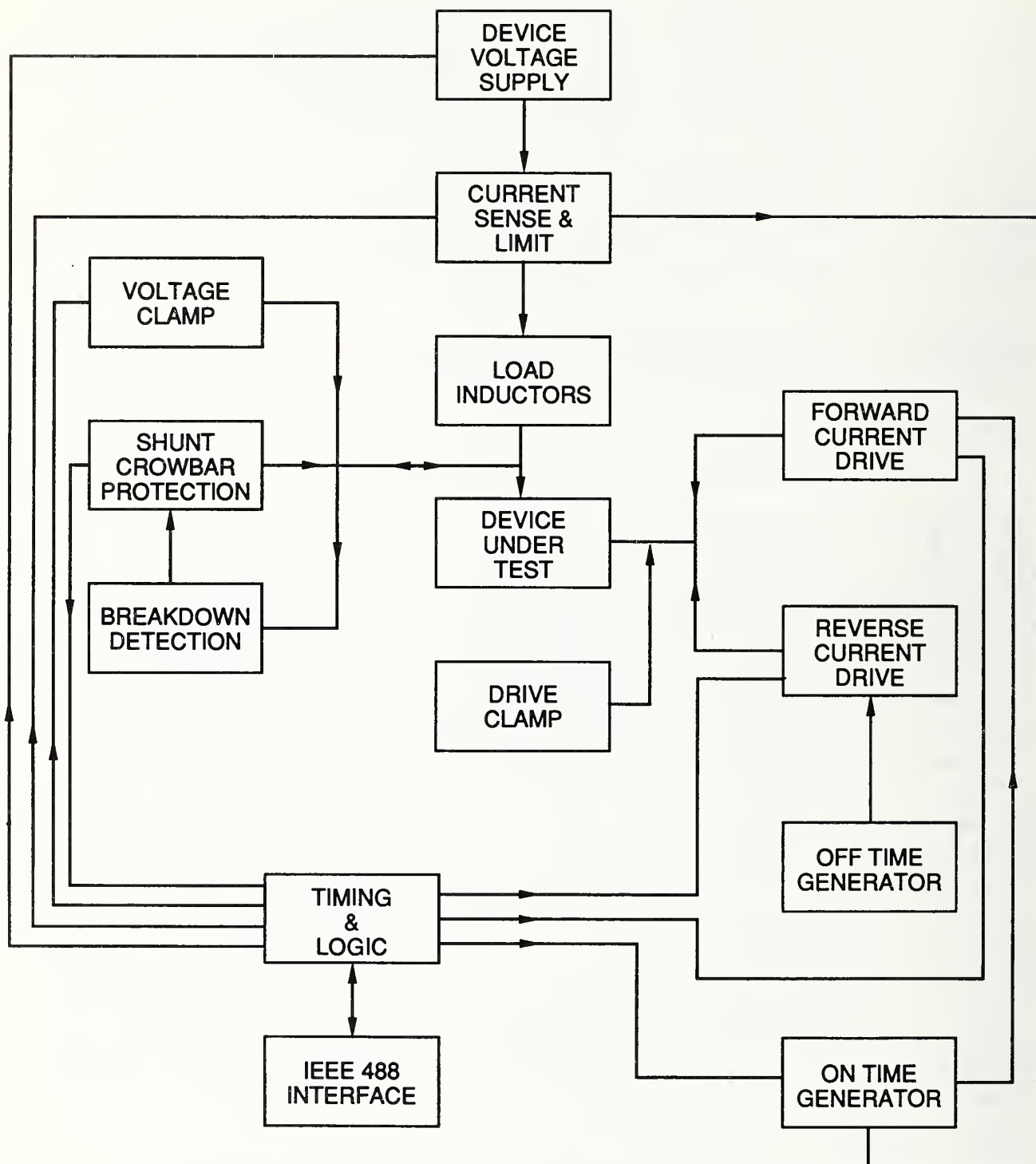
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Figure 1. Block diagram of the tester.

and amplitude. Voltage clamps can be set to limit the device voltages, both at the output terminal and the input terminal. The voltage clamp at the output terminal can be used to determine the limits of voltage that the device under test can withstand without breaking down. The shunt protection circuit is critical to the breakdown measurement, as it saves the device under test from destruction when breakdown occurs. Most of the parameters that determine the test voltages and currents can be set from the tester or remotely via a computer-controlled IEEE-488 bus interface [6]. The interface conforms to the ANSI-IEEE 488.1-1978 standard [6]. The functions that can be set by a computer include clamp voltage, on-time, forward current, reverse current, current limit, and one-shot test. The tester indicates a breakdown to the computer by flagging the service request line. The functions that are not controllable by the computer are the device supply voltage, turn-off time, drive clamp, reverse high-low range toggle, tally counter, internal or external device supply select, and the continuous (repetitive function).

When the tester is used without a computer, the various test parameters are set by the front-panel controls to the desired levels. These controls remain active at all times, even when a computer is being used. The locations of the front panel controls can be seen in figure 2, a photograph of the front panel of the tester.

3.2 Device Drive

Both the forward- and reverse-current drives can be set in 100-mA increments up to 25.5 A; in addition, the reverse drive can be set by a RANGE button to a range with 10-mA increments for special low-current tests. The button is only active when the reverse current is set to zero by rotating the REVERSE CURRENT knob counterclockwise, and this range cannot be set remotely. Both the forward and reverse drives are constant-current drives, and a clamp circuit provides for setting limits on the voltage. The nominal range of this clamp circuit is ± 4 V to ± 20 V, although fast transitions between the forward and reverse drives result in voltage overshoots caused by inductance and speed limitations in the clamping diodes. This clamp is mostly used to prevent base-emitter avalanche when turning off bipolar transistors.

The duration of both the forward and reverse pulses can be controlled independently. The forward, or ON-TIME, control is the more important as it determines, in part, how much current builds up in the load inductor and test device before the device is switched off. The reverse pulse need only be of sufficient duration to turn off the device under test. The actual "on-time" duration may be shorter than that selected by the ON-TIME control if the device current builds up to a value that exceeds the selected current limit. In that case, the actual on-time will be determined by the current-limit setting and will be displayed. Also, the on-time duration will be automatically adjusted to the shorter interval for subsequent tests. When looking at waveforms on an oscilloscope during repetitive tests, it is often desirable to adjust device current with the ON-TIME knob because the current can be raised and lowered with one knob, whereas current can only be lowered with the CURRENT LIMIT knob. Setting the CURRENT LIMIT knob to a high value assures
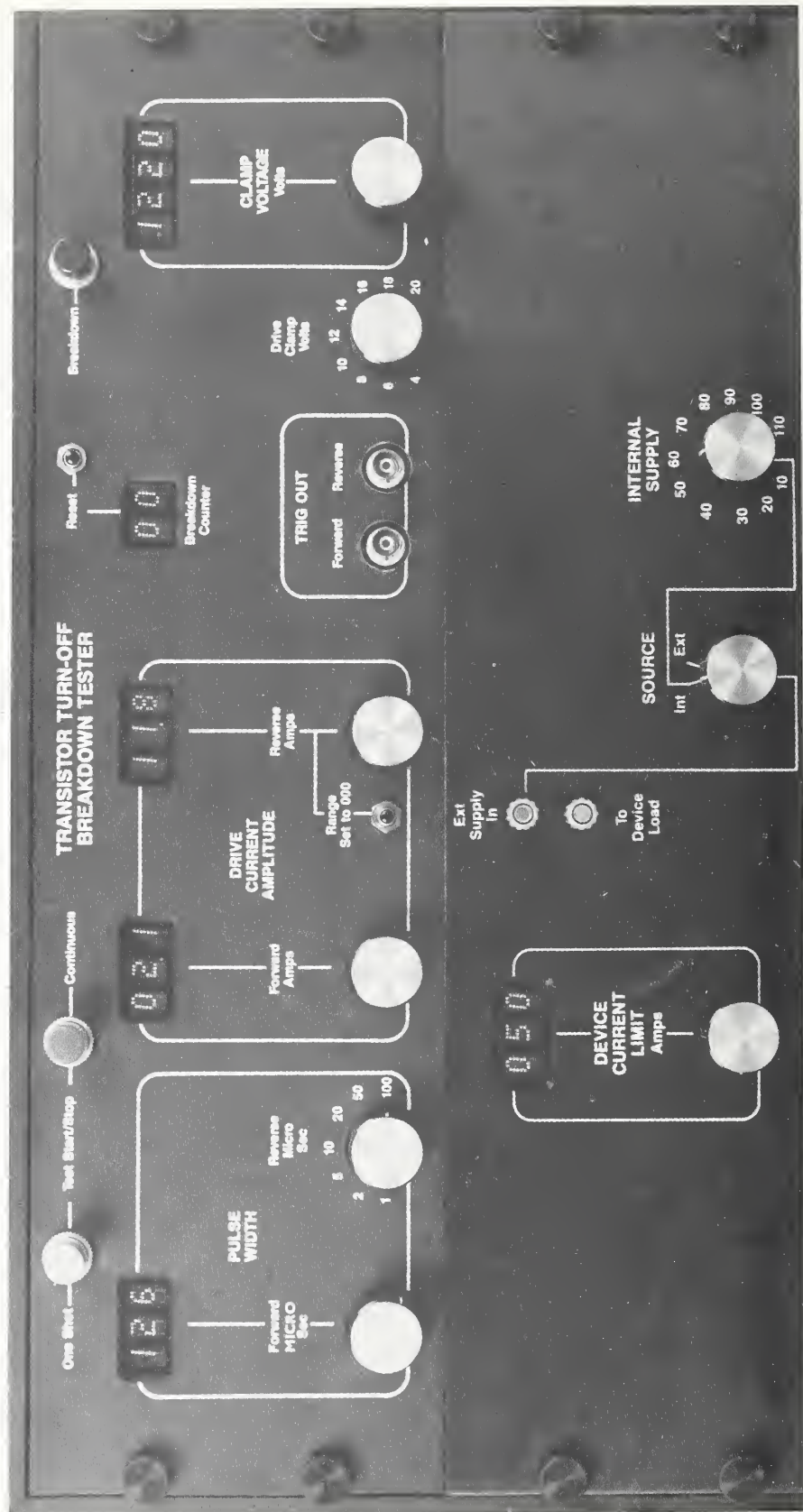
Figure 2. Front control panels of the tester.

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that the ON-TIME control can be adjusted without interference. Adjustment of device current by the ON-TIME knob provides finer current resolution at low currents than use of the CURRENT LIMIT control.

3.3 Special Breakdown Detection Circuit

The breakdown detection and high-speed shunt protection circuits sense transistor breakdown and divert current away from the device under test as rapidly as possible. The detection circuit uses a combination of voltage and current sensing to distinguish correctly between voltage collapse across the transistor caused by failure, and severe voltage overshoot of the clamp diodes, as these can look very much alike on an oscilloscope. Previous designs of breakdown detection circuits were prone to false indications of breakdowns.

3.4 Timing Circuits

Timing and logic circuits govern the proper sequence of operation of the circuits in the tester. There are two testing modes for operating the tester: a one-shot mode and a repetitive test mode. The one-shot mode, activated by pressing the ONE-SHOT button, causes the clamp voltage to ramp up to the set value. A gating signal is also provided to turn on an external voltage supply source for the device under test if such a supply is used. If the ON-TIME control is set to zero, the tester will hold in this initial state indefinitely; otherwise, a test will be executed about 2 s after the ONE-SHOT button is released. The test begins when the forward-current drive and the internal voltage supply for the device under test are turned on. When the device has been on for the amount of time specified by the on-time setting or when the device current has reached the limit set point, the on-pulse is terminated, and the reverse pulse is applied for the length of time specified by its setting. At the beginning of the reverse pulse, the clamp supply, internal voltage supply for the device, and gating signal for any external supply are turned off. All of these supplies are sufficiently slow that their outputs do not change significantly for the remainder of the test, and on the time scale of the test, appear to remain on.

The repetitive testing mode is activated by the CONTINUOUS button on the tester. In the repetitive mode, the device under test is turned on and off at about a 15-Hz rate. The clamp supply and the gating signal for an optional external voltage supply for the device remain turned on continuously. The internal device supply is only turned on during the forward or turn-on pulse. If a breakdown occurs, the protection circuit is activated, all supplies are turned off, and further testing stops. The repetitive mode is used most frequently when observing, with an oscilloscope, device turn-off for clamp voltage settings below those that would likely cause breakdown. It is then possible with the storage oscilloscope to capture a breakdown event once the clamp voltage is raised and a one-shot test is executed. Alternatively, the repetitive mode can be used to measure breakdown voltage directly by allowing the user to turn up the clamp voltage slowly until a breakdown occurs.

Whenever a breakdown occurs, the BREAKDOWN LIGHT is turned on and the BREAKDOWN TALLY COUNTER is incremented. The seven-bit counter counts up to 63 and starts over at 00. A RESET button is provided.

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Outputs are provided for oscilloscope triggering. The FORWARD TRIGGER output provides a pulse at the beginning of the turn-on pulse to the device, and the REVERSE TRIGGER provides one at the beginning of the turn-off pulse to the device.

3.5 Oscilloscope for Observing Breakdowns

During transistor breakdown tests, a voltage clamp can be imposed to prevent the collector (or drain for a MOSFET) voltage from going beyond a certain point. This clamp can be used to prevent transistor breakdown for the purpose of capturing an actual breakdown on an oscilloscope once the clamp voltage is raised sufficiently to force a breakdown in the transistor under test. To capture a breakdown with a storage oscilloscope, a sufficiently low clamp voltage can be used to prevent transistor breakdown while setting up the oscilloscope and observing the switching waveforms with no breakdown. Then, to force a breakdown, the clamp voltage is raised until a breakdown occurs. Generally when making breakdown tests, the maximum voltage that the device can withstand before collapsing is measured with a storage oscilloscope or fast digitizer. Alternatively, the clamp voltage can be incrementally raised until breakdown occurs to determine safe transistor switching limits. It should be noted, however, that it is possible to have several hundred volts of voltage overshoot in clamping action when the device turns off very quickly, thus making this a poor method for determining the switching limits when fast turn-offs are present.

4. CIRCUIT DESCRIPTION

Schematic numbers are referenced in the following circuit descriptions in a nonsequential order because of the way that the schematics are cross-referenced. The numbers in the diamond-shaped boxes on the schematics refer to connection points on correspondingly numbered schematics.

4.1 Main Power Supply

The main power supply is a 500-W parallel resonant half-bridge circuit that has a resonant frequency of 50 kHz. Schematic 15 shows the circuit for the primary side, and schematic 14 gives the secondary side. A 120-V line voltage is converted into approximately 320 V dc by rectifier block MDA2506 of which only the top two diodes are active in the voltage doubler configuration used. The triacs 2N6075A and SC250M3 form a soft-start circuit that limits in-rush current and protects the power MOSFETs by delaying application of power during the power-up sequence until their gates are receiving sufficient drive signal to keep them out of their linear region. An L-R oscillator (2N5682, 2N5680, L1501, T1501, and the 430-Ω resistor) operates the soft-start circuit and drives the gates of the MOSFETs with square waves. During the power-up sequence, the C2A neon lamp and the lamp-current pulse the oscillator. Once it is oscillating, the 2N3439 prevents further pulsing by the lamp. The amplitude of the oscillator builds up slowly as the two 1000-μF capacitors are charged through the 3-kΩ resistor. When the oscillation reaches sufficient amplitude, the 2N6075A sensitive gate triac is turned on to permit power to be applied to the main filter capacitors and power MOSFETs through a limiting 10-Ω resistor. This main power supply also provides a booster current through the 4-kΩ resistor to bring the amplitude of the

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Schematic 15. Main Power Supply – Primary Side.

Schematic 14. Main Power Supply – Secondary Side.
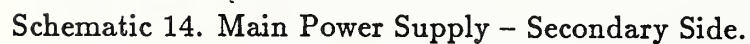
oscillator up further, guaranteeing that the main triac SC250M3 is turned on so that the 10-Ω limiting resistor and 2N6075A triac are shorted out. This booster current prevents the destruction of the smaller triac and the 10-Ω limiting resistor in the event of low line voltage. The MOSFETs drive a resonant tank circuit consisting of the 135-μH inductor (L1502) and the two 0.0047-μF capacitors on the secondary of the power transformer (T1401).

The output voltage of the power supply is determined by the frequency of the oscillator. The closer this frequency is to the resonant frequency of the tank network, the more power will be delivered. Regulation is achieved by controlling the frequency of the oscillator with L1501, which is a control reactor, and appropriate feedback circuits.

The $\pm$500-V supplies contain a large amount of energy storage, much more than is actually needed by the circuits that they supply. This high demand on the power supply at power-up actually aids the soft-start sequence by momentarily effectively shorting the output of the supply. With a shorted output, the resonating capacitor is shorted out, and little power is delivered to the load. Because the power cannot be delivered to the load, energy stored in the resonating inductor is returned to the main filter capacitors through the antiparallel diodes in the MOSFETs, creating less demand for power during the power-up sequence. As the capacitors on the secondary side of the transformer become partially charged, the power delivered from the resonant tank network increases until the capacitors become fully charged. When the capacitors become fully charged, the frequency is driven above the resonant frequency of the tank by the feedback error detection circuits and the control reactor, and the power transferred through the resonant tank network to the load is reduced to actual demand.

The power transformer (T1401) operates with 12 V rms per turn, and this voltage, when rectified and filtered, becomes about 16 V per turn. Some circuits in the tester require voltages that are not an integer multiple of 16 V, and T1402 and T1403 are used to derive some of these other voltages. The dual seven-turn winding on T1402 subtracts voltage from the center-tapped six-turn winding of the main transformer to yield $\pm$40 V dc. Some left-over power is used to produce 2 V dc, and the remaining power is dumped into the 15-V supply. If there is more remaining power than can be used by the 15-V supply, T1403 is used to return the excess to the rectified mains, and thus clamp the 2- and 15-V supplies. This clamping action becomes important when the load demand on the $\pm$40-V supply is high.

4.2 Internal Device Power Supply and On-Board Power Converter Circuits

Each of the sub-panel circuit boards contains an on-board power converter to supply power to the logic circuits on that board. These converters are buck-type regulators that run on 15 V dc supplied by the main power supply. Schematics 1 and 2 each show one of these regulators. The 2N6437 and MUR1560 diode are mounted together on a small, free-standing heat sink capable of dissipating about 3 W. Because of noise considerations, free-standing heat sinks are recommended, as opposed to chassis or frame-mounted ones,
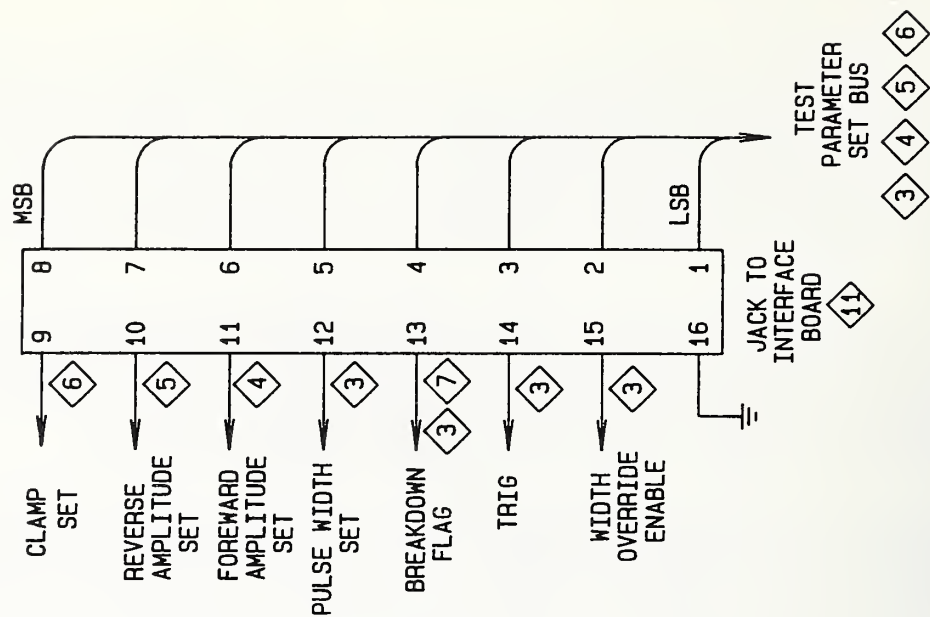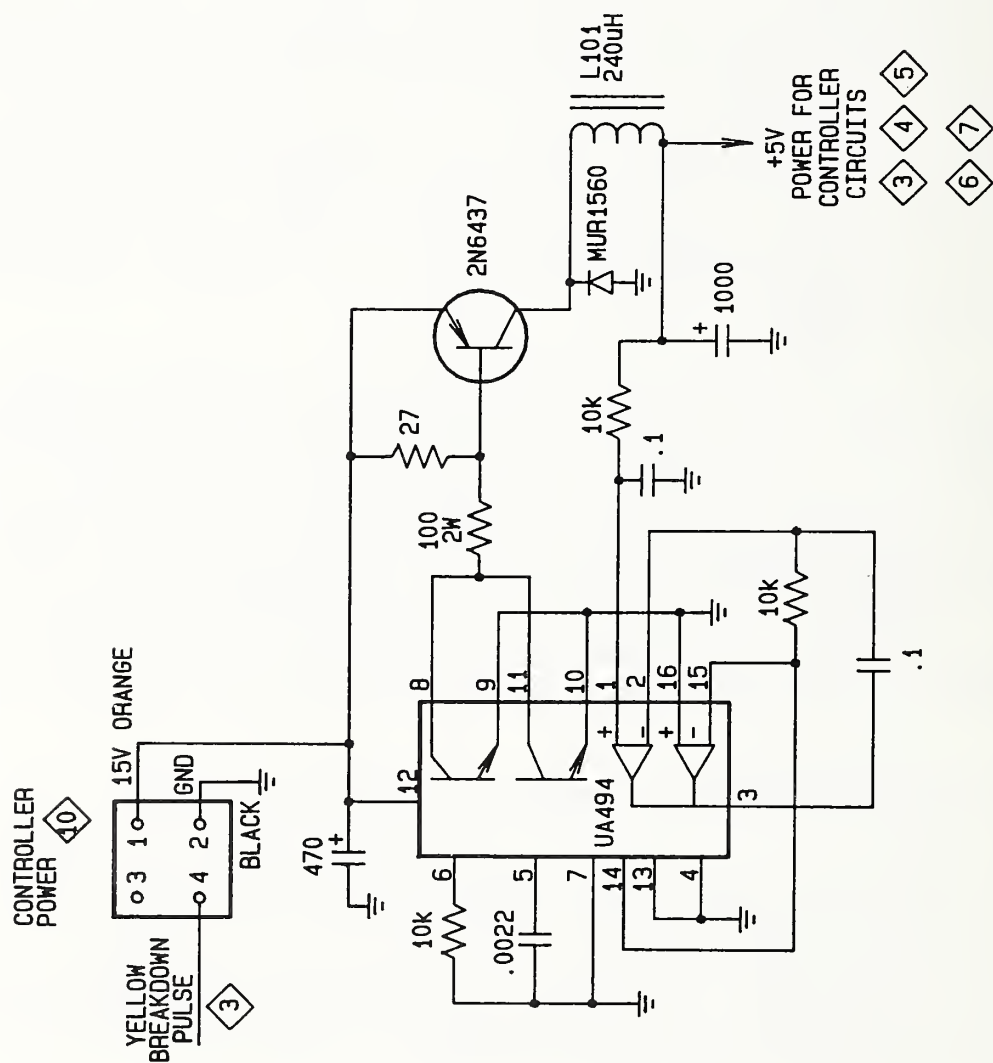
Schematic 1. On-Board Power Converter for Controller Circuits.

Schematic 2. Internal Power Supply for Test Device.

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with insulators for all the transistors in this apparatus that are used in switching type applications. The μA494 integrated circuit is a pulse-width controller.

Also given in schematic 2 is the circuit for the internal device power supply which can supply power to the device under test. Provision is also made to use an external supply, if desired. The internal supply is only gated-on during the Forward or On-Time cycle. This supply is a fly-back power converter which is adjustable from 15 to 150 V, and contains both instantaneous and average current limits to protect the power MOSFET, which is mounted on a heat sink capable of dissipating about 6 W. The output switch consists of ten parallel Insulated-Gate Bipolar Transistors with limiting resistors in the emitter circuit of each transistor. This configuration limits the output current to 400 A in the event of a shorted output, and permits about 100 V at 100 A to be supplied to the test transistor under pulsed conditions. T203 is a current-to-voltage transformer used to measure the supply current for the current limit circuits.

4.3 Clamp Supply

The clamp supply is a two-quadrant switching amplifier that can source and sink current for positive voltages. The amplifier can deliver a power output of up to ± 60 W, or ± 30 mA at up to 2000 V. Negative power represents power absorbed by the amplifier (negative current, positive voltage), and most of this power is not dissipated as heat, but converted back to the rectified power mains.

When a transistor is being tested and the device voltage rises above the clamp voltage, the current through the load inductor is diverted from the device under test into the clamp supply. In order to minimize voltage overshoot, the clamp supply must have a very low impedance for high-current, short-duration pulses fed into it while the voltage of the device under test is clamped. A low-inductance, 25-μF oil-filled capacitor rated at 2000 V is placed at the output of the clamp supply, physically located as close to the device under test as possible. The power-handling capability of the clamp supply has to be sufficiently high to be able to charge and discharge this clamp capacitor in a reasonable amount of time in order to make automation of this circuit practical, and a considerable amount of power must be removed as a result of the clamping action when repetitive testing is done.

Schematic 13 is a diagram for the clamp supply. The digital-to-analog converter (integrated circuit) DAC-08 converts eight bits of input to a current which is combined with a feedback signal from the output of the clamp supply to generate an error signal that drives the positive current output half of the supply. The digital-to-analog converter is configured to produce a resolution of 10 V per step. Numerical inputs 0 to 200 produce output voltages from 0 to 2000 V, whereas numerical inputs 201 to 255 are disallowed by the clamp controller. The current-sourcing portion of the supply is a half-bridge, quasi-resonant power converter with a voltage multiplier at the output. The power MOSFETs are mounted on a heat sink capable of dissipating about 20 W. L1302 is the resonating inductor, and is wound with litz wire to reduce heating due to skin and proximity effects. The 0.0047-μF capacitor on the secondary of T1307 is the resonating capacitor, and is a polypropylene type with a 1600-V rating. The 5-μF capacitor in series with L1302 is a dc-

Schematic 13. Clamp Voltage Supply.

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blocking capacitor, and is a high-current polypropylene type rated at 200 V. The 0.047-μF capacitors in the voltage multiplier are 1200-V polypropylene types. The capacitors in the feedback network have 600-V ratings.

The current-sinking portion of the clamp supply is a resonant power converter that is self-oscillating at a resonant frequency of about 110 kHz. On a dc basis, this circuit behaves like a constant-current sink from the plate of the top tube, although on an ac basis, the current waveform is a half sinusoid for half of the time and zero current for the other half of the time. The waveform at the input to resonating inductor L1301 is a square wave with an amplitude that scales with the clamp voltage. The resonating capacitor is actually parasitic capacitance in L1301 and T1302. The secondary voltage of T1302 is rectified and returned to the rectified power mains. The amount of current returned is proportional to the clamp voltage. T1303 is a feedback transformer which drives the power MOSFET, which in turn drives the tubes through T1304 to complete the oscillation loop. The MOSFET has a small clip-on heat sink. It is important to minimize the parasitic capacitance to ground at the circuit node where the two tubes join, as well as the capacitance between the heater for the top tube and ground. The driver winding in T1304 for the top tube and the heater winding in T1301 for the top tube are made with wire-wrap-type wire with the turns bunched together and fed through a piece of Teflon* tubing to separate them physically from the other windings on those transformers. These windings must float on top of a square wave that has an amplitude of up to 2500 V, peak-to-peak. Stray capacitance at the cathode and heater of the top tube translates into substantial power loss as this high voltage is switched at a high frequency. Care must be exercised in fabricating L1301 and T1302, as about 3000 V is present across these windings. Both L1301 and T1302 are wound with several layers of Teflon tape between each winding layer to give a high-voltage breakdown capability and a somewhat lower parasitic capacitance. The cores of both L1301 and T1302 are floating, and lead length is short. T1303 is physically located to result in the shortest possible primary lead length; the lead length for the secondary is much less important.

4.4 General Control Architecture

Many of the parameters that need to be set on the tester can be set by front panel controls as well as remotely by computer. The value of each of these parameters is defined by an eight-bit word which is stored in a pair of CMOS 4029 four-bit counters. The binary number stored in each pair of counters is converted to BCD format by the 74185 TTL chips (which require the 74902 buffer chips to interface the CMOS logic to TTL logic) and displayed by HP 5082-7300 integrated circuits which incorporate the BCD to seven-segment conversion function. The value of a test parameter can be loaded into a pair of counters from either a TEST PARAMETER SET BUS which is computer-driven, or from a rotary optical encoder which is mounted on the front panel of the tester. There is an optical encoder for each of the major parameters that affect the tests, along with the counter pairs and displays. The optical encoders are of the incremental type and produce 360 pulses per revolution. A 4029 counter is used to divide the 360 cycles by eight to

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*Teflon is a trademark of DuPont.

yield 45 increments per revolution for the various parameters that need to be set. It takes slightly over five revolutions to cover the 256 possible increments for each test parameter, with the exception of the clamp voltage, where only 201 are allowed. The 4013 chip is used to decode direction of rotation from the quadrature output that the optical encoder provides. The remaining assortment of AND and OR gates implement the stops for the rotary encoder. For all of the functions except the clamp supply, the stops are at count 0 and count 255, whereas the clamp has stops at count 0 and count 200. Much of the tester control circuitry is repeated for the various parameters that need to be set on the tester. Schematics 3, 4, 5, 6, and 8 contain portions that are mostly repetitive, but some have minor changes.

4.5 Forward Pulse-Width Controller

The forward pulse-width diagram is given in schematic 3. This circuit contains all of the various elements that govern the timing operation of the tester, including start test buttons for one-shot or repetitive testing, pulse-width control with clock, current-limit interrupt, forward pulse gate and trigger, and reverse trigger.

The controller generates pulses of widths from 0 to 255 μs by comparing an eight-bit number stored in a pair of 4029 counters with the status of a free-running clock. The clock consists of a 4001 oscillator and two 74LS393 counters. The comparison is done by three, four-bit comparator chips, including one 74LS85 TTL circuit and two 74C85N circuits. In the original construction of the controller, all of these chips were CMOS for reasons of improved noise immunity; however, the counters and first-stage comparator had to be changed to TTL because the CMOS devices were not fast enough. In principle, only two comparators and one eight-bit counter are needed to generate the required pulse widths. The additional counter and comparator used in this circuit implement the large dead time, so that the maximum duty factor is limited to 1/256. The $A > B$ output from the final comparator stage is the forward pulse which determines the length of time that the transistor under test is turned on. The $A = B$ output from the comparator momentarily becomes true at the end of the forward-current pulse, and this signal is used to trigger the reverse-current pulse generator which controls the turn-off signal for the transistor under test. If the logic level required to start the test is "true," then the forward pulse is passed on to the forward-drive amplitude controller as a gating signal, as well as to a scope trigger output circuit.

The logic level that permits a test to begin can be set "true" by either the CONTINUOUS test button, the ONE-SHOT button, or the trigger line which is computer-activated. The logic level is set "false" by either a breakdown pulse signal that indicates a breakdown has occurred or the expiration of a one-shot window in the single-test mode. Regardless of which input is used to start the test, there is a delay of about 2 s in test execution which gives the clamp voltage time to settle. This delay is generated by the 4024 counter. When testing is done in the repetitive mode, the delay occurs before the first test, but not in subsequent tests.

Schematic 3. Forward Pulse-Width Controller.

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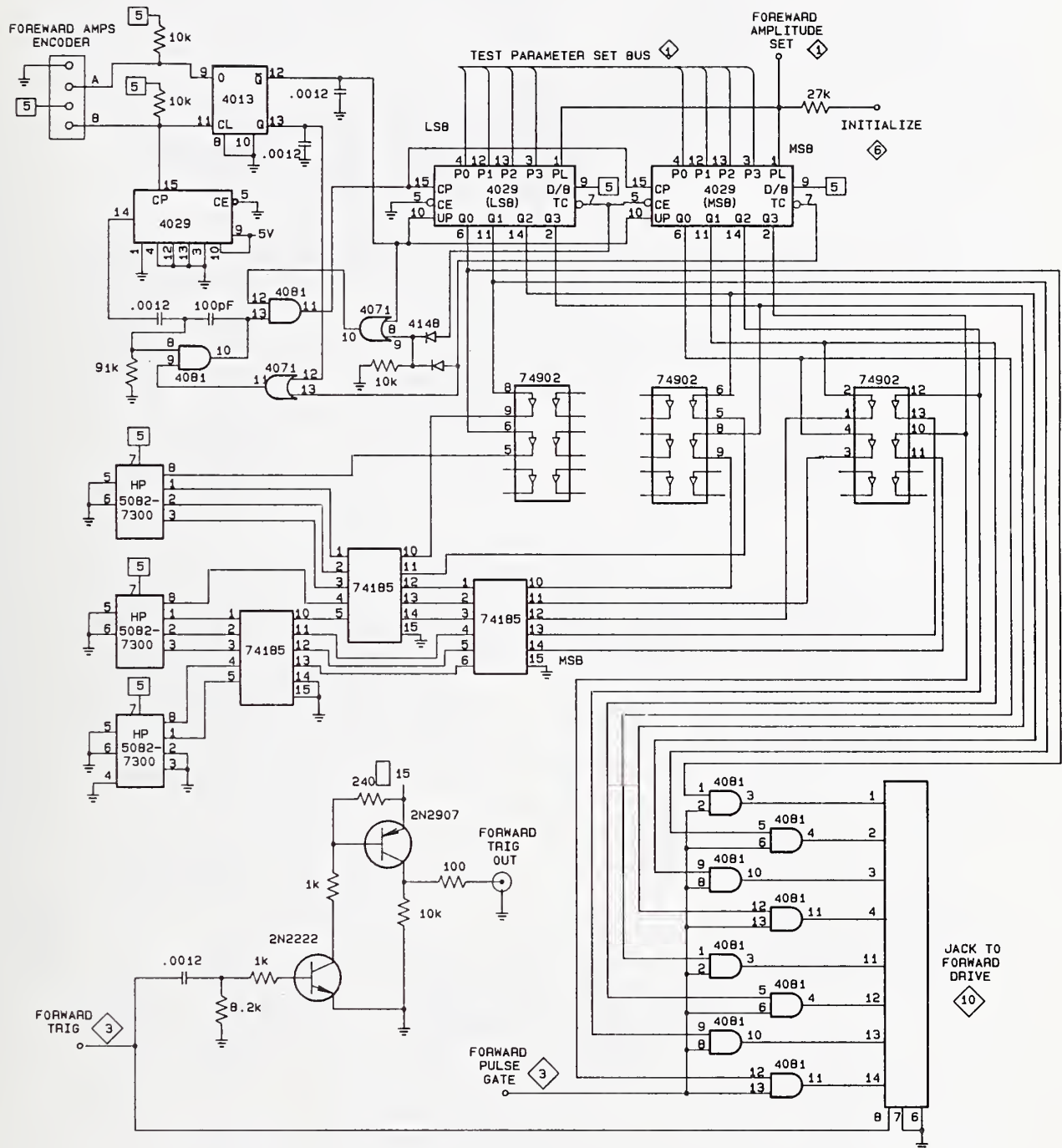
Schematic 4. Forward Drive Controller.

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Schematic 5. Reverse Drive Controller.
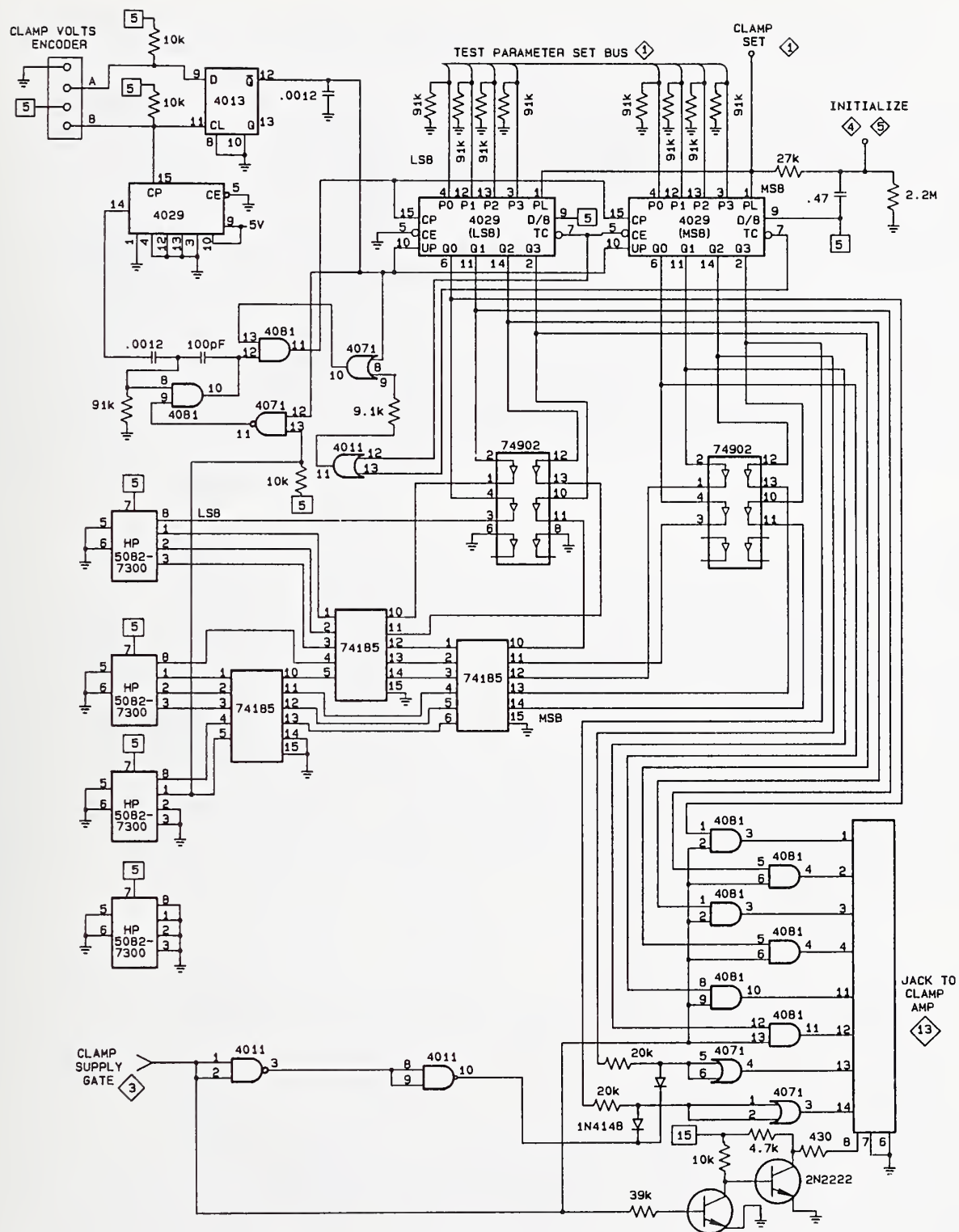
Schematic 6. Clamp Voltage Controller.

Schematic 8. Current Limit Controller.

The count for the 2-s delay will not start until the ONE-SHOT button is released, and the delay count will be reinitiated if the button is pressed again before the test executes.

If the forward pulse width is set to zero and any of the start inputs are activated, the tester will remain in a holding state as if the ONE-SHOT button were pressed but not released. Resetting the forward pulse width to a nonzero value will allow the test to execute. A yellow indicator (located inside the ONE SHOT button) lights during the 2-s delay regardless of which input activates the testing sequence. The CONTINUOUS button has a green light inside which is lit during repetitive testing. This button is pressed to start repetitive testing and pressed again to stop testing.

When the transistor under test breaks down, the protection circuit fires and sends a "breakdown" pulse signal to the controller which interrupts testing, lights the red breakdown light, sends a pulse to the breakdown tally counter, and flags the service request line of the computer interface circuit in order to tell the computer that a breakdown has occurred. When testing is interrupted, any forward or reverse pulse is terminated, and the clamp supply and the device supply are turned off.

4.5.1 Modifying the On-Time Period Automatically

A current-limiting feature in the tester terminates the forward or turn-on pulse if the current in the device under test reaches a set-point value. When the current-limit detector is activated, the 4034 bus register is enabled, and the clock is stopped. The status of the clock is transmitted to the loading ports of the 4029 counters, and the parallel load (PL) line is pulsed high so that the previous pulse-width byte is replaced with a new byte that describes the actual pulse width at the moment the current exceeds the limit set-point. The forward pulse is terminated as the $A > B$ comparator output becomes false, the $A = B$ output becomes true, and the reverse pulse generator circuit is triggered. The PL line goes low, followed by the width-override enable line, and the clock is allowed to resume operation. The new forward pulse width is thus stored by the controller for subsequent tests.

4.6 Clamp Controller

The clamp-voltage controller receives an input from either the panel-mounted optical encoder for the clamp voltage setting or from the TEST PARAMETER SET BUS which is accessed by a computer. The controller stores the input as an eight bit-word in a pair of counters in a manner similar to that of the pulse-width controller. The circuit for the clamp controller is given in schematic 6. The output of the controller is an eight-bit word which is sent to the clamp supply. This word is given the value of that stored in the counters whenever the clamp supply is gated on by the pulse-width controller, and it is given the value zero when the gating signal is false. The clamp supply is gated "on" about 2 s before one-shot tests, and during the forward pulse to the device under test. The supply remains on during repetitive testing. The gating signal is also brought out through a two-transistor buffer amplifier and made available for controlling an optional external device power supply.

The byte stored in the counters is set to zero at the time of power-up using an R-C network. This network is shared with circuits that control the drive amplitudes for the device under test.

The clamp-voltage setting is shown on a four-digit display. The voltage is settable in 10-V increments, up to 2000 V. The least significant digit is hard-wired to read zero.

4.7 Forward Drive Controller

The forward drive controller, shown in schematic 4, affects the amplitude of the forward turn-on pulse which is applied to the device under test. This circuit stores an eight-bit word which represents the amplitude of the forward pulse in 0.1-A increments from 0 to 25.5 A. The forward-pulse gate signal from the pulse-width controller circuit is used to gate the eight-bit word to the forward drive circuit. As for other functions in the tester, the eight-bit word parameter is stored in a pair of counters which are loaded either with a front panel control or from the TEST PARAMETER SET BUS under computer control.

4.8 Reverse Drive Controller

The reverse drive controller circuit is given in schematic 5. This circuit takes a "reverse" trigger pulse from the forward pulse-width controller and uses it to trigger a 74121 monostable multivibrator. The multivibrator generates pulse widths that are adjustable with a front panel switch in seven fixed durations from 1 to 100 μs. This pulse then gates an eight-bit word, that represents reverse pulse amplitude, to the reverse drive circuit in the same way as for the forward pulse. The eight-bit word for amplitude normally represents reverse or turn-off current for the device under test in 0.1-A increments up to 25.5 A. However, there is also a low current range which changes the representation to 0.01-A increments with a maximum current of 2.55 A. This range change is activated by a push button toggle, and the range can be changed only when the eight-bit word describing amplitude is set to zero. The decimal point on the display is shifted by the toggle action; however, the actual range selection is done by changing a reference voltage in the reverse drive circuit.

The amplitude of the reverse trigger pulse is increased to about 15 V by the two-transistor amplifier, and the trigger pulse is made available for scope triggering. A large amplitude scope trigger pulse is an advantage in preventing false scope triggering, as the triggering sensitivity on the scope can be reduced.

4.9 Forward Drive Amplifier

The forward drive amplifier circuit is given in schematic 10. The forward drive amplifier converts the eight-bit word from the forward drive controller into a constant-current output that drives the device under test to its on-state. The amplifier remains digital throughout, and the conversion to analog is done at the output where all of the digital current sources for the eight bits are summed. Many parallel transistors are used for the most significant bits. Each transistor conducts slightly less than 0.5 A when turned on and, given the short duty cycle, requires no heat sink. The output transistors chosen have nearly their

Schematic 10. Forward Drive Amplifier and D to A Converter.

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maximum gain at 0.5 A in order to maintain accurate current sourcing. The parallel configuration also yields high speed, although the output capacitance is high.

All of the collectors of the output transistors are connected to a 1-in. wide strip of double-sided circuit board that acts as a transmission line. The collectors are connected to one side, and the ground return which goes to the common (emitter or source) terminal of the device under test is connected to the other side. There are six 470-μF capacitors that are distributed along the length of the strip that bypass the power supply to the ground side of the board.

A bipolar clamp circuit limits the compliance of the output to chosen voltages between ±4 and ±20 V. Separate clamps which are a combination of active and passive circuits using Schottky-type diodes act on positive and negative overvoltages. The set-points for the positive and negative clamp voltages are symmetric about zero.

4.10 Reverse Drive Amplifier

The reverse drive amplifier circuit is given in schematic 9. This circuit is similar to that for the forward amplifier, except that it is the complement and sinks rather than sources current. The output of the reverse drive amplifier provides the turn-off drive for the device under test and is combined with the output of the forward drive amplifier.

The reverse drive amplifier has two current ranges which are determined by the "B" voltage that is developed at the drain of the 8N100 MOSFET. Normally, the "B" voltage is 12 V positive with respect to the −40 V supply to provide the normal high-current range. When the low-current range is selected, the "B" voltage is changed to about 1.2 V positive with respect to the −40 V supply.

4.11 Protection Circuit

The design and layout of the protection circuit determines how successfully devices can be tested without being degraded, as this circuit must detect device breakdown and remove the current in as short a time as possible. The protection circuit contains a high-speed crowbar which, when fired, connects the device end of the load inductor, which is supplying the test current, to a large negative voltage in order to divert the current away from the device quickly. A large negative voltage is used to overcome the parasitic inductances that separate the crowbar and the device under test more quickly.

4.11.1 Tester Box Assembly

Schematic 12 is a diagram of the protection circuit. This portion of the tester is hard-wired in the tester box to give the most flexibility for constructing wide copper conductors, ground planes, and transmission lines. This portion of the tester also contains physically large components, such as the clamp capacitor C1202, that need to be well supported mechanically and be close to the device under test and other protection circuit components. The power line input and line filter are shown on this drawing rather than on the power

Schematic 9. Reverse Drive Amplifier and D to A Converter.

Schematic 12. Crowbar Protection and Breakdown Sensing – Mainframe.

supply drawing because they are physically mounted on the tester box, and the power supply is a subassembly.

4.11.2 Crowbar Circuit

The crowbar uses 16 type 6LF6 vacuum tubes which are connected in parallel with a group of four series-connected SCRs. The effective cathode of the SCR string is connected to a momentary latching network that includes L1203 which is a physically large 40-μH inductor with a saturation current of 100 A. The crowbar uses the tubes for the first 300 ns, after which the SCRs take over the crowbar current. The tubes are very fast, but can conduct high plate current (in this case, 10 A each) for only a short period of time, while the SCRs turn on much more slowly, but can conduct the large current for a much longer period of time. The SCRs are fired from the cathode of one of the tubes through current divider transformer T1203.

Vacuum tubes were chosen for the design of the crowbar because of the combination of voltage and speed required for this circuit. The stand-off voltage required for the crowbar switch is 2600 V, and power gain is needed into the 100-MHz region.

It is important to minimize the parasitic capacitance at the collector or drain of the device under test in order to minimize snubbing, and a string of four reverse-biased diodes separates the device under test from the crowbar. Parasitic capacitance at the collector or drain causes a reduction of device current during the voltage rise portion of the turn-off, and a false indication of the switching capability of the device can be obtained. Parasitic capacitance also stresses the device when it breaks down. An additional four diodes separate the crowbar from the clamp capacitor (C1202) which is charged to the clamp voltage. Diodes are used in groups of four to obtain the required 2000-V capability. These two groups of diodes make up the clamp diode, although the chain is broken by the one-turn primary of current-sensing transformer T1201 which has a negligible effect on the clamping or crowbar action. An additional group of four diodes, in series with L1202, clamp the output of the crowbar to zero after a short negative voltage overshoot that speeds up the current diversion when the crowbar fires. A string of 91-kΩ resistors applies the clamp voltage to the crowbar to assure that the diodes that separate the device under test from the crowbar are reverse biased to the maximum extent possible, in order to minimize the capacitive loading to the device by the crowbar. The string of 1.5-MΩ resistors with the neon bulb is simply an indicator that the crowbar circuit is working properly, and the bulb is turned off completely when there is no leakage. If high-voltage leakage is present, the bulb will be lit when the clamp voltage is increased. An analog voltmeter indicates the actual clamp voltage, whereas the digital display associated with the clamp controller circuit indicates the set clamp voltage which is only gated on for tests.

The breakdown detection is done with a combination of voltage and current sensing, an improvement over the voltage derivative method that is commonly used. This detection circuit has a very high immunity to false triggering on clamped voltage overshoot. It is not uncommon to have clamped voltages overshoot by 300 V or more for fast-switching devices at high current, and the detection circuit can discriminate between such transients and

actual breakdown transitions of 140 V (or less if the clamp is active). The voltage sensing is done by coupling the device under test to the cathode of one-half of a 6BX7 tube through a 25-pF capacitor. The other half of the tube is used as a diode for optimum detector action. Current-sensing transformer T1201 develops a secondary voltage proportional to the clamp current, and this voltage is fed to the grid of the tube. The tube is thus connected in a fast differential cascode configuration. When the device under test does not break down but rather has its voltage clamped, the device voltage may overshoot the clamp voltage and make a negative transition as the clamp begins to act. This transition would improperly fire the crowbar were it not for the increasing clamp current which causes the grid of the tube to be driven negative, and thus the firing is blocked. In the event that a device begins to be clamped, but breaks down before all of the current is diverted, the clamp current will reverse because the clamp diodes need time to recover, the grid will be driven positive, and the crowbar will fire, possibly before the device voltage can collapse.

The output from the 6BX7 is coupled through a gate-drive transformer to a source follower MOSFET. The gate transformer parasitic inductance, together with the gate capacitance, is responsible for the bulk of the delay in the firing of the protection crowbar circuit, about 15 out of the total 25 ns. The gate transformer T1202 is physically small and has four parallel secondaries with short leads. A 20-to-1 turns ratio is optimum, determined by experimentation. The primary voltage pulse peaks at about 500 V at 0.5 A, providing up to 10 A of secondary current which is split between the gate and the protecting gate clamping diode. As the MOSFET turns on, its source terminal goes high, with a transition of about 600 V. The source remains high for a much longer period of time than the gate pulse that drives the MOSFET. The source terminal of this MOSFET is directly coupled to the gates of three more paralleled MOSFETs which are also source followers. They, in turn, drive the 6LF6 crowbar tubes. Each tube is driven with about 600 V at 2 A for about 300 ns. The time is determined by the bypass capacitors on the drains of the MOSFETs. The drive to the tubes is split between the grid and the screen. This unique way of driving the tubes allows them to be completely cut off with about 2600 V across them, but turned on hard on demand. When off, the grids and screens are fixed-biased 50 V negative with respect to the cathodes, and the cathodes are 580 V negative with respect to ground.

The plates of the 6LF6 tubes are each connected to a large copper plate that surrounds the bases of all the tubes, and this plate is separated by insulators from the chassis by about 4 mm to form a low inductance transmission line that can withstand 2000 V. The cathodes of the tubes are bypassed to the chassis at the bases of the tubes. The currents from all the tubes are collected at a point near the device under test where the clamp diodes are located.

When the current is shunted away from the device under test, it is desirable to minimize current reversal in the device. A diode and saturable inductor are placed in series with the device. The inductor is made by passing the device current through a number of amorphous "spike killer" cores, and the diode is a 600-V fast recovery type. When the current nears zero, the inductance increases from the near zero value it has when the cores are saturated to a value sufficiently large so as to suppress the large recovery current that

the diode would have when the current tries to reverse.

4.12 Device-Current Limit

The current-limit circuit measures the device current and compares it to an eight-bit number that is stored in a pair of 4029 counters. A diagram for this circuit is given in schematic 8. The eight-bit number can have a value of 0 to 255 which represents device current in amperes, although the maximum rated current for the tester is 100 A. The eight-bit number is loaded into the counters by means of either a front panel optical encoder or the computer driven TEST PARAMETER SET BUS. The eight-bit number representation of the current set value is converted to an analog voltage, and the LM339A analog comparator compares the analog voltage with the voltage developed by the current-to-voltage transformer T203 that measures the device current.

During a test, the device current is ramping up due to the load inductor. When the current reaches the set point, the output of the comparator goes high. The transition to the high level is turned into a pulse by the 510-pF capacitor, and the pulse is shaped into two pulses of different duration. The longer pulse enables the override function in the forward pulse-width controller circuit. The shorter pulse gates the count of the number of clock pulses accumulated during the forward current pulse which is then stored as the new value of the forward pulse-width byte needed for the device current to just reach the pre-set current limit. The shorter pulse, which is called On-Time Modifier on schematic 8, ungates the storage counters in the forward pulse-width controller to latch in the new value of on-time before the clock is released by the longer enable pulse. With the new value for the forward pulse width in place, the tester immediately goes into the turn-off portion of the test, and the current through the device is thereby limited.

4.13 Computer Interface

The circuit for the computer interface is given in schematic 11. The interface conforms to the IEEE-488 protocol [6] and uses the Fairchild 96LS488 chip which can be used in nonmicroprocessor, asynchronous systems. The interface has the main function of transferring numbers that are entered into the computer to the various functions that are set in the tester. There are five different parameters that can be set in the tester, and each is defined by eight bits. In addition, the tester must be triggerable by the computer, and the tester must be able to tell the computer that the device has broken down after a test.

The 96LS488 chip does most of the handshaking functions, while a few external loops with appropriate delays assures that the tester has sufficient time to accept the data that are needed to set the various test parameters. The chip contains all of the appropriate terminations for the data in/out lines, the handshake lines, and the control/status lines. The principles of the IEEE-488 data transfer are not discussed here, only the interface between the interface chip and the tester.

The address of the tester is determined by the five-section dip switch connected to A1-A5 of the 96LS488. An R-C network between the XTAL output and (not) CP input acts as
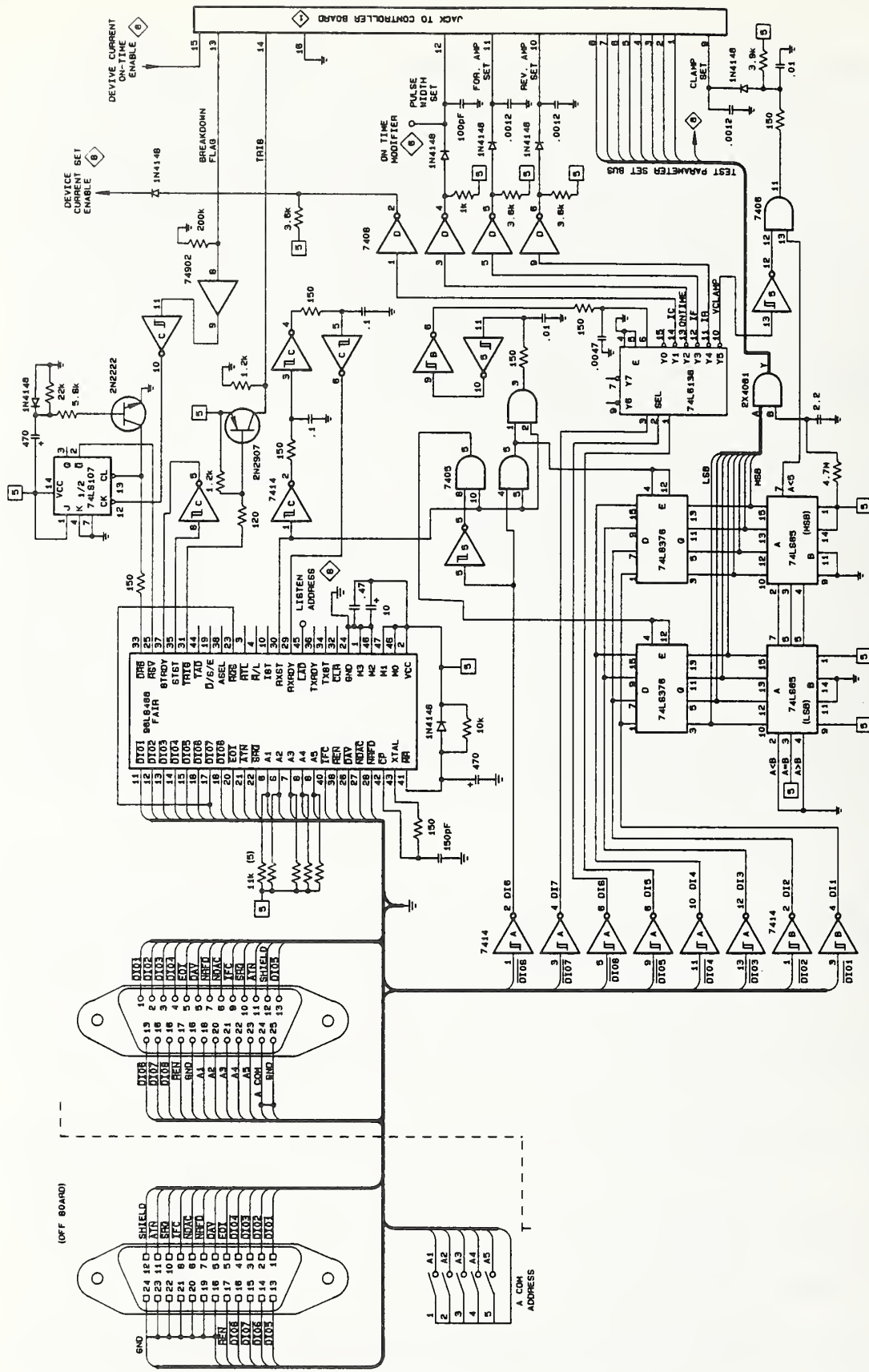
Schematic 11. IEEE-488 Computer Interface.

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a relaxation oscillator with an internal Schmitt-trigger inverter to make a 10-MHz clock. The (not) MR input is a reset and is initialized by the R-C network upon power-up. The M0 through M3 inputs set the chip in the Talker/Listener mode. The (not) LAD listener address output is connected to the decimal point of the display for the device-current limit circuit as an indicator that the tester has been addressed by the computer. This light flashes very briefly when the tester is successfully addressed, and is simply a system trouble-shooting aid for programming and address selection. The RXST output is driven high when valid data are on the DIO lines, and this output is used to tell the tester to accept the data and store it in the appropriate 74LS375 register, which is selected by the state of the DI8 line. The high on the RXST also is fed back to the RXRDY input through a delay circuit that tells the chip that the data have been accepted by the tester and that the chip can tell the controller in the computer that the data can be removed so that additional data can be presented.

The (not) RQS output is driven low if a service request is initiated by the 96LS488. This, in turn, is caused by the tester pulling the (not) RSV low in response to a device breakdown. The only information that the tester sends to the computer is one status bit that indicates the presence of a breakdown, and the (not) RQS is connected to the (not) DIO7 line to transmit this information. The (not) SRQ Service Request line is driven low to signal the controller in the computer that some device hooked up to the IEEE-488 bus has requested service. If, upon doing a Serial Poll, the controller finds that it is the tester, the conclusion is drawn by the computer that a breakdown occurred. The 74LS107 is used as a handshake between the tester and the 96LS488 chip for the service request sequence. The (not) DRB output is driven low when the chip is addressed to Talk and is in the Talker Active State. This transition clears the 74LS107 for another breakdown flag signal from the tester. The 2N2222 transistor is used to initialize the 74LS107 upon power-up.

4.13.1 Setting Parameters

Data to set each parameter in the tester are sent in two bytes. Each byte has four bits which are data and four bits which describe the destination for the data. One of the destination bits, DI8, is used to designate whether the four data bits, which are on lines DI1 through DI4, make up the four least significant bits, or the four most significant bits, of each eight-bit test parameter word. When the DI8 line is high, the four data bits in lines DI1 through DI4 are stored in the 74LS375 register for the most significant bits. The other three destination bits, DI5 through DI7, designate the particular test parameter that is to be set, and these bits are decoded by the 74LS138 into individual enable lines for the various counter-registers that contain the eight-bit words describing each test parameter.

The two 74LS85 comparators prevent the forbidden clamp voltage settings of 2010 through 2550 from being accepted by the tester.

4.14 Breakdown Tally Counter

The tally counter counts the number of breakdowns that occur up to a maximum count of 63, after which it starts over at zero. There is a push-button reset to return the count to
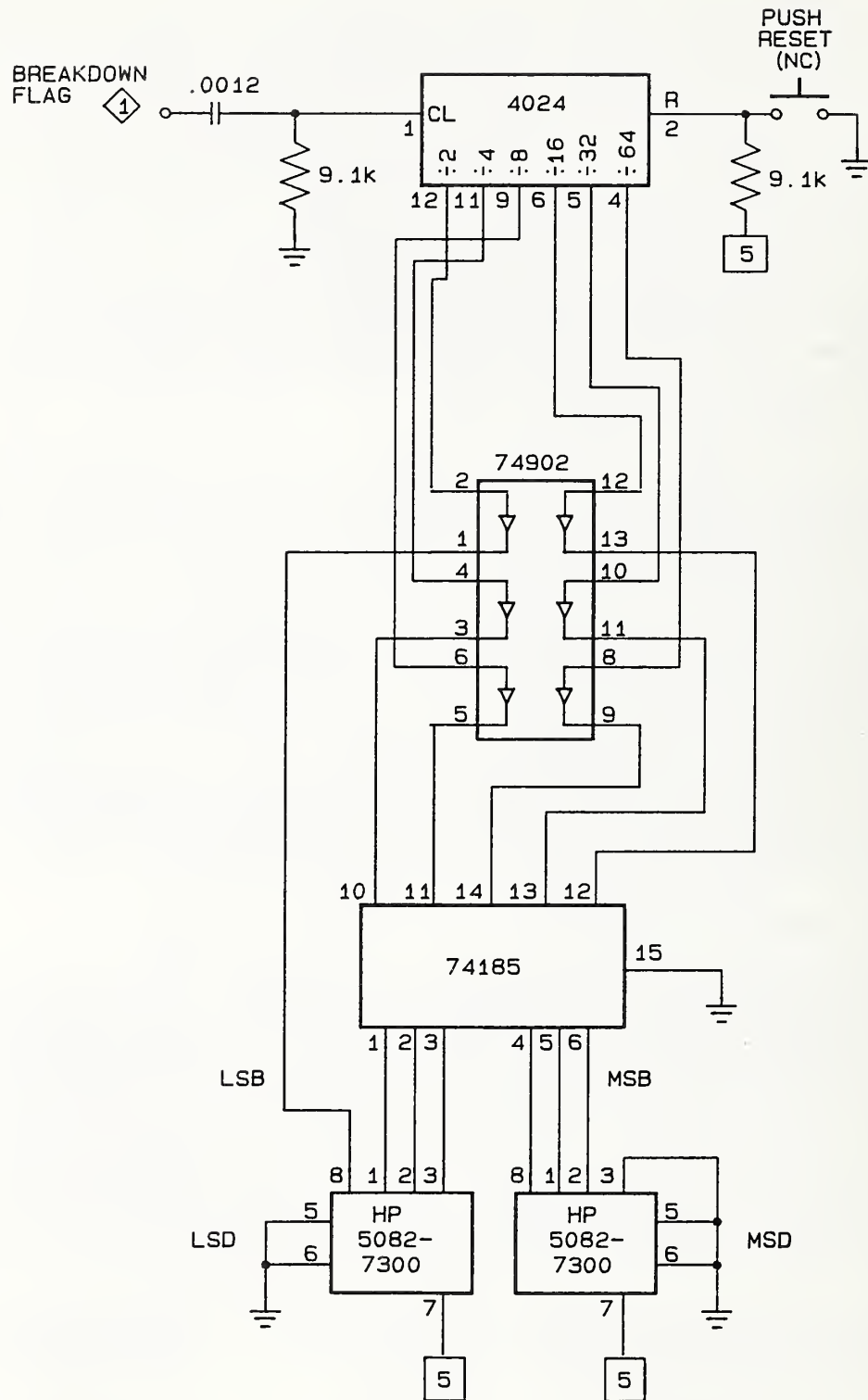
Schematic 7. Breakdown Tally Counter.

zero. The circuit diagram is given in schematic 7.

5. SPECIAL CIRCUIT COMPONENTS

This transistor turn-off tester uses many circuit components which have special ratings and characteristics. These special requirements occur as a result of the extensive use of high-frequency power conversion and the many uses of high voltage and high current in this instrument. Most of the diodes are fast-recovery types, and many require high-voltage capability.

Many of the capacitors in the power conversion circuits are high-voltage polypropylene types because other types of dielectrics have too much loss. Capacitors C1201, C1301, and C1501 are high-current types with rms current ratings in excess of 10 A, such as the Sprague 735P series. The clamp capacitor C1202 is a high-current oil-filled type, and the one used in this tester was made by CSI. The voltages of many of the capacitors are not marked on the schematics. In most cases, these capacitors are in low-voltage circuits and need not handle voltages greater than the supply voltage for that circuit. Some of these circuits, such as the protection circuit, operate with voltages of about 600 V and require capacitors sized accordingly.

Most of the inductors and transformers used in the tester are not available commercially and must be hand wound on appropriate cores. Table 1 lists the core types used, and the schematics show the number of turns for the various windings. Any special winding techniques are described in the circuit description portion of this publication. In general, adequate insulation must be used between windings to prevent the possibility of voltage breakdown. Extra care needs to be taken on transformers that isolate the line side of the power mains from the secondary side for safety reasons. Many of the inductors and transformers are wound with Teflon-insulated hook-up wire.

Some of the resistors used in the tester are more robust than their power rating suggests, as they have to withstand high surge currents. The 3-Ω resistor that is in parallel with L1203 is subjected to surges of 100 A. The 10-Ω resistor that is in series with the 2N6075A triac in the power supply experiences a surge of 15 A during the power-up sequence. Both of these resistors have 10-W ratings but are physically large old-style wire-wound types.

6. LOAD CIRCUIT FOR THE DEVICE UNDER TEST

In principle, the load for the device under test is simply an inductor. In practice, however, the load is actually made up of several inductors and other components. Figure 3 shows the circuit that is actually used. Three inductors, different values and different saturation characteristics, make up the composite load inductor. These inductors are not in table 1 as they are part of the test fixture for the device under test, and not part of the tester. The 300-μH inductor is made with 54 turns on a Ferroxcube EC70G plus EC70 core set, and saturates at 15 A. The 100-μH inductor is made with 23 turns on a Ferroxcube 1F4-1B4 core set with gaps of about 6 mm where the two cores butt up against each other, and it has a saturation of 100 A. The 1-mH inductor is made with 20 turns on a Ferroxcube 528T500/3E2A toroid core, and saturates at slightly less than 1 A.

Table 1. Core Specification for Inductors and Transformers

Part Number*	Core	Notes
L101	Ferroxcube 2616-3B7	26 turns, gap index card paper to 240 μH
L201	(same as L101)	(same as L101)
T201	Ferroxcube EC52 and EC52G	Wound with No. 24 magnet wire, primary inductance 3.7 mH, one gapped and one ungapped core
T202	Ferroxcube 846T250/3E2A	Toroid
T203	Ferroxcube 528T500/3E2A	Toroid
L1201	Toshiba "Spike Killer" (7 pcs) SA 8 × 6 × 4.5	1 pass through each of 7 toroids
L1202	Ferroxcube 768T188/3E2A	4 turns, toroid
L1203	Ferroxcube U-I, 2 sets, 1F5 and 1B5	100-A saturation, 8 turns No. 12 wire, approx. 2-mm air gaps, 40 μH
L1204	Ferroxcube 846T250/3E2A (2 pcs)	2 stacked toroids, No. 22 wire
T1201	Ferroxcube 768T188/3E2A	
T1202	Ferroxcube 768T188/4C4	Secondaries physically distributed around primary for best coupling; primary wound with wire-wrap wire
T1203	Ferroxcube 846T250/3E2A	
T1204	Ferroxcube 846T250/3E2A	
T1205	Ferroxcube 846T250/3E2A	
L1301	Ferroxcube EC52G (2 pcs)	585 turns, 30-mH, high-voltage, well-insulated layers

*The one or two digits preceding the last two digits of the part number correspond to the drawing number of the circuit in which the part is used.

Table 1. Continued

Part Number	Core	Notes
L1302	Ferroxcube EC52G (2 pcs)	140 μH, Litz wire, 150 strands No. 36 (eff. gauge No. 14)
T1301	Ferroxcube 846T250/3E2A	Low capacitance heater winding for top tube, made with wire-wrap wire, all turns of this winding in Teflon sleeve; other windings made with No. 26 Teflon hook-up wire
T1302	Ferroxcube EC52 (2 pcs)	High-voltage, well-insulated layers
T1303	Ferroxcube 204T250/3E2A	No. 26 Teflon hook-up wire
T1304	Ferroxcube 528T500/3E2A (2 stacked cores)	Low capacitance winding driving top tube, made with wire-wrap wire with all turns passed through Teflon sleeve; other windings made with No. 26 Teflon hook-up wire physically separated from each other
T1305	Ferroxcube 204T250/3E2A	
T1306	(same as above)	
T1307	Ferroxcube E75-3C8 (2 E cores)	Wound with No. 22 Teflon wire
T1401	Ferroxcube E75-3C8 (4 E cores, 2 pairs)	Primary 2X No. 22 Teflon wire; high-voltage secondaries No. 26 wire, other secondaries No. 22
T1402	Ferroxcube 846T250/3E2A	
T1403	Ferroxcube 528T500/3E2A	
L1501	Ferroxcube 782E272/3E2A (2 E cores in clasp and spring clip)	Control reactor. Each 20-turn winding wound with No. 26 Teflon wire on separate outside leg of inductor, placed in series so that the fluxes add. Cores must seat well and the total inductance of both windings is 2.6 mH. The 200-turn winding is made with No. 28 magnet wire on center leg with bobbin

Table 1. Continued

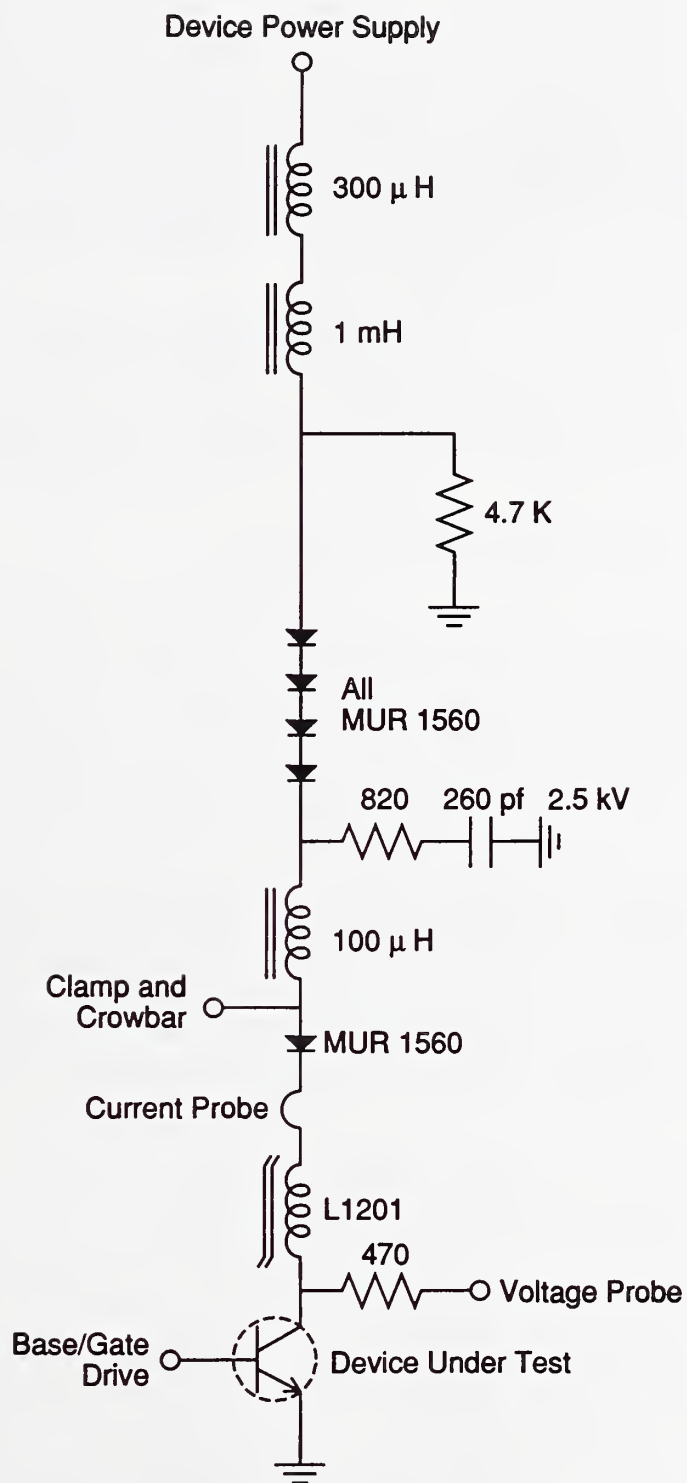| Part Number	Core	Notes
L1502	Ferroxcube EC70G (2 pcs) gapped	47 turns of Litz wire, 150 X 36 stranding, eff. gauge No. 14. Extra insulation between winding layers, 135 μH
L1503	(air core)	No. 18 magnet wire
L1504	(same as above)	
T1501	Ferroxcube 846T250/3E2A	

Figure 3. Device load circuit.

The 1-mH inductor works in conjunction with the four diodes and the 260-pF capacitor to prevent the voltage on the device under test from rapidly going to zero when the current in the 100-μH inductor goes to zero. Such a rapid voltage transition would be detected as a device breakdown by the detection circuit. The resistors associated with this L-C diode network are for damping purposes. The 1-mH inductor needs to store only enough energy to assure that the 260-pF capacitor is left in a charged state when the current goes to zero. The effect of the 1-mH inductor on the breakdown test itself is of no consequence, as it is in saturation for all test currents of interest, and it only adds a delay in the ramping up of the current when the device turns on.

The effective load inductance for test currents of interest is 400 μH for currents up to 15 A, and about 100 μH for currents between 15 and 100 A. The dual inductor system enhances accuracy of the current-limit circuit at the lower currents because the d_i/d_t is reduced, and there is more time resolution for establishing the proper on-time pulse width to achieve the desired set current.

7. PROGRAMMING THE BREAKDOWN TESTER

The tester can be addressed to listen as per IEEE-488 convention. Test parameters can be independently loaded into each of five registers: collector/drain current (I_c), on time, forward base/gate current (I_f), reverse base/gate current (I_r), and clamp voltage (V_{clamp}). The registers do not have to be reloaded for each test except where changes are desired. To load each register, two bytes need to be sent over the bus. The first byte to be sent contains the binary equivalent to the least significant hex digit (data lines DIO1-DIO4), the address of the specific register to which it is to be sent (DIO5-DIO7), and DIO8 set FALSE to indicate that it is the first byte of a two-byte command. The second byte sent contains the most significant hex digit (DIO1-DIO4), the address of the specific register, which will be the same as for the first byte (DIO5-DIO7), and DIO8 set TRUE to indicate that it is the second byte of a two-byte command. Each register is thus loaded with eight bits, representing decimal numbers between 0 and 255. For V_{clamp}, only decimal numbers between 0 and 200 are allowed. Below is a table giving the register coding.

Table 2. Register Coding

REGISTER	DIO5	DIO6	DIO7
I_c	TRUE	FALSE	FALSE
on-time	FALSE	TRUE	FALSE
I_f	TRUE	TRUE	FALSE
I_r	FALSE	FALSE	TRUE
V_{clamp}	TRUE	FALSE	TRUE

If the decimal number 125 is loaded into each of the registers, it will have the following meanings:

I_c (collector current):   125 A

on-time: 125 μs

I_f (forward current):   12.5 A

I_r (reverse current):   12.5 A (or 1.25 A if on low current range)

V_{clamp} (clamp voltage):   1250 V

As an example, suppose you wanted to program the tester to set the on-time to 241 μs. The required binary coding needed would be:

```
DIO8              DIO1
0 0 1 0 0 0 0 1   1st byte   (Hex 21)
1 0 1 0 1 1 1 1   2nd byte   (Hex AF)
```

Once the registers are set, the breakdown test can be initiated. The GET (Group Execute Trigger) command is used to trigger the test.

If a breakdown occurs, the RBSOA tester will issue a SERVICE REQUEST. The computer must do a serial poll, and when polled, the RBSOA tester will indicate a breakdown has occurred by answering with a status byte having DIO7 TRUE and the other DIO lines FALSE. When the polling is finished, the testing can resume, usually by resetting some of the registers and issuing GET again for another test.

When a series of tests are run, a time-out period must be inserted between each test; 3 s is recommended. The tester requires a set-up time to stabilize the clamp voltage after it receives the GET command.

8. REPRESENTATIVE OPERATIONAL WAVEFORMS

Some waveforms are given in this section to demonstrate various aspects of the operation of the tester. When the tester is triggered in the one-shot mode, there is a delay which gives the tester time to stabilize the clamp voltage before the test is executed. The clamp capacitor stores 50 J when charged to the maximum clamp voltage, and it takes some time for charging and discharging. Figure 4 shows the ramp up and ramp down for the clamp voltage when it is set to 2000 V. The clamp voltage is zero before the tester is triggered. Once triggered, the clamp voltage begins ramping up as the capacitor is charged with a near-constant current until the voltage reaches the set point. It takes slightly longer than 1 s to reach 2000 V, and correspondingly less time to reach lower set voltages. The test on the device under test is executed about 2 s after the one-shot trigger button is released. After the test is executed, the clamp voltage ramps back to zero, again, at a nearly constant current rate. The clamp voltage remains at the set point between tests in the repetitive test mode.

The output of the base/gate drive circuits is shown in figure 5, with the transition from forward current to reverse current expanded in figure 6. The forward pulse width is 30 μs,
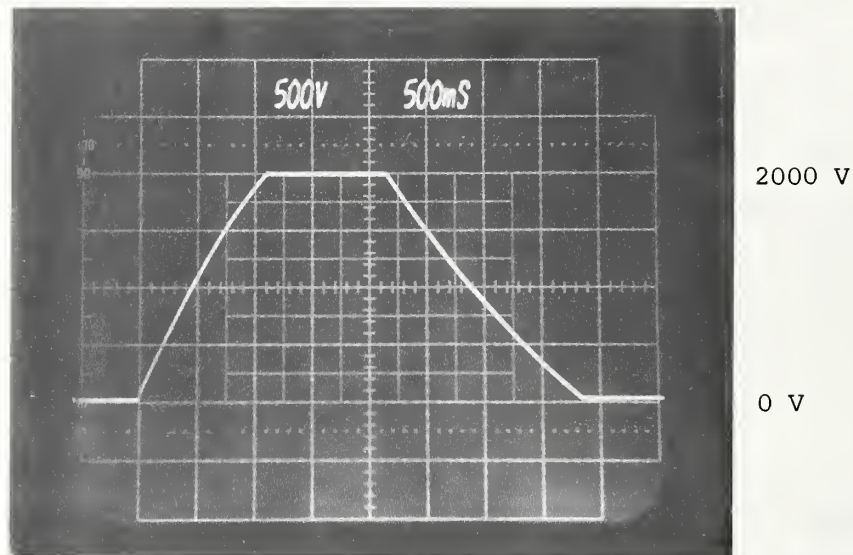
41

Figure 4. Clamp voltage ramp up and down when set to 2000 V. The scale factors are 500 V per division, vertical axis, and 500 ms per division, horizontal axis.
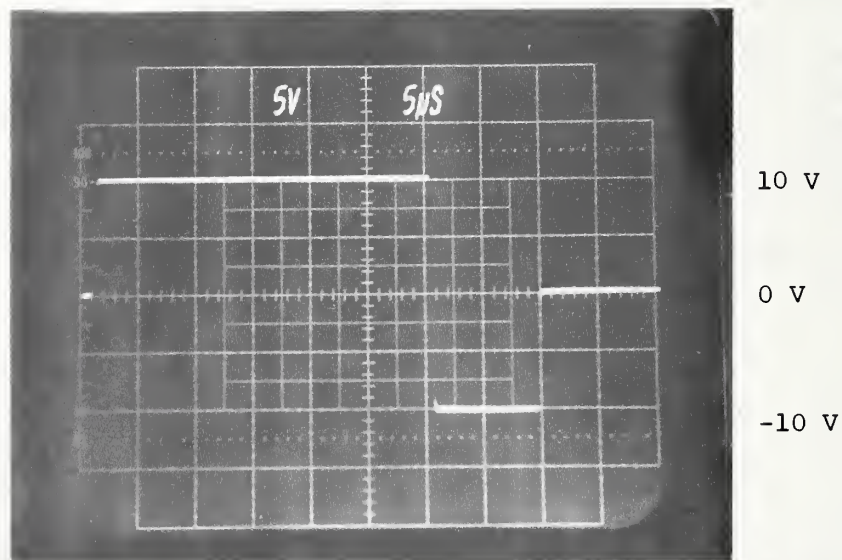

Figure 5. Output voltage developed by the constant current drive of the base/gate drive circuit across 1-Ω resistor when both the forward and reverse currents are set to 10 A. The scale factors are 5 V per division, vertical axis, and 5 μs, horizontal axis. The on-time is set to 30 μs, and the reverse pulse width is set to 10 μs.
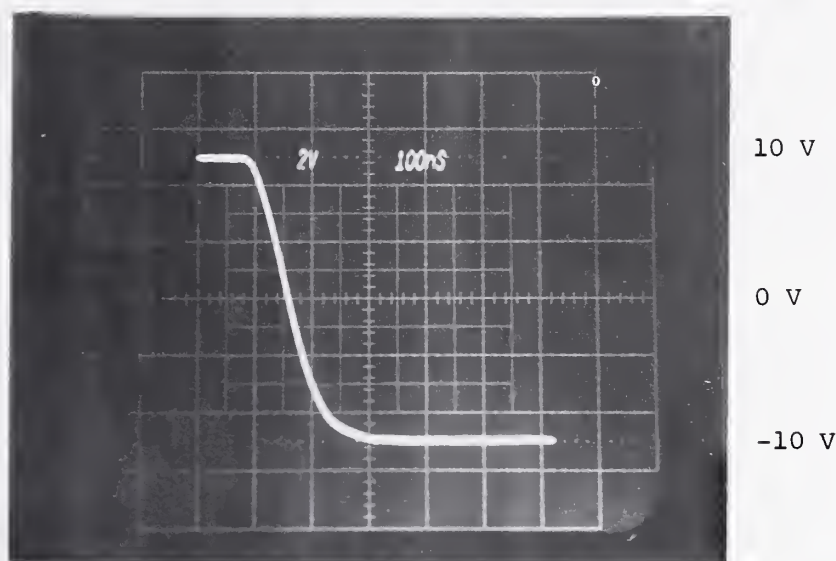
Figure 6. Expanded time scale showing the transition from forward to reverse drive for the same conditions as in figure 5. The oscilloscope is set to a reduced scale to achieve a faster writing speed. The vertical axis is 2 V per minor division and the horizontal is 100 ns per minor division.
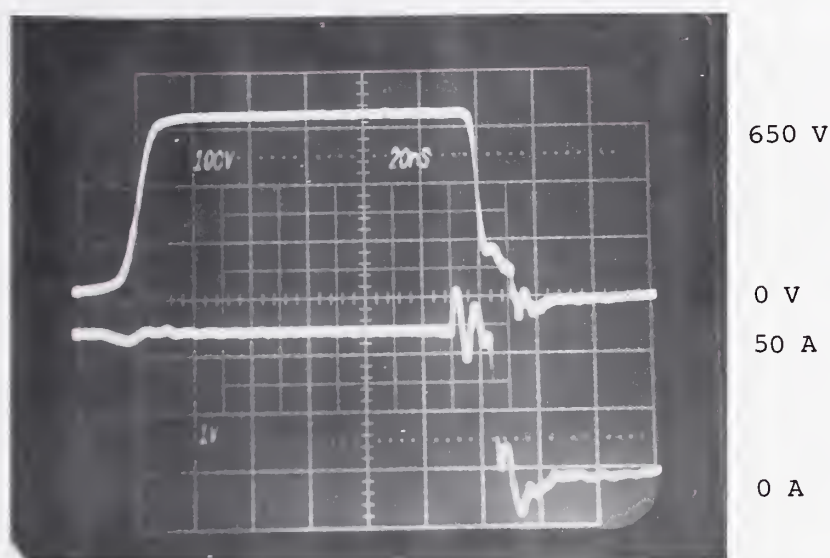
Figure 7. Current (bottom trace) and voltage waveforms for a MOSFET breakdown at a 50-A level. The scale factors are 100 V per minor division; 10 A per minor division, vertical axis; and 20 ns per minor division, horizontal axis.

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and the reverse pulse width is 10 μs. The forward- and reverse-current amplitudes are ±10 A, respectively, across a 1-Ω resistor. Note that figure 6 is taken with the oscilloscope set to reduced scale for faster writing speed, and the dimensional parameters shown are for the smaller divisions. The transition time for these conditions is 300 ns. The output capacitance for the driver circuits is quite large, due in part to the large number of output transistors, and as the drive currents are reduced, this transition time increases. The turn-off time for MOS-gate-controlled devices can be changed by using this effect, and it is not detrimental for bipolar transistor characterization since there is little change in base voltage from the turned-on state to the turned-off state.

Figure 7 gives the current and voltage waveforms for a MOSFET breakdown when it is attempting to turn off 50 A. The clamp voltage was set higher than the avalanche voltage, so no current was diverted to the clamp during the test. The upper trace shows that the drain voltage rose to about 650 V, at which point the device sustained avalanche breakdown at the full 50 A for about 220 ns. After 220 ns, the MOSFET went into full breakdown with the voltage collapsing to 150 V. The voltage collapse triggered the tester's protection crowbar circuit which diverted the current (bottom trace) in about 25 ns, and brought the drain voltage to zero.

Figure 8 demonstrates the freedom from susceptibility to false triggering that the breakdown circuit has for large clamp voltage overshoots. For this test, a MOSFET was turned off fast with a large reverse current. The clamp was set to 150 V, and the 15-A drain current had a fall time of about 10 ns. The drain voltage rose to about 430 V before the clamp became effective, producing a voltage overshoot of about 280 V, yet the protection circuit was not triggered. In tests where the clamp does not act, a breakdown voltage transition of 130 V is sufficient to trigger the protection crowbar. If the clamp does act during a test, a device breakdown will cause a sudden reversal of the clamp current before the clamp diodes recover. This will trigger the protection circuit, even if the collapse of device voltage is delayed until the diodes recover.

9. PHYSICAL HARDWARE LAYOUT

The tester was built in several subassemblies that plug together. The most critical part of the tester is the protection circuit, which was hard-wired into the mainframe in order to take advantage of the ground plane of the chassis. The ground plane forms part of the transmission line which increases speed for the protection circuit and adds shielding to prevent false triggering and erratic circuit operation. The following series of photographs show the various parts of the tester.

The entire tester is shown in figure 9. The device under test and the load inductors are on top of the front portion of the mainframe. The wiring for the protection circuit is behind the top panel which is removed in figure 10. A back view of the chassis is shown in figure 11. The tubes for the protection crowbar can be seen in the top part of the box, along with the copper plate that surrounds the bases of the tubes. The copper plate is electrically connected to the plates of the tubes, and forms a transmission line with the
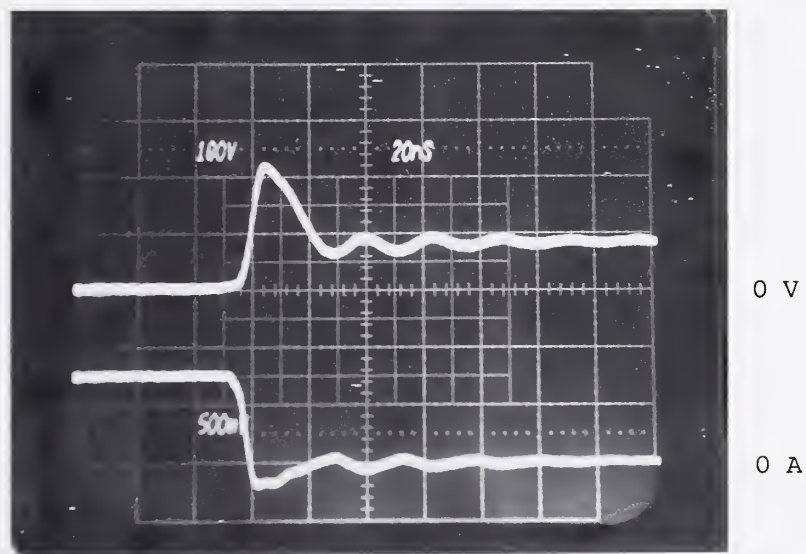
Figure 8. Clamp voltage overshoot (top trace) and current for high-speed device turn-off. The scale factors are 100 V per minor division and 5 A per minor division, vertical axis, and 20 ns per minor division, horizontal axis. The sub 10-ns device turn-off causes the device drain voltage to overshoot the clamp set point by about 280 V. The improved breakdown detection circuit for this tester is able to discriminate between this overshoot and actual breakdown, and does not issue a false trigger signal.
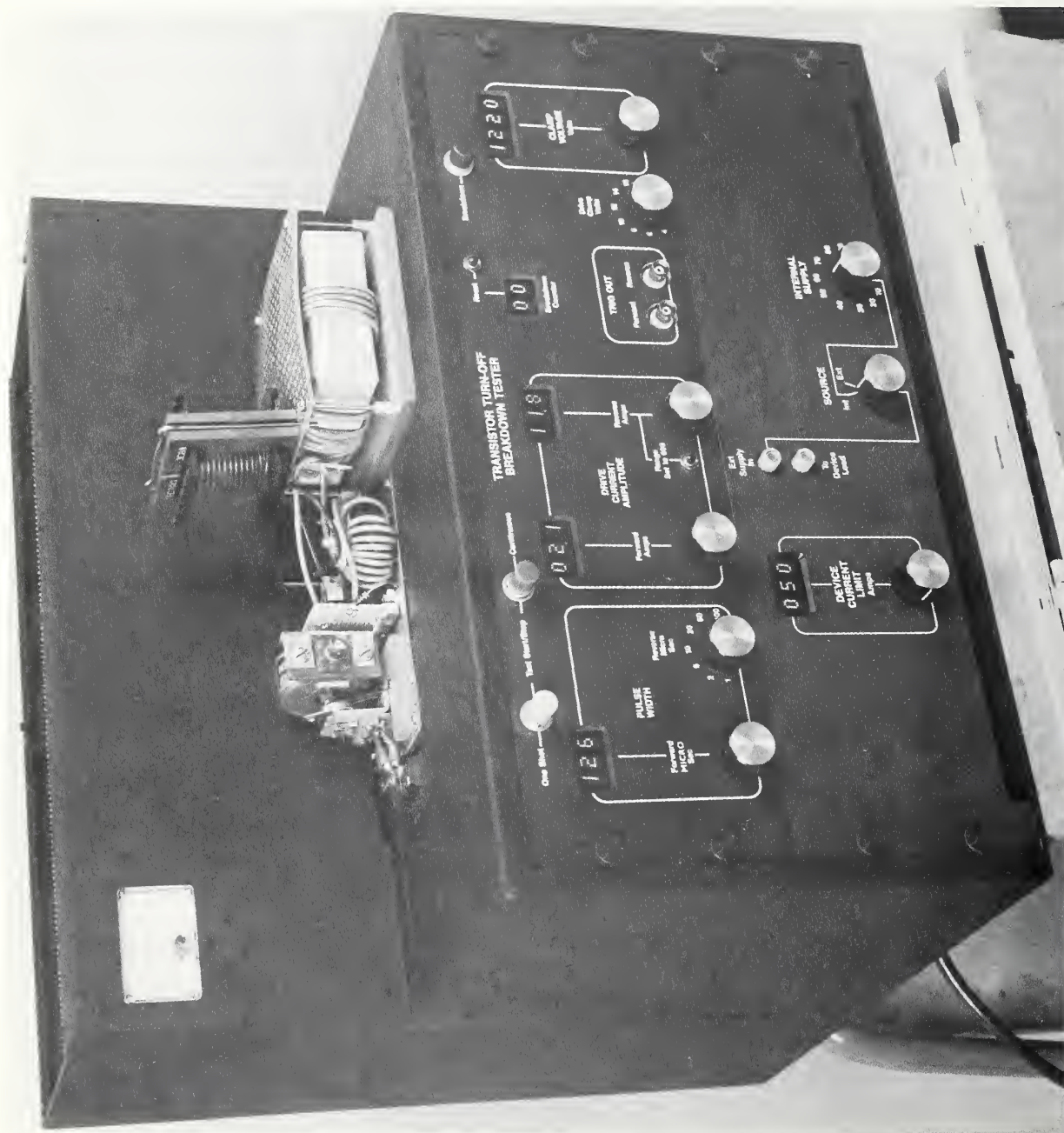
Figure 9. Photo of the entire tester.
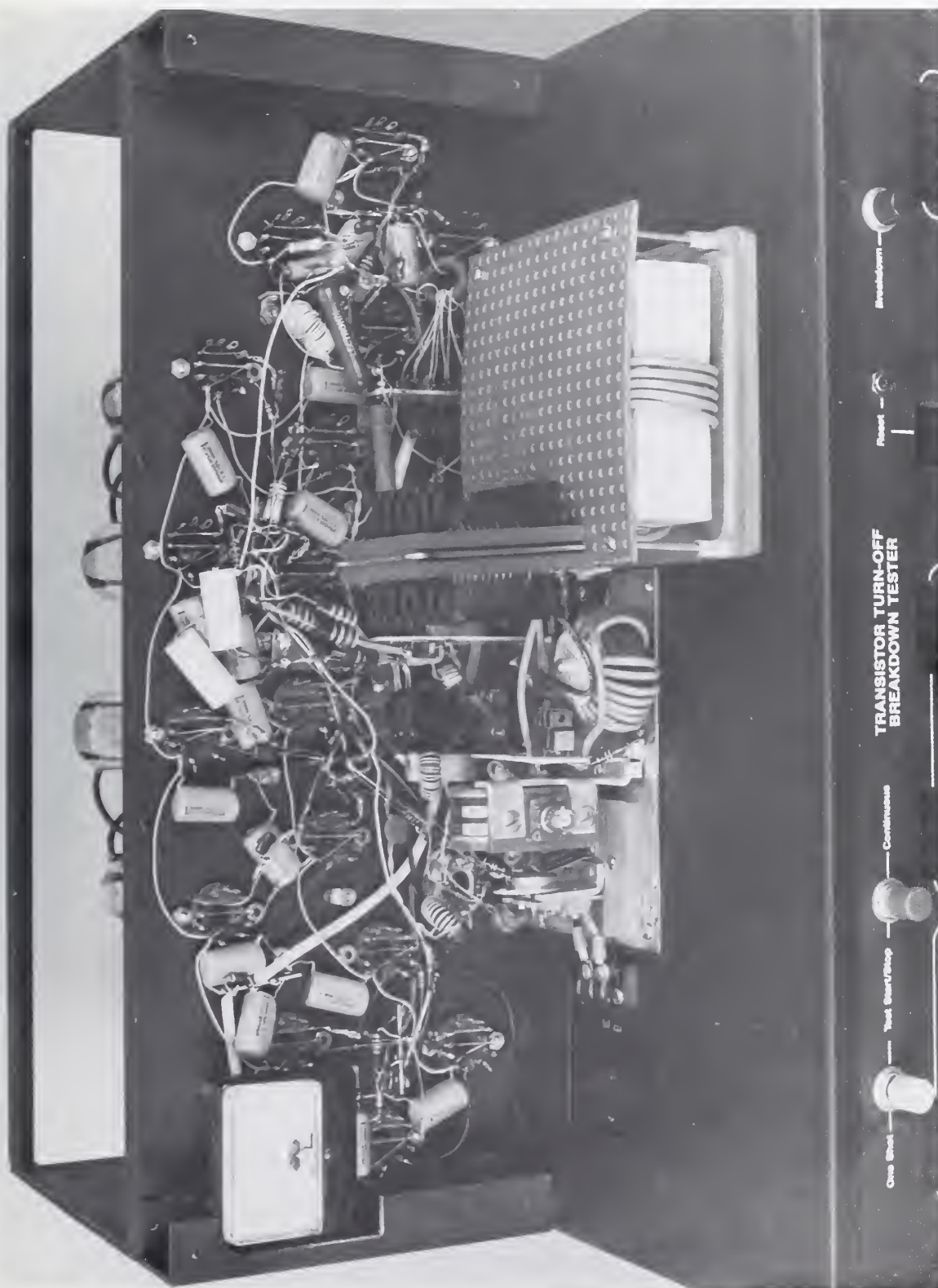
Figure 10. Crowbar wiring.
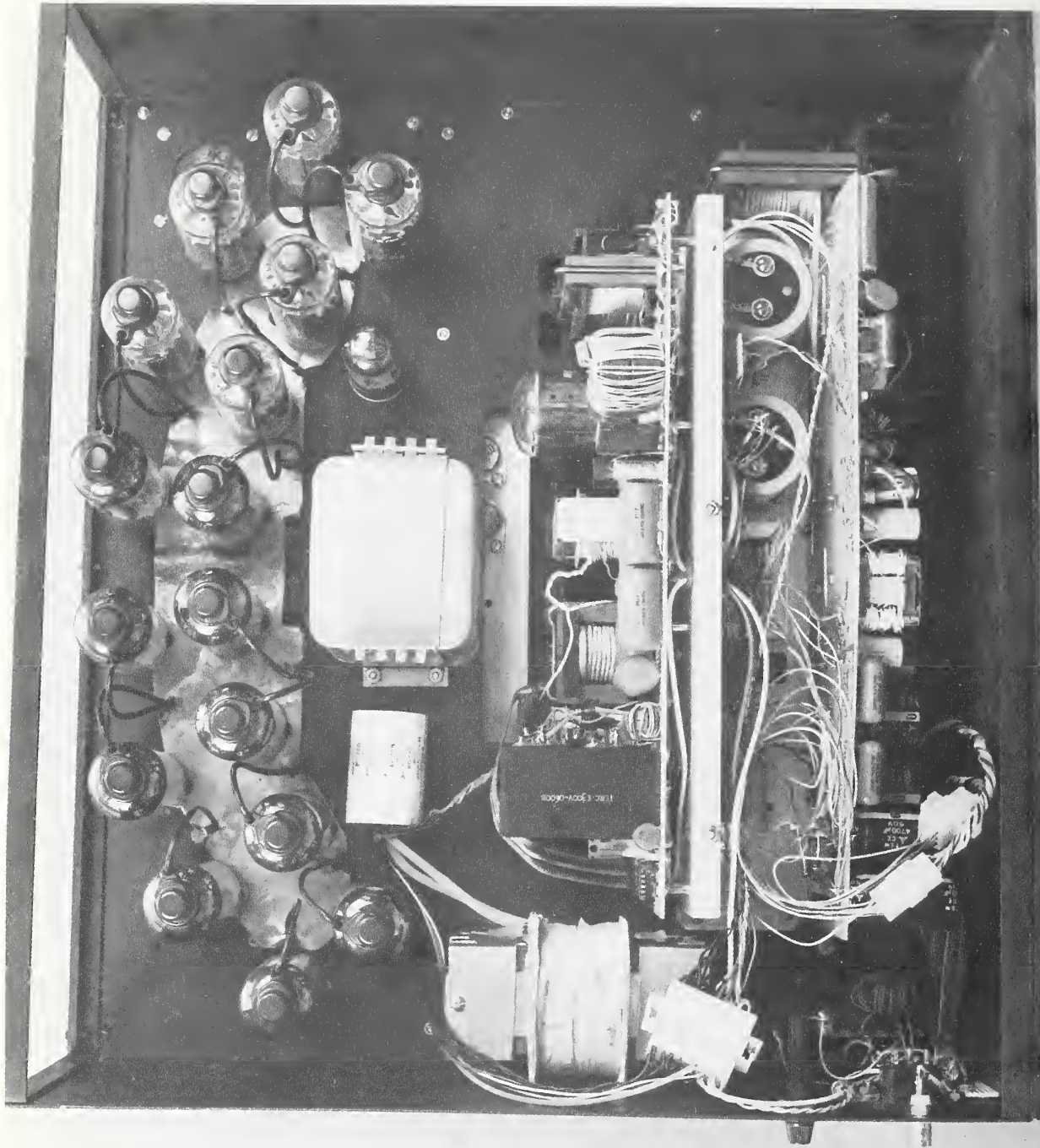
Figure 11. Back of the tester.

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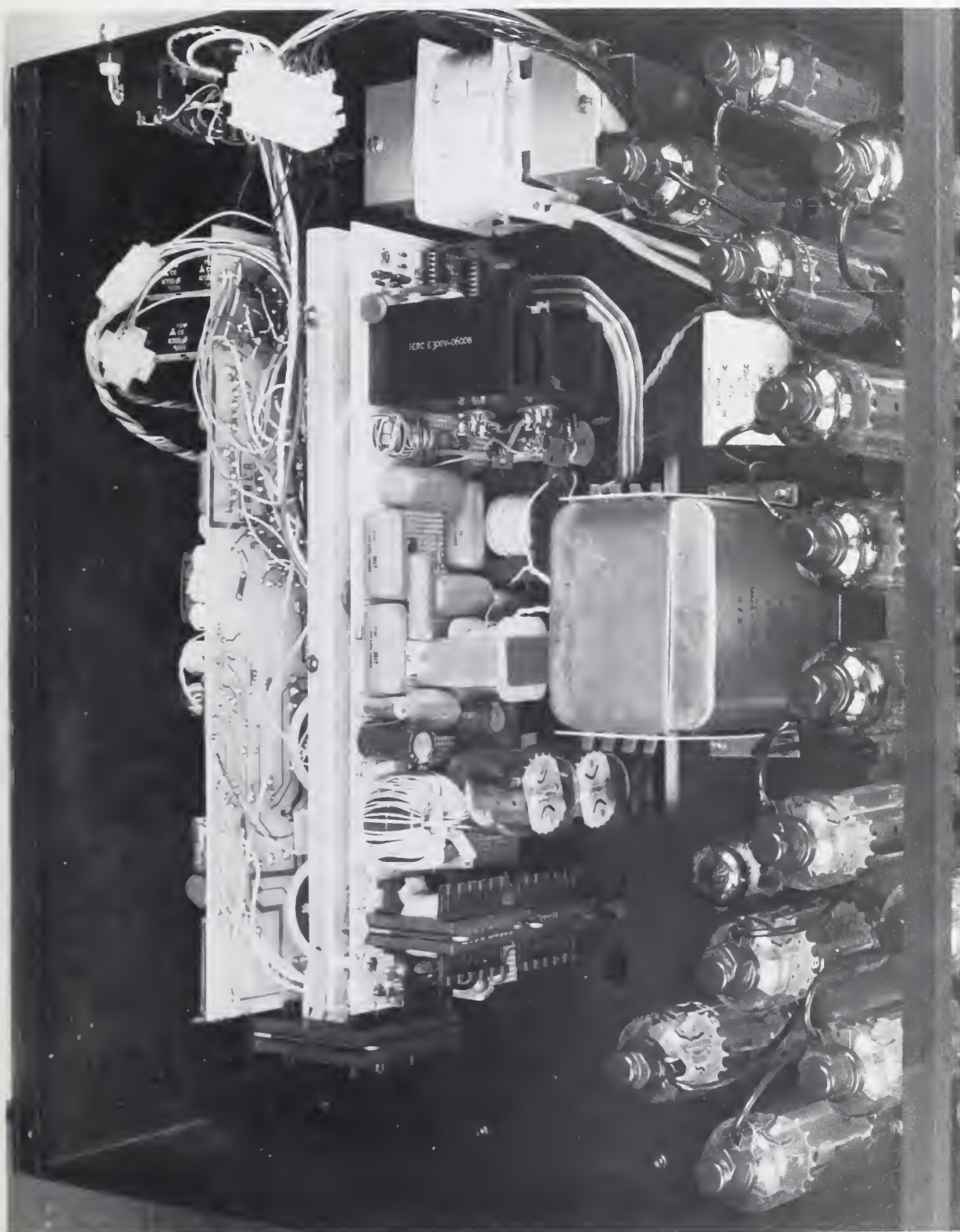
Figure 12. Clamp supply.

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Figure 13. Bottom layer of the main power supply.
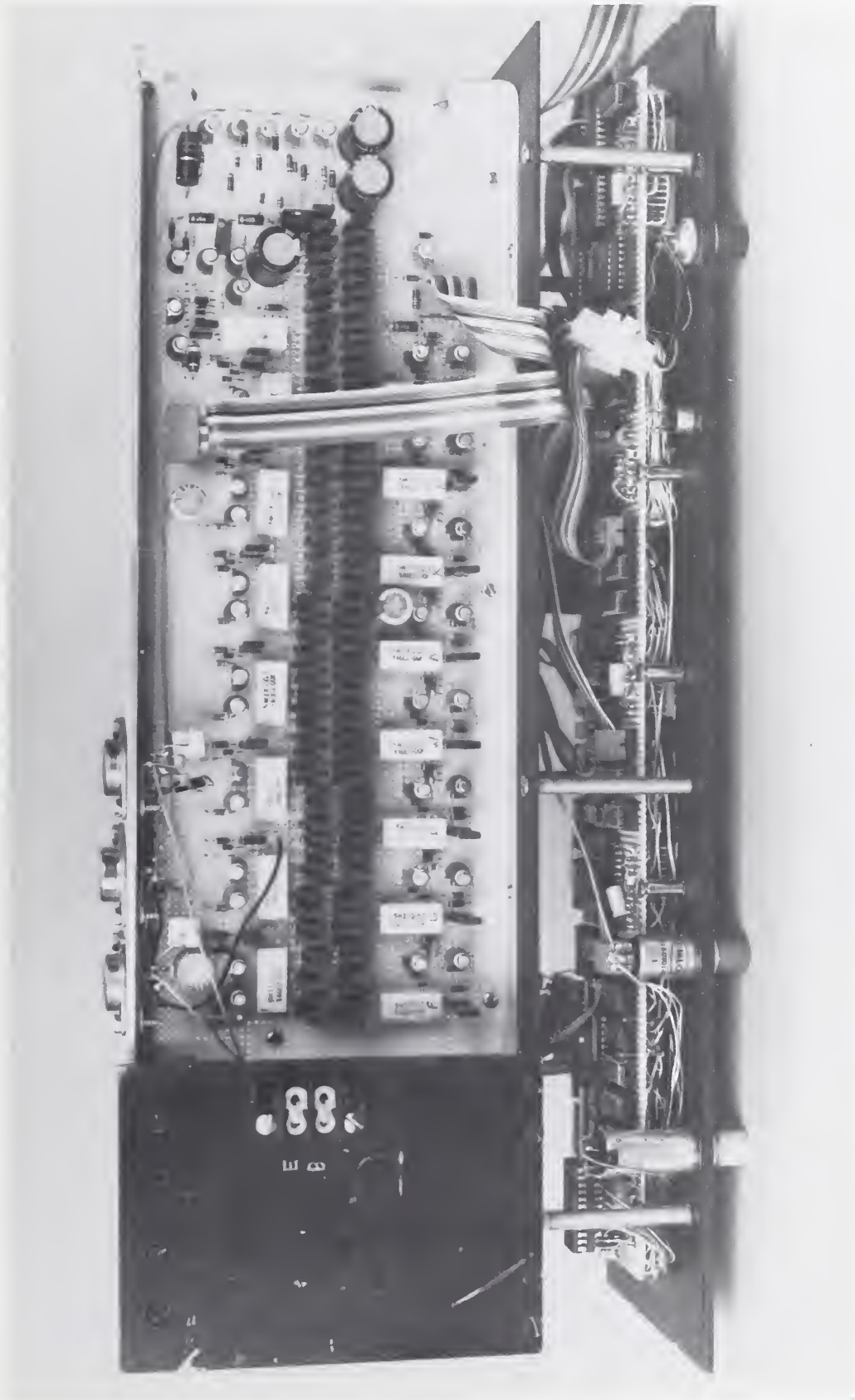
Figure 14. Base-gate drive circuit viewed from the top.
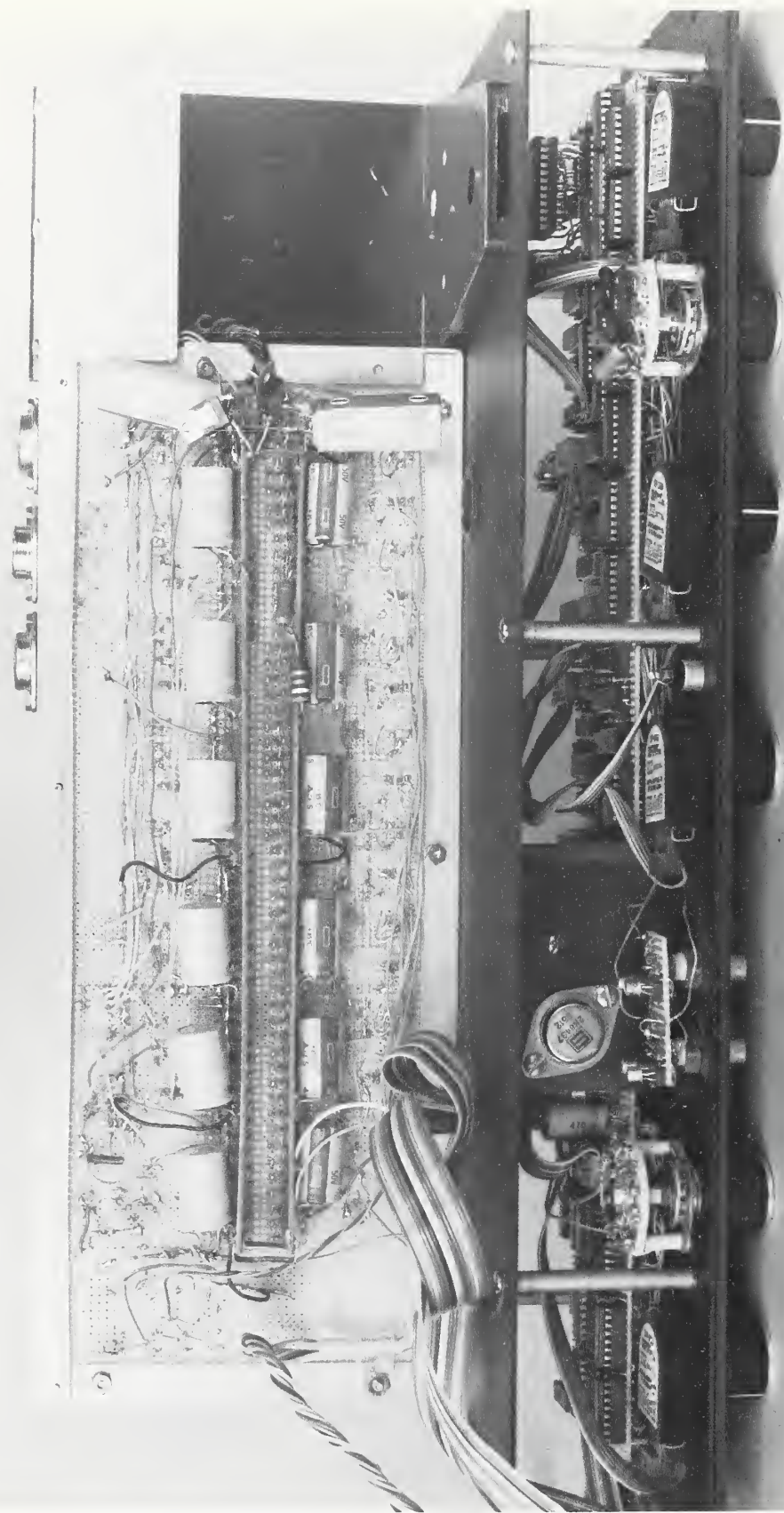
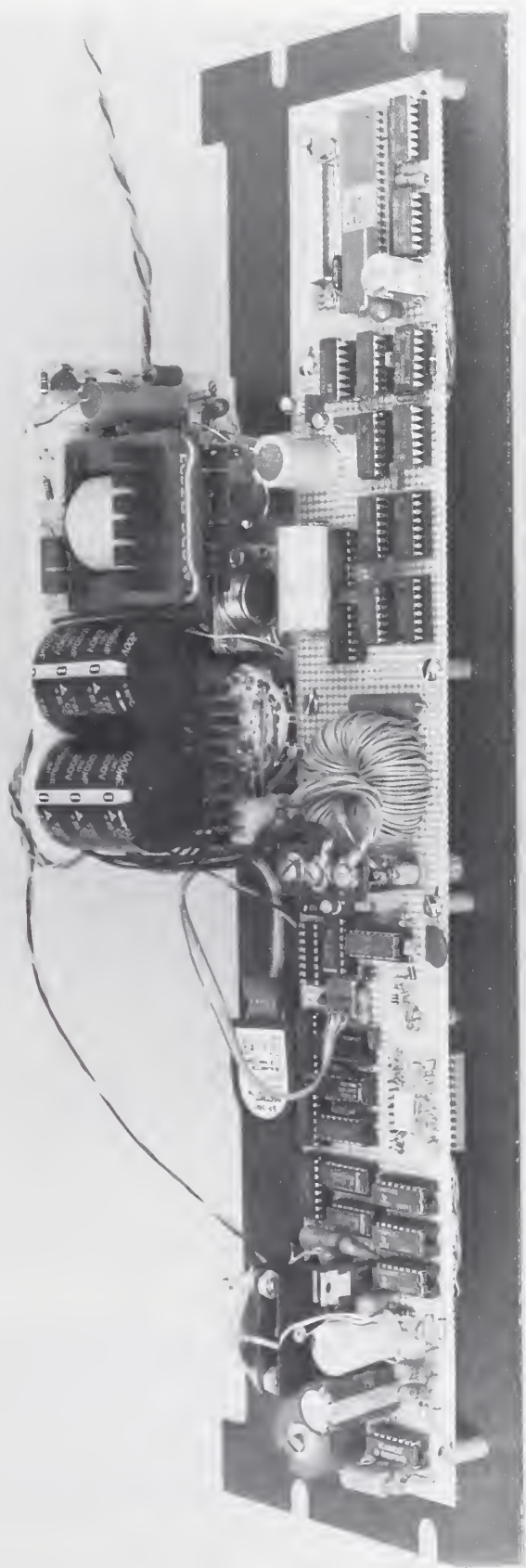Figure 15. Base-gate drive circuit viewed from the bottom.

Figure 16. Device power supply and computer interface.

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chassis ground plane. Two copper strips pass through holes in the chassis wall to connect the copper plate to circuit components connected to the device under test. The clamp capacitor, C1202, is the large rectangular object below the tubes. C1201 is visible to the left of the clamp capacitor, and L1203 is the large part on the left side of the chassis. The triple-layer subassembly that takes up most of the remaining space is the main power supply and the clamp supply. The clamp supply is the top layer and can be seen more clearly in figure 12. Figure 13 shows the bottom layer of the power supply.

The remaining parts of the tester are housed in subassemblies that are rack-mounted into the front of the tester. Figure 2 shows the front panels of the control portion of the tester. The top subassembly has most of the control circuits and the base/gate drive circuits, and the bottom subassembly has the interface and device-current control circuits. Figure 14 shows the base/gate drive from the top, and figure 15 shows it from the underside. The transmission line constructed from strips of circuit-board material is visible in figure 15. A circuit board that contains the digital control circuits is behind the front panel and is visible in both figures 14 and 15. Figure 16 shows the subassembly that contains the device-current control, the device power supply, and the interface circuits.

ACKNOWLEDGMENT

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4. TITLE AND SUBTITLE

Semiconductor Measurement Technology: A Programmable Reverse-Bias Safe Operating Area Transistor Tester

5. AUTHOR(S)

D. W. Berning

11. ABSTRACT (A 200-WORD OR LESS FACTUAL SUMMARY OF MOST SIGNIFICANT INFORMATION. IF DOCUMENT INCLUDES A SIGNIFICANT BIBLIOGRAPHY OR LITERATURE SURVEY, MENTION IT HERE.)

The circuits and construction of a transistor turn-off breakdown tester are described. Principles of operation for various circuits in the tester are discussed, as well as those for the complete system. Construction notes are given with layout guidelines. Included are complete circuit schematics and details of construction of special parts used in the tester. Specifications and performance data are also given in this document.

12. KEY WORDS (6 TO 12 ENTRIES; ALPHABETICAL ORDER; CAPITALIZE ONLY PROPER NAMES; AND SEPARATE KEY WORDS BY SEMICOLONS)

clamp circuits; converter circuits; drive circuits; fast-switching, high energy-circuits; inductive load switching; nondestructive measurements; power conversion; protection crowbar; reverse-bias breakdown; safe operating area; second breakdown; transistor; transistor-breakdown testing.

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