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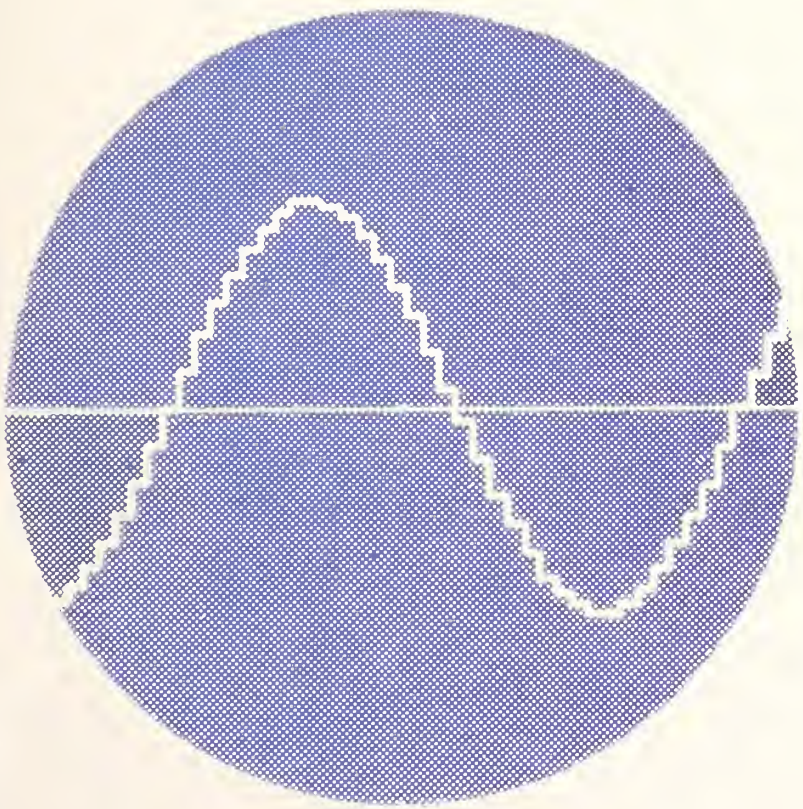
NBS Special Publication 707

Digital Methods in Waveform Metrology

Barry A. Bell, Editor

Proceedings of a Seminar



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[2] Some divisions within the center are located at Boulder, CO 80303.
[3] Located at Boulder, CO, with some elements at Gaithersburg, MD.

NBS Special Publication 707

Digital Methods in Waveform Metrology

Proceedings of the Seminar on
Digital Methods in Waveform
Metrology, held at the National
Bureau of Standards,
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and 19, 1983

Barry A. Bell, Editor

Center for Electronics and Electrical Engineering
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FOREWORD

On September 23 and 24, 1974, a workshop was held at the NBS, Gaithersburg facility to identify critical problem areas and metrology needs associated with modern electronic instrumentation. At that time the Electricity Division had begun to institute a new program in the general area of dynamic electrical measurements and standards in support of such instrumentation. An important concern was how well NBS is addressing the metrology needs vital to the growth of automatic test and measurement systems, and the development of new generations of automatic test equipment (ATE) which have become a significant part of the electronics industry. Representatives of twenty-five leading instrument manufacturers and users discussed the present and projected future requirements for improved physical standards, new measurement methodologies, better calibration and measurement assurance services, and systems performance validation. The discussion topics, session notes, feedback reports, and conclusions of the workshop are well documented in NBS Technical Note 865, "Critical Electrical Measurement Needs and Standards for Modern Electronic Instrumentation," issued in May 1975.

In following up on a number of the specific project activities that were recommended by the 1974 workshop, the Electronic Instrumentation and Metrology Group of the Electrosystems Division has designed and developed:

1. An audio frequency phase angle calibration standard.
    a. Continuous 2 Hz to 50 kHz frequency range.
    b. Programmable 0.1 volt to 100 volt rms dual output channels.
    c. Phase difference resolution of 1 part in 2^{8}, or approximately 0.0014 degrees.
    d. Systematic uncertainty of ±(0.005-0.030) degrees.
2. Precision digital-to-analog (D/A) reference converter standards.
    a. 18 and 20 bit resolution.
    b. Voltage (±10V) and current (±100 ma) outputs.
    c. Linearity of 1 to 2 ppm of full scale.
    d. 100 to 50,000 conversions per second.
    e. Low noise and thermal drifts (< 0.5 ppm/°C).
3. Accurate measurement standards using sampled-data techniques.
    a. Low frequency (0.1 - 120 Hz) sampling ac voltmeter with four decade (0.01, 0.1, 1.0, and 10 volt rms) ranges.
        i. Two cycle measurement interval (e.g., 20 second reading of 0.1 Hz input signal).

ii. Rms measurement accuracy of ±0.2% of reading.

iii. Fast Fourier Transform computation to display total harmonic distortion (THD).

b. Wideband (dc to 100 kHz) sampling wattmeter.

i. Based on earlier ac (to 5 kHz) sampling wattmeter prototype.

ii. Accuracy to ±0.1% of full scale range or better.

4. An automatic calibration system for ac voltage and ac/dc difference measurements.

a. Desktop computer-based, automatic system using the GPIB (IEEE-488) interface.

b. Elimination of a thermoelement (TE) comparator with ac/dc difference measurements accurate to better than 50 ppm (20 Hz - 20 kHz) and 100 ppm (20 kHz - 100 kHz).

c. Use of accurate, low noise TE measurement circuitry for higher accuracy (10 ppm or better), and faster measurement cycles (under development).

d. Documented software with the use of digital and graphical displays.

In all of the above developments, a considerable amount of new or improved measurement methodology has already been achieved. This work on sophisticated electronic laboratory standards has led to more convenient ways of testing the parameters of associated instrumentation. New NBS calibration services are now available for audio frequency phase meters, low frequency (0.1 - 10 Hz) ac voltmeters and sources, and 12-18 bit data converters.

It should also be noted that there have been several developments related to the aforementioned items such as means for characterizing sample/hold (S/H) amplifiers, gating and "viewing" circuits useful for making settling time measurements, and dynamic test methods for analog-to-digital (A/D) converters and transient recorders. The amplitude parameters (e.g., dynamic gain error, and sample-to-hold offset) of S/H amplifiers can now be measured using transformer bridge techniques with an accuracy of 50 ppm for signal frequencies up to 50 kHz. Aperture time (or, the sample time delay) and other time parameters can be determined with uncertainties of 4 ns, absolute, and 1 ns, relative, between two units under test. Present NBS diode bridge sampling gate and viewing circuit designs allow detection of voltage settling time errors of ±200 μV within 400 ns and ±2 mV(2000 μV) within 20 ns. The measurement of current settling time to within ±1 μA can be made in as short as 35 ns. Static tests developed so far for precision data converters (available as a routine calibration) include complete transfer function errors due to gain, offset, integral and differential linearity, with uncertainties on the order of 2-4 ppm. Dynamic testing for A/D converters (available on a

Special Test basis) provides a measure of the additional dynamic linearity errors caused by both electrical and thermal settling times in the measurement circuits of A/D converters. Also, the equivalent rms input noise for A/D converters can readily be measured to an uncertainty of about 20 percent.

All of these efforts are establishing a foundation on which to provide better metrology and calibration support for measurement systems and automatic test equipment (ATE). The work to develop more versatile NBS laboratory standards and associated test methods is being augmented by efforts to develop rigorous testing and calibration strategies by which to minimize the number of test points required in order to achieve the required level of confidence. Thus, both designers and users of ATE can have a systematic, time-efficient approach to the test and calibration process.

The papers contained in this special publication describe some of the measurement techniques, physical standards , and associated apparatus that have been developed by the staff of the Electronic Instrumentation and Metrology Group, and were the subjects of the presentations of the 1983 seminar on Digital Methods in Waveform Metrology. Our work continues in most of these efforts, and we look forward to being able to present and publish additional results in the future.

Barry A. Bell
Group Leader
Electronic Instrumentation and Metrology
Electrosystems Division

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PREFACE

ELECTRONIC INSTRUMENTATION AND METROLOGY GROUP
ELECTROSYSTEMS DIVISION

The Electrosystems Division is a part of the Center for Electronics and Electrical Engineering in the National Engineering Laboratory of NBS. The mission of the Division is to develop methods for measuring and analyzing electrical and electronic components, modules, instruments, systems, and the materials used in their construction in terms of performance and functional parameters as they affect the measurement capabilities of equipment in practical applications.

The Electronic Instrumentation and Metrology Group of the Division carries out projects which involve the development of standards and measurement methodology to support modern, high-speed electronic instrumentation that generally covers signals in the frequency range from dc to 1-10 MHz. New physical reference standards and associated test methods are being developed for directly evaluating the performance of data converters and transient waveform recorders, phase angle meters, RMS AC voltmeters and calibrators, precision function generators, and wideband signal analyzers. This work requires the design of experimental techniques and the construction of prototype circuits, subassemblies, instrument standards, and test/calibration systems. Staff of the Electronic Instrumentation and Metrology Group are prepared to provide the following services in these technical areas.

CALIBRATION - New NBS calibration services are available for low frequency (0.1 Hz - 10 Hz) ac rms voltage, phase angle measurements (2 Hz - 50 kHz), and transfer function parameters of 12-18 bit data converters.

RESEARCH AND DEVELOPMENT - In dc and low frequency electronic instrumentation, metrology to meet your special needs; assistance in solving measurement problems and improving your metrological capability.

DESIGN AND CONSTRUCTION - Special prototype instrumentation standards in limited quantities when there are no commercial sources.

TRAINING AND COOPERATIVE PROGRAMS - Seminars and individual training in appropriate aspects of dc and low frequency measurements, cooperative R & D projects with industry, postdoctoral research associateships.

SEMINAR AGENDA

DIGITAL METHODS IN WAVEFORM METROLOGY

OCTOBER 18, 1983

8:00 am Registration (B162)

8:30 am Welcome and Overview (A62)

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PRECISION WAVEFORM SYNTHESIS

9:00 am Digital Waveform Synthesis Techniques (A62)

N. M. Oldham - Electrosystems Division

9:45 am Phase Angle Standards and Calibration Methods (A62)

R. S. Turgel - Electrosystems Division

10:30 am Coffee Break

10:45 am Waveform Synthesis Lab (A132) and (B157)
(Discussion and Demonstration)

12:00 pm Lunch

SESSION II:

PRECISION WAVEFORM SAMPLING

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D. R. Flach - Electrosystems Division

1:45 pm Dual-Channel Sampling Systems (A62)

G. N. Stenbakken - Electrosystems Division

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2:45 pm Waveform Measurement Lab (B157) and (A158)
(Discussion and Demonstration)

4:30 pm End of Session

6:45 pm Dinner for Participants

NOTE: All sessions will be held in the Metrology Building (Bldg. 220).
The room number for each session is indicated in parenthesis.

SEMINAR AGENDA (Continued)

DIGITAL METHODS IN WAVEFORM METROLOGY

OCTOBER 19, 1983

SESSION III:

DATA CONVERTER CHARACTERIZATION

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T. M. Souders - Electrosystems Division

9:15 am Settling Time Measurements (A62)

H. K. Schoenwetter - Electrosystems Division

10:00 am Coffee Break

10:15 am Data Acquisition/Conversion Lab (A158) and (A132)
(Discussion and demonstration)

11:45 am Lunch

SESSION IV:

INSTRUMENTATION METROLOGY

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2:45 pm Informal Laboratory Discussions (all labs)

4:00 pm Wrap-Up Session/Feedback

5:00 pm Adjournment

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ABSTRACT

Modern electronic instrumentation metrology in the low frequency regime (dc-10 MHz) was discussed in lecture talks and papers presented at NBS, Gaithersburg, MD on October 18-19, 1983. The seminar program was organized into four main session topics, as outlined in the Seminar Agenda (see pp. viii and ix).

This special publication contains complete papers providing more technical details of the subjects presented at the seminar. For the sessions on Precision Waveform Synthesis, Precision Waveform Sampling, and Data Converter Characterization, six formal papers are given describing the hardware and software techniques used for developing NBS laboratory standards and apparatus for testing ac sources and voltmeters, phase angle meters, transient waveform recorders, wideband wattmeters, and digital-to-analog and analog-to-digital converters. For the informal session on Instrumentation Metrology, three subsequent papers have been written for publication. These have been included in the Appendices for completeness.

Key Words: Analog/digital converters; ATE; automatic test systems; conducted EMI; calibration methods; digital/analog converters; digital synthesis; phase angle; photoconductance; sample/hold amplifiers; sampling techniques; settling time; thermal voltage converters.

Disclaimer:

Certain trade names and company products are identified in order to specify the experimental procedure adequately. In no case does such identification imply recommendation or endorsement by the National Bureau of Standards, nor does it imply that the products are necessarily the best available for the purpose. Views expressed by the various authors are their own and do not necessarily represent those of the National Bureau of Standards.

DIGITAL WAVEFORM SYNTHESIS TECHNIQUES

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1. Introduction

The theory describing Digital Waveform Synthesis (waveform generation from digital data) was first described in the 1940s [1,2]. Applications at that time were generally limited to digital communications. With the advent of economical semiconductor memory and high resolution digital-to-analog converters (DACs), waveform synthesizers found wide application in many areas, including the audio industry. Progammable arbitrary waveform generators are now commercially available from several manufacturers.

2. Generation Technique

The most commonly used technique of digital waveform synthesis is shown in figure 1, where samples of the waveform of interest are stored in memory. The programmable clock and counter provide the memory with sequential addresses which are updated at the clock frequency. The memory address may be thought of as angular displacement, while the data corresponding to each address represents the amplitude of the function at equally spaced sample points. Data is applied to a DAC which generates a voltage step proportional to the digital code. Each step is held for one clock period, at which point new digital data is applied to the DAC. The resulting waveform is a staircase approximation of the "sampled waveform", reconstructed from stored data (the term "sampled waveform" is used throughout this text to identify the ideal waveform from which digital data was obtained). The sample-hold process may be described mathematically by a zero order polynomial thus; the reconstruction process is often referred to as a "zero-order-hold."

3. Frequency Response

The impulse response of a zero-order-hold is shown in figure 2. Its corresponding Fourier transform, given by equation (1), describes the frequency response of the reconstruction process [3,4],

$$G[h(t)] = \frac{T \sin(\pi fT)}{\pi fT} = T\,\mathrm{sinc}(\pi fT), \qquad (1)$$

where f = the frequency of interest
T = 1/Fs = the period of the sampling frequency Fs.

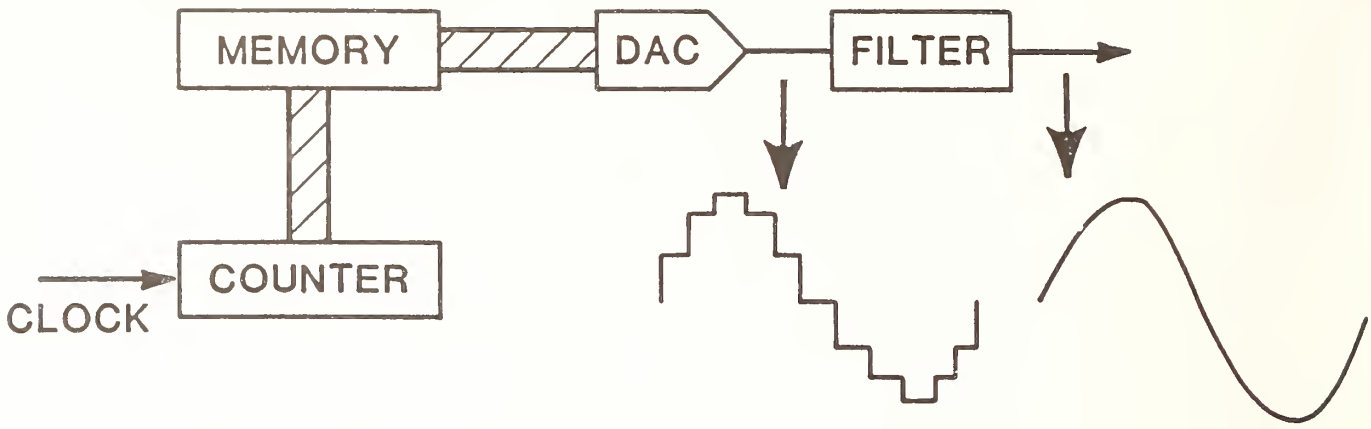
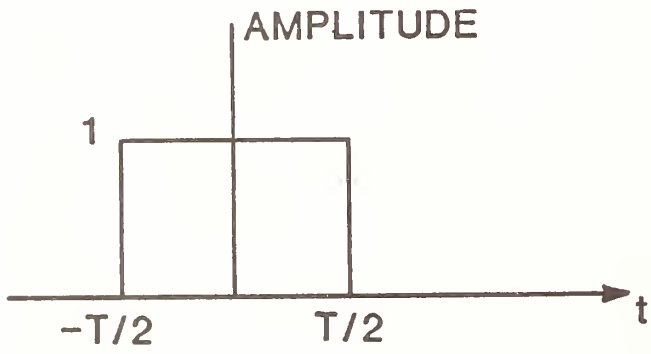


Figure 1. Block diagram of a digital waveform generator.



$$h(t) = 1 \text{ for } -T/2 < t < T/2$$
$$= 0 \text{ elsewhere}$$

Figure 2. Impulse response of the zero-order-hold.

Equation (1) defines the amplitude envelope within which frequency components generated by a zero-order-hold are constrained. The reconstruction contains frequency components not present in the original signal (sampled waveform). These additional components are generated when the sampling frequency and its harmonics are mixed with the signal, forming sum and difference pairs around harmonics of the sampling frequency [5]. If the sampling frequency and the signal are correlated, (an integral number of samples per period of the signal) the frequency components become regular sampling harmonics, F^-_{ik} and, F^+_{ik}, i.e.,

$$F^-_{ik} = iFs - kF \quad \text{and} \quad F^+_{ik} = iFs + kF \tag{2}$$

$$\text{for } i = 0 \text{ to } \infty \text{ (sampling frequency harmonics)}$$
$$k = 1 \text{ to } h \text{ (signal harmonics)}$$

where Fs is the sampling frequency, and F is the fundamental component of the signal. Rewriting equation 1 to include the peak value of each frequency component of the sampled waveform, V_k, the peak value of each reconstructed component, V_{ik}, is given by

$$V_{ik} = \frac{\sin(\pi F_{ik} T)}{\pi F_{ik} T} \left(V_k \right). \tag{3}$$

While equations (1)-(3) hold for any complex signal, the analysis given here will be limited to the synthesis of sinusoidal waveforms where k = 1.

To demonstrate the relationship of the sinc function to the harmonic components in a sampled system, consider the example shown in figure 3. In this example the first sampling component occurs at the 19th harmonic, and has a peak amplitude of approximately 5.2% of the fundamental. Other pairs of sampling components occur about harmonics of the sampling frequency as shown. If all of the sampling harmonics are eliminated with a perfect low pass filter, the remainder is a pure sinewave with a peak amplitude of approximately 99.6% of the original sampled sinewave.

As the number of samples per period is reduced the first sampling harmonic approaches the fundamental and actually appears below the fundamental if there are less than two samples per period. This condition, where the sampling component is folded into the signal bandwidth, is known as aliasing [5], and the signal can no longer be recovered with a low pass filter. This concept is described by the sampling theorem which states that any band-limited signal is uniquely represented by its samples if the sampling rate is at least twice the signal bandwidth [2].

4. RMS Value

The rms value of a pure sinewave is related to the peak value, V_p, by

$$V_{rms} = \left[\frac{V_p^2}{2\pi} \int_0^{2\pi} \sin^2 x dx\right]^{1/2} = \frac{V_p}{\sqrt{2}} \approx 0.707\ V_p. \tag{4}$$

The rms value of a reconstructed sinewave may be expressed in terms of the sum of the squares of the individual voltage steps, V_i.

$$V_{rms} = \left[\frac{1}{m} \sum_{i=1}^{m} V_i^2 \right]^{1/2} \quad (5)$$

where i is the step number, and m is the number of steps. Or, by definition [6], the rms value may be expressed as the sum of the squares of the peak value of each harmonic.

$$V_{rms} = \left[\sum_{0}^{\infty} \frac{V_h^2}{2} \right]^{1/2} \quad (6)$$

where h is the harmonic number.

The general solution for equation (4) may also be obtained from the trapezoidal rule of integration (which is identical to zero-order-hold sampling for functions having a period of 2π). The trapezoidal rule, which is normally an approximation of the integral of a function, provides an exact solution for the $\sin^2$ function [7]. Therefore, the rms value of the reconstruction (including sampling harmonics) is equal to the rms value of the sampled sinewave, $V_p/\sqrt{2}$. The only constraint on this relationship is that the reconstruction consist of at least 3 steps equally spaced within one period (see appendix).

5. Total Harmonic Distortion

The total harmonic distortion (THD) of the reconstructed sinewave is, by definition, [6]

$$THD = \left(\frac{1}{V_1^2} \sum_{h=2}^{\infty} V_h^2 \right)^{1/2} = \frac{1}{V_1} \left(\sum_{h=1}^{\infty} V_h^2 - V_1^2 \right)^{1/2} \quad (7)$$

where h and V_h are the harmonic numbers and the respective peak values of individual harmonics in the reconstruction. V_1 is the peak value of the fundamental component of the reconstruction.

From equations (4) and (6), the expression for THD may be simplified to

$$THD = \frac{1}{V_1} \left(2V_{rms}^2 - V_1^2 \right)^{1/2} = \frac{1}{V_1} \left(V_p^2 - V_1^2 \right)^{1/2} \quad (8)$$

where V_p is the peak value of the original sampled waveform.

Table 1 on the next page shows the relationship between two sinewave reconstructions, one composed of 20 steps and another composed of 200 steps.

Table 1
Comparison of rms error and THD

No. of steps Per Period	Unfiltered Reconstruction rms Error	Unfiltered Reconstruction THD	Filtered Reconstruction rms Error	Filtered Reconstruction THD
20	0	8.9%	-0.4%	0
200	0	0.9%	-0.004%	0

The rms error of the reconstruction is zero from equations (4), (5), and (6), while the THD is inversely proportional to the number of steps per period. If the distortion is removed with a perfect low pass filter, the remaining sinewave will have an rms error which is inversely proportional to the square of the number of steps per period.

The properties of synthesized sinusoidal waveforms described above represent theoretical limitations based upon ideal sampling. In practice, the reconstruction accuracy is further limited by a number of hardware parameters, some of which are described below.

6. Quantization

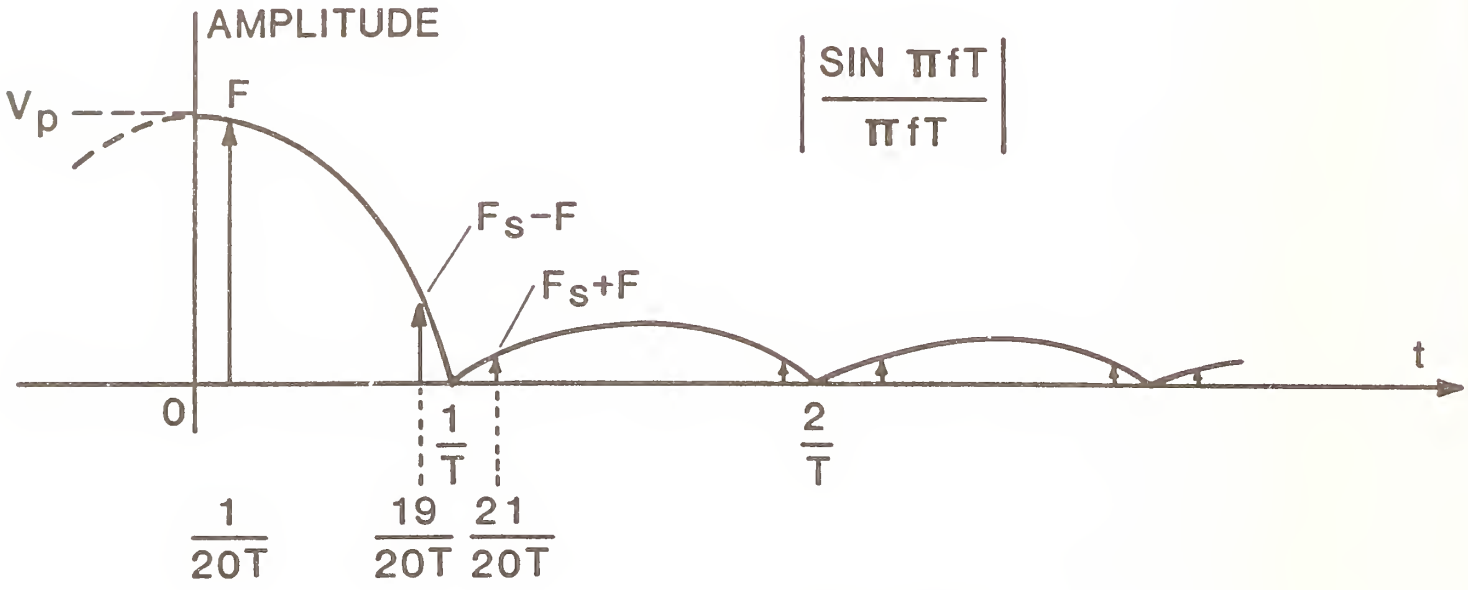
Although the sampled data which describes the waveform can be calculated with very high precision, they are ultimately rounded to a resolution of one least significant bit (LSB) of the generating DAC. The normalized magnitude of this quantization level is given by $q = 1/2^n$, where n is the number of bits in the DAC. The result of quantization is an error at each step in the reconstruction which varies randomly between $\pm q/2$ and adds noise to the synthesized waveform. The noise is wideband and falls within the signal bandwidth [1]. The noise power P_n is given by

$$P_n' = \frac{1}{q} \int_{-q/2}^{q/2} x^2 \, dx = q/12, \tag{9}$$

where x is the quantization error which varies from -q/2 to + q/2. The actual noise power, P_n, depends on the bandwidth of the low pass filter used to eliminate sampling components. Hence,

$$P_n = \frac{q^2}{12} \cdot \frac{\text{filter bandwidth}}{\text{1/2 sampling frequency}}. \tag{10}$$

SPECTRUM OF 20 STEP SAMPLED SINEWAVE



$$\text{AMPLITUDES:} \qquad F = \frac{\text{SIN}(\pi/20)}{\pi/20} = 0.996$$

$$F_S - F = \frac{\text{SIN}(19\pi/20)}{19\pi/20} = 0.052$$

Figure 3. Example of a reconstructed sinewave composed of exactly 20 equally spaced steps per period, where F is the fundamental component, $F_S = 1/T = 20F$ is the sampling frequency, and V_p is the peak value of the original sampled sinewave.

Figure 4. a. Glitch caused by switching skews at the major transition.
b. Typical glitches encountered in sinewave generation.

The signal power, P_S, is the square of the rms value which may be expressed in terms of n [8]. Thus,

$$P_s = \frac{V_p^2}{2} = \frac{V_{p-p}^2}{8} = \frac{(2^n q)^2}{8}, \qquad (11)$$

where V_{p-p} is the peak-to-peak value, which may be described in terms of the full scale range of the DAC ($2^n q$).

From (10) and (11), the power signal to noise ratio (SNR) for a waveform generated by an n bit DAC (followed by a typical low pass filter with a bandwidth of 3/8 of the sampling frequency) is

$$SNR = \frac{P_s}{P_n} = \frac{(2^n q)^2}{8} / \frac{3q^2}{48} = 2^{(2n+1)}. \qquad (12)$$

The SNR, expressed in dB, is 10 times the logarithm of this number, which may be simplified to

$$SNR = 6n + 3. \qquad (13)$$

Quantization errors are compounded if the DAC output is not a linear representation of its input. Nonlinearity is caused by individual bit errors and by superposition (summation) errors. Worst case SNR may be predicted from equation (13) by expressing the DAC in terms of equivalent bits. For example, a 12 bit DAC with 2 LSB nonlinearity is equivalent to a perfect 10 bit DAC (if the nonlinearity errors are randomly distributed), and will thus provide a SNR of 63 dB instead of the ideal 12 bit value of 75 dB.

7. Glitches

The term "glitch" refers to an unwanted pulse which is quite often difficult to capture and measure. In digital-to-analog converters, the largest glitches are caused by skews in switching times. Figure 4 shows how a full-scale pulse may occur if the most significant switch is slightly faster than the other switches.

Other glitches are caused by capacitive coupling between the digital and analog portions of each switch which provides paths for transferring charge from the logic signal to the analog output. Glitch energy is often expressed in coulombs (ampere-seconds) or volt-seconds.

Glitches introduce wideband harmonics which reduce the fidelity of the reconstructed waveform. Glitch distortion may be reduced by sampling the DAC output after the glitch has occurred (with a sample-hold amplifier) and holding that value through the next transition.

8. Timing Jitter

Cycle-to-cycle instability of the sampling frequency will cause fluctuations in the step width of the reconstructed waveform which, like quantization, results in wideband noise. It has been shown [8] that the SNR, expressed in dB, of a synthesized sinewave followed by a low pass filter of bandwidth F is given by

$$SNR = \frac{1}{(2\ \sin(\omega/2))^2(\Delta T/T)^2 FT}\ , \qquad (14)$$

where $\omega = 2\pi f$ (fundamental frequency)
T = sampling period
ΔT = peak jitter.

For audio frequency applications, transistor-transitor logic (TTL) jitter is sufficiently small to produce a SNR of 100 dB. At higher frequencies, or when using a slower family of logic circuits, jitter noise may become significant.

9. Amplifier Limitations

Conventional DACs provide a current output which is generally converted to a proportional output voltage with an operational amplifier. If the reconstructed waveform is unfiltered, the amplifier step response may seriously degrade fidelity. Slew-limiting, overshoot, and ringing may alter the rms value and introduce significant distortion. If however, the reconstructed waveform is filtered and the current to voltage conversion is performed by an active low pass filter, many of the amplifier limitations disappear. For example, sufficient band limiting by the filter will slow the amplifier response to the point that its slew limit is never exceeded. Noise introduced by the amplifier is generally more than 100 dB below the signal and may be negligible compared to quantization noise.

10. Other Techniques

A number of other techniques for synthesizing waveforms have been described in the literature. These vary from simple circuits which switch weighted voltage sources in a zero-order-hold reconstruction, to a rather complicated approach which synthesizes sinusoids from Walsh functions [9]. The latter uses a series of weighted Walsh functions to construct a sinewave in much the same way that a square wave can be constructed from a Fourier series. The frequency response of this approach differs from the sine look-up table method in that the sampling harmonics are defined by the sinc function, while the fundamental component is defined by the sinc^2 function.

The techniques described so far have employed a zero-order-hold reconstruction filter which does not interpolate between samples. The desired signal may be recovered by removing the sampling harmonics with a low pass filter (as long as the sampling theorem is satisfied).

In theory, a better initial approximation of continuous waveforms can be made by a first-order-hold which provides linear interpolation between samples. A special case of the first-order-hold, with a delay of one sample period is known as the linear-point-connector [4] (shown in figure 5). Its impulse response, h(t), shown in figure 5b, is a triangular function with the following fourier transform;

$$G[h(t)] = \left[\frac{\sin(\pi fT)}{\pi fT}\right]^2. \qquad (15)$$

The frequency response of the linear-point-connector is thus described by a $sinc^2$ envelope which greatly attenuates the sampling harmonics. Table 2 shows the magnitudes of the fundamental and first pair of sampling harmonics of a sinewave reconstructed from a zero-order-hold (ZOH) and a linear-point-connector (LPC).

Table 2

Magnitude of the frequency components generated by 20 and 5 step ZOH and LPC reconstructions, expressed as a percentage of the sampled sinewave.

Harmonics	20 Steps		5 Steps	
	ZOH	LPC	ZOH	LPC
Fundamental	99.6	99.2	93.5	87.5
1st Sampling Harmonic	5.2	0.3	23.4	5.5
2nd Sampling Harmonic	4.7	0.2	15.6	2.4

The implication is that the LPC can produce a sinewave of similar fidelity with one quarter the number of steps required by the ZOH, thus quadrupling the output frequency capability of the generator. In practice, the LPC is much more difficult to implement, and any increase in frequency range must be traded for increased circuit complexity. NBS is currently investigating several techniques for implementing the LPC, as well as a novel approach for describing arbitrary waveforms using an orthogonal set of Triangular Basis functions (not discussed in this paper).

11. NBS Sinewave Generator

To investigate the merits of digital synthesis techniques, a microcomputer controlled prototype ac voltage generator was developed at NBS [10]. The practical limitations in predicting the rms value (one of the calculable parameters) of the generated sinewave were evaluated using a thermal voltage converter, and errors of less than 50 ppm were observed between 10 Hz and 1 kHz. At higher sinewave frequencies, dynamic errors in the generator become significant, causing rms uncertainties of 100-200 ppm through the audio frequency range. However, because of the inherent amplitude stability of digital generators, it is possible to characterize the frequency response and apply software corrections based upon a least squares fit. The resulting

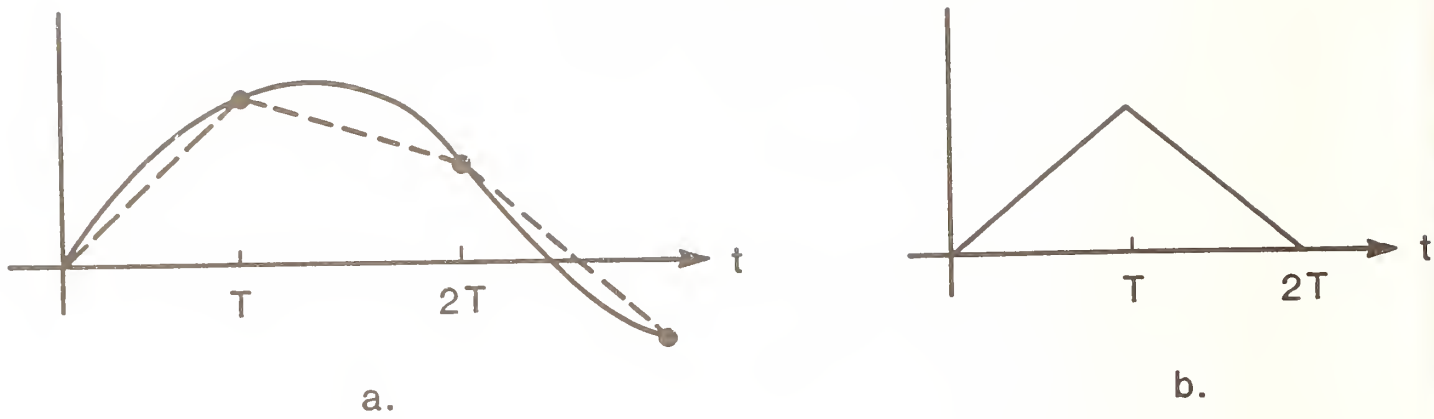
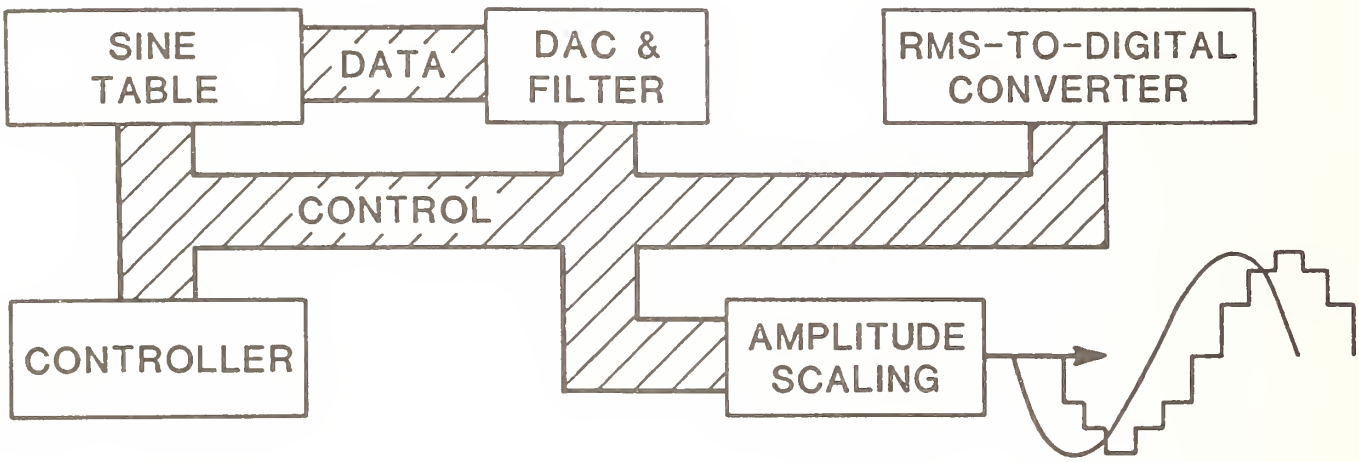


Figure 5. a. Linear-point-connector reconstruction.
b. Impulse response of the linear-point-connector.



BLOCK DIAGRAM OF THE AC REFERENCE STANDARD INCLUDING AN INTERNAL THERMAL CONVERTER (RMS-TO-DIGITAL CONVERTER) AND HIGH ACCURACY AMPLITUDE SCALING.

Figure 6. Programmable NBS ac source.

generator produces a 7 volt rms sinewave with 50 ppm rms uncertainty over a frequency range of 1 Hz to 50 kHz. High resolution dividers scale the waveform between 0-7 volts rms with little degradation in accuracy, providing a programmable ac source as shown in figure 6. Since the generator retains its frequency response characteristic for long periods, a daily gain calibration is sufficient to maintain the 50 ppm uncertainty. The source will ultimately provide fast, automated calibration support for a variety of rms responding voltmeters.

While the above described source has a number of advantages over conventional generators, its frequency range is somewhat limited. The frequency of digitally generated sinewaves is dependent upon the DAC speed and the number of steps per period used in the reconstruction. In practice, a 16 bit DAC cannot be operated at sampling frequencies much higher than 500 kHz. To maintain a THD of less than 1.4% (less than 100 ppm of the signal power is contained in the harmonics)requires 128 (2^7) steps per period, allowing an upper sinewave frequency of about 4 kHz. For higher frequencies, 12 bit converters can be operated at 10 MHz to generate sinewave frequencies of 78 kHz (128 steps) to 2.5 MHz (4 steps). Below 4 steps per period, the digital generator has little advantage over a conventional function generator.

12. Conclusions

Digital waveform generators provide an economical means for producing stable, high fidelity signals over a limited frequency range. Some theoretical properties and practical limitations have been described, with emphasis on sinewave reconstruction.

Digital synthesis, however, is particularly suited to the construction of complex waveforms which are extremely difficult to produce by conventional analog means. Instrumentation is commercially available which allows the user to program arbitrary waveforms with 8-12 bit resolution at sampling frequencies up to 5 MHz.

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APPENDIX

The rms value of a pure sinewave is given by

$$V_{rms} = \left(\frac{V_p^2}{2\pi} \int_0^{2\pi} \sin^2 x \, dx \right)^{1/2} = \left(\frac{V_p^2}{2\pi} \int_0^{2\pi} 1/2 \, (1-\cos 2x) dx \right)^{1/2} = \frac{V_p}{\sqrt{2}} . \quad (16)$$

The trapezoidal rule of integration provides a means for evaluating the integral of a function by dividing it into a finite number of trapezoids of equal width. The sum of the areas of each trapezoid represents an approximation of the integral which may be expressed as

$$\int_a^b f(x)dx \approx h\left(\frac{f(a)}{2} + f(a+h) + \ldots + \frac{f(b)}{2}\right) \quad (17)$$

where $h = \frac{b-a}{n}$, n = number of integration intervals.

For functions of period 2π, $f(a) = f(b)$ so equation (17) may be rewritten

$$\int_a^b f(x)dx \approx h(f(a) + f(a+h) + \ldots + f(a+(n-1)h)) . \quad (18)$$

The second term of (18) represents a summation of rectangular areas identical to a perfect zero-order-hold reconstruction. In addition, equation (18) provides an exact solution for the class of functions sinx, cosx, sin2x, cos2x....sin(n-1)x, cos(n-1)x, sinx [7].

From (16), the rms value of a pure sinewave requires an evaluation of a cos2x term and the trapezoidal rule gives an exact solution for $(n-1) \geq 2$. Therefore the rms value of the reconstructed sinewave equals the rms value of a pure sinewave ($V_p/\sqrt{2}$) where the reconstruction consists of at least 3 equally spaced steps.

PHASE ANGLE STANDARDS AND CALIBRATION METHODS

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1. Introduction

Phase angle is one of the quantities that describes the properties of ac circuits. Its measurement is important in a wide variety of applications which include analysis of feed-back amplifiers, servo-systems, communications circuits, oscillator and filter circuits, transformer characteristics, and other applications ranging from navigation to power systems and even to plasma physics experiments. Accuracy requirements differ widely for many of these applications, but from the point of view of the standards laboratory, calibration accuracy must be sufficient to handle precision commercial phase-angle meters with typical measurement uncertainties of 0.05 degrees and resolution of 0.01 degrees [1,2].

2. Definition

Phase angle is a measure of the time delay between two periodic signals expressed as a fraction of the period in units of angle. In theory, a phase angle is defined only if both signals have identical waveform and frequency. In practice, the waveforms are never completely identical, but usually only the phase angle between the fundamental component of each waveform is of interest. The extent to which harmonic distortion and noise influence the measurement depends somewhat on the operating principle and construction of the phase meter. For instance, zero-crossing type phase meters can be made to be insensitive to even harmonics and to in-phase odd harmonics under certain circumstances [3,4].

3. Measurement Principles

The measurement of phase angle is essentially a time ratio measurement, i.e., determining the delay between corresponding points on two waveforms relative to the signal period. Various methods to accomplish this are described in the literature. For example, a variable delay line can be used in conjunction with a phase detector [5]. Another method first translates all test signal frequencies to a chosen fixed frequency, with a heterodyne mixer which preserves the phase relationships, and then adjusts for a null in a phase detector using a calibrated phase shifter in one signal path [6]. Probably the most widely used method in precision laboratory phase meters relies on zero-crossing detectors in combination with a counter-timer or a pulse-width modulation scheme. The counter-timer method is relatively simple (see figure 1), but resolution is limited by the clock frequency of the timer. For instance, to obtain a resolution of 0.01 degrees with a 20 MHz clock, the frequency of the signals to be measured cannot exceed 550 Hz. At the cost of considerable complication, this limitation can be overcome by using fractional pulse-counting and pulse-averaging techniques [7,8,9].

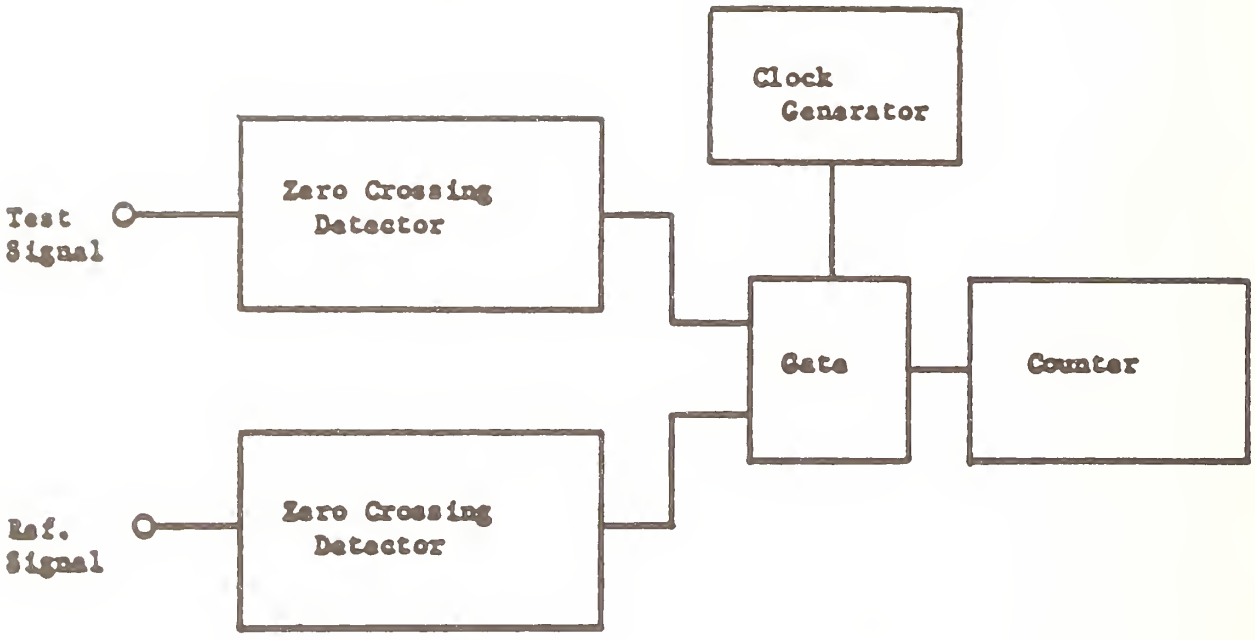

Figure 1. Counter-Timer Method.
The time elapsed between zero crossings of the "test" and "reference" signals is determined by counting clock pulses gated by the zero-crossing detectors.

In the pulse-width modulation scheme, the width of the pulse is made equal to the phase delay between the signals being measured with the period of the pulse equal to the period of the signal. In this case, high-frequency limitations occur only when the pulse rise time is no longer small with respect to the pulse width. Normally, many pulses are averaged to reduce the effects of jitter and noise.

Other phase-measuring instruments are often referred to as phase-angle voltmeters, vector voltmeters, or gain-phase meters. These instruments measure the magnitude of a signal as well as its phase angle with respect to a reference signal or, in the case of gain-phase meters, the ratio of the two input signals and the phase difference between them. The phase-measuring principle may either use zero-crossing phase sensitive detectors or phase shifting circuitry. The phase-measuring capabilities of these instruments are generally designed to be less accurate by an order of magnitude or more than those of high precision phase meters.

In recent years a completely different approach has also been used to measure phase. It is based on sampling the input signals periodically, digitizing the values obtained and storing them in memory. The phase angle is then determined from the data using a Fourier transform algorithm [10]. If the sampling frequency is an exact multiple of the fundamental of the signal frequency, a discrete Fourier transform can be used to calculate the phase angle. In this case the solutions are exact, and the algorithm does not contribute to the error. In the more general case, using asynchronous sampling, a fast Fourier transform is required and exact solutions are not always possible. The computation then contributes to the overall error of the determination. Commercial instruments based on this method have not yet been developed to the full accuracy possible with these techniques.

4. Sources of Error

4.1 Timing Errors

In practical zero-crossing type phase meters, the trigger levels of the zero-crossing detectors are never quite identical, which can lead to errors. In figure 2 (a), two input waveforms are shown displaced by a phase angle Φ and with an angular frequency ω. The time delay between the "true" zero crossings is Φ/ω. If one of the detector levels is offset relative to the other by a voltage E_{dc} then a timing error, Δt, is introduced (figure 2 (a,b)) which is equivalent to an apparent phase shift $\Delta\Phi = \omega\Delta t$, and this phase shift leads to an error in the measurement. It will be noted from figure 2 (a) that the timing errors Δt have opposite signs at the zero crossings with rising and falling slopes. It is possible, therefore, by averaging measurements made at both zero crossings to compensate for this type of error, as indicated in figure 2 (c).

A second source of such timing errors is distortion in the input waveforms. Harmonic components cause shifts in the zero-crossing points which, unless they are identical in both waveforms, will result in apparent phase shifts. Even harmonics cause symmetrical timing errors similar to those resulting from voltage offsets and can be compensated by averaging measurements at rising and falling zero crossings. However, components of odd order harmonics, which are not in phase with the fundamental, produce timing errors which cannot easily be eliminated and, therefore, limit the accuracy of the measurement.

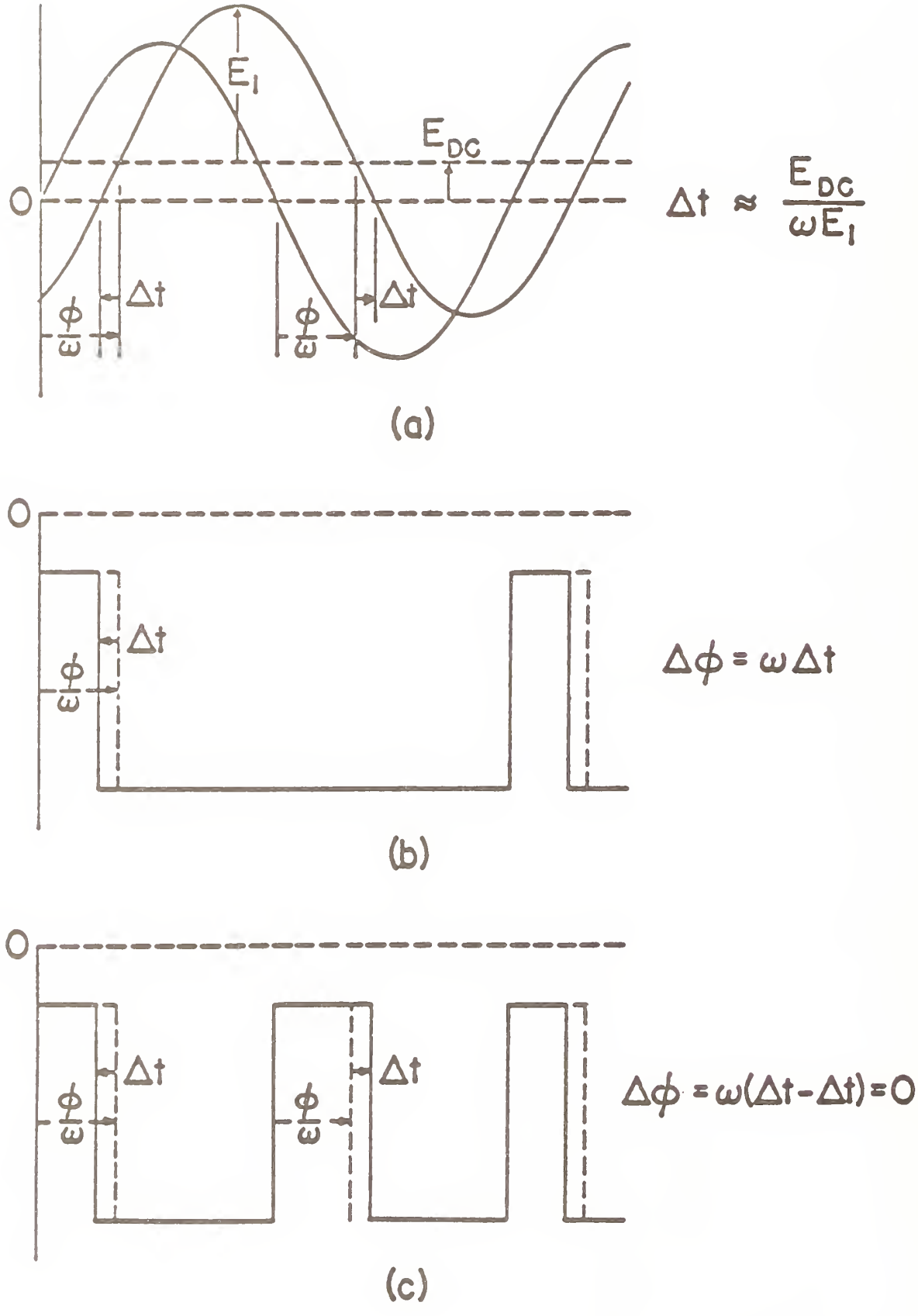

Figure 2. Offset Phase Errors.
Unequal voltage offsets in the zero-crossing detectors results in timing errors with opposite sign at the positive-and negative-going zero crossing.

Other timing errors arise from unequal propagation delays through the input amplifiers. To reduce the time taken to trigger the zero-crossing detectors, input amplifiers are generally over-driven. However, in practice, especially when the difference of the amplitudes of the input signals is large, it is not possible to have identical delays in both channels. Unequal delays produce spurious phase shifts, and the effect increases with signal frequency. For highest accuracy, therefore, both input signals should have almost equal amplitudes.

4.2 Stray Coupling

Combining part of the signal from one channel with that of the other causes an apparent phase shift, the magnitude of which is usually phase angle as well as frequency dependent. Careful design in the isolation of the signal paths and power supplies in the input stages of the phase meter, as well as in the external circuit, is required to minimize this effect.

4.3 Readout Offset and Linearity

In phase meters using pulse-width modulation, a dc level proportional to phase angle is produced that is often displayed on a digital panel meter. Offsets in the zero- and full-scale values of the panel meter, as well as non-linearities can contribute significantly to the phase meter error. Usually, the zero- and full-scale point are adjustable, but non-linearity errors cannot easily be eliminated.

5. Phase-Angle Calibration Standards

From a theoretical point of view there is really no need for a phase standard, because a phase angle is essentially a ratio and, therefore, not tied to fundamental units. A bootstrap procedure is possible by which a phase-angle calibration could be accomplished [11,12]. In practice, however, the cumulative errors inherent in such a procedure make attainment of high accuracy difficult. There is, unfortunately, no one simple way to verify accuracy, and a variety of approaches have to be relied upon to gain confidence in the measurement. A phase calibration standard, therefore, is a very useful tool from a practical point of view.

Traditional designs of phase calibration standards are based on two output signals in quadrature, established by means of auxiliary adjustments of inductive or capacitive circuit elements, or active equivalents. Calibrated voltage dividers are then connected between these outputs and the signals are mixed to provide the desired phase shift. This approach has been successful, but there are drawbacks. The frequency sensitive adjustments that are required for each calibration point can drift with time and temperature, making time consuming readjustments necessary. Accuracy specifications typically vary from 0.015 degrees to 0.060 degrees, depending on frequency range [13].

6. NBS Phase-Angle Calibration Standard

The design objectives for a new phase-angle calibration standard at NBS were aimed at an instrument that was intrinsically very stable, but at the same time, one which would respond and settle quickly to a new set of operating

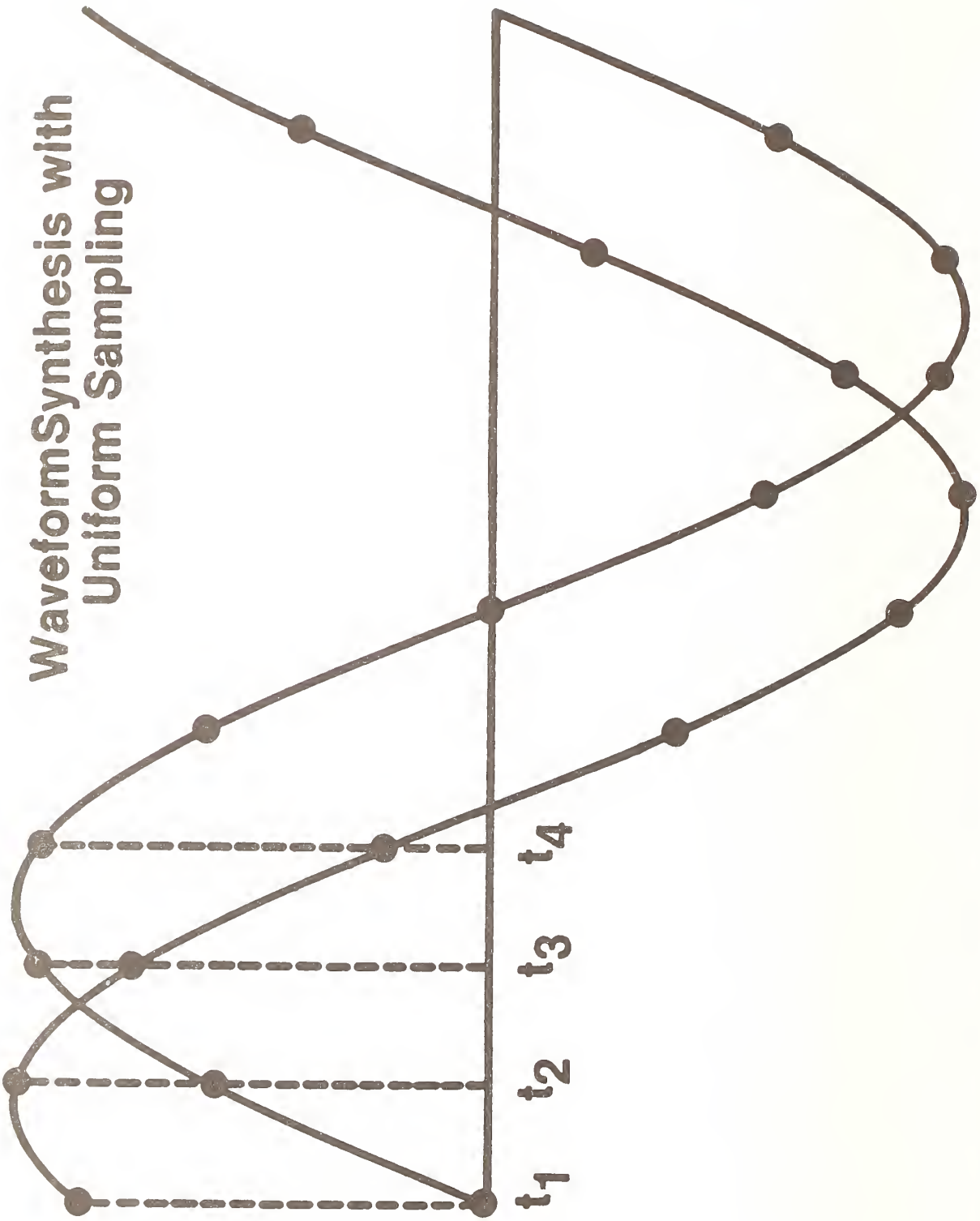

Figure 3. Waveform synthesis with uniform sampling.
Two sine waves with a known relative phase displacement are synthesized by calculating the appropriate values of the sine function at regular time intervals and converting the calculated values to voltages.

Functional Block Diagram of NBS Phase Standard

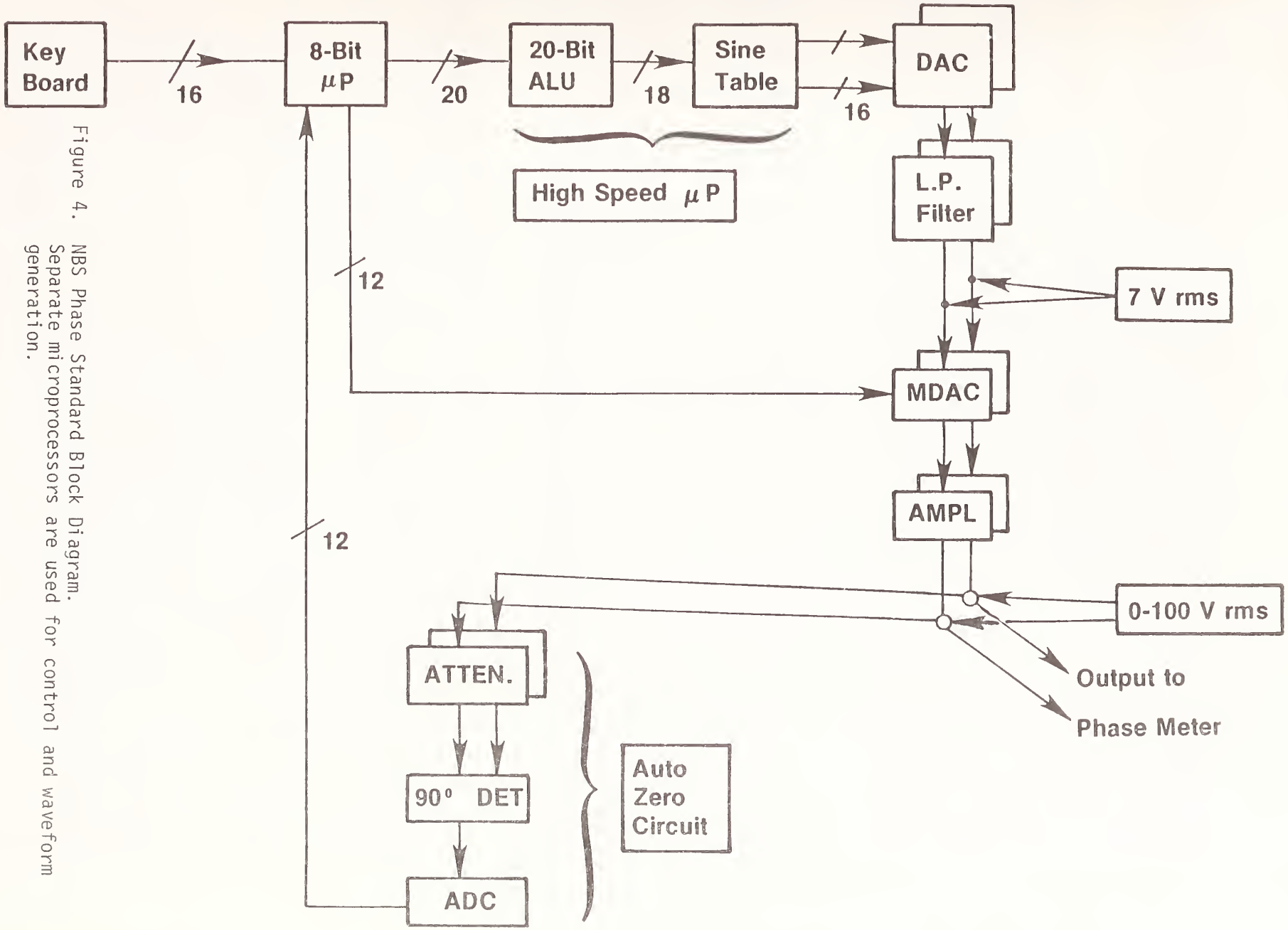

Figure 4. NBS Phase Standard Block Diagram. Separate microprocessors are used for control and waveform generation.

conditions [14,15]. Ease of operation for the user was another important consideration. These goals were met with a method that synthesized two signals with a known phase angle between them, using digital techniques. The method has the advantage that the desired phase angle is primarily determined by calculation and not by frequency sensitive circuit elements.

The NBS Phase Standard is a calibrator which produces two sinusoidal output signals with a phase angle that can be set to an accurately known value. The signals, which can range from 2 to 5000 hertz and 0.1 to 100 volts, can be applied directly to the phase meter under test during calibration. The phase resolution is one part in 2^{18}, or approximately 0.0013 degrees. The resulting phase angles have an uncertainty of ±0.005 degrees, with somewhat larger uncertainties when the amplitudes of the output signals are unequal. The output phase angle, frequency, and amplitudes are microprocessor controlled, and are adjustable from the front panel keyboard, or via an IEEE-488 bus interface (which is being developed).

6.1 Method of Signal Generation

The sinusoidal output signals are generated by simultaneously calculating points at equal intervals along both waveforms (t1, t2, t3, etc., see figure 3) and by converting these sets of numerical data points to analog output voltages, using dual channel digital-to-analog converters with appropriate filtering.

Referring to the block diagram of figure 4, operating parameters such as phase angle, signal frequency, and amplitudes are entered from the keyboard, converted to binary information by an 8-bit microprocessor, and transmitted to a 20-bit microprocessor which generates the numerical data for the desired waveforms. The phase angle (phase difference) between the two waveforms is determined by the computed relative signal magnitudes of the two waveforms at each of the sample points (figure 3).

The phase angle and frequency information from the keyboard is latched into registers of the arithmetic-logic unit (ALU) which also calculates the sample locations along the time axis (figure 3) in terms of the corresponding angles. These angles are then transformed into their sine function values using a combination look-up table and interpolation method. At the same time, the values calculated for the previous sample point are applied to a pair of 16-bit digital-to-analog converters.

The resulting 7-volt rms analog signals are filtered to remove harmonics introduced by the sampling process. A programmable gain stage and a high-voltage amplifier provide outputs from 0 to 100 volts, independently variable for each channel.

To compensate for possible differential phase shifts in the two channels, an auto-zero circuit is provided that measures and corrects relative phase errors under software control. The method is based on a quadrature detector and a sequence of measurements that compensates for internal phase and dc offsets. The output of the quadrature detector is digitized and fed back to the waveform generating hardware.

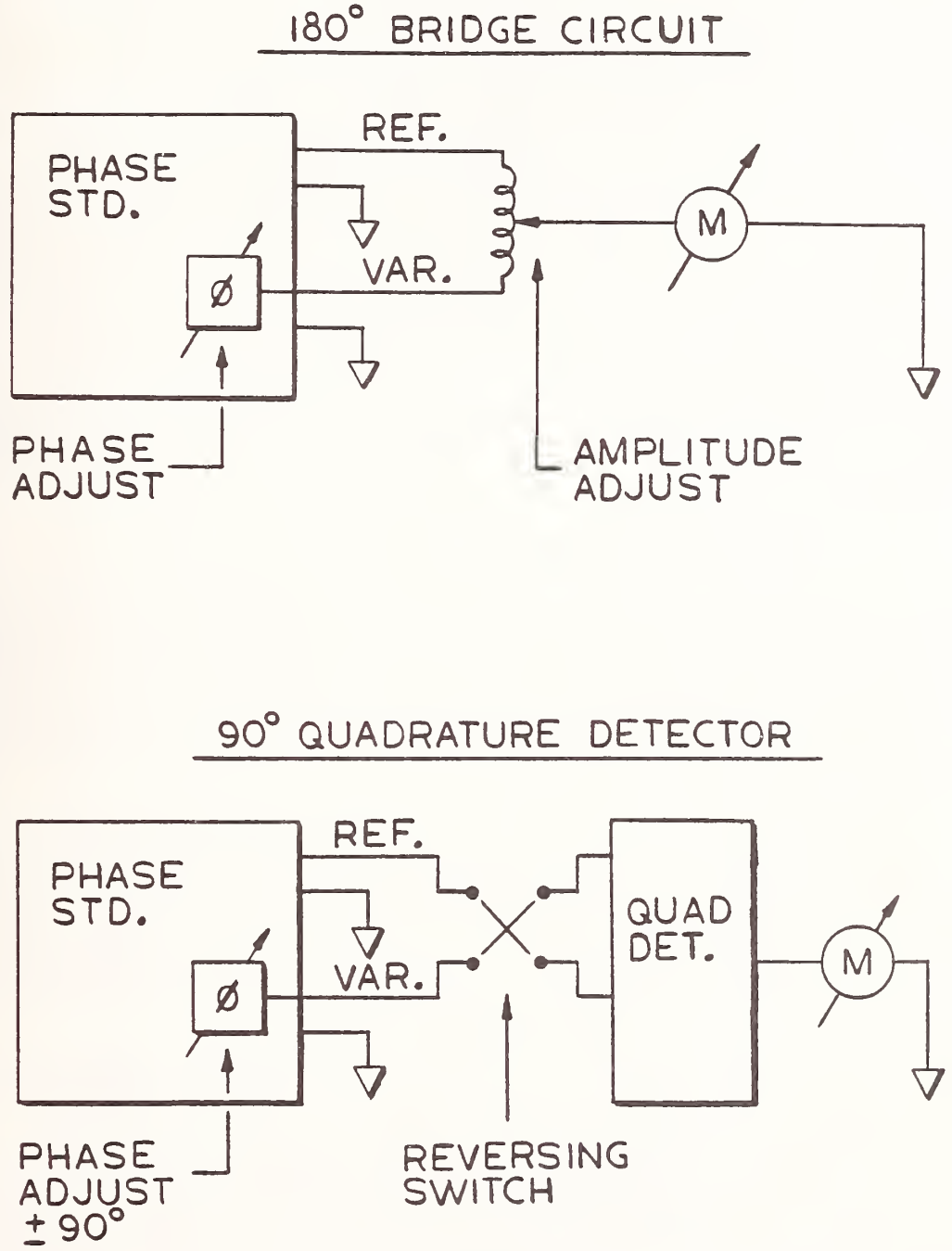

Figure 5. Test Methods
Two independent null methods are used to check fixed points on the phase angle scale (180° and 90°) of the Phase Standard.

6.2 Frequency Range Extension

The upper frequency limit of the Phase Standard is currently being extended to 50 kHz. The same principle of digital-waveform generation is used beyond 5 kHz, except that calculations are not carried out in real time. Calculated values for each waveform are stored in high-speed memory when setting up each range, and are then strobed to the converters to produce the higher-frequency output signal at a rate ten times faster than the data transfer during "low" frequency operation. For practical purposes, however, the change in the operating mode is not noticeable to the user. The price paid for the increase in speed is a reduction in the angular resolution as well as in accuracy. Angular resolution is a function of the number of possible voltage levels of the converter, as well as the number of sample points for each waveform. With present technology, the best compromise appeared to be the retention of the same number of sample points per waveform at the upper-frequency limit combined with an increase of the digital-to-analog conversion speed by a factor of ten. To gain speed, a reduction of the word size from 16 to 12 bits was necessary. This resulted in a loss of phase resolution by a factor of approximately 5 as determined by computer simulation. In practice, the uncertainty of the phase angle is related not only to the resolution but also to other factors, including the techniques available to make precision phase measurements at these higher audio frequencies.

6.3 Performance Evaluation

Analysis shows that for a 16-bit word, the quantization signal-to-noise ratio is close to -100 dB [16]. This noise amplitude at the zero crossing is roughly equivalent to an uncertainty of the phase of the zero crossing of just under one millidegree. In practice, actual converter characteristics will degrade this value. Experimental verification shows that the linearity of the NBS Phase Standard varies from better than 0.002 degrees at low frequencies to 0.005 degrees at 5 kHz.

Fixed points on the phase scale can be calibrated by two independent methods as shown in figure 5. In the 180-degree bridge circuit, the two outputs from the phase standard are set to a nominal phase angle of 180 degrees and applied to the ends of an inductive divider. The center tap of the divider is connected to a tuned null detector (M). The bridge circuit is balanced by adjusting the amplitude ratio with the divider tap, and the phase deviation by offsetting the Phase Standard from the nominal value.

A similar calibration test can be carried out at a nominal phase angle of 90 degrees by using an (external) quadrature detector [17]. Since at quadrature, the null reading is independent of signal amplitudes, only a phase-balancing adjustment is necessary. By interchanging inputs to the quadrature detector, voltage and phase offsets in the quadrature circuit can be compensated and so provide a high-accuracy quadrature measurement with an uncertainty of the order of 1 or 2 millidegrees.

7. Other Digital Phase Standards

Phase standards, using digital synthesis of sinusoidal waveform, but different principles to obtain phase displacement between the output signals, have been developed by the National Physical Laboratory in Britain and by the Japan Electric Meters Inspection Corporation (figures 6,7). The British design

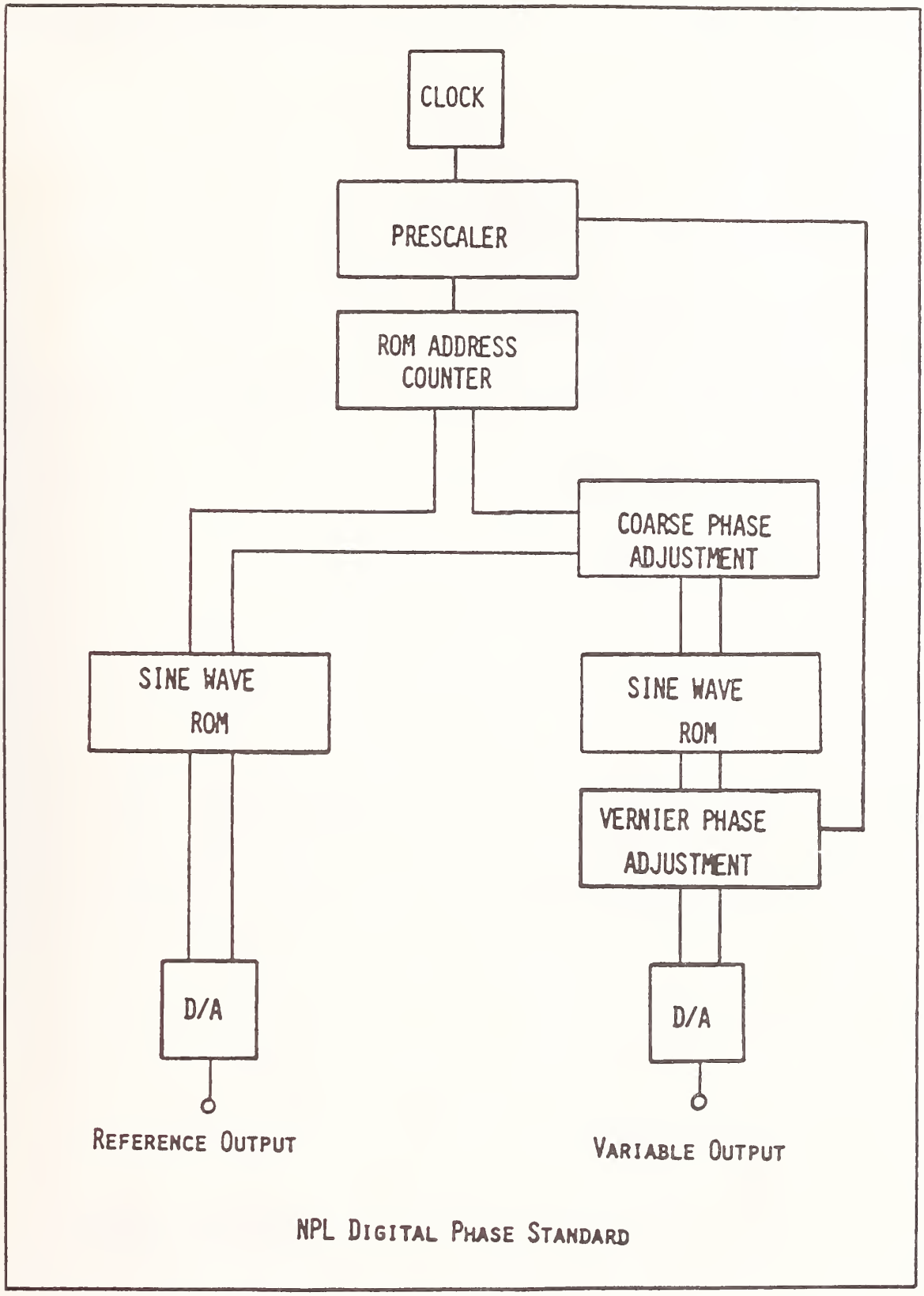

Figure 6. NPL Phase Calibration Standard.
Phase shifts are obtained by time delays equal to whole numbers and fractions of clock periods.

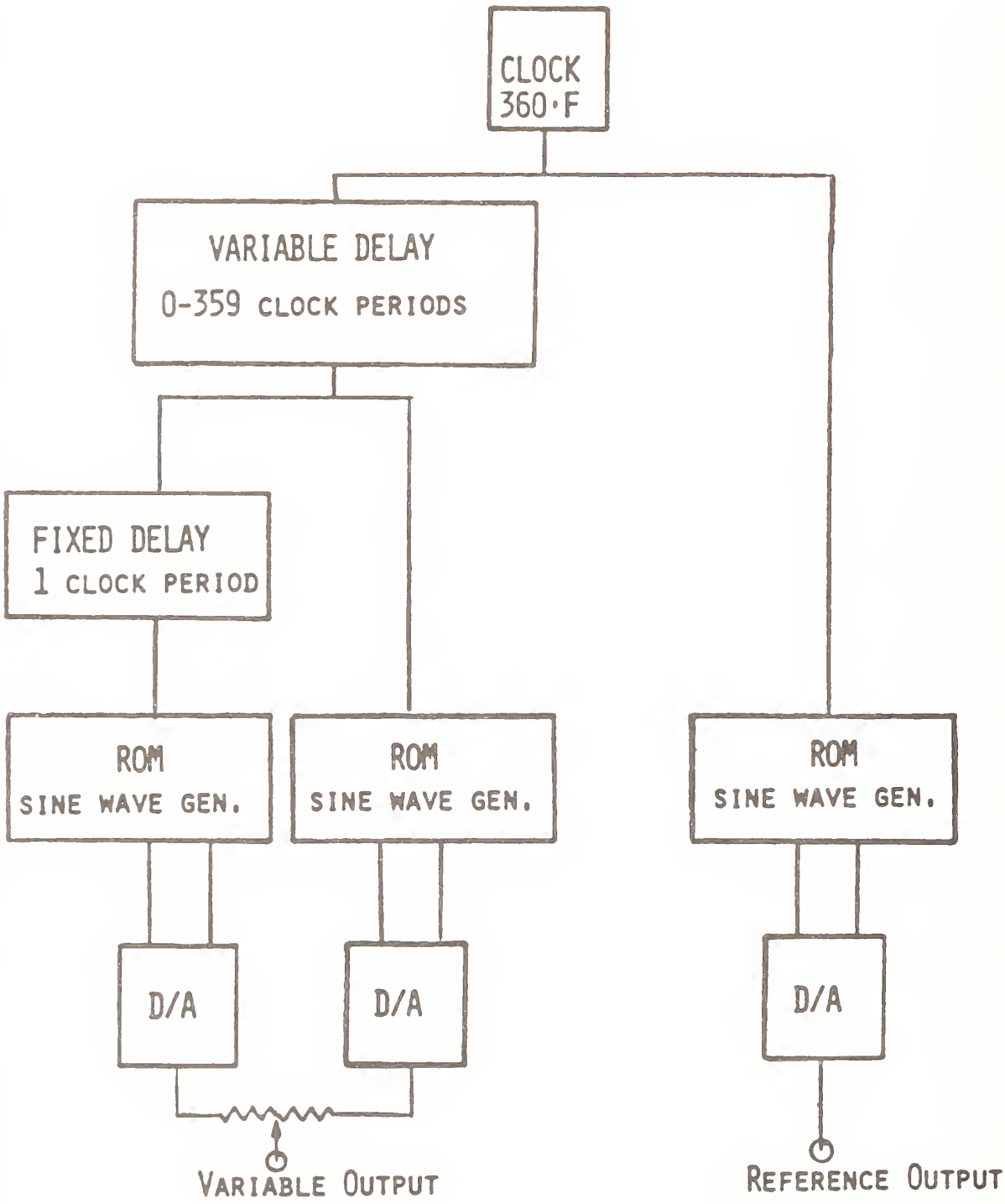

Figure 7. JEMIC Phase Calibration Standard.
Three waveforms are generated two of which have a fixed 1° phase difference and can be displaced relative to the third by 1° steps. Fine adjustment is obtained by analog mixing of the two signals 1° apart.

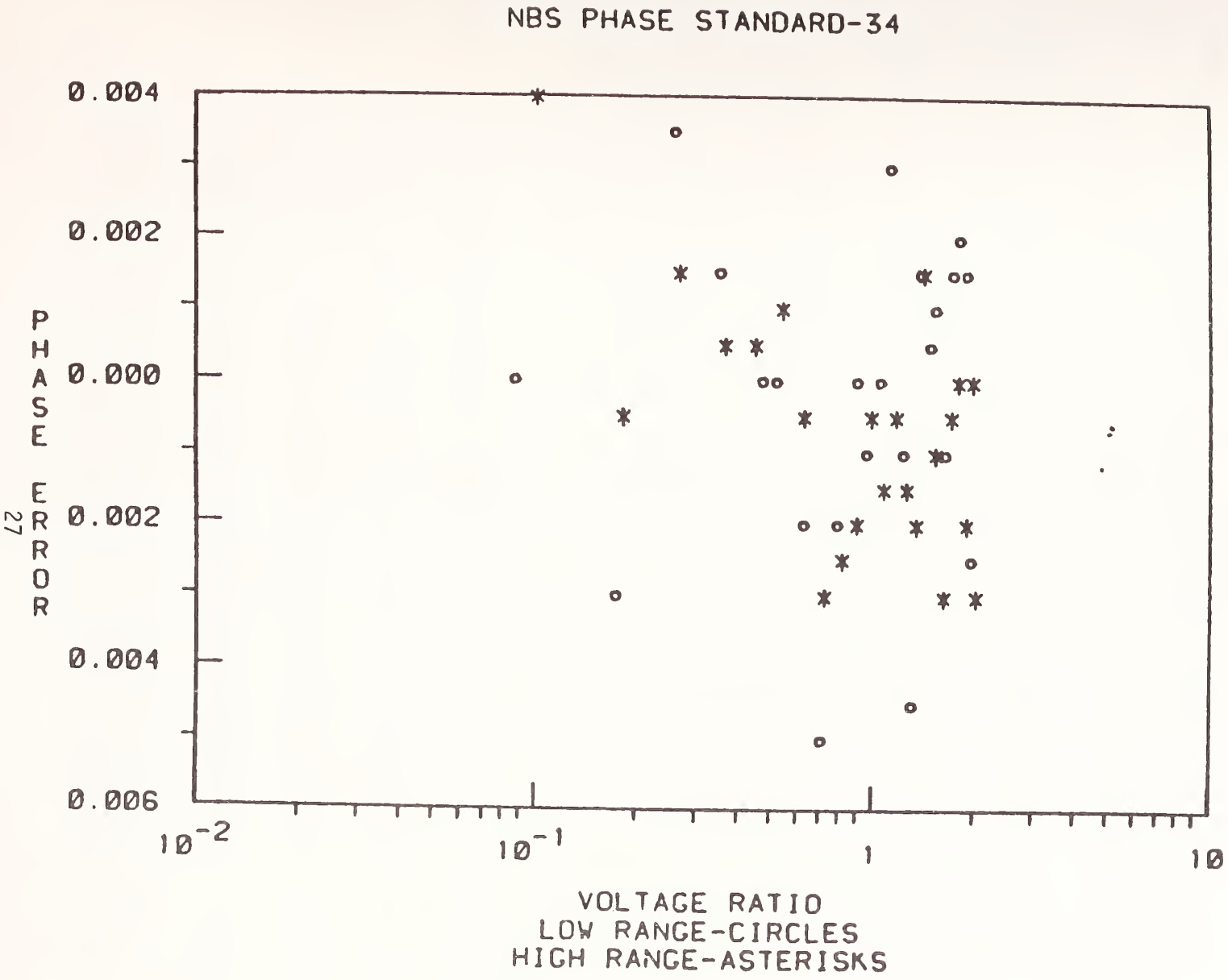

Figure 8. Phase Meter Correction as a Function of Signal Voltage. An example of meter corrections determined at randomly selected phase angles for various signal levels.

uses time delays equal to integer and fractional clock periods to provide a set of phase angles with a resolution that is frequency dependent [18]. The Japanese design uses three synthesized sine wave outputs two of which are switchable through 360 degrees with a 1-degree resolution and arranged so that there is a fixed one degree difference between them. Angular fine adjustment can then be obtained by connecting a voltage divider across the two variable outputs that are one degree apart [19].

8. Calibration Strategies

Phase-angle measurements of electrical waveforms involve three parameters: phase, frequency, and amplitude. To perform a complete calibration over this three-dimensional "measurement space" would require a large number of test points, an uneconomical procedure in most cases. Therefore, two different approaches must be considered, depending on the purpose of the calibration. When detailed corrections are required over a limited number of ranges, then measurements at a representative set of phase angles are made at the amplitude and frequency parameters specified. It is good practice to select phase angles to be measured in a random order, from a set of test points that are fairly evenly distributed over the range from 0 to 360 degrees. It is also advisable to take several readings at each phase angle to establish the repeatability of the measurement process and then to fit the data points to a model, linear or non-linear. This procedure not only provides calibration values between actual test points, but also improves the basis for the uncertainty statement.

Quite often, the purpose of the calibration is to determine whether the phase meter is within its specifications on various ranges. As pointed out, checking each range fully becomes uneconomical, and a different strategy is necessary. This approach involves a trade-off of detailed knowledge of the corrections for every possible range for a composite picture of measurement uncertainties. Such a composite picture is obtained by varying one parameter, e.g., amplitude, and measuring a limited number of randomly selected phase angles at each value of the parameter. The phase error can then be plotted against the value of the parameter (amplitude). Similarly, the relationship of the phase error bounds vs. frequency can be determined. A typical plot of this kind is shown in figure 8.

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CHARACTERIZATION OF WAVEFORM RECORDERS

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1. Introduction

Although transient waveform recorders have been in use for more than 15 years, no commonly accepted test procedures were in use for these instruments, particularly for the evaluation of errors associated with dynamic input signals. Within the past few years, however, manufacturers and others have begun to use test methods which involve the application of steady state, repetitive waveforms to evaluate the dynamic performance characteristics of these instruments. Parameters measured with these procedures include quantizing errors, differential linearity errors, integral linearity errors, missing codes, and aperture uncertainty. An advantage of the above method is that a sinusoidal waveform is employed for many of the tests, and these are easily generated and well characterized for frequencies up to 1 MHz. Some disadvantages include the necessity for generating low distortion sine waves at frequencies above 1 MHz, and the difficulty of generating linear ramp-like waveforms with the required linearity at repetition frequencies greater than a few kilohertz.

The tests described herein are essentially those in which the final output of the test is the result of digital signal processing on the waveform recorder's digital output, as shown in figure 1. Other types of tests, some of which don't require digital signal processing, are described in [1-4]. Different interpretations of the results of some of the tests described in this paper are also given in [4]. Figure 2 shows a test system similar to figure 1, except that the waveform recorder is partitioned into a series of functional modules. The tests described in this paper can also be applied to analog-to-digital (A/D) converters, if the functional modules shown in figure 2 can be provided. By the addition of a ranging amplifier, a sample-hold (S/H) amplifier, digital memory, and control logic, the A/D converter is configured to emulate a waveform recorder, one of whose properties is that the digital output is available only as a complete record, and random access to the individual codewords is usually not possible. A summary of the errors measured with the continuous waveform tests is given on page 28 of [21].

One test procedure to be described gives a "global" description of the waveform recorder errors already mentioned--a nonlinear, least squares, fitted sine wave test. Other test procedures described include a histogram test which measures differential linearity errors and missing codes, a fast Fourier transform test which measures integral linearity errors, and an aperture uncertainty test.

However, waveform recorders are often used to measure non-repetitive, transient input signals. Commonly accepted test procedures for characterizing the performance of waveform recorders with transient input signals are almost non-existent. One of the reasons for this situation is the difficulty of

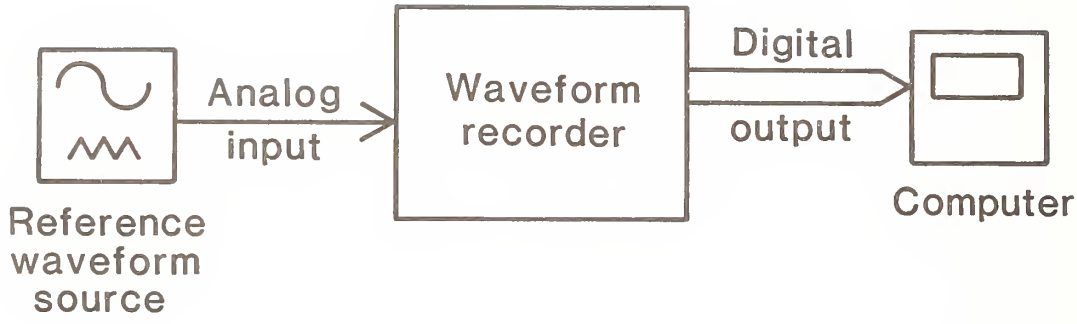

Figure 1. General measurement approach.

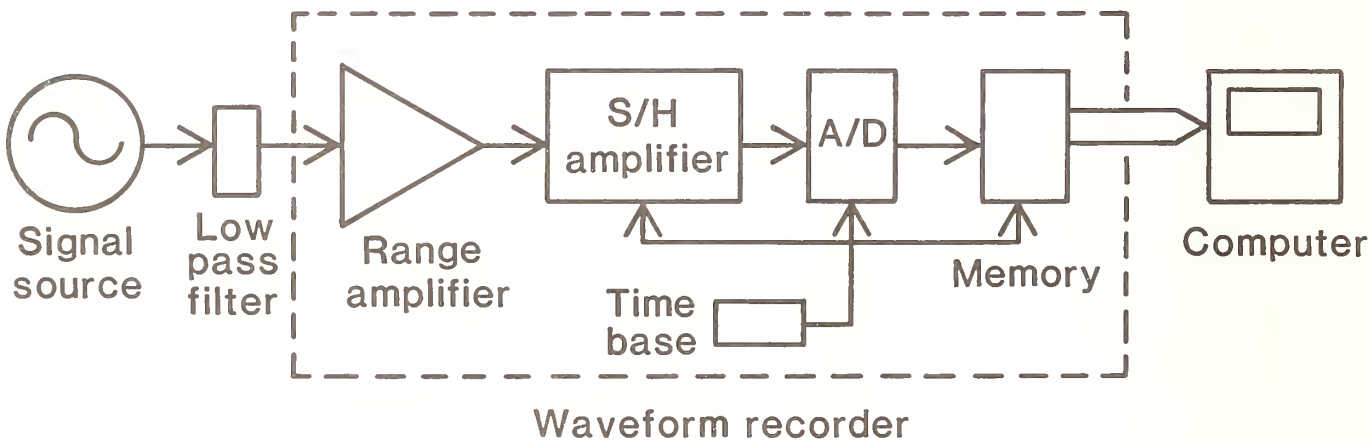

Figure 2. Test measurement system for sine wave inputs.

generating well characterized transient waveforms [5]. Also, the interpretation and application of the test results obtained from steady-state test procedures to the measurment of a transient input signal proves to be difficult. One test derived at NBS is described which measures the difference in the sample sets obtained between a steady state sine wave and a transient single-cycle sine wave [19]. The initial results of a transient step response test set under development is also described.

2. Sine Wave Curve Fit

One test method developed in the past several years for the characterization of waveform recorders is the "effective number of bits" test [1,2,6-10]. In this test, a high quality, low distortion, cyclically repeatable sine wave source is used at a frequency less than one-half of the sampling rate of the waveform recorder (to satisfy the sampling theorem), and uncorrelated with the sampling rate. For all of these tests, it is assumed that the sampling frequency is uniform and there are no missed samples. The requirement that the frequency of the applied sinusoidal input be uncorrelated with the recorder's sampling rate is extremely important, since this criteria establishes a randomness that allows the test procedure to be modeled as a Gaussian-like process. In the diagram of figure 2, the low pass filter (in this case functioning as an anti-aliasing filter) removes from the sine wave source harmonic components with a frequency greater than one-half of the sampling frequency of the recorder that could be aliased into the spectrum of the waveform recorder's output. Harmonic components with an amplitude greater than one-half of a least significant bit (LSB) of the test recorder can cause significant test errors and should be eliminated.

The sine wave test can be considered to be a "global" description of the sampling errors in a waveform recorder. This means that the recorder's errors are all averaged together to compute one numerical value, the effective number of bits, that is representative of the overall performance accuracy of the recorder.

The effective number of bits is computed using the waveform recorder's digital output record obtained with the sine wave source (and filter) applied to the input. A sine wave is then generated in software that is a best fit to the recorder's output record. Differences between the best fit software-generated sine wave and the digital output record are assumed to be errors in the waveform recorder. Normally, a digital record of 1024 points or less is transferred to the computer for signal processing. Using a technique that makes use of a nonlinear least squares curve fit routine [1,2,10], a sine wave of the form $Y = A + B \sin(CX + D)$ is fitted to the recorder's digital output data. A,B,C, and D are constants determined by the software fit routine from the X and Y data to obtain a best fit sine wave. The fit routine minimizes the expression

$$E = \sum_{k=1}^{M} [Y_k - A - B \sin(CX_k + D)]^2, \qquad (1)$$

where M = number of data points, k is the index for the kth data point pair (X_k, Y_k), X_k is the time the sample was captured, Y_k is the value of the sample, and E is the error function.

The error, E, is minimized by varying the parameters A, B, C, and D which correspond to offset, gain, frequency, and phase, respectively. The error minimum occurs when the four equations for the partial derivative of E with respect to A, B, C, and D are equal to zero:

$$\frac{\partial E}{\partial A} = -2 \sum_{k=1}^{M} (Y_k - A - B \sin(CX_k + D)) = 0$$

or,

$$\sum_{k=1}^{M} (Y_k - A - B \sin(CX_k + D)) = 0 \tag{2}$$

$$\frac{\partial E}{\partial B} = -2B \sum_{k=1}^{M} \sin(CX_k + D)\ (Y_k - A - B \sin(CX_k + D)) = 0$$

or,

$$\sum_{k=1}^{M} \sin(CX_k + D)(Y_k - A - B \sin(CX_k + D)) = 0 \tag{3}$$

$$\frac{\partial E}{\partial C} = -2B \sum_{k=1}^{M} X_k \cos(CX_k + D)(y_k - A - B \sin(CX_k + D)) = 0$$

or,

$$\sum_{k=1}^{M} X_k \cos(CX_k + D)(Y_k - A - B\sin(CX_k + D)) = 0 \tag{4}$$

$$\frac{\partial E}{\partial D} = -2B \sum_{k=1}^{M} \cos(CX_k + D)(Y_k - A - B \sin(CX_k + D)) = 0$$

or

$$\sum_{k=1}^{M} \cos(CX_k + D)(Y_k - A - B \sin(CX_k + D)) = 0. \tag{5}$$

The solution of equations (2), (3), (4), and (5) for A, B, C, and D is complicated and generally involves iterative processes [11,12]. A solution is outlined in [1], and software to implement it is given in [2]. Gain, offset and phase errors are not measured by the curvefit method because these parameters are determined from the waveform recorder's output data.

The rms value of E, which contains the global description of the waveform recorder's errors, is considered to be the "noise" of the system, and since the rms value of the signal S is $B/\sqrt{2}$, the rms signal-to-noise (S/N) ratio can

be computed. From this measurement of the S/N ratio, the effective number of bits, n_1, of the waveform recorder is calculated using the formula

$$n_1 = (S/N - 1.8)/6 \ , \tag{6}$$

where the S/N ratio in (6) is expressed in decibels [1].

To be meaningful, this value of S/N ratio must be compared with the one for an ideal n-bit recorder. The theoretical S/N ratio in the ideal case is based on the quantization noise of the internal A/D converter, which results from the uncertainty existing in the digitization of any unknown input to the A/D converter. Figure 3 depicts the quantizing error of an ideal 3-bit A/D converter. The quantity E shown in this figure is the quantizing error function of the ideal A/D converter. The rms value of the sawtooth waveform represented by E is thus the rms error of the ideal recorder. Figure 4 shows the calculation of the rms quantizing error in the ideal case. In terms of LSB's, where Q is one LSB = (full scale range (FSR))/2^n, then $E_{rms}(\text{ideal}) = Q/\sqrt{12}$. In calculating this ideal rms noise, the assumption is made that the (uncorrelated with the sampling frequency) sine wave input frequency causes a probability distribution of the sine wave values that is uniform throughout the ± 0.5 LSB interval. If this criterion is satisfied, then the S/N ratio for a full scale sine wave input is

$$S/N = \frac{(Q2^{n-1})/\sqrt{2}}{Q/\sqrt{12}} = 2^{n-1}\sqrt{6} \ . \tag{7}$$

Expressed in decibels,

$$20 \log (S/N) = 6.02n + 1.8, \tag{8}$$

for the ideal n bit recorder. As an alternative to the computation of effective bits given in (6), another expression often used is [1]

$$n_1 = n - \log_2 \left(\frac{\sqrt{E}}{Q/\sqrt{12}}\right) \ . \tag{9}$$

Figure 5 is a graphical representation of a portion of a sine wave curve fit. The residuals (data minus fitted curve) for the ideal case will all be within ± 0.5 LSB, and the rms value of the residuals will be $Q/\sqrt{12}$.

Figure 6 shows the residuals from a computer simulation of an ideal 10 bit, offset binary coded A/D converter with 512 sample points. The fit in this case was done using a commercial regression analysis package based on Marquardt's nonlinear least squares method. The value of the rms error was 0.292, which compares favorably with the theoretical value of $Q/\sqrt{12} = 0.289$.

Figure 7 shows the residuals from a 500 point test on an actual 10 bit recorder, sampling at 50 kHz. Note that many of the residuals are well beyond the ± 0.5 LSB limit. The magnitude of the rms error, E, is increased by these residuals, and as equation (9) shows, a larger value of E results in the effective number of bits becoming smaller. In the above case, the effective number of bits was about 7, rather than 10, the resolution of the waveform recorder.

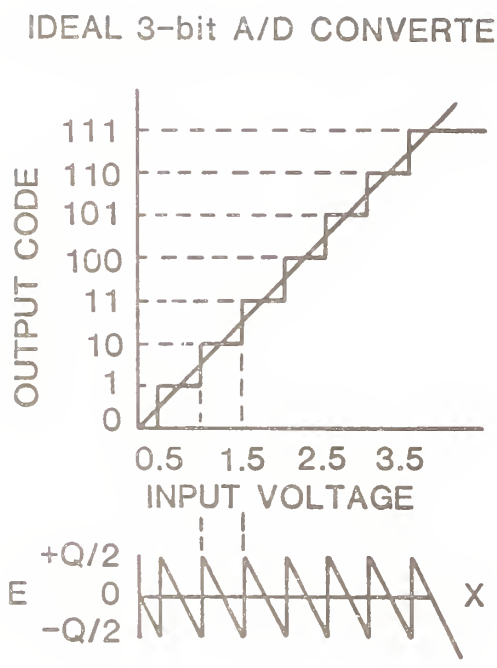

Figure 3. Quantizing error of ideal 3 bit analog-to-digital converter.

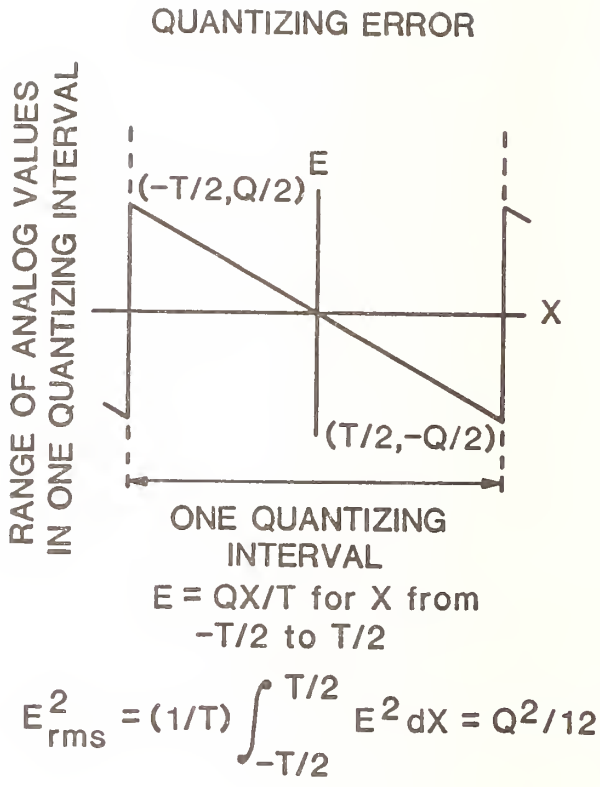

Figure 4. Quantizing error calculation.

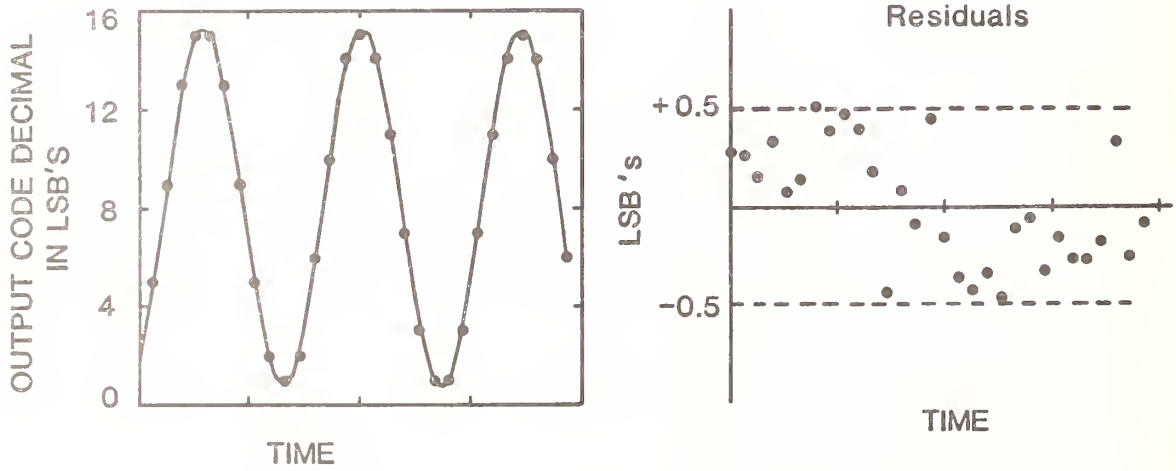

Figure 5. Sine wave nonlinear least squares curve fit to waveform recorder output data and the resulting residuals.

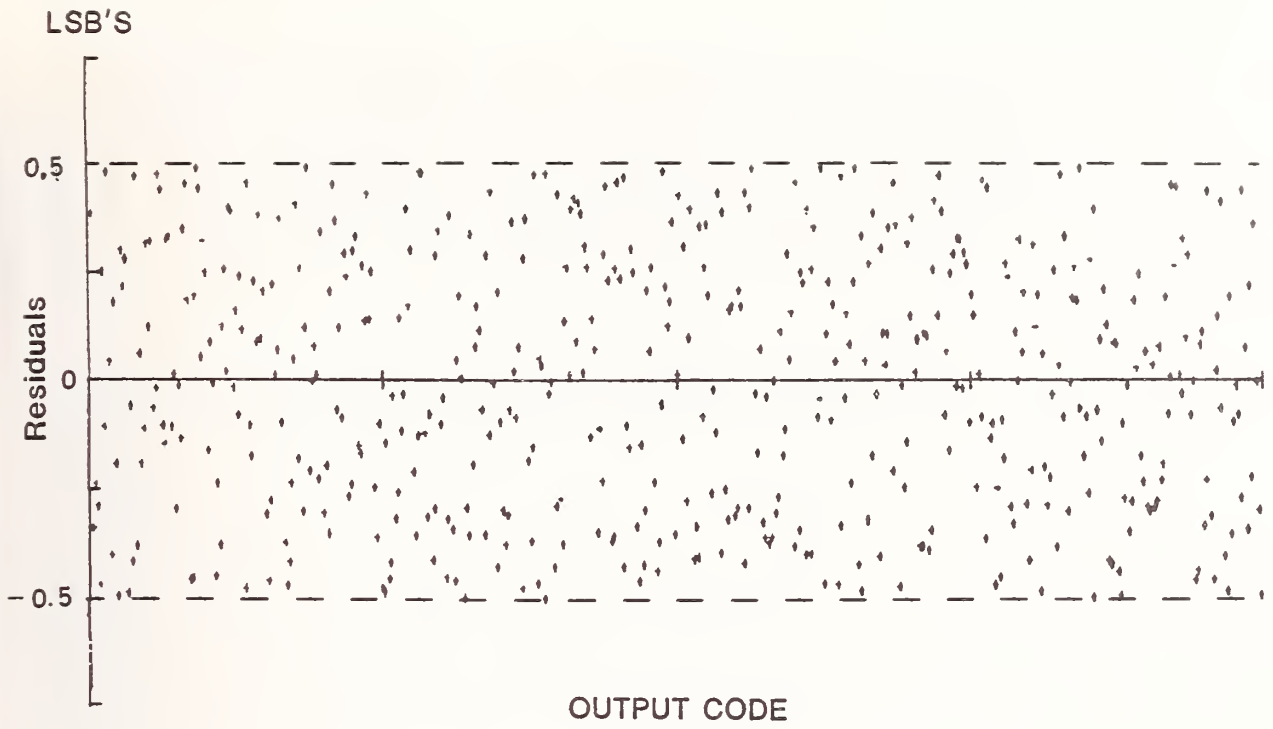

Figure 6. Computer simulation, of the residuals calculated using a nonlinear sine wave durve fit to a 512 sample data point record. Test instrument is a software modeled 10 bit errorless waveform recorder.

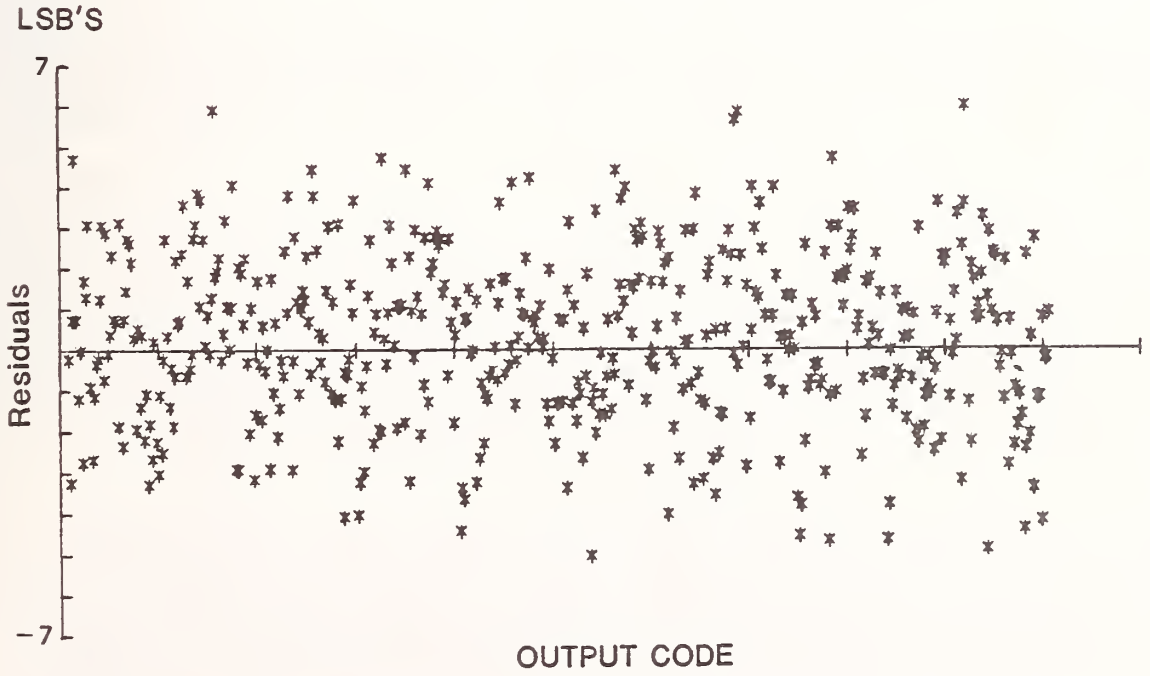

Figure 7. Residuals calculated using a nonlinear sine wave curvefit to a 500 sample data point record. Test instrument was a real 10 bit waveform recorder sampling at 50 kHz.

A plot of the effective number of bits vs. applied sine wave frequency for an 8 bit, 100 MHz sampling rate recorder at an applied voltage of 0.9 of FSR is shown in figure 8. The rapid fall off of effective bits vs. frequency is often observed in waveform recorders. For the recorder used to obtain the plot of figure 8, as the frequency of the input was increased, codes started to be skipped, which reduced the effective number of bits rapidly. These skipped codes, rather than uniform random noise, accounted for much of the decrease in effective bits.

When calculating the S/N ratio and effective number of bits, the amplitude of the applied sine wave has been taken into account. For a peak signal, V, (less than full scale),

$$S/N = 2V(2^{n-1}\sqrt{6})/(FSR). \tag{10}$$

The repeatability of the effective number of bits tests is described in [13]. Test conditions were that a 1 MHz and then 2 MHz sine wave at 0.5 of FSR was applied to a 9 bit recorder sampling at a rate of 20 MHz. Twenty computations of the effective number of bits were made. For the 1 MHz case, the mean value was 8.33 bits with a maximum value of 8.50 and a minimum value of 8.17, while in the 2 MHz case the values were 7.93, 7.77, and 8.07, respectively.

3. Fast Fourier Transform Test

The Fourier transform of a real time continuous signal x(t) is defined as

$$X(f) = \int_{-\infty}^{\infty} x(t)e^{-2\pi ift}\, dt\ . \tag{11}$$

For waveform recorders, the continuous function, x(t), becomes sampled data at uniform time intervals. The implementation of the Fourier transform for a signal, x(t), sampled at a finite number of data points M, and spaced Δt apart, is given by

$$X_d(f) = \sum_{k=0}^{M-1} x(k\Delta t)e^{-2\pi if(k\Delta t)}\ \Delta t\ , \tag{12}$$

and is often called the discrete Fourier transform (DFT). For real data, M data points gives M/2 discrete spectral lines with a frequency resolution of $\Delta f = 1/M\Delta t$. An implementation that greatly speeds up the computation of the DFT are the various algorithms usually grouped under the title of fast Fourier transforms (FFT). Use of these algorithms also brings restrictions on the number of sample points; for the more common implementations, the number of data points must be a power of two as in $1024=2^{10}$.

The FFT test, with a sinusoidal input [1,2,10,14], can be used to compute a S/N ratio, and thus determine the effective number of bits, as described previously. Details of the computation of the S/N ratios with the FFT test and a series of corrective factors which were needed to make the results from the FFT tests approximately equal to the fitted sine wave test are given in [10].

Compared with the fitted sine wave test, the FFT procedure is faster and does not require any initial values for the parameters A,B,C, and D, nor are there any problems with the convergence of the curvefit. Balanced against this advantage is the need to use a window function (Hanning window used for these tests), and the application of a series of correction factors (as explained in [10]) to make the results of the FFT method nearly equal to the curvefit method.

The FFT test is sometimes referred to as an integral linearity error test, since linearity errors in the input amplifiers, attenuators, and internal A/D converter cause harmonics of the input frequency to appear in the output Fourier spectrum. Figures 9(a) and 9(b) are representations of the linearity errors in the functional modules of a waveform recorder. Figure 9(a) depicts an S-shaped transfer characteristic that is typical of many amplifiers. The S-shaped characteristic, if it can be modeled by a series of polynominal terms of degree n (n odd), will generate odd harmonics in the output spectrum up to order n. Figure 9(b) shows a linearity error modeled with an even order polynominal of degree two. Transfer characteristics of this type will generate even harmonics of order n in the output spectrum. Figure 10 is a graph of a FFT spectrum obtained with a computer simulation of a 10 bit recorder with a 0.5 LSB quadratic nonlinearity (n = 2) of the type shown in figure 9(b). This nonlinearity resulted in the second harmonic spectral line shown in figure 10, and reduced the effective number of bits from 10 to 9.35. Figure 11 shows the results of a differential linearity error (wide or narrow code) on the FFT spectrum. On this figure there are five spikes visible in the output spectrum, which are a result of bit 3 of the A/D converter having a code width 0.5 LSB narrower than the ideal case. This condition has reduced the effective number of bits from 10 to 9.35.

The FFT spectrum will also be affected by wide band noise sources which will raise the level of the noise floor. The quantizing noise, a result of the inherent quantization of the input signal by the internal A/D converter, sets a lower limit to the noise floor. The S/N ratio is calculated by taking the rms value of the signal and dividing by the rms value of the remaining spectral lines after allowance for the leakage phenomena [10].

Figure 12 is a plot of an FFT test on a waveform recorder constructed from the functional modules, (see figure 2) which consisted of a S/H amplifier, a 12 bit successive approximation A/D converter, and a 12-bit wide 1024 word random access memory. The large third and fifth harmonics observed in the spectrum were caused primarily by integral linearity errors in the transfer characteristic of the S/H amplifier, like those shown in figure 9(a). Independent measurements on the S/H amplifier verified this nonlinearity in its transfer characteristic, which was still within its linearity specifications.

4. Histogram Test

A histogram is a compilation of the number of occurrences of each codeword in a digital output record [1,2,15-17]. If a triangular or sawtooth waveform of excellent linearity is applied, as shown in figure 13 (with the condition of no correlation of its fundamental frequency and the recorder's sampling rate), then the probability of the occurrence of each code is equal. This result is equivalent to saying that the input waveform has a uniform probability density function.

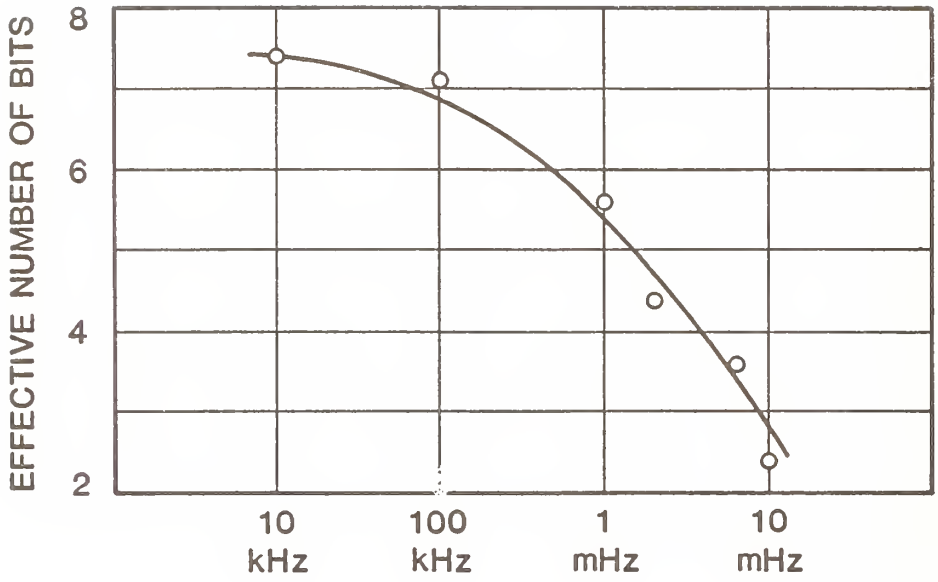

Figure 8. Eight bit recorder with maximum sampling rate of 100 MHz.

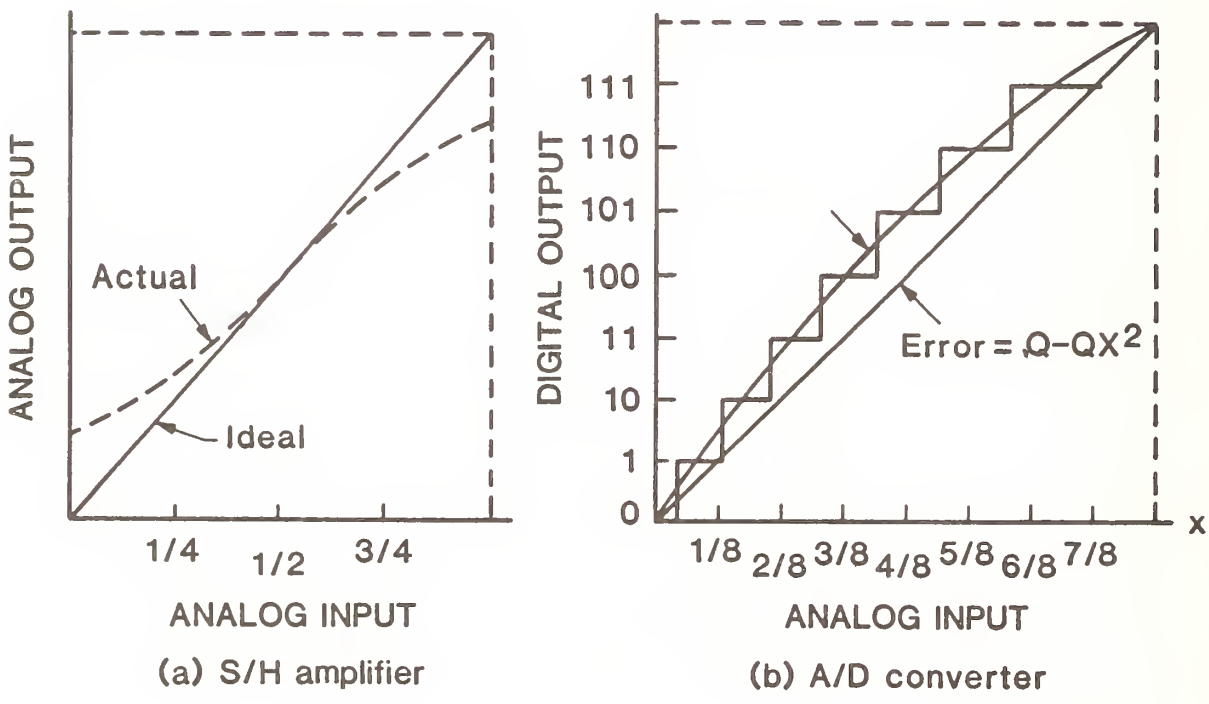

Figure 9. Examples of integral linearity errors in the functional modules of a waveform recorder.

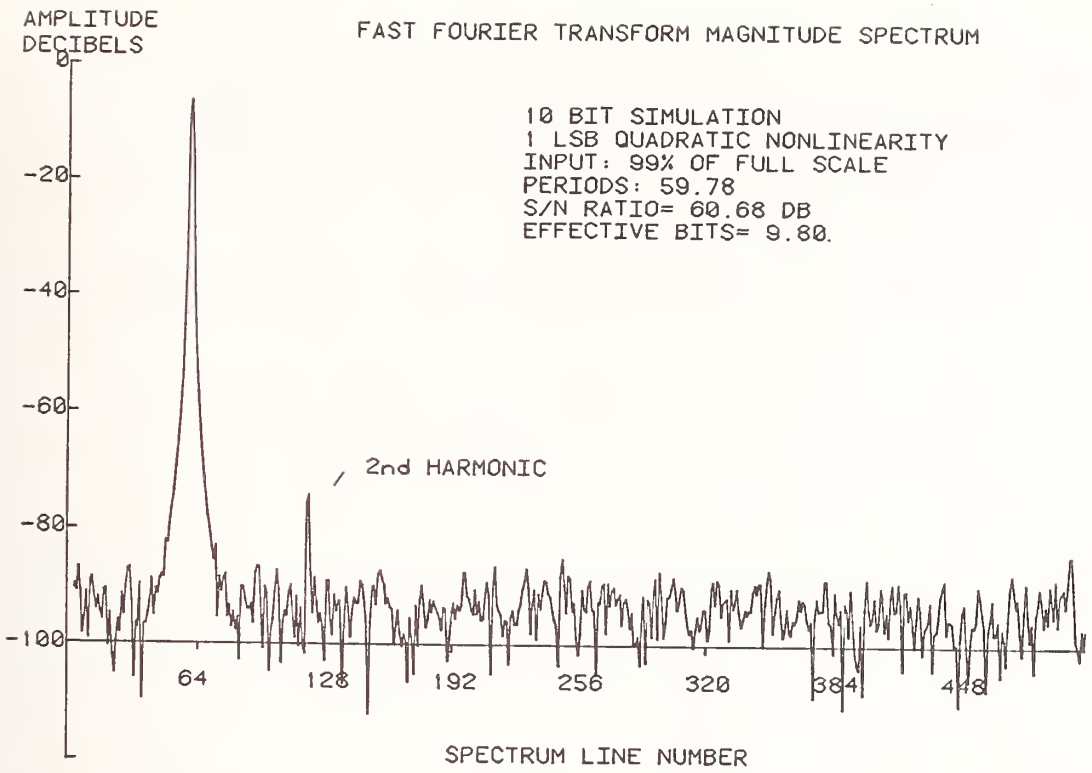

Figure 10. Spectrum from a 10 bit waveform recorder having the quadratic nonlinearity error shown in figure 9(b).

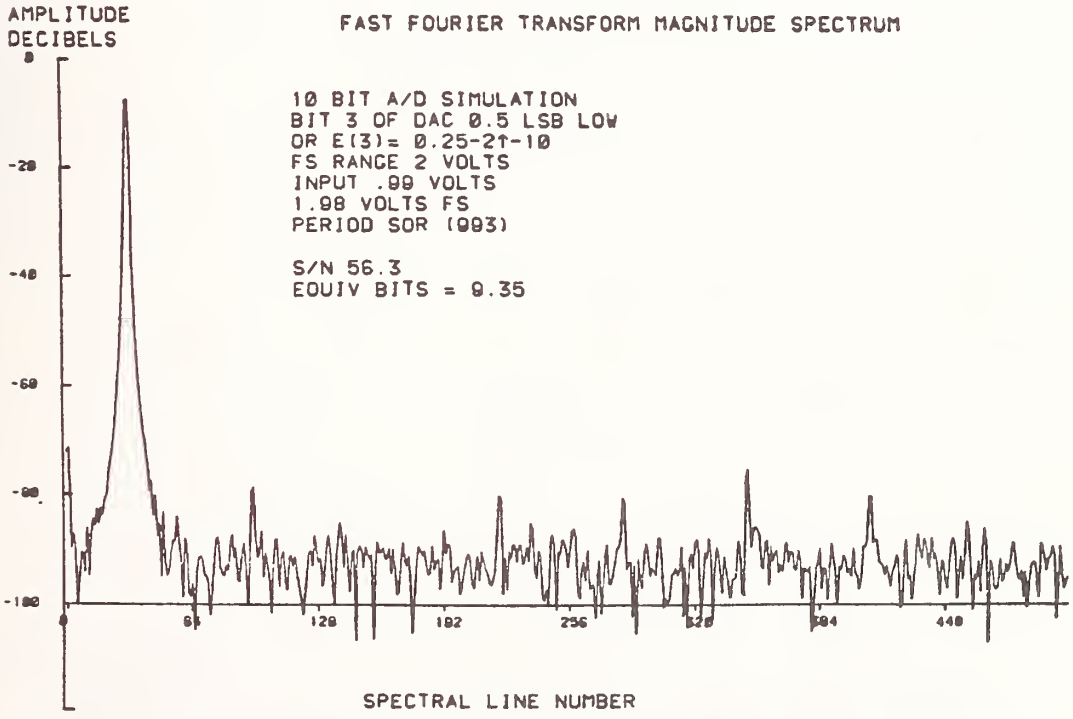

Figure 11. Computer simulation of a 0.5 least significant bit differential linearity error in bit 3 of a 10 bit recorder.

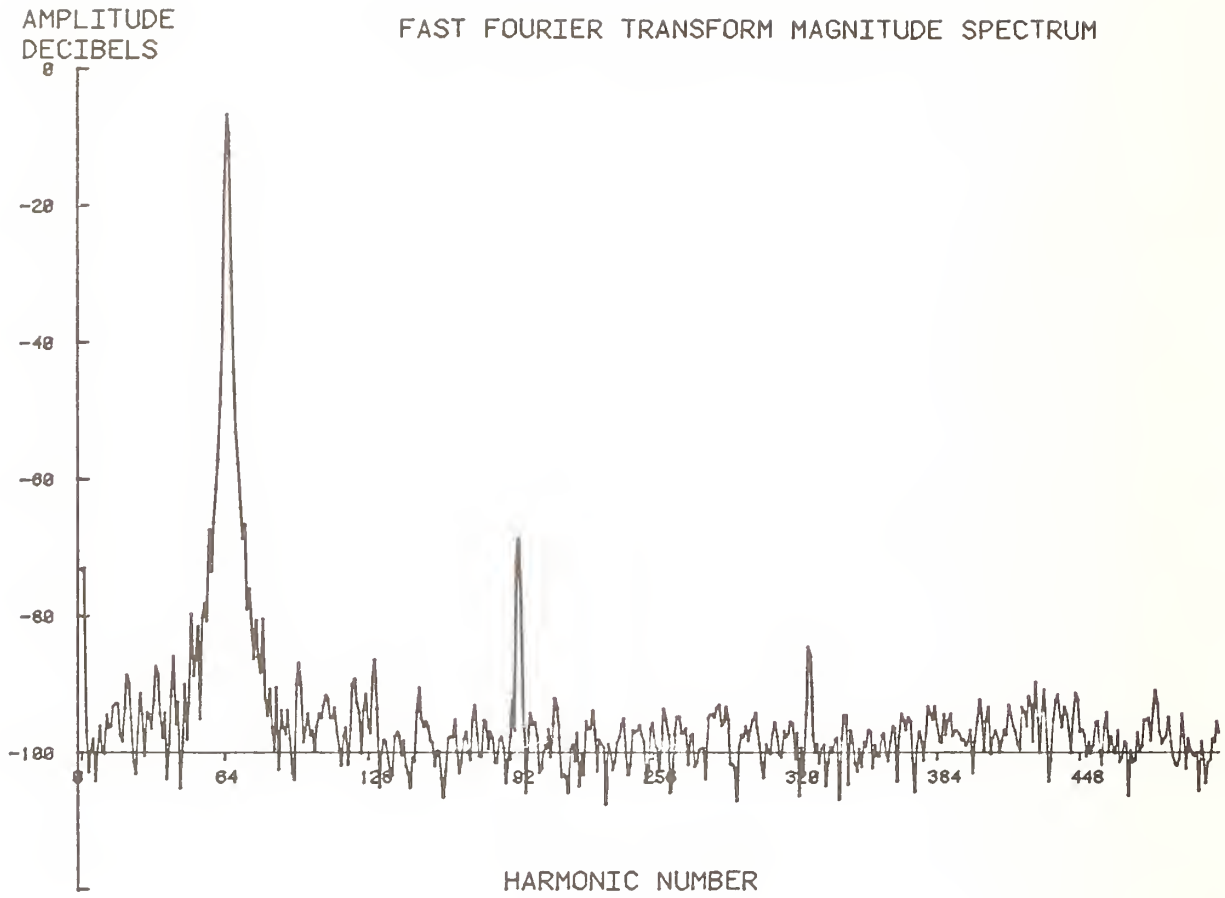

Figure 12. Sample/hold amplifier plus 12 bit analog-to-digital converter with a 1024 word memory.

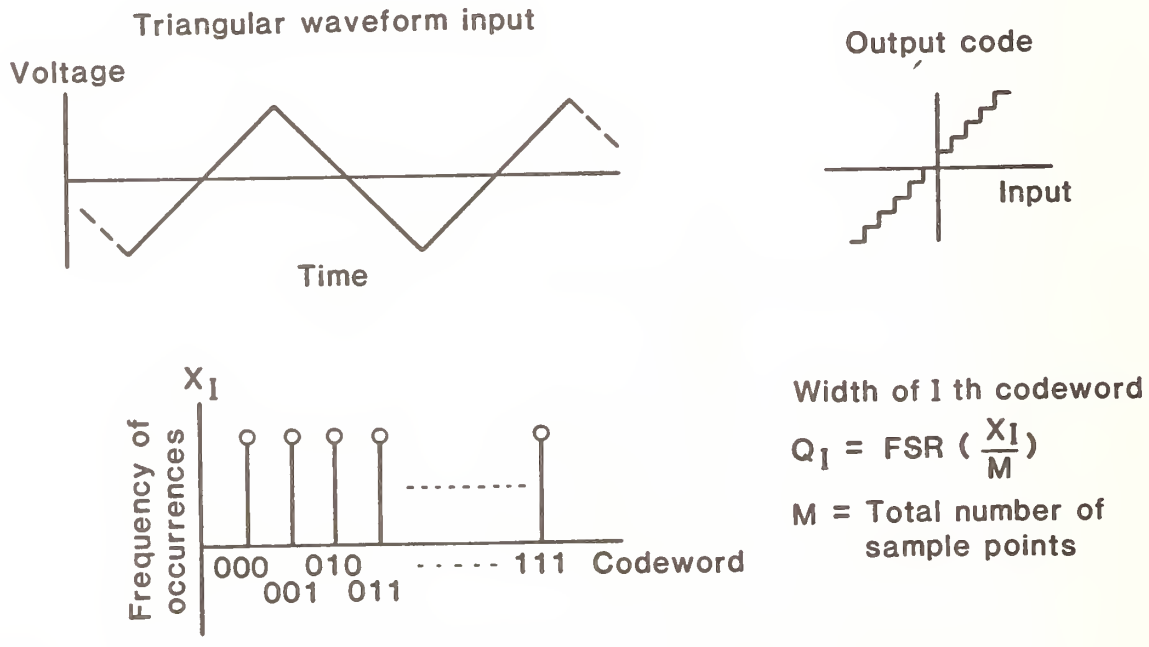

Figure 13. Histogram test using a triangular waveform as the input.

In an actual histogram test, the distribution of the number of occurrences of each codeword will not be equal, due to the statistical aspects of the test. If the test is repeated a number of times, however, the number of occurrences of a particular codeword will have an average value with a scatter about this value.

When an experiment is performed such that it has the properties listed below (see [18]), it qualifies as a Binominal experiment:

a.) a fixed number of trials,
b.) each trial must result in a "success" or a "failure" (a Binominal trial, also frequently called a Bernoulli trial),
c.) all trials must have identical probabilities,
d.) the trials must be independent.

The histogram test, as outlined above and in figure 13, meets the criteria for a Binominal experiment. The number of sample points is fixed, each sample point results in a codeword occurring or not occurring, the probability of a codeword occurring remains identical for each sample point, and the condition of no correlation between the applied fundamental frequency and the recorder's sampling rate meets the criteria for independence of the trials.

Thus, the probability of m "successes" out of M trials (or m occurrences of a particular codeword out of M sample data points for a n bit recorder) is represented by the Binominal distribution function

$$B(m,M) = \frac{M!}{m!(M-m)!} \; p^m \; q^{M-m}. \qquad (13)$$

In equation (13), p is the probability of a "success" (equal to 2^{-n} for a n bit recorder) and q is the probability of a "failure" (equal to $1-2^{-n}$). For large values of M, it is cumbersome to calculate the factorial terms in equation (13), and approximations to the Binominal distribution are used. It can be shown that when p is much less than one and M is large, the Binominal distribution is represented by the Poisson distribution function [19]

$$P(\lambda,m) = \frac{\lambda^m \; e^{-\lambda}}{m!}, \qquad (14)$$

where $\lambda = Mp$. The average value of the Poisson distribution is λ, and the standard deviation is $\sqrt{\lambda}$.

An important use of histogram tests is the detection of missing codes. A missing code means that a codeword has zero occurrences and is easily detected from a frequency of occurrence vs. codeword plot of the type shown in figure 14. However, a sufficient number of data points must be taken to ensure that the test does not register a false missing code. A complete solution to the problem of the random distribution of M things into R places is given in [24]. For the case of large M and R, it is shown that a suitable approximation results in a Poisson distribution. When applied to the missing code problem, the value of λ in equation (14) is equal to $Re^{-M/R}$, with $R = 2^n$. With this value of $\lambda = Re^{-M/R}$, the probability of m missing codes occurring over $R = 2^n$ codewords, when tested with M sample points, is given by equation (14). Note that M/R is the average number of code occurrences of each codeword. No missing

codes means that m = 0, and the probability of that event occurring is simply $e^{-\lambda}$. For a 10 bit recorder tested with 20,480 sample data points, the probability of no missing codes is calculated to be approximately 0.999998.

A second important use of histogram tests is the measurement of differential linearity errors (DLE), which are the variations in code width from the ideal value of one LSB. The width of a given codeword, Q_i, is determined from the data point record by the relationship

$$Q_i = (FSR) \frac{X_i}{M} , \tag{15}$$

where M is the total number of sample data points, and X_i is the number of occurrences of the designated codeword. If Q_i = one LSB, then the width of a one LSB wide code in terms of X_i is given by

$$Q = \frac{(FSR)}{2^n} = (FSR) \frac{X_1}{M} ,$$

and

$$X_1 = \frac{M}{2^n} . \tag{16}$$

The codeword distribution, X_i, is described by the Poisson distribution given in equation (14) with $\lambda = mp$. Again, a sufficient number of data points must be taken to ensure that the statistical variations in code width are small compared with the errors being measured. An example is the histogram test of a perfect 10 bit recorder using 102,400 sample data points. The average number of occurrences of each codeword is $M/2^n$ or 100. In terms of the Poisson distribution, the average value $\lambda = Mp$; when p = probability of the occurrence of one codeword, then $\lambda = M/2^n = 100$. Recall that the standard deviation of the Poisson distribution is $\sqrt{\lambda}$; thus, the standard deviation of the codeword distribution is 10.

The probability that all codes will lie within a certain code width is obtained by multiplying together the probabilities for each individual code being within that range. Still using the previous example, the width of a one LSB wide code is numerically equal to 100 occurrences of a codeword. To determine the probability that all codes lie within the range 0.5 to 1.5 LSB's (i.e., 50 to 150 occurrences of a codeword), first the following summation of the Poisson distribution is calculated:

$$P(m) = \sum_{m=50}^{150} \frac{100^m e^{-100}}{m!} . \tag{17}$$

The value of P(m) calculated from equation (17) is the probability of one particular codeword being within the 0.5 to 1.5 LSB range. For all 1024 codewords, the probability that all codes lie within the 0.5 to 1.5 LSB range is calculated to be 0.9987.

Figure 14 is a frequency of occurrence vs. codeword plot of a histogram test on a 10 bit, 10 MHz maximum sampling rate waveform recorder. For this test, a triangular waveform with a fundamental frequency of 9.9 kHz was applied, the sampling rate was 2 MHz, and 100,000 sample data points were captured. The nominal one LSB code width is 97.6 code occurrences. One-half of the recorder's range is shown, from octal code 1000 to 1777 (decimal code 512 to 1023). The results at the highest codes were disregarded due to slight overranging by the input signal. The 0.7 to 1.3 LSB code width (68.3 to 126.9 code occurrences on the vertical axis in figure 14 is exceeded by a number of codewords which are in excess of the total calculated for the ideal test. Calculations similar to those described using equation (17), but using 100,000 data points and a 0.7 to 1.3 LSB code width, indicate approximately 3 codes outside the 0.7 to 1.3 LSB range.

The histogram test can also be performed using a sine wave as the input stimulus. Sine waves are easier to generate and measure over a wide frequency range than are triangular-like waveforms of the required linearity. However, the probability density function of a sine wave is not uniform, but is described by the equation

$$P(V) = \frac{1}{\pi} \frac{1}{\sqrt{B^2 - V^2}} , \tag{18}$$

where B is the peak amplitude of the waveform and P(V) is the probability of an occurrence at a voltage V. The ideal probability of a code occurrence is obtained by integrating P(V) over a code width and is given by

$$P(I) = \frac{1}{\pi} \left[\sin^{-1} \left\{ \frac{(FSR)(I-2^{n-1})}{B2^n} \right\} - \sin^{-1} \left\{ \frac{(FSR)(I-1-2^{n-1})}{B2^n} \right\} \right], \tag{19}$$

where FSR = full scale range, B = peak amplitude of the input, I = offset binary code in decimal, and n = number of bits. The computation of the DLE is given by

$$DLE = \frac{(\text{Actual occurrences Ith code}) \; / \; (\text{total number of sample points})}{\text{Ideal probability of occurrence of Ith code}} - 1. \tag{20}$$

A computer simulated sine wave histogram test using 10,000 sample points on an 8 bit recorder is shown in figure 15. The shape of the frequency of occurrences vs. codeword plot clearly reflects the probability density function of a sine wave that is described by equation (18). Application of equations (19) and (20) to the data results in a linear plot of the DLE vs. codeword curve. This application of equations (19) and (20) is shown in figure 16 for an actual 100,000 sample point test on a 10 bit recorder. For this test, the applied sine wave frequency was 12 kHz, with 10 volts FSR applied voltage, and sampling rate of 10 MHz (maximum for this recorder). Evident from the DLE vs. codeword plot in figure 16 are a series of wide codes at the upper portion of the voltage range, some with DLEs greater than 2 LSBs.

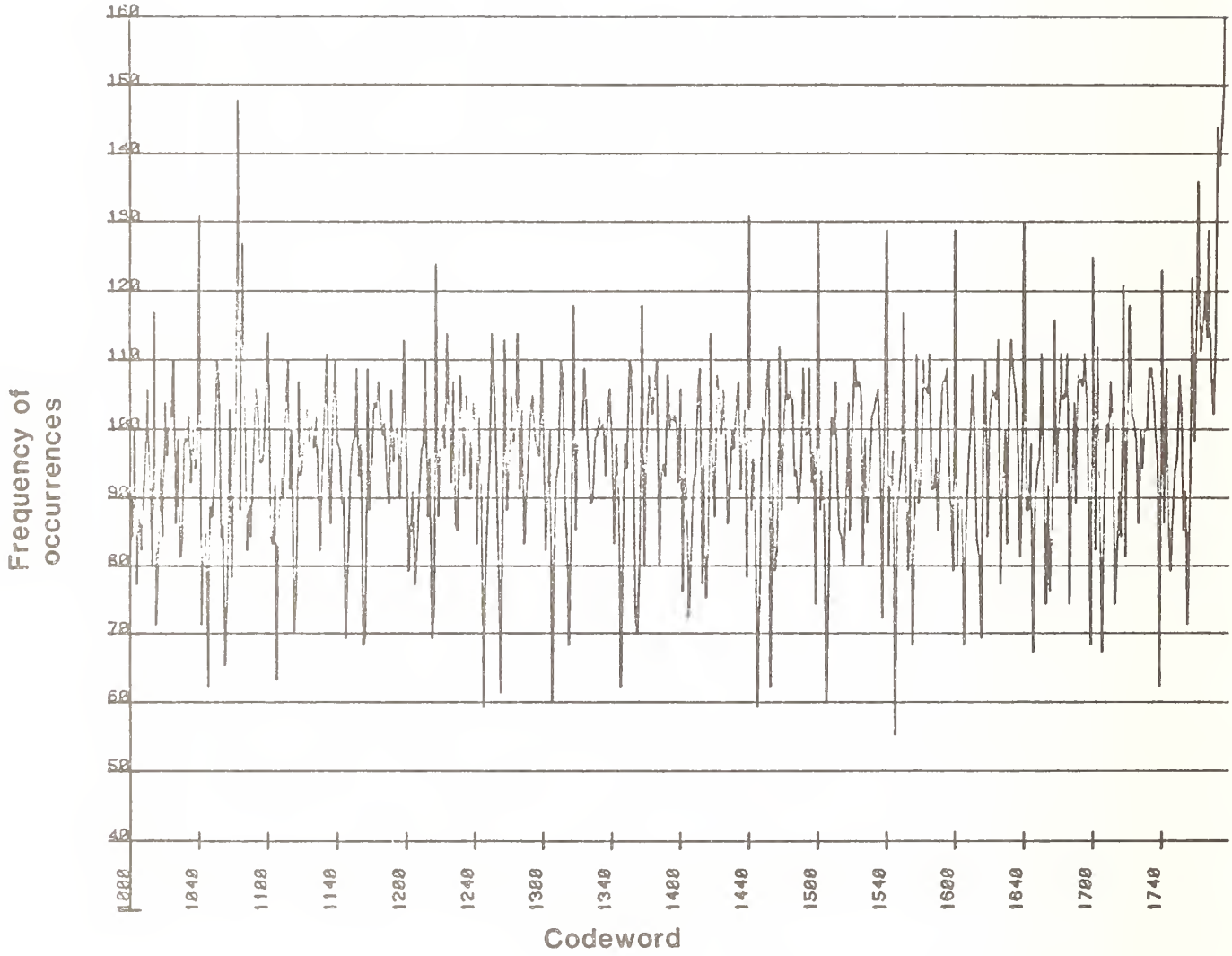

Figure 14. Portion of a histogram from a 100,000 sample point test. Ten bit waveform recorder tested with a 9.9 kHz triangular waveform input, and sampling at 2 MHz.

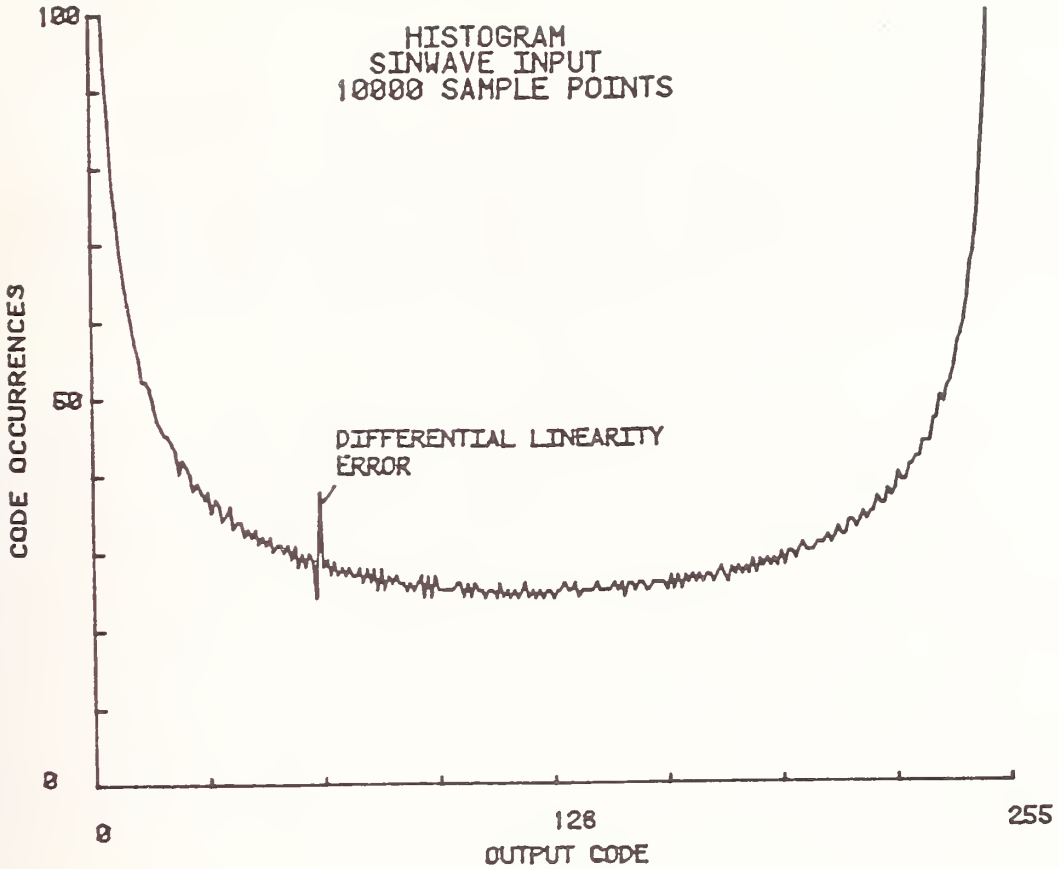

Figure 15. Computer simulation of a histogram test on a 10 bit recorder with a sine wave input.

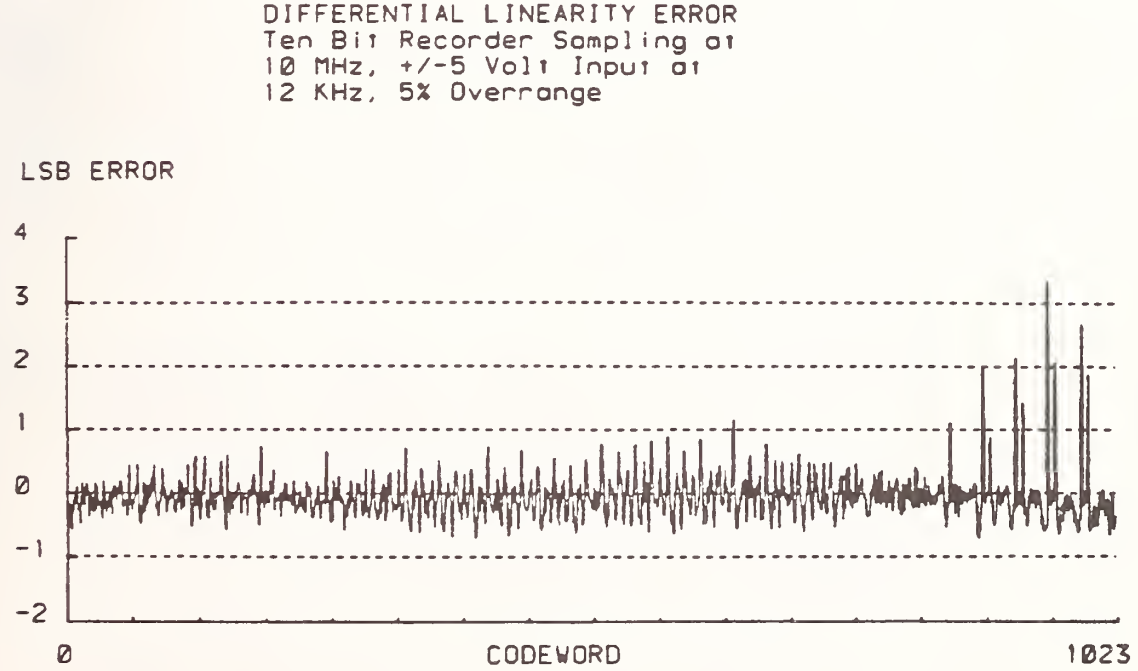

Figure 16. Histogram test on a 10 bit recorder with sine wave input, 100,000 sample points.

5. Aperture Uncertainty Test

Aperture uncertainty (jitter) is the random variations in the timing of the encode commands of the waveform recorder [20]. Figure 17 shows the effect of a random aperture uncertainty on the voltage measurement of a sine wave. The aperture error is given by

$$\varepsilon = \Delta t \, (dy/dt), \tag{21}$$

where Δt = aperture uncertainty, and dy/dt is the slope of the signal being measured. If a Gaussian distribution is assumed for the aperture uncertainty, then the rms value of the aperture uncertainty corresponds to the distribution's σ value (standard deviation). Figure 18 shows a procedure for measuring aperture uncertainty [2,3]. If the encode command to the waveform recorder can be phase locked to the analog input waveform (whose time instabilities must be substantially less than that of the waveform recorder), then the waveform recorder should sample the input waveform at the same point, and in the ideal case of no aperture uncertainty, only one output codeword will occur. Since the aperture uncertainty is modeled as a Gaussian distribution, a histogram of the output codes with a Gaussian distribution will result from this test, as shown in figure 18. The σ calculated for the resultant distribution corresponds to the rms error voltage ε produced by the rms aperture uncertainty Δt. Then, the jitter is calculated as

$$\Delta t = \varepsilon/(dy/dt). \tag{22}$$

6. Transient Tests

Waveform recorders are often used to record and store transient phenomena, not repetitive waveforms like the steady state sine waves used in the test methods just described. In an effort to compare a steady-state test response with a transient response, a test method [21] was devised at NBS which measures the difference between a continuous sine wave test response and a transient response. The transient signals used are single period sinusoids derived from the steady state sine wave by a S/H amplifier. Figure 19 shows the derivation of the single period sinusoid from the steady state sine wave with the use of a S/H amplifier. Every 20th period, with an appropriate fixed phase shift, a single cycle is taken from the steady state sine wave and applied to the waveform recorder.

The test is performed as depicted in figure 20 by first applying the steady state sine wave and capturing a data record, then switching the S/H amplifier to a mode where every 20th period a single cycle is captured, and a second data record stored. The portion of the data records where the single period sinusoidal occurred is subtracted from the corresponding portion of the data record in the steady state mode. Any residuals remaining, after the subtraction, are a measurement of the difference in the transient vs. steady state response, provided the conditions set out below are met:

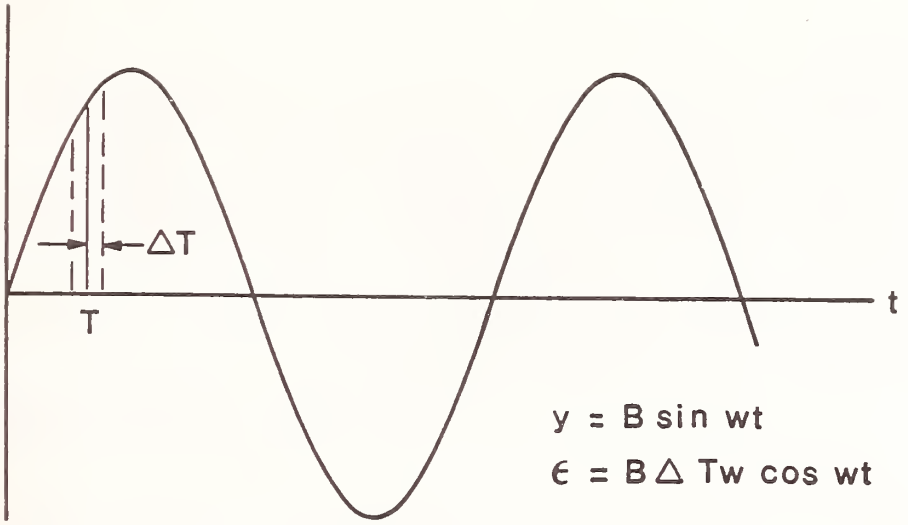

Figure 17. Effect of aperture uncertainty on the measurement of a sine wave.

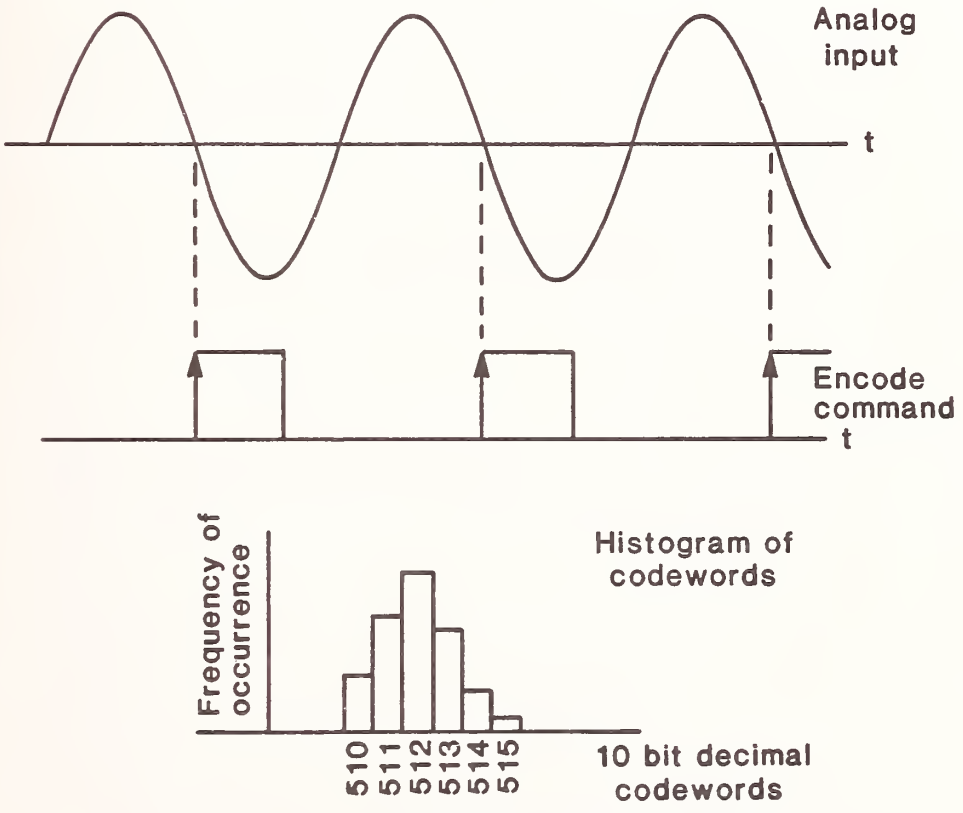

Figure 18. Aperture uncertainty test.

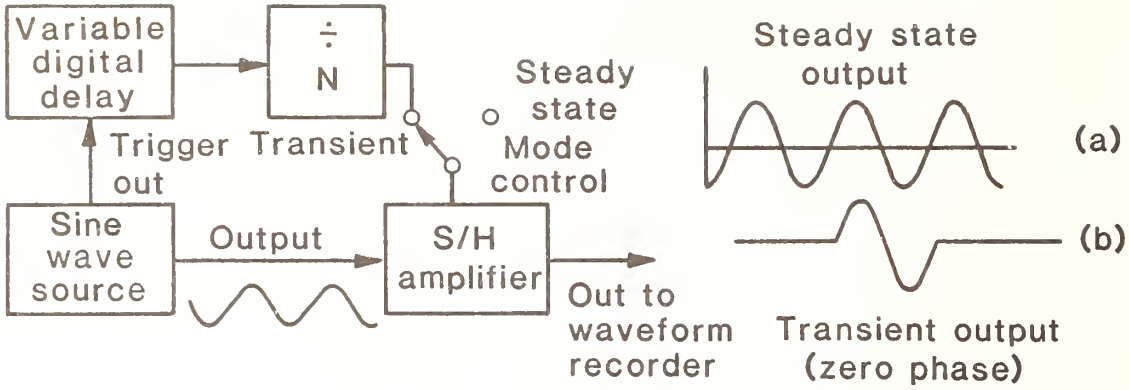

Figure 19. Single period transient sine wave generation.

Figure 20. Transient vs. steady state basic test method.

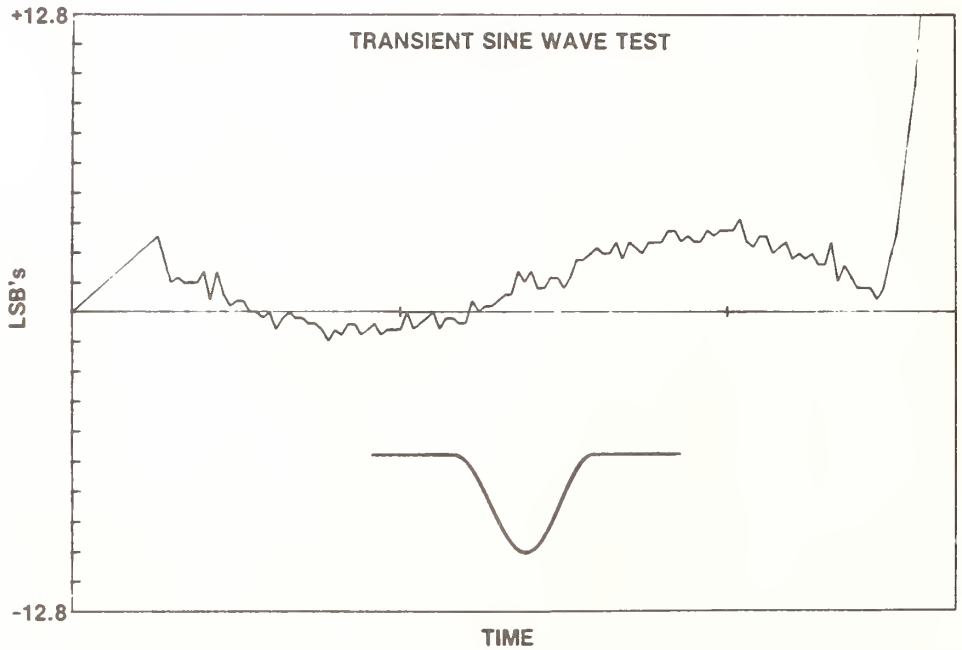

Figure 21. Transient minus steady-state response of a 8 bit, 100 MHz waveform recorder on ±0.5 volt range, with 100 nS sampling intervals. Input waveform is one cycle of a full scale 100 kHz sine wave as shown. Time skew and offset errors are present.

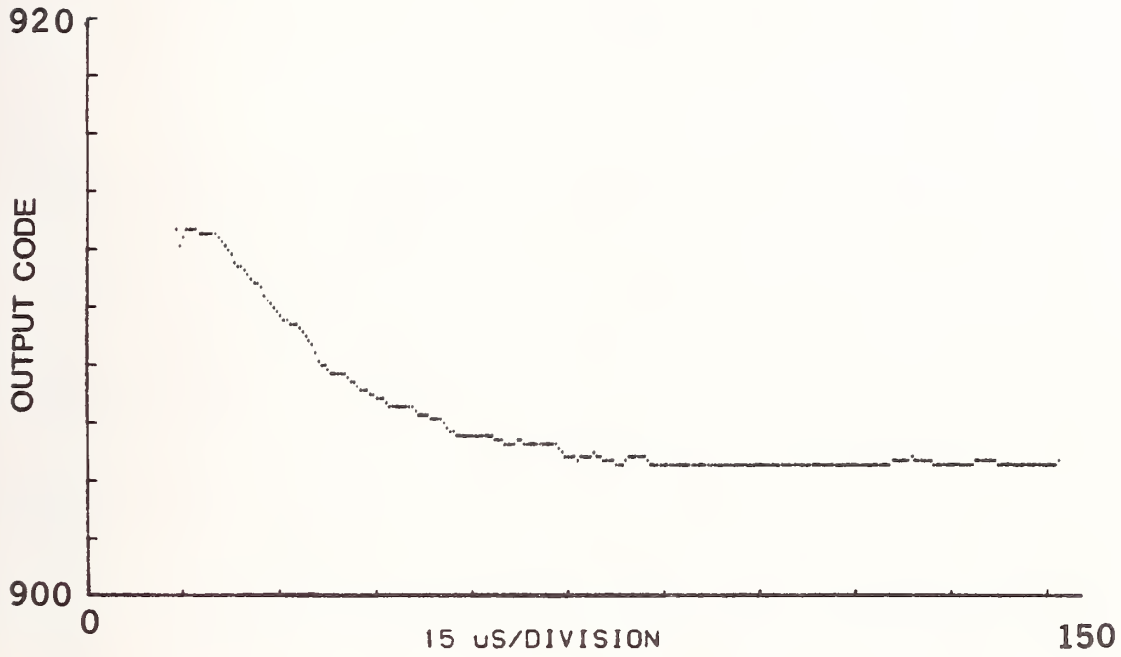

Figure 22. Step response of a 10 bit waveform recorder. Positive rise time step of -3.9 to +3.9 volts applied on ±5 volt range. Sampling rate was 5 MHz.

a.) Transient and steady-state waveforms are identical.
b.) The sine wave source is stable with no changes in amplitude and phase during application of the transient and steady state signals.
c.) The two data records are taken from identical segments of the two waveforms with no timing skew between them. A time skew of ΔT between the two records results in an error signal of the form

$$E(t) = B\omega\Delta T \cos \omega t, \tag{23}$$

that is superimposed on the difference between the two records. Averaging a number of record differences will reduce this effect, assuming that it is random.

Figure 21 shows the results of a test taken on an 8 bit, 100 MHz (maximum sampling rate) waveform recorder. The voltage range was ±0.5 volt, with 100 ns sampling intervals. Time skew and offset errors are present and further averaging is needed. Nevertheless, significant errors (>1 LSB) can be observed to occur over the full period of the transient sine pulse relative to the steady-state waveform.

A second type of transient test under development at NBS is a fast settling step response test. The details of the step-like generator used in these tests and methods of evaluating its peformance are given in [22]. This test system uses a step-like generator which rises (or falls) in a few nanoseconds from the first programmed voltage level to a second programmed voltage level. Once at the second voltage level, it settles within 40 ns to ± 0.02 percent of its final value with negligible overshoot. The length of time at the second level is programmable also, and the repetition rate at which the unit will run is a few megahertz. Voltage range levels are ± 5 volts on the high impedance input range and ± 1 volt on the 50 ohm input range. Figure 22 shows the results of a test on a 10 bit, 10 MHz maximum sampling rate recorder. A positive rise time step from -3.9 to +3.9 volts was applied on the ±5 volt range at a sampling rate of 5 MHz. The portion of the record shown is 20 LSB's from decimal code 900 to 920, and the graph covers a range of 300 sample points. The data were smoothed with a moving point average of 7 points. A relatively large transient overshoot of 6 LSB's is observable from this graph. About 70 μs were needed before the recorder had settled to its final value. These errors are possibly caused by a combination of dielectric and thermal effects at the instrument's input amplifiers.

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DUAL-CHANNEL SAMPLING SYSTEMS

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1. Introduction

Measuring two signals simultaneously with a dual-channel sampling system allows for the calculation of many quantities which cannot be calculated with a single channel instrument. For instance, if the voltage and current in a signal path are measured, the power in the signal (both real and reactive) can be calculated; or, if the stimulus and response waveforms for a circuit are measured, the circuit's transfer function can be determined. Since the dual-channel sampling approach preserves phase information, the transfer function data available from such systems includes both the frequency response and phase delay data.

As with single-channel sampling, the errors associated with dual-channel sampling arise from signal quantization effects, timing jitter, limited sampling rate, converter nonlinearities, truncation and signal processing algorithm. However, an important additional error source for the dual-channel system is differential time delay. This error source can result not only from a difference in timing of the strobe signals to the two sampling converters, but more significantly, from differences in the time delay of the input amplifiers.

This paper will concentrate mainly on the application of dual-channel sampling techniques to the measurement of electrical power and, to a lesser extent, on the application to electrical phase angle measurements. Theoretical relationships are developed for describing these sampling measurements and their associated errors. The procedures that can be used to calibrate such dual-channel instruments for these applications will be described as well. Figure 1 is a diagram of the basic dual-channel sampling system to be analyzed in this paper.

2. Sampled Power Measurements

Electrical power can be measured by sampling both the voltage and current waveforms applied to a given load. The product of these waveforms is the instantaneous power being drawn by the load. The average power going to the load can be determined by time averaging these products. The errors that are encountered in doing this measurement will be considered only for the case of periodic input signals. Most of the equations that follow apply to the more limited case of the voltage and current signals having only a single frequency. However, the method of extending these equations to waveforms with many harmonics are described in [1].

For sinusoidal voltage and current waveforms, the sampled signals can be represented by

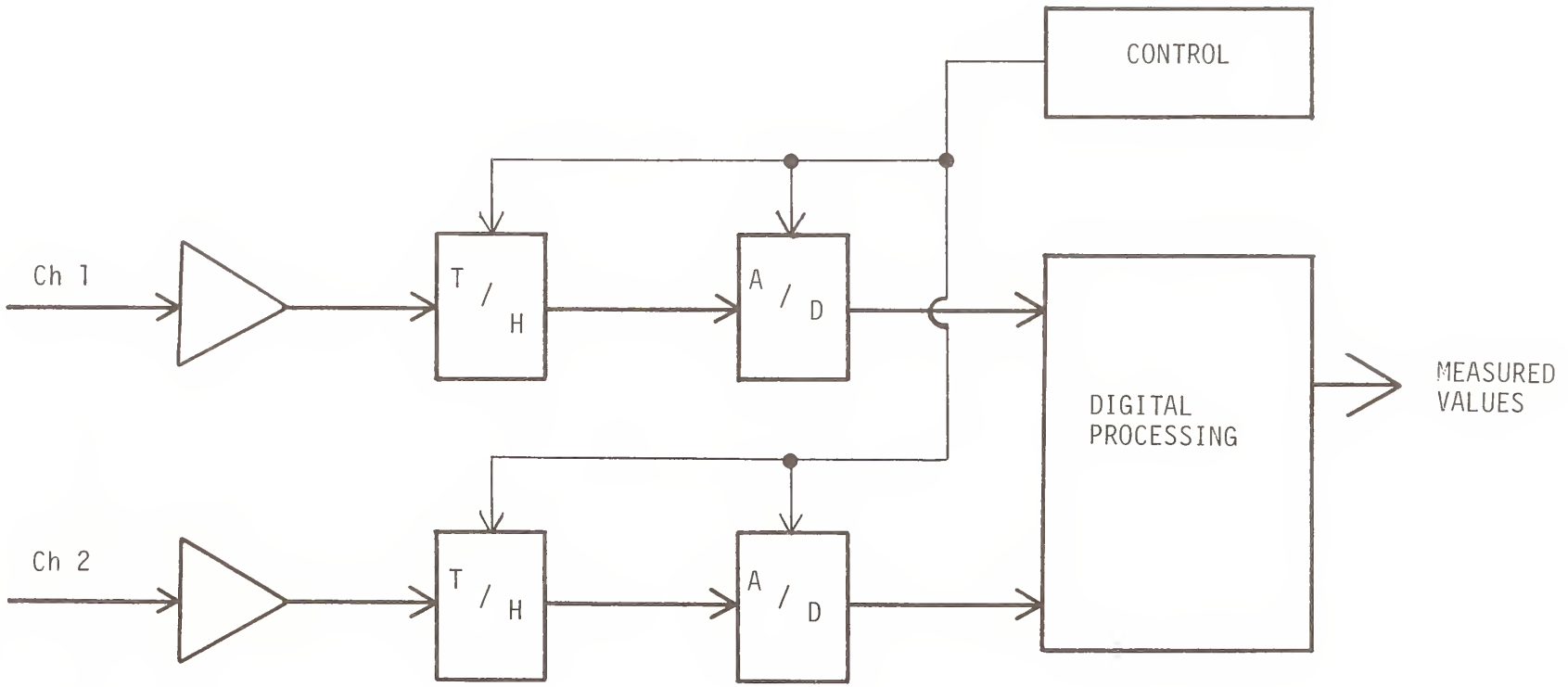

Figure 1. Basic dual-channel sampling system.

$$V_k = V \sin(\omega kT + \alpha) \tag{1}$$

and

$$I_k = I \sin(\omega kT + \alpha + \beta), \tag{2}$$

where k is the sample number, ω is the signal frequency in radians per second, T is the sample interval, α is the voltage starting phase angle, β is relative current phase angle, and V and I are the peak voltage and current values. The product of the two quantities represents the sampled power, P_k, and the average power in the signal can be approximated by averaging these products as [2]

$$W = \frac{1}{n} \sum_{k=0}^{n-1} P_k = \frac{VI}{2} \cos(\beta) - \frac{VI}{2n} \sum_{k=0}^{n-1} \cos(2\omega kT + 2\alpha + \beta), \tag{3}$$

where W is the indicated power and n is the number of samples averaged. The first term on the right is the true power so the sum term can be interpreted as the error E, that is

$$E = -\sum_{k=0}^{n-1} \frac{VI}{2n} \cos(2\omega kT + 2\alpha + \beta). \tag{4}$$

Expressing the cosine term as the real part of a complex exponential, the sum can be recognized as a geometric progression. Thus, the sum can be written as [1]

$$E = -\frac{VI}{2n} \frac{\sin(n\omega T)}{\sin(\omega T)} \cos(2\alpha + \beta + n\omega T - \omega T). \tag{5}$$

This equation can be put into a more useful form by letting $\gamma = \omega T$ be the sample interval expressed in radians of the input signal, and δ be the difference in radians between the summation interval $n\gamma$ and an integer number, c, of cycles of the input signal in the summation interval, i.e., $\delta = 2\pi c - n\gamma$. Define c' to be the number of cycles and partial cycles of the input signal in the summation interval, or $2\pi c' = n\gamma$. Figure 2 shows the relation between these parameters for an example of sampling one cycle of sinusoidal voltage and current signals. Using these variables the error E becomes [1]

$$E = \frac{VI}{2} \frac{\gamma}{2\pi c'} \frac{\sin \delta}{\sin \gamma} \cos(2\alpha + \beta - \delta - \gamma). \tag{6}$$

Equation 6 represents the error in the indicated power measurement resulting from the sampling approach. This error is usually referred to as the truncation error. The maximum error, E_{max}, will occur when the cosine term and sin δ term in (6) are ± 1; thus,

$$\left|E_{max}\right| = \frac{VI\gamma}{4\pi c'} \left|\frac{1}{\sin \gamma}\right| . \tag{7}$$

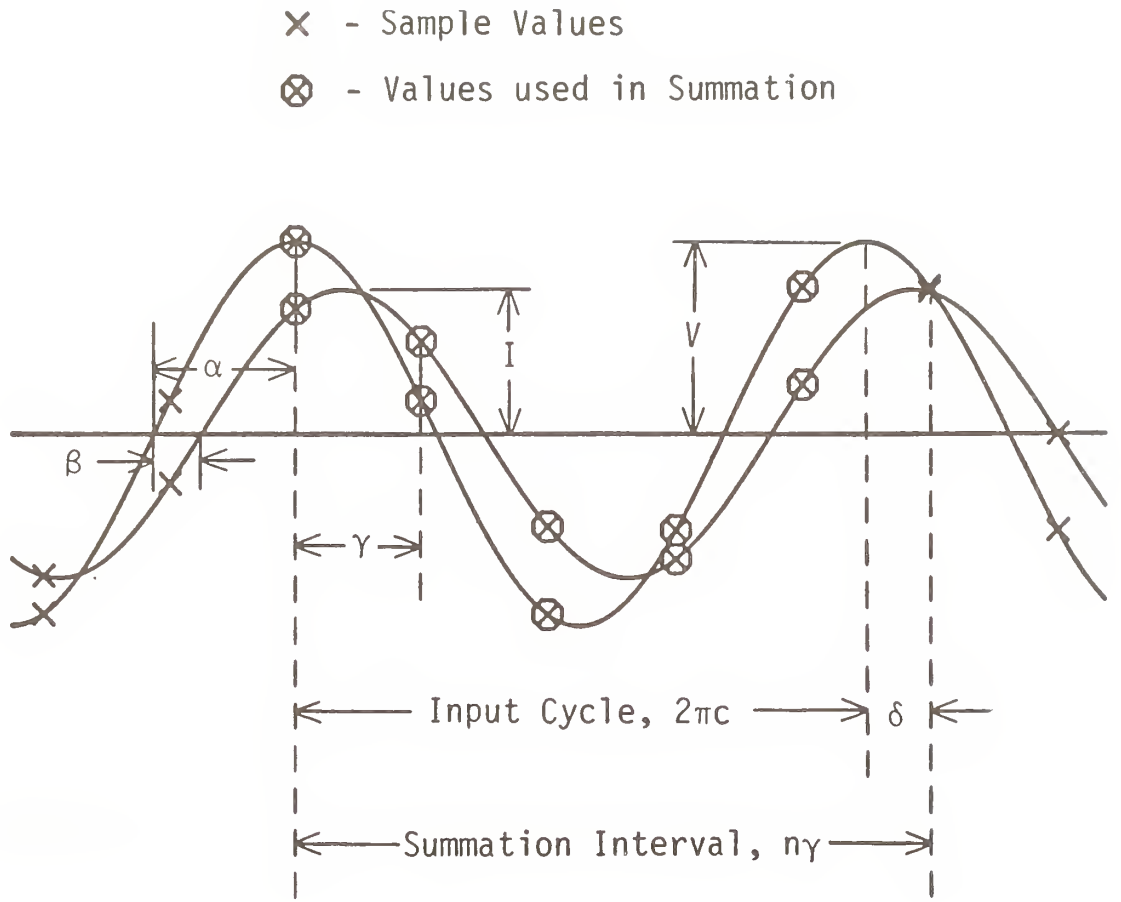

Figure 2. Example of sampling two signals showing the relationship of the sample times to the signal parameters.

When the signal frequency is much less than the sampling rate, γ will be a small angle and $\sin \gamma \approx \gamma$. Then the maximum error becomes

$$\left|E_{max}\right| \approx \frac{P_u}{2\pi c'} , \tag{8}$$

where P_u is the power at unity power factor, $P_u = VI/2$. In this case the error is inversely proportional to the number of cycles of the signal in the summation interval, $n\gamma$. This means that high accuracy measurements of low frequency signals require a very long summation time.

2.1 Reducing Truncation Error

There are several methods which can be used to reduce the truncation error. One method is to approximately synchronize the summation interval with the signal. This is done by adjusting the number of samples, n, in the summation interval such that the difference between the summation interval and the time to complete an integral number of cycles of the input signal is less than one sample interval($\delta < \gamma$). The maximum error then occurs when $\sin \delta = \sin \gamma$, provided that $\gamma < \pi/2$ and the cosine term in (6) is ± 1; thus,

$$\left|E'_{max}\right| = \frac{VI}{2n} = \frac{P_u}{n} . \tag{9}$$

The maximum error in this case is inversely proportional to the number of samples and independent of the signal frequency. Thus, the truncation error is reduced for signals sampled more than four times per cycle. As an illustration, consider a dual-channel system that samples at 300,000 samples per second and uses a summation interval of one half second, or about 150,000 samples. The maximum truncation error, without adjusting the summation interval for a 100Hz input signal, is ± 0.3 percent of the power at unity power factor, P_u. When the sampling interval is approximately synchronized with the input signal, the error is reduced to 0.0007 percent of P_u. Since this latter error is independent of frequency, it applies to any input signal which is sampled for one half second, with the exception of signals whose frequency is near to a multiple of half the sampling rate.

Another method that can be used to reduce the truncation error is to estimate and correct for the truncation angle δ. The method described below is good if δ is small so it should be used together with the approximate synchronization method. Defining the truncation factor, a, as the ratio of the truncation angle to the sampling angle $a = \delta/\gamma$, an estimate of the true power, P, can be calculated by

$$P' = \left(\frac{1}{n+a} \sum_{k=0}^{n-1} P_k\right) + \frac{aP_n}{n+a} . \tag{10}$$

Finally the truncation error can be eliminated by synchronizing the sampling with the input signal. Then if m samples are taken in n cycles, where m and n are integers, the truncation angle δ will be zero and thus (6) shows that the truncation error will be zero. While this approach has the advantage of no truncation error, a disadvantage is that the quantization errors are correlated. The effect of this correlation and a way to reduce the effect are described in a later section.

2.2 Noise, Jitter and Quantization

The three main sources of noise for the typical dual-channel system are the input amplifiers, the timing uncertainty or jitter of the clock and sample hold circuits, and the analog-to-digital (A/D) converters. A detailed discussion of these noise signals as they relate to single channel accuracy is given in [3]. In general, all three are broadband noise signals, where the amplifier noise has a constant Gaussian distribution, the jitter noise has a Gaussian distribution and an amplitude proportional to the rate of change of the input signal, and the A/D or quantization noise has a generally constant uniform distribution.

These noise sources can be considered as error signals added to the true input signal. Thus, the measured voltage, V_{km}, and current, I_{km}, signals can be represented as

$$V_{km} = V_k + e_{vak} + e_{vqk} + e_{vjk} = V_k + e_{vk}, \tag{11}$$

$$I_{km} = I_k + e_{iak} + e_{iqk} + e_{ijk} = I_k + e_{ik}, \tag{12}$$

where k indicates the sample number, the e_v's and e_i's are random error signals in the voltage and current channels, and the a, q, and j subscript represent the noise source as amplifier noise, A/D quantization, and clock jitter respectively. For the expression on the far right, the three noise terms have been combined. Then, the measured power terms are given by

$$P_{km} = V_{km}\, I_{km} = P_k + V_k\, e_{ik} + I_k\, e_{vk} + e_{ik}\, e_{vk}. \tag{13}$$

In general, the last error term is negligible. If the noise signals are uncorrelated, then when the samples are averaged the error will be reduced proportional to $n^{-1/2}$, where n is the number of samples taken. However, if the sampling is synchronized with the input signal, then averaging will not reduce the quantization error because they will be correlated. The significance of the correlation depends on the number of independent n_j versions of the sampled signals which are present in the data. Consider a signal that is uniformly sampled 1024 times during an integral number of cycles, n_c, of the signal. If n_c is 32, then every cycle of the incoming signal is sampled 32 times at the same phase angles. Thus, there is only one independent set of 32 samples of the signal ($n_j = 1$). The other 31 sets are not independent but are at the same phase angles. If n_c is 31, however, then all 31 cycles are sampled at different phase angles; thus $n_j = 31$. If n_c is 30, there are 15 independent sets of data ($n_j = 15$). The quantization error is reduced by approximately the reciprocal of the square root of the total number of independent samples n_i where

$$n_i = \frac{n\, n_j}{n_c} . \tag{14}$$

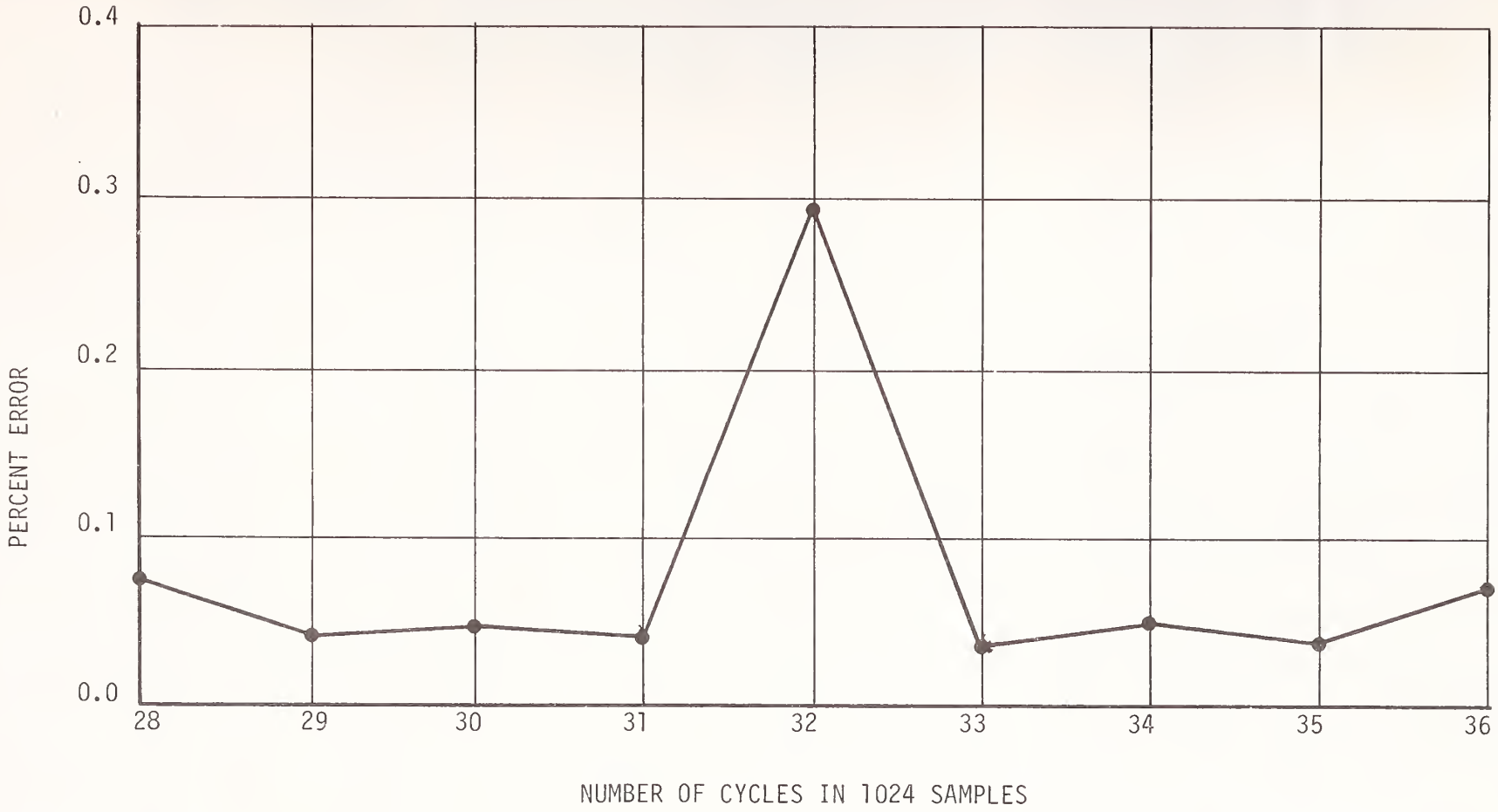

Figure 3 - The effects of correlated quantization noise appear in the standard deviation of 20 simulated power measurements using 8 bit quantization on two sinewaves.

Since for a sinewave the data points are not truly independent, the above relationship is only an approximation. The effects of correlated quantization noise can be shown by data taken from a computer simulation of sampled power measurements. In figure 3 the standard deviations of 20 simulated power measurements are plotted versus the number of cycles of the input signal which are in 1024 samples. The 20 simulated signals used to calculate each point had a random starting phase angle and random power factor. The error calculated is the percent of the power for a unity power-factor signal. Note how the standard deviations of the error are high for 32 cycles and low for those values of n that have no common factors with the total number of samples, 1024. This effect shows up most dramatically here because it is a simulation; thus, there is no random noise on the original signal. If the simulation is run with a random noise of about one least significant bit (LSB), most of this effect disappears. In the graph of figure 3 the data points have been connected with a straight line to better show the relative magnitudes, but this is not to imply that the data in-between follows this line. The in-between points represent nonsynchronized sampling, and the trend for these points is shown later in the section on phase angle measurements.

2.3 Frequency Response

One method of determining the frequency response of a dual-channel sampling instrument is to compare its response to that of a more accurate instruument. For dual-channel instruments which can indicate the root-mean-square (rms) value of each channel, these values can be compared to an accurate ac voltmeter. For wattmeters, where one channel must be a current input, then that channel must be compared to an accurate ac current meter. Finally, for wattmeters which cannot indicate the rms values of each channel, their frequency response can be determined by comparing it with a more accurate wattmeter.

Figure 4 shows the results of the NBS sampling wattmeter using a slight variation on the above approach. Instead of comparing the wattmeter output with the reading of a voltmeter, the wattmeter was compared to the output of an ac calibrator. The plot shows the frequency response for each channel and for the product ("power") mode where the same voltage is applied to both channels.

2.4 Differential Time Delay

When measuring power, any difference between the time delay of the two channels has the effect of changing the measured power factor. Let τ be the time delay of the voltage channel and $\tau + \tau_d$ be the time delay of the current channel, where τ_d is the differential time delay. Then the delayed voltage and current samples will be

$$V_{kd} = V \sin[\omega(kT + \tau) + \alpha], \tag{15}$$

$$I_{kd} = I \sin[\omega(kT + \tau_d + \tau) + \alpha + \beta], \tag{16}$$

and the indicated power, W_d, will be

$$W_d = \frac{1}{n} \sum_{k=0}^{n-1} V_{kd} I_{kd}, \tag{17}$$

or

$$W_d = \frac{VI}{2} \cos(\beta + \omega\tau_d) - \frac{VI}{2} \sum_{k=0}^{n-1} \cos\left[2\omega k\left(T + \tau + \frac{\tau_d}{2}\right) + 2a + \beta\right]. \tag{18}$$

Now, the first term on the right is not the true power, but is the power for signals with the same amplitudes and a power factor angle of $\beta + \omega\tau_d$. Thus, the error for a wattmeter which has such a differential delay increases in magnitude with frequency. This effect can be seen very clearly in figure 5, which is a plot of the errors measured for a commercial wattmeter which has a time delay error. If the truncation error part of (18) is not significant (i.e., it has been reduced by the methods described above or is zero because the sampling is synchronized), then the error due the differential time delay E_d can be determined by expanding the cosine term in (18). Then

$$E_d = \frac{VI}{2} \cos(\beta) - \frac{VI}{2} [\cos(\beta)\cos(\omega\tau_d) - \sin(\beta)\sin(\omega\tau_d)], \tag{19}$$

$$E_d = \frac{VI}{2} \cos(\beta) [1 - \cos(\omega\tau_d)] + \frac{VI}{2} \sin(\beta)\sin(\omega\tau_d). \tag{20}$$

In general, the differential time delay will be small compared to the time delay of the amplifiers which is related to the frequency response of the instrument. Thus, for signals within the frequency range of the instrument, $\omega\tau_d$ is a small angle and $\cos(\omega\tau_d) \approx 1$ and $\sin(\omega\tau_d) \approx \omega\tau_d$ then the error due to the differential time delay can be written as

$$E_d \approx \frac{VI}{2} \omega\tau_d \sin(\beta). \tag{21}$$

This relationship shows that the differential time delay error is approximately zero at unity power-factor, $\beta = 0°$, and is most significant at zero power-factor, $\beta = 90°$. Equation (21) also shows the error to be proportional to frequency, as was seen in the calibration curve of figure 5.

For power measurements in the audio frequency range, the error due to differential time delays can be very significant when low power-factor signals are being measured. As an example, if the power factor is 0.5 ($\beta = 60°$) for a 10 kHz signal, then a differential time delay of only 18 ns will cause a 0.1% error in the measured power.

For wattmeters which will accept two equal voltage inputs and give the average product ("power") of these signals, the differential time delay of that portion of the wattmeter can be determined independent of the time constant of the current shunt. The procedure for determining the time constant of the

current shunt will not be covered here but is described in [4]. Figure 6 shows the test setup for determining the time delay of a dual-channel sampling instrument. The phase source must provide nearly equal voltages and be able to provide stable phase angles near 90° and 270°. The variables for the voltage and phase angles of the source are defined in table 1. The average product ("power") reading for the normal, N, switch position with phase near 90° is

TABLE 1

PHASE SOURCE ERRORS

Channel	Phase Angle	Phase Error	Output Voltage
Reference	any	0	V_R
Variable	90°	θ_A	V_A
Variable	270°	θ_B	V_B

$$P_{N90} = \frac{V_R V_A}{2} \cos(\omega\tau - \frac{\pi}{2} - \theta_A - \omega\tau - \omega\tau_d), \tag{22}$$

where V_R is the amplitude of the reference channel, V_A is the amplitude of the variable channel at 90° and θ_A is the phase error at 90°. For θ_A and $\omega\tau_d$ small, this equation becomes

$$P_{N90} \approx - P_A (\theta_A + \omega\tau_d), \tag{23}$$

where $P_A = \frac{V_R V_A}{2}$. The readings at the other three combinations of switch settings and phase angle are approximately

$$P_{R90} \approx - P_A(\theta_A - \omega\tau_d), \tag{24}$$

$$P_{N270} \approx P_B(\theta_B + \omega\tau_d), \tag{25}$$

and

$$P_{R270} \approx P_B(\theta_B - \omega\tau_d), \tag{26}$$

where $P_B = \frac{V_R V_B}{2}$, V_B is the amplitude of the variable channel at 270° and θ_B

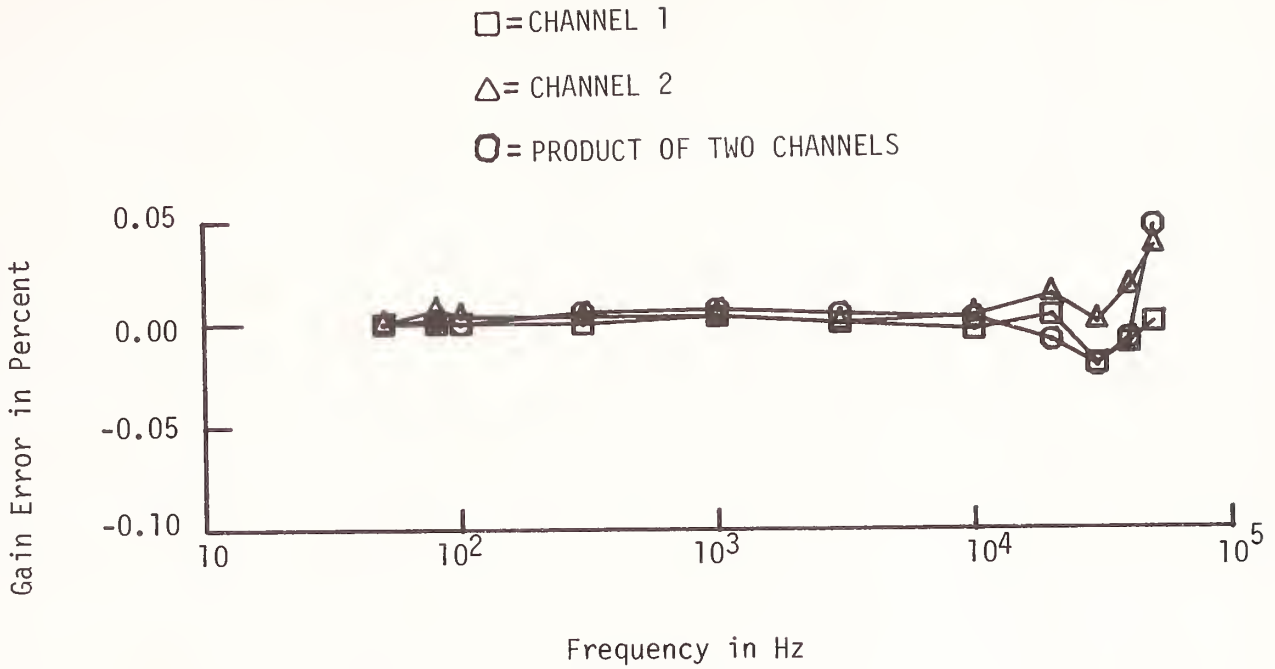

Figure 4. Frequency response of the NBS Wideband Sampling Wattmeter 5 V range.

is the phase error at 270°. Combining these four readings in the following manner gives

$$P_{N90} - P_{R90} - P_{N270} + P_{R270} \approx - 2\omega\tau_d(P_A + P_B). \tag{27}$$

This result gives a value for the time delay τ_d which is independent of the accuracy of the phase source angle. If the voltage from the variable channel of the phase source is independent of phase angle, then $P_A = P_B$ and this value can be measured at unity power factor.

These values can also be used to check the accuracy of the phase source by combining the readings as follows:

$$P_{N90} + P_{R90} - P_{N270} - P_{R270} \approx - 2P_A\theta_A - 2P_B\theta_B = P_{PS}. \tag{28}$$

Then for a phase source such as a digitally synthesized phase generator, which has high differential linearity, $\theta_A = \theta_B = \theta$ (the phase changes are very accurate) and stable voltages, $P_A = P_B$, (28) becomes

$$P_{PS} = - 4P_A\theta \quad . \tag{29}$$

This equation gives the error in the phase source and is independent of the accuracy of the product ("power") meter.

3. Phase Angle Measurement

A dual channel sampling instrument can measure the phase angle between two signals using several algorithms. Four techniques will be described in this section, and their accuracies will be compared using a computer simulation program. These techniques are the fast Fourier transform (FFT), the interpolated fast Fourier transform (IFFT), the discrete Fourier transform using the correct frequency (DFTCF), and the corrected discrete Fourier transform (CDFT).

The FFT is a widely used algorithm for converting sampled data from the time domain to the frequency domain. Implicit in the "fast" part of the name is that the number of samples used, N_f, is highly factorable and in most cases is restricted to be a power of two. The complex frequency components calculated by the FFT can be expressed as [5]

$$X_j(k) = \sum_{n=0}^{N_f-1} v_j(nT)e^{-ik\omega_s nT} \qquad k = 0, 1, \ldots, \frac{N_f}{2}, \tag{30}$$

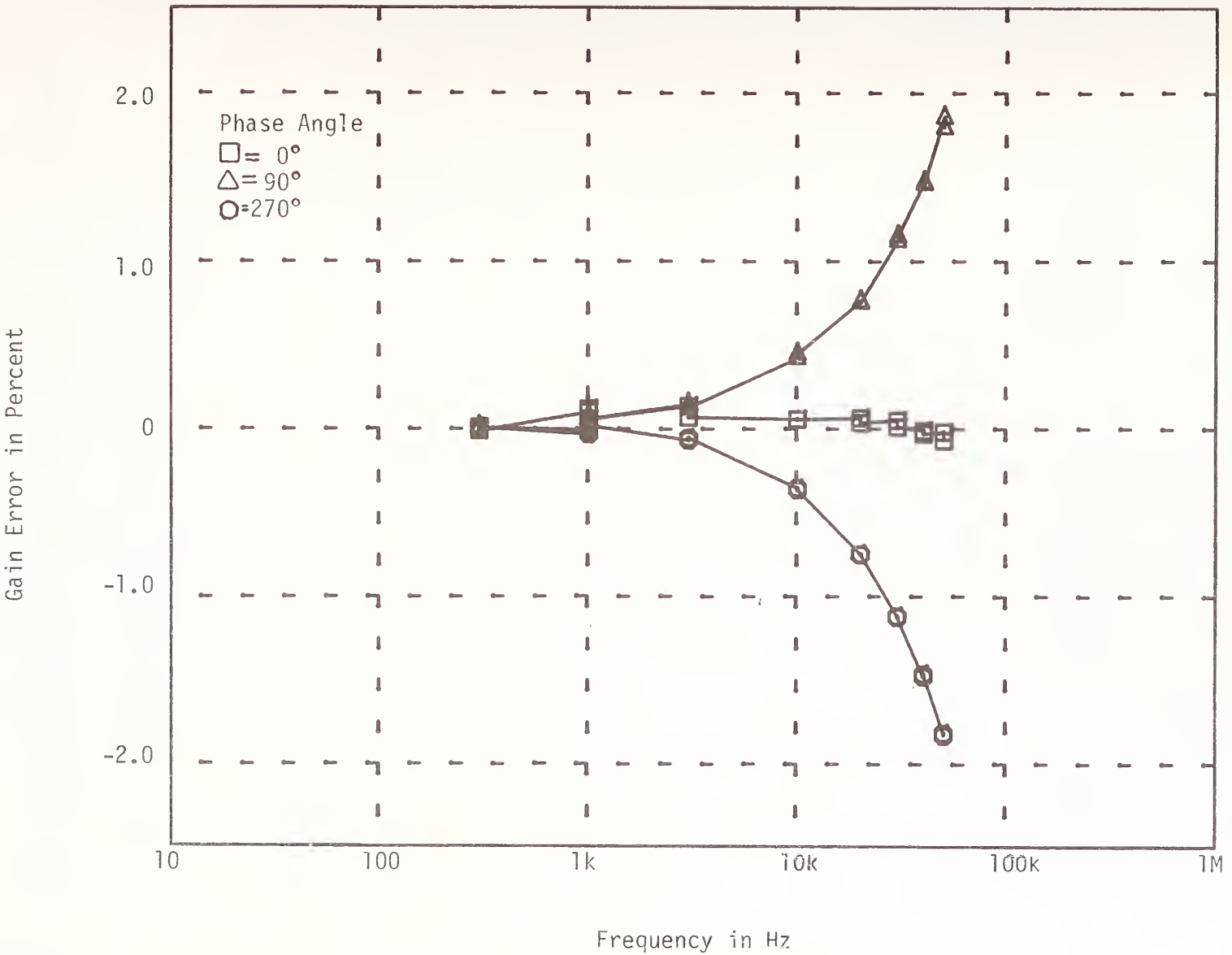

Figure 5. Frequency response of a commercial wattmeter with NBS wideband sampling wattmeter as reference shows the effects of a differential time delay.

where j, which designates the channel, is 0 or 1, T is the time between samples, ω_s is related to the total sample interval by $\omega_s = 2\pi/N_f T$, and $v_j(nT)$ are the sampled voltages for the j^{th} input channel. If the input voltage is a sinewave of frequency ω, the sampled values can be expressed as

$$v_j(nT) = V_j \sin(\omega nT + \phi_j), \tag{31}$$

where V_j is the peak voltage, and ϕ_j is the phase of the sinewave relative to the start of the sampling interval. Then the real and imaginary parts of the frequency components can be written as

$$\mathrm{Re}[X_j(k)] = V_j \sum_{n=0}^{N_f-1} \sin(\omega nT + \phi_j)\sin(k\omega_s T - \pi/2), \tag{32}$$

and

$$\mathrm{Im}[X_j(k)] = V_j \sum_{n=0}^{N_f-1} \sin(\omega nT + \phi_j)\sin(k\omega_s T). \tag{33}$$

These equations can be expressed in polar coordinates with an amplitude, A, and phase, Φ, given by

$$A_{jf}(k) = [\mathrm{Re}^2[X_j(k)] + \mathrm{Im}^2[X_j(k)]]^{1/2}, \tag{34}$$

and

$$\Phi_{jf}(k) = \arctan \frac{\mathrm{Re}[X_j(k)]}{\mathrm{Im}[X_j(k)]}. \tag{35}$$

If the sampling is synchronized with the input frequency such that an integral number of cycles c of the input signal are sampled in the sample interval, then $\omega = c\omega_s$, and it can be shown [5] that

$$A_{jf}(k) = \begin{cases} N_f V_j & k = c \\ 0 & k \neq c \end{cases}, \tag{36}$$

and

$$\Phi_{jf}(k) = \begin{cases} \phi_j + \pi/2 & k = c \\ \text{undefined} & k \neq c. \end{cases} \tag{37}$$

However, if the sampling is not synchronized with the input frequency, then c' cycles of the input signal will be in the sample interval where c' is not an integer. Many of the frequency components will be nonzero and the two largest

amplitude components will be for k = c, and k = c+1, where c is the integer part of c'. This phenomenon of spreading the single frequency to many frequency components is referred to as leakage in the FFT literature. In this case, none of the amplitudes or phases of the frequency components are related to the input signal as in (36) and (37); the amplitude and phase measured by the FFT is assigned the amplitude of the largest line and its corresponding phase. The results of the simulation show that this phase, which is the phase of the signal relative to the start of the sampling interval, can be in error by as much as 30° to 40°; however, for two channels, the difference in the phase of the largest line in each channel, $\Phi_1-\Phi_2$, is a good measure of the phase between the two channels. Thus, although this method gives a large error for the phase of each channel, if the two channels are sampled simultaneously both will have close to the same error. Figure 7 shows that the differential errors for the FFT method are, at most, a few tenth of a degree (note that 10^{-1} percent is 0.36 degrees).

The interpolated FFT (IFFT)[6] method makes use of the amplitudes and phase angles of the two frequency components with the largest amplitudes, $A_j(c)$, and $A_j(c+1)$. Define

$$\alpha_j = \frac{A_j(c+1)}{A_j(c)}, \qquad 0 \leq \alpha_j \leq 1, \tag{38}$$

and

$$\delta_j = \frac{\alpha_j}{1 + \alpha_j}, \qquad 0 \leq \delta_j \leq 1/2, \tag{39}$$

and

$$a' = \pi \frac{(N_f-1)}{N_f}. \tag{40}$$

Then, the interpolated phase angle, Φ_{jI}, is given by [6]

$$\Phi_{jI} = \Phi_{jf}(c) - a'\delta_j + \frac{\pi}{2}, \qquad A_j(c) > A_j(c+1), \tag{41}$$

or

$$\Phi_{jI} = \Phi_{jf}(c+1) - a'(\delta_j-1) + \frac{\pi}{2}, \qquad A_j(c) < A_j(c+1). \tag{42}$$

The simulation showed this phase angle to have a much smaller error than the FFT derived ϕ_j. However, the interpolated differences phase angle, $\Phi_{1I}-\Phi_{2I}$, in general had a larger error than the FFT difference phase angle (see figure 7).

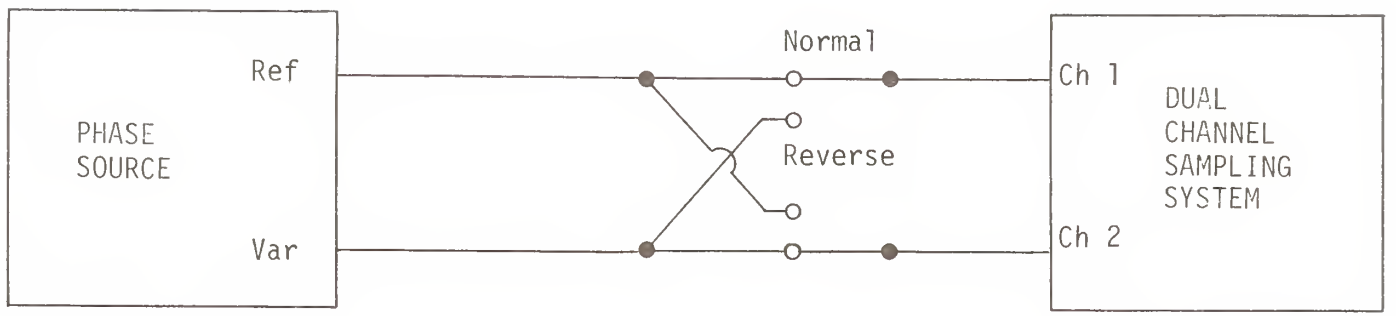

Figure 6. Test setup for measuring differential time delay and phase errors of source and time delays of dual channel sampling systems.

The DFTCF method uses the same formula for calculating a frequency component as the FFT, but uses only the number of samples N_d which cover almost c cyles of the input signal. That is, N_d is selected such that the truncation period, which as before is the difference between the summation interval, N_dT, and an integral number of cycles of the input signal, is less than one sample period T. The DFTCF method also assumes that the frequency, ω, of the input is known. The complex frequency component is then calculated as

$$X_{jd} = T \sum_{n=0}^{N_j-1} v_j(nT)e^{-i\omega nT}. \qquad (43)$$

If the input signal is written as (31), then the real and imaginary parts of (43) are given by

$$Re[X_{jd}] = V_jT \sum_{n=0}^{N_d-1} \sin(\omega nT + \phi_j)(\omega nT - \pi/2), \qquad (44)$$

and

$$Im[X_{jd}] = V_jT \sum_{n=0}^{N_d-1} \sin(\omega T + \phi_j)\sin(\omega nT). \qquad (45)$$

These equations have the same form as the power equations discussed in the first section and can be rewritten in a form like (3), with a constant term and a truncation error term. The phase angle, ϕ_{jd}, is calculated using the above real and imaginary parts in (35). Figure 7 shows this method gives accurate results for nonsynchronized sample sets.

The final phase calculation method is the corrected DFT (CDFT). This approach uses the same method as the DFTCF above, with the addition of a truncation correction similar to the one used in the power case (10). The fractional sample factor, a, is estimated from the known frequency and sample rate. This fraction can be estimated by measuring the number of samples, N_T, in a long sample interval, where $N_T \gg N_d$ as described in [2].

The accuracies of these four phase angle algorithms were compared using a computer program that simulates a dual-channel sampling system. This is the same simulator used to demonstrate the effects of quantization correlation on power measurements (see figure 2). Figure 7 shows the results of simulation where between 31 and 33 cycles of the input signal are sampled in 1024 samples with an 8 bit quantizer. Each point is the standard deviation of the errors for 20 simulations at random phase angles. All four methods give the same result for integral numbers of cycles. These points represent the condition where the input signal is synchronized with the sampling rate. As with the power simulation, the errors are larger for 32 cycles than for 31 or 33 because of the effects of correlation in the quantization errors. The in-between points

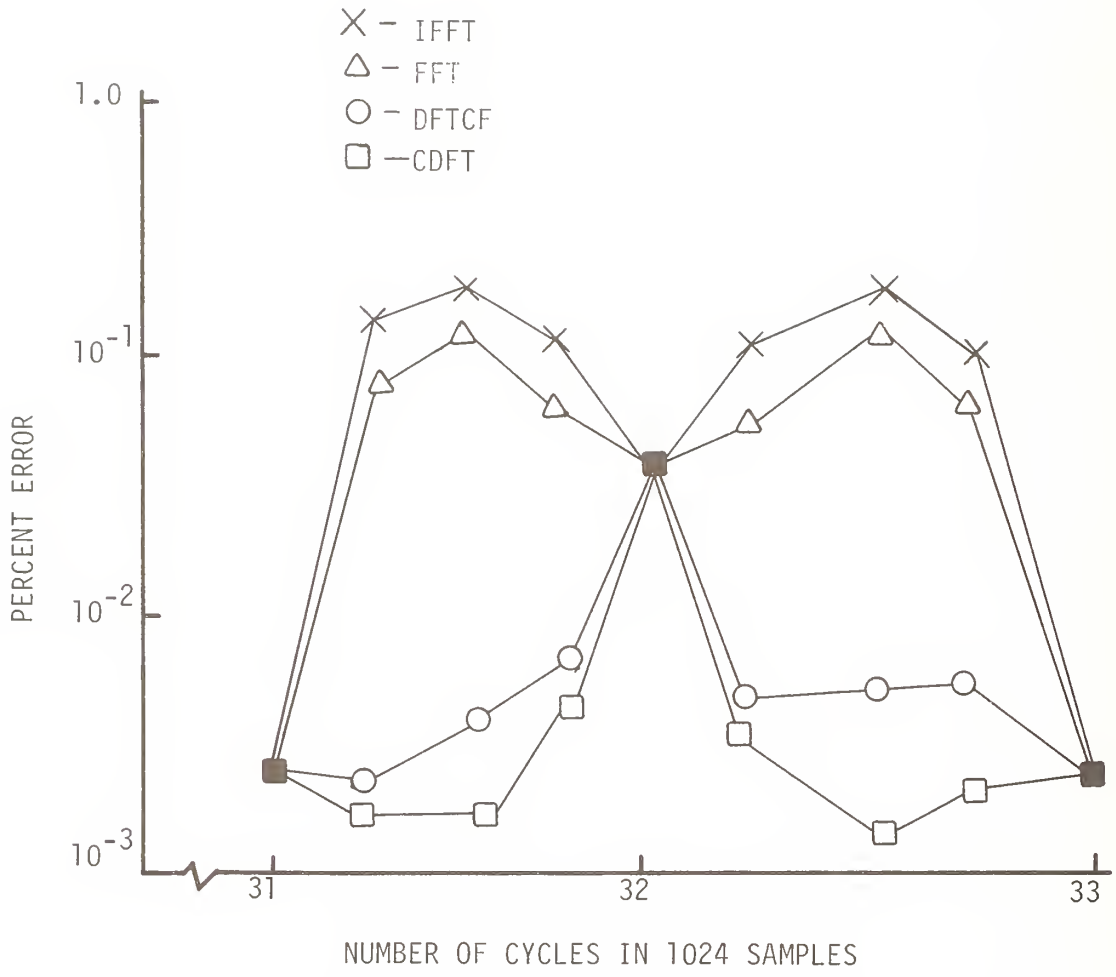

Figure 7. The standard deviation of the error in the calculated phase angle using four algorithms. Twenty simulations were made with random phase angles of two sine waves using 8 bit quantization. Note that 10^{-1} percent is equal to 0.36 degrees.

represent nonsynchronous sampling. The errors for the FFT and IFFT are larger for these values than the errors for the DFTCF and CDFT method. Thus, if the correct frequency is known or accurately measured, this information can be used to improve the accuracy of phase angle measurements for nonsynchronous sampling. Also, repeated measurements can be averaged to further reduce these errors and, as might be expected, the averaging process will reduce the error for the nonsynchronized cases but not for the synchronized cases. In the nonsynchronized cases, these standard deviations represent random error, whereas, in the synchronized cases they represent a bias value for each fixed phase angle.

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DATA CONVERTER TEST METHODS

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1. Introduction

A/D and D/A converters are presently being produced in a vast array of types and models, exhibiting a wide range of design approaches, operating speeds, and accuracies for a wide variety of applications. As might be expected, an equally large number of test methods has been developed, with each addressing the measurement of some specific characteristics of one or more of these types or models. It is the intent of this tutorial to review the more useful, and hence more widely used, test methods pertinent to the characterization of data converters for use in measurement or control instrumentation applications. With a few exceptions, little will be said, for example, about testing converters for applications such as audio and video recording and playback, or communications. The focus has been narrowed by concentrating mostly on static or quasistatic test methods, partly because relatively few dynamic test methods have been proposed, and in part because some dynamic test methods are being addressed in other presentations of this seminar [1, 2].

With this focus in mind, test methods have been included which measure one or more of the following characteristics:

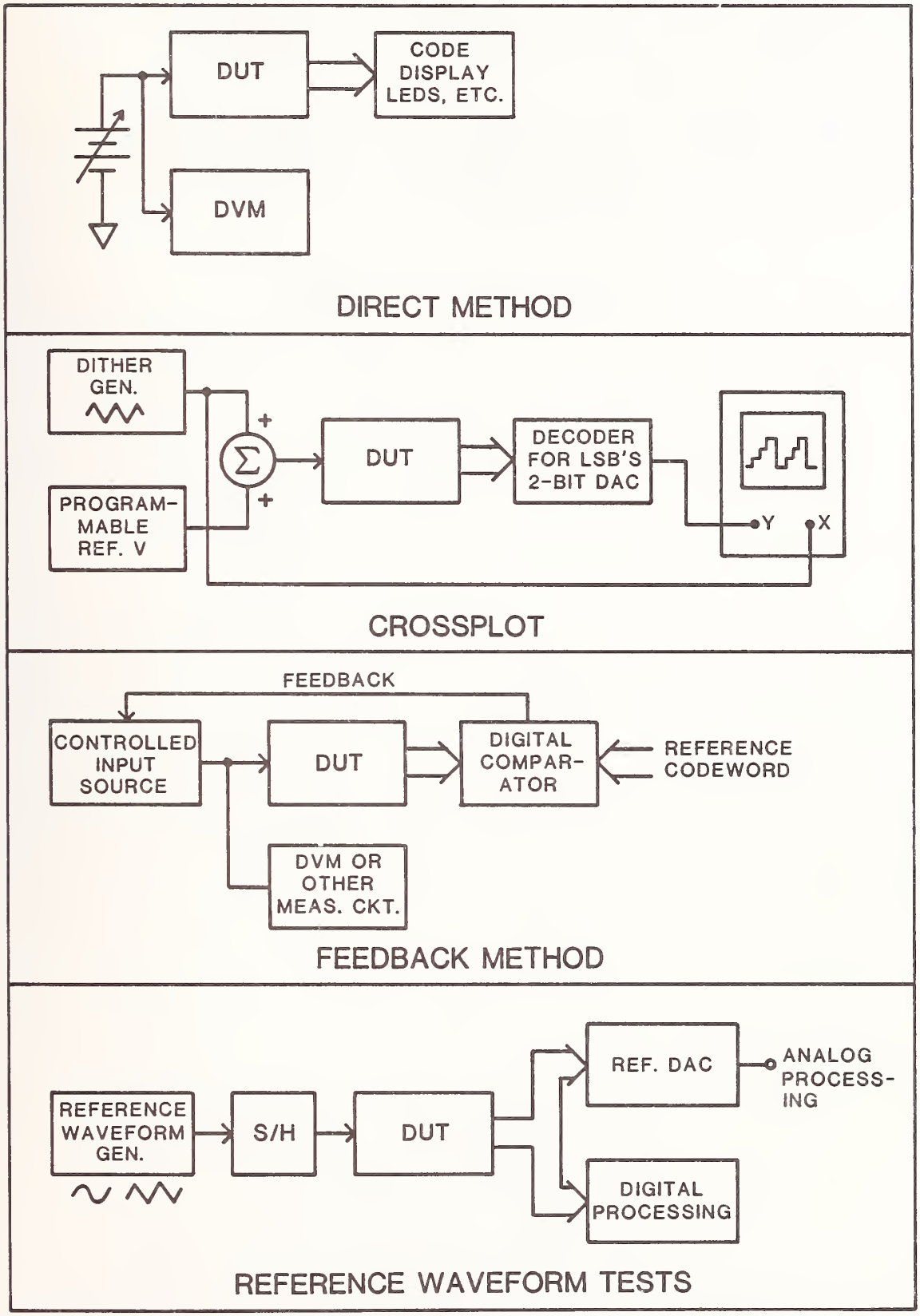
L	Integral Linearity	M	Monotonicity
DL	Differential Linearity	MC	Missing Codes
S	Superposition	N	Input Noise
O	Offset	H	Hysteresis
G	Gain	AC	Alternating Codes
SNR	Signal-to-Noise Ratio or	SR	Step Response
THD	Total Harmonic Distortion		

Characteristics listed in the first column are those generally applicable to both A/D and D/A converters, while those listed in the second column all apply to A/D converters only, with the exception of monotonicity, which usually only applies to D/A converters. Discussion and definitions of these terms can be found in references 4, 6, 8, 11, 12, and 13.

Somewhat arbitrarily, all pertinent test methods have been assigned to eight general approaches, divided equally among approaches for D/A and A/D converters. These eight measurement approaches are discussed below, and are represented schematically in the accompanying figures, along with a listing of the characteristics (keyed to the abbreviations in the above table) which they address, brief indications of their relative strengths and weaknesses, a list of references for further discussion and detail, and other brief comments.

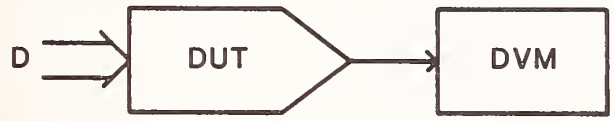
Parameters Measured	Advantages	Disadvantages	Comments	Refs
L DL S O G H	Simple to setup.	Very slow and tedious to perform. Requires operator judgement in locating transition levels.	Used as bench setup for very limited testing.	3 6
L DL O G H N	Gives rapid visual identification of differential linearity errors, hysteresis, noise problems, etc. Does not require accurate ref. except for meas. of O. and G.	Requires manual operation and visual quantification of performance.	Often used in production testing or manual tweaking, and detection of hysteresis and noise problems.	3 6
L DL S O G H SR N	Well suited for fast, automatic testing. Eliminates operator judgement. Can be adapted for dynamic step response testing.	Some output information in terms of specific codeword occurances and distributions is not available to operator.	Becoming industry standard for automated testing. Used in NBS calibration service.	5 8 10 11 7 12
L DL O G SNR THD	Potentially fastest method. All hardware commercially available for many versions.	Requires accurate S/H amplifier. Difficult to derive detailed linearity information. Difficult to correlate results with other methods.	Useful for audio, video, communications, and dynamic testing applications.	13 14 15 17 18 20

TEST METHODS FOR A/D CONVERTERS

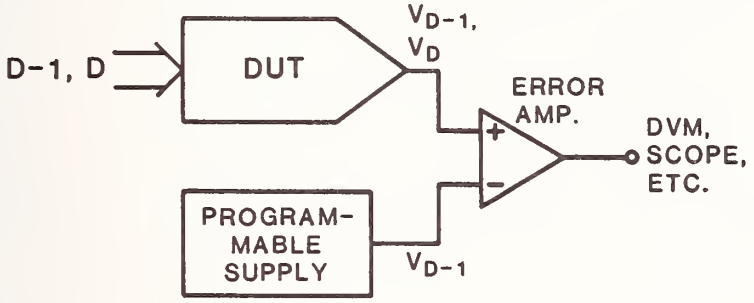


Parameters Measured	Advantages	Disadvantages	Comments	Refs
L DL O G M	Simple to implement in either manual or automatic form.	Very slow, particularly for high resolution converters.	Used as bench setup for very limited testing.	3
L DL	Requires no accurate standard or reference instrument. Simple to implement.	Limited capability. Assumes low superposition errors.	Used in production testing for manual tweaking, and used in self-calibration schemes.	3 6 9
L DL S O G M	Automated versions capable of very fast operation. All codes tests feasible for high resolution converters.	Requires independently calibrated reference DAC with 3-4 bits more accuracy.	Standard method for automated volume testing. Used in NBS calibration service.	3 6 8
SNR THD	Fast, simple to implement. Useful for audio parameters.	Not versatile.		3

TEST METHODS FOR D/A CONVERTERS



DIRECT MEASUREMENT



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0011	0100
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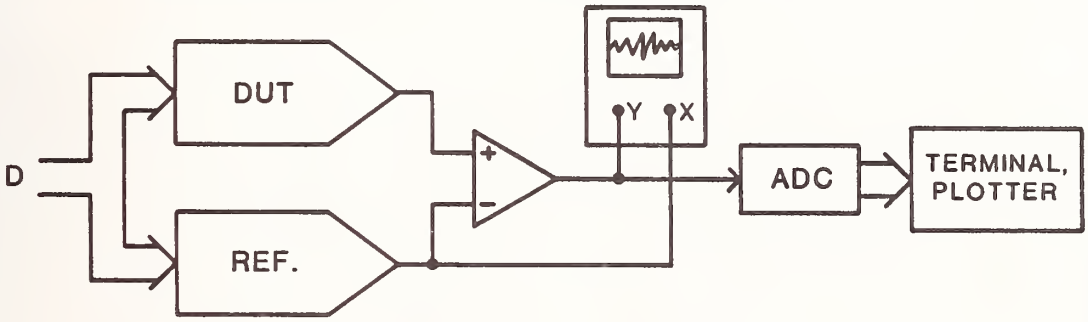
DIFFERENTIAL LINEARITY ERROR METHOD



COMPARISON METHOD

SINEWAVE TESTS

2. Test Methods for D/A Converters

A D/A converter accepts digital input codewords, D, and outputs discrete voltage (or current) levels, according to some codeword/output level correspondence. The purpose of a test method for D/A converters is to accurately measure this correspondence. Perhaps the most obvious approach to this task is the DIRECT METHOD, in which codewords of interest are sequentially input to the converter under test, and the corresponding output levels are measured using an accurate digital voltmeter. If only a relatively few codewords are to be considered, then they can be entered manually via a toggle switch register, and the DVM readings can also be logged by hand. If many codewords are to be tested however, the process can easily be automated by interfacing the converter and DVM to a microcomputer. Even so, as the resolution of the converter under test increases to 12 or more bits the time required to perform a complete test becomes prohibitively long using this method. For example, a complete test of a 12 bit converter, with measurement accuracy of 0.1 LSB, requires 2^{12} measurements to be made to an accuracy of 24 ppm. If one measurement can be made each second, the complete test will take over one hour. Similarly, a 16 bit converter would require an 18 hour test. Therefore, this method is generally limited to bench setups where relatively few codewords are to be tested. Such limited tests can be made, for example, when it has been determined that the test converters will have negligible superposition errors, i.e., that the linearity errors at any given codeword are the simple sum of the errors of the individual bits activated by that codeword. Thus, for such a converter having n bits of resolution it suffices to measure each bit individually, and all bits off, for a total of only n + 1 measurements. Limited test plans of this type are discussed in [3].

For situations where superposition errors are assumed to be negligible, as well as for general measurements of differential linearity errors, the DIFFERENTIAL LINEARITY ERROR METHOD is also useful. With this method, DLE measurements are made without requiring an accurate reference instrument such as the DVM in the previous method. The accuracy requirement is avoided by making only differential measurements of the small changes in output levels corresponding to adjacent codes. The changes are measured by subtracting a constant level nominally equal to the output corresponding to codeword D-1, from both the D-1 level and the D level, amplifying the resulting differences, and displaying them for example, on an oscilloscope. The change in the amplified differences when switching from code D-1 to code D, is simply the amplified change between the two levels. If codes D-1 and D are chosen to represent the major digital code transitions as indicated in the diagram, then the weight of each bit can be measured in terms of the total weight of all bits of lower order. For converters with negligible superposition errors, n pairs of measurements then provides all the information required to compute linearity errors at all codes [9]. Many implementations of this method exist, ranging from simple manual setups to fully automated systems. The DLE METHOD is frequently used on the production line for final adjustment of the bit weights.

When more complete testing is required, especially when superposition errors are significant, the COMPARISON METHOD is most widely used. With this method the device under test is compared directly with a well-characterized reference converter, at many or all input codes. The difference in outputs at each code is amplified, and either displayed directly on an oscilloscope, or

digitized and processed by a microcomputer. Offset and gain differences can be measured and adjusted either with hardware or software. Automated versions are capable of very high speed operation, making extensive (and sometimes all codes) testing feasible. The major disadvantage of this method is the requirement of a reference DAC having substantially greater accuracy (generally by 3 or more bits) than the test unit, and the necessity of providing an independent calibration for it. Nevertheless, this method has found wide usage, and is employed by the NBS data converter calibration service (for D/A converters) using, as the reference standard, an NBS-built 20-bit DAC [8].

For some applications, more global specifications such as total harmonic distortion, may be more useful than the typical linearity specifications, and in these cases, SINE WAVE TESTS are often performed. These tests use digitally generated "sinusoidal" test sequences, which can be strobed into the converter at the specified test frequencies. The converter under test outputs a zero-order hold approximation to a sine wave, and either analog or digital signal processing techniques are then used to evaluate the converter's response. This method differs from the others in that the measurements are inherently dynamic, since the converter's glitches and settling time contribute to the measured distortion. For this reason, however, it is difficult or impossible to directly compare the results of this method with the determinations of static linearity error produced by the other three methods.

3. Test Methods for A/D Converters

As opposed to the case of D/A converters, there is not a unique one-to-one mapping of voltage to codeword for A/D converters. Instead, the quantization process maps a continuous range of input voltages onto each output codeword. The analog levels which define an A/D converter's transfer characteristic are then the extremes of the quantization intervals, i.e., the voltage levels which correspond to transitions between adjacent output codewords. For this reason the testing of A/D converters is more complex, and generally requires means for locating the transition levels prior to their measurement. In the DIRECT METHOD, the operator accomplishes this process by adjusting the input voltage slowly until the desired code transition is detected by viewing a display of the output code states. After the appropriate code-transition level has been set, then the driving input voltage is measured, usually with a (higher precision) digital voltmeter. As with the direct method for D/A converters, this method is very slow and tedious. Furthermore it requires operator judgement in locating transition levels when significant noise is present. On the other hand, it is simple to implement as a bench setup for very limited testing.

A more comprehensive test method, and one that is often used in production testing, is the CROSSPLOT. With this method, a region of interest on the A/D transfer characteristic is first selected by setting a programmable voltage source to bias the input to the desired level, e.g., to the vicinity of a major code transition. A corresponding bias code is then generated by the test converter. The last two or three bits of this code are decoded with a simple resistor network (i.e., a two or three bit DAC), so that the least significant bits can be displayed on an oscilloscope. Codewords on either

side of the bias code will be generated if the input voltage is swept above and below the bias level, and in this manner, all of the code transitions in the vicinity of the bias code can be observed on the decoded output. A low frequency, low amplitude sine wave or triangular wave "dither" generator is commonly used to perform the sweeping operation, and to drive the x-axis sweep of the oscilloscope. The resulting output is a plot of the local code states around the selected code. The code transition levels and their spacings are readily observed, giving rapid visual identification of differential linearity errors, hysteresis, and noise problems. With care and the use of a calibrated, programmable bias voltage source, the system can be calibrated so that offset, gain, and integral linearity errors can be measured as well. Because the method relies on visual quantification of performance, however, the results are still operator-dependent, and the method is suitable for examining only a limited number of test regions, these being typically the major transitions where differential linearity errors, glitches, and hysteresis problems are greatest.

Most of these limitations are eliminated with the FEEDBACK METHOD. This technique is essentially an automated version of the DIRECT METHOD, and the function of the operator in seeking code transition levels is replaced by a feedback loop. Thus, the input voltage source is automatically controlled by the relationship of the converter's output code to a designated reference code. The control loop is designed to drive the input voltage to the code transition level bounded (on one side) by the reference code. Once the transition level has been reached, then it is measured using a digital voltmeter or other suitable equipment. The entire process is easily automated, with the controller generating the reference codewords and logging the voltage measurement data. The controlled input source is generally either a high resolution D/A converter, or an analog integrator whose input can be switched between positive and negative sources. This latter method is implemented in the NBS test system used in the data converter calibration service [8], and a reference DAC and comparison circuit are used to make the voltage measurements.

The FEEDBACK METHOD is well suited for fast, comprehensive testing and completely eliminates operator judgement. In addition to offset, gain, and differential and integral linearity errors, the general method can be adapted as well to measure equivalent input noise and hysteresis, to detect missing codes, and to perform dynamic step response testing [7, 8, 11]. On the other hand, for high resolution converters, an all codes test using the feedback method can still be time consuming. For accurate measurements to be made in the presence of significant transition noise, the feedback loop must be locked for as many as 100-200 conversion cycles of the test converter for each code transition level measured, and more time must be allowed to seek and lock on to each transition.

Finally, A/D converters may also be characterized using REFERENCE WAVEFROM TESTS. This approach is analogous to the sine wave tests described for testing D/A converters. The method relies on the ability to generate reference waveforms having very well defined amplitude and waveshape. For this reason, sinewaves are particularly well suited since they can be filtered rather easily to produce very low distortion signals. To obtain reasonable results the A/D converter under test must generally be preceded by a Sample/Hold amplifier to freeze the signal during the conversion process.

This requirement necessarily introduces the errors of the S/H amplifier into the measurement, however.

The digital output data from the test converter can be processed using either analog or digital techniques, the first with an accurate decoding DAC followed by a spectrum analyzer, and the second using direct digital signal processing methods. Typical test results include total harmonic distortion or signal-to-noise ratio, and differential linearity errors. As with the sine wave tests for D/A converters, the results from REFERENCE WAVEFORM TESTS include dynamic error sources such as timing jitter, and cannot be directly compared with the results from the other test methods described above. However, REFERENCE WAVEFORM TESTS are potentially very fast and can often be implemented using commercially available hardware. They are used primarily in testing components for communications applications.

4. Conclusion

In choosing the most appropriate test method for a given situation, a number of criteria should be considered. These include the work load to be handled, the number of different converter types to be accomodated, the resolution and accuracy requirements, the specific measurement parameters of interest, and the testing strategies to be implemented.

With so many codestates possible, the issue of a good testing strategy is especially important, particularly for high volume testing. An effective testing strategy depends on the kind of test information required, the measurement confidence needed, and the availability of adequate error models for describing the converters to be tested. With care and sufficient error modeling information, limited test plans can often be developed which are both efficient and effective in accurately predicting errors for all codes. This is especially true for D/A converters, since their superposition errors are generally small and very systematic.

Finally, if it has been decided that a flexible, fully automated test system is required, then a decision remains as to whether to buy one of the many commercial test systems now available, or to assemble your own. Almost all of the commercial systems make use of the COMPARISON METHOD for D/A converters, and the FEEDBACK METHOD for A/D converters, and are generally suitable for testing converters of up to at least 12 bits of resolution.

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SETTLING TIME MEASUREMENTS

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1. Introduction

Methods of measuring device settling times (STs) from 5 μs to less than 20 ns with corresponding accuracies of 1 ppm and 0.1% are described in this paper. Most of these methods are thought to represent state-of-the-art techniques, developed at NBS and in industry. Some of the ST measurement methods discussed are described in a March, 1983 paper [1]. Only a brief review of these methods will be given, showing only the salient features. Some of the NBS work has been concerned with measuring thermally induced transients and offsets in devices under test (DUTs). Methods of measuring these effects with ST measuring circuits are described.

2. Performance Criteria

Settling time (ST) is an important measure of the dynamic performance of D/A converters (DACs), operational amplifiers, precision voltage-step generators, analog multiplexers, and progammable power supplies. Settling time for these devices can be defined as follows (see figure 1). Following a prescribed input change, usually full-scale range (FSR), the settling time of the device is the time required for the output to reach and remain within a given error band whose center coincides with the final value. The settling error is equal to 1/2 the error band. For DACs, the error band is usually ±1/2 of a least significant bit (LSB). Note that part of the settling time is the time interval $t_2 - t_1$, the delay of the output relative to the input. This definition is also applicable to voltage step generators, triggered at time t_1. In some applications, the time interval $t_2 - t_1$ may be neglected, e.g., when a fast DAC or voltage-step generator is used to provide the stimulus for measuring the ST of an amplifier or the response of a waveform recorder.

An additional measure of the dynamic performance of these devices is the thermally induced transients and offsets caused by changes in repetition (or switching) rate, duty cycle, and output amplitude. These effects, as well as ST, cause the device accuracy to be different under severe dynamic conditions than under, say, quasi-static conditions.

3. Measurement Methods

3.1. Settling Time Circuit Problems

Common problems encountered in designing ST measuring circuits and systems are:

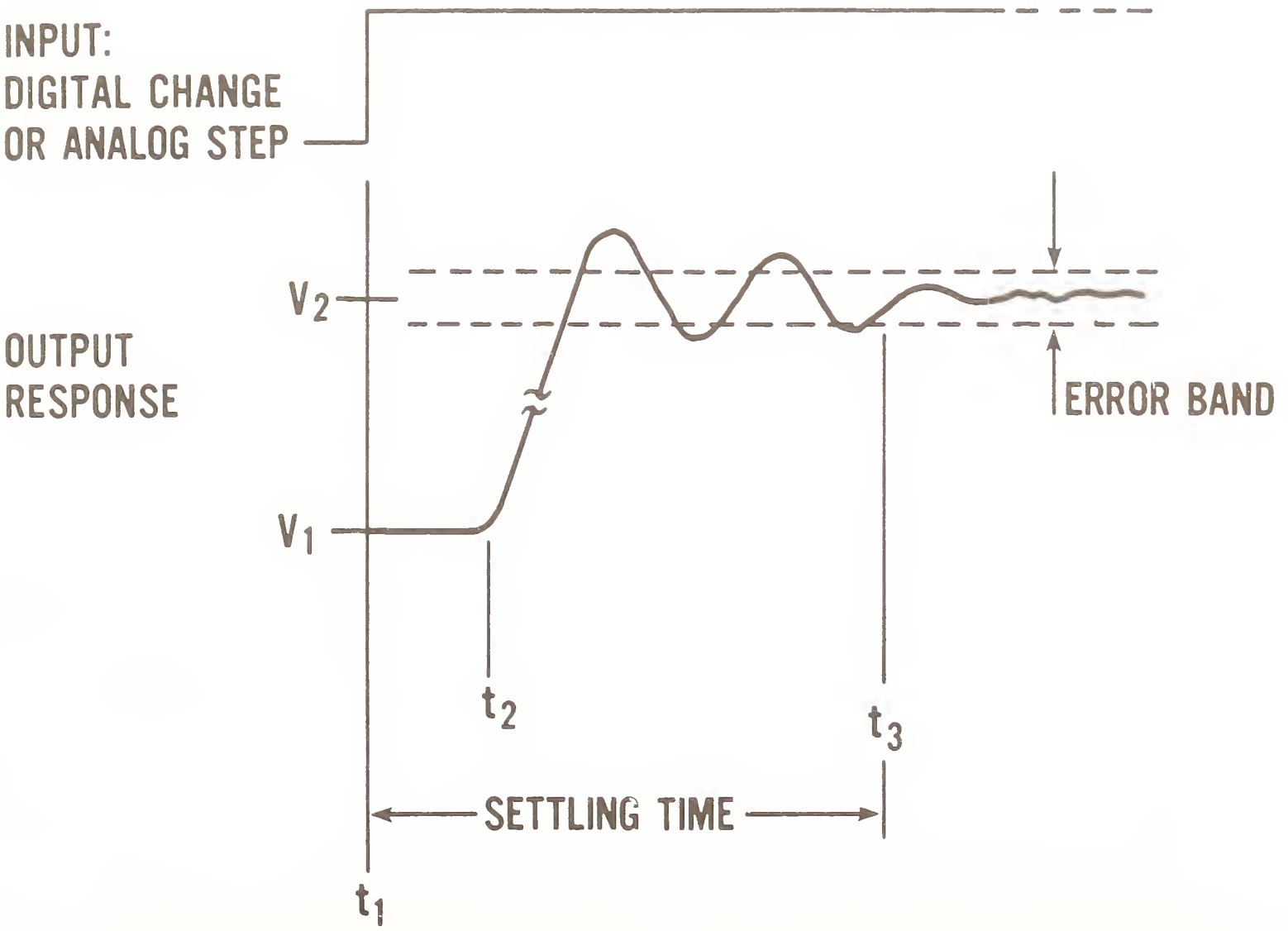


Figure 1. The definition of settling time. Also applicable to voltage step generators, triggered at time t_1.

(1) Overdrive of the ST circuit or oscilloscope connected to the output of the ST circuit,

(2) Thermally induced transients and offsets, caused by self-heating of components -- particularly transistors,

(3) Capacitive loading of the ST circuit, caused by an oscilloscope, connectors, cables, etc., and

(4) Insufficient gain-bandwidth of the ST circuit or associated oscilloscope.

These problems are not mutually exclusive. For example, increasing the bandwidth or using an active probe (or other buffer) to minimize capacitive loading usually increases thermal transients and offsets, and improving the voltage or current limiting to decrease circuit or oscilloscope overdrive may decrease gain-bandwidth.

If items (1) and (2) are very small, the ST measuring system can be used to measure thermally induced transients and offsets in the DUT. Also, if (1) and (2) are very small, items (3) and (4) largely determine the settling time T_t of the ST measuring system itself. Methods used to minimize the four types of problems listed above and the possible tradeoffs will be discussed in the following sections.

Use of a Schottky diode voltage-step generator to measure the settling time, including thermal effects, of ST measuring circuits is described in [1]. A step generator of this type is useful in determining the magnitude of each of the above problems. (Also, see reference 2 for a discussion on this type of pulse generator.)

3.2. Settling Time of the Test Circuit

In general, the ST of the test circuit (T_t) is not small enough to be ignored when measuring T_d, the ST of a DUT. However, if T_m is the observed settling time, i.e., the combined ST of the test circuit and the DUT, the value of T_d can usually be approximated by either

$$T_d \simeq \sqrt{T_m^2 - T_t^2} \qquad (1)$$

or

$$T_d \simeq T_m - T_t \ . \qquad (2)$$

The last relationship applies if the settling of the test circuit largely follows the DUT settling, rather than occurring simultaneously.

3.3. High Resolution Settling Time Measurements

The most detailed "real-time" examination of voltage steps can be made using a wide-band oscilloscope with a sensitive vertical amplifier. Oscilloscopes designed for real-time measurements are available with maximum vertical deflection sensitivities ranging from 10 μV/cm to 2 mV/cm. Corresponding bandwidths are typically 1 MHz and 200 MHz. Deflection

sensitivities as high as 20 - 50 μV/cm are useful for settling time measurements. Since the voltage step illustrated in figure 1 can be as large as 20 V, devices for measuring settling time often employ a biased voltage divider to shift level V_2 to near zero potential and use various circuits to limit the output signal prior to the voltage transition. This shifting and limiting ideally permits accurate measurement of voltage variations near the V_2 level and avoids overdrive of the oscilloscope prior to the transition.

These techniques are represented generically by Circuit A of figure 2. In addition to the voltage limiting at terminal p, this type of circuit further limits the voltage applied to the oscilloscope through use of either (or both) series current or shunt voltage limiters. A number of circuits used in industry employ this technique (e.g., see [3], [4]). NBS has used versions of this circuit to measure settling times in the range of 50 ns to 1 μs with corresponding settling errors of ±50 ppm and ±2 ppm of 10 V FSR. Circuit B employs carefully timed gate pulses which close switch S after voltage V_p has settled to within several millivolts of 0 V. Diode bridge or transistor switches are usually used for this circuit [5]. For both circuits, time t_1 represents the start of the negative voltage transition from the device under test (DUT) and t_2 is the time when the voltage enters the selected error band (not shown).

Before discussing detailed applications of these techniques, it should be mentioned that Circuits A and B can be dispensed with if the variable dc reference is replaced with a square wave generator whose output levels complement the DUT output levels [6]. This technique minimizes voltage V_p sufficiently to permit a direct connection to an oscilloscope. However, the ST measurement accuracy tends to be reduced by the generator waveform imperfections.

An ST circuit which incorporates both circuit techniques of figure 2 into its design is shown in figure 3.[1] This circuit was designed to measure DAC settling times in the 1-5 μs range to within a settling error of ±2 ppm of 20 V FSR. This circuit was also required for measuring the settling time of the voltage step generator employed in the NBS Data Converter Test Facility to dynamically test A/D converters [7]. The circuit basically consists of the following: 1) a precision voltage divider for comparing input signal levels, V_2, up to ±10 V with reference voltages, V_r, of the same nominal magnitude but of opposite polarity; 2) a wide-band amplifier (AR1), which has a gain of 10 for very small values of $|V_s(t) + V_r|$, for amplifying the signal output from the divider center tap; and 3) transistor series and shunt switches (S_1 and S_2), which connect the oscilloscope to either the amplifier output or signal ground (0 V), respectively. These switches are controlled by a window comparator which senses the magnitude of the output voltage from the amplifier, thus avoiding overdrive of the measuring device by excessively large signals. Switch S1 closes and S2 opens when the magnitude of the voltage at node d decreases to ~10 mV. Use of AR1 permits a relatively low sensitivity (1 mV/cm), wide bandwidth (100 MHz) oscilloscope to be used.

The next circuit (figure 4) was designed to work with very sensitive oscilloscopes without causing overdrive. It can be used to measure settling times as small as 5 μs to a settling error of ±1 ppm of 20 V FSR. The amplifier is used to limit the signal to the oscilloscope during the time intervals when the signal is not being viewed. If the settling time following the DAC voltage

[1] The circuits shown in figures 3, 4, 5, 8, 9, 14, and 15 were developed at NBS. More information may be obtained on these circuits from [1], or by contacting the author.

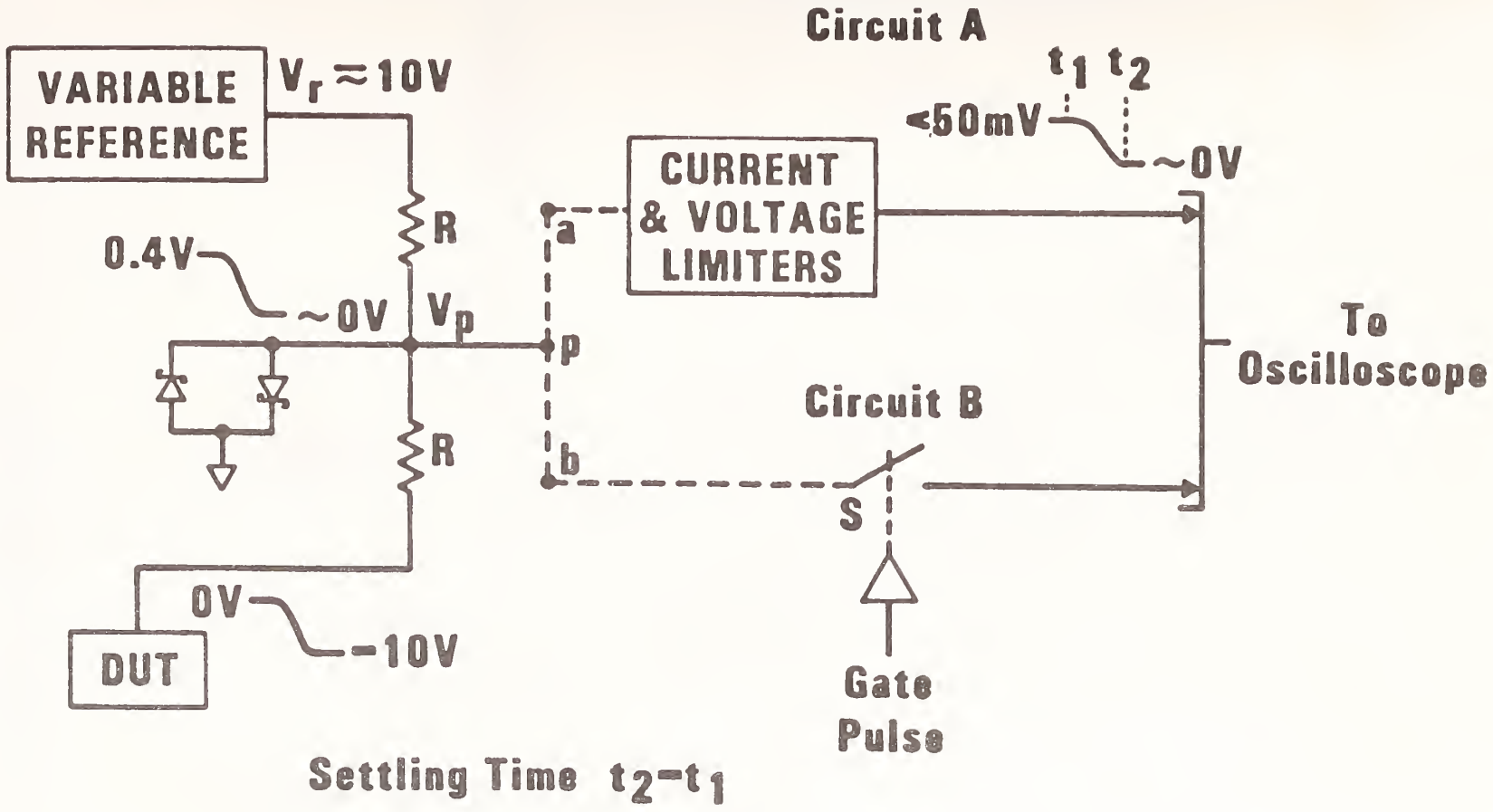


Figure 2. Circuits for measuring the settling time of voltage-output devices.

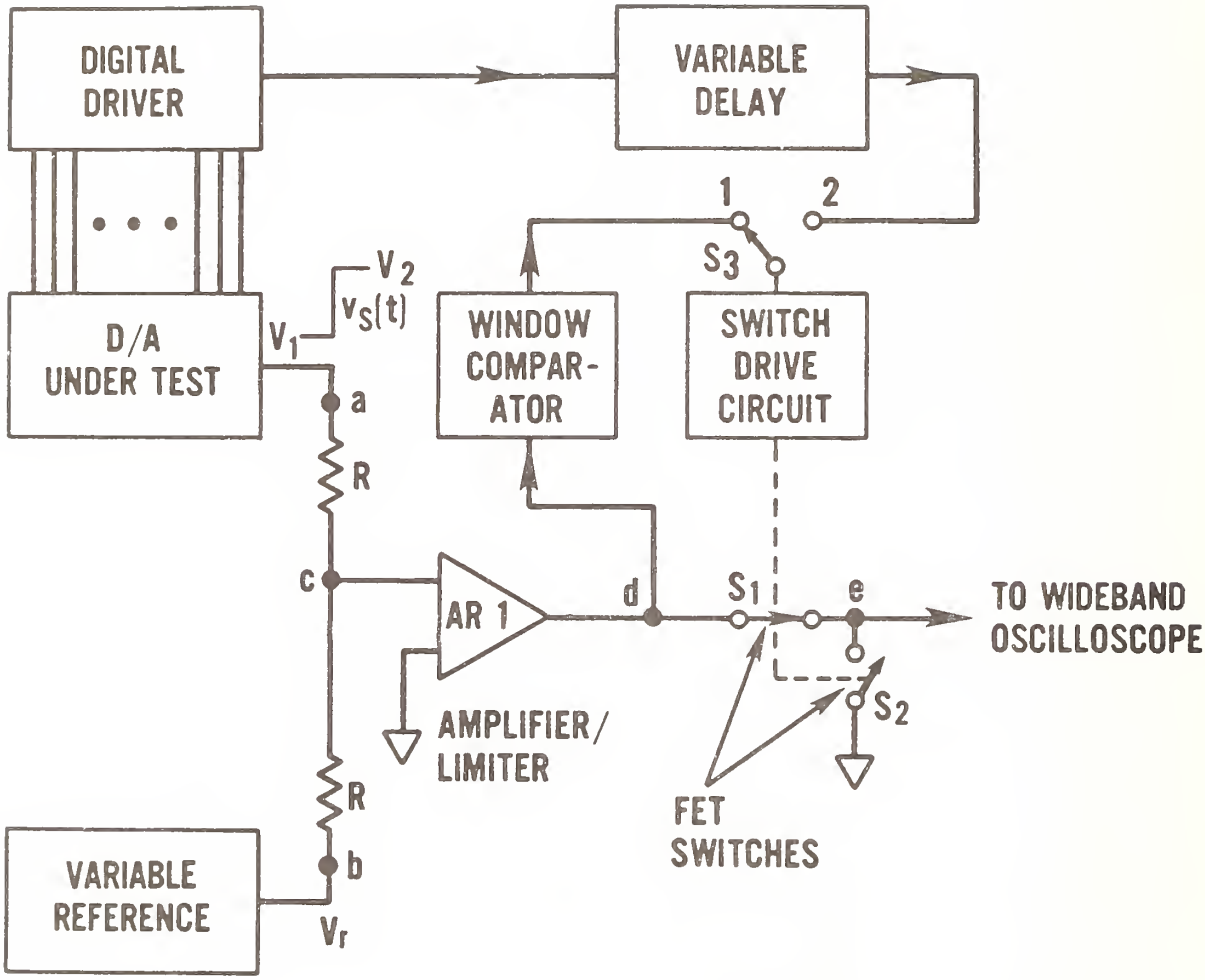


Figure 3. Circuit for measuring settling times in the 1-5 μs range to a settling error of ±2 ppm of 20 V FSR.

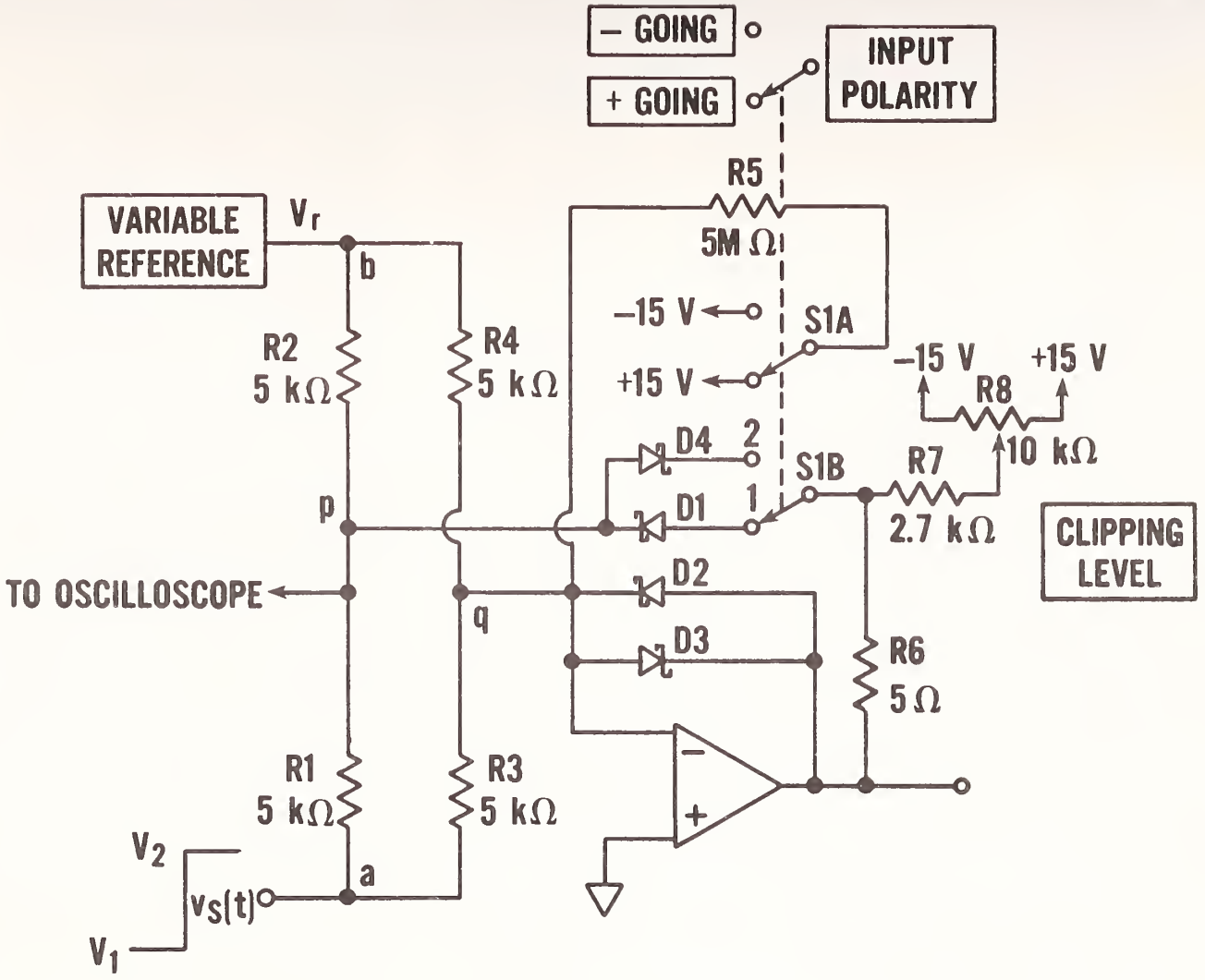


Figure 4. Circuit for measuring settling times as small as 5 μs to a settling error of ±1 ppm of 20 V FSR. This circuit is insensitive to changes in switching rate, duty cycle, and amplitude of the input signal.

transition from V_1 to V_2 is to be examined, and reference voltage V_1 (opposite in polarity to V_2) is adjusted so that $|V_2|$ is slightly larger than $|V_1|$, the the circuit operation is then as follows: Prior to the positive voltage step, D1 and D2 conduct. Diode D2 holds terminal q within microvolts of ground potential, and D1 holds terminal p within a few millivolts of ground. After $V_S(t)$ makes the transition to V_2, the output of the amplifier swings negative, reverse biasing D1 and D2. Thus, terminal p is isolated from the amplifier circuit, leaving only resistance in the signal path to the oscilloscope. To view negative going steps, the switch is changed to position 2. The oscilloscope most suitable for use with this circuit had a bandwidth of 1 MHz and a sensitivity ranging up to 10 μV/cm. (A 50-100 μV/cm sensitivity was usually used.) This test circuit was used to measure the settling time and recovery time effects of the NBS DAC-18 (18 bit D/A converter standard)[8], now used as a check standard for the NBS Data Converter Test Facility [9]. The circuit has also been used to test a number of commercial 16- and 18-bit DACs.

A sensitive analog comparator, designed for a special application to detect input imbalances as small as ±1.5 μV [10], can also be used as a very sensitive ST measuring circuit. The measured settling time T_t of this comparator with minimum noise filtering is 15 μs, to a settling error of ±0.4 ppm of 20 V FSR.

3.4. High Speed Settling Time Measurements

The remainder of this paper will be used to describe high speed ST test circuits. In most of these circuits, the ST measuring circuit is packaged in a small shielded container having a male BNC output connector that can be connected directly to the oscilloscope (or other measuring device) input connector, without the use of a coaxial cable. The effect of interconnecting cable attenuation will be shown in a later section.

A high speed ST circuit with current and voltage limiting is shown in figure 5. The bridge circuit and "zero bias" diodes D7 and D8 (or D9 and D10) function as current and voltage limiters, respectively. The maximum bridge output current is ±50 μA and the maximum voltage developed across D7 or D8 is ~±50 mV. The zero bias diodes are special high frequency Schottky diodes designed to rectify at very low signal levels. The purpose of buffer Q1-Q2 is to minimize the effect of oscilloscope capacitance. Transistor Q2 is used to shift the output voltage to approximately the input voltage level of Q1. If the wide-band amplifier AR1 is used instead of buffer Q1-Q2, the gain for the DUT input is increased from 2/3 to 2. Gain is determined by changing the reference voltage a known amount and measuring the output voltage change. With the Q1-Q2 buffer, this circuit can be used to measure STs as small as 50 ns to within ±0.01% of 10 V FSR. With AR1, STs as small as 70 ns can be measured to ±0.02% of 2 V FSR. The maximum measured self-heating effect of these circuits is approximately ±0.3 mV, referred to the input.

Figure 6 shows some types of current limiters that have been employed in ST measuring circuits. Maximum computed self-heating effects, using discrete transistors and diodes, is in the order of ±0.02, ±2 and ±10 mV (referred to the input) for circuits (A), (B), and (C), respectively. The corresponding ST-measuring capabilities range roughly from 50 ns to 15 ns. Circuit (C) is usually cascaded with a complementary stage for additional gain and to shift the output voltage level to ~0 V.

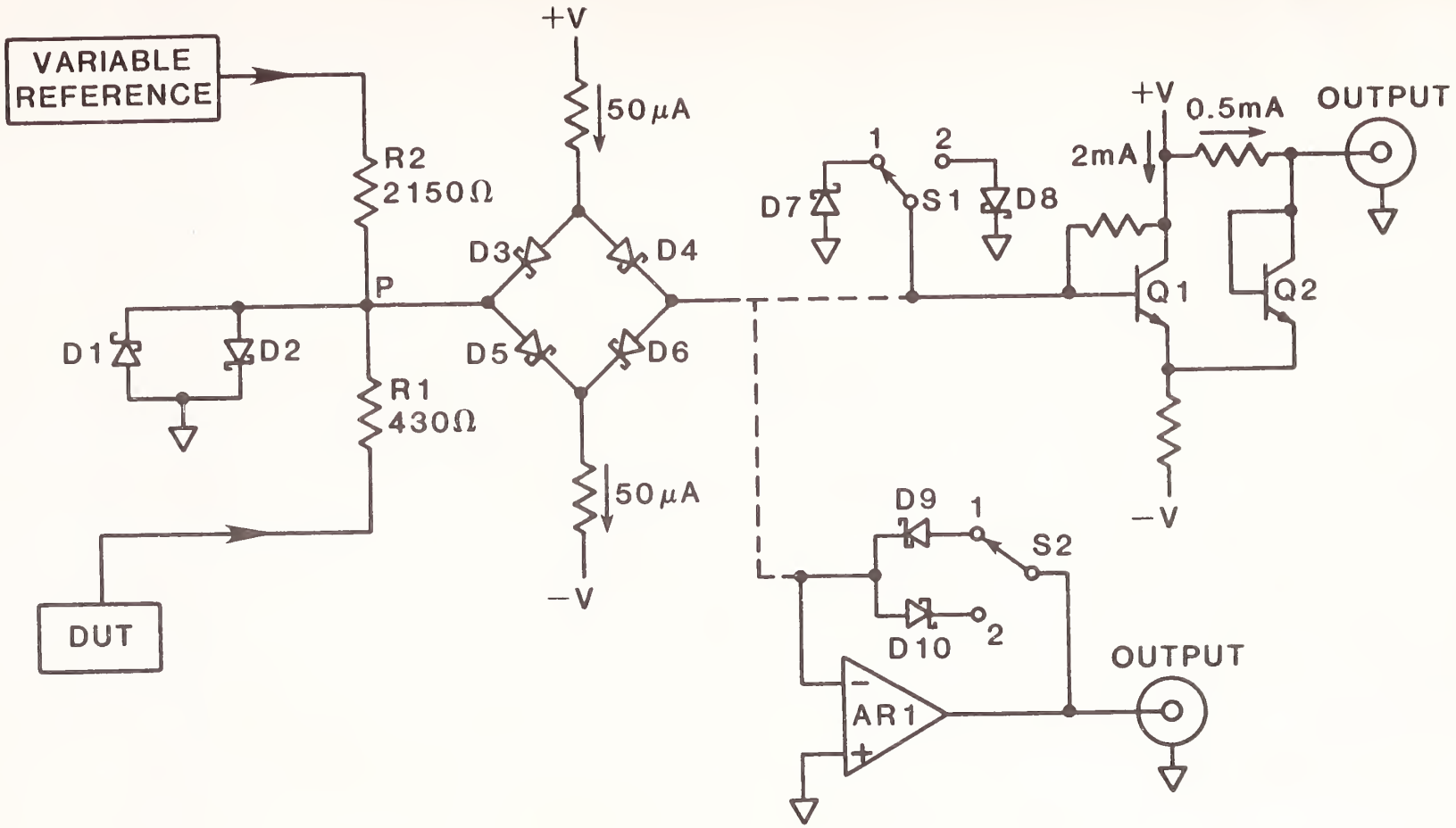


Figure 5. Circuit suitable for measuring STs as short as 50 ns to within ±0.01% of 10 V FSR using the Q1-Q2 buffer, and as short as 70 ns to within ±0.02% of 2 V FSR using AR1. The maximum self-heating effect with these circuits is approximately ±0.3 mV, referred to the input.

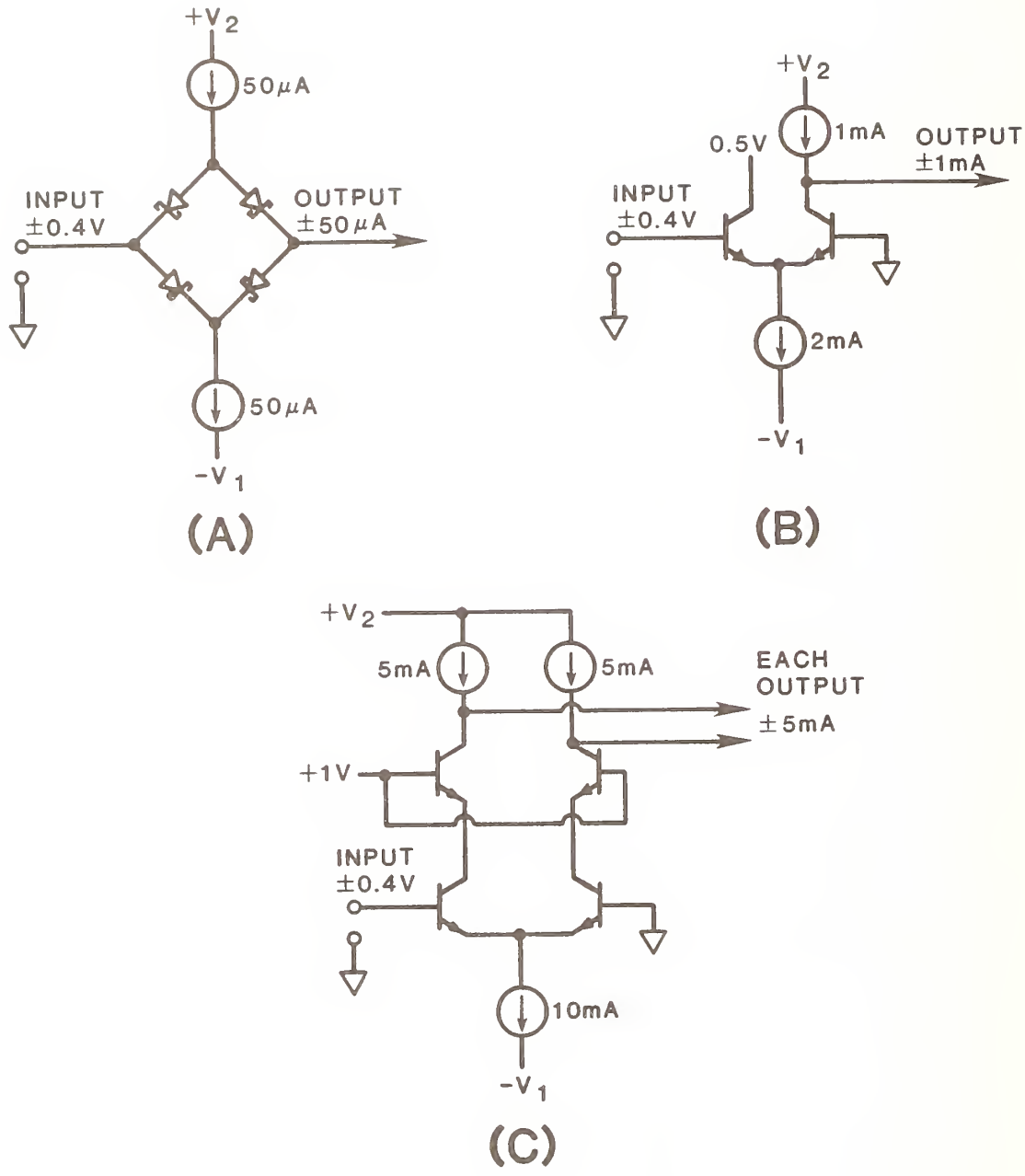


Figure 6. Some types of current limiters used in ST-measuring circuits. Maximum computed thermal effects referred to input, using discrete transistors and diodes, is in the order of ±0.02, ±2, and ±10 mV, for circuits in figures (A), (B) and (C). ST-measuring capability ranges (roughly) from 50 ns to 15 ns.

The use of a coaxial cable for interconnections can be a source of error in ST measurements. If the DUT is connected to the ST measuring circuit with an unterminated cable, cable capacitance or voltage reflections may increase the ST. If the cable is terminated in its characteristic impedance, high frequency attenuation will affect the ST measurement. Figure 7(a) shows the settling of a +5 V to -5 V transition from a state-of-the-art 12-bit DAC, using the measurement circuit shown in figure 5 (with buffer Q1-Q2). The lowest trace is the digital input to the DAC and the upper three traces (from bottom to top) are the ST circuit outputs for:

(1) A direct connection between DAC and ST circuit (no cable) and using a high impedance termination

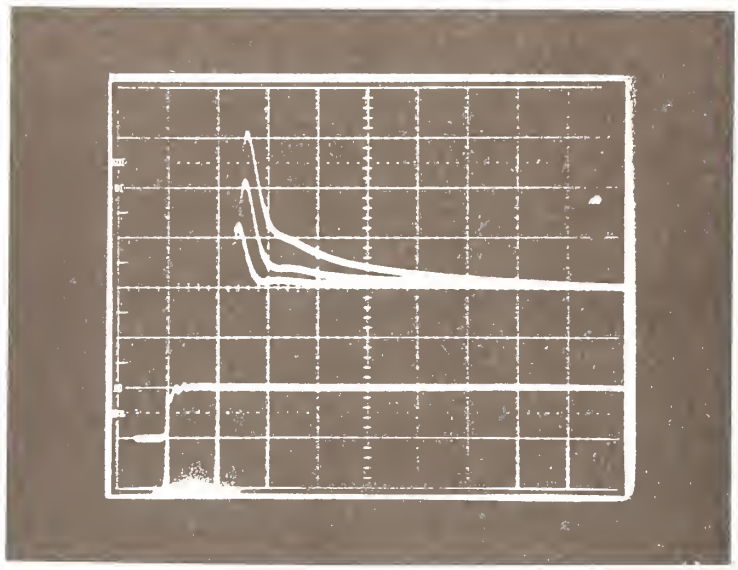
(2) Same as (1), except that a 50 Ω termination is used and

(3) Two feet of RG-58/U cable, terminated in 50 Ω, is used to connect between the DAC and the ST circuit.

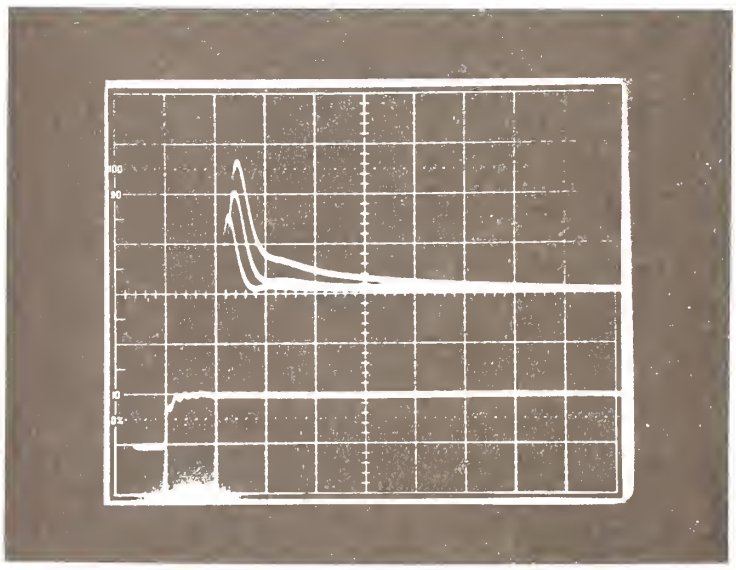
The measurement sensitivity for these three traces was 0.1%(of 10 V FSR)/cm. It is seen that high frequency attenuation in the terminated cable increases the settling error by approximately 0.07% and 0.04% at 200 ns and 300 ns, respectively, after the digital input to the DAC. The measurements were repeated using a peak detector with a 0.15%(of10 V FSR)/cm sensitivity (see figure 7(b)). High frequency attenuation in much longer transmission lines is treated in reference 11. The peak detector is described in a later section.

3.4.1. Current Output Devices

Current-output devices generally have a smaller ST and a smaller output voltage than voltage-output devices. Wide-band amplification is sometimes employed in Circuit A of figure 2, increasing the sensitivity sufficiently for ST measurements of current-output devices. (The DUT is connected directly to terminal p.) STs as short as 35 ns to within ±0.012% of 10 mA FSR have been reported using this technique [12]. Another type of test circuit for measuring the ST of current-output devices is shown in figure 8. The circuit employs a current-balancing technique to minimize the voltage applied to the oscilloscope. Switches S1 and S2 are in position 1 prior to time t_1, and in position 2 after t_1. Thus, the current in R_L is essentially zero except for the time interval between t_1 and t_2 when the DUT output current is settling. This technique is applied to the testing of a 12-bit DAC in figure 9. The TTL-to-ECL translator is used to switch the test DAC between all bits off to all bits on. The translator also supplies the drive current for transistor Q, which is turned off when the DAC bits are turned on. Turning Q off transfers I_2 from D3 to D4. Currents I_1 and I_2 are adjusted to be approximately equal to the DAC current with all bits on. Therefore, the value of $V_L(t)$ at the output is approximately 0 V before and after switching I_2. The intervening switching transient can be adjusted for minimum average value by the delay adjustment. Since thermal effects are negligible in this test circuit, it is well suited to measuring recovery time effects in the DUT. A unity-gain FET probe can be used to reduce the capacitive loading at the output to 3 pF. Thermal effects in the probe can be isolated from those of the DUT [1].



(a)



(b)

Figure 7. ST measurements for a 10 V transition from a voltage-output DAC. The sweep speed is 100 ns/cm. A limiter type of ST circuit with ±0.1%(of 10 V FSR)/cm sensitivity was used for Fig. 7(a); a peak detector with ±0.15%(of 10 V FSR)/cm sensitivity was used for Fig. 7(b). The upper two traces are for a 50 Ω termination using 2' of cable and no cable, respectively. The lowest of the three traces was for a high impedance termination.

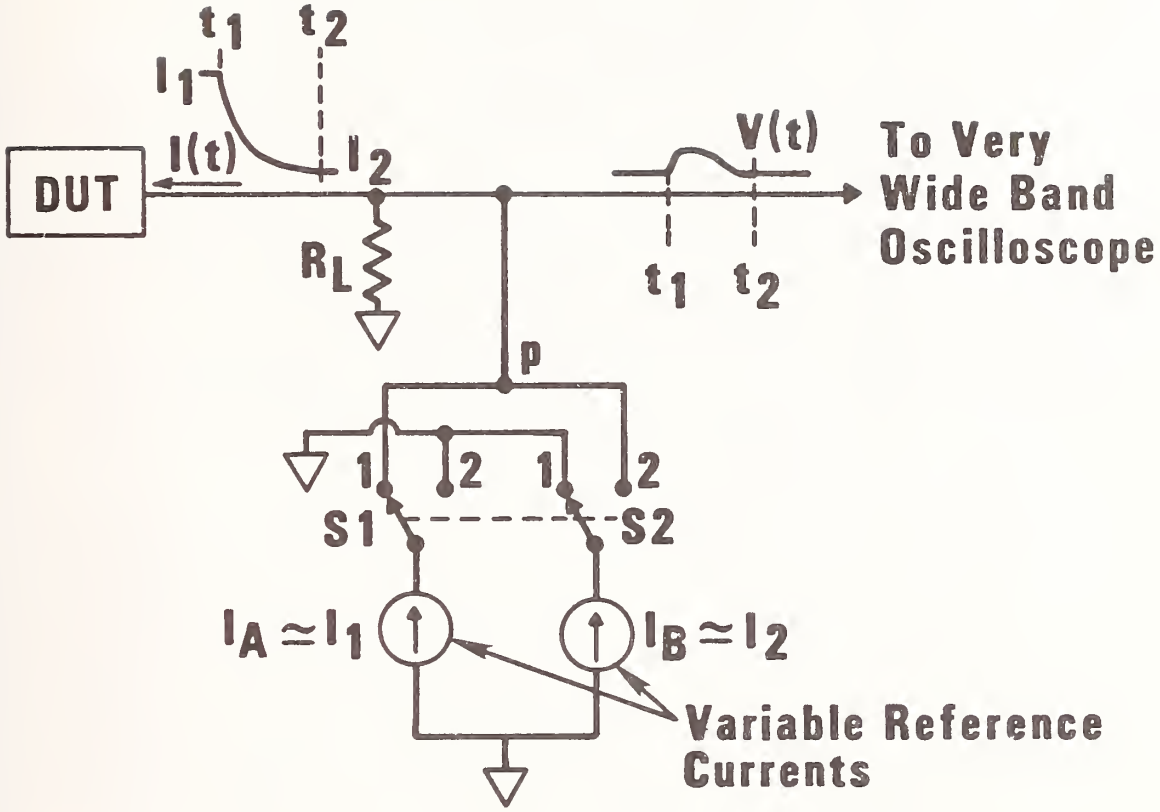


Figure 8. Circuit for measuring the settling time of current-output devices.

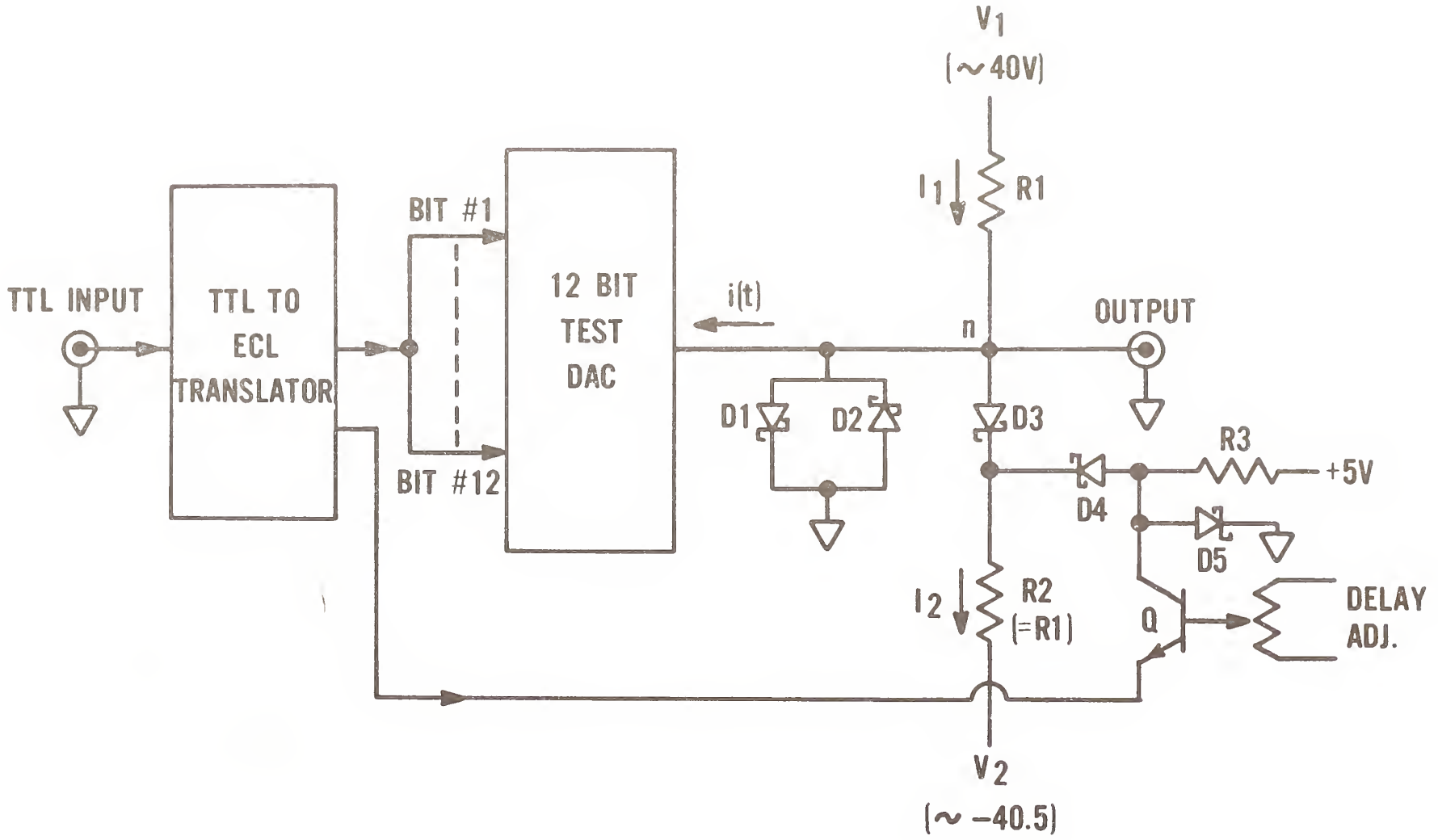


Figure 9. The technique shown in Fig. 8 as applied to testing a 12-bit DAC. Current I_2 is switched from D3 to D4 when the DAC current is turned on.

3.4.2. Comparator Circuits

Window comparators have been used to measure the ST of very high speed 6 and 8 bit current-output DACs [13]. These comparator circuits have also found application in automatic systems for measuring the ST of higher resolution voltage-output DACs [14]. These "real-time" measuring circuits have resolutions of 2-3 mV, typically. "Equivalent-time" measuring circuits, employing a sampling comparator, have been used recently to measure STs of approximately 5 ns to within 100 μV in the test of 8-bit video DACs [15]. Similar sensitivities have been obtained using this kind of circuit for testing 12-bit DACs with STs of approximately 35 ns [16].

The basis for these equivalent time circuits is the sampling voltage tracker (SVT) for analyzing periodic signals [17]. The SVT consists of a high speed sampling comparator and a voltage integrator in a feedback loop, and can be represented as shown in figure 10. The strobe pulses, 5 to 10 ns wide, cause the input waveform f(t) to be sampled (compared with the output voltage V_D of the integrator) at instants in time coinciding with the trailing edges of these pulses. Assume that the period of f(t) is T and that the value $f(t_1)$ is to be measured. Then, the strobe pulses must be timed to sample f(t) at times t_1, $t_1 + T$, $t_1 + 2T$, ..., etc. If, at the instant of a sample, $f(t) > V_D$, the output of the comparator $V_C(t)$ changes to the low state (-1.75 V) and V_D slowly ramps more positive. If $f(t) < V_D$, $V_C(t)$ changes to the high state (-0.85 V) and V_D slowly ramps more negative. The result of these comparisons is to drive V_D positive or negative until it nearly equals the amplitude of $f(t)$ at the instants of comparison. When $V_D \simeq f(t_1)$, the duty cycle of $V_C(t)$ is ~50% and V_D successively ramps up and down about an average value of $f(t_1)$. The peak-to-peak value of these ramps is approximately 0.45T/RC and, except for noise and offset errors in the comparator, the correct value of $f(t_1)$ lies within the peak values of V_D. Time constant RC is made sufficiently large to yield an acceptable uncertainty in V_D. If some other value of f(t), say $f(t_2)$, is to be measured, f(t) must be sampled at times t_2, $t_2 + T$, $t_2 + 2T$, ..., etc.

In figure 11, the SVT is employed in a system for characterizing DUT output voltage transitions, including the measurement of ST. The DUT may require a digital input or an analog input (e.g., voltage steps). The delay generator is used to time the strobe pulses, relative to the input signals to the DUT. The delay of the strobe pulses can be made in increments as small as 50 ps. The input voltage range of the comparator is ±3 V, and the RC time constant of the integrator has been set to 0.1 s. This system has been used to characterize the programmable NBS step generator, designed for testing waveform recorders [18]. Figure 12 shows a plot of a -3 V to +3 V transition of the generator, in which sampling delay increments of 0.5 ns were used. It appears that the measurement system is capable of characterizing step-like waveforms as well as yielding the ST to various settling errors: however, it is currently difficult to assign uncertainties to these measurements.

3.4.3 Other Circuits

Figure 13 shows the output from a peak detector, used to measure the ST of a 6 V negative step (+1 V to -5 V) from the NBS step generator. The vertical sensitivity is 0.15%(of 6 V FSR)/cm and the sweep speed is 10 ns/cm. The peak

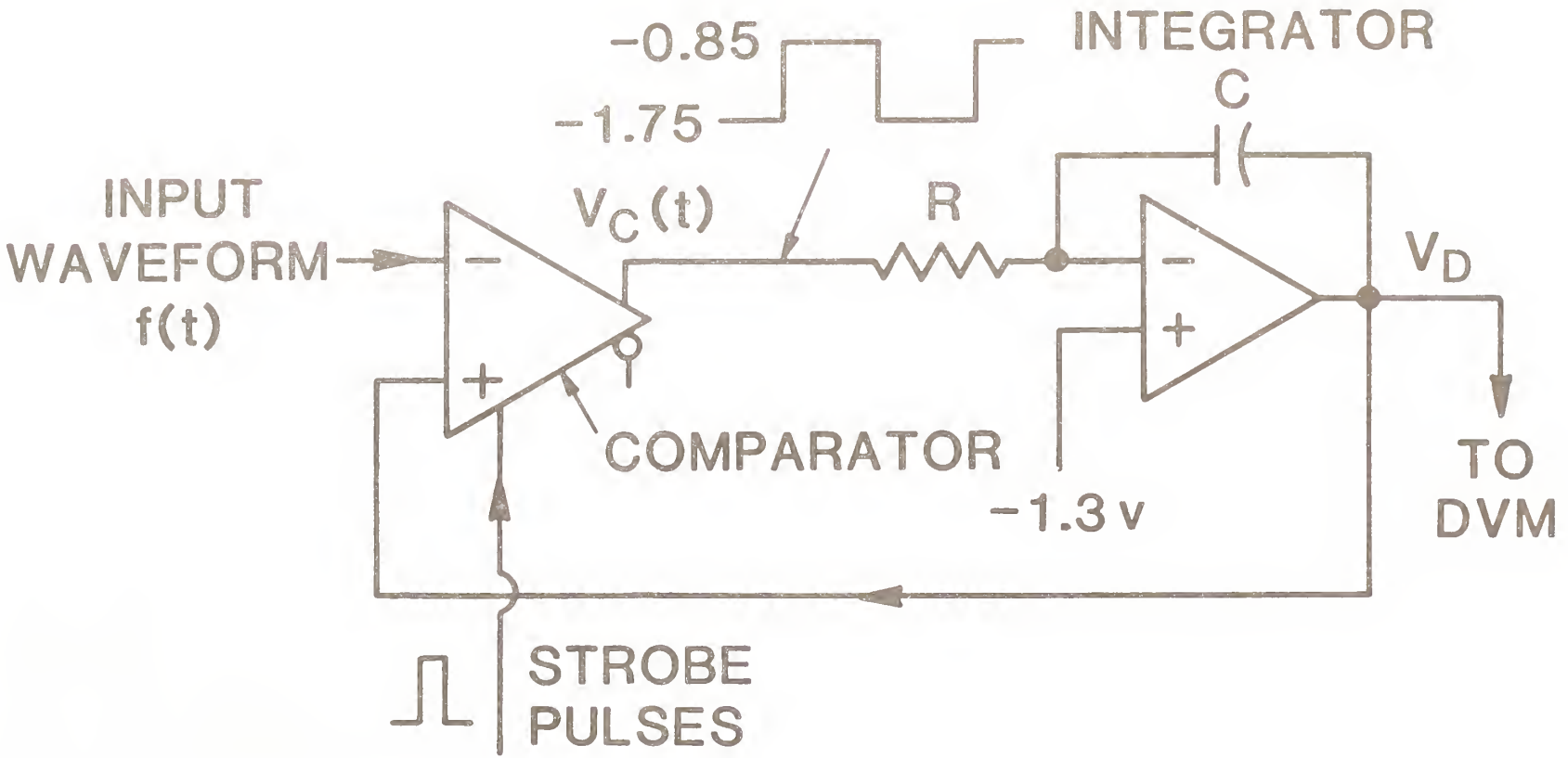


Figure 10. The sampling voltage tracker.

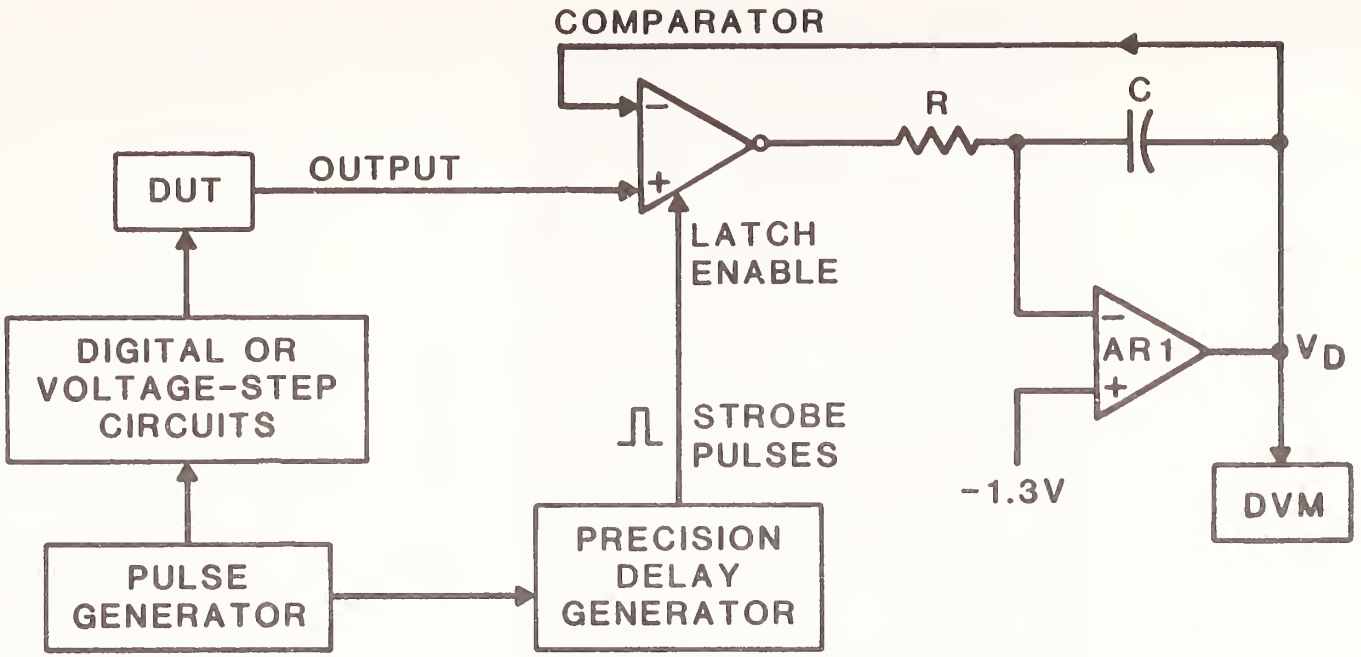


Figure 11. An equivalent time ST-measuring circuit using the sampling voltage tracker. Voltage V_D represents the output voltage from DUT at the time of the trailing edge of strobe (sampling) pulse.

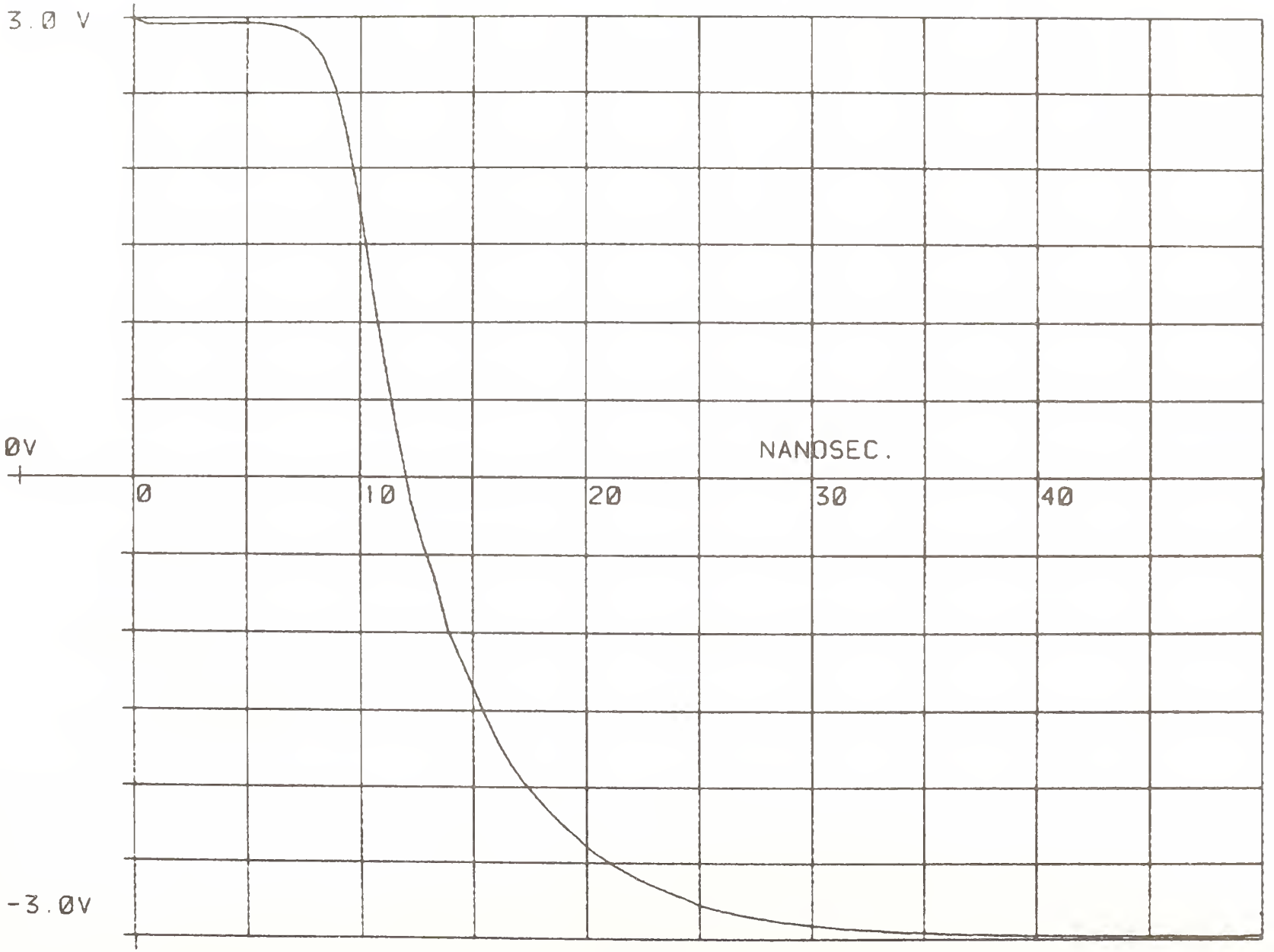


Figure 12. A plot of the -3 V to +3 V transition from the programmable NBS step generator, using the test circuit shown in Fig. 11. The waveform was effectively sampled every 0.5 ns.

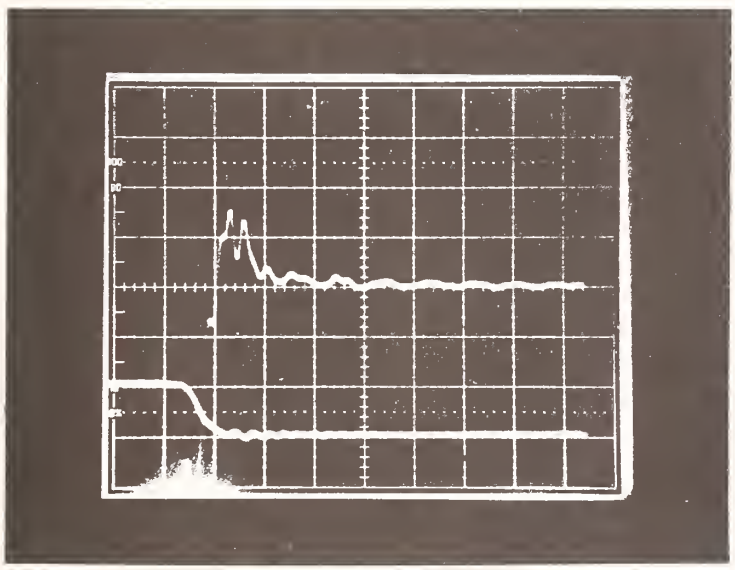


Figure 13. The output from a peak detector, used to measure the ST of a 6 V negative step from NBS step generator. Vertical sensitivity is 0.15%(of 6 V FSR)/cm and the sweep speed is 10 ns/cm. The lower trace indicates start of the voltage step, delayed 4 ns by the scope cable.

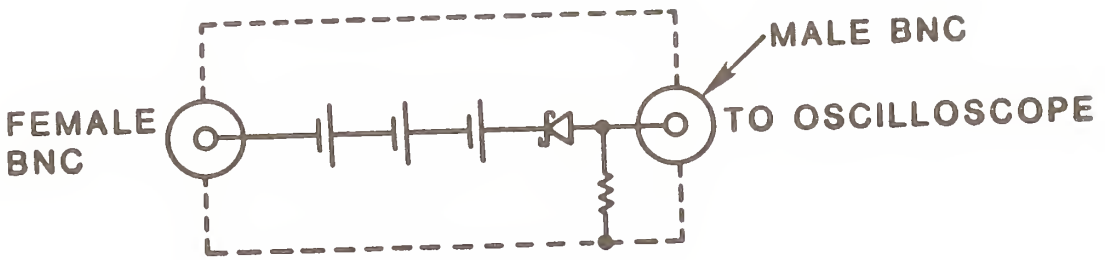


Figure 14. A peak detector using small mercury hearing aid batteries, ~1.5 V each. The voltage detection level is determined by the number of batteries employed.

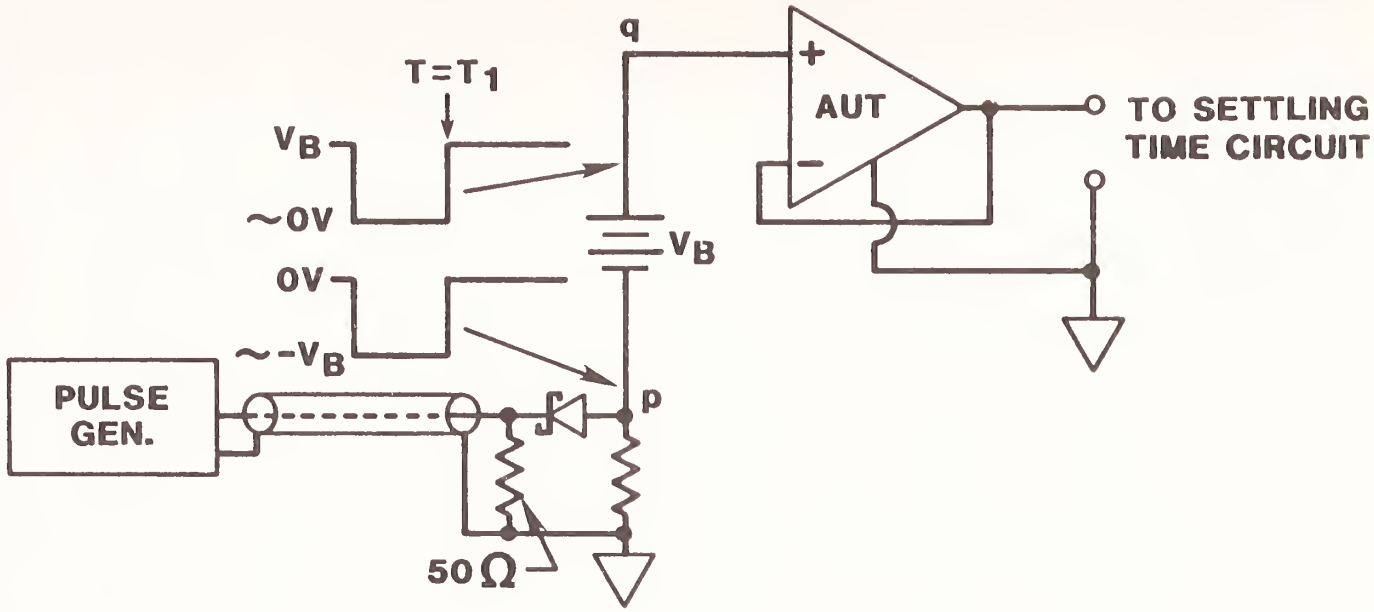


Figure 15. A method of generating positive or negative voltage steps from the waveform produced by a Schottky diode voltage-step (pulse) generator. Small hearing aid batteries are used for V_B.

detector used for this measurement, and those shown in figure 7(b), is illustrated in figure 14. The input voltage level following a transition is adjusted to exceed the sum of the battery voltage and diode forward drop by 50 - 80 mV (typically). Thus, the input voltage level is selectable in increments of ~1.5 V.

Voltage steps up to ±10 V are desirable for testing non-inverting operational amplifiers and many other high input impedance devices. Schottky diode voltage-step generators, mentioned previously, are a means of generating voltage steps with magnitudes up to 10 V; however, these generators produce steps to a final level of 0 V. Hearing aid batteries, packaged as shown in figure 14 (without the diode and resistor) can be used as shown in figure 15 to generate positive or negative voltage steps in increments of ~1.5 V.

4. Conclusion

For many years, settling time measurements have been employed to measure the STs of DACs, operational amplifiers, and certain other devices to within approximately ±0.1% (of FSR) of the final value. More recently, it has been necessary to characterize a much larger part of voltage transitions (than, say, the last 0.1%) from voltage-step generators, so that these devices can be used to test waveform recorders. Sampling oscilloscopes and SVTs have been used for these measurements. Since it is currently difficult to assign uncertainties to the measured transition voltages (V(t)), when dV/dt is greater than about 1000 V/μs, it is expected that efforts will increase to improve the accuracy of these measurements.

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APPENDICES

AN AUTOMATIC AC/DC THERMAL VOLTAGE CONVERTER AND AC VOLTAGE CALIBRATION SYSTEM *

K. J. Lentner, D. R. Flach, and B. A. Bell

Abstract

An automatic ac/dc difference calibration system is described which uses direct measurement of thermoelement emfs. In addition to ac/dc difference testing, the system can be used to measure some important characteristics of thermoelements, as well as to calibrate ac voltage calibrators and precision voltmeters. The system operates over a frequency range from 20 Hz to 100 kHz, covering the voltage range from 0.5 V to 1 kV. For all voltages the total measurement uncertainties expected (including the uncertainty of the specific reference thermal converters used) were 50 parts per million (ppm) at frequencies from 20 Hz to 20 kHz, inclusive, and 100 ppm at higher frequencies up to 100 kHz. The results of initial intercomparisons between the new system and the manual NBS calibration system, using single-range, coaxial-type, thermal voltage converters as transfer standards, are reported. The results show that the agreement between the two systems is better than the uncertainties originally expected, since the intercomparison of ac/dc differences differed by no more than 15 ppm.

Keywords: ac/dc difference; ac voltage measurement; automation; calibration; metrology; thermal voltage converter.

1. Introduction

Until recently, techniques for performing precision ac/dc difference measurements generally made use of manual testing methods which utilize photo-cell preamplifiers and light-beam galvanometers as votage detectors, in conjunction with manually balanced voltage comparators [1,2][1]. Careful attention to the reduction of systematic and random uncertainties in measurement methods, thermoelements (TEs), and thermal voltage converters (TVCs) has resulted in sufficient confidence in test data to allow results to be reported with total uncertainties at the 10-100-ppm level (or better, in special cases) over wide voltage and frequency ranges [3,4]. These manual test methods, however, are very time consuming and subject to errors due to operator fatigue and lack of skill. More recent work [5,6] overcame some of the deficiencies of manual test methods. However, the referenced systems still require the use of a TE voltage comparator which is not available commercially. Because of its special design, the comparator adds to a system's cost and complexity.

Stringent requirements are placed on the measurement system to resolve low-level voltages (about 10 nV), and to overcome the effects of large temperature coefficients and dc reversal differences of the TEs, as well as instabilities of the voltage sources. However, with the advent of stable and

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* Extracted from NBSIR 84-2973, Final Report to the Calibration Coordination Group of the DoD, November, 1984.

accurate analog voltage amplification techniques in combination with digital electronics, digital voltmeters are available with sufficient stability, linearity, resolution, and accuracy to meet the requirements of automated ac/dc difference measurements. Programmable ac and dc voltage sources also are available which lend themselves to adaption for automatic testing. Advances in analog/digital interfaces have improved the ease with which computers can be used to control these instruments.

The system to be described in this report was designed to overcome the deficiencies of present test methods by taking advantage of the technological advances described above. Specifically, some objectives were to: 1) utilize a desktop computer; 2) use commercially available programmable instruments whenever possible; 3) eliminate as much operator intervention as possible in order that testing could be done completely automatically at one fixed voltage range of the test unit; 4) eliminate the additional cost and complexity of using a TE voltage comparator; 5) use test procedures which assure that the test TE's output emf is held as constant as possible; 6) eliminate the effects of operator fatigue and lack of skill; and 7) achieve about the same level of uncertainty as is presently possible for general purpose ac/dc difference manual testing methods.

The system operates over a frequency range from 20 Hz to 100 kHz, covering the voltage range from 0.5 V to 1 kV. For all voltages the goal was to achieve total measurement uncertainties (including the uncertainty of the reference TVCs used) of 50 ppm at frequencies from 20 Hz to 20 kHz, inclusive, and 100 ppm at higher frequencies up to 100 kHz. In addition to performing ac/dc difference tests, the system can be used to calibrate ac voltage calibrators or precision ac voltmeters. Furthermore, as will be discussed later, automatic measurements of a TE's dc reversal difference, response time, and the value of the exponent "n" in the expression relating a TE's heater current and output emf can also be made.

2. Technical Approach

2.1 System Hardware

The new system differs from most present techniques for ac/dc difference measurements in that no TE voltage comparator is used. Eliminating the comparator places additional requirements upon the stability of the system's ac and dc voltage sources, the digital voltmeter (DVM) which measures a TE's output emf, and the switches which select a TE voltage to be measured by the DVM. The hardware development problem of obtaining low-thermal-emf-switches which could be automatically controlled was solved during previous work [5]. Manually operated low-thermal-emf-switches were modified by linking them to solenoids with 24-V operating coils energized by means of programmable relays.

TE voltages of about 10 mV must be measured to within about 10 nV to achieve 1-ppm comparison precision, and the DVM used to measure these voltages has the resolution necessary to make such a voltage measurement when extensive averaging of data is used. The DVM has an input resistance of about 10 GΩ, a 60-Hz common mode voltage rejection >40 dB, and a dc common mode voltage rejection >150 dB. On its most sensitive range (10-mV), the peak-to-peak low-frequency noise (dc to about 10 Hz) of the DVM, with its input shorted, was measured to be about 50 nV.

The dc voltage source has 10-V, 100-V, and 1-kV ranges with six-digit voltage setting capability on each range. Its specified accuracy is 50 ppm of setting to 10-V, and 100 ppm above 10-V. The ac voltage source also has six-digit voltage setting capability for voltage ranges of 1-V, 10-V, 100-V, and 1-kV, with specified accuracies in the range of about 0.02 percent to 0.1 percent, depending on the voltage and frequency ranges. Some typical results of stability tests made on these sources will be discussed later.

A block diagram of the system is given in Fig. 1, and an overall view of the system hardware shown in Fig. 2. The desk-top computer serves as the system controller and has about 60 kbytes of user-available memory. Magnetic tape cartridges are used for program and data storage. A video display terminal (CRT) is used for data display during testing and also serves as an aid during software development. Since the computer only has three input/output slots, an I/O expander is needed to accomodate the required instrumentation. The real-time clock is used for precise control of the time interval between applications of ac or dc voltages during a test, and the printer and plotter provide test records.

As indicated in Fig. 1, communication between the computer and the stimulus and measurement instrumentation is via the IEEE 488 bus. The digital panel meters (DPMs) monitor the voltage outputs from the dc and ac sources. During testing, readings of both the dc and ac source's output voltages are obtained by the DPMs. These voltage readings are made before the voltages are applied to the test circuit. If the measured voltages differ by more than 0.5 percent from the programmed values, the test is automatically aborted. High accuracy in these voltage readings is not necessary, since TVCs can readily withstand an applied voltage which is 120 percent of rated value. For the ac source, the output voltage is attenuated by a factor of 100 before being connected to the DPM. The attenuation is necessary in order to overcome the voltage-frequency product limitation of the DPM. The counter shown in Fig. 1 monitors the frequency of the ac source. If the counter reading differs by more than about 10 percent from the programmed frequency, the test is automatically aborted. The relay actuator is used to apply 24-V dc to the operating coils of the high-voltage relays as well as to the coils of the solenoids which operate the low-thermal-emf switches.[1] These switches select the output voltage of the standard TE (E_s) or the unit-under-test TE (E_t). The voltages, E_s and E_t, are applied directly to the input of the DVM, and the DVM voltage readings are then stored in the computer's memory for later processing.

2.2 AC/DC Difference Test Procedure

One of the advantages of using a TE voltage comparator is that, since small differences in the ratio of two TE emfs are measured directly, the output emf of the test TE can be allowed to drift slightly from its reference emf value when ac, +dc, or -dc voltages are applied [2,6]. In this new system, since no TE voltage comparator is used, the requirement for holding the test TE's emf constant is quite stringent. However, with automation and the rapid response time of the voltage sources (typically 50 μs

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[1] Construction details of the high-voltage relay and low-thermal-emf modules can be found in [7].

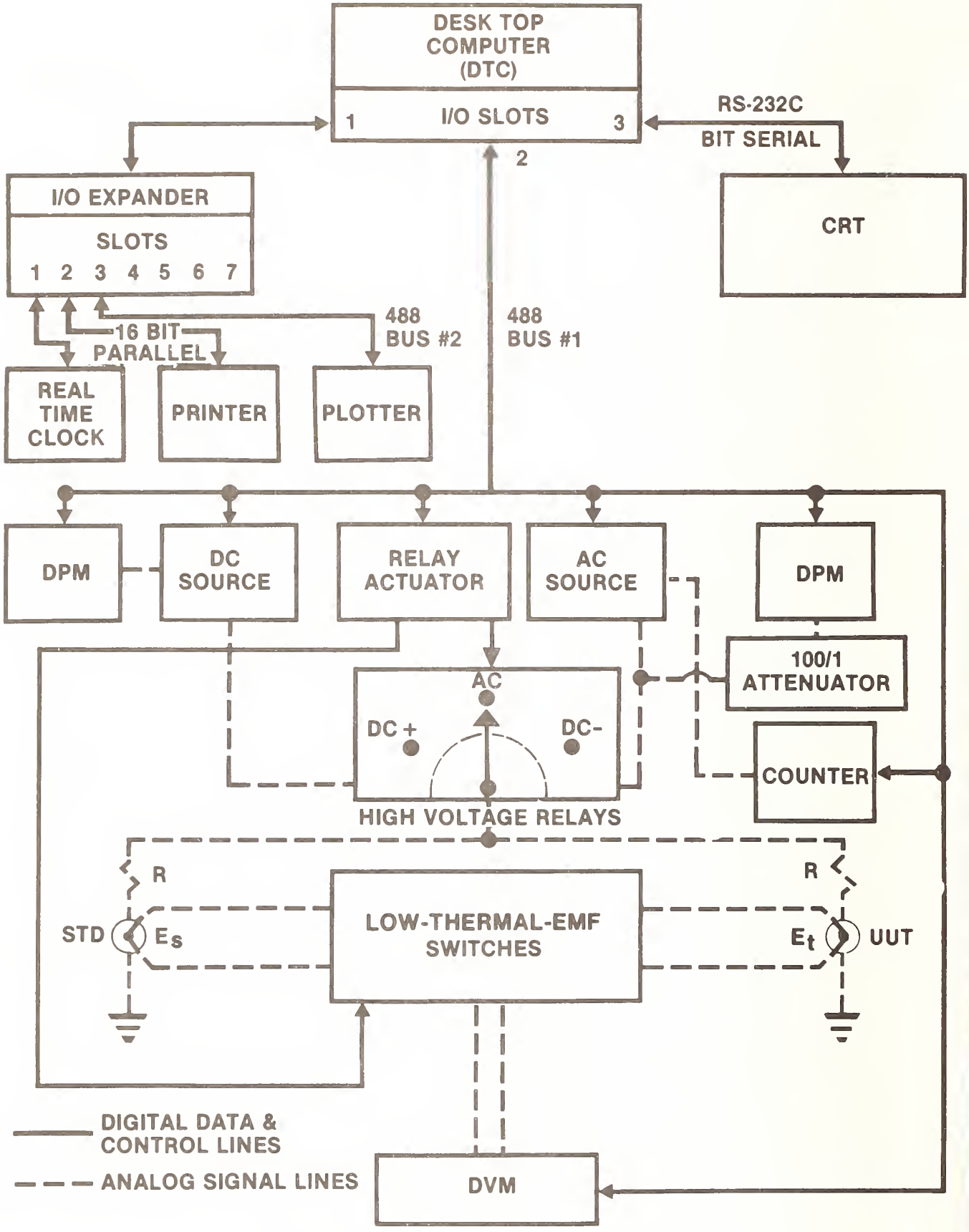

Figure 1. System block diagram

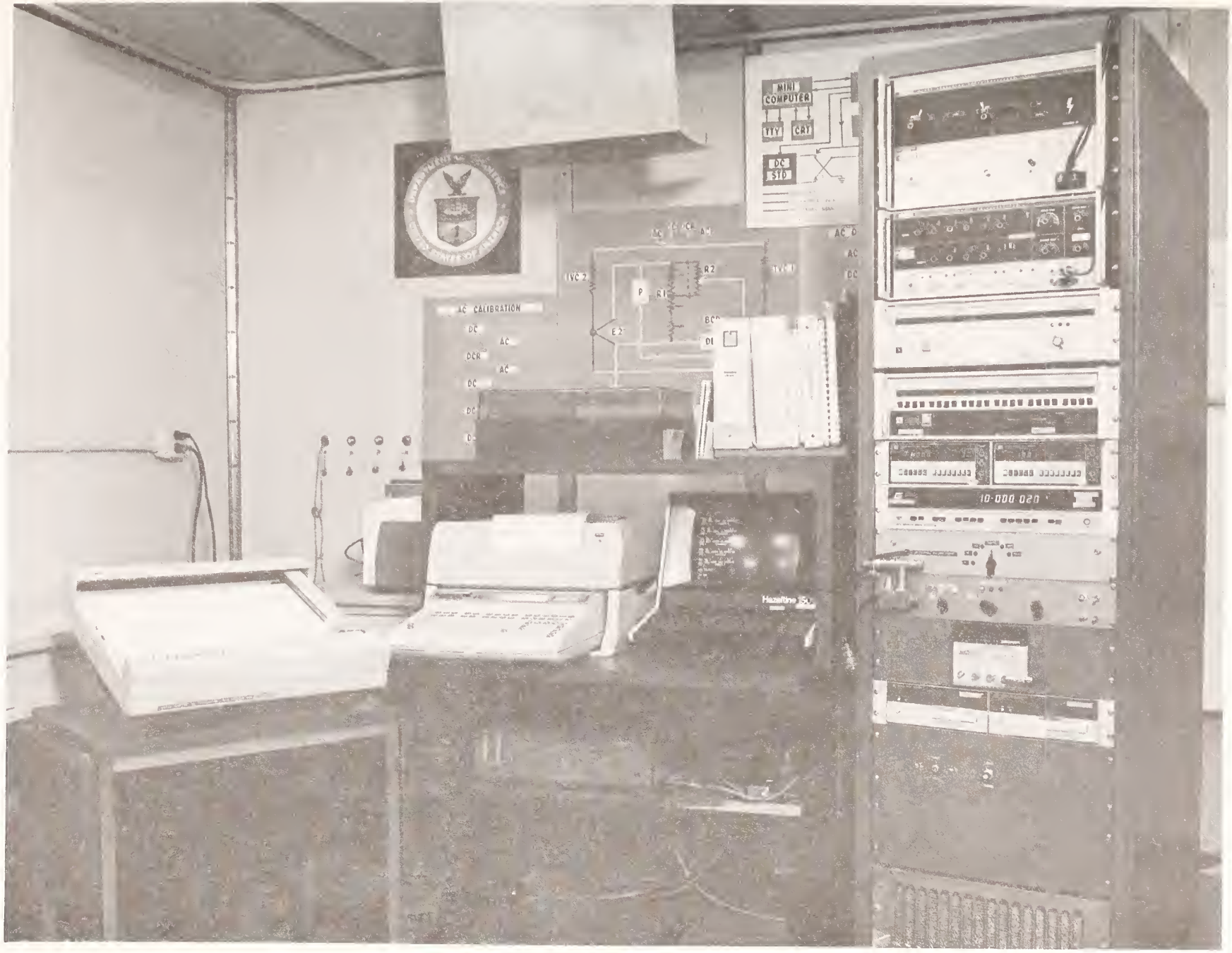

Figure 2. Automatic TVC and AC voltage calibration system.

for the dc source and a few milliseconds for small voltage changes for the ac source), the constant output requirement can be readily satisfied. The techniques used will be discussed in this section.

For a TVC with response defined by $E = KV^n$, where E is the output emf of the TE in the TVC, V is the voltage applied, and K and n are parameters characteristic of the particular TVC, the ac/dc difference is defined as

$$\delta = \frac{V_a - V_d}{V_d} , \tag{1}$$

where V_a is the applied ac voltage, and V_d is the average of the two polarities of dc voltage; i.e.,

$$V_d = \frac{V_+ + V_-}{2} . \tag{2}$$

V_a, V_+, and V_- are voltage values which give the same output emf of the TE. In a manual test system using a TE voltage comparator, the voltage difference, $V_a - V_d$, is determined by a second TVC, the standard. If the standard's response is defined as

$$E_s = K_s V_s^{n_s} , \tag{3}$$

it can be shown [2] that the ac/dc difference of the test TVC is

$$\delta_t = \frac{E_{sa} - E_{sd}}{n_s E_{sd}} + \delta_s = \frac{\Delta E_s}{n_s E_{sd}} + \delta_s , \tag{4}$$

where E_{sa} is the standard TE's emf when the voltage V_a is applied, E_{sd} is the standard TE's average emf when voltages V_+ and V_- are applied (cf. eq. 2), n_s is the standard's dimensionless characteristic n, and δ_s is the ac/dc difference (in ppm) of the standard determined as described in [1,2]. Equation 4 is numerically correct if dE_s is in nanovolts, E_{sd} in millivolts, and the "δ's" are im ppm. During a test, V_a, V_+, V_-, and V_a are adjusted until the same emf of the test TVC is obtained in each case when these voltages are applied in sequence.

In the automated system the test TVC's output emf is held constant in the following manner. With the nominal dc voltage applied to the test TVC, an output emf, E_{set}, is measured which is called the "set-point" voltage. In all subsequent applications of ac and dc voltages to the test circuit of

Fig. 1 the computer is used to adjust the voltage applied so that the test TVC has an output very nearly equal to E_{set}. A four-step procedure is used for making ac/dc difference measurements. The procedure consists of applying a sequence of ac, +dc, -dc, and ac voltages to both TVC's at approximately equal time intervals. The following operations are performed for each step in the procedure presently used with the system.

First, the nominal ac or dc voltage is applied, the test emf, E_t, is measured, and a difference voltage, dE_t, is calculated as

$$dE_t = E_{set} - E_t \ . \tag{5}$$

If the difference voltage is not sufficiently small, as discussed below, a voltage correction, dV_t, is calculated from

$$dE_t/n_t E_t = dV_t/V_t \ . \tag{6}$$

Hence,

$$dV_t = (dE_t/n_t E_t)V_t \ . \tag{7}$$

The correction, dV_t, is added to the nominal voltage, V_n, and a "reset" voltage, $V_r = V_n + dV_t$, is applied. The test emf, E_t, is measured again, and a second voltage correction, dV_2, is calculated using equations 5 and 7. The output emf of the standard TE, E_s, is now measured. A correction for the emf of the standard TE, dE_s, is calculated, using dV_2 to compensate for any deviation of the actual emf of the test TE from the set point E_{set}; i.e.,

$$dE_s = (n_s E_s dV_2)/V_r \ . \tag{8}$$

The corrected emf for the standard TE is then

$$E_{s1} = E_s + dE_s \ . \tag{9}$$

A discussion of the exact measurement procedure used is given below.

After completing the sequence of four steps by applying successively ac, +dc, -dc, and ac voltages, the ac/dc difference of the test TVC, δ_t, is calculated as

$$\delta_t = \frac{E_a - E_d}{n_s E_{sd}} + \delta_s, \tag{10}$$

where E_a is the average of the standard's corrected emfs determined for the two applications of ac voltage; E_{sd}, n_s, and δ_s are as defined in equation 4; and E_d is

$$E_d = \frac{E_{s1+} + E_{s1-}}{2}, \tag{11}$$

where E_{s1+} is the corrected emf calculated as in equation 9 when +dc is applied, and E_{s1-} is the corrected emf when -dc is applied.

In the computations previously discussed, account is taken of the finite resolution of the ac and dc voltage sources. The voltage setting remains unchanged if the output emf of the test TVC is close enough to the set-point voltage (E_{set}) that a least-significant-digit change in the voltage in the voltage source's output will provide no decrease in the magnitude of the calculated difference, dE_t.

A test run consists of four determinations of ac/dc difference and the average of the four determinations is calculated and printed on the system's printer. In general, three runs are normally made at each test voltage and frequency.

In order to increase the reliability of the emf measurements made by the DVM, and, therefore the reliability of the results, a unique measurment procedure is used. The procedure is necessary to compensate for instabilities in the ac or dc voltage sources or linear drifts in the standard or test TVCs. After the dc reset voltage V_r has been applied to the test TVC, five readings of its emf are obtained as illustrated in Fig. 3. The standard's average emf is obtained next by taking ten readings of its TE emf. If the standard deviation of an observation of the ten readings is > 300 nV, (300 nV = 17 ppm for a 10 mV TE emf with n = 1.8) the first reading is discarded and an eleventh reading is taken. The average of readings two through eleven is calculated and the standard deviation test limit again applied. The process continues until the average of any ten consecutive readings passes the standard deviation limit test. Up to ten attempts are made to obtain an average emf value with a standard deviation of an observation $\leq$ 300 nV. The test is aborted if the tenth attempt is unsuccessful.

When the ten reading average of the standard's emf is within the standard deviation test limit, five readings of the test TVC's emf are again obtained. As illustrated in Fig. 3, the average test TVC's emf is calculated as

$$E_t = \frac{E_{t1} + E_{t2}}{2} \quad . \tag{12}$$

where E_{t1} is the average of the first of the five test emfs, and E_{t2} is the average of the second of the five test emfs. The value of E_t obtained from equation 12 is used to calculate dE_s using equations 5, 7, and 8.

As the preceding equations show, the values of the exponent n for both the test and standard TVCs must be known. The exponent varies with applied voltage, and its variation can be determined by doing "n-tests." These tests will be discussed in the next section. For the standard TEs, the coefficents in the equation expressing the value of n as a function of output emf are stored in a data file in the system software. Once the operator has specified which standard TE is being used, the standard TE's output emf is measured with a +dc voltage applied, and the value of n_s is automatically computed. The values of the test TE's coefficients for n must be manually typed into the computer at the beginning of a test. To guard against mistakes in entering data, the computed values of n for the test TE must be within the limits 1.4 to 2.1.

An additional safeguard is contained in the ac/dc difference program to avoid application of voltages great enough to damage the TEs. When the reset voltage, V_r, is calculated, its value must be less than 120 percent of the rated voltage of the TVC. If the calculated reset voltage is outside this limit, the program aborts.

2.3 Other System Capabilities

2.3.1 AC Voltage Calibrations

As mentioned above, the system can readily be used to calibrate ac voltage calibrators using TVCs with known ac/dc differences. The output voltage of the test calibrator replaces the output voltage of the system's ac source, and the test calibrator's correction can be determined in terms of a calibrated dc source and the known ac/dc differences of the standard voltage converters used.

The correction to the test calibrator (in ppm) is

$$C_t = \frac{E_a - E_d}{nE_d} + \delta_s + C_{dc} \ , \tag{13}$$

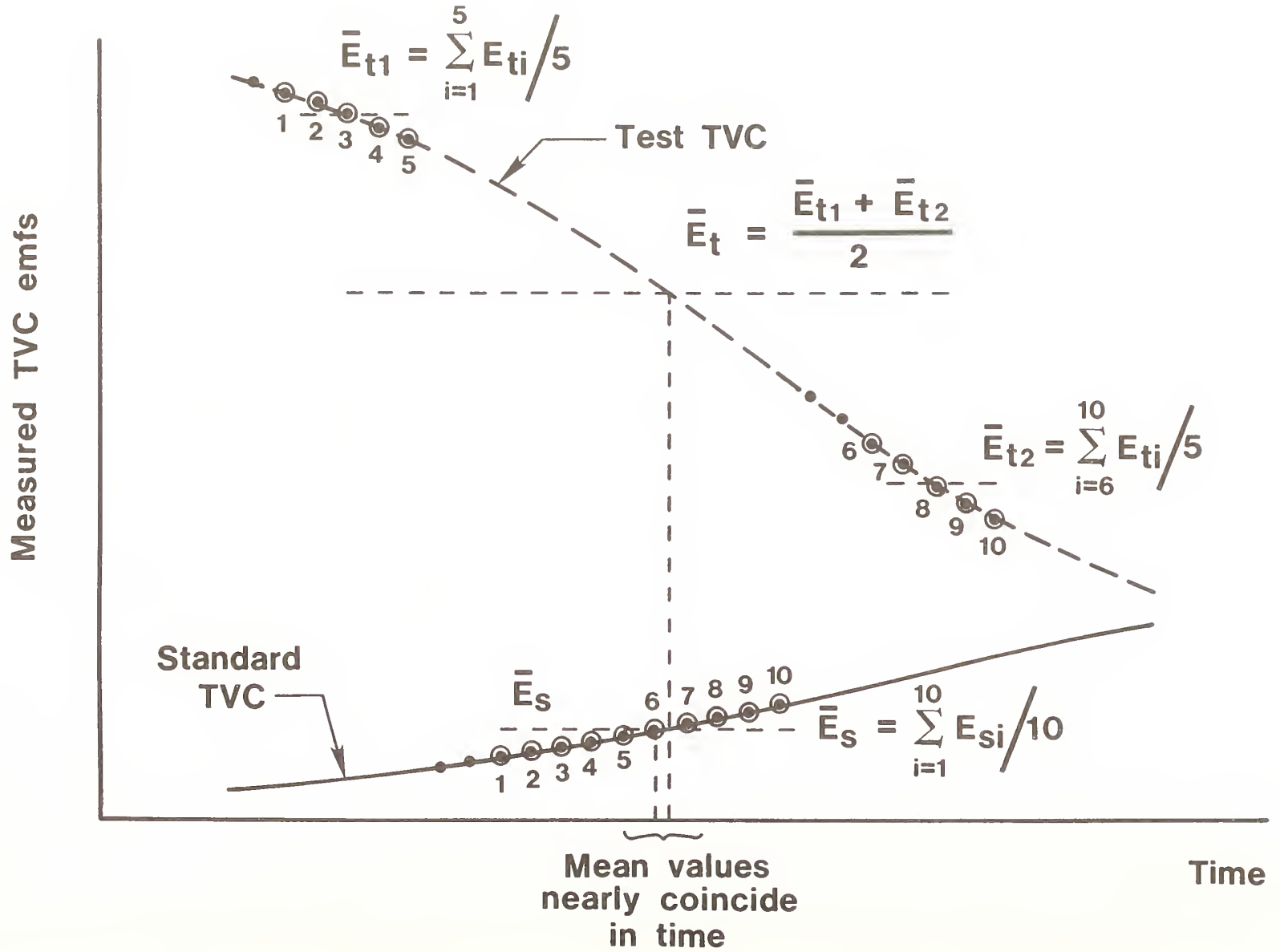

Figure 3. Present measurement procedure for obtaining average values of TVC emfs that compensates for drifts and obtains nearly simultaneous values for the mean values.

where E_a is the average of the measured emfs of the TVC with ac voltage applied, E_d is the average emf with direct voltage of both polarities applied, n_s is as previously defined, δ_s is the correction (in ppm) to the standard, and C_{dc} is the correction (in ppm) to the dc voltage source's nominal output obtained from calibration data. As in the case of ac/dc difference tests, the correction is in ppm if E_a-E_d is in nanovolts and E_d in millivolts. A simplified block diagram of the system connected for such an application is shown in Fig. 4.

For ac calibrations a program called ACCAL is used (see Table 4, Appendix B). As illustrated in Fig. 4, only one TVC is required and, as for ac/dc difference tests, the ten reading sequence of the TE's output emf is used (cf. $\overline{E}_s$ of Fig. 3). However, a different sequence of applying voltages to the TVC is used. The voltages are applied successively as ac_1, +dc, ac_2, -dc, and ac_3. The standard TVC's n coefficient is calculated using the TE average output emfs measured with +dc and -dc applied. A first correction, δ_1, is then calculated using

$$C_1 = \frac{\frac{(E_{a1} + E_{a2})}{2} - E_{d+}}{nE_d} , \qquad (14)$$

where $E_d = \frac{E_{d+} + E_{d-}}{2}$, and the other terms are as defined above. A second correction is computed as

$$C_2 = \frac{\frac{(E_{a2} + E_{a3})}{2} - E_{d-}}{nE_d} , \qquad (15)$$

and finally, the first average correction, C_{t1}, is computed as

$$C_{t1} = \frac{C_1 + C_2}{2} . \qquad (16)$$

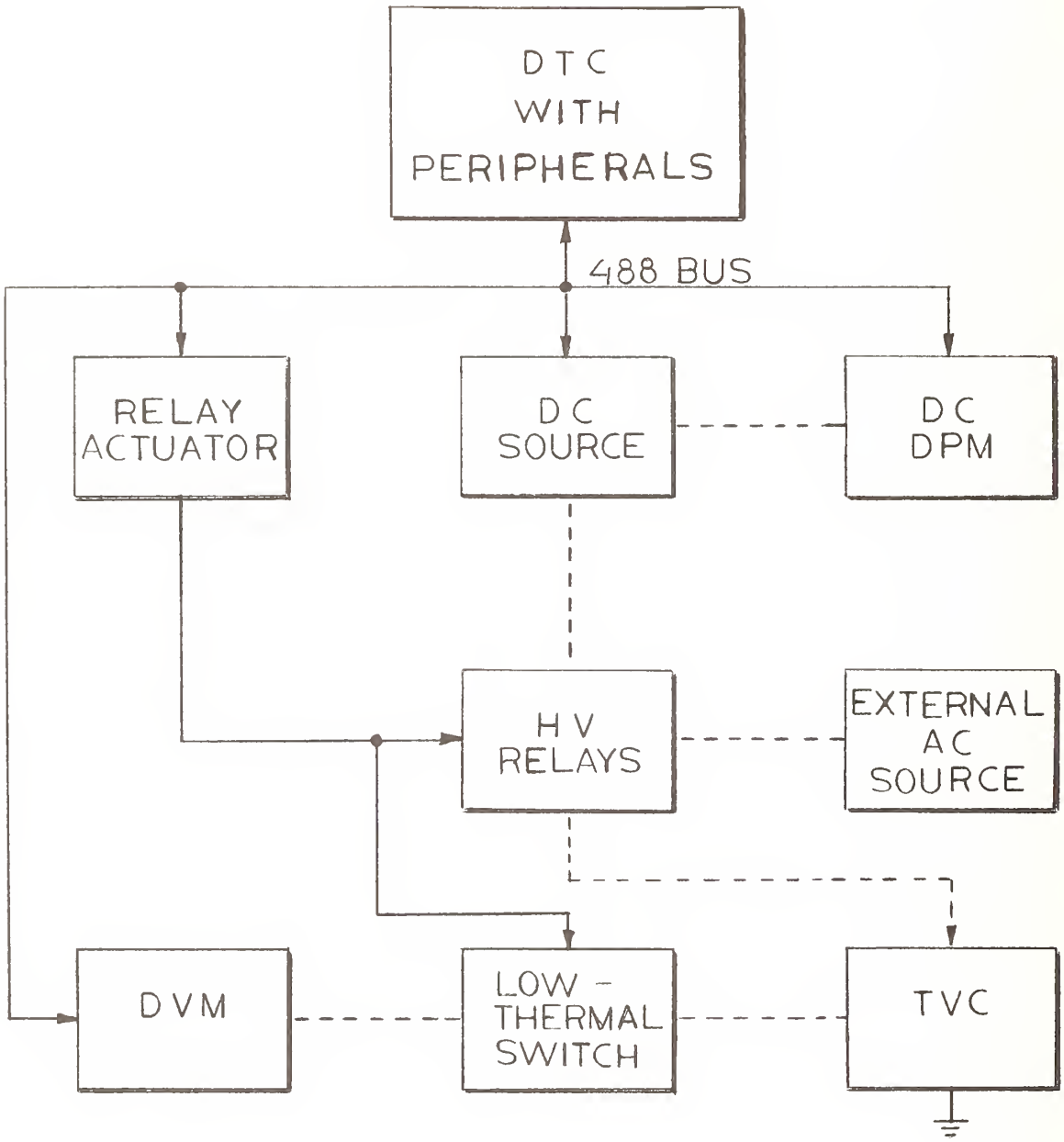

Figure 4. Block diagram of system when used to calibrate an external ac source.

As for ac/dc difference tests, four determinations constitute a test run. The average correction C_t of equation 13 is computed as

$$C_t = (C_{t1} + C_{t2} + C_{t3} + C_{t4})/4 + \delta_s + C_{dc} \quad . \tag{17}$$

This measurement technique is very useful also for calibrating precision ac DVM's. Since a correction, say C_{t1}, has just been determined for the ac source, the correct ac voltage applied to the standard TVC has just been determined. With a DVM connected at the input of the TVC, the DVM's reading can be recorded, and using the correction C_{t1}, a correction for the test DVM can then be determined.

2.3.2 Stability Tests

To control the variability in the test data, it is important to make sure that the voltage sources are quite stable. Thus, a progam called STABLE was written which uses the system's DVM to measure the stability of the voltage sources with time. Figure 5 illustrates typical stability test data for the dc source. At a nominal setting of 10 V, 20 voltage readings were taken over a time interval of about 20 minutes. The deviation of the measured voltage (in ppm) from the nominal voltage is defined as

$$\frac{\Delta V}{V} = \frac{V_1 - V_2}{V_2} \times 10^6 \quad , \tag{18}$$

where V_1 is the measured value, and V_2 is the nominal value. The maximum deviation measured was 1.3 ppm and the mean deviation was 0.6 ppm. The standard deviation of an observation was 0.5 ppm, and the 3σ limits for the mean were ± 0.3 ppm. The results indicate that the dc source has acceptable stability and is well within its specified accuracy of 50 ppm.

Typical results for a test of the ac source's stability are also shown in Fig. 5. Again, 20 readings were obtained during a 20-minute time interval. The test voltage was 10 V at a frequency of 20 kHz. Here the range of deviations was 40 ppm with the mean being 19 ppm. The standard deviation of an observation was 9 ppm, and the 3σ limits for the mean were ± 6 ppm. The discrete 10-ppm steps in the plotted data are due to the fact that the system DVM's resolution on its 10-V range is limited to 10 ppm.

2.3.3 TE Tests

As mentioned in the previous section, one important test that is readily performed automatically is that of determining a TE's "n" characteristic. Typical results for a 2.5-mA, VHF-type TE which was tested with a nominal 3-V range resistor are illustrated in Fig. 6.

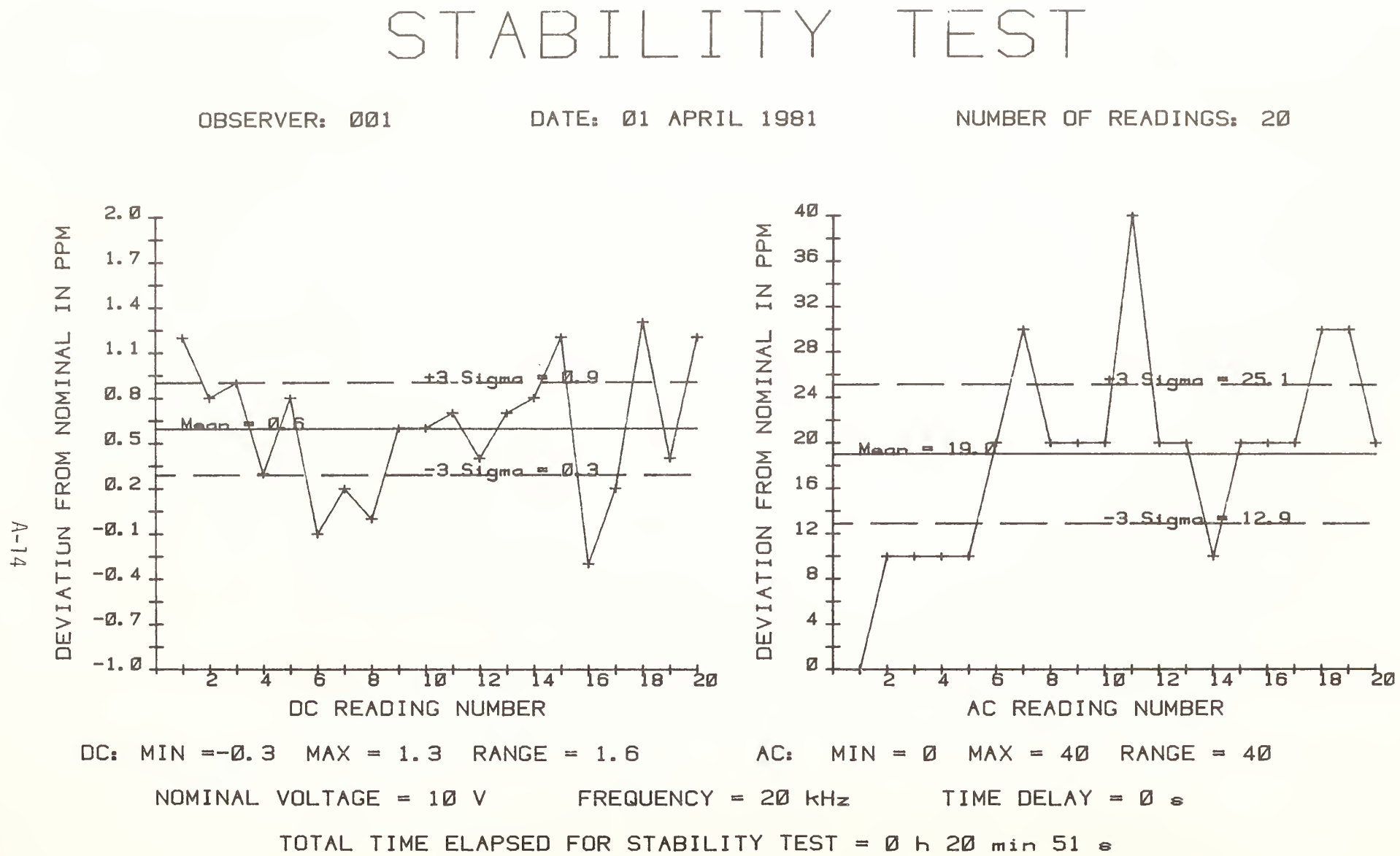

Figure 5. Plots from stability testing program.

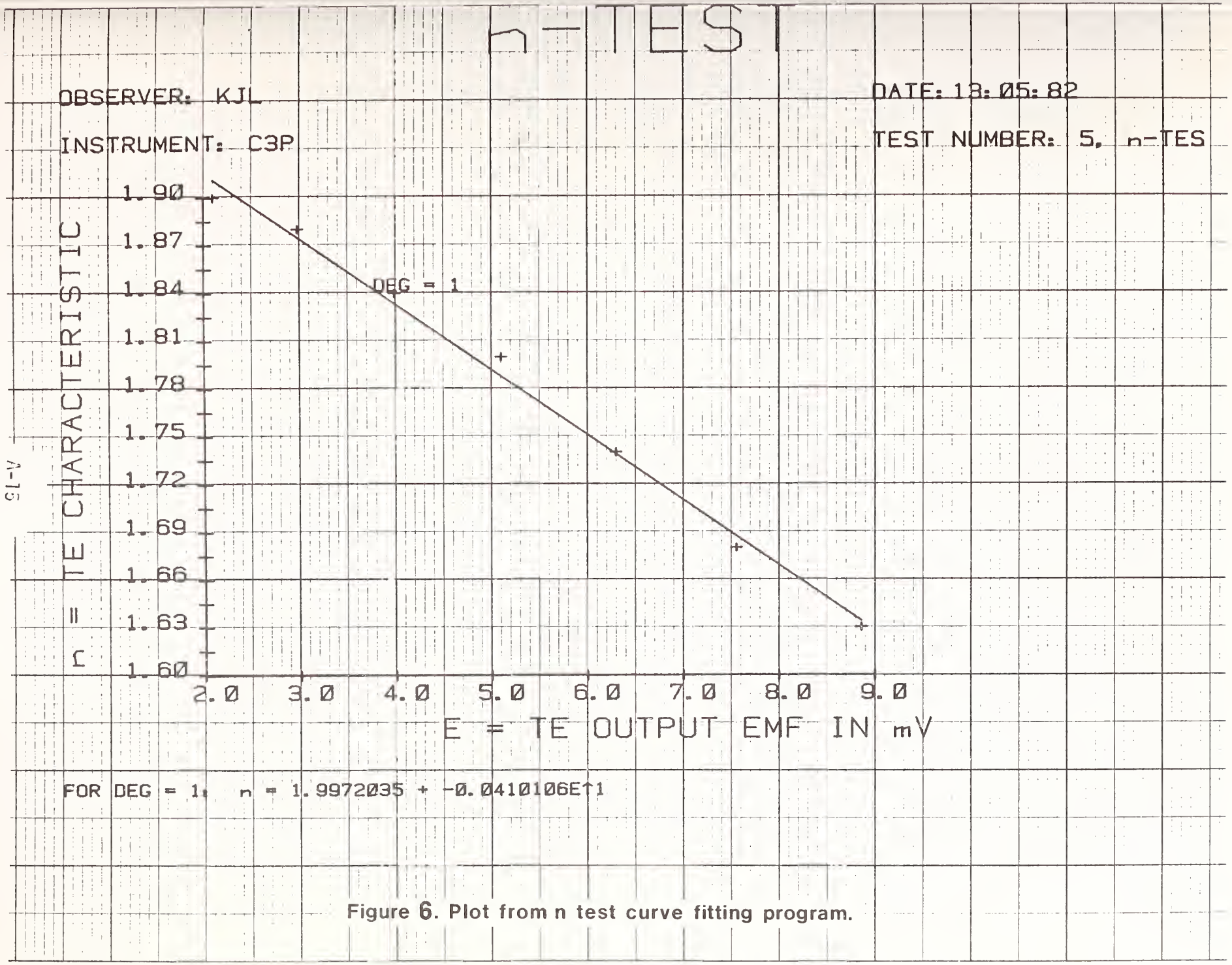

Figure 6. Plot from n test curve fitting program.

The characteristic n is defined by

$$n = \frac{\Delta E/E}{\Delta V/V} , \qquad (19)$$

where ΔE is the measured change in output emf for small changes in applied voltage ΔV, V is the nominal test voltage for the TVC, and E is the measured emf at the nominal test voltage. ΔV is programmed to be ± 0.5 percent of nominal test voltage V. Sufficient time is allowed after each voltage change for the TE to reach its final emf value.

For the results shown in Fig. 6, the TVC was tested from 50 to 110 percent of rated voltage. The total elapsed time to obtain the seven data points was about 1.25 hours.

Each value of n is computed as the average of four determinations at any given voltage. A least-squares analysis of the data provides the option of obtaining a fitted curve using up to a fourth-degree polynomial. An analysis of variance table and residual standard deviation are computed and printed so that the "goodness-of-fit" of the computed equation for n as a function of TE output emf can be determined. The printed data sheet also shows the values of n(measured) - n(computed). The figure shows an example of a linear fit which, in most cases, provides sufficient accuracy. The coefficients 2.00 and -0.04 are either stored in the computer's data file (for a standard TE) or are typed by the operator into the computer program for the TE under test at the beginning of an ac/dc difference test.

The dc reversal difference (DCRD) of a TE can also be readily determined. DCRD is defined as the difference in applied values of both polarities of dc voltage required to produce an equal output emf (or "constant output") of the test TE [7]. In order to facilitate DCRD measurements, "constant input" emf, α, is actually measured. This α is related to the DCRD by a factor of 1/n as

$$DCRD = (1/n)(\alpha) = (1/n)\ \frac{E_+ - E_-}{(E_+ + E_-)/2} , \qquad (20)$$

where E_+ and E_- are the TE output emfs with equal +dc and -dc (or "constant input") voltages applied, and n is as previously defined.

During acceptance tests of some TEs, the data showed much greater variation of DCRD from unit to unit than had been expected. The only information available indicated that the DCRD should reach a maximum value between 70 and 80 percent of rated heater current and should approach a zero value close to 100 percent of rated current. The results obtained did not

substantiate this information. Hence, a program was written to determine the DCRD as a function of applied voltage. Typical results for a 5-mA, UHF-type TE tested with a 60-V range resistor are shown in Fig. 7. In this test the voltage was varied from 50 to 120 percent of its rated value in 2-percent increments. It should be noted that the plotted data show α; hence, the DCRD values referred to a constant output emf would be smaller by the factor of n (see equation 15). In this test, the maximum α was about 700 ppm at 58 percent of rated voltage, and the minimum was about -330 ppm at 120 percent of rated voltage.

At the time the DCRD testing program was developed, the information on DCRD variation was limited. However, in the intervening time Inglis [9] has published a substantial amount of information in this area. Investigations at NBS have not been as extensive as those of Inglis, but, in general, the results obtained are in agreement with his published data.

The response time of a TE is also a characteristic which can readily be measured using the automatic system. Response time is obtained by making measurements of a TE's emf when full rated voltage is suddenly applied to the TE. The calculated response time, t, is the time taken for the output emf to reach 1 - (1/e) of its final value. Typical results for a 2.5-mA, VHF-type TE are shown in Fig. 8.

For the interested reader, detailed documentation is available upon request for most of the automatic test programs which are described in this report.

3. Measurement Results and Uncertainties

Manual calibration systems have been in operation for many years at NBS, and their uncertainties have been documented [1-3]. DC reversal difference, self-heating and ambient temperature effects, drift effects due to nonequal time intervals between emf measurements, unbalanced lead impedances, induced voltages from electromagnetic fields, and operator fatigue and lack of skill are some of the more common sources of error. The process of determining an estimated total uncertainty for a system is based upon 1) a history of measurement results, 2) careful measurements of standards with accurately known corrections, 3) theoretical analysis of sources of errors, along with, preferably, 4) intercomparison tests using two independent test methods [3]. A combination of processes 2 and 4 was used for the initial evaluation of the present automated system. The primary emphasis was placed on comparison of results obtained with a well-characterized manual system and those obtained with the new system.

A single-range (3-V), coaxial-type TVC was tested using established manual techniques, followed by tests on the automated system. The results obtained from the two test systems are shown in Table 1.

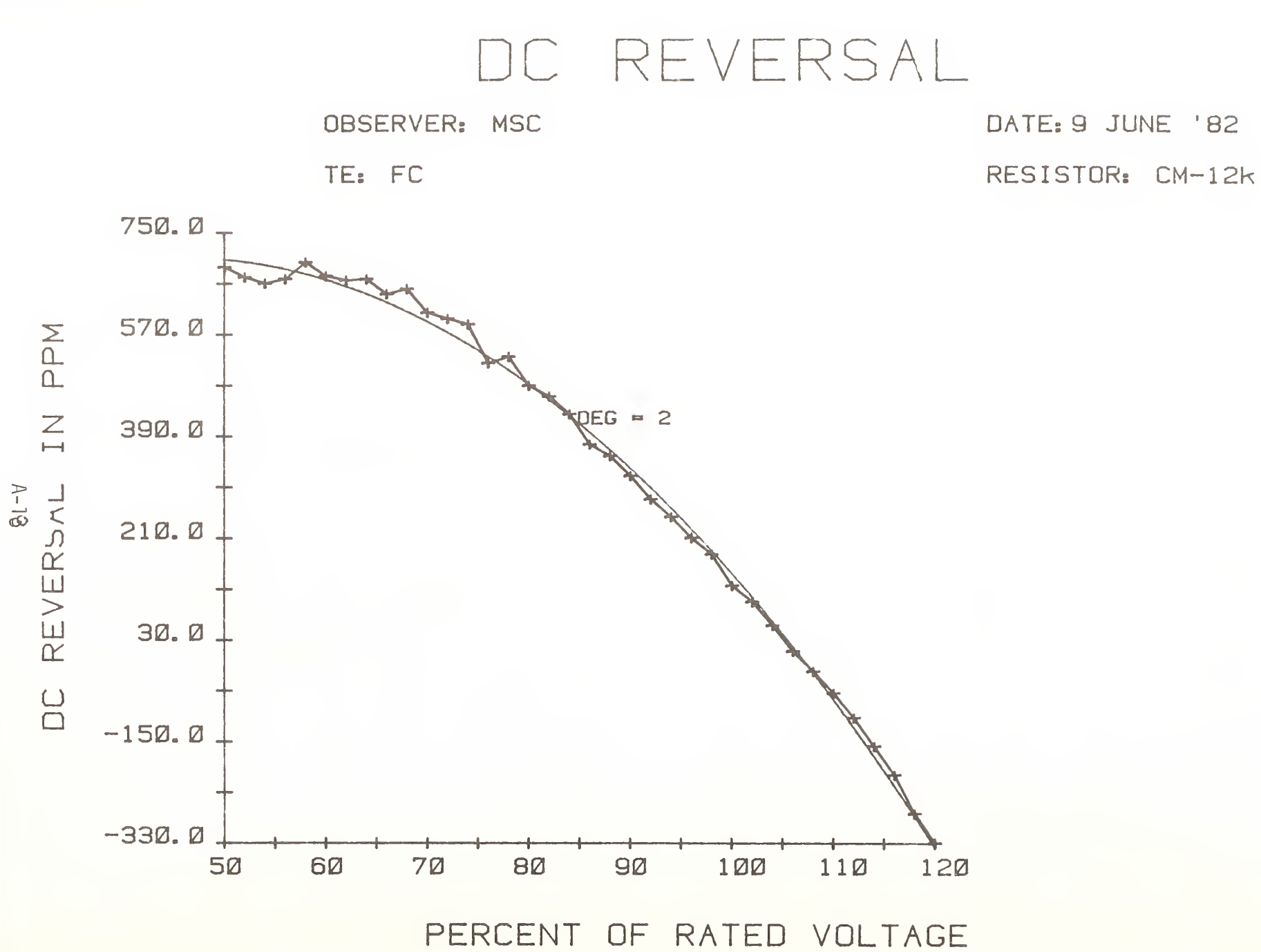

Figure 7. Plot from dc reversal difference program.

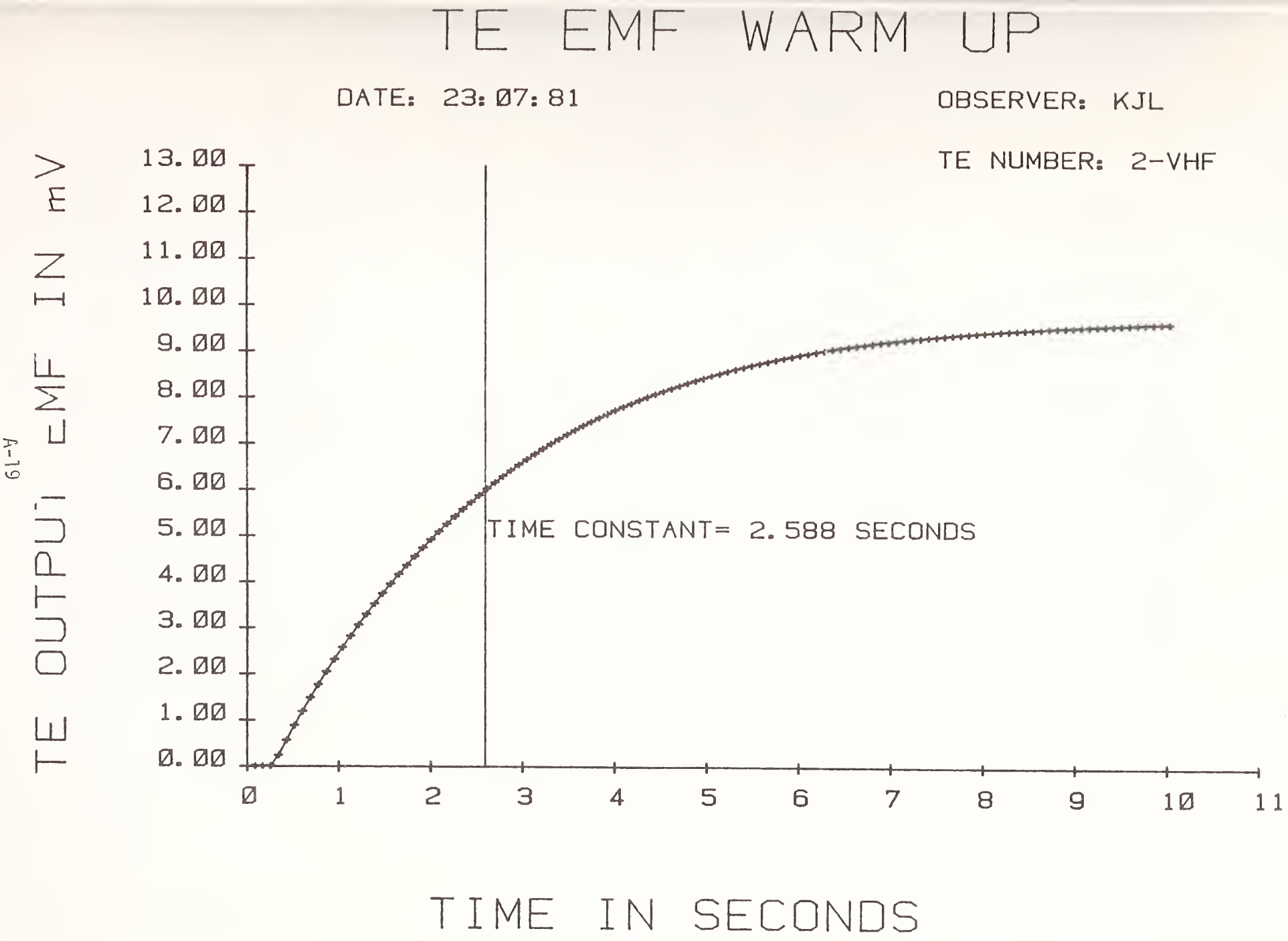

Figure 8. Plot from TE thermal response time program.

TABLE 1

3-V TVC AC/DC DIFFERENCE (ppm)

Frequency kHz	Manual	Automatic	Difference
0.02	0	2	-2
20	1	-9	10
50	-1	-9	8
100	-1	-4	3

For the automatic system, the values reported are the average of 12 determinations of the transfer standard's ac/dc difference. The random uncertainty was calculated as three times the standard deviation of the mean of the 12 observations, with the result that 3σ = 21 ppm for the worst case. For the manual system, three times the standard deviation of a comparison of two TVCs, plus an allowance for systematic errors in the comparison process, ranges from 6 ppm at 1 kHz to 12 ppm at 100 kHz [10]. In each case the differences between the results obtained with the two test methods is less than the combined uncertainties for a comparison of the same TVCs by the two methods.

A second test was made using a 10-V range TVC as a transfer standard. The test results are listed in Table 2.

TABLE 2

10-V TVC AC/DC DIFFERENCE (ppm)

Frequency kHz	Manual	Automatic	Difference
20	-4	-17	13
50	-3	-7	4
100	-1	6	-7

Both the 3-V and 10-V TVC transfer standards had small ac/dc differences. Therefore, a third intercomparison test was conducted using a transfer standard with large, but accurately known differences. The results of this test are listed in Table 3.

TABLE 3

50-V TVC AC/DC DIFFERENCE (ppm)

Frequency kHz	Manual	Automatic	Difference
5	29	26	3
10	56	52	4
20	121	121	0
50	320	310	10

The test results summarized in the three tables suggest a possible systematic uncertainty since the automatic system gave lower values for all but three test frequencies. Further investigation is required to evaluate whether or not this uncertainty is significant.

As was mentioned previously, the results reported are initial intercomparison tests. Neither sufficient tests were run nor data obtained to come to any definite conclusions regarding the systematic or random uncertainties of the automatic test system. However, since the difference of the ac/dc difference measurements for the three voltage converters tested did not exceed ±15 ppm, it appears that the new system should be able to achieve total uncertainties much less than had originally been anticipated. Further testing will be done to verify this hypothesis. Such testing will include a "build-up" process from a reference voltage of 10 volts to about 200 V at various frequencies. Also, a "step-down" testing process from the 10 V level to about 2 V will be performed.

In order to investigate the effects due to random uncertainties, repeat tests need to be done each day, for several tests. Analysis of the data from the replicated tests should provide statistical information on the "within day" and "between day" test data variability.

In any event, the small magnitude of the differences obtained in the intercomparison tests are significant in that each TVC transfer standard was tested on two completely different calibration systems using different converters as the reference standard.

4. Conclusions

The results indicate that it is feasible to make fully automatic precision ac/dc difference measurements at any one voltage. The principal advantage of the system is the elimination of the need for any type of manually- or automatically-balanced TE comparator, permitting the system to be assembled using commercially available instrumentation, except for the switching modules. This approach, therefore, should make automation attractive to many calibration laboratories faced with the need to make ac/dc difference measurements. Moreover, the system can be used as a nearly self-calibrating meter calibration system. Measurements can be done with minimal operator intervention, eliminating tedious and fatiguing manual

operations. Hence, personnel presently engaged almost exclusively in manual ac/dc difference tests can be freed to do other work. Experience gained during many years of testing with manually operated systems at NBS has shown that the precision of the test results is dependent upon operator skill. The automatic system's precision is independent of operator skill, elminating this variable in the experimental uncertainty.

5. Acknowledgements

The authors are indebted to M. S. Carter who wrote much of the software and solved many difficult programming problems encountered in developing the system. S. G. Tremaine, L. Freeman and E. V. Byland also made valuable contributions to some of the programs which have become part of the total system software. C. B. Childers helped greatly by doing the measurements on the manual system.

6. References

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APPENDIX A

System Equipment List

The use of trade names or company products does not constitute endorsement or recommendation by the National Bureau of Standards, and does not imply that the products named are necessarily the best available for the purpose.

1. Computer and peripherals

    a. Hewlett-Packard 9825T Desk Top computer (with 64 kbytes of memory)
    b. Hewlett-Packard 98034A 488 interface (2 each)
    c. Hewlett-Packard 98035A real time clock with options 002 and 025
    d. Hewlett-Packard 9866B option 025 thermal printer
    e. Hewlett-Packard 9872B option 025 plotter
    f. Hewlett-Packard 98036A serial interface with 98241 test adapter
    g. Hewlett-Packard 9878A I/O expander
    h. Hazeltime 1500 video display terminal
    i. Hewlett-Packard 98226A printer cradle
    j. Hewlett-Packard documentation software PN 09825-10020
    k. Hewlett-Packard statistical software PN 09825-15030
    l. Hewlett-Packard 59300-10001 HPIB verifications cassette with service notes 5312A-2 and 59306A-4
    m. Hewlett-Packard 59405-66503 HPIB test card
    n. Hewlett-Packard I/O extender board assembly PN 98124-67901

2. Tektronix P6007100 probe PN 010-0165-00 (shown as 100/1 attenuator in Fig. 1.

3. Hewlett-Packard model 3438 Digital Multimeter, option 15 with rack flange kit, PN 5061-0074, (2 each, shown as DPM in Fig. 1)

4. a. Hewlett-Packard 5300B counter mainframe with service note 5300B-1
    b. Hewlett-Packard 5301 10 MHz counter module with service note 5301A-1
    c. Hewlett-Packard 5312A HPIB interface module
    d. Hewlett-Packard 10853A rack mount kit for 5300B counter
    e. Hewlett-Packard 10548A service support package with service note 5300B-1

5. a. Hewlett-Packard model 59306A relay actuator (2 each)
    b. Rack mount kit, PN 5061-0094
    c. Rack flange kit, PN 5061-0074

6. a. Guildline Model 9577 precision digital voltmeter (shown as DVM in Fig. 1)
    b. Option 03 three terminal input lead (2 each)
    c. Option 07 low thermal lead kit
    d. Input connectors (2 each no part number)

e. Option 08 service manual
f. Option 09 service kit
g. Option 10 calibration cover
h. Option 11 488 interface

7. a. Electronic Development Corporation (EDC) model 501J rack mount dc voltage calibrator with minimum 25 mA current output
   b. Option B, sixth decade
   c. Option C, standby/ready signal
   d. Option D, 100 mV range
   e. Option J, bipolar operation
   f. 488 interface kit, PN KT-48
   g. Option AM-1, manual control panel and display (BCD)

8. EDC, model RA4 high voltage amplifier with 1kV output at 25 mA minimum current

9. a. John Fluke Manufacturing Co. 5200A Programmable AC Calibrator and 5205A Precision Power Amplifier
   b. Option 05, 488 interface for 5200A
   c. Rack kit for 5200, PN M07-205-600
   d. Rack kit for 5205, PN M10-205-600

10. Low-Thermal-Emf switching module (NBS design)

11. High-Voltage-Relay switching module (NBS design)

APPENDIX B

Major Programs

In this appendix, a list of the major programs used in the ATS is given. A brief explanation of the purpose of each program is also given. Detailed documentation, such as the example given in Appendix C, is available for most of the programs. A summary of the programs is given in Table 4.

1. Program name: STABLE

STABLE is a program which is used to check the stability of the system's dc and ac sources. These stability tests are useful to determine whether or not the sources are functioning properly. Occasionally, ac/dc difference test results appear to be erratic, and the stability tests are a convenient method to ascertain whether the erratic results may be due either to the ac or dc source, or both. Stability of the sources is measured by using the system's real time clock and DVM whose function, reading rates, and ranges are remotely controlled. The program computes the deviation from nominal voltage in ppm, and prints the values of measured voltage and the deviation.

When a stability test is complete, the operator has the option of plotting the measured deviations as a function of time using a program named PLOTTER.

2. Program name: n-TEST

As discussed in the text, this program is used to determine a TE's dimensionless characteristic "n." To determine the equation for "n" as a function of TE output emf, (in mV), a program called "STATIS" is loaded and executed at the end of an n-test. The operator has the option of obtaining up to a fourth-order polynominal equation using a least-squares curve fitting algorithm. A plot of the actual measured n versus TE emf and the fitted curve can also be obtained as an option.

3. Program name: DCRD

This program is used to determine a TE's dc reversal difference as defined by eq (16) of the text. The operator has the option of testing at any one fixed value of a TE's heater current. Both the constant input and constant output values of dc reversal difference are computed. Finally, the response time of the test TE is determined. Response time is defined as the time it takes for the TE to reach 63.2 percent of its final (99 percent level) emf when full rated heater current is applied as a step funtion. If the operator desires, a program called EMF PLOTTER is loaded and executed. This program plots the data obtained during a response time test.

4. Program name: ACCAL

This program is used to calibrate an ac voltage calibrator, whether that of the ATS or an external unit, or a precision DVM. The program is discussed in Section 2.3.1 of the text.

5. Program name: ACDC

This program is used for ac/dc difference testing, and is discussed in Section 2.2 of the text. At the beginning of the test, the operator types into the computer the parameters of test voltage, frequencies, and number of runs per frequency. One run consists of four determinations of ac/dc difference, with each determination and the average of the four values printed. The test is made completely automatically at any one fixed voltage.

Table 4. ATS Software Summary

Program Name	Purpose	Options	Approximate Lines of Code	Approximate No. of Bytes
STABLE	Check stability of ac and dc sources	Repeat; Plotter	400	12,500
PLOTTER	Plot results of STABLE	Replot	150	4,000
n-TEST	Determine n of a TE	Rerun: STATIS; 50-120% rated TVC range:	200	6,800
STATIS	Up to fourth order curve fit of n-TEST data	Repeat: Repeat n-TEST: DCRD: Plot: Replot	200	5,800
DCRD	Measures constant input and constant output dc reversal diff of a TE. Also correct DCRD when n≠2.	Rerun: TIME CNST: DCRD	250	9,000
TIME CNST	Measures response time of a TE	EMF PLOT	30	900
			This program is a subroutine option of DCRD which can be run without doing a DCRD test.	
EMF PLOT	Plots response time data	None	30	900
ACCAL	Calibrate an ac calibrator	Repeat: Delete Data: Change voltage: Change frequency	300	10,000
AC/DC DIFF	Calibrate a UUT for ac/dc difference automatically at one fixed voltage	10 runs/frequency: 20 frequencies/test	550	16,500

GALLIUM ARSENIDE (GaAs)-BASED PHOTOCONDUCTIVE SWITCHES FOR PULSE GENERATION AND SAMPLING APPLICATIONS IN THE NANOSECOND REGIME*

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Abstract

This paper describes the design of a set of optoelectronic switches having an interdigitated electrode structure and implemented with high resistivity GaAs photoconductive substrates. A theoretical analysis is developed for determining the pulsed light ON state resistance (peak conductance), OFF state (dark) resistance, and the associated capacitances for the various designed gap geometries. Data are provided on the processing steps used in successfully fabricating a working set of switches based on the theoretical design. A test apparatus is used to make measurements of the pulsed light conductance of these devices having nominal gap spacings of 5, 10, 20, and 40 μm.

1. Introduction

The purpose of this paper is to describe the design and performance of a set of optoelectronic switches having an interdigitated electrode structure which provides low enough ON state resistance for operation in 50-Ω switching applications. This performance has been achieved by the increased optical sensitivity of the interdigitated electrode design and by the low contact resistances realized from an ion implantation process used during the fabrication of the switches. Earlier devices having gaps with a planar electrode structure showed the feasibility of achieving a practical gallium arsenide (GaAs)-based photoconductive switch with low ON state resistance (high ON state conductance) using a pulsed laser diode, fiber-optic-coupled, light source [1].

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A set of optoelectronic switches (of the surface layer photoconductive gap type) was designed having an interdigitated electrode structure, the active area of which would be compatible with the use of a large core (1000 μm diameter) fiber used for irradiating the multiple finger gaps. Previous experience, however, had indicated that for a limited range of optical power a significant tradeoff would be required in the design of these devices in order to realize low ON state resistance (R_{on}), high OFF state (dark) resistance (R_{off}), and minimal gap capacitance (C_g). A high R_{off}/R_{on} contrast ratio of 10^6:1 or larger is required in most circuit applications for good signal-to-noise ratio. For purposes of minimal signal feed-through in the OFF state, a very low value of C_g is also required. Consequently, a theoretical analysis was carried out to determine some of these tradeoffs [2].

Much research has been devoted towards investigating the detailed response of photoconductors, especially with regard to speed [3]. In a more recent paper by Auston, the gap capacitance in parallel with a time varying conductance, was found to be a good model also for photoconductors when mounted in transmission line networks [4]. Perhaps the most optically sensitive photoconductors to date are the Fe-doped indium phosphide (InP) devices fabricated by C. H. Cox, et al. at the MIT Lincoln Laboratory, having 2 μm-wide gaps and fingers over a 50 μm x 50 μm active area [5].

The apparatus used for testing the performance of the photoconductive switches is shown schematically in figure 1. A pulsed laser diode emits pulsed infrared light into an optical fiber with photon energy, $h\nu$. Most of this light exits the fiber and irradiates the multiple gap area of the interdigitated electrodes deposited on the GaAs chip. Rapid generation of hole-electron pairs occurs in the irradiated GaAs material, thereby providing a conduction path between the electrode fingers.

2. Theoretical Considerations

Figure 2 shows the circuit used for analyzing the measurement setup of figure 1. The device under test can be modeled as a time varying resistance R_t, in parallel with a gap capacitance C_g, in series with two contact resistances R_c. The small amount of shunt capacitance and conductance can usually be neglected. Previous analysis [1] has shown that the output voltage is proportional to the total gap conductance G_t, i.e.

$$V_o(s) \simeq \left[\frac{G_t(s)R_\ell}{1 + G_t(s)R_\ell}\right] V_B, \qquad (1)$$

where $G_t = \frac{1}{R_t}$ = total gap conductance.

By observing the peak value of $v_o(t)$, an approximate value for the maximum peak conductance G_{tp}(or minimum gap resistance, R_{on}) can then be obtained from (1). Obviously, for high bias-voltage switching efficiency, the G_tR_ℓ product should be large. Consequently, for efficient voltage switching in low impedance applications, the peak gap conductance, G_{tp}, must be correspondingly larger.

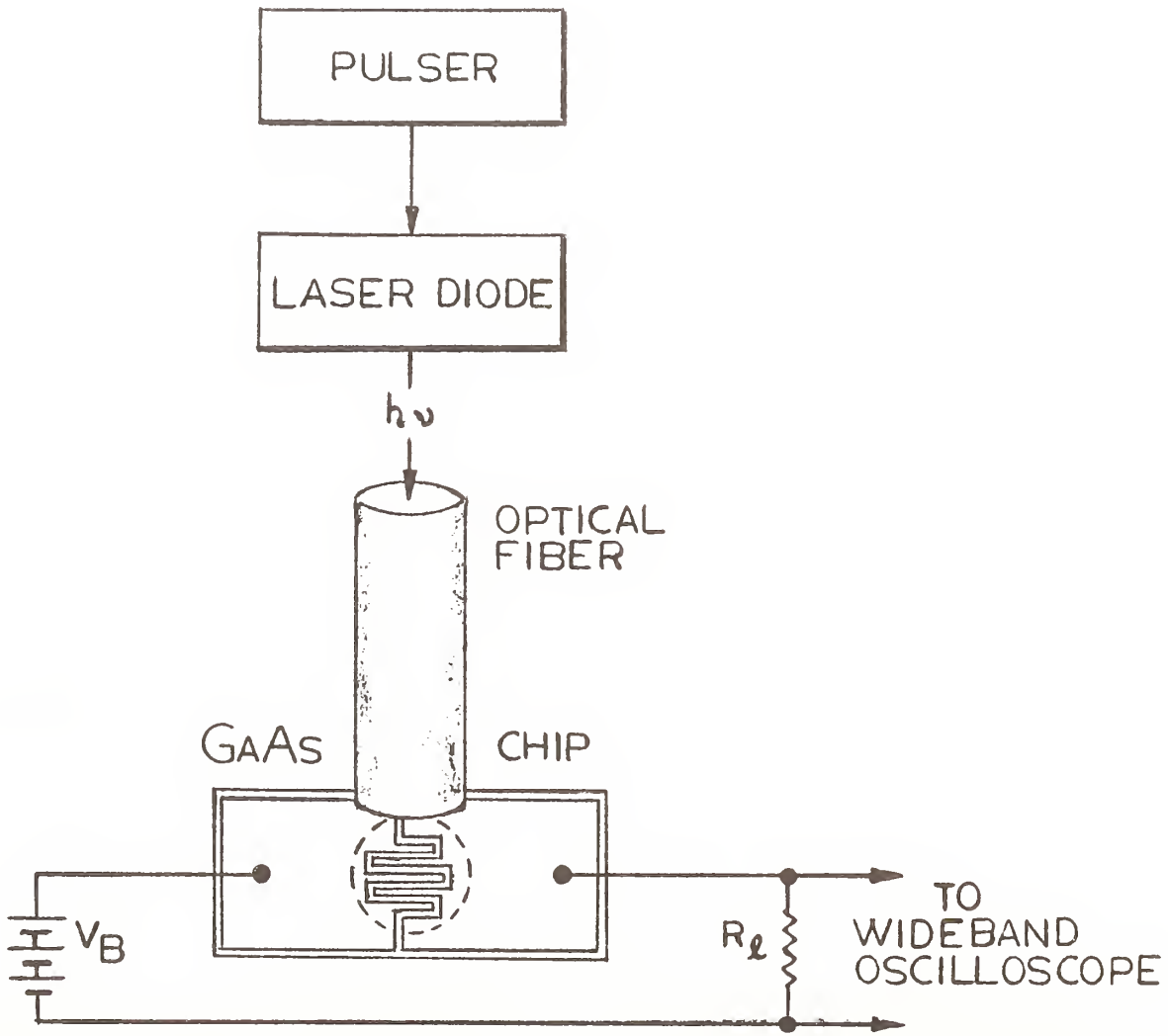


FIG. 1 BASIC CONFIGURATION OF GaAs SWITCHING APPARATUS

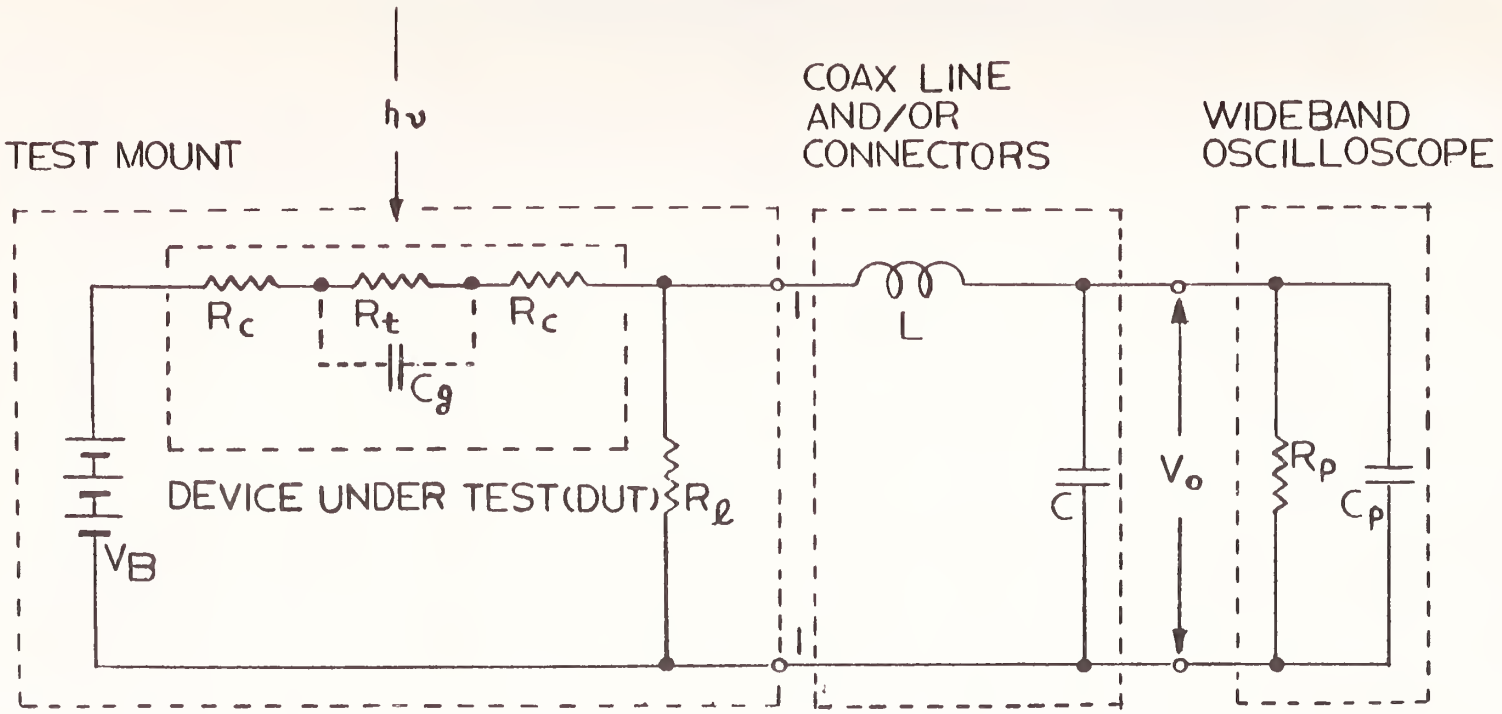


FIG.2 CIRCUIT MODEL OF PHOTOCONDUCTANCE MEASUREMENT-SETUP

To examine the factors that determine the total gap conductance, figure 3 shows an example of the computer generated pattern used for the contact mask of an interdigitated set of electrodes having 8 and 9 fingers, or 18 effective gaps, with a spacing of 20 μm. Such an electrode structure was designed to capture a maximum amount of optical energy from the fiber output port (as indicated by the dashed circle) for a given total length of the gap. Other similar patterns have fewer fingers, or total gaps, with gap spacings of 5, 10, and 40 μm. The width of a finger is designated W, the gap spacing is S, and a given gap length is denoted by L. Consider a "unit structure", as shown in figure 4, which depicts an idealized model of a section of the light-activated gap region. The bulk conductance of the unit gap (assuming that conduction is due to a single carrier), is then given by

$$G_t = \frac{1}{R_t} = (ne\mu)\,\frac{A}{S}\,, \tag{2}$$

where n = density of free carriers per unit volume,
e = charge of an electron,
μ = carrier mobility,
A = end face area of the activated carrier volume, and
S = gap (interelectrode) spacing.

The thickness of the activated carrier volume (absorption depth, $1/\alpha$) is a function of the photon energy, $h\upsilon$, of the laser light from the fiber. Letting N = number of photo-generated carriers and N_0 = equilibrium number of carriers in the dark, then $n = (N_0 + N)/SA$, and

$$G_t = \frac{(N_0 + N)\, e\mu}{S^2}\,. \tag{3}$$

Besides having high carrier mobility and small gap spacing, G_t is further increased only by increasing the number of photogenerated carriers, N. The generation of carriers (holes and electrons) in the gap is governed in turn by the excitation equation [1]:

$$\frac{dN}{dt} + \frac{N}{\tau} = \frac{A_g}{A_f}\,\frac{P}{h\upsilon}\,(1-\rho)\eta, \tag{4}$$

where N = number of photogenerated carriers,
τ = mean free carrier lifetime,
A_g = area of the interelectrode gap,
A_f = cross-sectional area of the optical fiber,
P = optical power from the fiber,
ρ = surface reflectance, and
η = quantum yield of internal photoelectric effect.

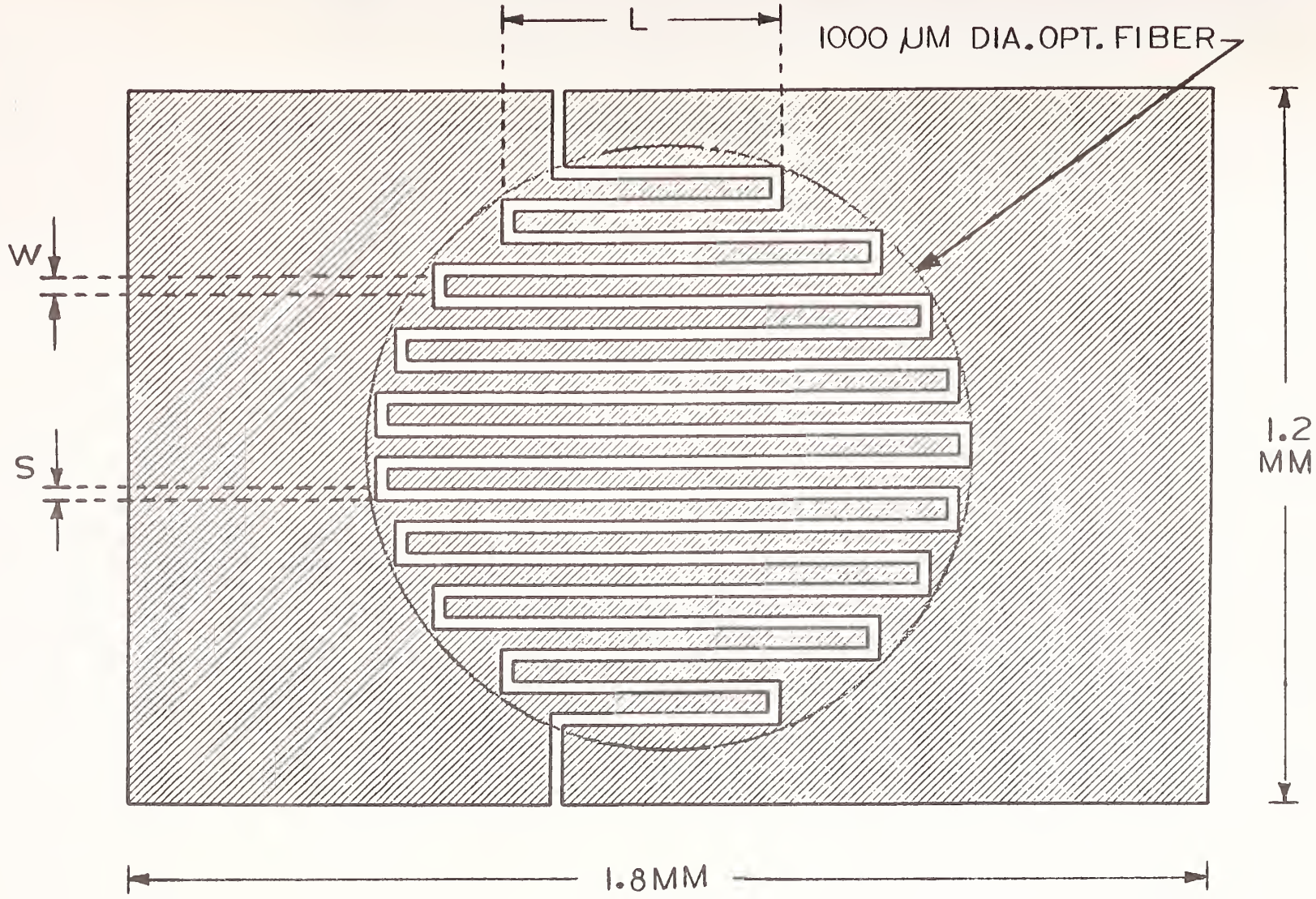


FIG. 3 INTERDIGITATED ELECTRODE PATTERN WITH L, W, AND S INDICATED.

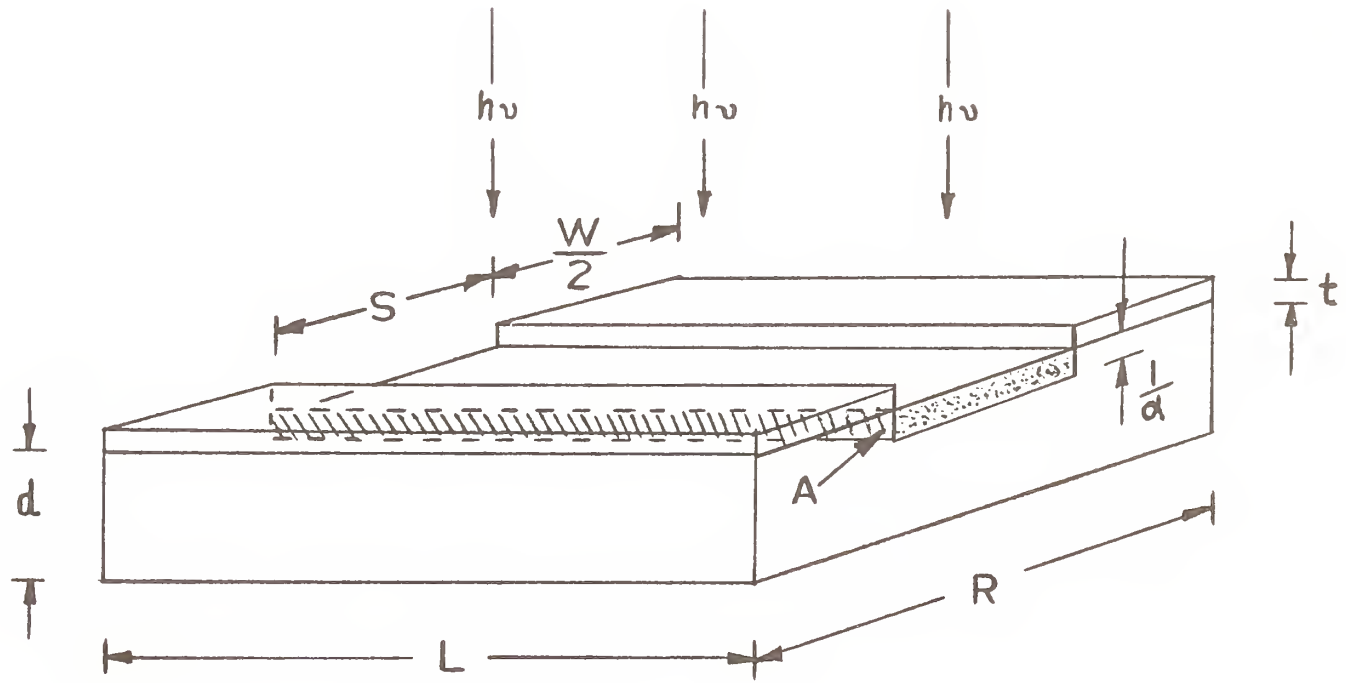


FIG.4 UNIT STRUCTURE MODEL OF A SECTION OF THE LIGHT-ACTIVATED GAP REGION

Thus, given the time dependent function of optical power P(t) and known or approximate values of the other above quantities, N(t) can be determined by equation (4). Two important solutions for equations (3) and (4), depending on the relative values of the optical pulse duration T, and the mean free carrier lifetime τ, are given in the Appendix.

One method of determining the gap capacitance of an interdigitated electrode pattern is to separate it into simpler single gaps, as sketched in figure 4. This approach is based on the fact that most of the excess charge caused by discontinuities is limited to regions near the gap, and that typically L>>W (so that fringe effects can be neglected). By using a two dimensional solution of Laplace's equation, and associated boundary conditions, the gap and shunt capacitances for the unit structure for different values of W, S, and d can be derived [2]. Summation formulas are developed in [2] for determining the gap capacitance per unit length, C_g(unit)/cm, and shunt capacitance, C_s(unit)/cm. Figure 5 shows curves of C_g(unit)/cm and $C_{s(unit)}$/cm plotted as functions of W/d and S/d. The gap capacitance of an interdigitated electrode structure, such as shown in figure 3, can then be calculated by summing the contributions of each unit structure, or

$$C_g = \sum_{i=1}^{N} L_i C_g(\text{unit}) + (N-1)W\, C'_g(\text{unit}), \qquad (5)$$

where N = number of gaps, and

$$C'_g(\text{unit}) = C_g(\text{unit}) \text{ for } W/d>>1.$$

After finding the total gap capacitance C_g, the OFF state (dark) resistance, $R_{tD} = R_{off}$, can then be determined from the relationship

$$R_{off}C_g = \frac{\varepsilon_o \varepsilon_r}{\sigma}, \qquad (6)$$

(provided $\varepsilon_r>>1$) where σ is the bulk conductivity of the photoconductive material of the gap in the dark. This $R_{off}C_g$ product is the nominal dielectric relaxation time of the gap modeled as a parallel plate capacitor [2].

3. Device Design and Fabrication

The design of the four interdigitated electrode patterns shown in figure 6 were based on achieving values of C_g from about 0.1 to 1 pF using unit structure dimensions compatible with the curves given in figure 5. An initial set of these devices was fabricated at NBS using high resistivity ($\rho = 10^6$ to 10^7 $\Omega \cdot$ cm) semi-insulating GaAs substrate material. Gold-germanium (AuGe) electrodes were deposited in the various patterns described above. These devices showed greater optical sensitivity than the planar gap devices in response to the pulsed light source (λ = 850 nm), indicating that the interdigitated electrode design produced higher pulsed light conductance than the earlier devices.

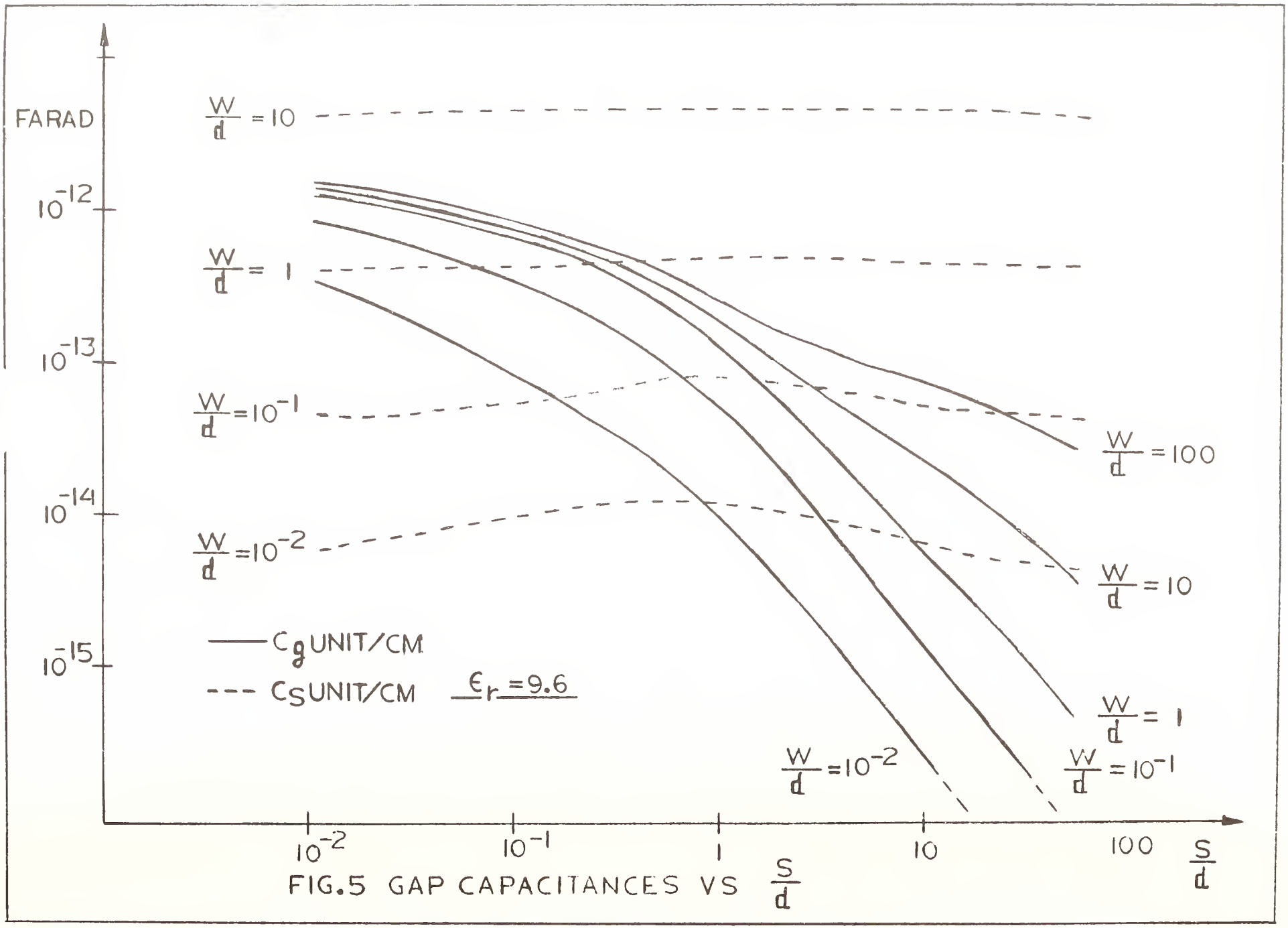
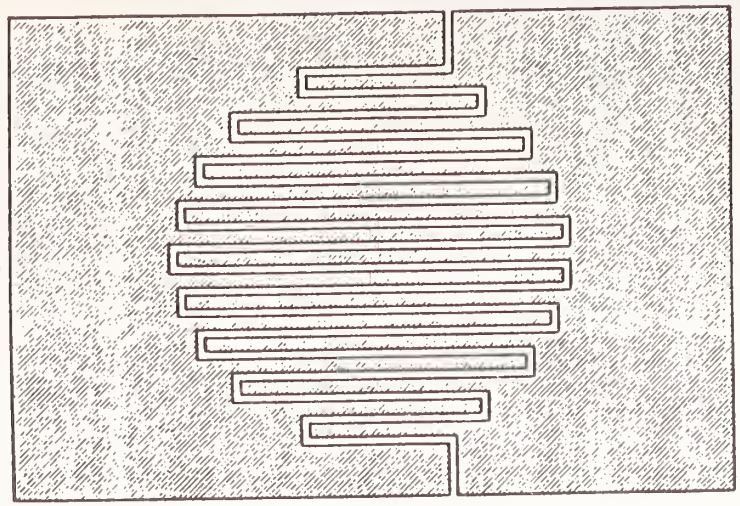
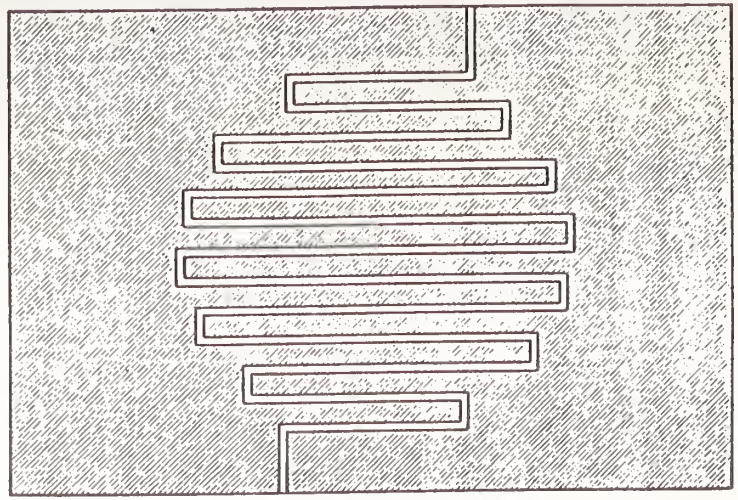


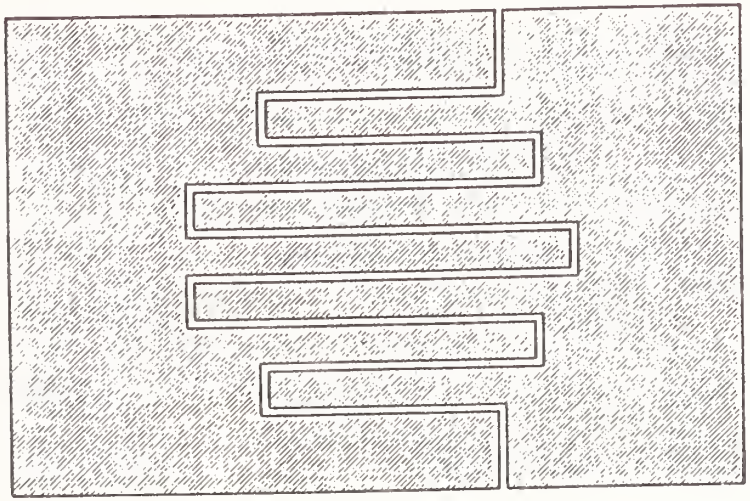
FIG.5 GAP CAPACITANCES VS $\frac{S}{d}$



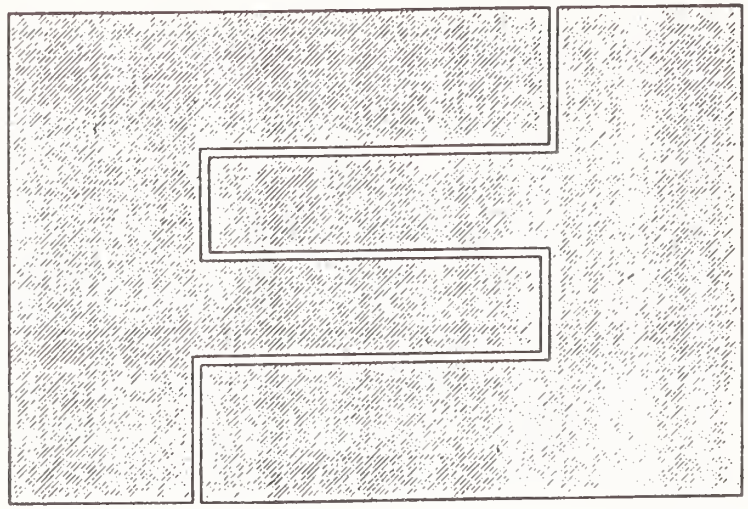
18 GAPS



13 GAPS



8 GAPS



3 GAPS

FIG.6 THE FOUR BASIC PATTERNS OF THE NES GaAs SWITCHES

A set of interdigitated electrode switches using the same basic contact masks was then fabricated by the ITT Corporation, Gallium Arsenide Technology Center, Roanoke, Virginia. The devices were made on commercially available 50.8 mm diameter undoped semi-insulating GaAs substrates with (100) orientation. The substrate material has a resistivity of about 2×10^7 $\Omega \cdot$ cm, electron mobility of 6800 $cm^2/V \cdot s$, and a dislocation density of approximately 3×10^4 cm^{-2}. For device fabrication, as shown in figure 7, a 2500 Å layer of SiO_2 is chemically vapor deposited over the wafer to provide surface passivation and encapsulation for implant annealing. To reduce contact resistance to the semi-insulating substrate, a selective n-type implant is done in the ohmic contact areas. Before performing the implant, the SiO_2 is etched in a CF_4 plasma to reduce its thickness to 1000 Å in the contact areas. Silicon ions at an energy of 120 keV and a dose of 1×10^{13} cm^{-2} are then implanted, and annealed at 850° C for 20 minutes, using the SiO_2 as an encapsulant. This implant provides a doping level of about 2×10^{17} cm^{-3}, allowing the formation of reproducible ohmic contacts with low contact resistance. Next, the windows in the SiO_2 layer are etched through to the GaAs surface, and AuGe/Ni ohmic contacts are patterned by liftoff. Good liftoff is assured by the fact that the AuGe/Ni thickness of 1800 Å is less than the SiO_2 thickness of 2500 Å. The ohmic contacts are then alloyed at 450°C for 1 minute. Finally, 2300 Å of Ti/Pt/Au is evaporated onto the ohmic contacts to provide better bond wire contact to the finished devices.

4. Test Results

Figure 8 shows a photograph of multiple oscilloscope traces taken of the output voltage, $v_o(t)$, from the photoconductance measurement setup for an 18 gap device (S8.40). The five different traces correspond to five distinct levels of peak optical power (out of the laser/optical fiber source) irradiating the switch, as indicated in the accompanying table. Traces (1), (2), and (3) correspond to responses where the increased peak output is nearly proportional to the increase in peak optical power, as theoretically predicted by equations (1) and (16). However, further increases in optical power, such as shown by traces (4) and (5), cause a response where the total volume of the light-activated gap has become saturated with carriers and the photoconductance has been maximized. The peak output voltage level is then limited by the contact resistances of the switch (see figure 2). The peak conductance of a complete set of the 8 gap devices (S4.40, S4.20, S4.10, and S4.05) was also measured as shown in figure 8, and summarized in Table 1, where $R'_{on} = R_{on} + 2R_c$. The value for R_{on} (calculated) was determined from equations (7) and (16) using nominal dimensional and material parameters with $P_p = 0.6$ W and $\tau = 750$ ps (see the section below on Computer Simulation).

Figure 9 gives a plot of capacitance versus frequency, summarizing the data obtained in making measurements of the gap capacitance, C_g, of the five devices reported on in this paper. These measurements were made on the NBS Type 2 bridge (used for calibrating precision capacitance standards) which has a resolution of 1×10^{-18} farads and an uncertainty of ±0.0001 pF [6]. A special test fixture was utilized for this purpose which has a residual capacitance of 0.024 pF or less, so that very good measurements to 0.1 pF (the estimated total uncertainty) are possible. As shown in figure 9, there is some frequency dependence on these measurements of C_g. The values de-

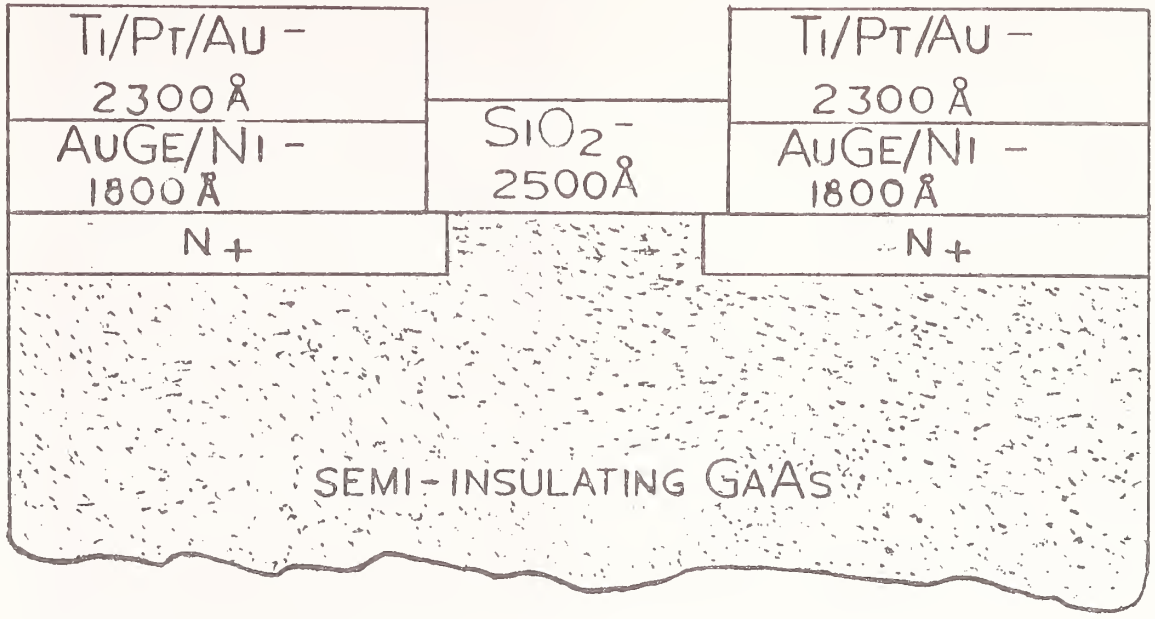


FIG.7 CROSS-SECTION OF THE FABRICATION PROCESSING DETAILS

S 8.40 DEVICE

P_{OF}	TRACE	R'_{ON}
2.0W	TOP 5	5.5 Ω
1.3W	4 SATURATION	7.9 Ω
0.93W	3	12.5 Ω
0.60W	2	31.6 Ω
0.24W	BOTTOM 1	110 Ω

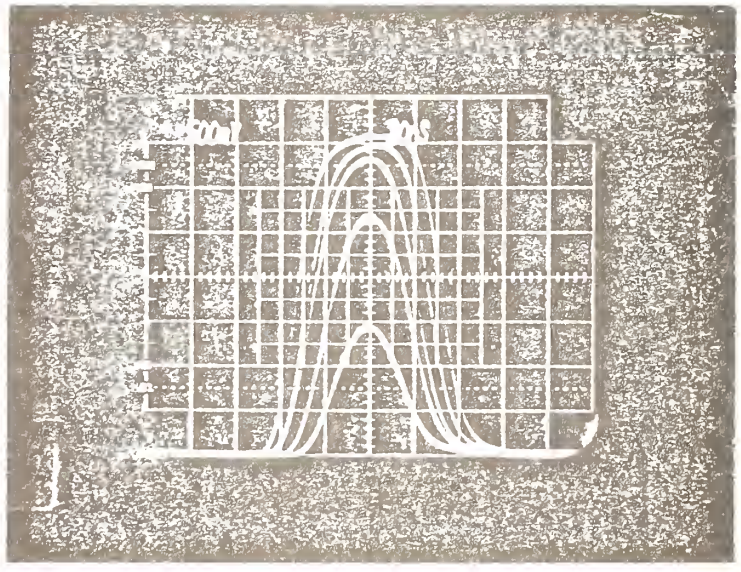


FIG.8 COMPARISON OF OUTPUT PULSES AS A FUNCTION OF PEAK OPTICAL POWER

DEVICE	R_{ON} CALC.	R'_{ON} MEAS.	$R_{CONT.}$ EST.	$R_{CONT.}$ MEAS.	C_G CALC.	C_G MEAS.	R_{OFF} CALC.	R_{OFF} MEAS.	$\frac{R_{OFF}}{R_{ON}}$
S8.40	12.1Ω	31.6Ω	9.7 Ω	6.2 Ω	0.4pF	1.4pF	46.2MΩ	159MΩ	5×10^6
S4.40	24.2Ω	37.0Ω	6.4 Ω	10.7 Ω	0.3pF	0.6pF	65.6MΩ	167MΩ	4.5×10^6
S4.20	12.1Ω	50.0Ω	18.9 Ω	4.4 Ω	0.4pF	1.1 pF	46.1MΩ	127MΩ	2.5×10^6
S4.10	6.0Ω	41.0Ω	17.4 Ω	4.4 Ω	0.5pF	1.1 pF	34.9MΩ	116MΩ	2.8×10^6
S4.05	3.0 Ω	33.3Ω	15.1 Ω	7.2 Ω	0.6pF	1.7pF	28.8MΩ	53MΩ	1.6×10^6

NOTE: S8.40 – 17 FINGERS – 18 GAPS – 40 μM GAP SPACING
S4.40 – 7 " 8 " 40 "
S4.20 – 7 " 8 " 20 "
S4.10 – 7 " 8 " 10 "
S4.05 – 7 " 8 " 5 "

TABLE 1

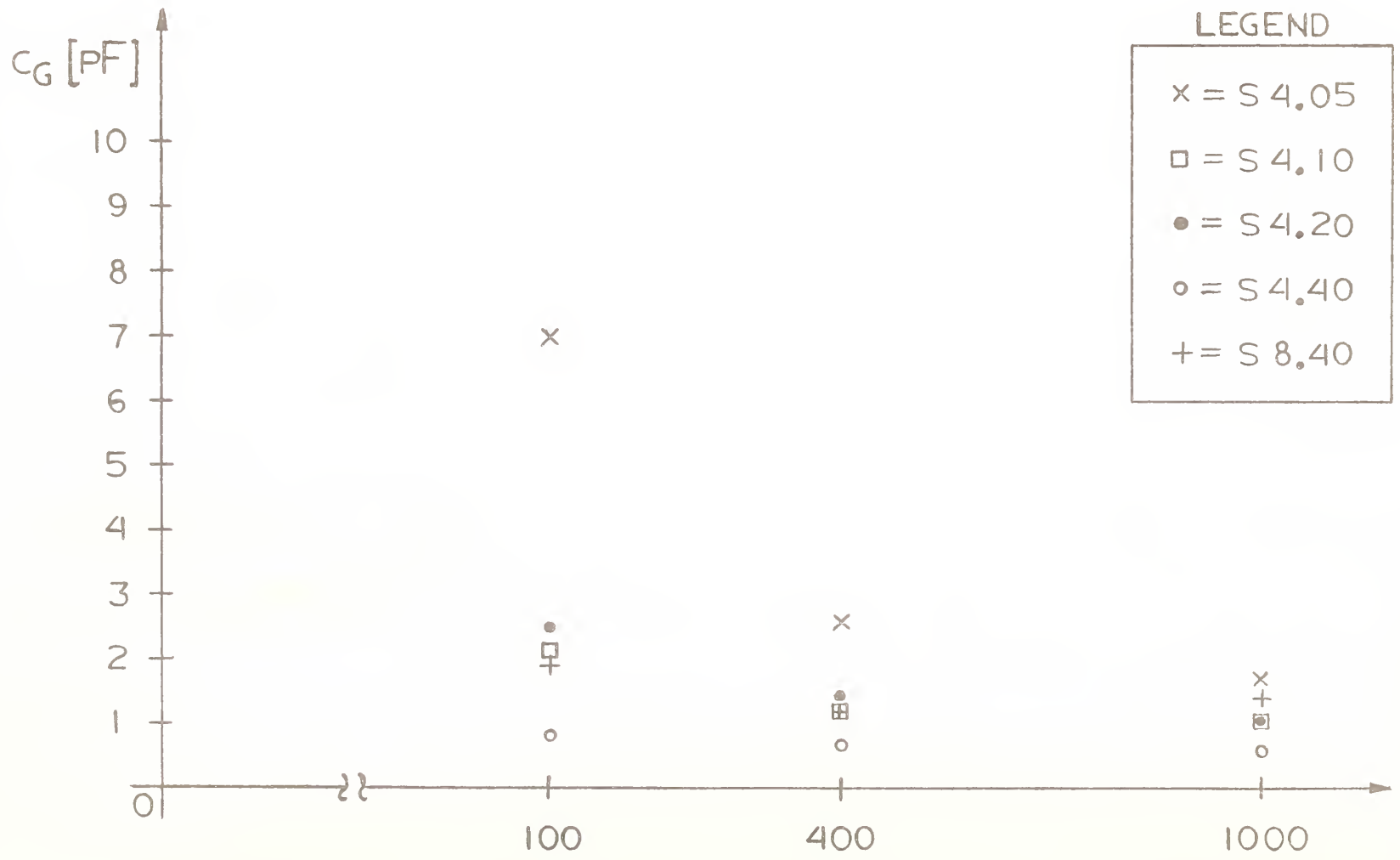


FIG. 9 PLOT OF GAP CAPACITANCE VS FREQUENCY [Hz]

termined at the standard test frequency of 1 kHz are summarized in Table 1. Because of the discrepancy between the calculated values of C_g and the measured values of C_g, additional work is needed to achieve greater confidence in the actual values of C_g obtained with these interdigitated gap designs.

Several means were available for measuring the large OFF state (dark) resistance (R_{off}) of these devices, including a high resistance ohmmeter and the excellent leakage (or, conductance, G) measurements available on the NBS Type 2 bridge. A third method for showing how R_{off} varies over several decades of voltage and current is shown by the I-V curve given in figure 10 for one of the 8 gap devices (S4.40). Ohmic behavior was typically obtained on the devices that worked well up to about 10 volts. The values of R_{off} (measured) used in Table 1 are an average of the three means used for making this measurement. The value for R_{off} (calculated) was determined using equation (6) with $\varepsilon_r = 10$, $\rho = 1/\sigma = 2 \times 10^7\ \Omega \cdot cm$, and $C_g = C_g$ (calculated).

6. Computer Simulations

Using the circuit model shown in figure 2, (neglecting R_c, L and C), as well as the theoretical relationships given in the section on Theoretical Considerations, a computer program was developed using extended SCEPTRE to simulate the transient light conductance response. The input optical power was approximated as $P(t) = P_p \sin^2 \omega t$, with a peak input of $P_p = 0.93$ W. Equation (4) was used for obtaining N(t) which was then the forcing function generating $R_t(t) = 1/G_t(t)$. The corresponding output voltage response, $v_o(t)$, is then provided by the SCEPTRE simulation program. Figure 11 shows a plot of the simulated output response with varying values of mean free carrier lifetime, τ, for the 18 gap device (S8.40). Nominal parameter values of gap spacing ($S = 40\ \mu m$), mobility ($\mu = 6800\ cm^2/V \cdot s$), wavelength ($\lambda = 850$ nm), area ratio ($A_r = 0.739$), $V_B = 4$ V, and $R_\ell = 50\text{-}\Omega$ were used for these simulations where an overall optical efficiency of $(1-\rho)\eta = 0.7$ was assumed. Apparently, a value of $\tau = 750$ ps most nearly approximates the actual mean free carrier lifetime of these devices.

The computer simulation program also provides the R_t response to the pulsed optical power. Using the same nominal parameter values as above, except with $A_r = 0.372$ for an 8 gap device (S4.40), figure 12 shows a plot of the simulated inverse variation of R_t with applied optical power $P = P_{of}$ from the fiber. Also plotted on figure 12 are the measured values of R'_{on} (see Table 1) for the S4.40 device. These results confirm the usefulness of the simulation model in predicting the performance of the interdigitated devices.

7. Conclusions

The testing results for determining the values of R_{on}, $R_{contact}$, C_g, and R_{off} parameters of a set of (interdigitated electrode) GaAs-based optoelectronic switches is summarized in Table 1. For an applied peak optical

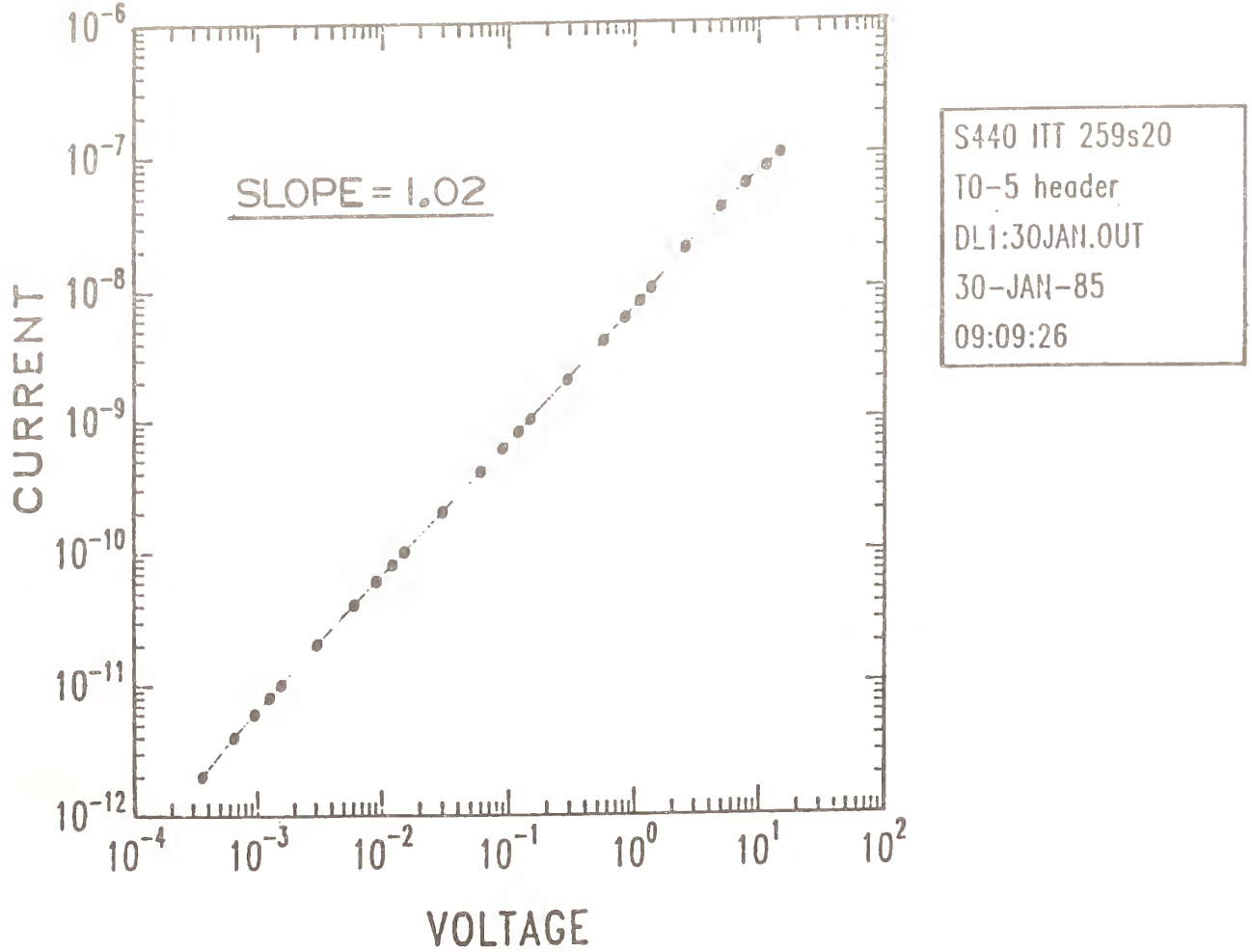


FIG.10 I-V PLOT OF AN 8-GAP DEVICE

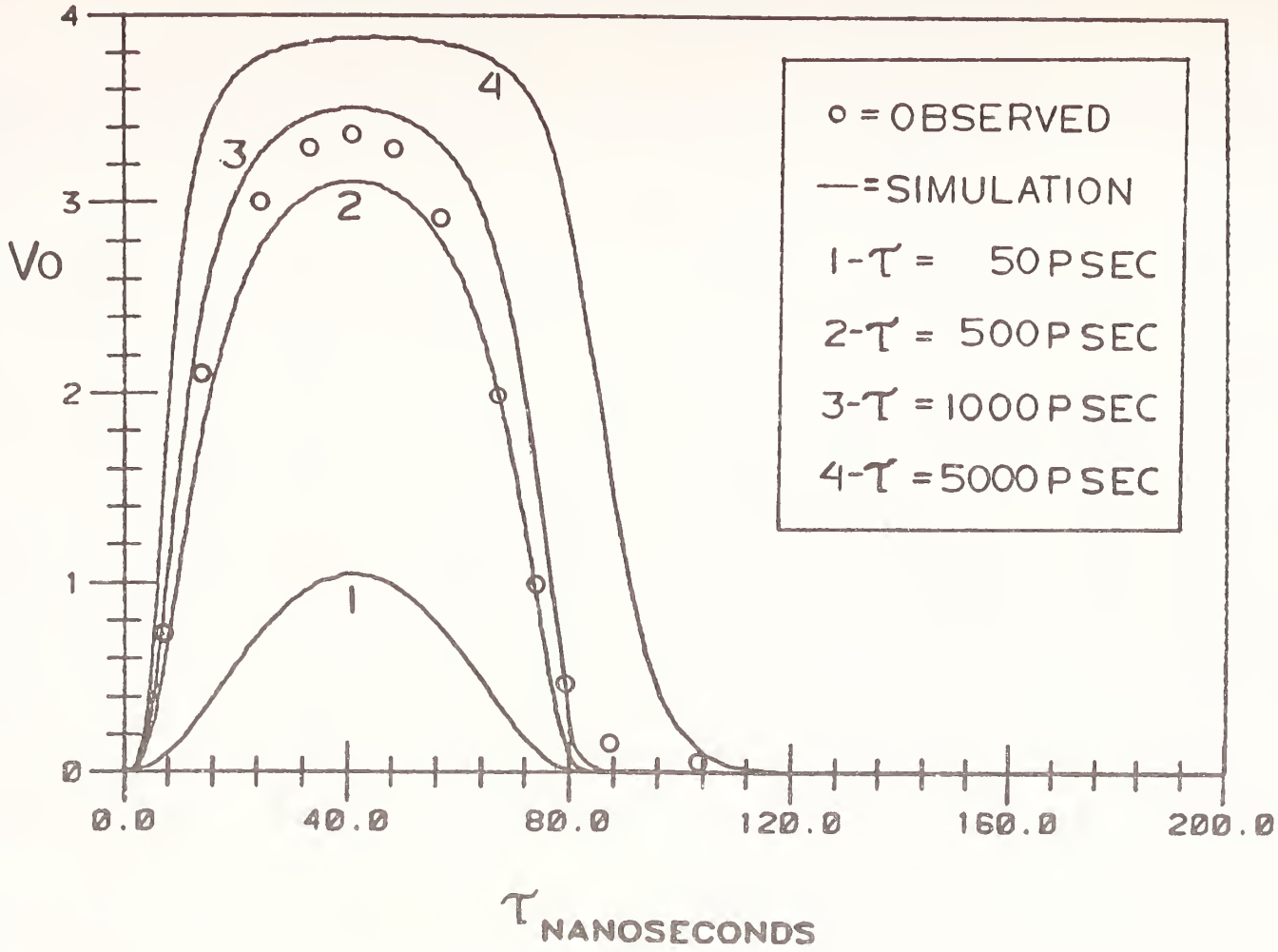


FIG. 11 PLOT OF SIMULATED OUTPUT VOLTAGE [Vo] FOR VARIOUS VALUES OF MEAN FREE CARRIER LIFETIME [τ]

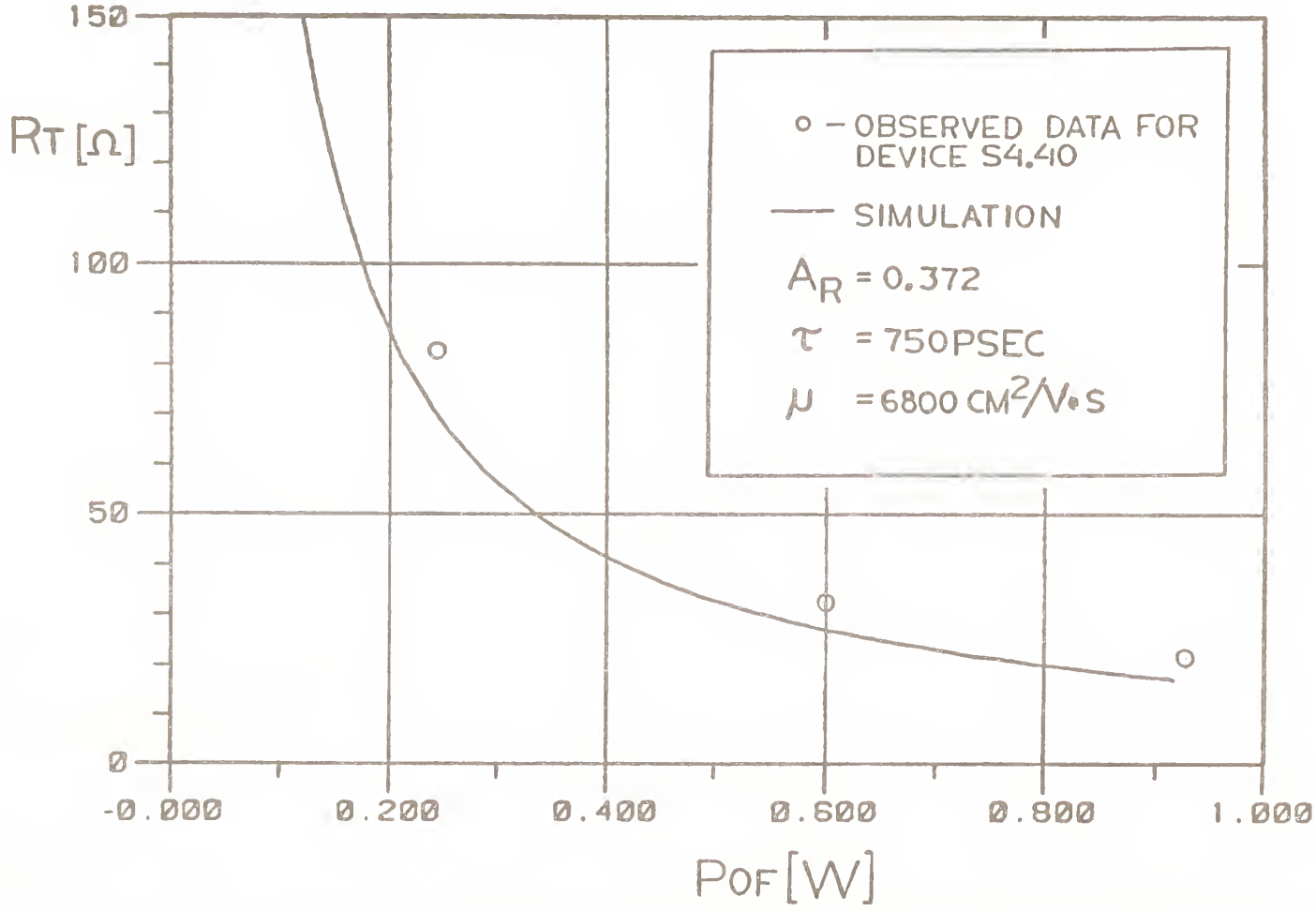


FIG.12 PLOT OF SIMULATED VARIATION OF RT WITH APPLIED OPTICAL POWER POF

power on the order of 1 W, saturation of these devices is achieved with a residual contact resistance of only about 10-Ω. Hence, efficient bias voltage switching of greater than 80 percent can be achieved in 50-Ω load environments with R_{off}/R_{on} contrast ratios of 10^6:1 or greater. Computer simulations of the circuit model and theoretical photoconductance properties of these devices are given which are in good agreement with the measurement results.

8. Acknowledgements

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APPENDIX

Two Solutions of Equations (3) and (4)

In equation (4), let

$$K = \frac{A_g}{A_f} \frac{1}{h\upsilon} (1-\rho)\eta, \tag{7}$$

so that

$$\frac{dN}{dt} + \frac{N}{\tau} = K\ P(t). \tag{8}$$

Let P(t) be an optical pulse of amplitude P_p and duration T, i.e.,

$$P(t) = P_p[u(t) - u(t-T)], \tag{9}$$

so that

$$sN(s) + \frac{N(s)}{\tau} = \frac{KP_p}{s} [1-\exp(-Ts)], \tag{10}$$

or,

$$N(s) = \frac{KP_p\tau}{s(1 + s\tau)} [1-\exp(-Ts)]. \tag{11}$$

The solution for N(t) is then

$$N(t) = KP_p\tau[1-\exp(-t/\tau)][u(t)-u(t-T)]. \tag{12}$$

When dealing with ultrashort pulse laser sources, then for $t \leq T \ll \tau$,

$$\begin{aligned} N(t) &\simeq KP_p\tau[1-(1-t/\tau)][u(t)-u(t-T)] \\ &= KP_pt[u(t)-u(t-T)], \end{aligned} \tag{13}$$

so that from (3), with N_0 negligible,

$$G_{tp} = \frac{K(P_p T)e\mu}{S^2} = \frac{1}{R_{on}} \cdot (T<<t). \qquad (14)$$

This result shows the peak conductance (minimum ON state resistance) to be dependent on the optical pulse duration, or energy of the light pulse. However, in the nanosecond regime where in many cases, $T>>\tau$, then for $t \leq T$,

$$N(t) \simeq KP_p\tau[u(t)-u(t-T)], \qquad (15)$$

and

$$G_{tp} = \frac{K(P_p\tau)e\mu}{S^2} = \frac{1}{R_{on}} . \quad (T>>\tau). \qquad (16)$$

The result in this case is that the peak conductance is dependent on the mean free carrier lifetime, independent of the optical pulse duration. Peak optical pulse power, and not pulse energy, is what determines G_{tp}, (or the minimum ON state resistance, R_{on}).

AN APPROACH TO ATE CALIBRATION VIA PERFORMANCE VERIFICATION AT THE SYSTEM INTERFACE *

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Gaithersburg, MD

Abstract

A method of verifying the performance of automatic test equipment (ATE) in its normal operating environment and configuration is presented as the best approach to achieving an overall system calibration. The method consists of the transport of well-characterized signal sources to the ATE station and the application of these electrical stimuli directly to a well-defined electrical interface on the test station. Data is presented on typical accuracies that have been obtained on limited parameters and ranges during the testing process, using calibrated commercial equipment.

1. Introduction

Several approaches have been used to assure that ATE systems perform properly. The traditional approach is the calibration of each "drawer" or instrument of the system. Typically, instruments such as a digital voltmeters, precision voltage or waveform sources, and frequency counters, are removed from the ATE station and sent to a calibration laboratory where their performance is evaluated and any necessary calibration adjustments are made. Such an approach has several shortcomings. For example, the test system often cannot be used during the time the instruments are removed for calibration unless replacements can be found. A more serious deficiency of this approach, from a metrology point of view, is the fact that instruments are not characterized in the same environment as they are used. For example, the accuracy of a digital voltmeter may exhibit sensitivity to temperature changes. Its normal operating temperature range in the ATE system may be quite different than that encountered in the calibration laboratory. In addition, interferences, such as high frequency signals produced by other instrumentation and computers in the ATE system may degrade the performance of such precision measurement equipment. These effects are usually not present when the performance of the measurement equipment is evaluated in the calibration laboratory. A further shortcoming of the practice of removal, calibration, and replacement of measurement equipment is that such procedures result in a calibration that does not account for losses and offsets in the signal path between the interface connector, where the unit under test UUT is

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connected, and the instrument terminals, where the instrument was calibrated. Since signals from the UUT are typically switched through relays and have relatively long path lengths, signal losses and offsets may affect the measurement accuracy, especially for low-level signals. In view of the shortcomings listed above, the user of ATE which has had instruments removed and calibrated outside the ATE system itself may have greater confidence in the equipment performance than is warranted.

Another calibration approach employed with ATE systems in order to increase the confidence in the resulting measurements is the use of various types of built-in test or self-testing schemes. If properly implemented, such schemes may be valuable towards assuring that measurements made by an ATE system are consistent. However, such techniques alone cannot perform a calibration function to determine the difference between values of physical quantities, such as voltage and frequency, measured by the ATE system and those measured quantities that have traceability to national standards. Measurements have traceability to a designated set of standards if and only if scientifically rigorous evidence is produced on a continuing basis to show that the measurement process is producing measurement results for which the total measurement uncertainty relative to national or other designated standards is quantified [1].

To assure verification of the performance of test equipment, and achieve meaningful traceability, well-characterized standards must be applied to the ATE station while it is operating in its normal environment. An example of such an "in-situ" station calibration is the Portable Automatic Test Equipment Calibration Concept (PATEC) used by the Air Force Guidance and Metrology Center. The PATEC concept consists of verifying the performance and calibrating certain critical or "core" instruments used by the ATE system using portable programmable calibrators connected via the system interface. After such direct calibration, the remainder of the instrumentation contained in the station are then calibrated by using the core instruments as standards, together with "wrap around" interface adapters. The Navy implements a similar concept using the Modularly Equipped and Configured Calibrators and Analyzers (MECCA). Both of these programs utilize portable calibration systems that assure the performance of ATE on site via a system calibration.

2. The Use of Transport Standards

The National Bureau of Standards (NBS) has had a program, in cooperation with the Department of Defense (DoD) to determine the feasibility of using transport standards to verify the performance and calibration of ATE systems [2]. The approach employs the use of portable transport standards with sufficient accuracy and long-term stability to properly characterize the ATE station under investigation. It was essential that these transport standards were sufficiently versatile so as to permit the application of a range of well-calibrated stimuli directly to the UUT interface connector. A realistic evaluation of the accuracy of the ATE system could then be made when the system was operating in essentially the same conditions as when testing a UUT.

Portable transport standards offer an advantage over alternative methods of characterizing an ATE station since the effects of losses and offsets occuring in the cabling and switching networks can be also properly characterized. In addition, it is desirable to be able to program the transport standards by means of a computer or instrument controller since statistically meaningful tests require that lengthy sequences of stimuli be applied to the ATE system under test. For example, to adequately characterize ac voltage measurements made by an ATE system, many combinations of voltage amplitudes and frequencies must be applied. Portable transport standards, in conjunction with portable "desk-top" controllers, offer a powerful way to generate such sequences, with the flexibility of making possible program changes on site.

3. Implementation of the Transport Standards for AC, DC, Phase, and Pulse Parameters

Based on a knowledge of the key measurement capabilities of an ATE system to be characterized, the parameters and ranges of the required stimuli can be selected. For example, in this particular project ac and dc voltages, electrical phase angle, and pulse duration were the quantities used to characterize one particular "third-generation" ATE system initially studied by NBS. DC voltages from +/- 100 mV to +/- 195 V, and ac voltages from 300 mV to 140 V (rms) at various frequencies from 50 Hz to 10 MHz were applied to the ATE system at the UUT interface connector in order to investigate its dc and ac measurement performance. Additionally, it was desired to verify the performance of the ATE station in measuring pulse duration over a range of 50 nS to 1000 ns.

Two transport packages consisting of test equipment were assembled; one for the dc and low-frequency ac voltage source, and the second for a pulse voltage source. The dc and low-frquency ac voltage source package contained a commercial meter calibrator, a digital voltmeter, and a desk-top computer/controller. The pulse source package contained a high resolution time synthesizer for generating pulses of precise time duration, and a pulse generator that was used to generate the output repetition rate of the pulses. In addition, an NBS Phase Angle Calibration Standard was used as a source of phase angle signals [3]. The NBS Phase Angle Calibration Standard produces a pair of digitally synthesized sine waves. All parameters, with the exception of the pulse repetition rate, were capable of being controlled by the computer/controller via an IEEE-488 bus. Thus, sequences of various voltages or pulse widths could be applied to the ATE system with a minimum of operator intervention.

Prior to applying these sources to an ATE system, the transport packages were carefully characterized to measure their accuracy, their stability with time, and the effects of temperature, line voltage, and other environmental factors that may affect their performance. In all cases, the characterization of the transport standards package was performed at the termination of the cable and adapters that were necessary to interconnect the standards with the ATE system under investigation. Furthermore, the input impedance of the ATE system was simulated with resistance-capacitance networks at the interconnection

interface. Thus, the electrical environment during the characterization tests performed on the transport standards approximated that encountered during the connection of the transport standards to the ATE system.

For example, the output of the dc transport source was intercompared periodically with the U.S. Legal Volt maintained by NBS. Over a period of five months, the dc source exhibited a 3 sigma uncertainty of less than 0.004 percent over a voltage range of +/-0.1 to +/-200 V dc. Likewise, over a three month period, the pulse source exhibited changes in pulse duration of less than +/-0.6 percent over the range of 50 to 1000 ns.

The voltage of the ac output from the source was measured as a function of rms amplitude and frequency by means of a thermal voltage converter. The ac and dc voltages of the source were available at the same output terminals by programming the source over the IEEE-488 bus. The output of the thermal converter was measured by the digital voltmeter, also controlled by the bus. In this manner, full control was exercised over the generation and application of ac and dc voltages to the converter and over the recording of the resultant thermocouple emf voltages. A multiplier (current scaling resistor), inserted between the source and the thermoelement allowed the thermal converter to be used over a voltage range of 2 to 600 V ac (rms).

The observed 3 sigma uncertainty in the voltage of the ac source over the frequency range of 50 Hz to 50 kHz was less than +/-0.01 percent during a three month period. The combined effects of temperature and line voltage changes along with additional uncertainties contributed by the thermal converters, voltmeter non-linearities, and effects due to movement of the source from the calibration laboratory at NBS to the remote ATE site gave conservative estimates of total uncertainties of +/-0.02 percent and +/-0.12 percent for dc and ac voltages, respectively.

AC voltages at frequencies between 50 kHz and 10 MHz are more difficult to measure accurately than those at lower frequencies. At the higher frequencies, small inductances and capacitances associated with the connection of the calibration source to the ATE system become important. If not properly accounted for, the losses in the cable between the wideband output of the source and the interface of the ATE system introduce a source of systematic uncertainty. To connect the source to the ATE system, a 1.5-m cable is required. Typically, this additional cable length provides an attenuation of the signal of approximately 0.6 percent at 10 MHz. Thus, all measurements were made using a 1.5 m length of RG-58/U cable connected to the wideband output unless otherwise specified.

The ac voltage output at the interface adapter pins, as a function of frequency, was determined by the use of a thermal voltage converter which has a specified input impedance of 50 ohms (+/- 0.3 percent) and a voltage range of approximately 0.2 to 0.45 V ac (rms). To measure voltages in excess of 0.45 V ac, a set of two precision 50-ohm coaxial attenuators was used that had power attenuations of 6 and 10 dB respectively. By means of the attenuators, either individually or in series, the voltage measurement range could be extended to 2.8 V ac. The overall uncertainty of the output voltage of the wideband source at the interface adapter pins was calculated to be +/-0.7

4. Application of Transport Standards to an ATE System

The transport standards were applied to several third-generation ATE systems used by DoD. Measurement programs were written in ATLAS to permit the ATE station to measure dc voltages, low frequency ac voltages in the frequency range of 50 Hz to 50 kHz, and high frequency ac voltages in the range of 50 kHz to 10 MHz. Additional programs measured pulse duration and phase angle. The transport standards were interconnected to the ATE system by means of the cables and the interface adapter that had been used in the characterization of the standards. This overall package permitted the application of the ac and dc voltages, pulses, and phase angles to the ATE system under the same conditions in which they were calibrated. In addition, a means was provided for the ATE station to generate a "test complete" pulse to the controller. The controller then instructed the transport standards to provide the next stimuli in a preprogrammed sequence. The measurements from the ATE station were printed and recorded on the system disk file. In this manner, an extensive set of measurement data could be obtained to analyze the errors of the ATE system being characterized since all the data was in "machine compatible" form.

5. Conclusion

The use of accurate transport standards has been demonstrated to be a useful concept for the characterization and calibration of ATE systems. In order to meaningfully characterize the performance of an ATE system, the signals must be accurately determined at a defined measurement interface over the range of environmental conditions that typically would be encountered.

6. References

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11. ABSTRACT (A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here)

Modern electronic instrumentation metrology in the low frequency regime (dc-10 MHz) was discussed in lecture talks and papers presented at NBS, Gaithersburg, MD on October 18-19, 1983. The seminar program was organized into four main session topics, as outlined in the Seminar Agenda (see pp. viii and ix).

This special publication contains complete papers on the subjects presented at the seminar, providing more of the technical details. For the sessions on Precision Waveform Synthesis, Precision Waveform Sampling, and Data Converter Characterization, six formal papers are given describing the hardware and software techniques used for developing NBS laboratory standards and apparatus for testing ac sources and voltmeters, phase angle meters, transient waveform recorders, wideband wattmeters, and digital-to-analog and analog-to-digital converters. For the informal session on Instrumentation Metrology, three subsequent papers have been written for publication which are included for completeness in the Appendices.

12. KEY WORDS (Six to twelve entries; alphabetical order; capitalize only proper names; and separate key words by semicolons)

analog/digital converters; ATE; automatic test systems; conducted EMI; calibration methods; digital-analog converters; digital synthesis; phase angle; photoconductance; sample/hold amplifiers; sampling techniques; settling time; thermal voltage converters.

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