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Semiconductor Measurement Technology

Quarterly Report
April 1 to June 30, 1974

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[2] Part of the Center for Radiation Research.
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Semiconductor Measurement Technology

Quarterly Report, April 1 to June 30, 1974

W. Murray Bullis, Editor

Electronic Technology Division
Institute for Applied Technology
National Bureau of Standards
Washington, D.C. 20234

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PREFACE

The Semiconductor Technology Program serves to focus NBS efforts to enhance the performance, interchangeability, and reliability of discrete semiconductor devices and integrated circuits through improvements in measurement technology for use in specifying materials and devices in national and international commerce and for use by industry in controlling device fabrication processes. Its major thrusts are the development of carefully evaluated and well documented test procedures and associated technology and the dissemination of such information to the electronics community. Application of the output by industry will contribute to higher yields, lower cost, and higher reliability of semiconductor devices. The output provides a common basis for the purchase specifications of government agencies which will lead to greater economy in government procurement. In addition, improved measurement technology will provide a basis for controlled improvements in fabrication processes and in essential device characteristics.

The Program receives direct financial support principally from three major sponsors: the Defense Advanced Research Projects Agency (ARPA),* the Defense Nuclear Agency (DNA),† and the National Bureau of Standards (NBS).× The ARPA-supported portion of the Program, Advancement of Reliability, Processing, and Automation for Integrated Circuits with the National Bureau of Standards (ARPA/IC/NBS), addresses critical Defense Department problems in the yield, reliability, and availability of integrated circuits. The DNA-supported portion of the Program emphasizes aspects of the work which relate to radiation response of electron devices for use in military systems. There is considerable overlap between the interests of DNA and ARPA. Measurement oriented activity appropriate to the mission of NBS is a critical element in the achievement of the objectives of both other agencies.

Essential assistance to the Program is also received from the semiconductor industry through cooperative experiments and technical exchanges. NBS interacts with industrial users and suppliers of semiconductor devices through participation in standardizing organizations; through direct consultations with device and material suppliers, government agencies, and other users; and through periodically scheduled symposia and workshops. In addition, progress reports, such as this one, are regularly prepared for issuance in the NBS Special Publication 400 sub-series. More detailed reports such as state-of-the-art reviews, literature compilations, and summaries of technical efforts conducted within the Program are issued as these activities are completed. Reports of this type which are published by NBS also appear in the Special Publication 400 sub-series. Announcements of availability of all publications in this sub-series are sent by the Government Printing Office to those who have requested this service. A request form for this purpose may be found at the end of this report.

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* Through ARPA Order 2397, Program Code 4D10 (NBS Cost Center 4259555).

† Through Inter-Agency Cost Reimbursement Order 74-811 (NBS Cost Center 4259522).

× Through Scientific and Technical Research Services Cost Centers 4251126, 4252128, and 4254115.

SEMICONDUCTOR MEASUREMENT TECHNOLOGY

QUARTERLY REPORT
April 1 to June 30, 1974

Abstract: This quarterly progress report describes NBS activities directed toward the development of methods of measurement for semiconductor materials, process control, and devices. The emphasis is on silicon device technologies. Principal accomplishments during this reporting period include (1) identification of surface preparation procedures which improve the quality of spreading resistance measurements, (2) preparation of a videotaped tutorial discussion of thermally stimulated current and capacitance measurements, (3) completion of an analysis of the apparent position of an opaque edge when viewed with incoherent and coherent illumination, and (4) completion of the construction of a flying-spot scanner. Results are also reported on capacitance-voltage and two-probe resistivity measurements; analyses of thermally stimulated current and capacitance measurements on metal-oxide-semiconductor (MOS) capacitors; a review of methods for characterizing interface states associated with thin oxide films on silicon; fabrication of a test pattern based on the charge-coupled device; a preliminary comparison of filar and image shearing eyepieces for line-width measurement; a review of technologies in use for photomask inspection and measurements; procedures for determination of correct photoresist exposure; epitaxial layer thickness; scanning electron microscopy; mathematical modeling of ultrasonic bonding; leak test procedures; thermal resistance measurements on transistors and Darlington pairs; and transistor thermal response measurements. Supplementary data concerning staff, publications, workshops and symposia, standards committee activities, and technical services are also included as appendices.

Key Words: Boron redistribution; Darlington pairs; dopant profiles; electrical properties; electronics; epitaxial layer thickness; flying-spot scanner; gold-doped silicon; hermeticity; measurement methods; microelectronics; micrometrology; MOS devices; oxide films; photomasks; photoresist; resistivity; scanning electron microscopy; semiconductor devices; semiconductor materials; semiconductor process control; silicon; spreading resistance; test patterns; thermal resistance; thermal response; thermally stimulated capacitance; thermally stimulated current; ultrasonic bonding; voltage contrast mode; wire bonds.

1. INTRODUCTION

This is a report to the sponsors of the Semiconductor Technology Program on work during the twenty-fourth quarter of the Program. It summarizes work on a wide variety of measurement methods for semiconductor materials, process control, and devices that are being studied at the National Bureau

of Standards. The Program, which emphasizes silicon-based device technologies, is a continuing one, and the results and conclusions reported here are subject to modification and refinement.

The work of the Program is divided into a number of tasks, each directed toward the study of a particular material or device property or measurement technique. This report is subdivided according to these tasks. Highlights of activity during the quarter are given in section 2. Subsequent sections deal with each specific task area. References cited are listed in the final section of the report.

The report of each task includes a narrative description of progress made during this reporting period. Additional information concerning the material reported may be obtained directly from individual staff members identified with the task in the report. The organization of the Program staff and telephone numbers are listed in Appendix A.

Background material on the Program and individual tasks may be found in earlier quarterly reports as listed in Appendix B. From time to time, publications are prepared that describe some aspect of the program in greater detail. Current publications of this type are also listed in Appendix B. Reprints or copies of such publications are usually available on request to the author.

Communication with the electronics community is a critical aspect both as input for guidance in planning future program activities and in disseminating the results of the work to potential users. Formal channels for such communication occur in the form of workshops and symposia sponsored or co-sponsored by NBS. Currently scheduled seminars and workshops are listed in Appendix C. In addition, the availability of proceedings from past workshops and seminars is indicated in the appendix.

An important part of the work that frequently goes beyond the task structure is participation in the activities of various technical standardizing committees. The list of personnel involved with this work given in Appendix D suggests the extent of this participation. In most cases, details of standardization efforts are reported in connection with the work of a particular task.

Technical services in areas of competence are provided to other NBS activities and other government agencies as they are requested. Usually these are short-term, specialized services that cannot be obtained through normal commercial channels. To indicate the kinds of technology available to the Program, such services provided during the period covered by this report are listed in Appendix E.

2. HIGHLIGHTS

Particularly significant accomplishments during this reporting period include (1) identification of surface preparation procedures which improve the quality of spreading resistance measurements, (2) preparation of a videotaped tutorial discussion of thermally stimulated current and capacitance measurements, (3) completion of an analysis of the apparent position of an opaque edge when viewed with incoherent and coherent illumination, and (4) completion of the construction of a flying-spot scanner.

In addition, a Symposium on Spreading Resistance was held in June at NBS, Gaithersburg under the joint sponsorship of NBS and ASTM Committee F-1 on Electronics. At the symposium, 90 participants representing 53 organizations from seven countries heard 24 papers which demonstrated that the spreading resistance technique, first utilized in the semiconductor industry more than 10 years ago, is beginning to receive wide acceptance as a measurement tool and is now appreciated as a method offering both high spatial resolution and great flexibility in terms of the variety and complexity of semiconductor structures to which it can be applied. The proceedings of the symposium are being published separately. See Appendix C for a summary of this and other dissemination activities.

Highlights of progress in technical task areas are listed below.

Resistivity; Dopant Profiles — A significant advance was made in the understanding of the influence of surface preparation techniques on spreading resistance measurements, and several improved procedures for preparing polished surfaces suitable for making spreading resistance measurements were identified. It appears to be possible to trace a variety of previously encountered problems to the aqueous nature of the polishing medium. To obtain stable surfaces, water residues must be thoroughly removed or non-aqueous polishing media employed.

Junction capacitance-voltage measurements were made on a series of diodes of four different sizes formed by diffusion into a uniformly doped wafer. These measurements were made in an experiment to test the various correction factors applied in the algorithm for reducing capacitance voltage data. Since these factors depend strongly on the area-to-periphery ratio, it is important to establish their validity over a range of diode sizes of interest. Satisfactory results were achieved.

Further progress was made in the analysis of the boron redistribution problem and the results of an interlaboratory evaluation of the two-probe method for measuring resistivity of silicon crystals, conducted in cooperation with ASTM Committee F-1, were analyzed and reported.

Initial attempts were made to profile the middle layer of a three layer structure, equivalent to profiling the base of a transistor, by means of the junction capacitance-voltage method. Difficulties not accounted for by the models being used to analyze the data were encountered and are being further investigated. Work on the reevaluation of Irvin's curves

which relate resistivity to impurity density was directed this quarter primarily toward development of the fixture suitable for automated differential sheet resistance measurements.

Crystal Defects and Contaminants — The physical model which had been developed to predict the dynathermal current and capacitance response of the gold acceptor center in silicon was improved by incorporating a more complete expression for the depletion width in an MOS capacitor. This improvement will facilitate the extension of the model to other impurities and defect centers.

As an experiment in new forms of dissemination of information, a 35-minute tutorial videotape, Defects in *p-n* Junctions and MOS Capacitors Observed using Thermally Stimulated Current and Capacitance Measurements, was produced late in the quarter. This full color videotape is available for distribution on loan without charge. As an added feature, arrangements can be made for the author to be available for a telephone conference call to answer questions and provide more detailed information, following a prearranged showing of the videotape.

Oxide Film Characterization — Three electrical techniques for measuring interface state densities were analyzed and compared. Preliminary measurements were made to test sodium contamination levels of various processing materials. A detailed review of the sensitivities, sampling volumes, and other characteristics of various surface analysis techniques was undertaken. Study of ion microprobe mass analysis and x-ray photoelectron spectroscopy continued along previously reported lines.

Test Patterns — Design work for the charge coupled device test structures, being conducted at the Naval Electronics Laboratory Center, has been completed and the mask set prepared. In addition analysis of the charge coupled device in several operating modes has been initiated to establish the algorithms necessary to extract the desired parameter information from the experimental measurements.

Photolithography — Visits to an additional 15 device manufacturers, photomask and photoresist suppliers, and manufacturers of mask alignment or inspection equipment confirmed the four major problem areas previously identified: line width measurement, edge definition, mask and photoplate inspection, and mask registration. Initial efforts in the next phase of this work include a study to quantify the effects responsible for obtaining different dimensional measurements on the same artifact when using a filar or image shearing eyepiece and a thorough analysis of the various technologies now being used or proposed for use to automatically inspect photomasks for defects, pattern errors, or registration faults. This work is being conducted in cooperation with the Lawrence Livermore Laboratory. The photomask industry has particularly emphasized the importance of development by NBS of standards for line width measurements at the 1 μm level.

An analysis of the apparent position of an opaque edge of ideal geometry when viewed through a microdensitometer showed that the true edge was at the half power point for incoherent illumination and at the quarter power point for coherent illumination.

Epitaxial Layer Thickness — Preliminary comparisons were made between the step-relaxation method, one of two thickness measurement methods based on use of the transient high-frequency capacitance-voltage characteristic of an MOS capacitor, and the infrared reflection and spreading resistance methods.

Wafer Inspection and Test — Work was completed on the assembly of the flying-spot scanner intended to evaluate electrical properties of devices before and after exposure to the electron beam of the scanning electron microscope. In addition, a cylindrical detector intended to increase the sensitivity of the scanning electron microscope in the voltage contrast mode was assembled and installed.

Interconnection Bonding — The effort on mathematical modeling of the motion of an ultrasonic wire bonding tool, undertaken to determine the mechanisms by which the metallurgical weld is formed and to lay the basis for a quantitative in-process monitoring scheme, resulted in an analysis which qualitatively predicts the normalized vibration amplitude of a variety of bonding tools of different sizes and materials.

Hermeticity — Interlaboratory evaluation of the helium mass spectrometer and radioisotope techniques for measurement of fine leaks are being conducted in cooperation with ASTM Committee F-1. Preliminary evaluation of the novel procedure for a dry, quantitative gross leak test began. A sensitive mass spectrometer was constructed for use in evaluating this type of instrumentation for the measurement of trace elements in the semiconductor processing environment and on wafer surfaces as well as for the investigation of gas flow mechanisms in leaks in hermetic packages.

Thermal Properties of Devices — An analysis showed that the overlap diode model can be used to explain several experimental observations of differences between apparent thermal resistance as measured with the emitter-base and collector-base junction voltages as temperature sensitive parameters on wide-base and narrow-base transistors. Preliminary measurements of thermal resistance were made on commercial Darlington circuits.

A one dimensional model for power transistor cooling was shown to predict transient thermal response for periods up to 250 μs. With the model, it is possible to estimate both average junction temperature and area of power generation at steady state from experimental measurements of the cooling curve.

Impact of Automation on Measurement Requirements — Initial efforts have begun on a study of automated integrated circuit processing and assembly contracted to Arthur D. Little. This work is intended to provide additional criteria for selection of priorities to be assigned in connection with measurement method development in the program. Initial results suggest that considerable attention should be directed toward routinely used wafer measurements: sheet resistance; thickness of oxide, epitaxial or diffused layers; visual inspection; and capacitance-voltage.

3. RESISTIVITY; DOPANT PROFILES

3.1. Spreading Resistance Methods

Surface preparation procedures which improve the quality of spreading resistance measurement have been identified [1]. Erratic behavior and poor reproducibility had been observed, especially on *p*-type specimens with resistivity greater than 1 Ω·cm, when constructing calibration curves for use with the spreading resistance instrument (NBS Tech. Note 806, pp. 9-10). Later in measuring radial resistivity profiles of the 10 Ω·cm *p*-type wafers intended for use as one of the set comprising Standard Reference Material 1520 (NBS Tech. Note 806, p. 66), it was found that the spreading resistance method gave much greater variability (on a macroscopic scale) than either the four-probe method suitably corrected for off-center measurement [2] or the photovoltaic method [3]. During the present quarter, unexpectedly large level shifts in spreading resistance were observed on beveled 10 Ω·cm *p*-type specimens between the freshly polished bevel surface and the unpolished original top surface.

In all cases, the surfaces had been chem-mechanically polished with an aqueous based silica sol [4]. A series of experiments was carried out on beveled specimens similar to those on which the level shifts had been observed. After polishing, the specimens were bathed or swabbed in a solution of hydrofluoric acid, chromic acid, ammonium hydroxide, or ammonium hydroxide and hydrogen peroxide but in no case was there reasonable agreement between the spreading resistance value on the beveled surface and that on the original top surface. Baking out the specimen at 70 to 100°C under partial vacuum for 15 min also failed to resolve the discrepancy. Comparison of these observations with those of members of other laboratories led to the recommendation* that the bakeout temperature be at least 150°C.

This higher temperature bakeout treatment in partial vacuum was applied for 15 min to specimens that had been bevel polished with silica aquasol and other polishing materials with the results that the spreading resistance value did not change significantly from one side of the bevel vertex to the other and it also corresponds with the resistivity as measured by the four-probe method [5]. An example of these results is shown in figure 1. In related experiments it was also observed that polishing media which are not aqueous based do not require the high temperature bakeout; this observation is in good agreement with those of Mayer and Schwartzmann [6].

After the wafers were baked at 150°C for 15 min the scatter around the calibration curve regression line was considerably reduced. This is illustrated in figure 2 where the ratio of spreading resistance to resistivity as measured by the four-probe method is plotted against the resistivity.

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* A. Mayer, RCA, Somerville, New Jersey 08876 (private communication).

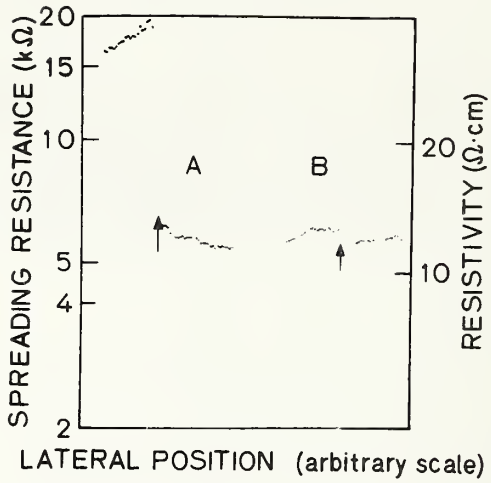

Figure 1. Spreading resistance of a 10 Ω·cm p-type silicon specimen bevel polished with silica aquasol. (A: Not baked out; B: Baked out after polishing. In each case, the arrow indicates the position of the bevel vertex.)

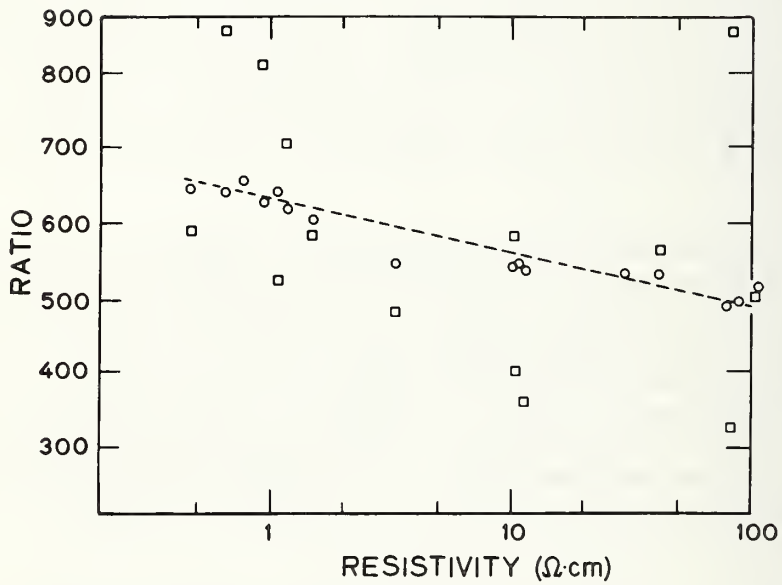

Figure 2. Ratio of spreading resistance to four-probe resistivity for p-type silicon wafers polished with silica aquasol. (□: Not baked out; ○: Baked out after polishing.)

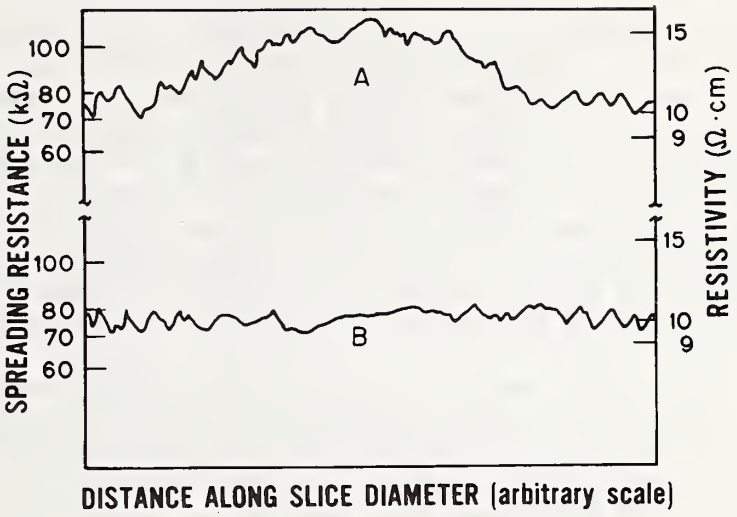

Figure 3. Radial resistivity profile of a 10 Ω·cm *p*-type silicon wafer polished with silica aquasol. (A: Not baked out; B: Baked out after polishing.)

It should be noted that this mode of presentation enhances departures from the line of regression which might be lost in the conventional log-log plot of spreading resistance against resistivity.

A 15 min bakeout at 160°C also improved the quality of macroscopic radial resistivity profiles determined by the spreading resistance method as illustrated in figure 3. For this wafer the profile as measured by either four-probe and photovoltaic techniques showed variation of less than ±5 percent. The upper plot in the figure which was taken along a diameter after polishing but before bakeout shows an apparent variation of about 50 percent, but after the bakeout the variation is reduced to that of the other methods as shown in the lower plot.

Although the mechanism for the observed surface effects is not fully understood, it is probably associated with the aqueous nature of the polishing media. Such effects may be reduced by variation of polishing conditions such as loading, rate of surface feed, or the nature of the polishing substrate, but bakeout after polishing has been shown to remove the effects almost completely. It must be noted that the magnitude of the effects may be related to conductivity type or resistivity level or both. Hence, isolated experiments on a limited number of specimens may be inadequate to characterize a particular polishing process for the full spectrum of specimen types which may eventually be encountered. (J. R. Ehrstein)

3.2. Junction Capacitance-Voltage Method

An experiment was carried out to obtain a preliminary assessment of the adequacy of available peripheral [7,8] corrections for use in deducing dopant density from capacitance-voltage measurements on gated p^+n junction diodes of different sizes. The experiment involved analysis of capacitance-voltage data taken on the four gated p-n junction diode test structures on test pattern NBS-2 (NBS Tech. Note 788, pp. 15-17) [10]. Three of these structures (Nos. 1, 6, and 9) are circular, with diameters of 6, 20, and 60 mils (0.15, 0.5, and 1.5 mm), respectively; the fourth (No. 4) is square, 18 mils (0.44 mm) on a side. The pattern is repeated every 200 mils (5.08 mm) in both directions over the wafer.

Measurements were made on wafer 575, an initially homogeneous 10 Ω•cm, n-type wafer, which was selected after preliminary measurements indicated that the dopant density was relatively independent of depth and that the flat-band voltage was fairly constant over the wafer surface. Measurement was attempted on each gated p-n junction of the four types on the slice. Reverse bias voltages of 2, 5, 10, and 20 V were applied. At each voltage the capacitance was measured with the gate biased at -6.7 V which represented a nominal value of flat-band voltage for the wafer. The dimensions of three to five diodes of each type were measured on photomicrographs and an average diameter or width was calculated for each type. An area was calculated from this average diameter or width for use in all dopant density calculations for each type of diode.

Because of gate-to-substrate shorts, gate-to-diffused layer shorts, or excessive leakage, not all devices could be measured. Three values of dopant density were computed for each measurable diode by using differences in capacitance measured at 2 and 5 V, 5 and 10 V, and 10 and 20 V. The peripheral correction for the circular junctions was performed using eq (3) of [7] assuming $W_2 = W_t$ and $W_1 = 0$ as defined therein. The peripheral correction for the square junction was performed using eq (16) of [8] making similar assumptions. Diffused layer corrections [9] were also applied. The average and the percent relative sample standard deviation of the three dopant density values were calculated for each measurable diode, and a map of the average values was made as shown in figure 4. The groups of four in the figure represent the four diodes within a cell of the test pattern. The dashes denote diodes which could not be measured. Values in parentheses indicate that a measurement was made but that it was rejected because of excessive deviation from the average or excessive scatter.

On the map of figure 4 there are twelve squares in which all four diodes were measurable. These 48 diodes constituted a statistical population which was subjected to analysis to determine whether on the average all diode geometries gave the same dopant density values. The grand average dopant density, N, calculated for each diode type, is listed in table 1. All four values of N fall within a range less than 3 percent of the

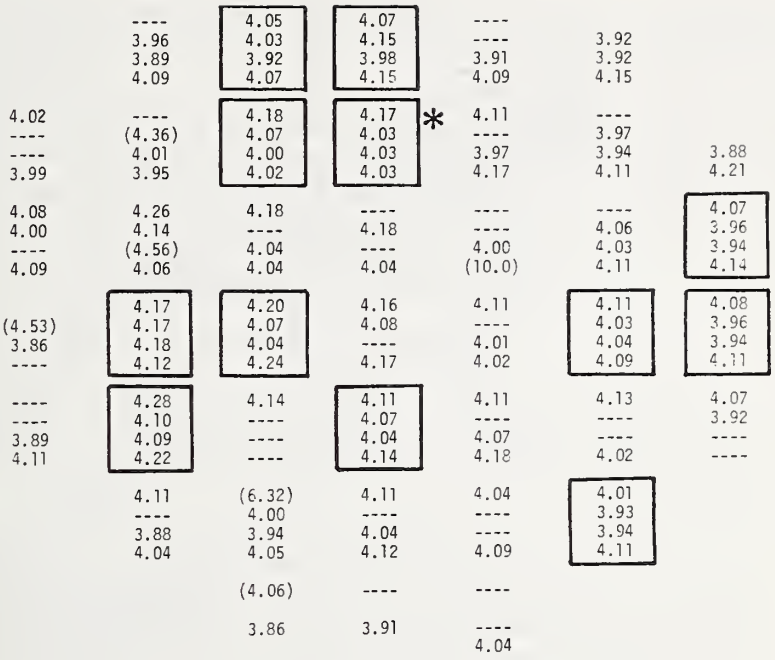

Figure 4. Wafer map of average dopant density derived from capacitance-voltage measurements. (Each group of four numbers represents measurements made within a unit cell of test pattern NBS-2 on slice 575. Dopant densities as measured on structures 4, 9, 6, and 1 are listed from top to bottom in each group. The boxed data were used in the statistical analysis described in the text. The data of figure 5 were taken on the cell marked with an asterisk.)

Table 1 — Oopant Oensity Profiles from Capacitance-Voltage Measurements

Diode Type	N, cm^{-3}	S_N, %	N_1, cm^{-3}	N_3, cm^{-3}	Δ, %
4	4.13×10^{14}	0.82	4.10×10^{14}	4.16×10^{14}	1.46
9	4.05	1.20	4.01	4.10	2.30
6	4.01	1.14	3.97	4.06	2.22
1	4.12	0.64	4.11	4.13	0.54
All	4.08	0.95	4.05	4.11	1.63

overall grand average for all 48 diodes listed in the bottom line of the table. For the same population, the percent relative sample standard deviations for each type were averaged to obtain the values S_N listed in table 1. Most of the variability was due to the fact that there was a systematic increase in calculated dopant density as the reverse bias was increased. To examine this systematic increase the dopant densities computed from measurements at 2 and 5 V and at 10 and 20 V were averaged for each diode type to obtain N_1 and N_3, respectively. These values are listed in table 1 together with Δ, the percent increase of N_3 over N_1. Except for the case of the 6-mil diodes, S_N is only 50 to 60 percent of Δ. For the 6-mil diodes, S_N is greater than Δ which suggests that in this case S_N is dominated by random error (such as that introduced by stray capacitance) rather than the systematic increase. This is not unexpected since stray capacitance is a more significant error source for the smaller diodes.

To demonstrate the need for the peripheral correction, the capacitances of the four diodes in the cell indicated by an asterisk in figure 4 were measured for reverse biases of 0, 0.5, 1, 2, 3, 5, 7, 10, 14, 20, 27 and 35 V and the dopant density was calculated for each adjacent pair of capacitance values with and without the peripheral correction applied. The results are shown in figure 5. For this experiment the measuring system was modified such that the meters for reading the capacitance and bias voltage were powered through line voltage regulators to suppress noise and the digital voltmeter for reading the output of the capacitance meter was operated in a filtered mode to achieve resolution to four significant figures. In addition the calculations were made with values of area calculated from the measured dimensions of each diode in the cell rather than from the averaged dimensions used in the previously described analysis. The diffused layer correction was applied throughout. The particularly good agreement of the corrected profiles of the 18-, 20- and 60-mil diodes is evident. The corrected profile of the 6-mil diode is about 5 percent below the other three. This discrepancy might arise because the peripheral capacitance comprises a comparatively large percentage of the measured capacitance in the case of the 6-mil diodes as indicated in table 2. The fact that a one-sided junction is assumed in calculating the peripheral capacitance leads to a systematic error which is greatest when the peripheral capacitance is a significant fraction of the measured capacitance. There is also a discrepancy between the dopant densities of figures 4 and 5 for the particular diodes in question. This discrepancy is due in part to the fact that different areas were used to obtain the values of dopant density presented in the two figures and in part to differences in the experimental set ups. The relative importance of these two causes may be assessed by examining table 3 in which are shown the dopant densities as determined using both measuring systems and both sets of area values. As expected, the differences in area result in identical shifts for both measuring systems. The variation between measuring systems

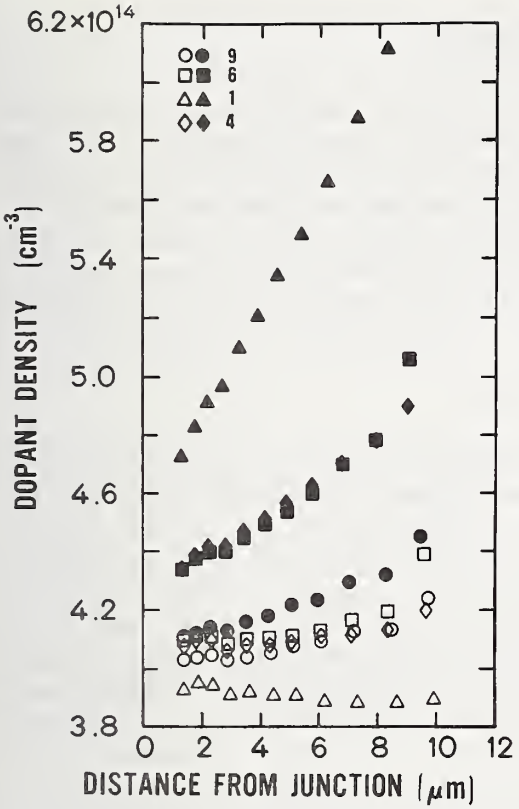

Figure 5. Apparent dopant density determined from capacitance-voltage measurements with (open data points) and without (solid data points) application of the peripheral correction. (The diffused layer correction was applied in both cases. Measurements were made on the cell marked with an asterisk in figure 4.)

Table 2 — Ratio of Peripheral Capacitance to Measured Capacitance

Diode Type	C_p/C_m, %
4	5.98
9	1.88
6	5.43
1	16.28

Table 3 — Dopant Density from Capacitance-Voltage Measurements Taken and Analyzed in Different Ways

	Measuring System #1 (fig. 4)		Measuring System #2 (fig. 5)	
Diode Type	Average Dimension	Individually-Measured Dimension	Average Dimension	Individually-Measured Dimension
4	4.16×10^{14} cm^{-3}	4.18×10^{14} cm^{-3}	4.07×10^{14} cm^{-3}	4.09×10^{14} cm^{-3}
9	4.00	4.04	4.03	4.07
6	4.00	4.17	3.94	4.11
1	4.05	4.01	3.95	3.91

appears to be random and may be due as much to other sources of random error as to changes in the measuring system.

Considering the experimental conditions and uncertainties which have been discussed, it may be tentatively concluded that dopant densities can be calculated from junction C-V data which are precise to within a few percent independent of geometry for diodes having geometries similar to those which have been studied. Confirmation of this conclusion requires collection and analysis of a larger amount of data.

(R. L. Mattis and M. G. Buehler)

3.3. Mathematical Models of Dopant Profiles

Starting with appropriate initial concentrations $C_1(z, 0)$ and $C_2(y, 0)$ at time $t = 0$, and appropriate boundary conditions, the Volterra integral equations discussed previously (NBS Spec. Publ. 400-4, pp. 9-11) were solved for the two unknown heat potentials $Q(\tau)$ and $R(\tau)$ in the infinitesimal dimensionless time interval $\Delta t = \tau_2 - \tau_1$ where $\tau_1 = 0$. Next, from the definitions of $C_1(z, t)$ and $C_2(y, t)$ in terms of $Q(\tau)$ and $R(\tau)$, the values of $C_1(z, \Delta t)$ and $C_2(y, \Delta t)$ in their appropriate domains were calculated. By using these quantities as new initial distributions and repeating the previous cycle of computations the values of $C_1(z, t)$ and $C_2(y, t)$ were calculated at times $2\ \Delta t$, $3\ \Delta t$, . . . These values of the concentrations were then compared with the known exact solutions of Grove, Leistiko and Sah [11]. The comparison showed good agreement in the interior of each domain but the values of C_1 and C_2 at the moving boundary drifted uniformly upward instead of remaining constant as they should have. The instability seemed to be inherently connected with the fact that $C_1(y, t)$ and $C_2(z, t)$ were being computed and used in each cycle of the computations. A modified program has been written in which only the initial values of $C_1(y, t)$ and $C_2(z, t)$ are used to compute $Q(\tau)$ and $R(\tau)$ for all times Δt, $2\ \Delta t$, . . . The new program, written in FORTRAN, is being debugged. (S. R. Kraft* and M. G. Buehler)

3.4. Two-Probe Method

The results of an interlaboratory round-robin evaluation of a two-probe method for measuring resistivity of cylindrical ingots were analyzed. The round robin had been conducted by ASTM Committee F-1 on Electronics which developed the test method [12]. Eight cylindrical silicon crystals with room temperature resistivity in the range 9×10^{-4} to 4×10^{3} $\Omega \cdot$cm were used in the round robin. Each participating laboratory was asked to make five independent measurements for each of two orientations 90 deg apart around the circumference at each of 11 lengthwise positions on each

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crystal. Five laboratories participated. One reported data as required, the second reported five measurements per position which not only did not seem to be independent but also exhibited apparent transcription errors, the third reported only an apparent average value at each position on only five of the crystals, the fourth produced some data useful for comparison but these data were not complete enough to be used in the analysis, and the fifth produced no usable data. It is not certain that the positions were numbered from the same end by each laboratory. It is assumed that the orientations were held constant for each crystal by any one participant, but that they differed from laboratory to laboratory for the same crystal. In most cases, the number of significant figures reported varied from laboratory to laboratory.

Since the method of test centers on the average of five measurements for any one position, it would have been preferable to analyse the round robin in terms of such averages. However, because of the way in which data were reported from the several laboratories, it was judged that analysis in terms of the median of a set of five readings would be more reliable. For sample size five, from normal distribution, the variability of medians is only slightly larger than that of means, and median values are much less sensitive to outliers. Of course, for the laboratory reporting only averages, the average value had to be substituted for the median.

In the following discussion, the crystals are numbered 1 to 8 in order of increasing resistivity. Analysis was based on data from crystals as follows: from crystals 1, 2, and 3: two labs, eleven positions, and two orientations; from crystals 4, 5, 6, 7, and 8: three labs, eleven positions, and two orientations. This data base, though meager, was adequate to estimate the variability of the method.

One way analyses of variance were done for each crystal, to check for significant differences between laboratory-orientation combinations. There were eleven measurements (positions) for each class (laboratory-orientation). Statistically significant differences were observed in half the crystals; these were investigated further in subsequent analyses.

Separate two way analyses for laboratory and lengthwise position effects were run for each crystal, with both orientations being averaged at each position. A significant lengthwise position effect was observed on all crystals except crystals 5 and 8, and a moderately significant laboratory effect was observed on all crystals except crystals 5 and 7. Residuals from these two way analyses normalized to the means cover a range of one order of magnitude in a reasonably random fashion, whereas the absolute resistivity values of specimens spanned 6 1/2 orders. This suggests that the random variability increases with resistivity and that variability expressed as a percentage of the mean might be expected to be reasonably constant.

Table 4 — Analysis of Two-Probe Resistivity Round Robin

Crystal	Grand Average Resistivity, Ω·cm	Difference of Lab Average from Grand Average, %			Range of Lab Averages, percentage points	Estimate of Standard Deviation, %	Difference from Grand Average, %	
		Lab 1	Lab 2	Lab 3			of Lowest Position Average	of Highest Position Average
1	0.000929	-0.23	+0.23	-----	0.46	1.9	- 3.4	+ 6.2
2	0.0163	+0.15	-0.15	-----	0.30	1.2	- 2.5	+ 3.6
3	0.128	-0.20	+0.20	-----	0.40	1.6	- 3.8	+ 2.8
4	1.55	-0.07	-0.60	+0.67	1.27	3.6	- 1.4	+ 1.4
5	11.7	-0.57	-0.65	+1.22	1.87	5.3	- 1.9	+ 4.5
6	155.	+0.40	-0.65	+0.25	1.05	2.9	- 2.0	+ 1.0
7	1007.	-0.20	+0.70	-0.50	1.20	3.3	-12.	+31.
8	3190.	+3.0	+3.9	-6.9	10.8	30.	- 3.2	+ 5.1

Regressions were done against position, for each laboratory and each crystal, to see if the position differences were consistent over laboratories. Residuals from low-order polynomial fits were remarkably similar across laboratories, indicating that there were definite position effects. The specific order of polynomal is not important; the significant result is that the resistivity is a smooth function of lengthwise position and its variation is large compared to inherent measurement variability. That is, the lengthwise variations are real, not artifacts of data scatter masked by a paucity of laboratories.

For each crystal, the average of all measurements made by each laboratory was computed. A grand average of these laboratory averages was also calculated for each crystal. These are listed in column 2 of table 4. The percent deviations of the laboratory averages from the grand average are listed in columns 3 to 5 of the table. The range of these deviations, listed in column 6 of the table, was used for estimating the overall measurement variability of this method. The values for range can be converted into estimates of standard deviation by multiplying by the factors 0.86 and 0.59 for two-laboratory and three-laboratory data, respectively. Since the range values are based on averages of 22 individual medians (two orientations, eleven positions) it is necessary to multiply by an additional factor of $\sqrt{22}$ to obtain an estimate of the standard deviation for the individual medians of five measurements. These estimates are listed in column 7 of the table.

Crystal 8 required further investigation. Laboratory 3 showed significant negative bias for this crystal, position by position, as well as in average value. The average bias for laboratory 3 on this crystal with

respect to the average of the other two laboratories is -10.3 percent. Considering only the measurements by laboratories 1 and 2, the estimate of standard deviation of medians of five repetitions is reduced to less than 3 percent. However, if the data of laboratory 3 are retained but translated to remove the bias, and if the variability of the bias of each of the three laboratories is considered, the standard deviation is estimated to be approximately 10 percent.

On the basis of the data available, it seems reasonable to conclude that a laboratory similar to the participants in the experiment, working carefully, and taking the mean or median of five repetitions at one location on a crystal, will estimate the true resistivity with a standard deviation of 4 percent or less when the resistivity is 1000 Ω•cm or less, and with a standard deviation of about 10 percent for a resistivity in the neighborhood of 3500 Ω•cm.

Taking the calculations one step farther, one sees that the 3-sigma limits for the "true" value of resistivity at a given point are at ±12 percent from the mean of a set of five repetitions at that point, for resistivities up to 1000 Ω•cm, and at ±30 percent for resistivities near 3500 Ω•cm.

In addition, an estimate was made of the lengthwise variation of resistivity for each crystal. This was done by first taking the average of medians for both orientations and all laboratories at each lengthwise position of each crystal. The lowest and highest such averages are indicative of the lengthwise resistivity variation. These averages, expressed as percent differences from the grand average for the crystal, are listed in columns 8 and 9, respectively, of table 4.

Finally, an estimate was made of variability within one laboratory. For the set of data which was most complete, the ranges of the sets of five repetitions were calculated for each orientation and each position, for each ingot. These ranges were then averaged for each ingot, and converted to estimates of the standard deviation of a median or mean of five repetitions. The values obtained ranged from 0.04 percent to 0.5 percent, for crystals 1 to 7 and 1.3 percent for crystal 8. Eliminating the two positions on each end of crystal 8 reduced its value to 0.8 percent. Now 0.5 percent is markedly less than the several percent obtained when analyzing results from several laboratories. This is not surprising; in fact, it would be surprising if measurements taken by one laboratory did not cluster better than those taken by several different laboratories. It is, however, another justification for the word of caution about unexplained sources of variation that ought to accompany all precision statements, especially those involving only one laboratory or one experimenter or one technique. (J. R. Ehrstein and J. A. Lechner*)

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4. CRYSTAL DEFECTS AND CONTAMINANTS

4.1. Thermally Stimulated Current and Capacitance Measurements

The theoretical model for the dynathermal current and capacitance responses of an MOS capacitor reported previously (NBS Tech. Note 806, pp. 13-16, NBS Spec. Publ. 400-1, pp. 16-19, and NBS Spec. Publ. 400-4, pp. 27-33) has been solved numerically and the dynathermal current response plotted as a function of temperature. The numerical solution involves solving the transcendental expression for the depletion width W of an MOS capacitor. This can be computed by integration of the previously reported derivative equation [eq (11) of NBS Spec. Publ. 400-4, p. 31] with the constant of integration evaluated at time zero where W equals its initial phase I value. The resultant equation for an *n*-MOS capacitor is:

$$\left(\frac{\varepsilon_s X_o}{\varepsilon_o} + W_{IIf}\right) \ell n \left(\frac{W - W_{IIf}}{W_{Ii} - W_{IIf}}\right) = W_{Ii} - W + \left(\frac{\varepsilon_s X_o}{\varepsilon_o} + \frac{W_{IIf}}{2}\right) \ell n \left(\frac{N_d - N_t}{N_d - n_t}\right)$$

$$- \frac{\varepsilon_s X_o}{\varepsilon_o} \int_0^t \frac{p_t e_p \, dt}{(N_d - n_t)} + \frac{1}{2} \int_0^t \frac{W \frac{dn_t}{dt}}{(N_d - n_t)} \, dt \qquad (1)$$

where W_{Ii} is the depletion width at the beginning of phase I, W_{IIf} is the depletion width after phase II, ε_o is the dielectric constant of silicon dioxide, ε_s is the dielectric constant of silicon, X_o is the oxide thickness, p_t is the hole density at a defect center, e_p is the hole emission rate, n_t is the electron density at a defect center, N_t is the acceptor defect dopant density, and N_d is the donor dopant density. Temperature dependent terms are W, e_p, p_t, and n_t.

Values for W_{Ii} and W_{IIf} are obtained from measured values of capacitance:

$$W_{Ii} = \varepsilon_s A(C_{Ii}^{-1} - C_o^{-1})$$

and

$$W_{IIf} = \varepsilon_s A(C_{IIf}^{-1} - C_o^{-1})$$

where A is the area of the MOS capacitor and C_{Ii}, C_{IIf}, and C_o are the capacitances measured at the beginning of phase I, at the end of phase II, and with the capacitor forward biased into accumulation as shown in the

idealized curves in figure 6. Equation (1) was solved iteratively at various temperatures. At the lowest temperature the initial value of W was taken as W_{Ii}. This was inserted into the right-hand side of eq (1) and a new value for W was obtained. The process was repeated by substituting the previous value of W in the right-hand side of eq (1) and solving for a new value until successive values of W differed by less than 10^{-3} W. The process was then repeated for higher temperatures by using as the initial value of W the value found at the next lower temperature.

Plots of depletion width against temperature for the gold acceptor in an *n*-MOS silicon capacitor are shown in figure 7 for temperatures from 180 to 320 K. The heating rate β was taken as 10 K/s, C_o as 14.00 pF, C_{IIf} as 7.33 pF, and C_{Ii} as 3.20 pF. For curves A and B, the ratio N_d/N_t was taken as 25 while for curve C it was taken as 5. Curves B and C were computed from the complete equation. For curve A it was assumed that $(dn_t/dt) = 0$; in this case terms 3 and 5 on the right-hand side of eq (1) become zero.

Dynathermal current response of gold acceptors in an *n*-MOS capacitor was calculated from the previously reported equation [eq (12) of NBS Spec. Publ. 400-4, p. 31] for current. The quantity W was calculated from eq (1), e_n and e_p were calculated from previously reported expressions [eqs (6) and (7) of NBS Spec. Publ. 400-4, pp. 27, 29] and n_t and p_t were calculated from integral equations reported elsewhere [13]. Since eqs (7c) and (7d) of [13] greatly exceed the capability of calculators with only 12 significant figures, it was necessary to reformulate them in such a way that the magnitudes could be reduced by approximately the tenth root and that the values could be accumulated incrementally in order to avoid fatal round-off errors. Geometrical parameters were chosen to correspond with those of Device No. 2107.7 on which experimental dynathermal response has been reported (NBS Spec. Publ. 400-1, p. 17). Plots were made of current as a function of temperature for heating rates of 0.5, 1, 2, 5, and 10 K/s. The general shape of the curves agrees very well with the experimental curves obtained on Device No. 2107.7. Comparisons of the theoretical and experimental phase I and phase II emission temperatures have been given previously (NBS Spec. Publ. 400-4, pp. 32-33) as plots of heating rate against emission temperature. The peaks of the theoretical current response are in excellent agreement with the theoretical plot of heating rate against phase II emission temperature.

(W. E. Phillips and M. G. Buehler)

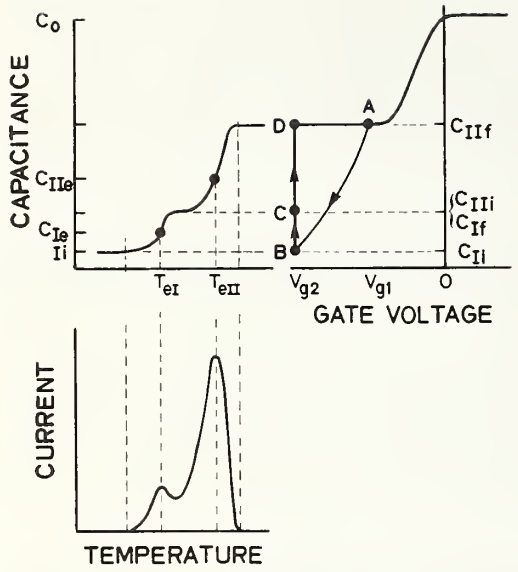

Figure 6. Capacitance-voltage characteristic and dynathermal current and capacitance response of an ideal, gold-doped n-MOS capacitor.

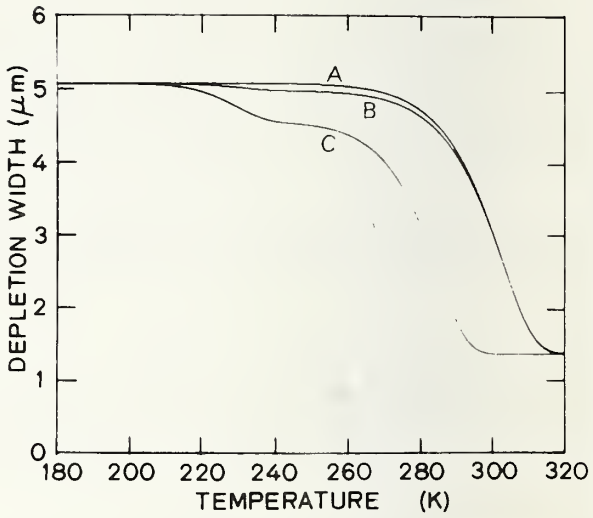

Figure 7. Calculated depletion width of a gold-doped silicon n-MOS capacitor during dynathermal response measurements. (See text for a discussion of conditions for each curve.)

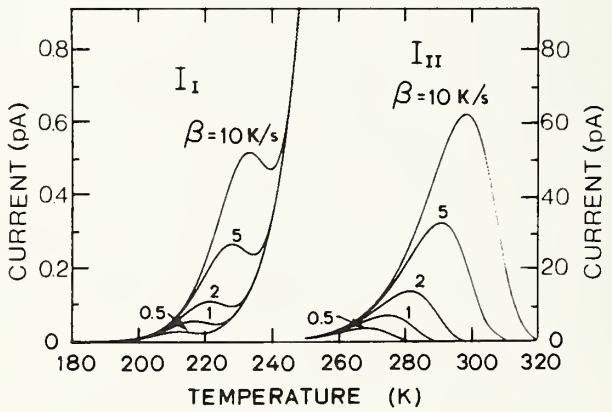

Figure 8. Calculated phase I and phase II dynathermal current response to gold acceptors in a silicon n-MOS capacitor for various heating rates.

5. OXIDE FILM CHARACTERIZATION

5.1. Measurement of Interface State Density

Electronically active defects located near the interface of a silicon-silicon dioxide structure give rise to various effects, such as carrier trapping and injection, which can degrade device performance. These interface states are known as fast states* because they can readily exchange charge with the bulk silicon. These states can be characterized by their charge, their capture cross section, and their density and distribution in energy across the band gap of silicon.

Three techniques for measuring the interface state density and energy distribution were reviewed. Each of these techniques involves the measurement of characteristics of MOS capacitors: the low frequency capacitance-voltage (C-V) characteristic, the temperature dependence of the high frefrequency C-V characteristic, or the frequency and bias dependence of the conductance.

Use of the low frequency C-V characteristic to determine interface state densities was first suggested by Berglund [14]. The basic assumption is that the a-c test frequency is low enough that all interface states remain in thermal equilibrium. Consider the band diagram and equivalent circuit for the MOS capacitor in figure 9. The oxide capacitance, semiconductor depletion capacitance, and the surface state capacitance, all per unit area, are shown as C_o, C_D, and C_{ss}, respectively; C is the total measured capacitance per unit area. There are no loss elements since it is assumed that the surface states and the semiconductor space charge are in equilibrium. The d-c bias, V, applied to the MOS capacitor results in a surface potential, ψ_s; the Fermi energy, E_F, is constant throughout the structure. The interface state density, N_{ss}, is shown schematically on the band diagram. For any given surface potential only the interface states near the Fermi energy communicate with the bulk silicon. Therefore, by sweeping the Fermi energy across the gap (by varying the applied potential which, in turn, varies the surface potential) it is possible to determine the distribution of interface states in the forbidden gap.

From the equivalent circuit, it is evident that:

$$C_{ss} = \left(\frac{C}{1 - \frac{C}{C_o}} - C_D \right) .$$

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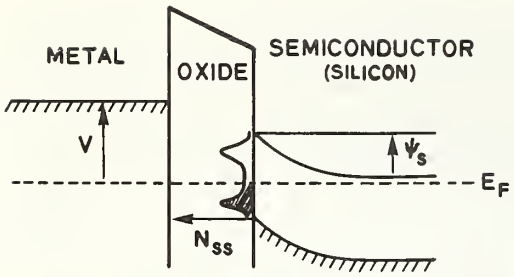
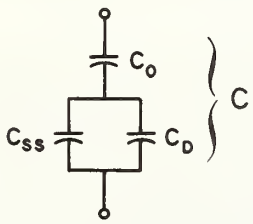
* The term, fast state, is a relative notion since a state which is fast at room temperature (i.e., which can readily exchange charge with the bulk) may not be fast at low temperature.

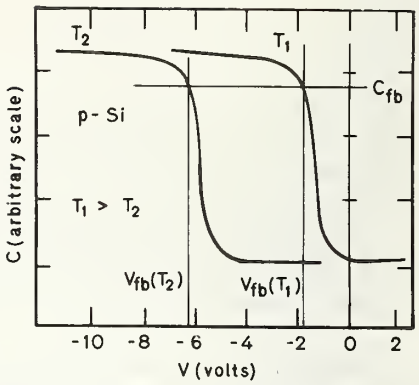


a. Energy band diagram.

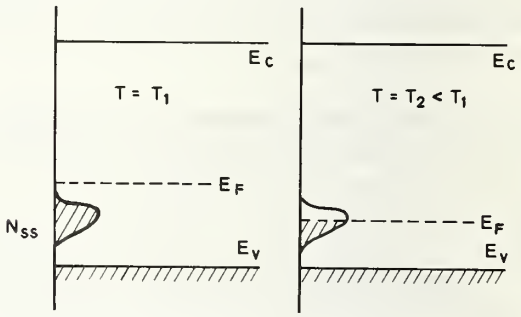


b. Equivalent circuit.

Figure 9. Representations of an MOS capacitor in the low frequency approximation. (See text for discussion of symbols.)



a. High frequency capacitance-voltage curves which show shift in flat-band voltage.



b. Silicon energy band diagram which shows shift in Fermi energy.

Figure 10. Effect of temperature on properties of a p-MOS capacitor. (See text for discussion of symbols.)

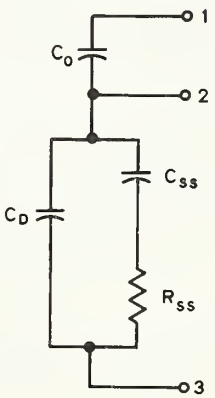


Figure 11. Equivalent circuit used for the analysis of the conductance technique. (See text for discussion of symbols.)

Since C_o is determined by biasing the capacitor into accumulation, the first term in the brackets is explicitly determined from the experimental C-V characteristic. Given the dopant density, and the area and oxide thickness of the capacitor, $C_D(\psi_s)$ can be calculated [15]. Note that C_D is a function of ψ_s while C is a function of V. Therefore, it is also necessary to develop a relationship between ψ_s and V. Berglund [14] showed that:

$$\psi_s(V_1) - \psi_s(V_2) = \int_{V_1}^{V_2} \left(1 - \frac{C(V)}{C_o}\right) dV. \qquad (2)$$

Except for the constant of integration, the potential can be calculated simply from the experimental data. The integration constant is determined by comparing the potential curve calculated from eq (2) with the potential curve calculated from ideal C-V characteristics [15]. It is thus possible to relate the interface state density to the low frequency capacitance, $C(\psi_s(V))$:

$$N_{ss}(\psi_s) = \frac{C_{ss}(\psi_s)}{q} = \frac{1}{q}\left(\frac{C(\psi_s(V))}{1 - \dfrac{C(\psi_s(V))}{C_o}} - C_D(\psi_s)\right).$$

For a particular value of ψ_s, the position of the Fermi energy above the valence band edge at the surface is given by $\Delta = E_F - E_{V(bulk)} - \psi_s$ (for *n*-type material) or by $\Delta = \psi_s + E_F - E_{V(bulk)}$ (for *p*-type material).

Traditionally, the low frequency C-V characteristic has been measured using lock-in techniques. However, for frequencies below 5 Hz, this method becomes difficult. An alternative is to use the quasi-static technique [16]. In this method, the displacement current of the MOS capacitor is measured in response to a slow linear voltage ramp. If the ramp is "slow enough" (5 to 500 mV/s), the surface states remain in equilibrium and the displacement current is proportional to the low frequency capacitance.

The second technique to be considered is the temperature dependence of the high frequency C-V characteristic. This is the Gray-Brown [17] method where the flat band voltage of the MOS capacitor is monitored as the temperature is varied. An example of a high frequency C-V characteristic and a simplified silicon band diagram are shown in figure 10 for the case of a *p*-MOS capacitor. At temperature T_1, the Fermi level is assumed to be above the surface states which are filled and electrically neutral. As the temperature is lowered, the Fermi level moves closer to the valence

band edge; this causes depopulation of the surface states. The loss of electrons at the interface requires a larger negative bias voltage in order to maintain the flat band condition. Thus, as the temperature is lowered the C-V characteristic (for *p*-type devices) shifts to the left. The experimental procedure is to record the flat band voltage, $V_{fb}(T)$, as a function of temperature by monitoring the flat band capacitance, C_{fb}. The change in the flat band voltage is directly related to a change in the charge at the interface. Similarly the change in the surface potential with temperature is directly related to the shift in the Fermi energy. A graphical differentiation of a plot of the charge as a function of surface potential yields the interface state density. This technique is effective only around a small region of the band gap near the majority carrier band edge. Probing of the surface states near both the valence and conduction band requires both *p*-type and *n*-type specimens.

The third technique for measuring interface state density is the conductance method of Nicollian and Goetzberger [18]. In this technique, the frequency and bias dependence of MOS conductance is measured. Nicollian and Goetzberger showed that the conductive losses in the semiconductor space charge region and the oxide are negligible; hence, the a-c conductance in an MOS structure is due entirely to the interface states.

The simplified equivalent circuit for the MOS capacitor with surface states is shown in figure 11. The capacitive elements were defined in the discussion of figure 9b; the loss element associated with the interface states is R_{ss}. Experimentally, the appropriate measurement is to determine the impedance of the MOS capacitor, Z_{13}, as a function of frequency for values of bias from depletion to inversion. From each value of $Z_{13}(\omega,V)$, the oxide reactance, $Z_{12} = 1/j\omega C_o$, is subtracted and the result inverted to obtain the admittance, Y_{23}, associated with the semiconductor portion of the structure. For each value of bias voltage ($V(\psi_s)$), the maximum in the real part of the admittance determines C_{ss} and $N_{ss}(\psi_s)$. It is only necessary to find the relation between V and ψ_s. This can be done by the Berglund procedure [14] which was discussed earlier. Although this technique allows the probing of regions away from the band edges, it does not give information near the middle of the gap. To get data in both halves of the gap requires the use of both *n*-type and *p*-type specimens.

Of the three methods considered here, it is generally acknowledged that the conductance technique gives the most accurate results. However, it requires the collection of much data on both types of specimens and fails to obtain information in the mid-gap region. The temperature technique does not require as much data as the conductance technique but also suffers from lack of information in the mid-gap region. However, it does very well near the band edges, but requires both types of specimens. The

quasi-static technique is able to probe the entire mid-gap region using either type of specimen and fails to probe only the band edge region. It also has the advantage of being a relatively simple experiment to conduct.

(R. Y. Koyama)

5.2. Sodium Contamination Studies

To test the sodium contamination levels of various materials routinely used in the processing facility, analyses were made with a flame spectrometer. Most materials studied exhibited sodium levels of 0.5 parts per million or less. The photoresist developer contained about 1.7 percent sodium. The results of these analyses are summarized in table 5. The technique is sensitive to less than 0.1 parts per billion sodium and has an estimated accuracy of ±25 percent or better, at this level.

Samples of oxidized silicon treated with photoresist and developer are currently being prepared to study the amount of sodium which is transferred from the developer to the oxide during processing.

(T. C. Rains* and S. Mayo)

Table 5 — Flame Spectrometer Analysis for Sodium Contamination

Material	Sodium Level, ng/ml
Photoresist	50
Photoresist Developer	16.8×10^6
Hydrogen Peroxide	250
Ammonia	8
Buffered Etch for Silicon Dioxide	100
Hydrochloric Acid	500
Acetone	0.8

* NBS Spectrochemical Analysis Section, Analytical Chemistry Division.

6. TEST PATTERNS

6.1. Charge-Coupled Device Test Pattern

The six photomasks required for processing the charge-coupled device (CCD) test pattern were completed and tested for alignment accuracy with a stack-up test. This test is an extension of the procedure for three or more photomasks given in the ASTM Recommended Practice for Determining Multiple Photomask Registration [19]. In it the fabrication process is simulated by taking silicon wafers through a sequence of oxidations interspaced by photomasking steps; diffusion steps are omitted.

For example, to establish the alignment accuracy of six photomasks, seven wafers are oxidized. The pattern from the first photomask is applied and etched in the silicon dioxide. One wafer is set aside; the other six are oxidized and the pattern from the second photomask is aligned to the etched pattern on each of the six wafers and the second set of windows is etched into the wafers. This process is continued, setting aside one wafer at each step, until all the masks have been used. The result is a series of wafers, each one differing from the preceding one by the presence of the pattern from an extra mask level. Corrections, if required, can then be introduced with a minimum of wasted effort, cost, and delay. The stack-up test demonstrated that the design accuracy has been maintained through the process of layout, placement, digitizing, and art work generation and that the resolution of the masks is within the specified tolerances.

Photomicrographs of examples of the two test pattern dice taken from a fully fabricated, metallized, and passivated wafer are shown in figure 12. These photomicrographs show the placement of the various test structures included in the patterns (NBS Spec. Publ. 400-4, p. 46). The conductivity types given are appropriate to *n*-channel charge-coupled devices. A photomicrograph of a whole wafer is also shown in the figure. This photomicrograph illustrates the location of the two types of dice on the wafer: one column of conventional structures (die No. 1) with a column of CCD test structures (die No. 2) on each side.

Test fixtures, probe cards, preliminary test procedures, and computer programs for data analysis are being prepared for the experimental phase of the effort which is designed to establish the applicability of the CCD as an efficient and sensitive process control test structure. Analysis of the CCD with respect to different operating conditions has demonstrated the ability of the device to function not only as a CCD but as an MOS field effect transistor, a gated diode, and an MOS capacitor by use of the proper set of externally adjustable voltage levels. Thus, results obtained on the CCD can be directly compared with results obtained on more conventional test structures. (I. Lagnado* and M. G. Buehler)

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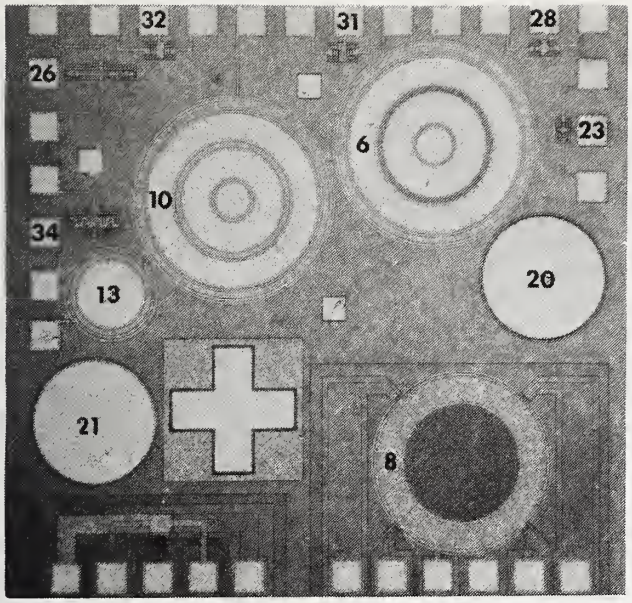
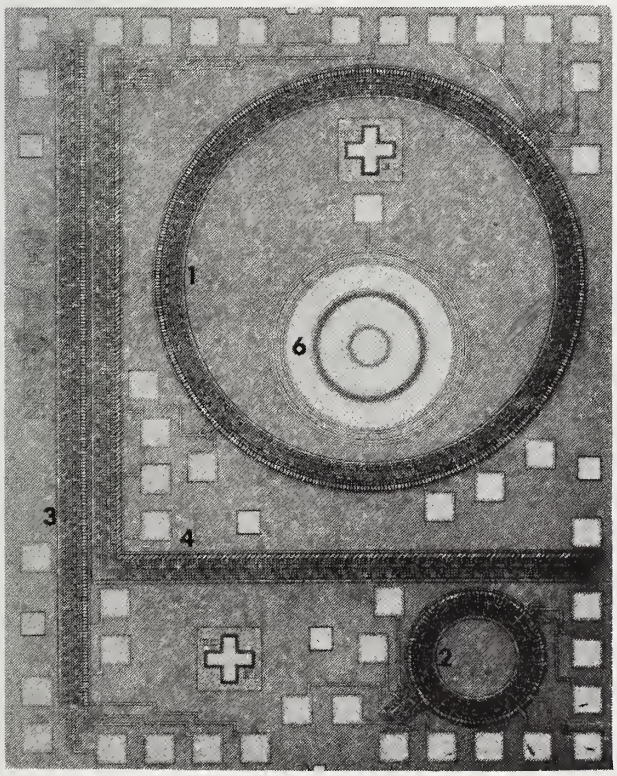
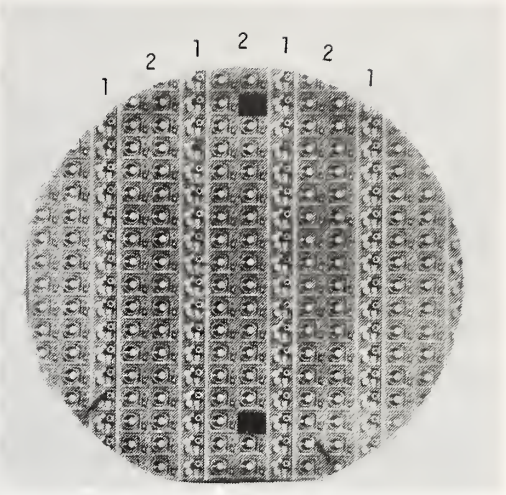
* Naval Electronics Laboratory Center, San Diego, California 92152.



a. Die No. 1: Conventional test structures. The overall horizontal dimension is about 103 mil (2.6 mm). (Magnification: ∿ 31 X).



b. Die No. 2: CCD test structures. The overall horizontal dimension is about 103 mil (2.6 mm). (Magnification: ∿ 31 X).



c. Whole 2-in. (51-mm) diameter wafer showing columns of Die 1 and Die 2. (Magnification: ∿ 1.1 X).

Structure	Description
1	128-bit circular CCD
2	32-bit circular CCD
3	64-bit linear CCD
4	64-bit parallelogram CCD
6	Gated n^+p junction (diameter = 20 mil, 0.51 mm)
8	Gated van der Pauw resistor in n^+-layer
9	Metal to n^+-layer contact resistor
10	Substrate (p-type) resistor
13	p-MOS capacitor with field plate (diameter = 11.4 mil, 0.29 mm)
20	p-MOS capacitor (gate oxide) (diameter = 20 mil, 0.51 mm)
21	p-MOS capacitor (field oxide) (diameter = 20 mil, 0.51 mm)
23	n-channel MOSFET (W/L = 2, L = 0.4 mil, 0.010 mm)
26	n-channel MOSFET (W/L = 12.5, L = 0.4 mil, 0.010 mm)
28	n-channel MOSFET (W/L = 1, L = 1.0 mil, 0.025 mm)
31	n-channel field oxide MOSFET (Isolation check)
32	n-channel field oxide MOSFET (W/L = 1, L = 1.2 mil, 0.030 mm)
34	n-channel MOSFET (W/L = 25, L = 0.4 mil, 0.010 mm)

Figure 12. Photomicrographs of the CCD test pattern.

7. PHOTOLITHOGRAPHY

7.1. Photomask Metrology

The information gathering phase of this effort was completed with visits to technical personnel responsible for research or production at eight additional facilities which produce or use photomasks. The problems of line width measurement and edge definition initially identified (NBS Spec. Publ. 400-4, p. 49) were more fully defined and activity was undertaken to begin to resolve the problems.

The line width measurement problem is complicated because the dimensions of the photomask or integrated circuit (IC) geometry approximate the wavelength of the visible light used to make the measurements. Under these conditions certain basic properties of light, such as the degree of coherence, have a large effect on image formation and, therefore, affect the accuracy and repeatability of the measurement. The degree of coherence basically determines the interference and diffraction effects exhibited by light. This factor has largely been ignored by manufacturers of optical instruments who, up to now, have concentrated on improving the quality of lenses, mirrors, and mechanical adjustments. Photomask and IC manufacturers, in general, are not aware of the limitations and conditions imposed on optical-measurement instruments by the degree of coherence. As a result, organizations in the photomask and IC industries spend much time and capital on equipment to improve only the reproducibility of their own in-house measurements. The approaches taken to ensure reproducibility usually include careful control of facility environment, low turnover in personnel trained to make visual measurements, and relying on the results of one basic type of instrument such as the filar eyepiece or the image shearing eyepiece.

An effort to quantify the effects responsible for obtaining different dimensional measurements on the same artifact when using the filar eyepiece or the image shearing eyepiece was begun. Initial measurements of the diameter of a metal wire (nominal diameter 15 μm) and a pinhole (nominal diameter 10 μm), which were the only suitable artifacts immediately available, were completed. Measurements were made with the use of reflected or transmitted partially coherent light from an incandescent source* with a blue Wratten No. 45 filter† and transmitted coherent (laser) light of wavelength 632.8 nm. In each case the measurements made by the

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* Light produced by an incandescent source and focused by a lens is completely incoherent only when the source to lens distance is very small and the angle from the source subtended by the lens diameter is very large. As the source to lens distance increases, the coherency of the light increases to give partially coherent light. Generally the degree of coherency is not known [20].

† Certain commercial equipment is identified in this paper in order to specify the experimental procedure adequately. This identification does not imply recommendation or endorsement by the National Bureau of Standards, nor does it imply that the equipment identified is necessarily the best available for the purpose.

two systems differed by between 0.2 and 1.7 μm. No definite conclusions applicable to photomask metrology were drawn from these data because they were obtained from measurements on materials which do not necessarily have the same properties as IC photomask materials. Nevertheless, the differences obtained illustrate the problems encountered in comparing measurements made with the two types of eyepieces. The next step is to make similar measurements on hard-surface chromium-on-glass artifacts which more closely duplicate the geometry and materials used for IC photomasks.

The second problem defined was that of locating a physical edge for a line or other geometrical pattern. This problem is intimately related to the problem of line width measurement since one must locate an edge to which the measurement can be referenced. In addition, the actual physical profile of the edge is important to an IC manufacturer since it is relevant to defining an active region for the device. Here again, optical instruments are the primary means for measurement, and such properties as the degree of coherence bear directly on the resulting determination of edge definition.

A theoretical analysis was made of the apparent position of an opaque edge of ideal geometry in incoherent and coherent light when viewed through a microdensitometer or other optical equipment. These results showed the edge to shift by 1.6 μm into the light area when the illumination was changed from completely incoherent to completely coherent radiation and the edge position was assumed to be at the half power point. This analysis also showed that the true edge was at the half power point for the completely incoherent light and at the quarter power point for the completely coherent light. Since coherent light is easy to produce and control with a laser it was concluded that measurements using laser radiation and the quarter power point for edge definition should be explored. (J. M. Jerke* and D. B. Novotny)

7.2. Automated Photomask Inspection

Visits made to an additional 15 companies representing both photomask manufacturers and users confirmed that major problems in the manufacturer of photomasks are, as previously identified (NBS Spec. Publ. 400-4, pp. 49-50), visual defects, registration errors between layers, difficulty in establishing critical dimensions, and photoplate blank quality.

It was found that the IC industry is currently using the following methods and equipment for photomask inspection. Masks are inspected for visual defects by persons who observe the functional pattern or photomask through microscopes. Magnifications of 10 to 30X are used to detect gross defects such as glass chips, cracked glass, chemical stains, fogging, foreign particles, array rotations, and scratches. A magnification of approximately

* NBS Optics and Micrometrology Section, Optical Physics Division.

100X is used to detect pattern defects such as pinholes greater than 2.5 μm, bridging between two adjacent opaque areas or between two adjacent clear areas, extensions (2.5 μm or greater) into either clear or opaque areas, and opaque spots (2.5 μm or greater) in clear areas. Image quality is inspected using a magnification of approximately 400X. Defects revealed in this inspection include graininess, semitransparent areas that should be opaque, and ragged edges on pattern geometries.

Critical dimensions of photomask functional patterns are currently measured with an image shearing eyepiece on a microscope, a filar type eyepiece on a microscope, or a closed circuit TV camera combined with a microscope and an electronic measuring micrometer. Approximately 60 percent of the facilities visited used the image shearing eyepiece for critical dimension inspection. It is especially useful for dimensions above 5 μm and is a relatively rugged piece of equipment which is easy to use. The filar eyepiece was used by about 40 percent of the facilities visited. It was prefered by most for the measurement of dimensions less than 5 μm. A common problem with this system is locating a line edge when the hair line is traversing from an opaque to a clear area. There are problems of comparing dimensions measured by both systems (see sec. 7.1.). The TV system can be used to measure line widths in the 1 μm range with a precision of ±25 nm (±1 μin.). However, calibration of this system is difficult, the image quality is a function of the illumination intensity, and day-to-day correlations between measurements are poor.

Inspection for registration involves the use of optical comparators in which the image on the photomask of one layer is superimposed optically on the image on the photomask of another layer. Differences in registration are measured by optical micrometers.

Currently the IC industry is operating in the measurement range of critical dimensions on high volume production of 5 ± 0.5 μm with increasing activity in the 2 ± 0.2 μm range. Registration tolerances range from ±0.5 to ±1.2 μm with some special applications held to ±0.25 μm. Practical line width limits on masks are estimated as 2.5 μm for emulsion and 0.5 μm for hard-surface photomasks [21].

(D. R. Ciarlo*, P. A. Schultz*, and D. B. Novotny)

7.3. Photoresist Exposure

An interpretation of results section was written for a Recommended Practice for the Determination of Correct Photoresist Exposure [22] which is now ready for ballot by the Processing Subcommittee of ASTM Committee F-1 on Electronics. The document was also rewritten in ASTM format and edited.

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* Lawrence Livermore Laboratory, Livermore, California 94550.

This recommended practice, based primarily on the work of Goldrick and Plauger [23], provides a method for determining both the minimum exposure energy and the optimum exposure energy for both positive and negative photoresists of a given resist film thickness as used in the manufacture of photomasks and microelectronic components. A method for converting the optimum exposure energy to the parameters of time and radiant power density is given. The limitations of the practice when used with unstable actinic radiation exposure sources and the use of a radiometer to determine the source stability are considered in the document.

In this method photoresist is coated on a wafer or mask substrate, dried and exposed through a step tablet. The resulting images are developed. Data are taken from these developed images from which the minimum and the optimum exposures are calculated.

The determinations of minimum and optimum exposures are useful for quality control inspection of photoresist materials and the determination of correct exposure parameters for photomask and microelectronic components processing. In this practice it is recommended that the actual production masks be used for determining the correct exposure in critical production processes, where the topography of the substrate, the relationship of mask apertures and final circuit geometries, and other parameters may affect the photoresist processing steps.

Photoresist overexposure results in line broadening or window shrinking for negative photoresist and line shrinking or window broadening for positive photoresists. Photoresist underexposure results in incomplete adhesion for negative photoresists and incomplete photoresist removal for positive photoresists. Furthermore, a knowledge of the optimum photoresist exposure is necessary for the accurate reproduction of mask pattern images on photoresist-coated wafers or mask substrates. A knowledge of the minimum photoresist exposure is necessary for the approximation of minimum contrast requirements for off-contact exposures. (D. B. Novotny)

8. EPITAXIAL LAYER THICKNESS

8.1. Step-Relaxation Method

The investigation of metal-oxide-semiconductor (MOS) capacitance methods for measuring the layer thickness of thin epitaxial layers (NBS Spec. Publ. 400-4, pp. 51-53) was continued with an experimental comparison of the step-relaxation method with the infrared reflectance method [24] and the spreading resistance method [25].

The topside aluminum and backside gold were removed from five n/n^+ epitaxial wafers on which the layer thickness had been measured by the step-relaxation method (see table 12, NBS Spec. Publ. 400-4, p. 53). A section was scribed and broken parallel to the flat and at a distance from the flat corresponding to the original location of devices 1 and 2. The oxide was removed from the larger portion of each wafer, and an infrared reflectance spectrum for the range of wavelengths from 2.5 to 25 μm was taken using a dual-beam spectrophotometer. The layer thicknesses were calculated as directed in ASTM Method F 95 [24] from the extrema of the reflectance spectra, the resistivities of the substrates as measured by the four-probe method [5], and the appropriate phase shift corrections. The phase shift corrections for substrates with resistivity of 0.001 Ω•cm and greater were taken from the table in ASTM Method F 95; additional phase shift corrections for resistivity down to 0.0003 Ω•cm were calculated from a set of curves reported by Schumann [26]. The results are listed in table 6 in the column labeled Infrared Reflectance Method. For comparison, the average of the thickness as measured by the step-relaxation

Table 6 — Epitaxial Layer Thickness

Wafer No.	Layer Resistivity, Ω•cm	Substrate Resistivity, Ω•cm	Layer Thickness, μm			
			Step-Relaxation Method[a]	Infrared Reflectance Method	Step-Relaxation Method[b]	Spreading Resistance Method
2302	2.5	0.0012	2.95	3.93	2.80	3.3
2351	1.0	0.0017	1.47	3.28	1.49	4.6
2352	1.0	0.0009	1.46	3.20	1.47	---[c]
2203	7.5	0.015	4.69	5.87	5.03	6.6
2204	5.6	0.014	----[d]	6.09	5.17	5.4

[a] Average of thickness measured on devices 3, 4, and 5.

[b] Thickness measured on device 1 or device 2.

[c] The constant level of spreading resistance characterizing the substrate was not reached abruptly in this wafer making the thickness determination obscure.

[d] The epitaxial layer here was too thick to be measured by the step-relaxation method for an applied voltage step from +100 V to -100 V.

method on devices 3, 4, and 5, which are near the center portion of the wafer, is also listed. It is found that the value measured by the infrared reflectance method is consistently larger than the value measured by the step-relaxation method.

The smaller sections of each wafer, still having oxide on the top surface, were bevel lapped at an angle of 1 deg, 9 min with the top surface. The spreading resistance was measured at 5 μm increments down the bevel with a two-point spreading resistance probe. The probes were loaded with 20 gf (196 mN). The layer-substrate interface was taken to occur at the point where the uncorrected measured spreading resistance reached the constant level appropriate to the substrate. These layer thickness values are listed in table 6 in the column labeled Spreading Resistance Method. For comparison, the thickness as measured by the step-relaxation method on device 1 or device 2, which was located near the center of the smaller wafer section, is also listed. (R. L. Mattis)

9. WAFER INSPECTION AND TEST

9.1. Flying-Spot Scanner Development

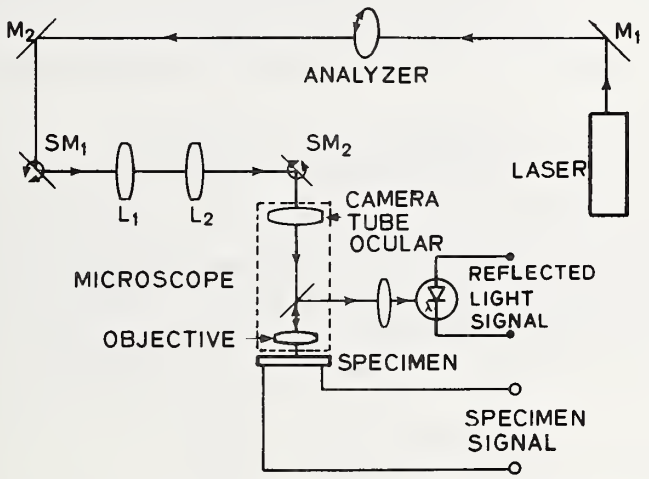
The optical flying-spot scanner was assembled and operated with a laser source of wavelength 0.6328 μm. The design incorporates optical system concepts from several sources [27-29]. The scanner is rugged and does not appear to be susceptible to outside influences such as building vibrations. The scan raster is incident on the specimen, which is clamped onto the observation stage, through the camera tube of a binocular microscope. With oculars of the same magnification used for the binocular eyepieces and in the camera tube, the scan field is approximately the same as the field of view seen through the eyepieces.

A schematic diagram of the scanner is shown in figure 13a. To save space the 5 mW laser is mounted vertically on a frame bolted to the microscope stand. Space is also saved by folding the optical system, and this is the purpose of the fixed mirrors M_1 and M_2. Since the light from the laser is polarized, the light intensity may be conveniently controlled as shown with a rotatable analyzer. The first scanning mirror, SM_1, provides vertical deflection of the beam at frequencies variable from 0.01 Hz to about 1.1 kHz, the mechanical resonant frequency; frequencies of a few hertz are usually used. The vertically deflected beam is collected by the lens system L_1 and L_2 and refocussed (deflection reduced to zero) on the second scanning mirror SM_2. This refocussing technique [29] allows large scanning angles to be achieved using small-size deflection mirrors. Mirror SM_2 is at the exit pupil point for the camera tube ocular, and deflects the beam in the horizontal scan direction. This mirror and associated driving circuit are identical to SM_1 and its driver; SM_2 is usually driven at about 1 kHz. On passing through the microscope, the laser beam is focussed on the specimen in a raster scan. The signal output from the specimen is displayed on a monitor screen shown in the picture of the equipment in figure 13b. The monitor beam is driven in synchronism with the raster pattern.

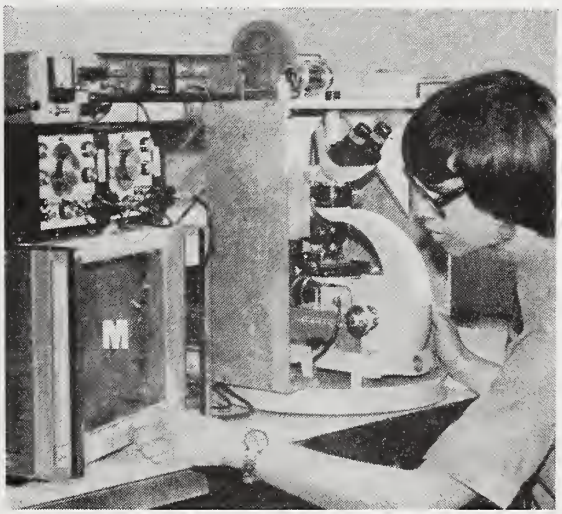
Some useful and fairly novel features were incorporated into the scanner. The first allows one to zoom in on the specimen region of interest. The scan oscillators produce blanking and monitor sweep waveforms of constant amplitude in addition to adjustable amplitude waveforms for the deflection mirrors. The drivers, one for vertical deflection, and one for horizontal deflection, have d-c offset controls. With the use of these offset controls and the amplitude controls, it is easy to move the center of the optical scanning raster to any part of the field and then increase the monitor screen magnification of the region of interest by decreasing the mirror drive; the raster deflection on the monitor screen remains the same.

The second feature provides the capability of exactly locating specimen photoresponse with respect to topographical details such as metallization stripes. This capability was incorporated by adding a separate optical

circuit, with a permanently mounted photodiode, to provide a signal proportional to the light reflected from the specimen while scanning. This was accomplished by splitting off the reflected beam with the half-silvered mirror in the microscope tube. This mirror was originally intended to provide vertical illumination when the microscope is used for visual observation; this capability was retained.



a. Schematic diagram of light and signal paths. The light path between M_1 and M_2 is directly behind the light path between SM_1 and SM_2. SM_1 rotates around a vertical axis, and SM_2 rotates around a horizontal axis.



b. Photograph of system including monitor screen (M).

Figure 13. Flying-spot scanner.

The operation of the scanner was checked with a chrome-on-glass test target. With favorable conditions, such as with the use of a medium to high-powered microscope objective lens, the smallest elements, 2 μm wide stripes separated by 2 μm, were resolved. This test was made with essentially identical results two ways; one way used the reflected light circuit described, and the other used a photodiode in back of the test pattern to convert the transmitted light to an electrical signal for the monitor scope. (D. E. Sawyer, D. W. Berning, and G. J. Rogers)

9.2. Scanning Electron Microscopy — Voltage Contrast Mode

The sensitive cylindrical secondary electron detector (NBS Spec. Publ. 400-4, pp. 54, 56) was completed and assembled, as illustrated in figure 14, for use in the scanning electron microscope. The sensitivity of this detector to voltage variations on the specimen is dependent on the bias conditions existing on the parts of the detector [30]. Bias is applied to the top plate, to the bottom plate, and to an insulated insert in the bottom plate. Measurements have been started to determine the sensitivity for this detector as a function of specimen potential and detector biases. (W. J. Keery and L. M. Smith)

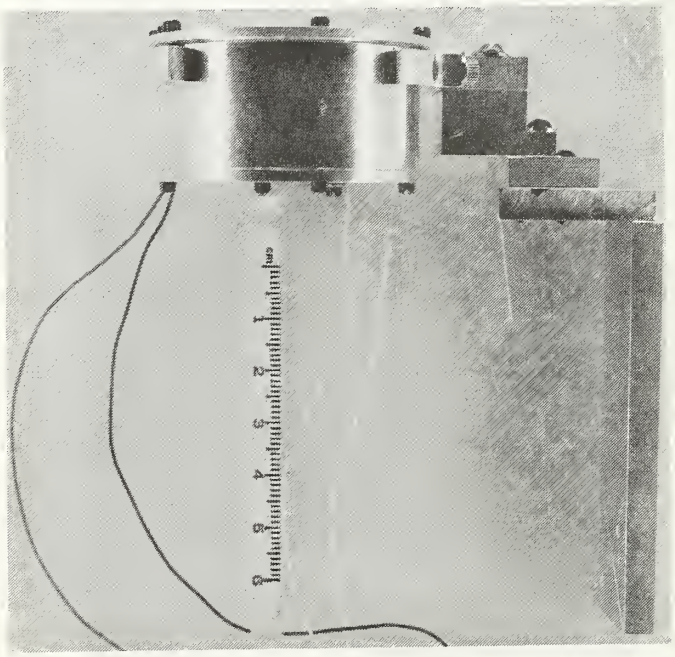


Figure 14. Cylindrical secondary electron detector with mounting bracket for use with the eucentric stage of the scanning electron microscope.

10. INTERCONNECTION BONDING

10.1. In-Process Bond Monitor

To provide a qualitative and semiquantitative basis for the dependence of the vibration of ultrasonic bonding tools in the unloaded phase of operation upon material and geometrical properties, a uniform beam prototype was used as a model for the tool. This model consists of a uniform cross-section beam clamped at the transducer horn, $x = 0$, and driven sinusoidally at frequency ω. The vibration amplitude at $x = 0$ is taken equal to a. The equation which describes the motion of the tool in space and time is (NBS Spec. Publ. 400-4, pp. 65-66):

$$\frac{\partial^4 y(x,t)}{\partial x^4} + \frac{\rho A}{EI} \frac{\partial^2 y(x,t)}{\partial t^2} = 0, \tag{3}$$

where $y(x,t)$ is the vibration amplitude at position x and time t, ρ is the volume density of tool material, A is the cross sectional area of the tool, EI is the flexural rigidity of the tool. Since the tool is driven sinusoidally, separation of variables is assumed in the form $y(x,t) = a \sin \omega t\, Y(x)$. Equation (3) then becomes:

$$\frac{d^4 Y(x)}{dx^4} - \frac{\rho A \omega^2}{EI} Y(x) = 0, \tag{4}$$

which has as its general solution:

$$Y(x) = B_1 \sinh (qx) + B_2 \cosh (qx) + B_3 \sin (qx) + B_4 \cos (qx),$$

where the coefficients B_1, B_2, B_3, and B_4 are determined by the boundary conditions appropriate to the problem, and q is, at fixed frequency, a constant given by:

$$q = \left(\frac{\rho A \omega^2}{EI}\right)^{1/4} .$$

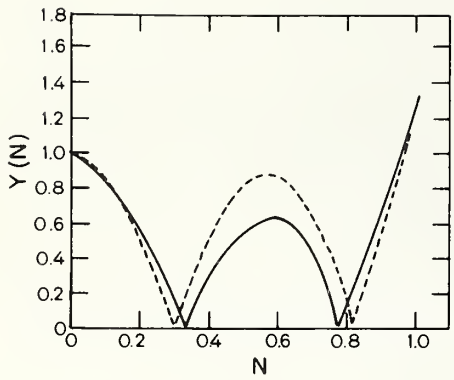
The boundary conditions relevant to the present problem are:

$$Y(0) = 1 \qquad Y'(0) = 0$$
$$Y''(\ell) = 0 \qquad Y'''(\ell) = 0 ,$$

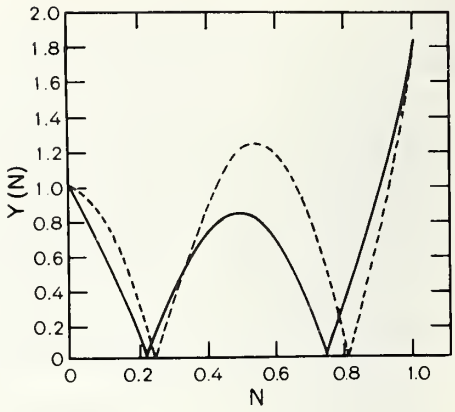
where the primes represent differentiation with respect to x, and ℓ, the value of x at the free end of the tool, is the tool extension below the horn. The particular solution of eq (4) is:

$$Y(N) = \frac{1}{2E(Z)} \left(A(Z)[\sin(NZ) - \sinh(NZ)] + B^{+}(Z)\cosh(NZ) + B^{-}(Z)\cos(NZ)\right)$$

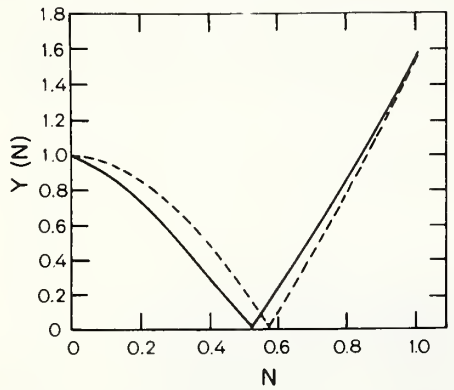
where:



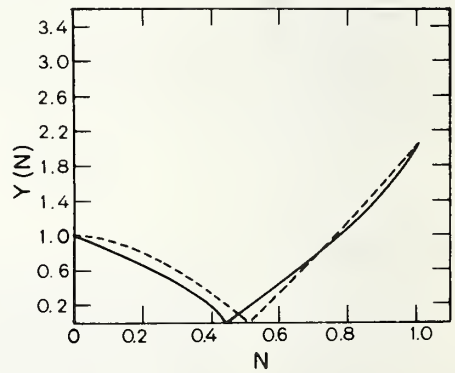
a. Long tungsten carbide tool of conventional design. Solid curve: measured; dashed curve: calculated for a uniform beam for which $q\ell$ = 5.55.



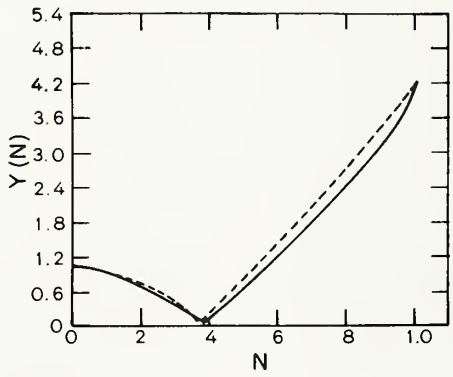
b. Long titanium carbide tool of conventional design. Solid curve: measured; dashed curve: calculated for a uniform beam for which $q\ell$ = 5.27.



c. Short tungsten carbide tool of conventional design. Solid curve: measured; dashed curve: calculated for a uniform beam for which $q\ell$ = 2.39.



d. Short titanium carbide tool of conventional design. Solid curve: measured; dashed curve: calculated for a uniform beam for which $q\ell$ = 2.25.



e. Short tungsten carbide tool of thin-line design. Solid curve: measured; dashed curve: calculated for a uniform beam for which $q\ell$ = 2.05.

Figure 15. Measured and calculated normalized vibration amplitudes of ultrasonic bonding tools.

Table 7 — Tool Properties

Material	Design	Extension (ℓ), mm	$q\ell$	q, mm^{-1}
	conventional	14.2	5.55	0.39
Tungsten Carbide	conventional	6.4	2.39	0.38
	thin-line	6.4	2.05	0.32
Titanium Carbide	conventional	14.2	5.27	0.37
	conventional	6.4	2.25	0.35

$$Z = q\ell,$$

$$N = x/\ell,$$

$$E(Z) = 1 + \cosh(Z)\cos(Z),$$

$$B^{\pm}(Z) = E(Z) \pm \sinh(Z)\sin(Z),$$

and

$$A(Z) = \sin(Z)\cosh(Z) + \cos(Z)\sinh(Z).$$

To compare this solution with experimental data on several ultrasonic bonding tools (NBS Tech. Notes 788, pp. 35-41 and 806, pp. 30, 31, 33) [31], Y(N) was computed for N between 0 and 1 in steps of 0.05 and Z = $q\ell$ between 0 and 9 in steps of 0.01. The experimental data were written in terms of the dimensionless variables N and Z and then normalized to the amplitude of the tool at the transducer horn. The best fit of Y(N) to the experimental data was selected by choosing the value of Z which resulted in the least percent difference between the calculated and experimental nodal positions and vibration amplitudes at the tool tip. The resulting curves are shown in figure 15 for the cases of a long tungsten carbide tool, a long titanium carbide tool, a short tungsten carbide tool, a short titanium carbide tool, all of conventional design, and a short tungsten carbide tool of thin-line design. In each case the curves agree qualitatively quite well and the locations of the nodes and the values of Y(N) at N = 1 agree to within 10 percent.

The value of q was computed from the values of $q\ell$ and ℓ for each tool. The results are presented in table 7. The greater deviation between the q value for the thin-line tool and the rest is not unexpected since the thin-line tool is least well described by the uniform beam model.

This analysis provides a basis for the numerical solution of the general nonuniform beam equation which is presently under consideration.

(J. H. Albers)

11. HERMETICITY

11.1. Hermeticity Test Standards

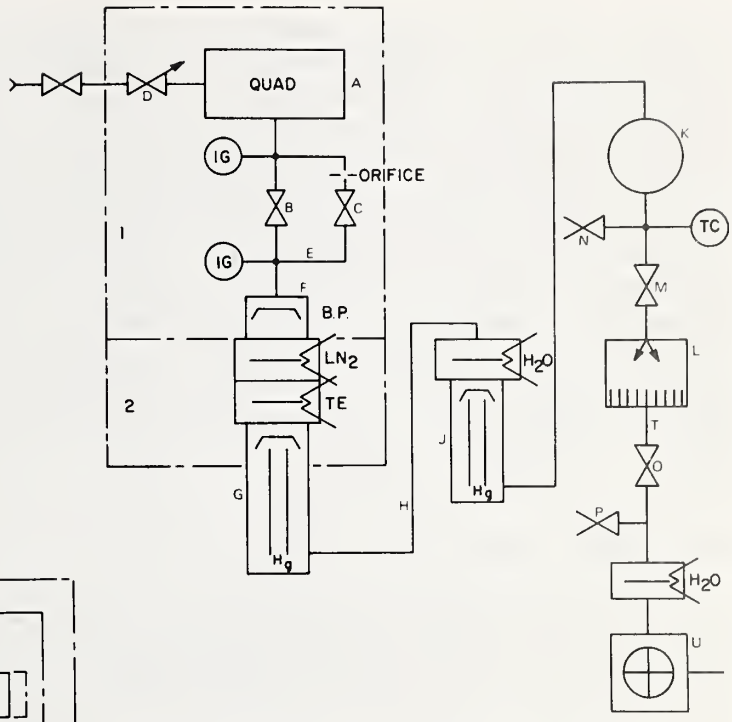
Testing has been completed at all five participating laboratories on the first phase of the interlaboratory evaluation of the recommended practice for hermetic testing with a helium mass spectrometer leak detector [32] being conducted in cooperation with ASTM Committee F-1 on Electronics. In this phase measurements were made on 50 glass capillary leaks in open ended tubulations. The leaks were grouped into five batches of ten leaks each. To reduce the danger of damage to the leaks during testing, the groups were circulated so that each laboratory measured two groups. Of these, one group of leaks was tested for the first time, while the second had been measured previously by another laboratory. All testing was by appointment and was refereed. All leaks have survived and agreement appears good. This phase of the evaluation was intended to establish a leak rate for each of the leaks. The next phase entails sealing off these capsules and the measurement of the leaks by the back pressurization technique specified in the test method [32].

As a result of interest developed at the ARPA/NBS Workshop on Hermeticity Testing for Integrated Circuits [33], plans have been initiated within ASTM Committee F-1 for a round-robin intercomparison of leak testing by radioisotope procedures [34]. (S. Ruthberg)

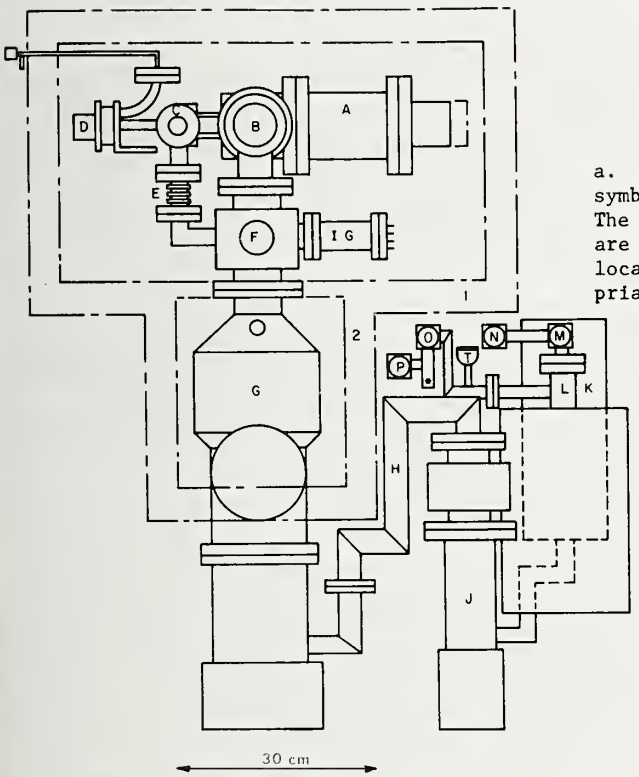
11.2. Mass Spectrometer Application

The sensitive mass spectrometer, designed to evaluate the use of this type of instrumentation for the measurement of trace elements in the semiconductor processing environment and for the investigation of gas flow mechanisms in leaks in hermetic packages (NBS Spec. Publ. 400-4, pp. 67-68), was assembled and preliminary checkout was begun.

The system is illustrated in figure 16. Standard symbols [35] are used in the vacuum circuit (fig. 16a). The cascaded mercury diffusion pumping array (G, H, J), double trapped with liquid nitrogen and thermoelectric cooling, is intended to produce an ultrahigh vacuum with minimum contamination and to allow a wide range of gas loads. A bypass orifice is provided to set controlled pumping conditions for stable calibration. Fore pumping is accomplished with a sorption pump (L) in conjunction with a ballast volume (K). In this way operation can be continued over an extended period, while the sorption pump can be used intermittently. A mechanical forepump (U) is also incorporated for those phases of operation which require high gas flow rates or extended, unattended periods; however, gas passage is through the sorption pump which has been modified to double as a trap for oil vapor. Two ovens are provided for bakeout to 400°C. Oven number 1 includes the quadrupole mass analyzer section and the manifold proper, while oven number 2 includes the trapping array and the upper part of the ultra high vacuum diffusion pump. A chilled blocking plate (F) is placed above the traps in oven number 1.



a. Vacuum circuit. The letter and number symbols correspond with those in the sketch. The bellows (E) and the thermocouple gauge (T), are not shown on the vacuum circuit; they are located in the positions marked by the appropriate letter symbol.



b. Sketch. The letter and number symbols correspond with those in the vacuum circuit. The line to valve (D) lies behind valves (B) and (C). The ionization gauge connected to the quadrupole tube, the thermocouple gauge connected to the reservoir (K), and the baffled mechanical forepump (U) are not shown on the sketch; the forepump is connected to the line marked with an asterisk under the valve (O).

A	quadrupole tube
B	2-in. (51-mm) bakeable valve
C	1-1/2-in. (38-mm) bakeable valve
D	bakeable leak valve
E	bellows
F	spool with blocking plate
G	double trapped mercury diffusion pump
H	foreline to booster pump
IG	nude ionization gauge
J	mercury booster pump with chilled baffle
K	ballast reservoir
L	modified sorption pump
M, N, O, P	flow control valves
T	thermocouple gauge
U	mechanical forepump with chilled baffle
1	top bakeout oven
2	bottom bakeout oven

Figure 16. Quadrupole mass analyzer system.

The operational sequence uses dry nitrogen gas for diffusion sweeping during start up and shut down of the diffusion pumps to minimize mercury backstreaming and contamination. After cold traps are activated, the pumps are in operation, and the pressure is $\leq 10^{-6}$ Torr, the blocking plate is chilled, oven number 1 is brought to 200°C, oven number 2 is activated, the main diffusion pump is turned off, and the main cold traps are allowed to warm. Both ovens are brought to about 400°C. After a suitable period, the lower oven is cooled, the traps are activated, the main pump is turned on, and the blocking plate is allowed to come to oven temperature. Baking with the upper oven is continued for the desired period. This operational sequence was carried out and produced a pressure of about 1×10^{-10} Torr (1.3×10^{-8} Pa) after a bakeout of several hours duration. Further prolonged bakeout and operation is expected to reduce the ultimate pressure accordingly. (S. Ruthberg and W. A. Cullins)

11.3. Dry, Quantitative Gross Leak Test

Time constants and expected behavior were analyzed further for the static expansion-differential pressure method which has been proposed (NBS Spec. Publ. 400-4, p. 70) to fill the need for a convenient quantitative test for measurement of integrity of hermetic packages in the gross leak range [$>10^{-5}$ atm·cm^3·s^{-1}($>10^{-6}$ Pa·m^3·s^{-1})]. A compact prototype apparatus has been designed to derive operational characteristics, to test precision, and to obtain experience in the testing of packages with internal volume up to about 1 cm^3.

A basic limitation on the sensitivity and precision of the method is the temperature drift between the test and reference chambers. An experiment has been initiated to determine temperature limitations of the method. (S. Ruthberg and W. A. Cullins)

12. THERMAL PROPERTIES OF DEVICES

12.1. Thermal Resistance Methods — Power Transistors

An analysis was undertaken to explain the observed facts that measurements of the thermal resistance of power transistors using the forward biased emitter-base junction voltage as the temperature sensitive parameter (TSP) give higher thermal resistance values than measurements using the forward biased collector-base junction voltage (NBS Tech. Note 806, pp. 45-47) and that wide-base devices have a smaller difference in measured thermal resistance for the two methods than do narrow-base devices (NBS Tech. Note 717, p. 31). The first of these observations appears to contradict the normal expectation that, since most of the power dissipation occurs at the collector-base junction, the collector-base junction voltage when used as the TSP would indicate a higher temperature than the emitter-base junction voltage. One might be tempted to explain the first observation by reasoning that the heat flow from the emitter to the heat sink through the emitter lead is so much smaller than the flow from the emitter through the collector that any net heat generation, no matter how small, in the emitter-base region would increase the emitter-base junction temperature above that of the collector-base junction. If this assumption were correct, however, then a wide base device would have a higher thermal resistance from emitter-base junction to collector-base junction because of the increased heat flow path length.

An alternative explanation has been offered by Plumlee and Peterman [36], who make the point that the entire collector-base junction is at a uniform temperature during calibration but that the portion of the collector-base junction directly under the emitter-base junction is heated to a significantly higher temperature than the portion under the base electrode metallization during transistor operation when there is internal device power dissipation. The drop in internal collector-base voltage during operation causes a change in the division of measuring current between the junction area under the base metallization and that portion under the emitter. The effect is to increase the current and thus the current density in the portion of the junction under the emitter, and thus cause the indicated collector-base junction voltage to be higher during measurement than during test for the same junction temperature. This higher junction voltage corresponds to a lower temperature than actually exists and thus to a smaller thermal resistance than would be indicated if the difference in the effective areas of the junction during calibration and measurement were the same.

This effect is illustrated graphically in figure 17 which shows portions of the temperature-voltage curves for a hypothetical collector-base junction with the same junction current under calibration and operating conditions. Curve B is the calibration curve which was obtained under isothermal conditions and with a measuring current low enough to be uniformly distributed over the junction area. When a measurement is made immediately after a period of operation, the measuring current is concentrated in the

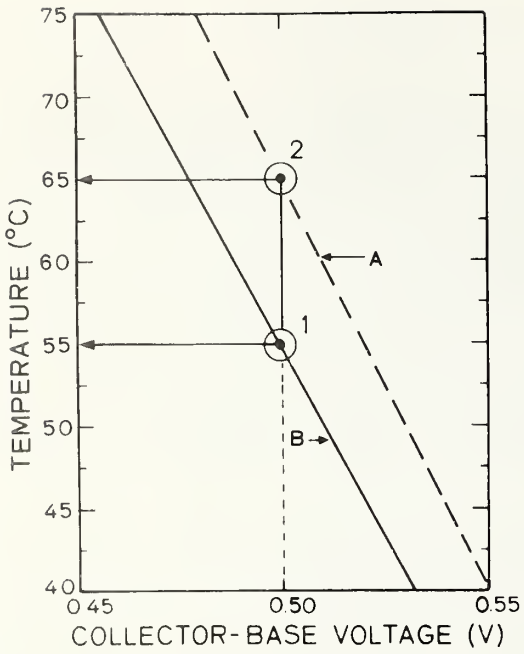
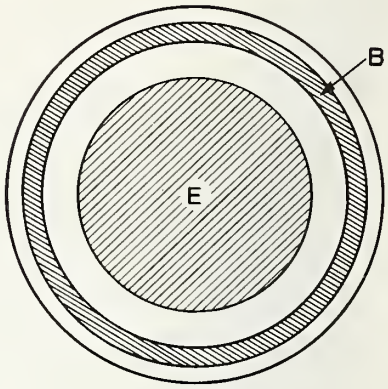
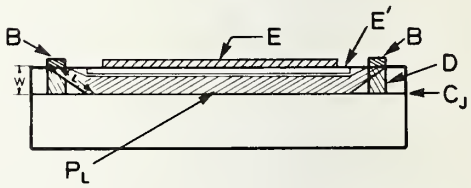


Figure 17. Temperature-voltage curves for a hypothetical collector-base junction under operating (A) and calibration (B) conditions for the same total junction current.



a. Top view.



b. Cross section (not to scale).

B	Base electrode
C_J	Collector-base junction
D	Overlap diode current path
E	Emitter electrode
E'	Emitter diffusion
L	Edge length (L>W)
P_L	Lateral current path
W	Base width

Figure 18. Diagrams of transistor showing current paths for overlap diode model.

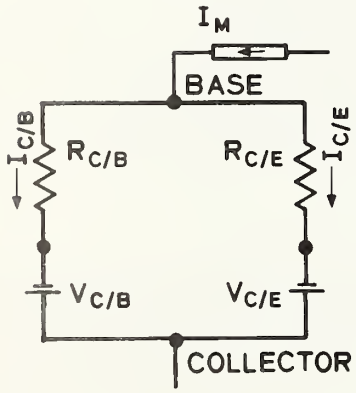


Figure 19. Equivalent circuit for analysis of collector-base voltage in overlap diode model.

hotter central portion of the junction; thus the current density is greater during measurement then during calibration. The temperature-junction voltage relationship appropriate to this higher current density, curve A in the figure, lies above the calibration curve. As an example, consider a measured junction voltage of 0.5 V. Although the calibration curve appropriate to the measuring current indicates that the junction temperature is 55°C (point 1), the temperature which corresponds to this voltage is actually 65°C (point 2).

This model has also been proposed by Wheatley* who uses the term "overlap diode" to identify the effective diode formed by the base electrode and the collector junction area directly under it. This is the area which is not raised significantly in temperature during operation and it contains the principal portion of the collector junction area which is not active during operation. There is no counterpart to the overlap diode in the case when the emitter-base junction-voltage is used as the TSP. The present analysis indicates that this model is consistent with the observation that there is less deviation between emitter-base and collector-base measurements for wide-base than for narrow-base devices.

Assume the overlap diode and lateral current paths in the base during calibration and during measurement are a concentric ring and a truncated circular cone, respectively, as shown in figure 18. This structure can be represented by the equivalent circuit of figure 19 where the branch labeled C/B refers to the base current path in the overlap diode and the branch labeled C/E refers to the lateral base current path in the active region of the transistor. It is reasonable to assume that the ratio of resistances, $R_{C/E}$ to $R_{C/B}$, is lower for a wide-base device than for a narrow base device. The measuring current, I_M, is constant but will divide according to the resistances and internal junction voltage drops, $V_{C/E}$ and $V_{C/B}$. The measured junction voltage at the device terminals is:

$$V_{CB} = I_{C/B}R_{C/B} + V_{C/B} = I_{C/E}R_{C/E} + V_{C/E}.$$

If the temperature dependence of $V_{C/E}$ (the temperature of the overlap diode region is assumed constant) and the current dependence of both $V_{C/E}$ and $V_{C/B}$ are taken into account, it can be shown that for a considerable range of parameter values the change in V_{CB} between calibration and operating conditions is less for a narrow-base device than for a wide-base device. (S. Rubin)

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* C. F. Wheatley, Jr., RCA, Somerville, New Jersey 08876 (private communication).

12.2. Thermal Resistance Methods — Darlington Pairs

The use of monolithic Darlington power transistors is increasing rapidly but at present there appears to be no accepted standard method for thermal resistance testing of these devices. Work was initiated during this quarter in an effort to develop a satisfactory standard test method.

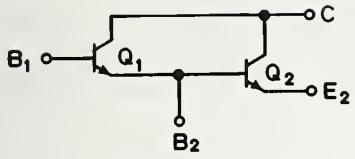
There are at present in wide commercial production four configurations of monolithic Darlingtons as shown in figure 20. The configuration in figure 20a contains two transistors in tandem with no additional integrated components. This is a trivial case to measure because the emitter and base region of both transistors are connected to device terminals. Hence, the emitter-base voltage of either the input or the output transistor can be measured in the manner used with a single transistor, even though the devices are heated for test in the Darlington tandem configuration as they would be operated in practice.

The configuration in figure 20b is more difficult to measure since it is not possible to measure independently either junction of the output transistor. However, one can measure the collector-base junction voltage of the input transistor independently and a series combination of the two emitter-base junction voltages.

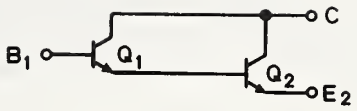
The configurations in figures 20c and 20d are similar in that both have integrated bias-return resistors and a diode, but they differ in placement of the diode. From the standpoint of measurement of thermal resistance, the former configuration appears more desirable because the output diode can be used for sensing the temperature in the region of the output transistor where the thermal problems are likely to be most severe. However, if the resistor R_2 is small enough (<100 Ω), the collector-base junction of transistor Q_2 can be measured.

Several temperature sensitive parameters (TSP) are used to measure the thermal resistance of single transistors [37]. Since the Darlington is composed of two transistors, it would appear to offer increased possibilities. However, in the absence of the external connection B_2, the options are severely restricted. If the three-terminal Darlington configurations are placed in the transistor socket of a thermal resistance measuring circuit, the series combination of the emitter-base voltages of both transistors can be measured by either the emitter-only switching method [38] or the emitter-and-collector switching method (NBS Tech. Note 743, pp. 34-35). It is necessary to use a measuring current that is large enough that the emitter-base junctions of both transistors Q_1 and Q_2 operate linearly for either of these methods. In the case of emitter-only switching the current must be large enough that it is not altered significantly by leakage current multiplication in transistor Q_1.

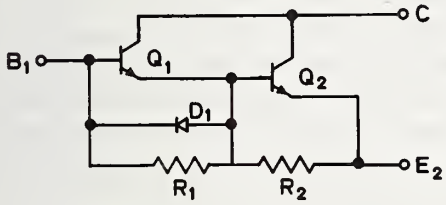
Initial measurements of this kind were made on several Darlington circuits. All devices studied were measured by the emitter-only switching method;



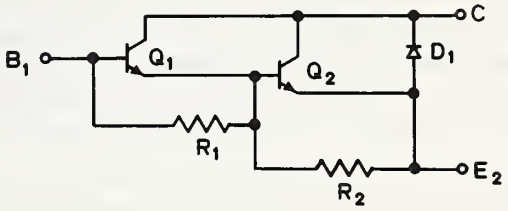
a. Four-terminal stripped Darlington.



b. Three-terminal stripped Darlington.



c. Three-terminal Darlington with integrated resistors and input diode.



d. Three-terminal Darlington with integrated resistors and output diode.

Figure 20. Commercially available Darlington circuits.

Table 8 — Calibration Curves for a Darlington Circuit

	Lot I #0		Lot II #1		Lot III #2		Lot III #3	
T°C	V_{EB}, V	slope, mV/°C	V_{EB}, V	slope, mV/°C	V_{EB}, V	slope, mV/°C	V_{EB}, V	slope, mV/°C
25	1.153		1.168		1.179		1.165	
		4.28		4.28		4.20		4.44
50	1.046		1.061		1.074		1.054	
		4.48		4.48		4.44		4.48
75	0.934		0.949		0.963		0.942	
		4.60		4.60		4.56		4.64
100	0.819		0.834		0.849		0.826	
		4.84		4.80		4.76		4.88
125	0.698		0.714		0.730		0.704	
		5.12		5.04		5.04		5.04
150	0.570		0.588		0.604		0.578	

Table 9 — Comparison of Electrical and Infrared Measurements of Thermal Resistance on Two Darlington Devices

Device Technology	Circuit Type	Electrical Measurements (Both Transistors)		Infrared Measurements Transistor Q_2			
				Constricted Region		Non Constricted Region	
		ΔT, °C	R_θ, °C/W	ΔT, °C	R_θ, °C/W	ΔT, °C	R_θ, °C/W
Epitaxial Base	d	36	1.1	55	1.6	10-30	0.3-0.9
Single Diffused	d	25	0.7	38	1.1		

some were also measured by the emitter-and-collector switching method. Calibration curves were measured on four 10-A Darlington epitaxial-base transistor pairs of the same type (fig. 20d) taken from three lots with the same date code. The emitter-base series voltage, V_{EB}, was measured at intervals of 25°C with a measuring current, I_M, of 12 mA and a collector-emitter voltage, V_{CE}, of 12 V. The results are presented in table 8 which lists both the voltages measured at each temperature and the temperature coefficients calculated from voltage differences over each 25°C interval. Because of the non-linearity, which probably is caused by the presence of the integrated resistors, a calibration curve must be used when V_{EB} is used as the TSP. Note that the temperature coefficient is about twice that of a discrete transistor as would be expected since two junction voltages are being measured in series.

Preliminary infrared microradiometer measurements were made on two Darlington circuits after opening the cases. Because of the leakage multiplication inherent in Darlington transistor, the infrared measurement, which must be made on unprotected devices, is more difficult. It was necessary to heat the devices for an hour at 150°C to drive out moisture before measurements could be made on uncapped devices which had been stripped of their varnish or silicone rubber protective coating by methods which had proved satisfactory when testing discrete devices.

The results of these measurements, which showed hot spots due to a current constriction near the emitter of each output transistor, Q_2, are listed in table 9. In addition, the apparent temperature was measured electrically by the emitter-only switching method. The series voltage, V_{EB}, was used as the TSP, the voltage was measured at several time intervals after cessation of the power pulse and extrapolated back to zero time on a plot of voltage against the square root of time [38].

Although the deviation between the extrapolated electrical measurements and the infrared measurements of the hot spot temperature appears to be excessive when compared to previous measurements made at similar currents and voltages on discrete devices having similar active areas, it is not surprising when one considers that only one of the two series transistors, the output transistor, heats up significantly during operation while both transistors are uniformly heated during calibration. Further, since the base current of the output transistor, Q_2, is much greater than the base current of the input transistor, Q_1, the temperature coefficient of the emitter-base voltage of the output transistor is less than that of the emitter-base voltage of the input transistor.

The tentative conclusion from this preliminary work is that the thermal resistance of commercially available Darlington circuits can be measured by the emitter-only switching method in a conventional transistor test circuit although there is a significant decrease in sensitivity to hot

spots compared to that which would be expected when measuring discrete devices. It should also be noted that while measuring currents from 1 to 10 mA are suitable for measuring most discrete devices, currents from 12 to 100 mA were necessary to measure the Darlington devices studied.

(S. Rubin)

12.3. Transient Thermal Response

It has been shown that the cooling response of a semiconductor device is a function of the thermal distribution of the device at steady state (NBS Spec. Publ. 400-4, pp. 71-74). Further study has indicated that the steady state thermal characteristics of power transistors can be estimated from the cooling response curve [39].

In particular, it has been found that for times up to about 250 μs, one dimensional transient heat flow theory can be used to describe power transistor cooling:

$$T_J = T_{Js} - Kt^{1/2}$$

where T_J is the junction temperature at time t after power has been removed from the transistor, T_{Js} is the average junction temperature in steady-state operation, and K is a constant which is given by:

$$K = \frac{2P}{A(\rho\pi kc)^{1/2}}$$

where P is the power dissipated, A is the area of power dissipation, and ρ, k, and c are the density, thermal conductivity, and heat capacity of the material. For silicon, $\rho = 2.33$ g/cm^3 and $c = 0.71$ W·s/g·°C so K is equal to $0.877\ P/A\sqrt{k}$ where k is a function of temperature [40].

Consequently the cooling curve, when plotted as T_J against $t^{1/2}$, can be extrapolated to time, t, equal to zero to give an estimate of T_{Js}, and the slope of the cooling curve can be used to give an estimate of the effective area of power generation within the device at steady state.

As an aid in establishing the validity of the one dimensional cooling concept for power transistors, a computer program, TRUMP [41], was used to simulate a transistor cooling from the steady state condition. A model with cylindrical symmetry was used. In the model, the heat source is centered on the top surface of the chip and the chip rests on a copper heat sink the same diameter as the chip. The copper heat sink rests on an infinite heat sink, and the sides of the copper-silicon system and the top surface of the chip are assumed adiabatic. The variation with temperature of the thermal conductivity of silicon was taken into account.

Table 10 — Peak Temperature Cooling Curve Data

A, cm^2 (given)	T_{Js}, °C (calculated)	T_{Js}, °C (extrapolated)	k, W/cm·°C	A, cm^2 (from slope)
0.00277	186.7	182.5	0.83	0.00294
0.00565	107.2	106.5	1.10	0.00580

Table 11 — Average Temperature Cooling Curve Data

A, cm^2 (given)	T_{Js}, °C (calculated)	T_{Js}, °C (extrapolated)	k, W/cm·°C	A, cm^2 (from slope)
0.00277	157.8	149.0	0.92	0.00367
0.00565	90.7	88.1	1.15	0.00683

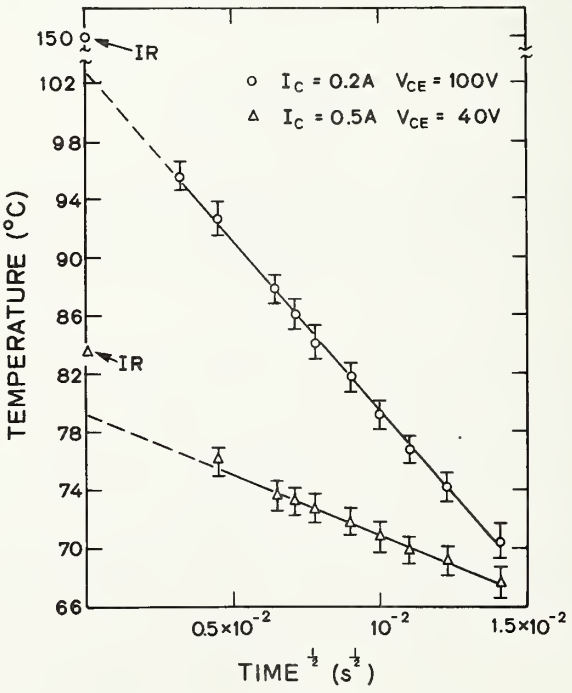


Figure 21. Measured cooling response of a power transistor. (The points labeled IR are temperature at steady state conditions as measured by an infrared microradiometer.)

Calculations were first made for the peak temperature as a function of time for two different heat source areas on a silicon chip 250 μm (10 mils) thick with a radius of 1.44 mm (57 mils) and a power dissipation of 25 W. The heat sources were assumed to have radii of 424 μm (16.7 mils) and 297 μm (11.7 mils) corresponding to 8.7 and 4.3 percent of the chip area respectively. These temperatures (for $t > 0$) were then plotted as a function of $t^{1/2}$. The steady state peak temperature was determined by extrapolating to $t = 0$ and the area of power generation was calculated from the slope using a value of thermal conductivity appropriate to the temperature. The results are given in table 10 where the extrapolated peak temperature is compared with the peak temperature calculated at $t = 0$ and the area is compared with the given area.

To simulate actual measurement conditions, the cooling response was also generated in terms of a spatially averaged temperature for the heat source of each size by multiplying the temperature at the center of each node (of the computer model) by the area of the node, then summing the products and dividing by the total area of the heat source. This was done as a first approximation to the way in which the electrical measurement techniques might average the junction temperature. These data were manipulated and plotted in the same way as the peak temperature data in order to obtain an extrapolated average temperature and the area of power generation. The results are shown in table 11.

It has also been found experimentally that the cooling curve follows the one dimensional model. As an example, two cooling curves for the same device at the same power, but different operating conditions are shown in figure 21. These curves are plotted as T_J against $t^{1/2}$ and extrapolated to steady state ($t = 0$). Also shown is the infrared determination of the peak temperature at steady state.

The slopes of the curves indicate that the portion of the chip area in which power is generated at steady state is 10.5 percent for the upper curve and 29 percent for the lower curve. The averaging effect of the electrical measurement is particularly severe for the smaller source in that the extrapolated electrical measurement at $t = 0$ is about 30 percent below the infrared measurement. For the larger heat source, though, the extrapolated measurement is only about 5 percent below the infrared measurement. In experiments with the transistors in this study the electrically-measured peak temperatures were not more than 15 percent below the peak temperatures measured by infrared when 30 percent or more of the chip was conducting. If less than 10 to 15 percent of the chip was conducting, the extrapolated electrical measurement was usually more than 40 percent below the infrared measurement. These results indicate that both experimental data and three dimensional computer simulations agree well with the theoretical predictions of the one dimensional heat flow model. (D. L. Blackburn and F. F. Oettinger)

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APPENDIX A

SEMICONDUCTOR TECHNOLOGY PROGRAM STAFF

Coordinator: J. C. French*
Secretary: Miss B. S. Hope*
Consultant: C. P. Marsden¶†

Semiconductor Characterization Section

(301) 921-3625

Dr. W. M. Bullis, Chief
Dr. M. G. Buehler, Asst. Chief

F. H. Brewer
Miss F. C. Butler+
M. Cosman
Mrs. K. E. Dodson+
Dr. J. R. Ehrstein
Dr. R. Y. Koyama
Mrs. K. O. Leedy
Dr. D. C. Lewis
Dr. A. G. Lieberman
R. L. Mattis
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H. A. Schafft, Asst. Chief — Processing

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G. G. Harman
Miss D. L. Hines+
W. J. Keery
H. K. Kessler
J. Krawczyk
T. F. Leedy
Y. M. Liu
Miss C. A. Main
Dr. D. B. Novotny
L. M. Smith
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Electron Devices Section

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D. W. Berning
Mrs. A. D. Glover+
Mrs. B. A. Oravec¶+
M. K. Phillips
M. C. Rhodes¶
G. J. Rogers
S. Rubin
D. E. Sawyer
L. R. Williams

¶ Part Time
+ Secretary
× Summer
* Telephone: (301) 921-3357
† Telephone: (301) 921-3621

APPENDIX B

SEMICONDUCTOR TECHNOLOGY PROGRAM PUBLICATIONS

B.1. Prior Reports

A review of the early work leading to this Program is given in Bullis, W. M., Measurement Methods for the Semiconductor Device Industry — A Review of NBS Activity, NBS Tech. Note 511, December, 1969.

Quarterly reports covering the period July 1, 1968, through June 30, 1973, were published as NBS Technical Notes with the title, Methods of Measurement for Semiconductor Materials, Process Control, and Devices:

Quarter Ending	NBS Tech. Note	Date Issued	NTIS Accession No.
September 30, 1968	472	December 1968	AD 681330
December 31, 1968	475	February 1969	AD 683808
March 31, 1969	488	July 1969	AD 692232
June 30, 1969	495	September 1969	AD 695820
September 30, 1969	520	March 1970	AD 702833
December 31, 1969	527	May 1970	AD 710906
March 31, 1970	555	September 1970	AD 718534
June 30, 1970	560	November 1970	AD 719976
September 30, 1970	571	April 1971	AD 723671
December 31, 1970	592	August 1971	AD 728611
March 31, 1971	598	October 1971	AD 732553
June 30, 1971	702	November 1971	AD 734427
September 30, 1971	717	April 1972	AD 740674
December 31, 1971	727	June 1972	AD 744946
March 31, 1972	733	September 1972	AD 748640
June 30, 1972	743	December 1972	AD 753642
September 30, 1972	754	March 1973	AD 757244
December 31, 1972	773	May 1973	AD 762840
March 31, 1973	788	August 1973	AD 766918
June 30, 1973	806	November 1973	AD 771018

After July 1, 1973 quarterly reports were issued in the NBS Special Publication 400 subseries with the title, Semiconductor Measurement Technology:

Quarter Ending	NBS Spec. Publ.	Date Issued	NTIS Accession No.
September 30, 1973	400-1	March 1974	AD 775919
December 31, 1973 March 31, 1974	400-4	November 1974	

B.2. Current Publications

As various phases of the work are completed, publications are prepared to summarize the results or to describe the work in greater detail. Publications of this kind which have been issued recently are listed below:

Sandow, P. M., A Transistor with Simultaneously Diffused Emitter and Base, *Solid-State Electronics* 17, 404-406 (April 1974).

Harman, G. G., A Metallurgical Basis for the Non-Destructive Wire Bond Pull Test, *12th Annual Proceedings, Reliability Physics 1974,* Las Vegas, Nevada, April 2-4, 1974, pp. 205-210. (Available from Publications Sales Dept., The IEEE, 345 E. 57th Street, New York, New York 10017, Catalog No. 74CH0839-1PHY.)

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Forman, R. A., Thurber, W. R., and Aspnes, D. E., The Second Indirect Band Gap in Silicon, *Solid-State Communications* 14, 1007-1010 (May 1974).

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Buehler, M. G., *Semiconductor Measurement Technology:* Microelectronic Test Patterns: An Overview, NBS Spec. Publ. 400-6 (August 1974).

Lewis, D. C., On the Determination of the Minority Carrier Lifetime from the Reverse Recovery Transient of *pn*R Diodes, *Solid-State Electronics,* to appear.

Ciarlo, D. R., Schultz, P. A., and Novotny, D. B., Automated Inspection of IC Photomasks, *Technological Advances in Micro and Sub-Micro Photofabrication Imagery,* Society of Photo-Optical Instrumentation Engineers, San Diego, California, August 21-23, 1974, to appear.

Ehrstein, J. R., ed., *Semiconductor Measurement Technology:* Spreading Resistance Symposium, NBS Spec. Publ. 400-10 (December 1974).

Ehrstein, J. R., Improved Surface Preparation For Spreading Resistance Measurements on *p*-type Silicon, *Semiconductor Measurement Technology:* Spreading Resistance Symposium, J. R. Ehrstein, ed., NBS Spec. Publ. 400-10 (December 1974), pp. 249-255.

Rogers, G. J., Sawyer, D. E., and Jesch, R. L., *Semiconductor Measurement Technology:* Measurement of Transistor Scattering Parameters, NBS Spec. Publ. 400-5 (December 1974).

B.3. Availability of Publications

In most cases reprints of articles in technical journals may be obtained on request to the author. NBS Technical Notes and Special Publications are available from the Superintendent of Documents, U.S. Government Printing Office, Washington, D. C. 20402, or the National Technical Information Service, Springfield, Virginia 22161, or both. Current information regarding availability of all publications issued by the Program is provided in the latest edition of NBS List of Publications No. 72 which can be obtained on request to Mrs. K. O. Leedy, Room B346, Technology Building, National Bureau of Standards, Washington, D. C. 20234.

APPENDIX C

WORKSHOP AND SYMPOSIUM SCHEDULE

C.1. Proceedings or Reports of Past Events:

Symposium on Silicon Device Processing, Gaithersburg, Maryland, June 2-3, 1970. (Cosponsored by ASTM Committee F-1 and NBS). Proceedings: NBS Spec. Publ. 337 (November 1970).

ARPA/NBS Workshop I. Measurement Problems in Integrated Circuit Processing and Assembly, Palo Alto, California, September 7, 1973. Report: NBS Spec. Publ. 400-3 (January 1974).

ARPA/NBS Workshop II. Hermeticity Testing for Integrated Circuits, Gaithersburg, Maryland, March 29, 1974. Report: NBS Spec. Publ. 400-9 (to appear).

Spreading Resistance Symposium, Gaithersburg, Maryland, June 13-14, 1974. (Cosponsored by ASTM Committee F-1 and NBS). Proceedings: NBS Spec. Publ. 400-10 (to appear).

ARPA/NBS Workshop III. Test Patterns, Scottsdale, Arizona, September 6, 1974. Report: NBS Spec. Publ. 400-15 (to appear).

C.2. Calendar of Future Events:

ARPA/NBS Workshop IV. Silicon Surface Analysis, Gaithersburg, Maryland, April 23-24, 1975. For information, contact K. O. Leedy (301) 921-3625.

APPENDIX D

STANDARDS COMMITTEE ACTIVITIES

ASTM Committee F-1 on Electronics

M. G. Buehler, Semiconductor Measurements Subcommittee; Process Controls Section

W. M. Bullis, Editor, Semiconductor Crystals Subcommittee; Secretary, Editorial Subcommitee; Semiconductor Measurements, Semiconductor Processing Materials, Hybrid Microelectronics, and Quality and Hardness Assurance Subcommittees; Insulating Materials Section; Advisory Committee

J. R. Ehrstein, Chairman, Resistivity Section; Semiconductor Crystals, Semiconductor Processing Materials, Semiconductor Measurements and Hybrid Microelectronics Subcommittees

J. C. French, Chairman, Editorial Subcommittee; Secretary, Advisory Committee; Semiconductor Crystals, Semiconductor Processing Materials, Semiconductor Measurements, Hybrid Microelectronics and Quality and Hardness Assurance Subcommittees

G. G. Harman, Secretary, Interconnection Bonding Section

B. S. Hope, Committee Assistant Secretary

K. O. Leedy, Chairman, Interconnection Bonding Section

T. F. Leedy, Dielectrics Section

D. C. Lewis, Semiconductor Crystals, Semiconductor Processing Materials, Semiconductor Measurements, Hybrid Microelectronics, and Quality and Hardness Assurance Subcommittees

C. P. Marsden, Committee Secretary; Advisory Committee

R. L. Mattis, Semiconductor Crystals, Semiconductor Measurements, and Editorial Subcommittees

D. B. Novotny, Editor, Semiconductor Processing Materials Subcommittee

W. E. Phillips, Chairman, Lifetime Section; Secretary, Semiconductor Crystals Subcommittee; Semiconductor Processing Materials; Semiconductor Measurements, and Hybrid Microelectronics Subcommittees

G. J. Rogers, Quality and Hardness Assurance Subcommittee

S. Ruthberg, Semiconductor Processing Materials, Hybrid Microelectronics, and Quality and Hardness Assurance Subcommittees

A. H. Sher, Semiconductor Crystals, Semiconductor Processing Materials, and Hybrid Microelectronics Subcommittees

W. R. Thurber, Semiconductor Crystals and Semiconductor Measurements Subcommittees

ASTM Committee E-10 on Radioisotopes and Radiation Effects

W. M. Bullis, Subcommittee 7, Radiation Effects on Electronic Materials

J. C. French, Subcommittee 7, Radiation Effects on Electronic Materials

D. C. Lewis, Subcommittee 7, Radiation Effects on Electronic Materials

Electronic Industries Association: Solid State Products Division, Joint Electron Device Engineering Council (JEDEC)

F. F. Oettinger, Chairman, Task Group JC-11.3-1 on Thermal Considerations for Microelectronic Devices, Committee JC-11.3 on Mechanical Standardization for Microelectronic Devices; Chairman, Task Group JC-25-5 on Thermal Characterization of Power Transistors, Committee JC-25 on Power Transistors; Technical Advisor, Thermal Properties of Devices, Committees JC-22 on Rectifier Diodes and Thyristors, JC-20 on Signal and Regulator Diodes, and JC-30 on Hybrid Integrated Circuits

S. Rubin, Chairman, Council Task Group on Galvanomagnetic Devices

D. E. Sawyer, Task Group JC-24-5 on Transistor Scattering Parameter Measurement Standard, Committee JC-24 on Low Power Transistors

H. A. Schafft, Technical Advisor, Second Breakdown and Related Specifications Committee JC-25 on Power Transistors

Electronic Industries Association: Government Products Division

F. F. Oettinger, Chairman, Task Group G-12-08-74 on Recommendations for Military Usage of Proposed Standards and Test Methods for Thermal Resistance, Committee G-12 on Solid State Devices

IEEE Electron Devices Group

J. C. French, Standards Committee

H. A. Schafft, Standards Committee Task Force on Second Breakdown Measurement Standards

IEEE Magnetics Group

S. Rubin, Chairman, Galvanomagnetic Standards Subcommittee

Society of Automotive Engineers

J. C. French, Subcommittee A-2N on Radiation Hardness and Nuclear Survivability

W. M. Bullis, Planning Subcommittee of Committee H on Electronic Materials and Processes

IEC TC47, Semiconductor Devices and Integrated Circuits

S. Rubin, Technical Expert, Galvanomagnetic Devices; U.S. Specialist for Working Group 5 on Hall Devices and Magnetoresistive Devices

APPENDIX E

SOLID-STATE TECHNOLOGY & FABRICATION SERVICES

Technical services in areas of competence are provided to other NBS activities and other government agencies as they are requested. Usually these are short-term, specialized services that cannot be obtained through normal commercial channels. Such services provided during the last quarter, which are listed below, indicate the kinds of technology available to the program.

E.1. Thin Metal Films (J. Krawczyk)

Thin films of aluminum and gold were evaporated onto the front and back sides, respectively, of silicon wafers intended for MOS device production for the Harry Diamond Laboratories.

E.2. Semiconductor Device Assembly (J. Krawczyk)

Silicon wafers containing arrays of transistors were scribed, the resulting dice attached to TO-5 headers, and the devices bonded with gold wire leads for the Harry Diamond Laboratories.

E.3. Scanning Electron Microscopy (W. J. Keery)

Scanning electron micrographs of a proposed SEM magnification standard were taken for the NBS Lattice Defects and Microstructures Section.

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16. ABSTRACT (*A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.*)

This quarterly progress report describes NBS activities directed toward the development of methods of measurement for semiconductor materials, process control, and devices. The emphasis is on silicon device technologies. Principal accomplishments during this reporting period include (1) identification of surface preparation procedures which improve the quality of spreading resistance measurements, (2) preparation of a videotaped tutorial discussion of thermally stimulated current and capacitance measurements, (3) completion of an analysis of the apparent position of an opaque edge when viewed with incoherent and coherent illumination, and (4) completion of the construction of a flying-spot scanner. Results are also reported on capacitance-voltage and two-probe resistivity measurements; analyses of thermally stimulated current and capacitance measurements on metal-oxide-semiconductor (MOS) capacitors; a review of methods for characterizing interface states associated with thin oxide films on silicon; fabrication of a test pattern based on the charge-coupled device; a preliminary comparison of filar and image shearing eyepieces for line-width measurement; a review of technologies in use for photomask inspection and measurements; procedures for determination of correct photoresist exposure; epitaxial layer thickness; scanning electron microscopy; mathematical modeling of ultrasonic bonding; leak test procedures; thermal resistance measurements on transistors and Darlington pairs, and transistor thermal response measurements. Supplementary data concerning staff, publications, workshops and symposia, standards committee activities, and technical services are also included as appendices.

17. KEY WORDS (*six to twelve entries; alphabetical order, capitalize only the first letter of the first key word unless a proper name; separated by semicolons*)

Boron redistribution; Darlington pairs; dopant profiles; electrical properties; electronics; epitaxial layer thickness; flying-spot scanner; gold-doped silicon; hermeticity; measurement methods; microelectronics; micrometrology; MOS devices; oxide films; photomasks; photoresist; resistivity; scanning electron microscopy; semiconductor devices; semiconductor materials; semiconductor process control; silicon; spreading resistance; test patterns; thermal resistance; thermal response; thermally stimulated capacitance; thermally stimulated current; ultrasonic bonding; voltage contrast mode; wire bonds.

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