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Semiconductor Measurement Technology:

Differential Capacitance-Voltage Profiling of Schottky Barrier Diodes for Measuring Implanted Depth Distributions in Silicon

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PREFACE

This study was carried out at the Hughes Research Laboratories (HRL) as a part of the Semiconductor Technology Program at the National Bureau of Standards. The Semiconductor Technology Program serves to focus NBS efforts to enhance the performance, interchangeability, and reliability of discrete semiconductor devices and integrated circuits through improvements in measurement technology for use in specifying materials and devices in national and international commerce and for use by industry in controlling device fabrication processes. The work was supported by the Defense Advanced Research Projects Agency, ARPA Order 2397, Program Code 6D10, through the National Bureau of Standards' Semiconductor Technology Program, Contract 5-35891. This contract was monitored by Dr. Kenneth F. Galloway as the Contracting Officer's Technical Representative. Drs. W. M. Bullis, K. F. Galloway, and D. R. Myers provided technical review of this report for the National Bureau of Standards.

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This report discusses experimental and analytical aspects of differential capacitance-voltage profiling of ion-implanted carrier depth distributions using reverse-biased Schottky barrier diodes and the associated accuracies, experimental errors, and ranges of applicability.

Key words: automatic C-V profiler analyses; carrier depth distributions; differential capacitance-voltage profiling; ion implantation; ranges of application and limitations; Schottky barrier diodes; SIMS and C-V profile comparisons.

1. INTRODUCTION

1.1 The Purpose and Application

The general purpose of this report is to provide practical information and experimental data that will aid in the accurate design and fabrication of ion-implanted dopant profiles. Implantation is often utilized because it is known to be capable of greater control of dopant profiles than other dopant techniques. This potential superiority of implantation is lost in the practical world of device and circuit fabrication unless adequate knowledge and control of the range and shape of the implanted ion depth distribution and the factors that influence them are available. Knowledge of these factors and their application by the semiconductor device and integrated circuit industry should lead to increased production yield, field reliability, and device performance through the greater accuracy and tighter specifications that can be held through the use of the implantation dopant process.

The specific goal of the work described in this report was to establish controlled and reproducible Schottky barrier diode and differential capacitance-voltage profiling technologies for measuring depth distributions or profiles of p- and n-type ion-implanted layers in silicon. Differential capacitance-voltage (C-V) profiling measures the depth distribution of carriers (electrons or holes) in a semiconductor in the carrier density range from 10^{13} to 10^{18} cm^{-3}. One application for which it is useful is the measurement of depth distributions of carriers resulting from ion implantation of semiconductors where the ion fluence or dose is less than about 10^{13} cm^{-2}.

The capacitance-voltage and capacitance-frequency behavior of semiconductor devices can be used in the evaluation of material purity, impurity density and depth distributions, interface-state and deep-level impurity densities and response times, insulator purity and thickness, and insulator effects on surface behavior of semiconductor devices. Differential C-V measurements of reverse-biased diodes can be used to determine the presence of electrically active carriers and to plot their density profiles. This technique measures directly the density of carriers without requiring associated mobility measurements and corrections for varying mobility. The technique is applicable to compound semiconductors, for which controlled layer removal (stripping) is difficult.

The differential C-V profiling technique and its accuracy and limitations have been described by a number of authors, including its originators, Thomas, Kahng, and Manz [1], and others [2-10]. Schottky diodes were used in this work because they provide a good approximation to the step junction model on which the equations for differential C-V profiling are based; in fact, Amron [2] concludes that "whenever possible, Schottky diodes should be used..."

1.2 Ion-Implanted Depth Distributions

A treatment that has come to be known as the LSS theory after its developers [11] models the semiconductor host as a dense gas to represent an amorphous solid, and predicts a Gaussian depth distribution for implanted atoms, characterized by a projected mean depth or range R_p and a characteristic width or standard deviation σ or range straggle ΔR_p, defined as the half-width at $e^{-1/2}\ N_{max}$. Calculations of R_p and ΔR_p have been made by many workers [12-17].

The introduction of higher order moments into these statistical treatments can explain shapes that differ from the Gaussian distribution. An example of such a treatment is the Pearson IV used by Hofker [18], which considers a third moment called skewness (γ_1) and a fourth moment called kurtosis (β_2), the first and second moments being the average range or mode (R_m or μ) and range straggle or standard deviation (ΔR_p or σ), respectively. The calculated range R_p may be greater than or less than the first moment depending upon whether the third moment is negative or positive.

The LSS theory assumes the substrate to be amorphous. In practice, most semiconductor substrates that are implanted are crystalline rather than amorphous. Because of the crystalline nature of the substrate, experimentally measured depth distributions can be different from the calculated distribution. The crystalline substrate can be oriented so as to appear relatively amorphous or atomically random in the direction of the incident ions to best simulate the assumed amorphous condition of the LSS theory; this is the "random equivalent" orientation. However, in this so-called "random equivalent" orientation of the crystalline substrate, some ions can penetrate deeper than the calculated range R_p to produce a "channeling tail" on the deep side of the depth distribution. The magnitude of this tail depends on the variables that occur in the expression for the critical angle for channeling ψ_c [19], which are the ion and substrate masses, the ion energy, and the substrate lattice spacings. Its magnitude

also depends on the degree of crystallinity or openness of the axial and planar channels of the substrate lattice which is also affected by the amount of accumulated damage that is produced by the prior implantation. Thus, the final distribution depends on the total ion fluence or dose, the tail being more significant for low fluences and becoming less significant as damage increases, until saturation occurs when the substrate becomes amorphous as a result of the implantation damage. The saturated magnitude of the tail remains as the ion fluence increases. "Amorphization fluences" vary with the mass of the ion from about 10^{14} to 10^{16} cm^{-2}.

Ions can also be implanted along the open low-index directions of the semiconductor crystal, in which case the ions have a greater probability of being guided or channeled deeper into the crystal down the axial and planar channels. This effect occurs until the lattice is damaged enough by the ions that are not channeled to a deep range to be made amorphous in the implanted region, that is, when the axial channels become blocked. The amorphization fluence in these cases is higher (by a factor of ~2 to 5).

1.3 Ranges of Application and Limitations

The technique of differential C-V profiling is applicable to most semiconductor materials. It is ideal for determining depth distributions for lower fluence implants, for measuring channeling tails on distributions in crystalline substrates, and for measuring channeled distributions. It is especially useful for studies where a large number of samples need to be examined or a large number of values of variables are required, because the sample processing is simple and the experimental measurement of the profile requires only a short time. It is much faster than the method of controlled layer removal (stripping) with Hall measurement of the carriers. The technique is useful for estimating the energy levels of deep acceptor or donor states of implanted species by estimating the shift in depth of the peaks of the implanted profiles [20,21]. This latter measurement requires the knowledge of the depth of the implanted atoms, for example, by an LSS range calculation. Thus, there may be some error associated with this measurement resulting from differences between calculated and actual ranges.

Kennedy and O'Brien [3] argue that differential C-V profiling measures the majority carrier distribution and this distribution may differ from that of the atom depth distribution. However, this effect is small for profiles deeper than about 0.5 μm and causes only a small correction (~1 to 5 percent in depth) to the C-V profiles for densities below about 10^{15} cm^{-3}, as shown in section 5.1 of this report and by Moline [4], Moline and Reutlinger [22], and Reddi and Sansbury [6], and by comparisons of C-V carrier profiles and secondary-ion-mass spectroscopy (SIMS) atom profiles for samples implanted with the same or slightly different ion fluences. Evaluations of range, straggle, skewness, and kurtosis are made near the peak of the depth distribution, or above ~10^{15} cm^{-3}, and are little affected by the "Kennedy-O'Brien correction." The "Kennedy-O'Brien correction" does have an effect in the region of channeling tails on random equivalent implants in crystalline materials; the magnitude of the correction decreases with increasing depth of the profile (see sec. 5.1).

The range of depth that can be measured by differential C-V profiling of Schottky barriers is about 0.08 μm to 10 μm. These extremes cannot be measured in a single profile, however. A rule of thumb is that the depth distribution can extend over one order of magnitude in depth. For example, a distribution that extends to a depth of 0.8 μm might give information to within 0.08 μm of the surface, but a distribution that extends to 6 μm would give data only to within about 0.6 μm of the surface. The zero bias depletion depth, which is the controlling factor for the shallow side, varies with the depth of the charges and the density of the dopants (the profile itself). Depths of 0.08 μm to 8 μm are associated with the general range of ion energy from 10 to 1,000 keV, depending upon the mass of the implanted ion.

Effects of annealing temperature and implantation temperature can be followed by C-V profiling. The technique is not useful for high ion fluences nor for ion species that do not produce carriers in the crystal.

A more widely applicable, but physically destructive, method for depth profiling electrical activity is the measurement of spreading resistance on beveled specimens. Spreading resistance and its comparison with C-V and SIMS techniques are described by Albers *et al.* [23].

2. DIFFERENTIAL C-V PROFILING

2.1 The Technique

The basic concept underlying all capacitance measurements of charge density in semiconductor devices is Poisson's equation, expressed in one dimension as:

$$\frac{d^2V}{dx^2} = \frac{\rho(x,\ldots)}{\varepsilon} , \qquad (1)$$

where x is the distance measured parallel to the applied electric field and ρ, V, and ε are the total charge density, electrostatic potential, and permittivity, respectively, all measured at x. In general, ρ may be a function of x, angular frequency (ω), temperature (T), and other variables. By measuring the dependence of ρ on one or more of these parameters by capacitance measurements, it is possible to determine characteristics of the charge distribution in particular devices and implanted regions. For cases where the energy level of the impurity is such that not all of the impurities are ionized at ambient temperature, e.g., for indium in silicon at 300 K, the applied voltage may ionize the remainder.

The device geometries most frequently evaluated by capacitance techniques are generally of two classes: (1) rectifying junction devices and (2) field effect devices [metal-oxide semiconductors (MOS) and metal-insulator semiconductors (MIS)]. The first class includes metal-semiconductor surface barrier (Schottky) diodes, one-sided (step) p-n junctions where one side is heavily doped compared with the other, and multilayer junction devices. Schottky barrier diodes of p^+n and pn^+ junctions are frequently referred to as one-sided junctions because essentially all of the bias voltage drop

occurs across the more lightly doped side of the junction. The second class includes MOS and MIS capacitors and other devices in which the field plates of the capacitor are separated by an essentially nonconducting layer. Because the information available from capacitance measurements for the two classes of devices is different, the two classes are treated separately.

In rectifying devices, the free carrier density n (at thermal equilibrium) can be obtained directly as a function of distance x from the junction by C-V techniques. With the assumption of completely ionized impurities and an abrupt depletion region edge, the dopant density and depth relationships are:

$$n(x) = \frac{C^3}{e\varepsilon A^2 \frac{dC}{dV}} \tag{2a}$$

and

$$x = \frac{\varepsilon A}{C} , \tag{2b}$$

where A is the area of the device, and x is the depletion width or space-charge region width. As the reverse-bias voltage V is increased, the depletion width x increases, causing a decrease in capacitance. The area of junction A must be known well or a significant error can result in n(x). One advantage of C-V profiling is that the probing rf voltage can be on the order of kT (~25 mV at room temperature), thereby minimizing errors caused by rectification and diffusion capacitance at low reverse bias voltage. The quantity measured in eqs (2a) and (2b) is the carrier density. It is possible, however, to determine the ionized impurity density by further differentiation of the C-V data. For completely ionized impurity species in nondegenerate *n*-type material, Poisson's equation is given by:

$$\frac{d^2V}{dx^2} = \frac{e}{\varepsilon} \left[n(x) - n_D(x) \right], \tag{3}$$

where $n_D(x)$ is the donor density. Kennedy and O'Brien [3] show that:

$$\frac{d^2V}{dx^2} = - \frac{d}{dx} \left[\frac{kT}{e} \frac{1}{n(x)} \frac{dn(x)}{dx} \right]. \tag{4}$$

Substituting eq (4) into eq (3) and solving for $n_D(x)$ gives

$$n_D(x) = n(x) + \frac{kT\varepsilon}{e^2} \frac{d}{dx} \left[\frac{1}{n(x)} \frac{dn(x)}{dx} \right]. \tag{5}$$

This correction to obtain the dopant density from the measured carrier density is discussed in more detail in section 5.1.

Capacitance-voltage data can be obtained using capacitance bridge measurements at a single high frequency (f ~ 10^5 to 10^6 Hz), while the applied bias is changed aperiodically at an average repetition rate of the

order of 0.01 to 0.1 Hz. The effect of deep impurities on such measurements is important. Impurities with response time slower than the periodic time of the high frequency signal affect the C-V relationship by altering the static depletion layer width (because they can equilibrate with the bias changes), but do not alter the high frequency variation in the depletion layer width (because they cannot equilibrate with the high frequency). Measurements of the variation of the C-V curves with frequency can yield information concerning the response times, energy levels, and densities of deep electrically active impurities [24,20].

The capacitive behavior of MOS structures is more difficult to analyze than that of simple rectifying junction devices. However, a wealth of information can result from available analysis techniques. Capacitance-voltage measurements at a fixed frequency provide a method of determining fixed charge density in the insulator region, interface density, insulator thickness, and impurity density in the semiconductor region. Combined with capacitance measurements *versus* frequency at fixed biases, these measurements can be used to determine surface potential, standard deviation of surface potential, and interface state density and majority carrier cross section as a function of surface potential [25,26].

There are several reasons why profiling measurements by the bridge technique may not be desirable. First, most analyses involve differentiation of the capacitance data. The consequent loss of data can be severe, and potentially important effects can be entirely overlooked in such an analysis. Thus, continuous measurements are clearly desirable from a statistical point of view, if the measurement accuracy of the continuous method approaches that of a bridge technique. Secondly, the length of time required to perform the full set of measurements needed for a complete analysis is sufficient to make evaluation of a large number of samples prohibitive. Further, potentially important effects may be overlooked because of the unwieldiness of the bridge technique. For these reasons, automatic C-V plotting instruments have been developed, particularly for the evaluation of impurity density *versus* distance in Schottky and junction devices, for example, the second harmonic method of Copeland [27]; the mixed frequency technique of Baxandall [28]; and the techniques of Gordon, Stover, and Harp [29]; Anderson, Baron, and Crowell [30]; and Miller [31]. The technique of Gordon *et al.* overcame many of the problems encountered with the rf harmonic techniques by utilizing the 1-kHz ac signal directly, rather than the harmonic.

There are two general categories of sample preparation for C-V profiling measurements in rectifying junction devices - Schottky barrier or junction. Schottky barriers create a better approximation to the step junction model, are more convenient, and are a nondestructive way to make contact. However, they may be leaky and may not always allow complete depletion of materials with high breakdown voltages. Interfacial effects at the metal-semiconductor junction can cause anomalous current-voltage (I-V) and C-V behavior. Fabrication of a p-n junction requires more steps, but produces a diode with excellent leakage characteristics. For a Schottky barrier, a suitable metal such as titanium or aluminum is used on p-type silicon, or gold is used for n-type silicon and for gallium arsenide. The metal dots may be either evaporated through a mask or produced by photolithographic techniques. A p-n

junction can be formed by diffusion, ion implantation, or epitaxial growth of a p-layer on an n-region, followed by metallization and etching of a mesa junction. In either of the above procedures, a back ohmic contact is also prepared, for example, by implantation. During profiling, the p-n junction is reverse biased and the depletion region extends toward the n-substrate. It is not necessary to fabricate a mesa in order to obtain profiling data. Buehler [32] has worked out corrections for a planar diode geometry. Before profiling, it is important to check the I-V characteristics of the sample, to determine whether the device is leaky, and in the cases where avalanche breakdown occurs, what maximum voltage can be used to profile accurately.

For a junction device, a C-V profile gives information near the junction and not necessarily near the peak of an implanted distribution. Profiles are usually measured in high resistivity or in lightly doped material (low implantation dose) to avoid avalanche breakdown. Surface effects, like inversion layers, can contribute to the capacitance and cause errors. Errors at lower dopant densities can result from the presence of significant free carrier distributions (see the discussion of the Kennedy-O'Brien correction, sec. 5.1). Charge neutrality in implanted semiconductors is discussed by Grimshaw and Osborne [33]. For n^+ in n- or p^+ in p-material, C-V measurements may not distinguish between dopant species with shallow energy levels and other deep-level charge centers. The accuracy of the measurements can be verified by making DLTS or Hall measurements to determine the energy level of the dopant species. Another problem can be that heavily doped samples become inductive, making C-V profiling invalid for heavily doped regions ($> \sim 10^{18}$ cm^{-3}). Limitations of the C-V technique for ion-implanted profiles are discussed by Wu *et al.* [7], but most of their chosen analytical profiles are not encountered in careful C-V profiling done within the region of validity of the techniques.

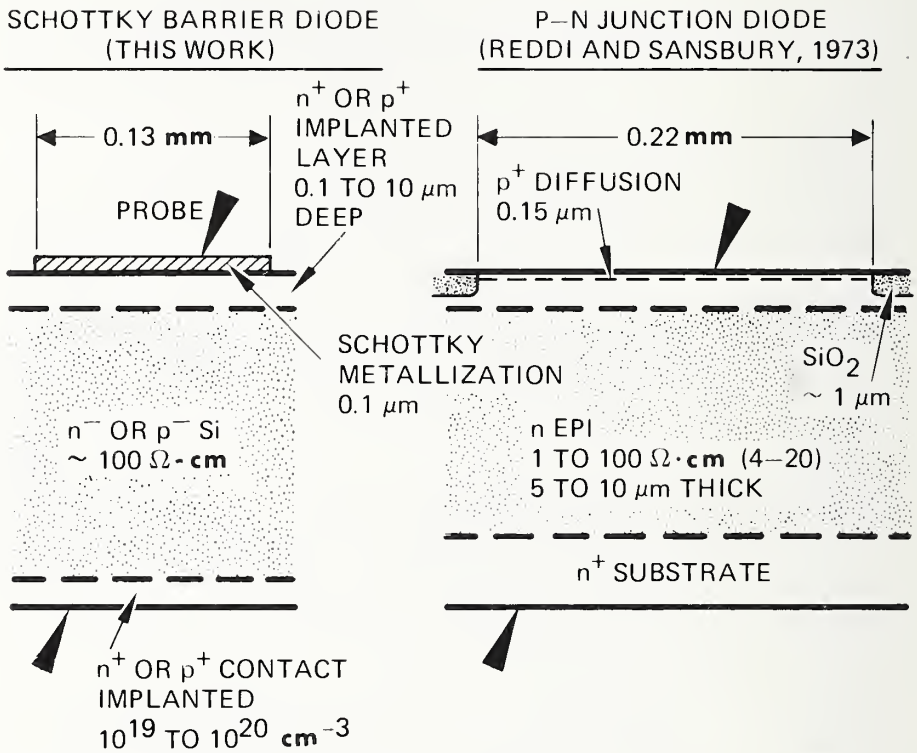
A differential C-V profiler calculates the carrier distribution by measuring the equivalent capacitance C and changes in the capacitance with applied voltage dC/dV of a reverse-biased diode. The area A of the diode must be measured independently and fed into the profiler which calculates (by analog or digital techniques) n(x) and x from the equations

$$n(x) = \frac{\left(C_{eq}\right)^3}{q\varepsilon A^2 \left(\frac{dC_{eq}}{dV}\right)} , \tag{6a}$$

$$x = \frac{eA}{C_{eq}} , \tag{6b}$$

as in eq (2), but where C_{eq} is the equivalent capacitance measured by the profiler which is related to the true diode capacitance C_s as follows:

$$C_{eq} = \frac{C_s}{\left[1 + \left(\omega C_s R_s\right)^2\right]} = \frac{C_s}{\left(1 + Q_s^{-2}\right)} , \tag{7}$$



ADVANTAGES OF SCHOTTKY BARRIER:

PROFILE CLOSER TO SURFACE: LOWER ION ENERGY OR HIGHER Z

BOTH PEAK AND TAIL IN SAME PROFILE

Figure 1. Diode configurations for C-V profiling.

where $Q_S = (\omega C_S R_S)^{-1}$. In this expression, $\omega = 2\pi f$ where f is the frequency of the profiler measuring circuit, C_S is the true diode capacitance, and R_S is the resistance of the diode. It is shown below that small diodes are required for good accuracy in differential C-V profiling.

Two diode configurations are illustrated in figure 1. As noted on the figure, two advantages of the Schottky barrier technique are the ability to measure the profile somewhat closer to the surface for shallow depth distributions (~80 nm *versus* ~150 nm), and to measure both the peak and the tail of a given distribution in the same profile, that is, with the same diode. Neither diode geometry will allow the profile to be measured close to the surface if the profile extends deeply into the substrate (e.g., greater than 1 μm). The Schottky barrier technique does not require correction for back depletion effects, see, e.g., [32].

This report discusses experimental work which used only the Schottky barrier technique; a description of use of the *p-n* junction technique is given by Reddi and Sansbury [6]. In the work reported here, a vacuum hold-down applied to the reverse side of the silicon wafers provided good electrical contact to the reverse side of the samples, as well as mechanical stability during the measurements. A 25-μm gold probe under compression provided the electrical contact to the 0.13- and 0.25-mm diameter Schottky barrier metallizations. For all samples studied, except for a few very deep implants, the C-V profiles were obtained for reverse biases well below the avalanche breakdown voltages of the Schottky diodes, which varied from as high as 120 V for deeper implants to about 10 V for shallow implants. Photosensitivity of the Schottky diodes was checked frequently to ensure that no errors occurred in the depth profiles as a result of incident ambient light.

As Amron [2] points out, any underestimation of the geometric (measured) areas of the Schottky diodes (metallizations) causes the computed values of n(x) and x to be larger and smaller, respectively, than the true values, causing the measured C-V profiles to be higher in n(x) and closer to the surface than the actual carrier depth distributions. This is in agreement with our observation that when a difference is observed between profiles measured by the differential C-V technique and by the SIMS technique, the C-V profile is slightly nearer the surface and sometimes slightly higher. Amron [2] also points out that in the use of the experimental $\Delta C/\Delta V$ to approximate dC/dV in the profiling equations, $\Delta C/\Delta V < dC/dV$ for all values of $\Delta C/C$ and the approximation error becomes larger as $\Delta C/C$ increases (ε in Amron's notation). Therefore, the computed values of n(x) are greater than the true values of n(x).

2.2 The Procedure

The steps in this ion-implanted electrical dopant profile measurement technology in silicon (differential C-V profiling using reverse-biased Schottky diodes) are:

- Design experiment: ions, energies, fluences, silicon orientations, angles, and implantation and annealing temperatures;
- Select, identify, and prepare material;

- Implant contacts;
- Perform experimental implants;
- Anneal implants;
- Anneal contacts (sinter, if evaporated);
- Deposit Schottky diode metallizations;
- Measure Schottky diode areas;
- Measure I-V characteristics, zero-bias capacitance values, and check breakdown voltages;
- Evaluate and select Schottky diodes for profiling;
- Measure differential C-V profiles;
- Analyze, reduce, and compare data;
  - Perform Kennedy-O'Brien correction;
  - Subtract background substrate dopant density;
  - Check reproducibility; and
  - Check for time stability.

2.3 Profiler Circuit Analysis

The capacitance meter in differential C-V profiling circuitry measures the parallel equivalent circuit shown in figure 2. The analysis that follows assumes that the phase angle of the measuring circuit in the capacitance meter for the diodes is small enough that any resulting error is negligible. That is, it is assumed that $\phi G_{eq}/\omega$ is negligible compared with the value of capacitance C_{eq}. This subject is discussed by Anderson, Baron, and Crowell [30]. The phase rejection error of the C-V profiler used in our work is quoted as 1 percent at $Q_s = 3$; we measured an error of ~1 percent at $Q_s = 1$ so the instrument specification is conservative and the phase error is negligible, as assumed above. The circuit actually "seen" by the capacitance meter is shown in figure 3. The shunt resistance R_{sh} is so large ($>10^7$ Ω) for good diodes in the reverse-biased region where the data are recorded that its influence on the circuit is negligible; R_{sh} can be reduced to 10^5 to 10^6 Ω without affecting the measured profiles.

The admittance, Y_{eq}, seen by the capacitance meter is:

$$Y_{eq} = \left[R_s + \left(j\omega C_s\right)^{-1}\right]^{-1} = \left[R_s - \frac{j}{\omega C_s}\right]^{-1} = \frac{R_s + \frac{j}{\omega C_s}}{R_s^2 + \left(\frac{1}{\omega C_s}\right)^2} . \qquad (8)$$

In the parallel representation (fig. 2) we obtain:

$$Y_{eq} = G_{eq} + j\omega C_{eq} = \frac{1}{R_s} \frac{\left[1 + \frac{j}{\omega C_s R_s}\right]}{\left[1 + \left(\frac{1}{\omega C_s R_s}\right)^2\right]} = \frac{1}{R_s} \frac{\left[1 + jQ_s\right]}{\left[1 + Q_s^2\right]} , \qquad (9)$$

giving

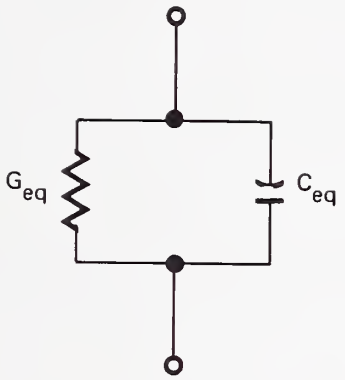


Figure 2. Parallel equivalent circuit.

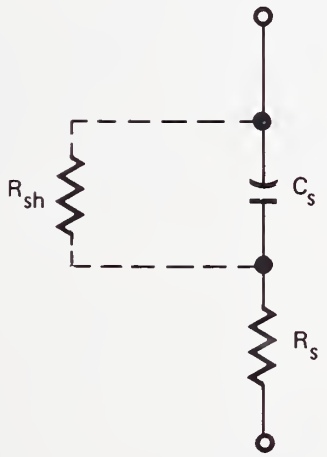


Figure 3. Series equivalent circuit seen by capacitance meter.

$$\omega C_{eq} = \frac{Q_s}{R_s\left[1 + Q_s^2\right]} . \tag{10}$$

Therefore, the capacitance used for differential C-V profiling [eqs (2a) and (2b)] is

$$C_{eq} = \frac{C_s}{\left[1 + Q_s^{-2}\right]} = \frac{C_s}{\left[1 + \left(\omega C_s R_s\right)^2\right]} . \tag{11}$$

For the 0.12-mm diameter diodes used in this study, R_s is estimated to be about 2 kΩ so that at a frequency of 1 MHz, $Q_s \approx 80/C_s$, where C_s is in units of picofarads.

Differentiation of eq (11) yields:

$$\frac{dC_{eq}}{dV} = \frac{dC_s}{dV} \frac{\left[1 - \left(\omega C_s R_s\right)^2\right]}{\left[1 + \left(\omega C_s R_s\right)^2\right]^2} . \tag{12}$$

Then by substituting eqs (12) and (11) into eq (6a), we obtain:

$$n(x)_{meas} = n(x)_{eq} = \frac{-C_s^3}{q\varepsilon A^2 \frac{dC_s}{dV}\left[1 - \left(\omega C_s R_s\right)^4\right]} = \frac{1}{1 - Q_s^{-4}} n(x)_{true} . \tag{13}$$

For $\left(\omega C_s R_s\right)^4 << 1$, we can expand the denominator to obtain:

$$n(x)_{meas} \doteq \left[1 + Q_s^{-4}\right] n(x)_{true} . \tag{14}$$

Thus, the dopant density measured by the profiler, $n(x)_{meas}$, is an accurate representation of the true density to within about 1 percent if the Q_s of the circuit is as low as 3.

Now let us treat the x measured by the profiler in a like manner. Substituting eq (11) into eq (6b) gives:

$$x_{meas} \doteq \frac{\varepsilon A}{C_s}\left[1 + \left(\omega C_s R_s\right)^2\right] = \left[1 + Q_s^{-2}\right] x_{true} . \tag{15}$$

In this case, Q_s must be ⩾10 for the error to be 1 percent or less. This is a more stringent requirement than the one derived for n(x).

2.3.1 Frequency

The Q_s criterion is more easily met by using a low measurement frequency. However, a high frequency is required to guarantee that deep levels do not influence the capacitance measurements and thereby distort the C-V profiles from the desired shallow carrier distribution as discussed in section 2.1

(see also [20] and [21]). A value of f = 1 MHz is sufficient to overcome this limitation and is typically used in differential C-V profilers, as it is in the experiments and analyses described in this report. Any higher value of frequency hurts the tradeoff criterion for Q_S.

2.3.2 Influence of Diode Size

If the diode diameter D is increased, C_S increases as D^2 and R_S decreases approximately as D^{-1}, so:

$$Q_S \propto D^{-1} . \tag{16}$$

Therefore, if D is doubled or quadrupled, Q_S is halved or quartered and the validity of n(x) and x measured by the profiler deteriorates. Increasing the diode area also increases the probability of overlaying a defect in the substrate which can result in an unusable diode. This can be detected from current-voltage measurements before profiles are measured. As the size of the dots is reduced, the edge or perimeter effects increase [34].

2.3.3 Influence of Substrate Resistivity

Because R_S is approximately proportional to the resistivity ρ_S of the diode substrate, Q_S can be advantageously increased by decreasing ρ_S. Such an increase in Q_S allows larger diode sizes to be used or higher capacitance samples to be studied, such as those with higher implantation fluence or shallower dopant profile, both leading to higher dopant density. However, a low value of R_S implies a high value of background substrate dopant level. The C-V profiling technique is limited in its ability to measure high carrier densities by avalanche breakdown near the surface of heavily doped surface regions as the diode bias is increased. The maximum value of n(x) that can be measured by C-V profiling is about 10^{18} cm^{-3} for shallow doped regions (100 to 200 nm) and approaches 10^{17} cm^{-3} for deep profiles (1 to 10 μm).

A low value of R_S leaves little room for measurement between the background carrier density and maximum measured n(x). Thus, a high value of R_S is desired to give maximum data in n(x), but then the detrimental effect on Q_S is encountered. The resulting practical range of background substrate dopant level is roughly 10^{14} to 10^{15} cm^{-3} or about 10 to 100 Ω•cm for the resistivity of the silicon substrate, varying slightly, depending on whether the carriers are electrons or holes. Substrates of 10 and 100 Ω•cm resistivity were used in this work. For ~100 Ω•cm substrates the value of R_S calculated using spreading resistance is about 2000 Ω. For example, the use of 10 Ω•cm substrates has allowed somewhat lower energy implants to be profiled (5 and 10 keV). Another help in obtaining profiles of lower energy implants is to use higher fluences in order to increase the dopant density beyond the depth that corresponds to the zero bias depletion depth.

If differential C-V profiling data are required in semi-insulating substrates (e.g., high resistivity GaAs) or in substrates on insulators (e.g., SOS) where R_S is very high, it is necessary to fabricate a lateral geometry configuration where contact is made to the side of the Schottky barrier

diodes. In such cases the value of R_S is not uniform because of pinch-off effects at high reverse biasing conditions [35].

2.3.4 Error Analysis

Let us examine the limitations of validity imposed by the requirements that:

$$Q_S \geq 3 \text{ for } n(x) \tag{17a}$$

and

$$Q_S \geq 10 \text{ for } x \, . \tag{17b}$$

For the 0.12-mm diodes on the implanted surfaces of our samples, the zero-bias capacitance, C_0, varies from 2 to 20 pF. C_0 is the maximum value of C_S; C_S decreases to small values for large reverse bias. Thus, Q_S varies from large values to 4, which fulfills the criterion (18a) for n(x). If C_0 is 30 pF, $Q_S \geq 3$ and the maximum error in n(x) is expected to be 1 percent. If C_0 becomes 50 pF as it can for larger dots, $Q_S \geq 1.67$. Data may be recorded with an error of <1 percent for values of reverse bias that keep C_S below 30 pF. As the applied voltage decreases (that is, as the measured profile approaches the surface) and C_S exceeds the limiting value of C, the value of n(x) becomes incorrectly large rapidly, as is illustrated in figure 4.

The situation for increasing D is more serious for x than for n(x). Examining eqs (16) and (15), we see that if D is doubled or quadrupled (from 0.12 to 0.25 or 0.50 mm), then a C_0 of 10 pF becomes 40 or 160 pF, and an R_S of 2000 Ω becomes 1000 or 500 Ω, and x_{meas} = 104 percent or 116 percent of x_{true}. We have measured displacements of these magnitudes for diodes 0.50 mm in diameter, compared directly with 0.13-mm diodes, as illustrated in figure 5.

For a 0.12-mm diameter diode with R_S = 2000 Ω, the upper limit on C_S for ≤1-percent error in x is 8 pF. A C_S of 16 pF results in an x that is 4 percent too large. A C_S of 20 pF leads to a 6-percent error. Thus we see that either only diodes with C less than 8 pF should be used or the error in the measured x of the C-V profiles should be quoted, or the values of x should be corrected for it.

Voltage breakdown is another characteristic of a diode that can affect a C-V profile. For a depth distribution that requires a large applied voltage to deplete it completely, the applied voltage may exceed the breakdown voltage of the diode. This voltage may be 50 to 100 V. Such a situation is illustrated in figure 6. In this figure, the value of n(x) is seen to increase rapidly at diode breakdown. It is also possible for the value of n(x) to decrease at the breakdown condition.

2.3.5 Phase Error

Any nonnegligible phasing error that may exist in the capacitance measuring circuit should be taken into account in the total error analysis. The phase error can be determined for the measuring system by artificially introducing a resistance along with a standard calibration capacitor. The profiler used in this work could be adjusted to minimize any phase angle error.

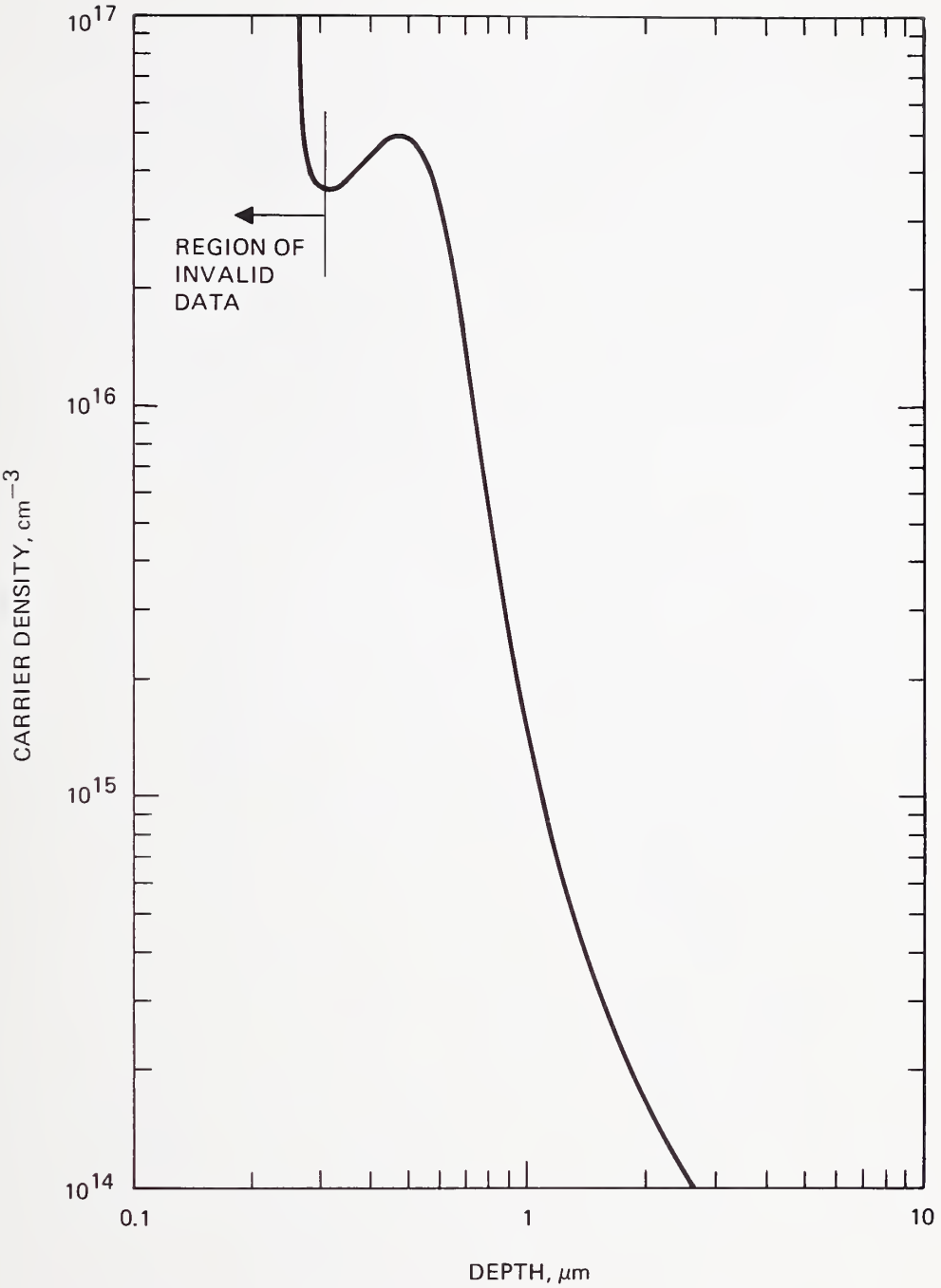


Figure 4. A C-V profile that shows the nature of an error caused by a high sample capacitance.

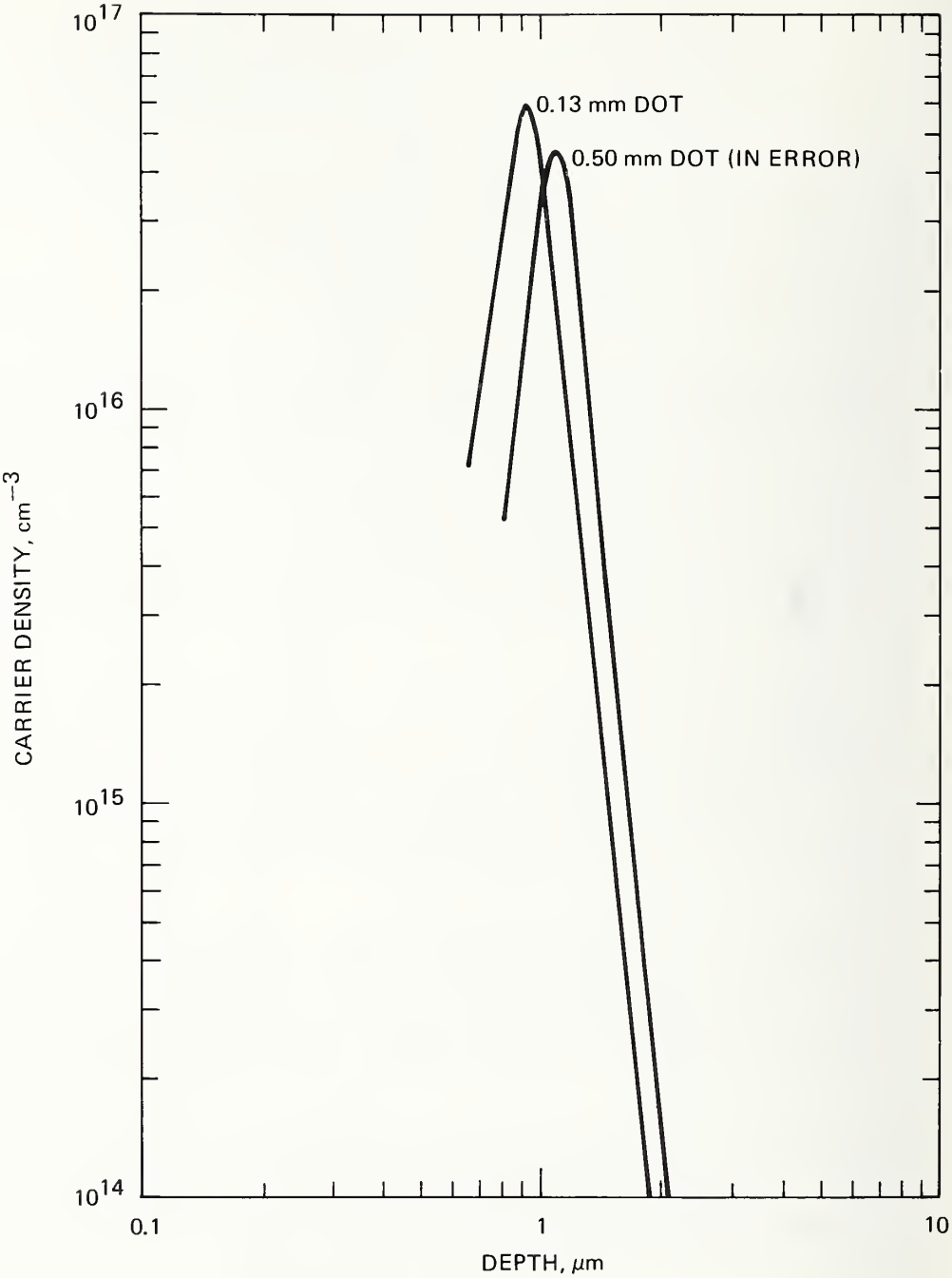


Figure 5. Two C-V profiles that show the nature of an error caused by using a sample area that is too large.

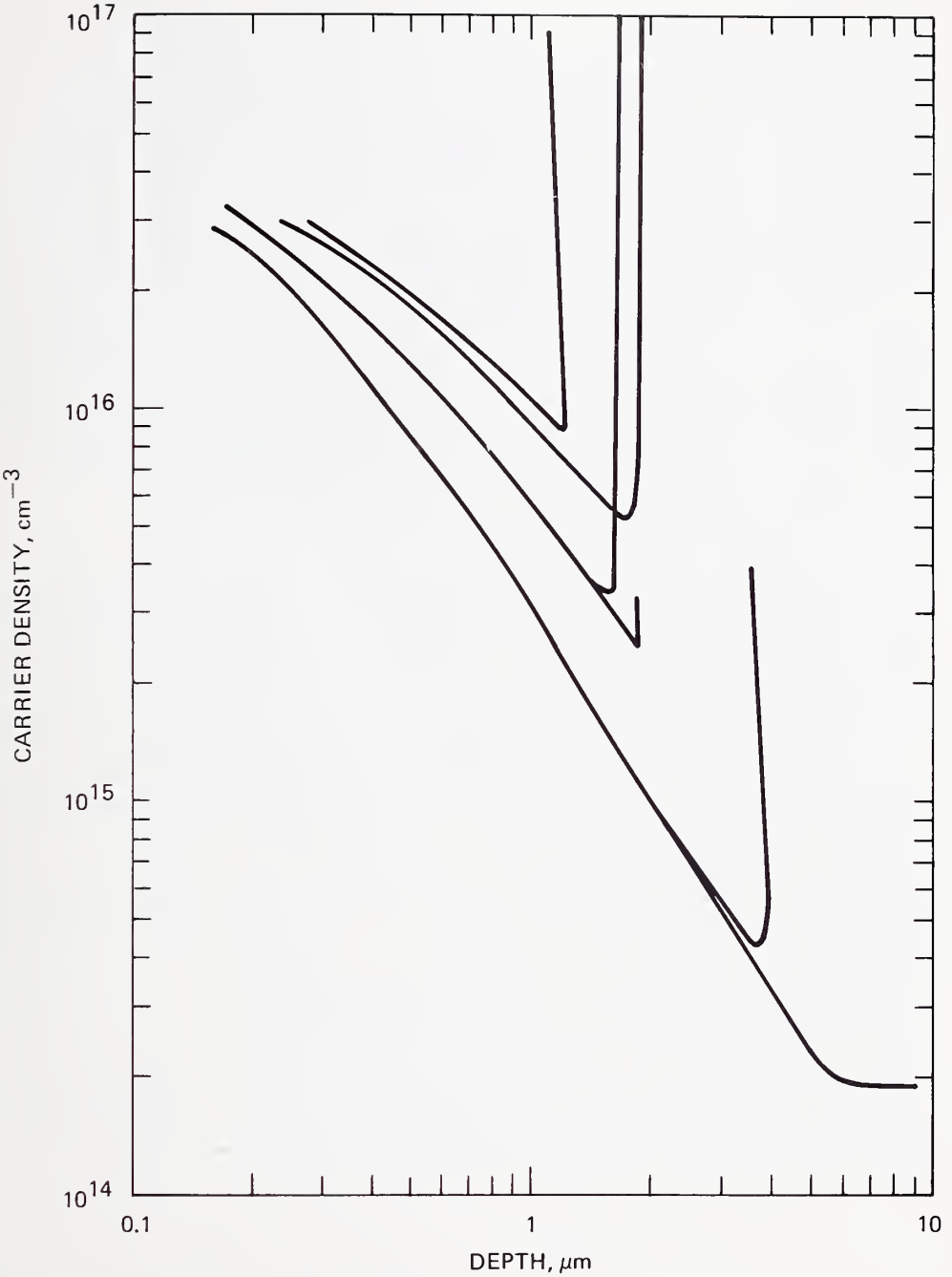


Figure 6. Several C-V profiles that show the nature of the loss of data caused by voltage breakdown.

2.3.6 Voltage Sweep Rate

In measuring dopant densities by automatic C-V profiling techniques, the reverse bias may be automatically swept for the calculation of density *versus* depth. The influence of the rate at which the voltage is swept was determined. A profile for 300-keV boron in silicon was repeatedly measured as the voltage sweep rate was varied on an automatic C-V profiler. The results are shown in figure 7, where five bias voltage sweep rates are plotted on the same figure with the corresponding C-V profiles. The voltage was always started at 20 V and decreased to 0 V. The two sweep rates above the slowest (2 and 3) show small distortions in the "tail" region of the distribution. The high rates (4 and 5) show large distortions of the profile indicating erroneously large depths. The highest rate (5) also distorts the curve at the peak of the profile (making the density too low) and on the shallow side of the peak of the implanted distribution (too shallow).

2.3.7 Ambient Light Intensity

The intensity of light in the environment of the Schottky barriers during the C-V measurements has been observed to influence the shape of the profiles. Light-stimulated carrier generation around the periphery of the Schottky barriers may be the cause. The effect is documented below. C-V profiles were measured for various Schottky barriers on (111) silicon surfaces implanted with 300-keV boron while various levels of light were incident on the barriers. The Schottky barriers were aluminum, titanium-gold, and molybdenum-gold. Light intensities used were: a) room darkened; b) overhead room lights on (normal lighting); and c) a microscope lamp directly illuminating the barriers, such as occurs while contacting the Schottky barriers with the gold probe.

The results are shown in figure 8 for each of the three light intensities on each of the three Schottky structures. Observations from these results are:

- The presence of normal room light does not affect the C-V profiles for any of the Schottky structures examined.
- The presence of more concentrated light from a microscope lamp distorts the C-V profiles significantly for all three Schottky structures, but in different ways.
- For the aluminum Schottky, the effect of light is to depress the peak artificially and to widen the profile at high densities.
- For both the titanium-gold and molybdenum-gold Schottkys, the effect of light is to increase the height and narrow the width of the peak of the distribution (but more significantly for molybdenum-gold than for titanium-gold), and to move the entire distribution to shallower depth.
- For all three Schottkys, the background dopant density is artificially raised. The trend becomes more pronounced from aluminum to titanium-gold to molybdenum-gold.

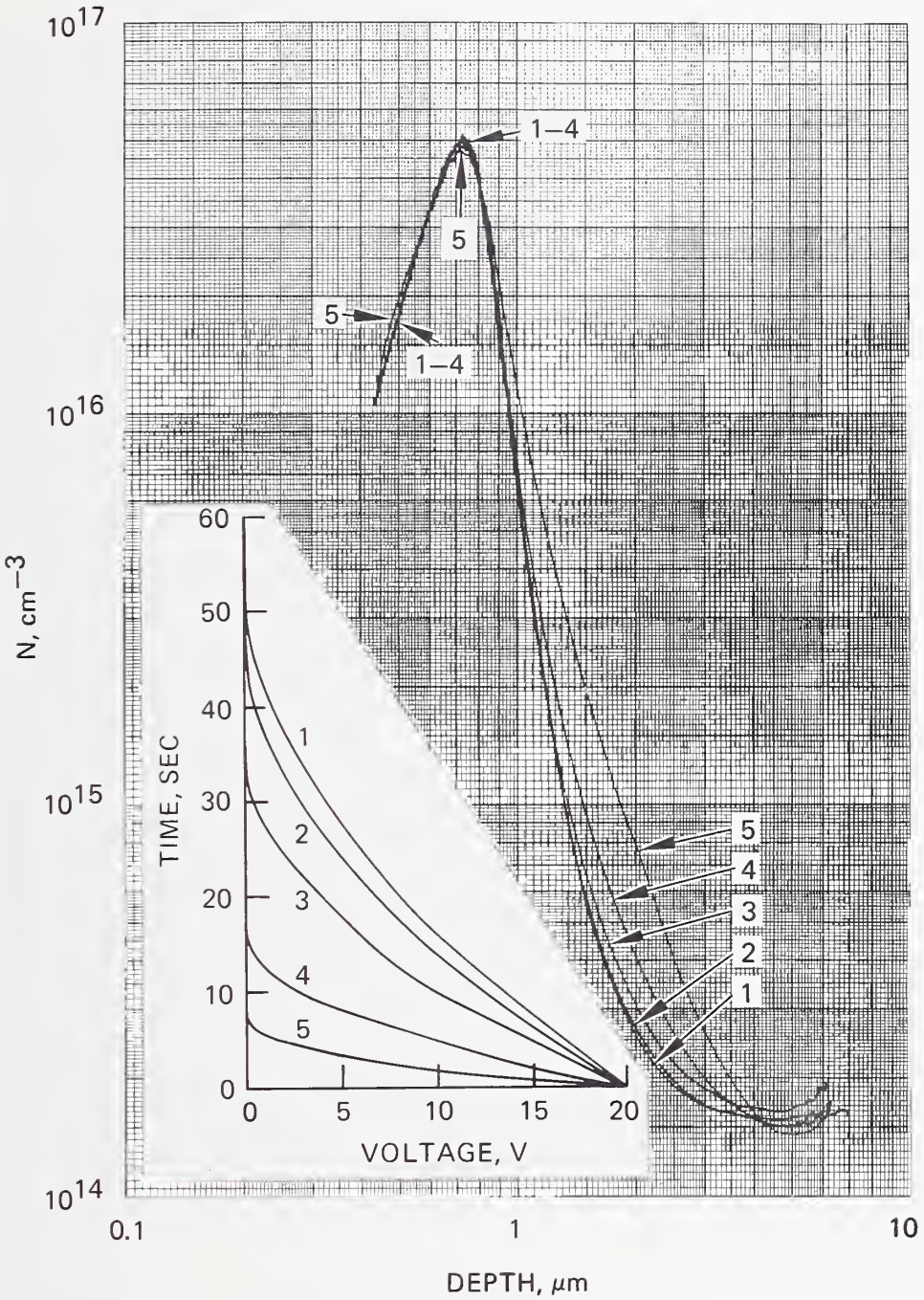


Figure 7. C-V profiles for a silicon specimen implanted with 300-keV boron for various voltage sweep rates shown in the inset.

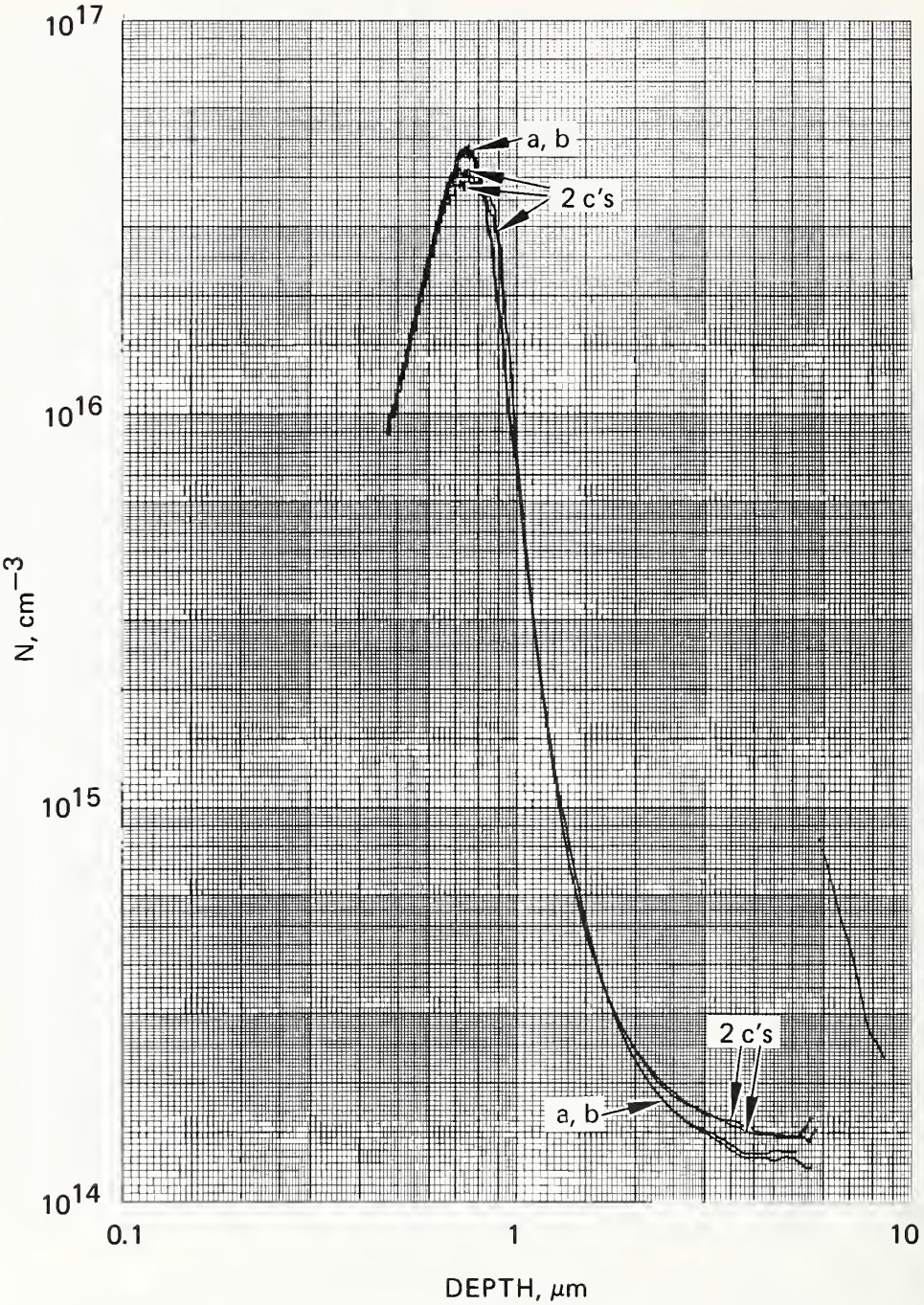


Figure 8a. C-V profiles for varying light intensity environments; aluminum Schottky barrier (300-keV boron in silicon). a) darkened room; b) normal lighting; c) microscope lamp.

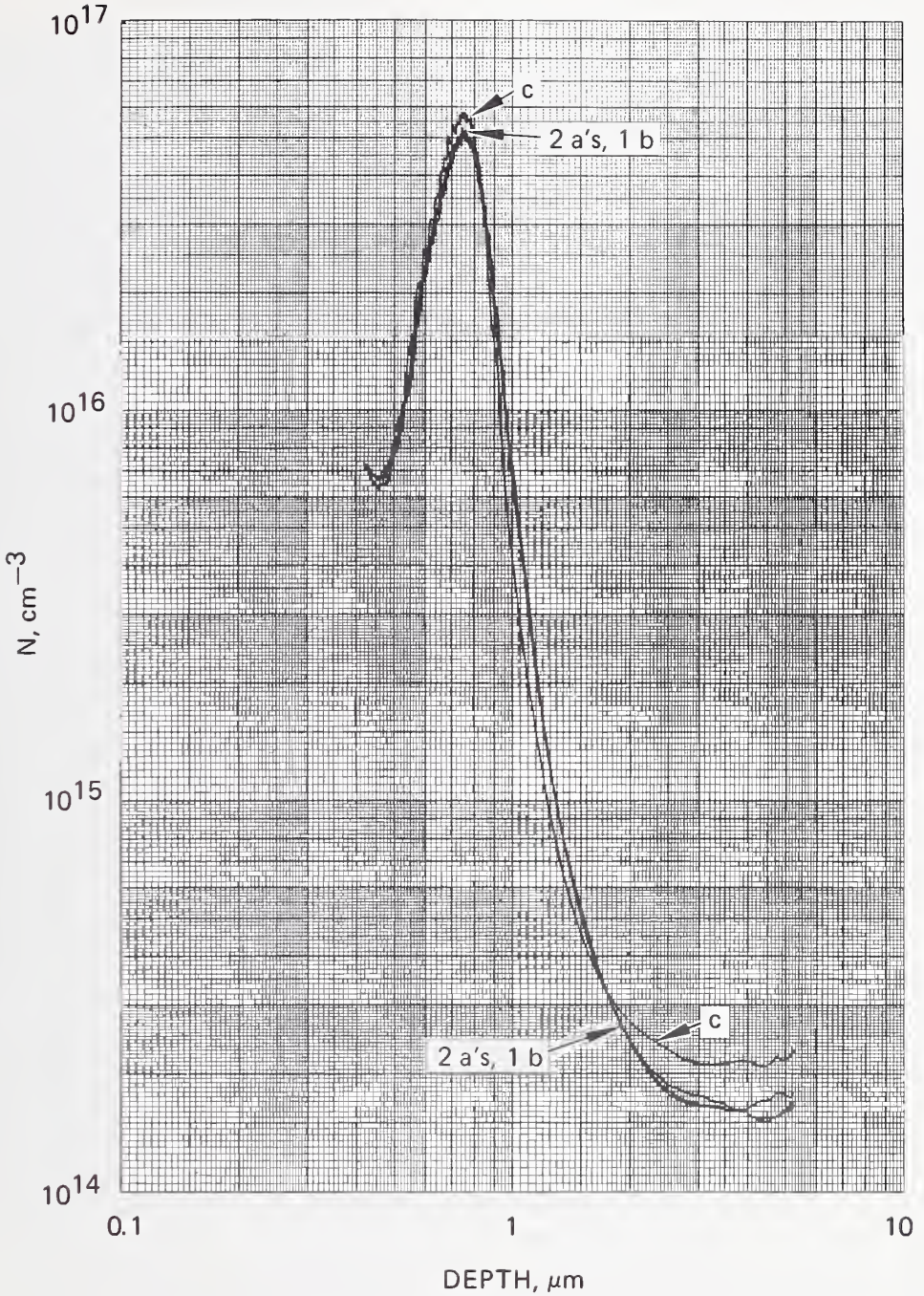


Figure 8b. C-V profiles for varying light intensity environments; titanium-gold Schottky barrier (300-keV boron in silicon). a) darkened room; b) normal lighting; c) microscope lamp.

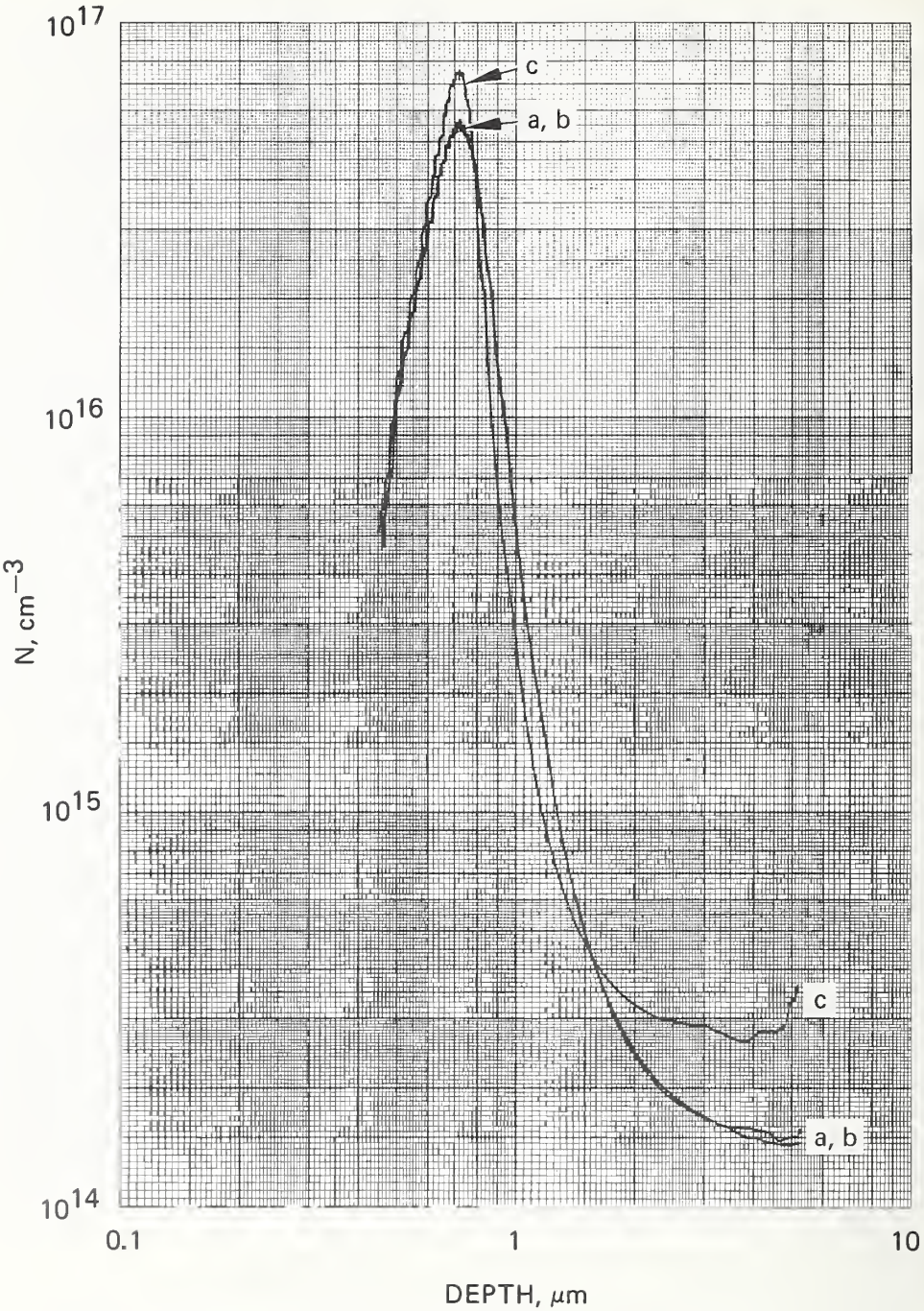


Figure 8c. C-V profiles for varying light intensity environments; molybdenum-gold Schottky barrier (300-keV boron in silicon). a) darkened room; b) normal lighting; c) microscope lamp.

2.3.8 Cable Compensation and Zero Calibration

Two practical details of C-V measurements using a capacitance meter involve proper compensation for the probe cable and zeroing of the capacitance meter. Detailed studies of the effect of these two adjustments and how they were performed showed that significantly incorrect profiles can result if these two procedures are not carried out in the manner described below which yields consistent and accurate profiles.

With the probe cable attached for a C-V measurement, but not contacting a sample (withdrawn one probe diameter from contact), the cable compensation is adjusted to maximize the capacitance reading on the most sensitive scale and then the capacitance meter is zeroed on the scale on which the measurements will be made (determined by the sample capacitance under zero applied voltage). The capacitance meter should be zeroed each time a different capacitance scale is used. The measured capacitance associated with a probe-to-sample spacing of one probe diameter is ~0.01 pF, indicating no likely error from this source if cable compensation is carried out.

2.3.9 Experimental Errors

The following error analysis is based on the fundamental expressions of eq (6). The error limit on the diameter of the Schottky barriers measured optically with a calibrated eyepiece reticle is about 1 percent, so the error limit on the area (A) is about 2 percent. The error in the measurement of capacitance (C) is about 2 percent so the error in C^3 is 6 percent. The error in dC/dV is about 3 percent. Combining these, the rms error in n(x) is ~7 percent; and the rms error in x is ~3 percent. These error limits are valid only if the measurement frequency, diode resistance, and diode capacitance are such as to make the diode Q be greater than 5, as shown above.

During C-V profiling for cases where the zero-bias capacitance is large enough to cause some error, but no error occurs at higher biases, the deep portion of the depth distribution (higher reverse bias) is accurate; but closer to the surface where the value of C surpasses the value of negligible error, n(x) becomes erroneously high, the error becoming larger as the surface is approached. For cases of deep profiles where large reverse bias is required to deplete through the charge distribution, diode leakage currents and finally breakdown may occur, causing errors in the profiles. Current-voltage measurements of the diodes prior to profiling can be used to determine if such effects will occur for the required reverse biases. We have found that carefully prepared Schottky barrier diodes on p- and n-type silicon surfaces implanted with ~10^{12} cm^{-2} ion fluences will support reverse bias in excess of 100 V and that such values of bias are required to deplete through deep channeled profiles (~5 to 10 μm).

2.4 Summary

In summary, this analysis shows that it is essential to use diodes with a C_0 less than the limits established in the above analysis or to record data only for capacitances below these limits if the as-measured depth distributions of electrical activity are to be valid within 1 percent.

Otherwise, the profiles should be corrected according to this treatment, or appropriate errors should be quoted.

The zero-bias capacitance C_0 of a diode can be controlled via dot size and dopant density. Higher dopant densities can be studied by decreasing the dot size. Profiles can be obtained closer to the surface by decreasing the dot size or the substrate resistivity, with a corresponding loss of profile at lower densities in the latter case.

Profile measurements should be made only for diodes that exhibit good I-V characteristics in both forward and reverse bias. The diodes should not break down or leak significantly for voltages up to those required to deplete through the implanted region, that is, until the complete profile is obtained, or data should be reported only for voltages up to the breakdown or leakage values.

Our experience has shown that by using the criteria defined above, reproducible and consistent implanted profiles can be obtained for diodes that exhibit 0.5- to 30-pF capacitance and depth distributions from 80 nm to 10 μm. For distributions deeper than ~3 μm, applied reverse bias up to 100 V may be required to obtain a complete profile from one sample. Dopant densities can be measured from 10^{14} cm^{-3} up to about 3×10^{17} cm^{-3} at depths below 0.3 μm, and up to about 8×10^{16} cm^{-3} at about 1 μm, with a gradation between. The maximum implantation fluence that can be profiled is about 2×10^{12} cm^{-2} for distributions that extend ≥1 μm in depth, and about 2×10^{13} cm^{-2} for depths of about 0.1 to 0.2 μm, with a gradation between.

It is important to determine for a given C-V profiler what maximum voltage sweep rate does not distort the depth distribution and then to keep the sweep rate below this value. The maximum sweep rate for the C-V profiler used in this work is ~0.5 V/s. Care must also be taken to ensure that profile distortions are not caused by intense light shining on the diode that is under reverse bias. Normal room light was found in this work to cause no distortions, but localized intense light did cause a significant change.

3. SCHOTTKY BARRIERS

3.1 Introduction

The physics and practical aspects of the use of Schottky barriers on semiconductor surfaces is a well-established and studied field [36-56,20, 24]. Their use for measuring the properties of ion-implanted layers has been studied specifically [48-50,52,20]. Our need in this study was for stable, reproducible Schottky diodes with hard current-voltage (I-V) characteristics and high breakdown voltage (V_B). The literature indicated that gold and aluminum were possibilities and that certain difficulties might be encountered, such as aging (time-dependent effects). Therefore, we studied several metallization systems on both *p*-type and *n*-type implanted silicon to verify what systems were valid for this project. The metals chosen were gold on *n*-type and aluminum on *p*-type silicon.

3.2 Metals for Schottky-Barrier Formation on p-Type and n-Type Silicon

We have studied and compared the four metallizations: aluminum, gold, titanium-gold, and molybdenum-gold, on p-type (boron-implanted) and on n-type (phosphorus- or arsenic-implanted) (111) silicon surfaces. We studied cleaned (unetched) surfaces and surfaces etched in concentrated hydrofluoric acid (HF) just prior to Schottky barrier deposition. We followed the aging of these Schottky barrier metallizations until stabilization was reached. The I-V characteristics of the barriers and the dopant profiles obtained by C-V measurements of the underlying implanted surface were recorded. The results are reported below.

A set of eight 100 Ω•cm, p-type samples was implanted with 300-keV boron, four with HF-etched surfaces and four with unetched surfaces, and their C-V profiles were followed for about 18 months. The four metal systems were evaporated in an electron-beam evaporator at approximately 10^{-7} Torr. The Schottky barriers were dots 0.13, 0.25, 0.50, and 1.0 mm in diameter, defined by a contacting mask, in the metal film which was 100.5 (±2.0) nm thick.

Four of the surfaces were cleaned by ultrasonic degreasing followed by acetone, alcohol, and deionized water rinses. Four other surfaces were dipped in a standard HF etch for 15 s and rinsed. The metallizations were evaporated sequentially on these latter four samples. All Schottky barriers for all four metal systems on the etched surfaces were shorted initially and remained shorted. No C-V profiles were ever obtained for any of them. Some indication of an increase in shorted resistance was observed with time. These results are consistent with the work of Turner and Rhoderick [45].

Good Schottky I-V characteristics and fair C-V profiles were obtained immediately for the four metal systems placed on cleaned, but unetched, silicon surfaces (assumed to have ≤3 nm of native oxide present at the time of deposition). For the p-type surfaces, the C-V profiles changed slightly during the first two or three hours and then stabilized. Schematic representations of the C-V profiles showing the characteristics of the initial and stabilized C-V profiles for the four metallization systems are shown in figure 9. In all cases, the measured background dopant level decreased with time until it reached the substrate dopant level. Aluminum was the most stable metallization, changing only slightly in background level; it is felt to be the best choice for routine work on p-type silicon. Gold gave information closer to the surface, but aged significantly, and the measured carrier densities are higher than predicted analytically. Titanium-gold gave the least information and changed the most with time. Molybdenum-gold aged some and was the most difficult to deposit. Aluminum is the easiest metal system to use, ages the least, and has given the most reliable data. We have checked some aluminum Schottky barriers after 30 months, and the C-V profiles have not changed during that time.

The same four metallization systems were studied for n-type (phosphorus) implanted silicon. The I-V, C-V, and capacitance data for the four Schottky barrier systems are shown in figure 10. Gold was good and was therefore always used in this program. Titanium-gold was universally bad. Aluminum and molybdenum-gold were sometimes fair or even good, but often bad. The specific features of the bad I-V and C-V curves are shown in the figure. It

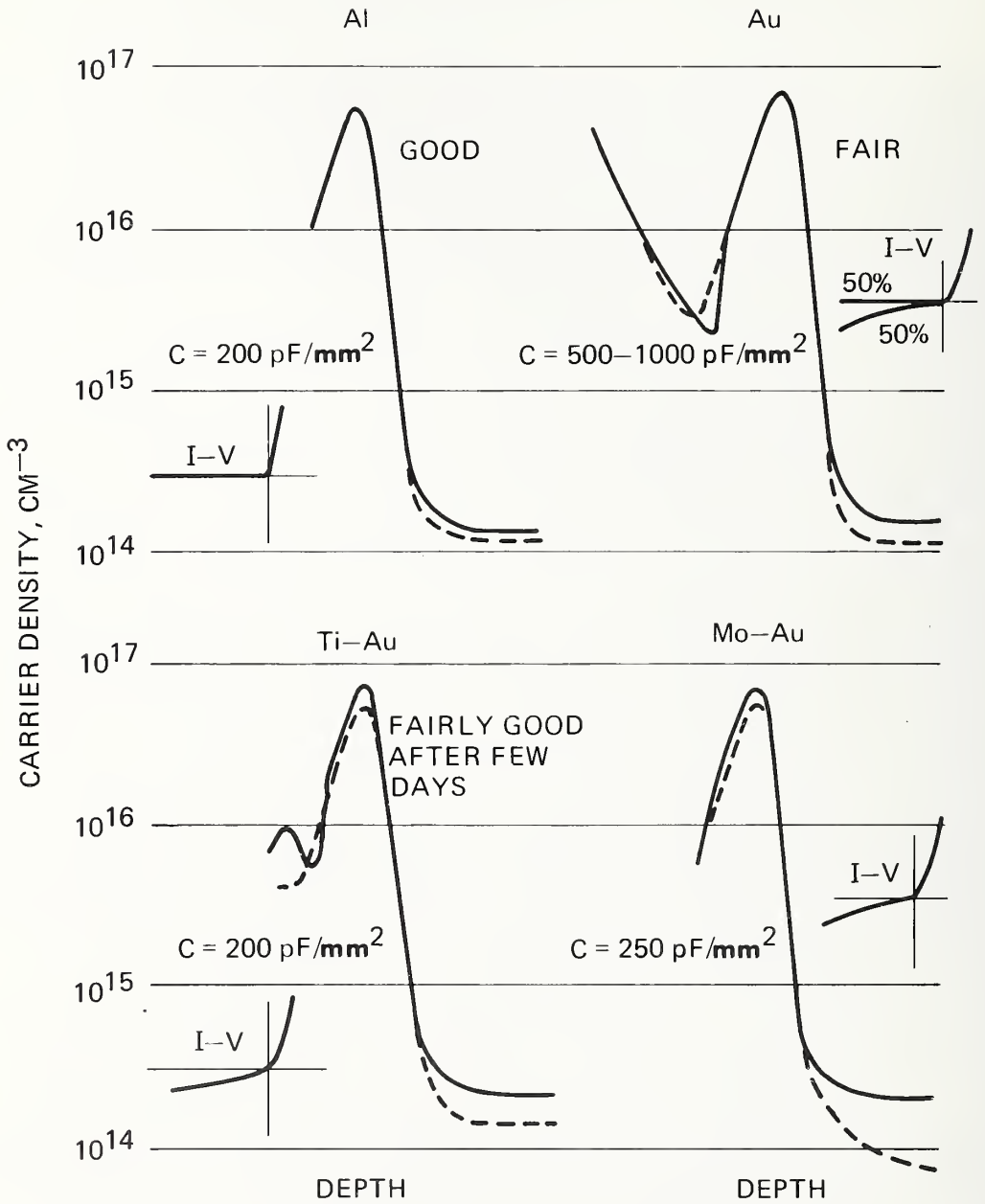


Figure 9. C-V profiles and Schottky barrier data for four metallization systems on p-type, ~100 Ω•cm implanted silicon surfaces (300-keV boron). (Solid curves: immediately after metal deposition; dashed curves: after stabilization. Both scales are logarithmic. Vertical scale is density ranging from 10^{14} to 10^{17} cm^{-3}; horizontal scale is depth ranging from 0.1 to 10 μm.)

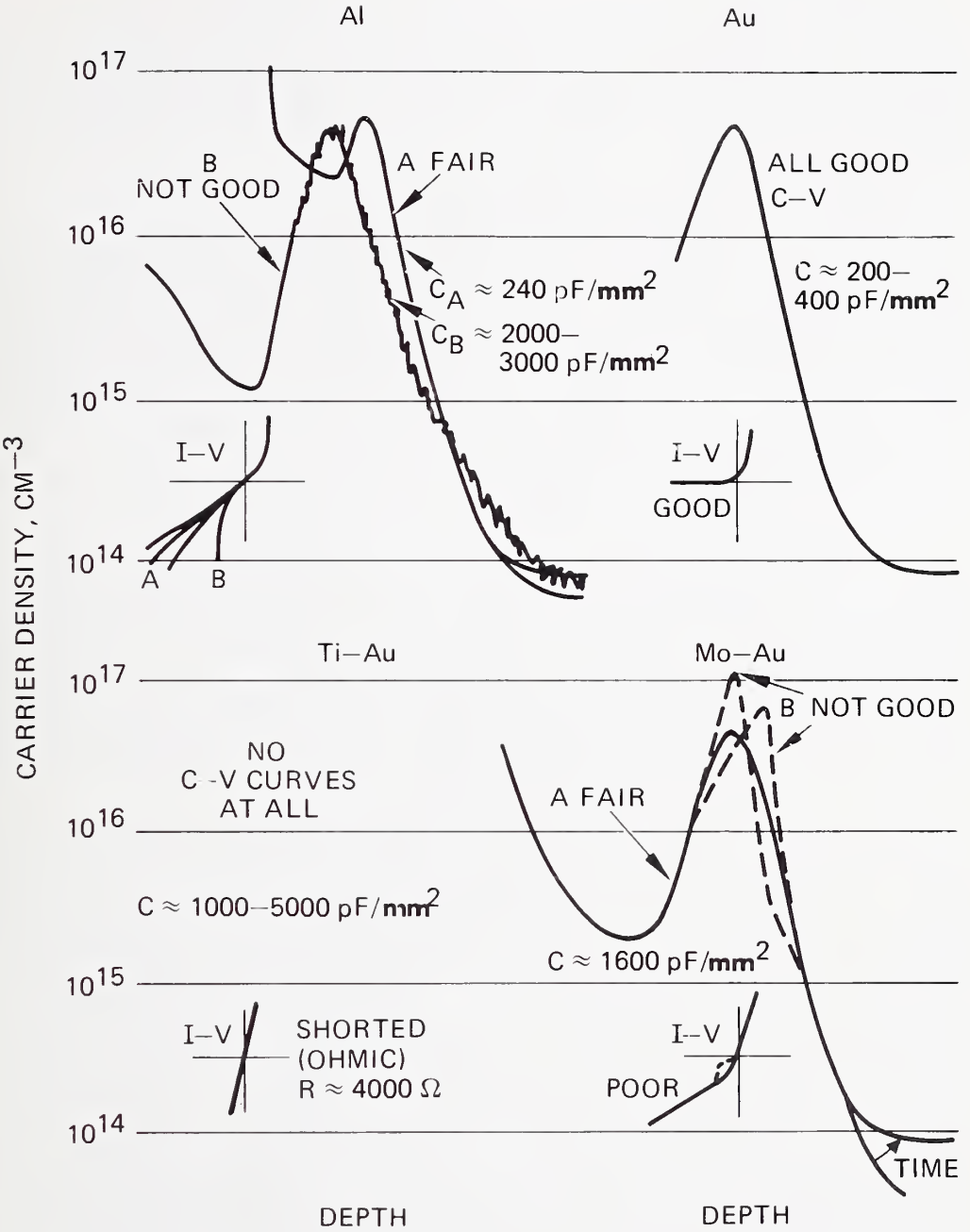


Figure 10. C-V profiles and Schottky barrier data for four metallization systems on n-type, ~100 Ω•cm implanted silicon surfaces (600-keV phosphorus). (Solid curves: immediately after metal deposition; dashed curves: after stabilization. Both scales are logarithmic. Vertical scale is density ranging from 10^{14} to 10^{17} cm^{-3}; horizontal scale is depth ranging from 0.1 to 10 μm.)

was learned that the I-V curve quality and the value of C can almost always be used to determine whether a C-V curve is going to be good or bad. The value of C should be 200 to 400 pF/mm^2 for the ~0.7-μm deep profile shown and the I-V curve should be rectifying. The metal film thickness should be between 50 and 250 nm.

3.3 Schottky Barrier Height Measurement and Aging

Three experimental techniques for measuring Schottky barrier heights have been the I-V, C^{-2}-V, and photoemission threshold techniques reviewed by van Otterloo and Gerritsen [56]. They conclude that, of these, the C^{-2}-V method is capable of producing the most accurate results. In the C^{-2}-V technique, the reciprocal of the square of the differential capacitance is plotted *versus* the applied reverse bias (and slightly into forward bias). The Schottky barrier height ϕ_B is determined from the intercept of a straight line drawn through these data as follows:

$$\phi_B = \text{Intercept} + \frac{kT}{q} + \phi_F + \text{I.F.} , \qquad (18)$$

where ϕ_F is the Fermi energy relative to E_C (the bottom of the conduction band) and I.F. is the image force effect. The terms I.F. and kT/q are generally considered negligible (~0.02 eV). Examples of C^{-2}-V plots for aluminum Schottky barriers on 100 Ω•cm *p*-type (100), (110), and (111) silicon (float-zone-refined) and for gold Schottky barriers on 100 Ω•cm *n*-type (100) and (111) silicon are shown in figures 11 and 12. The intercepts from which values of ϕ_B are obtained from eq (18) are indicated. Values of ϕ_B from ~0.65 to 0.85 V are inferred.

As stated by Turner and Rhoderick [45], there is a wealth of evidence in the literature that a silicon surface is inevitably covered with a thin oxide layer of the order of 1 nm thick. Muret and Deneuville [55] report that chemically prepared silicon surfaces are covered with 0.5 nm of oxide as measured by ellipsometry. These 0.5 and 1 nm numbers are consistent with our Rutherford backscattering measurements that indicate that our implanted silicon surfaces are covered with oxygen corresponding to about two monolayers of silicon dioxide. These layers are so thin that electrons can easily tunnel through them, but the effective barrier height can also be affected. Positive ions moving under the influence of the high built-in field to be neutralized at the metal surface migrate less easily through the oxide layer. During this migration, a temporary dipole would modify the barrier height in a time-dependent way. This is the probable mechanism for aging of Schottky barriers that is discussed in the literature. Aging of Schottky barriers is discussed for silicon by Turner and Rhoderick [45] and Muret and Deneuville [55], and by Nicollian *et al.* [51] for gallium arsenide.

3.4 Schottky Barrier Area and Quality Measurement Techniques

Two key factors in the measurement of C-V profiles using Schottky barriers are the determination of the area and the quality of the Schottky barrier metallization. Area determination is possibly the largest source of error in the measurement of dopant profiles by the C-V technique. Schottky

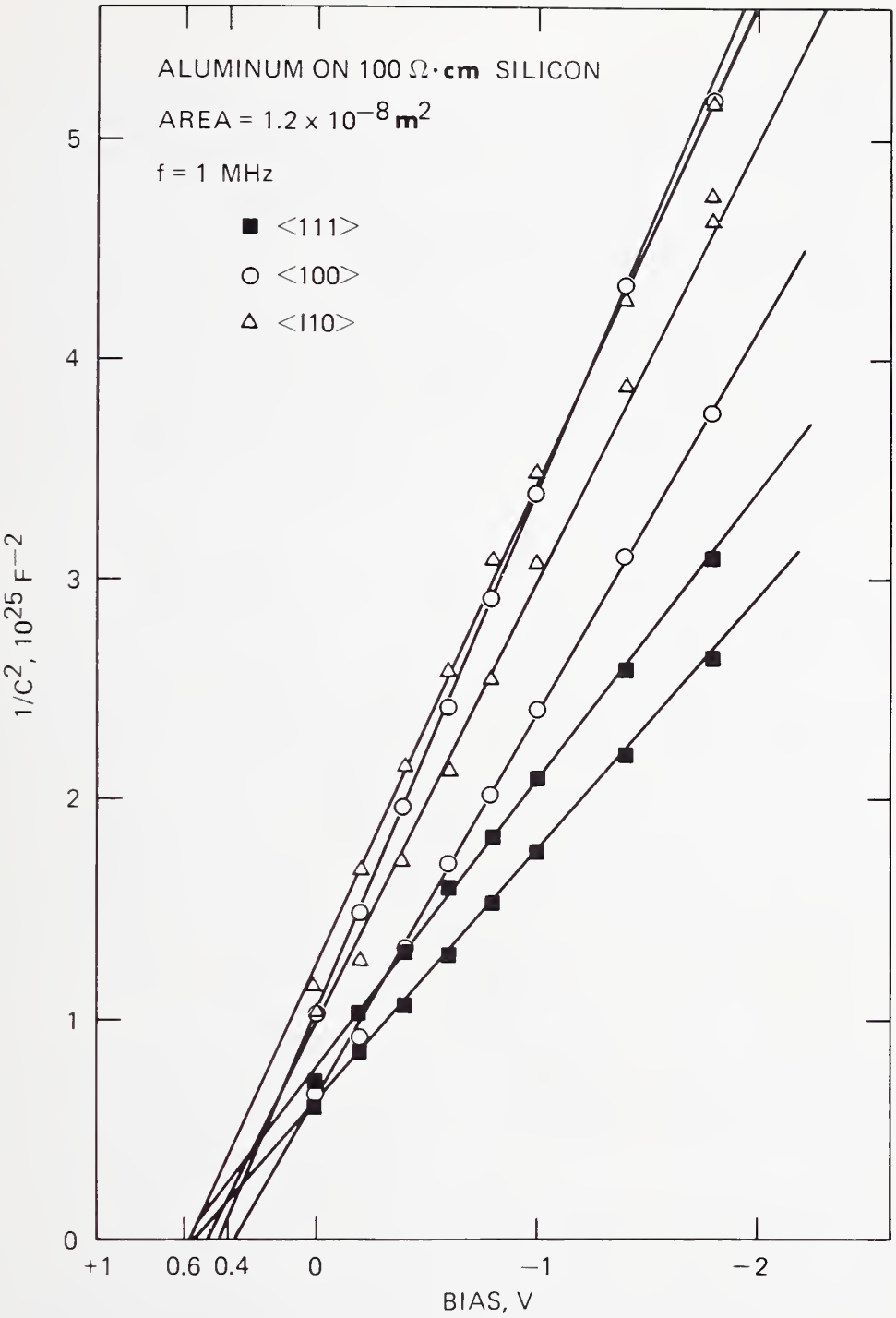


Figure 11. Plots of C^{-2}-V Schottky barrier height determination; aluminum on *p*-type silicon.

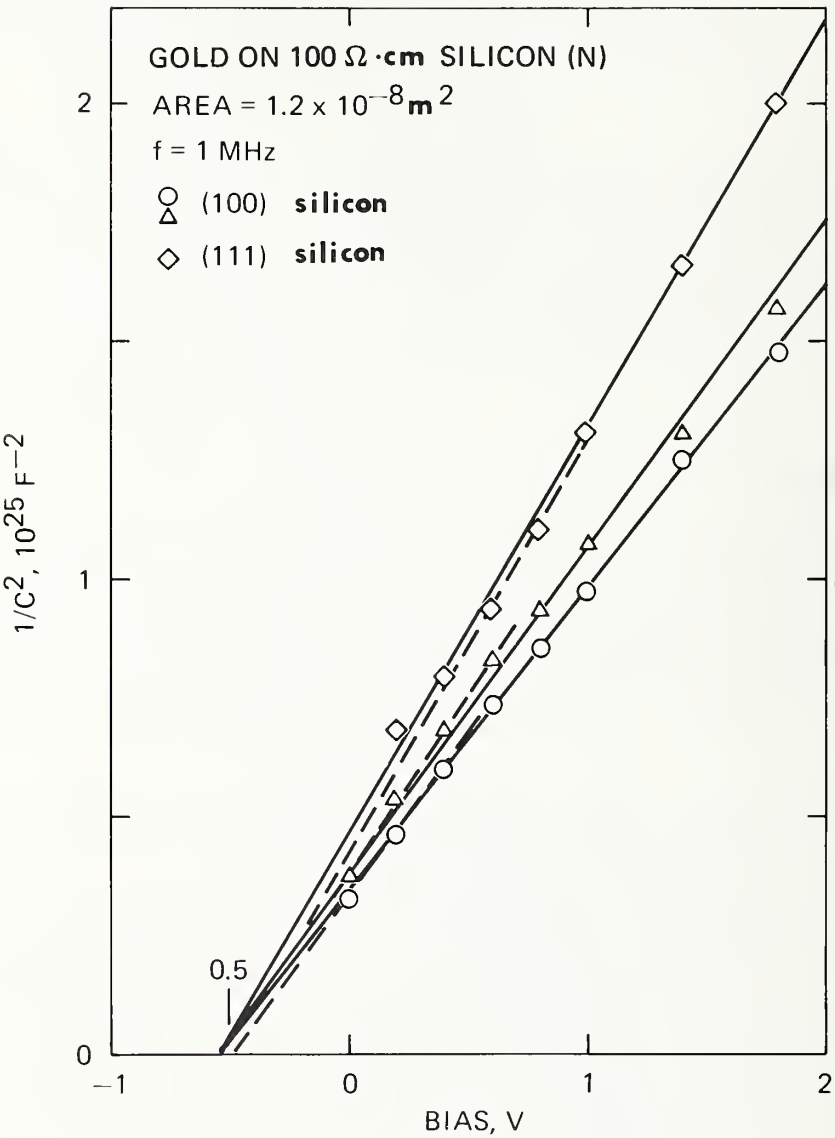


Figure 12. Plots of C^{-2}-V Schottky barrier height determination; gold on *n*-type silicon.

barriers were fabricated for this work with diameters of 0.13, 0.25, 0.50 and 1.0 mm. The I-V characteristics of the 0.13-mm dots were consistently good. Acceptable I-V characteristics and C-V profiles were obtained for some of the 0.25-mm dots.

The areas of the Schottky barrier metallizations used were calculated from the average of two orthogonal measurements of the diameter. The diameter measurements were accurate to about 1 percent. Dots with irregular edges were not used for C-V measurements, nor were significantly nonround dots or dots with damage or imbedded dirt used. Optically unobservable errors and flaws can result from spots of poor adhesion or defects in the silicon beneath the surface. We feel that such unobservable errors can be eliminated by measuring C-V curves for six or eight Schottky barriers and discarding any curves that deviate significantly from the majority that agree closely. Usually one out of six 0.13-mm dots was in disagreement, while five agreed, indicating a yield of about 83 percent.

The current-voltage characteristics of the Schottky barriers were measured on a curve tracer set at 10 μA and 2 V. Some typical examples for 0.13- and 0.25-mm dots on n- and p-type silicon are shown in figure 13. A description of the samples is shown in table 1. The I-V characteristics of Schottky barriers that gave good C-V profiles are shown in a, b, and c. I-V characteristics of leaky barriers which nevertheless provided useful C-V profiles are shown in a' and b'. Schottkys with I-V characteristics like those shown in a", b", d, and d' produced unreliable or no C-V profiles.

3.5 Attempts to Improve C-V Profiles of Schottky Barriers

Four experiments were carried out to determine the merits of several silicon surface treatments to improve the C-V characteristics of Schottky barriers. One of these, which had negative results, was carried out as part of the on-going aging study described in the previous sections. Etching the surface in HF to remove the native surface oxide prior to depositing the Schottky metal was found not to provide improved characteristics.

In another experiment a shallow p^+ or n^+ layer was formed at the surface before deposition of the Schottky barrier by implanting low energy boron or phosphorus. A 10-keV, 5×10^{11} cm^{-2} boron implant made on the surface of a standard 300-keV, 1.5×10^{12} cm^{-2} boron implant annealed at 750°C had no effect on the C-V measured dopant profile.

Another experiment involved annealing a 300-keV boron-implanted sample in air at 900°C instead of in the standard dry argon or nitrogen annealing environment. This procedure affected the C-V profile. The value of R_p was slightly larger than the norm, but no more so than some of the Schottky barriers that deviated from the norm of normally annealed samples. The value of N_{max} was normal and the profile on the deep side of the peak was normal. The capacitance at the peak itself was unstable. The shallow side of the peak of the profile to the surface was destroyed. The curve dropped only slightly from the peak of the distribution, then shot vertically upward between 0.4 and 0.2 μm, and finally moved deeper as the applied voltage decreased to zero. The surface region to a depth of about 0.5 μm did not yield valid C-V profile information.

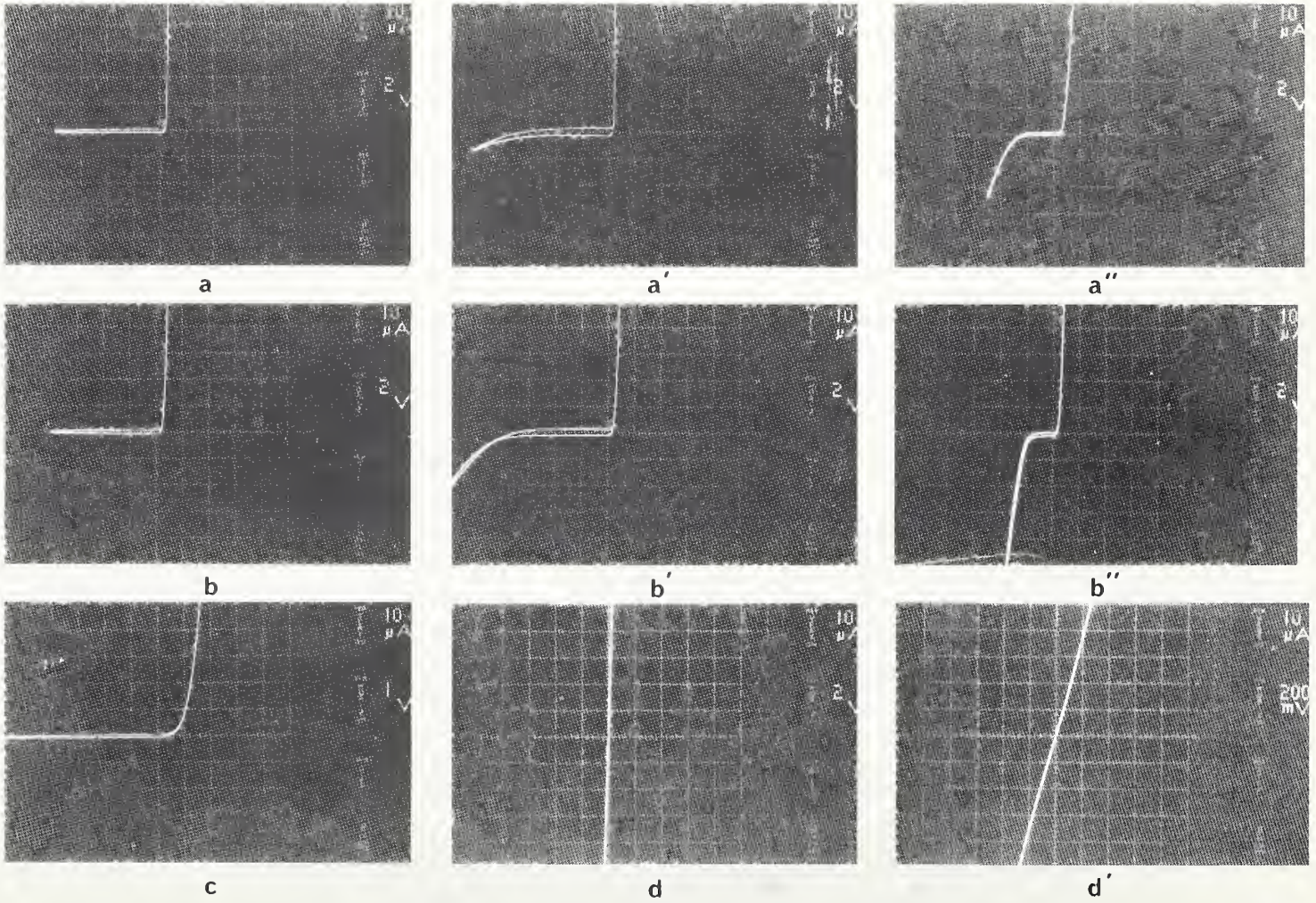


Figure 13. Typical I-V characteristics for Schottky barriers on p- and n-type ion-implanted silicon surfaces (see table 1 for description of samples).

Table 1. Typical Schottky Barrier Structures on Ion-Implanted Silicon Surfaces.

Identification[a]	Implant	Diameter (mm)	Metal	C_0(pF)
a	300-keV boron	0.13	aluminum	2.5
a'	300-keV boron	0.25	aluminum	11-14
a"	300-keV boron	0.25	aluminum	11-14
b	600-keV phosphorus	0.13	gold	2.7
b'	600-keV phosphorus	0.25	gold	11-14
b"	600-keV phosphorus	0.25	gold	11-14
c	300-keV boron	0.13	titanium-gold	2.6
d	300-keV boron	0.13	aluminum[b]	15
d'	300-keV boron	0.13	aluminum[b]	15

[a] I-V characteristics shown in figure 13.
[b] Silicon dip etched in HF before aluminum deposition.

Four samples implanted with 300-keV boron were selected from other experiments which had already been carried through the C-V profiling stage and were successively annealed at 100°C, 200°C, and 250°C in air, while C-V profiles were measured after each annealing step. One sample, which had been annealed at 750°C and yielded a normal C-V profile, was chosen as a control sample to see what effect this heat treatment had on a normal sample; the measured range and straggle parameters of this sample did not change, but the shape to the curve became slightly more Gaussian and smoother. The other three samples were chosen because of their originally poor C-V profiles to see if thermally accelerated aging could improve their profiles.

One of these samples had been annealed at 450°C and should have been normal, but all dots initially produced C-V profiles that were too shallow and too high in dopant density, or showed a double peak, one at nearly the correct depth and one closer to the surface. The 100°C heat treatment caused no change. The 200°C treatment resulted in a great improvement. All dots produced nearly normal curves; some exhibited a rising tail to the surface. After the 250°C treatment, some improvement occurred in the deep side tail, but the surface side of the peak became differently sloped and curved too much. This experiment led to the tentative conclusion that a 200°C ± 25°C heat treatment would not harm good C-V profiles and might improve initially poor ones.

The remaining two samples were random and aligned implants annealed at 1050°C. Most of the dots on these two samples had initially produced no profile at all; one or two dots had given a peak at the proper depth, but were unintelligible everywhere except at the peak, yielding only a value of R_p. The 100°C and 200°C heat treatments had no effect at all. The 250°C treatment seemed to have a slight effect on the curves, but produced no improvement. It is known from SIMS measurements [18] that boron begins to diffuse at about 900°C and that by 1050°C the boron moves significantly, some probably to the surface. The tentative conclusion is that annealing at temperatures above 900°C is not satisfactory.

3.6 Summary

In the preceding sections, we discussed a number of aspects of Schottky diodes appropriate for differential C-V profiling. Some of the conclusions of this work are listed below:

- Schottky diodes must have fairly hard I-V characteristics to give valid C-V profiles.
- Schottky diode areas must be accurately known or measured (~2 percent) to give acceptably accurate C-V profiles.
- Schottky diode diameters between about 0.1 and 0.3 mm gave good yield and undistorted profiles; larger diodes produced erroneous and nonreproducible profiles. Area presents a tradeoff between higher ratio of peripheral edge to area for small areas and higher probability of overlaying a defect for large areas. The 0.13-mm dots gave consistently good results, but 0.25-mm dots were sometimes poor (shorted). Lower defect density material

might allow larger area, except that for larger areas, errors may result from the larger capacitance and lower diode Q.

- Diode breakdown voltages must be adequate to allow the implanted region to be depleted completely, or only partial profiles will be obtained.

- Silicon surfaces chemically cleaned prior to metallization gave better I-V characteristics and C-V profiles than surfaces which had been HF etched.

- Gold on n-type silicon and aluminum or titanium on p-type silicon are good choices of Schottky metallizations; others may or may not be good and should be carefully investigated before being used.

- Aluminum and gold Schottky barriers should be allowed to "age" for one and three days, respectively, before profiling to ensure stable, reproducible C-V profiles. Aging of aluminum and gold Schottky barriers was observed to occur as described in the literature; that is, the I-V and C-V characteristics changed with time and then stabilized. Aluminum Schottky barriers on clean (unetched) or cleaved silicon surfaces typically stabilize in a few hours to one day. Other metals like gold may require a few days. Once stabilized, I-V and C-V characteristics were not observed to change over 24 months.

- Special treatments to improve Schottky barrier diodes: no improvement was observed when a shallow p^+-surface layer was implanted on a p-implanted surface. In particular, this layer did not give C-V profile data closer to the surface. Annealing implanted surfaces (prior to Schottky metal deposition) in air instead of in dried argon or nitrogen resulted in poorer I-V characteristics and in poor C-V profiles. Heating surfaces with poor I-V and/or C-V characteristics had no effect on some implanted surfaces, and on others, 200 or 250°C caused noticeable improvement, while 100°C did not.

As a result of our study of thousands of Schottky diodes on surfaces implanted with a wide variety of ions, energies, and fluences, we have been able to construct the guide shown in figure 14 for values of zero-bias capacitance that will yield good C-V profiles. This guide is principally based on diodes with diameter of 0.13 mm. A significant feature of this guide is that the usable capacitance values decrease as the depth of the implanted profile increases. This occurs for deeper implants at roughly constant ion fluence. Higher fluences can be used at low energies (shallower penetration). The upper limits of fluence that we observed are roughly: 1 to 1.5×10^{12} cm^{-2} for ions and energies that produce profiles that extend deeper than 3 μm; 1.5 to 2.5×10^{12} cm^{-2} for 1 to 3 μm; and 2 to 5×10^{12} cm^{-2} as the depth decreases below 1 μm. These quoted fluences are for ions that produce full electrical activity. These doses may be divided by the electrical activation coefficient for cases of incomplete activation.

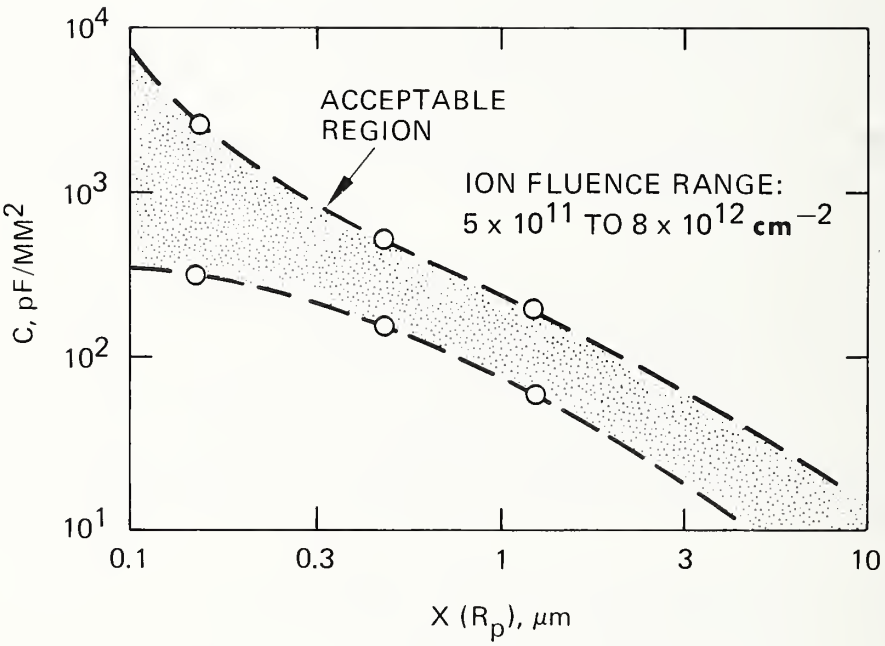


Figure 14. Capacitance values for good C-V profiles of varying depth.

4. SAMPLE PREPARATION, IMPLANTATION, AND PROCESSING

4.1 Summary

The following procedure has been developed and used to prepare and profile samples reproducibly using the differential C-V technique with reverse-biased Schottky diodes.

Starting Material: Select 10 to 100 Ω•cm *n*- or *p*-type silicon (*n* for *n*-type implants and *p* for *p*-type implants) (see sec. 4.2).

Cleaning: Rinse with trichlorethylene, acetone, alcohol. Rinse with deionized water. Do not etch or cleave.

Formation of Back Contacts: *n*-type: Implant back surface with low-energy *n*-type dopant to make n^+ layer (e.g., As^+). *p*-type: Implant back surface with low-energy *p*-type dopant to make p^+ layer (e.g., B^+ or Al^+).

Implantation: Implant desired dopant in front surface of sample, under desired conditions, such as in the random equivalent or in an aligned orientation [19,57,58].

Anneal: To activate implanted dopant anneal in vacuum, in nitrogen from liquid nitrogen, or in argon for 20 to 30 min at the appropriate temperature for the implanted dopant or for a selected annealing study. Annealing studies are performed at this point by varying the annealing temperature for a group of pieces cut from the same implanted wafer.

Schottky Barrier Formation: Evaporate metal films about 100 nm thick over the implanted surface of silicon wafers to form Schottky metallization. Define arrays of dots 0.13 and 0.25 mm in diameter by a metal mask or by photolithography. For thermal evaporation of aluminum and gold, use deposition rates of about 10 nm/s and vacuum conditions of about 2 to 6 × 10^{-6} Torr during evaporation. For electron-beam evaporation, use a vacuum condition between 5 × 10^{-8} and 2 × 10^{-7} Torr and a deposition rate between 0.2 and 0.6 nm/s. (Film thicknesses in the electron-beam evaporation system could be controlled to ±2 nm.)

I-V Measurements: Measure the I-V characteristics of the Schottky diodes in order to determine three important qualities of each diode before C-V profiles are measured. Accept only diodes which are not shorted, which have "hard" I-V characteristics, and which exhibit no significant leakage. Determine the value of voltage at the beginning of breakdown or determine that breakdown does not occur at the maximum voltage that will be used to obtain the C-V profile; the maximum reverse-bias voltage that may be required to deplete through a deep implant may be as much as 100 V.

C-V Measurements: Calculate x and n(x) calibrations using appropriate equations for the profiler being used. Calibrate the profiler recorder. Mount the sample. Make contact with the probe to give a stable capacitance reading. Raise the bias voltage to a level that brings the profile to the background level on the recorder. Switch the profiler to automatic sweep and record the C-V plot as the reverse-bias voltage decreases to zero.

Alternatively, plot the profile for increasing reverse-bias voltage. (Forward and reverse profiles agree if the voltage sweep rates are sufficiently slow that no distortions occur. The increasing voltage technique is especially useful when the implanted profile is very deep and there is a risk of breaking down the diode before the depletion region is driven entirely through the distribution. Measuring the profile in the increasing voltage mode may allow a profile to be obtained up to the breakdown voltage, whereas increasing the voltage to the high breakdown voltage first may cause an irreversible voltage breakdown change in the diode.)

4.2 Material

There are many sources of good silicon today. Therefore, it is probably useful only to state what material was found to be satisfactory for the experimental work described here. While some material was used from other sources, especially for particular crystallographic orientations, most of the work was done using (low-oxygen) float-zone-refined silicon. The material was chem-mechanically polished to within ±1 deg of the (111) surface with a [110] flat and had fewer than 300 etch pits per square centimeter.

The older literature estimates that a natural oxide less than 2.5 nm thick exists on such surfaces; newer literature estimates it to be about 0.5 or 1 nm. (See sec. 3.3.) We performed a measurement using Rutherford backscattering to determine the approximate amount of oxygen and other observable heavier elements on the surface of the material being used. The results for the material described above were that the amount of oxygen on the surface was $\sim 3 \times 10^{15}$ cm^{-2}, which is compatible with the 0.5 or 1 nm number, and no heavier elements were observed within the detection sensitivity.

5. DATA ANALYSES

5.1 The Kennedy-O'Brien Correction

The Kennedy-O'Brien correction [3] is a modification applied to the measured majority carrier density n(x) to correct it to the true ionized impurity density distribution $n_D(x)$. This correction is given as:

$$n_D(x) = (x) + \frac{kT\varepsilon}{e^2} \frac{d}{dx} \left[\frac{1}{n(x)} \frac{dn(x)}{dx} \right] . \qquad (19)$$

At the peak of carrier density profiles where R_p is measured, there is essentially no correction to be made for values of R_p or R_m. The correction has a negligible effect on values of ΔR_p (or σ) if these are measured above 10 percent of the peak density, as they usually are.

The magnitude of the correction is illustrated in figures 15 and 16, for profiles of various depths and shapes. The magnitude of the correction depends on the magnitude, the slope, and the second derivative of the distribution [see eq (19)]. The correction is seen to be small for deep

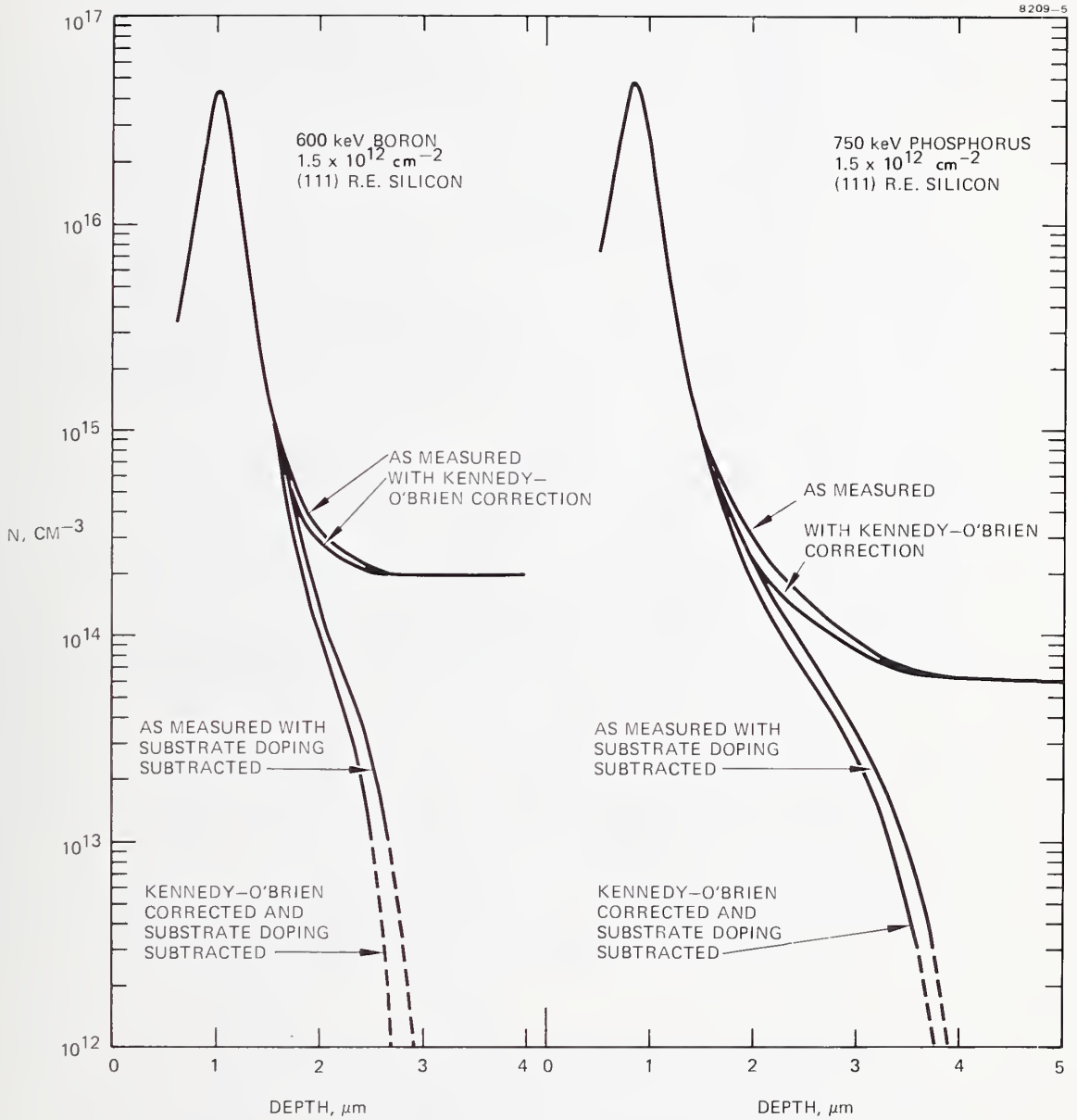


Figure 15. Typical deep C-V profiles showing effects of Kennedy-O'Brien correction and of correction for substrate dopant level.

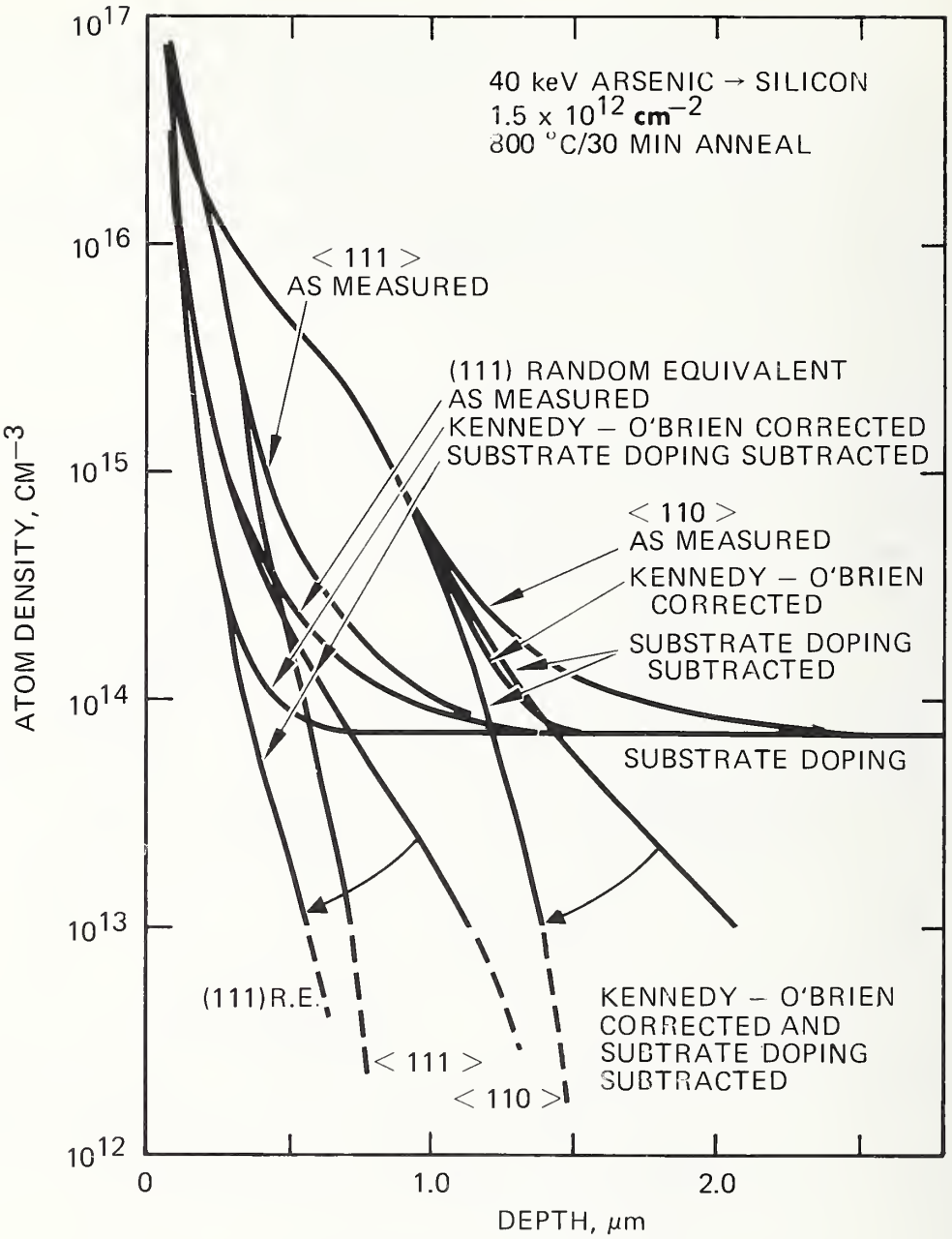


Figure 16. Typical shallow C-V profiles showing effects of Kennedy-O'Brien correction and of correction for substrate dopant level.

profiles (fig. 15); it is less than 1 percent in the depth at 10^{15} cm^{-3}, and varies from 4 to 6 percent in the depth from the mid 10^{14} cm^{-3} range to 10^{12} cm^{-3}. These errors in depth are less than the experimental error. The corresponding errors in the total implanted distribution (the areas between the as-measured and corrected profiles) are less than 0.3 percent. The magnitude of the error increases as the profiles become shallower. An example of the effect on profiles of different shapes is illustrated in figure 16 by showing the as-measured and corrected profiles for 40-keV arsenic in the (111) random equivalent, <111> channeled, and <110> channeled orientations. For the <110> channeled case, where the second derivative is negative (above 10^{15} cm^{-3}), the correction is negligible; where the second derivative is positive (below ~5 × 10^{14} cm^{-3}), the correction is progressively larger with increasing depth, causing a significant correction to the profile and being ~13 percent in depth at 10^{14} cm^{-3} and increasing to ~40 percent at 10^{13} cm^{-3}. For the <111> channeled profile, the correction in depth begins to be significant at 3 × 10^{15} cm^{-3}, is 10 percent at 1 × 10^{15} cm^{-3}, is 35 percent at 10^{14} cm^{-3}, and is ~50 percent at 10^{13} cm^{-3}. For the (111) random equivalent orientation, the entire profile is corrected from its beginning at 3 × 10^{16} cm^{-3}; the correction is ~8 percent in depth at 1 × 10^{16} cm^{-3}, is ~35 percent at 1 × 10^{15} cm^{-3}, is 60 percent at 1 × 10^{14} cm^{-3}, and is 80 percent at 1 × 10^{13} cm^{-3}. The corresponding errors in the total implanted distribution are 0.3 percent for the <110> channeled profile, 0.9 percent for the <111> channeled profile, and >5 percent for the (111) random equivalent profile. The corresponding profile for 20-keV arsenic in the (111) random equivalent orientation after the correction and after substrate dopant level subtraction is zero everywhere in the measured region; that is, it does not exist deeper than 0.1 μm with a density above about 10^{14} cm^{-3}.

In summary, the Kennedy-O'Brien correction is small for deep profiles and becomes increasingly significant as profiles become shallower. The correction is greater when the second derivative is negative, such as it is for tails on random equivalent implants, than for when it is positive, such as it usually is for channeled profiles. The correction decreases as the density increases; it is significant above 10^{15} cm^{-3} only for profiles less than ~0.5 μm in depth. The correction can alter shallow (< ~0.5 μm) C-V profiles drastically and should always be applied in those cases.

5.2 Background Subtraction

Ordinarily, the differential C-V profiling technique is used to measure a carrier density or dopant profile in a semiconductor material with a base dopant level in the 10^{14} to 10^{15} cm^{-3} range. This background dopant level is ordinarily recorded as part of the differential C-V profile and can be easily subtracted from the total recorded profile after the Kennedy-O'Brien correction has been made. This is illustrated in figures 15 and 16 for implanted profiles in *n*-type and *p*-type silicon with background dopant levels of 0.6 × 10^{14} cm^{-3} and 2.0 × 10^{14} cm^{-3}, respectively. It is seen that the resulting implanted profiles can be extended to 10^{13} cm^{-3}, or even to ~10^{12} cm^{-3}, by the subtraction of the background dopant level. The accuracy of the curves in the low 10^{13} cm^{-3} and 10^{12} cm^{-3} decades is progressively reduced.

6. COMPARISONS OF C-V AND SIMS PROFILES*

6.1 The SIMS Technique and Experimental Accuracies

The general SIMS technique is described adequately in the literature [59, 60]. A comprehensive discussion of the considerations that affect the accuracy of SIMS measurements of implanted depth distributions, including ion beam, environment, sputtering process, and target surface and bulk effects, is given by Hofker [18]. In the results reported here, essentially the same type of experimental equipment, techniques, and parameters were used as Hofker used. In brief, an oxygen ion beam was used, typically of 5-keV energy and 1- to 5-μA current; the secondary ions recorded were $^{6,7}Li^+$, $^{9}Be^+$, $^{10,11}B^+$, Al^+, AsO^-, SbO^-, etc.; the environment pressure was $\sim 3 \times 10^{-7}$ Torr; data are ignored for the first ~10 nm of sputtered surface; and depth scales are calibrated by surface profilometer measurements of the sputtered crater depths in the center of the craters, combined with monitoring of the sputtering rate. The secondary ions were collected from only the central region of the sputtered crater and several sputtering runs were compared for reproducibility for each implanted region, both for profile and for crater depth. Hofker indicates that crater depth measurements are accurate to within about 3 percent. Reproducibility from measurement-to-measurement is about ±5 percent. Our results would indicate a reproducibility of ±5 to 10 percent. Crater profiles are flat within ±10 percent in the region from which the secondary ions are collected.

The values of atom density for SIMS depth distributions are determined as follows. For profiles that have not redistributed, the area integral of the profile is equated to the implanted ion fluence. The measured ion fluence may be accurate to within 1 to 5 percent if careful secondary suppression techniques are employed [61], and may be more typically in error by 10 to 20 percent. Thus, SIMS absolute density measurements may be accurate within 5 percent, or 10 to 20 percent. The accuracy within a profile varies with the total number of counts at each depth compared with the background level and counting statistics. For our measurements, the statistical variations at two selected representative values were ±1000 counts at 50,000 counts or 2 percent and ±20 counts at 60 counts or 33 percent. This latter value is representative of the background region or lowest atom density portion of a SIMS profile.

6.1.1 Experimental Errors

For the SIMS data, all depths are accurate to within ±7 percent or 30 nm, whichever is larger. The ±7 percent is determined by the reproducibility of crater depths measured by a surface profilometer; the absolute accuracy of the measurements is probably 30 nm. The relative error in atom density is ±2 percent at 50,000 counts (about the fourth decade of SIMS data) and ±30 percent at 50 counts (about the first decade of SIMS data) from SIMS counting statistics. The absolute error is ±2.5 percent, determined by the accuracy

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* The SIMS data reported here were obtained by Dr. J. Comas of The Naval Research Laboratories. This work was supported in part by ARPA through NBS Orders 708041 and 801846.

of the ion fluence measurement using a current integrator and a good secondary suppression geometry [61].

For the C-V profiles, the rms error in atom density [n(x)] is 7 percent; in depth (x), it is 3 percent, determined from analysis of the C-V profiler equations and the required experimental measurements. The Kennedy-O'Brien correction (sec. 5.1) causes a foreshortening in x of a maximum of about 3 percent in the low 10^{14} cm^{-3} atom density range on the deep side of the profiles, decreasing to 0 percent at the peak of the profile, for slopes that are typical of random equivalent or channeled implanted depth distribution.

Implantation energy in this work was accurate to about 2 percent by periodic calibration of the implanter with a 1-percent, 300-kV voltmeter. The major effect of this ~2-percent error is in the absolute value of ion range; it has little effect on straggle or profile shape parameters. Implanted ion fluences are 2 to 3 percent accurate in absolute value and reproducible to better than 1 percent using current integrators shown to have adequate response to implantation conditions [61].

6.2 Comparison of SIMS Atom and C-V Carrier Distributions

The sensitivities of the SIMS and C-V techniques for beryllium in silicon make the Be-Si system an ideal vehicle for comparison of depth distribution of atoms measured by SIMS and the associated carrier electrical activity (acceptor in this case) measured by differential C-V profiling. The sensitivities are such as to allow the two techniques to be used on the same or identically implanted samples over a small range of ion fluence from about 1×10^{12} to 5×10^{12} cm^{-2} [62]. The approximately 40-percent electrical activation of acceptor activity for beryllium in silicon allows the beryllium fluence to be as high as 5×10^{12} cm^{-2} for 40 to 600 keV for the C-V technique. The sensitivity of positive-ion-mode SIMS for beryllium allows SIMS profiles to be measured for densities as low as ~10^{13} cm^{-3} (near 10^{-10} parts) or for a corresponding fluence down to 10^{12} cm^{-2}.

Normalized SIMS and C-V profiles for 100-keV beryllium in random equivalent silicon are shown in figure 17. The C-V acceptor distributions are for 500°C annealing temperature and an ion fluence of 3×10^{12} cm^{-3}. Two unannealed SIMS atom distributions are shown for comparison. The lower fluence SIMS data are seen to agree with the C-V acceptor distribution on the deep side of the profile. The higher fluence SIMS curve is less deep. Little change occurs in the SIMS distribution after 500°C annealing [62].

The following conclusions are drawn from these and other similar data: 1) At 100-keV ion energy, the C-V electrical profile agrees with the SIMS atom profile on the deep side for the comparably low fluence. 2) The SIMS profile for the low fluence is relatively wider on the deep side (deeper) because of the greater effect of channeling that results from scattering in the random equivalent orientation of crystalline silicon for densities less than about one order of magnitude below the maximum. For some fluence between 10^{13} and 5×10^{15} cm^{-2}, the channeling tail effect saturates because damage blocks the channels. 3) The SIMS and C-V profiles yield about the same value of half width (ΔR_p) at $e^{-1/2}$ N_{max}. 4) The C-V curve is somewhat higher than SIMS curves on the surface side of the distribution. This is attributed to

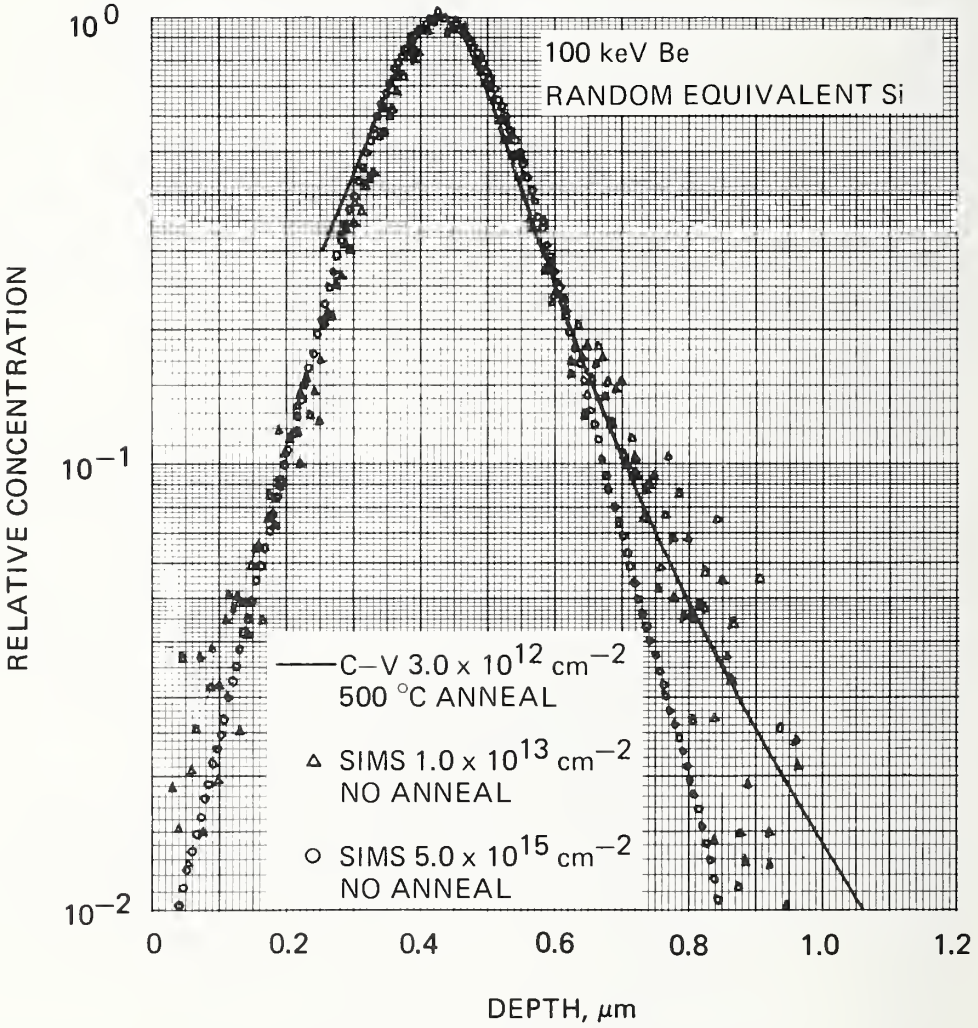

Figure 17. SIMS and C-V profiles for 100-keV beryllium in silicon.

the C-V profiling measurement technique; as the surface is approached, the value of capacitance measured by the system increases to its maximum value and the Q of the diode approaches the region where some error may be introduced that increases the value of the density artificially when high resistivity silicon is used to give good information on the deep side. The additional use of a lower resistivity substrate would give better near-surface data, at the expense of data for lower density. The use of a lower ion fluence would produce a lower zero-bias capacitance and would also improve this situation. This effect is seen to be small or negligible where ΔR_p is usually measured. The concept of a ΔR_p that is associated with a Gaussian distribution is seen to be rather inappropriate for beryllium depth distributions because they are not Gaussian; both C-V and SIMS distributions become continuously wider than Gaussian as the density decreases, corresponding to a fourth moment or kurtosis.

Similar curves for 300-keV boron are shown in figure 18 to allow a comparison between beryllium and boron, a commonly used ion in silicon. Annealing at 800°C is done to ensure full electrical activation at these low ion fluences. The C-V profile for the much lower fluence agrees with the unannealed SIMS profile on the deep side but is again slightly higher on the surface side, such as to agree roughly with the similarly annealed SIMS profile. These profiles imply that 800°C annealing causes a movement of boron ~50 to 75 nm in each direction for a fluence of 3×10^{14} cm^{-2}, but not for 1.5×10^{12} cm^{-2}. Independent measurements have shown that no diffusion occurs at 800°C for 1.5×10^{12} cm^{-2} boron implants. This suggests that the movement is implantation-damage-associated. The deep side curves are seen to have opposite curvature for the two annealing conditions. The widths (ΔR_p) are again the same.

7. CONCLUSIONS AND SUMMARY

Ion-implanted depth distributions can be obtained from C-V measurements for the columns III and V dopants in silicon and for other ions that produce donor or acceptor electrical activity, such as columns II and VI elements. The range of ion energy that can be studied corresponds to that which penetrates about 150 nm (about 10 keV for light ions, up to about 80 keV for heavy ions) to at least 1 or 2 MeV.

We observe that the depth profiles for light ions exhibit distinct channeling peaks and only small scattering tails. We observe that as the ion mass increases, the scattering-channeled tails increase significantly and the channeling peaks become indistinct and finally disappear. Our measured ranges R_p agree quite well with the LSS calculations of Brice (1971) and Johnson and Gibbons (1970) for nearly all ions usually within a few percent. The range straggles calculated by Brice are larger than those of Johnson and Gibbons and our measured ΔR_p's are up to 50 percent larger still than the values of Brice in agreement with the discussion of Kalbitzer and Detzman [63].

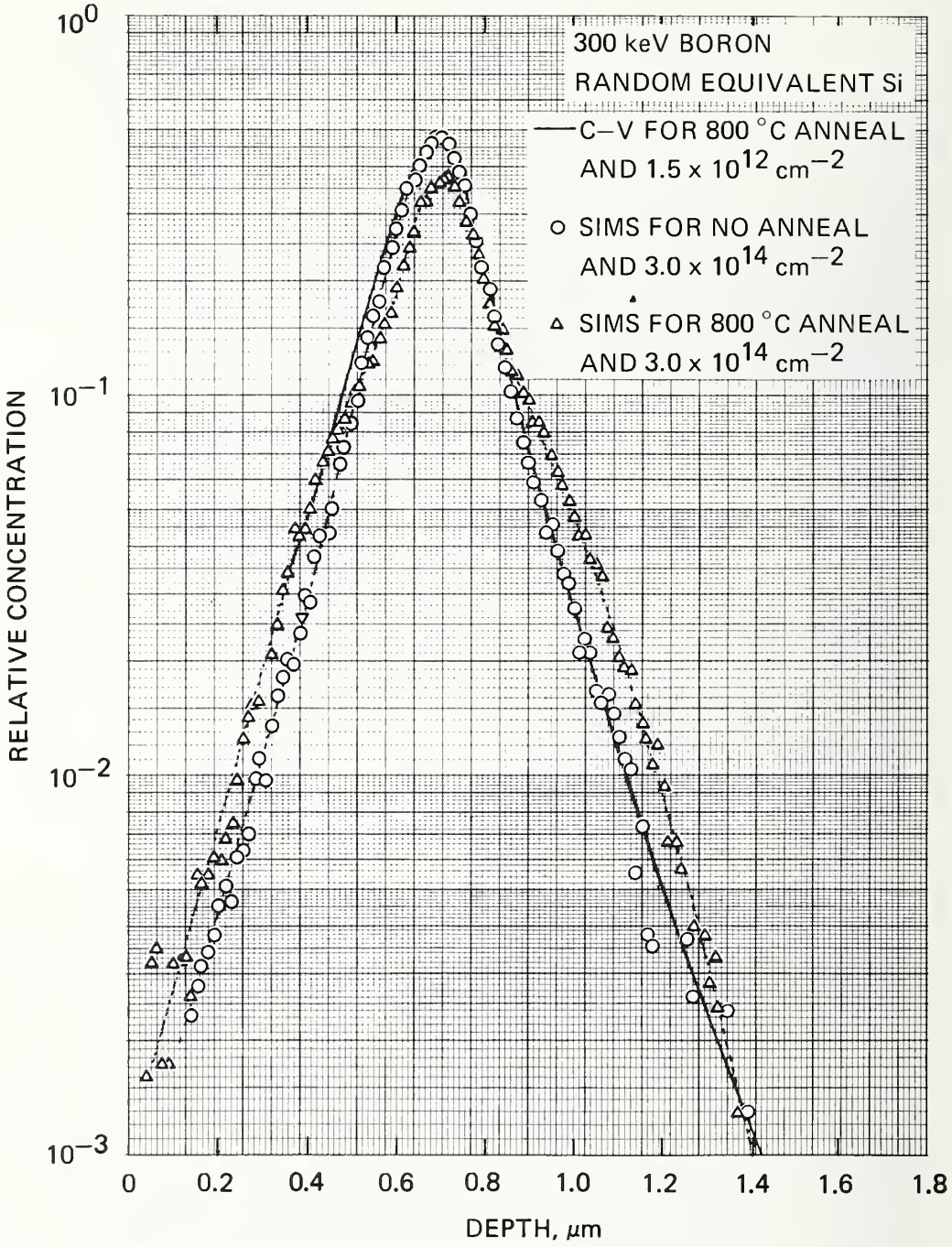

Figure 18. SIMS and C-V profiles for 300-keV boron in silicon.

7.1 What Can Be Measured By Differential C-V Profiling

Our extensive investigations during this program have shown that differential C-V profiling of the electrical activity in ion-implanted semiconductor layers can be used to study a wide variety of characteristics of the implantation and annealing process steps, including those listed below.

- Annealing Activation: the depth distribution and total activation efficiency; threshold temperatures for the onset of electrical activation and electrical activity as a function of annealing temperature; annealing time requirements at a given temperature.

- Thermal Redistribution: changes in the depth profile of electrical activity as annealing progresses.

- Values of Profile Parameters: R_p and ΔR_p for Gaussian depth distribution; R_m, γ_1, and β_2, for non-Gaussian depth distributions; R_c, σ_c, γ_{1c}, and β_{2c}, the first, second, third, and fourth moments of channeled peaks; the fraction of ions contributing to the channeled, dechanneled, random, and (sometimes) quasi-random fractions of an aligned implantation depth distribution.

- Range-Energy Curves: the depth distributions of electrical activity as a function of ion energy and parameters such as peak depth (R_m) *versus* energy, ΔR_p *versus* energy, R_c *versus* energy, etc.

- Stopping Power Values: from the range-energy curves.

7.2 Limitations on the C-V Profiling Technique

There are distinct limitations on the ranges of validity of the technique, discussed in detail in the body of this report. The ranges of carrier density and depth in which the technique can yield reliable results are:

- Carrier Density: $\sim 10^{13}$ to mid 10^{17} cm^{-3}. Densities below 10^{13} cm^{-3} can be recorded for high resistivity substrates (such as semi-insulating material), but they are of questionable validity due to the small values of Q for these conditions. The lower part of the 10^{13} cm^{-3} decade usually results from subtraction of the background dopant density and therefore becomes less accurate than the higher densities.

- Depth: 80- to 100-nm minimum for shallow implants, successively greater depths for successive deeper implants; the maximum depth has no particular limit, but a practical limit is imposed by the breakdown voltage of the diode under study. Good diode technology can make this value high. We have observed breakdown voltages of 100 to 120 V and corresponding implanted profiles up to 10 μm deep.

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