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Test Patterns NBS-28 and NBS-28A: Random Fault Interconnect Step Coverage and Other Structures

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Semiconductor Measurement Technology: Test Patterns NBS-28 and NBS-28A: Random Fault Interconnect Step Coverage and Other Structures

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Semiconductor Measurement Technology: TEST PATTERNS NBS-28 and NBS-28A: RANDOM FAULT INTERCONNECT STEP COVERAGE AND OTHER STRUCTURES

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ABSTRACT

This report describes microelectronic test structures for detection of random faults in interconnect step coverage and associated process parametric and physical analysis test structures included in two test patterns, NBS-28 and NBS-28A, recently designed under the device test structure program at the National Bureau of Standards. Information about the geometry and application of the test structures in these two test patterns is provided for those who wish to fabricate or utilize the test patterns prior to their complete evaluation at NBS. Test pattern NBS-28 consists of a random fault test structure for measuring the integrity of metal interconnects stepping over polysilicon lines. The structure is a metal serpentine 0.93 m long with 8-µm linewidth and spacings stepped over polysilicon lines with 8-µm linewidths and spacings. The serpentine is divided into nine arrays containing 150, 220, 480, 960, 2880, 5760, 13440, 28800, and 62400 steps, respectively. Test pattern NBS-28A contains three similar, but reduced, step-coverage structures with 4-, 2-, or 1-µm linewidths and spacings. Test pattern NBS-28A also contains 37 other microelectronic test structures for providing process parameter or physical analysis information. Some of these are new structure designs which are now undergoing development and evaluation.

Key Words: Electronics; interconnect; microelectronics; random fault; step coverage; test structures.

1. INTRODUCTION

Microelectronic test structures are useful for measuring a variety of material and process parameters which affect the functioning of integrated circuits [1]. One critical parameter is the density of random faults. As a part of a comprehensive project to develop and evaluate microelectronic test structures, the National Bureau of Standards has designed two test patterns, NBS-28 and NBS-28A, for detecting random faults in interconnect step coverage. This report provides information about the geometry and application for those who wish to fabricate the test patterns prior to their complete evaluation at NBS. The test patterns are compatible with a simple nMOS or pMOSprocess. The structures in the test patterns are divided into three general groups: random fault structures for interconnect integrity; process parametric structures; and physical analysis structures. These are discussed in sections 2 through 4.

2. RANDOM FAULT STEP-COVERAGE STRUCTURES

Interconnections represent one of the most serious problems in VLSI circuits [2]. The number of faults is proportional to interconnect area, and thus the problems of detecting and eliminating faults become worse with everincreasing IC size and complexity. For example, with 12 interconnection levels, circuit wiring will consume more than half the area of a die with 25,000 gates; with fewer levels the area consumed is even greater [2]. The random fault structures on test patterns NBS-28 and NBS-28A are intended to assess the capability of a process to produce a single level of fault-free metal interconnects as a function of area and as a function of linewidth and spacing. The present structure configuration is an extension of the random fault step coverage test structure on test pattern NBS-7 [3-5] redesigned to include more steps with smaller dimensions, and to permit investigation of methods of testing and data analysis in more detail.

Test pattern NBS-28, shown in figure 1, contains a metal interconnect stepcoverage test structure, and two alignment structures for positive and negative photoresist. The pattern was designed to be fabricated in a selfaligned silicon gate nMOS or pMOS process. The step-coverage structure is a serpentine of metal with lines and spacings of 8-µm stepping over polysilicon lines with 8-µm widths and spaces. A deposited oxide typically 700 nm thick separates the metal and polysilicon. The profile of this oxide over the polysilicon step is strongly dependent on processing and is one of the major factors affecting the quality of the metal interconnect. The serpentine, 0.931 m long, is subdivided into nine subarrays containing 150, 330, 480, 960, 2880, 5760, 13440, 28800, and 62400 steps. A configuration such as this permits the interconnect yield, i.e., the fraction of unfaulted subarrays of interconnect area A on a wafer, to be measured experimentally. The serpentine configuration has the advantage of compactness. It has the disadvantage that a short between metal lines, an unintended fault, may interfere with measurement of the intended fault, an open circuit.

Double probe pads on the structure are used for two purposes. (1) A continuity test between the two probes on each pad can be used to detect a prober registration problem or an improperly etched passivation layer. (2) A precise four-probe resistance measurement can be made which may be useful in detecting shorts. Current is applied through two probes and voltage is measured with two other noncurrent-carrying probes to eliminate the effects of contact resistance between probe and pad.

The polysilicon lines are not connected together electrically, except for two which are connected together at one end and to probe pads at the other end. A four-probe resistance measurement can be made to check the quality of the long polysilicon lines. The resistance of these lines can be estimated using the sheet resistance and linewidth data which can be obtained from the double cross-bridge structures, such as those included in test pattern NBS-28A.

A detail of a portion of the upper left-hand corner of the step-coverage structure is shown in figure 2. The solid bars are metal and the light bars, polysilicon. The detail shows the connection between the leftmost two polysilicon lines and the extensions of the metal lines leading to the contact pads on the left side of the structure.

The test pattern was designed to be fabricated in a self-aligned silicon gate nMOS or pMOS process [6]. The five mask levels required to fabricate it are shown in figures 3 through 7. The first mask level, in figure 3, is used to define MOSFET sources and drains and other windows in the thermal oxide for doping with impurities by means of diffusion or ion implanting. The second mask level, in figure 4, is used to define polysilicon features. The third mask level, in figure 5, is used to cut windows in the oxide levels for metal-to-diffusion/implant or metal-to-polysilicon regions. The fourth mask, in figure 6, is used to define metal features. The fifth mask, in figure 7, is used to cut windows through the passivation layer to the bonding pads.

The structures numbered 1, 2, and 3 in test pattern NBS-28A in figure 8 are reductions of the 8-µm linewidth and spacing random fault step-coverage structure to 4-, 2- and 1-µm lines and spacings, respectively. The total length of metal line in each is 46.6, 23.3, and 11.6 cm, respectively. The five mask levels required to fabricate test pattern NBS-28A are shown in figures 9 through 13. They serve the same functions as those described for test pattern NBS-28.

3. PROCESS PARAMETRIC STRUCTURES

Process parametric structures are electrical test structures used for assessing material, process, and device parameters. When a problem is encountered with the process, the process parametric structures can be helpful diagnostic tools. There are 28 process parametric structures, all on the NBS-28A test pattern (see fig. 8). They include: capacitors, contact resistors, double (orthogonal) cross bridges, MOSFETs, inverters, an NAND gate, and surface leakage structures. Key dimensions of these structures are given in table 1. There are four capacitors (4 through 7): circular geometry with polysilicon over gate oxide over diffusion; square geometry with polysilicon over gate oxide over diffusion; circular geometry with metal over deposited and field oxide over substrate; and square geometry over deposited and field oxide over substrate. These are used for dielectric measurements and for comparison of the effects of round and square geometry on the measured value of capacitance.

The contact resistors (8 and 9) are used for the four-probe measurement of contact resistance of metal-polysilicon and metal-diffusion/implant contacts.

The double cross bridges are a new design, an extension of the cross bridge [7]. They are intended for measuring metal, polysilicon, and diffusion/implant sheet resistance and linewidth in orthogonal directions. The three structures (10, 11, and 12) are shown in more detail in figures 14, 15, and 16, respectively. A second four-probe bridge sheet resistor has been added to the original cross bridge with its long axis normal to the four-probe bridge sheet resistor in the cross bridge. The metal sheet resistance and linewidth obtained from structure 10 are useful for estimating the resistance of the metal lines in the random fault structures.

The MOSFETs (13 through 22, 27, 28, and 30), inverters (23 through 26), and NAND gate (29) are used to determine if the process can produce a working

active device and to compare the performance of active devices of differing channel and gate geometries.

The two structures for measuring surface leakage are new and included in the test pattern for initial evaluation. The first surface leakage structure (31), shown in figure 17 in more detail, is intended to measure conductance along a field oxide-substrate interface. A serpentine of field oxide is produced by etching a pattern with interdigitated fingers in the oxide with mask level 1 (fig. 9). The fingers are doped in the diffusion/implant step of the process. Leakage current between the fingers is measured with an ammeter in series with a voltage source connected between the top and bottom probe pads of the structure in figure 17. The effective conducting serpentine region (between the fingers) is 8 µm long and 14.5 mm wide. Metal covers the serpentine and most of the interdigitated fingers for biasing if necessary.

The second surface leakage structure (32), shown in figure 18, is intended to measure the conductance along the gate oxide-substrate interface. In this case a serpentine of polysilicon over gate oxide in the self-aligned silicon gate process is used to define intedigitated fingers (see mask level 2, fig. 10). These are also doped in the diffusion/implant step of the process. The leakage measurement and serpentine geometry are the same as in structure number 31. The polysilicon can be used for biasing, if necessary.

Structure No.	Description
4.	Round capacitor with 0.0829 mm ² area, comprised of polysilicon over gate oxide over diffusion/implant.
5.	Same as 4 except square geometry with same area.
6.	Square capacitor with 0.0829 mm^2 area, comprised of metal over field oxide.
7.	Same as 6 except for round geometry with same area.
8.	Four terminal contact resistor with 8- μm square window, metal-to-diffusion/implant.
9.	Same as 8 except for metal-to-polysilicon.
10.	Double cross bridge with center-to-center distance between the voltage taps, $L_m = 120 \ \mu m$; linewidth, $W_m = 16 \ \mu m$; voltage tap width, $D_m = 8 \ \mu m$; and voltage tap length, $T_m = 32 \ \mu m$.
11.	Same as 10 except the conductor is polysilicon instead of metal and $T_m = 16 \ \mu m$. The polysilicon is deposited on a gate oxide over a diffusion/implant window to simulate a silicon gate.
12.	Same as 11 except the conductor is a diffusion/implant region in- stead of polysilicon.
13.	FET with 160- μm wide channel and 28- μm wide self-aligned polysilicon gate.
14.	FET with 160- μm wide channel and 26- μm long channel. Unlike the other FETs in this test pattern, this FET has a metal gate 28 μm wide over field oxide.
15.	FET with 120- μm wide channel and 8- μm wide self-aligned polysilicon gate.
16.	FET with 12- μm wide channel and 8- μm wide self-aligned polysilicon gate.

Structure No.	Description
17.	Same as 15 except channel and gate width are reduced 1/2.
18.	Same as 16 except channel and gate width are reduced 1/2.
19.	Same as 15 except channel and gate width are reduced 1/4.
20.	Same as 16 except channel and gate width are reduced 1/4.
21.	Same as 15 except channel and gate width are reduced 1/8.
22.	Same as 16 except channel and gate width are reduced 1/8.
23.	Inverter made of structures 15 and 16 (8- μ m gates).
24.	Inverter made of structures 17 and 18 (4- μ m gates).
25.	Inverter made of structures 19 and 20 (2- μ m gates).
26.	Inverter made of structures 21 and 22 (1- μ m gates).
27.	Structure 15 reduced 1/8. The entire structure is reduced rather than just the channel width and gate width as in structure 21.
28.	Structure 16 reduced 1/8. The entire structure is reduced rather than just the channel width and gate width as in structure 22.
29.	NAND gate formed by adding structure 15 to structure 23.
30.	Short channel MOSFET test structure. There are 9 gates of 1-, 1.5-, 2-, 2.5-, 3-, 3.5-, 4-, 6-, and 8-µm width [8].
31.	Field oxide surface leakage structure. The effective field oxide surface is 14.5 mm wide by 8 μm long.
32.	Gate oxide surface leakage structure. The effective gate oxide is 14.5 mm wide by 8 μm long.

4. PHYSICAL ANALYSIS TEST STRUCTURES

Physical analysis structures are visual, mechanical, and analytical test structures used for process control. Eight physical analysis structures which are described in table 2 are located on test pattern NBS-28A. These are the structures numbered 33 through 40 in figure 8. They include visual aids for alignment, linewidth resolution, and etch control; a profilometer for mechanical thickness measurements; diffusion/implant and polysilicon areas for measurement of impurity profiles by means of secondary ion mass spectroscopy (SIMS area); and two sets of alignment marks, one for positive and one for negative photoresist. Each set contains marks for coarse and fine alignment. Coarse alignment marks for positive and negative photoresist are also provided on NBS-28.

For clarity, a larger scale drawing of the profilometer (structure number 37 in fig. 8) is shown in figure 19. Figure 20 is a schematic of a longitudinal section through the middle of the profilometer showing the approximate thick-nesses of the various levels.

Structure No.	Description
33.	Secondary ion mass spectroscopy (SIMS) area; 240-µm square diffusion/implant with 232-µm square passivation window.
34.	Secondary ion mass spectroscopy (SIMS) area; 240-µm square polysilicon with 232-µm square passivation window.
35.	Resolution structure on each mask level with 1-, 2-, 4-, 8-, and $16-\mu$ linewidths.
36.	Etch control structure on each mask level with 0-, 1-, 2-, 4-, and 8- μ m spacing on levels 1, 3, and 5, and 0-, 1-, 2-, and 4- μ m spacing on levels 2 and 4.
37.	Profilometer structure for mechanical thickness measurements. Details are shown in figures 19 and 20.
38.	NBS logo.
39.	Positive photoresist mask alignment marks. There are two sets, for coarse alignment (64- by 64-µm squares concentric with 56- by 56-µm squares), and fine alignment (32- by 32-µm squares concentric with 28- by 28-µm squares). Mask levels are indicated by bars following each set of alignment marks.
40.	Same as 39 except that the structure is for use with negative photoresist.

SUMMARY

The structures in two recently designed test patterns, NBS-28 and NBS-28A, have been described. They fall into three groups: random fault structures for assessing the capability of a process to produce fault-free interconnects stepping over polysilicon lines; process parametric structures which include electrical test structures such as capacitors, contact resistors, double cross bridges, MOSFETs, inverters, a NAND gate, and developmental surface leakage structures designed to provide various data for process control; and physical analysis structures such as alignment marks, visual aids for etch control resolution, a profilometer, and SIMS areas.

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Figure 1. NBS-28 test pattern, composite of all levels.



Figure 2. Detail of upper left-hand corner of random fault interconnect step-coverage test structure Dark bars are metal and light bars, polysilicon. A link connects the first two polysilicon lines together. on NBS-28.

Figure 3. Level 1 of NBS-28, source and drain definition level (nMOS or pMOS process). This level is only necessary when being processed with drop-ins of other test patterns or integrated circuits on the same wafer.



Figure 4. Level 2 of NBS-28, polysilicon definition.

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Figure 5. Level 3 of NBS-28 contact window definition.



Figure 6. Level 4 of NBS-28, metal definition.

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Figure 7. Level 5 of NBS-28, passivation openings.



Figure 8. NBS-28A test pattern, composite of all levels.



Figure 9. Level 1 of NBS-28A, source and drain definition (nMOS and pMOS process).



Figure 10. Level 2 of NBS-28A, polysilicon definition.



Figure 11. Level 3 of NBS-28A, contact window definition.



Figure 12. Level 4 of NBS-28A, metal definition.

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Figure 13. Level 5 of NBS-28A, passivation openings.



Figure 14. Metal double cross bridge structure. The dimensions are $L_m = 120 \mu m$, $W_m = 16 \mu m$, $D_m = 8 \mu m$, and $T_m = 32 \mu m$.



Figure 15. Polysilicon double cross bridge structure. The dimensions are $L_m = 120 \ \mu m$, $W_m = 16 \ \mu m$, $D_m = 8 \ \mu m$, and $T_m = 16 \ \mu m$.



Figure 16. Diffusion/implant double cross bridge structure. The dimensions are $L_m = 120 \ \mu m$, $W_m = 16 \ \mu m$, $D_m = 8 \ \mu m$, and $T_m = 16 \ \mu m$.



Figure 17. Field oxide surface leakage structure.



Figure 18. Gate oxide surface leakage structure.







The thick-Schematic of a longitudinal section through the middle of the profilometer. nesses of the levels are approximate. Figure 20.

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