NBS SPECIAL PUBLICATION 400–61

U.S. DEPARTMENT OF COMMERCE / National Bureau of Standards

Semiconductor Measurement Technology:

Metrology for Submicrometer Devices and Circuits

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Semiconductor Measurement Technology:

Metrology for Submicrometer Devices and Circuits

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Issued June 1980

Library of Congress Catalog Card Number: 80-600054

National Bureau of Standards Special Publication 400–61
Nat. Bur. Stand. (U.S.), Spec. Publ. 400–61, 41 pages (June 1980)
CODEN: XNBSAV

U.S. GOVERNMENT PRINTING OFFICE
WASHINGTON: 1980

For sale by the Superintendent of Documents, U.S. Government Printing Office, Washington, D.C. 20402
Price $2.25
(Add 25 percent additional for other than U.S. mailing)

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METROLOGY FOR SUBMICROMETER DEVICES AND CIRCUITS*

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The metrological requirements of semiconductor microelectronics, always challenging, are made even more stringent by the trend toward submicrometer devices and structures. This comes about not only because of the obvious demands associated with the smaller feature sizes of circuit elements but also because of the attendant requirements for more efficient design verification aids, computer simulations, and process validation and control techniques and because of the concurrent trend toward larger die and package sizes. This paper examines the types of metrological requirements associated with submicrometer devices and structures, summarizes the present state of the art in selected critical areas of metrology, and reviews current research and development efforts on advanced measurement technology, especially those at the National Bureau of Standards.

Key Words — Dimensional metrology; electronics; integrated circuits; materials characterization; measurement methods; microelectronics; microstructures; semiconductors.

1. INTRODUCTION

The semiconductor device field has long provided many challenges for the metrologist. The purity, perfection, and cleanness required of the materials, the tiny dimensions of the devices, and the multidisciplinary nature of the field have all contributed to the metrological difficulties. Although a great deal of progress has been made over the years, the speed with which the semiconductor field develops continually provides new challenges. The trend toward submicrometer devices is the latest in a long series of such developments. The more stringent metrological requirements associated with microstructure geometries arise not only because of the obvious demands associated with the smaller feature sizes of circuit elements but also because of the attendant requirements for more efficient design verification aids, computer simulations, and process validation and control techniques, and because of the concurrent trends toward larger die and package sizes.

Two major types of metrology — dimensional metrology and materials characterization — are required to provide the basic understanding of submicrometer structures and to interpret device and circuit characteristics. In addition, ancillary techniques associated with analysis of process chemicals, control of process steps, and characterization of packages are also needed. In this paper, we examine these three types of metrological requirements,

* This report is an edited and expanded version of an invited paper presented at the Conference, Microcircuit Engineering '79 — Microstructure Fabrication, Aachen, West Germany, September 27, 1979.

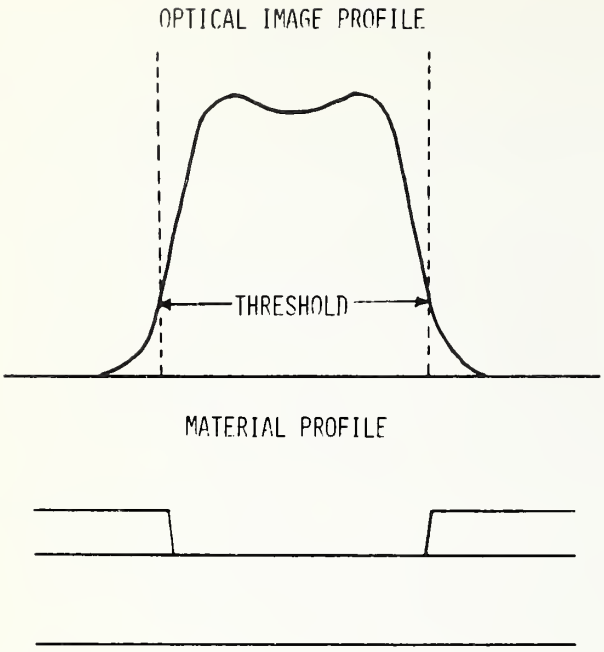
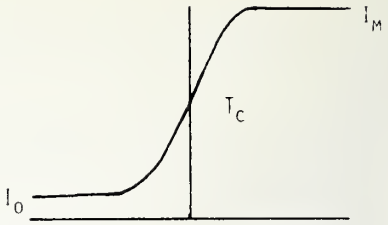
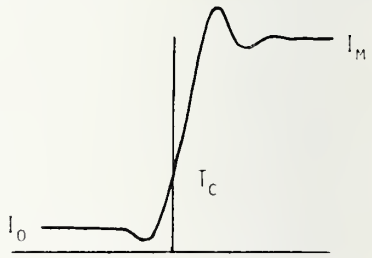


Figure 1. Schematic representation of the cross-sectional material profile of a transparent line in an opaque background and the corresponding optical image profile of a line scan from one side to the other. (After Nyyssonen [1])



a. Limit of incoherent illumination.



b. Limit of coherent illumination.

Figure 2. Line-edge image profiles for limiting conditions of microscope operation. (After Nyyssonen [1])

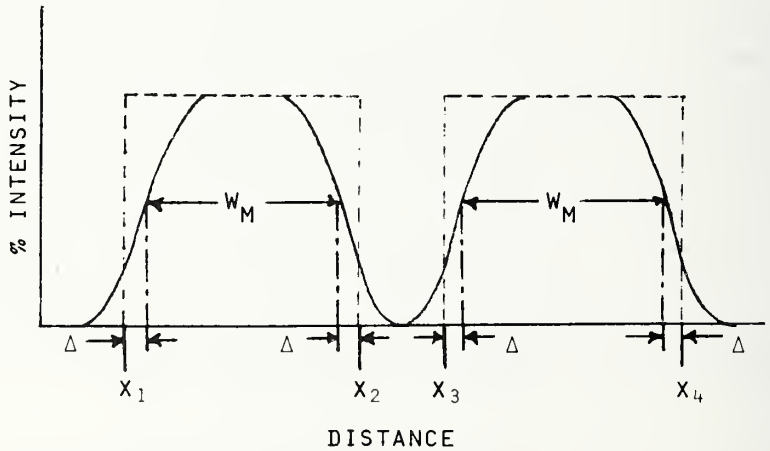


Figure 3. Optical image profiles (solid curves) of two adjacent ideal clear lines in an opaque field (dashed lines). The line spacing is $x_3 - x_1$ (or $x_4 - x_2$) and the width of the lines is $x_2 - x_1$ (or $x_4 - x_3$). The true threshhold is located a distance Δ (in a direction toward zero intensity) from the threshold assumed in making the measurement. (After Nyyssonen and Jerke [4])

summarize the present state of the art in selected metrology areas which bear on these requirements, and review current research and development efforts on advanced measurement technology for the semiconductor industry, with emphasis on efforts at the National Bureau of Standards. Techniques for a wide variety of dimensional measurements are considered in section 2. Materials characterization methods are reviewed in section 3. Several other types of measurements are mentioned briefly in section 4.

2. DIMENSIONAL METROLOGY

Dimensional measurements are, of course, critical for submicrometer technology. Both line-spacing and linewidth measurements are necessary to characterize circuit geometries and to quantify pattern registration, surface distortion, and surface stability. Dimensional measurements are also necessary to determine layer thicknesses, flatness and finish of surfaces, and characteristics of particulates on surfaces or in fluids. At the present time, techniques for these measurements on the micrometer and submicrometer scales are in an embryonic state.

Dimensional measurements on semiconductor device and integrated circuit patterns are generally carried out with the use of a measurement system based on an optical microscope. Measurements of this type require interpretation of an optical image of the line or space as shown schematically in figure 1 [1]. The threshold on the optical image profile is the value of transmittance or reflectance which corresponds to the actual material edge. This value depends on the nature of the particular optical system employed for the measurement. For example, the thresholds for abrupt edges viewed by incoherent and coherent illumination, shown in figure 2, are significantly different. In the limit of incoherent illumination, the threshold T_c is:

$$T_c = 0.5\ (I_O + I_M)\ ,$$

where the transmittance or reflectance is denoted as I_O on one side of the edge and as I_M on the other as shown in figure 2 [1]. In the limit of coherent illumination, the threshold is:

$$T_c = 0.25\ (I_O + I_M + 2\ \sqrt{I_O I_M}\ \cos\ \phi)\ ,$$

where ϕ is the optical phase difference between light rays passing through the materials on the two sides of the line edge. The degree of coherence of the illumination in an optical microscope can be varied by changing the ratio of the numerical apertures of the objective and condenser lenses [3].

For pitch, or line-spacing, measurements errors due to improper selection of threshold cancel so that accurate measurements between edges of the same type on features can be made without accurate knowledge of the actual threshold, but for width measurements such errors add rather than cancel. This is illustrated in figure 3 [4]. If the image profiles of the two lines are assumed identical, the measured distance between the thresholds assumed for the left-hand edges of the lines is given by:

$$P = (x_3 + \Delta) - (x_1 + \Delta) = x_3 - x_1\ ,$$

Table 1 — Results of Linewidth Measurements Made with a Variety of Optical Microscope Measurement Systems. (After Nyyssonen and Jerke [4])

Type of System	Linewidth (Micrometers) Spaces		Lines	
Photometric	0.98	3.13	0.87	2.87
Filar Eyepiece	1.05	3.17	0.73	2.68
Filar Eyepiece	1.44	3.71	0.66	2.78
TV Filar	0.85	3.05	1.14	3.00
Filar Eyepiece	1.12	3.36	0.71	2.71
Shearing Eyepiece	0.81	2.96	0.98	2.98
Filar Eyepiece	1.55	3.68	0.94	2.88
Filar Eyepiece	1.16	3.57	0.66	2.66
Shearing Eyepiece	0.73	2.82	1.04	3.05
TV-Image Scanning	0.85	2.93	1.06	2.83
Shearing Eyepiece	0.93	2.93	0.99	2.95
Photometric	1.00	3.10	0.75	2.80

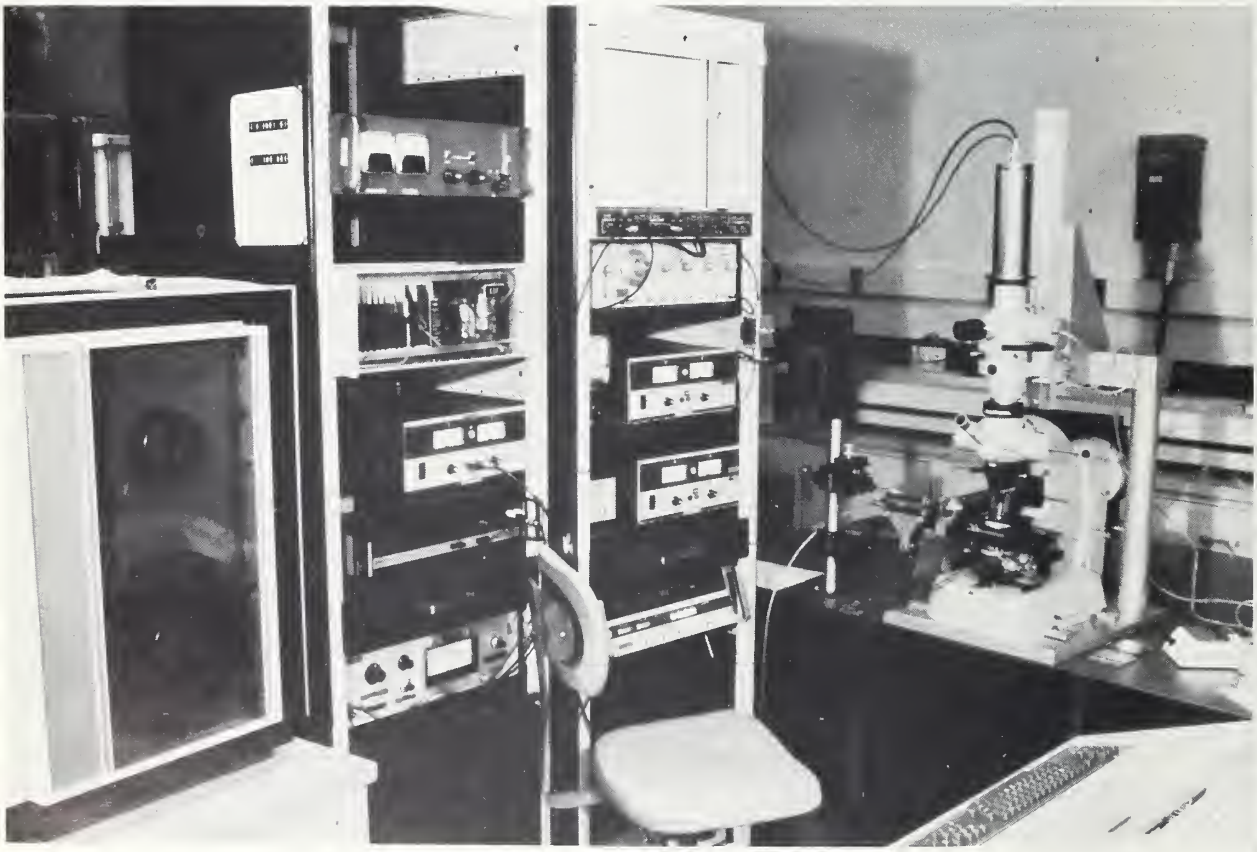


Figure 4. Scanning photometric microscope for measurements in transmitted light. (Photo by W. R. Smallwood)

where Δ is the distance between the assumed and actual thresholds as shown in the figure. The measured distance P is seen to be the true distance between similar points on the two lines. On the other hand, the measured width of the left hand line is given by:

$$W_M = (x_2 - \Delta) - (x_1 + \Delta) = x_2 - x_1 - 2\Delta \ .$$

The measured width differs from the true width by twice the distance between the assumed and actual thresholds. Therefore, for accurate measurements of feature widths, it is necessary to establish the correct threshold. Various microscope measurement systems, such as those equipped with filar, image shearing, or video eyepieces, have different edge detection thresholds [5,4]. It is well known that apparent differences of a quarter of a micrometer or more are observed when measuring widths, lines, or spaces with different systems [6]. Typical results of linewidth measurements made by a variety of optical systems on the same nominal 1- and 3-μm wide lines and spaces on antireflective-chromium photomask-like artifacts are listed in table 1 [4]. Each system was adjusted for pitch or line scale only.

Concern with such errors increased substantially about five years ago when it became apparent that feature sizes for integrated circuits would soon reach the submicrometer range [7]. Since that time, the problem of optical measurement of linewidths has been under investigation at NBS. Procedures have been established to permit measurements with an accuracy of about 50 nm on lines or spaces as narrow as 500 nm in thin layers (that is, layers less than 400 nm thick for measurements in transmitted light and layers less than 200 nm thick for measurements in reflected light) [3]. To do this the theory of the optical microscope was extended to take into account the spatial coherence of the illumination [3] and optical phase changes at material interfaces [8]. Experimental measurements were made on an automated scanning photometric microscope, pictured in figure 4. The numerical aperture of the objective lens is 0.9 and that of the condenser lens is 0.6 to provide effectively coherent illumination and to minimize flare light. For measurements in transmitted light, illumination is provided by a tungsten-halogen source, filtered to provide radiation sharply peaked at 530 nm.† In operation, the test object is moved so that the optical system is always used axially. The signal is detected with a photomultiplier through a narrow line slit with an effective width of 0.13 μm at the object plane. The microscope incorporates a novel piezoflex stage, developed at NBS, to provide smooth motion in the horizontal plane [9] and automatic piezo-controlled focusing to avoid dimensional changes in the image due to changes in lens-to-specimen distance. Comparisons between experimental measurements of the image edge profiles and the calculated profiles show extremely good agreement as can be seen by the example in figure 5 [8]. To make such comparisons, the experimental profile (solid line) and calculated profile (open circles) are simply superimposed by matching at the threshold. In this example, I_o is taken as 0.01 and ϕ is taken as 90 deg.

Procedures have been worked out for measurement of linewidths in these ranges with the use of many of the types of linewidth measuring systems available in the field. To facilitate calibration of these instruments, NBS plans to issue

† A 0.5-W krypton laser source and a somewhat more sensitive photomultiplier-detector system are required for measurements in reflected light [8].

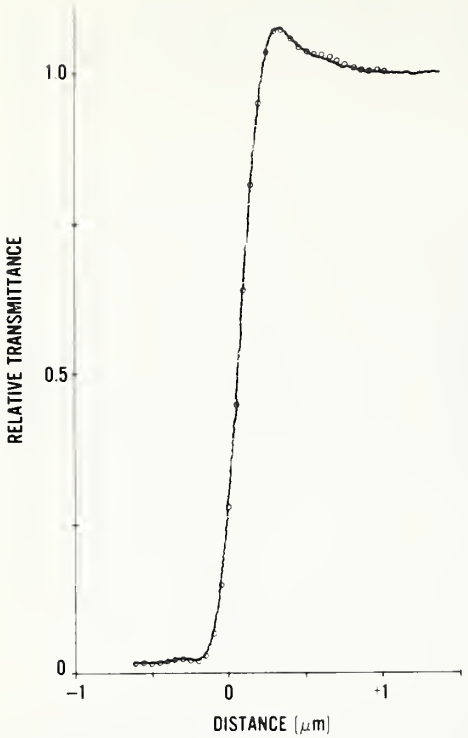


Figure 5. Comparison of experimental (solid curve) and calculated (open circles) edge profiles for antireflecting chromium on glass. (After Nyyssonen [8])

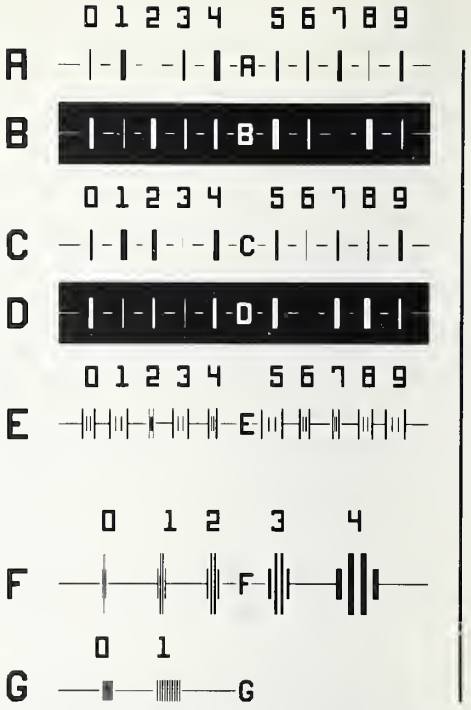


Figure 6. Patterns for linewidth and associated measurements on an artifact designed for use in evaluating and calibrating linewidth measurement systems.

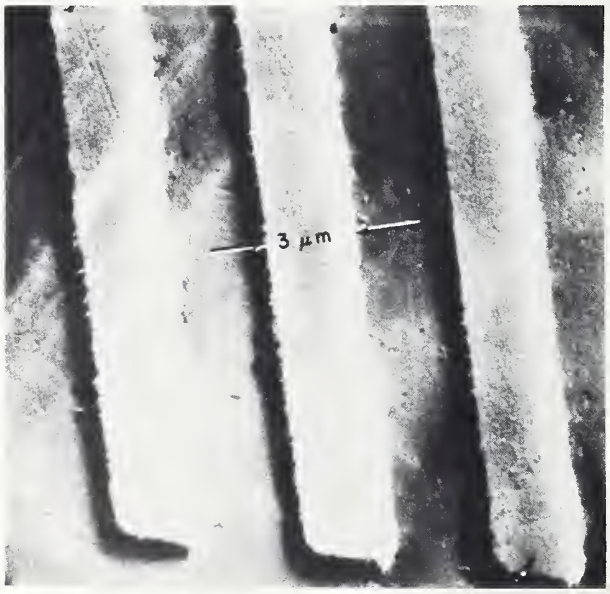


Figure 7. Scanning electron micrograph of three nominally 3-μm wide antireflecting chromium lines on a glass substrate. (Micrograph by W. J. Keery)

as standard reference materials a series of artifacts which contain a variety of patterns as shown in figure 6. Four sets of lines and spaces in the 0.5- to 10-μm range (rows A-D) comprise the basic patterns [10]. Other patterns are included to permit line-spacing calibrations (row E), setting of edge detection thresholds and line-to-space ratios on automatic measuring instruments (row F), and testing for lead screw errors (row G). Each artifact contains 8 such patterns, one of which is calibrated and certified by NBS. The first of these artifacts, which is fabricated in an antireflecting chromium film on a glass substrate, is designed for use in measuring opaque photomasks in transmitted illumination. Together with the associated measurement procedures [11], this artifact provides the user with the capability of evaluating his own measurement procedures and calibrating his measuring instrument.

At the present time, the principal limitation on the accuracy of linewidth measurements is the shape and uniformity of the material edge being measured; the measurement technique must be extended to account for both the slope and waviness of the edge which are evident in the scanning electron micrograph in figure 7. In addition, the theory must be extended to permit accurate measurements of lines and spaces in thicker layers. Both these extensions are essential for measurements on very large scale integrated circuit wafers or chips.

Optical techniques are not suitable for measurement of the widths of lines or spaces less than about 500 nm wide. For such features an electron probe must be employed. In making the electron-probe measurements, it is also necessary to consider the characteristics of the material edge profile. Preliminary comparisons between electron probe and optical measurements of widths of lines in the 1- to 10-μm range have yielded generally satisfactory results for opaque lines in a clear field, but not for clear lines in an opaque field [12]. These preliminary electron probe measurements were made with a conventional scanning electron microscope adapted for the purpose; a first-order model of the edge profile was used to interpret the results. Additional work to address the difficulties encountered with the clear lines is now being carried out at NBS. A specially designed electron microscope designated the microlength calibrating electron probe (MCEP), with integral polarization interferometer [13], is being used for the electron-probe measurements, and more sophisticated edge profile models are being developed.

Line-spacing determinations, as noted earlier, are somewhat less demanding; calibrations down to about a micrometer can presently be performed by NBS on suitable artifacts supplied by the user [14]. Nevertheless, calibrations of line spacings in the submicrometer range will probably require the use of an electron probe such as the MCEP.

Line-spacing measurements can be used to establish registration of patterns and distortion characteristics of substrate surfaces. It is projected that pattern registration will be required to an accuracy of less than 10 nm. Measurements to such an accuracy over distances of 1 cm or more are presently not practical. Among the critical factors are the maintenance of smooth translation of the test specimen and retention of focus of the measuring probe. This latter factor requires control of the lens-to-specimen spacing in the submicrometer range. An advanced class of high quality x-y stages which will achieve these characteristics over translational motions of 1 cm

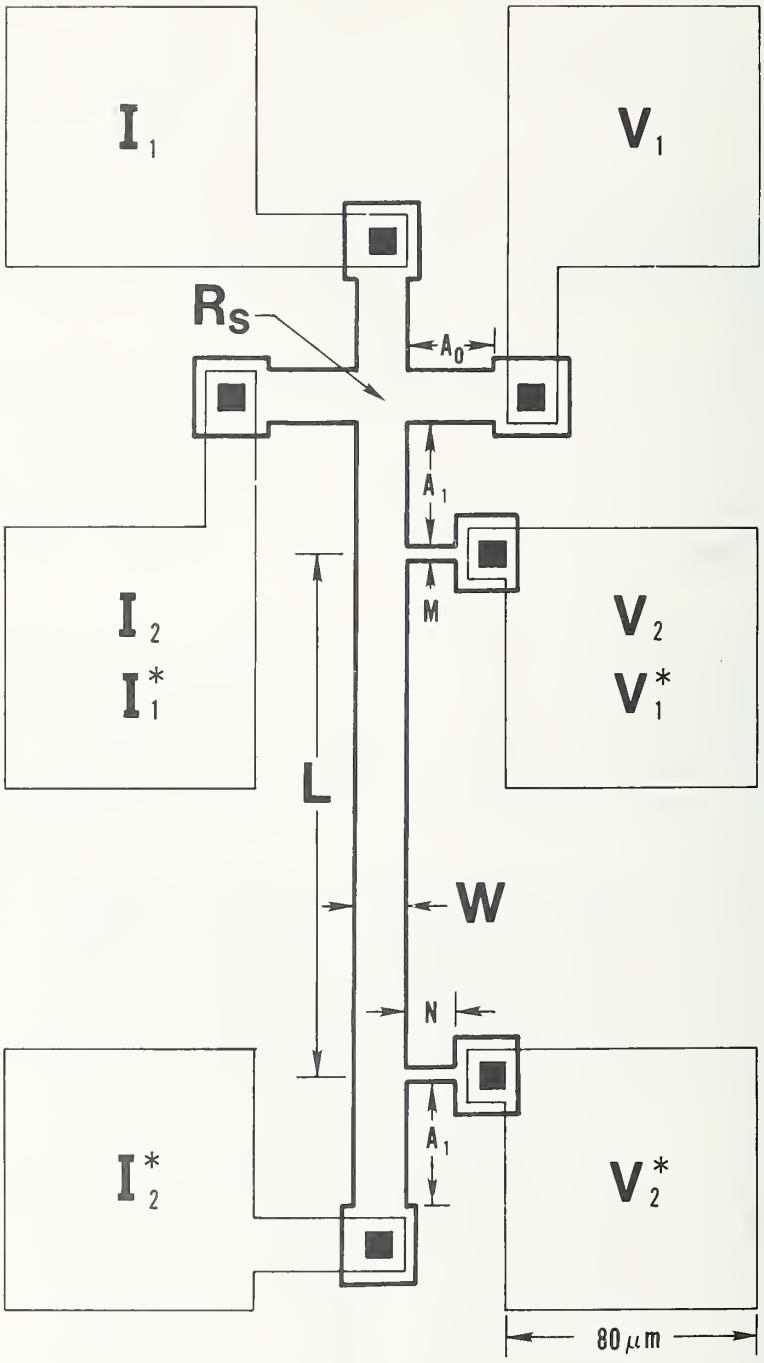


Figure 8. Outline drawing of a three-level cross-bridge sheet-resistor test structure. The three levels shown are channel (heavy outline), contact window (solid), and metal (light outline). A single-level cross-bridge can also be fabricated in metal; in this form the channel and metal levels are combined and the contact window level is omitted. (After Carver *et al.* [15])

and more is currently under development at NBS in connection with studies of surface topography. Such stages will be very important in the extension of optical techniques for measurement of line spacings to determine pattern registration and surface distortion.

Microelectronic test structures, suitably replicated across the surface of a wafer, permit the measurement of geometrical quantities electrically. Microelectronic test structures are device-like structures fabricated in the same way as integrated circuits. Two major types of microelectronic test structures are of interest for dimensional measurements. The cross-bridge test structure is used to determine the width and sheet resistance of conducting regions [15]. One form of this structure is depicted in figure 8.* Analysis has shown that the cross-type sheet resistor is a symmetrical van der Pauw structure which yields a value of sheet resistance $R_s(VDP)$ which is independent of the structure size [16]:

$$R_s(VDP) = \frac{\pi}{\ln R} \frac{\Delta V}{I} ,$$

where I is the current passed from contact I_1 to contact I_2 and ΔV is the potential difference between contacts V_1 and V_2. Ideally, the effective width of the bridge region, W, is given by the product of the design distance between potential contacts on the bridge portion of the structure, L, and the ratio of the sheet resistance as measured by the cross portion of the structure to the sheet resistance as measured by the bridge portion [17]:

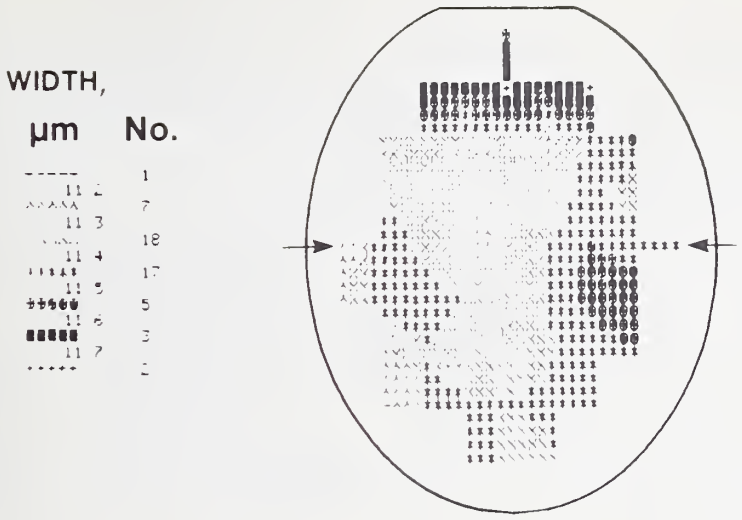
$$W = R_s(VDP) L \frac{I^*}{\Delta V^*} ,$$

where I^* is the current passed from contact I_1^* to contact I_2^* and ΔV^* is the potential difference between contacts V_1^* and V_2^*. Measurements of W can be made with a resolution of about 10 nm.

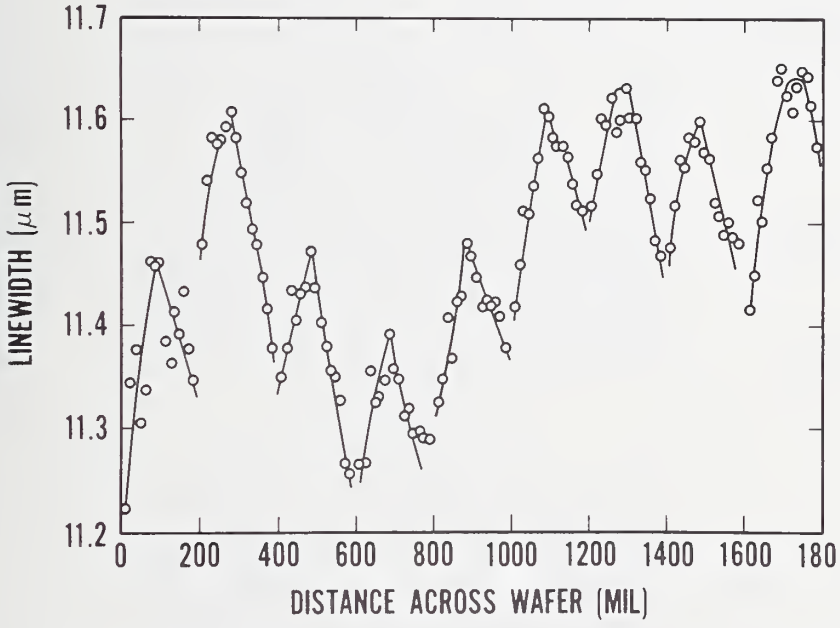
If cross-bridge structures are replicated across the entire wafer, it is possible to make a map of the linewidth variations. For example, test pattern NBS-21 is a single-level pattern formed in the metal over an oxide by repeating the 5- by 5-mm cell shown in figure 9 [18]. The upper map in figure 10 shows the width of the lower-left structure in each cell. Denser symbols represent wider values of linewidth. It can be seen that the width variation is somewhat random in nature. The program which generated this wafer map was designed to interpolate between actual data points which appear at every fourth symbol [19]. Consequently, the fine structure within the cell cannot be observed on the map. When data from all the structures in a given row are plotted as in the lower chart of the figure, it can be seen that there is a variation in linewidth that is periodic with the cell dimension in addition to random variations. The periodic variation can be attributed to the system used to fabricate the photomask; variations from cell to cell in the linewidth at a given point in the cell matrix can be attributed to the photolithography asso-

* Other forms of this structure have been reported in the literature; see, for example, Wahl, F. E., and Perloff, D. S., Techniques for the Evaluation and Display of VLSI Process Uniformity, *Proc. Microelectronics Measurement Technology Seminar*, San Jose, California, February 6-7, 1979, pp. 17-26.

Figure 9. One cell of test pattern NBS-21, an 8 by 15 array of single-level cross-bridge sheet-resistor test structures. (After Linholm [18])



a. Wafer map of the linewidth of the lower left structure in each cell. The number of structures in each width interval is shown in the table at the left.



b. Linewidth of the structures along one line (denoted by arrows in a) of test pattern NBS-21 as a function of position on the wafer.

Figure 10. Linewidth variation determined with test pattern NBS-21. (After Linholm and Buehler [20])

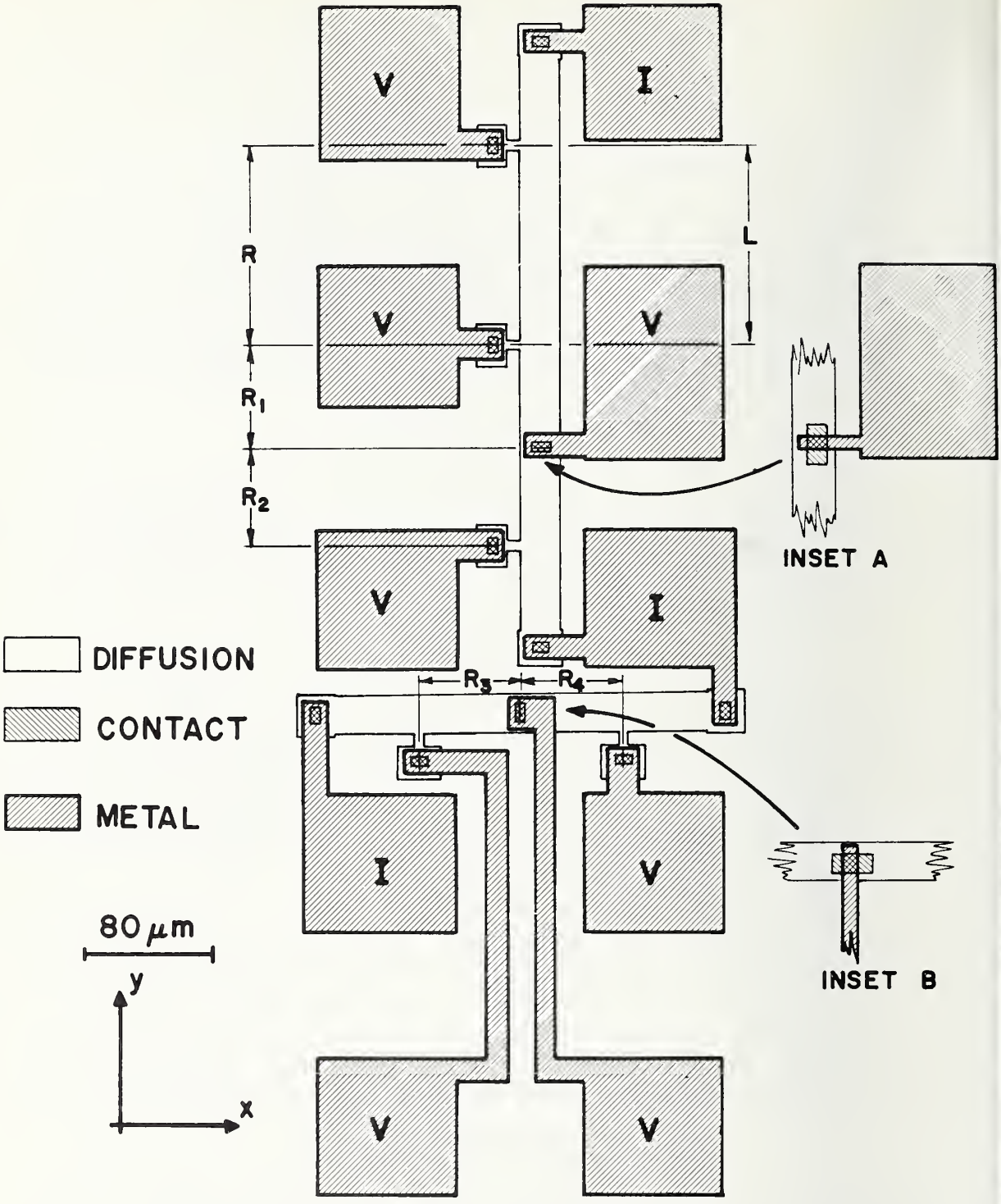


Figure 11. Outline drawing of three-level production-compatible electrical alignment test structure. The form shown in the main drawing is for use in determining alignment between the diffusion (channel) and contact window levels; the modifications shown in the insets are made to allow determination of the alignment between the diffusion and metal levels. (After Russell *et al.* [21])

ciated with printing the pattern, to variations in etching the pattern, or to both [18,20].

The production-compatible electrical alignment test structure* shown in figure 11 provides a means for direct electrical determination of the alignment between the channel (diffusion) and contact-window mask levels (main drawing) or between the channel and metal levels (insets) [21,22]. When there is perfect alignment between the two mask levels, resistance R_1 is equal to resistance R_2 and resistance R_3 is equal to resistance R_4. Misplacements of the upper level with respect to the lower in the x- and y-directions are given by

$$\Delta L_x = \frac{L}{2} \frac{R_3 - R_4}{R}$$

and

$$\Delta L_y = \frac{L}{2} \frac{R_2 - R_1}{R} ,$$

where resistance R and the length L are defined in figure 11. When fabricated into a test pattern with 6-μm minimum-linewidth design rules, this structure can resolve misregistration of the order of 100 nm. If the structure is replicated across the wafer, it is possible to make complete wafer maps of the misalignment as illustrated in figure 12. In these maps, the length of the vector indicates the displacement; the distance scale is given at the bottom. Under ideal conditions, these maps can be analyzed to extract the translational, rotational, and radial components [23], leaving a residual which may result from process-induced wafer distortion, from variations in the test structure, or from both.

Both the cross-bridge and electrical alignment test structures are potentiometric in nature. In order to provide accurate results, these structures must be fabricated in layers with uniform resistivity, and the active regions must have uniform cross sections. Deviation from these conditions, asymmetries in the voltage-tap geometry (as shown in the photomicrograph of figure 13), and

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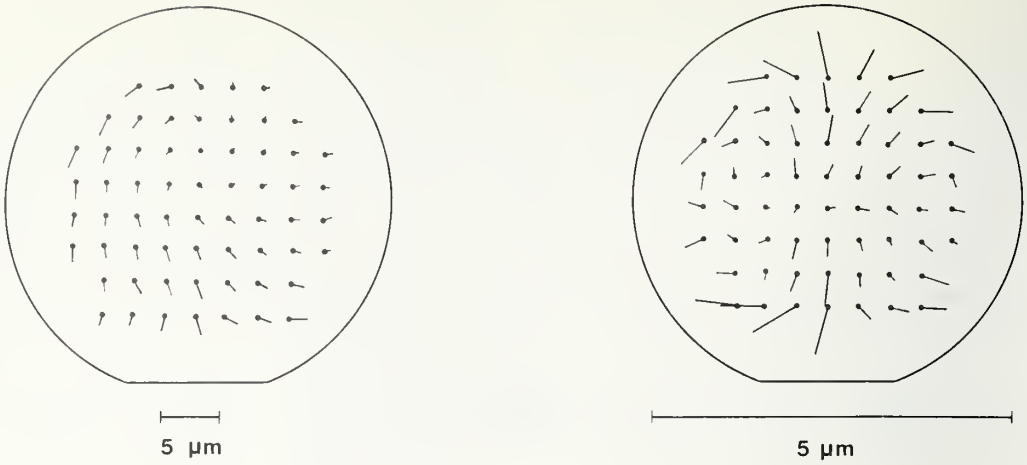
* This style of production-compatible electrical alignment test structure is patterned after that reported by Thomas, D. R., and Pearson, R. D., [An Electrical Photolithographic Alignment Monitor, *Digest of Papers, Govt. Microcircuit Applications Conf.*, Orlando, Florida, November 1974, pp. 196-197.] Another style of production-compatible electrical alignment test structure has been reported by Stemp, I. J., Nicholas, K. H., and Brockman, H. E. [Automatic Measurement and Analysis of Misalignments in Integrated Circuit Processing, *Proc. Conf. Microcircuit Engineering '78*, Cambridge (1978)] and by Wahl, F. E., and Perloff, D. S. [*loc. cit.*] Perloff has described a single-mask electrical alignment tester intended primarily for evaluation of mask aligners and projection printers [A van der Pauw Resistor Structure for Determining Mask Superposition Errors in Semiconductor Wafers, *Solid-State Electronics* 21, 1013-1018 (1978)]. In utilizing a production-compatible electrical alignment test structure similar to the one pictured in figure 11, Perloff adds a second sheet resistor perpendicular to the first to account for the possibility that the width of the potentiometer bars may depend on direction [Wahl, F. E., and Perloff, D. S., *loc. cit.*].



a. Original data (Device 15.1, Wafer 17).

b. Residual displacements after removal of translational and rotational components.

Figure 12. Vector maps of contact-window-to-channel alignment at 62 sites on a 2-in. diameter silicon wafer. The position of the dot represents the location of the test structure on the wafer, and the length and direction of the line correspond to the length (as given by the dimensional scale below the map) and direction of the displacement. (After Carver *et al.* [15])

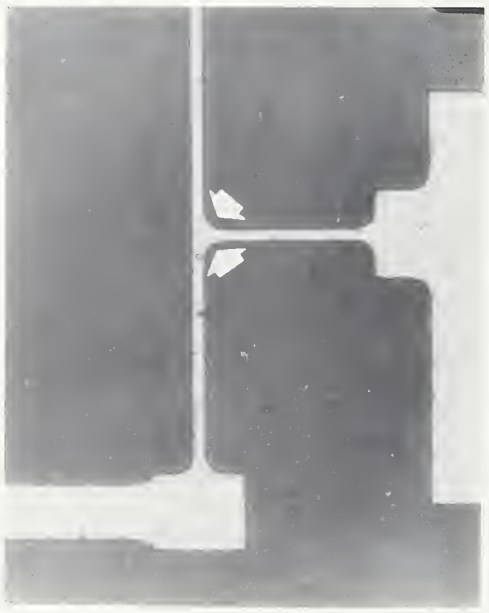


Figure 13. Photomicrograph of a portion of a 2-μm wide single-level, cross-bridge sheet-resistor test structure fabricated in aluminum on an oxidized silicon substrate showing asymmetries in the voltage-tap geometry (arrows). (Photomicrograph by T. J. Russell and W. J. Keery)

any source of distortion in the current lines (which may be caused, for example, by shunting at the voltage taps or crowding at the current contacts) are all potential sources of error in these measurements. While these error sources do not appear to be very serious for structures fabricated in geometries of 6-μm or larger, they are expected to become quite significant for structures fabricated with micrometer and submicrometer geometries.

Another dimension which must be controlled carefully is the thickness of various films and layers which comprise a microstructure. Control of the thickness of oxide or other insulator films is particularly critical for submicrometer devices. For example, for MOS integrated circuits, it is expected that gate oxides will be the order of 50 nm thick with a uniformity and accuracy requirement of about 1%. At the present time, there are no standards for film thickness or step height when either quantity is required to have a value in the range between 10 and 1000 nm. NBS does offer a limited step-height calibration service based on stylus profilometry [24]; present measurement uncertainty is as high as 20% for thicknesses of about 50 nm. During 1980, NBS is planning to issue a standard reference material for oxide-film thickness measurements by ellipsometry. This standard will consist of a thermally oxidized silicon wafer; the oxide thickness will be between 50 and 100 nm. Although a reproducibility of 1 to 2% is expected for ellipsometry measurements on these standards, there is no assurance that the ellipsometric values will agree with values obtained by stylus profilometry. In fact, one of the major reasons for the large uncertainty in thickness calibrations is the disagreement between values deduced from the three commonly used measurement techniques: stylus profilometry, ellipsometry, and interferometry. Because these differences exceed the resolution capabilities of each of the techniques, they are usually attributed to test specimen characteristics (such as design, uniformity, and stability), to inadequate models of the measurement techniques, and to differences in the material parameters to which the individual measurement techniques respond. Intercomparison of these three thickness measurement techniques on the scale appropriate for microstructures would be a major research project.

Stylus techniques and interferometry are also utilized in measurements of surface finish and flatness. In addition, light scattering techniques are also employed. A principal problem in connection with stylus measurements of surface topography is the smoothness and planarity of the stage which moves either the specimen or the stylus. The previously mentioned high-quality x-y stages are essential if stylus techniques are to be utilized to determine surface topography in regimes appropriate for microstructures.

The final dimensional measurement area to be considered relates to particulates which may appear in fluids or on surfaces. Both light scattering and microscopical techniques are utilized in sizing and counting such particles. Standard procedures do not exist for sizing particles smaller than 5 μm. Sizing and counting particles smaller than 10 to 25 μm remains more an art than a science. Comparisons between various techniques are being made by Subcommittee 10 (Process Chemicals) of ASTM Committee F-1 on Electronics with increasing success. Work on particulates was also undertaken in the fall of 1979 by a subcommittee (Testing of Process Chemicals for Semiconductor Technology) of DIN Committee NMP 221 on Testing of Materials for Semiconductor Technology. Extension of these various techniques to the submicrome-

Table 2 — Selected Properties of Single-Crystal Silicon. (After ref. [32])

Property	Current Capabilities		Requirements for VLSI
	Czochralski	Float Zoned	
Resistivity n-type (P), Ω·cm	1-40	1-300	100-400
Resistivity n-type (Sb), Ω·cm	0.005-10		0.0002-0.02
Resistivity p-type (B), Ω·cm	0.005-50	1-300	100-400
Resistivity gradient (four-probe) %	5-10	20	<1
Resistivity microsegregation, %	10-15	20-50	<1
Minority carrier lifetime, μs	30-300	50-500	300-1000
Oxygen, ppma	5-15	Not detected	Uniform and controlled
Carbon, ppma	1-5	0.1-1	0.1
Heavy-metal impurities, ppba	1	0.01	0.001

Figure 14. A TO-100 header with attached test chip (quadrant 1 of test pattern NBS-3) on the left [A] and temperature-sensing diode on the right [B]. The devices are mounted to gold-plated regions on a thin sapphire slab to provide thermal contact but electrical isolation.

ter regime, essential for controlling particulate contamination in the fabrication of microstructures, is a major undertaking which has not yet been adequately addressed. The NBS Center for Mechanical Engineering and Process Technology has undertaken a basic research effort in wave optics which responds to a portion of the problem. Among the results expected from this long range project is extension of the theoretical basis for scattering of light by particles and fibers to the regime where the size of the scatterer is near the wavelength of light.

3. MATERIALS CHARACTERIZATION

A wide range of techniques is available for characterizing the physical, electrical, and optical properties of semiconducting and other electronic materials. The available techniques have been summarized briefly in a number of recent reviews [25-30]. Standard test procedures for many techniques are under development both in Germany (by DIN Committee NMP 221) and in the United States (by ASTM Committee F-1) [31].

Semiconductor characterization for microstructures is made more difficult by the greater demands for control and uniformity of the chemical and defect properties of the materials, by the necessity for analyzing for distributions of dopant and trace impurities in ever smaller volumes, and by the necessity for characterizing interfacial and surface regions. The present state of the art of characterization techniques with respect to their application to characterization of microstructures has been recently considered in some detail by the Panel on Thin Film Microstructure Science and Technology of the Solid State Sciences Committee of the National Academy of Sciences [32]. As an example of the problems encountered, consider some of the projected requirements for single crystal silicon substrates to be used in very large scale integrated circuits listed in table 2, extracted from the Panel's report.

The demonstrated reproducibility of the four-probe method for measuring resistivity in the 100 to 400 $\Omega \cdot$cm range is $\pm$5% [33], much larger than the 1% uniformity required on both macro and micro scales. The situation is not as bleak as it might appear at first glance however, because the large scatter obtained in the interlaboratory comparative experiments is attributable partly to nonuniformities in the test specimens; reproducibility of $\pm$2% was obtained on homogeneous specimens of lower resisitivity.

The control of both oxygen and carbon impurities in the silicon crystal appears to be essential. Fully satisfactory methods to test for these impurities are not yet available; much greater understanding of the nature of these impurities in the silicon lattice will be required before satisfactory methods can be developed.

Reduction of heavy metal contamination is necessary to achieve the high lifetimes required. Deep level transient spectroscopy and other deep level measurement techniques are widely used in detecting heavy metal impurities [34]. Use of these techniques requires formation of a junction diode or MOS capacitor such as those in the first quadrant of test pattern NBS-3 [35] shown mounted on the header in figure 14. Generally the measurements are made on devices individually packaged together with a temperature sensor, such as the small silicon diode shown mounted on the header to the right of the test

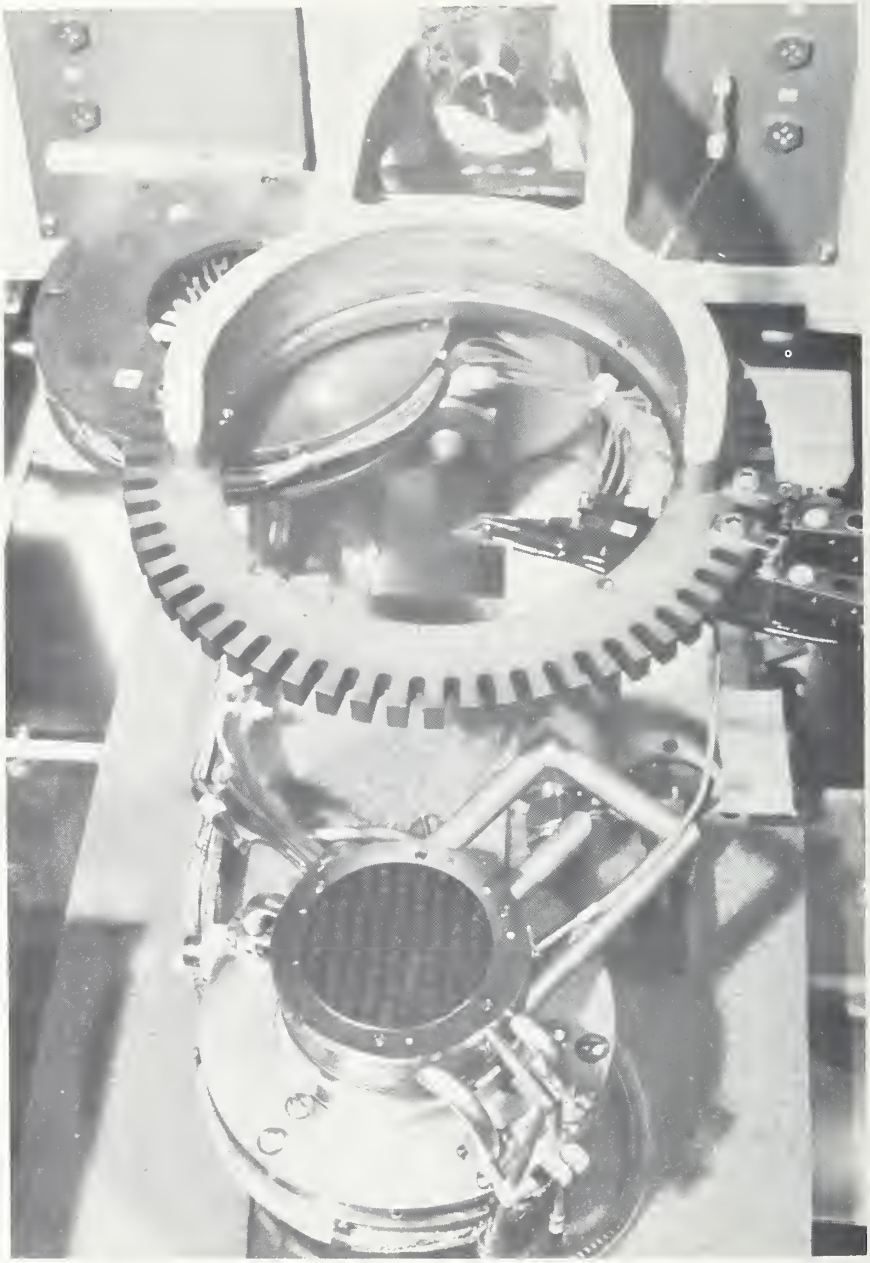


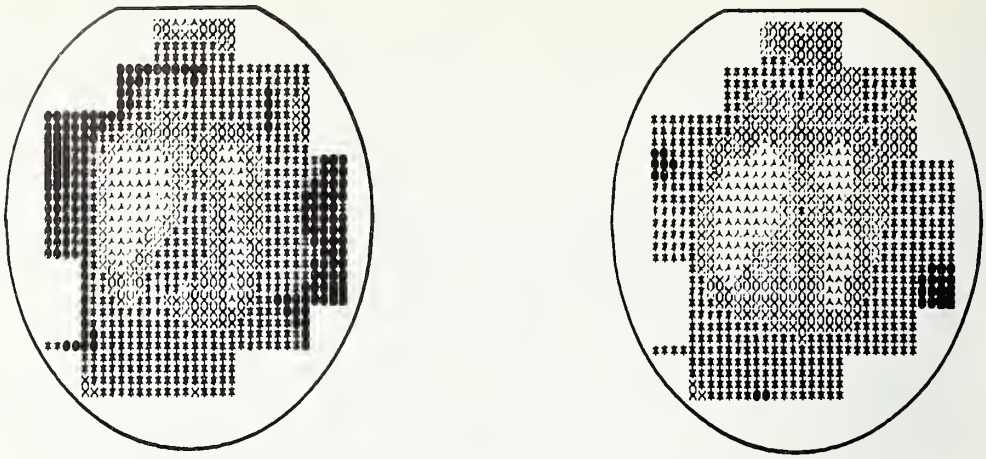
Figure 15. Photograph of 2-in. diameter silicon wafer mounted in variable temperature prober.

chip, which adds time and complexity to the specimen preparation. NBS has developed a variable temperature wafer prober pictured in figure 15 for use in making deep level measurements on unscribed wafers [36]. With this instrument, it is possible to make wafer maps of the density of the deep level impurities and to compare the density distribution with maps of other parameters such as leakage current or carrier lifetime [37]. Typical maps [19] are reproduced in figure 16. NBS has also undertaken to conduct an informal interlaboratory comparison of various deep level measurement techniques. In this comparative study, two well-characterized gold-doped silicon gated diodes are being circulated among interested participating laboratories.

Although electrical measurements, such as Hall effect or transient capacitance measurements, can in special cases provide information about the identity of certain impurities in semiconductors, physical analysis techniques are generally recognized as being required for adequate identification of impurities. Generally speaking, the sensitivity of the various beam techniques is reduced as the sampling area is decreased as shown in figure 17, also taken from the report of the Microstructures Panel [38]. No techniques are available which have part-per-million atomic sensitivities in sampling areas of the order of 1 μm or less in diameter. Development of standards and interlaboratory comparisons to provide estimates of the reproducibility of these techniques in their conventional ranges are only just getting underway in ASTM Committee E-42 on Surface Analysis. An indication of the current state of the art is provided by the results of a preliminary study of the ion microprobe mass analysis (IMMA) technique recently carried out for NBS. These results suggest that the repeatability of this technique when measuring phosphorus implants in silicon over a period of about a week is the order of 10% [39]. This variation may also be due principally to microinhomogeneities in the material as noted earlier in regard to resistivity measurements.

Although these techniques, with the exception of IMMA (or secondary ion mass spectrometry, SIMS), are not well suited to profiling impurities in semiconductors, they have proved extremely valuable in compositional studies of interfaces. For example, through very careful analysis of Auger electron spectroscopy (AES), taking into account electron escape depth, ion beam mixing, and electron stimulated desorption considerations, the Electron Spectroscopy Group at Stanford has developed the model for the silicon/silicon dioxide interface shown in figure 18 [40]. These experiments also took advantage of the fact that AES can provide information on the chemical state of certain species. Additional information on the chemical state is available from x-ray photoelectron spectroscopy. Results of such measurements demonstrate that the transition region between silicon and silicon dioxide which contains partial oxides of silicon is very narrow [41].

Microelectronic test structures can also be used to determine material characteristics. Some years ago Krausse used a matrix array of aluminum contacts to determine the resistivity uniformity of a wafer by spreading resistance measurements [42]. Bulk resistivity can be measured with the use of the planar four-probe square array shown in figure 19 [43]. The use of junction diodes and MOS capacitors for making deep level measurements has already been mentioned; these structures can also be used to determine dopant profiles from incremental capacitance-voltage (C-V) measurements, usually at 1 MHz [44]. Dopant-profile measurements can be made by dc techniques if a four-



(a) (b)

Figure 16. Wafer maps of gold acceptor density (a) and diode junction leakage current (b) showing correlation between these quantities. The maps show five equal ranges; the darkest symbol denotes the highest range. The gold acceptor density varies from 1.9 to 7.6 x 10^{13} cm^{-3}, and the leakage current varies from 0.26 to 1.05 nA. (After Koyama [37])

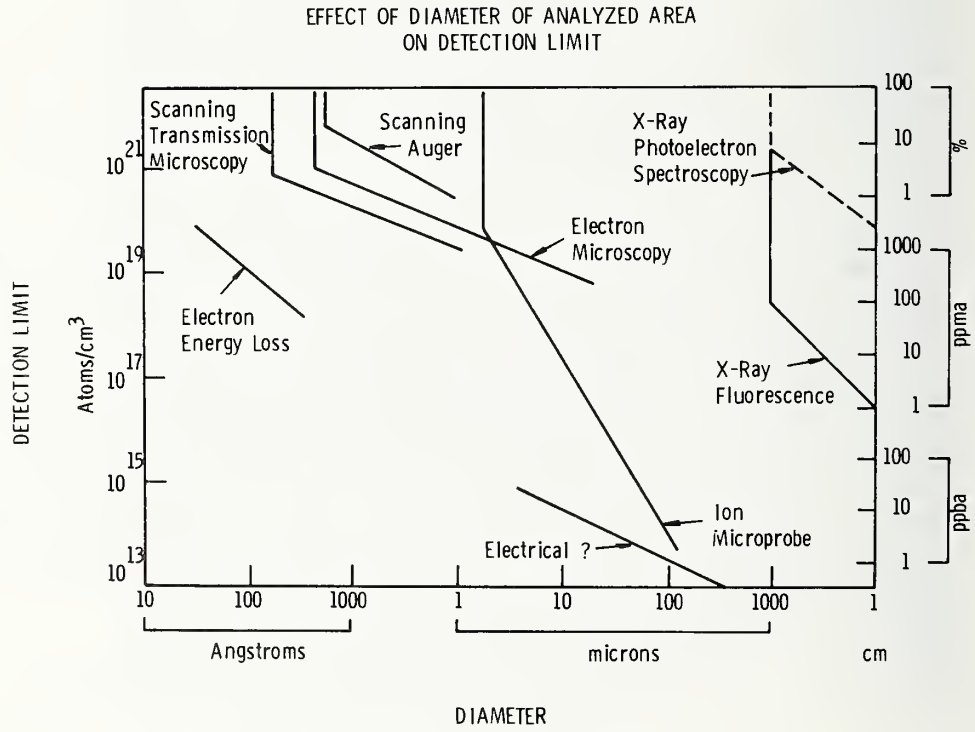


Figure 17. Effect of diameter of analyzed area on detection limit of various analytical methods. (After Larrabee [38], courtesy of Texas Instruments Incorporated)

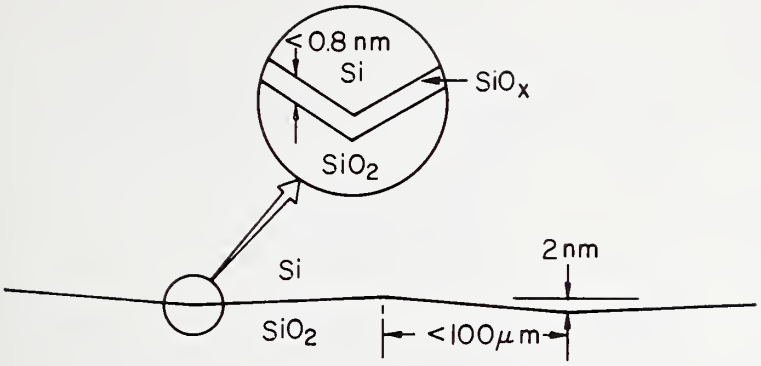
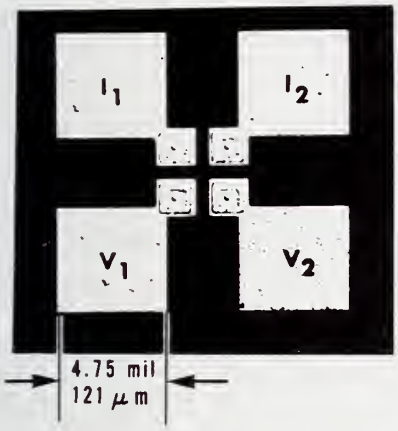
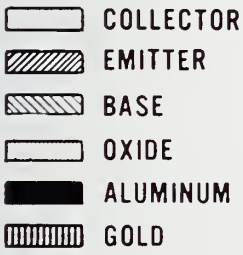


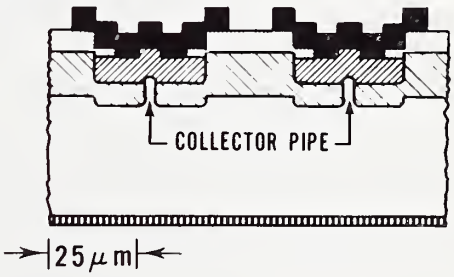
Figure 18. Model of the Si-SiO_2 interface on thermally oxidized silicon wafers as derived from sputter Auger studies. (After Helms *et al.* [40])



a. Photomicrograph of overall structure including probe pads.

b. Detail of one of the four contact region.





c. Schematic cross section of the planar square array four-probe resistor test structure (scaled in horizontal direction only).

Figure 19. Planar four-probe test structure for measurement of bulk resistivity. (After Buehler and Thurber [43])

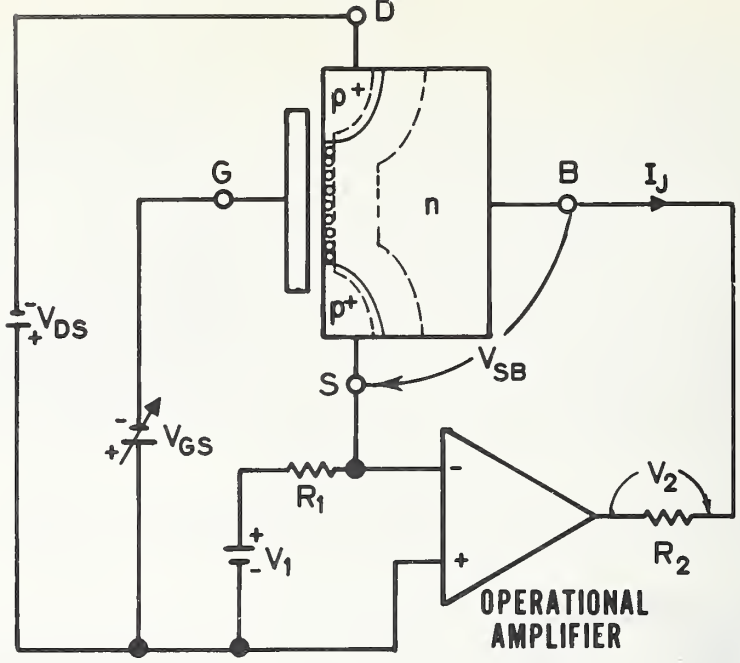


Figure 20. Circuit for obtaining the dopant profile in the gate region of a p-channel enhancement-mode MOSFET. (After Buehler [45])

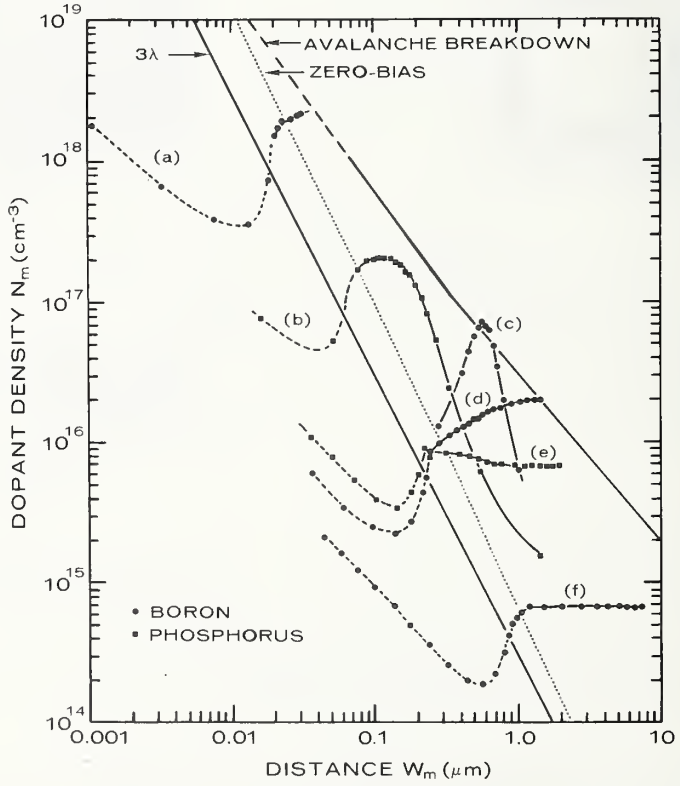


Figure 21. Dopant profiles of boron diffusion (a), phosphorus implant (b), boron implant (c), boron-doped bulk (d) and (f), and phosphorus-doped bulk (e). The dips in the profiles to the left of the 3λ line are artifacts of the measurement; dopant density values measured in this region do not represent the true profile. (After Buehler [46])

terminal enhancement-mode MOSFET is employed [45,46]. This structure and its associated test circuit are shown in figure 20. The device is operated in the linear current region. Ideally, both the depletion width and the dopant density can be obtained from high-speed dc measurements made on a conventional wafer prober. As the gate-source voltage V_{GS} is changed, the source-drain current is held constant by adjusting the source-body voltage V_{SB}. The depletion width is given by:

$$W_m = \frac{\varepsilon_s}{\varepsilon_o} X_o \frac{dV_{SB}}{dV_{GS}} ,$$

and the dopant density at this position is given by:

$$N_m (W_m) = \frac{\varepsilon_o^2}{q \varepsilon_s X_o^2} \left(\frac{d^2 V_{SB}}{dV_{GS}^2} \right)^{-1} ,$$

where ε_s and ε_o are the dielectric constants of silicon and silicon dioxide, respectively, X_o is the oxide thickness, and q is the electronic charge. Figure 21 shows a selection of profile measurements made with the MOSFET profiler. Like the rf (CV) method, this method cannot provide information at depths beyond the depletion depth associated with voltage breakdown in the silicon or for distances between the surface (or the junction) and the zero-bias depletion depth. The latter limitation may limit application of these techniques for measurement of dopant profiles in very thin layers as might be found in many submicrometer devices.

The gated diode is a powerful tool for determining the magnitude and origin of leakage currents [47]. As shown in figure 22, the device is sensitive to currents in various portions of microelectronic device structures, depending on the gate voltage. Because of the difficulty of measuring the very small currents in the very high impedance reverse-biased diode, this device has not been widely utilized. However, by adding integral circuitry, including a MOSFET source-follower output amplifier as shown in figure 23, the measurements can be made rapidly with ordinary dc wafer-probing equipment [48,49]. An example of such measurements is the wafer map of generation lifetime shown in figure 24; here the denser symbols relate to shorter lifetimes. It must be emphasized that careful design and accurate modeling are required to insure that the integrated test structure is measuring the desired quantities and is not dominated by parasitics [50]. Also, it should be observed that reducing critical dimensions of either integrated or discrete test structures to submicrometer dimensions requires design and modeling efforts very similar to those employed in making submicrometer integrated circuits.

The reduction in lateral dimensions is generally accompanied by some reduction of the vertical dimension which adds to metrological difficulties. For example, semiconducting layers become fully depleted at very small voltages, which complicates the interpretation of electrical measurements as alluded to previously. Hot-carrier effects, which are encountered because of the very large electric fields which appear across thin insulating and depleted semiconducting layers, must also be taken into account in interpreting electrical measurements. The interpretation of beam analysis methods is also complicated when measurements are made in very thin layers. For example, ion beam

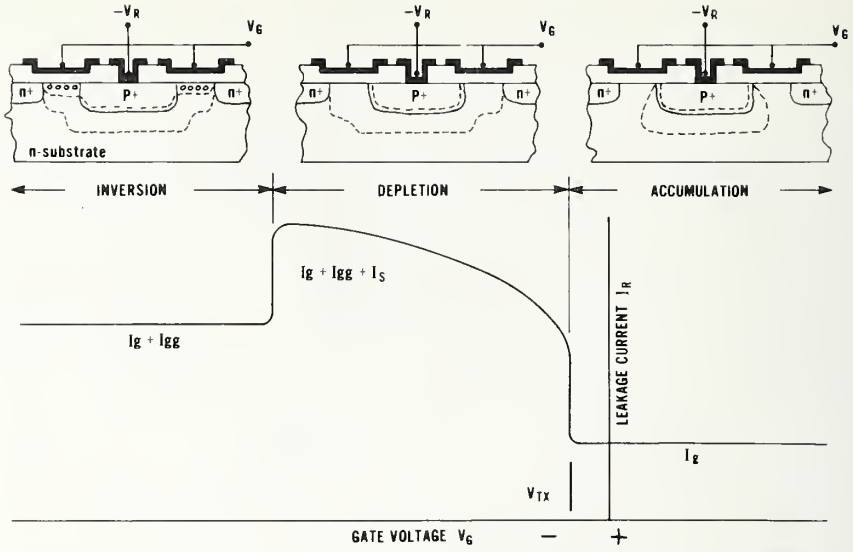


Figure 22. Idealized curve of leakage current I_R of a p^+n gated diode at a fixed value of reverse bias V_R as a function of gate voltage V_G. The dashed curves in the insets at the top schematically illustrate the spatial extent of the depletion region. The current components are I_g, the generation current in the depletion region under the metallurgical junction; I_s, the surface current generated by interface states under the gate; and I_{gg}, the generation current in the depletion region under the gate. The voltage V_{TX} is the extrapolated threshold voltage. (After Carver and Buehler [49])

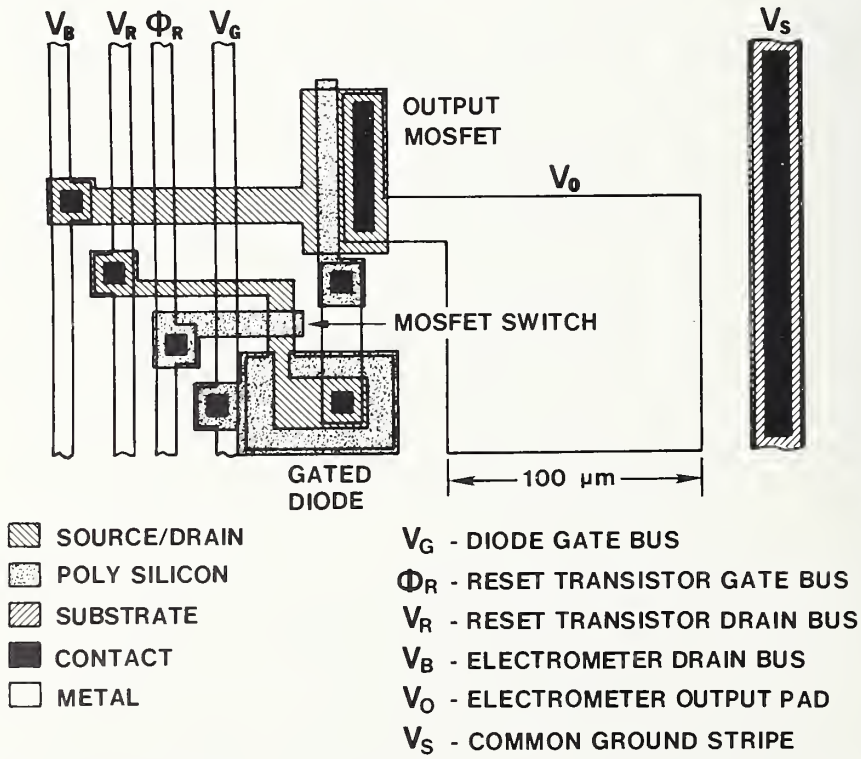


Figure 23. Outline drawing of integrated gated-diode test structure with output MOSFET electrometer and MOSFET reset switch.

mixing effects are observed as deep as 3 nm below the surface when sputter profile measurements are made with a 1-keV ion beam [51]. The mixing depth for the higher energy ion beam used for ion microprobe mass analysis is substantially larger.

Many of the techniques used to fabricate microstructures involve substantial amounts of ionizing radiation. Calculations have been made of the dose deposited in oxide layers by several processing steps [52,53]. For example, figure 25 shows the dose deposited during typical exposure during direct-write electron-beam lithography. This radiation can introduce neutral traps into the oxide [54]. Temperatures higher than 550°C are required to anneal out these traps; those which remain may later cause device failure. Because the commonly employed threshold-voltage-shift tests do not detect neutral traps, it is necessary to develop new test procedures to assure that the annealing steps have been effective.

High-resolution scanning acoustic microscopy [55] is a new technique for direct imaging of the crystal or device chip. The instrumentation, shown in figure 26, is relatively simple to use because it responds to the elastic properties of the specimen. Acoustic microscopy provides the possibility of observing defects, such as the voids under metallization crossovers shown in figure 27, which are not detectable by the more traditional imaging methods such as visible-light, infrared, or electron microscopy.

4. OTHER METROLOGY

Microstructure fabrication imposes additional demands on the purity of process chemicals and gases. Chemical purity to the degree required for microelectronic fabrication is not a trivial matter. Only recently have specifications for chemicals used in microelectronics been prepared and methods to test for impurities in these chemicals been assembled [56]. It remains to be demonstrated whether these specifications and test procedures will be adequate for chemicals to be used in fabrication of submicrometer devices and structures.

A variety of new processing technologies is required to fabricate microstructures. A new set of measurements, replacements for the traditional times and temperatures, is essential for controlling the new processes if reproducible devices with predictable characteristics are to be manufactured.

For example, accurate control of shallow, low-dose ion implantations is critical to modern device performance. Careful studies have been made of secondary particle collection procedures to improve the accuracy of dose measurements [57]. A systematic investigation of the dependence of implant profiles on the beam alignment angle led to the conclusion that in a variety of circumstances significant channeling tails can exist for alignment angles commonly thought to yield random-equivalent implants [58]. NBS has had some inquiries which suggest there might be a need for standards to relate the sheet resistance of an implanted layer to the implanter machine parameters. Although it would appear that the already developed dose measurement procedures would be adequate to predict the sheet resistance, additional standards may be required for use in manufacturing environments.

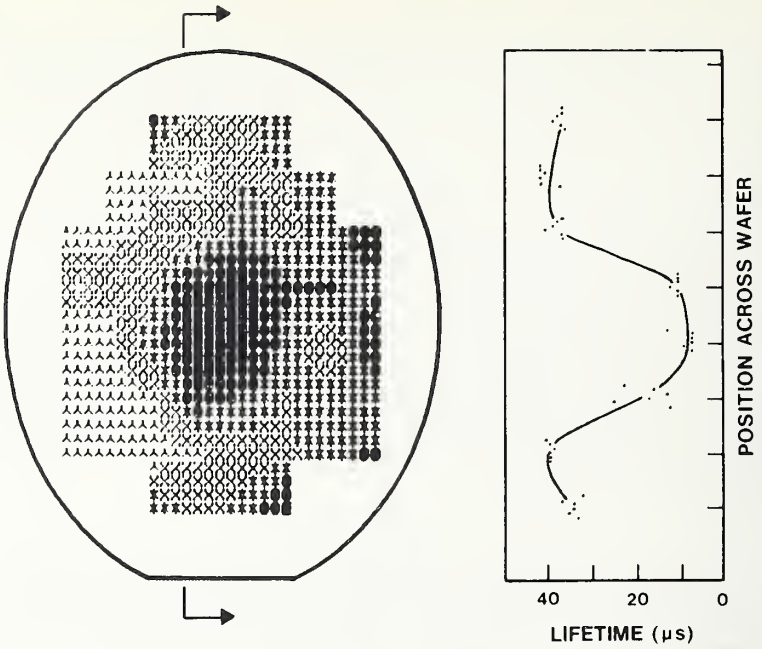


Figure 24. Wafer map of generation lifetime as determined from measurements on integrated gated-diode test structures fabricated with a p-channel, self-aligned polysilicon gate technology. The values given on the map are averages of measurements made on six diodes in each cell; darker symbols represent lower lifetime. The graph on the right shows the results of individual measurements in the line of cells identified by the arrows on the wafer map.

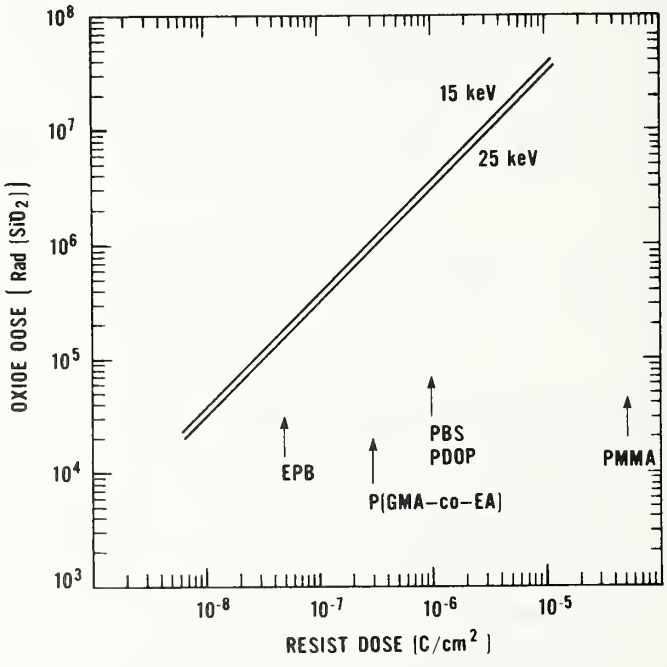


Figure 25. Dose deposited in a 100-nm thick oxide under 1-μm thick aluminum and 500-nm thick resist as a function of the dose in the resist for 15- and 25-keV electrons. The doses required to expose typical e-beam resists are indicated by the vertical arrows. (After Galloway *et al.* [53])

Sensitive measuring techniques are also needed to evaluate the annealing step required to activate implants [59]. For shallow, low-dose implants, only capacitance voltage profiling appears to have adequate sensitivity for measuring dopant profiles. Figure 28 shows the highly doped surface region produced by annealing of a low-dose implant with a 1-μs pulse from a dye laser. The scanning electron microscope operated in the charge-collection mode appears to be the most appropriate technique for studying electrically active defects in implanted regions; these defects may or may not be removed by the annealing step. The three scanning electron micrographs in figure 29 show — from left to right — unannealed, thermally annealed, and 1-μs pulse-laser annealed regions. Defects appear as the dark areas of the micrograph. Annealing with pulsed or scanned steady-state lasers is currently a very active research field. Different laser conditions have yielded significant differences in impurity redistribution and defect removal properties; new metrology is required for characterization and control of the laser sources.

Plasma etching is an important process for patterning microstructures. At the present time, the physics of the plasma etching mechanism is not well understood and a good in-line monitoring system for this process is not yet available. Neither mass spectrometry nor optical spectroscopy provides data on either etch rate or uniformity of etching, although both techniques provide end point information. Interferometric monitoring provides both etch rate and end point information but does not provide data on the etching uniformity.

Process-induced structural faults, such as pin holes in insulating films, shorts between layers in the structure, or open circuits in the metal interconnection runs, represent yield-limiting factors in microstructure fabrication. These faults may occur randomly or they may be clustered in various localized positions. Test structures for these faults may be series or parallel strings (designed to be tested with a continuity tester) or memory-like addressable arrays as shown in figure 30 [18]. Both types of structures must occupy substantial areas on the wafer if they are to be effective. At the present time, the models for analyzing the results obtained on such structures are extremely crude; nevertheless, qualitative and semiquantitative information can frequently be obtained.

The large die and package configurations associated with very large scale integrated circuits impose additional requirements on the measurement of mechanical integrity of the package, interior moisture levels in the package, and heat transfer characteristics of the die package configuration. Accurate measurements of these quantities are, at the present time, virtually impossible. All these areas are currently under investigation, but the work is in such an early stage that definitive results have not yet been achieved.

5. SUMMARY

In summary, selected types of metrology associated with submicrometer devices and structures have been examined with emphasis on problems associated with dimensional metrology and characterization of semiconducting materials. Generally speaking, metrology on the scale required for microstructures is still in an embryonic state. Resolution and sensitivity of conventional methods for both dimensional measurements and materials characterization must be ex-

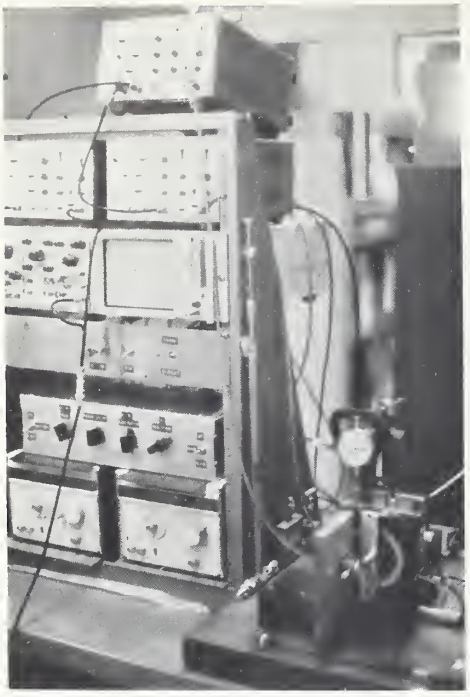


Figure 26. Experimental setup for 370-MHz scanning acoustic microscope. (Photo by Hughes Research Laboratories)

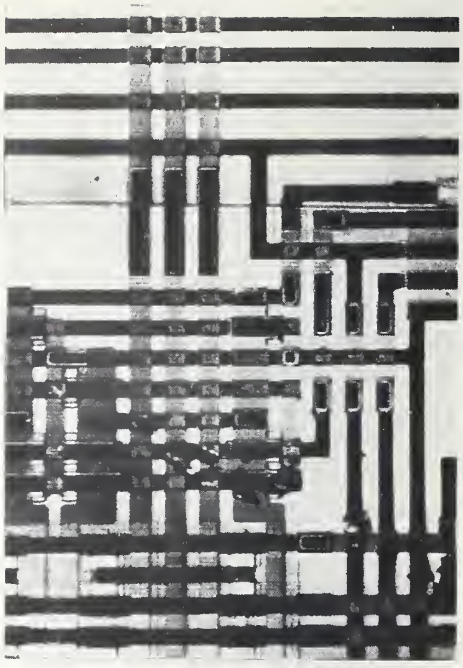


Figure 27. Scanning acoustic micrograph of a section of a silicon-on-sapphire integrated circuit which illustrates structural detail under the metallization stripes. (Micrograph by C. F. Quate, Stanford University)

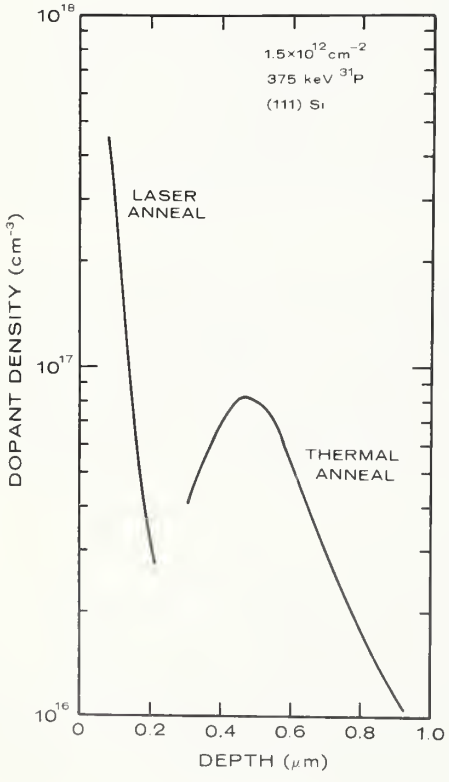
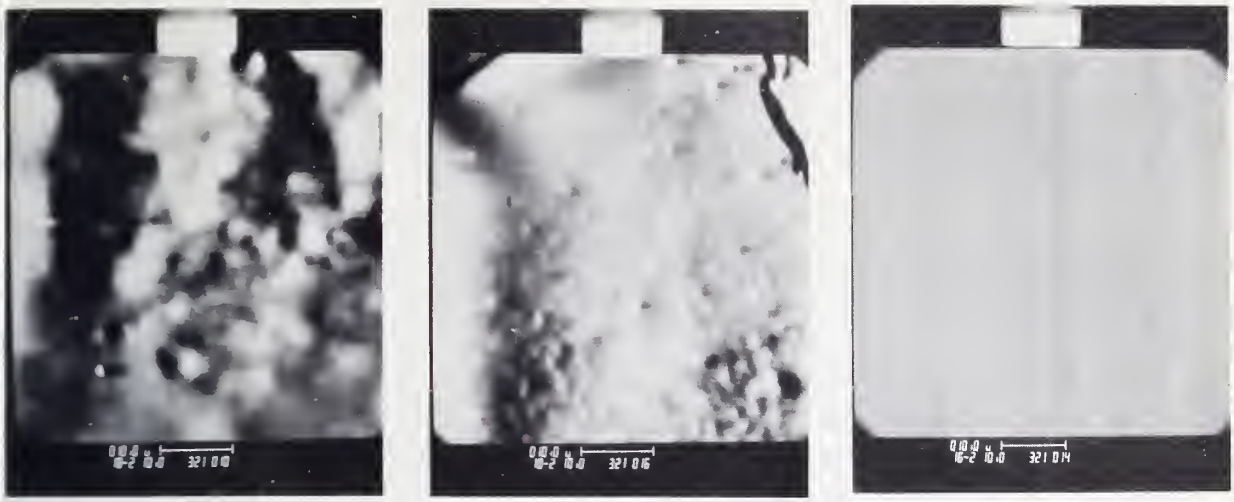
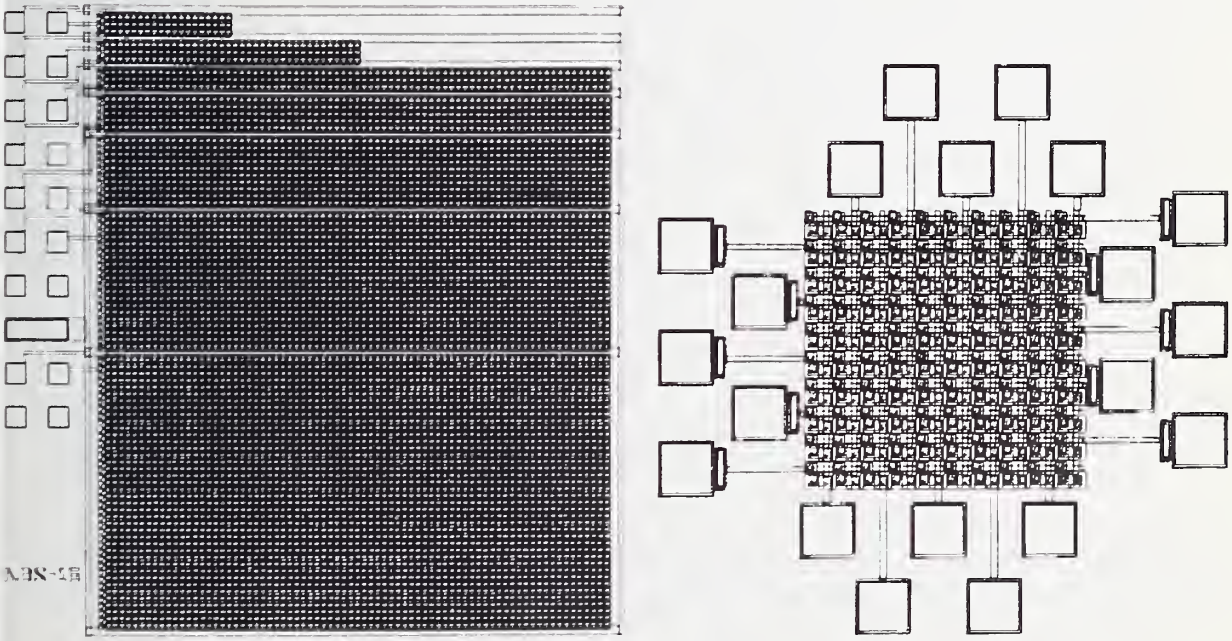


Figure 28 (left). Capacitance-voltage profiles of a phosphorus-implanted silicon wafer characteristic of thermally annealed and laser-annealed areas of the wafer, illustrating highly doped surface region produced by laser annealing. (After Myers *et al.* [59])



(a) (b) (c)

Figure 29. Charge collection scanning electron micrographs of as-implanted (a), thermally annealed (b), and laser-annealed (c) regions of a silicon wafer implanted with boron to a dose of about 10^{12} cm^{-2}. (After Myers *et al.* [59])



a. Parallel-string tester for leakage in gate and field oxides.

b. A 10 by 10 array of individually addressable MOSFETs.

Figure 30. Outline drawings of random fault testers included on test pattern NBS-16. (After Linholm [18])

tended if these are to be useful in the submicrometer range. In some cases adequate methods do not yet exist, and new methods and standards must be developed. This need is widely recognized, and considerable activity for this field is now underway at many laboratories throughout the world to provide the advanced measurement technology needed for the reproducible manufacture of microstructures with predictable characteristics.

6. ACKNOWLEDGMENTS

The author wishes to thank the many members of the staff of the NBS Electron Devices Division and its contractors who have conducted the research reported herein for detailed discussions of their work and for their assistance in the preparation of this manuscript. In addition, he wishes to thank Graydon Larrabee of Texas Instruments for permission to reproduce figure 17 and for providing an original drawing of this figure. Finally, he wishes to thank the organizers of the Microstructure Fabrication Conference for the valuable opportunity to participate in the conference.

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NBS-114A (REV. 9-78)

U.S. DEPT. OF COMM. BIBLIOGRAPHIC DATA SHEET	1. PUBLICATION OR REPORT NO. NBS Spec. Publ. 400-61	2. Gov't. Accession No.	3. Recipient's Accession No.

4. TITLE AND SUBTITLE
Semiconductor Measurement Technology: Metrology for Submicrometer Devices and Circuits

5. Publication Date
June 1980

6. Performing Organization Code

7. AUTHOR(S)
W. Murray Bullis

8. Performing Organ. Report No.

9. PERFORMING ORGANIZATION NAME AND ADDRESS

NATIONAL BUREAU OF STANDARDS
DEPARTMENT OF COMMERCE
WASHINGTON, DC 20234

10. Project/Task/Work Unit No.

11. Contract/Grant No.

12. SPONSORING ORGANIZATION NAME AND COMPLETE ADDRESS *(Street, City, State, ZIP)*

Same as above

13. Type of Report & Period Covered
Final

14. Sponsoring Agency Code

15. SUPPLEMENTARY NOTES

☐ Document describes a computer program; SF-185, FIPS Software Summary, is attached.

16. ABSTRACT *(A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.)*

The metrological requirements of semiconductor microelectronics, always challenging, are made even more stringent by the trend toward submicrometer devices and structures. This comes about not only because of the obvious demands associated with the smaller feature sizes of circuit elements but also because of the attendant requirements for more efficient design verification aids, computer simulations, and process validation and control techniques and because of the concurrent trend toward larger die and package sizes. This paper examines the types of metrological requirements associated with submicrometer devices and structures, summarizes the present state of the art in selected critical areas of metrology, and reviews current research and development efforts on advanced measurement technology, especially those at the National Bureau of Standards.

17. KEY WORDS *(six to twelve entries; alphabetical order; capitalize only the first letter of the first key word unless a proper name; separated by semicolons)*

Dimensional metrology; electronics; integrated circuits; materials characterization; measurement methods; microelectronics; microstructures; semiconductors.

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UNCLASSIFIED	41
20. SECURITY CLASS (THIS PAGE)	22. Price
UNCLASSIFIED	$2.25

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