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Semiconductor Measurement Technology:

Comprehensive Test Pattern and Approach for Characterizing SOS Technology

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Semiconductor Measurement Technology:

Comprehensive Test Pattern and Approach for Characterizing SOS Technology

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PREFACE

This work was performed in the RCA Integrated Circuit Laboratory, J. H. Scott, Director, N. Goldsmith, Group Head, and W. E. Ham, Project Scientist. Many people supported this effort during the various phases of the work. In the initial phases during drawing and digitizing of the structures, N. Kudrajashev, G. Meray, A. O'Toole, and E. Strouse were instrumental. Thanks are also due to N. Kudrajashev for pursuing the computer-aided design through difficult delays until perfect reticles were obtained. E. Strouse provided the technical support for processing the wafers, and A. O'Toole performed many of the manual and semi-automatic tests and took many of the photographs during the automatic testing stages. N. Capone was very helpful in constructing a semiautomatic probing station used for preliminary testing. P. Herkart was invaluable for producing a practical realization of the test block concept. F. Brehm and N. Goldsmith were very helpful in creating some of the software needed for data reduction after automatic testing. Thanks are also due to the drafting, reprographic services, and technical editing departments for their determination to make it happen.

Because the tooling within the contractor's photomask facility is in English units, the photomask dimensions do not conform to the International System of units. The English units are used only for representing the features on the photomasks and fabricated wafer and are not used in computations.

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The contract was monitored by Richard L. Raybold and Martin G. Buehler as the Contracting Officer's Technical Representative. Technical review of this work was provided by Martin G. Buehler, Loren L. Linholm, John M. David, W. M. Bullis, and Julian K. Whittaker.

Abstract

This report contains detailed information concerning a comprehensive approach to parametric process characterization for IC processes. This includes defining the general areas of importance, devising structures which are sensitive to these areas, devising methods for testing the structures, documenting the structures, tests, and results, producing suitable data reduction and presentation schemes, and considering the implementation of the methods in a practical sense. Proper methods for automatically testing some of these structures are explored. Seven divisions were created for the general types of test structure: (1) individual structures of nominal dimensions, (2) closely spaced identical structures, (3) structures of various sizes, (4) series and parallel combinations of structures, (5) structures especially sensitive to lithographic properties, (6) basic circuit building blocks, and (7) small area test circuits.

A test pattern, compatible primarily with silicon on sapphire technology, which integrates into a single mask set (6 levels) test structures to measure the properties of each of these basic divisions, was created and partially tested. This concept of total integration is shown to be valuable for determining causes and effects of many kinds with the use of only a small number of test wafers. An attempt was made to use computer-aided techniques as much as possible. These found application in mask making (the masks would have been much more difficult to create without the computer), documentation (where computer line drawings were used as the basic drawings), testing (where a standardizable building block approach was implemented), and finally, the traditional use of the computer for data reduction and presentation. The test pattern contains 175 individually identified test structures and has approximately 1250 electrical access pads for each chip. The chip dimensions are 258 by 258 mil (6.553 x 6.553 mm). All of these structures are documented with cross sections and line drawings. A discussion of the intended uses of the structures, of their peculiarities, and samples of actual test results for many of the structures are included. A "small-signal" approach to testing, data analysis, and test structure design was used in several cases. For the test structure design, the small-signal approach is particularly useful with respect to physical structure sensitivity. For the testing, it finds traditional applications in the measurement of slopes, while in the data analysis differences in identically acquired data from different wafers are frequently the desired information.

Results from a limited use of the pattern on a sampling of wafers from a few lots indicated that contact resistance effects and deposited oxide pin holes were much more important than previously thought. Alignment measurements between photomasking levels were obtained with an accuracy of $\pm$250 A. The closely spaced and nominally identical structures are shown to be especially valuable for determining the nature of the individual measurements and for providing some of the best clues to the causes of the observed variations.

The uses of the overall approach include processing facility comparisons using structures with understandable outputs, detecting the least controlled parts of the process, providing a solid base on which to define circuit design rules, and predicting parametric yield loss to be expected due to circuit design-process incompatibility.

Key Words: Comprehensive process characterization; design rules; intradie parametric integrity; LSI circuits; mask alignment tolerances; modular test programs; parametric yield limitations; performance limitations; photomask performance; process control; test patterns; test structures; total process integration.

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1. INTRODUCTION

1.1 Overview

This document describes a comprehensive approach for measuring many of the parametric properties of the processes and devices used in the fabrication of integrated circuits. The approach first considers that dividing the features of the process into a few specific categories and then dealing with each category on its own will provide a more tractable situation than attempting to deal with all of the properties at the same time. This basic concept of modularization pervades the entire effort. Once the categories are defined, consideration is given to the nature and specific methods of obtaining and using data to quantify the various features of the category. Obviously any effort of this magnitude will not be optimum until several attempts, each building on the previous efforts, have been completed. This work represents a "third level" attempt and relies heavily on previous experience.

There are restrictions on the specific reduction to practice to be described. In the first place attention is directed mainly towards MOS (Metal-Oxide-Semiconductor) processes and is further aimed at thin-film semiconductors on insulating substrates. The most common technology of this type uses thin-film silicon (typically 0.4 to 0.8 μm thick) epitaxially deposited on single-crystal sapphire wafers. This technology is usually abbreviated "SOS." In the second place this work does not attempt to measure the frequency of small numbers of randomly placed "defects" which may exist on the wafer surface. It does, however, address the possible consequences of specific types of defects. Thirdly, it is not expected that all of the possible measurements will be needed in any specific application. An attempt is made to provide a method for obtaining any desired information which is not excluded by the above restrictions.

In most cases, and certainly in the case of SOS, a set of seven general areas of interest which apply to parametric characterization can be listed. This is done in figure 1.

A	B	C	D
OVERALL FACILITY PROPERTIES (PRODUCT FLOW)	SPECIFIC PARAMETER DISTRIBUTIONS (SPATIAL OR NUMERICAL)	REPRODUCIBILITY FROM WAFER TO WAFER	LITHOGRAPHIC PERFORMANCE

E	F	G
PROPERTIES OF SPECIFIC PROCESSING STEPS	TIME-ENVIRONMENT STABILITY OF PARAMETERS AND/OR PHYSICAL PROPERTIES	ANY CROSS-COUPLING BETWEEN A-F

Figure 1. Areas of interest for parametric characterization.

These seven areas provide the beginning point for the comprehensive approach addressed in the first paragraph. For each of these areas one must first devise elements or test structures which are sensitive to the features of interest in each category. One must then select a measurement method for each test structure.

A further consideration must be given to the *nature* of the measurement desired. In particular one must be aware that a fundamental difference exists between measurements made on structures which are assumed to be perfect in macroscopic physical terms and those which are not. The former are defined, for purposes of this document, as parametric structures while the latter are referred to as defect-sensitive structures. In some cases it is possible for a structure to be both types. Although it is possible to perform defect studies using small areas of the wafer, it is essentially impossible to adequately measure random defect behavior relevant to LSI (Large Scale Integration) circuits without using large dedicated areas of the wafer.

Even if one is willing to expend the sizable effort and expense required for fabricating large-area, random defect-sensitive structures, it is also required that *predictable* or at least reproducible defect density levels be available. In particular, if photomasks are used to fabricate the test structures, the defect density levels in the masks *as well as* those in the process of interest must be known and not be variable. Typically, using photomasks to fabricate the test structures produces a strongly variable defect density because every time the masks are used to make a print, the defect density changes. One can probably establish relationships (functional forms) between apparent defect density and the area occupied by the test structure for a given set of conditions. The probability of a defect being in a certain size area may be exponentially related to the area, for example. However, this effort is likely to be fruitless if not misleading unless all of the parameters of the functional form are known when the measurement is performed (i.e., not what they were the last time the measurement was attempted). In other words, using the results of a defect study of this type to predict the results of another experiment (the yield of a particular circuit type, for example) is very likely to *appear* valid because the functional form is satisfied but in fact may be totally misleading because the parameters (defect densities, for example) on the measurement vehicle are different (for any number of possible reasons) from those used to make the circuits.

The parametric approach also depends on the reproducibility of the process, but it is relatively immune to the effects of random defects. Thus a deliberate choice was made to avoid attempting to deal with effects which depend on random defect *density* in the belief that this type of work is best done on volume production of actual working circuits. In the volume production mode the randomness can be dealt with using statistical methods, and the results will be meaningful. It is difficult to justify the volume expense incurred if the product cannot be sold. The parametric approach does allow certain information about defects, and for this purpose it is convenient to define three classes as shown in figure 2.

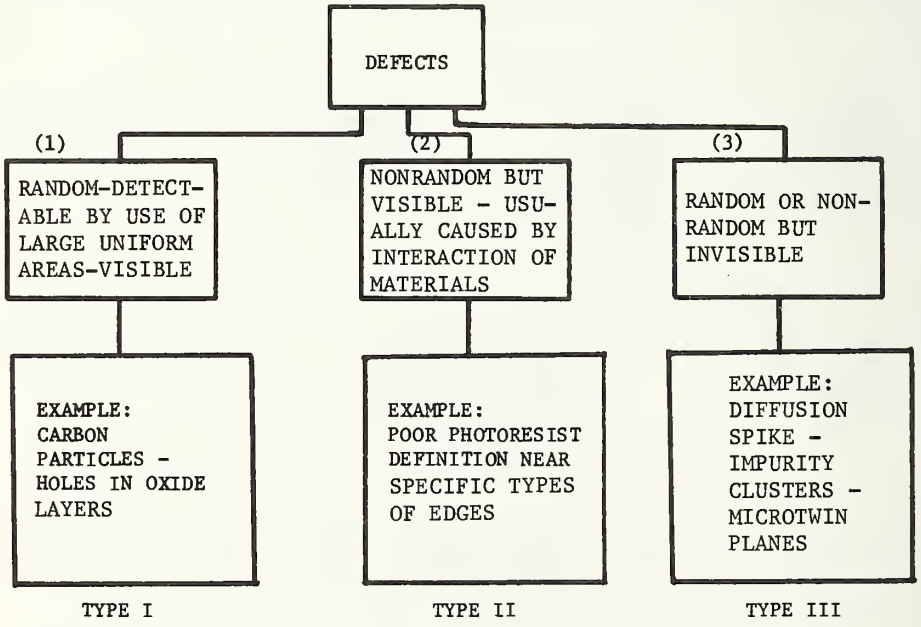

Figure 2. Types of defects.

As mentioned above the type I defects in figure 2 will be ignored except to note the effects of certain visible defects in the parametric behavior of parametric structures. These defects generally affect only *yield* of devices. They do not affect performance unless they limit the size or operating range of the circuit which can be produced with any nonzero yield. In general, it is very costly to perform truly meaningful defect studies of this type because of the inherently large dedicated areas required, the large variation in defect densities usually experienced, and the large number of processing steps which must

be examined to *simulate* the actual circuit. Parametric studies, on the other hand, can be easily be performed on structures which exactly represent the situation in a circuit and are relatively inexpensive since they require only a small number of samples.

The second type of defect is visible optically and will be addressed in this work. This type of defect can be characterized by examining a small local area. If the photoresist has poor definition near an edge, for example, it is only necessary to measure the extent of this effect over a distance of perhaps 10 times the extent of the effect. If a structure which exhibits this effect fails in extended sections but not in local regions, the failure is, by definition, due to a type I defect.

The third type is not directly considered in the work reported here. It may be possible in some cases to relate the data acquired from the test vehicle to these invisible defects with subsequent experimentation.

If cost is the main issue, one must focus some effort on defects since they are sometimes a major factor in determining the yield of good working circuits. If performance is the main issue, one must focus on parametric properties and intelligent design. If the parametric properties of the process are well known, it is possible to design a circuit not only for optimum performance but also for optimum yield. For example, if the alignment tolerances being achieved in the facility used to manufacture the circuit are well known and have been thoroughly measured, there is no question concerning the design rules to use between levels from a mask-technology point of view. Nor is there a question when a designer is deliberately pushing the design for better performance at the expense of yield. Similar statements can be made for any other parameter. Yield loss due to parameters falling outside the design limits can be reasonably predicted before making the circuit. On the other hand, performance loss can be obtained by allowing more tolerance than necessary in the design. All too frequently attempts are made to adjust the processing parameters to the circuit design. It is suggested here that attempts should also be made to adjust the circuit design to the process *as it currently exists*. This work provides key inputs to the parametric properties and provides a way to obtain much of the information needed for optimum circuit design.

A large and comprehensive collection of test structures which allow the measurement of many of the properties of the areas of interest listed in figure 1 will be described in detail. This collection of structures is referred to as the "test pattern," the "test vehicle," or simply "the pattern." Testing procedures for the structures are also considered. This work is a direct outgrowth of the ideas set down by Ham and Crossley [1] and by Crossley and Ham [2]. The volume of structures has been expanded and the testing procedures have been detailed, but the basic ideas and the implementation method are identical.

Although the pattern was intended originally to test the parametric properties of an LSI process, it has been found that it is also useful for testing virtually every technology that it encounters. In particular it was useful for debugging computer-aided mask-making software.

The list of people who can use the results from a pattern of the type to be described is very long. A partial list is given below.

- Anyone who wants to produce circuits from a known process
- Those who have no direct control over the actual processes used for making their circuits
- Circuit designers
- Process control engineers
- Agencies requiring line qualification

---

1. Ham, W. E. and Crossley, P. A., "Test Structure Design Criteria and Results of Electrical Tests for Silicon on Sapphire Integrated Circuit Processes," Metallurgical Society of AIME, Conference Program, Abstract D4, p. 14, Boston, MA, Aug 1972.
2. Crossley, P. A. and Ham, W. E., "Use of Test Structures and Results of Electrical Tests for Silicon on Sapphire Integrated Circuit Processes," J. Electron. Mater. 2, No. 4, 465-483 (1973).

- Those who want to determine which facility to use for a particular product
- Reliability engineers
- Materials analysis scientists
- Process designers
- Circuit probing engineers
- Photomask engineers
- Photoresist engineers

Obviously the interests of these possible users are widely different and the tests performed and the excitation levels used during the tests cannot be specified in general. The one thing all users have in common is that they would like to believe that the results obtained from a characterization effort will apply again under the same conditions. This is discussed in more detail in subsection 1.4.

1.2 Key Features

a. Spatial Integrity

One of the most important features of the test pattern is the inclusion of various spatial resolutions. The spatial variations observed provide the best clues available concerning the expected variations over areas typical of a circuit. They are also very useful in determining the value of measurements from a single test device in terms of the area of the wafer which is represented by the device. It is apparent that if the entire wafer area is measured, as in the defect sensitive pattern case, a large dedicated area is required for a small amount of information. We therefore choose to use part of the surface area for detailed local measurement, and to leave part of the area for other types of measurement. One is *forced* to choose between spatial resolution and the number of different types of process characteristics available if a single test vehicle is used. In the comprehensive approach taken here, a mixture of depth of information in terms of the number of different aspects of the process available with a detailed spatial resolution for certain key parameters is used.

In general, locating a specific integrated circuit processing position can be considered as a multidimensional proposition. Some of the considerations are:

- The position on the wafer surface with respect to the wafer edge.
- The position on the wafer surface with respect to other surface positions.
- The depth below the surface of the wafer.
- The position relative to other wafers.
- The position in the processing fixture.

All of the above are part of the spatial content of the data. The first two are handled by design of the test vehicle and the testing procedure used, the third is determined by the test structure and the process used, while the fourth and fifth are handled by the bookkeeping procedures used during the processing of the wafers.

Omitting the spatial identification in the specification of data provides the possibility for missing correlations that exist, for grossly misinterpreting the meaning of the data, and for erroneously concluding that "the test vehicle does not represent the product so why bother." It is of paramount importance that the processing position be religiously attached to the data and that the spatial distribution and position be examined along with the numerical values.

Conversely it is pointless to use a measurement to infer something concerning the properties of another device unless the measurement also applies within known limits at the position of the other device.

b. Process Component Separation

A second key feature involves separating specific process components from each other. To this end, test structures are formed from the basic materials of construction and process sequence used to form the product of interest to maximize the sensitivity of their measured output to some known property of the structure or of its fabrication history. The materials, interfaces, geometrical shapes, and fabrication steps are the *test structure* components while the output reflects the characteristics of the process components. In some cases, complicated structures depend critically on the successful achievement of many different processing steps while others are sensitive to only one step. The more complicated the test structure, the greater the importance of knowing the success of forming its components.

Higher order test structures include devices which depend on a specific type of electrical contact or structures which contain many elements. These higher-order structures are formed so that the interaction of a controlled number of components can be studied. This controlled number is usually minimized. In some cases, however, such as the MOS transistor, several components can be studied rather independently of one another in one test structure.

Thus a hierarchy of test structures which progress from very simple to very complicated is included in the test vehicle. In general it is necessary that each level of this hierarchy be characterized in order to proceed to the next level. If complete characterization is not necessary, the ability for thorough characterization is included in the vehicle in case it is needed. *A reliable process component separation is possible only if all sublevels needed for the structure are suitable.*

c. Test Structure Stimuli and Outputs

For most applications, the basic stimuli applied to the test structures are either of an optical nature or of an electrical nature. Situations exist where other physical or chemical stimuli are used (such as SEM, TEM, electron microprobing, etc), but in many cases structures suitable for visual examination will also be suitable for these stimuli. Those which are not are usually too small or cannot be included in the test vehicle because of space limitations. Thus the most basic division is therefore between the structures stimulated electrically and those stimulated by photons. Any electrically accessible structure can also be used as an optically accessible structure, and this duality forms a cornerstone for partially evaluating the suitability of the structure for the electrical measurement. The basic outputs are scattered, reflected, diffracted (or otherwise affected by the sample) photons or an electrical current or voltage.

The optical structures form the simplest and most basic tests. One cannot expect a reliable measurement from a test structure which does not have the intended physical structure. The most basic electrical test is for the nature of the electrical contact to the important part of the electrical test structures. This electrical contact proceeds through a wire or probe to a pad (usually metallized). Further connections through metal lines, "contact holes," and diffused layers may be necessary to electrically reach the desired part of the test structure. This latter connection sequence is a worst case for test structures and may, in fact, be used to distinguish between circuits and test devices. If electrical access to a device requires passing current through another device, then the system can be treated as a circuit.

Several examples of higher order structures which use another and different type of stimuli are included in the vehicle. These stimuli are essentially physical in nature but provide as real a stimulus as an applied voltage. These stimuli are positional or dimensional differences in otherwise identical structures. The electrical stimuli used for each part of the structure are identical while the output reflects the effect of the physical differences. For example, two identical three-terminal MOS transistors positioned such that for exactly the same electrical stimuli the current flows in the opposite direction in each device provide nearly the same stimuli as that of reversing the polarity of the applied voltage in one device. There is one major difference, however. In the case of reversing the voltage polarity and remeasuring the same device, some effects may remain during the second measurement (hot electron injection, for example). The true effect of only reversing the current flow can be seen only in another nominally identical structure. If the other device is rotated 180 degrees, no effects of changing the

electrical stimuli and sensing system to the opposite polarity will be seen. Thus by using a physical "stimuli," it is possible to perform a greater depth of characterization than is possible by electrical stimuli alone.

In the above example there was an option of reversing the electrical system polarity. When dimensional differences are involved, there is no such option. The "stimuli" of varying a dimension of an otherwise identical structure can provide a very useful output which is unattainable by any other means.

When reasonable operation of a test structure has been achieved, two properties are of critical importance to the application of the results to an LSI circuit: (1) the minimum physical size obtainable and (2) the number of identical structures that can be fabricated at the same time without a failure. The minimum size obtainable is obviously of considerable importance since packing density and performance can be dramatically affected by a decrease in certain minimum dimensions. Furthermore, a great deal of insight and diagnostic capability can sometimes be achieved by examining test structures that are *smaller* than the smallest in a circuit. Successful operation of these smaller devices usually indicates that a larger device will also be successful. Whereas it is impossible to adequately (and simultaneously) simulate all of the large number of elements in an LSI circuit in a test structure (because of the large space requirements as discussed earlier), a great deal of confidence in the *essential* process components can be achieved by simultaneously examining several identical devices instead of only one. This is also a type of physical stimulus.

d. Total Integration

Perhaps the single most important feature of the comprehensive approach is the fact that *precisely the same* process is used to fabricate *all* of the structures on the wafer (except, of course, for the processing position). That is to say that the same chemicals, masks, furnaces, silicon, etc were used. This feature is entirely missing in defect studies. If one has ever tried to duplicate an unusual phenomenon using "identical processing," he will appreciate that no two processes are identical, no matter how carefully the processing is done. Therefore, it is important in this approach to have all of the structures which are likely to be useful for characterizing any phase of the process included in the same vehicle.

Provisions for separating the process components, for dealing with spatial integrity, and for implementing the other features mentioned earlier were made in the vehicle to be described in detail in the later sections. A class of purely optically accessible tests is also considered wherein the absolute limits of the lithographic technology and the relationships of different lithographic levels to each other are measured. Additional types of test structures address the operation of certain collections of devices which form basic circuit building blocks, and the dynamic performance of these collections. A relatively complete analysis of a process used to fabricate a CMOS LSI circuit can be obtained from the collection of test structures to be described. These structures depend only on the process and the *device* design. They are intended to be completely circuit-design-independent. The general partitioning chosen should be useful for any MOS technology. The specific layout could also be used in most cases. Many structures were designed so that the electrical access would not need to be changed for different technologies. This allows libraries of general test and analysis programs to evolve.

Total integration demands that the test structure design allow devices to be operated independently of other devices, even if common connections exist. This is easily achieved because the pads contacted by probes not being used for the test are completely electrically open and unable to provide a current path. For bulk silicon processes, the substrate, in addition to the unused probes, may be completely isolated from ground during testing to eliminate the need for specific device isolation. This allows a much greater packing density for test devices. In other words, the bulk devices can be essentially the same as SOS devices as far as testing is concerned. When the bulk substrate potential is determined by a test device, only one device at a time may be connected.

Of particular importance in the total integration feature of the comprehensive approach is the cross referencing available between various aspects of the process.

Since the processing is "identical" within any small area of the wafer, specific and direct correlation between electrical effects and the physical properties (as revealed optically) or between other electrical effects from neighboring devices can be made by simultaneously performing both types of test. Total integration can be instrumental to providing the most rapid route to the *correct* answer.

One of the most important outfalls of this approach has been the concept of the super-integrated test structure. Several examples of this type of structure exist on this pattern. For example, the structures of subsections 3.13, 3.14, and 3.15 (section 3) integrate most of the important features of the transistor properties, contact resistance properties, and diffused sheet resistance properties into one small section of silicon. Structures described in subsection 3.19 through 3.23 (section 3) integrate many different types of diode and transistor into the same small silicon bar. Each integration performed saves at least one pad and produces results on devices which are more closely spaced. For production use in most cases integration should be done to minimize the number (not the size) of bonding pads wherever possible.

1.3 Relationship to Other Types of Test Vehicles

There are at least five general types of vehicle used in the manufacturing of integrated circuits; each has its own special function and none can provide all the answers. There are two basic divisions between use of test devices. These are (1) those which are manufactured as part of the wafer used to make operating circuits and (2) those which are manufactured as a specific test vehicle. There is also an intermediate division which is sometimes used where test wafers are interspersed within those used for circuitry. This is essentially the same as (2) above. The vehicles falling into the first division are:

(1) Individual test structures on the circuits (usually on the periphery)

(2) Collections of individual test structures on the wafer with the circuits but at certain selected sites only (called diagnostic keys, test runs, test element groups, etc)

(3) An actual circuit

Those falling into the second division are:

(4) Defect-sensitive test patterns, dedicated spatial resolution patterns, other patterns dedicated to specific purpose

(5) Whole wafers of type 2 above

(6) Comprehensive test vehicles

Types 1, 2, and 3 have the property that they *must* have been processed with the exact process used for making operating circuits while types 4, 5 and 6 may not have been processed exactly as a circuit.

A comparison of the relative merits and features of these different types of vehicle is shown in Table 1. It is clear that a wide variety of functions can be served by the vehicles. The comprehensive vehicles are the best approach when little is known about the process and can be extremely valuable for rapid and accurate diagnosis when processing problems arise. Thus they serve a function which cannot be realized by the other types.

1.4 General Mode of Intended Use of the Test Pattern

a. Data Acquisition and Reduction

It should be clear at this point that most of the parametric properties of an MOS process are available from the structures on the pattern to be described. In fact there

TABLE 1. FEATURES OF VARIOUS TYPES OF TEST VEHICLE*

Type	Total Area Covered by Test Vehicle	Circuit Area Represented by Test Vehicle	Wafer Area Represented by Test Vehicle	No. of Parameters Available	Spatial Resolution	Specific Interpretations Obtained from Data	Effort to Use	Potential Rewards	Typical Use and Comments
1 - Individual test structures on the circuits (usually on the periphery)	1	1	5	2	3	5	3	5-10	Wafer Acceptance Testing (WAT) - crude diagnostics - fairly good representation of wafer area
2 - Collections of individual test structures on the wafer with the circuits but at certain selected sites only (called diagnostic keys, test runs, test element group, etc)	1	5	1-4 depending on deployment	7	1	6	5	5	Wafer Acceptance Testing (WAT) - diagnostics - very poor representation of wafer area
3 - An actual circuit	10	10	10	2	3	2	2	2-10 depending on the problems	Yield mapping - visual analysis of failed parts - can be a very excellent vehicle under some conditions
4. Defect-sensitive test patterns, dedicated spatial resolution patterr, other patterns dedicated to specific purposes	10	5-10	10	1	3-10 depending on type	1	2-10 depending on number of samples and tests performed	3	Defect Characterization - dedicated spatial parametric studies - only very small part of process studies under any one set conditions - large numbers of samples required
5. Whole wafers of type 2 above	10	5	10	8	3	8	8	8	Process characterization - usually very weak in spatial integrity function - tend to be designed for specific circuit problems - or as WAT chip
6. Comprehensive test vehicles	10	8	10	10	10	10	2-10 depending on tests required	10	Nearly complete total process. Characterization - designed primarily for whole wafer use - careful attention to total integration - small number of samples needed

*The numbers represent a relative ranking within the same column. 0 is the lowest; 10 is the highest.

are many more parameters available than can reasonably be measured at any one time. If all were measured at one time, there would be such an overwhelming volume of data, even in very reduced form such as three-dimensional plots, that the entire effort would be incomprehensible. Fortunately only a small part of the total available data is likely to be of particular interest at any given time and this is the key to the successful implementation of this pattern.

In addition to the vast number of parameters available on a single pattern, there is the issue of other process positions such as the position of the wafer with respect to other wafers during processing, the wafer position in the processing fixtures, and the average effects from a typical size processing lot for the facility used to manufacture the wafers. This pattern would typically be used across the entire wafer in order to obtain the maximum information concerning process position. (It is of course possible to put the entire pattern at certain selected sites among the actual circuit for direct comparison of circuit performance with parametric performance.) Much in the same way that a single measurement from a test structure has a zero confidence level for process characterization, data from a single wafer have a zero confidence level with respect to other wafers. It is therefore necessary to examine several wafers before any claim to total process characterization can be made. Similar statements can be made concerning wafer lots. It is obvious that each wafer involved in the test must be *thoroughly and completely identified* if any statements with respect to the process positions are to be made. Similarly each pellet on the wafer must be identified although this can easily be done automatically during testing. The better the wafer processing history is known, the better the data can be related to the process. This wafer identification and its processing history must be accounted for independently and cannot be built into a testing program. On the other hand, for some applications the processing history is of secondary interest. Such a case may arise, for example, when one wants to know only the overall performance of the process and is not interested in the details of why and where. This may be important if one wants to know which facility to use for a particular circuit design. In this case the only identification needed is the facility used.

A minimum of three wafers from a pack of three different lots (preferably processed with runs of circuit wafers) is suggested if the results are to be used with any confidence. If the lithographic limits are of interest, at least three independently fabricated sets of masks (starting from the software stage) should be used for each lot. These nine wafers provide a minimum data sample. If inconsistencies are found, additional lots may be needed for complete characterization. Of course fewer wafers may be used but this invariably leads to questions of reproducibility. It is difficult to argue with the data sample suggested. If fewer wafers must be used for practical reasons, one can still produce some "typical" parametric information and can demonstrate "capability" in small volume. "If it can be done once, it is possible" types of statements can be made.

Every data point desired may exist at least nine times. It is quite clear, therefore, that the testing to be done must be very carefully considered before one becomes buried in a mass of irrelevant data. Once the set of wafers exists, the testing can be performed completely independently of the facility and in any order.

Once the structures of interest have been identified, the test block approach (see section 1.5) makes test programming almost trivial. The user must know enough about his interests to be able to specify the testing conditions, but generating the actual test program (a process which typically requires days) can be reduced to minutes. This concept is a major breakthrough in the field of test structure testing. It should also be noted that complete documentation and test identification are provided by the test block approach. Proper testing of test structures requires at least as much knowledge and skill as testing an LSI circuit. Some suggested groupings of tests are given in Appendix C. Usually the results of an initial testing will suggest the next round of tests needed. It may require several passes over the same wafer with different probe cards to obtain all of the data desired. (We note that changing probe cards is a trivial exercise for most probers and that the wafer does not need to be realigned. Probe cards can be changed in less than 1 minute.) One should have, after this testing exercise, all the data needed for his purpose. He is then faced with using these data.

The most common use of the data is a comparison with other similar data. It is therefore important that the same reference scales be used for the same parameters. This means that autolimit plots should *not* be used in most cases. It is usually sufficient to use data in histogram form *and* in wafer map form for the comparison. We note that even with all the data reduction provided by wafer maps and histograms, a very considerable number of plots are involved in characterizing one facility. It may require substantial effort to find the important differences; this is to be expected since IC processes are very complicated. Further work to transform the reduced data into a form which represents a set of "facility" parameters would be useful. Such an effort could follow the methods outlined in section 4 for the type II data. Of course less ambitious goals for characterizing individual process components can be carried out using well-known methods.

Some of the uses for this type of effort are summarized below.

- Provide a means for measuring the characteristics of a specific *process* (not circuit) which can be used to determine the suitability of the process for specific applications.
- Provide a means for determining what design tolerances *must* be allowed for in order for the process to *be able* to produce the expected result.
- Provide a standard for comparing different processes or facilities (for qualification purposes, for example).
- Provide a means for diagnosing processing problems that is somewhat independent of *visible* defects.
- Provide a means for determining the limitations and potential weaknesses in a specific process.
- Provide a means for in-depth analysis of interrelationship of parameters independent of processing pecularities.
- Provide a means for determining the sensitivity of the results to the details of the processing.
- Provide a source of structures for building specific purpose patterns.

1.5 Testing Considerations

a. General

Of all the features of comprehensive process characterization, none have the power to determine the total effectiveness of the effort more than the testing procedure employed. Improper test procedures, test documentation, test sequences, and/or test equipment have been responsible for a large portion of the *negative* feedback from efforts such as this where there is not always direct and immediate payoff. One *must* recognize the *subtle* points of performing, and especially of interpreting the results of, the measurements attempted. We shall consider the test procedures first.

The test procedures considered here are the sequence and type of stimuli applied and the sequence and type of response measured. When one applies only a single stimulus and response measurement, he must rely almost completely on *previously established models and experience* for confidence in the results. The magnitude of the response is the only clue to the validity of the testing procedure. Whereas many times it is true that the magnitude of the response does indicate a valid test, it is also possible that a "reasonable" value is not known, especially for the particular wafer being measured. The necessity for more than one measurement thus becomes apparent, if one is to have any confidence in the results.

There are two basic methods for accomplishing this multiple measurement procedure. The first involves the basic methodology, mentioned earlier, of examining nearly identical devices which differ from each other by a minimal amount (such as by position on the wafer surface). One can then compare the two results and obtain a great deal of confidence in *some features of the measurement*. In particular, any difference in the results must be due either to the precision of the measurement system or to differences in the properties of the device. Clearly, disagreement of the two measurements shows that the system as a whole is imprecise and that further investigation is needed. Close agreement of the results provides information that the system as a whole is precise, and that the result obtained is not (within a certain confidence limit) an accident. The latter case does not guarantee that the result is correct, only that it is repeatable.

The second basic method for producing confidence is to examine the same device under different stimulus conditions. In general, one takes a risk that previous stimuli may have changed the device so that the second measurement does not reflect the initial state of the device. (It is always possible to repeat the initial measurement to determine the degree of change.) In this method, a hierarchy of confidence levels exists. Performing only one additional measurement can provide a great deal of confidence in the suitability of the device to produce the expected measurement. Here, as with the first method, several additional measurements can be combined to produce greater confidence. The hierarchy of tests varies strongly from device to device. There are, however, some common features which can listed for most devices:

- Suitable electrical contacts
- Suitable isolation from other devices or from the media supporting the device
- Acceptable isolation from nominally insulating parts of the device
- Is the stimulus required within the range available from the generating hardware
- Is the response measured within the range available from the measurement hardware
- Input or output properties compatible with measurement system
- Linearity of response to stimuli (if expected)
- Bilaterality of response to stimuli (if expected)
- Degree of matching expected functional form of response to stimuli
- Suitable stability with respect to time, temperature, or previous testing

To be as confident as possible that *all of the conditions* for a valid result are met, it is necessary to perform tests related to the above list and, *in addition*, to perform tests on many nominally identical structures. Since this procedure is clearly expensive in terms of test time, a compromise must be made for some types of applications. The items with the best known, understood, and most predictable features should be eliminated first. Any item not included introduces a degree of doubt into the interpretation of the results. If the measurement can be performed at several different locations on the wafer surface, it should most certainly be done. Multiple measurements cause a linear increase in effort for many types of sensitive instruments where the electrical access points must be manually adjusted and the data must be recorded by hand. A completely automated system of data acquisition bypasses the linear effort increase for multiple measurement and is one of the most important reasons for considering automatic measurement. (It has been

found that by simply making the electrical access scheme automatic a dramatic reduction in effort for multiple measurements can be achieved.) The automation of the measurements also makes it possible to implement the items listed above with relatively small increases in overall effort. It will probably always remain true that some measurements are impractical to automate. We chose for the remainder of this report, however, to concentrate almost exclusively on the methods which are possible to automate.

Another reason for concentrating on automatic measurements is that one can make the judgment process for valid data reproducible and "operator-independent." Thus, whenever the program is used on the machine, the same decisions for the same inputs *will be* made.

b. Use of Models

A model is an expression of a set of data into a compact form from which one can *predict* the behavior of another device having the same basic form. We choose here to use "previously established models" as a guide to the functional form of response expected with regard to a *change* in stimulus. We are faced with a situation in the SOS case where detailed models are simply not known, as the following discussion for the SOS/MOS transistor indicates. The fundamental principles of MOS transistor operation have been published by many authors and in several textbooks [3,4]. In general, we seek to use the simplest approach consistent with experimental results, and no attempt has been made to devise a more exact model or to understand the detailed micro-operation of the devices formed from SOS. It may be categorically stated that although the basic operation of the SOS/MOS transistor is qualitatively similar to those of MOS transistors formed on bulk silicon, fundamental differences exist which are not readily adaptable to detailed modeling. These fundamental differences arise from two basic sources. The first is the lack of an isopotential "substrate" in the SOS case, and the second (and generally, more important) is that the silicon used for SOS has many defects (largely planar) [5,6].

The lack of a substrate causes two effects which are somewhat unique to SOS devices. The first of these is that a depletion region is limited to the extent of the silicon film and this can cause charges to appear in the silicon at the bottom interface for certain values of gate voltage. This alters the potential distribution in the silicon and can cause ill-understood contributions to the top surface potential.

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3. Cobbold, R. S., "Properties of Metal Oxide Semiconductor Junctions," Chapter 6, pp. 181-238, "Static Theory of Inversion Layer MOS Transistors," Chapter 7, pp. 239-271, "Charge, Capacitance and Small Signal Properties of MOS Transistors," Capacitance and Small Signal Properties of MOS Transistors," Chapter 8, pp. 272-304, *Theory and Applications of Field Effect Transistors*, (Wiley-Interscience, New York, 1970).
4. Grove, A. S., "Surface Effects and Surface Controlled Devices," Part III, *Physics and Technology of Semiconductor Devices*, pp. 263-355 (John Wiley and Sons, New York, 1967).
5. Schlotterer, A. and Zaminer, Ch., "Kristallbaufehler beim epitaxialen Wachstum von Silizium auf Magnesium-Aluminum-Spinell," Phys. Status Solidi 15, 399-411 (1966).
6. Ham, W. E., Abrahams, M. S., Buiocchi, C. J., and Blanc, J., "Direct Observation of the Structure of Thin, Commercially Useful Silicon on Sapphire Films by Cross Section Transmission Microscopy," J. Electrochem. Soc. 124, No. 4, 634-636 (1977).

The second effect is that it is not possible to control the reference potential throughout the entire channel region by making contact to the undepleted silicon from an external contact. This is one possible cause of departure from saturation at certain values of drain voltage [7,8] which is sometimes called "the kink." For very thick (>2 μm) or heavily doped SOS films, it is possible to make electrical contacts to the undepleted silicon throughout the entire channel region, but this situation does not represent a practically interesting case for the electronics industry.

The defects in the silicon raise severe questions concerning the model to apply to the test device. It has been shown that silicon with high defect density can be made to conduct strongly and behave in much the same way as defect-free silicon [9]. On the other hand, it has also been shown that junctionless devices can be made to behave in much the same way as junction devices as far as leakage current behavior is concerned because of their defect nature [9]. It is therefore clear that unless the defect nature of the device is known *a priori*, the correct model to apply in detail is not known.

The fact that different microscopic mechanisms may be operating does not make the detailed measurement or characterization of the devices less meaningful or less accurate. It simply means that less dependence on previously established models and the *assumed* meaning of results of these models is wise. We have chosen an approach which extracts the fundamental *external* behavior of the test structure in a way in which the results can be used for *comparison* of nominally identical structures and can be used to predict the "small-signal" behavior around the measured points. We have used previously established models only to obtain an expected functional form of variation. A good example is shown in the discussion for the ungated diode (section 3.21).

The testing problem reduces to that of specifying the type of test to be performed (voltage measurement, current measurement), the sequence in which tests are performed, points in the measurement at which decisions are made, and the type of output to be obtained.

c. Test Block Concept

For any given device it is possible to devise a test sequence and to define the decision points. It is usually possible to unite the testing procedure in such a way that stimulus levels and limit values for these decision points are variable while the basic execution sequence is maintained. If one can also define the electrical access points in general terms, he can completely specify a testing procedure by the following:

- Name of program
- List of electrical access points
- List of stimulus values
- List of decision limit values

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7. Nakahara, M., Iwasawa, H., and Yasutake, K., "Anomalous Enhancement of Substrate Terminal Current Beyond Pinch-Off in Silicon n-Channel MOS Transistors and Related Phenomena," Proc. IEEE 56, 2088-2090 (1968).
8. Farrington, D., "Anomalous Current-Voltage Characteristics of Floating Bulk MOSFET's," Extended Abstracts of the Electrochemical Society Meeting, New York, Vol. 74-2, Abstract 145, pp. 345-347, (Oct 1974).
9. Ham, W. E., "The Measurement and Interpretation of the Electrical Properties of SOS," Extended Abstracts of the Electrochemical Society Meeting, Las Vegas, Vol. 76-2, Abstract 172, pp. 462-464, (Oct 1976).

We note that this approach does not contain any limitations imposed by a particular testing machine in terms of test program language or test hardware. There are many advantages to writing test programs using this test block concept:

- The program is available for other structures, other pin configurations, other stimulus levels, or other criteria for valid tests *without reprogramming*. A thoroughly debugged and working version of the program is immediately available for any change desired as long as the change falls into one or more of the classes made variable.

- Confidence that the same test procedure is used by every user of the program. Users other than the original writer can be certain that system limitations and programming peculiarities of the test language have been accounted for.

- Complete documentation of the test conditions is readily obtainable from the program name and the values assigned to the variables. A detailed flow chart of the main program must be available for common reference.

- Larger master test programs can readily be created from the individual test blocks by appending other test blocks to the first. We have been able to create master test programs in 10% of the time required before implementing this concept. They *work the first time* and are completely documented automatically. A schematic example of a portion of a master test program created using test blocks is shown in figure 3.

- Users do not need to understand the programming language or the pecularities of the testing hardware if the test block is properly written. However, the test block concept exacts a price - slightly less efficient test programs. It may be necessary to duplicate some measurements with the multiple test block approach. Also a small price is paid in the packing density of the final program. These problems appear anytime a "standard cell" approach is used. The advantages far outweigh the disadvantages since the primary price is paid in CPU time, and not in actual measurement time.

Any given device will have a *family* of test blocks that can be used. This family will generally consist of three basic parts:

- The most complete, general test for the structure. This part is complete in the sense that all of the features of first-order interest are included; it is impossible to unite a complete test program for any structure. This part would normally be used when very little experience has been obtained on the process or structure, and maximum confidence is needed. This version is very expensive in terms of testing time and, in general, is not suitable for production use.

- A version suitable for production testing is less complete but includes essential data fault protection.

- An "idiot" version wherein a measurement is blindly made without protection.

We have attempted to provide the most complete general test for those structures which have been tested automatically and to provide a list of the less general versions. Examples of this can be found in the "detailed descriptions" in section 3. If a user is not satisfied with any of the versions in the existing library, he should write his own.

The ability to "chain" test blocks together provides the possibility of using the results from previous test blocks to specify the stimuli in the current test block. It also provides the ability to skip a section based on the results of a previous test

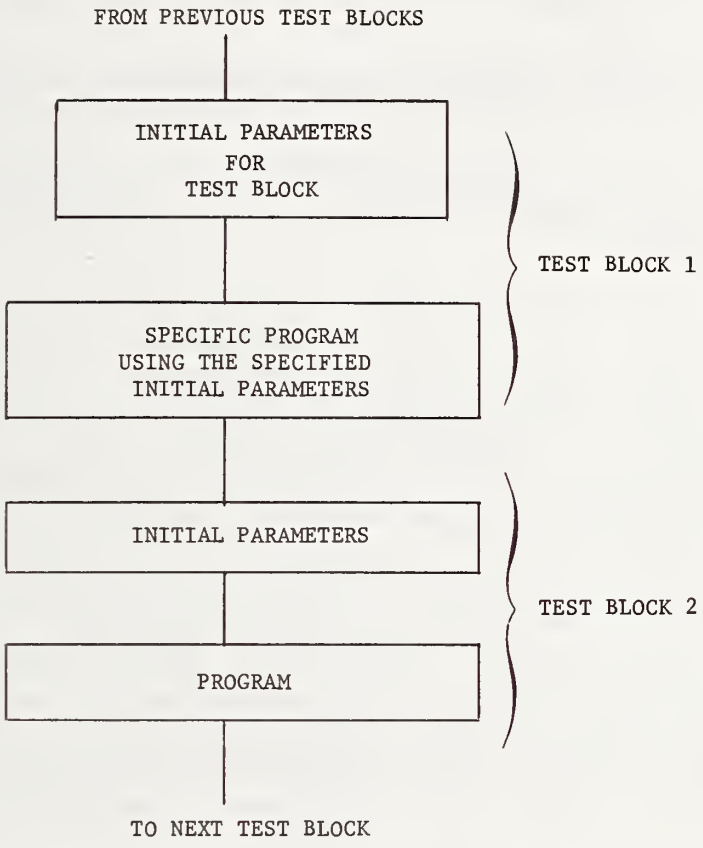


Figure 3. Organization of master test program using test blocks.

block. There is also a class of test blocks which applies to structures with a variable number of access points such as a multi-terminal gate structure. The following four classifications of test blocks have been identified:

- Self-contained
- Needs results from previous tests to specify stimuli
- Sends control to other blocks based on results
- Needs specifications of a variable number of electrical access points.

Below is a list of some features of the test program creation scheme.

- Provides ability to respond to different stimulus requirements and electrical access points quickly and with confidence
- Creation of basic test block must be done *before* requirements to use exists
- Test blocks contain basic measurement commands and test sequences such that *standardized* measurement techniques are *guaranteed* to be used. Stimuli levels are variable

- Test program *documentation* is completely specified by the parameter list used for the test block

- Test blocks are assembled into a master production test program

Many examples of the use of programs created by this method are distributed throughout this volume. They have been very satisfactory and have produced large savings in programming time.

Some details of execution methods and of some of the data documentation methods which are useful in the actual testing are discussed in section 4. Other examples are distributed throughout section 3.

1.6 Documentation Methods and Report Organization

As evidenced by the volume of this report, documentation of a pattern of this type is far from trivial. The most important factor is the number of structures. Section 3, by far the most lengthy, provides a detailed description of each structure on the vehicle. The only real innovation in this section besides creating the organization is the use of the multicolor computer-drawn check plots as the basis for the line drawings. These line drawings reduce the drafting costs by at least a factor of two. Unfortunately maintaining the colors in a form suitable for mass production is not economical and a black and white photograph of the multicolored drawings was used as the basic drawing. These drawings were then labeled by their mask level for those lines whose identification was not reasonably clear. The documentation of each of the descriptions constitutes a relatively complete and self-contained report of the structures of the description.

Sections 2, 4, and the appendices are much less voluminous. Section 2 describes the gross features of the vehicle including the layout, electrical access schemes, possible processes which could be used, and the placement of individual structures. Section 4 considers some details of testing methods and discusses the results of using the vehicle on a small test sample of wafers. The appendices describe the mask levels, the electrical access patterns which can be used, some spinoff patterns which have resulted from the main pattern, and a cross reference list for quickly locating a structure for a particular purpose.

2. PATTERN DOCUMENTATION

2.1 General Considerations

a. Layout

The test pattern is partitioned into five main sections. Each section has one or more specific classes of devices. Briefly, these sections are:

Type I - General Purpose: Many different test structures with nominal dimensions.

Type II - Spatial Integrity: A few high-information-density structures, closely spaced.

Type III - Geometrical Variations: Several important test structures with widely different geometries.

Type IV - Redundancy: Several important test structures connected in series or in parallel for simultaneous testing.

Type V - Optical, Circuit Building Block, and Dynamic: Test structures for measuring the characteristics of the lithographic technology, the characteristic of circuit building blocks, and the dynamic operation of simple building block connections.

Each main section is designed to be tested independently from every other section. Each section is laid out so that the structures primarily intended to be tested automatically are located on the *periphery* of the section. Those structures which are not of primary interest for automatic probing but which may be tested automatically are located within the periphery in such a way that they can be automatically probed. Structures intended for manual probing are located at arbitrary positions within the periphery.

These five types are integrated into a square pattern 258 mil on a side as illustrated in figure 4. A photomicrograph of the entire chip is shown in figure 5. An entire wafer containing only the chip is shown in figure 6.

b. Electrical Access

(1) Pad Design. Pads are an extremely important part of any electrical/test structure. They are in series with the device and all electrical information passes through the pads. It is therefore beneficial to make the pads as forgiving as possible. One method which eliminates many problems in probing is to make the pads as large as possible. In some cases, pads up to 30 mil on a side have been used. In general, if the pads are smaller than the typically used size in an actual circuit, they will place constraints on testing the test device which do not exist for testing the circuit. This factor alone can provide a built-in bias against testing the test device. A large pad also minimizes problems from conductors running close to the pad edge. A probe making suitable contact to the pad may also make suitable (but undesirable) contact to the conductor.

On the other hand, there are at least two reasons for making the pads as small as possible. Shrinking the pad size decreases the space required for the test structure. It also decreases the possibility that a pinhole in the oxide under the pad (for pads over silicon, which is supposed to be isolated from the pad) will cause a short-circuit. The area of metal damaged by the probe is usually independent of the pad size.

For silicon-on-sapphire (and, usually, for bulk silicon) the pad size for the test devices should be at least as large as the circuit pads which are conventionally 4 mil on a side. The only reason for using a smaller pad would be lack of space. A very few exceptions to the 4-mil pad are found throughout the pattern. In general, shrinking the pad size is very poor economy if there is *any* reasonable chance that the shrinking will cause a question concerning proper contact. Many times probing would have been very difficult (particularly automatic probing) if the pads had been smaller than 4 mil. These difficulties are usually caused by nonideal X-Y tables, probe cards, and probes. Although the

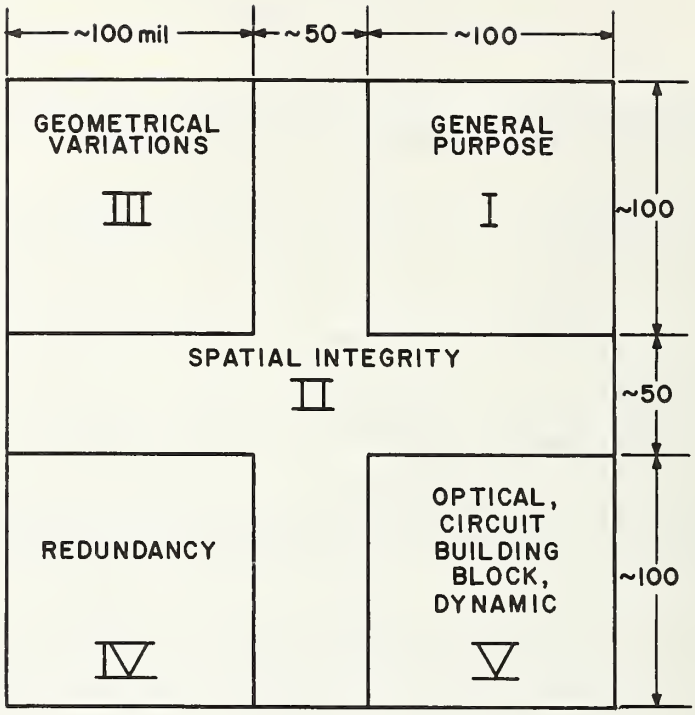


Figure 4. Layout of types.

specifications of these items may indicate that smaller pads are possible to probe, the fact remains that the difference between a valid measurement and a poor measurement or between a measurement and no measurement at all may be due to a pad that could have been made larger (or should not have been shrunk). Frequently, test devices on circuit perimeters are made with smaller pads than those in the circuit when it would have caused no difficulty to enlarge them. *Small pads are poor economy.*

For SOS, the pads are diffused, the edges are covered with SiO_2, and the metal (Al) makes intimate contact with the diffused silicon. This design ensures that the aluminum will not be scraped off the pad during probing or bonding, and that good step coverage is obtained. This procedure also allows for many probings to be made to the same pad without a problem. Typically, pads of this type can be probed 50 or more times without failure. This design is unsatisfactory for some bulk silicon processes unless substrate contact is desired. Polysilicon can be used on top of field oxide as the diffused silicon for some bulk processes. Figure 7 illustrates the essential features of the pad design. The contact edges are nominally 0.1 mil from the silicon edge.

Since the primary function of the pads is to provide electrical contact through probes, criteria for wire bonding need not be considered. Therefore, a pad-to-pad center spacing of 6.0 mil (152 μm) was chosen. This allows nearly twice as many pads per unit area as the 8.0-mil centers commonly used when wire bonding is needed. Metal lines are allowed to approach the edge of the pad to 0.3 mil (7.6 μm), if necessary. A wider spacing is desirable and is used where possible.

(2) Pad Classification. Five different classifications of pads have been created. The classification depends mainly on the type of electrical testing to be used.

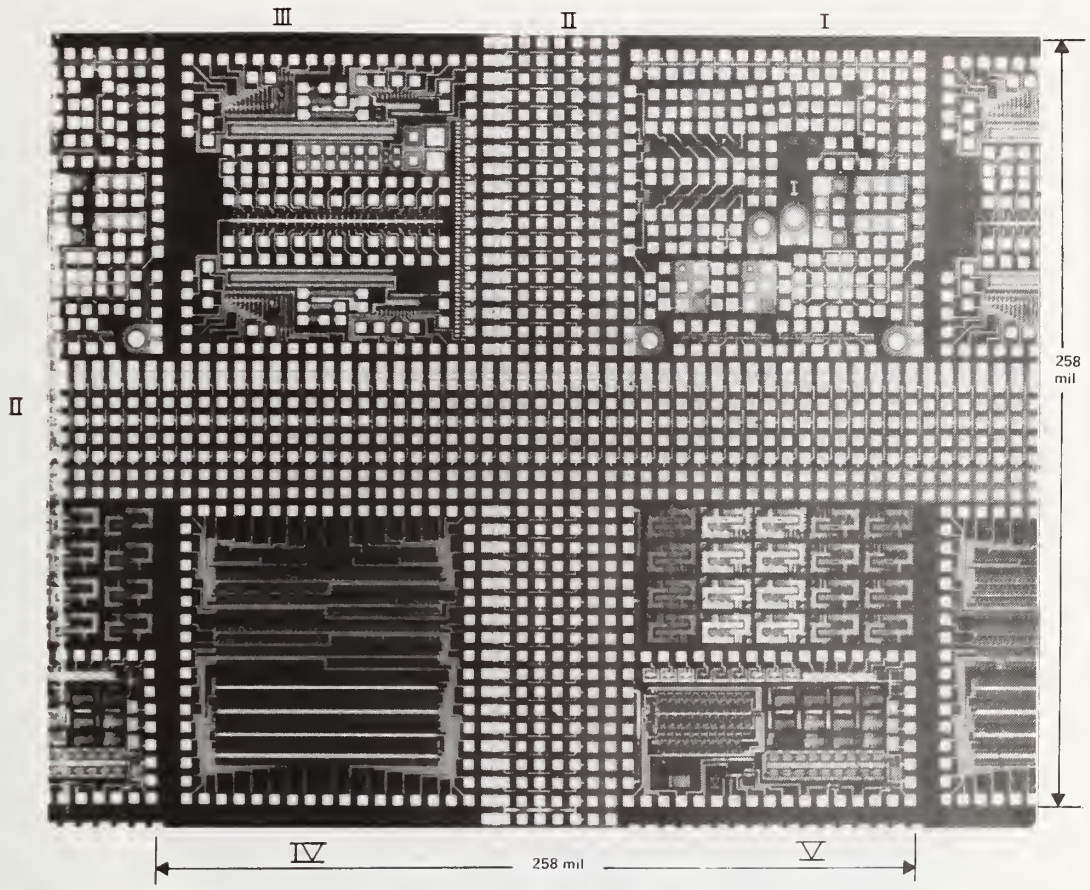


Figure 5. Complete pattern.

Type A: These pads are found on the periphery of the quadrant for types I, III, IV, and V. Access through commercially available probe cards is possible, and these pads would be expected to be used frequently. A minimum size of 4.0 mil is used for type A pads. Type II patterns use exclusively type A pads.

Type B: These pads are found near or on the periphery of the quadrants and may be accessed through commercially available probe cards. They are available for use if needed but regular use is not anticipated.

Type C: These pads are found in the interior sections of the quadrants and are intended to be used only with manual probing from micromanipulators. They may have any size which may be easily probed. A minimum size of 1.0 mil (25.4 μm) is used.

Type D: These pads are larger than the others and are intended for use where manual probe contact under wide temperature variations is contemplated. The larger size may be needed to maintain probe contact as the wafer heats and cools. This type pad is also useful for Kelvin probing. The current version of the pattern does not use this type of pad.

Type E: These pads are a subdivision of type C pads except that they belong to test structures which are not normally used. The most obscure positions are suitable for these pads.

More than one classification may apply to certain pads, but usually one suffices.

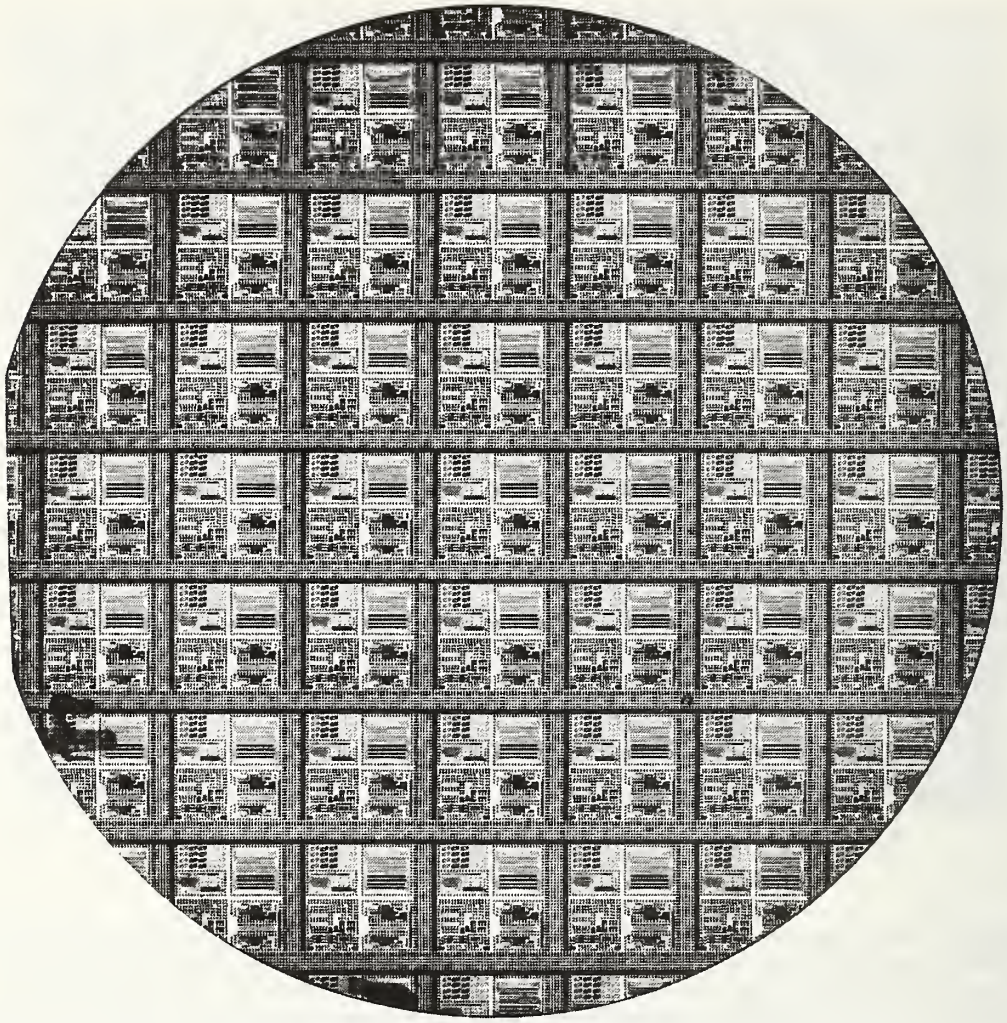


Figure 6. A 2-in.-diameter wafer containing the vehicle shown in figures 4 and 5. Step and repeat distance is 258 x 258 mil.

c. Mask Levels

(1) SOS Silicon-Gate Single Epitaxial Type CMOS Process. One possible CMOS/SOS process involves the use of only one type of silicon [10]. This process makes use of a device that is unique to SOS type technologies for providing either the n- or p-channel transistor for CMOS circuits. The device is a junctionless transistor formed from silicon of the same type as the source and drain, and is sometimes inappropriately called a deep-depletion transistor. The key to the successful operation of this device is that the silicon can be completely depleted throughout, and low minimum currents are thereby obtained. The operation of this device is otherwise very similar to that of MOS transistors with junctions. With the junctionless device a CMOS technology can be implemented with only a single epitaxial layer.

10. Heiman, F. P., "Thin-Film Silicon-on-Sapphire Deep Depletion MOS Transistors," IEEE Trans. Electron. Devices ED-13, No. 12, 855-862 (1966).

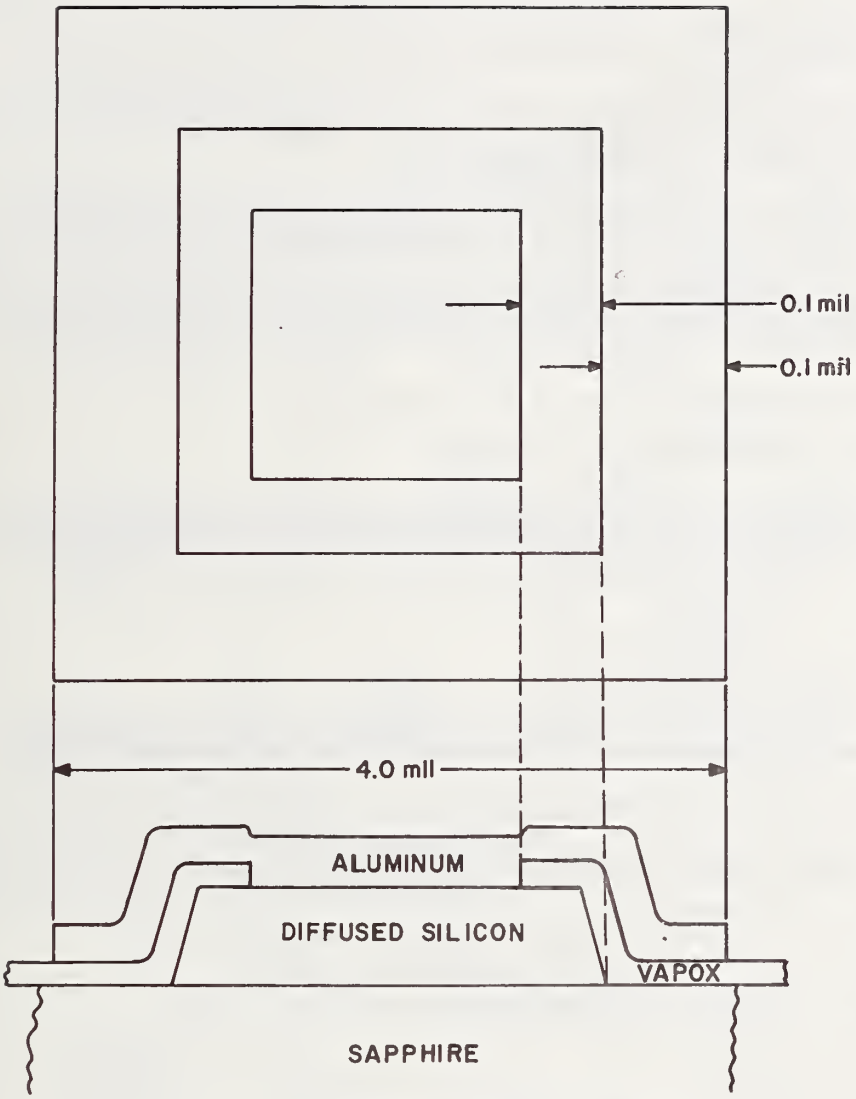


Figure 7. Pad design (not to scale).

In this process, the transistors can be one of four types: p+np+, p+pp+, n+nn+, n+pn+. The conventional definition of device type is that an enhancement mode is formed when the silicon between the heavily doped regions is of opposite type to that of the heavily doped regions. A deep-depletion device [10] is formed when the material is of the same type (n+nn+ or p+pp+). The electrical behavior of these devices depends much more strongly on the type of the heavily doped regions than on the type of the lightly doped regions. In fact it is sometime difficult to tell the difference between n+nn+ devices and n+pn+ devices. Therefore, consider mainly channel (or contact) type rather than distinguishing between enhancement and depletion mode. The channel is field-induced by the gate potential and exists mainly in the part of the device immediately below the gate dielectric. If positive charge is induced, a high lateral current can be obtained only with p+ heavily doped regions. If negative charge is induced, a high current can be obtained only with n+ heavily doped regions. Therefore, n+ heavily doped regions (also called sources and/or drains) *imply* an n-channel device and p+ heavily doped regions *imply* a p-channel device. A typical layout of a transistor is shown in figure 137.

The lightly doped regions for both channel types are the same type of silicon in this process. Therefore, p+np+ and n+nn+ devices are formed if the silicon is n type and p+pp+ and n+pn+ devices are formed if the silicon is p type. The processing sequence and channel types are not affected by the type of the starting silicon. Therefore, the

type of epitaxial silicon being used is not specified in the drawings, it being understood that it is always the same type on any given wafer.

For purposes of identifying the masking levels and describing the test structures, it is helpful to have a specific process in mind. The documentation to follow uses a single epitaxial process which is described below.

This process is not necessarily the recommended process, nor is it particularly unique or unusual. Many other processes using different diffusion sources, ion implantation, gate materials, island formation techniques, etc are also compatible with these masks. The semiconductor could be any of the known semiconductors including GaAs and Ge. A complete list of possible processes is not practical to produce. (The actual masks are shown in Appendix A.)

The process proceeds according to the following steps:

(1) Define epi islands (mask level 1)

* A mask level 2 is sometimes useful at this stage as described in non-junctionless processing below. It is not used in this process but the number 2 is preserved.

(2) Grow channel oxide ($\sim$1100 Å)

(3) Deposit polysilicon (5000 Å)

(4) Diffuse polysilicon (p+)

(5) Define poly (mask level 3)

(6) Etch channel oxide (self-aligned)

(7) Deposit p+ diffusion source or p+ diffusion mask

(8) Define (7) (mask level 4)

(9) Deposit p+ diffusion source or perform n+ diffusion

(10) Open contact holes (mask level 5)

(11) Deposit aluminum

(12) Define aluminum (mask level 6)

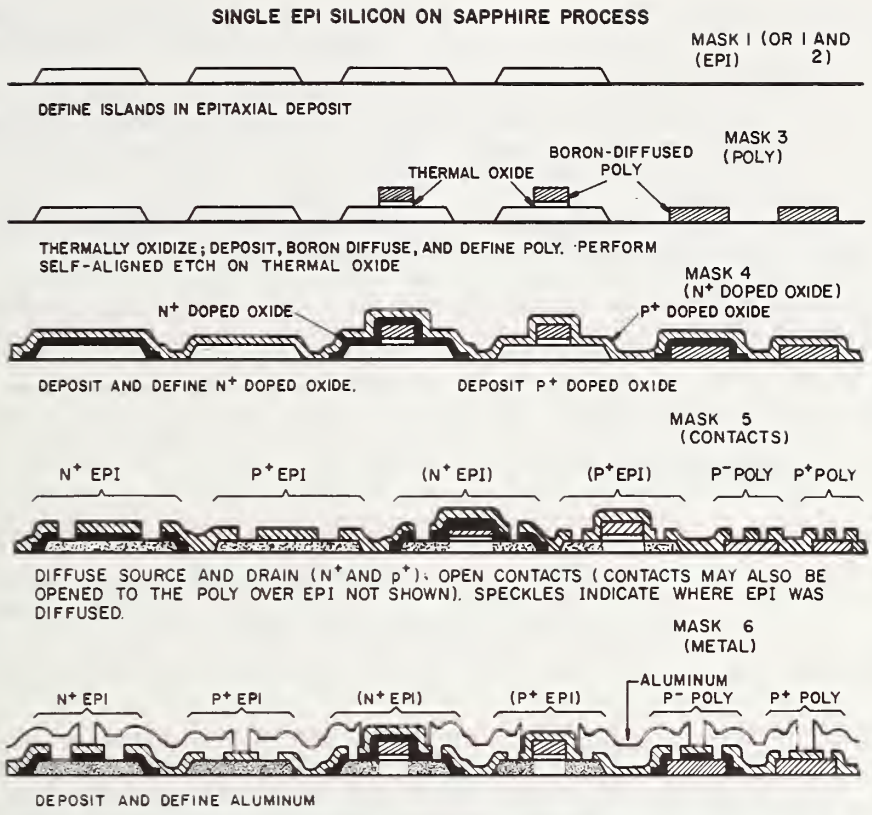
(13) Deposit SiO_2 overcoat (optional)

(14) Open overcoat (OC) (mask level 7)

This specific process (which was used for the test structures which were fabricated to test the mask set) is illustrated in figure 8. Note that all silicon epi which is not covered by polysilicon will be either p+ or n+. Space is allowed, however, for devices that are not limited by the restrictions of this process. This will be discussed later in the detailed descriptions as needed. Note also that one of the transistors will always be of the deep-depletion type in this process. If the epi is n type, the n-channel transistor is deep depletion; if the epi is p type, the p-channel transistor is deep depletion. If all four possible types of device are desired, two wafers are needed - one with n type epi and the other with p type epi. No process currently used has both enhancement mode and junctionless devices of the same channel type on the same wafer.

A code has been adopted for creating cross-sectional views of the structures in conjunction with the above process and is shown in Table 2.

Epi silicon under the n+ oxide will be n+ and epi silicon under p+ oxide will be p+. The polysilicon is doped twice - once during its original definition (using the etch-resistant properties of boron-doped silicon) and once during the source-drain diffusion.



(N+ EPI) denotes epi which is under the poly gate where an n+ region exists at the gate edge. This structure is also an n-channel device.
(P+ EPI) denotes epi which is under the poly gate where a p+ region exists at the gate edge. This structure is also a p-channel device.

Figure 8. Single epi silicon-on-sapphire process.

TABLE 2. CODE USED IN CROSS-SECTIONAL DRAWINGS

MASK LEVEL NUMBER	CODE	NAME
	Doping: Light / Heavy	
1		Epi
2	None	Epi #2 or counterdoping see text
3		Poly
4		n^+ Oxide (An SiO_2 layer containing atoms that dope silicon n type)
None		p^+ Oxide (An SiO_2 layer containing atoms that dope silicon p type)
5	None	Contact
6		Metal
7		Passivation or OC (overcoat) Not shown above

The cross-sectional views do not distinguish between the doping type of the silicon, it being understood that if p+ oxide is in contact with the epi silicon it will be p+ and that if n+ oxide is in contact with the epi silicon it will be n+.

Since the poly is first doped heavily with boron, it will remain p+ throughout the process. During the source-drain diffusion, however, some additional p dopant is introduced from the p+ oxide and some compensating dopant is introduced from the n+ oxide. Therefore, two kinds of poly are produced. The poly under the p+ oxide is denoted p+ poly while that under the n+ oxide is denoted p- poly in order to distinguish it from the poly under the p+ oxide. Both kinds of poly are in fact heavily doped p type.

Since the lightly doped epi silicon can occur only under the poly and the type of this silicon is irrelevant to the test structure, the following notation is used to identify the epi regions:

(n+ epi) is epi under p- poly

(p+ epi) is epi under p+ poly

Usually (n+ epi) is associated with an n-channel device and (p+ epi) is associated with a p-channel device. In some structures both (n+ epi) and (p+ epi) exist in the same device. Immediately above any regions of (n+ epi) or (p+ epi) a channel dielectric (SiO_2 in figure 8) will exist. This is denoted by a thin clear space between the epi and the poly.

A composite set of cross sections showing various stages of forming the final structure is shown in figure 8.

(2) Non-Junctionless Processing. Note that in the single epitaxial type processing mask level 2 is not mentioned. This level allows formation of devices from either type of starting material and allows elimination of the deep-depletion or junctionless device if desired. One can also form both channel types as junctionless devices if desired. The precise use of this mask depends on the method used to create the two types of material.

In one method, this second level is used for definition of a second epitaxial layer of type opposite from the first. This method requires a compatible first level. In another method, the second level is used as an ion-implantation mask. The same first level as used for the single epi process can be used here. For most structures mask level 4 can be used as the ion-implantation mask and will serve as level 2. A specific level 2 mask does not currently exist for non-ion-implanted processes. The number 2 is preserved, however, since a masking function may be needed at this stage of the process.

(3) Gate Metallization. Precisely the same layout can be used for non-refractory metal-gate processes. In these processes the channel regions are not defined by the gate metallization. Slight modifications in all mask levels after the second are required to use these masks for metal-gate processes. Space is allowed for certain metal-gate structures which are not possible with self-aligned gates.

(4) Application to Bulk Silicon Process. A great deal of duality exists between SOS and bulk CMOS processes. Since the bulk devices use holes in the field oxide where SOS uses silicon islands, largely the same layout can be used for both SOS and bulk. Duality exists between the SOS epi layers and the "well" and undiffused bulk starting material. In the simplest case, the test vehicle is used with whole wafers of undiffused starting material and other whole wafers which have received the doping process for the "well" region. This is analogous to using only a single type of starting epi silicon in the SOS process. Of course, the deep-depletion device will not exist on the bulk silicon. Certain additional structures for testing field oxides, "well" junctions, or other items peculiar to bulk silicon CMOS could be implemented in presently unassigned space. These masks have been used for some limited bulk silicon work which will not be described here.

(5) Partial Processing. If only a part of a process is of interest, it may not be necessary to use all of the mask levels. For example, the overcoat is frequently omitted. In another case where only properties of diffused layers are important only one mask level to define the silicon after the diffusion may be necessary. If only one type of device

(i.e., n channel or p channel) is of interest, level 4 may be omitted. Other specific situations may not require all of the levels.

It must, of course, be recognized in the interpretation of the results that *an incomplete process* has been used if all the mask levels are not used.

d. Dimensions

Many test structures included are intended to test for phenomena in devices characteristic of a certain size. The "typical" dimensions considered may vary, depending on the exact photolithographic capabilities or other criteria such as maximum potential to be applied (punchthrough, etc). Although a section of the test pattern is devoted to considering the optimum sizes for specific applications, some standard dimensions must be chosen for application to specialized individual structures. For the particular SOS process considered here, the typical transistor gate length is 0.3 mil (7.6 μm). (Metric equivalents are not given in certain cases since the test vehicle was produced in English units, which is a common industrial practice.) The minimum *typical* size contact hole is 0.3 mil x 0.3 mil and the typical epi island is 0.6 mil (15.2 μm). These dimensions can be adjusted in different mask sets so that the particular process of current interest can be characterized. The following three classes of dimension have therefore evolved:

- Fixed (F) - normally no change
- Variable (V) - may change by a relatively small amount
- Variable (H) - may change position with respect to other lines or edges.

Of course, large changes in dimensions are not allowed since they would, in general, necessitate changes in layout. Most lines and edges are of the H category. Lines are designated only by (V) on the drawings - unlabeled lines are either (F) or (H). Typically, the only (F) lines are those defining the type A and type B pads since fixed probe cards exist to access these pads.

2.2 Detailed Description of Pattern

a. Type I Pattern

(1) Purpose. The type I pattern is intended to provide a comprehensive collection of individual structures of typical dimensions. These individual structures are primarily useful as electrically accessible devices. At least one of every normally used combination of *components* is attempted.

(2) List of Structures. See figure 8 and table 2 for definitions of terms.

Test Structure Number	Name	Discussion Section	Page No.
I-1	p-Channel MOS transistor; edgeless Purpose: measure transistor parameters on simplest transistor structure	3.1	51
I-2	n-Channel MOS transistor; edgeless Purpose: as I-1	3.1	51
I-3	Gate-controlled diode; edgeless Purpose: measure p-n junction properties on simplest junction structure	3.1	51
I-4	n^+p^+ diode; edgeless Purpose: measure zener properties on simplest structure	3.1	51
I-5	Gate-controlled bridge resistor; n^+ contacts Purpose: measure epi resistance under controlled surface conditions	3.2	79

Test Structure Number	Name	Discussion Section	Page No.
I-6	Gate-controlled bridge resistor; p^+ contact Purpose: as I-5	3.2	79
I-7	Crossover; Al over n^+ epi crossover Purpose: measure continuity, resistance, capacitance, and dielectric strength of two levels of conductors separated by a dielectric	3.3	89
I-8	Crossover; Al over p^+ epi Purpose: as I-7	3.3	89
I-9	Crossover; Al over p^- poly Purpose: as I-7	3.3	89
I-10	Crossover; p^- poly over (n^+ epi) Purpose: as I-7	3.3	89
I-11	Crossover; Al over p^+ poly Purpose: as I-7	3.3	89
I-12	Crossover; p^- poly over (p^+ epi) Purpose: as I-7	3.3	89
I-13	Crossover; p^+ poly over (n^+ epi) Purpose: as I-7	3.3	89
I-14	Crossover; p^+ poly over (p^+ epi) Purpose: as I-7	3.3	89
I-15	MOS capacitor; p^- poly on (n^+ epi) Purpose: measure parameters derivable from MOS capacitor measurements such as dielectric thickness, interface charge, dielectric strength, and doping density	3.4	101
I-16	MOS capacitor; Al on n^+ epi - edge mostly Purpose: measure dielectric strength and thickness of deposited doped oxide and possibly indicate doping level of diffusion	3.5	101
I-17	MOS capacitor; Al on n^+ epi corner Purpose: geometrical variation on I-16	3.5	101
I-18	MOS capacitor; Al on n^+ epi top only Purpose: as I-17	3.5	101
I-19	MOS capacitor; Al on n^+ epi top mostly but crossing edge Purpose: as I-17	3.5	101
I-20	MOS capacitor; p^- poly on (n^+ epi) top only Purpose: geometrical variation on I-15	3.4	101
I-21	MOS capacitor; p^- poly on (n^+ epi) top only - *small* Purpose: as I-20	3.4	101
I-22	MOS capacitor; p^- poly on (n^+ epi) edge Purpose: as I-20	3.4	101
I-23	MOS capacitor; p^- poly on (n^+ epi) corner Purpose: as I-20	3.4	101

Test Structure Number	Name	Discussion Section	Page No.
I-24	MOS capacitor; p^+ poly on (p^+ epi) top mostly but crossing edge Purpose: as I-15	3.4	101
I-25	MOS capacitor; Al on p^+ epi edge mostly Purpose: as I-16	3.5	101
I-26	MOS capacitor; Al on p^+ epi corner Purpose: as I-17	3.5	101
I-27	MOS capacitor; Al on p^+ epi top only Purpose: as I-17	3.5	101
I-28	MOS capacitor; Al on p^+ epi top mostly but crossing edge Purpose: as I-17	3.5	101
I-29	MOS capacitor; p^+ poly on (p^+ epi) top only Purpose: as I-20	3.4	101
I-30	MOS capacitor; p^+ poly on (p^+ epi) top only - *small* Purpose: as I-20	3.4	101
I-31	MOS capacitor; p^+ poly on (p^+ epi) edge Purpose: as I-20	3.4	101
I-32	MOS capacitor; p^+ poly on (p^+ epi) corner Purpose: as I-20	3.4	101
I-33	MOS capacitor; Al on p^+ poly top only Purpose: as I-16	3.7	113
I-34	MOS capacitor; Al on p^+ poly top mostly but crossing edge Purpose: geometrical variation of I-33	3.7	113
I-35	MOS capacitor; Al on p^+ poly edge Purpose: as I-34	3.7	113
I-36	MOS capacitor; Al on p^+ poly corner Purpose: as I-34	3.7	113
I-37	MOS capacitor; Al on p^- poly top only Purpose: as I-16	3.7	113
I-38	MOS capacitor; Al on p^- poly top mostly but crossing edge Purpose: as I-34	3.7	113
I-39	MOS capacitor: Al on p^- poly edge Purpose: as I-34	3.7	113
I-40	MOS capacitor; Al on p^- poly corner Purpose: as I-34	3.7	113
I-41	MOS capacitor; poly on (epi) - 2 sided - top mostly Purpose: as I-15 except low-frequency type C-V curves as obtained	3.6	111
I-42	MOS capacitor; poly on (epi) - 2 sided - top only Purpose: geometrical variation of I-41	3.6	111

Test Structure Number	Name	Discussion Section	Page No.
I-43	MOS capacitor; same as I-42 } for Purpose: as I-42	3.6	111
I-44	MOS capacitor; same as I-41 } double- Purpose: as I-41 } epi processes		
I-45	Metal VDP (Van der Pauw) Purpose: measure metal resistivity	3.8	118
I-46	Floating-gate VDP; p^+ contacts Purpose: measure gate potential - primarily Al-gate structure	3.10	141
I-47	Floating-gate VDP; n^+ contacts Purpose: as I-46	3.10	141
I-48	Gate-controlled VDP; p^+ contacts Purpose: geometrical variation of I-6	3.9	135
I-49	Gate-controlled VDP; n^+ contacts Purpose: geometrical variation of I-5	3.9	135
I-50	p^+ Epi VDP Purpose: measure resistivity and Hall coefficient	3.8	118
I-51	n^+ Poly VDP Purpose: as I-50	3.8	118
I-52	n^+ Epi VDP Purpose: as I-50	3.8	118
I-53	p^+ Poly VDP Purpose: as I-50	3.8	118
I-54	Bridge resistor for p epi; ungated Purpose: measure resistivity or Hall coefficient - for Al-gate processes	3.11	143
I-55	Bridge resistor for n epi; ungated Purpose: as I-54	3.11	143
I-56	n^+ Epi contact test Purpose: measure effect of contacts on diffused resistor	3.12	150
I-57	n^+ Epi sheet resistance Purpose: measure sheet resistance of diffused layer	3.11	143
I-58	p^+ Epi contact test Purpose: as I-56	3.12	150
I-59	p^+ Epi sheet resistance Purpose: as I-57	3.11	143
I-60	p^- Poly contact test Purpose: as I-56	3.12	150
I-61	p^- Poly contact test Purpose: as I-57	3.11	143
I-62	p^+ Poly contact test Purpose: as I-56	3.12	150
I-63	p^+ Poly sheet resistance Purpose: as I-57	3.11	143

Test Structure Number	Name	Discussion Section	Page No.
I-64	n-Channel MOS transistor with substrate contact (narrow channel) Purpose: measure effects of substrate potential on MOS transistors	3.16	163
I-65	p-Channel MOS transistor with substrate contact (narrow channel) Purpose: as I-64	3.16	163
I-66	n-Channel MOS transistor with grounded substrate - design 1 Purpose: as I-64	3.17	163
I-67	n-Channel MOS transistor with grounded substrate - design 2 Purpose: as I-64	3.17	163
I-68	p-Channel MOS transistor with grounded substrate - design 1 Purpose: as I-64	3.17	163
I-69	p-Channel MOS transistor with grounded substrate - design 2 Purpose: as I-64	3.17	163
I-70	n-Channel MOS transistor; ordinary Purpose: measure parameters derivable from MOS transistor such as field-effect carrier mobility (see p. 82), threshold voltage, drain breakdown voltage	3.13	156
I-71	Non-channel effect test; n-channel MOS transistor Purpose: measure resistance without channel	3.14	156
I-72	n^+ Epi sheet resistance test on n-channel MOS transistor Purpose: measure diffused silicon contribution to transistor voltage drop	3.15	156
I-73	p-Channel MOS transistor; ordinary Purpose: as I-70	3.13	156
I-74	Non-channel effect; p-channel MOS transistor Purpose: as I-71	3.14	156
I-75	p^+ Epi sheet resistance test on p-channel MOS transistor Purpose: as I-72	3.15	156
I-76	n-Channel MOS transistors for life-radiation test Purpose: identical devices to be biased differently during testing	3.13	156
I-77	p-Channel MOS transistors for life-radiation test Purpose: as I-76	3.13	156
I-78	Continuity test; all connections Purpose: measure continuity through all types of connections	3.18	168
I-79	n^+np^+ Gate-controlled diode Purpose: goemetrical variation of I-3	3.19	172

Test Structure Number	Name	Discussion Section	Page No.
I-80	p^+nn^+ Gate-controlled diode Purpose: as I-79	3.19	172
I-81	n^+nn^+ Diode gate-controlled resistor Purpose: calibration structure for I-82, epi resistivity	3.20	172
I-82	n^+nn^+ With floating gate Purpose: measure floating-gate potential - also Al-gate structure	3.20	172
I-83	n^+p^+ Diode; no gate Purpose: zener breakdown voltage and leakage	3.20	172
I-84	p^+nn^+ Diode with floating gate Purpose: Al-gate structures	3.23	172
I-85	n^+p^+ Diode; metal gate Purpose: measure effect of gate potential on zener characteristics	3.22	172
I-86	n^+nn^+ Floating-gate device (Al-gate structure)	3.20	172
I-87	n^+nn^+ Floating-gate device (Al-gate structure)	3.20	172
I-88	p^+pn^+ Gate-controlled diode Purpose: as I-79 - for double-epi processes	3.19	172
I-89	n^+pp^+ Gate-controlled diode Purpose: as I-79 for douple-epi processes	3.19	172
I-90	p^+pp^+ Gate-controlled resistor Purpose: as I-81, calibration for I-91 - for double-epi processes	3.20	172
I-91	p^+pp^+ Diode with floating gate Purpose: as I-82, for Al-gate process - for double-epi processes	3.20	172
I-92	p^+n^+ Diode; no gate Purpose: as I-83	3.21	172
I-93	n^+pp^+ Diode with floating gate Purpose: as I-84 - for double-epi processes	3.23	172
I-94	n^+p^+ Diode with metal gate Purpose: as I-85	3.22	172
I-95	n^+pn^+ Floating-gate device Purpose: as I-86 ---- Al-gate structure	3.20	172
I-96	p^+pp^+ Floating-gate device Purpose: as I-87 ---- Al-gate structure		

for double-epi

Devices I-88 to I-96 are intended for double-epi processes wherein the silicon would be of the opposite type to that in devices I-79 through I-87. In the actual devices made, the same silicon material is used for devices I-79 through I-90. Therefore, only I-90 and I-91 are different from the devices I-79 to I-87.

(3) Device Locations. The locations of the type I test structures are shown in figure 9.

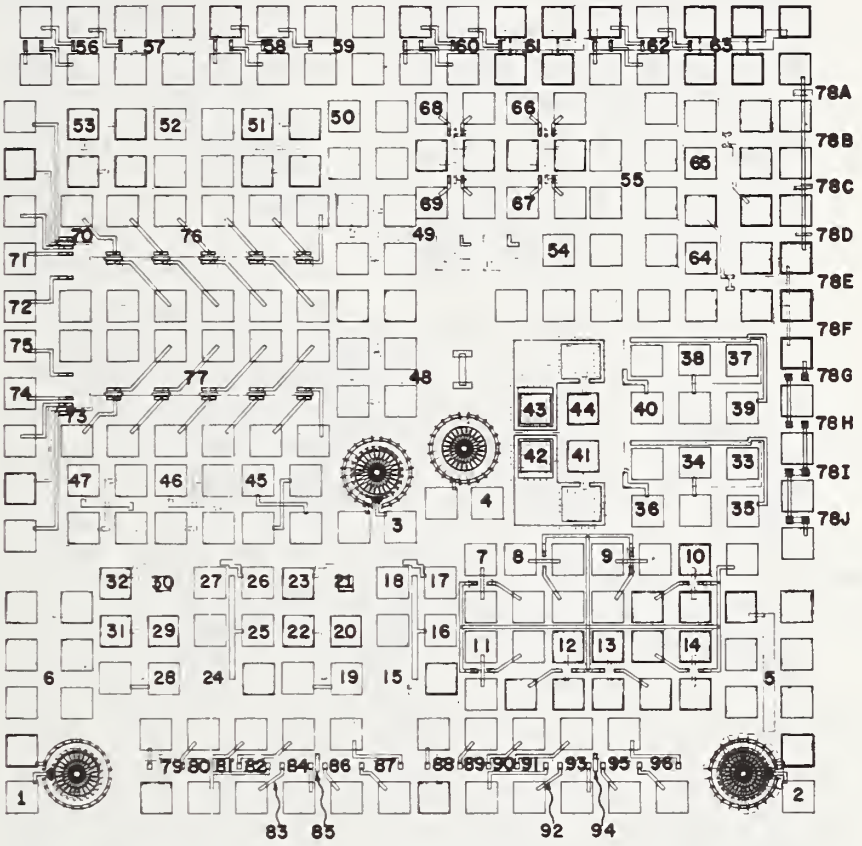


Figure 9. Test structure locations - type I.

(4) Pad Identification. For convenience in identifying electrical access points, each pad has been numbered as shown in figure 10.

(5) Pad Classification. Type I pad classification is shown in figure 11.

b. Type II Pattern

(1) Purpose. The purpose of the type II pattern is to provide information concerning how certain electrical parameters vary with small changes in position. The type II pattern consists of five devices: two capacitors, two MOS transistors, and a probe contact (resistance) test. Two capacitors are included to allow for the possibilities of two types of epi or to allow for the possibility of using two different schemes of diffusion on a single epi process. Two transistors are needed to provide information of relevance to CMOS processes. One transistor of each channel type is included. The probe contact test is also used as a coding test as described below. The entire element is approximately 6.0 x 42.0 mil.

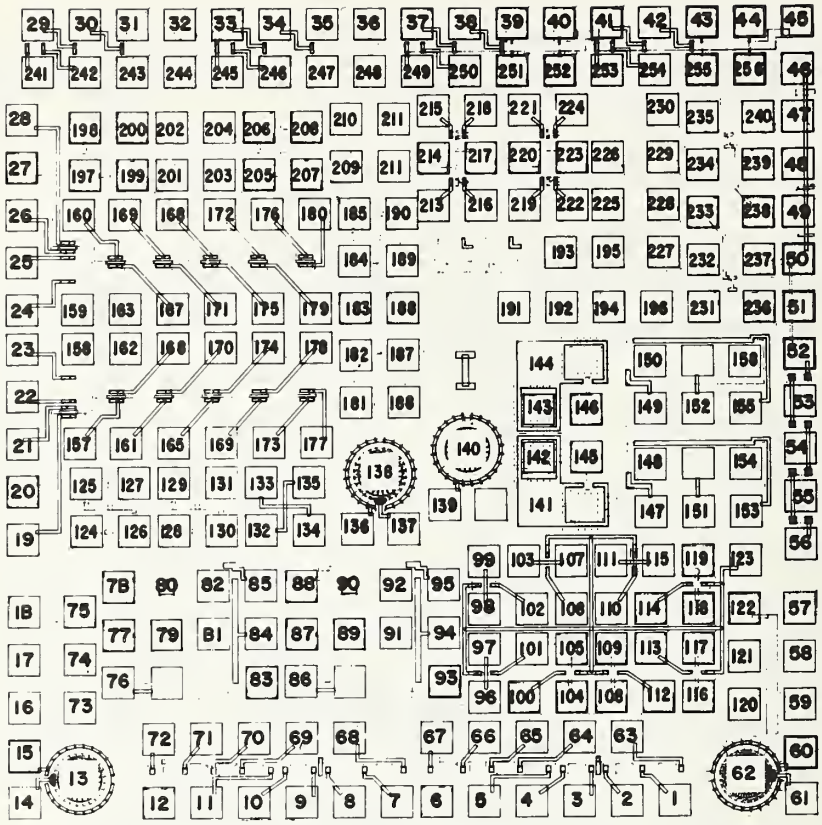


Figure 10. Pad identification - type I.

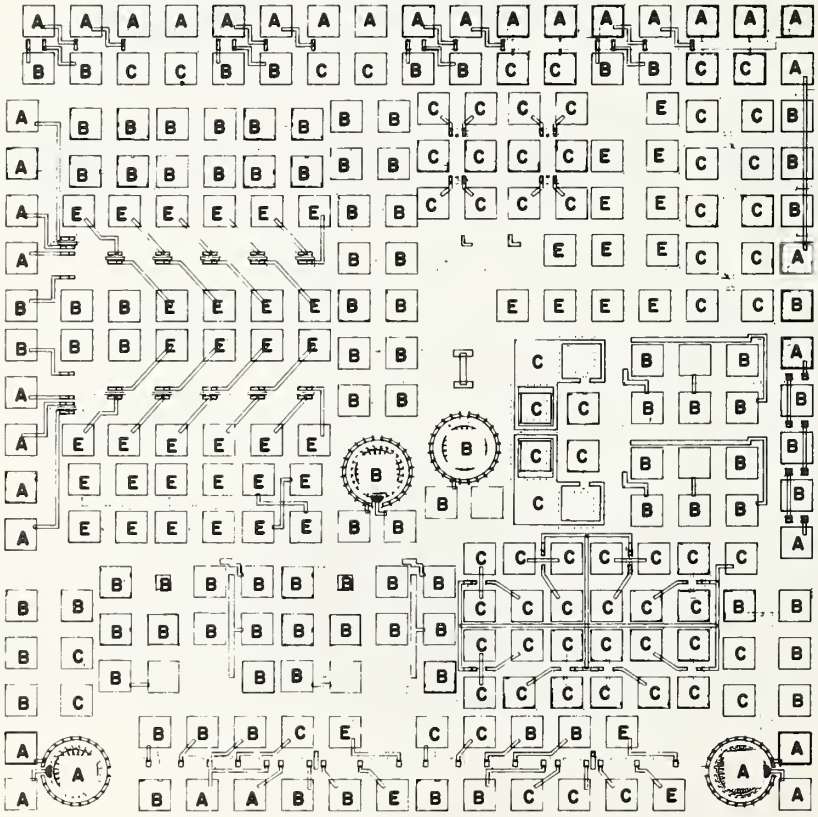


Figure 11. Pad classification - type I.

This type of pattern is intended to allow measurement at a local level of closely spaced identical devices. One basic question to answer is how far from the device being measured does the measurement apply? In particular, information regarding the significant parameters of the transistors and of the material is sought. Some of these parameters include:

- Gate dielectric strength
- Epi doping level
- $Si-SiO_2$ interface charges
- Gate dielectric thickness
- Transistor leakage current
- Epi resistivity
- Field effect mobility
- Transistor threshold voltage
- Transistor source-drain breakdown voltage

By spacing these identical devices as closely as possible, localized profiles of parametric values can be measured. The actual device spacing tested can be any multiple of 6.0 mil. The individual devices are then tested according to the particular information desired using the procedures suggested for the devices of the type I pattern.

The basic layout of this pattern is illustrated in figure 12. The "X" direction has continuous element-to-element registry. At the center of the "cross" the "Y" direction pattern is discontinuous at the intersection but the pads are in continuous registry. This allows automatic skipping of the devices in the intersection region when the "Y" direction pattern is being probed.

The first test is to measure the current produced when a predetermined voltage is applied to the probe contact test structure. If the probes are improperly placed, improperly adjusted, worn, or probing a "Y" direction element in the intersection, the measured current will not be sufficiently high. Under automatic control the wafer would be stepped to the next device. Under manual control the cause of the high contact resistance would be determined and removed. Therefore, continuous plots can be obtained only in the "X" direction, but protection against recording invalid data is built into the probing procedure.

(2) List of Structures.

Test Structure Number	Name	Dicussion Section	Page No.
II-1	MOS capacitor; single diffusion type Purpose: measure contact spatial integrity of parameters derivable from MOS capacitor measurement such as dielectric strength and thickness, interface charge, and doping density	3.24	195
II-2	MOS capacitor; double diffusion type Purpose: as II-1, except that low-frequency type C-V curves are obtained	3.25	195
II-3	n-Channel MOS transistor Purpose: measure spatial integrity of MOS transistor parameters	3.26	201

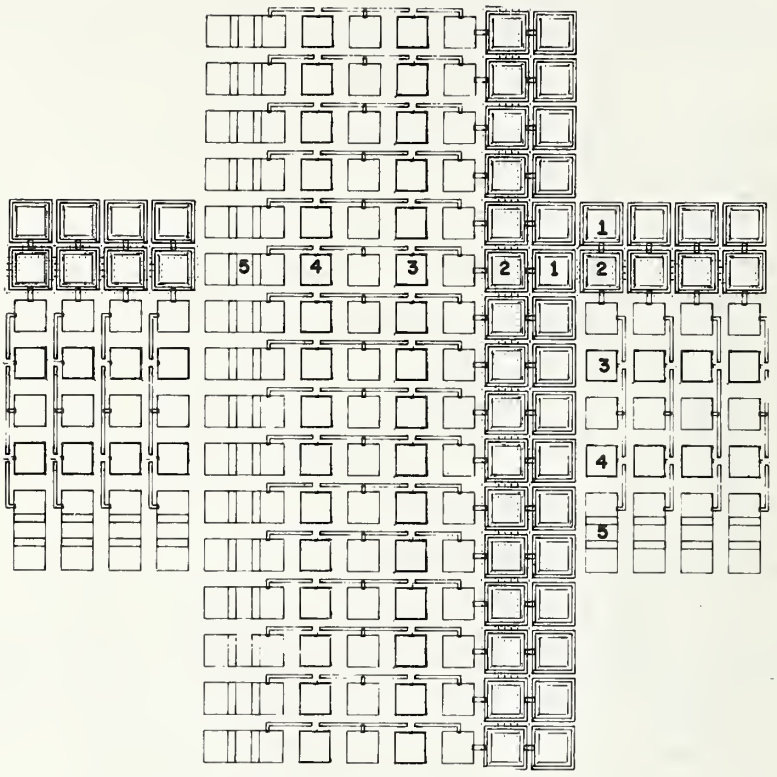


Figure 12. Device locations - type II.

Test Structure Number	Name	Discussion Section	Page No.
II-4	p-Channel MOS transistor Purpose: as II-3	3.26	201
II-5	Probe resistance test Purpose: measure variations in probe resistance across wafers and verify suitable contact	3.27	206

(3) Device Locations. The type II device locations are shown in figure 12.

(4) Pad Identification. Pad identification for type II is shown in figure 13.

(5) Pad Classification. Type II pad classification is shown in figure 14.

c. Type III Pattern

(1) Purpose. The type III pattern is intended to provide information concerning the effects of different geometrical features of certain selected test structures.

The devices in the type III pattern consist of MOS transistors, MOS capacitors, and contact resistance structures. The length, width, and orientation of critical dimensions vary. Due primarily to space limitations, other devices of obvious but usually second-order interest have not been included. Notably among these are conductors of various widths and separations (on flat surfaces and crossing steps) and bridge and van der Pauw structures of

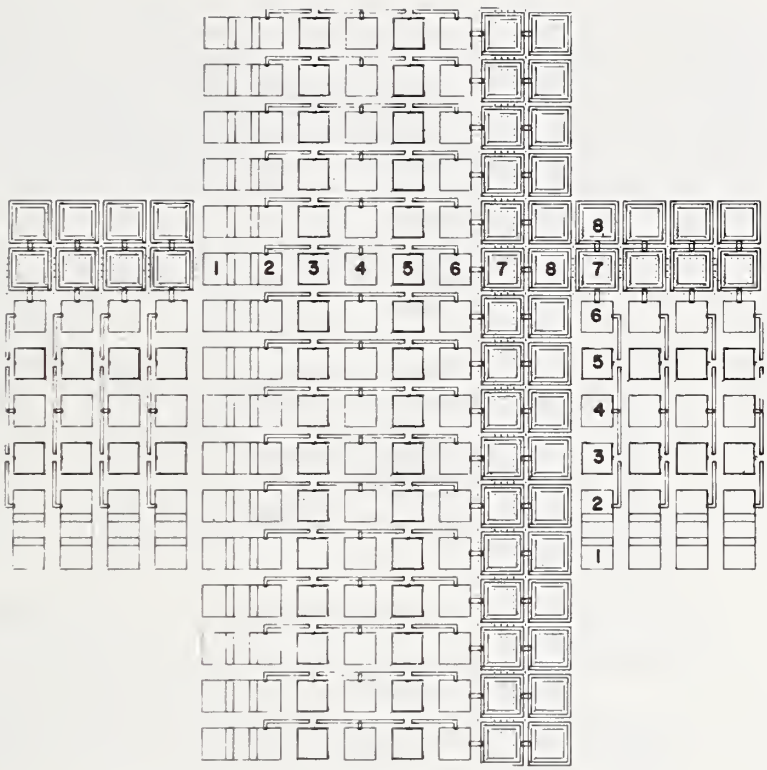


Figure 13. Pad identification - type II.

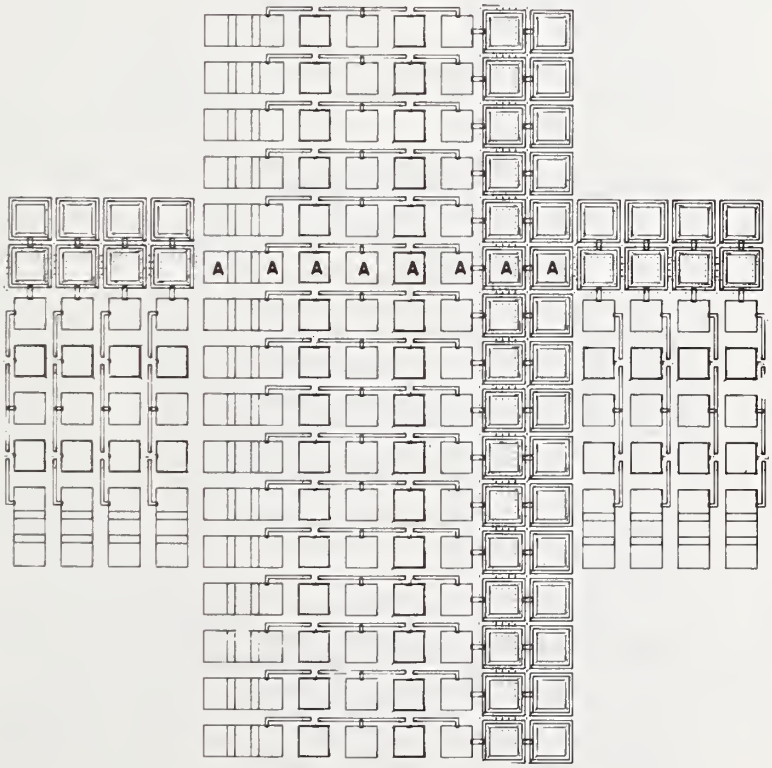


Figure 14. Pad classification - type II.

various sizes. The visual properties of all conductors of various sizes are available in the type V pattern (both on flat surfaces and crossing various steps). It may be appreciated from examining the type V pattern that this type of test requires many pads to perform the test properly and that the results can be predicted by visual observation in most cases. Open-circuits crossing a step because of step geometry are detectable in the type I pattern for all types of conductors and steps. The omission is therefore deliberate and does not substantially decrease the value of the pattern. Some examples of bridge patterns of various size exist in the type V pattern.

(2) List of Structures.

Test Structure Number	Name	Discussion Section	Page No.
III-1	n-Channel MOS transistors; variable channel length Purpose: measure effects of various channel lengths	3.28	210
III-2	p-Channel MOS transistors; variable channel length Purpose: as III-1	3.28	210
III-3	n-Channel MOS transistors; variable channel width Purpose: measure effects of various channel widths	3.28	210
III-4	p-Channel MOS transistor; very wide channel Purpose: typical output devices	3.30	210
III-5	p-Channel MOS transistor; variable channel width Purpose: as III-3	3.29	210
III-6	p-Channel MOS transistors; very wide channel Purpose: as III-4	3.30	210
III-7	n-Channel MOS transistors; variable channel length and width; edgeless Purpose: measure effects of different channel geometrics on edgeless MOS devices	3.31	210
III-8	p-Channel MOS transistors; variable channel length and width; edgeless Purpose: as III-7	3.31	210
III-9	n-Channel MOS transistors; variable orientation Purpose: measure effects of orientation on transistor characteristics	3.32	211
III-10	p-Channel MOS transistors; variable orientation Purpose: as III-9	3.32	211
III-11	MOS capacitors - gated resistor - n-channel; variable channel length Purpose: measure material properties and interface properties	3.33	220
III-12	MOS capacitor - gated resistor - p-channel; variable channel length Purpose: as III-11	3.33	220

Test Structure Number	Name	Discussion Section	Page No.
III-13	Substrate contact transistor; variable size Purpose: measure effects of substrate (i.e., subsurface) potential	3.34	223
III-14	Contact opening test; n^+ epi Purpose: measure optimum contact geometry relative to a standard large contact	3.35	226
III-15	Contact opening test; p^+ epi Purpose: as III-14	3.35	226
III-16	Contact opening test; p^- poly Purpose: as III-14	3.35	226
III-17	Contact opening test; p^+ poly Purpose: as III-14	3.35	226

(3) Device Locations. The type III locations are shown in figure 15.

(4) Pad Identification. Pad identification for type III is shown in figure 16.

(5) Pad Classification. Type III pad classification is shown in figure 17.

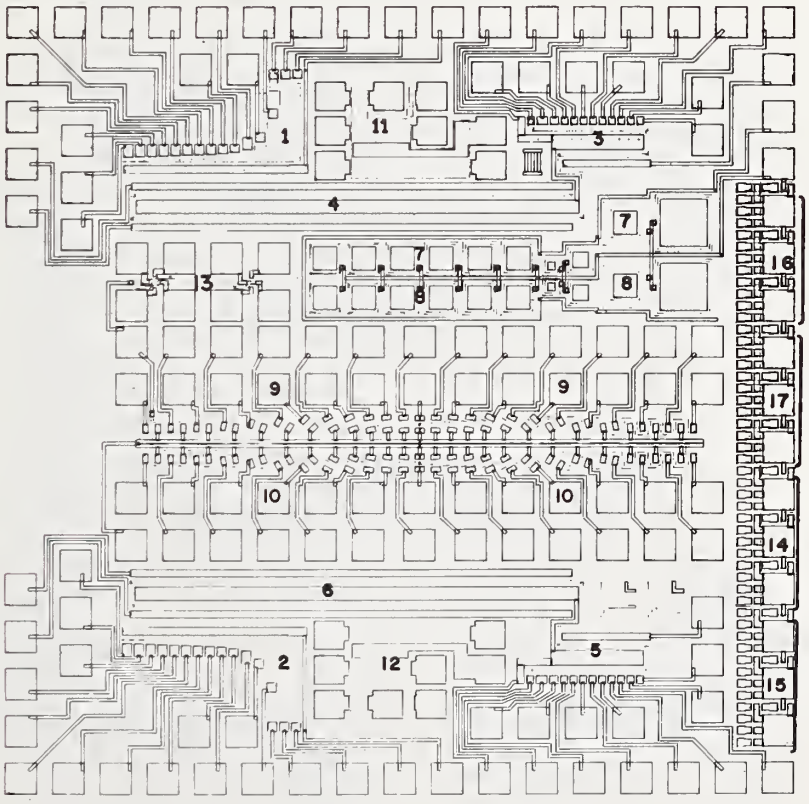


Figure 15. Device locations - type III.

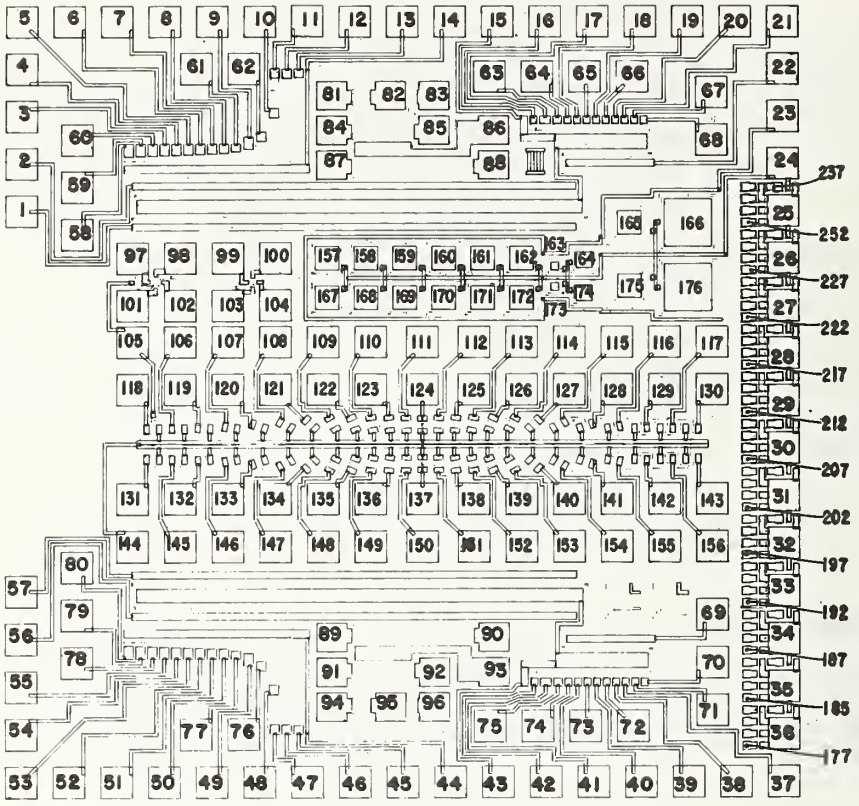


Figure 16. Pad identification - type III.

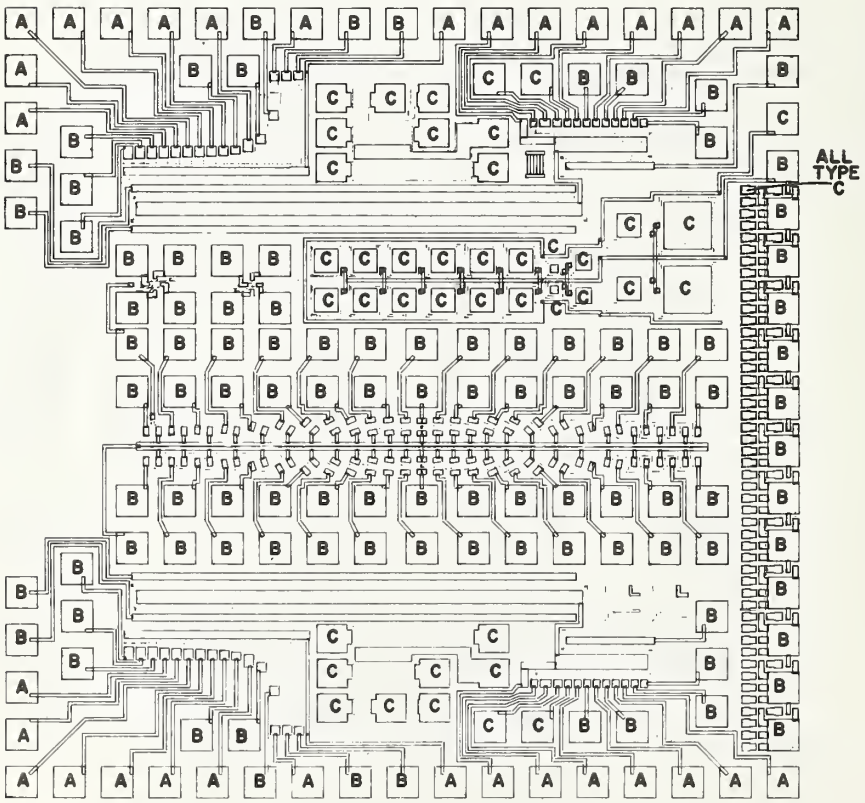


Figure 17. Pad classification - type III.

d. Type IV Pattern

(1) Purpose. The type IV pattern is intended to provide information concerning the parametric behavior of many devices at a time. The devices in the type IV pattern consist of MOS transistors, crossovers, and contact resistance structures. These devices are connected in series or in parallel with varying number of devices available.

The relatively large numbers of devices greatly increases the chances of finding defective devices to study. Some indication of the LSI (large-scale integration) performance is also available. The varying numbers of devices provide a type of physical stimulus as discussed in Section 1.2c.

(2) List of Structures.

Test Structure Number	Name	Discussion Section	Page No.
IV-1	n-Channel MOS transistors; narrow channel [also poly, (n^+ epi) crossovers] Purpose: measure properties of a large number of parallel devices	3.36	230
IV-2	p-Channel MOS transistors; narrow channel [also poly, (p^+ epi) crossovers] Purpose: as IV-1	3.36	230
IV-3	n-Channel MOS transistors; long channel Purpose: as IV-1	3.37	230
IV-4	p-Channel MOS transistors; long channel Purpose: as IV-1	3.37	230
IV-5	p^+ Epi contacts and Al, p^+ epi crossovers Purpose: measure contact integrity on a variable large number of contact and crossovers	3.38	241
IV-6	n^+ Epi contacts and Al, n^+ epi crossovers Purpose: as IV-5	3.38	241
IV-7	p^+ Poly contacts and Al, p^+ poly crossovers Purpose: as IV-5	3.38	241
IV-8	p Poly contacts and Al, p^- poly crossovers Purpose: as IV-5	3.38	241
IV-9	Combination contact - crossovers; all types Purpose: measure total process electrical continuity	3.39	248

(3) Device Locations. The type IV device locations are shown in figure 18.

(4) Pad Identification. Pad identification for type IV is shown in figure 19.

(5) Pad Classification. Type IV pad classification is shown in figure 20.

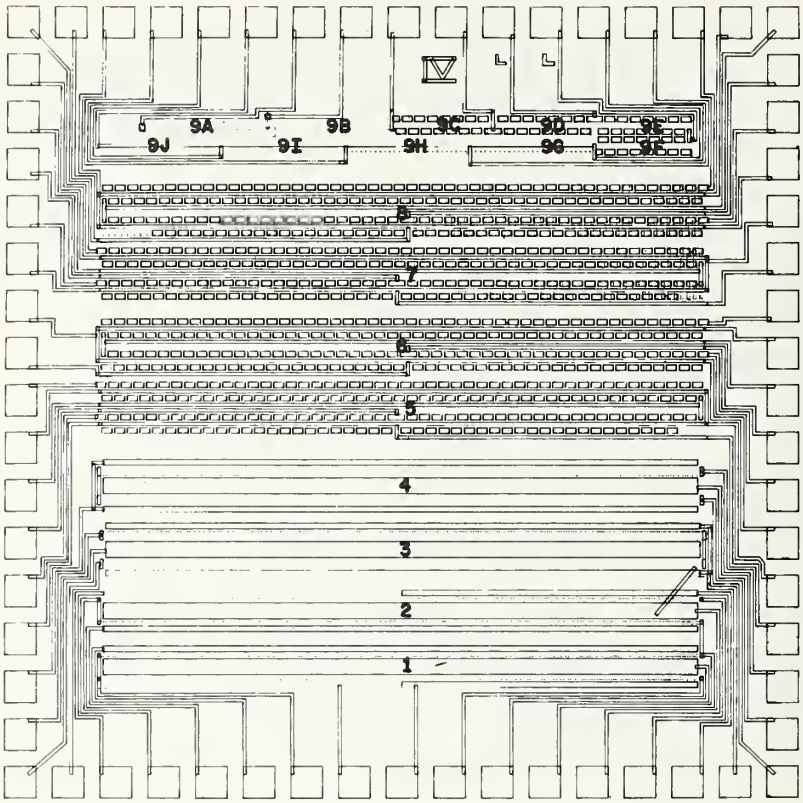


Figure 18. Device locations - type IV.

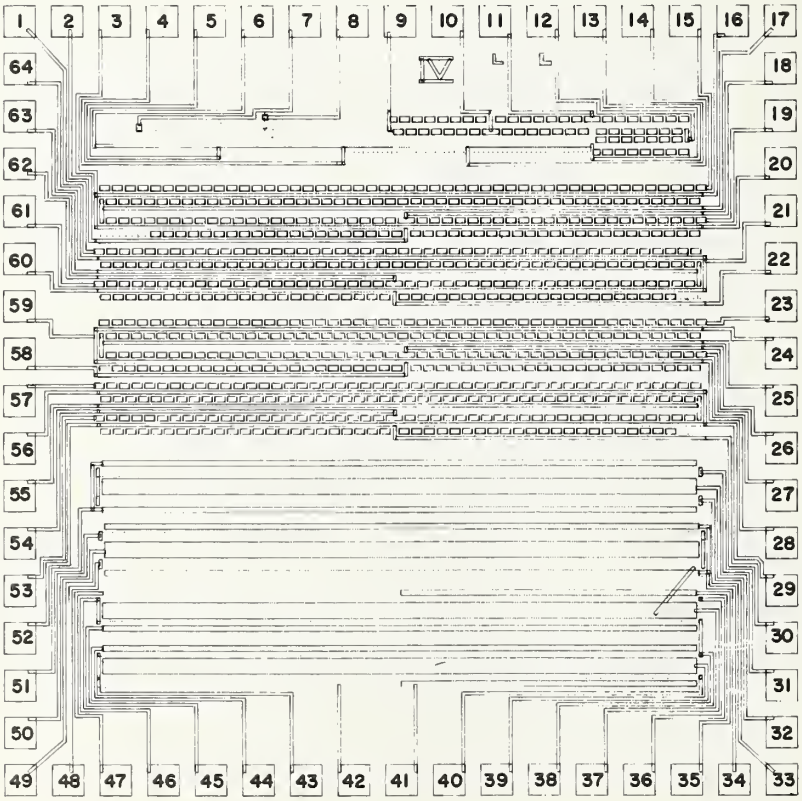


Figure 19. Pad identification - type IV.

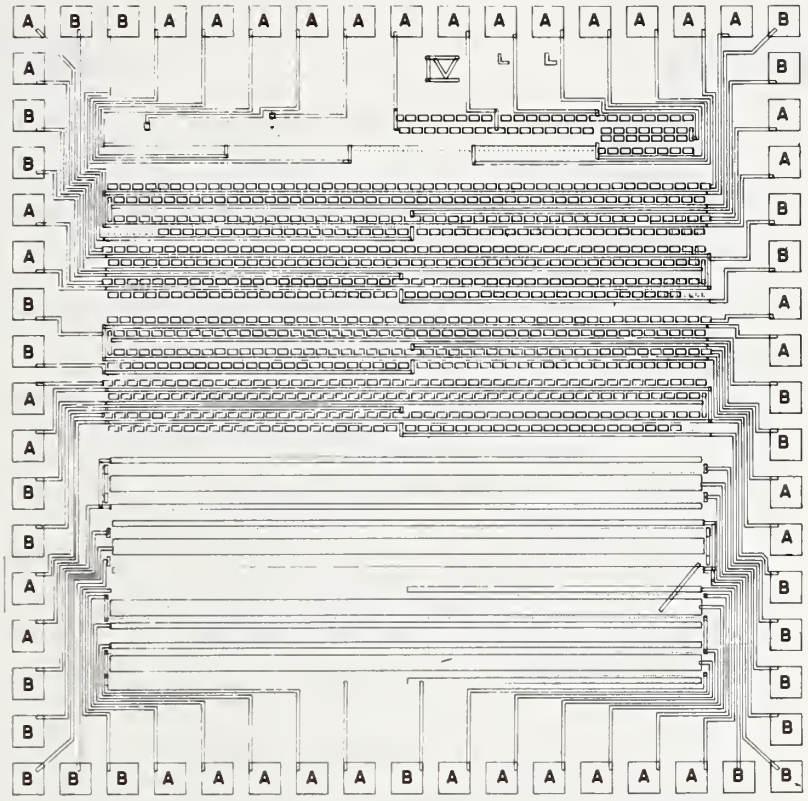


Figure 20. Pad classification - type IV.

e. Type V Pattern

(1) Purpose. The type V pattern is intended to provide information concerning the lithographic properties, the operation of certain basic CMOS building blocks, and their dynamic performance.

The devices include the optically and electrically accessible lithographic structures and certain CMOS building block structures.

(2) List of Structures.

Test Structure Number	Name	Discussion Section	Page No.
V-1	Electrical resistivity - dimension; epi Purpose: measure epi dimensions electrically	3.40	258
V-2	Electrical resistivity - dimension; poly Purpose: measure poly dimensions electrically	3.40	258
V-3	Electrical resistivity - dimension; Al Purpose: measure aluminum dimensions electrically	3.40	258
V-4	2-Level interaction - design rule epi; poly Purpose: measure optimum spacings between mask levels	3.41	261
V-5	2-Level interaction - design rule - epi; Al Purpose: as V-4	3.41	261

Test Structure Number	Name	Discussion Section	Page No.
V-6	2-Level interaction - design rule; poly - Al Purpose: as V-4	3.41	261
V-7	2-Level interaction - design rule; epi - contact Purpose: as V-4	3.41	261
V-8	2-Level interaction - design rule; poly - contact Purpose: as V-4	3.41	261
V-9	Electrical alignment test; poly - epi Purpose: measure alignment between two mask levels electrically	3.42	279
V-10	Electrical alignment test; poly - epi Purpose: as V-9	3.43	279
V-11	Electrical alignment test; poly - Al Purpose: as V-9	3.42	279
V-12	Electrical alignment test; epi - contact Purpose: as V-9	3.44	279
V-13	Electrical alignment test; poly - contact Purpose: as V-9	3.44	279
V-14	Electrical alignment test; epi - n^+ oxide Purpose: as V-9	3.45	279
V-15	Electrical alignment test; contact - Al Purpose: as V-9	3.46	279
V-16	2-Level interaction - sizes; contacts on n^+ epi Purpose: measure minimum size achievable and actual size achieved	3.47	289
V-17	2-Level interaction - sizes; n^+ oxide on p^+ poly Purpose: as V-16	3.47	289
V-18	2-Level interaction - sizes; n^+ oxide on p^+ epi Purpose: as V-16	3.47	289
V-19	2-Level interaction - sizes; poly on epi Purpose: as V-16	3.47	289
V-20	2-Level interaction - sizes; contacts on on p^- poly Purpose: as V-16	3.47	289
V-21	2-Level interaction - sizes; Al on p^+ epi Purpose: as V-16	3.47	289
V-22	2-Level interaction - sizes; contacts on p^+ epi Purpose: as V-16	3.47	289
V-23	2-Level interaction - sizes; Al on n^+ epi Purpose: as V-16	3.47	289
V-24	2-Level interaction - sizes - epi on sapphire Purpose: as V-16	3.47	289
V-25	2-Level interaction - sizes; Al on p^+ poly Purpose: as V-16	3.47	289

Test Structure Number	Name	Discussion Section	Page No.
V-26	2-Level interaction - sizes; contacts on p^+ poly Purpose: as V-16	3.47	289
V-27	2-Level interaction - sizes; Al on p^- poly Purpose: as V-16	3.47	289
V-28	Sizes; Al on sapphire Purpose: measure actual size of level achieved	3.48	289
V-29	Sizes; n^+ on sapphire Purpose: as V-27	3.48	289
V-30	Sizes; poly on sapphire Purpose: as V-27	3.48	289
V-31	Sizes; epi on sapphire Purpose: as V-27	3.48	289
V-32	Alignment measurement; contacts - epi Purpose: measure alignment between two levels optically	3.49	300
V-33	Alignment measurement; n^+ oxide - poly Purpose: as V-21	3.49	300
V-34	Alignment measurement; n^+ oxide - epi Purpose: as V-31	3.49	300
V-35	Alignment measurement; poly - epi Purpose: as V-31	3.49	300
V-36	Alignment measurement; contact - metal Purpose: as V-31	3.49	300
V-37	Alignment measurement; metal - poly Purpose: as V-31	3.49	300
V-38	Alignment measurement; metal - epi Purpose: as V-31	3.49	300
V-39	Alignment measurement; contact - poly Purpose: as V-31	3.49	300
V-40	Alignment keys } L-shape	3.50	308
V-41	Alignment keys } squares	3.51	308
V-42	Surface profilometer Purpose: measure actual film thickness achieved	3.52	311
V-43	NOR gate ring oscillator - 32 stage Purpose: verify dynamic operation of complicated device interconnection	3.53	313
V-44	Inverter ring oscillator - 18 stage Purpose: verify dynamic operation of relatively simple device interconnection	3.54	313
V-45	Inverter Purpose: standard CMOS building block	3.55	319
V-46	Transmission gate Purpose: standard CMOS building block	3.56	319

Test Structure Number	Name	Discussion Section	Page No.
V-47	NAND gate Purpose: standard CMOS building block	3.57	319
V-48	NOR gate Purpose: standard CMOS building block	3.58	319

(3) Device Locations. The type V device locations are shown in figure 21.

(4) Pad Identification. Pad identification for type V is shown in figure 22.

(5) Pad Classification. Type V classification is shown in figure 23.

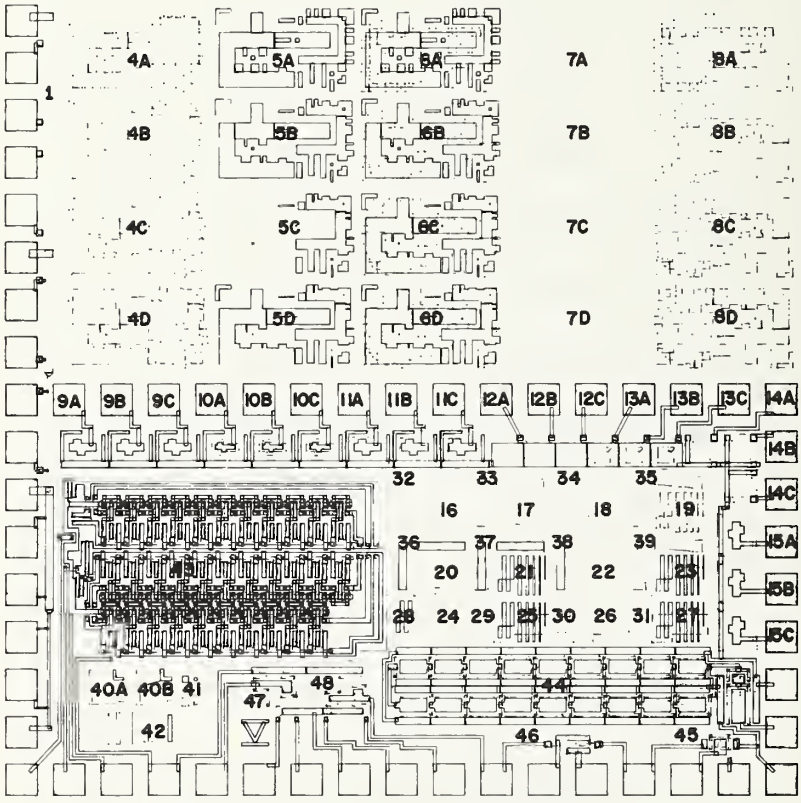


Figure 21. Device locations - type V.

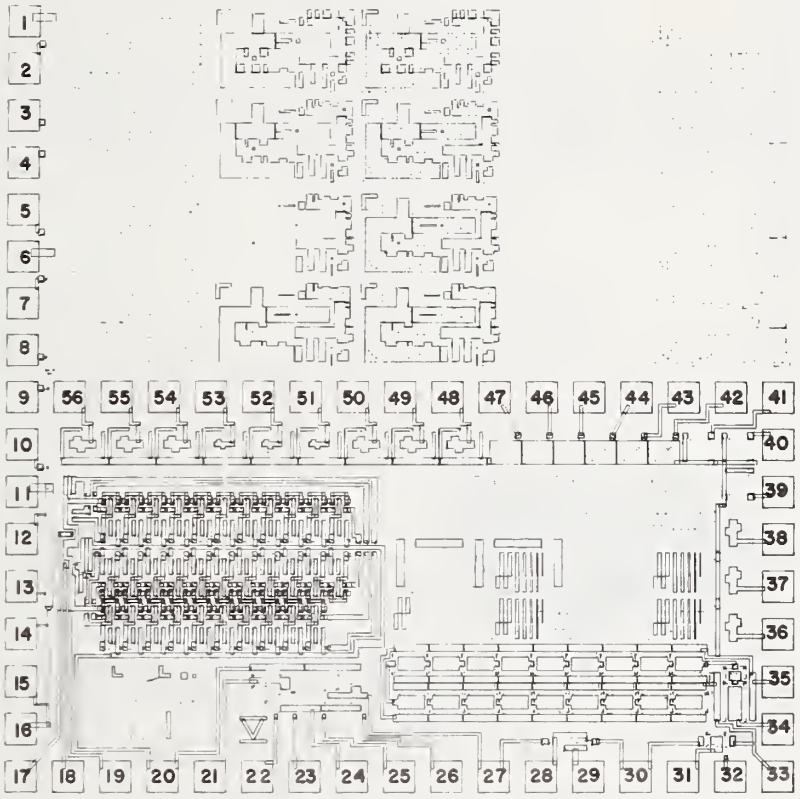


Figure 22. Pad identification - type V.

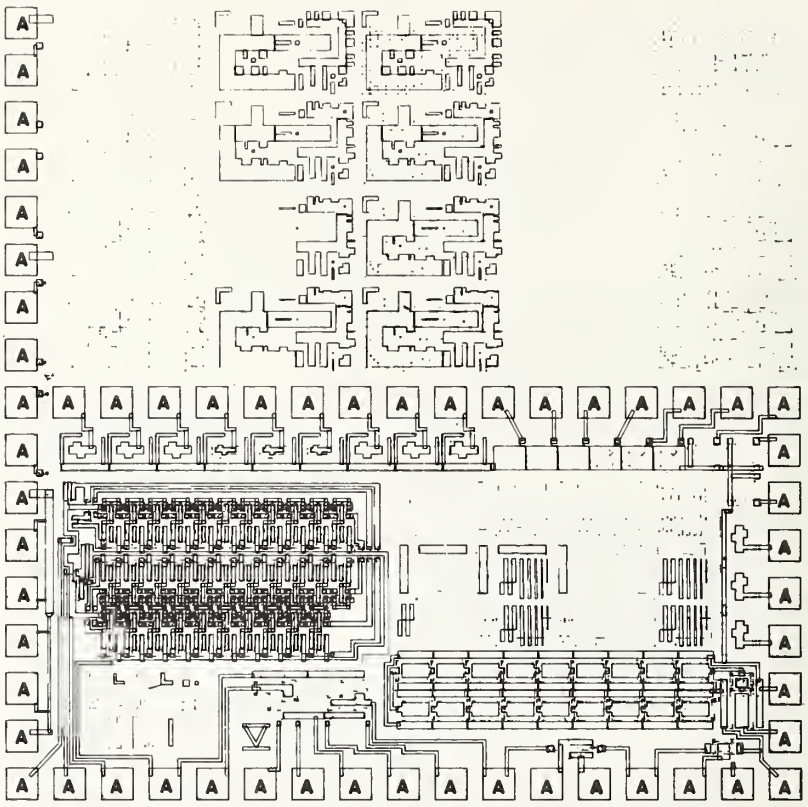


Figure 23. Pad classification - type V.

3. DETAILED DISCUSSION AND DESCRIPTIONS OF INDIVIDUAL STRUCTURES

This section contains the information concerning the overall purpose and general considerations to be used for all structures included on the pattern. Several types have been analyzed and tested in some detail while others have not. Each description (which applies in some cases to many different structures) is organized as indicated below:

(a) Purpose

(b) Verbal description

(c) Line drawing using computer checkplots for basic lines - cross sections and line identification provided by draftsman as necessary.

(d) Halftone photograph

(e) Identification of electrical access points

(f) Verbal description of method of testing

(g) List of parameters needed to describe the recommended tests

(h) Flow chart of recommended test in most general case

(i) List of outputs available

(j) List of less general versions of test procedures

(k) Discussion of special equipment necessary for acquiring the raw data

(l) Examples of data acquired from structure including appropriate samples of reduced data

(m) Potential pitfalls of structure

(n) Comments on overall usefulness of structure and possible improvements

(o) Other related structures

The purpose generally indicates the measurement made with the test structure under discussion.

The verbal description describes the physical structure in terms of dimensions, etc.

The line drawing is produced by using a computer checkplot for the basic lines. All critical lines are numbered to correspond to the mask level. Since computer drawings are used, some figures are present which do not make sense upon first examination. Figures are sometimes created by superposition of other figures, thereby creating lines which do not actually exist in the finished structure. One must realize that this method of drawing exists when examining the line drawings. A black and white photograph is taken of the multicolor computer checkplot (available from the author) to form the basic drawing. Different colors produce a different gray scale but this should not be relied on to distinguish the various levels since the pen pressure or other details of the computer drawing may also produce different gray scales within the same level. If it is helpful to understand the structure, a cross-sectional view is shown, assuming the process shown in figure 8 is being used. Of course, this process is not necessarily the one used, but it helps to illustrate the mask levels. These cross sections are taken across the region indicated by a thin drawn line. The conventions used in figure 8 and table 2 are followed throughout.

The passivation or overcoat is normally not shown in the cross sections. If it is shown, it is designated 'OC.'

One or more halftone photographs of a structure typical of the description are shown.

The electrical access points are listed by name and number. The positions within the pattern where the description is used are noted.

One of the major segments of the detailed descriptions is the method of testing. This includes a discussion of the principle of operation, the sensitive portions of the structure, any necessary theory, and, most importantly, a description of the actual process of testing.

A list of the parameters needed to specify the automatic testing conditions is presented with the name and symbol used.

A flow chart of the most general version of the testing process is presented. These flow charts and the entire testing procedure are meant to be a suggestion of a good method of testing. In most cases, these suggestions would deserve, at least, a place in the library for the structure, but they are not meant to be gospel and certainly do not comprise the only possible good program which could be used. As stated earlier there usually does not exist a "best" program for a structure, although "best" programs may exist for specific applications of the test structure. If a "core" exists where the actual measurement is done, this is highlighted in the flow chart.

A list of outputs available from the general test program is provided with the output name and the symbols used.

A list with a brief description of the less general versions of the structure is shown.

If special equipment is required for the measurement, a discussion of the requirements and of the possibility of automating the measurement is presented. Special equipment would be equipment requiring more than 4-digit resolution, voltages <1.000 mV or >100 V, currents <1 μA or >1 A, active circuits, nonelectrical excitation, or other features not found in usual voltage/current measurements.

Samples of data acquired from the structure are presented, if available.

A discussion of the potential problems one may have with the structure or test method is included.

A brief assessment of the overall usefulness of the structure and a mention of possible improvements that may be incorporated in more refined versions is given.

Finally, other related structures which may be used for measurements similar or related to those of the structure being described are referred to.

The following list indicates the structures which will be described in the terms detailed above. The bracketed structures are discussed as a group.

	Test Structure Class	Test Structure Numbers	Page No.
1.	MOS Transistors; Edgeless	I-1, I-2, I-3, I-4	51
2.	Gate-Controlled Bridge Resistors	I-5, I-6	79
3.	Crossovers	I-7, 8, 9, 10, 11, 12, 13, 14	89
4.	Poly-Gate MOS Capacitors on epi-single contact type	I-15, 20, 21, 22, 23, 24, 29, 30, 31, 32	101
5.	Aluminum-Gate MOS Capacitors on epi-single contact type	I-16, 17, 18, 19, 25, 26, 27, 28	101
6.	Poly-Gate MOS Capacitors on epi-double contact type	I-41, 42, 43, 44	111
7.	Aluminum-Gate MOS Capacitors on poly-single contact type	I-33, 34, 35, 36, 37, 38, 39, 40	113
8.	Ungated van der Pauw Sheet Resistor	I-50, 51, 52, 53, 45	118
9.	Gate-controlled van der Pauw Sheet Resistor	I-48, 49, 54, 55	135, 143
10.	Floating gate van der Pauw Sheet Resistor	I-46, I-47	141
11.	Ungated Bridge Resistor	I-57, 59, 61, 63	143
12.	Four-Point Contact Resistance Structure	I-56, 58, 60, 62	150
13.	MOS Transistors; ordinary	I-70, I-73, 76, 77	156
14.	Channel Contact Test; MOS Transistors	I-71, I-74	156
15.	Source-Drain Diffusion Test; MOS Transistors	I-72, I-75	156
16.	Substrate Contact MOS Transistors	I-64, I-65	163
17.	Grounded Substrate MOS Transistors	I-66, 67, 68, 69	163
18.	Continuity Test; single devices	I-78, (A-J)	168
19.	Gate-Controlled Diodes	I-79, 80, (I-88, 89, 90, 91)	172
20.	Floating Gate surface ion test	I-81, 82 (I-86, 87, 95, 96)	172
21.	n^+ p^+ Diode; ungated	I-83 (I-92)	172
22.	n^+ p^+ Diode; metal gate	I-85 (I-94)	172
23.	Floating-Gate Diode	I-84 (I-93)	172
24.	MOS Capacitor on epi-single contact type, type II	II-1	195
25.	MOS Capacitor on epi-double contact type, type II	II-2	195
26.	MOS Transistors; ordinary, type II	II-3, II-4	201
27.	Probe Resistance Test	II-5	206

	Test Structure Class	Test Structure Number	Page No.
28.	MOS Transistors; variable channel length	III-1, III-2	210
29.	MOS Transistors; variable channel width	III-3, III-5	210
30.	MOS Transistors; drivers	III-4, III-6	210
31.	MOS Transistors; square - edgeless	III-7, III-8	210
32.	MOS Transistors; variable orientation	III-9, III-10	211
33.	MOS Capacitors; gate-controlled resistors	III-11, III-12	220
34.	MOS Transistors with substrate contact; variable size	III-13	223
35.	Contact Opening Test	III-14, 15, 16, 17	226
36.	MOS Transistors; narrow channel, type IV	IV-1, 2	230
37.	MOS Transistors; wide channel, type IV	IV-3, 4	230
38.	Contact-Crossover Test, type IV	IV-5, 6, 7, 8	241
39.	Continuity Test, type IV	IV-9 (A-J)	248
40.	Electrical Dimension Test	V-1, 2, 3	258
41.	Two-Level Interaction; design rule test	V-4, 5, 6, 7, 8	261
42.	Electrical Alignment Test, type 1; Al-epi	V-9, 11	279
43.	Electrical Alignment Test, type 2; Poly-epi	V-10	279
44.	Electrical Alignment Test, type 3; contact -epi	V-12, 13	279
45.	Electrical Alignment Test, type 4; n^+ -epi	V-14	279
46.	Electrical Alignment Test, type 5; Al-contact	V-15	279
47.	Two-Level Interaction; sizes	V-16 thru 27	289
48.	Sizes; single level	V-28, 29, 30, 31	289
49.	Two-Level Interaction; alignment	V-32 thru 39	300
50.	Alignment Keys; L-shaped	V-40	308
51.	Alignment Keys; squares	V-41	308
52.	Surface Profilometer	V-42	311
53.	NOR Gate Ring Oscillator	V-43	313
54.	Inverter Ring Oscillator	V-44	313
55.	Inverter	V-45	319
56.	Transmission Gate	V-46	319
57.	NAND Gate	V-47	319
58.	NOR Gate	V-48	319

3.1 MOS Transistors; Edgeless - I-1, I-2, I-3, I-4

Purpose - The purpose of structures I-1 and I-2 is to measure MOS transistor parameters on the simplest transistor structure. Structure I-3 measures p-n junction properties on the simplest junction structure, and structure I-4 measures zener properties on the simplest structure.

Verbal Description - Edgeless devices are those in which *none* of the active device area intercepts the edge of the silicon island. The least complicated structure to interpret uses a completely closed (i.e., with no discontinuities) active area. A minimum of sharp corners is obtained by using as nearly a circular shape as possible with the mask generation system. In the particular system used for these devices, this is a 24-sided equilateral polygon.

The principal active area of these devices is a ring of polysilicon with 6.0-mil inside diameter and 6.6-mil outside diameter, with a small "bulge" for the electrical contact. All contact pads are contained on the top of the epi layer to avoid any problems with metal continuity or dielectric breakdown across the island edge. The inner contact is made with a 5.6-mil-diameter circular pad.

Test structures I-1 and I-2 (MOS transistors) are entirely covered by n^+ and p^+ doped oxide, respectively. Test structure I-3 (gate-controlled diode) has the n^+ doped oxide "splitting" the polysilicon ring and covering the entire inner area. Test structure I-4 (n^+ p^+ diode) has no poly ring or contact. In this structure the inner diameter of the poly forms the edge of the n^+ doped oxide. The inner junctions of all of these devices are the same length.

A comparison of the desired configuration with the computer-generated version is shown in figure 24.

Line Drawing - The line drawing for this structure is shown in figure 25.

Halftone Photograph - The photomicrograph for this structure is shown in figure 26.

Electrical Access Points - There are three electrical access points consisting of:

- PDRN - the drain contact (the inner circle) is contacted directly to diffused silicon
- PSOR - the source contact (the outer circle) is contacted directly to diffused silicon
- PGATE- the gate contact is on top of the field oxide and does not contact diffused silicon near the probe.

Testing Method -This structure is tested in the same manner as any MOS transistor. Test results for SOS transistors are sometimes sensitive to the structural properties of the device. In particular, this structure allows (at the expense of introducing an uncertainty in the measurement due to an angular variation of properties of the device) elimination of those properties peculiar to the edge of the silicon island. These properties have been shown to be detrimental to the performance of SOS devices, particularly with regard to anomalous leakage currents and gate dielectric strength [11, 12]. A comparison of the properties of edgeless devices with equivalent edge devices provides a convenient method of separating the effect of edges. This method was the subject of a recent contract with NRL [12], and a detailed discussion of the edge effects can be found in the final report.

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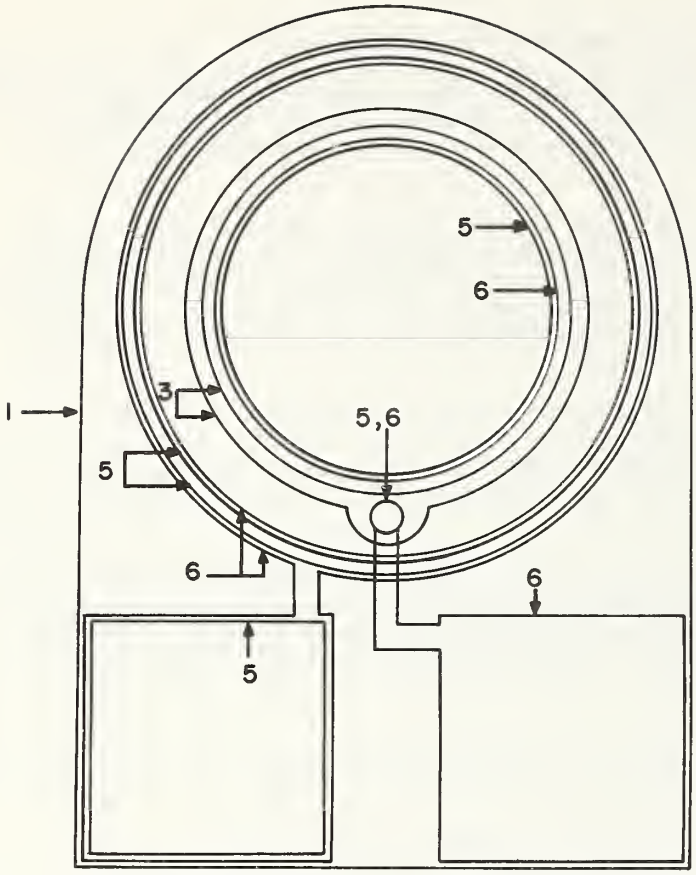
11. Flatley, D. W. and Ham, W. E., "Electrical Instabilities in SOS/MOS Transistors," Extended Abstracts of the Electrochemical Society Meeting, New York, Vol. 74-2, pp. 487-489, (Oct 1974).
12. Ham, W. E., "High Speed Complementary Metal-Oxide-Semiconductor/Silicon-on-Sapphire Development," Final Report, Phase II, Contract No. N00014-73-C-0090, Office of Naval Research, Department of the Navy, Washington, DC (Nov. 1975).



Numbers refer to mask levels.
Pads are 4.0 mil on a side.
See section 2.1c, pp. 20-25.

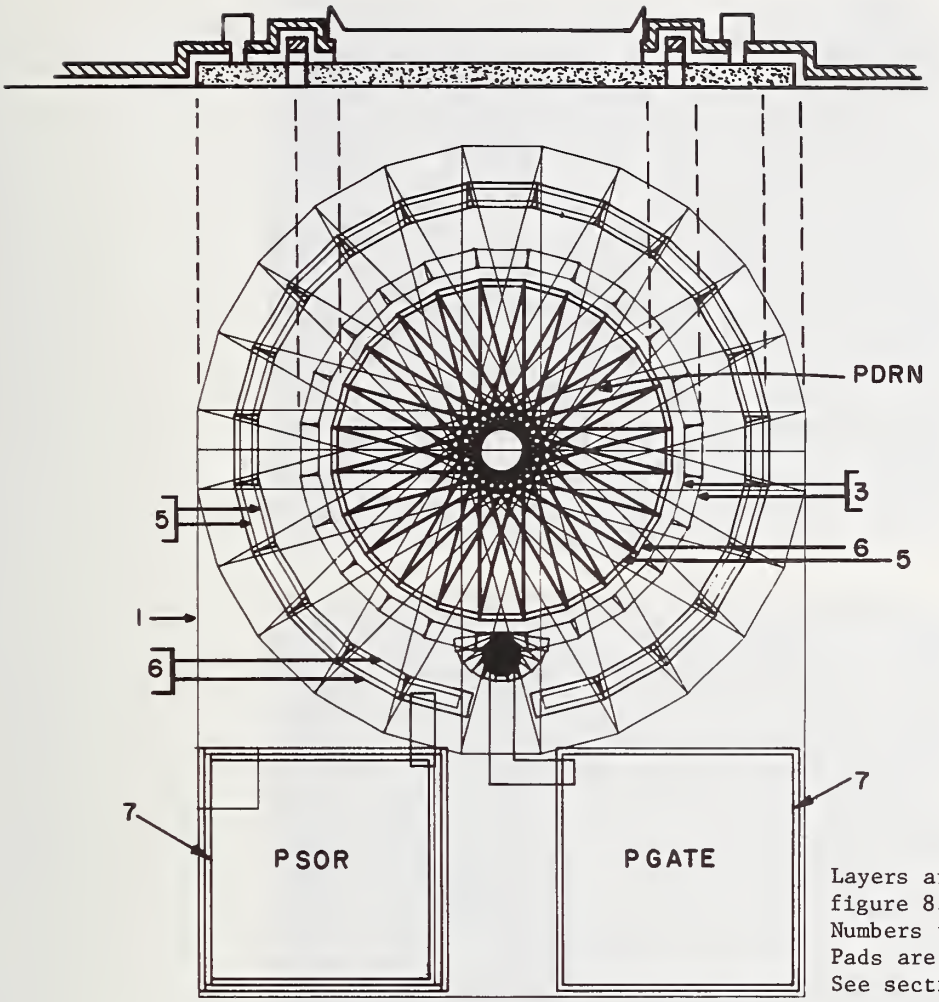
Figure 24. Ideal structures.

Since MOS transistors form a considerable fraction of the test structures on this test pattern and the major differences between these structures are sizes and physical placement, with respect to each other, it seems appropriate to describe the testing procedure here.

The MOS transistor is the most versatile test structure available for characterizing SOS processes. Therefore, it requires more kinds of testing than most of the structures. Test blocks for determining the initial suitability, the high-current regions, the low-current regions, the high-voltage regions, and the post-test suitability are needed for the general testing of these devices.

(1) Testing Method - Initial Suitability: (INSU1) - This block is used to determine that the transistor is suitable for further testing. It measures the gate leakage, the nominal threshold voltage, and the room temperature threshold voltage stability.

The threshold voltage is measured by an operational amplifier method wherein both enhancement- and depletion-type devices can be measured with equal accuracy and precisely known drain bias conditions. The basic circuit used is shown in figure 27. The threshold voltage measured in this manner bears no tie whatever to a conduction model. It is simply defined by the gate voltage required to produce whatever current is chosen to be the threshold level. The *most basic* feature of an MOS transistor which is suitable for further measurement is that this threshold voltage be within a reasonable range. This simple measurement eliminates all devices with badly shorted gates, improper contacts, very poor carrier mobility, serious surface-state problems, missing connections, etc. Using the operational amplifier method one either measures a true value of threshold voltage or the amplifiers will saturate.



Layers are identified in figure 8, p. 23.
Numbers refer to mask levels.
Pads are 4.0 mil on a side.
See section 2.1c, pp. 20-25.

Figure 25. p-Channel transistor; edgeless, test structure I-1, computer line drawing and cross section.

This method is used for every *measurement* called "threshold voltage" although as we shall see, other "threshold voltages" can be derived by extrapolation from these (and other) types of measurements taken at different current levels.

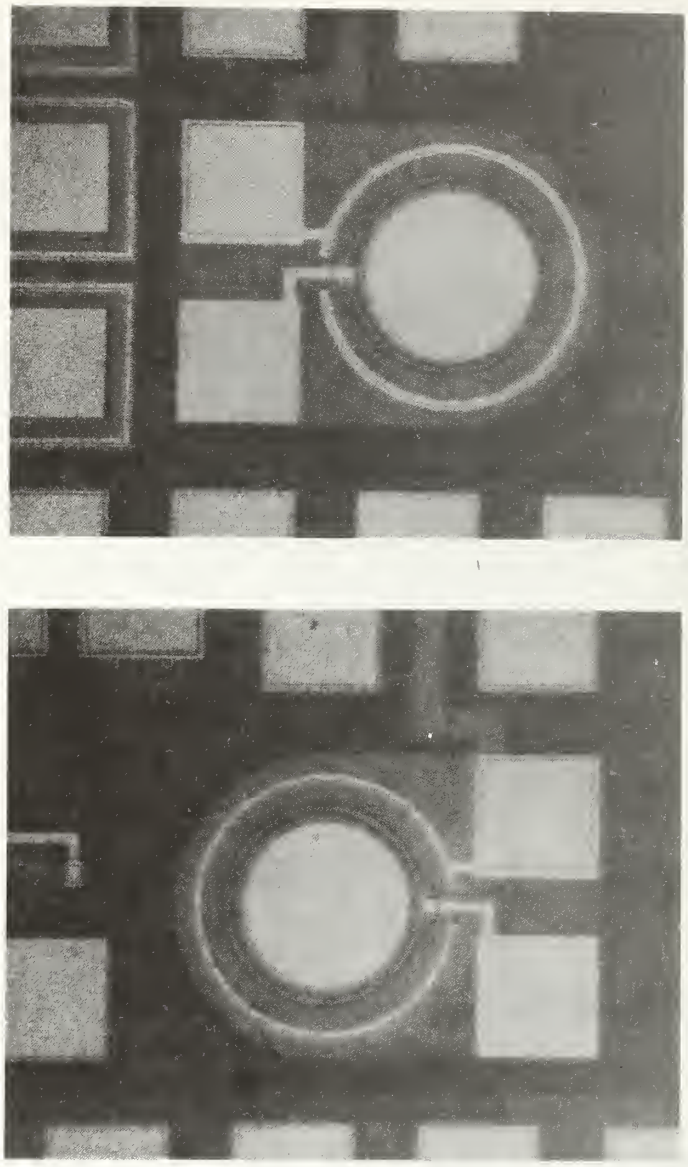
The next test involves measuring the gate current under positive bias. This obviously requires a meter which is sensitive at the gate current limit of interest. If the gate current is greater than the chosen limit, the device is declared unsuitable and testing is stopped.

After applying the positive stress voltage for a predetermined time, the threshold voltage is measured again. If this value differs from the original value by more than a predetermined amount, the device is declared unstable and testing is stopped.

Similar tests under negative gate bias are then performed.

Initial Parameters

- Drain voltage level for threshold test (VDVTI)
- Drain current level for threshold test (IDVTI)



(a)

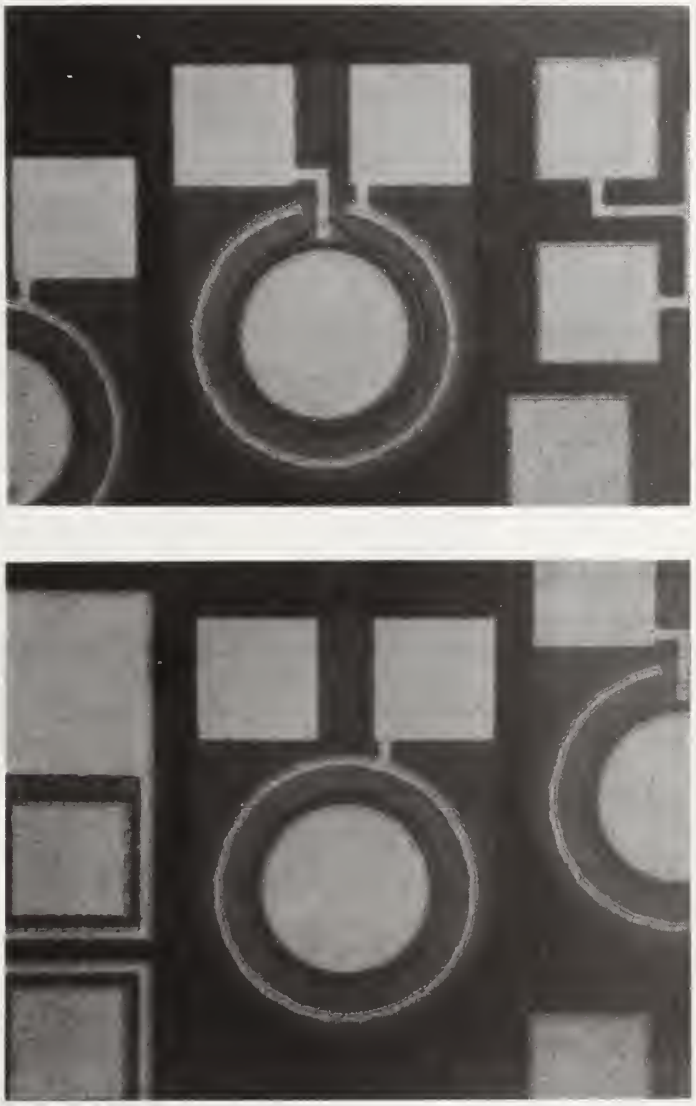
(b)

Figure 26. Photomicrographs. (a) p-channel transistor; edgeless, I-1, (b) n-channel transistor; edgeless, I-2.

- Maximum tolerable threshold voltage (VTMA)
- Gate stress voltage (GSV)
- Gate stress time (GST)
- Maximum allowable gate current (IGMA)
- Maximum tolerable threshold shift (DVTMA)

Flow Chart

The flow chart for INSU1 is shown in figure 28.



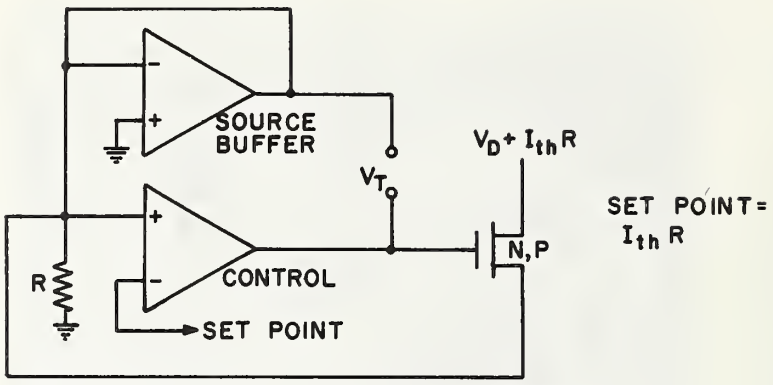
(c)

(d)

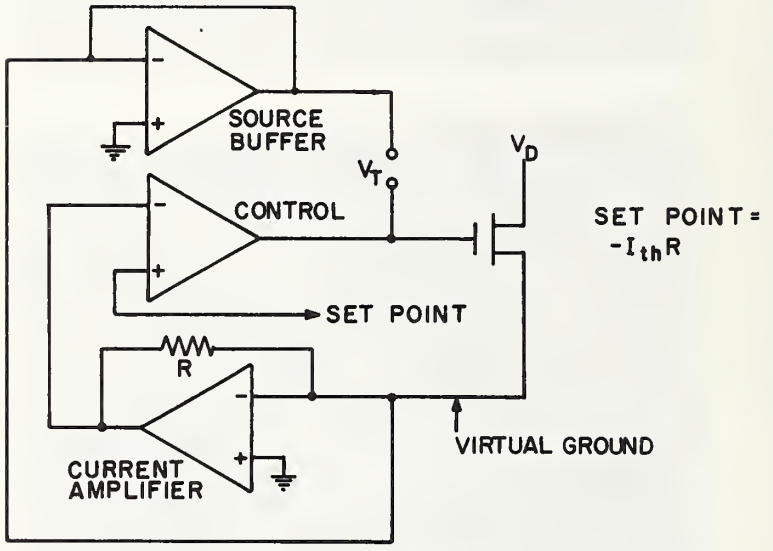
Figure 26. Continued. (c) Gate-controlled diode; edgeless, I-3 and (d) n^+p^+ diode; edgeless, I-4.

List of Outputs

	NAME
• Gate voltage at (VDVTI), (IDVTI)	VT1
• Gate conduction after (GST) at (GSV) positive pol.	IGIP
• Gate voltage at (VDVTI), (IDVTI)	VT2
• Gate conduction after (GST) at (GSV) rev. pol.	IGIN
• Gate voltage at (VDVTI), (IDVTI)	VT3



(a) NARROW CURRENT RANGE OPERATION



(b) WIDE CURRENT RANGE OPERATION

Figure 27. Operational amplifier circuits for measuring threshold voltage. The amplifiers are FET input type. Teledyne-Philbrick model 1021 amplifiers have been used successfully. The resistors, R, are chosen so that $I_{th}R$ is within a suitable range for the amplifiers.

Less General Versions

- INSU2 - measures gate current and threshold voltage
- INSU3 - measures gate current only
- VTHRES1- measures threshold voltage only by a two-point extrapolation at two different current levels using a square root plot to I = 0.
- VTHRES2- measures threshold voltage only by the current level at a specified drain voltage
- VTHRES3- measures threshold voltage only by a five-point least-squares extrapolation of the square root of the drain current to I = 0.

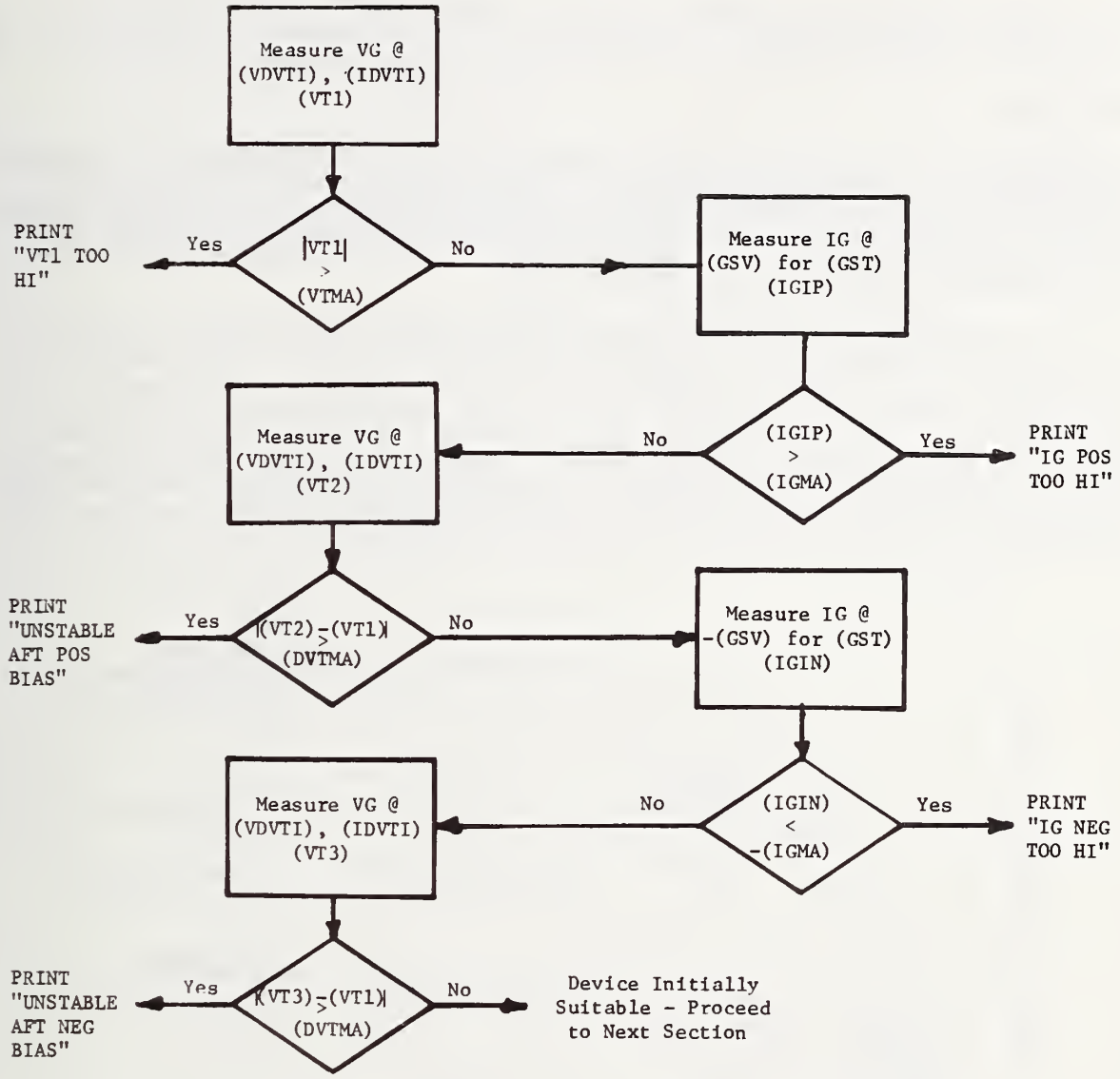


Figure 28. Flow chart for INSU1.

Special Equipment

As mentioned earlier, a current meter capable of measuring a low gate current is necessary. This current level depends strongly on the current levels of interest in other measurements. Typically, this level should be less than 10 nA, and for very low level applications such as junction leakage measurements, one should be able to measure at least 10 times lower gate current than typically measured leakage currents. In the system used for many of the measurements reported here the gate current system is capable of measuring current no lower than ∿10 nA with any accuracy. It is possible to measure leakage current in the 1-pA range using an external picoammeter, as described later. These low current leakage measurements may be dominated by the gate current. Interpretation of any junction leakage results obtained indicating current lower then the gate current measurement capability must be done with the knowledge that the gate current may be important. An example is shown later where the leakage current is actually dominated by the gate current, although the measurements look reasonable.

Other special equipment required is the operational amplifier circuit in figure 27. Wihtout this circuit an iterative procedure must be used to determine the threshold voltages in the general case (where depletion mode devices must be considered).

Data Output

The primary data output from this test block is the diagnostic messages which appear during execution. The most common cause for initial unsuitability is that the initial threshold voltage is out of range. Numerous examples have been found, however, where room-temperature threshold voltage instability and gate dielectric failures have caused the problem. The primary function of this test block is, however, to send control to other test blocks rather than to acquire parametric data.

(2) Testing Method - High-Level Current Tests (HCUR1) - This test block is used for measuring the characteristics of interest at relatively high current levels (well above the leakage level). Typically the drain chracteristics appear as shown in figure 29. These characteristics may be conveniently divided into two different regions defined by the drain voltage. At low drain voltage, strong dependence of the current on drain voltage is seen, while at high drain voltages, relative independence is found. This is an observed fact for these types of devices and does not depend on any detailed model. We will, however, use a simple, previously discussed [3] representation for the current in these two regions.

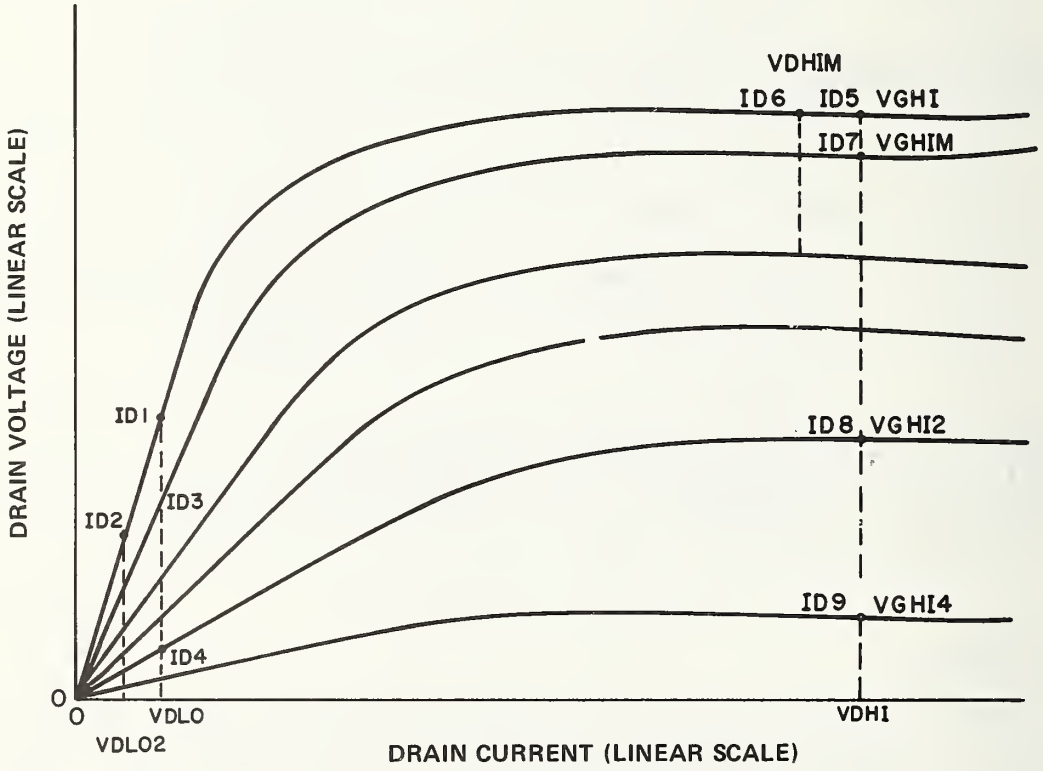


Figure 29. High-level drain current tests.

At low drain voltages, the current is crudely proportional to the drain voltage and to the gate voltage, while at high drain voltages the current depends crudely on the square of the gate voltage. We chose to use the standard form for the equation in the linear region as:

$$I_D = KLIN \left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2} \right) \quad (1)$$

One can rearrange this equation in a convenient form to plot as

$$\frac{I_D}{V_{DS}} = KLIN \left((V_{GS} - \frac{V_{DS}}{2}) - (V_T) \right) \quad (2)$$

and V_T can be found by extrapolating I_D/V_{DS} vs $V_{GS} - V_{DS}/2$ to $I_D = 0$. This VT is called VTLIN. Similarly, KLIN can be found directly from the slope of the line. In general, this line will not be straight because KLIN is not a constant. This will be discussed in a later section. Nevertheless, a definite parameter can be defined by using only two points at a known drain voltage (VDLO). We have chosen in this case to use the gate voltages defined by

$$VGHI = VT1 + VGMVT \quad (3)$$

and by

$$VGHI2 = VT1 + VGMVT/2 \quad (4)$$

where VT1 is the threshold voltage measured as in INSU1, and VGMVT is a user-chosen parameter. It may well happen that VTLIN is not equal to VT1, and, in general, this will be the case. Note, however, that VT1 is *not directly involved* in the calculation of VTLIN or KLIN; it is only used to put the measurement into the correct "ball park." This procedure is illustrated in figure 30.

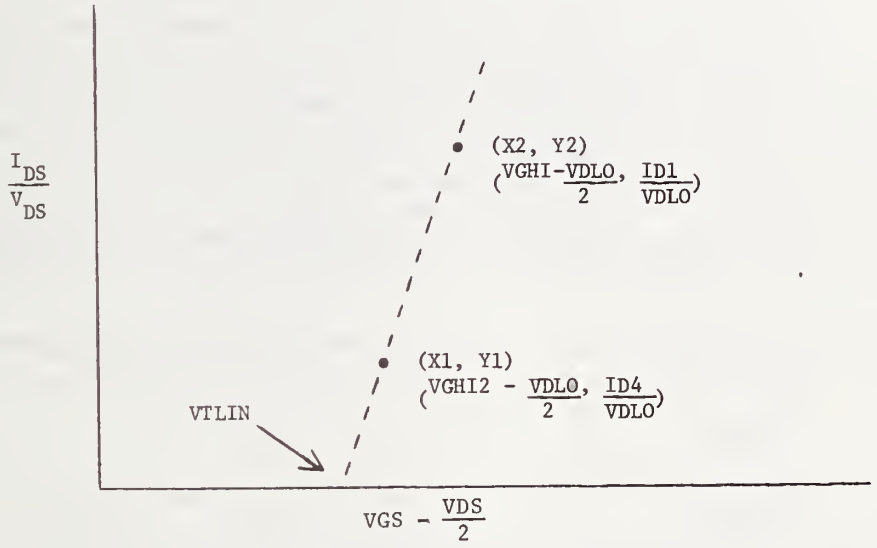


Figure 30. Linear region tests.

$$VTLIN = \frac{X1*Y2 - Y1**2}{Y2 - Y1} \quad (5)$$

$$KLIN = \frac{ID1}{[(VGHI - VTLIN)*VDLO - (VDLO**2)/2]} \quad (6)$$

Other tests of interest at the low drain voltage are the extrapolation of the nominally linear portion of the curve to $I_D = 0$. This is done using ID1 and ID2 in figure 29. If the magnitude of the drain voltage at the extrapolated intersection (VDE) is larger than a predetermined value, the device probably has faulty contacts or is not functioning normally for some other reason. Thus, a satisfactory value of VDE is necessary for further testing. Similarly, ID1 of figure 29 must be greater than a predetermined limit chosen to represent reasonable behavior. One additional measurement is obtained at VDLO and VGHIM (where VGHIM = VGHI - 0.1 VGMVT). This measurement can be used to obtain an indication of the local (small-signal) gain in the low-drain voltage region or as an additional point in the determination of VTLIN and KLIN. The gain is calculated as

$$\text{GMLIN} = \frac{\text{ID1} - \text{ID3}}{0.1*\text{VGMVT}} \tag{7}$$

At high drain voltages (designated by the user as VDHI) the current is assumed to behave according to the general functional form

$$I_D = \text{KSAT} \frac{(\text{VGS} - \text{VTSAT})^2}{2} \tag{8}$$

Note that KLIN and KSAT are not necessarily equal. The factor of two in the denominator is used so that both KLIN and KSAT will be nominally the same if the device follows the simple textbook theory. Five current measurements at or near VDHI are made as shown in figure 29. We have chosen a three-point least-squares method for determining KSAT and VTSAT. These points are ID5, ID8, and ID9. The least-squares method follows that given in Ref. 13. The square roots of these drain currents are plotted against VGS, and the intersection of the least-squares fit is assumed to be VTSAT, while the slope is given by $\sqrt{\text{KSAT}/2}$. This discussion is illustrated in figure 31. Perhaps the most important feature of this extrapolation method is that it is (at least for nominally well-behaved devices) *independent of the channel geometry* for the threshold voltage. This provides a very convenient method for separating the factors determining the actually achieved high-level currents. Another important reason to use the three-point least-squares method is that an additional parameter which represents how well the data actually fits the original functional form can be derived as a natural consequence of the calculations. This parameter is available whenever a least-squares method is employed and, in general, will be included for all tests used in this work. It has been designated as FQULXXX where XXX designates the variable of interest. The mathematical name for this parameter is the standard error of estimate.

Two additional parameters are calculated to represent the output impedence and the small-signal saturation gain:

$$\text{GOUT} = \frac{\text{ID5} - \text{ID6}}{0.1*\text{VDHI}} \tag{9}$$

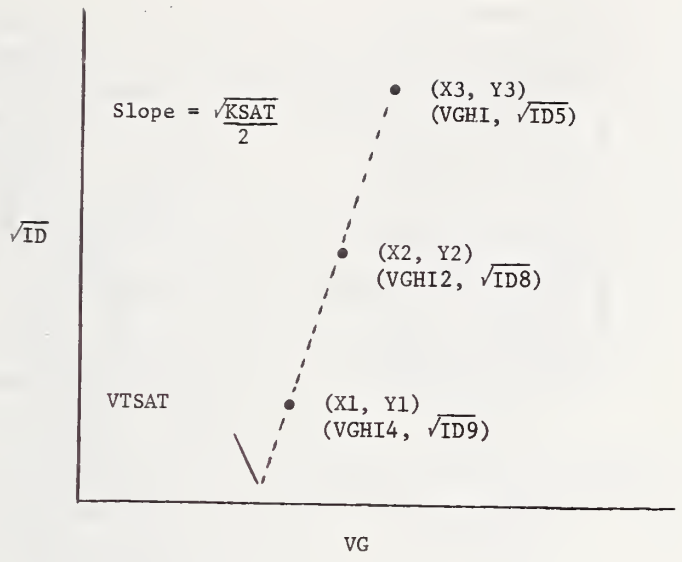
$$\text{GMSAT} = \frac{\text{ID5} - \text{ID7}}{0.1*\text{VGMVT}} \tag{10}$$

These measurements complete the general version of the high-level current tests.

Initial Parameters

- Drain voltage for initial threshold voltage measurements (VDVTI)
- Drain current level for initial threshold voltage measurements (IDVTI)
- Drain voltage for linear region (VDLO)
- Difference between threshold voltage and high-level gate voltage (VGMVT)

13. Speigel, M. R., "Correlation Theory," Chapter 14, *Theory and Problems of Statistics*, pp. 241-248 (Schaum, New York, 1961).




```
S1 = 3
S2 = X1 + X2 + X3
S3 = Y1 + Y2 + Y3
S4 = X1Y1 + X2Y2 + X3Y3
S5 = X1**2 + X2 **2 + X3**2
S6 = Y1**2 + Y2**2 + Y3**2
Y = AX + B where
A = SQRT(KSAT)/2 = (S1*S4 - S2*S3)/(S1*S5 - S2**2)
B = A*VTSAT = (S5*S3 - S2*S4)/(S1*S5 - S2**2)
FQULID = SQRT ((S6 - A*S4 - B*S3)/(S1-2))
```

Figure 31. Saturation region tests.

- High-level drain voltage (VDHI)
- Minimum (ID1) tolerable (ID1MN)
- Maximum (VDE) tolerable (VDEMA)

Definitions Used

(VGHI) = (VGMVT) + (VT1)

(VDLO2) = (VDLO)/2

(VGHIM) = (VGHI) - 0.1 (VGMVT)

(VGHT2) = (VT1) + (VGMVT)/2

(VGHI4) = (VT1) + (VGMVT)/4

(VDHIM) = 0.9 (VDHI)

Flow Chart

The flow chart for HCUR1 is shown in figure 32.

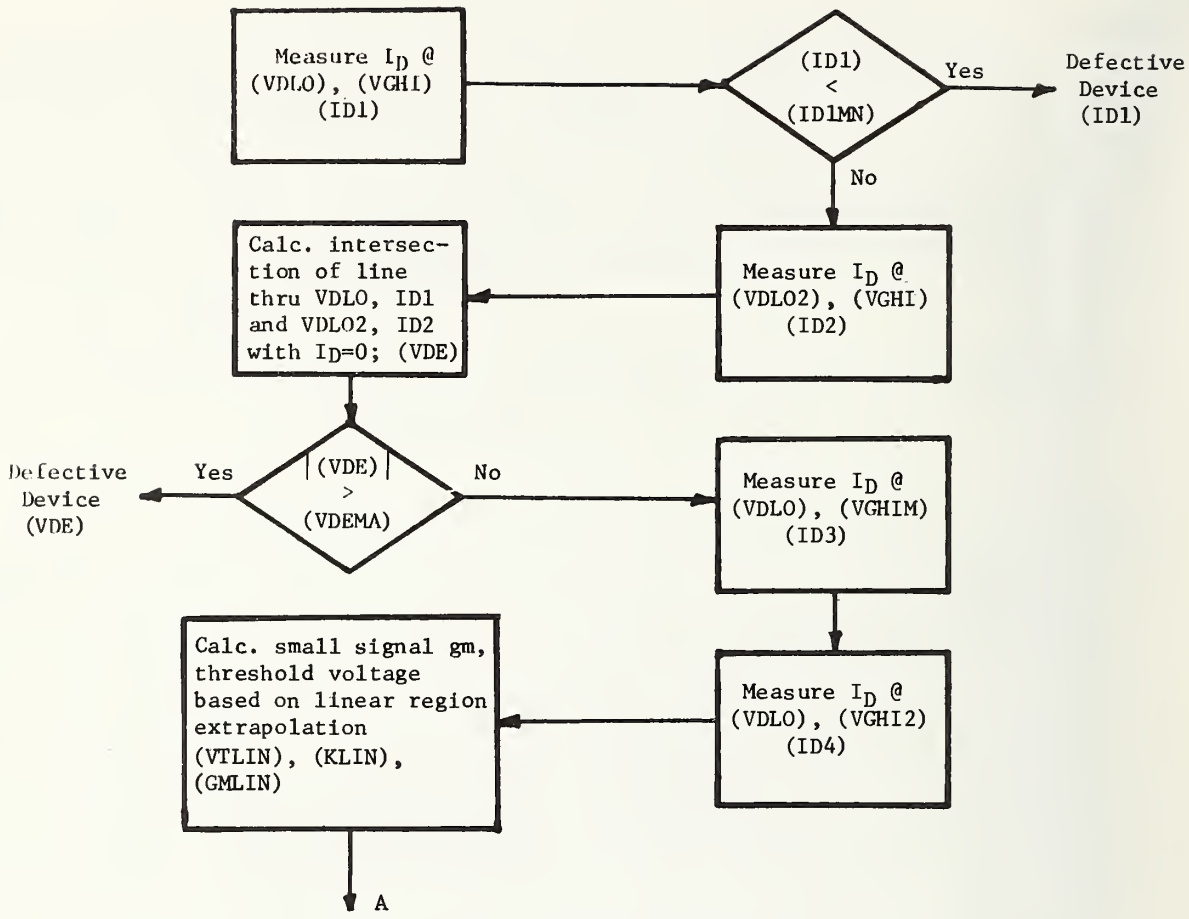


Figure 32.1. Flow chart for HCUR1.

List of Outputs

	NAME
• I_D @ (VDLO), (VGHI)	ID1
• I_D @ (VDLO2), (VGHI)	ID2
• I_D @ (VDLO), (VGHIM)	ID3
• I_D @ (VDLO), (VGHI2)	ID4
• I_D @ (VDHI), (VGHI)	ID5
• I_D @ (VDHIM), (VGHI)	ID6
• I_D @ (VDHI), (VGHIM)	ID7
• I_D @ (VDHT), (VGHI2)	ID8
• I_D @ (VDHI), (VGHI4)	ID9
• Small signal-gain linear region	GMLIN
• Threshold voltage linear region	VTLIN
• Proportionality factor linear region	KLIN

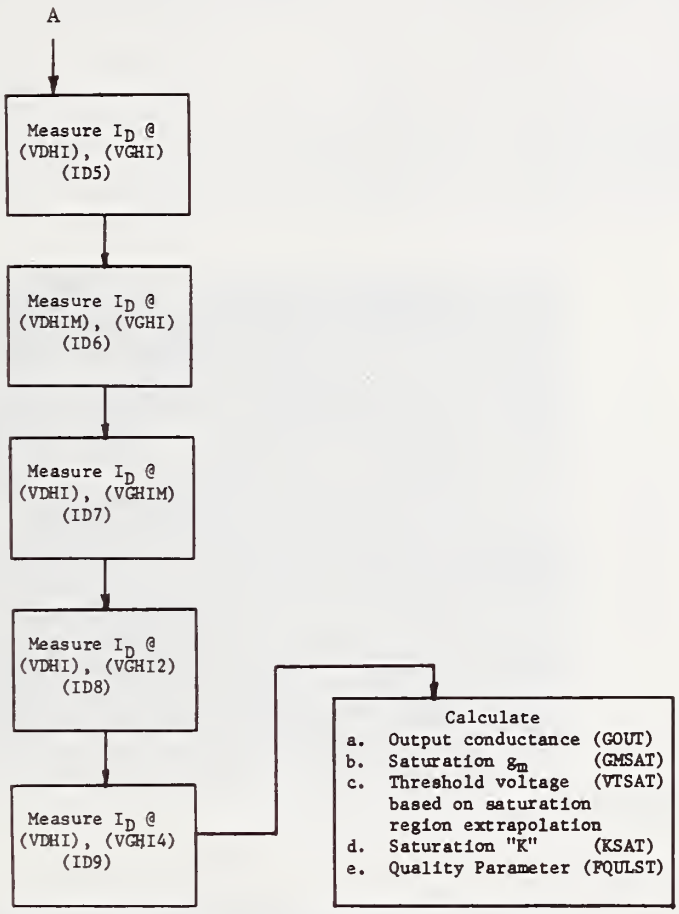


Figure 32.2. (Continued).

- Output conductance saturation region — GOUTST
- Small signal-gain saturation region — GMSAT
- Proportionality factor saturation region — KSAT
- Threshold voltage saturation region — VTSAT
- Quality parameter saturation region — FQULST

Less General Versions

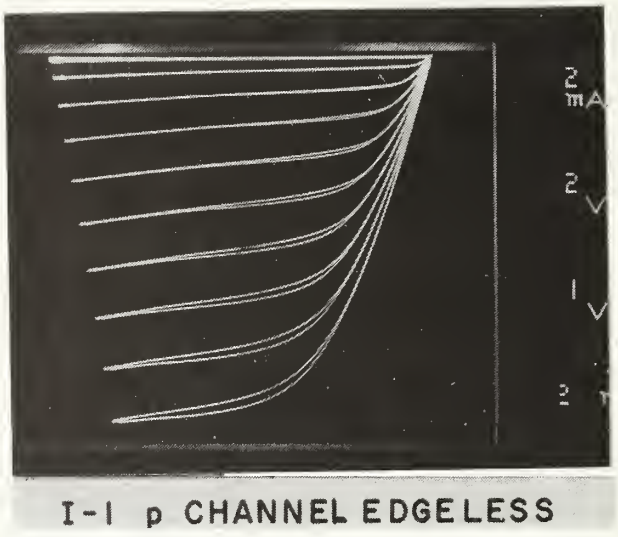
- HCUR2 - measures both linear and saturation regions; uses VDE and ID1 rejection criteria; uses two-point measurement; outputs: VTI, VDE, VTSAT, KSAT
- HCUR3 - measures only drain current at a specified gate voltage and drain voltage
- HCUR4 - measures drain current at a specified drain voltage and at specified *difference* between threshold voltage (which is supplied from other tests) and applied gate voltage

Special Equipment

This test block does not require any special equipment.

Samples of Data

The data produced by this test block is best seen in a conventional curve tracer plot of the drain characteristics as shown in figure 33. Computer-acquired data have shown substantial differences between VTLIN and VTSAT and between KLIN and KSAT which illustrate the wisdom of not using the same model for both regions. In addition, numerous failures have been noted because of ID1 being too low or |VDE| being too high.



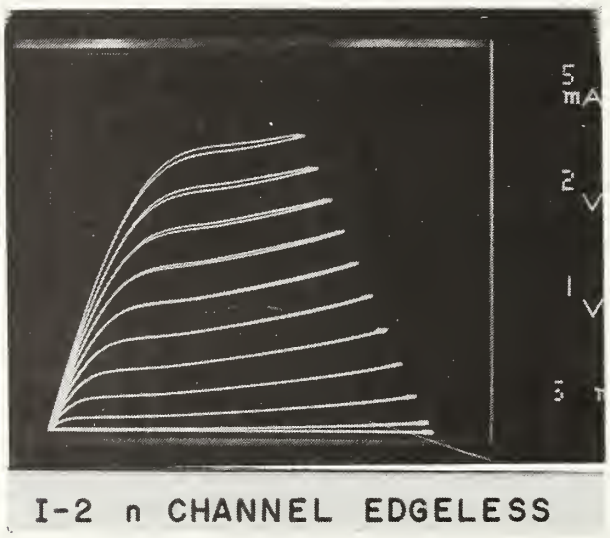


Figure 33. Drain characteristics of I-1 and I-2. Gate and drain voltage are the same scale (1 V step, 10 V max and 2 V/div, respectively). Current scales are 2 mA/div for I-1 and 5 mA/div for I-2.

(3) Testing Method - Low-Level Measurements - Low-level measurements are of particular importance for SOS devices because the leakage current levels are one of the least understood and least controlled parameters. The relatively high current levels existing under nominal off conditions are directly responsible for SOS devices having difficulty in producing competitive dynamic retention times. In addition, they can cause large arrays of devices to consume excessive power under quiescent conditions. The behavior of the edge regions is largely seen in the low-level behavior [9]. The theory of low-level MOS operation or subthreshold operation, as it is sometimes called, has been discussed in the literature and will not be repeated here except to note that typically, three nominal regions exist as one changes the gate bias at constant drain voltage. These are:

- A region where the gate has only small effect on the current level.
- A region where the current depends exponentially on the gate voltage.
- A region where the current follows one of the high current formulas.

We are particularly interested in the first two regions in this section. It is frequently observed that the current in the gate voltage independent region is not gate-voltage independent. Therefore, one cannot simply measure the current under nominal "off" conditions and expect to have characterized this region. Typically, for circuit applications the "off" state is defined by VG = 0. This does not necessarily represent the minimum current level, however, especially if edge currents are significant [11]. The application of relatively high gate voltages of the polarity to accumulate surface majority carriers frequently causes substantially higher currents particularly at high drain voltages as shown in figure 34. It is therefore likely that the minimum current will occur at a gate voltage less than 0 but greater than heavy accumulation. This minimum current is important since it most nearly represents the fundamental behavior of the silicon material. It is also used to define a low level threshold voltage by extrapolating the exponential region (see figure 34) to the minimum current level. Other points of interest are the current flowing at VG = 0, at high drain biases and the behavior at low drain biases. The low drain bias (e.g., 100 mV) behavior is important because it allows determination of the properties under low field conditions. Phenomena such as avalanche multiplication, hot carrier effects, or Schottky emission are eliminated from consideration. The high drain bias (e.g., 5 to 10 V) is of interest because this parameter may determine the upper bounds for device operation and is usually observed to be much less controlled than the low drain bias region. One must be especially careful of gate current for these measurements.

The intersection of the exponential region with the minimum current provides a threshold voltage (weak inversion threshold) which is nearly independent of mobility and surface states in the inversion half of the band. This threshold has the best communication to the traditional factors which influence threshold voltage (oxide thickness, doping densities, metal work function, etc.) since it is not influenced by mobility and surface state factors. The slope of the exponential region is indicative of various types of problems, including surface states, poor quality silicon (low mobility), and edge currents.

Initial parameters

- Low level drain voltage (VDLLO)
- High level drain voltage (VDLHI)
- High level current (IDL1)
- Gate voltage increment for exponential slope (VGINC)
- Gate voltage for heavy surface accumulation (VGACC)

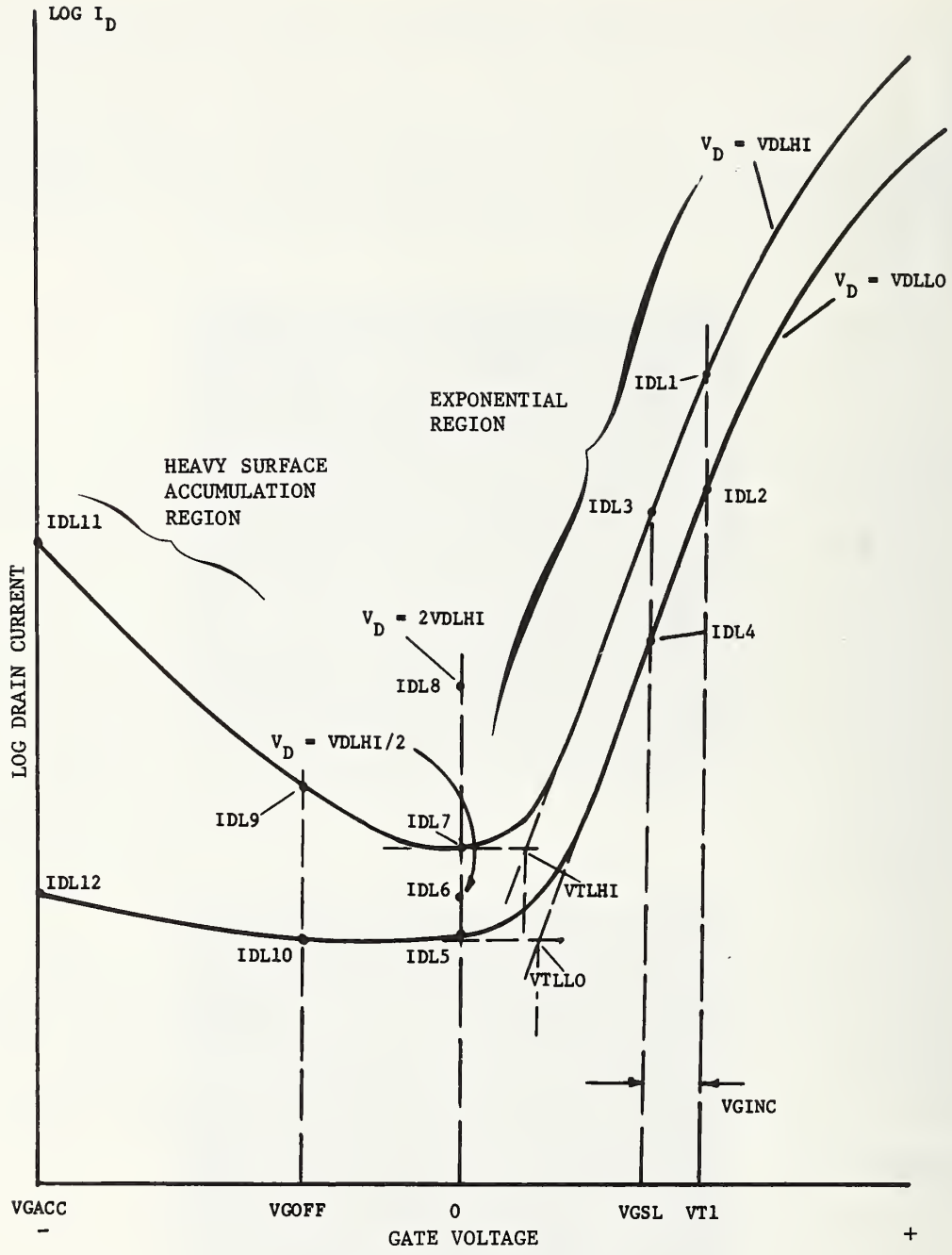


Figure 34. Low-level tests.

Flow Chart

	NAME
• Measure V_G @ (VDLHI), IDL1	(VT1)
• Measure I_D @ (VDLLO), (VT1)	(IDL2)
• Measure I_D @ (VDLHI), (VGSL)	(IDL3)
• Measure I_D @ (VDLLO), (VGSL)	(IDL4)

- Measure I_D @ (VDLLO), (O) (IDL5)
- Measure I_D @ (VDLHI)/2, (O) (IDL6)
- Measure I_D @ (VDLHI), (O) (IDL7)
- Measure I_D @ (VDLHI), (O) (IDL8)
- Measure I_D @ (VDLHI), (VGOFF) (IDL9)
- Measure I_D @ (VDLLO), (VGOFF) (IDL10)
- Measure I_D @ (VDLHI), (VGACC) (IDL11)
- Measure I_D @ (VDLLO), (VGACC) (IDL12)

Definitions:

(VGSL) = (VT1) - (VGLIN)

Calculate: VTLLO = Intersection of minimum of (IDL5), (IDL10), and (IDL11) with extrapolation of line through (VT1), (IDL2); (VGSL), (IDL4)

VTLHI = Intersection of minimum of (IDL7), (IDL9), and (IDL11) with extrapolation of line through (VT1), (IDL1); (VGSL), (IDL3)

EXPSLO = Slope of exponential region at (VDLLO)

EXPSHI = Slope of exponential region at (VDLHI)

List of Outputs

The outputs from this section are given in the flow chart.

List of Test Blocks

General Test Block LCUR1

LCUR2 - Identical to LCUR1 except that only one drain voltage is considered

LCUR3 - Low current measurement at a specified gate voltage and drain voltage

Special Equipment

These low level measurements clearly require the ability to measure currents at least as low as 1 pA. We have found that the most convenient method of making these measurements is a current amplifier with a log feedback element commonly called a log picoammeter. This meter is connected directly to the device at the probing station through a special highly isolated relay matrix located immediately behind the probe card connector. The current amplifier method is relatively insensitive to cable capacitance so the special matrix does not appreciably slow the data acquisition. This method may require several seconds to settle to a low data value; however, if one knows approximately the current level involved, he can adjust the system timing so that as little as a few milliseconds are needed if the current is high enough. By using the data value obtained at a short time the system can automatically decide if longer settling time is needed. This method is useful for any low current measurement including gate dielectric current and does not require an active buffer on the chip.

Samples of Data

Some of the data shown in this section was derived from the edge transistor structure described later (structures I-70 and I-73). These structures are equivalent to those described here in terms of testing procedures and illustrate the points made just as well.

Typical plots of low level phenomena from the structures are shown in figures 35, 36, and 37. We note that the edge devices, particularly the n-channel devices, have a low level gate conduction phenomenon which is on the same current level as the current of interest. This shows clearly in the plot but was missed during automatic testing because the gate current limit was set too high. The gate current was measured by the normal system current meter which has a limit of ∿1 nA while the measured drain current was typically much lower. Figure 38(a) shows a plot of the gate currents measured by the normal system current meter on the same log scale as that measured from the special low current system for the drain leakage [figure 38(b)]. The current measured by the system meter is due to system leakage, not gate leakage. Therefore, the measurement of the transistor leakage was not adequately protected for low gate leakage but was protected for fully shorted gates. Clearly this type of data must use the low current system for both gate and drain current for adequate validity. The list of data for IDL10 (see figure 34) is presented in figure 39. These data seem very reasonable and are indeed correct. The interpretation of the data is very likely to be incorrect because it is seriously affected, if not dominated, by the gate current. We also note that since VTLLO (shown in figure 40) is negative, the device is not exhibiting minimum current at $V_G = 0$. This agrees with the analog plot (figure 36). VTLLO is also affected by the gate current since it is calculated from currents measured in the region affected by the gate current. On the other hand, the automatic data reflect reasonable agreement with the analog plots and show that with proper protection against spurious currents these low level phenomena can be measured automatically in significant quantity.

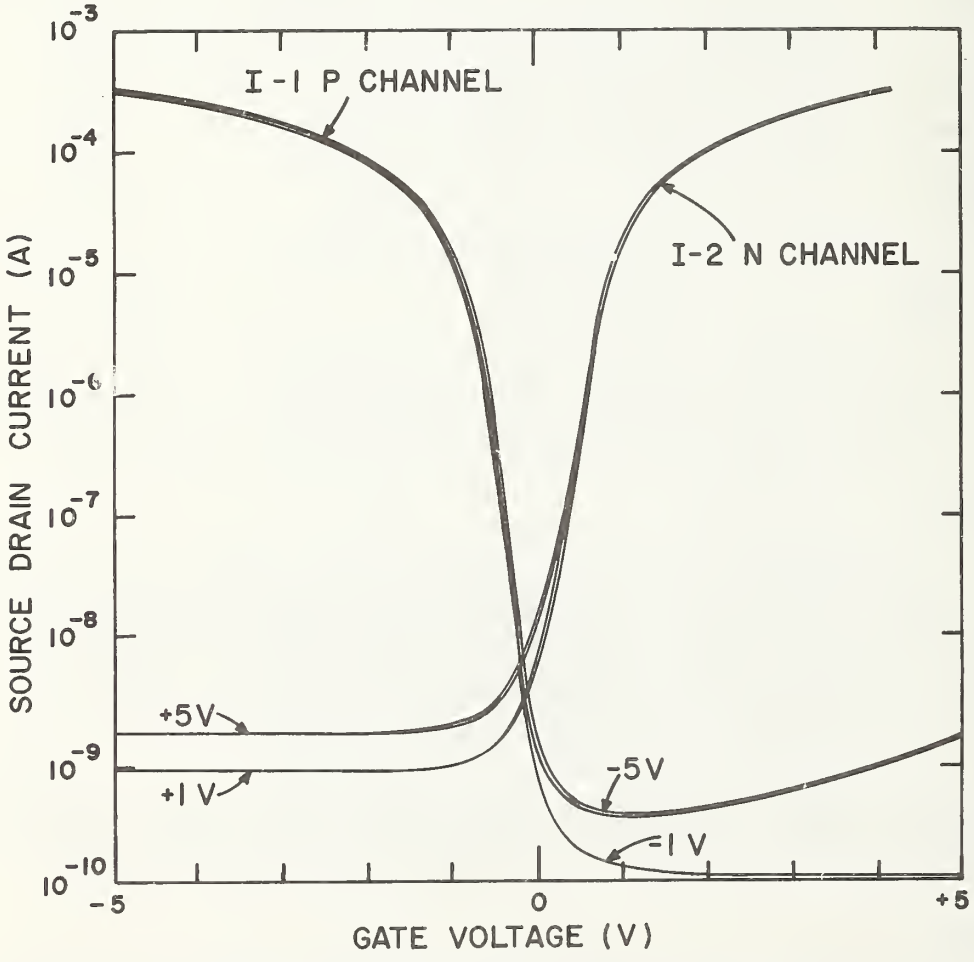


Figure 35. Log gate transfer characteristics of structures I-1 and I-2.

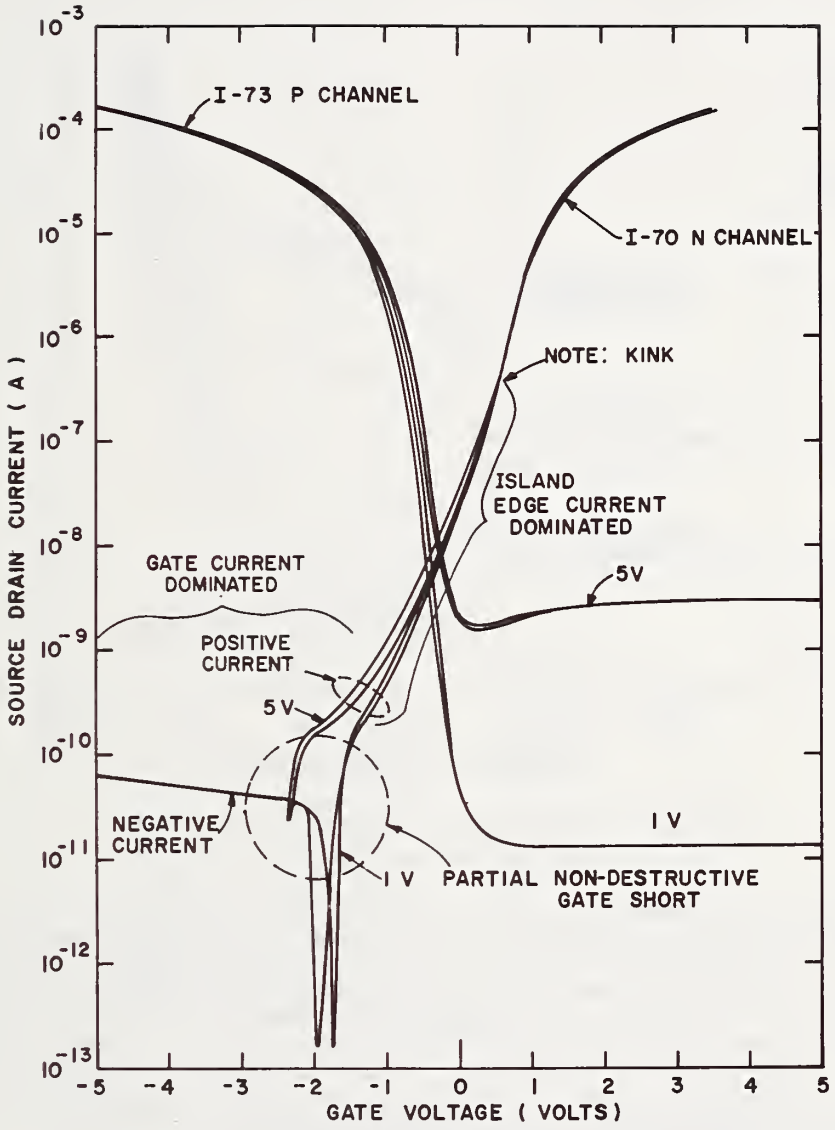


Figure 36. Log gate transfer characteristics for two devices with edges at constant drain voltage. The hysteresis effects are due to carrier trapping properties of the device; they are not caused by instrumentation. Note low-level errors caused by gate conduction for the n-channel device.

(4) Testing Method - Drain Breakdown - Drain breakdown is defined for the purposes here as that drain voltage required to produce a certain drain current at a specified gate voltage. The gate voltage would usually be specified such that no channel exists or such that a nominal off state is achieved. This method again completely bypasses the need for detailed understanding of the mechanism involved. For the SOS case there is evidence that drain breakdown does not proceed in the same manner as for bulk silicon devices, particularly for the n-channel device. One reason for this is that the current does not have a thick substrate to use for current transport between source and drain. Other reasons are probably related to the defect nature of the silicon. In any case, it is

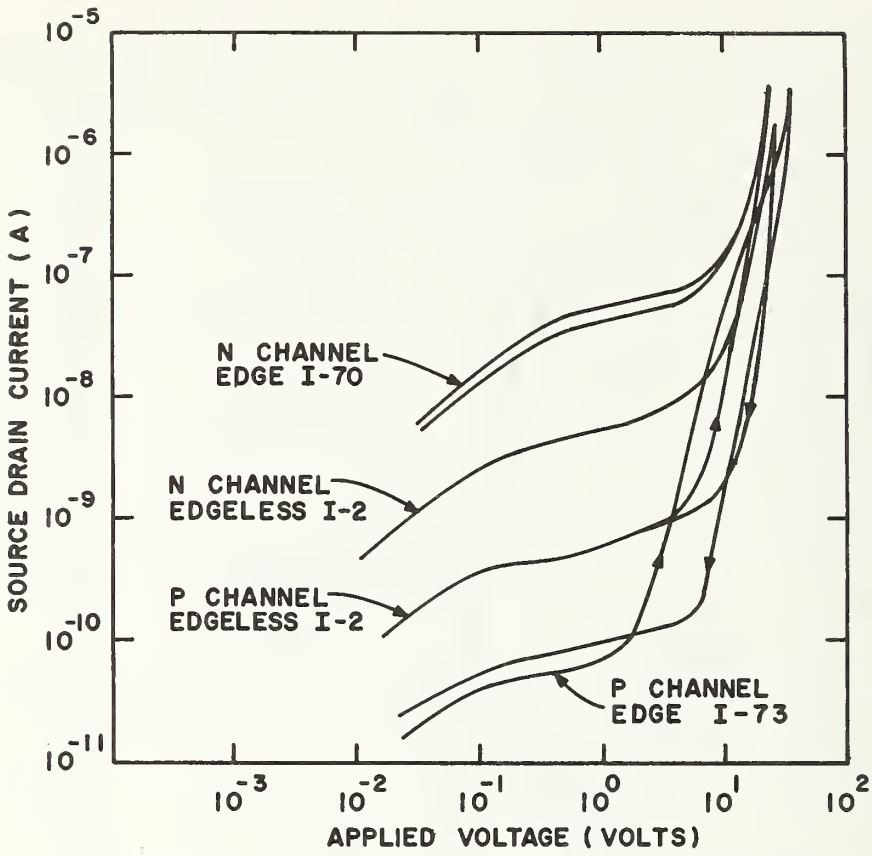


Figure 37. Drain leakage currents at zero gate voltage for various transistors.

usually seen for the HCl steam-grown silicon dioxide gates used for the devices investigated here that very substantial changes in the voltage can exist after applying a high voltage as seen in figure 41. (This may be related to avalanche injection into the oxide near the drain.) These changes are primarily a function of the voltage applied but also depend on the time of application of the bias. Rather than try to perform detailed measurements of this region (which is frequently not of first-order importance to the circuit), we have chosen to simply measure the voltage required to produce a certain current after a certain time. This method provides a solid base from which comparisons can be made. We note that if the current level is sufficiently high (>1 μA, for example), the measured voltage is almost independent of the current level.

Initial Parameters

- Low current drain breakdown level (IDBDL)
- High current drain breakdown level (IDBDH)
- Time for application of high current (THC)

Flow Chart

- Measure V_D with $\left\{\begin{matrix} V_G = (\text{VGOFF}) \\ I_D = (\text{IDBDL}) \end{matrix}\right\}$ (LCBVD)

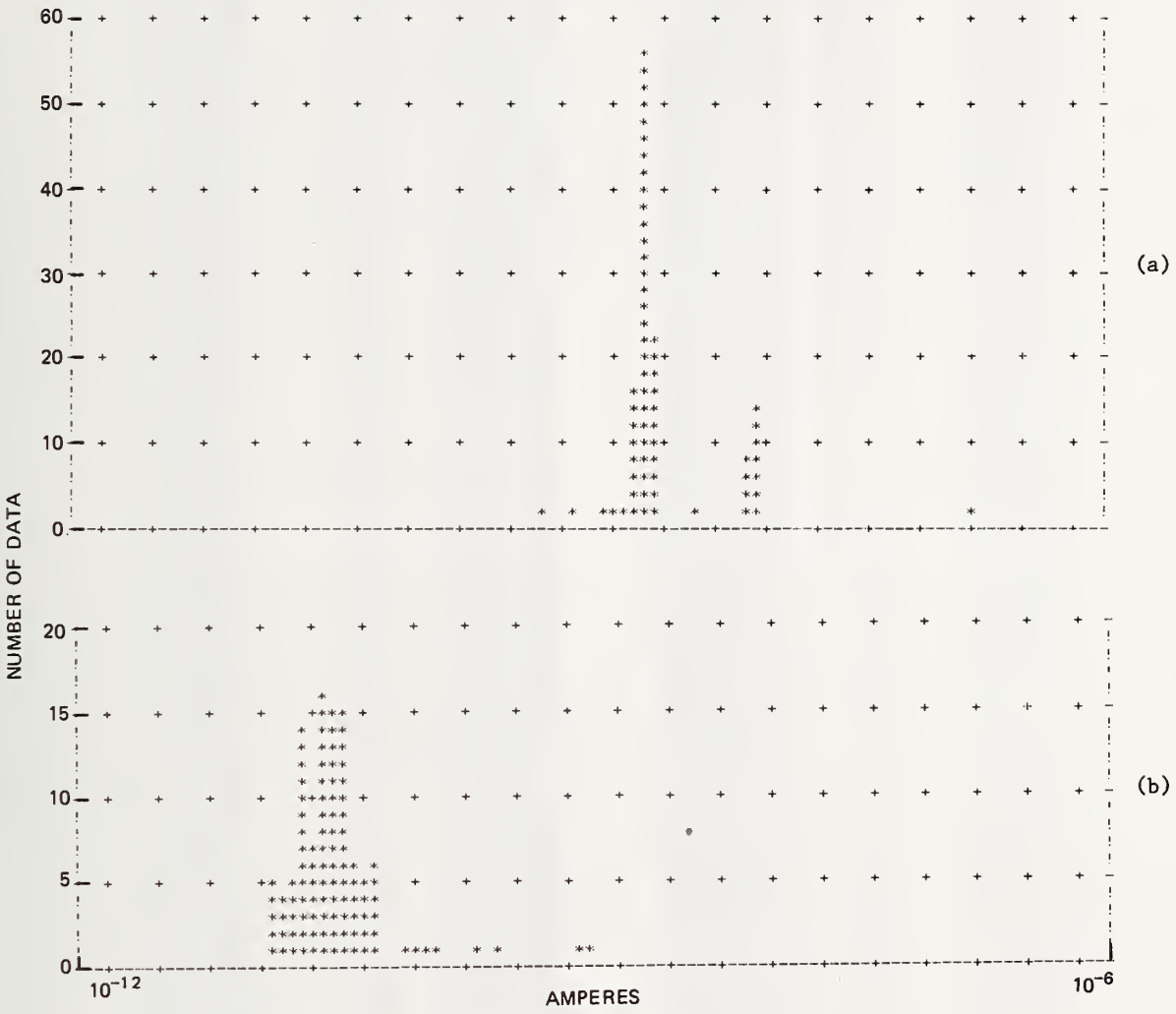


Figure 38. (a) Gate current at 10 V measured by system meter.
(b) Drain leakage current at 5 V measured by low current system.
Log scales are used between 10^{-12} and 10^{-6} A.

- Measure V_D with $\left\{\begin{matrix} V_G = (VGOFF) \\ I_D = (IDBDH) \end{matrix}\right\}$ (HCBVD)
- Measure V_D after applying (VGOFF), and (IDBDH) for (THC): (HCBVDC)

List of Outputs

- Low level drain breakdown (LCBVD)
- High level drain breakdown (HCBVD)
- High level drain breakdown after (THC): (HCBVDC)

49 CHIPS FOR TEST 26

	CATEGORY	TEST RESULT	X POSITION	Y POSITION	SORTED DATA
1	4	.48196E-10	500	500	.44979E-10
2	4	.12532E-09	499	500	.48196E-10
3	4	.11508E-09	498	500	.50351E-10
4	4	.80539E-05	497	500	.50584E-10
5	4	.88310E-10	496	499	.51524E-10
6	4	.10666E-09	497	499	.52968E-10
7	4	.12942E-09	498	499	.55209E-10
8	4	.16558E-09	499	499	.57413E-10
9	4	.16033E-09	500	499	.63389E-10
10	4	.19907E-09	501	499	.75338E-10
11	4	.11669E-09	502	498	.78345E-10
12	4	.13490E-09	501	498	.80356E-10
13	4	.16144E-09	500	498	.82988E-10
14	4	.10965E-09	499	498	.83949E-10
15	4	.10186E-09	498	498	.84530E-10
16	4	.84530E-10	497	498	.87703E-10
17	4	.87703E-10	496	498	.88310E-10
18	4	.82988E-10	495	498	.91414E-10
19	4	.83949E-10	495	497	.93544E-10
20	4	.57413E-10	496	497	.95282E-10
21	4	.91414E-10	497	497	.98404E-10
22	4	.10765E-09	498	497	.10070E-09
23	4	.16181E-09	499	497	.10186E-09
24	4	.25469E-09	500	497	.10399E-09
25	4	.17419E-09	501	497	.10666E-09
26	4	.93544E-10	502	497	.10765E-09
27	4	.55209E-10	502	496	.10790E-09
28	4	.19231E-09	501	496	.10965E-09
29	4	.33190E-09	500	496	.11508E-09
30	4	.18072E-09	499	496	.11669E-09
31	4	.12023E-09	498	496	.12023E-09
32	4	.10399E-09	497	496	.12532E-09
33	4	.80356E-10	496	496	.12942E-09
34	4	.78345E-10	495	496	.12972E-09
35	4	.75338E-10	496	495	.13490E-09
36	4	.95282E-10	497	495	.13615E-09
37	4	.10790E-09	498	495	.16033E-09
38	4	.12972E-09	499	495	.16144E-09
39	4	.31262E-09	500	495	.16181E-09
40	4	.17022E-09	501	495	.16558E-09
41	4	.50351E-10	502	495	.17022E-09
42	4	.44979E-10	501	494	.17419E-09
43	4	.13615E-09	500	494	.18072E-09
44	4	.98404E-10	499	494	.19231E-09
45	4	.10070E-09	498	494	.19907E-09
46	4	.63389E-10	497	494	.25469E-09
47	4	.50584E-10	496	494	.31262E-09
48	4	.52968E-10	498	493	.33190E-09
49	4	.51524E-10	499	493	.80539E-05

Figure 39. IDL10 (see figure 34) at VD = 1.0 V, VG = 2 V (structure I-70). The test result represents IDL10 in A.

Less General Versions

- General test (DRBD1)
- Single current level (DRBD2)

Special Equipment

No special equipment is required for these tests.

Samples of Data

Data acquired from structure I-70 is shown in figure 41. These data were acquired at 1.0 μA for a short time in part A and at 50 μA for approximately 100 ms in part B. A drastically different distribution is seen as might be expected from the analog plot of

VTLLO49 CHIPS FOR TEST 31

	CATEGORY	TEST RESULT	X POSITION	Y POSITION	SORTED DATA
1	4	-.13283E 01	500	500	-.17353E 03
2	4	-.13201E 01	499	500	-.27898E 01
3	4	-.13997E 01	498	500	-.27519E 01
4	4	-.17353E 03	497	500	-.23412E 01
5	4	-.99013E 00	496	499	-.22281E 01
6	4	-.18550E 01	497	499	-.21471E 01
7	4	-.20801E 01	498	499	-.20801E 01
8	4	-.12244E 01	499	499	-.20672E 01
9	4	-.14228E 01	500	499	-.20668E 01
10	4	-.19796E 01	501	499	-.20634E 01
11	4	-.20634E 01	502	498	-.20041E 01
12	4	-.15459E 01	501	498	-.19796E 01
13	4	-.15552E 01	500	498	-.19730E 01
14	4	-.12861E 01	499	498	-.19281E 01
15	4	-.15098E 01	498	498	-.19125E 01
16	4	-.10755E 01	497	498	-.18710E 01
17	4	-.92081E 00	496	498	-.18550E 01
18	4	-.90238E 00	495	498	-.18417E 01
19	4	-.60114E 00	495	497	-.18056E 01
20	4	-.79352E 00	496	497	-.18011E 01
21	4	-.12186E 01	497	497	-.17472E 01
22	4	-.18417E 01	498	497	-.16657E 01
23	4	-.18710E 01	499	497	-.15552E 01
24	4	-.21471E 01	500	497	-.15459E 01
25	4	-.22281E 01	501	497	-.15098E 01
26	4	-.16657E 01	502	497	-.14562E 01
27	4	-.14562E 01	502	496	-.14228E 01
28	4	-.27519E 01	501	496	-.13997E 01
29	4	-.27898E 01	500	496	-.13283E 01
30	4	-.20668E 01	499	496	-.13201E 01
31	4	-.19281E 01	498	496	-.13054E 01
32	4	-.17472E 01	497	496	-.12861E 01
33	4	-.11063E 01	496	496	-.12244E 01
34	4	-.11656E 01	495	496	-.12186E 01
35	4	-.13054E 01	496	495	-.12154E 01
36	4	-.18056E 01	497	495	-.11656E 01
37	4	-.20672E 01	498	495	-.11639E 01
38	4	-.18011E 01	499	495	-.11063E 01
39	4	-.20041E 01	500	495	-.10755E 01
40	4	-.23412E 01	501	495	-.99013E 00
41	4	.13240E 02	502	495	-.92081E 00
42	4	.13184E 02	501	494	-.90238E 00
43	4	-.19125E 01	500	494	-.79352E 00
44	4	-.12154E 01	499	494	-.60114E 00
45	4	-.19730E 01	498	494	.13184E 02
46	4	-.11639E 01	497	494	.13200E 02
47	4	.13200E 02	496	494	.13240E 02
48	4	.13322E 02	498	493	.13322E 02
49	4	.13367E 02	499	493	.13367E 02

Figure 40. VTLLO (see figure 34) at VD = 1.0 V (structure I-70). The test result represents VTLLO in V.

figure 37. Clearly the application would dictate the testing parameters which should be used. The population above the center peak is due to open circuits (≈40 V was the maximum possible voltage for this test).

(5) Testing Method - Saturation Characteristics: The Kink - As mentioned before, the drain characteristics of SOS transistors usually do not exhibit the simple form commonly found on bulk silicon transistors. (It is possible to produce bulk silicon transistors which have characteristics similar to those of SOS transistors by leaving the substrate potential floating.) There is a very simple method for measuring the magnitude of the kink as illustrated in figure 42. In this case the slope of the drain characteristic at a specified gate voltage is measured as a function of drain voltage. As one proceeds from an initial starting point toward higher drain voltages, the slope decreases monotonically until the kink is reached. At this point the second derivative of the curve changes sign. After this point two types of behavior are seen on different devices. In the simplest case the second derivative will change sign only once; this type is characterized by the

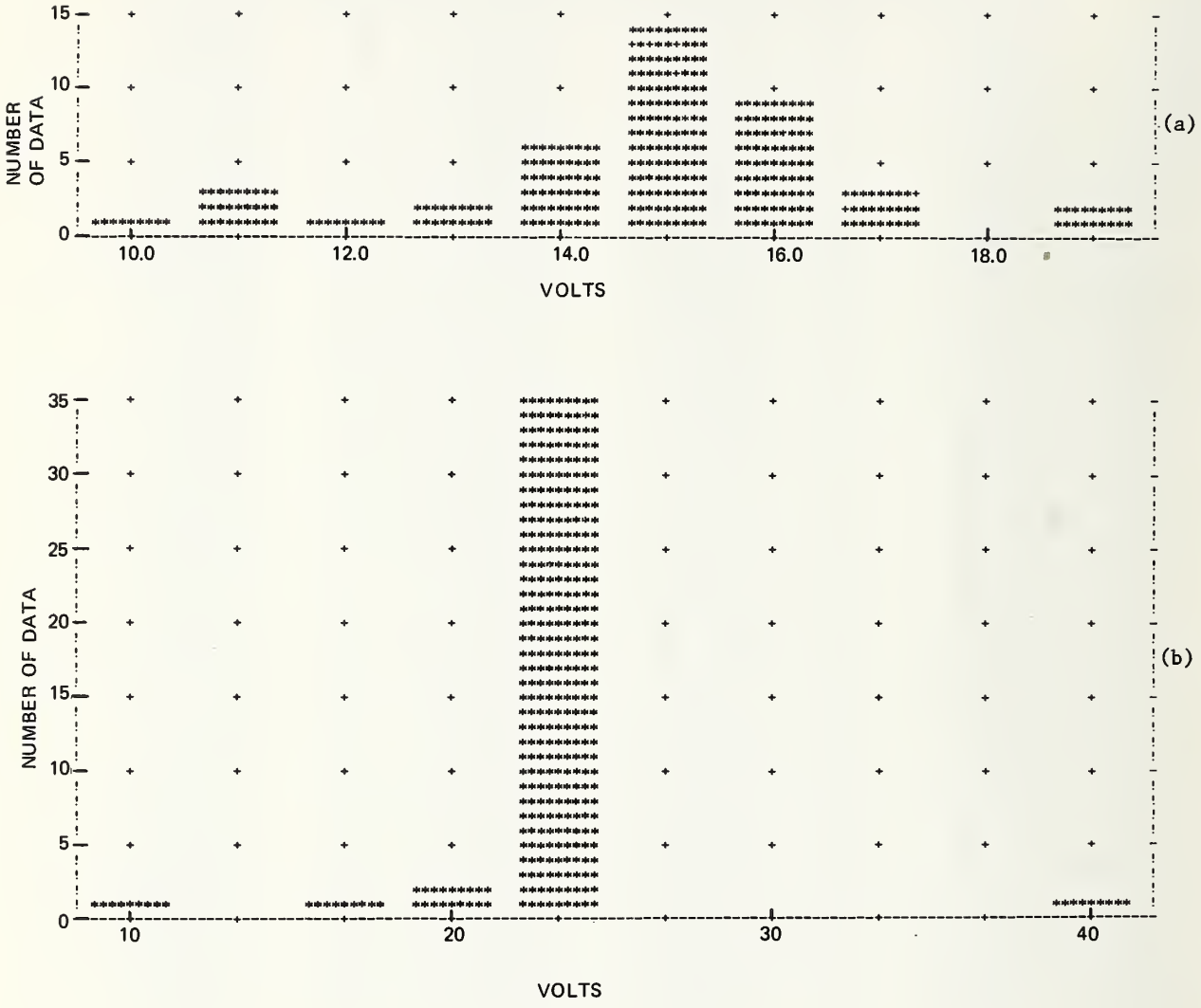


Figure 41. Drain breakdown voltages under different testing conditions, (a) low current short time, (b) high current long time.

ratio of the slope just before the kink to that at a specified gate voltage higher than the kink voltage. This voltage difference is arbitrarily specified at 1 V for the program described here. In other words if the second derivative changes sign only once:

$$KINKFO = \frac{GDMIN1}{GD\big|_{VG = VGKINK + 1}} \tag{11}$$

Of course it is possible and is sometimes found that the second derivative does not change sign in the drain voltage range of interest. In this case no kink exists and testing is halted after the maximum drain voltage is reached.

When the second derivative first changes sign, the drain voltage increment is decreased in order to search carefully for a second change of sign in the second derivative. We have chosen to decrease the stepping rate by 10X as shown in figure 42. This decrease can cause errors because of inaccurate current readings if the kink is small, but it is

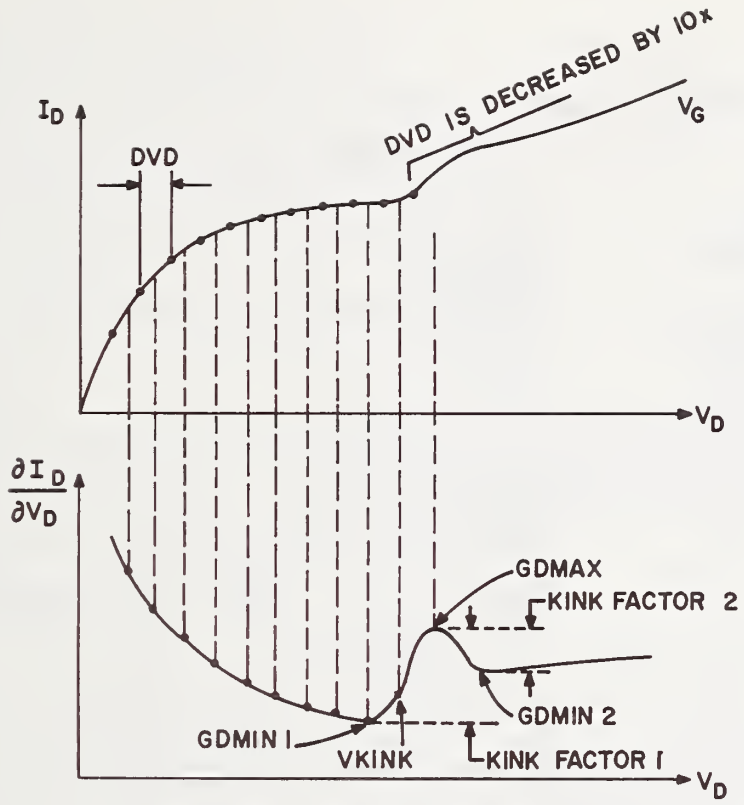


Figure 42. Measurement and parameters derived from nonideal drain characteristics.

necessary in order to find the second kink if it exists. If a second kink is not found within 1 V of the first kink, the testing is halted. If a second kink is found the following parameters are calculated.

$$\text{KINKF1} = \frac{\text{GDMIN1}}{\text{GDMAX}} \tag{12a}$$

$$\text{KINKF2} = \frac{\text{GDMIN2}}{\text{GDMAX}} \tag{12b}$$

These three kink factors quantify the kink behavior of any transistor. We note that the algorithm required for these procedures is relatively complicated.

The measurements are indicated as results of dc stimuli. For this particular measurement the use of small-signal ac stimuli to obtain the GD-VD data directly has a significant advantage in that the noise level of the measurement can be greatly reduced.

The basic method would not change. Many testers do not have the capability of supplying and detecting these ac signals.

Initial Parameters

- Gate voltage for measurement (VGKINK)
- Initial drain voltage (VDINIT)
- Drain voltage increment (DVD)

Flow Chart

The flow chart is shown in figure 43.

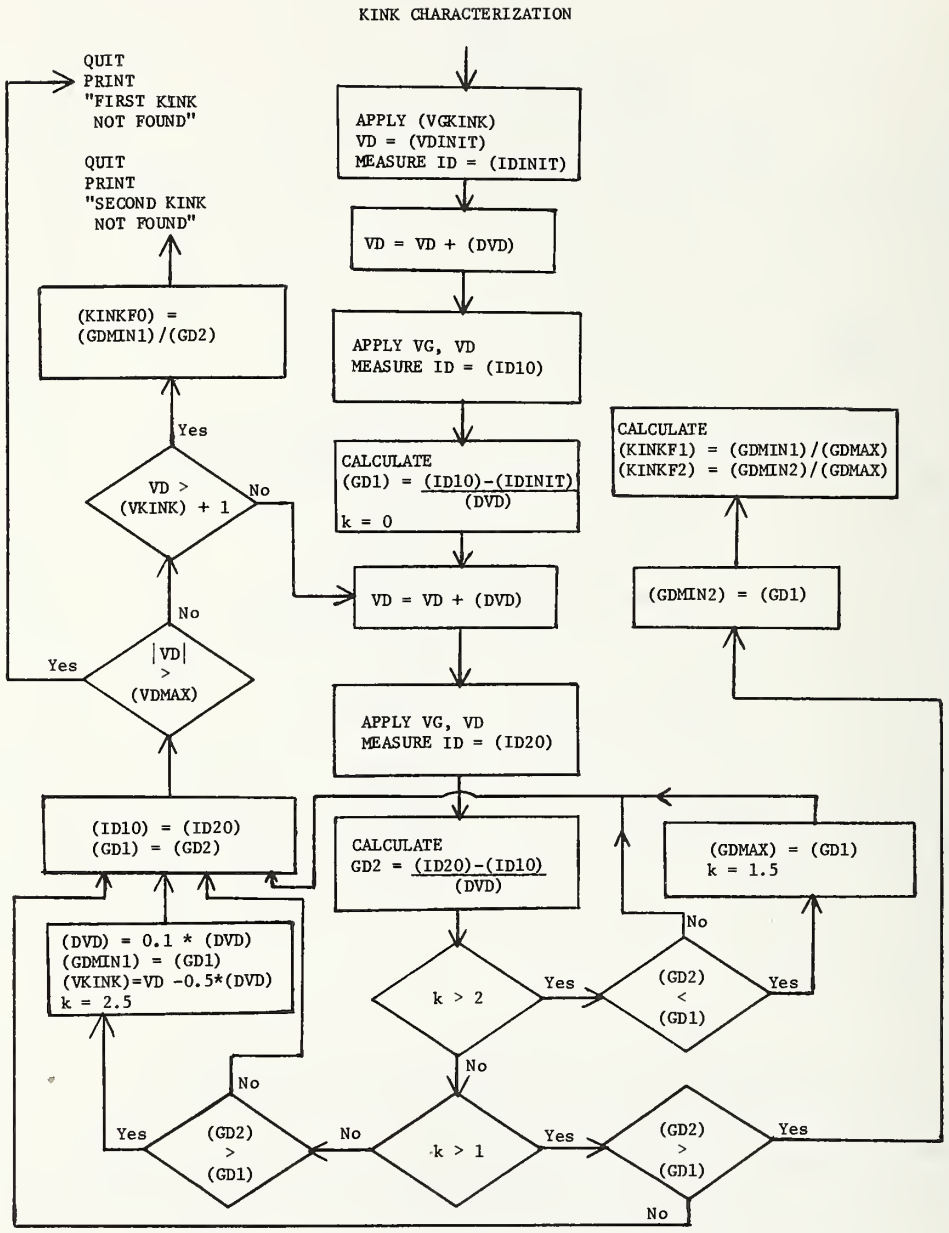


Figure 43. Kink characterization flow chart.

List of Outputs

- First kink voltage (VKINK)
- Minimum output conductance (GDMIN1)
- Peak output conductance (GDMAX)
- Second minimum in output conductance (GMIN2)

- Kink factor for only one kink (KINKF0)
- Kink factor for first kink when a second kink is found (KINKF1)
- Kink factor for second kink (KINKF2)
- Voltage for second kink (VD)

Less General Versions

No other versions currently exist.

Special Equipment

The current meter must be able to resolve the differences in current observed when DVD is decreased to 0.1 * DVD. This is primarily a resolution problem in the A-D system but is not a severe constraint if the current reading is not noisy since all measurements are made on the same meter and the same device with precisely the same connections and usually the same meter ranges. If noise is a problem, several readings will have to be taken and averaged to produce a usable reading.

Samples of Data

No data have been acquired from this program to date.

(6) Testing Method - Post-Test Suitability - After testing has been accomplished on the structure, it is usually desirable to determine if the testing procedure changed the properties of the device. This may be done by retesting with any of the previous tests or more commonly by repeating the initial suitability tests. No dedicated test blocks have been created specifically for determining post-test properties. A convenient way to distinguish between an initial test and a post-test is to prefix the test block name with a PST when it is used as a post-test.

Potential Pitfalls - This structure provides an average reading over the entire family of theta orientations possible. It therefore may not scale exactly with single orientation devices. The geometry of the gate is not easy to analyze near the aluminum contact. For optimum results most currents should be measured in the center portion since the current at that point *must* flow through the device. The gate pad is located over field oxide, and therefore one must consider that a weak gate may be due to the field oxide instead of the channel oxide. This field oxide is normally much thicker than the channel oxide; however, the field oxide is of larger area than the channel and is subject to pinhole formation during the contact etch.

Overall Usefulness - This structure is very useful for separating effects due primarily to the edges of the islands. Its usefulness could have been markedly improved if a structure identical to this one but with a small slit cut in the silicon to provide two edges without substantially altering the other geometries (figure 44) had been provided. (A family of these structures with slits cut at various angles could also be used to study the effects of theta rotation on the edge properties. This function is available from other structures, however.) It is also possible to form a small internal contact. This structure is slightly more complicated than the one used and cannot be used to make metal gate devices (figure 45).

Other Related Structures - All MOS transistors on the pattern are very closely related to this structure. The basic operation and testing procedure used would be identical.

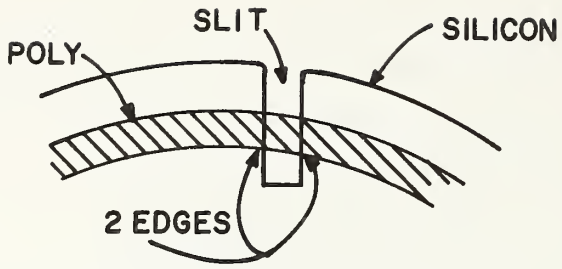


Figure 44. Improved edge structure.

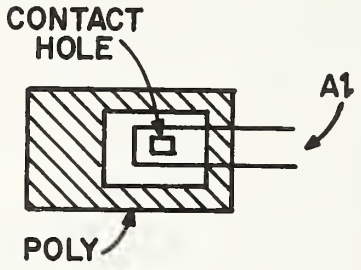


Figure 45. Small edgeless structure.

3.2 Gate-Controlled Bridge Resistors - I-5, I-6

Purpose - The purpose of this structure is to measure epitaxial resistance under controlled surface conditions.

Verbal Description - These structures are of the standard bridge shape with the width of the bars being 1.0 mil and the separation between the center lines of the potential probes being 4.0 mil. The potential probes are 0.2 mil wide. A p^+ polysilicon gate (p^- poly in the bar with the n^+ contacts - structure I-5) covers the entire active area of the bars.

Line Drawing - The line drawing for this structure is shown in figure 46.

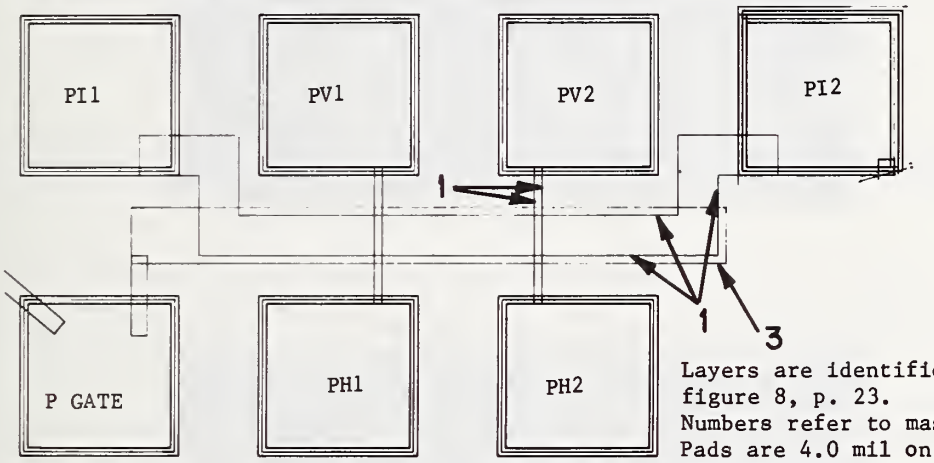


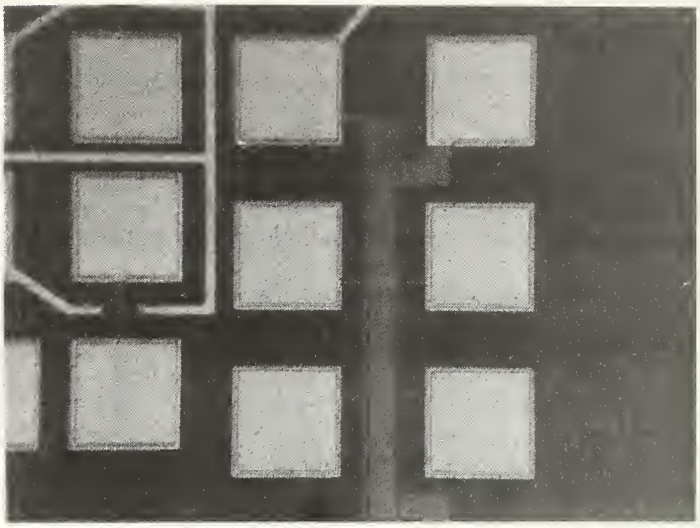
Figure 46. Gate-controlled bridge resistor, test structure I-5, computer line drawing.

Halftone Photograph - The photomicrograph for this structure is shown in figure 47.

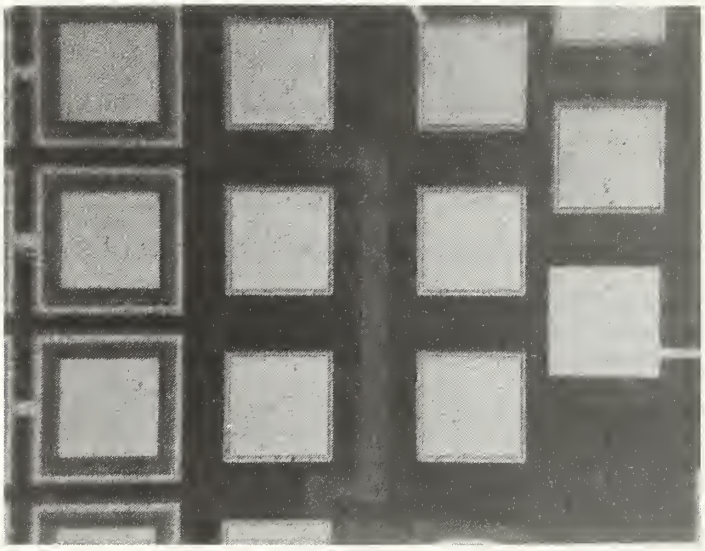
Electrical Access Points - This structure has seven electrical access points in addition to the implied isolation points of the substrate and neighboring devices. These are all standard pads with PGATE being a poly pad. These points are designated:

- PI1 - current contact
- PV1 - potential probe
- PV2 - potential probe
- PI2 - current contact
- PGATE - gate
- PH1 - Hall or transverse potential contact
- PH2 - Hall or transverse potential contact

Testing Method - This structure is tested by fixing the gate potential at some predetermined value, either forming or measuring the current through PI1 and PI2 and measuring the resulting voltage across any set of two voltage probes. This is the normal method although any potential may be measured for specific purposes. Although it is possible to use any reasonable voltage between PI1 and PI2, the presence of a gate will create nonuniform vertical fields distributed throughout the structure with resulting nonuniform conductivity at high applied voltages. This structure is also useful for diagnosing the field distribution in the silicon at high applied voltages, but this use will not be discussed further at this point. For proper operation of this structure the applied voltage should be such that the voltage measured across PV1 and PV2 is approximately one-fourth of the applied



(a)



(b)

Figure 47. Photomicrographs of gate-controlled bridge resistors; (a) n^+ contacts (I-5), (b) p^+ contacts (I-6).

voltage. Under these conditions the applied potential is nearly uniformly distributed between the current contacts. The voltage across the gate dielectric (and surface space-charge region if present) will be nonuniform by an amount equal to the voltage between PV1 and PV2 and will be equal to the applied gate voltage minus the potential between the voltage probes and the grounded current contact. Notice that a high contact resistance can alter the apparent vertical field being applied and that this can cause substantial errors at high applied voltages. The best method is to use an applied voltage such that an error in the gate voltage equal to this voltage does not cause a substantial error in the measured result. If the device has good contact, one can use a slightly higher applied voltage, but even in the best case two-thirds of the applied voltage will appear as a difference between the applied gate voltage and the grounded current terminal near one of the potential probes. Typically applied voltages of less than 100 mV are suggested. This produces a measured voltage of $\sim$25 mV.

The potential between the opposite voltage probes (PV1 and PH1) can be used as a check on the isotropy of the conductivity of the material. This is done by applying constant voltage or current to PI1 and PI2 and measuring the potential (PV1, PH1) at different gate voltages. If the potential varies non-monotonically with gate voltage or is larger than could be accounted for by the physical displacement of the arms, it is due to anisotropic conductivity as discussed, for example, in refs. 9 and 14. PH1 and PH2 are also useful for making Hall voltage measurements. We note that anistropic conductivity will not affect the measured Hall voltage since the drive for the Hall voltage is a magnetic field.

The potential between the voltage probes (PV1 and PV2) is used to infer the sheet resistance of the material at the gate voltage being used. This sheet resistance is given by

$$\rho_S = \frac{V_{12}}{I} \quad \frac{W}{L} \tag{13}$$

where W is the width of the silicon (1.0 mil in this case) and L is the distance between the centerlines of the voltage probes (4.0 mil). There is usually little problem with measuring V_{12} or I. L is defined by the mask geometry only (typically actual dimensions are accurate to better than 50 μin.).

Since the centerline position is the required dimension, L is not affected by image transfer or etching techniques. On the other hand, W is determined primarily by these techniques. One therefore will find the primary error in this measurement (at any given gate potential) to be due to not knowing W accurately. Clearly, as W is decreased, the error increases. W cannot be made arbitrarily large for several reasons, the most important being that the uniformity of current flow becomes the dominant unknown when the current is not confined between relatively narrow known boundaries. A compromise value of 1.0 mil was therefore chosen since this can be reasonably accurately produced with most processes and does not result in an unduly large structure.

It is of critical importance that the gate not contribute substantially to the current since this would cause first-order errors in the results. It is also of critical importance that the structure be isolated from its surroundings - from both the substrate material and from neighboring devices. If the device is junction-isolated, all voltages must be such that the junction properties are not violated. This is not a particular problem for SOS devices but it is of first-order importance to bulk silicon measurements.

The basic method for obtaining data at a particular gate voltage is described in detail in subsection 3.11 below.

One of the most important properties of this structure is that one can control the charge concentration of the surface of the film by changing the gate voltage. This gives the ability to measure parameters other than sheet resistance by noting the dependence of the sheet resistance on the gate voltage. For example, it is possible to control the depth of the surface space-charge layer* by biasing the surface into depletion. For thick SOS films (>0.8 μm, for example) this controlled depletion provides some information about the depth resistivity profile in the film. For films of typical device thickness (<0.6 μm) interpretation of nonphysical profiles (i.e., electrical depth profiles) is difficult at best because of their defect density. This limits the testing area of importance for device-quality films to the surface electrical properties. The surface is the important part of the film for MOS devices in any case, and the interpretations to be made are not particularly difficult.

If the conductivity of the surface is proportional to the number of free charges, than $\Delta\sigma_S \propto \Delta Q_S$. Similarly ΔQ_S is given by Gauss' law $\Delta Q_S \propto \Delta VG$ where VG is the gate voltage.

*If such a layer exists. It is not always clear that defects in the silicon are not responsible for data that would normally be interpreted as space-charge layers [14].

14. Ham, W. E., "The Electrical Characterization of Heteroepitaxial Semiconducting Films," Chapter 6, *Heteroepitaxial Semiconductors for Electronic Devices*, Ed. G. W. Cullen and C. C. Wang, pp. 216-263 (Springer-Verlag, New York, 1978).

The proportionality factor between σ_S and Q_S is defined as the surface or field effect mobility (μ_S or FEM) and the proportionality between Q_S and VG is the gate capacitance, C.

$$\mu_S = \frac{\Delta\sigma_S}{C\Delta VG} \tag{14}$$

This parameter is easily measured by measuring σ at two closely spaced values of VS. It is found that this parameter is not constant for different values of VG and therefore casts very substantial uncertainty on the validity of the simple models mentioned in the last section. This is a beautiful example of using models mainly for small-signal variations.

The gated bridge resistors therefore are measured exactly like ungated bridge resistors except that the gate voltage must be specified and the gate current must be considered.

It is also possible to measure the mobility of the surface charges with this structure using a Hall effect method. This is primarily useful to define a trapping ratio, TR:

$$TR = \frac{\mu_S}{\mu_H} \tag{15}$$

where μ_H is the Hall mobility. This factor is good only to the accuracy of the Hall scattering factor. The primary purpose of this ratio is to determine whether trapping or surface scattering is dominating μ_S. If TR $\approx$ 1.0, then surface scattering is dominant. If TR < 1.0, then trapping is important. Since Hall measurements are difficult to automate, this approach has not been tested here.

*Initial Parameters** -

- Maximum gate current (IGMAX)
- Gate voltage for high conductivity (VGHICON)
- Gate voltage for low conductivity (VGLOCON)
- Equivalent thickness of thermal SiO_2 (TOX)

Flow Chart - The flow chart for this structure is shown in figure 48.

List of Outputs - All outputs from the test described below are available. In addition:

- Gate current (IG)
- Field effect mobility (FEMBRRES)

Less General Versions -

- Complete (uses complete sheet resistance program) GBRRES1
- Production version GBRRES2

This version is like the complete version but uses very simple single measurements for sheet resistance.

Special Equipment - This structure requires a floating voltage sensing system if only one voltage measurement is to be performed to obtain the potential difference between PV1 and PV2. This sensing system should have low capacitance, high resistance inputs. The exact values required must be determined experimentally by noting the value of sheet resistance required to change the voltage reading. Typically we have used input impedances from 10^9 to 10^{12} ohm. For most applications 10^9 ohm is sufficient.

*In addition to those described in subsection 3.11 below.

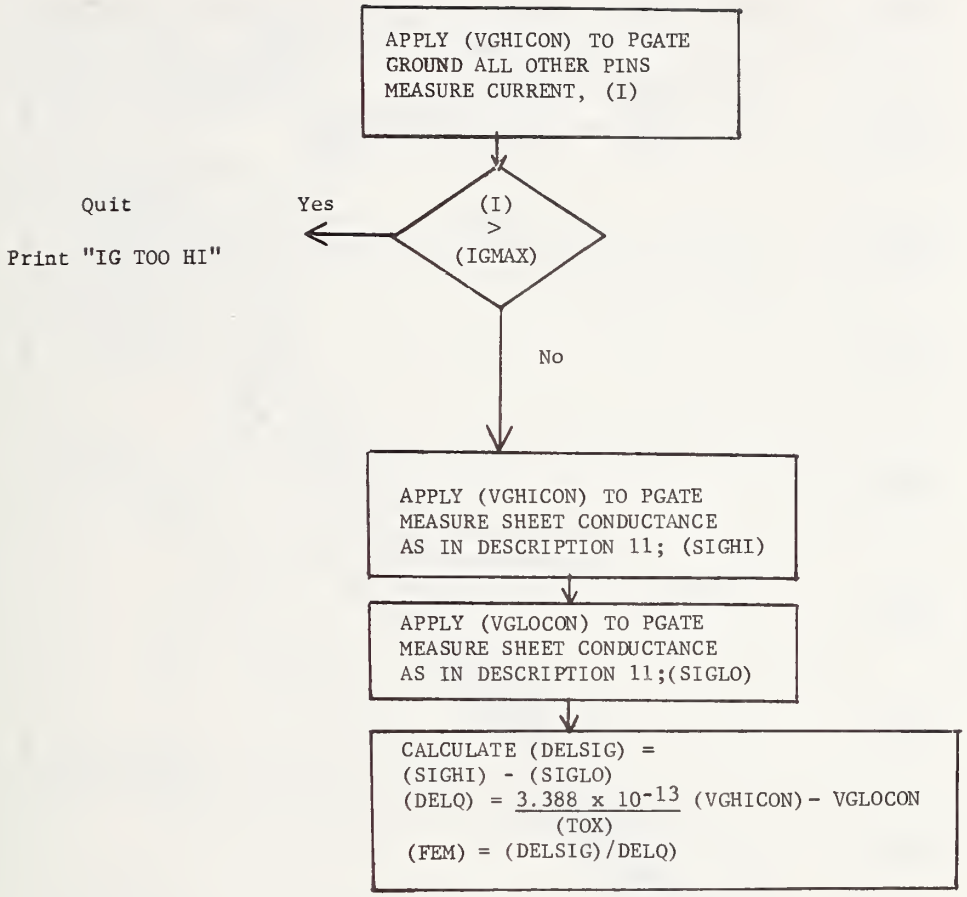


Figure 48. Flow chart for GBRRES1.

Samples of Data - A plot of the voltage between PV1 and PV2 (V_{12}) versus the gate voltage is shown for various applied voltages in figure 49. Note that only at low applied voltages does the measured V_{12} agree with geometrical voltage division over the entire gate voltage range considered. A linear dependence on applied voltage is seen at high applied voltages. As the surface becomes more heavily charged, the geometrically expected voltage is reached. This behavior is due to pinch-off effects near the applied voltage terminal. As the surface becomes very heavily charged, the potential becomes linearly distributed along the length of the structure. Since the silicon potential distribution is not predictable before measurement and, more importantly, since the effects on the vertical field are not negligible, the best region of operation is at applied voltage <100 mV. When the surface charge is lost due to insufficient gate field, V_{12} becomes unstable, indicated by a dashed line in figure 49. This behavior is caused by the silicon becoming too resistive to drive the voltage sensing lines. This is another example of the difficulty of attempting to measure the nonsurface properties of a thin-film structure of this type.

Another plot of μ_S (FEM) as a function of gate voltage is shown in figure 50. Here two nominally identical wafers were used, and the measurements were performed manually. The total current and V_{12} values were read for each gate voltage. V_{12} was read to four places and is not significantly in error. VG was set to 3.5 digits and I was measured with an analog current meter. 100 mV was applied and VG was changed in 0.5-V increments in all cases. Both structures I-5 and I-6 were measured. Those structures with p^+ contacts were supplied with negative gate voltage while those with n^+ contacts were supplied with positive gate voltages. Both polarities are plotted as positive in figure 50. Several points in this figure are worthy of discussion.

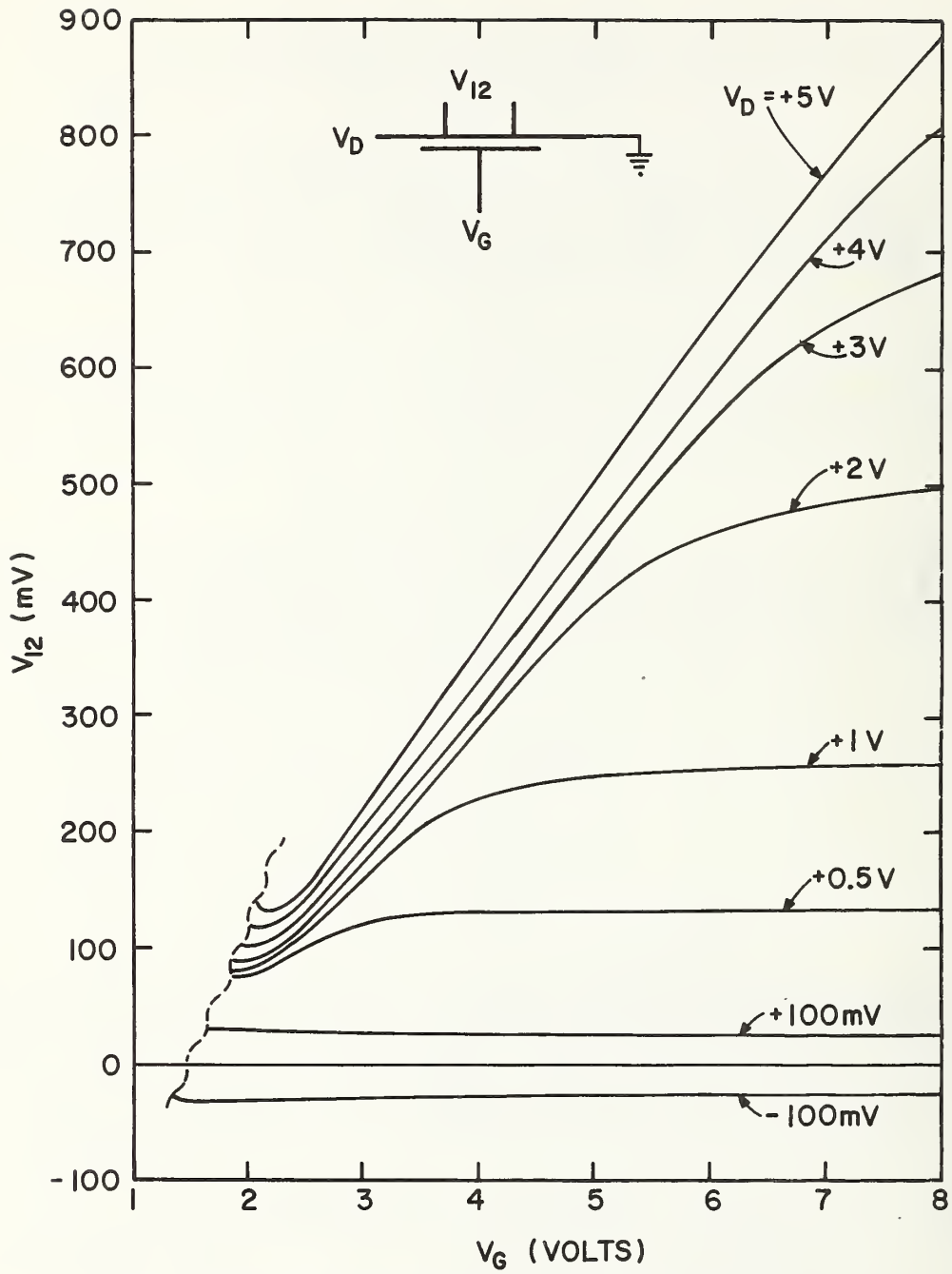


Figure 49. Dependence of V_{12} on the applied voltage and on the gate voltage. TOX is approximately 1000 Å.

The surface mobility is definitely not constant as a function of gate voltage. More importantly it is not even functionally the same for the two wafers. This clearly indicates that a constant parameter model cannot be used with respect to the gate voltage for the field-effect mobility and that any attempt to incorporate a specific functional form into the model will be invalid for some wafers.

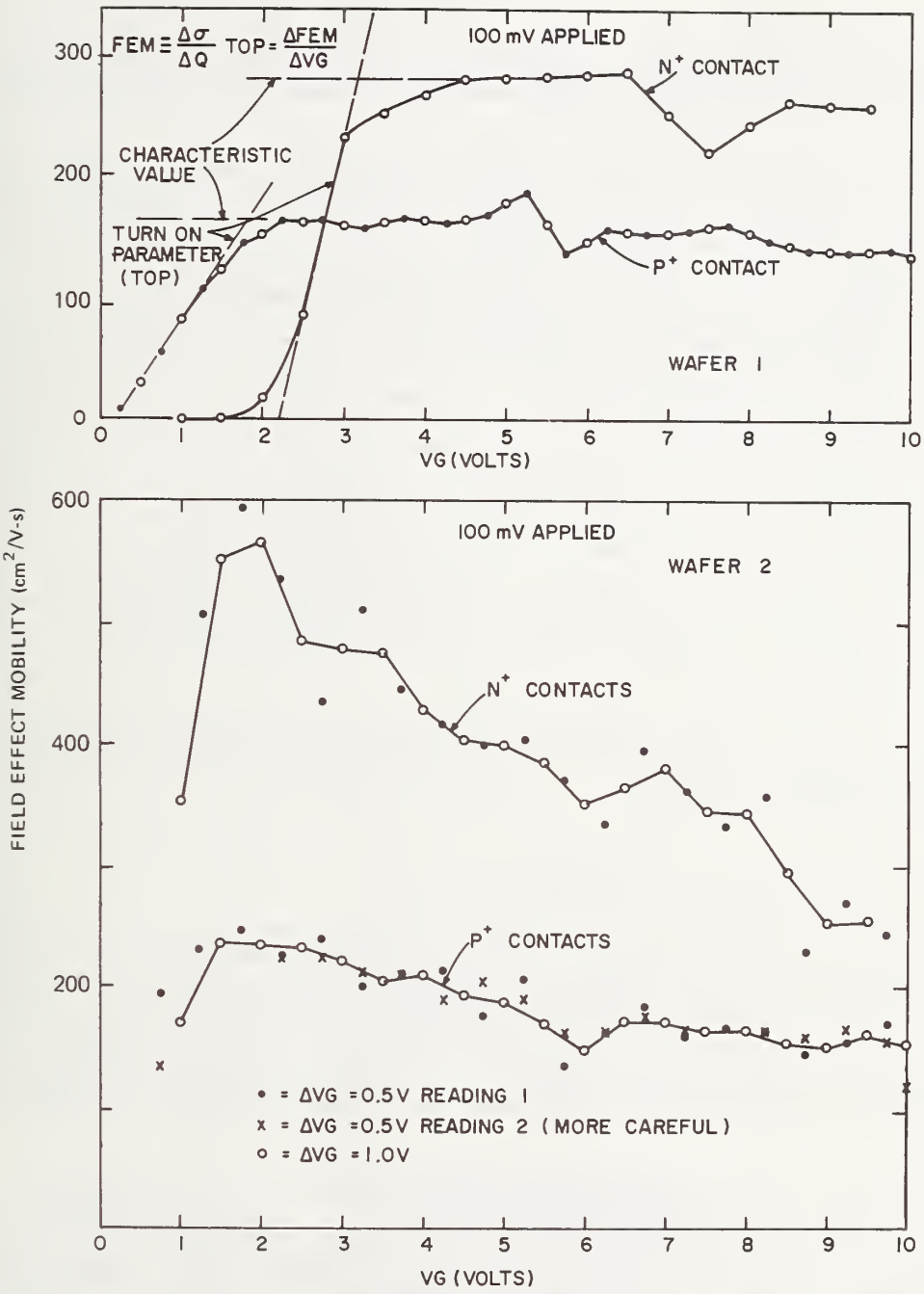


Figure 50. Field-effect mobilities as function of gate voltage.

We also note a considerable scatter in the data. This scatter is due almost entirely to the inability to read precisely the analog meter used for these data. This was investigated for the p^+ contact device from wafer 2. In this plot three sets of data from the same device are plotted. Data were first acquired by attempting to extract only three digits from the current meter. Another set was gathered attempting to read the analog meter to 3.5 to 4 places. The initial set of data was used to complete μ_S at $\Delta VG = 0.5$ V; this is indicated by solid points. This same set of data was used to calculate μ_S at $\Delta VG = 1.0$ V. This is indicated by the open points. The second set of data was used to compute the X's at $\Delta VG = 0.5$ V. Clearly there is much less scatter with $\Delta VG = 1.0$ V or with the more careful current measurements. The lines are drawn through the $\Delta VG = 1.0$

points for all samples. These data were collected mainly from the same scale of the current meter and would have much less scatter if taken automatically where no judgment concerning the correct value for current was necessary. It requires four full digits to obtain ∿3% precision for ΔVG = 0.5 V.

A third feature of these plots is the nature of the curves at low VG. Recall that for any wafer both n^+ and p^+ contacts are formed in silicon which is doped precisely the same (i.e., the same epi layer). Applying simple-minded semiconductor theory, one would expect that there would be a constant difference between the threshold gate voltage of the n^+ and p^+ devices. This is clearly not the case, however, for if one defines the threshold (in mobility terms) as that gate voltage at which the mobility is 0.5 of its maximum, then for wafer 1 the difference in thresholds is ∿4.1 V. For wafer 2 it is ∿1.8 V. This very clearly shows that simple-minded ideal semiconductor thinking quickly leads to contradictions when dealing with heavily defected silicon. The shape of the μ_S vs VG plot as the curve proceeds from 0 to its maximum is a measure of the trapping properties of the surface. We have indicated that this slope may be represented as a turn-on parameter given by ΔFEM/ΔVG. If a region exists where μ_S is nearly constant, we will call that value characteristic for the FEM of that device. Although detailed data were not gathered at the low gate voltages (which is less demanding on the current meter since ΔI/ΔVG is larger in this gate voltage range), it is clear that wafer 1 requires considerably more surface charge to produce a respectable mobility than wafer 2. (This phenomenon was discussed in refs. 9 and 14). Induced charges are being trapped until the traps are filled. When the traps are filled, the induced charges are mobile and contribute to $\Delta\sigma_S$. However, when the traps are filled they provide charged scattering centers for those induced charges which are mobile, and the peak μ_S is less. Note that both n-channel and p-channel devices are similarly affected.

We have also noted the presence of a "dip" in μ_S has a significantly larger percentage range. This dip has been tentatively identified as an excited trap level. Note that all significant differences between the two wafers have vanished at VG = 10.0 V where the surface charge density is very high.

We have thus again established experimentally the earlier conjecture that application of detailed models to a system of this type is not wise.

Measurements of μ_S have been obtained automatically using ΔVG = 1.0 V and assuming (TOX) was not a variable (this was shown to be true from other structures). Typical results from this measurement are shown in figure 51. Data from the wafers used for the curves shown in figure 50 were acquired across the entire wafers. For the n^+ contact structures VG = 6 and 5 V were used while VG = -3.5 and 4.5 V were used for the p^+ contact structure. Note that good agreement is obtained between the automatic and manual measurement and that wafer 1 in addition to having a lower overall μ_S has a significantly larger percentage scatter. (Wafer 1 is plotted using limits of 0 to 500 instead of limits of 0 to 1000 used for wafer 2.)

Typical Hall data from a gated controlled bridge resistor is shown in figure 52. These data were acquired on a structure with n^+ contacts. V_H^+ is the potential across PV1 and PH1 with positive magnetic field and V_H^- is with negative magnetic field. Note that measurement becomes essentially impossible at gate voltages below 1 V. Again, the surface properties are the only ones readily available. The Hall mobility may be calculated at any gate voltage from the following formula:

$$\mu_H = \frac{\left((V_H^+ - V_H^-)/2\ (L/W)\ (10^5)\right)}{(V_{12})\quad (B \text{ in kilogauss})} \tag{16}$$

Notice that (TOX) is not needed for this calculation. For the particular data shown at VG = 2 V, μ_s = 530 $cm^2/V\text{-}s$. This again is only the mobility of the carriers that are free to move.

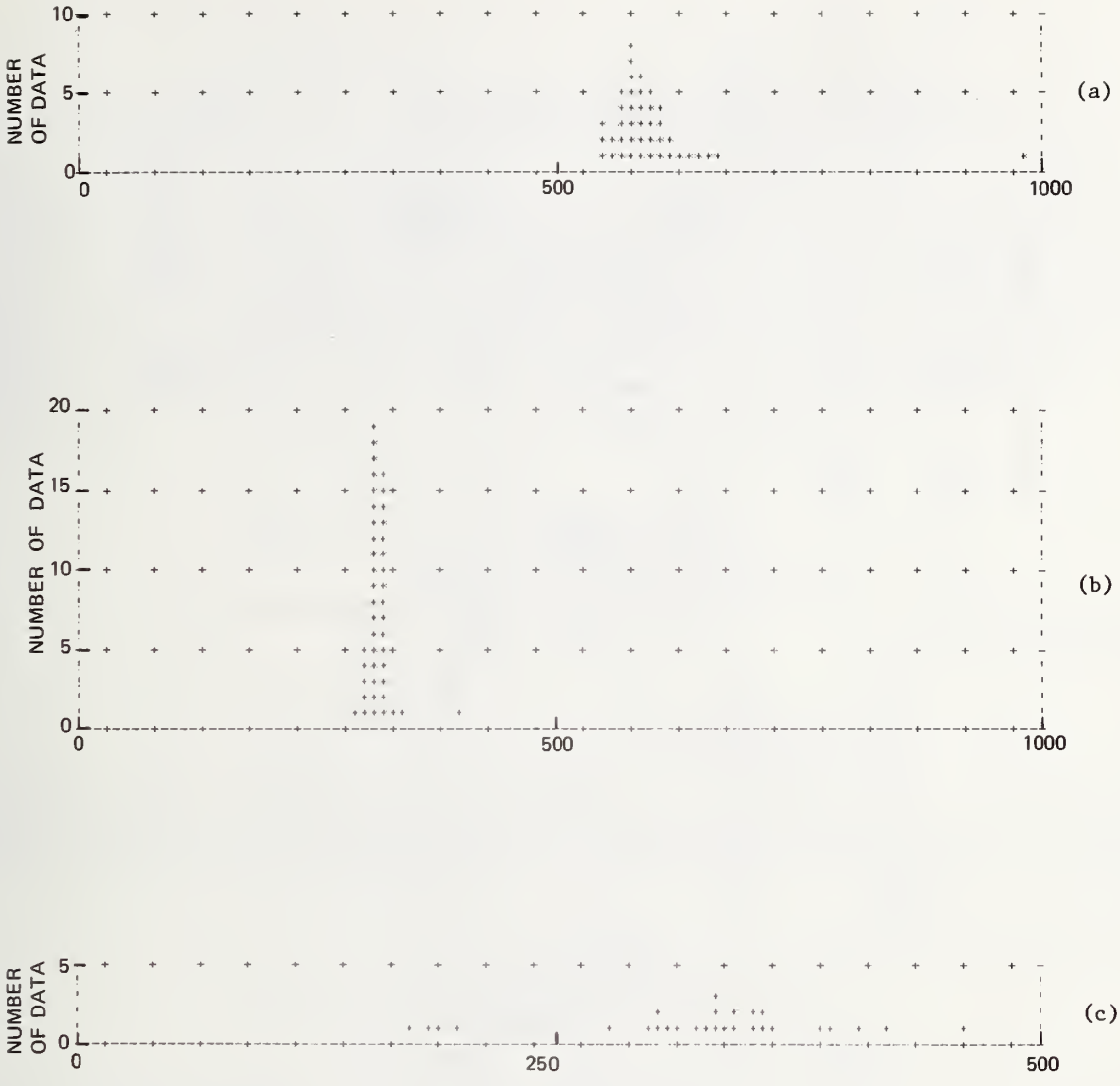


Figure 51. Field-effect mobilities.
(a) n-Channel wafer 2
(b) p-Channel wafer 2
(c) n-Channel wafer 1

Potential Pitfalls - Previously discussed.

Overall Usefulness - This structure is useful for a number of parameters. The main value lies in the ability to probe the epi surface properties independent of contact effects and to control the surface potential independently. One must know, *a priori*, what gate voltage to use. This is usually not a serious problem as long as attention is confined to the surface behavior. However, it is a very serious problem if one wants to profile the film since the critical relationship between VG and depth in the film is needed. This can be provided from MOS capacitor measurements (perhaps on the same structure) for some types of film but this requires special equipment and very careful interpretation [9]. For automatic measurement it is best to confine the attention to surface properties. There are no particular improvements noted for this description.

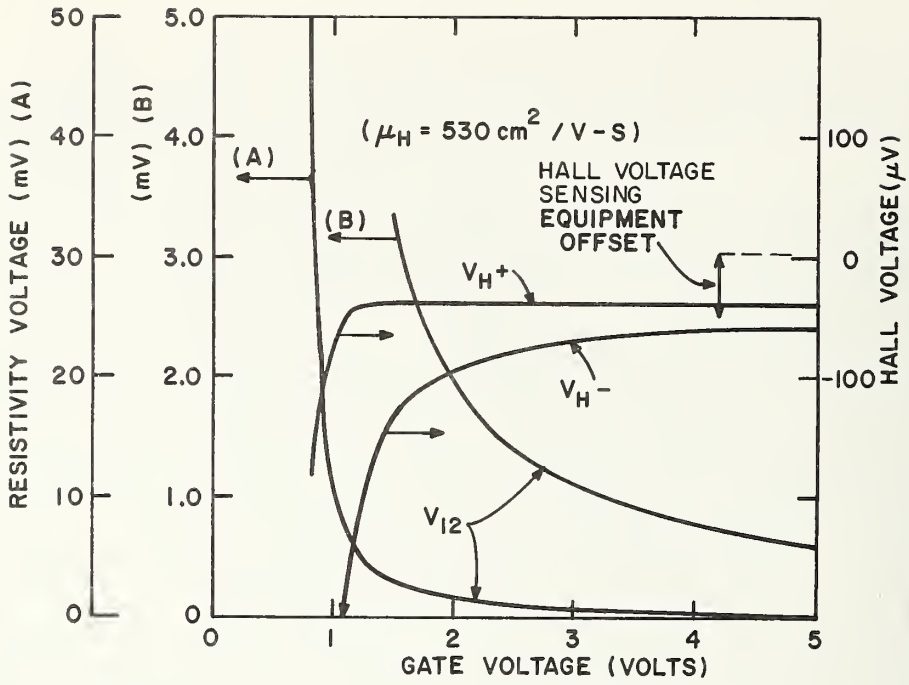


Figure 52. Typical Hall and resistivity data from I-5 (n^+ contacts). The film thickness is 0.6 μm.

Related Structures - This structure is closely related to the long-channel MOS structures III-1 and III-2 and to the ungated bridge resistors I-54, I-55, I-57, I-59, I-61, and I-63. The closest relatives, however, are the gate-controlled van der Pauw structures I-48 and I-49.

3.3 Crossovers - I-7, I-8, I-9, I-10, I-11, I-12, I-13, I-14

Purpose - The purpose of the crossovers is to measure continuity, resistance, capacitance, and dielectric strength of two levels of conductors separated by a dielectric.

Verbal Description - The crossover test structure consists of two conductive materials crossing each other with a dielectric separation. These materials are n^+ epi, p^+ epi, (n^+ epi), (p^+ epi), p^- poly, p^+ poly, and Al. All silicon is 0.3 mil wide at the intersection, and all Al is 0.4 mil wide at the intersection. The upper material is contacted directly by probes at pads. The lower material is contacted through 0.2 x 0.6 mil contact holes by metal which is ultimately contacted at pads. All structures have four independent electrical access points. The p^- poly over (p^+ epi) (structure I-12) is a poor structure because the n^+ mask must align exactly with the poly to avoid forming (n^+ epi). This combination would not normally be used. Similar comments apply to structure I-13 (p^+ poly over n^+ epi).

Line Drawing - The line drawing for this structure is shown in figure 53.

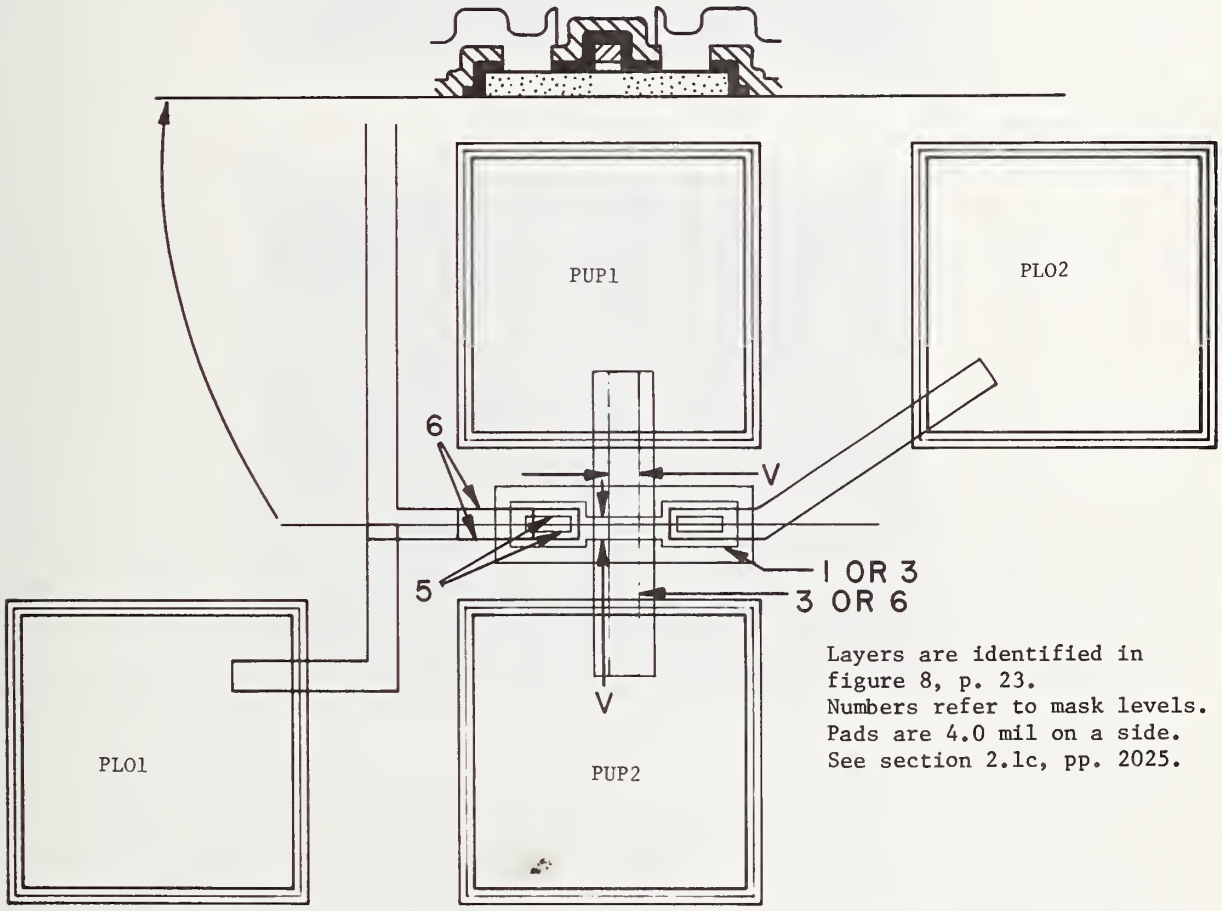
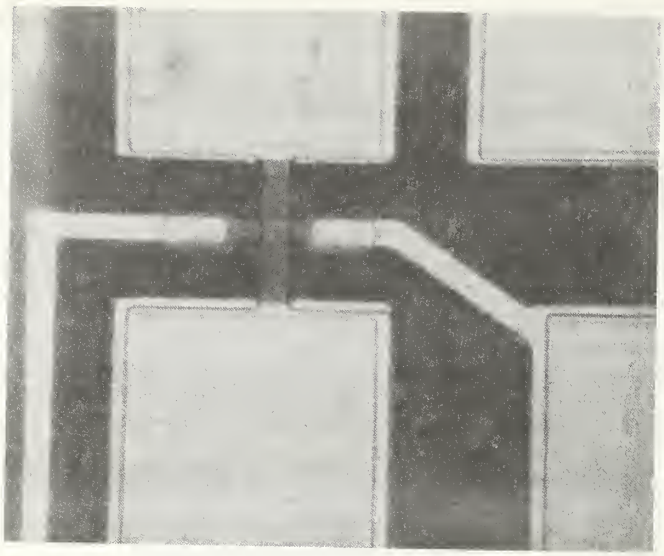
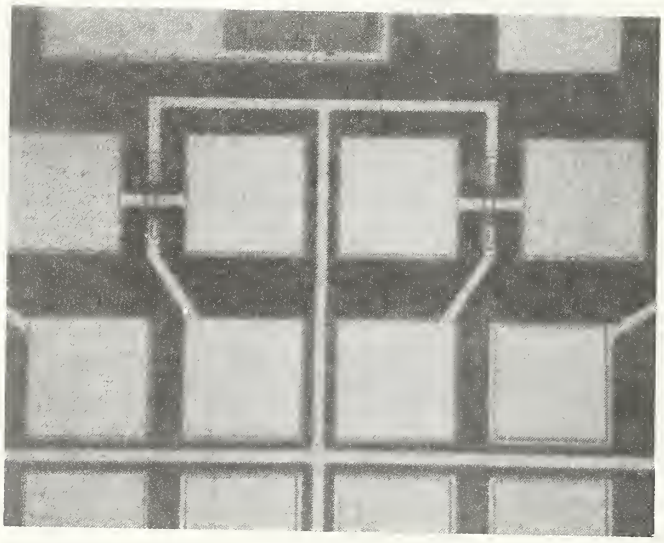


Figure 53. Crossover, test structures I-7 through I-14, line drawing and cross section.

Halftone Photograph - The photomicrograph for this structure is shown in figure 54.

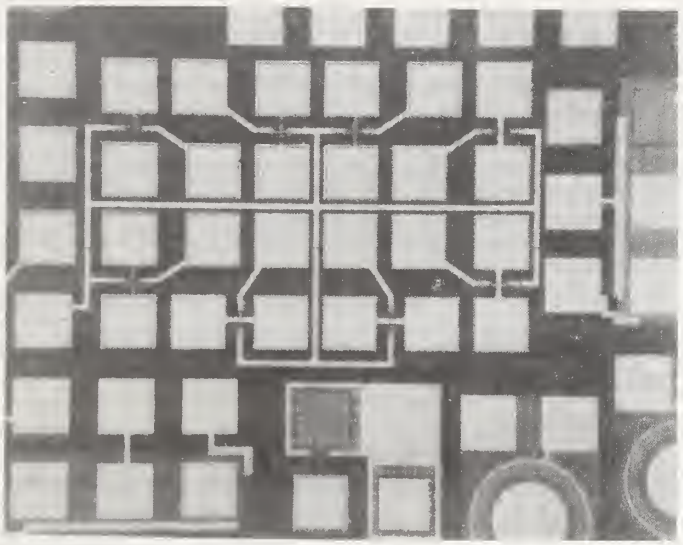


(a)



(b)

Figure 54.1. Photomicrographs;
(a) single crossover,
(b) two crossovers, and



(c)

Figure 54.2. (c) entire family of crossovers.

Electrical Access Points - This structure has four electrical access points designated as:

PLO1, PLO2 } lower conductor

PUP1, PUP2 } upper conductor

If the conductor is poly, a poly pad is used.

Testing Method - This structure exists as a combination of three separate structures and, in general, would be tested for one or all of these separate structures. The result of these tests may, however, be different than either conductor alone since interaction between the conductors may exist. The first two structures are essentially two-terminal resistors consisting of the upper conductor alone and the lower conductor alone. As long as the third structure, the MOS capacitor between the upper and lower conductor, is not conducting, then either resistor may be tested separately. Therefore, the first test needed is for the leakage between the upper and lower conductor. This would typically be performed by connecting PUP1 and PUP2 together and PLO1 and PLO2 together to form a two-terminal MOS structure. The generalized testing of two-terminal MOS structure is discussed in detail in the next subsection (3.4). For purposes of this description it is sufficient to ensure that no appreciable current exists between the resistors at a specified voltage. (This is the TTMDS3 version in the next section.) Once this is established, we may test the upper and lower conductors as two independent resistors. The MOS capacitor structure will be treated in the next section. We shall now describe the generalized two-terminal I-V measurements needed to characterize these conductors.

These measurements apply also to other devices commonly called "resistors," sheet resistors, or contact resistors. Their nominal characteristics are linear and bilateral. It may be readily appreciated that when these are true, the structure is completely characterized by a single measurement. In actual practice it is frequently found that severe departures from linearity and bilaterality exist and that these can cause first-order misinterpretation of the measurements. We therefore provide the possibility of quantifying the measurements in terms other than simply V/I.

The most common cause of nonlinearity or nonbilaterality is a nonideal contact to the semiconductor. This is frequently caused by slight amounts of residual oxides left in the opening for the metallization for a variety of possible reasons. This type of contact can sometimes be made to behave more ideally by applying a relatively large voltage. Experience has shown that often seemingly nonconducting samples can be made to conduct strongly under these conditions. However, it is also possible to avoid detecting a condition where application of the test voltage actually changes the characteristics of the contacts during the test. To ensure that the contacts are not "formed" during testing, a low voltage test is first done so that reasonable currents are flowing initially. If the current is too low, then an entirely different testing approach is taken.

The measurements described here are steady-state dc although an ac signal can be used advantageously to measure a local slope and for specific testing as described later. Transient measurements are so fast due to the very short dielectric relaxation times that they are not practical for most testers.

Of course, complete specification of nonlinearity and bilaterality is possible only by measuring the entire I-V curve. This approach may be necessary in a few cases. Nearly all the important information for a particular application can usually be determined by examining the curve in a region around a characteristic application voltage, and this is the main approach taken here.

Testing proceeds by first applying a low voltage and measuring the resulting current. If this current is not high enough (as determined from previous knowledge), testing is either halted or proceeds as if the contacts are poor but may possibly be "formed" into a suitable contact. If it is chosen to continue to test, voltage is applied in successively increasing steps until the current exceeds the value chosen for the limit. This value is also determined from previous knowledge. The maximum possible applied voltage is also chosen to avoid excessive testing time.

If the initial current is suitable, testing proceeds by applying voltages and measuring the currents noted in figures 55 and 56. The characteristic application voltage is designated as (VI) and all other applied voltages are multiples of (VI). Nonlinearity and/or nonbilaterality of the structure are measured as indicated in figure 56. In addition, the local resistance around (VI) is measured by applying a voltage a small amount above (VI); (VIP), and a voltage a small amount below (VI); (VIM). These amounts are somewhat arbitrary but have given the values (VIP) = 1.25 * (VI), VIM = 0.75 * (VI) for the specific program here. The linearity measurements are made by three methods. One must first make a decision concerning the ability to apply stimuli greater than (VI). Is this range of operation of interest? Will the higher excitation give misleading measurements due to heating, etc? It is assumed that the structure can stand at least twice the excitation provided at (VI) without introducing errors for the flow chart program. If this is not possible, then one may use another convenient point such as 0.5 * (VI) as the second excitation level. Clearly, a necessary condition for linearity is that the curve pass through zero. This is tested by calculating the intersection of the line through (VI), (II), and (2VI), (I2I) with I = 0. This point should be close to V = 0 and the amount of deviation from zero is a measure of the nonlinearity. Another measure of the linearity is the ratio between the small-signal resistance around (VI) and the dc resistance at (VI) while a third is the current ratio (I2I)/2*(II).

Similarly, a bilaterality parameter is calculated which is the ratio between the difference in current at (VI) and -(VI) to twice the initial current.

This program could be used for either or both conductors in the crossover structure but is particularly suited to the conductor with contact holes. The total test program for this structure would then consist of an initial test to determine that the upper and lower conductors are isolated followed by two programs which characterize the conductor as two-terminal resistors. Finally, the properties of the MOS structure are measured. This test is last because it is necessary to ensure that the conductors are suitable as contacts for the MOS structure and more importantly because the MOS tests are frequently destructive. The MOS measurements are discussed in the next section.

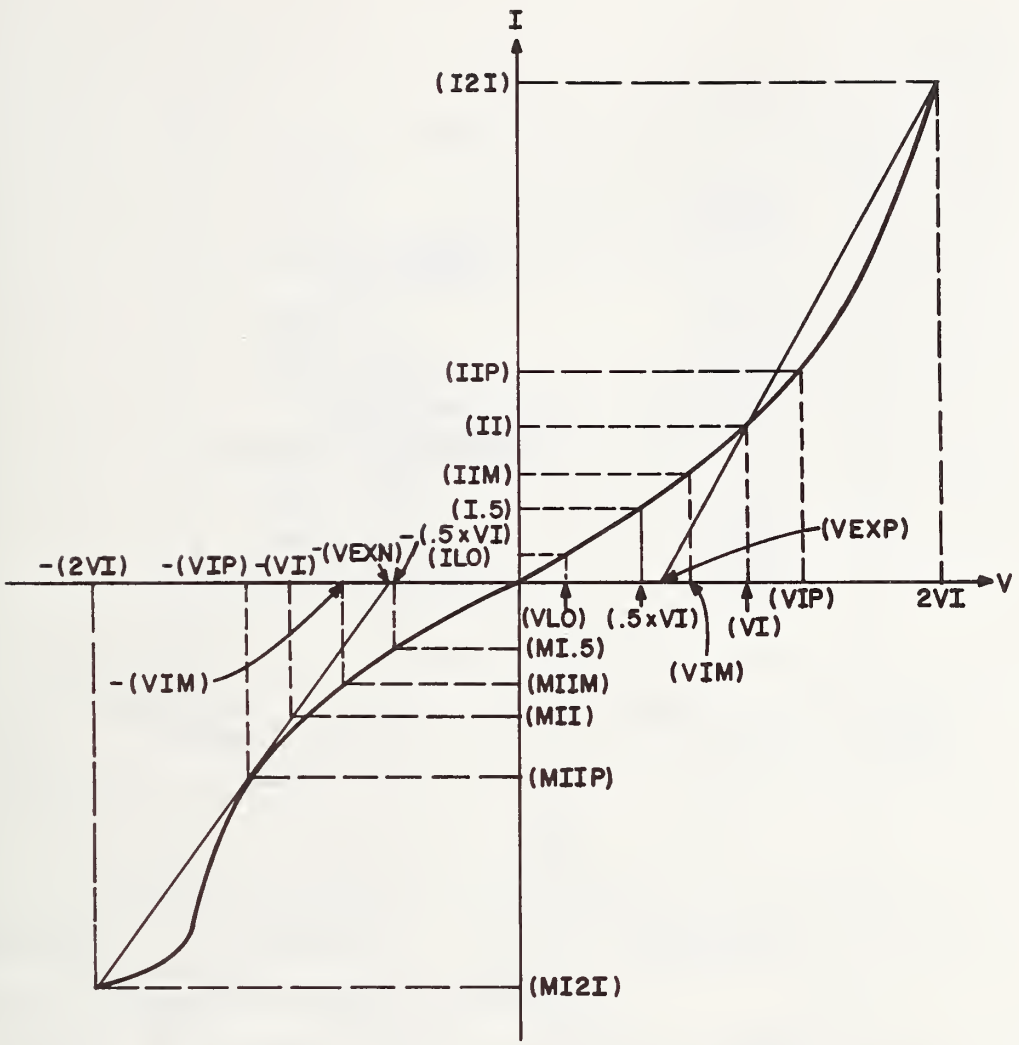


Figure 55. Generalized two-terminal I-V characteristics.

The above tests are all dc and as such have the ability to detect dc current only. This limitation can affect the diagnostic power of the electrical measurements. Particularly for structures which consist of multiple connections such as this one, it is impossible to determine where the open-circuit is occurring from dc measurements. In addition to the conductor not being continuous over a step, the following can also be responsible for an open-circuit indication.

- Broken metal (scratched or not properly defined)
- Nonopen contact hole
- Broken conductor (scratched or not properly defined)

Considerable information concerning the nature of the dc open-circuit can be obtained by examining the ac coupling available between the pads. Scratched connections would have very low coupling; closed contacts would have another type; while discontinuous step crossings would have yet another type. The ac response provides a complementary stimulus which can be used to considerable advantage for this type of test structure. For very complex crossover tests, as on the type IV quadrant, for example, the ac tests are even more valuable. Unfortunately, these excitations are frequently missing from automatic testers.

Initial Parameters

- Initial low voltage (VLO)
- Minimum acceptable current at (VLO) (ILOMN)
- Characteristic voltage for test (VI)
- Determine contact breakdown voltage? (CONVB)

  Positive number = yes

  Negative number = no
- Voltage increment for contact breakdown tests (VINC)
- Maximum number of cycles for contact breakdown test (MXCYCL)
- Current level for contact breakdown (ILIM)

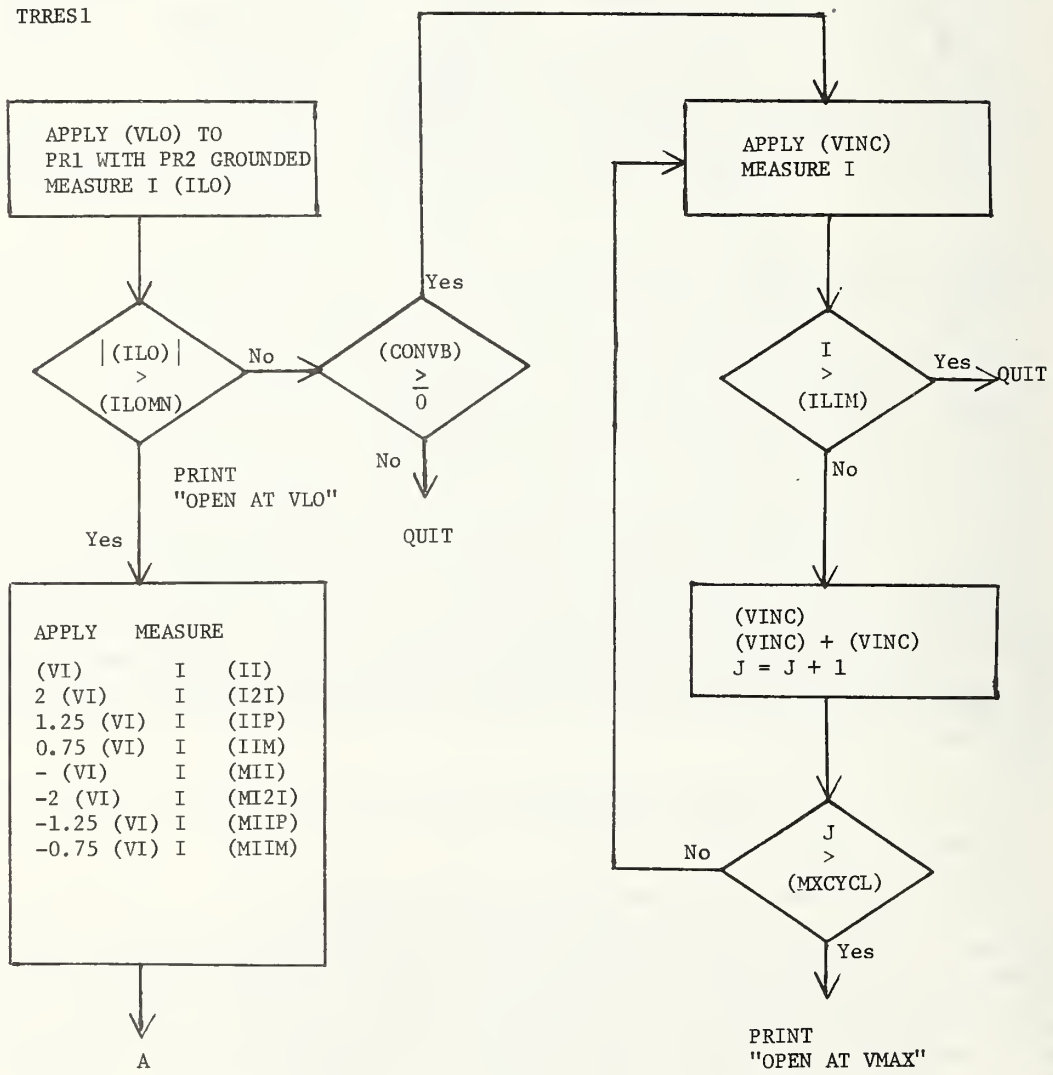


Figure 56.1. Flow chart for TTRES1.

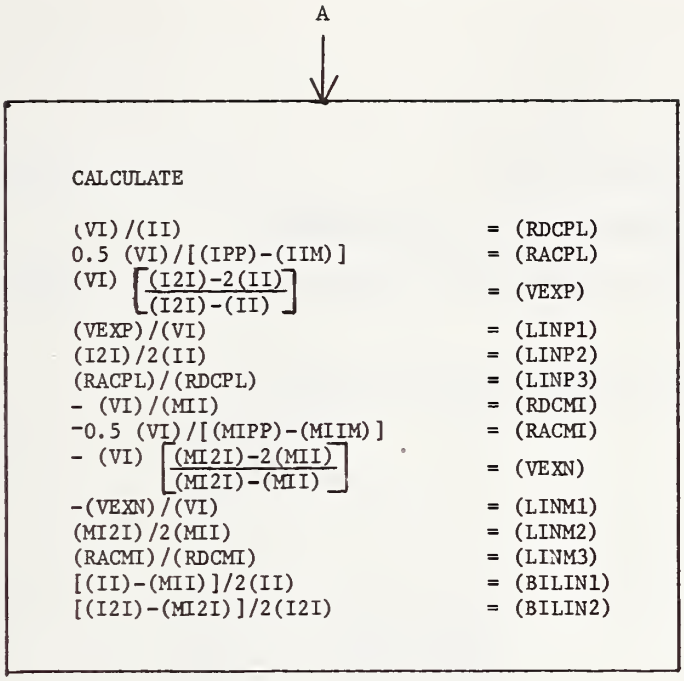
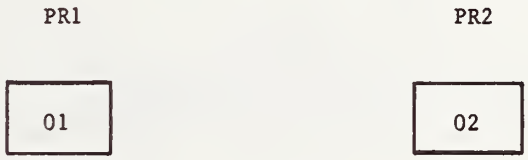


Figure 56.2. (Continued)

Test Pads:



Flow Chart - The flow chart is shown in figure 56.

List of Outputs - The outputs for this test are listed in the first block of the flow chart.

Less General Versions - Since this test block is of very considerable importance to many of the structures, other versions will be described with flow charts for this section only.

Test Blocks for Two-Terminal Resistors

Complete	[TTRES1]
Standard	[TTRES2]
Simplest	[TTRES3]

Complete:
- initial low voltage measurement
- dc resistance
- small-signal resistance
- large-signal resistance
- 3 types of linearity
- 2 types of bilaterality
- determination of contact
- breakdown voltage

Standard:
- initial low voltage measurement
- dc resistance
- bilaterality
- linearity

Simplest:
- dc resistance

(1) TTRES2

Initial Parameters:

- Initial low voltage (VLO)
- Minimum acceptable current at (VLO) (ILOMN)
- Characteristic voltage for test (VI)

Flow Chart

The flow chart for TTRES2 is shown in figure 57.

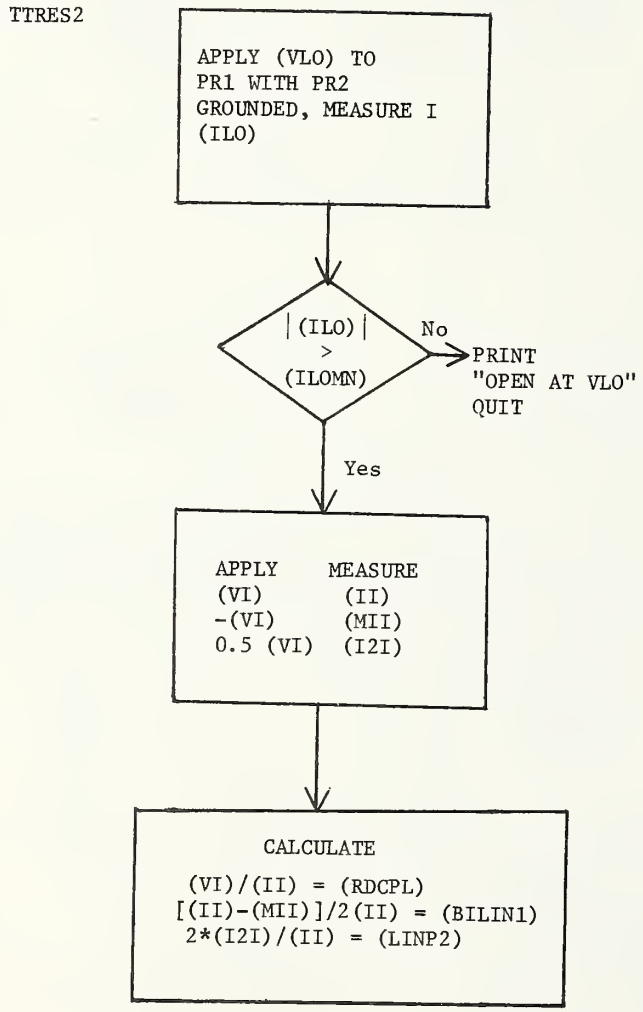


Figure 57. Flow chart for TTRES2.

(2) TTRES3

Initial Parameters:

- Characteristic voltage for test (VI)

Flow Chart

The flow chart for TTRES3 is shown in figure 58.

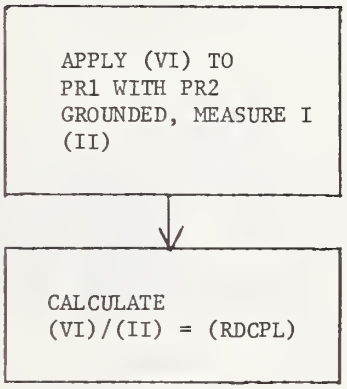


Figure 58. Flow chart for TTRES3.

Special Equipment - No special equipment is necessary for this test.

Samples of Data - No data have actually been obtained from this structure; however, two-terminal resistance data have been acquired on other structures which are very similar. The set of data in figure 59 illustrates the application of TTRES1 to an n^+ epi two-terminal resistor.

The tests are identified from the following list:

```
 3    ILO      I56N+EPI TTRES1
 5    RDCPL    I56N+EPI TTRES1
 7    LINP1    I56N+EPI TTRES1
11    LINP2    I56N+EPI TTRES1
13    RACPL    I56N+EPI TTRES1
16    LINP3    I56N+EPI TTRES1
17    RDCMI    I56N+EPI TTRES1
19    LINM1    I56N+EPI TTRES1
23    LINM2    I56N+EPI TTRES1
25    RACMI    I56N+EPI TTRES1
28    LINM3    I56N+EPI TTRES1
29    BILIN1   I56N+EPI TTRES1
30    BILIN2   I56N+EPI TTRES1
```

Note that the histograms are generated using the data to set the limits and that direct comparison is not possible without examining the scales. For this particular structure, a great deal of "overkill" was used since all of the linearity and bilaterality parameters are very close to 1.00 or 0.00. The application voltage (VI) was 1.0 V, and the extrapolated voltage, as revealed by LINP1 and LINM1, was less than 20 mV for both polarities. The positive side had much lower values ($\sim$4 mV) which were approximately centered around zero while the negative side was nearly all positive. In any case, 20 mV out of a 2.0-V stimulus would be acceptable for most applications.

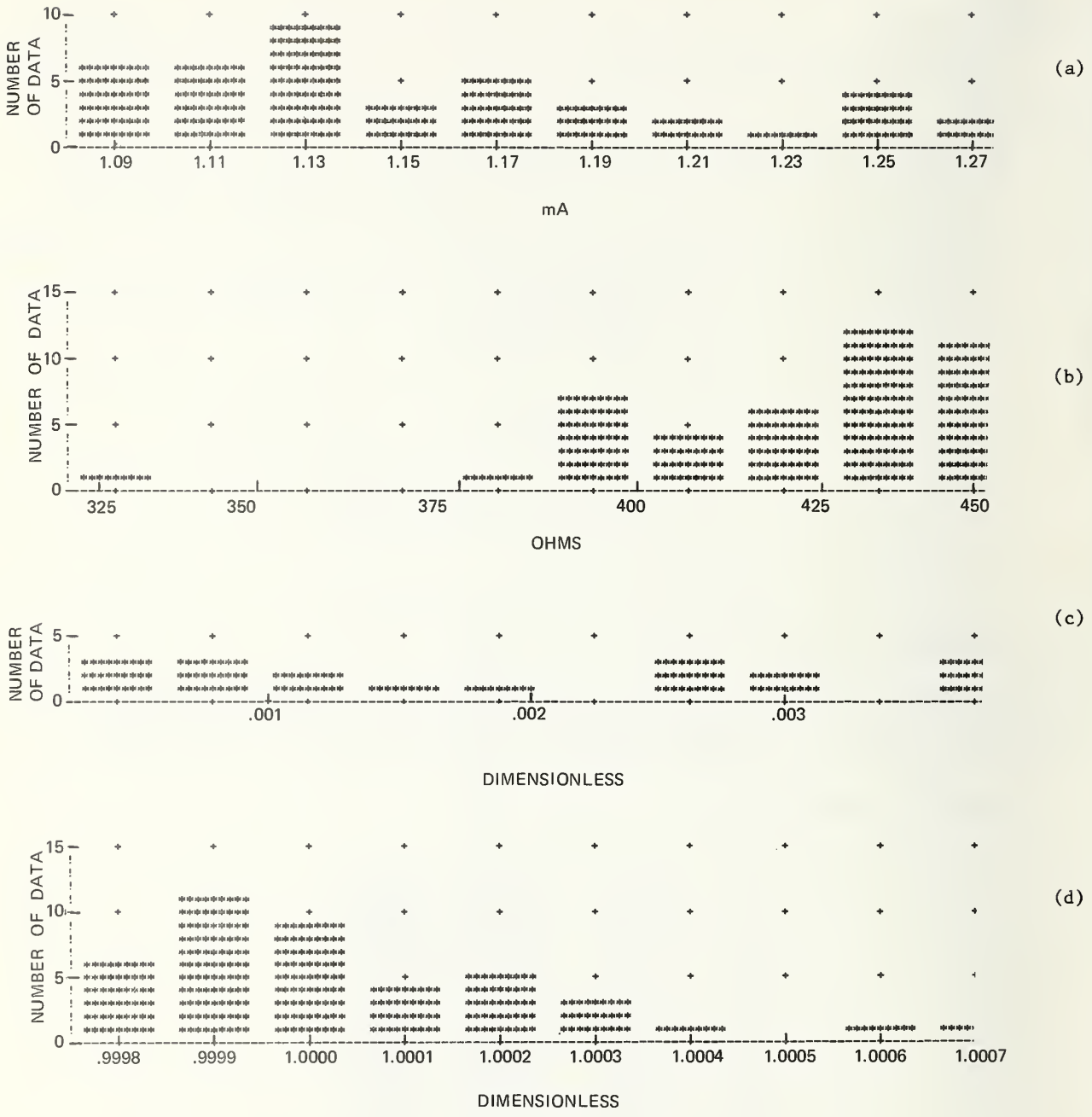


Figure 59.1. (a) ILO in mA, (b) RDCPL in ohm, (c) LINP1, (d) LINP2

Potential Pitfalls - As with any two-terminal device it may not be possible with this structure alone to separate continuity of the conductor over the step problems, from contact to the conductor problems. Examinations of other structures in conjunction with this structure can help to separate contact problems.

Overall Usefulness - Since this structure has not been tested here it is difficult to comment on its usefulness. The primary purpose of this structure is for diagnosing problems which

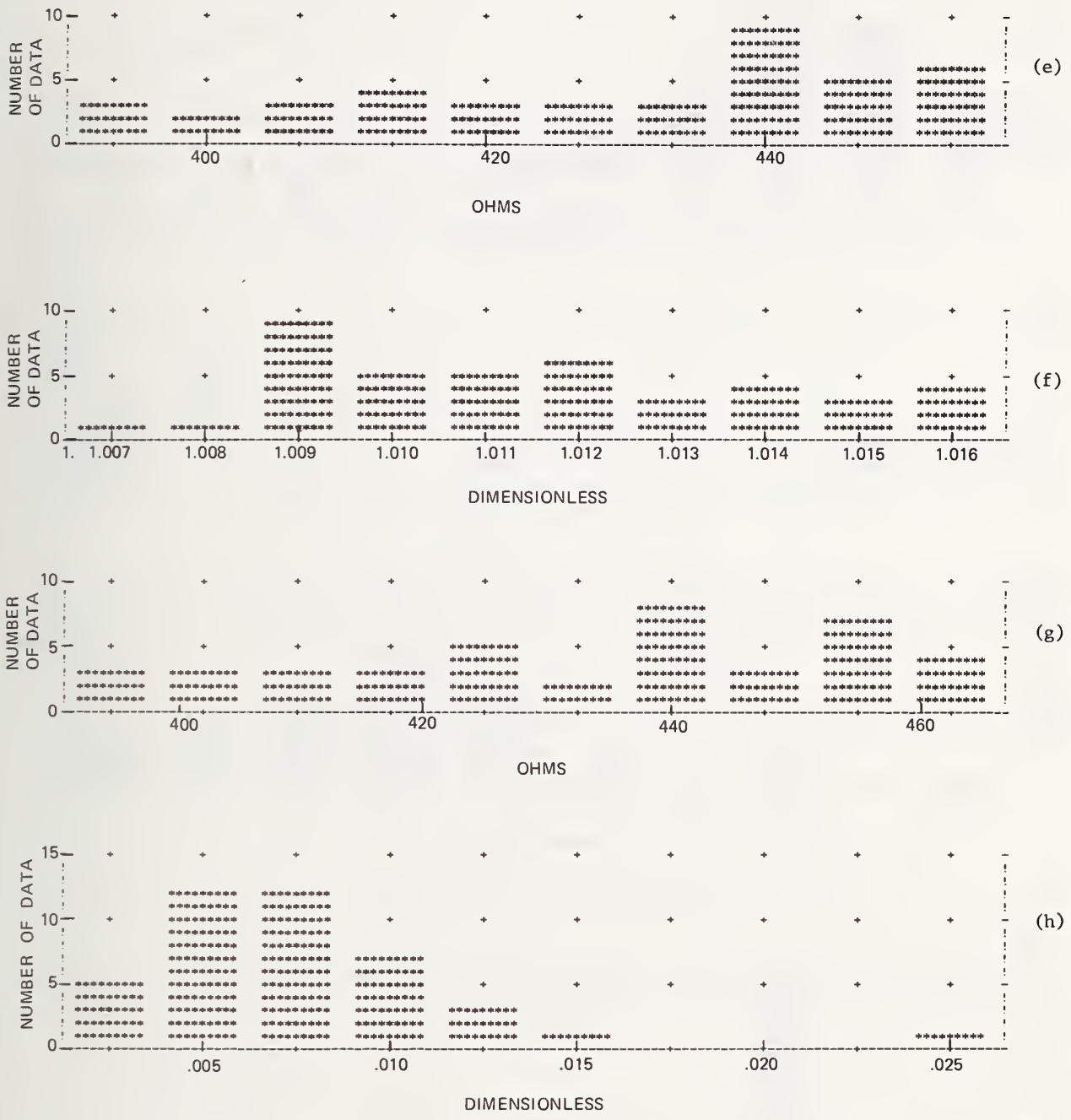


Figure 59.2. (Continued) (e) RACPL in ohm, (f) LINP3, (g) RDCMI, (h) LINM1.

develop in other structures, particularly with regard to continuity of conductors. For the intended purpose of this structure no apparent improvements are suggested. One could supply a voltage tap behind the contact to help diagnose contact problems.

Related Structures - This structure is related to nearly every structure where a conductor crosses an edge. It is useful in conjunction with I-56, I-58, I-60, I-62, I-78, and IV-1-9.

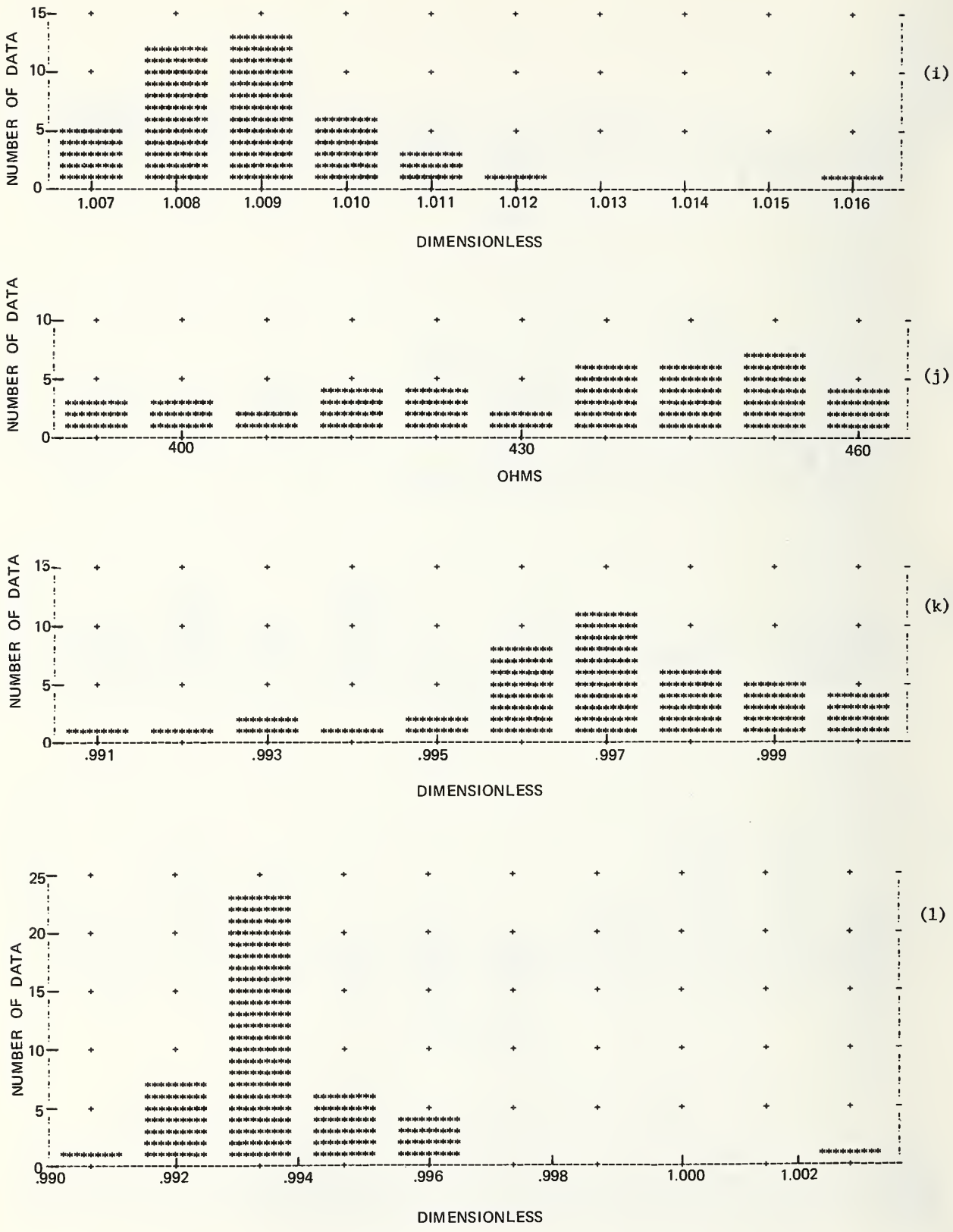


Figure 59.3. (Continued) (i) LINM2, (j) RACMI in ohm, (k)LINM3, and (l) BILIN1.

3.4 Poly-Gate MOS Capacitors; Single Diffusion on Epi - I-15, I-20, I-21, I-22, I-23, I-24, I-29, I-30, I-31, I-32

3.5 Al-Gate MOS Capacitors; Single Diffusion on Epi* - I-16, I-17, I-18, I-19, I-25, I-26, I-27, I-28

Purpose - The purpose of test structure I-15 is to measure parameters derivable from MOS capacitor measurements such as dielectric thickness, interface change, dielectric strength, and doping density. Structures I-20, I-21, I-22, I-23, I-24, I-29, I-30, I-31, and I-32 are geometrical variations with the same purpose as I-15.

The purpose of test structure I-16 is to measure dielectric strength and thickness of deposited doped oxide and possibly indicate doping level of diffusion. Structures I-17, I-18, I-19, I-25, I-26, I-27, and I-28 are geometrical variations with the same purpose as I-16.

Verbal Description - These structures are all contained on a single epi island which is contacted by a common diffusion. The entire island is covered either by an n^+ or a p^+ doped oxide.

The poly capacitors differ from each other in the part of the epi island which they cover. Structures I-20 and I-29 are confined entirely to the top of the epi as are the smaller structures I-21 and I-30. In order to avoid placing a probe directly on the top of the active area structures I-15 and I-24 cross the island edge to a separate poly pad. Structures I-22 and I-31 have a large intersection with the epi island edge while structures I-23 and I-32 cover the top, edge, and corner of the epi.

The aluminum capacitors have similar structural variations. I-18 and I-27 are confined entirely to the top of the diffused epi, I-19 and I-28 cross the island edge with a minimal strip of Al to an external pad, I-26 and I-25 make large contact with the edge, and I-17 and I-26 cover the corner of the epi island. All of the aluminum structures have the pad aluminum resting on bare sapphire to avoid any possible step problems at the pad edge.

The basic size of the large capacitors is 4.0 mil on a side. For those which cross the edge, a compensating reduction is made so that that active area is nominally constant. The small capacitors I-21 and I-30 are 2.0 mil on a side.

Line Drawing - The line drawing for this structure is shown in figure 60.

Halftone Photograph - The photomicrograph for this structure is shown in figure 61.

Electrical Access Points - All pads on this description are gate connections except for PSUB indicated in the figure 60. PSUB is common to all structures.

Testing Method - All of the structures in this description fall into the general classification of two-terminal MOS structures. Those structures are nominally nonconductors in a steady-state dc sense and are capacitively conductive in an ac sense. The measurements fall into one or more of the following classifications:

- Steady-state ac
- Transient ac
- Steady-state dc
- Transient dc

We will limit the measurements to the steady-state conditions. We define the measurements under steady-state ac conditions as *capacitance* or *conductance*, and the measurements

*Earlier we indicated our intention to bracket the discussion of some structures. For the reader's convenience and for the sake of continuity, we will maintain a numerical sequence, and, therefore, may have multiple section numbers in "bracketed" discussions.

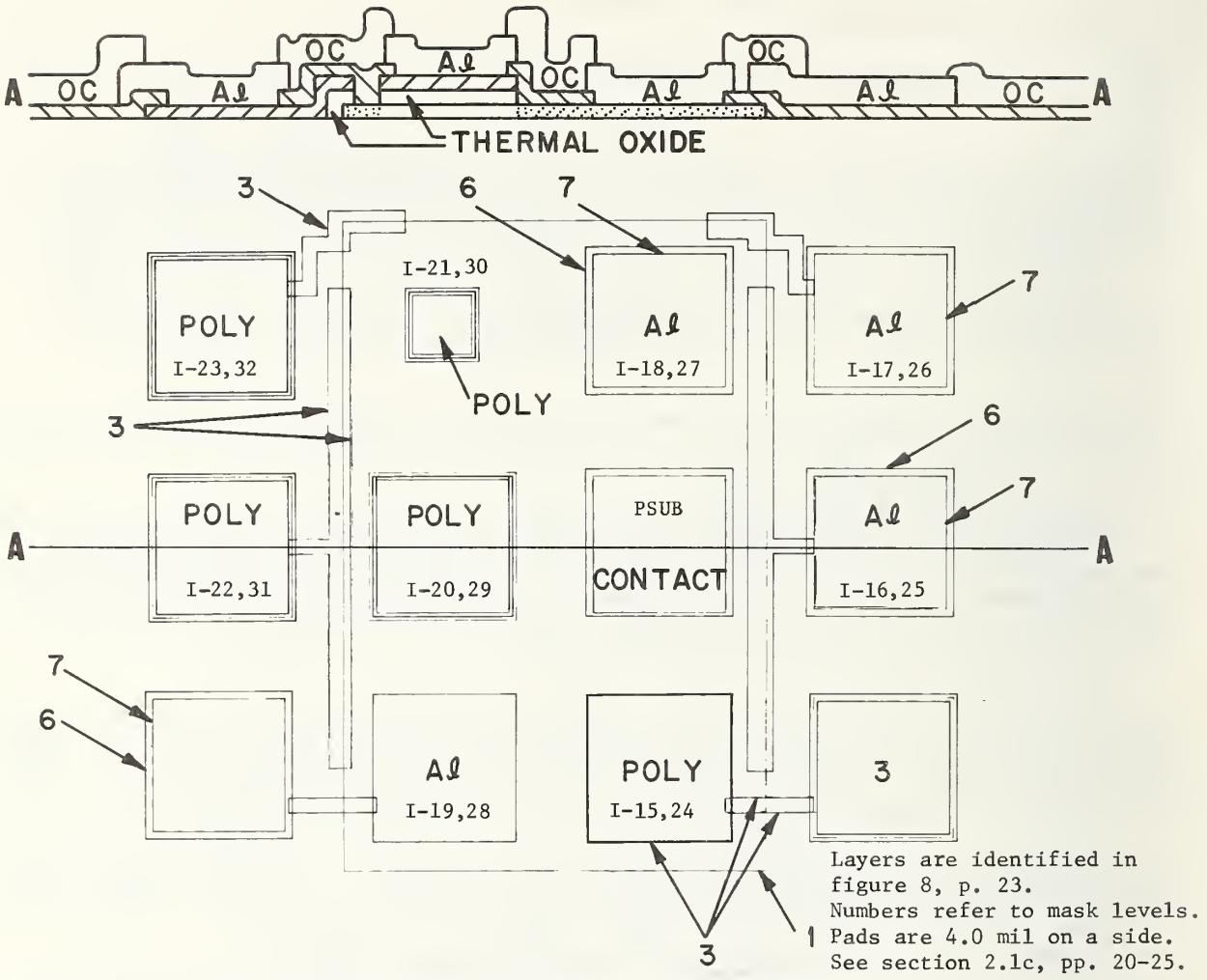


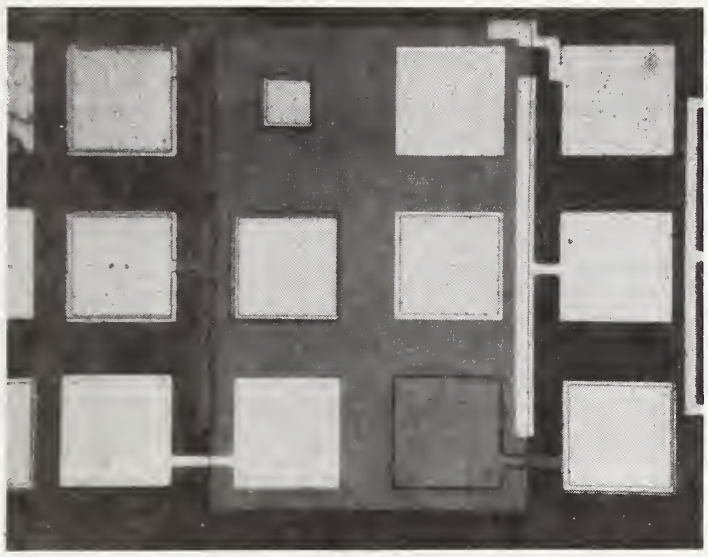
Figure 60. Poly gate and Al gate MOS capacitors, single diffusion on epi, test structures I-15 through I-32, line drawing and cross section.

under steady-state dc conditions as *dielectric strength*. It is well recognized that capacitance measurements can be made using transient dc methods (the so-called quasi-static approach). These methods require much larger structures than we are dealing with here in order to produce current high enough to measure accurately. We therefore choose to disregard these measurements for our applications.

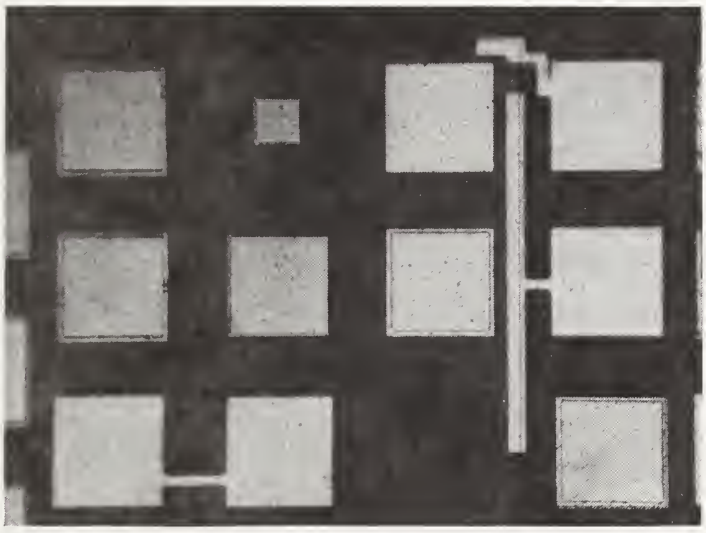
With the appropriate hardware, both capacitance and dielectric strength measurements are possible on the same structure at the same probing time. A complete room-temperature characterization must include both. The more usual case, however, is that only one of the two can be measured on the same structure at the same time, and this is the approach taken here. Many of the two-terminal MOS structures are designed with the thought of using almost exclusively only one of the measurement classifications. Consider first the dielectric strength.

One of the most important features of dielectric strength measurements is that the measurement process may change the characteristics of the test structure. The measurements are not always nondestructive, particularly at high fields. The changes may occur so rapidly that it is not possible to detect the precise conditions which caused the change. One must therefore proceed very cautiously and ensure that all relevant data are collected *before* a situation is created which irreversibly changes the sample.

We are dealing here with the concept of measuring the current which flows throughout the entire sample. Inferences can be made concerning the uniformity of the current flow by



(a)



(b)

Figure 61. Photomicrographs, MOS capacitor (a) n^+ epi and (b) p^+ epi.

examining data from structures which are nominally identical except for their geometry. This is the only way to gain any insight into the uniformity of current flow from two-terminal electrical measurements. The process, therefore, becomes one of measuring the I-V characteristics nondestructively and accurately.

The capacitance and conductance can also be measured on any of these structures. A detailed discussion of C-V measurements on SOS films is given in ref. 14. It is shown that although these measurements can be made, they are somewhat difficult to automate and also somewhat difficult to interpret. Some examples of C-V measurements are shown in figure 134.

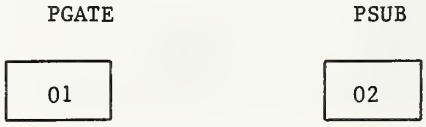
The basic method of testing the dielectric strength properties is simply to apply a voltage and measure the resulting current. This voltage is applied in successive steps until the current exceeds a predetermined limit. This limit will usually be picked so that the current is much above the low field leakage. For example, a typical current limit might be 10^{-6} A whereas the low field leakage might be $<10^{-12}$ A. By picking a limit so that the current is well above the background, the actual size of the structure becomes of second-order importance to the voltage required to produce the limit current. It is

usually found that conduction becomes noticeable just prior to actual destructive breakdown. Since the details of this region may be of interest in some cases, it is wise to incorporate a means to save the data as the voltage is being increased because there will be no availability of data after destructive breakdown. In the most general case the voltage will be increased in steps alternating polarity (i.e., first +10 V and then -10 V) to handle any possible polarity dependence. It is also possible that the lowest potential of interest may be very close to destructive breakdown and that the iteration may be in very small steps. Usually, the lowest potential of interest is near zero, and the voltage is stepped in steps of a least a few volts. The very low potential allows one to separate the initial "shorts" from those requiring a significant potential to fail. It is possible, since charge injection and trapping is frequently the basic mechanism of breakdown, that the time of application of the voltage may be significant. It is well known that the dielectric strength measured with the slow rise time pulses normally found in analog testers may not be the same as those actually experienced during electrostatic discharge. These measurements nevertheless provide a basis for comparison of structural variations and are quite valuable.

Initial Parameters

- Initial polarity (BEGPOL)
- Initial voltage (BEGVOL)
- Step size (STPSZ)
- Maximum number of steps (MAXSTP)
- Stress time/step (STPTM)
- Current fail limit positive (ILPOS)
- Current fail limit negative (ILNEG)
- I-V curve desired (IVCV)

Test Pads



Flow Chart - The flow chart is shown in figure 62.

List of Outputs - The output from the program is the final value of voltage. This is the voltage at which failure occurred or the value assigned if failure did not occur.

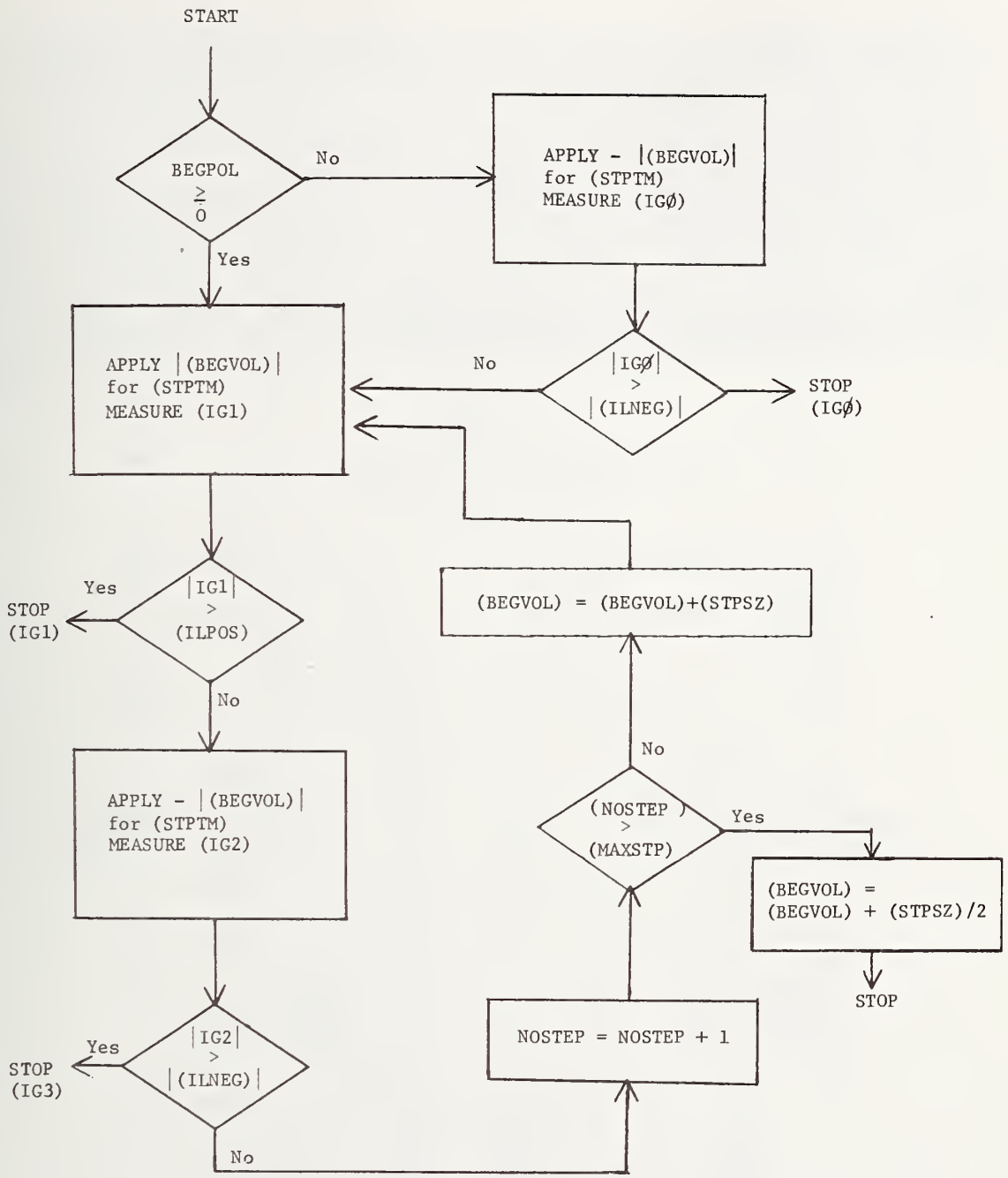
Less General Versions

- Complete (TTMDS1)
- One polarity only (TTMDS2)
- Current at a specific voltage (TTMDS3)

Two-Terminal MOS Dielectric Strength - One Polarity Only

Initial Parameters

- Polarity (POL)
- Initial voltage (BEGVOL)



Notes: (1) If IVCV is positive, each voltage-current pair is stored for future plotting.

(2) Each measurement may be repeated N times to increase stress time/step.

(3) The value of voltage used to cause the failure is defined as the fail voltage.

(4) If failure is not detected after (MAXSTP), the voltage is assigned the value (BEGVOL) + (STPSZ)/2 so that any data having half multiples of STPSZ will be due to failure not being detected.

Figure 62. Two-terminal MOS dielectric strength - complete (TTMDS1).

- Step size (STPSZ)
- Maximum number of steps (MAXSTP)
- Stress time/step (STPTM)
- Current fail limit (ILIM)
- I-V curve desired (IVCV)

Flow Chart

The flow chart for TTMDS2 is shown in figure 63.

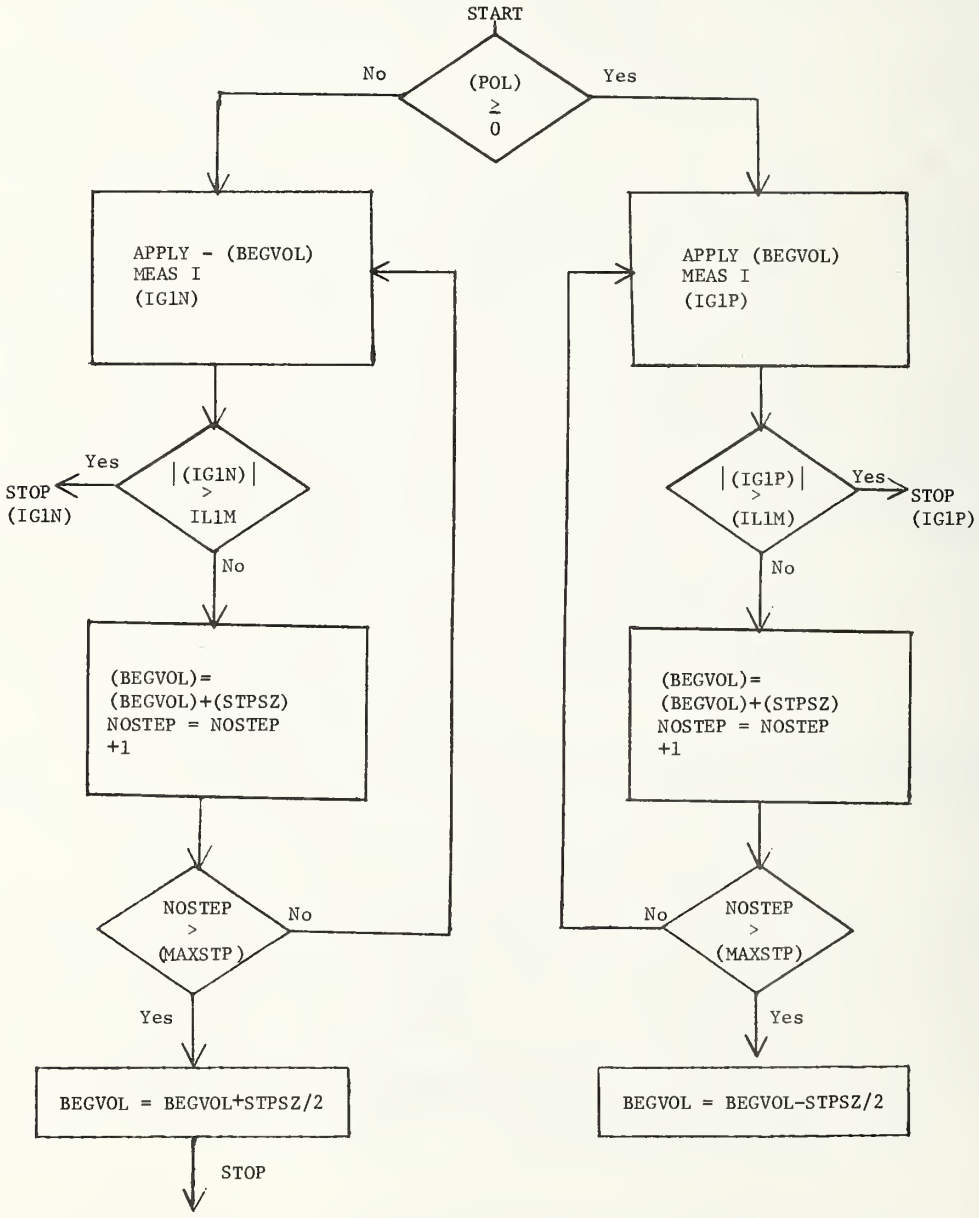


Figure 63. Two-terminal MOS dielectric strength - one polarity (TTMDS1).

Special Equipment - No special equipment is required unless very low current limits or a very high voltage for the desired tests are needed. Typically if the field oxide or other thick dielectric does not fail at 100 V, it will likely not be of particular interest in any case.

Samples of Data - These structures were tested using TTMDS1 with the starting voltage at 0.1 V, the step size at 5.0 V and (MAXSTP) at 19. The results for all of the aluminum-gate structures are shown in figure 64. All of these histograms are plotted on the same voltage scale of -100 to +100 V. We note that nearly all of the devices did not fail after 95.1 V (the maximum) and those that did fail, failed at 0.1 V. All of the structures have at least one failure, but structure I-25 had 7 out of 47 failures. This structure is the "edge mostly" structure. This clearly indicates a weakness in this process at the island edge. This is not a fundamental weakness, however, because both I-26 and I-28 have aluminum covering an edge. One must conclude that a point defect phenomenon which is concentrated at the edge is responsible and that this defect is, in effect, a pinhole since the structure failed at low voltage.

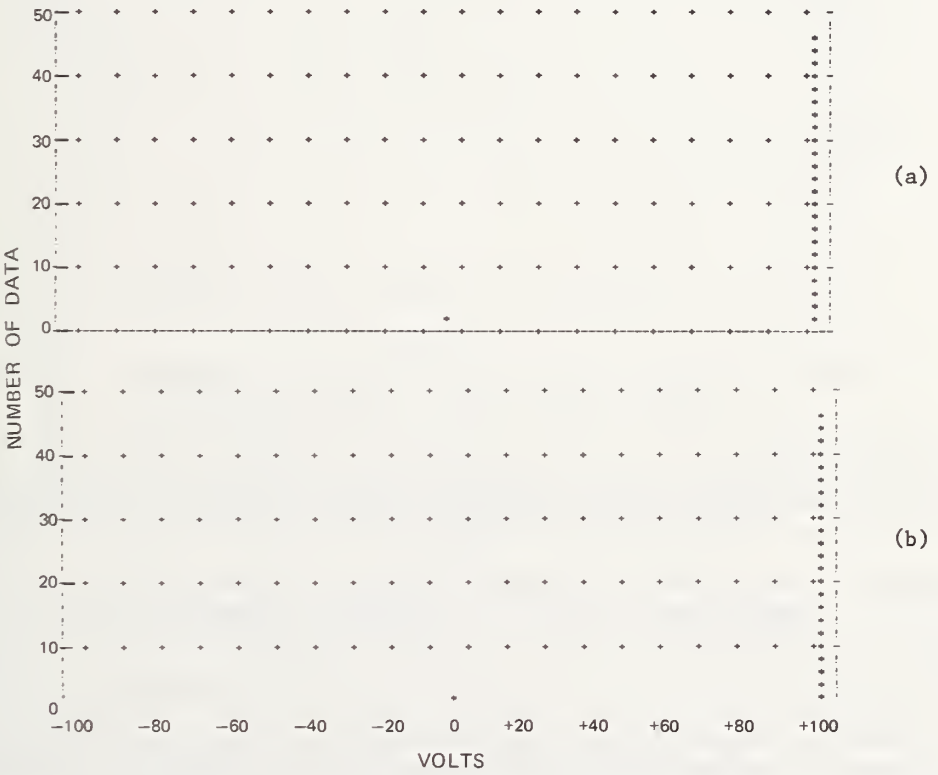


Figure 64.1. Histograms of dielectric strength for aluminum gate structures (a) I-27 and (b) I-28. Scale is -100 to +100 V.

The same program was used on the poly-gate structures with the results shown in figure 65. These scales are the same as those for the aluminum-gate devices but the data are entirely different. In this case many examples of structures which failed at intermediate voltages are found. The structure with large poly covering only the top of the epi (I-29) all failed at 95 V. The small structure covering only the top of the epi (I-30) had a few which did not fail and, surprisingly perhaps, several which failed near zero. These failures are not completely explained. A small tail near the peak distribution is also noted and currently unexplained. In any case distinct differences are found which were not expected.

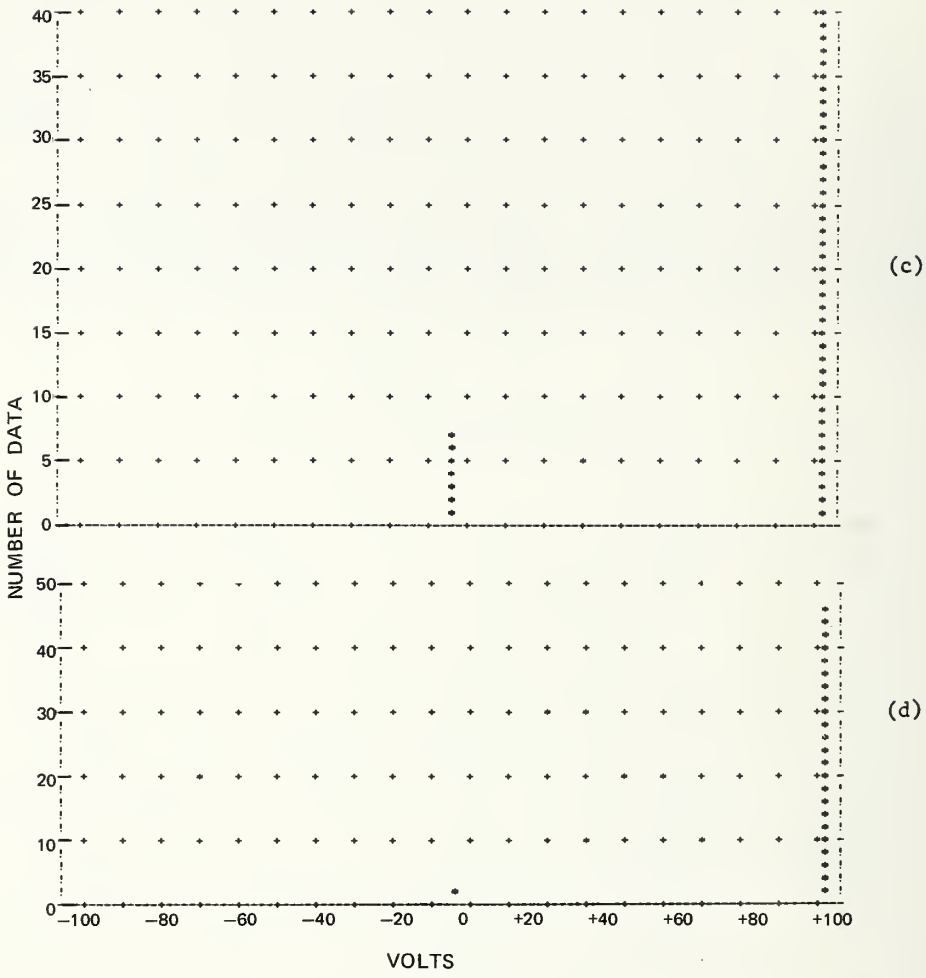


Figure 64.2. (Continued). Histograms of dielectric strength for aluminum gate structures (c) I-25 and (d) I-26. Scale is -100 to +100 V.

When the poly is allowed to cross the island edge, first-order effects are found. Structure I-24 has only a small amount of poly crossing the edge yet the entire distribution is changed. (Detailed TEM examinations have revealed the reason for this behavior and will be reported at a future date.) Some data on this subject were recently reported (ref. 15). Most of the data lies between -35 and +35 V but some data exist at which no breakdown was found. This indicates that not all of the structures failed at the edge and that either these devices failed "open" or that not every exposure to the edge is fatal. Since I-29 all failed at 95 V and none of the I-24 devices *failed* at more than ~50 V, it is very suspicious that I-24 should exhibit superior performance. A failed open state is therefore tentatively concluded for the unfailed I-24 devices; perhaps the narrow poly melted. This contention could be tested by using structure I-14 (the p^+ poly crossover structure). The other structure which contained the edge, I-30, showed no anomalous high breakdowns and showed a strong increase in the population near zero. When the corner was added in structure I-32, the population near zero increased still further.

15. Ham, W. E. and Eaton, S. S., "Anomalous Electrical Gate Conduction in Self-Aligned MOS Structures," Technical Digest IEDM, Cat. No. 76 CH1151-OED, Abstract No. 14.2, pp 323-326, Washington, DC (Dec 1976).

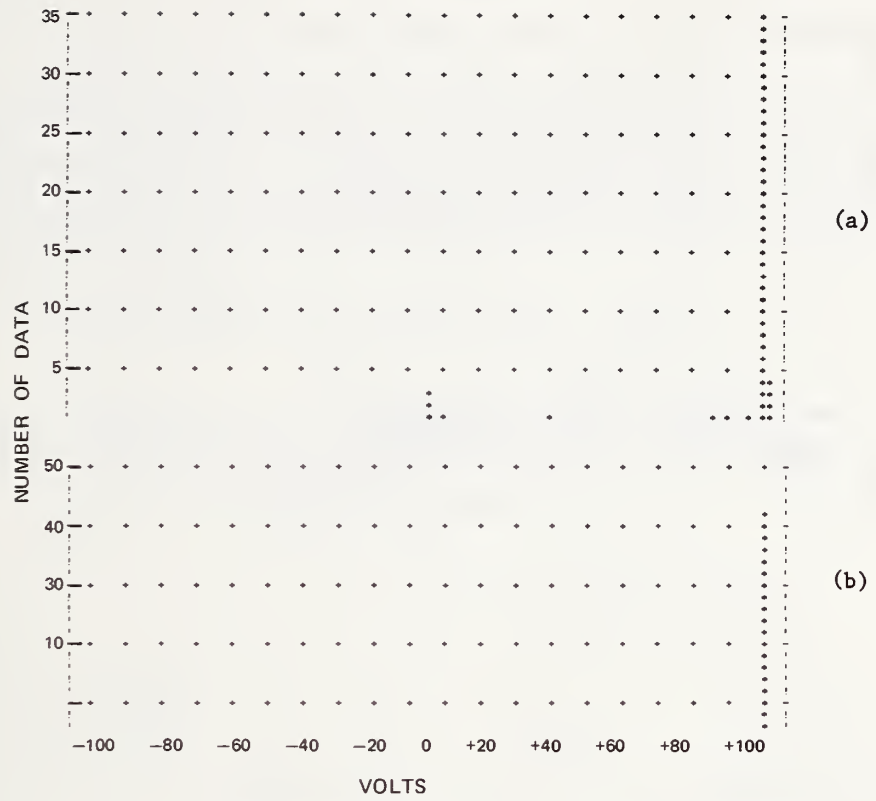


Figure 65.1. Histograms of dielectric strength for poly gate structures (a) I-30 and (b) I-29. Scale is -100 to +100 V.

Figures 64 and 65 contain significant information. Relatively detailed statements can be made concerning the effects of physical structure on the behavior of the dielectric strength by comparing the results from these structures with each other. They are as identical as possible in every way except in those differences *designed* into the structures.

Potential Pitfalls - If one attempts to use the "edge mostly" structures for C-V measurements, he will find that the measured capacitance will depend very strongly on the alignment of the poly or aluminum to the epi. (This feature can actually be used to test for alignment [16]). There are some questions concerning the performance of the small poly device (I-30) as discussed above.

Overall Usefulness - This description is extremely useful for measuring the effects of structure on the electrical properties of MOS diodes. No improvements are suggested.

Related Structures - These structures are related to the structure of subsection 3.3 and to every other structure using an MOS configuration. They are closely related to I-33, I-34, I-35, I-36, I-37, I-38, I-39, I-40, I-41, I-42, I-43, I-44, II-1 and II-2.

16. Ham, W. E., "Data Acquisition for Laboratory Use" in *ARPA/NBS Workshop III - Test Patterns for Integrated Circuits*, NBS Special Publication 400-15 (1976).

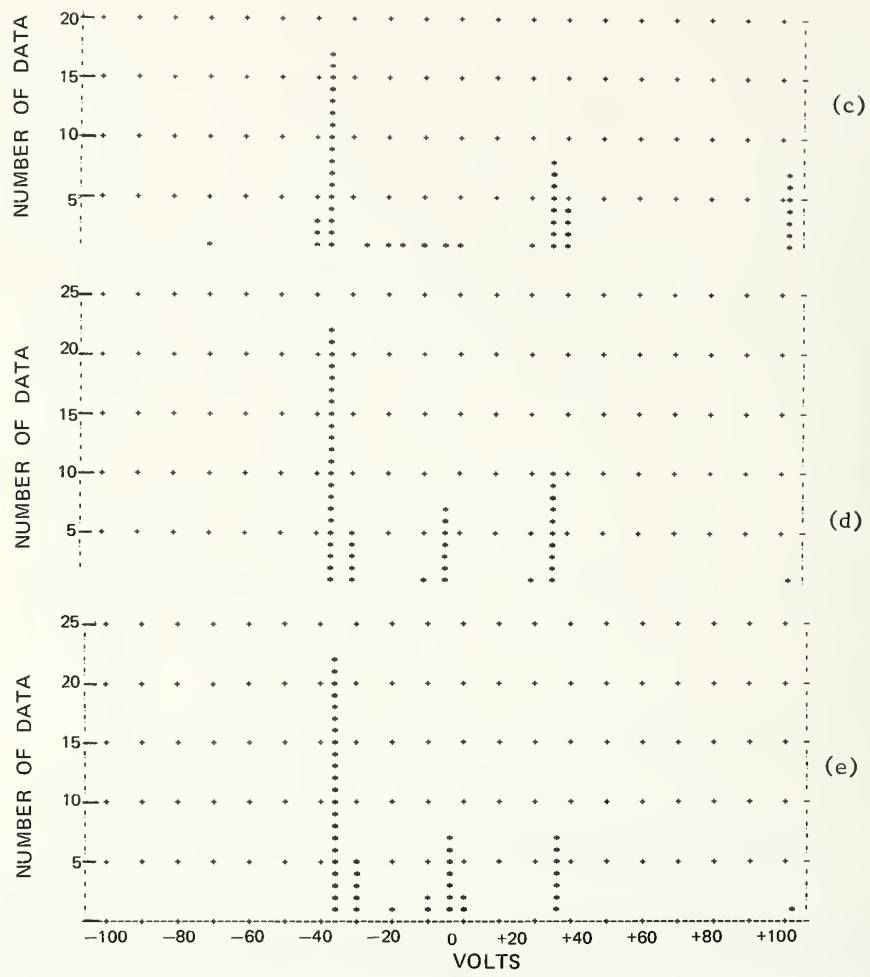


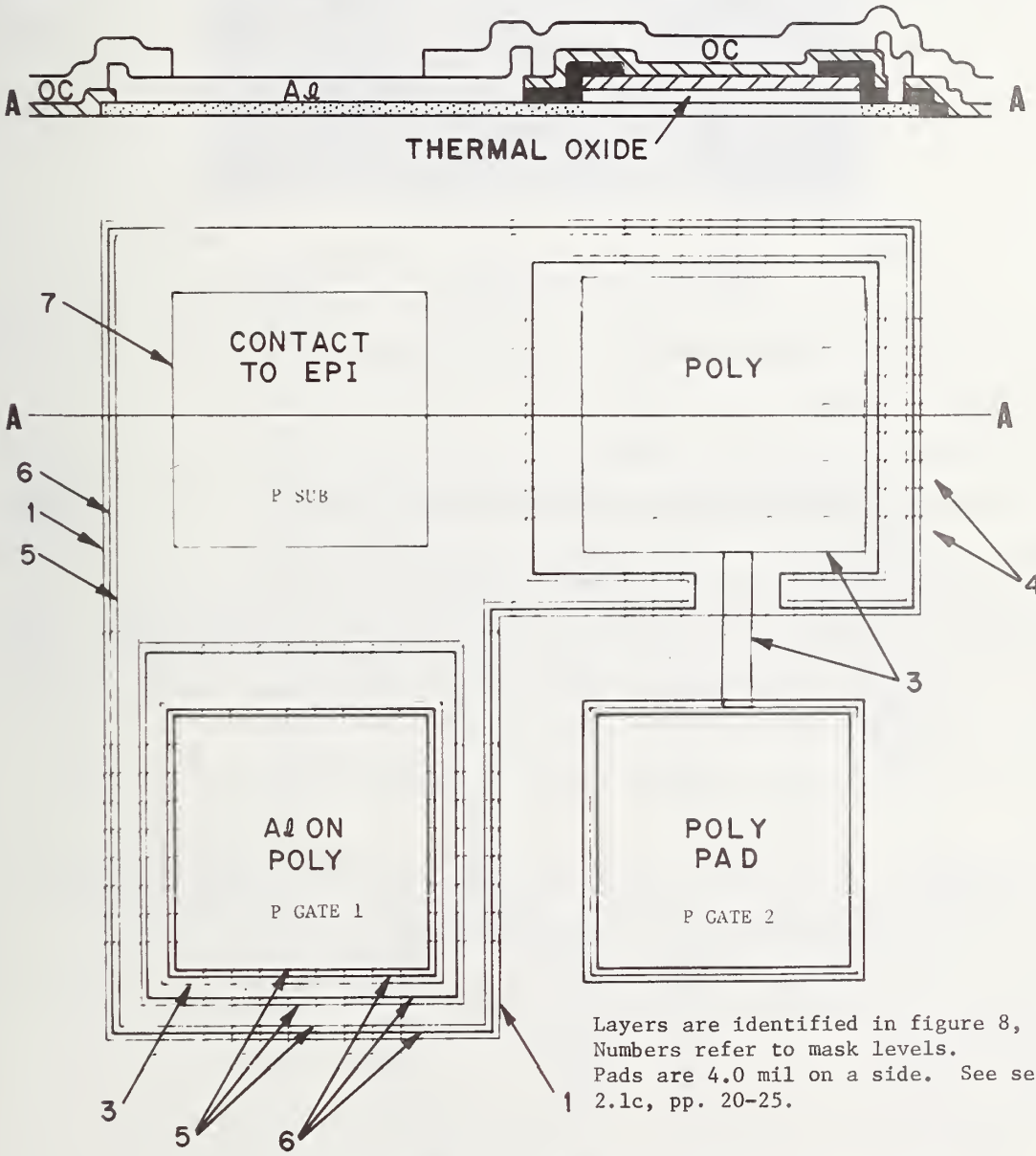
Figure 65.2. (Continued). Histograms of dielectric strength for poly gate structures (c) I-24, (d) I-31, and (e) I-32. Scale is -100 to +100 V.

3.6 Poly MOS Capacitors on Epi-Double Contact Type - I-41, I-42, I-43, I-44

Purpose - This test structure measures parameters derivable from low-frequency type C-V curves.

Verbal Description - These structures consist of poly on epi with alternating n^+ and p^+ diffusions surrounding the periphery of the poly. In one structure (I-42 and I-43), the poly is confined entirely to the top surface of the epi with Al covering most of the poly surface. The other structure (I-41 and I-44) has the poly connected to an external poly pad. These structures may be probed without placing the probe over the active area of the capacitor. In addition, aluminum over the active area is avoided. As in the structures in description 3.5, the active area is 16 mil^2.

Line Drawing - The line drawing for this structure is shown in figure 66.



Layers are identified in figure 8, p. 23.
Numbers refer to mask levels.
Pads are 4.0 mil on a side. See section 2.1c, pp. 20-25.

Figure 66. Poly MOS capacitor on epi-double contact type, test structures I-41 through I-44, computer drawing and cross section.

Halftone Photograph - The photomicrograph for this structure is shown in figure 67.

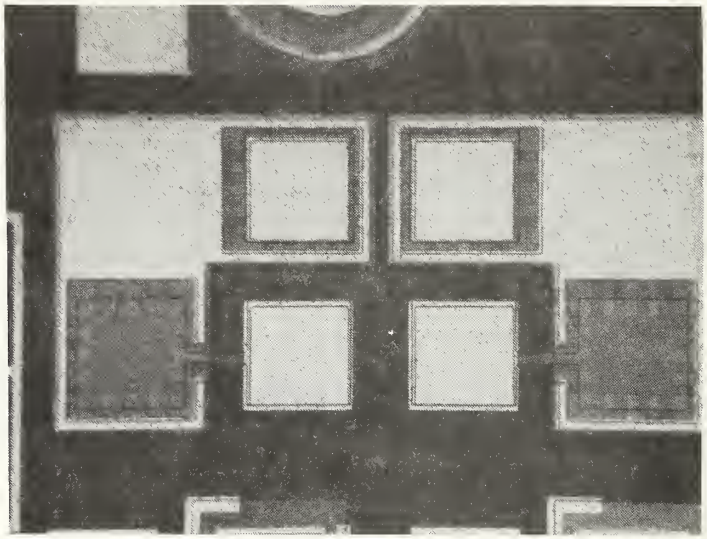


Figure 67. Photomicrograph of poly MOS capacitors on epi-double contact type, test structures I-41 through I-44.

Electrical Access Points - This structure has three electrical access points:

- "Substrate" contact P SUB
- Gate contact - top only P GATE 1
- Gate contact - top mostly P GATE 2

Testing Method - This structure may be tested as described in subsection 3.4 or may be tested by C-V, G-V methods. The alternating diffusions provide a low frequency type C-V plot at high frequencies since an ample supply of minority carriers exists at the perimeter of the gate regardless of the material type. This structure is primarily used for diagnostic purposes and was not tested automatically here. One can determine the approximate gate voltage at which inversion occurs independent of mobility with this structure. Examples of data from a structure very similar to this are shown in subsection 3.25. This type of structure is described in detail in ref. 14.

Potential Pitfalls - There are no potential pitfalls that are not common to any SOS/MOS capacitor.

Overall Usefulness - This structure provides the ability to examine the entire surface potential range on the same interface at relatively high frequency (>10 kHz). This can be useful for diagnosing effects of annealing schedules, radiation damage, etc. This structure is not normally automatically tested. No improvements are suggested.

Related Structures - Structure II-2 is nearly identical. Also I-64, I-65, I-66, I-67, I-68, I-69, II-1, III-11, III-12, and III-13 are related.

3.7 MOS Capacitor; Single Diffusion on Poly - I-33, I-34, I-35, I-36, I-37, I-38, I-39, I-40

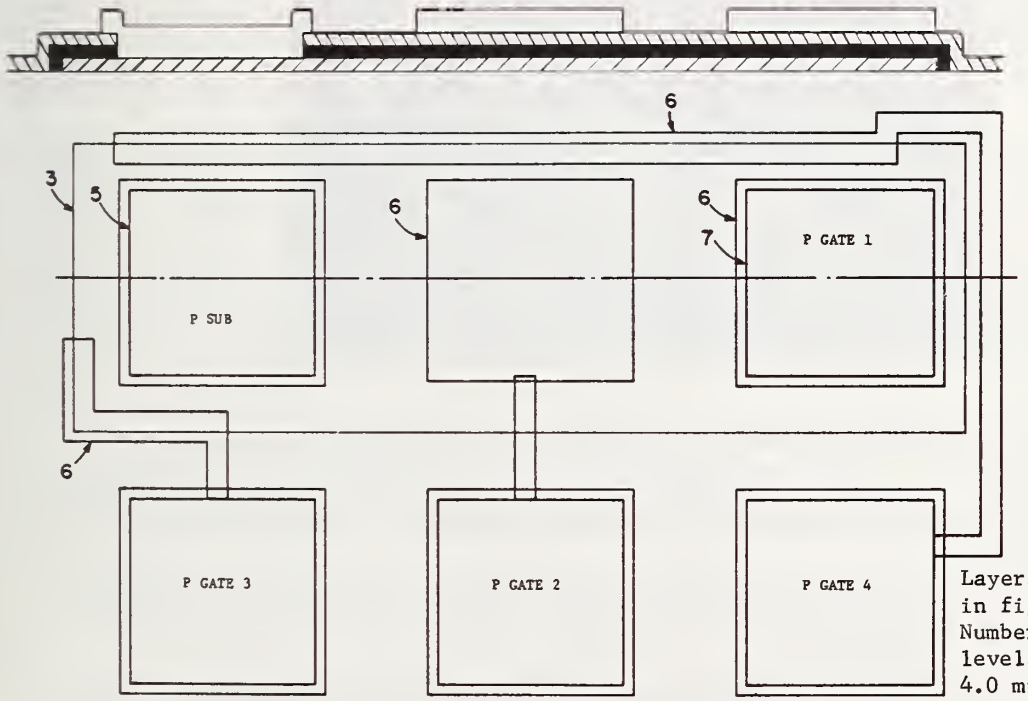
Purpose - The purpose of this test structure is to measure dielectric strength and thickness of deposited doped oxide and possibly to indicate the doping level of diffusion.

Verbal Description - This structure is similar to the aluminum capacitors on diffused epi described in subsection 3.4 except that diffused poly is used. There are four different capacitors and an ohmic contact in this structure. Each rectangle is approximately 4.0 mil (102 μm) on a side. The ohmic contact is the upper left rectangle. It provides electrical contact to diffused epi. The four capacitors are described as: (1) metal confined entirely to the top of the epi; (2) most metal confined to the top of the epi but contact made at external pad; (3) metal overlapping the epi edge; (4) metal crossing an epi corner. In the process under consideration, the dielectric would normally be deposited doped oxide several thousand Å thick.

Electrical Access

- "Substrate" contact — P SUB
- Gate - top only — P GATE 1
- Gate - top mostly — P GATE 2
- Gate - corner — P GATE 3
- Gate - edge mostly — P GATE 4

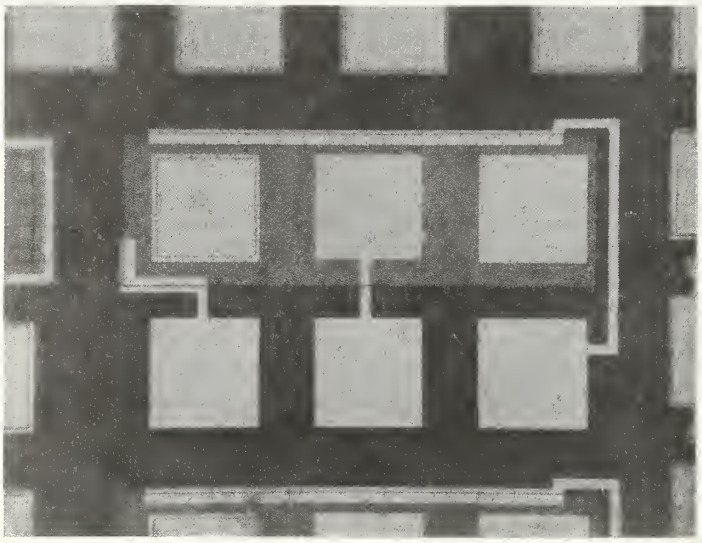
Line Drawing - The line drawing for this structure is shown in figure 68.



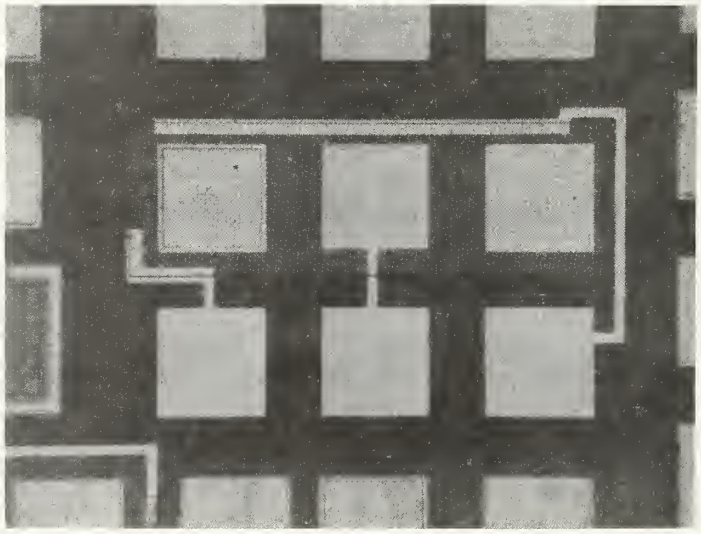
Layers are identified in figure 8, p. 23. Numbers refer to mask levels. Pads are 4.0 mil on a side. See section 2.1c, pp. 20-25.

Figure 68. MOS capacitor-single diffusion on poly, test structures I-33 through I-40, line drawing.

Halftone Photograph - The photomicrograph for this structure is shown in figure 69.



(a)



(b)

Figure 69. Photomicrographs of MOS capacitor, (a) n^+ poly and (b) p^+ poly.

Testing Method - This structure is philosophically identical to that described in subsection 3.4 and is automatically tested precisely the same way. The only difference is that the silicon here is poly.

For this structure C-V measurement may be used with less care than with the devices of subsection 3.5 since the silicon is highly conductive. Similar tests can also be applied to the structures of description 3.5.

The main information sought from this structure is the effective dielectric strength. Also of interest is the doping level of the diffused silicon and the electrical dielectric thickness.

Since the material is heavily doped, one would not expect a significant variation in capacitance with applied dc voltage. On the other hand, if a significant variation were found, it would suggest that the silicon was not diffused properly. The capacitance-voltage measurements may be made between P GATE 1 and P GATE 2 to avoid possible problems with the ohmic contact P SUB.

The effective electrical dielectric thickness is determined by the value of the capacitance and the area of the metal.

The suggested manual testing procedure is:

- Measure capacitance between P SUB and P GATE 1.
- If value is reasonable, measure variation in capacitance with applied voltage. It should be small. If significant, either doping is low or ohmic contact is giving problems. If value is not reasonable, determine if the dielectric is short-circuited or if the ohmic contact is bad. (Other test structures are used for the ohmic contact test.)
- If dielectric is short circuited, stop. If ohmic contact is bad, measure capacitance as a function of voltage between P GATE 1 and P GATE 2. Significant variation indicates a relatively low doping level.

Samples of Data - The histograms in figures 70 and 71 were obtained from the structure using the test programs described in subsection 3.4. The beginning voltage was 0.1 V, the step size was 5.0 V, and the highest test voltage was 95 V. The fail limit was 1.0 μA. All plots have the same scales (-100 to +100 V). It is readily seen that only two populations exist, namely, those which fail at low voltages and those which do not fail at 95 V. This is strongly suggestive of pinholes in the oxide since no intermediate population is seen. Other wafers tested which were fabricated at a different facility were much better having very few shorts and still having no intermediate population. We can conclude from these data that no fundamental problem exists due to the structure and that pinholes are the dominant failure mode. (There may be a slight tendency for the top only device to have fewer shorts.) Similar tests on the same wafer using description 3.4 (Al on epi) showed many fewer short-circuits. This strongly suggests that the pinholes are basically caused by the poly (possibly by "black specks").

Potential Pitfalls - The only problem likely to occur is that, if the dielectric strength of the edge is low, P GATE 2 may be unsuitable for making the capacitance measurements at high gate voltages.

Overall Usefulness - This structure has clearly been very useful for determining the properties of the field oxide. One small improvement would be to make the nominal area of the edge-mostly structures the same as the top-mostly structures. This would eliminate any difference due to area and would make the interpretations somewhat more certain. The corner structure could be made to have the same edge length and top area as the others and could be made to cross two corners.

This different behavior in field oxide pinhole density has been one of the most glaring differences between processes and facilities that has been found.

Other Related Structures - This structure is related to those described in subsections 3.3 and 3.4.

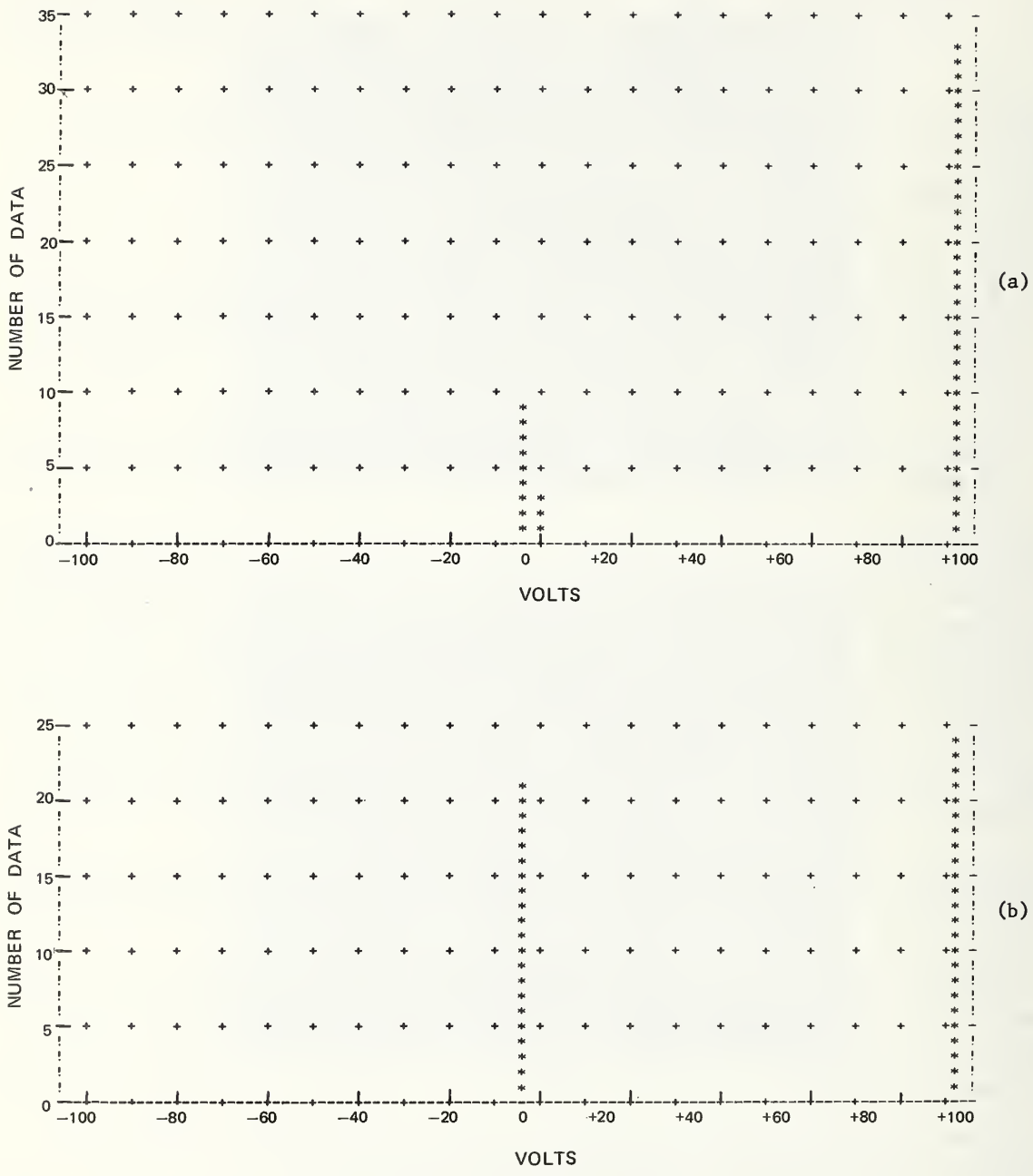
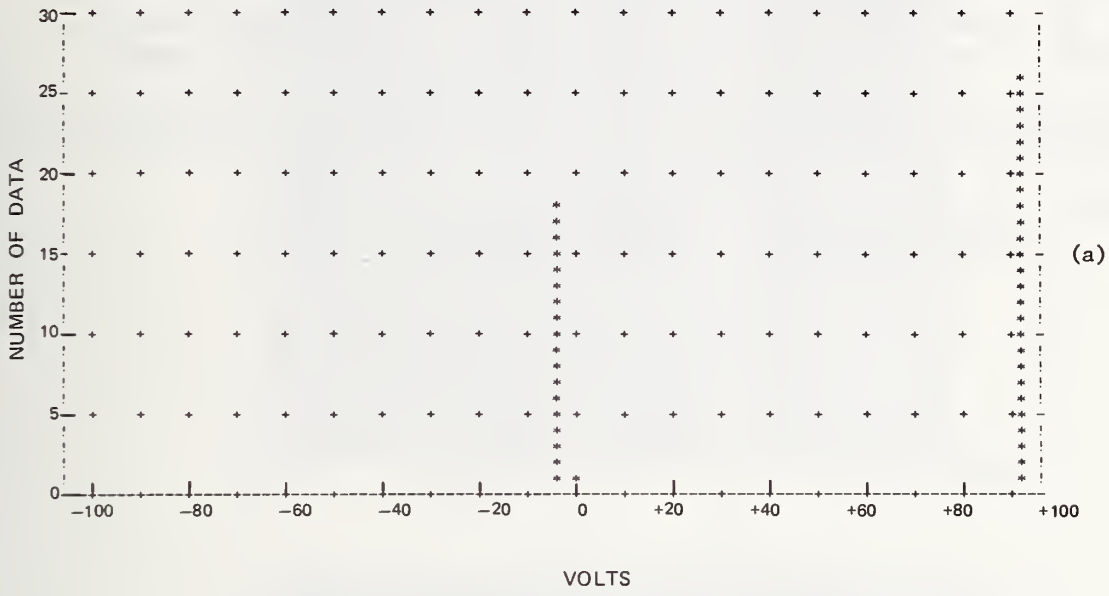


Figure 70. (a) Histogram of I-33 result (top only).
(b) Histogram of I-34 result (top mostly).



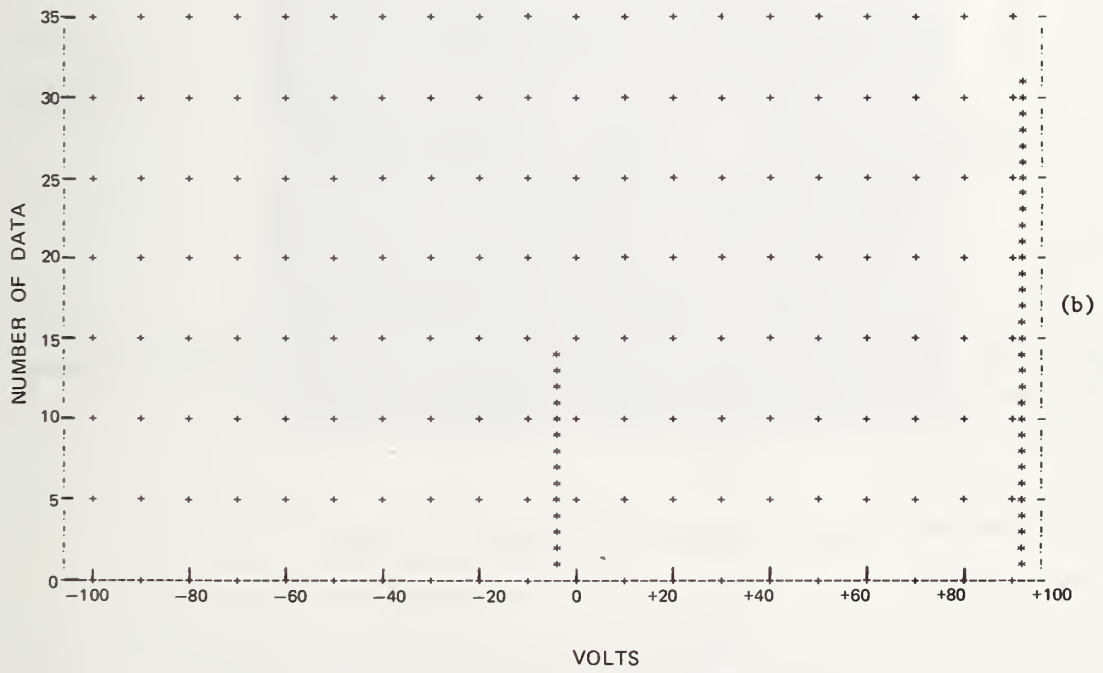


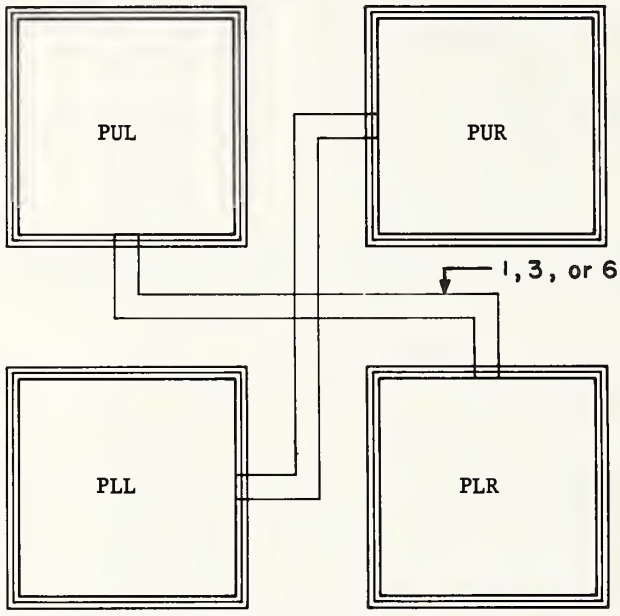
Figure 71. (a) Histogram of I-35 results (edge mostly).
(b) Histogram of I-36 results (corner).

3.8 Ungated van der Pauw Sheet Resistor - I-45, I-50, I-51, I-52, I-53

Purpose - The purpose of test structure I-45 is to measure metal resistivity; structures I-50 through I-53 measure resistivity and Hall coefficient of semiconductor elements.

Verbal Description - These structures are in the form of a cross with 0.4-mil-wide arms. The distance from the center of the cross to the pads is 4.0 mil. These structures have a ratio of periphery-to-contact of approximately 20.

Line Drawing - The line drawing for this structure is shown in figure 72.



Layers are identified in figure 8, p. 23.
Numbers refer to mask levels.
Pads are 4.0 mil on a side.
See section 2.1c, pp. 20-25.

Figure 72. van der Pauw sheet resistor; ungated, test structures I-45, I-50 through I-53, computer line drawing.

Halftone Photograph - The photomicrograph for this structure is shown in figure 73.

Electrical Access Points - In addition to the implied points from which the structure must be isolated (the substrate and neighboring devices), there are four electrical access points. Since these are all functionally equivalent and symmetrical, we do not distinguish between them on the basis of electrical function. Instead they are identified with respect to some arbitrary reference (the bottom of the page in this case) as:

- Upper left pad PUL
- Upper right pad PUR
- Lower left pad PLL
- Lower right pad PLR

Testing Method - Van der Pauw measurements may fall into one or more of the following classifications:

- Symmetrical
- Unsymmetrical
- Steady-state ac
- Steady-state dc

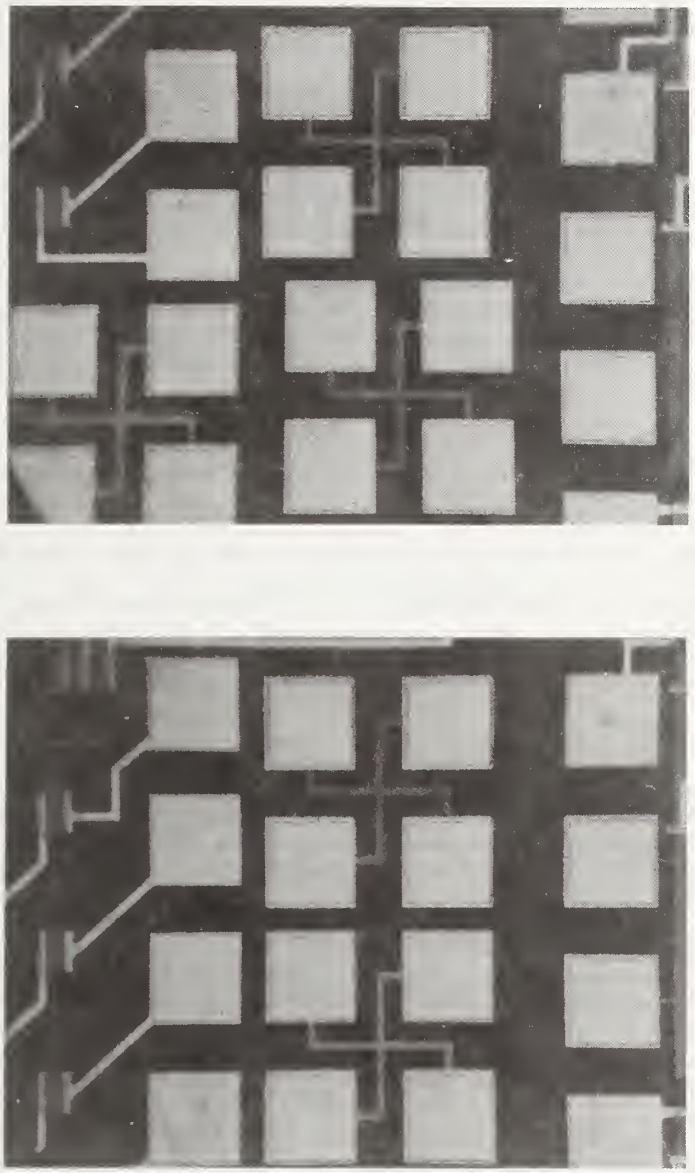


Figure 73. Ungated van der Pauw structures.

- Gate-controlled (Description 3.9)
- Non-gate-controlled (Described in this section)
- Hall effect
- Sheet resistance

Van der Pauw measurements have the outstanding advantage that small changes in the geometry of the structure cause no important changes in the measurement; this is the main reason why they are included. They also provide the ability to examine small areas. In general, the parameter sought from this structure is the sheet resistance. The Hall effect is also available, but, in general, the data are not obtainable with automatic testing equipment. We shall restrict the testing of these structures to the sheet resistance.

We assume that any photolithographically defined structure designed by a reasonably knowledgeable person will be completely symmetrical since there is no apparent advantage to using a nonsymmetrical structure.

The measurements required for the van der Pauw structures do not depend on frequency for most situations. The only issue distinguishing the frequency of the measurement is noise (electrical or thermal). The testing conditions are specified therefore in dc terms, with it being understood that, if necessary (and/or possible), an ac excitation may be used. The ac excitations will remove the necessity for both positive and negative measurements.

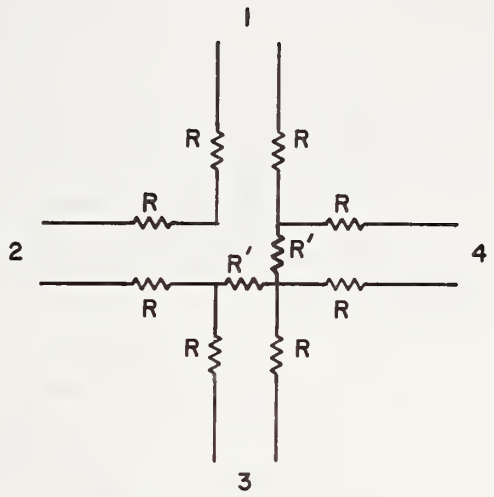
The main classification which must be specific for the van der Pauw structure is the dependence of the sheet resistance on surface potential. Although the essential measurement process is the same for both structures, much greater care must be exercised for the gate-controlled structure. In the same way, it is possible to extract much more information from a careful measurement.

The ungated van der Pauw structures are useful for material which is not substantially affected by surface potential, or for materials whose surface potential is self-determined (i.e., metals). They are designed to be symmetrical.

There are at least two considerations which may cause asymmetrical measurements in these structures: (1) actual asymmetry in the physical structure and (2) actual asymmetry in the electrical properties of the material. It is nearly always found that rotating current and voltage probes by 90^{o} causes unequal results. This necessitates an averaging process which reveals as nearly as possible the desired sheet resistance. This averaging process (if used) removes any possibility of investigating the asymmetry of the electrical properties.

The asymmetry in the physical structure is minimized by constraining the current flow to known paths, and by making the contact points small compared with the periphery. This results in the cross-shaped structure used for all the van der Pauw measurements. With this structure, only electrical asymmetries present near or in the intersection are important in the measurement. This eliminates macroscopic variation as a cause for error.

The structure is made so that the intersection point is definable to a high degree of accuracy with the technology. Each arm is nominally identical. The minimum arm width is determined by the physical uniformity of the edge and by the electrical properties of the edges. Ideally, one would like the edges to be nonconductive and of zero thickness. If the edge is less conducting than the body, the effect is mainly to change the sample dimension to a smaller size. As long as the physical extent of the edge region is small compared with the body (i.e., as long as significant current does not flow in the edge region), no serious error should result. When the edge is more conductive than the body, however, serious efforts can be seen. The current will strongly tend to flow in the edge, both because it is more conductive and because the path length is shorter on the edge between adjacent arms, particularly near the intersection point than it is through the body. It is possible to detect a serious edge conduction by measuring the resistance between different sets of arms. The edge path length is longer between opposite arms than between adjacent arms by a resistance ratio of 2:1.5 as shown in figure 74. Nonidentical resistances between adjacent (R_{adj}) and opposite (R_{opp}) pairs of arms may indicate a serious edge conduction. If the ratio R_{opp}/R_{adj} is consistently the same for all combinations of arms, and is between 1.0 and 1.33, some preferential edge conduction may be indicated. If a semiconductor is being measured and the edges have the opposite conductivity type from the body, then they may not be a problem, even if they are conductive. This depends on the type being used at the end of the arms. If the contacts are, for example, n+ silicon and the edge regions are p-type, no significant currents will flow through the edges since a reverse-biased junction exists at least at one of the contacts on the edge.



$$R_{12} = 2R \| 6R = \frac{12R}{8} = 1.5R$$

$$R_{24} = 4R \| 4R = \frac{16R}{8} = 2R$$

Figure 74. Edge resistance.

If the edges are of the same type as the body, then the situation is much more difficult to detect and eliminate. The resistance test is not sensitive to a conductive edge unless the edge is very much more conductive than the body. This is because the edges on opposite arms are connected *through* the body at the intersection (R' in figure 74). This type of situation must be dealt with on edgeless structures with a four-point probe. The best test for screening out edge problems still seems to be the resistance ratio test, and the structures are defined to be suitable if the resistance ratio is 1.0 ± ~5%. Of course these resistance tests are subject to the same type of errors as any other resistance tests as described in subsection 3.3. To ensure accurate resistance measurements, a Kelvin-type measurement must be made which would require four additional pads and some additional measurement. It is questionable whether most users would be willing to use a structure of this type since it would then be more complicated to use than the bridge structure.

In addition to the resistance ratio tests, other tests to ensure adequate contact are recommended. These tests concern the possibility of spurious connections between contacts and the possibility of the probe and/or the metal pad to the material of interest being unsuitable. The simplest tests require only that a reasonable current be forced through the contacts and that the characteristics of the contacts are stable with time. If the resistance ratio tests are to be used, it is also critical that the contacts be of essentially zero resistance. One property of a good contact is that when zero current is flowing (in the dark), zero voltages be produced at the voltage sensing probes; another very good test is that doubling the current doubles the voltage. Both of these tests are necessary to ensure reasonable operation of the test structure. This structure is intended only for use with linear materials.

Perhaps the most insidious problem with the van der Pauw structure is the possibility of spurious current paths. This problem is especially severe on bulk silicon structures which are junction-isolated. A necessary condition for a valid van der Pauw measurement is that essentially all the current flowing goes through the desired part of the structure. Testing for spurious current paths requires a fifth (and possibly a sixth) contact which may be another pad or the bulk substrate or both. Current must not flow in appreciable quantity from the structure to the fifth contact at the voltage used during the measurement. For SOS, this problem is minimal.

In the most general case where the sample is unknown, the first task is to determine the current level needed for the measurements. In general it is easier to specify the voltage level required because the measured voltage will be much less than the applied voltage. Figure 75 shows that only ∿1.1% of the applied voltage appears across the potential terminals. If four-digit accuracy is needed (for the measurement of the uniformity of ion-implanted layers, for example), a sensed signal of ∿100 mV is required for most automatic testers, and this dictates an applied voltage of ∿10 V. Clearly not all structures can support this much voltage without substantial if not destructive heating. This voltage level is not a problem for the resistive layers of interest here. Using a chart such as figure 75 one can therefore choose the approximate voltage to be applied. The current flowing in each arm is measured and the results are averaged. If this resulting current can be supplied by the equipment, testing is continued.

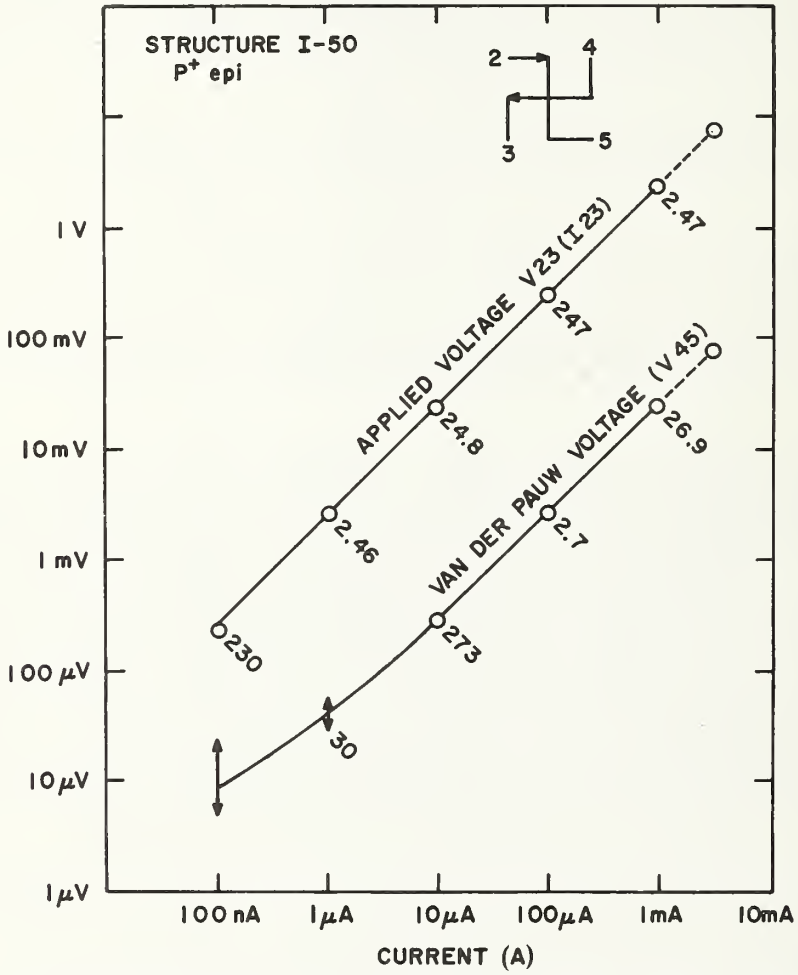


Figure 75. Voltage levels involved in van der Pauw measurements. The number on the curves represent actual numerical values at the decade of current. The arrows on the lower curve indicate the uncertainty in the voltage measurement.

The structure is tested next for spurious current. This problem is relatively small for SOS structures but can be very serious for bulk silicon structures. If the spurious current is too large, testing is halted.

Next, a test is done to ensure that the contacts to the arms are reasonable. This is done by grounding two of the arms and measuring the voltage between the remaining two. It is not necessary that the contacts be of very low resistance, but they must be sufficiently low resistance that they can force the voltage sensing to ground in the time allowed for the measurement. If the measurement is not sufficiently low, the testing is halted and a bad contact is assumed.

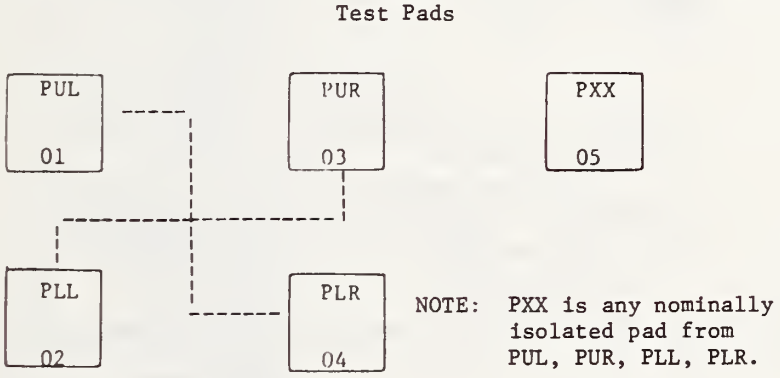
The two-point resistance between each set of arms is measured next. These data are valuable for determining the structural integrity of the arms and also provide a direct internal check on the van der Pauw results if there is no appreciable contact resistance. If the resistance of any arm is greater than a specified maximum, testing is halted. This maximum resistance is provided mainly to ensure that the voltage sensing system is not loading the structure during the measurement.

If the testing reaches this point, a test for linearity and bilaterality is done, which consists of measuring the van der Pauw voltage at the current level found for this structure, at the negative of this value, and at half of this value. Two parameters are calculated to reflect the linearity and bilaterality of the measurements.

Finally, the actual van der Pauw measurements are performed. These consist of measuring the van der Pauw voltages and two parameters which represent the quality of the structure and of the material are calculated.

Initial Parameters -

- Appropriate applied voltage (VAPP)
- Minimum tolerable test current (IMIN)
- Maximum tolerable test current (IMAX)
- Maximum tolerable spurious current (ISPURM)
- Maximum acceptable residual voltage with no current (VIØ)
- Maximum acceptable resistance between arms (RAMX)



Flow Chart - The flow chart is shown in figure 76.

List of Outputs - Figure 77 shows the outputs.

Less General Versions -

- Complete - unknown sample [UVDP1]
- Complete - current level specified [UVDP2]
- Standard - current unknown [UVDP3]
- Standard - current level specified [UVDP4]
- Simplest - current unknown [UVDP5]
- Simplest - current level specified [UVDP6]

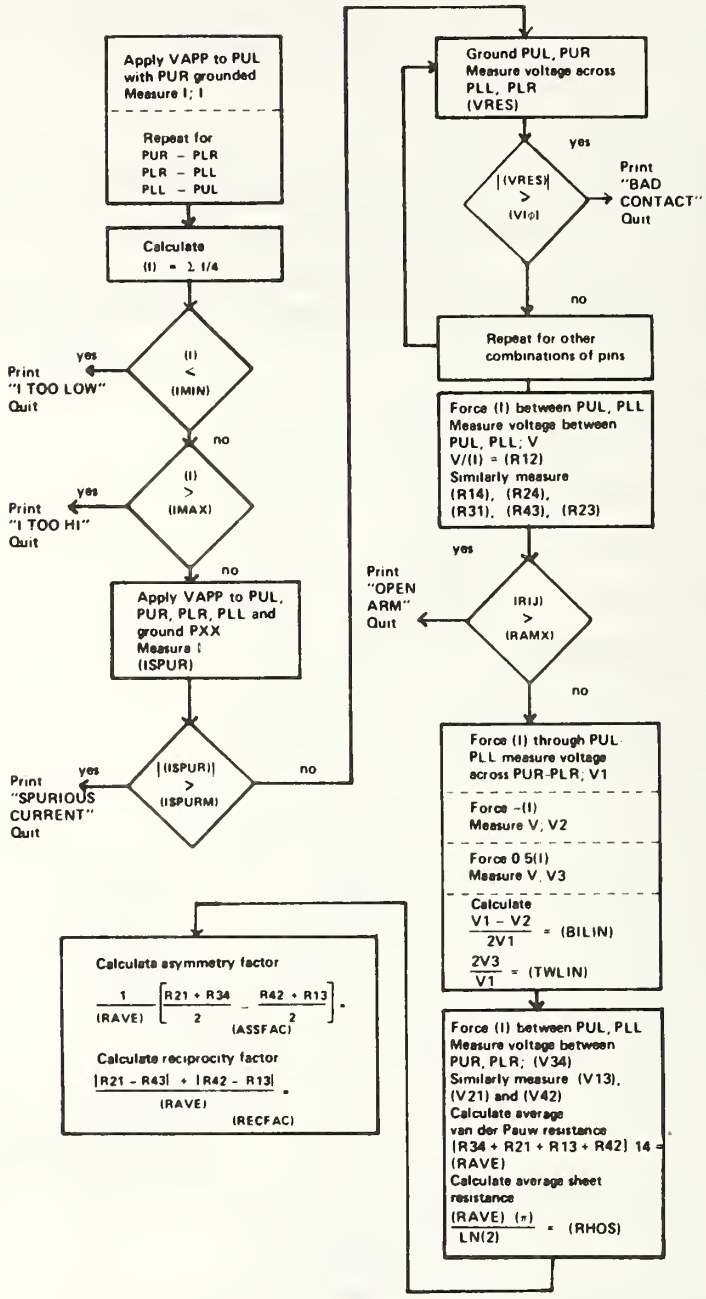


Figure 76. Flow chart for UVDP1

Complete: Test for spurious current

linearity

0I-0V

arm resistance

VDP resistance (asymmetry)

average sheet resistance

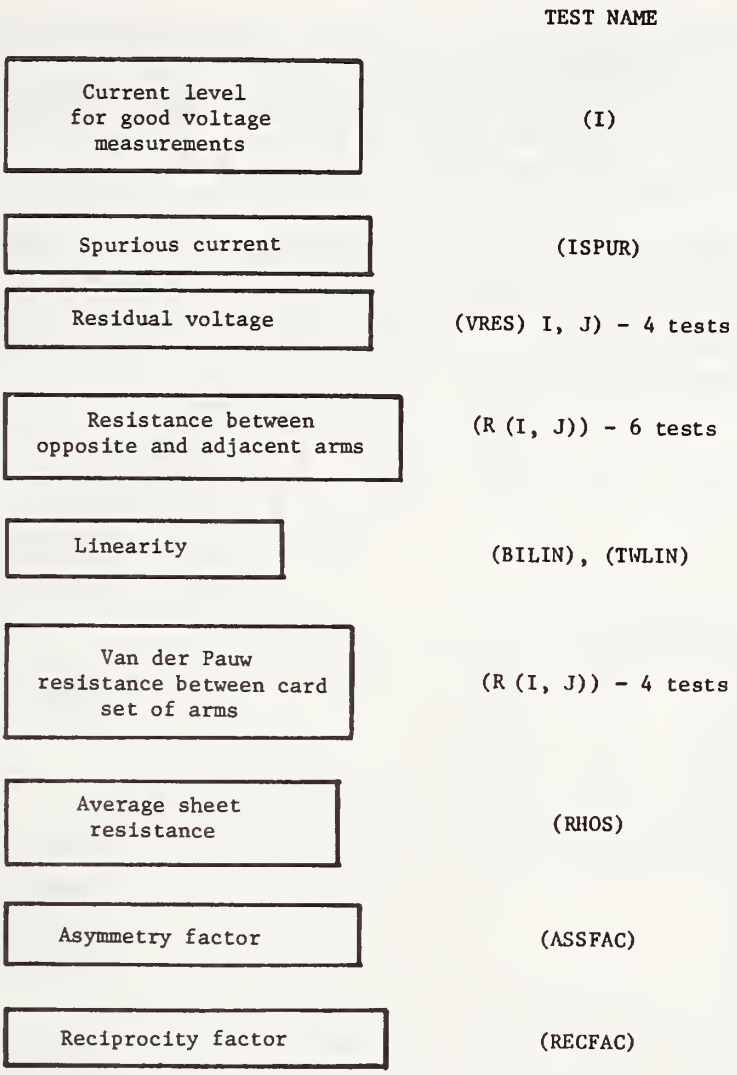


Figure 77. Outputs for ungated van der Pauw test block UVDP1.

Standard: Test for spurious current

OI-OV

average sheet resistance

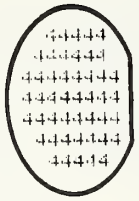
Simplest: Test for average sheet resistance

Special Equipment - As with the structure described in subsection 3.2, a floating voltage sensing system is desirable.

Samples of Data - A relatively extensive examination of this structure has been conducted. According to the results presented in NBS publication 400-21 this structure should have a theoretical error much less than the capabilities of our measurement system. We find this to be true here. Measurements of structure I-53 (p+ poly) indicated that an applied voltage of ~142 mV produced a measured signal of ~1.7 mV for a ratio of ~1.2%. This sheet resistance of this particular poly was measured to be 75.76 ohm/square at 1.00-mA level on the van der Pauw. This result was compared with the conventional bridge-shaped structure

(I-63) where a nominal value of 76.8 ohm/square was measured. In the bridge structure a current level of 1.00 mA produced a measured signal of ~45 mV, or approximately thirty times that of the van der Pauw device. The agreement between the two measurements is well within the uncertainties of the geometry of the bridge-shaped sample. It is therefore quite clear that the cross-shaped van der Pauw structure has no serious design or theoretical problem. This structure allows a very fine spatial resolution of resistivity. Measurements on bulk silicon using structures similar to those of this section have been reported [17].

Figure 78 shows a set of maps from a composite automatic test program. This output clearly shows the location of bad devices. Figure 78(a) is a plot of all tested sites. Figure 78(b) through (e) are the locations of the good structures of each type noted. For example, there are five structures of the type I-50 which were not suitable. All of these were located on peripheral pellets. In fact, there was only one bad structure of any type which was not located on the edge.



(Blanks indicate invalid structure at that position.)

```
WITH ALL BUGS REMOVED
-> XYCAT 2 28 59 90 121
  47 CHIPS FOR TEST   2
CATEGORY MAP   REV 00 00      X =497.504  Y =491.497
   44444
  444444
44444444
44444444
44444444
 4444444
  44444
  42 CHIPS FOR TEST  28
CATEGORY MAP   REV 00 00      X =438.504  Y =491.497
 44444
444444
4444444
4444444
4444444
444444
 444 4
  44 CHIPS FOR TEST  59
CATEGORY MAP   REV 00 00      X =497.504  Y =491.497
  44444
 444444
 4444444
44444444
 4444444
 444444
  44444
  42 CHIPS FOR TEST  90
CATEGORY MAP   REV 00 00      X =437.504  Y =491.497
  44444
 444 44
 4444444
44444444
 4444444
 444444
  4444
  45 CHIPS FOR TEST 121
CATEGORY MAP   REV 00 00      X =497.504  Y =491.497
   44444
  444444
  4444444
44444444
 4444444
 4444444
  44444
```

(a) All tested sites

(b) All sites for which valid data was obtained from structure I-50 (p+ epi)

(c) As B for structure I-51 (p^- poly)

(d) As B for structure I-52 (n+ epi)

(e) As B for structure I-53 (p+ poly)

Figure 78. Wafer of maps of valid structures.

17. Buehler, M. G. and Sawyer, D. E., "Microelectronic Test Patterns Aid Production of Custom IC's," Circuits Manufacturing 17, No. 2, 46-56 (1977).

Figure 79 shows a comparison of the two-point arm resistance for structure I-50. These histograms show that nearly identical distributions were obtained from each set of arms. The fact that nearly all of the arms have the same resistance lends confidence to the accuracy of the measurements. One rarely sees experimental data as closely matched as those of figure 79.

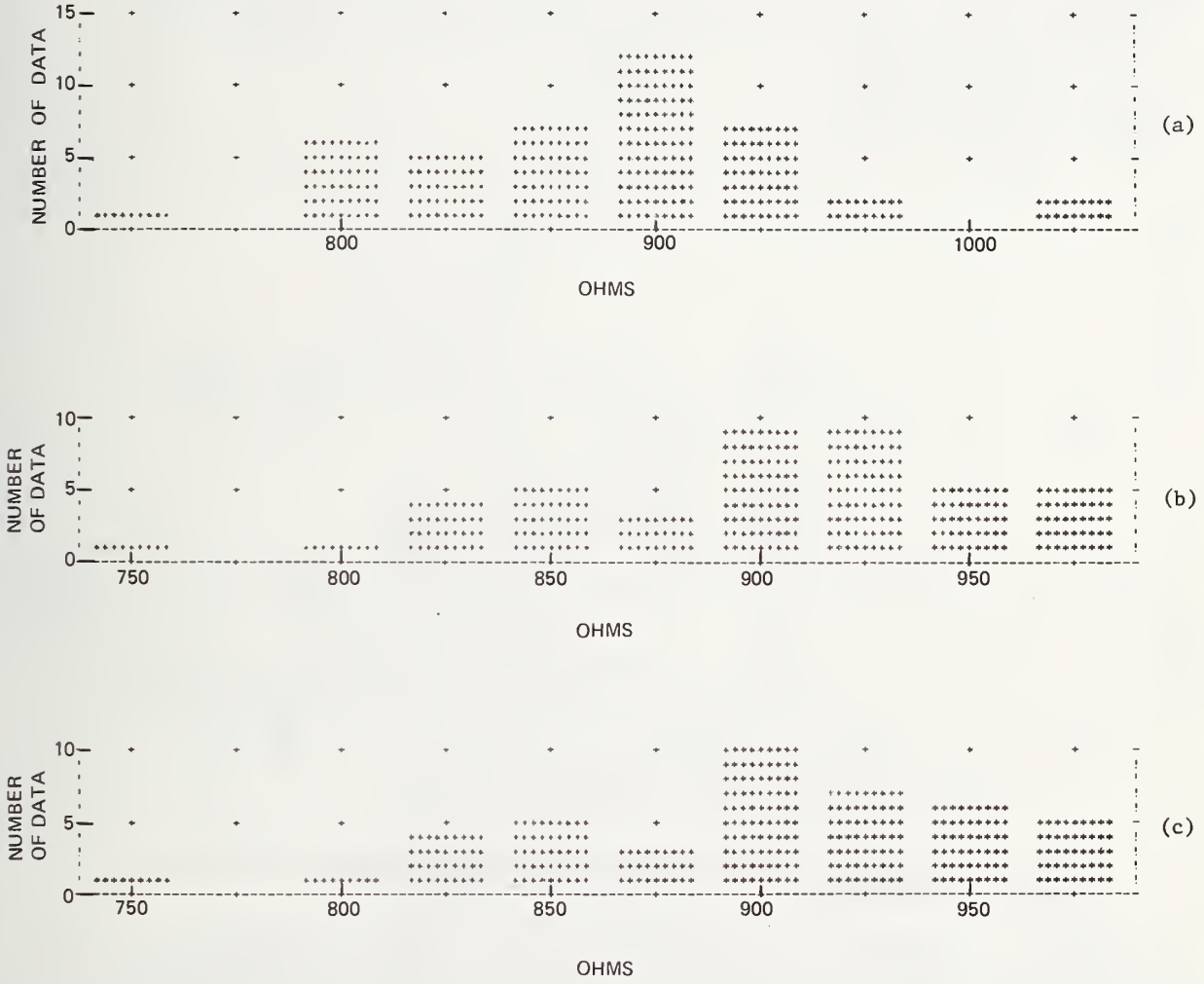


Figure 79.1. (a) through (c). Two-point resistance between all different sets of arms of structure I-50 (p+ epi).

The results of the linearity tests are shown in figure 80. For nearly all of the data, the measurements were bilateral to within 0.8%. The linearity parameter was slightly reduced to approximately 2%. Subsequent experiments revealed that this small error was due to self-heating of the structure during the measurement.

The asymmetry factor is shown as a list of test results in figure 81. Note that (with one exception) the largest asymmetry is 0.033, with the distribution nearly symmetrical around zero. This is quite reasonable, considering the actual dimensions of the structure.

The reciprocity factor shown in figure 82 indicates that the material is of phenomenally good quality, with the largest reciprocity factor being 0.0017.

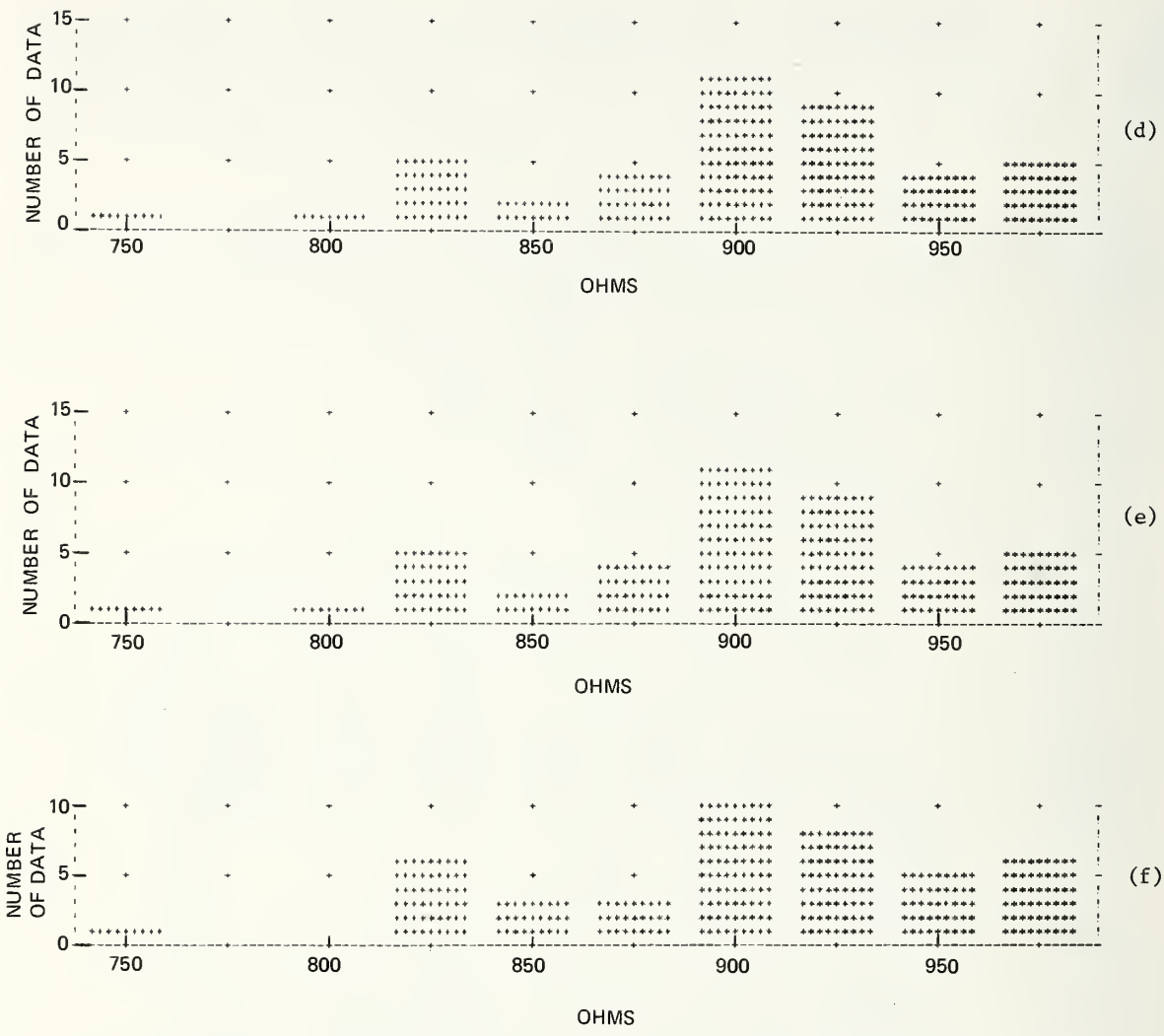


Figure 79.2. (Continued). (d) through (f). Two-point resistance between all different sets of arms of structure I-50 (p^+ epi).

Finally, the van der Pauw sheet resistance is shown in figure 83, where all of the measured values appear. Note that this distribution is quite similar to those seen for the arm resistance in figure 79. It is also worth noting that the expected arm resistance calculated from the approximate number of squares times the van der Pauw sheet resistance is seen to agree well with the measured arm resistance. This set of data for van der Pauw sheet resistance has a great deal of confidence tested into it.

It has also been directly verified that relatively large changes in the physical structure cause no problem with the van der Pauw results. The structure shown in figure 84 produced the correct sheet resistance even though the arm resistance was noticeably asymmetrical. This structure was also successful in measuring aluminum resistance although this had to be carried out manually since the measured voltages were quite low.

Potential Pitfalls - The most important pitfall is that one may neglect to test properly for isolation. Use of this structure on bulk material to test ion-implantation uniformity without doing suitable isolation testing has resulted in vastly erroneous results.

Overall Usefulness - This structure has the advantage that one can measure a very small volume of material without undue concern for the actual size of the structure. If these

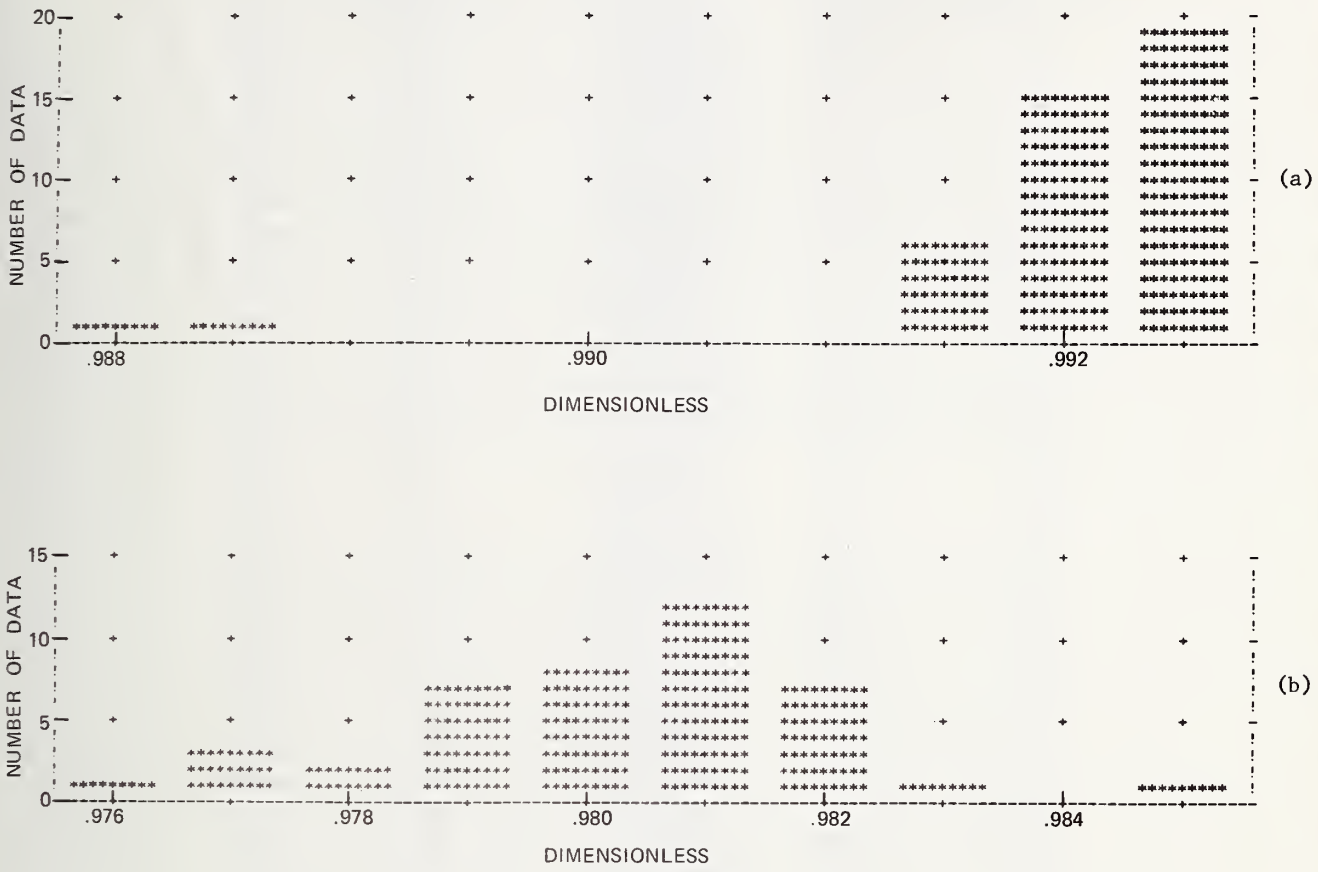


Figure 80. (a) (BILIN) For structure I-50 (p^+ epi).
(BILIN) = effect of reversing current polarity.
Ideal value = 1.000.

(b) (TWLIN) For structure I-50 (p^+ epi).
(TWLIN) = effect of using half the original current.
Ideal value = 1.000.

aspects are of interest, then this structure is of great usefulness since it is perhaps the only structure with these properties. For many applications the more familiar bridge structure discussed in the next section provides all the spatial resolution and accuracy needed. A more important feature of the van der Pauw structure is the ability to perform internal checks on the results. In addition to the van der Pauw method, there is a three-point resistor built into the structure. This method uses current through opposite arms and measures the potential at the center. If the center potential is half of the applied potential this ensures that the contact resistance is at least the same for the two current contacts. Typically for the process used here, the contact resistance would cause an error of the order of 0.1% or less. It is also possible to add additional terminals to the structure to complete immunity from the effects of contact resistance. Such an approach has been reported by Buehler [18] wherein two additional terminals were added to one of the arms. This provided an integration of a bridge structure with a van der Pauw structure. The price paid for

18. Buehler, M. G., David, J. M., Mattis, R. L., Phillips, W. E., and Thurber, W. R., "Planar Test Structures for Characterizing Impurities in Silicon," Extended Abstracts of the Electrochemical Society Meeting, Toronto, Vol 75-1, Abstract No. 171, pp. 403-404, (May 1975).

	CATEGORY	TEST RESULT	X POSITION	Y POSITION
1	4	.00000E 00	503	497
2	4	-.80712E-03	501	497
3	4	-.80052E-03	500	497
4	4	.00000E 00	499	497
5	4	.00000E 00	498	496
6	4	-.80623E-03	499	496
7	4	.00000E 00	500	496
8	4	.00000E 00	501	496
9	4	-.13609E-05	502	496
10	4	-.76366E-03	503	496
11	4	-.13905E-05	504	495
12	4	-.81024E-03	503	495
13	4	.00000E 00	502	495
14	4	-.85526E-03	501	495
15	4	.82486E-03	500	495
16	4	-.12899E-05	499	495
17	4	.00000E 00	498	495
18	4	.81004E-03	498	494
19	4	.00000E 00	499	494
20	4	.00000E 00	500	494
21	4	.00000E 00	501	494
22	4	-.03366E-03	502	494
23	4	.16976E-02	503	494
24	4	.00000E 00	504	494
25	4	-.82402E-03	504	493
26	4	.00000E 00	503	493
27	4	.13949E-05	502	493
28	4	.00000E 00	501	493
29	4	-.17494E-02	500	493
30	4	-.80614E-03	499	493
31	4	-.79895E-03	498	493
32	4	.00000E 00	498	492
33	4	.79308E-03	499	492
34	4	.00000E 00	500	492
35	4	.00000E 00	501	492
36	4	-.85582E-03	502	492
37	4	.84998E-03	503	492
38	4	.77501E-03	503	491
39	4	.82642E-03	502	491
40	4	.00000E 00	501	491
41	4	-.79290E-03	500	491
42	4	.75777E-03	499	491

Figure 81. Asymmetry factor for structure I-50 (p^+ epi).

this approach is loss of symmetry but this is not important if the arms are narrow. It is also possible to form a highly integrated structure by using only one additional pad as shown in figure 85.

This structure bears embarrassing resemblance to the well known Hall bar. The van der Pauw can be used in conjunction with the bridge to actually measure the width of the arm. This method of comparing van der Pauw results with bridge results to obtain a width was reported by Buehler [18].

If the structure is constrained to have only four pads, no changes are suggested.

Other Related Structures - Other related structures are I-46, I-47, I-48, and I-49.

	CATEGORY	TEST RESULT	X POSITION	Y POSITION
1	4	-.90738E-02	503	497
2	4	.20162E-02	501	497
3	4	.20022E-02	500	497
4	4	-.23638E-01	499	497
5	4	.43694E-02	498	496
6	4	.12487E-01	499	496
7	4	-.78247E-02	500	496
8	4	-.16289E-02	501	496
9	4	.73164E-02	502	496
10	4	-.19499E-01	503	496
11	4	-.79911E-02	504	495
12	4	.93242E-02	503	495
13	4	-.90209E-02	502	495
14	4	.47049E-02	501	495
15	4	.25159E-01	500	495
16	4	-.25880E-01	499	495
17	4	.31556E-02	498	495
18	4	.36422E-02	498	494
19	4	.32011E-02	499	494
20	4	-.48355E-02	500	494
21	4	-.21784E-01	501	494
22	4	.10410E-01	502	494
23	4	.33949E-02	503	494
24	4	-.74379E-02	504	494
25	4	-.11123E-01	504	493
26	4	.12111E-01	503	493
27	4	.50221E-02	502	493
28	4	.24699E-00	501	493
29	4	-.12248E-01	500	493
30	4	.25397E-01	499	493
31	4	-.43932E-02	498	493
32	4	-.19320E-01	498	492
33	4	.43575E-02	499	492
34	4	-.16324E-02	500	492
35	4	-.82843E-03	501	492
36	4	-.64197E-02	502	492
37	4	-.21680E-01	503	492
38	4	-.33740E-01	503	491
39	4	-.11976E-01	502	491
40	4	-.21368E-01	501	491
41	4	-.83358E-02	500	491
42	4	.20837E-01	499	491

Figure 82. Reciprocity factor for structure I-50 (p^+ epi).

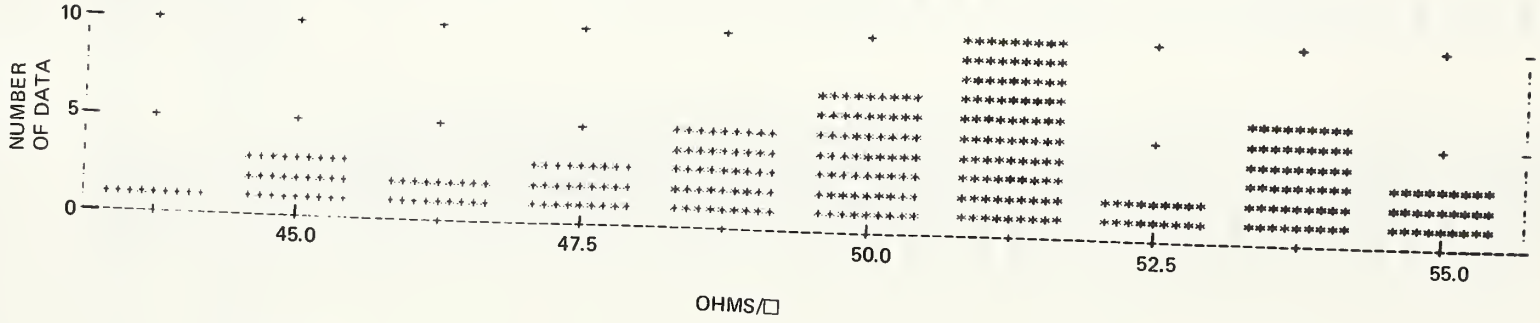


Figure 83. van der Pauw sheet resistance for structure I-50 (p^+ epi).

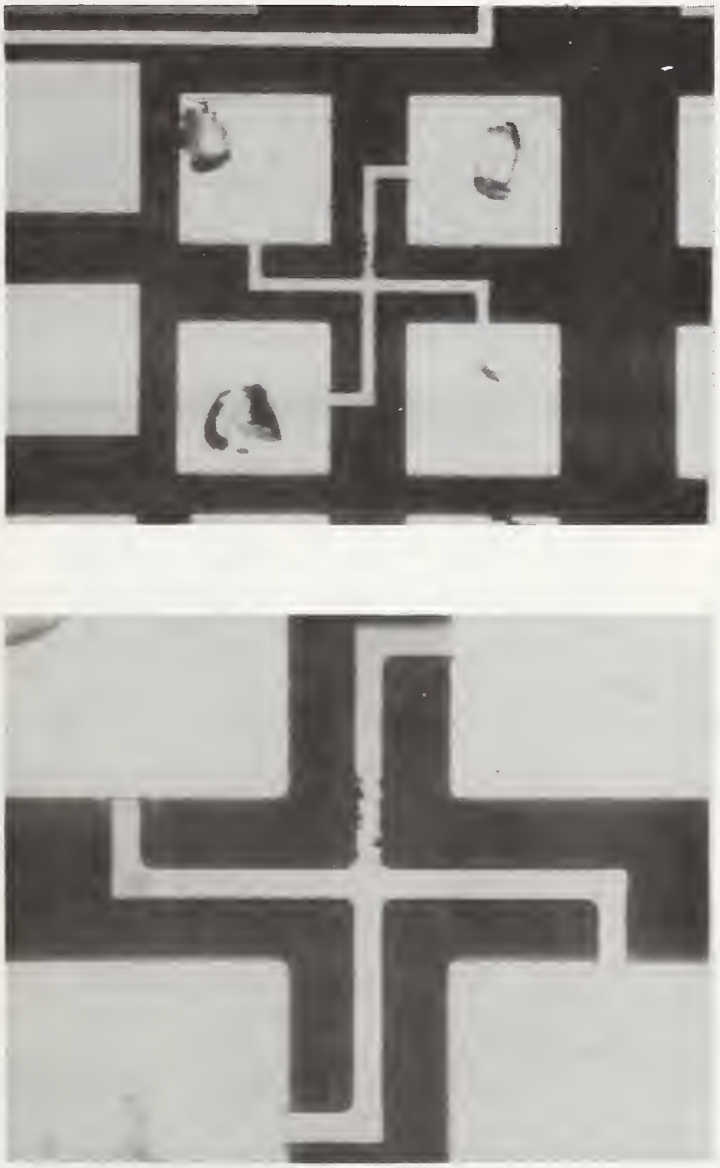


Figure 84. van der Pauw structure where severe physical disruption exists. This structure still works well.

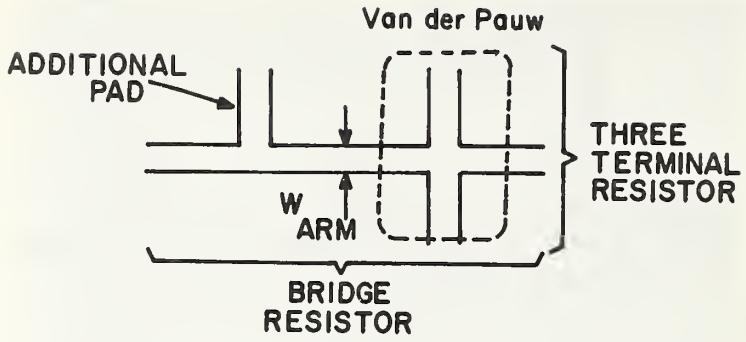


Figure 85. Integrated test structure.

3.9. Gate-Controlled van der Pauw Sheet Resistor - I-48, I-49

Purpose - The purpose of this test structure is to measure epi resistance under controlled surface conditions.

Verbal Description - These structures are identical to that of subsection 3.8 except that a polysilicon gate covers the active area of the device. This process requires that the material under the gate be undiffused. The edge of the gate is removed from the edge of the pad by 0.3 mil. This changes the effective periphery-to-contact ratio slightly to 18.5 from 20 in the ungated structure.

Line Drawing - The line drawing for this structure is shown in figure 86.

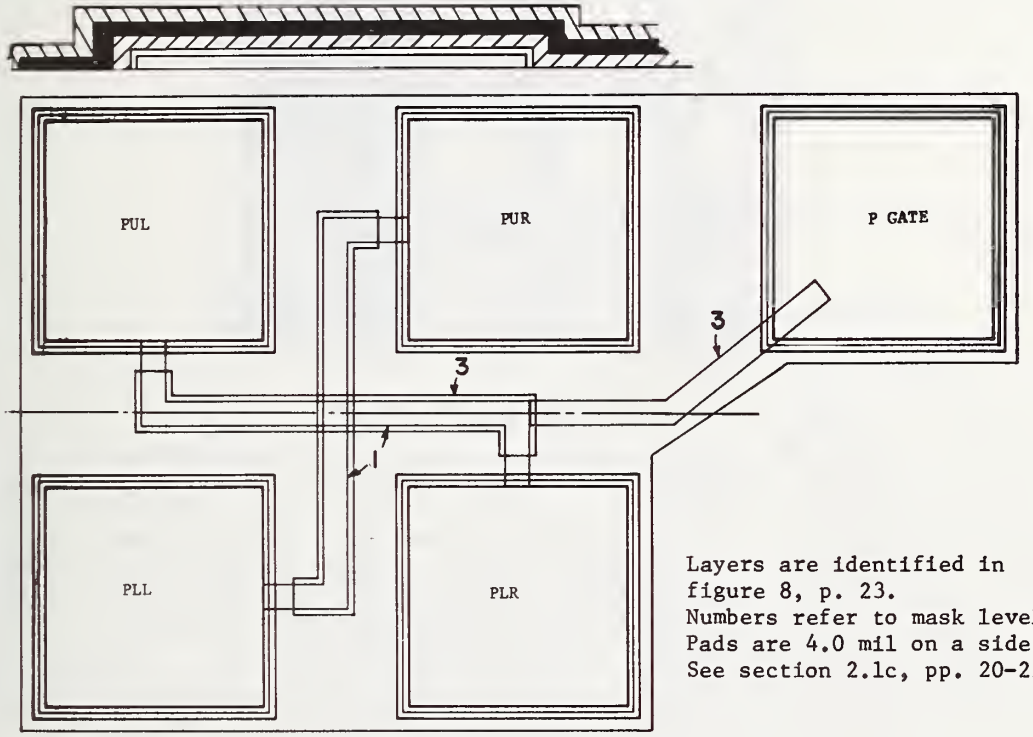


Figure 86. Gate-controlled van der Pauw sheet resistance, test structure I-48 and I-49, computer line drawing and cross section.

Halftone Photograph - The photomicrograph for this structure is shown in figure 87.

Electrical Access Points - These are the same as those of subsection 3.8 except a gate pad is added (PGATE).

Testing Method - This essential structure was first described in references 1 and 2. Precisely the same considerations are given to both the gate-controlled van der Pauw structures and the non-gate-controlled structures except:

- The applied potential must be more carefully controlled.
- The possibility of gate current must be considered both before and after the test.
- This structure is used only for material whose electrical properties are significantly modified by changes in surface potential.

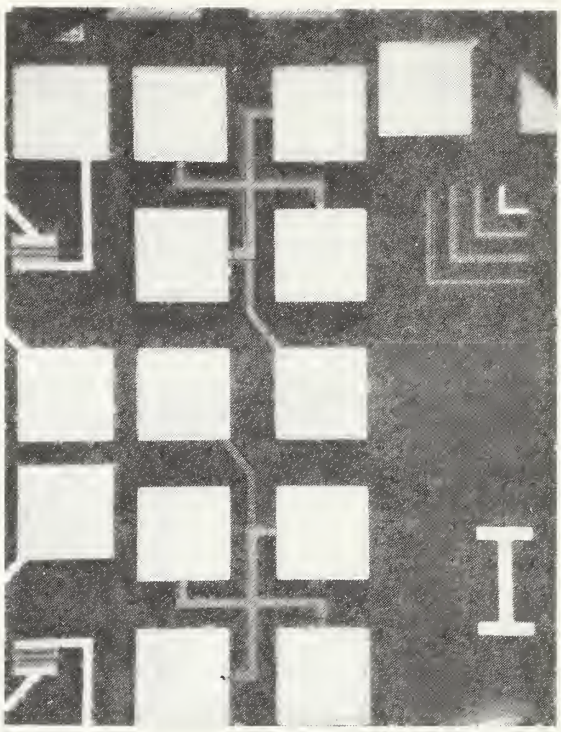


Figure 87. Photomicrograph, gate-controlled van der Pauw structures I-48 and I-49.

The surface potential of the material is not directly determinable from this structure. The results of changing the surface potential can be measured, but the desired gate voltage for the measurement must be determined independently. The reference potential, i.e., the potential of the vertical field-free portion of the material in the intersection, is measured directly by using one of the potential arms. This potential will change as the gate voltage is changed, and, in general, this must be taken into account to establish the desired vertical field. One can maintain a constant known vertical field at the intersection using one of the operational amplifier circuits shown in figure 88. If a floating gate voltage reference supply is available, the top circuit should be used. In the more usual situation where only a single-ended source is available, the bottom circuit will maintain a constant potential across the oxide at this intersection.

This function can also be realized by an iterative procedure or by restricting the applied voltage to low values so that the material potential at the intersection is essentially zero.

The applied potential must be restricted to be less than the dielectric strength of the gate dielectric. It must be great enough to allow a voltage large enough to be measured accurately to appear at the voltage sense terminals. We note that arbitrarily increasing the applied voltage will not linearly increase the measured voltage after the pinch-off point is reached. The voltage will concentrate near the applied voltage terminal under these conditions and will not be transmitted to the intersection region. The applied potential must also be such that nominally the same potential exists throughout the intersection region. For example, if the applied potential must be restricted to be uniform to within 100 mV, then the applied potential must be restricted to $\sim$(100 mV) (18/3) = 600 mV, where 3 is the approximate extent of the intersection region referred to the arm width and 18 is the length-to-arm-width ratio. The gated van der Pauw structure is related to the ungated van der Pauw structure in the same way that the gated bridge resistor is related to the ungated bridge resistor. The discussion in the gated bridge resistor section (3.2) applies here also. The ability to examine small volumes of material under controlled surface conditions is perhaps the most important feature of the van der Pauw structure.

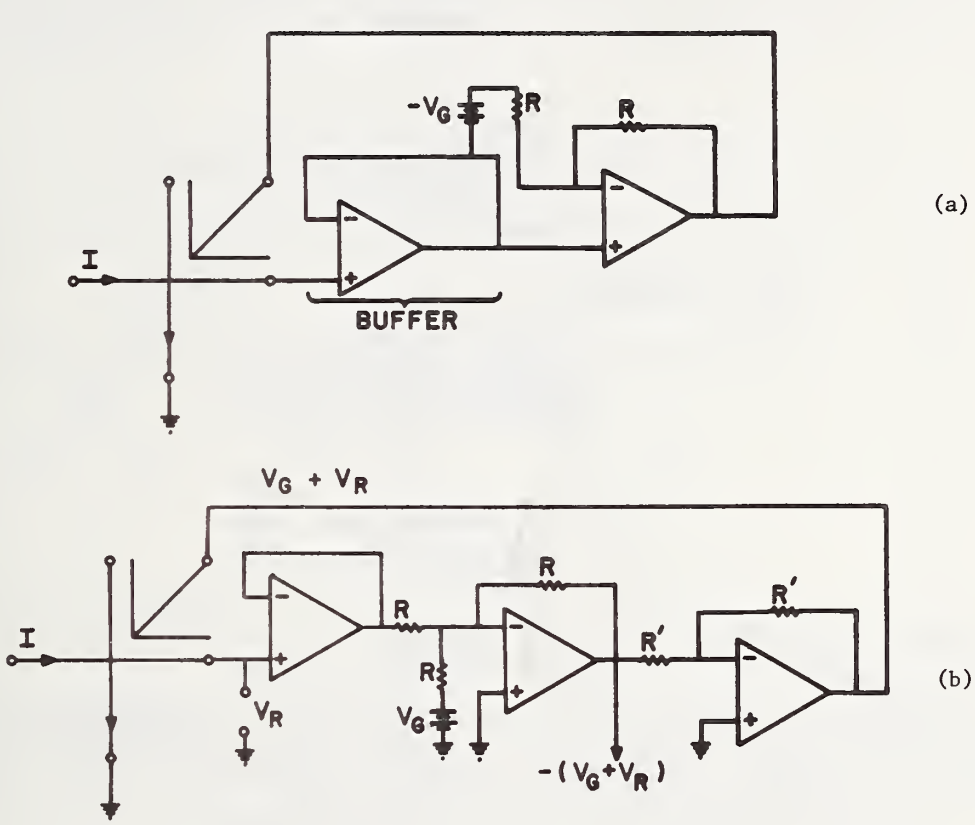
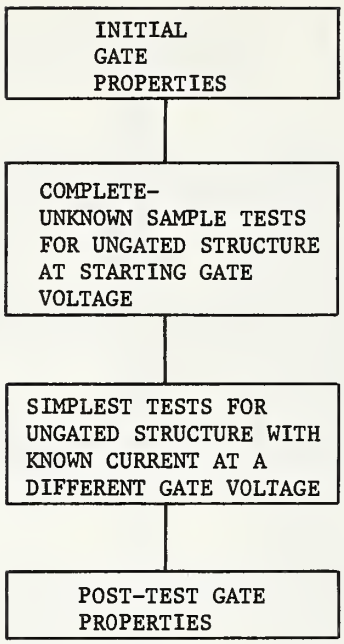


Figure 88. Circuits for maintaining constant gate bias at the intersection. (a) With floating voltage source, (b) with grounded voltage source. Teledyne-Philbrick model 1021 FET input amplifiers have been used for these circuits.

Each time a gate voltage is chosen, a complete ungated type of measurement may be done. Usually only one complete test will be needed and the sheet resistance at the other gate voltages of interest can be measured by the simplest method (block 5 or 6 of the ungated). Since the actual measurements to be used are identical to those of the ungated structure except for the application of the gate voltage, we do not repeat these blocks of tests here.

Flow Chart - A complete test program for the gate-controlled structures is obtained by putting the blocks needed together with the gate-related blocks preceding and after the actual tests. For example, the following program may be constructed.



The choice of gate voltages is strictly the decision of the user. They may come from other tests or from other prior knowledge.

List of Outputs - The outputs from this program are the sheet resistance (or any other outputs available from the test block used). These outputs may be combined to calculate a field-effect mobility or other parameter involving different gate voltages. Of particular interest from the structure may be the reciprocity factor. This factor has been observed to deviate from the ideal as noted in the data sample section.

Less General Versions - Gate-controlled van der Pauw test blocks:

- Initial gate suitability [IGVDP0]
- Complete - unknown sample [GVDP1]
- Complete - current level specified [GVDP2]
- Standard - current level unknown [GVDP3]
- Standard - current level specified [GVDP4]
- Simplest - current level unknown [GVDP5]
- Simplest - current level specified [GVDP6]
- Post-test gate suitability [PGVDP0]

See ungated van der Pauw test blocks for explanation.

Special Equipment - Since the applied voltage cannot be increased so that a large voltage is available for measurement (because of pinch-off effects), one is faced with measuring very low voltages typically <1 mV with reasonable accuracy. This precludes automatic testing for this structure. A very high impedance, high stability, voltage sensing system is needed and this system should be capable of floating measurements. Typically 1.0-μV resolution would be needed. In addition one of the circuits shown in figure 88 may also be needed.

Samples of Data - Only very limited data have been acquired with this structure to date. Figure 89 shows the results from the gated van der Pauw structures I-48 and I-49. These structures are particularly interesting because they show examples of strong failure of reciprocity. They also clearly show the limitation of the quasi-conventional methods of characterizing SOS films.

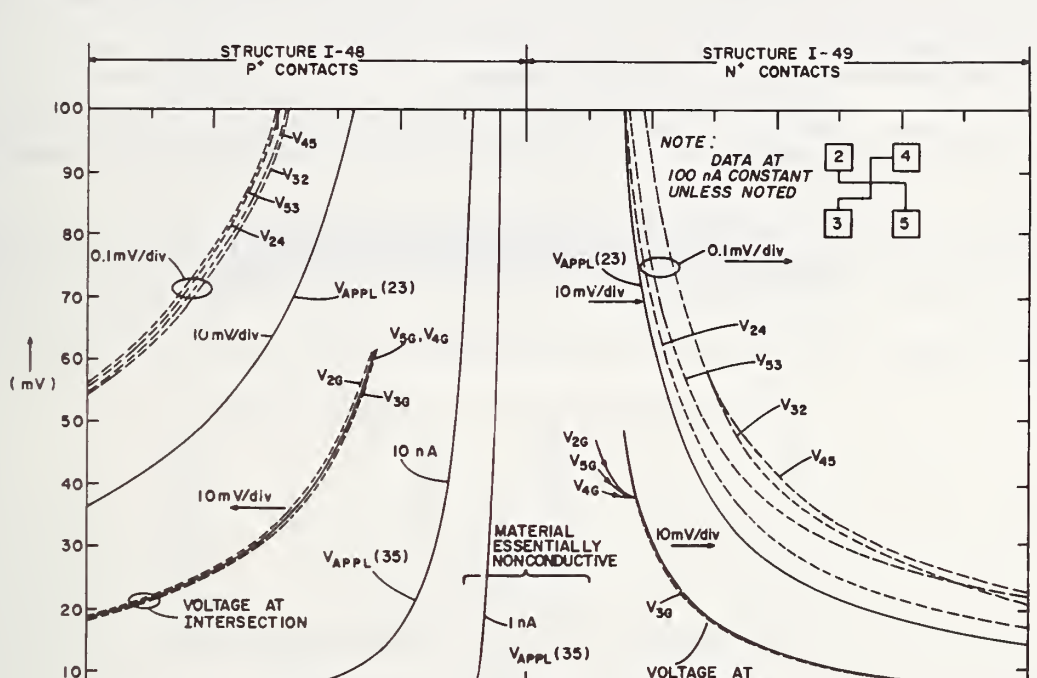


Figure 89. Performance of gated van der Pauw structures at room temperature.

These measurements are all performed under constant current conditions. Several of the voltages appearing across the arms are plotted as a function of gate voltage in figure 89. Both structures are plotted on the same graph. This is reasonable since the undoped silicon under the gate is precisely the same for both structures. In fact, these structures differ from each other only in the type of contact used. Notice that there is a region of gate voltage where neither structure yields comprehensible results. For this range of gate voltage the epi silicon is of too high a resistance to be examined by this technique. Good results are obtained only when the silicon is made conductive by the induced surface charge. The "intrinsic" properties of this epi are that it is essentially insulating. Good results are obtained, however, in the range of gate voltage where the surface is made reasonably conducting.

Three sets of curves are plotted for each device. The variation of the applied voltage as a function of gate voltage and the variation of the potential of the intersection are plotted on the same scale (10 mV/div), while the van der Pauw voltage for four different combinations of arms are plotted on the same gate voltage scale but on a 0.1-mV/div scale. For the contacts used on these structures there is only very small contact resistance. This is seen in the fact that the voltage at the intersection is accurately one-half the applied voltage at each gate voltage. The potential at the intersection does not deviate from the expected value by more than 1 mV for any combination of arms. This means that the field across the oxide at the intersection can be readily calculated from the applied voltage and the gate voltage. It also means that over distances of the order of the size of the structure (10 mil) that linearity is experienced in the resistivity of the epi.

On the other hand, serious deviations from the reciprocity demanded by linear systems are found in the van der Pauw voltage, particularly for the n+ contact structure. This can be most readily explained by assuming that the epi exhibits some anisotropy in its conductivity on a local scale (0.4 mil). Considering the highly defected structure of the silicon, this seems to be a reasonable explanation. The diagnostic power of these test structures is considerable, although the accurate testing is somewhat cumbersome, and the automatic testing of these structures requires special equipment.

Potential Pitfalls - None not previously discussed.

Overall Usefulness - The primary use for this structure is the accurate local profiling of sheet resistance, asymmetry factor, reciprocity factor, and field-effect mobility.

It is the local nature of the measurement and the fact that the current may be passed in several directions through the *same silicon* that make this structure worth considering. Higher voltages could be obtained by shortening the arms. (This could be done by modifying only the gate mask.) In general this structure does not appear to be a production type.

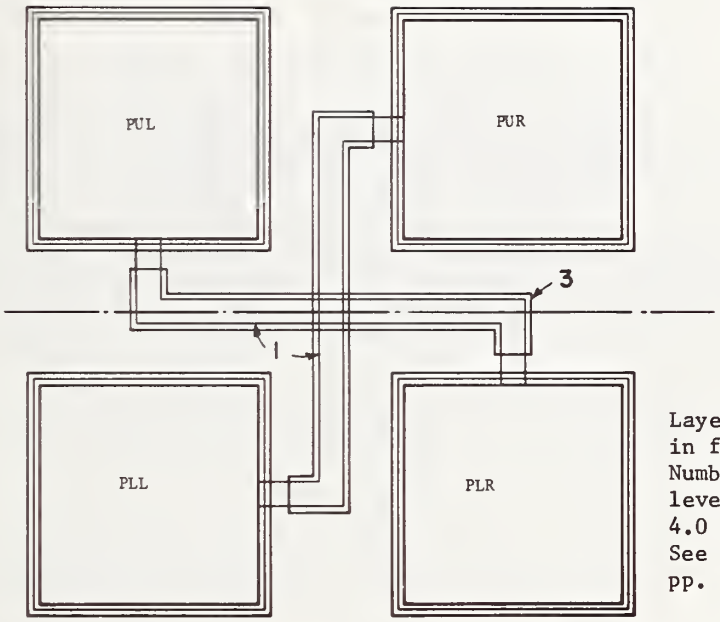
Related Structures - The most closely related structures are I-5 and I-6. Others are I-46 and I-47.

3.10 Floating-Gate van der Pauw Sheet Resistor - I-46, I-47

Purpose - The purpose of this test structure is to measure gate potential - primarily Al-gate structure.

Verbal Description - These structures are identical to those in subsection 3.9 except that the gate is not contacted; the structures are related to the devices of subsections 3.20 and 3.23 and are intended primarily for aluminum-gate processes. In the aluminum-gate processes these structures would have no gate. In order to provide undiffused silicon it is necessary to cover the epi with a gate in the silicon-gate process.

Line Drawing - The line drawing for this structure is shown in figure 90.



Layers are identified in figure 8, p. 23. Numbers refer to mask levels. Pads are 4.0 mil on a side. See section 2.1c, pp. 20-25.

Figure 90. Floating-gate van der Pauw sheet resistor, test structures I-46 and I-47, computer line drawing and cross section.

Halftone Photograph - The photomicrograph for this structure is shown in figure 91.

Electrical Access Points - These are the same as the ungated van der Pauw of subsection 3.8.

Testing Method - These structures are intended to provide some information concerning the potential of a floating poly gate under various conditions. The gate potential is determined by measuring the sheet resistance of the structure using methods indicated in subsections 3.8 and 3.9 and then adjusting the potential of similar gate-controlled structures such that the same resistance is measured. The floating gate should be at the same potential as the controlled gate when the sheet resistances are the same.

Special Equipment - The same considerations apply to the structure as to those of subsection 3.9.

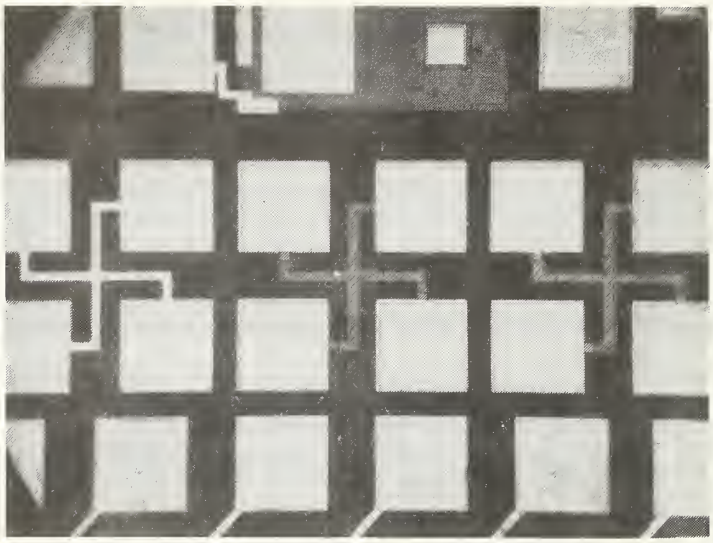


Figure 91. Photomicrograph, floating-gate van der Pauw structures I-46 and I-47.

Samples of Data - No data have been acquired from this structure.

Potential Pitfalls - One must be very careful to consider the time dependence of the floating-gate potential. The floating-gate potential must be stable during the measurement; it does not need to be stable before or after, however.

Overall Usefulness - This measurement method is primarily intended for aluminum-gate processes where a lightly doped epi is covered by an oxide which may have surface charge. However, it can be useful for determining the effects of humidity, for example, on the possible potentials of lines left floating in a circuit (by an unopened contact hole, for example). It can show how much variation can be obtained by varying the environment.

Related Structures - These structures are used in conjunction with I-48 and I-49 and are related to I-82, I-84, I-86, I-87, I-91, I-93, I-95, and I-96.

3.11 Ungated Bridge Resistors - I-54, I-55, I-57, I-59, I-61, I-63

Purpose - Test structures I-54 and I-55 measure resistivity and Hall coefficient for Al-gate processes; test structures I-57, I-59, I-61, and I-63 measure sheet resistance of the diffused layer.

Verbal Description - These structures are similar to those of subsection 3.2 except that no gate is used and the potential arm centerlines are 6.0 mil instead of 4.0 mil. Devices I-54 and I-55 are not suitable for the silicon-gate process since the epi will be diffused. Devices I-57, I-59, I-61, and I-63 are an integral part of the devices of subsection 3.2.

Line Drawing - The line drawing for this structure is shown in figure 92.

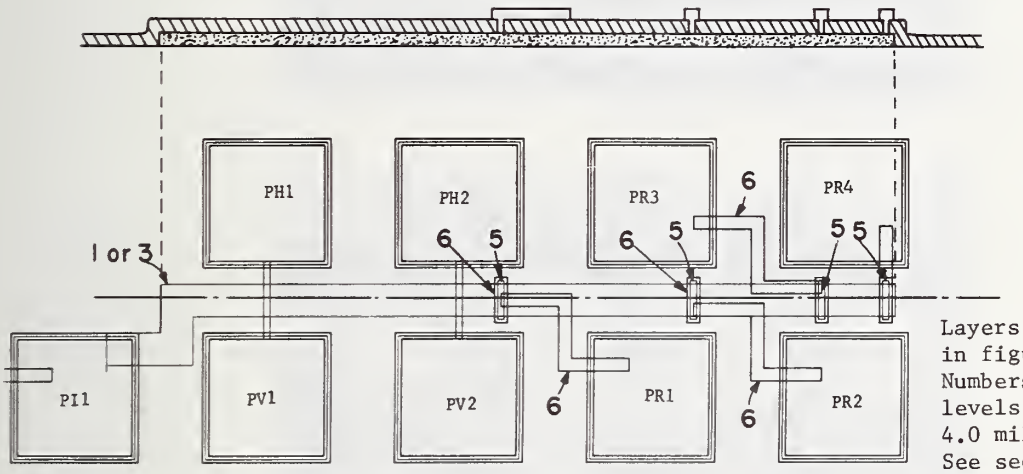


Figure 92. Ungated bridge resistors, test structures I-54, I-55, I-57, I-59, I-61, and I-63, computer line drawing and cross section.

Halftone Photograph - The photomicrograph for this structure is shown in figure 93.

Electrical Access Points - This structure has six access points in addition to those implied for isolation. These are the same as those of subsection 3.2.

- Current contact 1 — PI1
- Potential contact 1 — PV1
- Potential contact 2 — PV2
- Potential contact 3 — PH1
- Potential contact 4 — PH2
- Current contact 2 (any of) — PR1, PR2, PR3, PR4 — PI2

Testing Method - This structure is similar to the ungated van der Pauw structure in the general testing approach and comments made concerning the gate-controlled bridge resistor are also relevant. The applied voltage in this case can be much lower than in the ungated van der Pauw case. Typically applied voltages of 1.0 V are used which provide a signal level of

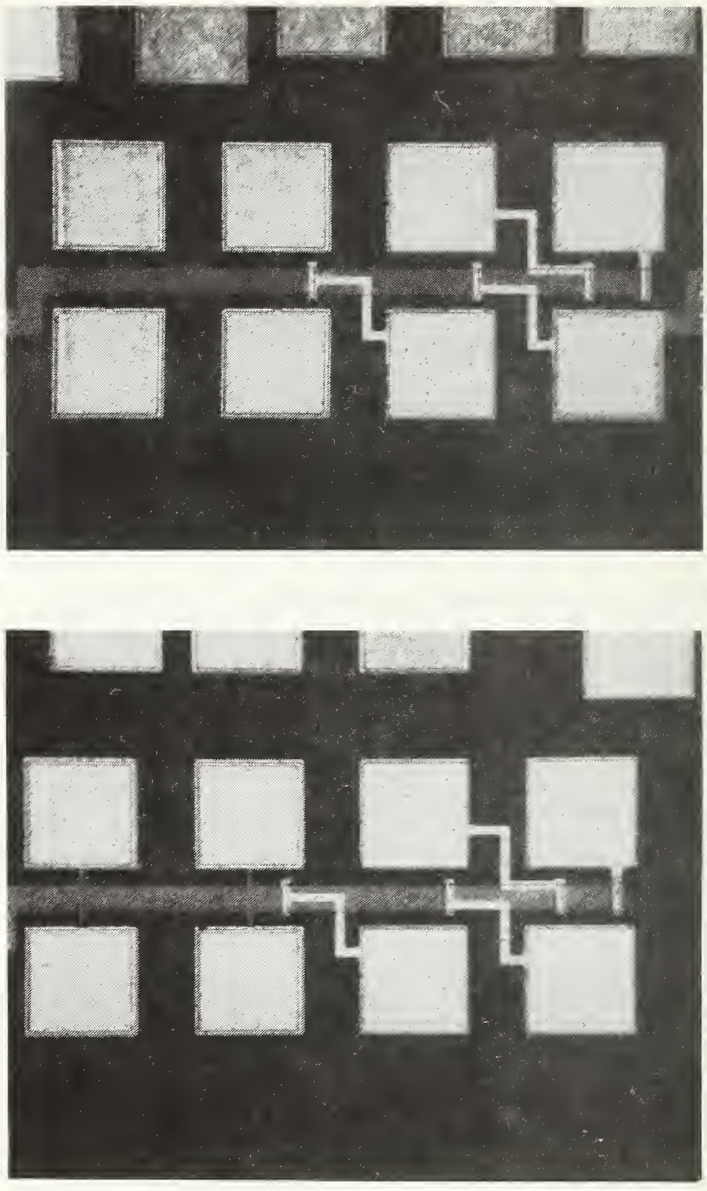


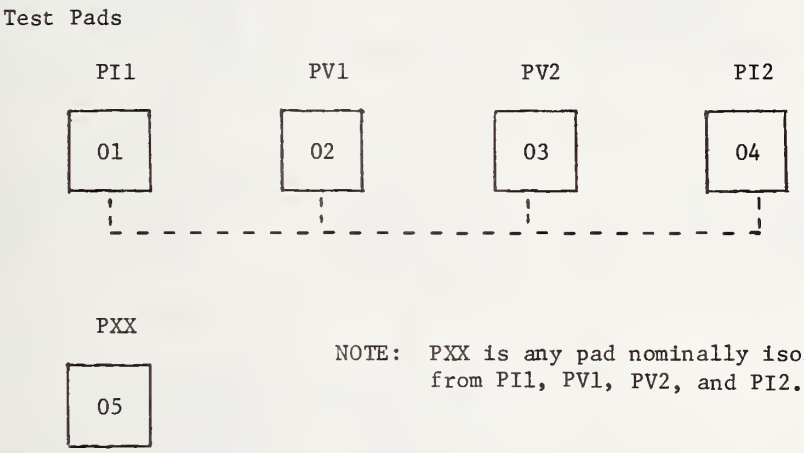
Figure 93. Photomicrograph, ungated bridge resistor and four-point contact resistance structure.

∿300 mV. Philosophically, the testing is the same as the ungated van der Pauw and the reader is referred to the flow chart for more details. Note that the asymmetry and reciprocity factors are now missing.

Initial Parameters

- Appropriate applied voltage (VAPP)
- Width to length ratio (WOVERL)
- Minimum tolerable test current (IMIN)
- Maximum tolerable test current (IMAX)
- Maximum tolerable spurious current (ISPURM)

- Maximum acceptable residual voltage with no current (VIO)
- Maximum acceptable resistance between current probes (RAMX)



Flow Chart - The flow chart is shown in figure 94.

List of Outputs - The outputs are shown in figure 95.

Less General Versions

- complete - unknown sample [BRRES1]
- Complete - current level specified [BRRES2]
- Standard - unknown current [BRRES3]
- Standard - current level specified [BRRES4]
- Simplest - current unknown [BRRES5]
- Simplest - current level specified [BRRES6]

Complete: spurious current
linearity
OI-OV
bilaterality
average sheet resistance

Standard: spurious current
OI-OV
average sheet resistance

Simplest: average sheet resistance

Special Equipment - A floating voltage sensing system is again desirable.

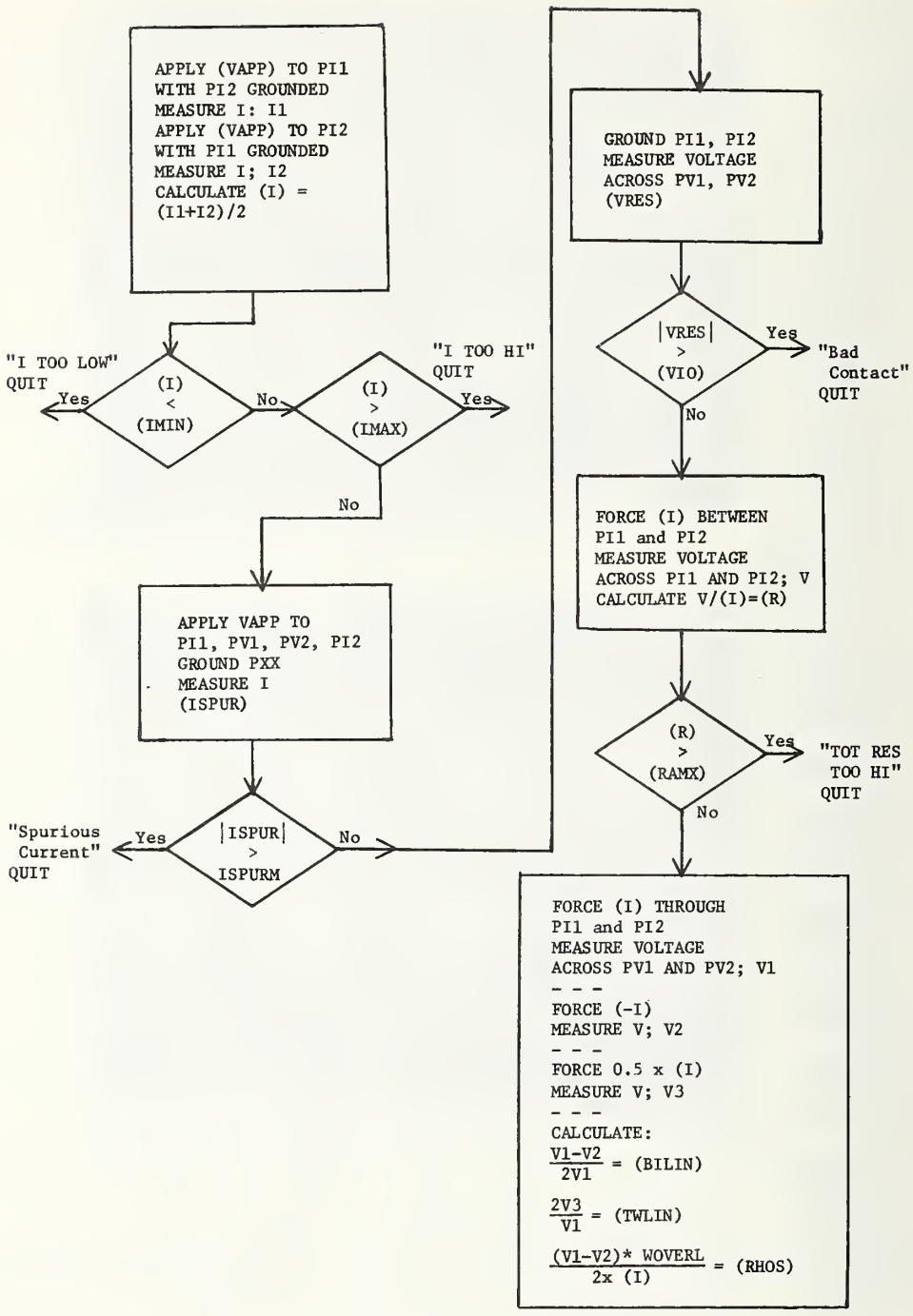


Figure 94. Flow chart for BRRES1.

Samples of Data - A typical data set from a diffused poly sample is:

Current	1 μA	10 μA	100 mA	1 mA
Applied Voltage	1.697 mV	16.84 mV	168.2 mV	1.681 V
Measured Voltage	0.590	5.570	55.34	0.5533

ρ_S = 92.2 ohm/square

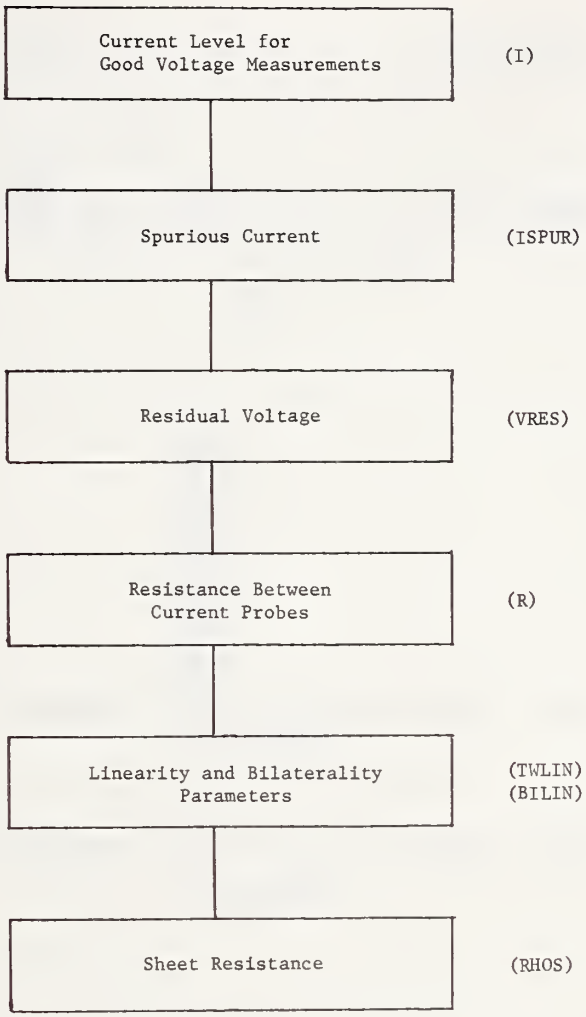


Figure 95. Outputs for BRRES1.

These data suggest that currents of at least 100 μA be used in order to eliminate low voltage measurement errors. Data from structure I-57 were automatically acquired with this program using an applied voltage of 1.0 V. Typically the residual voltage was <0.2 mV with zero applied voltage. Histograms of the data are shown in figure 96(a). Figure 96(b) is a plot of the total sample resistance ~800 ohm and shows the bilateral parameter BILIN. Note that BILIN is quantized; this is due to the resolution of the analog-digital (a-d) converter, not to the sample. Note also that the worst-case BILIN is 0.3%. The linearity parameter [Fig. 96(c)] was also nearly equal to 1. Using 1.003± for all samples, the standard deviation of this parameter was 0.0000. This parameter was so close to being the same for all the devices that this histogram program did not produce a plot. These slight deviations from ideality were caused by the a-d converter not being exactly trimmed to zero. Finally, the sheet resistance is shown in figure 96(d). A three-dimensional plot of these data showed that it was smoothly distributed across the wafer.

This test program was also used extensively in part of an internally funded program for measuring the uniformity of ion-implanted resistors on bulk silicon with superb results. Many defective structures were found which would probably have been tested as good if the "intelligent" test programs were not used.

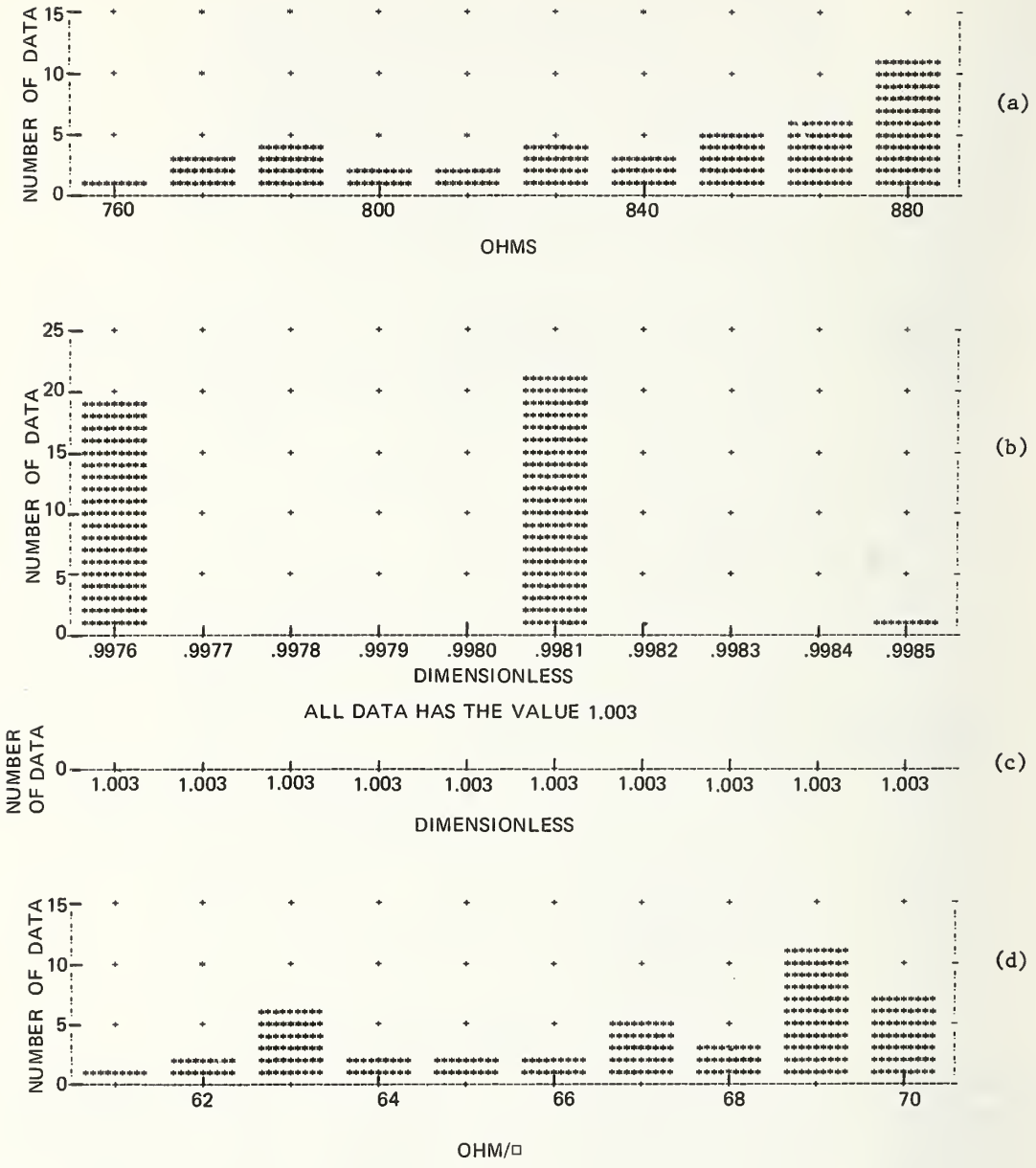


Figure 96. Histograms of data from BRRES1
(a) R in ohm, (b) BILN in ohm
(c) TWLIN, and (d) RHOS in ohm/□.

Potential Pitfalls - It is easy to forget the sensitivity of these structures to the width of the body. Also, one must be sure to apply only reverse bias to junction-isolated structures on bulk silicon. In this case, the test calling for (-I) in figure 94 is done by reversing the current terminals, not by reversing the current polarity.

Overall Usefulness - These structures provide exact data on the resistance of 1.0-mil (designed) conductors which are 6.0 mil long. This translates to sheet resistance when the body width is known. These devices are generally inferior to the van der Pauw device if there are no signal level problems and there are no appreciable local nonuniformities in the actual sheet resistance. The bridge resistors provide an average resistance over a much larger volume than the van der Pauw. The larger signal levels obtained with this structure and

the relative ease of interpreting the results from these structures make them useful enough to continue using. They are also useful in conjunction with making "quick and dirty" contact resistance measurements as discussed in the next section.

Other Related Structures - Related structures are I-72, I-75, I-5, I-6, V-1, V-2, and V-3.

3.12 Four-Point Contact Resistance Structure - I-56, I-58, I-60, I-62

Purpose - The purpose of this structure is to measure the effects of contacts on a diffused resistor.

Verbal Description - These structures are formed as shown in figure 97. The spacings between the center lines of the 0.2 x 1.0 mil contacts are 6.0, 4.0, and 2.0 mil, respectively. These devices are part of those described in subsection 3.11. The two contacts closest to the potential probes are at the same separation as the potential probes in subsection 3.11 and are also used to provide current contacts for the ungated bridge resistor.

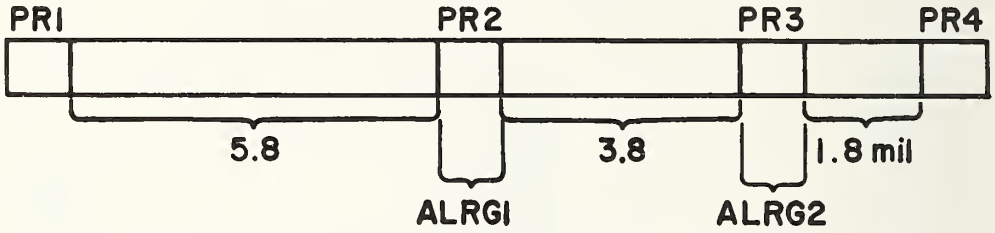


Figure 97. Four-point contact resistance structure.

Line Drawing - See subsection 3.11.

Halftone Photograph - See subsection 3.11.

Electrical Access Points - This structure has four pads in addition to those implied points needed for isolation:

- End contact near 6-mil section — PR1 (E6)
- Contact between the 6- and 4-mil section — PR2 (64)
- Contact between the 4- and 2-mil section — PR3 (42)
- End contact near 2-mil section — PR4 (2E)

Testing Method - The contact resistance is defined for the purposes here to be that portion of the resistance which cannot be accounted for by the geometrically expected resistance of the material between the contacts. If the length of the contact is L_c and the separation of the centerlines of the contacts is S, then the contact resistance per unit width is

$$2R_c = R_m - (S - L_c)R_s \qquad (17)$$

where R_s is the sheet resistance of the material between the contacts and R_m is the measured resistance. Since S and L_c are known and R_s is assumed constant, R_c can be determined by the value of R_m when $S - L_c = 0$.

If R_s is known, then only one measurement of R_m is necessary.

Typically, the metallization will be of the order of 30 mΩ/square, and the contact resistance between two probes will be several hundred milliohms. The exact value of the total resistance is quite variable and will be on the order of 1 ohm. Typical sheet resistances (R_S) are at least 20 ohm/square for the process considered here so that in the worst case of two squares (40 ohm total), the measured resistance will consist of ∿2.5% probe resistance and twice the contact resistance in addition to the silicon resistance. This amount of error is usually insignificant. Additional detail concerning the potential drop at the actual contact may be obtained by using a Kelvin probe on the probing pad or by providing a voltage tap on the metal immediately above the actual contact. The tests described for this structure measure the actual contact resistance and the probe and metal run resistance. The term "contact resistance" includes these resistances. This structure

is similar in some ways to a recently published method [19] wherein only three contacts were used.

For the process considered here the epi is ∿0.6 μm thick, and the contacts are ∿5 μm wide. This produces an aspect ratio of ~10 μm. The edge of the contact window is therefore a better reference point in this case than the centerline, and this was used in the above equation. In other words, it is assumed that the contact resistance begins at the edge of the contact. Defining contact resistance in this manner may eliminate the necessity to understand the details of the current transport near the contact. The contacts are allowed to cross entirely over the silicon bar in order to make the current flow as uniform as possible near the contact. There will be some nonuniformity near the silicon edges since the edge and the top are both contacted with metal. In the regions under the contacts, which are denoted ALRG1 and ALRG2 in figure 97, the silicon may be of much different resistivity than in other parts of the structure due to sintering or alloying processes. It is possible that this entire region is a metal-silicon alloy. If this region is much more conductive than the other silicon, the primary contact resistance will in fact be at the edge of the contact window. The sheet resistance of the alloyed regions will depend on how deep the alloying process has proceeded.

One can measure the resistance of this region by passing current between PR1 and PR3, for example. The current necessarily had to pass through ALRG1 and this potential drop can be inferred from the following equation.

$$\text{RALRG1} = R_{m_{13}} - 2R_c - (5.8 + 3.8)R_s \tag{18}$$

Similarly

$$\text{RALRG2} = R_{m_{24}} - 2R_c - (3.8 + 1.8)R_s \tag{19}$$

These two parameters should be equal.

R_c and R_s must be known for these calculations. It is readily apparent from eq. (17) that if one plots R_m versus $S-L_c$, the slope will be R_s and the R axis intercept will be $2R_c$. Since three points are available, namely,

$$\begin{aligned} S_1 - L_c &= 5.8; \quad R_{m_1} \\ S_2 - L_c &= 3.8; \quad R_{m_2} \\ S_3 - L_c &= 1.8; \quad R_{m_3} \end{aligned} \tag{20}$$

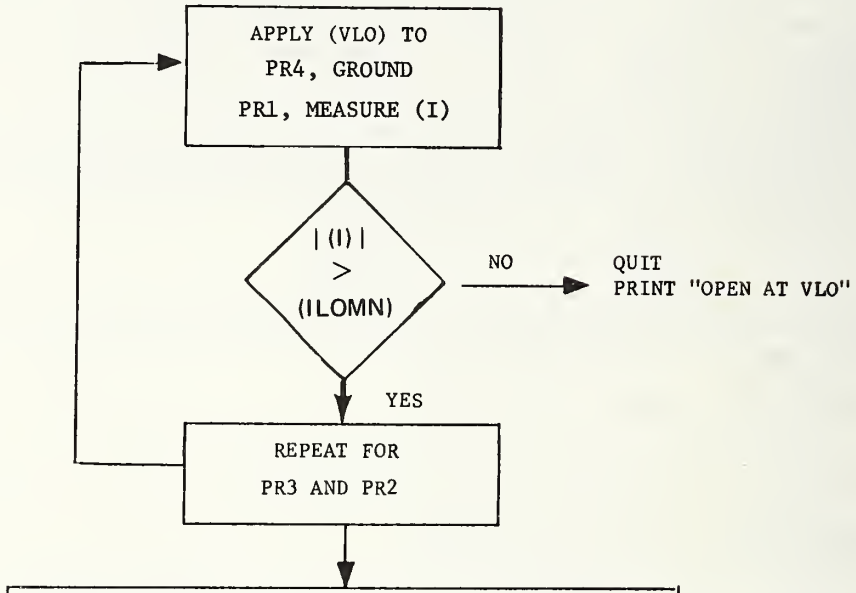
a least squares fit is used to determine the best line. The real power of using three points instead of two as in ref. 19, however, is that a self-check is available on the consistency of R_c (and/or R_s). If three points do not fall on a straight line, then either R_c (most likely) or R_s is not the same for every measurement. (It is, of course, possible that a physical defect such as partially missing silicon is the underlying cause for a nonstraight line.) The least squares analysis allows a parameter to be computed which quantifies the degree of fit. Furthermore, any systematic change in L_c will only shift the line to the right or left and will not affect the slope. R_s is therefore determined independent of the details of the contact opening geometry. R_c will be affected by changes in L_c but with the definition of contact resistance used here this is still the resistance not accounted for by the *expected* resistance between the contacts.

19. Naguib, H. M. and Hobbs, L. H., "Al/Si and Al/Poly-Si Contact Resistance in Integrated Circuits," J. Electrochem. Soc. 124, No. 4, 573-577 (1977).

Initial Parameters

- Initial low voltage (VLO)
- Minimum acceptable current at (VLO): (ILOMN)
- Voltage for resistance measurement (VI)

Flow Chart - The flow chart is shown in figure 98.



APPLY (VI)	GROUND	MEASURE I	CALCULATE R
PR4	PR1		(R14TOT)
PR3	PR1		(R131OSQ)
PR2	PR1		(R126SQ)
PR4	PR2		(R246SQ)
PR3	PR2		(R234SQ)
PR4	PR3		(R342SQ)

CALCULATE:

Sheet Resistance	(RSCONTR)
Contact Resistance	(CONTRES)
Linearity Coefficient	(FQUALRC)
Sheet Resistance of Alloyed Region 1	(RSALRG1)
Sheet Resistance of Alloyed Region 2	(RSALRG2)

Figure 98. Flow chart for CONTRES1.

List of Outputs - The outputs are given by the parameters in the last two boxes of the flow chart.

Less General Versions

Complete: CONTRES1

Single Measurement: CONTRES2

Only one less general version currently exists. In this version the sheet resistance is measured from the bridge structure (or elsewhere) and is used as an independent input to Eq. (17). Only one resistance measurement is then required to calculate R_c.

Special Equipment - No special equipment is needed.

Samples of Data - Data from structure I-60 (p^- poly) is plotted in figure 99. It is clearly seen that a good straight line exists, and that the contact resistance from two contacts is 13 ohm. The sheet resistance from the slope of the line is 94.5 ohm/square assuming a nominal 1.0-mil bar width. The resistances of the alloyed regions were found to be

RALRG1 = 11.2 Ω or 56 ohm/square

RALRG2 = 10.3 Ω or 51.5 ohm/square

This agreement is quite good since the difference between relatively large numbers is involved. We note that the resistance of the alloyed regions is less than that of the "bulk" but not as much as one might suspect. This reduction is caused in part by the shunting effect of the metal and is not well understood at present.

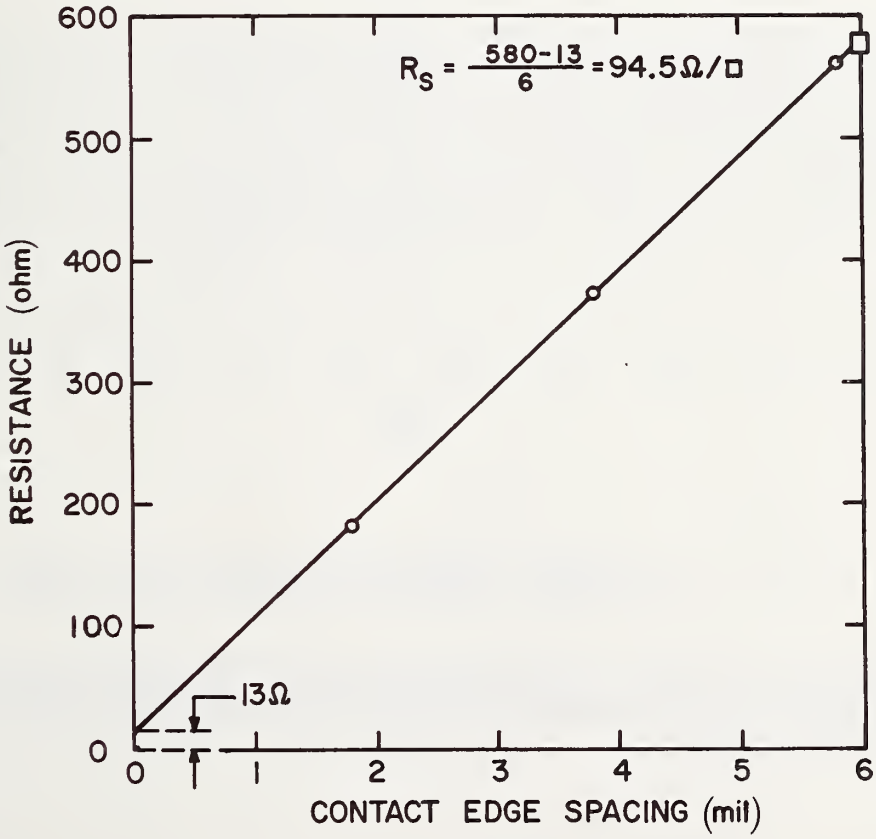


Figure 99. Contact resistance measurement from structure I-60 (p^- poly).

Data collected automatically are shown in figure 100. Plots (a) and (b) are from the same wafer and are plotted on the same scale. Plots (c) and (d) are from a different wafer and are plotted on a scale ten times less sensitive. The limits are 0 to 100 ohm for (a) and (b) and 0 to 1000 ohm for (c) and (d). Plots (a) and (c) are from structure I-56 (n+ epi) while (b) and (d) are from structure I-58 (p+ epi). We note vast differences between the plots. The p+ samples are clearly much less resistive than the n+ samples. The differences between wafers is even more striking. Examination of the linearity parameter showed that the second wafer was not producing straight lines as required for the method. Examination of the n+ epi sheet resistance data from other structures on the second wafer showed that it was not erratic but that it was higher than that of the first wafer. The individual contact resistances were therefore very erratic, and this showed clearly on the linearity parameter. It was not thought before these data were acquired that this was a particularly important test for MOS structures. It is now apparent that first-order effects are present on some wafers with regard to contact resistance.

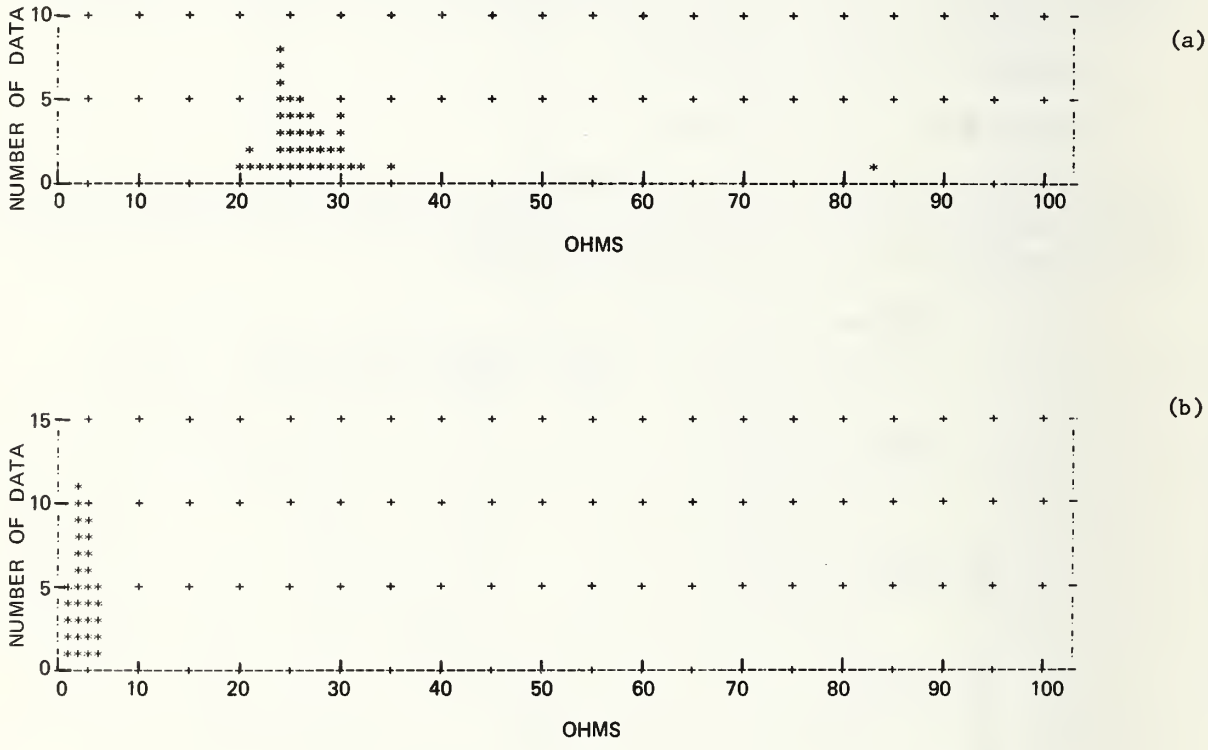


Figure 100.1. (a) Contact resistance for structure I-56 (n+ epi).
(b) Contact resistance for structure I-58 (p+ epi).

Potential Pitfalls - In this structure again the sheet resistance depends linearly on the actual width of the body. If one uses sheet resistances from structures other than that of the bridge resistor on the same silicon bar, there may be a considerable error in the measured contact resistance.

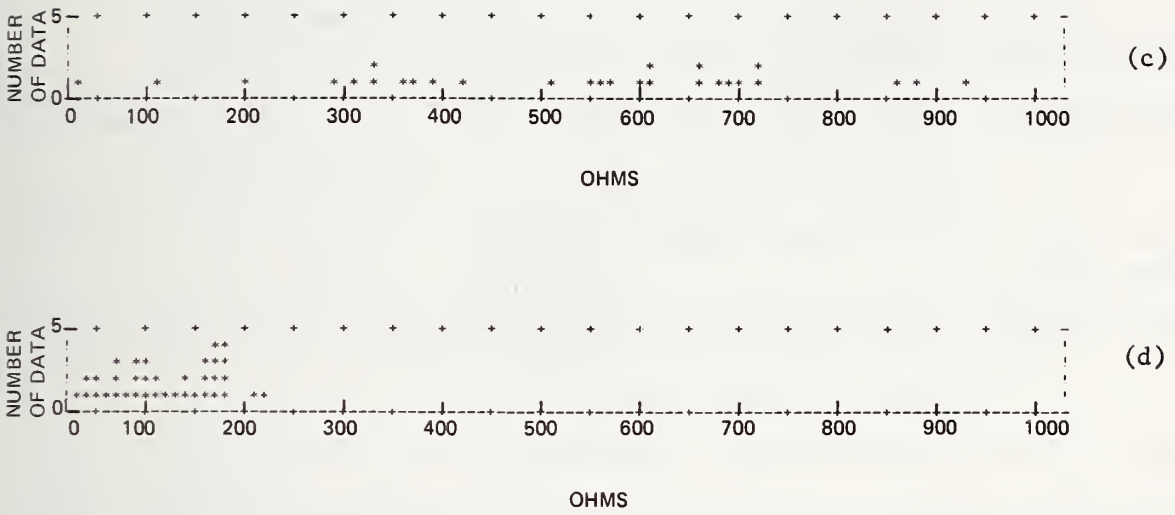


Figure 100.2. (Continued). (c) Contact resistance for structure I-56 (n^+ epi) on a different wafer from (a).
(d) Contact resistance for structure I-58 (p^+ epi) on a different wafer from (b).

Overall Usefulness - This structure is very useful for measuring accurately (5%) contact resistance above ∿10 ohm. (It is always useful for detecting serious contact resistance problems.) When the contact becomes comparable to the probe resistance, serious errors are introduced by the probes. If space and the number of probes allow, additional pads contacting the metal over the contact hole should be used to provide a Kelvin type measurement. When straight lines are obtained of measured resistance vs ($S-L_c$), this structure is at least as good as the bridge structure for measuring sheet resistance. When the lines are not straight, one knows something is wrong (unlike the three-point method). For the application used here, no changes are suggested.

Other Related Structures - Related structures are I-78, II-14, III-15, III-16, III-17, IV-5, IV-6, IV-7, IV-8, and IV-9.

3.13 MOS Transistors - I-70, I-73

Purpose - This test structure measures parameters derivable from the MOS transistor, such as field-effect mobility, threshold voltage, and drain breakdown voltage.

Verbal Description - These devices are ordinary MOS transistors with a channel geometry of 0.3 x 2.0 mil. They are an integral part of those described in subsections 3.14 and 3.15.

3.13A MOS Transistors; Stability Test - I-76, I-77

Purpose - These test structures are identical to I-70 and I-73 and are biased differently during testing.

Verbal Description - These transistors have a gate which is common to the transistor of subsection 3.13; there are five additional transistors which are identical to that of 3.13.

3.14 MOS Transistors; Channel Contact Test - I-71, I-74

Purpose - This test structure measures resistance without the channel region.

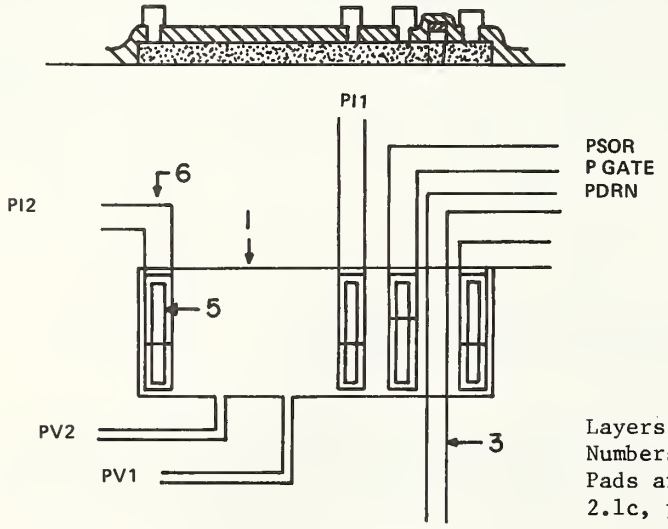
Verbal Description - This structure is formed by effectively removing the channel region from the MOS transistor of subsection 3.13. The contact holes are 0.2 x 1.6 mil on 2.0-mil-wide epi. The edge-to-edge distance for the contact is 0.6 mil. This structure is part of the same epi as the MOS transistor of subsection 3.13.

3.15 MOS Transistor; Diffusion Test - I-72, I-75

Purpose - This test structure measures the contribution of diffused silicon to the transistor voltage drop.

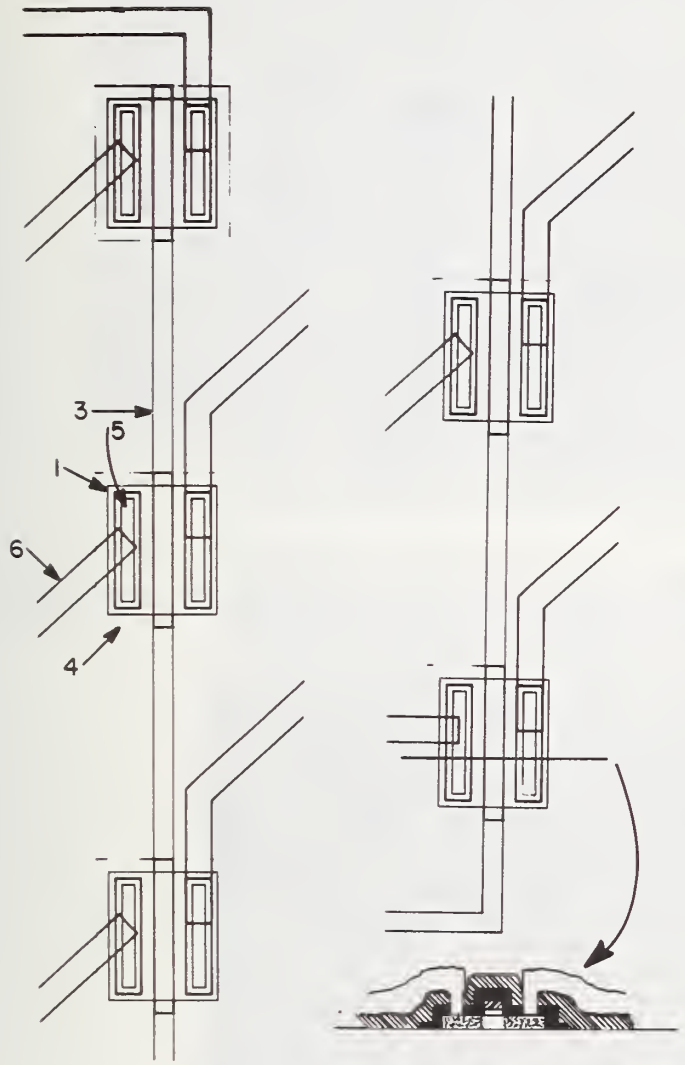
Verbal Description - This structure is an integral part of those of subsections 3.13 and 3.14 and is closely related to those of subsection 3.11. The device is 3.0 mil long with 0.2-mil potential probes whose centerlines are spaced 1.0 mil apart.

Line Drawing - The line drawing for structures I-70 through I-75 is shown in figure 101; the line drawing for I-76, I-77 is shown in figure 102.



Layers are identified in figure 8, p. 23.
Numbers refer to mask levels.
Pads are 4.0 mil on a side. See section 2.1c, pp. 20-25.

Figure 101. MOS transistor, test structures I-70 - I-75, computer line drawing and cross section.



Layers are identified in figure 8, p. 23.
Numbers refer to mask levels.
Pads are 4.0 mil on a side.
See section 2.1c, pp. 20-25.

Figure 102. MOS transistor for life-radiation test, test structures I-76, I-77, computer line drawing and cross section.

Halftone Photograph - The photomicrograph for structures I-70 through I-75 is shown in figure 103; the photomicrographs for I-76, I-77 are shown in figures 104 and 105.

Electrical Access Points - The composite structure has seven access points for I-70 through I-75; I-76, I-77 has 11 additional pads. Structure I-76, I-77 is used with structure I-70, I-73.

Transistor Drain	PDRN	I-70 through I-75
Gate	PGATE	
Transistor Source	PSOR	
Current Contact 1	PI1	
Potential Contact 1	PV1	
Potential Contact 2	PV2	
Current Contact 2	PI2	

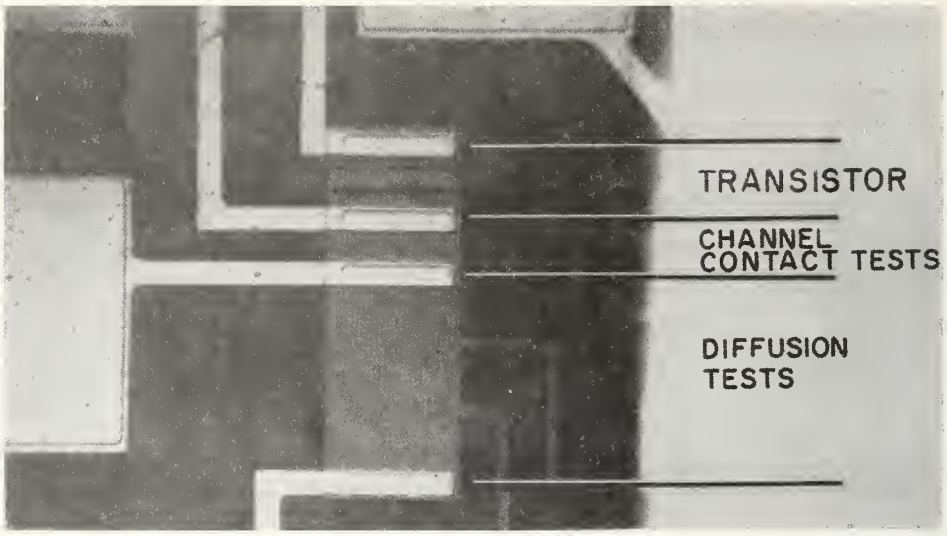


Figure 103. Composite MOS transistor (I-70 - I-75) test structure, photomicrograph.

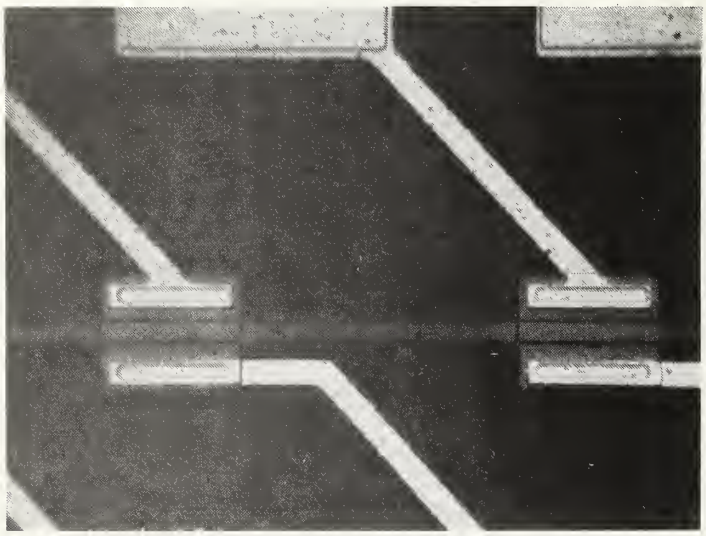


Figure 104. Individual transistors, test structures I-76, I-77, photomicrograph.

Transistor Sources	PSOR2-6	I-76, I-77
Transistor Drains	PDRN2-6	

Testing Method - Structures described in subsection 3.13 and 3.13A are used together for stability tests under different stress polarities. There are six different combinations of gate-drain polarities which may produce different results after bias-temperature or ionizing radiation stress testing. These conditions with the source grounded are:

GATE	Drain
POS	GND
NEG	GND
GND	POS

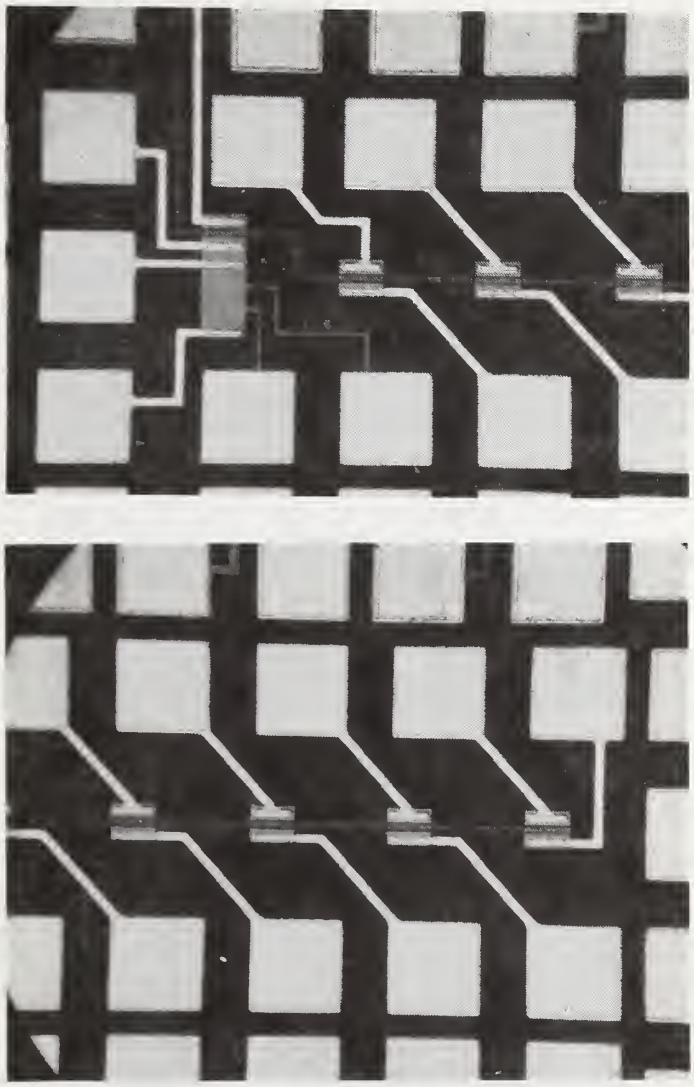


Figure 105. Both ends of the test transistor string, test structures I-76, I-77, photomicrograph.

GND	NEG
POS	NEG
NEG	POS

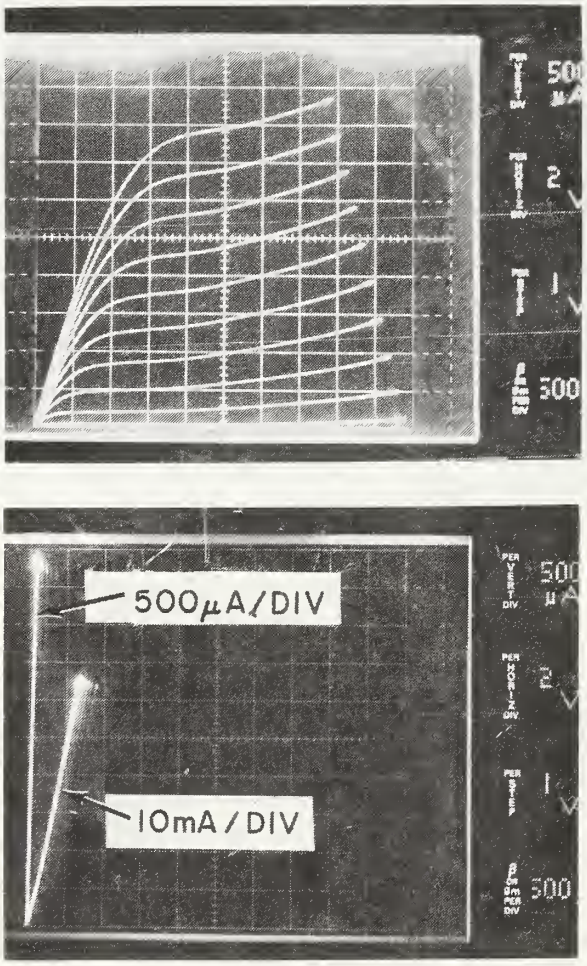
Since these devices are symmetrical, gate = POS, drain = POS is equivalent to gate = GND, drain = NEG, and gate = NEG, drain = NEG is equivalent to gate = GND, drain = POS. Normally this testing requires simultaneous contacting of all pads involved (13 total), and this may be done using a probe card and a "hot chuck" or may be done by packaging the structure and bonding the pads. In any case it is important that all devices be stressed at the same time so that differences due to multiple heat cycling, etc. are not present in the results. This provides an excellent method for separating the fundamental causes of the parametric changes observed. The parameters may be measured by the methods outlined in subsection 3.1.

Structures I-70 through I-75 are also used together for measuring properties of transistors as discussed in subsection 3.1 and particularly for determining the effect of the contacts and diffusions on the observed properties of the transistor. Structure I-71,

I-74 allows current to be passed through the same contact as the transistor and shows very clearly and quickly how much effect the electrical connections to the channel region are having. If a problem exists with the connection to the channel region, further separation into the properties of the diffusion can be done on structures I-72 or I-75. I-72 and I-75 are purposely made small so that one can examine material as close to the actual transistor as possible. Extreme accuracy is not required for the type of information needed for this application. For automatic testing structure I-71, I-74 is tested as a two-terminal resistor, and structure I-72, I-75 is tested as an ungated bridge resistor.

Special Equipment - None except as required for the individual structures.

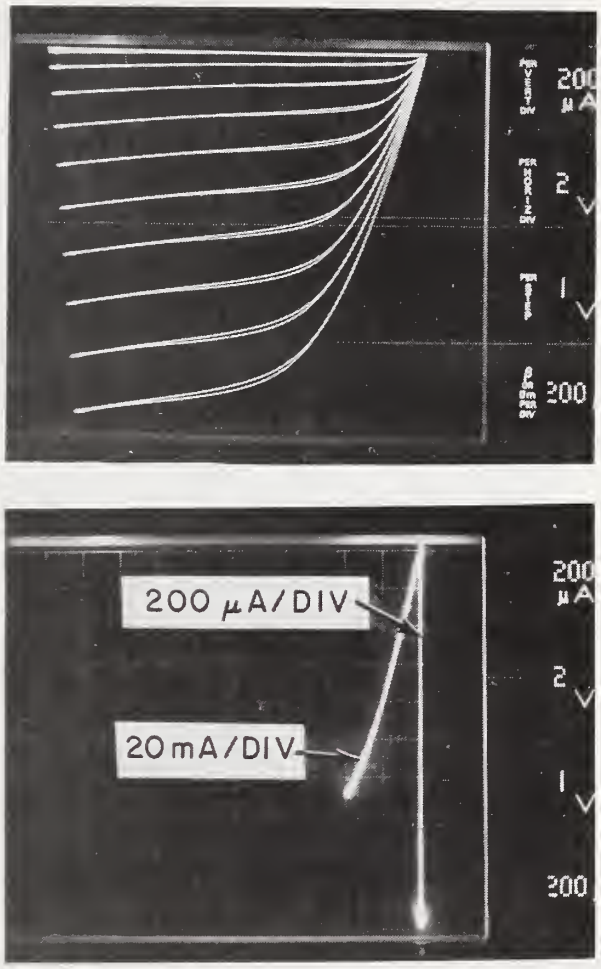
Data Sample - Some results were given in subsection 3.1 for the transistor tests. Structures I-76 and I-77 have not yet been tested. A typical use of structure I-71, I-74 is shown in figure 106. Here the drain characteristics of n-channel transistor (I-70) are shown at 500 μA/div, 2 V/div, and gate voltage steps of 1.0 V. The characteristics of structure I-71 are shown below on the same scale as those of the transistor. It is seen that at the highest current (∿5 mA) only ∿400 mV are dropped across I-71. The effect is small but slightly noticeable. More importantly the amount of effect is *known*. At very high current (60-mA range), a substantial effect is found but this range of operation is not attainable with the transistor. Another example is shown in figure 107 where a p-channel transistor is used. Here we find no detectable potential drop due to the contact scheme at the transistor current level. This result is consistent with the contact resistances found previously. Contacts to n^+ layers were very much more resistive than contacts to p^+ layers.



(a)

(b)

Figure 106. (a) Drain characteristics of an n-channel transistor, (b) channel contact effects.



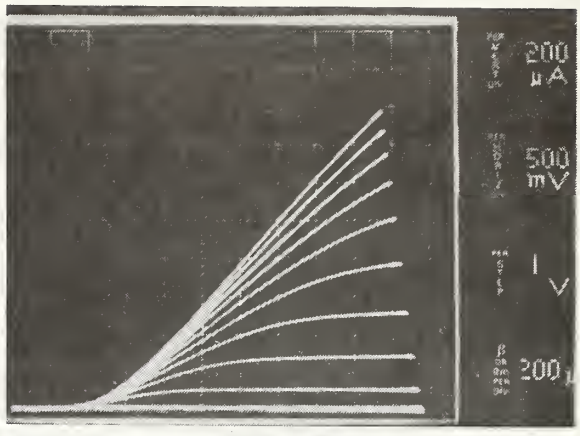
(a)

(b)

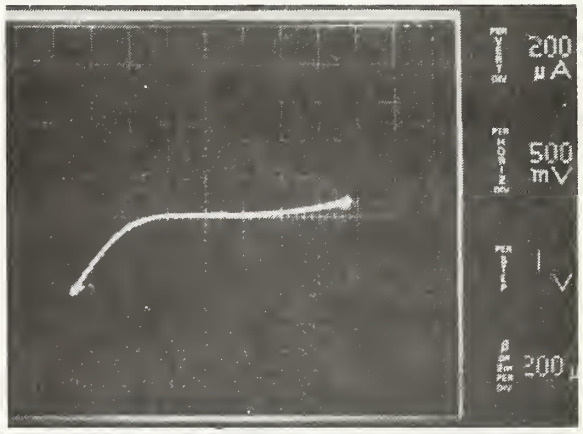
Figure 107. (a) Drain characteristics of a p-channel transistor, (b) channel contact effects.

If the effects were always this small, they would usually be insignificant. The effects are frequently found to be very important, however, as figure 108 illustrates. Although the characteristics of the transistor appear normal in gross terms, a substantial voltage offset is seen near the origin. This effort could be due to a number of causes of varying complexity (including, for example, oxide charge concentrations near the drain).

By using only the transistor, a cause cannot be unambiguously determined. Figure 108(b) shows the current voltage characteristics of structure I-71 where no channel region is involved. Current is passing through the same contact for this device as for the transistor. Note that the third quadrant of figure 108(b) appears very much the same as the beginning portion of the uppermost curve of figure 108(a). It is therefore concluded that the anomalous characteristics are not caused by the channel region. Measurement of the diffused epi resistance from structure I-72 showed that a negligible contribution from the silicon existed. One is left with only one possibility -- the contact to the diffused silicon. This contact is behaving as a poor diode, possibly because of improper metal annealing procedures (Al-rich Si (p+) and n+ diffused epi). The precise cause of the problem is not clear, but the nature and location of the effect is unambiguous. We note that the transistor curves are crudely normal, and a simple-minded automatic test would probably find "reasonable" results from the transistor. The protection used in the transistor tests recommended here, particularly the extrapolated line at low drain voltages, would not have allowed this transistor to be tested.



(a)



(b)

Figure 108. (a) Drain characteristics of structure I-70 (CMOS transistor) indicating a serious deviation from the expected behavior. (b) I-V characteristics of structure I-71.

Potential Pitfalls - None noted.

Overall Usefulness - These structures seem to function precisely as intended and are very valuable for their intended purposes. No changes are suggested. It might make the bonding process easier if the pads of structure I-76, I-77 were somewhat less crowded.

Other Related Structures - I-1, I-2, and all other MOS transistors are related to structure I-70, I-73.

3.16 Substrate Contact MOS Transistors - I-64, I-65

Purpose - The purpose of these test structures is to measure the effects of substrate potential on MOS transistors.

Verbal Description - These structures are MOS transistors with provision for electrically contacting the silicon underneath "substrate" by analogy to bulk silicon devices. The nominal channel dimensions are 0.3 x 1.0 mil. The substrate is contacted on both sides of the channel for optimum contact. These structures are primarily useful for double epitaxial processes.

3.17 Grounded Substrate MOS Transistors - I-66, I-67, I-68, I-69

Purpose - These test structures serve the same purpose as structures I-64 and I-65, to measure the effects of substrate potential on MOS transistors.

Verbal Description - These devices are related to the devices of subsection 3.16. The source side is composed of both diffusion types. One diffusion is of the same type as the drain and the other is of the same type as the epitaxy. The channel is 0.3 x 0.6 mil. One design of this device uses a region 0.1 mil wide on each side of the source for a heavily doped region of opposite type to that of the source (case A, see figure III, structures I-66 and I-68). The other design (case B) has this oppositely doped region 0.2 mil wide in the center of the source (structures I-67 and I-69). The contacts must cross the edge in order to ensure contacts to the edge diffusion for case B. The contacts are therefore well removed from the channel region in order to avoid any possible problem with etching along the epi island edge during contact opening.

Line Drawing - The line drawing for structures I-64 and I-65 is figure 109; the line drawing for structures I-66 through I-69 is shown in figure 110. Figure 111 shows a perspective view of the line drawing in figure 110.

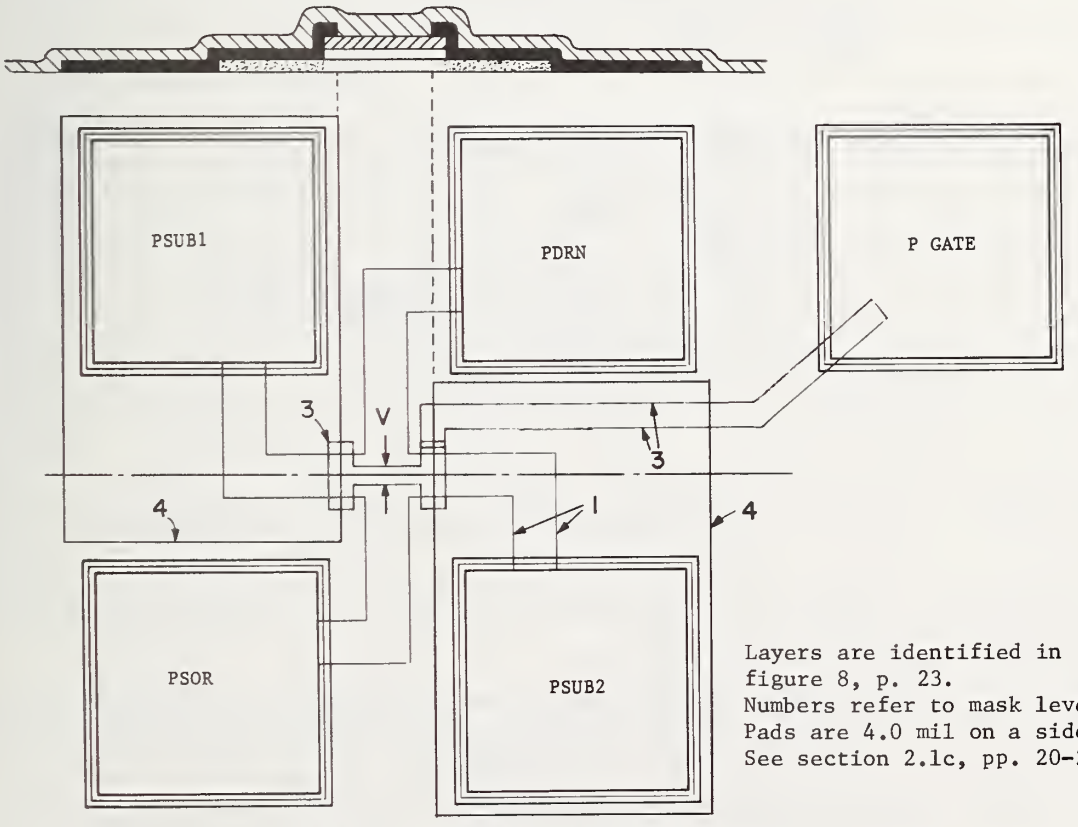
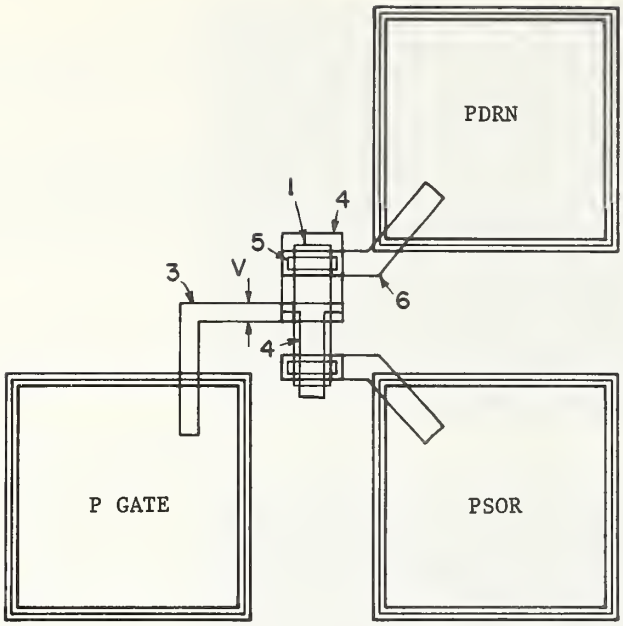
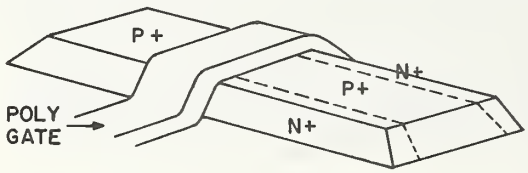


Figure 109. MOS transistor with substrate contact, test structures I-64 and I-65, computer line drawing and cross section.

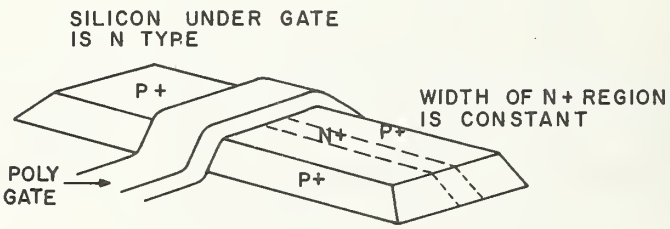


Layers are identified in figure 8, p. 23.
Numbers refer to mask levels.
Pads are 4.0 mil on a side.
See section 2.1c, pp. 20-25.

Figure 110. MOS transistor with grounded substrate, test structures I-66 through I-69, computer line drawing. The structure shown is case A (I-66).



CASE A NO SOURCE JUNCTION ON EDGE



CASE B SOURCE JUNCTION ON EDGE

Figure 111. Perspective view of figure 110. I-68 is case A; I-69 is case B.

Halftone Photograph - The photomicrographs for structures I-64, I-65 and I-66 through I-69 are figures 112 and 113, respectively.

Electrical Access Points - Both structures have the usual MOS transistor connections:

Gate	PGATE
Source	PSOR
Drain	PDRN

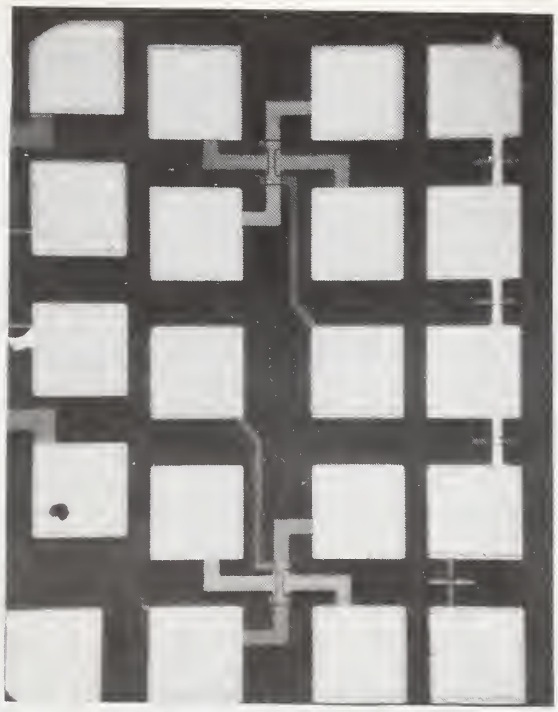


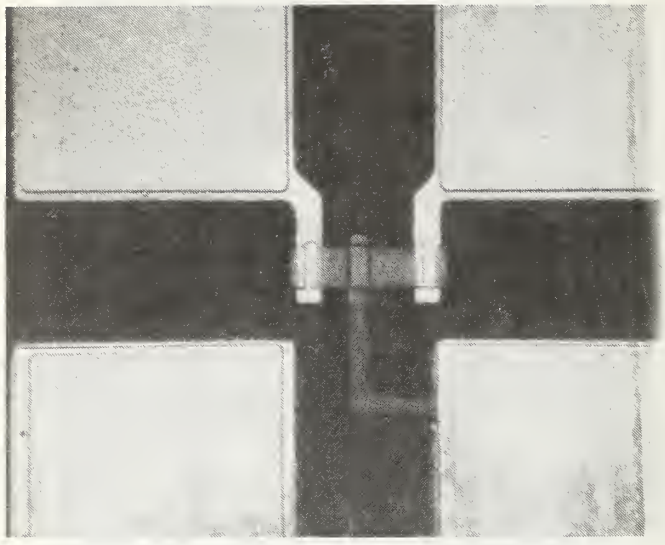
Figure 112. Photomicrograph, two substrate contact transistors, I-64, I-65.

Test structures I-64, I-65 have two additional "substrate" contacts

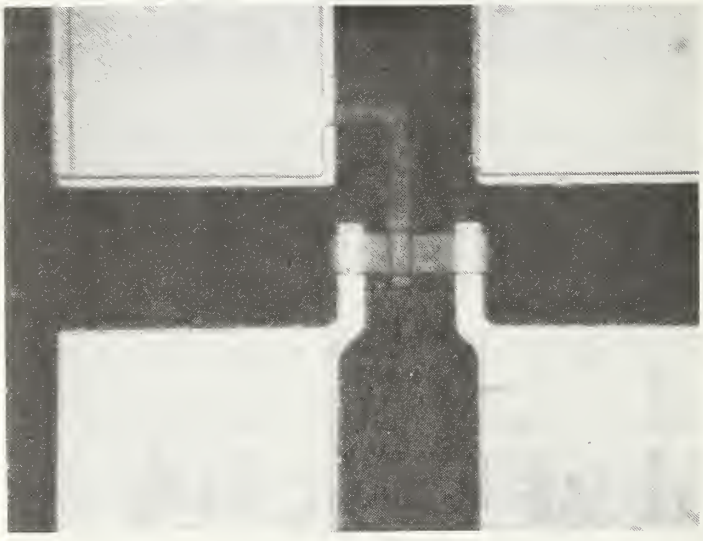
"Substrate" Contact 1	PSUB1
"Substrate" Contact 2	PSUB2

Testing Methods - These structures are provided in an attempt to make electrical contact to the silicon in the channel region which is not depleted. This silicon is called the "substrate" here by analogy to bulk silicon. Serious questions exist as to whether it is really possible to make good electrical contact to this region since the ratio of silicon thickness to lateral extent is very low (<0.1). In addition to the geometrical disadvantages, the conductivity of the undepleted silicon is very low near the sapphire due primarily to its very poor crystal structure. It is desirable to attempt contact to this region since a floating "substrate" causes instabilities in the effective threshold voltage and may be the primary cause of the "kink" (see subsection 3.1(5), p. 73). This is made by a heavily doped region of the same type as the undepleted silicon at the edge of the gate. One would expect that by varying the gate potential a change in the current between PSUB1 and PSUB2 would be found as the depletion region edge moves throughout the silicon. By grounding PSUB1 and PSUB2, one creates as nearly as possible a situation where the substrate is grounded as is usual in bulk silicon devices. One also can vary the "substrate" potential or can cause a deep-depletion effect with these terminals. The deep-depletion effect is done by biasing the substrate contact so that any minority carriers appearing at the surfaces will be removed through the contacts. This allows the gate field to penetrate deeper into the silicon since no inversion layer forms to neutralize the gate charge. This is particularly useful if thick silicon films are used.

The "substrate" grounding scheme of structures I-64, I-65 requires a great deal of space and is completely impractical as a circuit element. One can perform this grounding procedure only on the source side by forming one of the structures of type I-66 through I-69. In this case the "substrate" is grounded if the source is grounded; in any case the "substrate" is not floating. Two structures are provided. In one the "substrate" contact is on the outer edge (case A) and the source junction is not exposed to an edge and the source junction is on an edge (case B). There is currently no reason to expect that case A



(a)



(b)

Figure 113. Photomicrographs of MOS transistor with grounded substrate, test structures I-66 through I-69. (a) Case A of figure 115 and (b) case B of figure 115.

and case B should be different but both types are included in any case. One would not expect to operate this device as a symmetrical device since the substrate contact is on the source side. A certain reduction in gain is also expected since the "substrate" contact blocks minority carriers and less of the channel width is available for conduction. These structures are primarily experimental devices and are tested mainly using curve tracer or other manual methods.

Data Sample - Very little data from these structures have been acquired to date. Figure 114 shows curve tracer plots from I-67 and I-68. Both polarities are shown using a double exposure. With the normal connections reasonable curves are obtained, and the "kink" is slightly reduced. With the reverse connections it is clearly seen that the source and drain are not interchangeable. A slight hysteresis is still observed in the p-channel device.

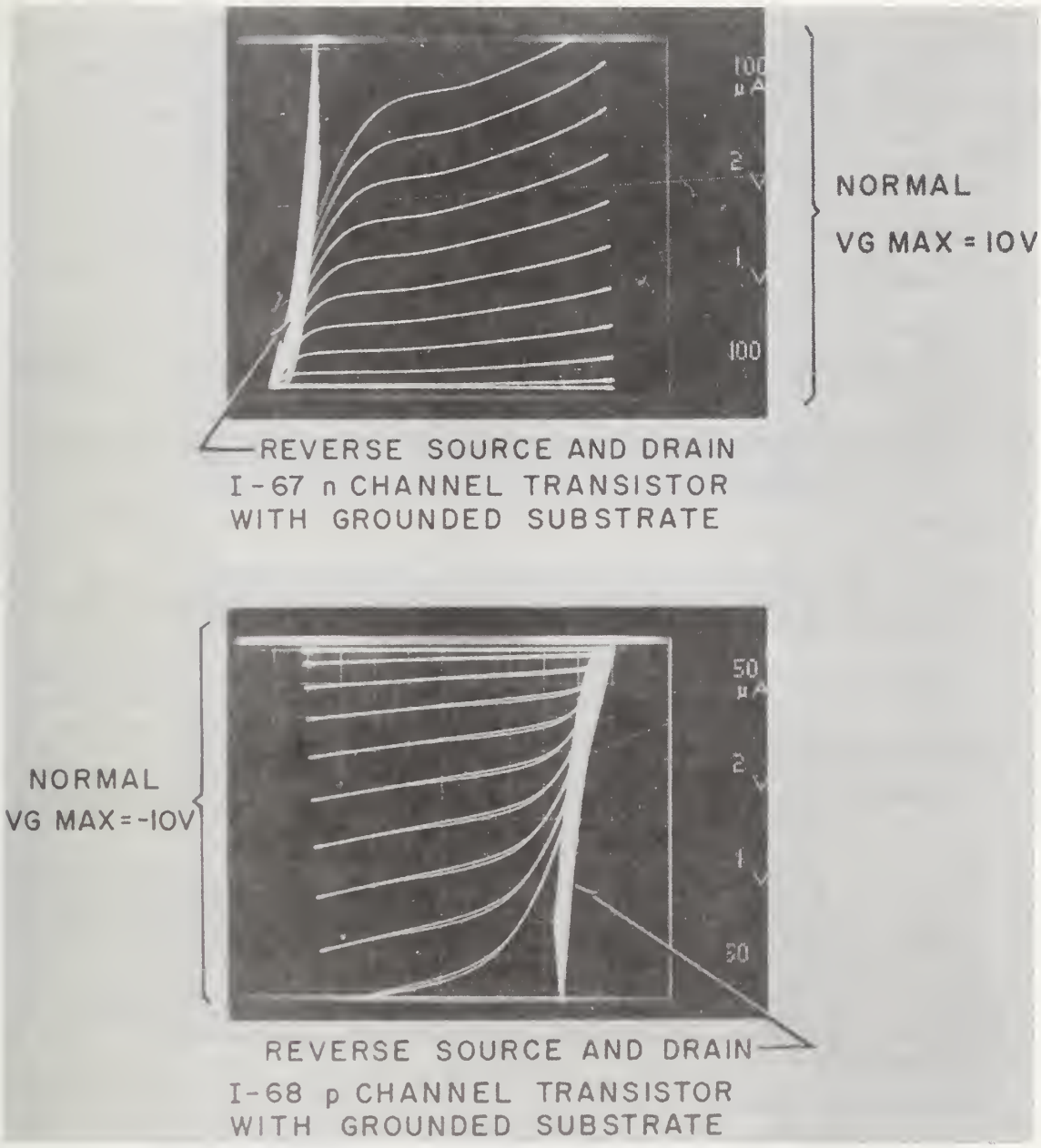


Figure 114. Drain characteristics of grounded "substrate" transistors. n Channel - 100 µA/div, p channel - 50 µA/div, both - 2 V/div, 1 V/step.

Potential Pitfalls - The major pitfall of these structures is assuming that simple-minded models can be applied to characterize the "substrate" region. The SOS "substrate" is not the same as a bulk substrate because of its thinness and extremely poor physical structure.

Overall Usefulness - These structures are valuable primarily to determine if any improvement in the drain characteristics can be obtained by varying the "substrate" bias. Structures I-66 through I-69 can be used as circuit elements if symmetry is not required (transmission gates, for example, may not use these elements).

Other Related Structures - These structures are closely related to III-13.

3.18 Continuity Test - I-78

Purpose - This test structure measures continuity through all types of connections.

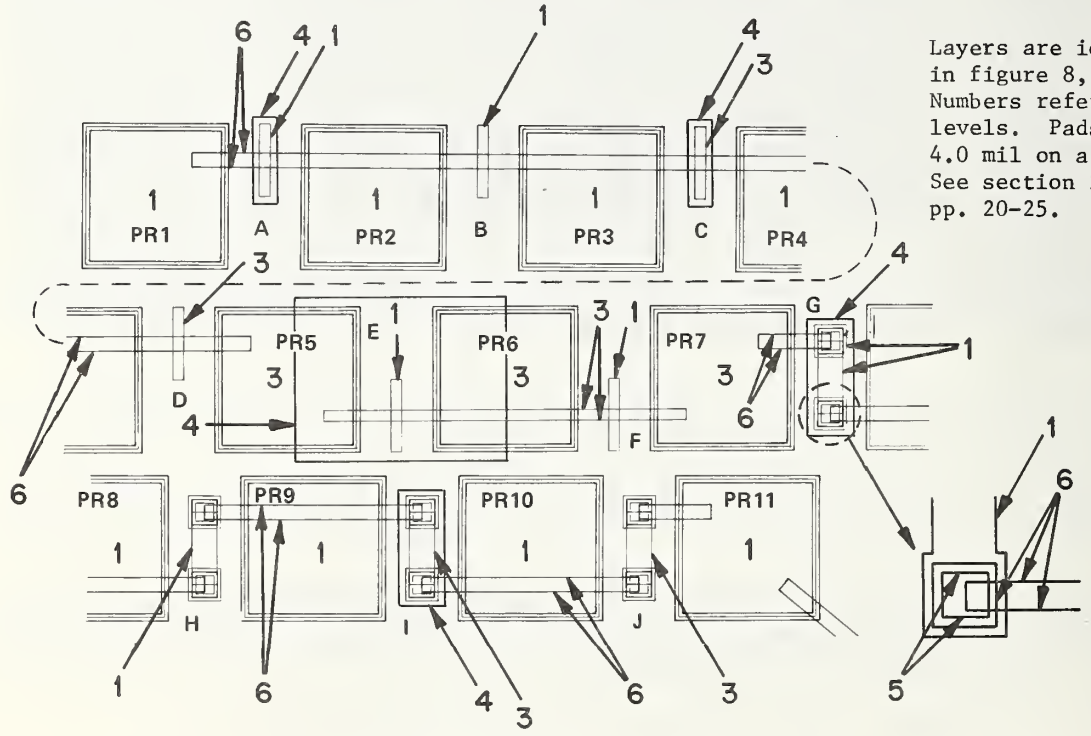
Verbal Description - In this structure every type of electrical connection used in the process is connected in series. There are ten types of these connections:

- Aluminum (0.4 mil) over n+ epi (0.3 mil)
- Aluminum over p+ epi
- Aluminum over n+ poly
- Aluminum over p+ poly
- Poly 0.3 mil over (n+ epi) (0.3 mil)
- Poly over (p+ epi)
- Contact (0.5 x 0.5 mil) to n+ epi (0.7 mil)
- Contact to p+ epi
- Contact to p+ poly
- Contact to p+ poly

The contacts are confined entirely to the top of the epi or poly to avoid possible spurious edge contact. A pad is provided for individual testing of each connection.

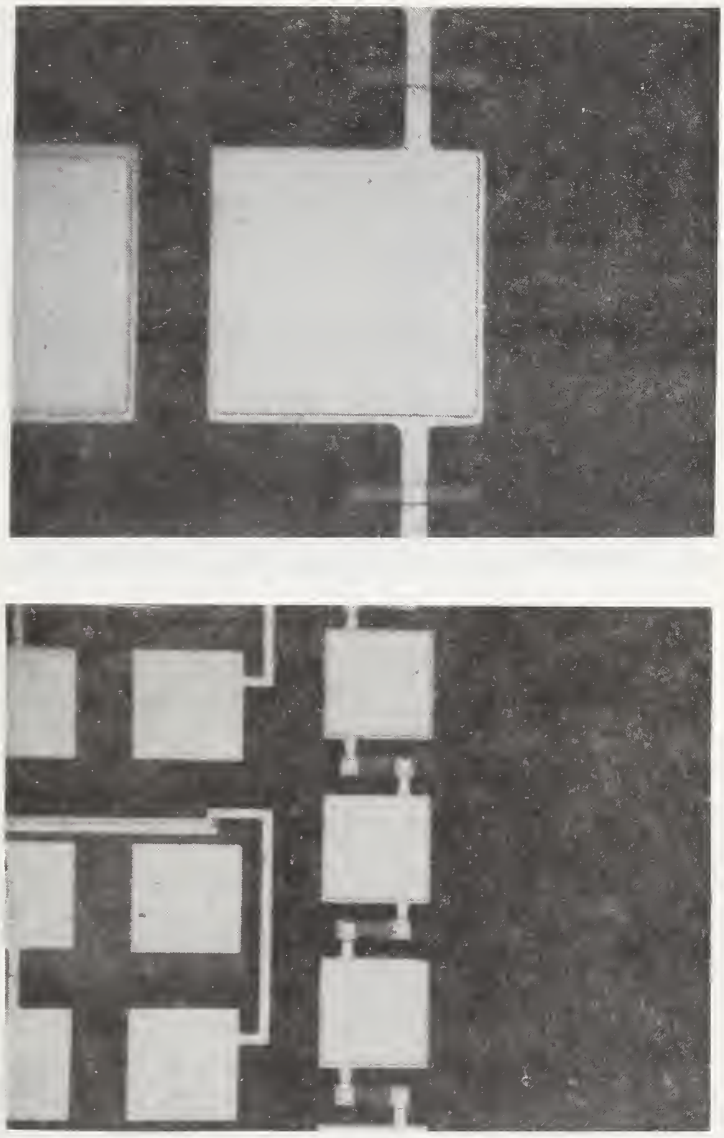
Line Drawing - The line drawing for this structure is shown in figure 115.

Halftone Photograph - The photomicrograph for this structure is shown in figure 116.



Layers are identified in figure 8, p. 23. Numbers refer to mask levels. Pads are 4.0 mil on a side. See section 2.1c, pp. 20-25.

Figure 115. Continuity test, test structure I-78, computer line drawing.



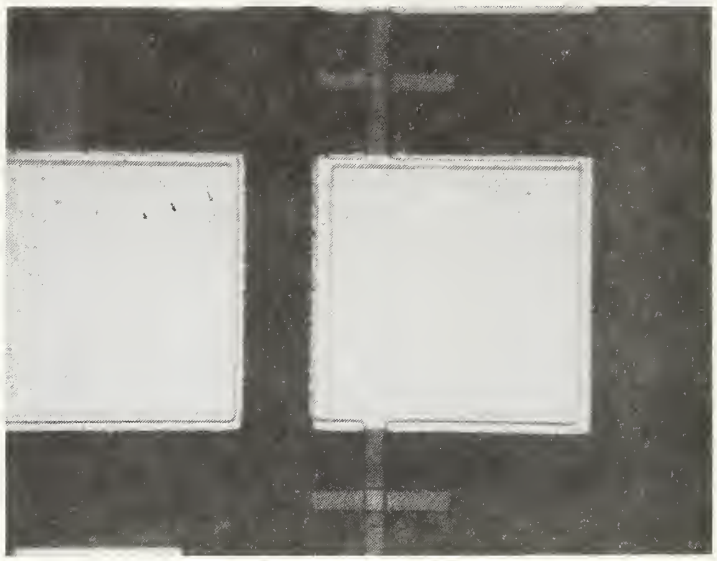
(a)

(b)

Figure 116.1. Photomicrographs, continuity test, test structure I-78. (a) Aluminum over silicon and (b) contacts to silicon.

Electrical Access Points - This structure has 11 access points.

- END-A PR1
- A-B PR2
- B-C PR3
- C-D PR4
- D-E PR5 (poly)
- E-F PR6 (poly)
- F-G PR7 (poly)



(c)

Figure 116.2. (Continued) (c) Poly over silicon.

- G-H PR8
- H-I PR9
- I-J PR10
- J-END PR11

Testing Method - This structure is tested as a two-terminal resistor as described in subsection 3.3. Any two terminals at a time may be tested. A convenient testing sequence is to first test between PR1 and PR11 to determine if any continuity problems exist. If any are found, test in sections until the problem is isolated. The problem can be found by an iterative procedure where only five tests at most are required to isolate the open connection. This may proceed according to figure 117.

Samples of Data - This structure has not been tested thoroughly; it should work very well with automatic testing. One wafer was tested manually and it was found that the contacts which were confined entirely to the top of the silicon were not completely open. This in itself was not particularly interesting until it was noted that the contacts on one of

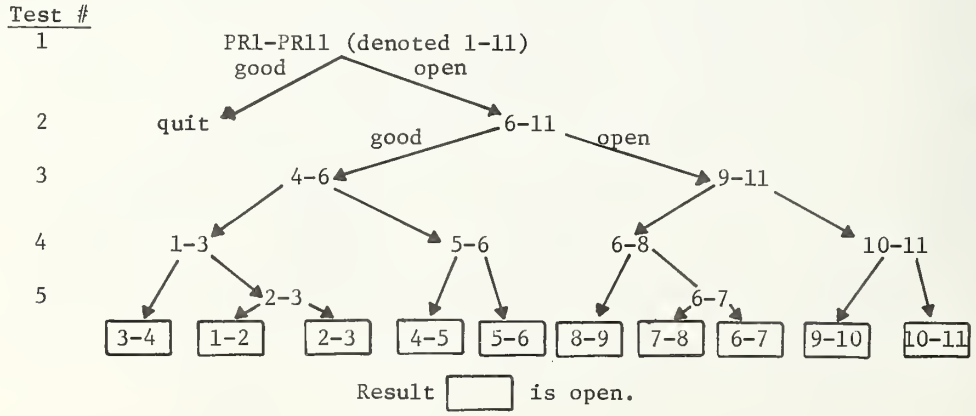


Figure 117. Procedure for detecting location of open circuit.

the structures described in subsection 3.12 (where the contact crosses a silicon edge) did conduct quite well. This structure was therefore instrumental in diagnosing where (physically) the problem existed.

Potential Pitfalls - None obvious.

Overall Usefulness - This structure is extremely useful for determining if a continuity problem exists anywhere in the process. It would have been useful to provide, in addition to the connections shown, a structure where the metal is required to cross a contact hole in order to conduct (see figure 118). If the metal is discontinuous at the edge of the contact, this structure would detect it unambiguously. This type of failure is detected in the current version as an open contact but it is not clear precisely where the open circuit is.

Other Related Structures - All contact resistance and crossover structures are related to this structure.

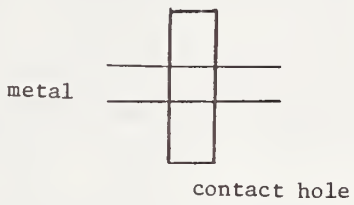


Figure 118. Suggested additional continuity test.

3.19 Gate-Controlled Diodes - I-79, I-80, I-88, I-89

Purpose - This test structure measures p-n junction properties on the simplest junction structures.

Verbal Description - These devices are related to those of structure 1 except that the junction is 1.0 mil long and is exposed to an island edge. Devices I-79 and I-80 are identical except that the junction is on the opposite side of the gate. Devices I-88 and I-89 are for double-epi type processes only. The gate in this structure is 2.0 mil long.

3.20 Floating-Gate Surface-Ion Test - I-81, I-82, I-83, I-86, I-87, I-90, I-91, I-95, I-96

Purpose - These test structures fulfill several functions. I-81 serves as a calibration structure for I-82; I-82 measures floating-gate potential. Structure I-83 measures zener breakdown voltage and leakage. Structure I-90 serves as a calibration structure for I-91, and I-91 measures floating-gate potential for the Al-gate process for double-epi processes.

Verbal Description - This structure is intended primarily for aluminum-gate processes; it is related to structures described in subsections 3.10 and 3.23. Device I-81 has its gate potential determined by an external source while device I-82 is identical except that its gate is floating. In the aluminum-gate process device I-82 has no gate.

3.21 n^+p^+ Diode; Ungated - I-92

Purpose - The purpose of this test structure is to measure zener breakdown voltage and leakage.

Verbal Description - This structure is closely related to structure I-4. The junction is 1.0 mil long and has no metallization over the junction. The junction intersects the epi island edge.

3.22 n^+p^+ Diode; Metal Gate - I-94

Purpose - This test structure measures the effect of gate potential on zener characteristics.

Verbal Description - The structure is identical to the structure described in subsection 3.21 except that an aluminum gate covers the junction.

3.23 Floating-Gate Diodes - I-93

Purpose - This test structure measures floating-gate potential for double-epi processes.

Verbal Description - These structures are designed for aluminum-gate processes where the gate does not extend all the way across the channel region. They are not particularly useful for silicon-gate processes. Devices I-84 and I-93 can be used in conjunction with devices of subsection 3.19 which are identical except that the gate potential is determined externally. Devices I-85 and I-94 are identical to devices I-80 and I-89.

Line Drawing - The line drawing for all these structures is shown in figure 119.

Halftone Photograph - The photomicrograph for these devices is shown in figure 120.

Electrical Access - This description has 11 electrical access points:

• Gate connection for all gate-controlled structures	PGATE	
• Various connections as shown in the line drawing	PN+1	PN+6
	PN+2	PP+1
	PN+3	PP+2
	PN+4	PP+3
	PN+5	PN+P+

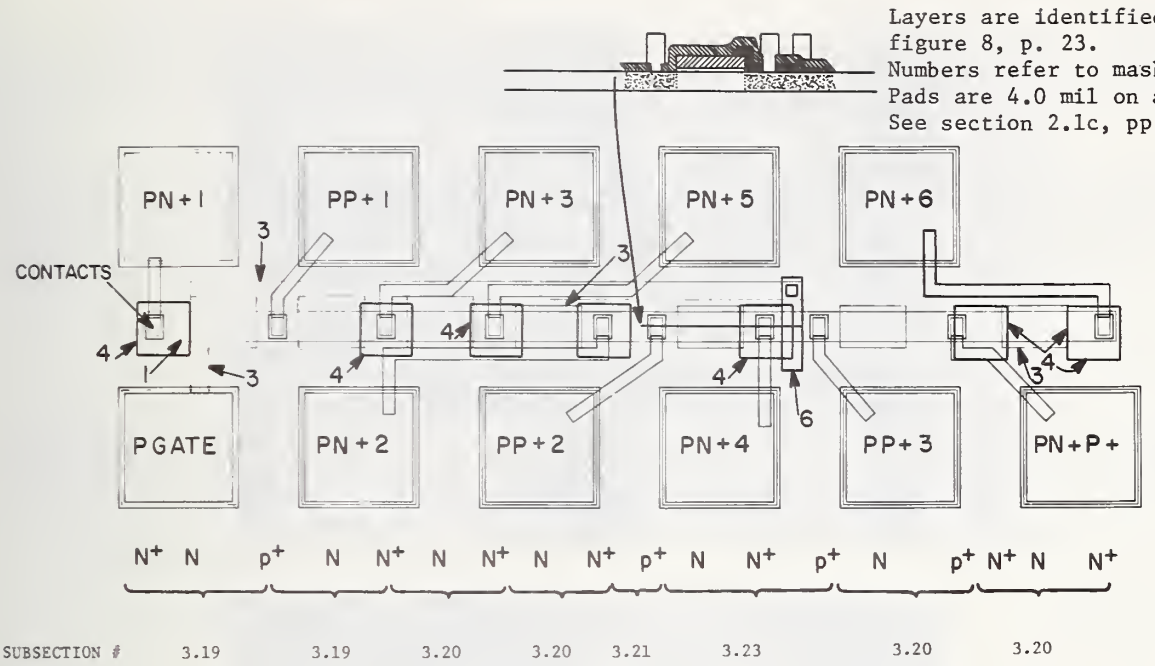
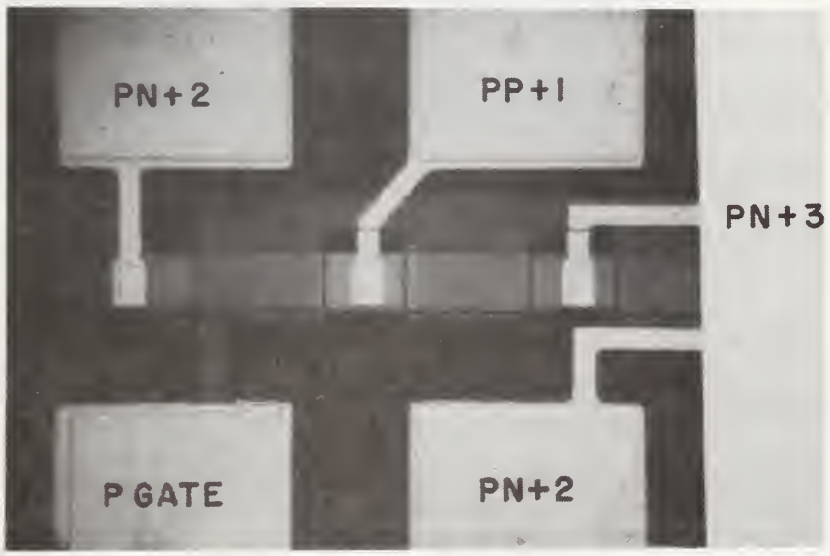


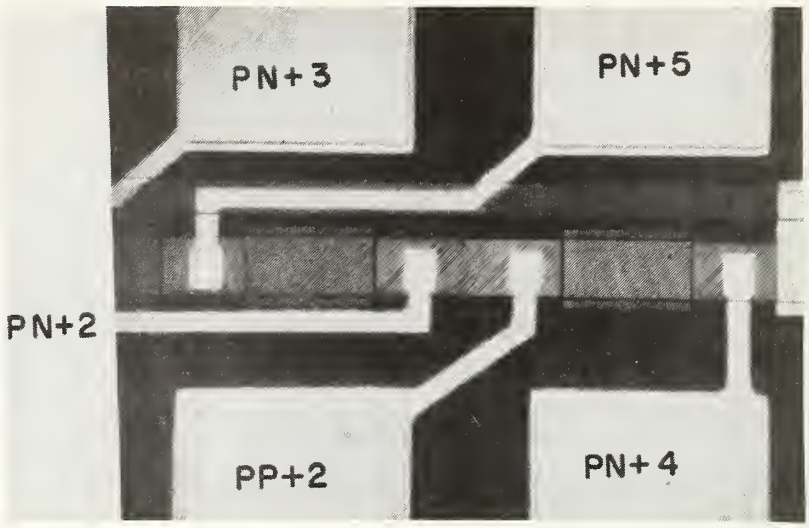
Figure 119. Gate-controlled and floating-gate diodes, test structures I-79 through I-96, computer line drawing and cross section.



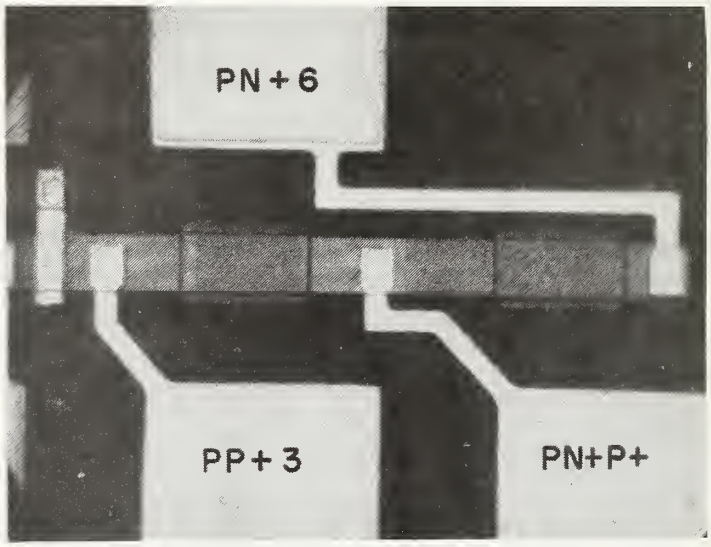
(a)

Figure 120.1. Photomicrographs of composite structure, test structures I-79 through I-96, (a) Left end.

Testing Method - Most of these devices are not of great interest and will not be discussed in detail. The floating-gate structures are used in the same way as the floating-gate van der Pauw structures described in subsection 3.10. The gate-controlled diodes differ from those on bulk silicon in that there may be very large series-resistance effects; they are otherwise similar. The only structure which will be discussed in detail is the n^+p^+ diode with no gate. This structure is sometime used for gate protection circuitry and illustrates very well some features of comprehensive process characterization, particularly the use of model-like analysis to obtain more error-free data from local slopes measured using dc techniques.



(b)



(c)

Figure 120.2. (Continued) (b) center section, and (c) right end.

These measurements are for devices commonly called "diodes" or "zeners." Their nominal characteristics are high nonbilateral and nonlinear. Since the diode itself is nonlinear and nonbilateral, it is difficult to detect a situation where the contacts to the silicon are causing difficulty. If contact difficulties exist, these are best detected on the structures designed to handle these situations. The tests used here assume at least linear contact characteristics.

There are four properties which characterize diodes in their most basic form. These are:

- Rectification ratio
- Forward resistance
- Reverse leakage
- Reverse breakdown

Each of these must be defined in terms of an applied voltage or impressed current; these voltages and currents may vary widely depending on the application of interest. Usually any measurement in the forward direction will be restricted to less than 1.0 V for silicon junctions.

One can also use the idealized diode models in the literature to extract other parameters which may apply to the test structure if it satisfies the model. Notable among these are the slope in the forward direction and the extrapolated intersection of the logarithm of the forward current to zero applied voltage. These parameters contain information regarding the internal operation of the structure. One form of the diode equation is:

$$I = I_o \left[\left[e \left(\frac{q\ V_a - IR}{nkT} \right) \right] - 1 \right] \tag{21}$$

where V_a is the measured applied voltage and I is the total current. The current is assumed to flow uniformly across the entire structure. R is a series resistance which may be in the contact pads, the contact holes, or the silicon.

This equation can also be written as:

$$V_a = \frac{nkT}{q} \ln \left(\frac{I}{I_o} + 1 \right) + IR \tag{22}$$

and

$$\frac{\partial V_a}{\partial I} = R_{forward} = \frac{nkT}{q} \left(\frac{1}{I + I_o} \right) + R \tag{23}$$

also

$$\frac{\partial \log \left(I + I_o \right)}{\partial V_a} = \frac{1}{2.303} \frac{q}{nkT} \left[1 - \frac{R}{R_{forward}} \right] \tag{24}$$

For most bulk silicon applications, R is very small as is I_o. This may not be the case for SOS diodes, particularly for R.

In the simplest case, when both I_o and R are small

$$\log I = \frac{q}{2.303\ nkT} + \log I_o \tag{25}$$

and the extrapolation of log I to $V_a = 0$ is log I_o as shown in figure 121.

$$\frac{\partial \log I}{\partial V_a} = \frac{q}{2.303\ nkT} \tag{26}$$

which defines n. If R is not negligible and I_o is small, one can determine its value from two measurements of $\partial V_a / \partial I$ and eq. (23). The extrapolation of 1/I to 0 yields R as shown in figure 122. Also the slope of $\partial V_a / \partial I$ vs 1/I yields nkT/q. Alternatively, n may be found from eq. (24).

Clearly, if I cannot be made much larger than I_o, then analysis is much more difficult. An approximate upper bound to I_o can be obtained by measuring the current under reverse-biased conditions. However, it is well known that this value differs from the extrapolated I_o. If I_o is very large, it is doubtful that the structure is suitable for detailed measurement.

Equation (24) is preferable to eq. (23) for determining n since log I vs V_a is nominally a straight line when R is small and the value of n does not depend on a *local* derivative of a nonlinear curve as in eq. (23).

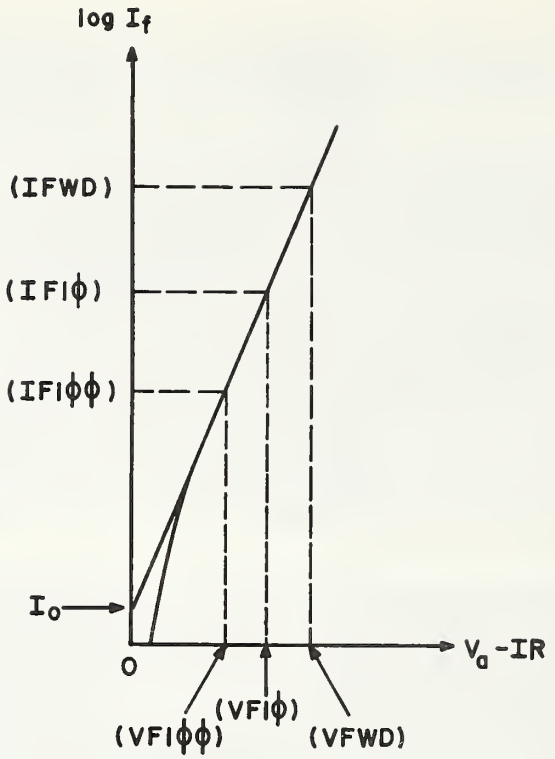


Figure 121. Log forward characteristics of an ungated diode.

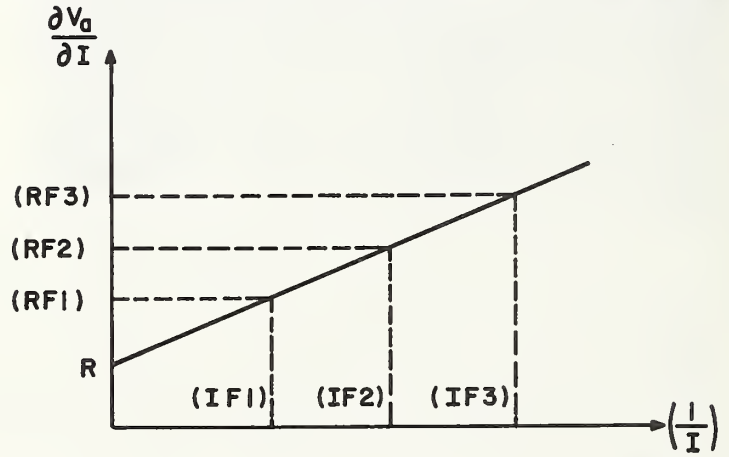


Figure 122. Extrapolation to determine series resistance.

The basic division made in the testing of SOS diodes (and other types as well) is between those devices which are likely to have large series resistance and those which are not. In general any SOS diode which has a lightly doped side will probably exhibit serious series resistance in the forward direction. Any diode of the so-called n^+p^+ type will probably not have large series resistance.

The following discussion shows how the resistances may be measured using dc techniques.

For $I >> I_o$, R small:

$$I = I_o \exp \frac{qV}{nkT} \tag{27}$$

If the current is increased by a factor of 1 + A, the resulting voltage VP is given by

$$(1 + A)\ I = I_o \exp \frac{qVP}{nkT} \tag{28}$$

from which

$$I_o = (1 + A)\ I \exp \frac{-qVP}{nkT} \tag{29}$$

Similarly VM is defined by

$$(1 - A)\ I = I_o \exp \frac{qVM}{nkT} \tag{30}$$

In general

$$\frac{dI}{dV} = \frac{q}{nkT}\ I_o \exp \frac{qV}{nkT} \tag{31}$$

Now, using the linear approximation to the slope

$$\frac{dI}{dV} = \frac{2AI}{VP - VM} = \frac{q}{nkT}\ I_o \exp \frac{qVS}{nkT} \tag{32}$$

VS is the voltage where the measured slope actually exists. This is shown graphically in figure 123. The dashed line is the actual characteristic. Substituting for I_o in the above equation

$$\frac{2AI}{VP - VM} = \frac{q\ (1 + A)}{nkT}\ I \exp \frac{q}{nkT}\ (VS - VP) \tag{33}$$

Rearranging eq. (33)

$$\frac{2nkT}{q}\left(\frac{A}{1 + A}\right)\left(\frac{1}{VP - VM}\right) = \exp \frac{q}{nkT}\ (VS - VP) \tag{34}$$

from which

$$VS = \frac{nkT}{q}\ \ln\left[\frac{2nkT}{q}\left(\frac{A}{1 + A}\right)\left(\frac{1}{VP - VM}\right)\right] + VP \tag{35}$$

This is the actual voltage from which the slope is measured. From eq. (23) with $I >> I_o$ and R small

$$dV = \frac{nkT\ dI}{qI} \tag{36}$$

and from eq. (32)

$$\frac{dI}{I} = 2A \tag{37}$$

So,

$$dV = \frac{2\ AnkT}{q} \tag{38}$$

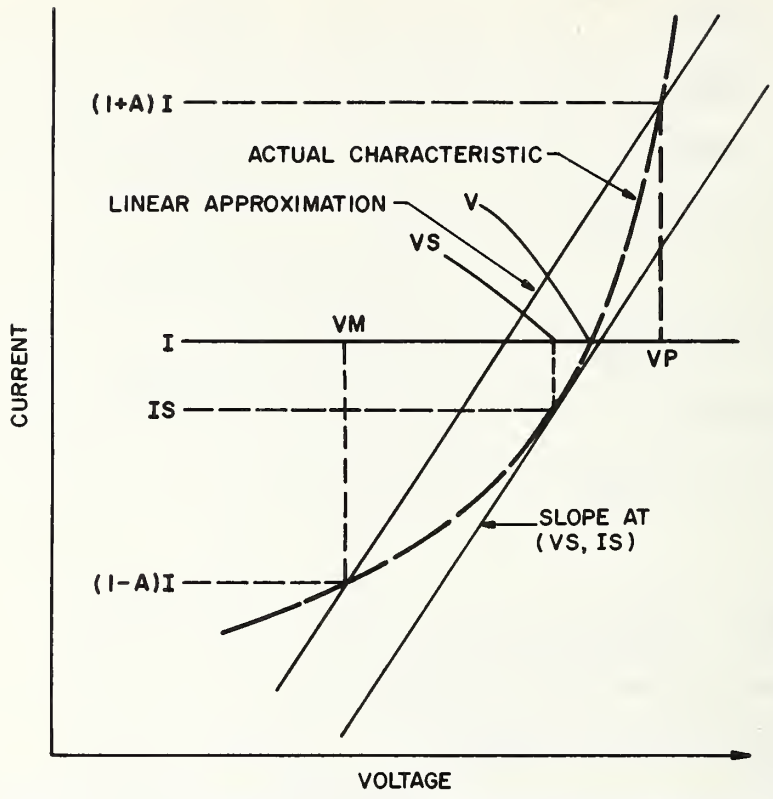


Figure 123. Measurement of local slope using dc techniques.

and

$$n = \frac{q\ dV}{2\ AkT} \tag{39}$$

The value of A necessarily depends on the value of dV that can be accurately measured by the tester. Typically, 0.1-mV resolution is the best available. For 1% accuracy dV must be >10 mV which requires $A \geq 0.2$. Figure 124 shows the dependence of dV on A and n at room temperature. Notice that dV does not depend on the size of the diode being measured. Using eq. (38) in eq. (35) we find that:

$$\boxed{VS = \frac{VP - VM}{2\ A} \ln\left(\frac{1}{1 + A}\right) + VP} \tag{40}$$

Substituting VS from eq. (40) we find:

$$IS = (1 + A)\ I \exp\left[\ln\left[\frac{1}{1 + A}\right]\right] = I \tag{41}$$

Therefore, IS = I and does not need to be computed. The simplest way to compute VS is to take the average of VP and VM. A typical example:

Suppose A = 0.100, n = 1.000

VP - VM = 5.20 mV from eq. (38) or figure 124

VP - VS = 2.48 mV from eq. (40)

In this case the difference between the actual value and average of VP and VM is 2.60 - 2.48 = 0.12 mV.

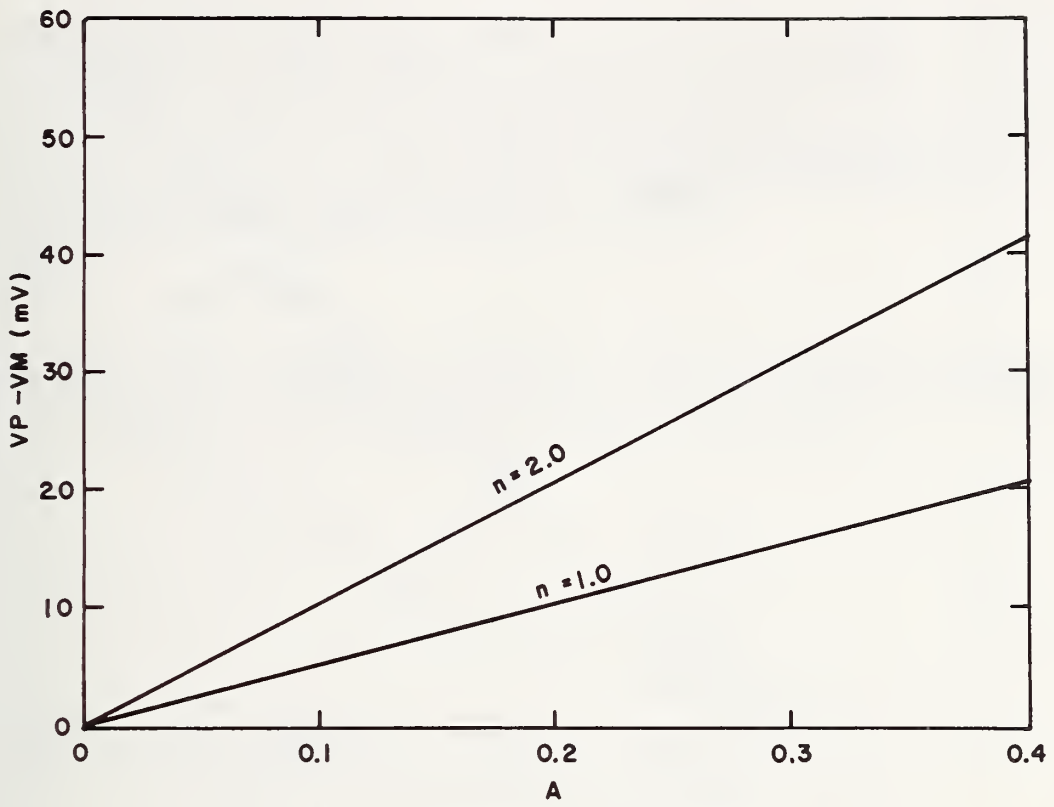


Figure 124. Dependence of dV on A and n.

In general

$$VS - VP = \frac{VP - VM}{2}\left[\frac{1}{A}\ln\frac{1}{1+A}\right] \tag{42}$$

or the error introduced by the nonlinearity of the curve is:

$$r_\varepsilon = \frac{1}{A}\ln\left(\frac{1}{1+A}\right) \tag{43}$$

We note that this error is relative to the ideal and does not represent absolute error which is much smaller. The absolute error ΔV_ε is given by:

$$\Delta V_\varepsilon = \left(\frac{VP - VM}{2}\right) - (VP - VS) \tag{44}$$

$$\Delta V_\varepsilon = \frac{VP - VM}{2} + \frac{VP - VM}{2}\left(\frac{1}{A}\ln\frac{1}{1+A}\right) \tag{45}$$

$$\Delta V_\varepsilon = \frac{nkT}{q}\left(A + \ln\frac{1}{1+A}\right) \tag{46}$$

If the tester being used has the capability to calculate VS, then no appreciable error is introduced. It is readily seen from figure 125, however, that at A = 0.2 less than 1.0-mV error results from using the linear approximation to the slope.

The automatic testing of these structures proceeds by first testing that a nominally good contact is being made. We apply 400 mV in the forward direction, and the resulting current is measured. This voltage is arbitrary but fixed in the program. This voltage should be sufficient to turn on virtually any diode safely but sufficiently to produce at least 10 nA of current. These limits could have been put into the program as input

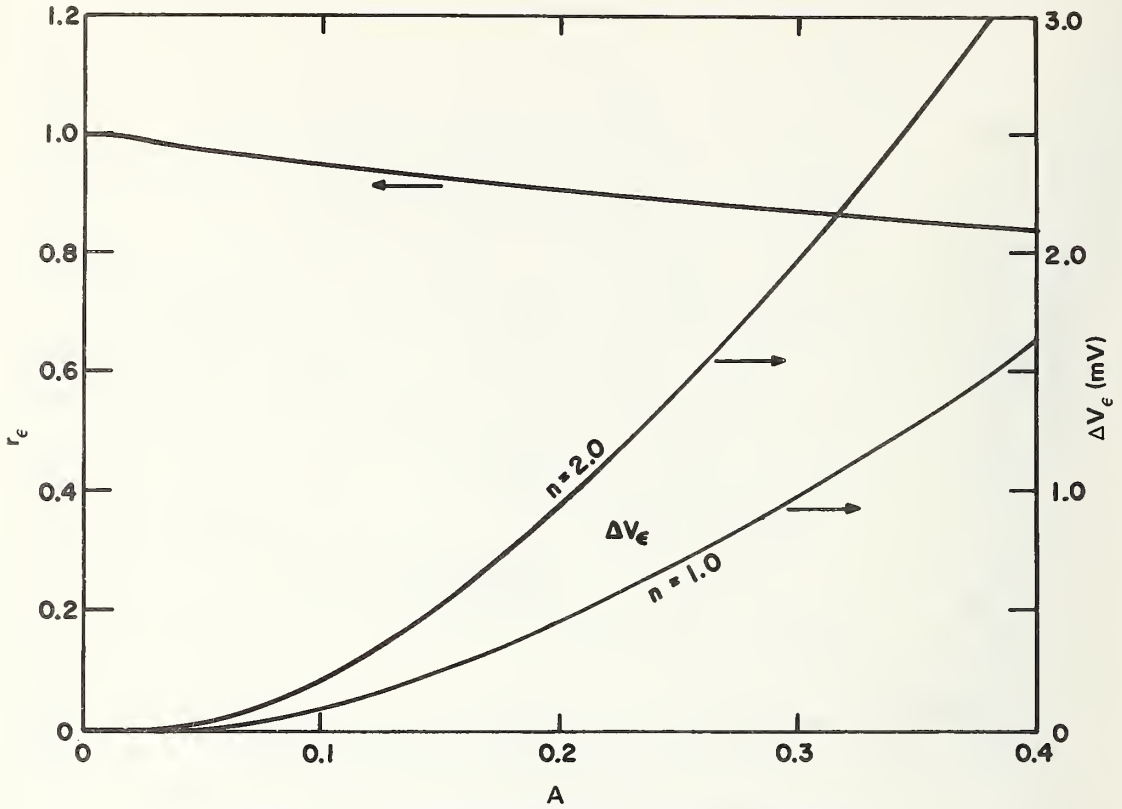


Figure 125. Dependence of ΔV_ε and r_ε on A and n.

variables but the purpose here is only to check continuity and these would not normally need to be changed. Testing proceeds by forcing a characteristic current (IFWD) through the device and measuring the resulting voltage (VFWD). If this voltage is too high, testing is halted. -(VFWD) is then applied and the current (IREV) is measured. This current is used with IFWD to calculate a rectification ratio IFWD/IREV. If the rectification ratio is not larger than a specified limit, testing is halted. This would represent a very poor reverse characteristic. A reverse current is then forced, and the resulting voltage is recorded as the reverse breakdown (VB). A voltage is also initially specified to measure the reverse leakage (VREV). If (VREV) is greater than (VB), the leakage measurement is bypassed since applying too high a reverse voltage would probably destroy the diode. If the leakage is too high, testing is halted.

The forward resistance is then measured at three current levels, namely, (IFWD), 0.5*(IFWD), and 0.25*(IFWD). This resistance is measured by the method described in the theoretical section by forcing (1 + A)*(IFWD) and (1 - A)*(IFWD) and measuring the resulting voltage. If the difference between these voltages is not between 75 and 200 times the resolution limit of the tester, A is either increased or decreased by a factor of 2 from its initial value of 0.1 until the voltage difference lies in the above range. (The resolution limit is the smallest detectable increment in measured current.) If more than three attempts to find a suitable value of A are required, this section is bypassed. When three values of forward resistance are found, a least squares fit is performed and the series resistance is calculated as shown in figure 122. A value of the injection factor (NLIN) is also found from the slope as indicated by eq. (23). Also a linearity factor (FQULN) is calculated which measures the degree of fit to the straight line.

At this point the voltages at (IFWD)/10 and (IFWD)/100 are measured. Another least squares fit is done on the log of these data to determine the injection factor and Iϕ. Again a quality factor is calculated which indicates the degree of fit to the straight line. It is possible that a shunt resistance also exists for these SOS diodes (near the bottom or on the edges, for example). If this is true, the characteristics will depart drastically from the log behavior at low forward voltages. The current will be much too high if the effect is important. A measurement (ILFM) is performed, therefore, at a low forward voltage (VFL), and the expected current from the log equation found for the device in previous

tests is also calculated. If the measured current is greater than five times the calculated current, a possibility of a shunt resistance is assumed and the test continues. A test is also made to ensure that this current level is greater than the system limit. In cases where the measurement is not going to be used again (for calculations, etc) it is not critical that this limit be used. In this case, however, the measurement will be used for a calculation and will be rejected. If not, testing is completed. If testing continues, a measurement (ILRM) is done at -(VFL). If this current agrees with the measured current at +(VFL) within a factor of two, a shunt resistance is calculated.

$$\text{RSHUNT} = \frac{2\ (\text{VFL})}{(\text{ILFM}) + (\text{ILRM})}$$

Notice that if measurements are near the system limit, (ILRM) will always have a larger average than (ILFM). This is because all potentially low values of (ILRM) will not be included in the average since they will not have been acquired when ILFM is too low. This shunt characteristic may not be very linear. This completes the testing.

Initial Parameters (UGD1)

- Forward current level (IFWD)
- Forward voltage limit (VFLIM)
- Minimum rectification ratio IF/IREV (RECMN)
- Voltage for reverse current (VREV)
- Current for reverse breakdown (IBD)
- Maximum reverse current (ILMAX)
- Minimum voltage resolution of tester (VRESOL)
- Low forward voltage for shunt resistance (VFL)

PN+	PP+
01	02

See figure 126 for initial parameters.

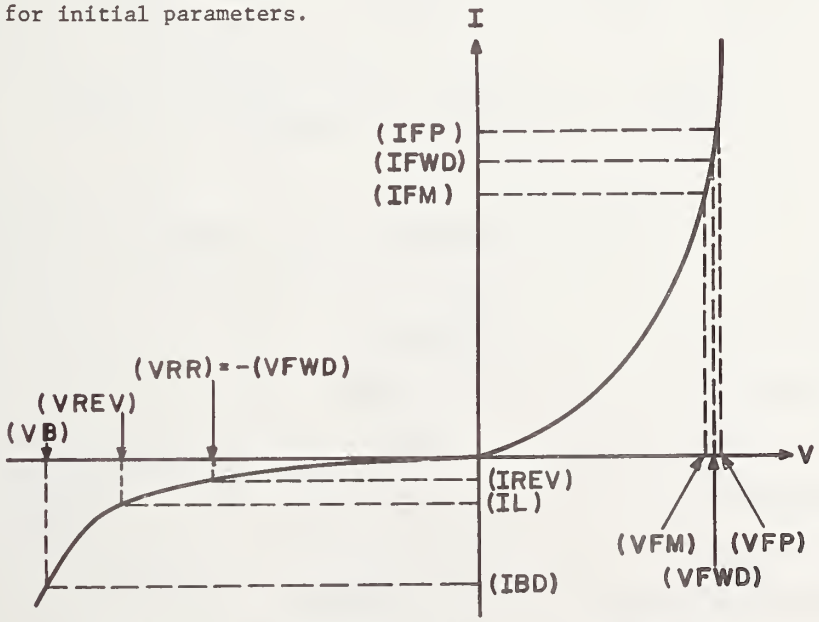


Figure 126. Definitions of some initial parameters.

Flow Chart - The flow chart is shown in figure 127.

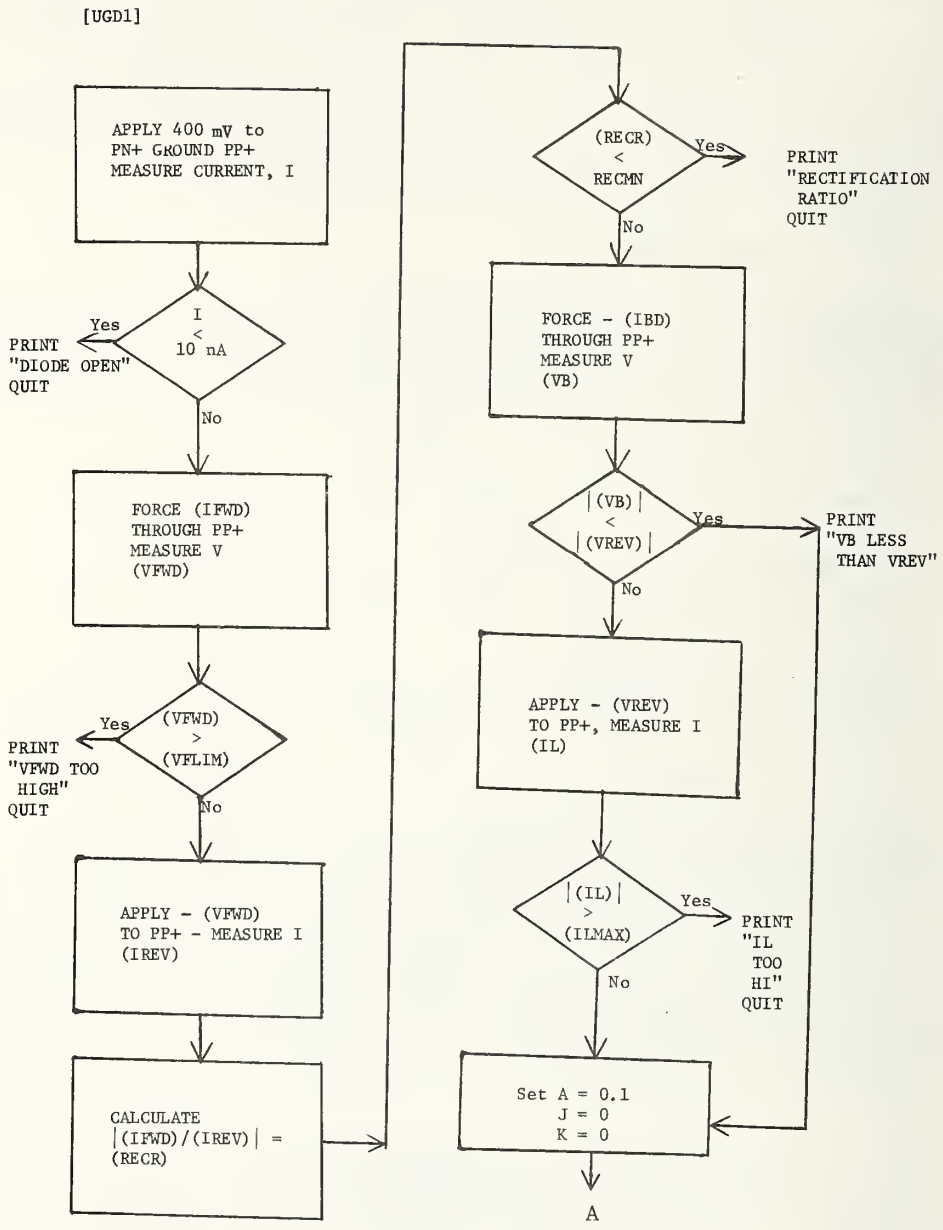


Figure 127.1. Flow chart for UGD1.

List of Outputs

- dc forward voltage (VFWD)
- Rectification ratio (RECR)
- Reverse breakdown voltage (VB)
- dc reverse leakage (IL)
- Series resistance (RSER)
- Injection factor linear (NLIN)

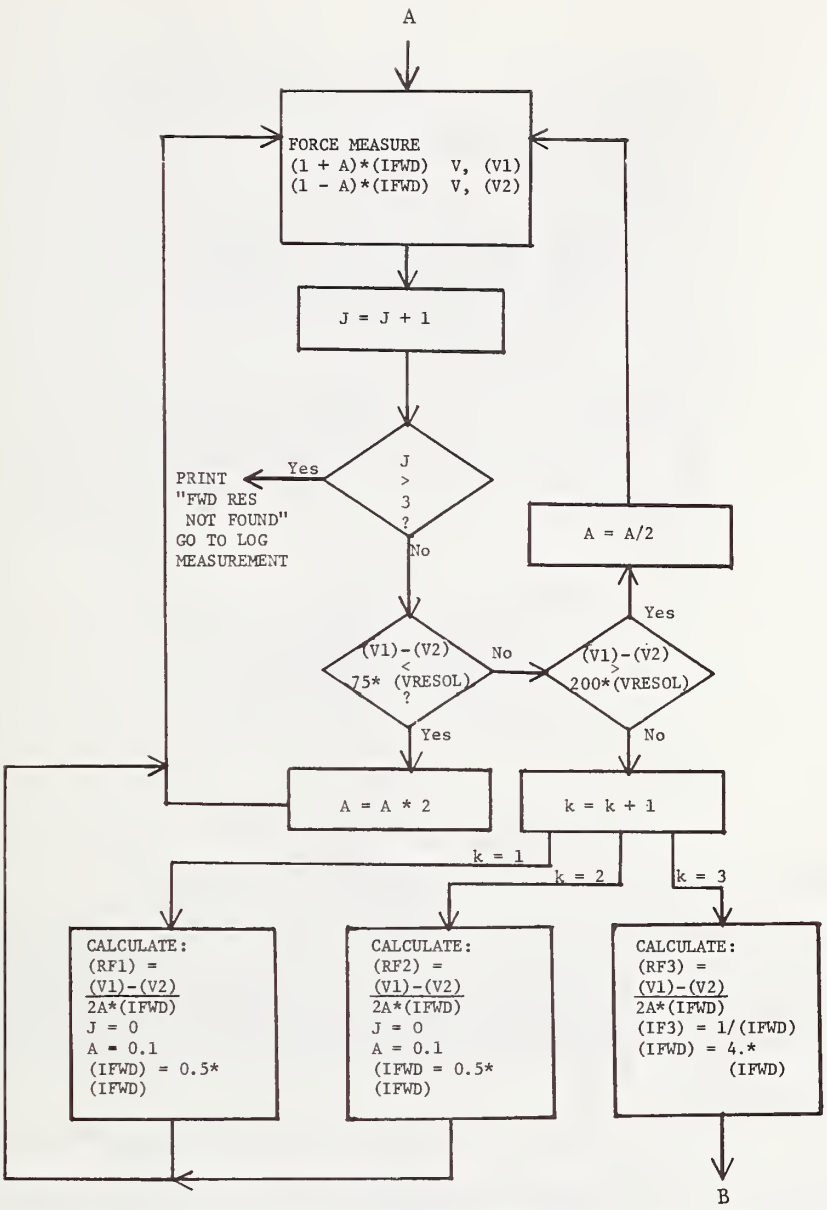


Figure 127.2. Continued.

- Forward leakage (I_o) (IO)
- Ideality factor linear (FQULN)
- Ideality factor log (FQULG)
- Shunt resistance (RSHUNT)

Less General Versions

Measures forward voltage
Rectification ratio
Reverse leakage
Reverse breakdown
} UDG2

Measures forward voltage
Reverse breakdown
} UDG3

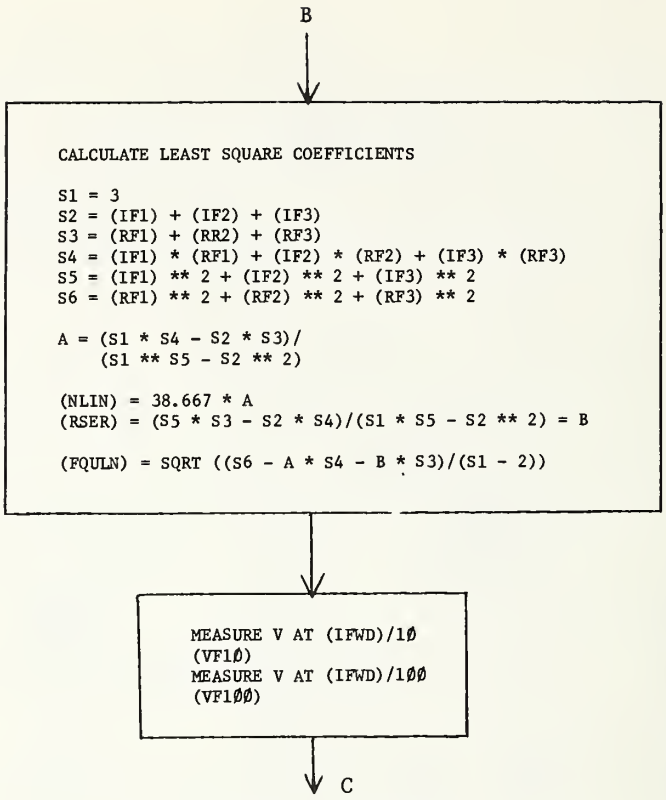


Figure 127.3. Continued.

Special Equipment - None unless very low currents are measured.

Samples of Data - Only the n^+p^+ diode (structure I-92) has been measured to date. Typical forward and reverse characteristics are shown in figure 128. A semi-log plot of another typical device is shown in figure 129. Note that the curves approximately fit a shunt resistance curve at low biases. This device is highly nonideal in the reverse direction but exhibits reasonable linearity in the log forward plot. Of particular interest perhaps is the linear forward curves at high currents. Clear evidence of series resistance is found in figure 128(d).

Histograms of automatically acquired data are shown in figure 130 and are explained in Table 3.

Potential Pitfalls - The measurements assume linear contact characteristics. If this is not present, first-order errors may be experienced.

Overall Usefulness - These structures are primarily useful as an independent test on overall process quality. The n^+p^+ diode is the only structure which yields any information which is independent of gate potential concerning the p-n junction properties of the process. If the contact geometry were slightly easier to analyze, one could obtain accurate values of the combined diffused layer resistances from the series resistance measurements. This set of structures is usually of second-order importance.

Other Related Structures - Related structures are I-46, I-47, I-3, and I-4.

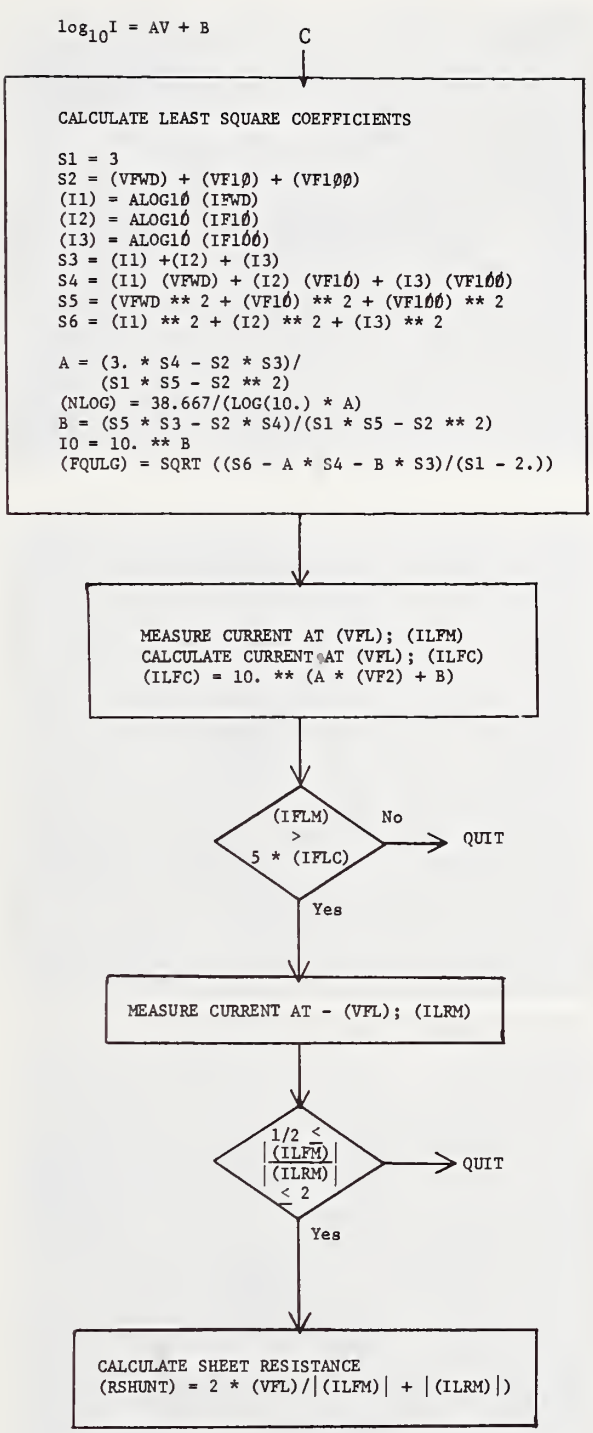
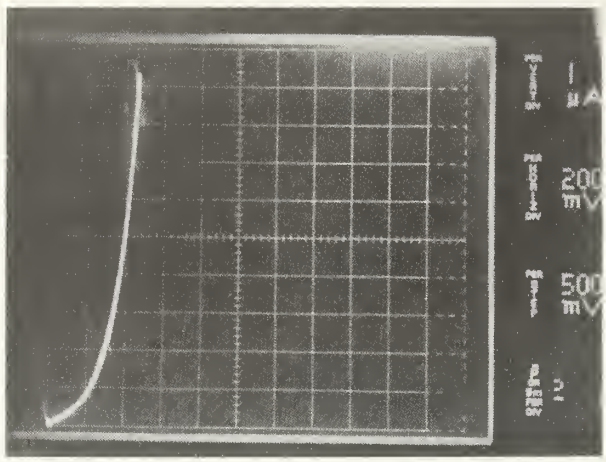
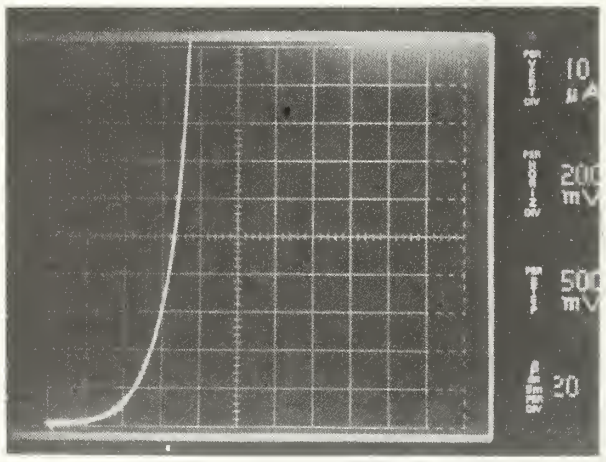


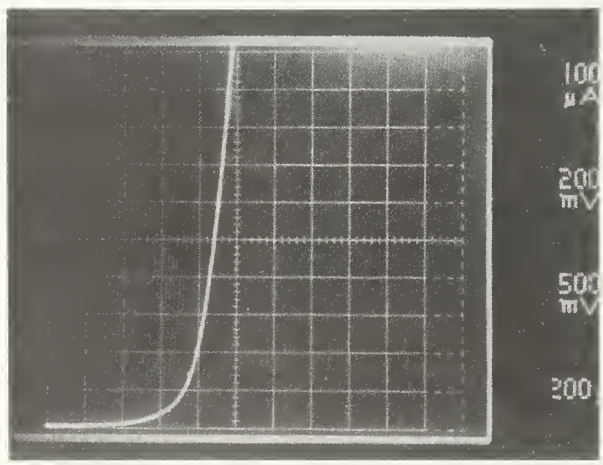
Figure 127.4. Continued.



(a)

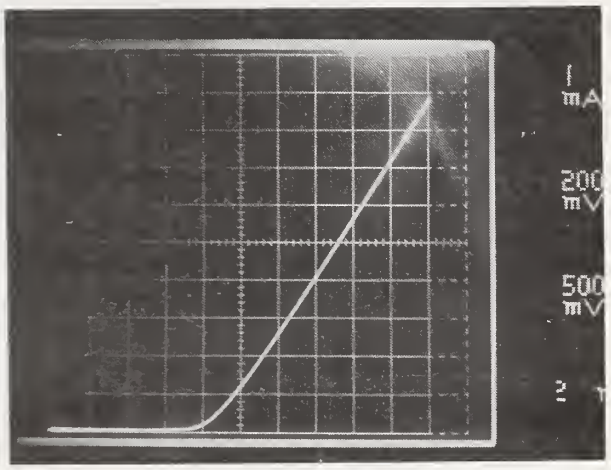


(b)

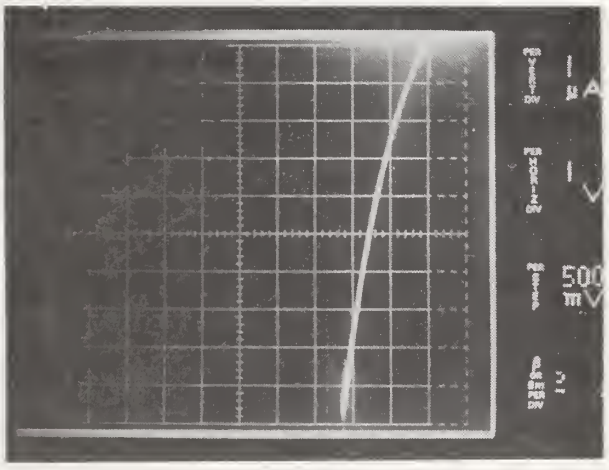


(c)

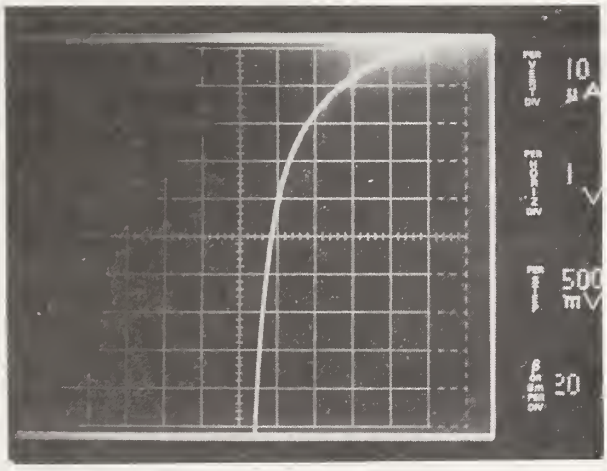
Figure 128.1. Characteristics of the n^+p^+ diode (structure I-92). Forward characteristics, (a) 200 mV/div, 1 µA/div, (b) 200 mV/div, 10 µA/div, and (c) 200 mV/div, 100 µA/div.



(d)

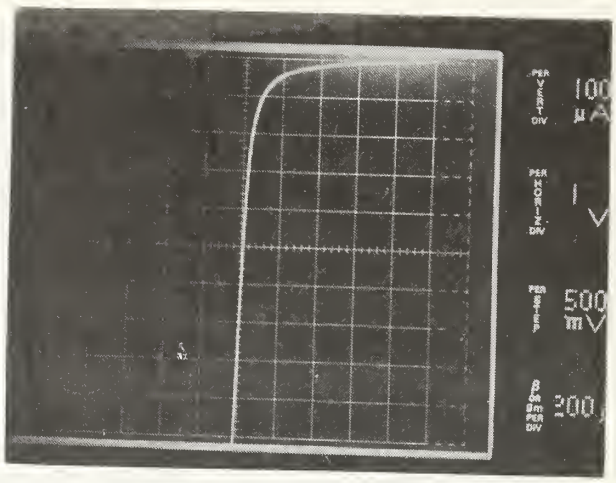


(e)

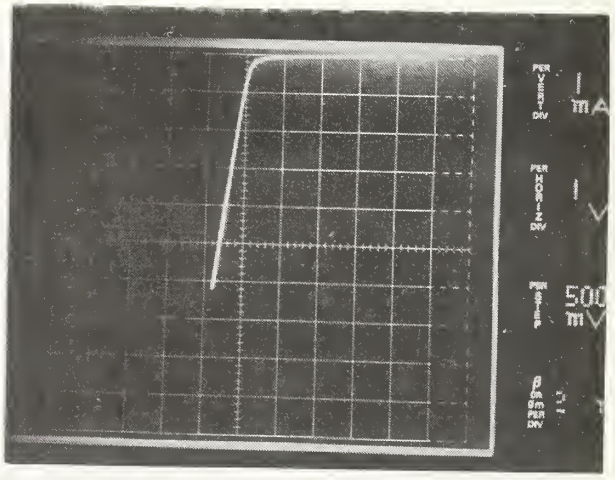


(f)

Figure 128.2. (Continued) Forward characteristics, (d) 200 mV/div, 1 mA/div, reverse characteristics, (e) 1 V/div, 1 μA/div, and (f) 1 V/div, 10 μA/div.



(g)



(h)

Figure 128.3. (Continued) Reverse characteristics, (g) 1 V/div, 100 µA/div, and (h) 1 V/div, 1 mA/div.

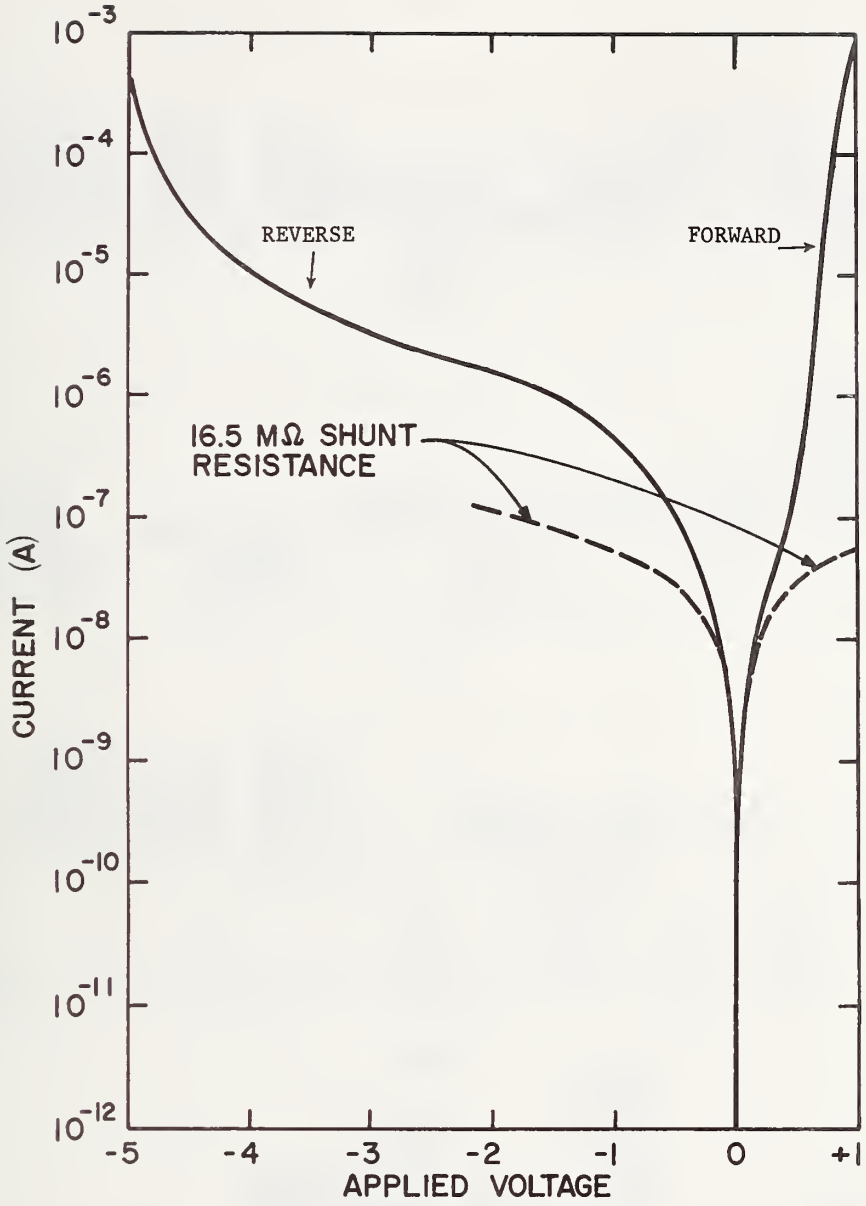


Figure 129. Log characteristics for ungated n^+p^+ diode. (Structure I-92, subsection 3.21).

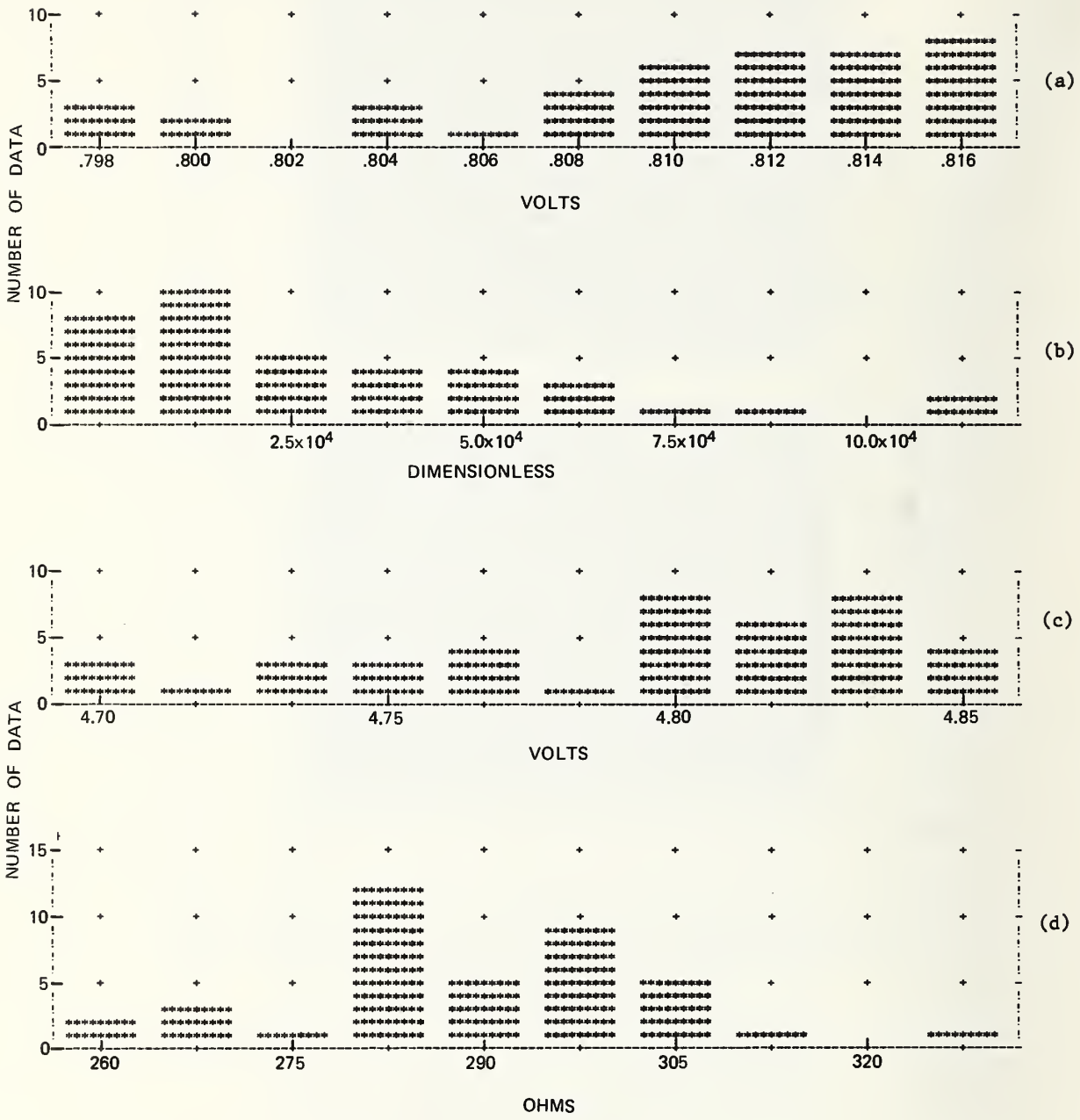


Figure 130.1. Histograms of automatically acquired data.
(See table 3 for explanation.)

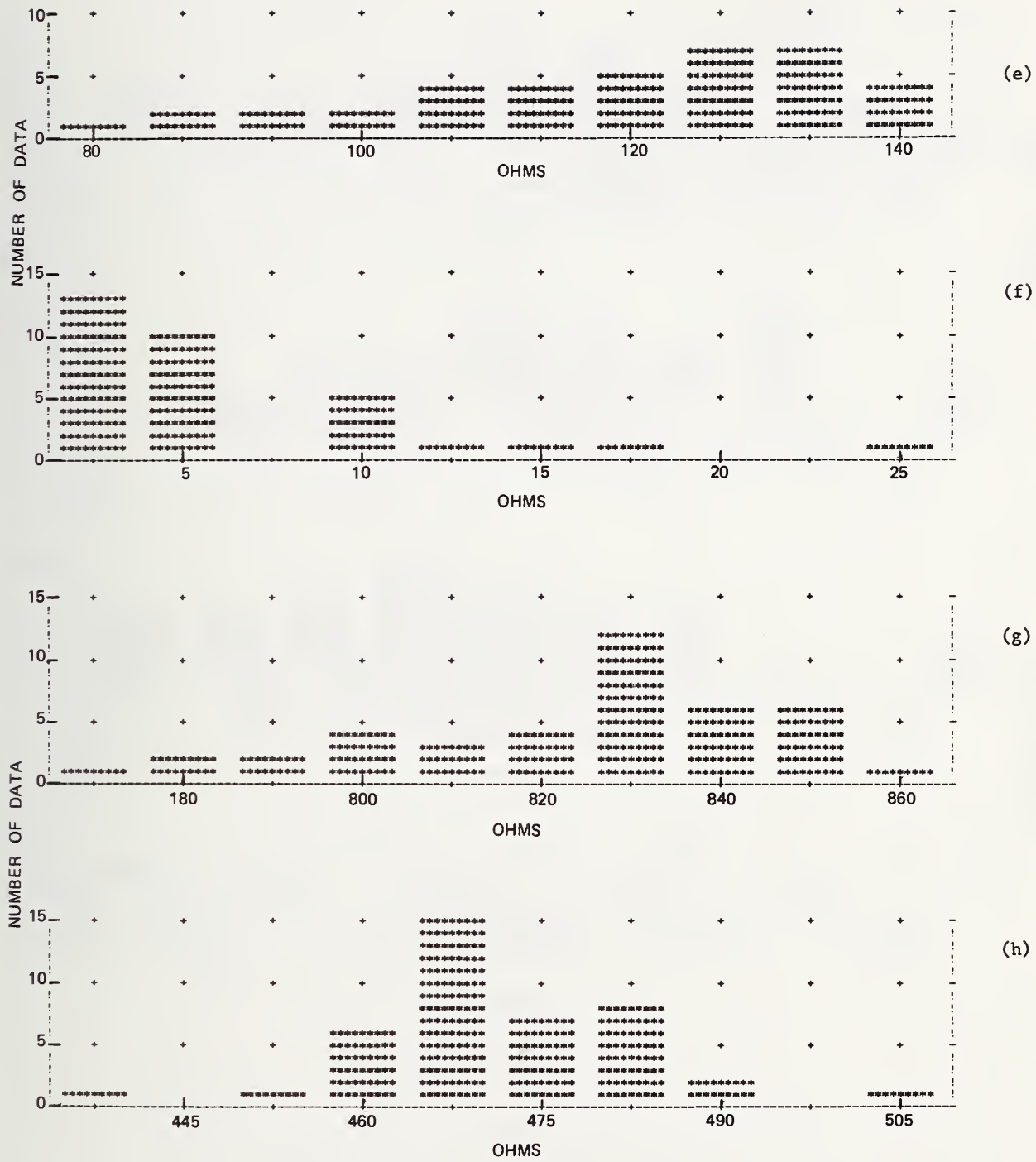


Figure 130.2. Continued.

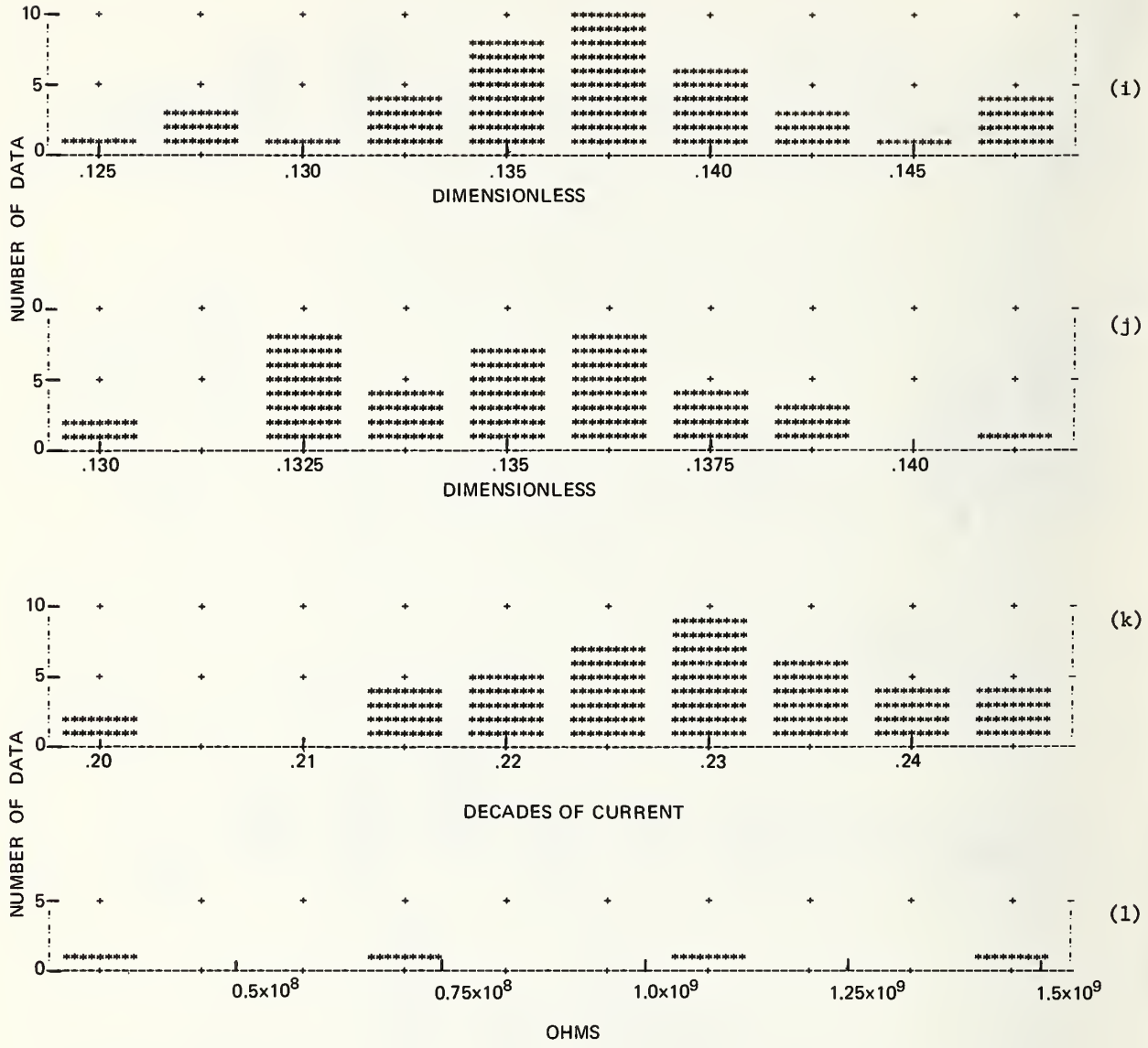


Figure 130.3. Continued.

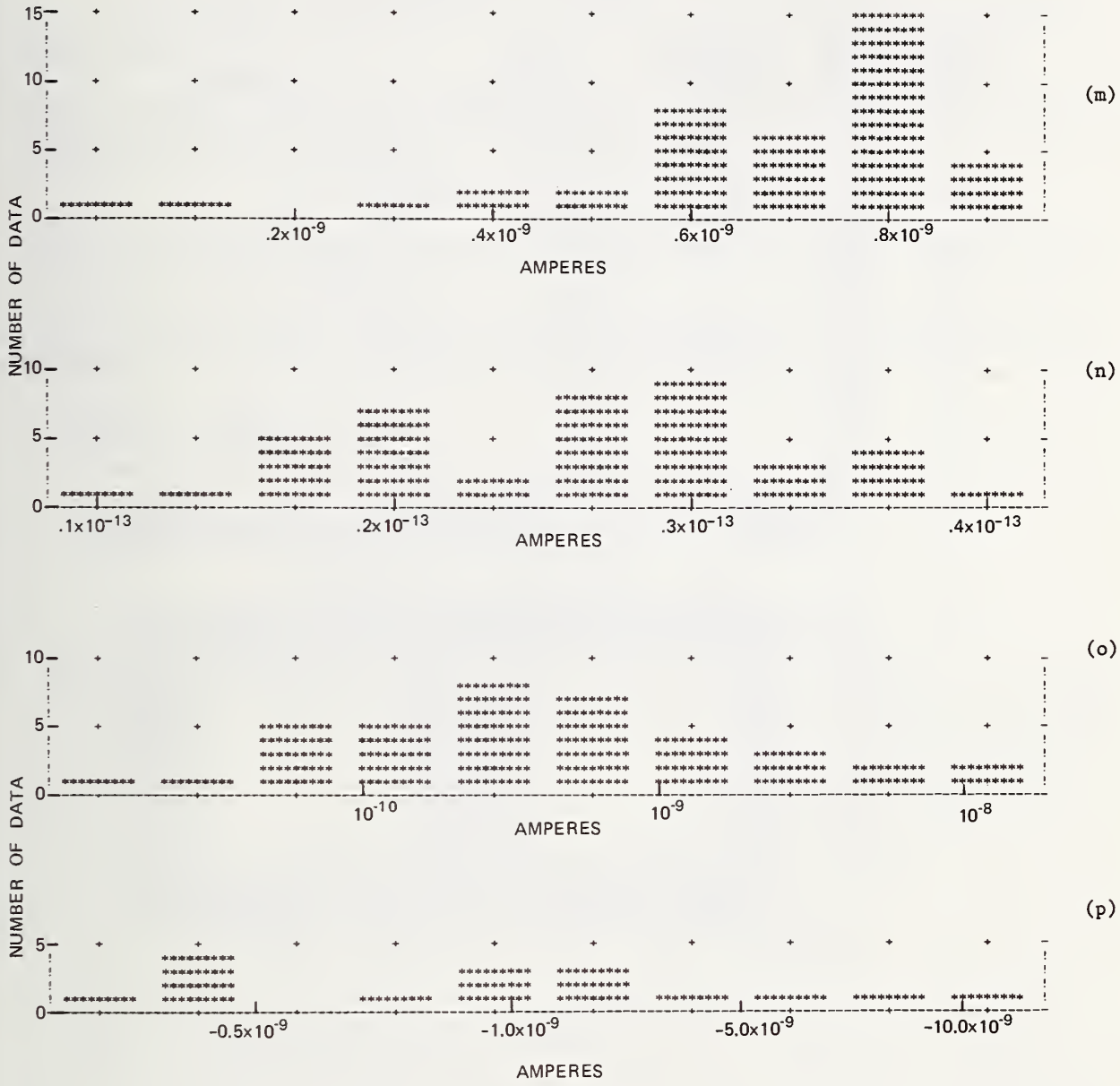


Figure 130.4. Continued.

TABLE 3. DISCUSSION OF FIGURE 130

Figure Section	Test Name	Excitation Level	Mean Value	Comments
(a)	VFWD	200 μA	0.815 V	good
(b)	RECR	---	3.86×10^{4}	good
(c)	VB	-100 μA	4.79 V	good
(d)	RF1	200 μA	293 Ω	good
(e)	RSER	---	117 Ω	excellent
(f)	FQULN	---	7.97 Ω	fair fit
(g)	RF3	50 μA	826 Ω	good
(h)	RF2	100 μA	477 Ω	good
(i)	NLIN	---	1.37	good
(j)	NLOG	---	1.35	excellent agreement with NLIN
(k)	FQULG	---	0.230	units are decades of current
(l)	RSHUNT	200 mV	9.2×10^{7} Ω	very few data
(m)	IL	-3.0 V	6.8×10^{-10} A	below system limit
(n)	Iϕ	---	2.0×10^{-14} A	log average
(o)	ILFM	200 mV	7.3×10^{-10}	below system limit
(p)	ILRM	-200 mV	1.5×10^{-9}	below system limit note: higher average than ILFM

3.24 MOS Capacitor; Single-Diffusion Type - II-1

Purpose - This test structure measures spatial integrity of parameters derivable from MOS capacitor measurements such as dielectric strength and thickness, interface change, and doping density.

Verbal Description - This structure is nearly identical to device I-20 of subsection 3.4 except that it stands alone and is repeated many times. The gate is 4.00 mil on a side and is surrounded by an n^+ diffusion.

3.25 MOS Capacitor; Double-Diffusion Type - II-2

Purpose - This structure serves the same purpose as structure II-1 except that low-frequency type C-V curves are obtained.

Verbal Description - This structure nearly is identical to devices I-42 and I-43 of subsection 3.6. The 4.0 x 4.0 mil gate is surrounded by alternating n^+ and p^+ diffusions of 0.4 mil width.

Line Drawing - The line drawing for these structures is shown in figure 131.

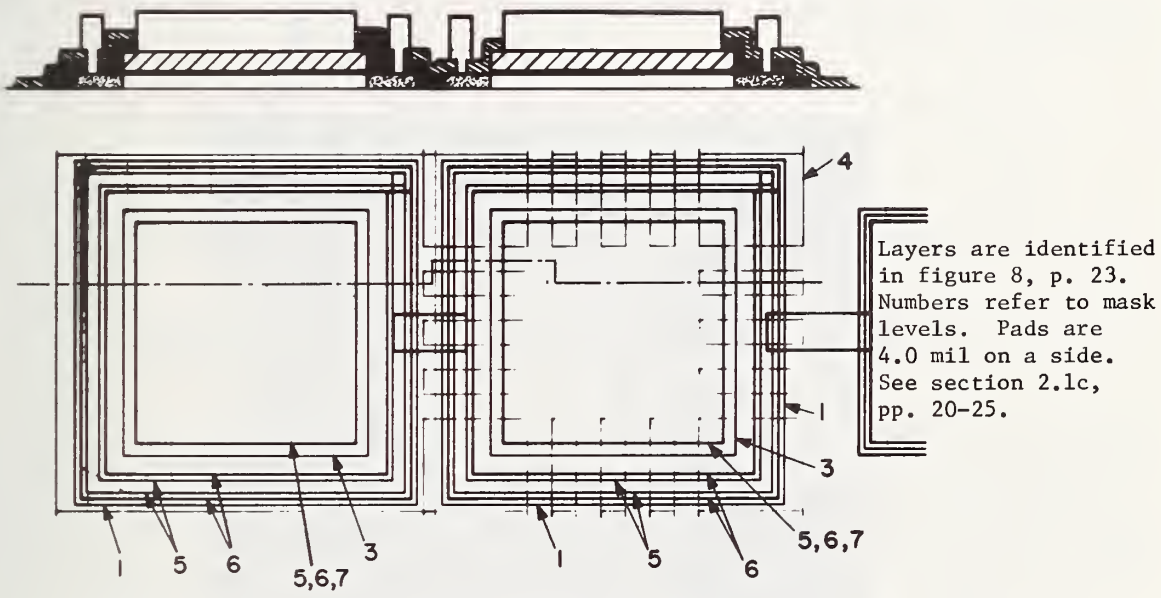


Figure 131. MOS capacitors, test structures II-1 and II-2, computer line drawing and cross section.

Halftone Photograph - The photomicrographs for structures II-1 and II-2 are figures 132 and 133, respectively.

Electrical Access - These descriptions are accessed by a common substrate connection and a gate for each. These are designated PSUB and PGATE, respectively.

Testing Method - These structures are tested by the methods outlined in subsections 3.4 and 3.6. A lock-in amplifier is used with the input head electrically shielded if C-V and/or G-V curves are desired. Discussions of the methods of making and interpreting these measurements are given in ref. 14. Since the gate area is reasonably large, there is little error in the area from device to device. Therefore, these structures are good for mapping the electrical dielectric thickness across wafers. They also provide an *indication* of the flat-band integrity across wafers. Both of these measurements require the ability to measure capacitance.

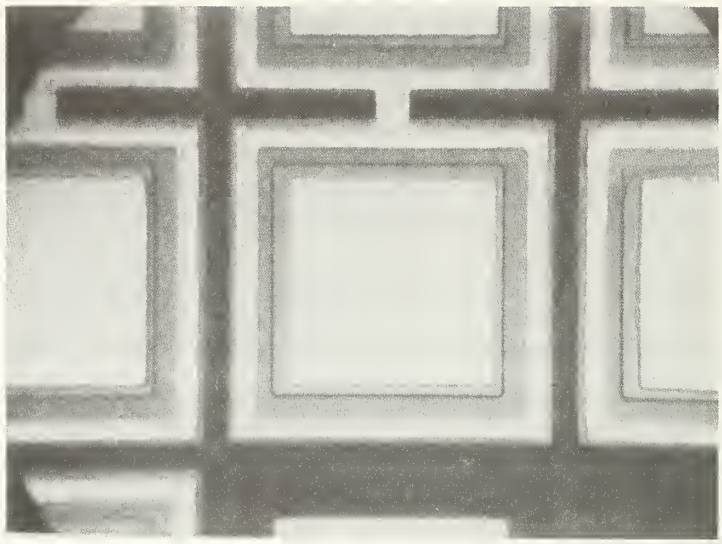


Figure 132. Photomicrograph, single-diffusion type MOS capacitor, test structure II-1.

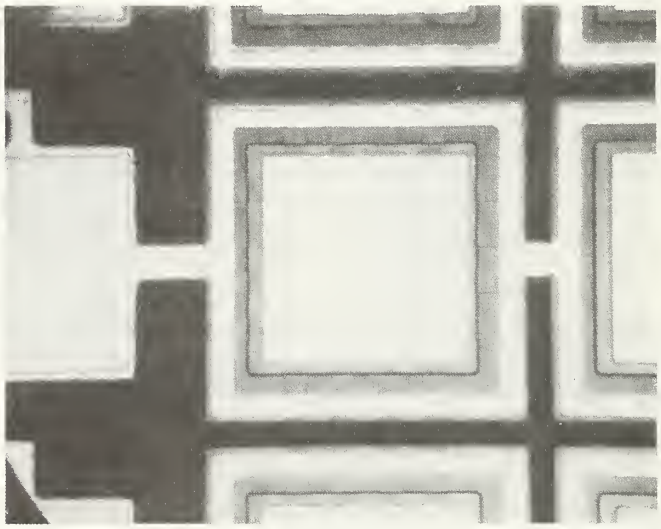


Figure 133. Photomicrograph, double-diffusion MOS capacitor, test structure II-2.

The primary use of these structures, however, is to measure the dielectric strength properties of the channel oxides on structures which have no edges and to correlate the optical properties observed with the electrical properties. For example, the failure locations may be visible as burned spots. These tests were described in subsection 3.4. In addition, comparison of structure II-1 with II-2 can show if the type of substrate contact is affecting the electrical properties.

Special Equipment - For C-V and/or G-V measurements, typically frequencies of $\leq$10 kHz are desirable because of the very high series resistance of the epi [14], and the capacitance levels are typically on the order of 1 to 5 pF maximum. This requires a lock-in amplifier approach using commercial equipment.

Samples of Data - Plots of the steady state C-V (90° current) and G-V (0° current) characteristics obtained from these structures are shown in figure 134. The curves were generated using lock-in amplifier techniques at 10 kHz. These curves are almost precisely as expected and exhibit serious series resistance effects at capacitances below 1.75 pF. We note excellent agreement in the accumulation capacitances for both structures. Agreement is actually better than the plot indicates. In the original data there was no discernible difference between the accumulation capacitances for either structure. In addition, the inversion and accumulation capacitances are identical.

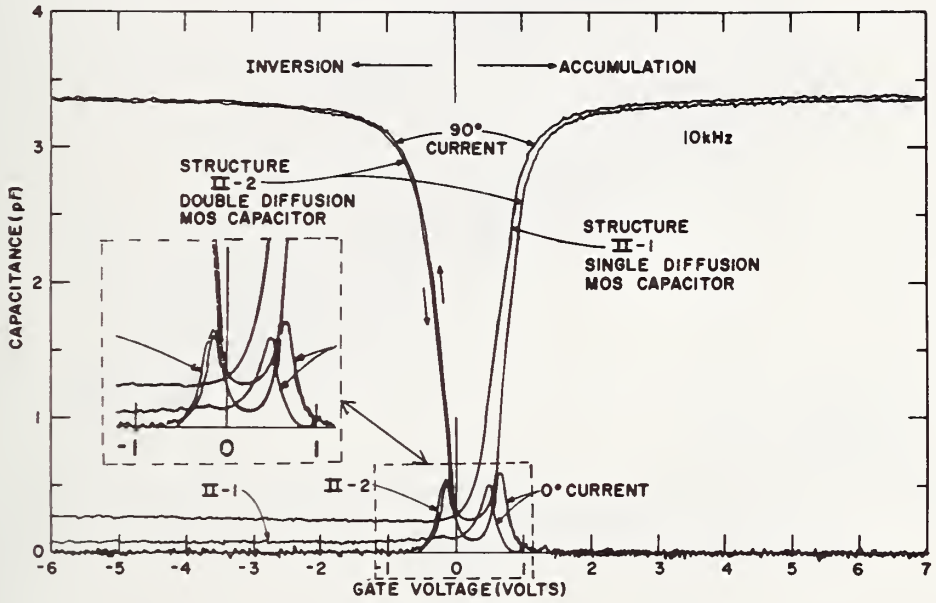


Figure 134. Results from the typical II-1 and II-2 structures. Both C-V and G-V are plotted on the same scale for convenience.

A surprising result was found in the flatband voltages observed, however. The structure with p+ doped oxide over part of the gate (II-2) is shifted to the right with respect to the other device (II-1). This result is quite unexpected, and the reasons uncertain at present. Two likely possibilities for this shift are: (a) shift in the work function of the poly due to difference in poly doping and (b) preferential annealing behavior due to different atomic transport of active species through the oxides over the poly. None of the devices on this pattern can resolve this issue since it is built into the process. This difference would usually go completely unnoticed since it is relatively small (0.15 V) and would normally be buried in the noise of the measurement or uncertainty in other parameters which influence the flatband potential.

Such a difference could have major implications in some circuits where threshold matching is critical.

A family of C-V and G-V plots at 10 kHz across a wafer at 132-mil increments is shown in figure 135. This method of data presentation is very valuable for condensing this relatively sophisticated data into a readable form. Note that the only significant deviation (on this scale) across the entire wafer occurred at the very edge. Plots at 6-mil increments of the accumulation capacitance across a 1-in. wafer showed local variations of the order of 0.5% while a smoothly varying trend of ~5% across the entire wafer was found.

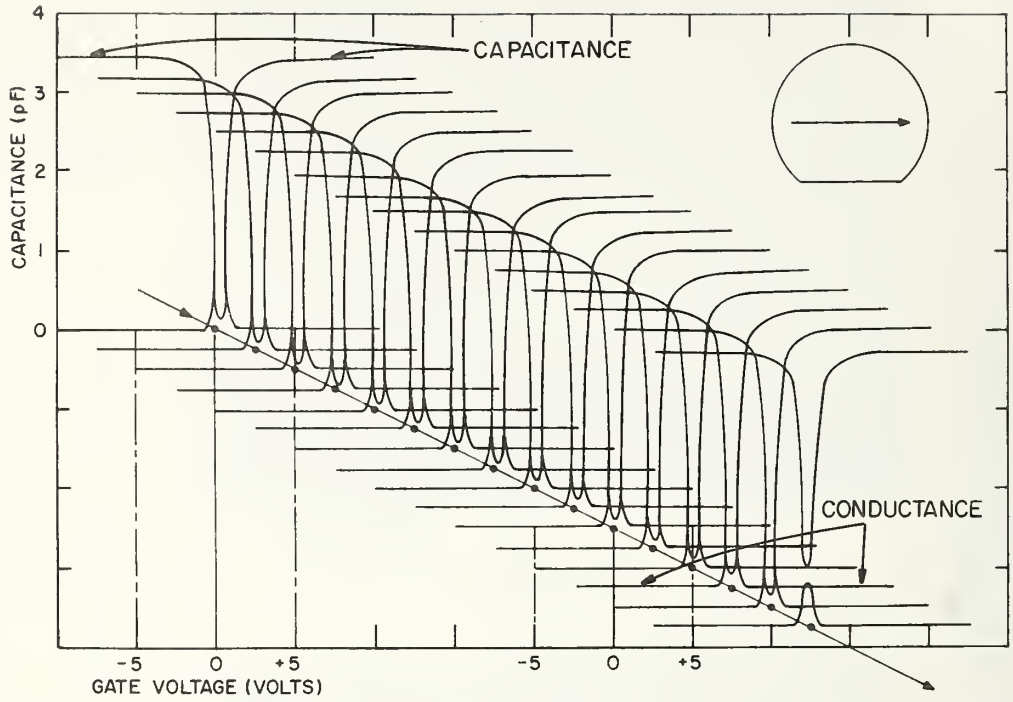


Figure 135. Capacitance and conductance similar to that in figure 134 from structure II-2 across a diameter of a 2-in. wafer plotted in a three-dimensional representation. The capacitance and conductance nearly coincide near VG = 0 [14].

Automatic dielectric breakdown data were acquired on several wafers. Some wafers showed very few failures at less than the expected field. Others, however, showed distributions similar to figure 136(a). In these plots the fail limit was 1 μA, and the step size was 5 V. Both plots have fixed limits of -100 to +100 V. The data in figure 136(b) were obtained from structure II-2 while those in figure 136(a) were obtained from the structure II-1 immediately adjacent. We note that the two distributions are drastically different. Note also that these data represent one pass across a 3-in. diameter wafer and that 448 data points are presented. The main difference between II-1 and II-2 was the presence of the n+p+ junction, and subsequent investigation revealed that the failure was occurring at that point. This would usually not have been found nearly as quickly nor as certainly (if at all) were it not for this comprehensive approach to process characterization.

Potential Pitfalls - There are no pitfalls with these structures which are not present in any SOS/MOS capacitor.

Overall Usefulness - As has been seen in the data sample these structures provide potentially a great deal of information which is not easily obtainable from small MOS transistors. This information includes channel oxide thickness, flatband voltage, surface state density, doping profiles (within the limits of the correlation between capacitance and depth), inversion point (using structure II-2), maximum depletion depth (on thick films when series resistance is not severe), and dielectric strength properties. Unfortunately, most of this information requires a dedicated lock-in amplifier to measure both the capacitance and conductance simultaneously. Such instruments are commercially available, but it is not clear that the information obtained is worth the effort of automating these measurements. Parallel, if not exactly equivalent, information is obtainable from the MOS transistor or gate-controlled resistors. This decision to automate or not is particularly perplexing when one sees the valuable information obtainable from simple dielectric strength measurements. If one combines the dielectric strength measurements with C-V and G-V measurements, either a special relay matrix or a C-V, G-V instrument which can also detect dc current is required. The relay matrix would be used to switch between the C-V, G-V meter and the dc current meter. An alternative is to use the C-V or G-V data as an

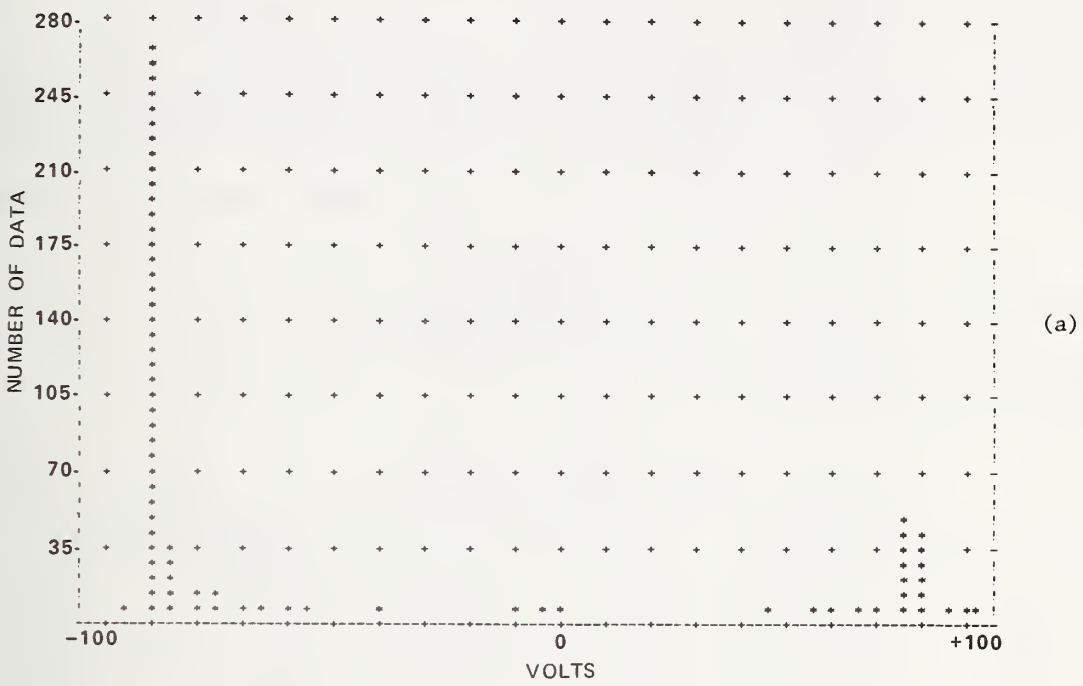
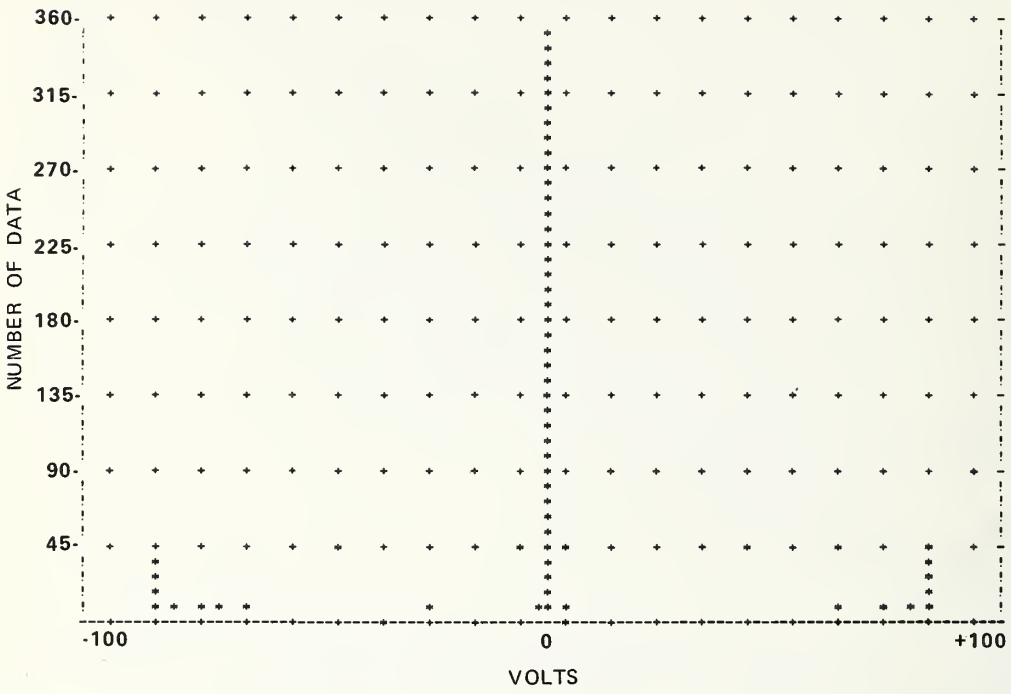


Figure 136.1. Breakdown data on fixed scales (-100 to +100 V). (a) Structure II-1 (single diffusion).

indirect indication that the dielectric strength has been exceeded. This can be done, but frequently the input stages are severely overloaded when dielectric failure occurs and this may damage the instrument. Even if damage does not occur, the time for recovery from the overload can be excessive (30 s or more for one instrument). We are therefore forced to conclude that under the boundary conditions of minimal special equipment and minimal data acquisition time, the dielectric strength is the primary output from these structures. They are quite good for obtaining these data as small edgeless structures and have been used to provide a base line for dielectric strength data.

Other Related Structures - All other MOS capacitors are related to these. Of particular interest are I-20, I-42, and I-43.



(b)

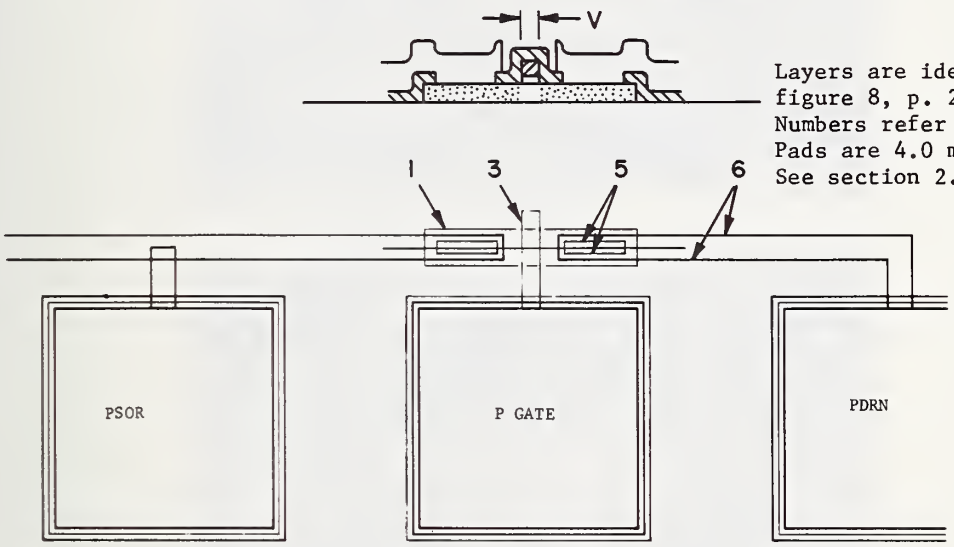
Figure 136.2. Continued.
(b) Structure II-2 (double diffusion).

3.26 MOS Transistors - II-3, II-4

Purpose - These test structures measure spatial integrity of MOS transistor parameters.

Verbal Description - These structures are the same as those of subsection 3.16 except that the channel dimensions are 0.3 x 0.6 mil and the contacts are 0.2 x 1.0 mil. This structure has the gate directly connected to a poly pad. The contacts are not allowed to cross the island edge in order to allow the contacts to approach near to the channel region.

Line Drawing - The line drawing for this structure is shown in figure 137.



Layers are identified in figure 8, p. 23.
Numbers refer to mask levels.
Pads are 4.0 mil on a side.
See section 2.1c, pp. 20-25.

Figure 137. MOS transistor, test structures II-3 and II-4, computer line drawing and cross section.

Halftone Photograph - The photomicrograph for this structure is shown in figure 138.

Electrical Access - These are ordinary MOS transistors with the usual contact points:

Source contact	PSOR
Gate contact	PGATE
Drain contact	PDRN

Testing Method - These structures are tested exactly as those of subsections 3.1 or 3.13.

Samples of Data - These structures have been used to produce many plots of transistor parameters across many wafers. One could fill many pages with various types of leakage, threshold, drive current, drain breakdown, etc data that have been acquired from these structures. Typically the data are plotted either as a three-dimensional representation similar to that used for the capacitance-voltage data (fig. 135) or as a plot of individual points as a function of position. The three-dimensional representation provides a method for examining literally millions of data points simultaneously. Occasionally it is valuable to use the methods described in section 4 or to simply study a list of numbers representing the main features of the data.

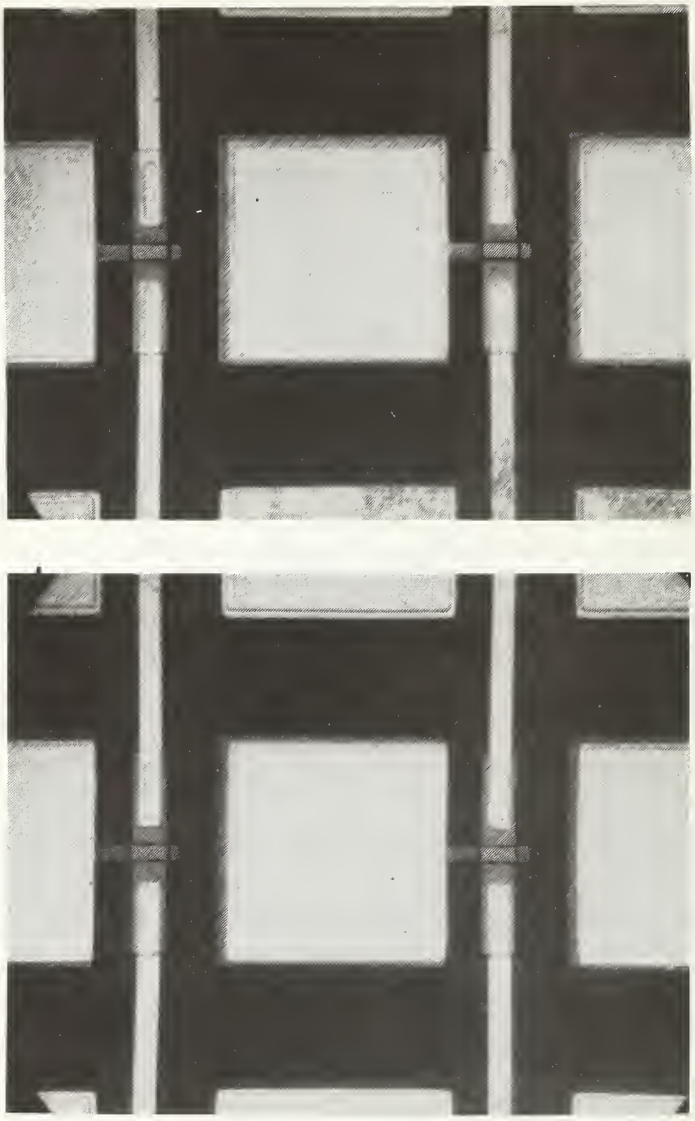


Figure 138. Photomicrograph, MOS transistors
(a) n-channel (II-3) and
(b) p-channel (II-4).

A plot of the log drain current as a function of gate voltage from various positions is shown in figure 139. Here the three-dimensional plot is used. The currents are independent of gate voltage at gate voltages less than ~-2 V for most of the devices. An instability is noted in the current immediately above the minimum which is due to edge currents. The degree of the instability is clearly apparent and shows differences of ~0.5 to 1.0 decade of current and ~0.2 to 0.6 V. The more unstable devices seem to be grouped together which strongly suggests that phenomena other than on a microscopic level are important. The devices which have gate-voltage-dependent currents below -2 V were examined *during the test* and found to have black "specks" in the channel area. Thus, a direct correlation between physical structure and leakage was established. The blank space indicates devices which were not suitable for measurement. On the scale used there is no difference between these devices at high currents. The key to being able to make these statements is the volume of information which is assembled into an easily digested form and the ability to simultaneously compare electrical data with a) itself, b) neighboring devices, c) slightly different stimulus levels on the same structure, d) stimulus history (hysteresis), e) wide ranges of stimuli, and f) the physical structure as revealed by its optical properties (microscopic examination).

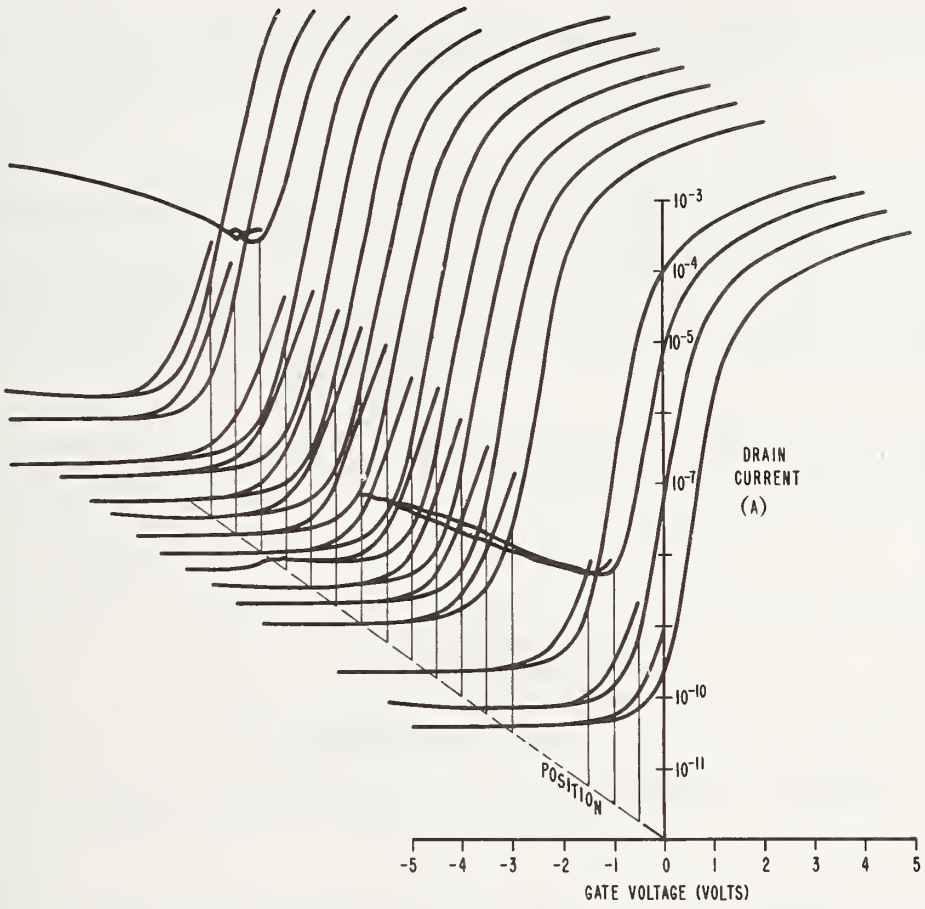


Figure 139. Three-dimensional representation of log gate transfer characteristics for an n-channel device (II-3).

The number of plots that one can put on a single sheet and still be able to resolve the curves is limited, and the data acquisition time is likely to be considerable. Representing a single pass across one 2-in. wafer can require 10 or more sheets of paper and involves many millions of data points. The plot of individual points as a function of just the position variable can also be very valuable and can be obtained in a very short time with automatic equipment. Such a plot is shown in figure 140. These plots obviously do not contain as much information as the three-dimensional plots because only two variables are involved. They are very valuable for examining a large number of devices quickly. Figure 140 shows the drain current at VG = -5 V and VD = -5 V for a p-channel transistor (structure II-4). This represents the drive current available from these devices when used with a 5-V power supply.

Approximately 1.5 in. of a 2-in. wafer is shown. Several very interesting features of these data are noted.

- A significant number of the devices have no output on the scale used here.
- The distribution observed shows a very "fuzzy" nature.
- Gradual trends in the data over relatively large distances are observed.
- There is a tendency for zero output devices to cluster together.
- Approximately $\pm$20% total variation is seen across the wafer for operating devices.

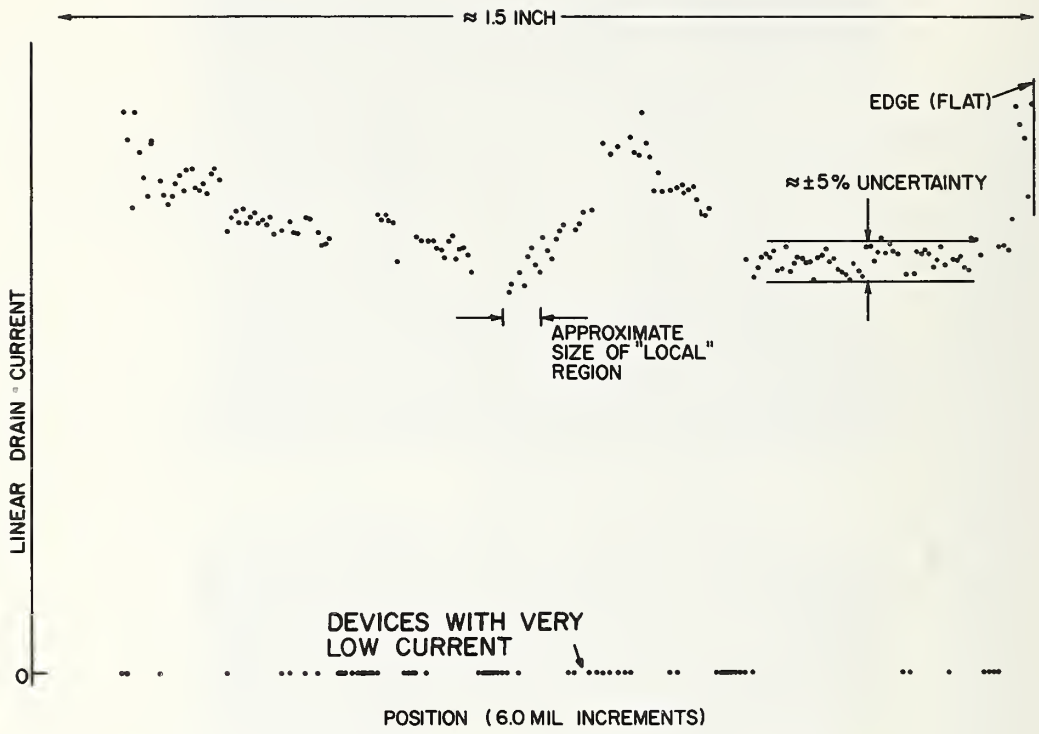


Figure 140. p-Channel saturation current in heavy inversion.

- The zero output devices are probably not caused by probing problems since low currents are detected on the same devices and n-channel devices in the same row exhibited much fewer instances of zero output devices.
- The fuzziness may be caused primarily by differences in the geometry of the channel regions. If material properties are responsible, the 6.0-mil spacing is not close enough to produce a smooth curve.
- Within a "local" area, whose size is approximately 50 mil in this case, an uncertainty of $\pm$5% exists.

Obviously, the most interesting observation here is the zero output devices since these would be fatal to virtually any circuit. The "personality" of the system is readily apparent from data of this type. The significance of a single-device measurement is clarified. Subsequent investigation showed that a surface-state problem was probably responsible for the low output devices. Some examples of very high resistance contacts were also found. Many wafers have been tested with no problems of this type; the phenomenon is therefore not inherent to SOS.

The programs for generating the type II parameters discussed in section 4 have not been completed; no examples are available. Examination of figure 140 clearly shows that the analysis suggested in section 4 could be effectively used here.

Potential Pitfalls - Although these devices are designed without "pushing" normally available lithographic capabilities, the channel dimensions are well within the range where an uncertainty exists as to the actual channel dimensions. One must be very careful not to read too much into the "fuzziness" observed in terms of material properties. On the other hand, extrapolated threshold voltages (for example) are relatively insensitive to small changes in

channel geometry and may be interpreted somewhat more confidently. In any case the fuzziness observed does represent the parameters available for circuit design (for this particular channel geometry). Whatever the causes, large devices can usually expect to be less "fuzzy" and smaller devices can expect to be more "fuzzy."

Overall Usefulness - These structures are the most useful of all the structures for correlating physical defects with electrical performance. They can produce "spreading resistance" type plots over wafer surfaces but without the limitation to only one parameter. A clear picture of many details of the material and the overall parametric integrity can be obtained from these structures. They provide detailed information concerning the tolerances which must be allowed over any particular circuit area. We note that over any given circuit only ~5% variation in device current would be expected in the case of figure 140; but that if the entire wafer were considered 20% allowance would have to be made. This kind of information can be very useful for developing the highest performance circuit possible with the technology.

There are no improvements suggested for this structure. It should be noted, however, that this structure can be very effectively used to characterize contact-diffusion resistance by processing without the poly. One can examine both types of diffusion together (using both II-3 and II-4) or use only one type (by eliminating mask level 4) and plot the resistance between two contacts or four contacts in series or in parallel.

Other Related Structures - These structures are related to all other MOS transistors.

3.27 Probe Resistance Test - II-5

Purpose - This test structure measures variations in probe resistance across wafers and verifies suitable contact.

Verbal Description - This structure consists of a bar of aluminum 4.0 mil wide and 10 mil long. Each end of the bar is a standard bond pad and the aluminum crosses the steps of the islands at the edges of the pads.

Line Drawing - The line drawing for this structure is shown in figure 141.

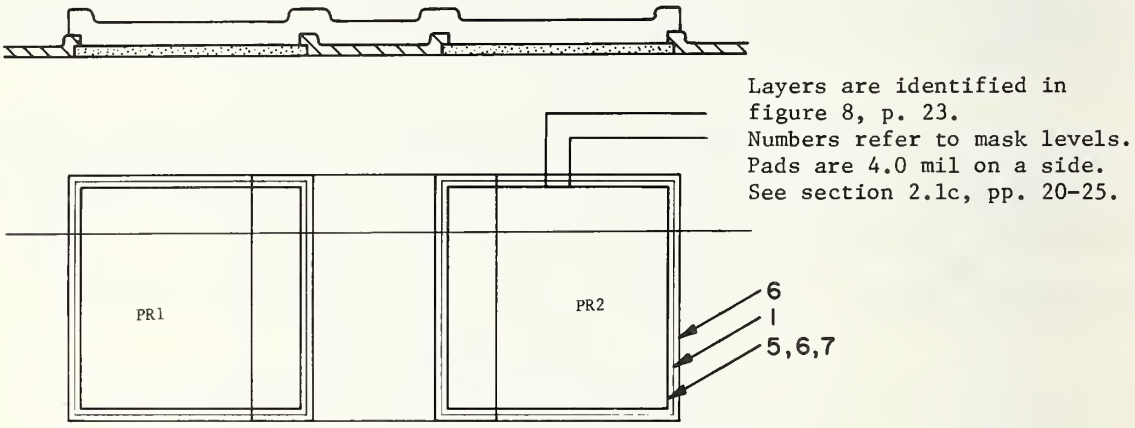


Figure 141. Probe resistance test, test structure II-5, computer line drawing and cross section.

Halftone Photograph - The photomicrograph for this structure is shown in figure 142.

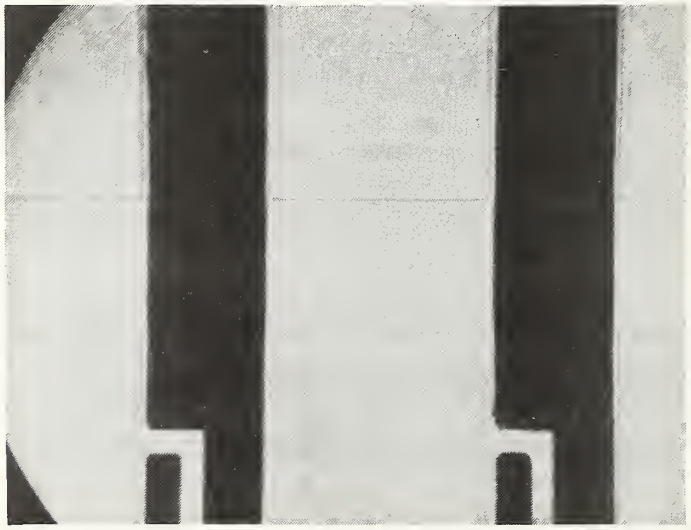


Figure 142. Photomicrograph, probe resistance test, test structure II-5.

Electrical Access - The two bond pads are designed as PR1 and PR2.

Testing Method - This structure is tested as a two-terminal resistor as described in subsection 3.3. The test can be performed in several ways for different purposes. The most important feature of this structure is that it tests the total system for electrical contact as it exists in almost every pad in the pattern. In other words all the series resistance

present from the point where the sense lines (in the automatic tester) terminate to the point where the metal runs off the pad is represented by the resistance between PR1 and PR2. Assuming the sense line terminates on a connector (connector C) which is on the end of a cable which is connected to the probe card connector (connector PC), this resistance includes:

(1) R of connector C

(2) R of wire between connector C and connector PC

(3) R of connector PC

(4) R of connector PC to probe card

(5) R of metal lines on probe card

(6) R of metal line to probe

(7) R of probe itself

(8) R of probe to aluminum

(9) R of aluminum on top of pad

(10) R of aluminum on edge of pad and again as the return path is taken back to connector C.

It is clearly impossible to separate all of these components with a single resistance measurement. Any other design of this structure would not represent the actual situation for most of the structures. If the metal between the pads were made narrow, the dominant resistance might be in this metal, and this would make the interpretation of these data even more difficult. (The aluminum resistance itself is available from other structures.) Fortunately, one would not expect most of the resistance above to change from device to device. By far the most likely resistance to change from device to device is the probe to aluminum resistance since this is determined by factors such as probe skid, oxide build-up on probe surface, etc. The next most likely candidate is the aluminum itself. Measurements of aluminum resistance across wafers has shown that this parameter is usually stable and has a value of ~30 milliohm/square for the thickness typically used here. This would produce perhaps 50 milliohm of the total resistance depending, of course, on the exact placement and contact area of the probe. Therefore, as one probes across a wafer, the change in resistance found represents the change in the resistance 8, 9, and/or 10. One can short the probes together using a thick gold substrate or touch the probes together or use any other reasonable means to obtain a minimum resistance. (One can also put the sense line as close to the probe tip as possible to minimize the error.) This minimum resistance is the total of the fixed resistances 1 through 7 above. Of course, if the probe card is removed or the connector unsoldered, this resistance may change.

The object of this exercise is to understand and measure effectively the expected resistance existing between the measurement system and the sample. It is not necessary to go further to separate the resistance components unless the resistances existing are not tolerable. It is important to use voltage stimuli for these measurements to avoid "forming" the contacts with the high voltage possibly experienced from unsatisfied current sources. Passive probes in particular must perform without "forming." Typically the total resistances experienced in the system used for this work are of the order of 1 ohm. This requires applied potential in the few millivolt range for device currents in the few milliampere range.

Samples of Data - Results of the probe resistance test across a 2-in.-diameter wafer are shown in figure 143. The total system resistance is plotted since this is effectively what the measurement system sees. The portion of the resistance due to the probes and aluminum is between 40 and 480 milliohm (for two probes). There is relatively severe local scatter but an overall trend exists across the wafer. This trend is perhaps caused by wafer or chuck warpage with resulting overdrive variation. The local scatter probably represents mainly probe to aluminum resistance and is possibly caused by alternate aluminum oxide formation after one probing and subsequent removal after the next probing. In any case

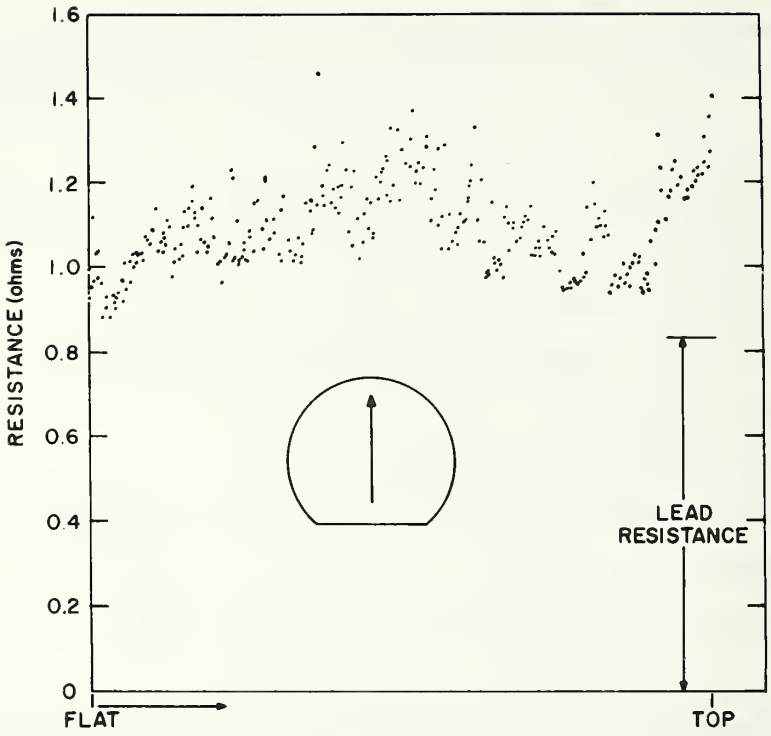


Figure 143. Probe resistance measured from structure II-5 using fine tungsten probes. The probe resistance is the difference between the measured resistance and the lead resistance.

it is clear that the total system resistance ranges between 0.9 and 1.4 ohm for this sample. Any variations of this order (0.5 ohm) in contact resistance, for example, can reasonably be explained by probe resistance variations.

Data from another wafer and another probe card are presented in figure 144. Here it is seen that the resistance ranges from ~1 to 2 ohm with a mean from 126 samples of 1.36 ohm. This represents a typical case for the system used here.

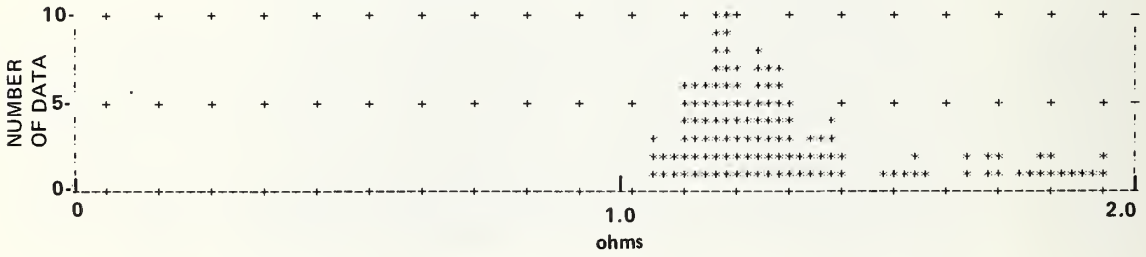


Figure 144. Data from another wafer and probe card, structure II-5.

Potential Pitfalls - These tests must be done with voltage applied and current measured. The Al_2O_3 layer which builds up on aluminum pads can be "formed" (punched through) by high voltages in some cases, and constant current measurements are likely to produce these high voltages. If a low compliance limit is set (10 mV or less), constant current measurement could also be used.

Overall Usefulness - This structure is indispensible for confidence in the electrical contact method and for an estimate of the error introduced by assuming a zero resistance probing process. It is also very useful for detecting a "Y" type II element in the intersection as mentioned earlier. Other uses are monitoring of probe resistance changes and other changes which may influence the measured resistance. If more detail is desired in separating the component of the resistance, other structures such as aluminum without steps or more widely spaced probes (to minimize the probe placement error in the total resistance) could be employed. This does not seem to be a valuable way to spend one's energy unless these 1- to 2-ohm resistances are causing trouble. They cause a small amount of trouble in the absolute accuracy of the measured contact resistance but are negligible for virtually every other purpose. No changes are recommended.

Related Structure - The aluminum resistance structures I-45 and V-3 are useful for measuring the aluminum resistivity on sapphire.

3.28 MOS Transistors; Variable Channel Length - III-1, III-2

Purpose - These test structures measure the effects of various channel lengths.

Verbal Description - This structure contains 15 ordinary type transistors whose channel width is constant at 1.0 mil and whose channel lengths are 0.05, 0.1, 0.15, 0.2, 0.25, 0.3, 0.35, 0.4, 0.5, 0.7, 1.0, 2.0, 5.0, and 10.0 mil. One device has 0.3-mil channel width and 10.0-mil channel length. All devices have common sources and gates and are all oriented the same way.

3.29 MOS Transistors; Variable Channel Width - III-3, III-5

Purpose - These test structures measure the effects of various channel widths.

Verbal Description - This structure contains 12 ordinary type MOS transistors whose channel length is fixed at 0.3 mil. The width of the epi islands are 0.05, 0.1, 0.15, 0.2, 0.25, 0.3, 0.35, 0.4, 0.5, 0.7, 1.0, and 10.0 mil. All devices have common sources and gates.

3.30 MOS Transistors; Very Wide Channel - III-4, III-6

Purpose - These test structures are typical output devices.

Verbal Description - This structure contains two ordinary MOS transistors with very wide channels (55 mil). One transistor has a channel length of 0.3 mil and the other has a channel length of 0.2 mil. The devices have common sources and gates.

3.31 MOS Transistors; Edgeless - III-7, III-8

Purpose - These structures measure the effects of different channel geometrics on edgeless MOS devices.

Verbal Description - This test structure contains 20 ordinary MOS transistors of both types whose channel regions are not allowed to touch the edge of the epi islands. These transistors have sharp corners on the gates but otherwise are similar to those described in subsection 3.1. The following set of parameters are provided for the channel which is basically square.

Inside Periphery (mil)	Channel Length (minimum)
14.4	0.15
14.4	0.2
14.4	0.25
14.4	0.3
14.4	0.35
14.4	0.4
14.4	1.0
6.4	0.3
10.4	0.3
26.4	0.3

These devices have common gates and sources with the drain contained within the gate.

3.32 MOS Transistor; Variable Orientation - III-9, III-10

Purpose - These test structures measure the effects of orientation on transistor characteristics.

Verbal Description - This structure contains 50 ordinary transistors of both channel types with a channel region of 0.3 x 1.0 mil. These transistors are oriented differently with respect to each other with the following angular displacement:

0°	60°	95°	175°
2°	70°	100°	178°
5°	--	110°	180°
10°	80°	120°	
--	85°	135°	
20°	88°	150°	
30°	90°	160°	
45°	92°	170°	

All transistors have common gates and sources.

Line Drawing - The line drawings for these structure are presented as follows:

Structures III-1, III-2: figure 145

Structures III-3, III-5: figure 146

Structures III-4, III-6: figure 147

Structures III-7, III-8: figure 148

Structures III-9, III-10: figure 149

Halftone Photograph - The photomicrographs for these structure are shown as follows:

Structures III-1, III-2: figure 150

Structures III-3, III-5: figure 151

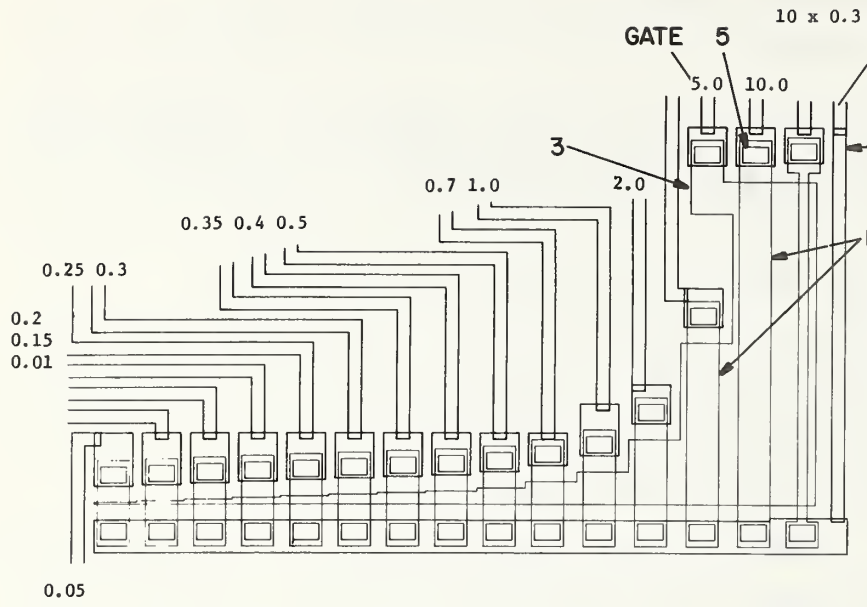
Structures III-4, III-6: figure 152

Structures III-7, III-8: figure 153

Structures III-9, III-10: figure 154

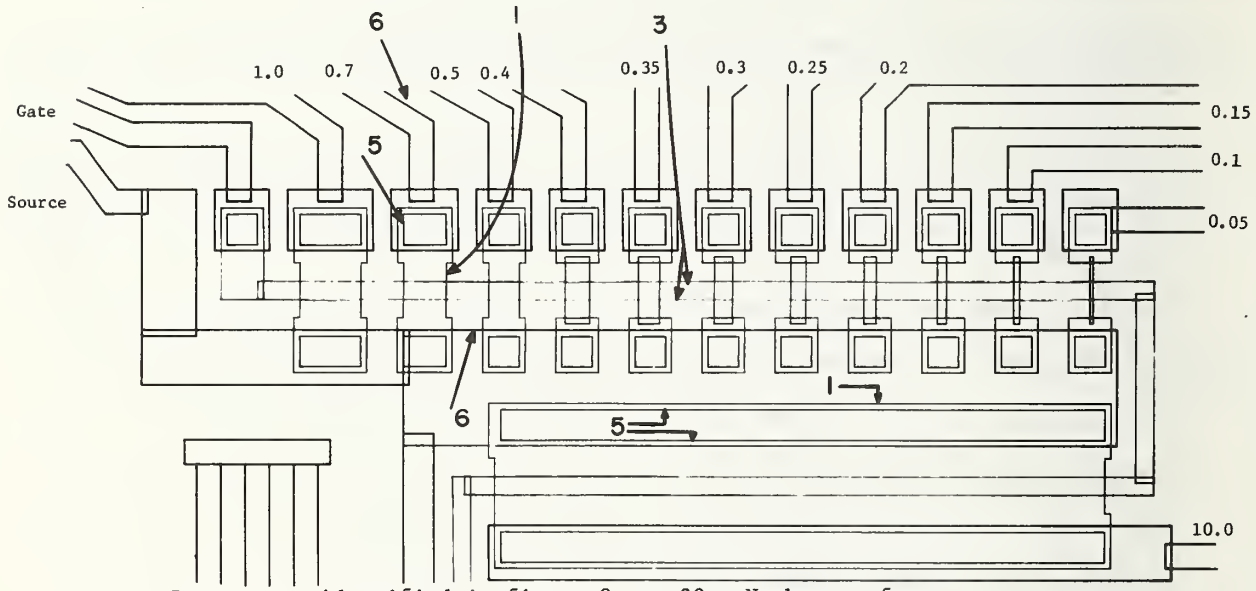
Electrical Access - These descriptions all have common sources and gates. The drain pads are unique to each device. It is more expedient to refer to the line drawings for identification of these drain pads than to list them all here.

Testing Method - These descriptions are all tested the same way and are all ordinary MOS transistors. Refer to subsections 3.1 and 3.13 for details. It is particularly important that one ensure that the gate is not short-circuited or conducting in any other device connected to the common source. Both erroneous gate voltages (especially if the short-circuit occurs between the transistor under test and the gate supply) and, of course, spurious currents can result. The devices in each of these descriptions are as nearly as possible identical to each other except for the designed-in differences. (Differences between



Layers are identified in figure 8, p. 23. Numbers refer to mask levels. Pads are 4.0 mil on a side. See section 2.1c, pp. 20-25.

Figure 145. MOS transistor; variable channel lengths, test structures III-1, III-2, computer line drawing.



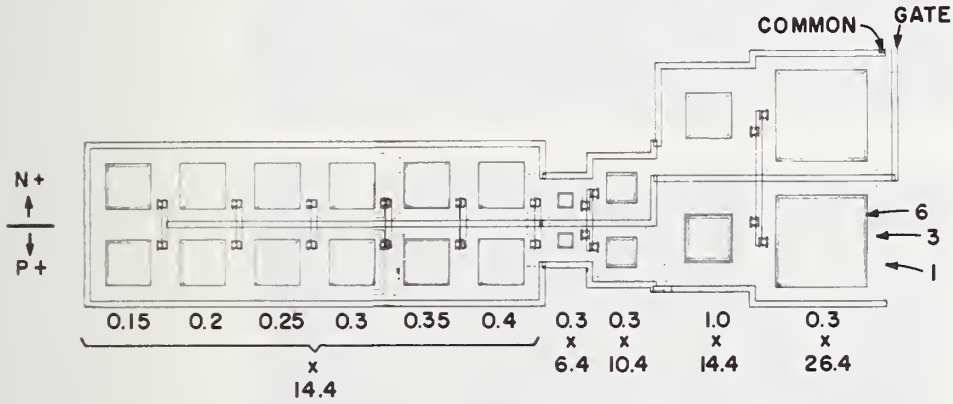
Layers are identified in figure 8, p. 23. Numbers refer to mask levels. Pads are 4.0 mil on a side. See section 2.1c, pp. 20-25.

Figure 146. MOS transistor; variable channel width, test structures III-3, III-5, computer line drawing.

nominally identical devices are addressed in the type II pattern.) By comparing the results obtained from these structures, one can obtain an empirical design curve for any of the geometrical features which are varied. These data are useful in designing the circuit intelligently and in arriving at the limit of applicability of existing models. The lithography is pushed to the limits obtainable with the currently available system. The same principles would apply of course to other systems of lithography.

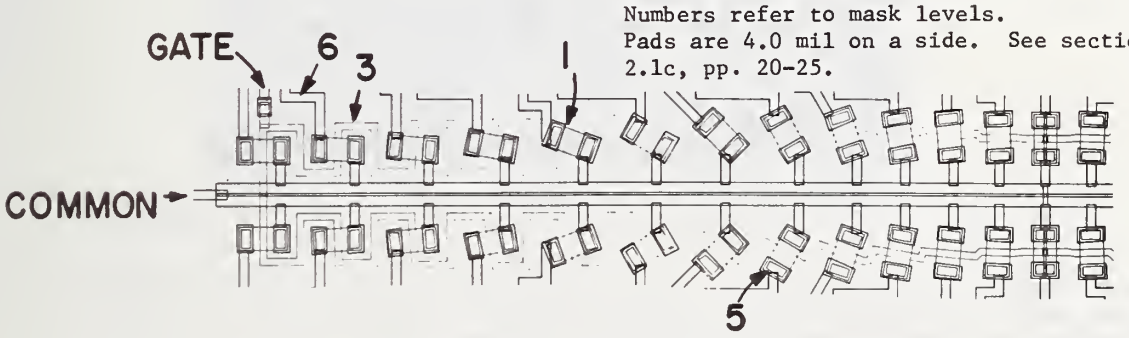
Special Equipment - None except as required for the individual transistor measurements.

Figure 147. MOS transistor; very wide channel, test structures III-4, III-6, computer line drawing.



Layers are identified in figure 8, p. 23. Numbers refer to mask levels. Pads are 4.0 mil on a side. See section 2.1c, pp. 20-25.

Figure 148. MOS transistor; edgeless, test structures III-7, III-8, computer line drawing.



Layers are identified in figure 8, p. 23. Numbers refer to mask levels. Pads are 4.0 mil on a side. See section 2.1c, pp. 20-25.

Figure 149. MOS transistor; variable orientation, test structures III-9, III-10, computer line drawing. Only half of the structure is shown.

Samples of Data - Only very limited data have been acquired from these structures. None will be presented here except a comment that drastic effects are seen when the channel is made too short (breakdowns drop and leakages increase, in particular), and some correlations with angular rotation have been noted particularly in the channel current under heavy inversion conditions.

Potential Pitfalls - The most serious pitfall of these structures is that they are not independent of each other. They have two common connections.

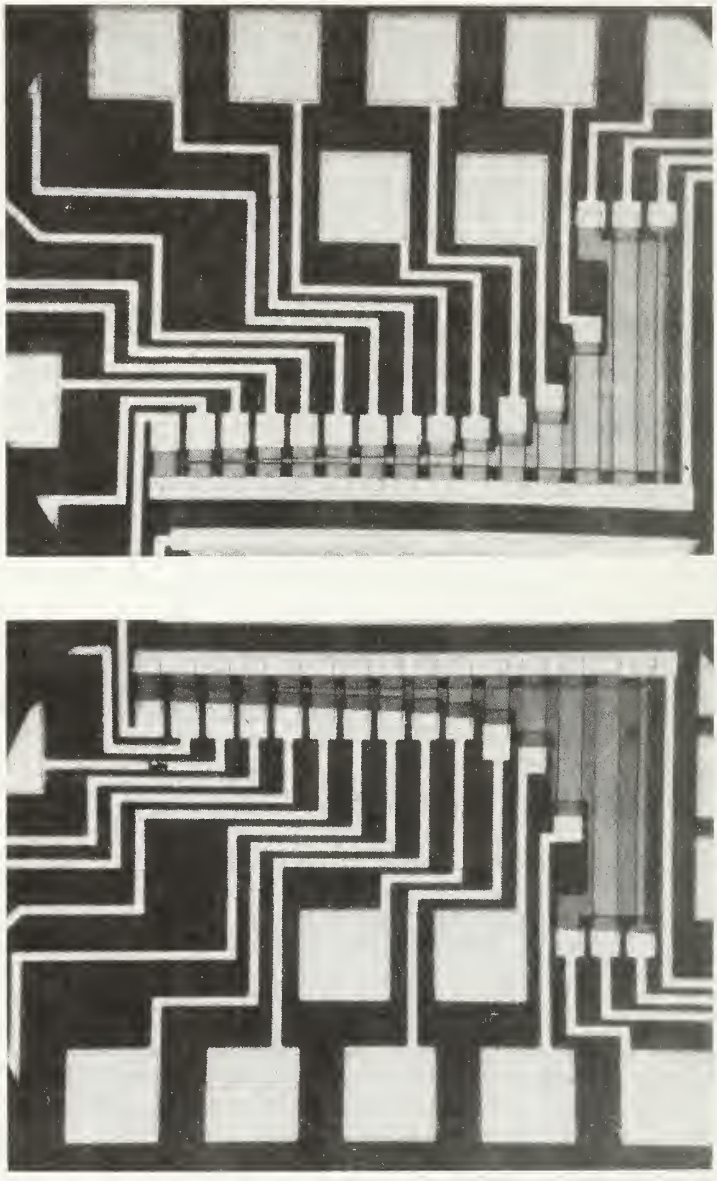


Figure 150. Photomicrographs, MOS transistor; variable channel lengths, test structures III-1, III-2.

Overall Usefulness - Clearly these descriptions provide the backbone for any model that may be developed with respect to the geometrical features of these transistors. They are indispensable in providing complete parametric data from the process.

Related Structures - All MOS transistors are related to these descriptions.

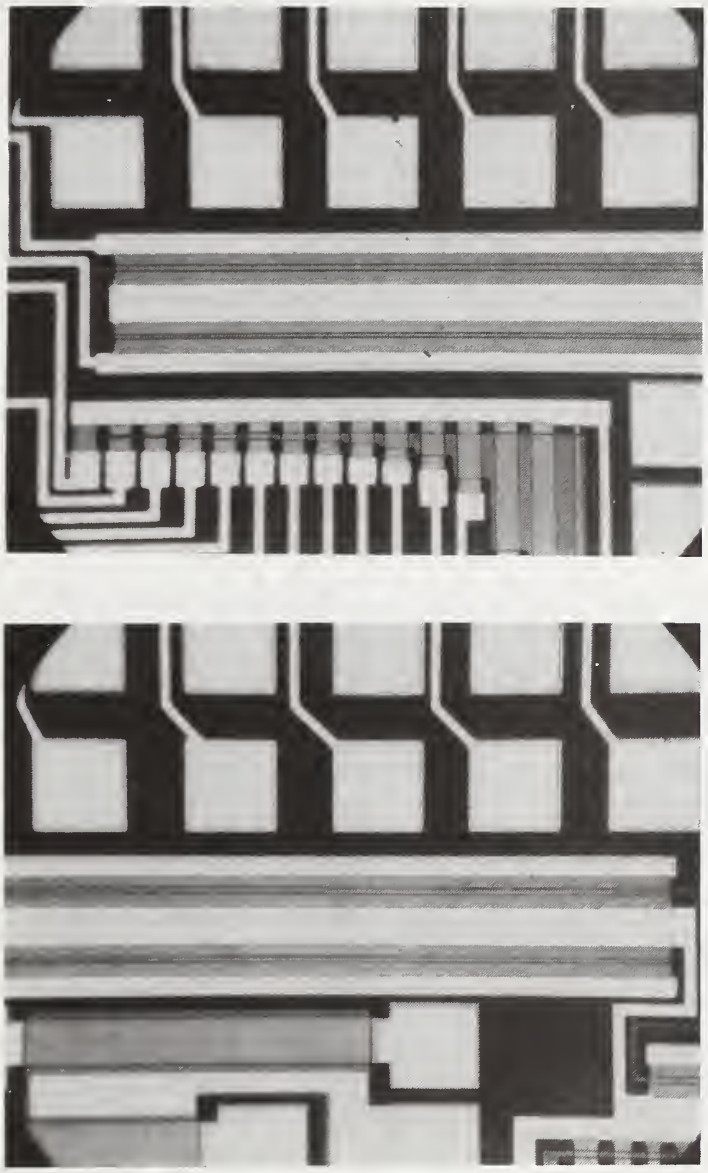
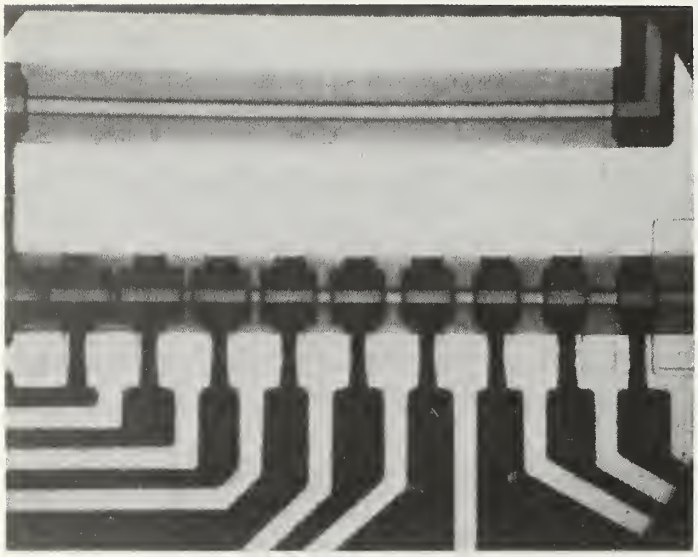
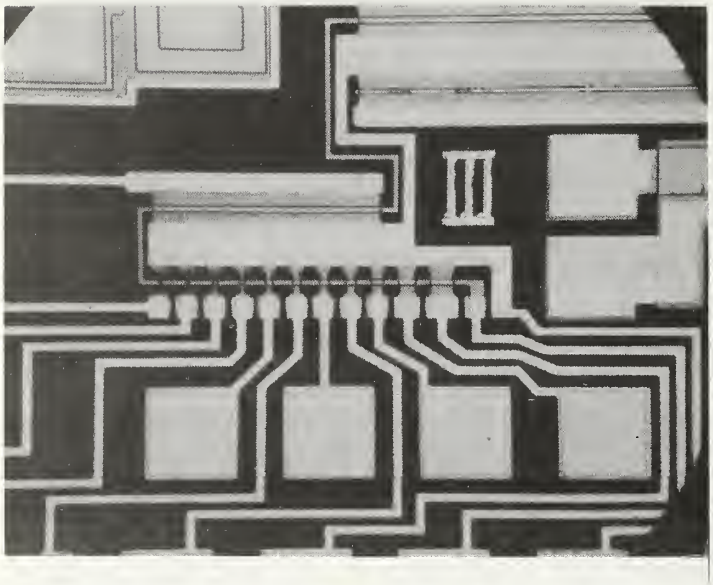


Figure 151. Photomicrographs, MOS transistor; variable channel widths, test structures III-3, III-5.



(a)



(b)

Figure 152. Photomicrographs, MOS transistor; very wide channel, test structures III-4, III-6. (a) Left end and (b) right end.

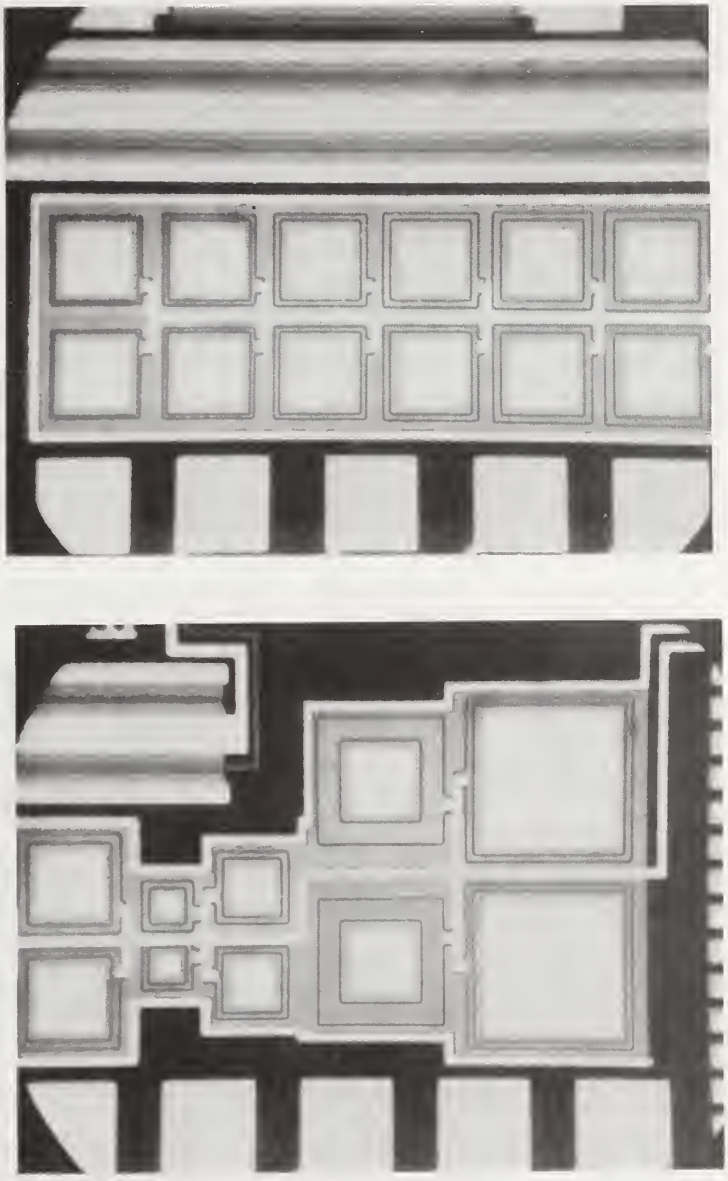
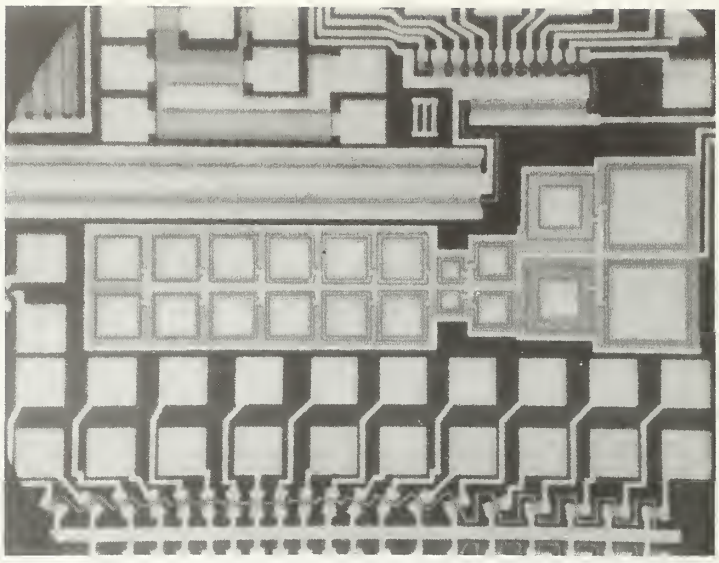
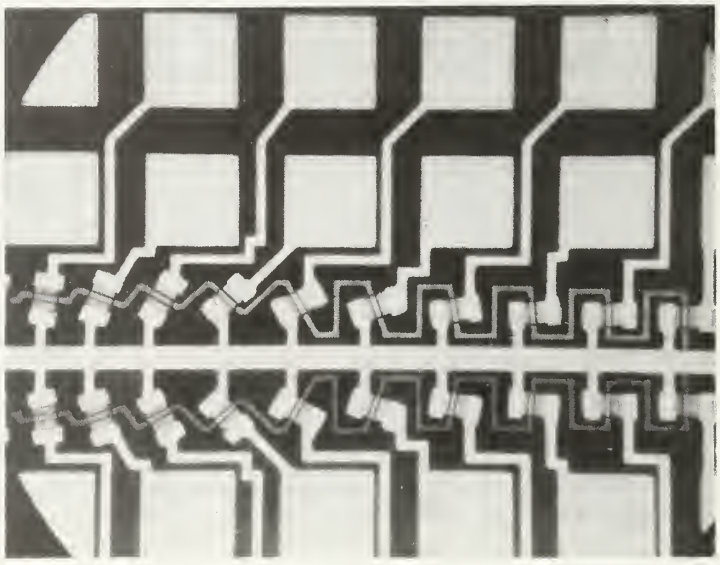


Figure 153.1. Photomicrographs, MOS transistor; edgeless, test structures III-7, III-8. (a) Variable channel length and (b) variable channel width.



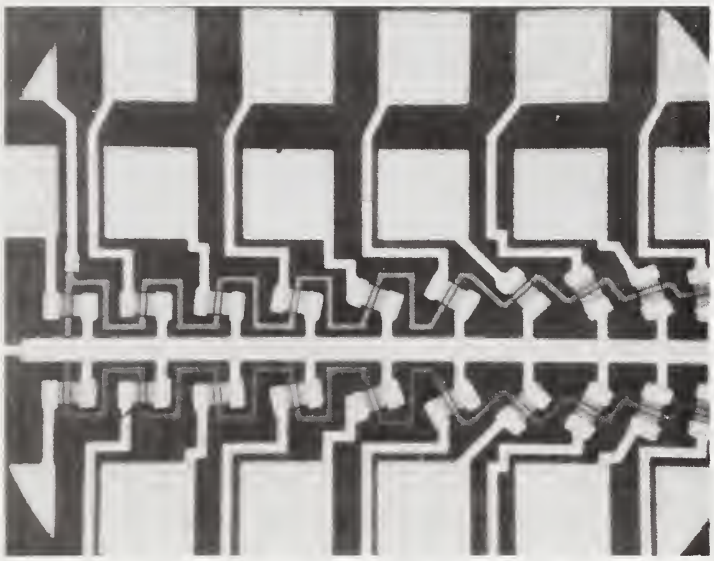
(c)

Figure 153.2. (Continued) (c) Entire structure.

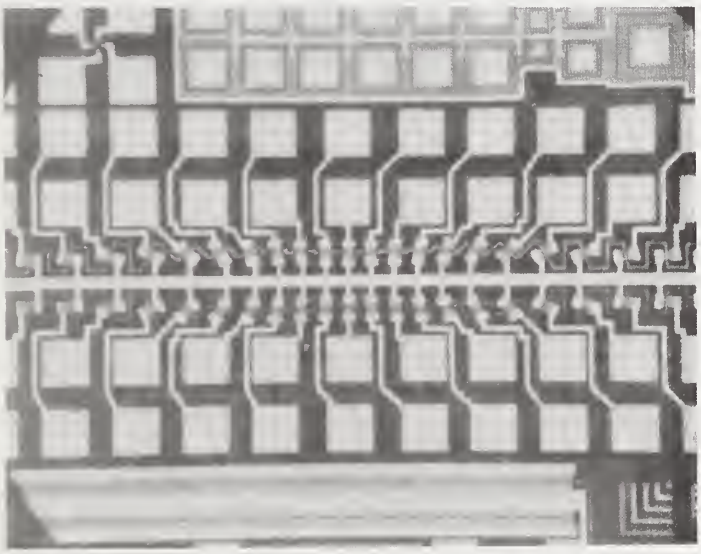


(a)

Figure 154.1 Photomicrographs, MOS transistor; variable orientation, test structures III-9, III-10. (a) Right end.



(b)



(c)

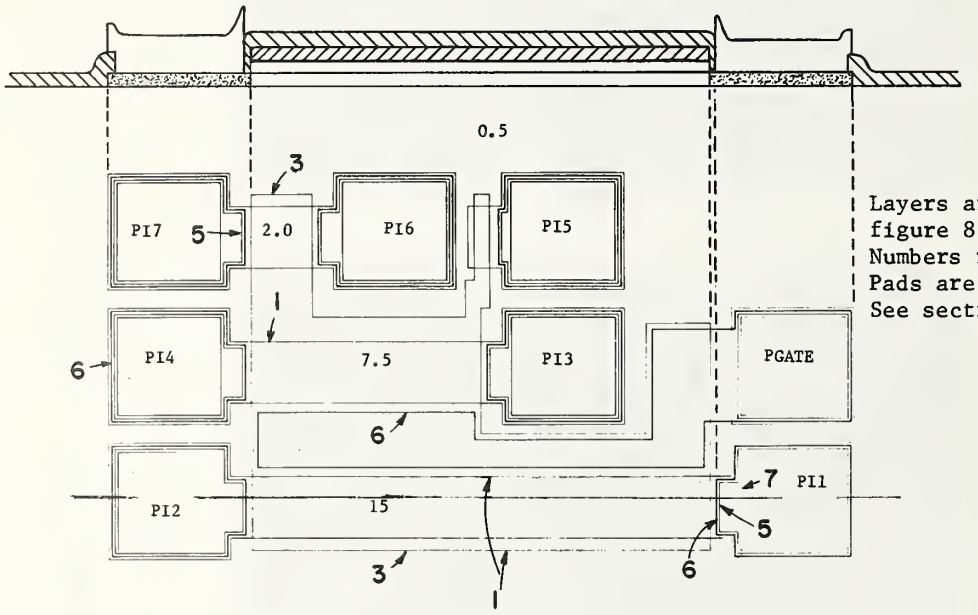
Figure 154.2. (Continued) (b) Left end and (c) entire structure.

3.33 Most Capacitor; Gate-Controlled Resistors - III-11, III-12

Purpose - These test structures measure material properties and interface properties.

Verbal Description - These structures are essentially MOS transistors with large channel areas. The active area is contacted at two points at either end of the gate except for the smallest channel area device which is contacted only on one side of the active area. All devices have 2.0-mil-wide active areas, and the following lengths are included: 15.0, 7.5, 2.0, and 0.5 mil. All devices have a common gate and completely independent current contacts.

Line Drawing - The line drawing for this structure is shown in figure 155.



Layers are identified in figure 8, p. 23.
Numbers refer to mask levels.
Pads are 4.0 mil on a side.
See section 2.1c, pp. 20-25.

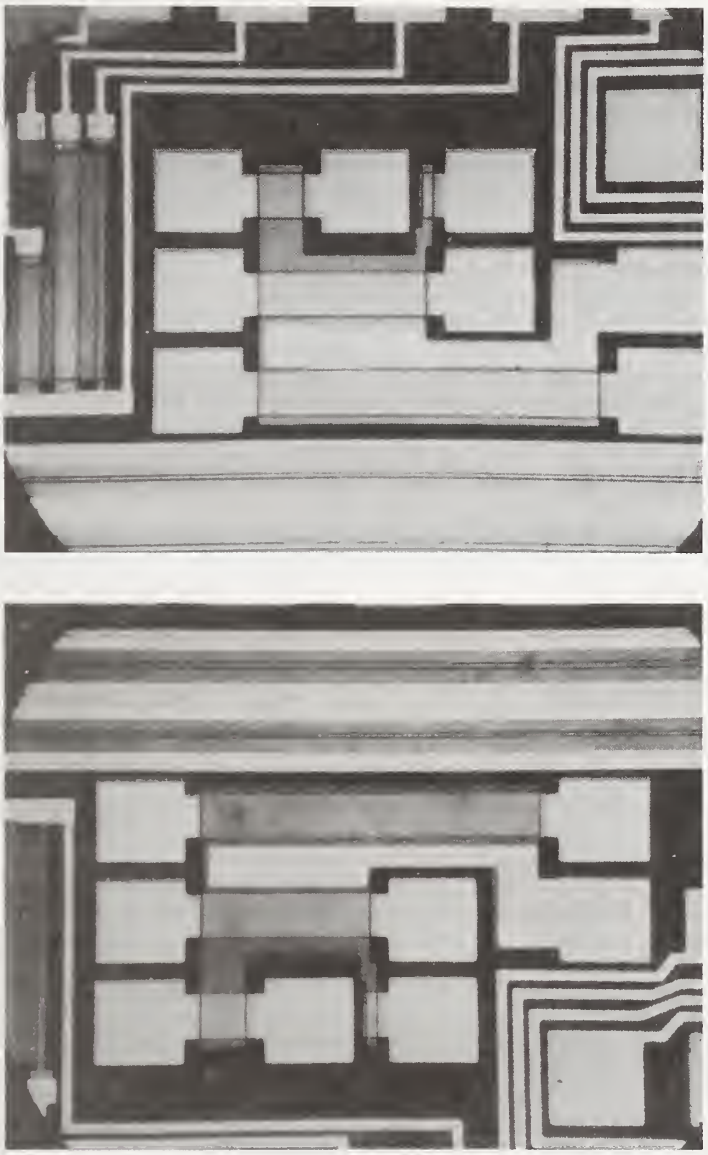
Figure 155. MOS capacitor; gate-controlled resistors, test structures III-11, III-12, computer line drawing and cross section.

Halftone Photograph - The photomicrograph for this structure is shown in figure 156.

Electrical Access - This description has eight access points. One is a common gate and the others are designated current contacts.

Gate	PGATE
15-mil device	PI1, PI2
7.5-mil device	PI3, PI4
2.0-mil device	PI6, PI7
0.5-mil device	PI5

Testing Method - These structures are included because they provide the ability to perform both I-V and C-V, G-V analysis on precisely the same silicon. The gate areas are made large enough so that accurate capacitance values are obtained. Since the capacitance is so markedly affected by the series resistance, provision for varying this resistance both by varying the gate field and by varying the length of the gate is provided. Furthermore, provision for actually measuring this resistance exists by measuring the resistance between the current contact at low applied voltages. A complete implementation of I-V, C-V, and G-V therefore



(a)

(b)

Figure 156. Photomicrographs, MOS capacitor; gate-controlled resistors, test structures III-11, III-12. (a) n^+ contacts and (b) p^+ contacts.

exists in the same structure. This structure is designed with the assumption that depletion will not proceed beyond the inversion point. This is usually sufficient to deplete most of the film for the doping levels and film thicknesses of greatest interest. If uniform depletion exists, one can obtain a resistivity profile of the film by comparing the measured resistance at various gate voltages. For example, changing the gate voltage by ΔV causes a change in the depletion width ΔW with a resulting change in the measured sheet conductance $\Delta\sigma$. The conductivity of the layer depleted by the change ΔV is therefore $\sigma = \Delta\sigma/\Delta W$. If W is known from the capacitance, a resistivity profile may be thereby obtained. Also, if the C-V curve can be related to the doping of the film, N, a mobility profile may also be obtained. This method has the advantage that it does not require Hall measurements on thin films (which as seen previously is difficult) but has the disadvantage that complete reliance on the C-V curve for both W and N exists. On the other hand, by using the previously published correction factors for SOS/MOS capacitors (ref. 14) accurate C-V curves may be obtained well into the region dominated by series resistance since the series resistance is

independently measured by the current contacts. Even with accurate C-V curves the relationship between the film doping and the capacitance may not correspond to the classical relationships because of the defective nature of the silicon. It is very difficult to determine the validity of the assumed relationships.

Special Equipment - Lock-in amplifiers to measure C-V and G-V are needed as described in subsections 3.24 and 3.25.

Samples of Data - This structure has not yet been tested in this form. Reference 14 shows some results on similar structures.

Potential Pitfalls - Here again the simple-minded concept of a physically perfect film can cause misinterpretation of the results. No fundamental pitfalls exist.

Overall Usefulness - Although this structure has not yet been tested, it has the potential to probe deeper into the film with accurate C-V data than any other structure previously published. Valid profiles at least of resistivity should be obtainable with less question concerning the validity of the measurement technique than other similar methods.

Related Structures - This structure is related to the gate-controlled bridge resistors I-5 and I-6 and to the various MOS capacitors on the pattern. It is basically a big MOS transistor.

3.34 MOS Transistor with Substrate Contact - III-13

Purpose - The purpose of this test structure is to measure effects of substrate (i.e., subsurface) potential.

Verbal Description - This structure is a variation of the devices of subsection 3.14. These devices are symmetrical in the channel with respect to the type of diffusion. The channel region is of a "cross" shape with the regions immediately adjacent to the source and drain having 0.6 mil width in one device (case A) and 0.3 mil in the other (case B). The center part of the channel widens to 1.0 mil in case A and to 0.5 mil in case B.

Line Drawing - The line drawing for this structure is shown in figure 157.

Halftone Photograph - The photomicrograph for this structure is shown in figure 158.

Electrical Access - This description has nine access points:

Common Gate	PGATE
n^+ Contacts, large device	PN+1L, PN+2L
p^+ Contacts, large device	PP+1L, PP+2L
n^+ Contacts, small device	PN+1S, PN+2S
p^+ Contacts, small device	PP+1S, PN+2S

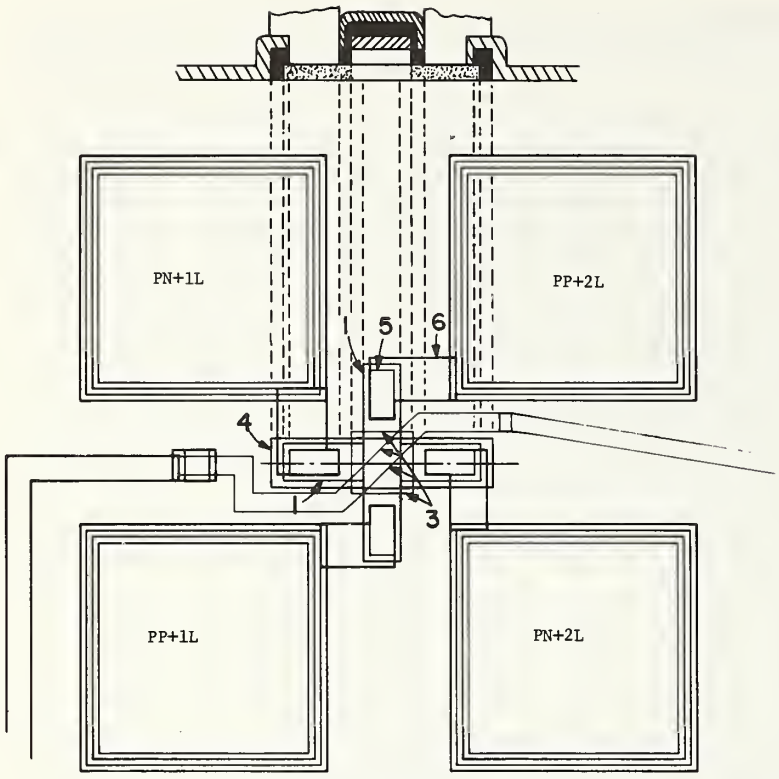
Testing Method - This structure can be tested with the same methods used for the structures of subsection 3.16. The primary difference with this structure is that it is symmetrical with respect to both n+ and p+ contacts. This structure can be used to compare both electron and hole transport through *the same silicon.* Electrons flow between the n+ contacts when the surface layer is n type, and holes flow between the p+ contacts when the surface layer is p type. Measurement between adjacent arms is essentially a gate-controlled diode structure. When the surface is neither accumulated nor inverted, all terminals are "off." This structure can provide some unique circuit functions.

The gate is allowed to extend over the corners of the intersection region so that n+ p+ junctions will not exist. Of equal importance is the method for obtaining electrical access to the gate. It is not clear that electrical contact can be easily made without placing a contact hole over the channel area. This is impossible for very small devices. The method chosen was to bring the access to the gate through the poly itself by allowing a 45° section to cross the edge at a corner as shown in the line drawing. This method allows considerable tolerance for misalignment as the photograph shows. The poly is misaligned to the silicon by nearly 0.2 mil yet the structure is still usable with only small errors due to the channel shape.

Although a probe card exists for this structure, the testing programs have not yet been written. Tests would proceed as in the individual structures listed below:

	Lc x Wc
n-Channel transistor	1.0 0.6
p-Channel transistor	1.0 0.6
Gate-controlled diodes	
Substrate contact transistors	
MOS capacitor	

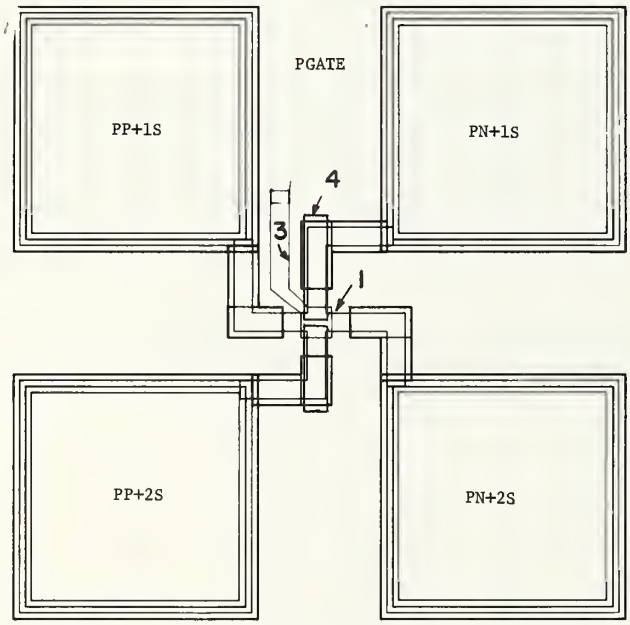
All of these functions are available on the same silicon, the same junction, etc so that detailed diagnosis of very complicated phenonema is conceivable. This is a super-integrated test structure.



(a)

Layers are identified in figure 8, p. 23.
Numbers refer to mask levels.
Pads are 4.0 mil on a side.
See section 2.1c, pp. 20-25.

PGATE



(b)

Layers are identified in figure 8, p. 23.
Numbers refer to mask levels.
Pads are 4.0 mil on a side.
See section 2.1c, pp. 20-25.

Figure 157. MOS transistor with substrate contact, test structure III-13, computer line drawing; (a) large device and (b) small device.

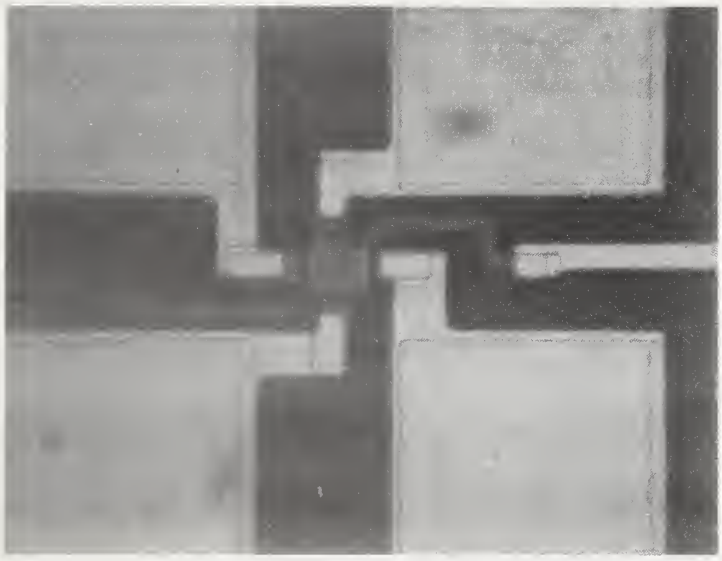


Figure 158. Photomicrograph, MOS transistor with substrate contact, test structure III-13 (larger).

Special Equipment - None except as required to test the individual components.

Samples of Data - No data have been acquired to date from this structure.

Potential Pitfalls - The sacrifice made for super-integration was loss of geometrical simplicity. Very complicated analyses are required to obtain exact solutions to the field and current lines. A built-in uncertainty on the order of perhaps 20% exists due to the geometrical complexity.

Overall Usefulness - When the structure is used to *compare* electron and hole transport on a relative scale, the geometrical factors are the same and therefore probably irrelevant. Other first-order tests such as the effect of grounding the "substrate" or other tests described in subsection 3.16 are also possible. In general this structure could be used on a production basis since a large quantity of "not too precise" information is available from a small area and changes from previous performance could be readily detected.

This device cannot compete with ordinary transistors as a circuit element if short channel lengths are required. On the other hand, it can produce unique switching functions at a relatively low gain. For low performance circuits some advantages may be gained from this structure as a circuit element.

Related Structures - The structures of subsection 3.16 are closely related to this description.

3.35 Contact Opening Test - III-14, III-15, III-16, III-17

Purpose - These test structures measure optimum contact geometry relative to a standard large contact.

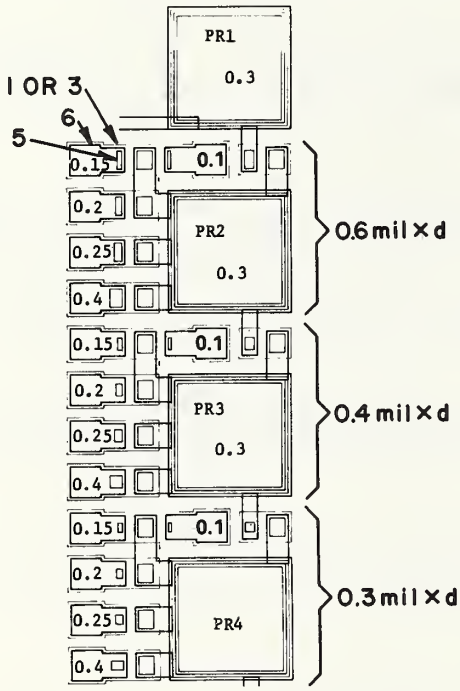
Verbal Description - This structure consists of 18 different sizes of contact opening. The closest side of the contacts to a standard sized contact is constant at 0.5 mil. The standard contact is 0.5 x 0.6 mil. The following sizes of contact are included:

0.3 x 0.1	0.4 x 0.1	0.6 x 0.1
0.3 x 0.15	0.4 x 0.15	0.6 x 0.15
0.3 x 0.2	0.4 x 0.2	0.6 x 0.2
0.3 x 0.25	0.4 x 0.25	0.6 x 0.25
0.3 x 0.3	0.4 x 0.3	0.6 x 0.3
0.3 x 0.4	0.4 x 0.4	0.6 x 0.4

All contacts are confined to the top of the silicon.

Line Drawing - The line drawing for this structure is shown in figure 159.

Halftone Photograph - The photomicrograph for this structure is shown in figure 160.



Layers are identified in figure 8, p. 23.
Numbers refer to mask levels.
Pads are 4.0 mil on a side. See section 2.1c, pp. 20-25.

Figure 159. Contact opening test, test structures III-14 through III-17, computer line drawing.

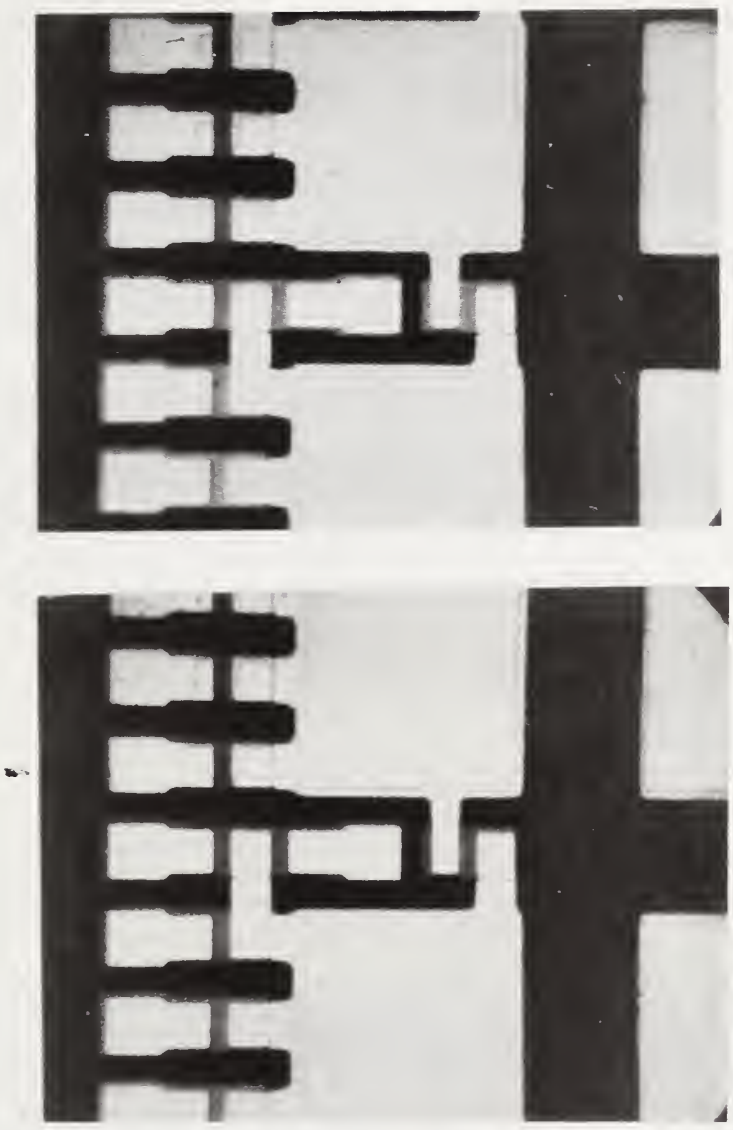


Figure 160. Photomicrograph, contact opening structures III-14 through III-17.

Electrical Access - This structure has 4 major access points and 15 minor access points. The major points are designated:

0.3 x 0.6	PR1
0.3 x 0.4	PR2
0.3 x 0.3	PR3
END	PR4

Each of the above pads is standard sized and is also connected to five other 0.5 x 0.6 contacts (except PR1). The minor access points are designated as follows:

0.6 x 0.1	P.6.1
0.6 x 0.15	P.6.15
0.6 x 0.2	P.6.2
0.6 x 0.25	P.6.25
0.6 x 0.4	P.6.4
0.4 x 0.1	P.4.1
0.4 x 0.15	P.4.15
0.4 x 0.2	P.4.2
0.4 x 0.25	P.4.25
0.4 x 0.4	P.4.4
0.3 x 0.1	P.3.1
0.3 x 0.15	P.3.15
0.3 x 0.2	P.3.2
0.3 x 0.25	P.3.25
0.3 x 0.4	P.3.4

These are all 1.0 x 1.0 mil pads for which the aluminum is not allowed to cross an island edge.

Testing Method - This structure is designed around a "standard" sized contact hole somewhat arbitrarily picked to be 0.5 x 0.6 mil. Other sizes of holes are placed with their edges 0.5 mil from the 0.6-mil edge of the standard hole on the same silicon island. The basic measurement is done between the large standard pads or between a standard pad and a small pad. The resistance between these pads consists of the probe resistance, the aluminum resistance, the contact resistance, and the resistance of the silicon. These measurements assume that the probe resistance and the aluminum resistance are at least constant. It is also assumed that the sheet resistance of the silicon is constant over the area of the structure. The basic tests performed are the two-terminal resistance tests described in subsection 3.2.

There are two basic methods of using the structure. In the first (and most important) method, a correlation between contacts which appear to be open and those which are actually electrically open is sought. It has been found that this correlation is far from perfect especially for small contact holes. The total resistance is very high when the opening is not complete. In the second mode a comparison is made of the total resistance between one set of contact holes and between another set having the dimension parallel to the standard hole the same as the first set. The difference in resistance is the difference in the contact resistance. By plotting the total resistance as a function of the variable dimension, we can estimate the values for other sizes of holes by extrapolation or interpolation. When the contact resistance departs from the trend as the dimensions are shrunk, the smallest usable size is established. These tests are primarily for engineering purposes and do not yield a specific contact resistance. We are therefore relatively uninterested in a detailed analysis. The data acquired here are again primarily used for creation of design charts and to test the processes' ability to make suitable contact to the silicon for various sizes of designed contact holes.

Special Equipment - One must have the ability to probe small pads in order to use all of this structure.

Samples of Data - No data have been acquired from this structure.

Potential Pitfalls - This structure uses a two-point method instead of a four-point method. It is therefore possible that probe resistance and aluminum resistance (particularly crossing a step) could be influencing the measurements. If these factors are serious, they will affect the largest holes most. Furthermore since the probing is manual, it is possible to probe directly on top of the 0.5 x 0.6 mil contact hole to obtain directly the probe and aluminum resistance. Therefore, with a small amount of additional effort these measurements can be made with confidence.

Overall Usefulness - The uses of this description were discussed under "testing method" above. This structure again addresses the bottom limits obtainable. It does not guarantee that many contacts of the smallest successful size can be made simultaneously. It is difficult to obtain computer-compatible data and large values of data due to the probing arrangement used. This arrangement was necessary because of the large number of pads required; there are 76 pads in all the structures using this description. Also, the hole sizes chosen are slightly larger than are usually available. The basic methodology of the structures is good and should not be changed. Within the context of this effort the only change recommended for this structure is that the 0.3-mil set of contacts be changed to 0.2 mil.

3.36 MOS Transistor; Narrow Channel - IV-1, IV-2

Purpose - These test structures measure properties of a large number of parallel or series devices.

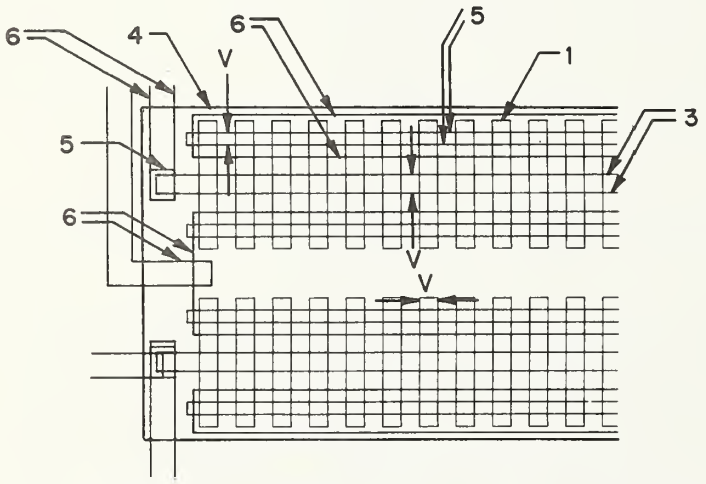
Verbal Description - This structure consists of many MOS transistors connected in parallel. The individual devices have 0.3 x 0.3 mil channel regions and 0.3 x 0.2 mil contact holes which cross the island edge. The transistors are separated from each other by 0.3 mil. All devices have the same source and gate connections. This structure has 249 transistors in two rows of 125 and 124 with drain connections to all in the 125 row and to each of 62 in the 124 row. The gate crosses all 249 epi islands with a tap at both ends and in the middle.

3.37 MOS Transistor; Wide Channel - IV-3, IV-4

Purpose - These test structures serve the same purpose as structures IV-1, IV-2.

Verbal Description - This structure is identical to structures IV-1, IV-2 except that the channel is 1.0 mil long and all 250 devices are connected with common gates, sources, and drains. The gate crosses all 250 islands with taps at both ends.

Line Drawing - Line drawings for structures IV-1 and IV-2 are shown in figures 161 and 162; line drawings for structures IV-3 and IV-4 are shown in figures 163 and 164.



Layers are identified in figure 8, p. 23. Numbers refer to mask levels. Level 1 islands are 0.3 mil wide. See section 2.1c, pp. 20-25.

Figure 161. MOS transistor; narrow channel, test structures IV-1 and IV-2, computer line drawing.

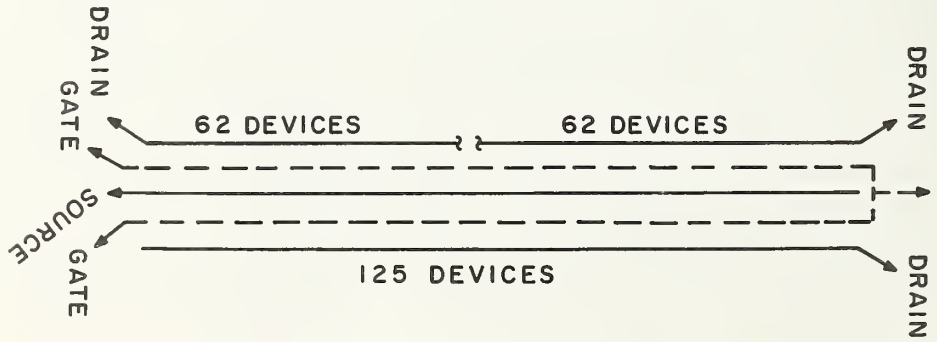
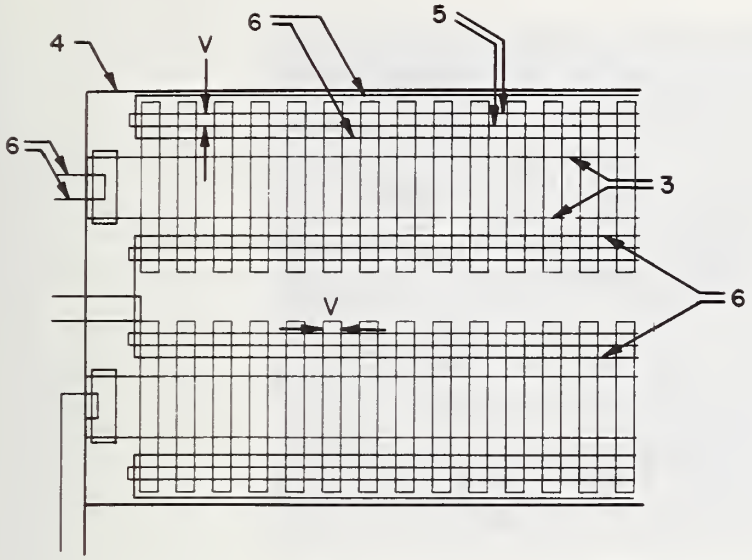


Figure 162. External connections, narrow channel.



Layers are identified in figure 8, p. 23. Numbers refer to mask levels. Level 1 rectangles are 0.3 mil wide. See section 2.1c, pp. 20-25.

Figure 163. MOS transistor; wide channel, test structures IV-3 and IV-4, computer line drawing.

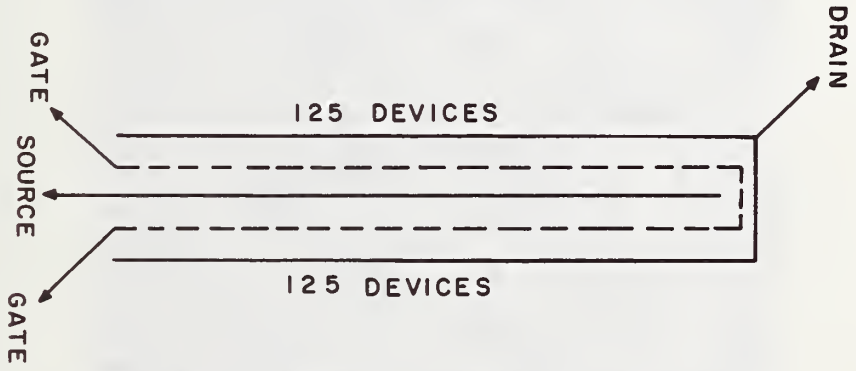
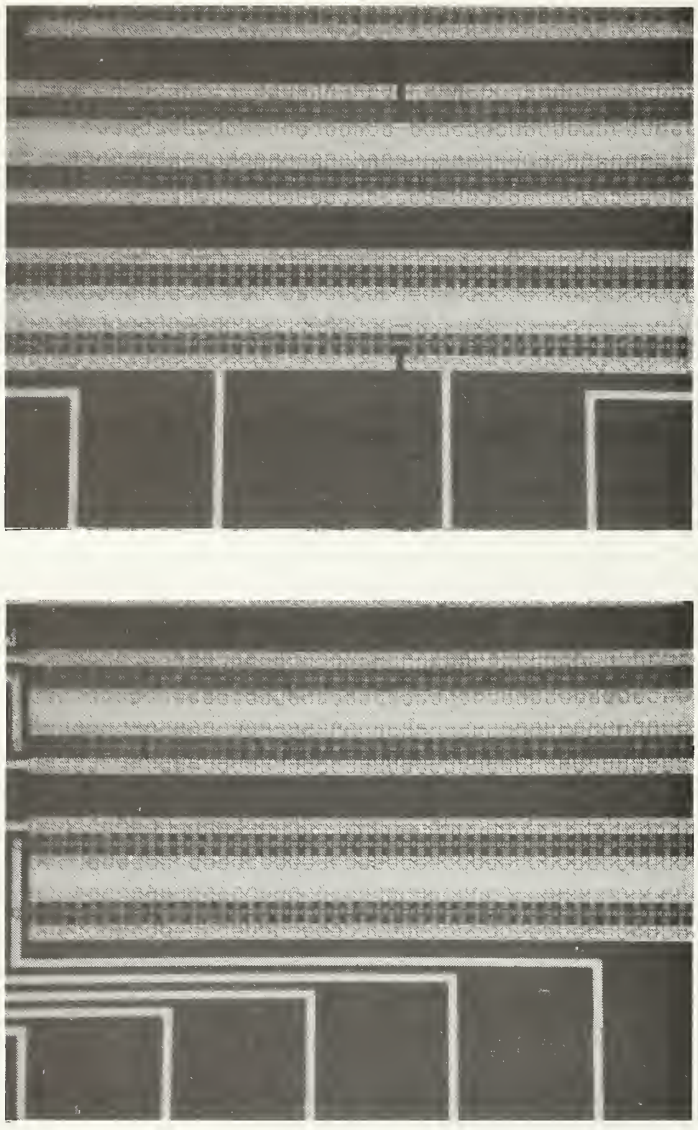


Figure 164. External connections, wide channel.

Halftone Photograph - Photomicrographs for structures IV-1 and IV-2 are shown in figure 165 and for structures IV-3 and IV-4, figure 166.

Electrical Access - Structures IV-1 and IV-2 have seven electrical access points designated:

125-device drain connection	P125D
62-device drain connection 1	P62D1
62-device drain connection 2	P62D2
End gate connection 1	PGATE1
Center gate tap	PGATE2
End gate connection 2	PGATE3
Source connection	PSOR



(a)

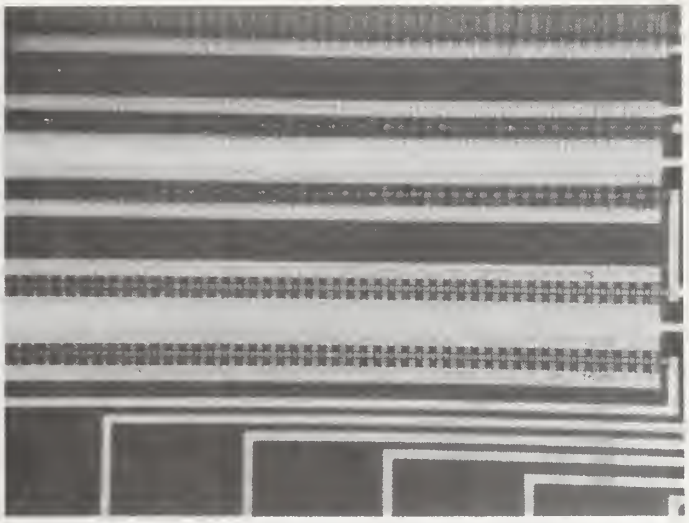
(b)

Figure 165.1 Photomicrographs, MOS transistor; narrow channel, test structures IV-1 and IV-2. (a) Center section and (b) left end.

Structures IV-3 and IV-4 have four access points designated:

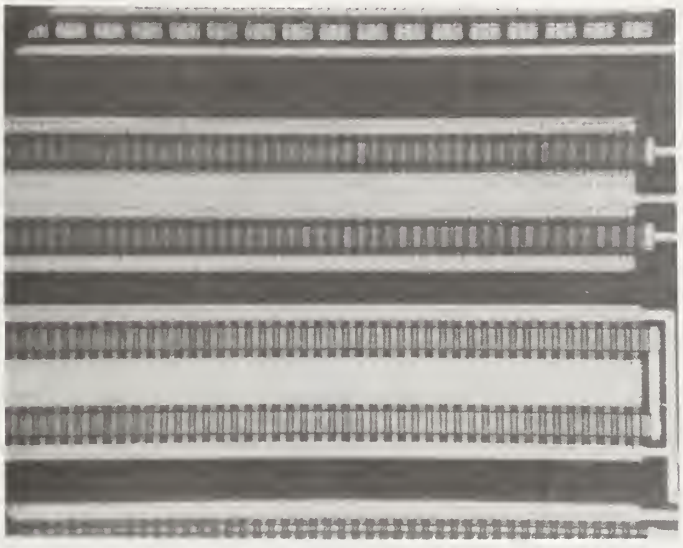
Drain connection	PDRN
Gate connection 1	PGATE1
Gate connection 2	PGATE2
Source connection	PSOR

Testing Method - These structures are tested basically as any other MOS transistor. There are, however, certain features of testing these structures which can provide unique information concerning the ability to use many devices in the same local area. The device must first be tested for initial suitability; this is done by testing for gate continuity and for gate current. The test for gate continuity also allows for calculation of properties of poly over many silicon steps. The gate current is measured by grounding all the source and drain pads and by measuring the current through all the gate pads. It is done after the



(c)

Figure 165.2. (Continued) (c) Right end.

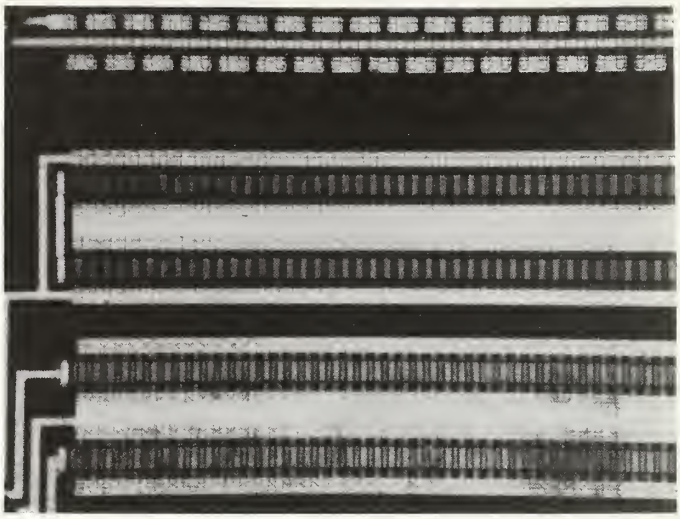


(a)

Figure 166.1 Photomicrographs, MOS transistor; test structures IV-3 and IV-4. (a) Right end.

gate continuity test in case the gate continuity test itself damaged the gate. The gate continuity is measured by measuring the resistance between the three different combinations of gate connection as shown in the flow chart. If the gate resistance is too high, testing is halted. The gate resistance and parameters indicating the ratios of the gate resistance are calculated. Notice that the doubling and halving, etc, done to calculate these linearity parameters are contained in the device itself not in the excitation. This is the essence of the philosophy for the type IV pattern. The device itself, using a significant number of elements, provides the excitation levels. For the gate the bilaterality parameters do not apply. However, they do apply for the transistor measurements.

The transistors of subsection 3.37 are tested the same as any three-terminal transistors except the gate continuity is used in addition to any other initial suitability test desired. These wide-channel devices are included so that the effects of the short channels may be separated from those of longer channels by comparison of the results of the two descriptions. The transistors of subsection 3.36 are tested primarily for leakage, drive current, and drain breakdown since these are the parameters most likely to be affected by the



(b)

Figure 166.2. (Continued) (b) Left end.

parallel connection of large numbers of devices. Detailed flow charts of these measurements will not be supplied since the measurements are the same as those for a single transistor. The parameters calculated are unique to this type of structure, however. The subscripts 621, 622, and 125 refer to the transistors with P62D1, P62D2, and P125D, respectively. The subscript TOT refers to a measurement with P62D1, P62D2, and P125D connected together as a single drain. The drive current is measured at a specified gate voltage and drain voltage as is the leakage current. The drain breakdown is measured by applying 62 times the current level desired for one device to P62D1 and P62D2 and 125 times this current to P125D. The total breakdown voltage is found by shorting P62D1, P62D2, and P125D together and forcing 249 times the single device current through the composite. These measurements are all done at the same specified gate voltage. This process produces the following set of data:

ID621
ID622
ID125
IDTOT
IL621
IL622
IL125
ILTOT
BVD621
BVD622
BVD125
BVDTOT

Since the breakdown voltages are not additive, this is their final form. We note that BVDTOT may be higher than any of the others due to walkout effects. BVDTOT is measured after these devices have been broken down once. The following parameters are calculated from the leakage and breakdown data:

For the drive current:

Duplicate linearity, DULIND = ID621/ID622

Twice linearity, TWLIND = (ID621 + ID622)/(ID621 * 2)

Bilaterality, BILIND = (ID621 + ID622)/ID125

Four times linearity, 4LIND = (IDTOT)/(ID621 * 4)

Current for one device, 1DLIND = (ID621 + ID622 + ID125)/249

Similarly for the leakage current:

Duplicate linearity, DULINL = IL621/IL622

Twice linearity, TWLINL = (IL621 + IL622)/(IL621 * 2)

Bilaterality, BILINL = (IL621 + IL622)/IL125

Four times linearity, 4LINL = (ILTOT)/IL621

Current for one device, 1DLIND = (IL621 + IL622 + IL125)/249

These parameters indicate the parametric integrity experienced on the average by a large number of devices. One can also define limits for these outputs as being indicative of success or failure. This can produce a type of "yield" data for certain types of failure. These descriptions are insensitive to open circuits in individual devices. Similarly they are insensitive to a single device being moderately different from the others. They are very good for determining when a single device is very much more conductive than the others. The main value, however, is in determining the possibility of predicting the *total* effects a large number of devices. For example, the total standby current of a CMOS memory could be reasonably predicted from these data.

Initial Parameters

Applied Voltage	VAPP
Maximum acceptable gate resistance for 125 gates.	RLIM

Flow Chart - The flow chart is shown in figure 167.

Samples of Data - A small data sample was automatically acquired from one wafer. The results from the gate continuity test and from the drive current and drain breakdown are presented.

The gate continuity data are shown in figure 168. Here (a) and (b) are the data from RGATE1 and RGATE2, respectively. These distributions are almost identical. The total resistance is seen in figure 168(a); these data are almost exactly the same as those in (a) and (b) except twice as large. This excellent agreement is reflected in figure 168(d) where TWLINR is plotted. The deviation from 1.000 is in the third decimal place and is probably due to the zero offset of the a-d system. Thus very good parametric integrity exists for this parameter. Things are not this good, however, for the drive current and the linearity parameters. At least $\pm$15% variation in the drive current and in the parametric integrity parameters are seen. It is not currently known whether this is typical of SOS in general or just of this specific wafer; a suspicion exists that this wafer may not be representative since the breakdown voltages shown in figure 168(n) through (q) are lower than usually seen. Here we see that nearly identical breakdown voltage exists for all testing conditions and that the lowest is seen for BVDTOT where all devices are simultaneously examined.

Potential Pitfalls - There are none if the devices are used as suggested.

Overall Usefulness - These structures provide an active structure which has a reasonable complexity but is easily testable. Unfortunately only certain types of failure are detectable with this structure, but these tend to be the ones most often suspected of causing problems. Visual analysis of failed structures provides direct feedback concerning the types and causes of failures. This method has been used to locate gate dielectric failures at the poly-epi island edge, for example. Also these structures may be repeated in order to cover a large area so that failures are more likely to occur. For example, in an RCA-funded program the structure of subsection 3.37 was repeated many times (in a separate mask set) to provide up to 11,750 transistors at a time as shown in Appendix B. This structure covers an area comparable to a large circuit.

If space permitted, a single device from the string could have been made available. This would allow better determination of the causes of failures. If this single device fails, the failure of the string is not due to random causes. Of course, single devices are available in other parts of the pattern.

Related Structures - All single MOS transistors and the poly-epi crossover structures I-10, I-12, I-13, I-14, IV-9A, and IV-9B are related to this description.

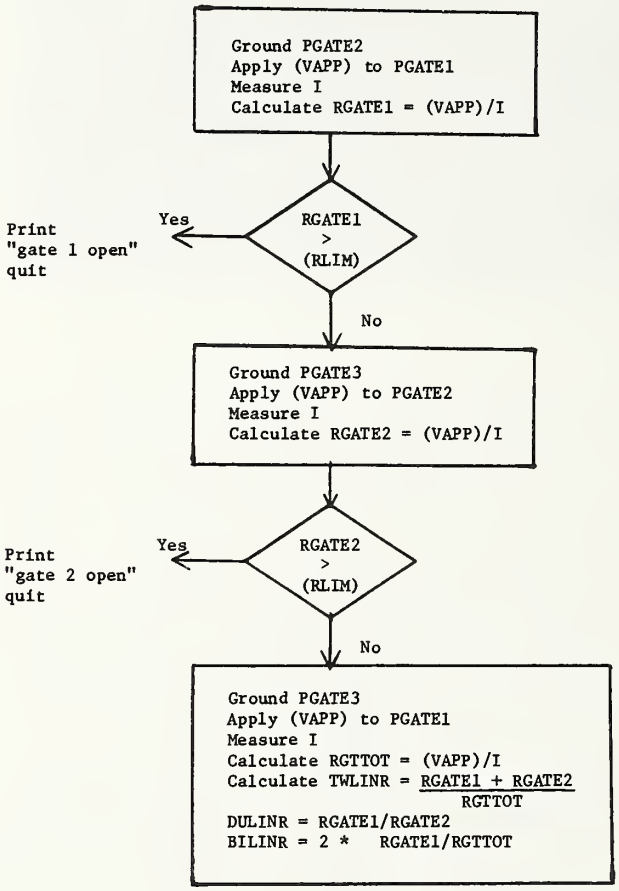


Figure 167. Flow chart for gate continuity.

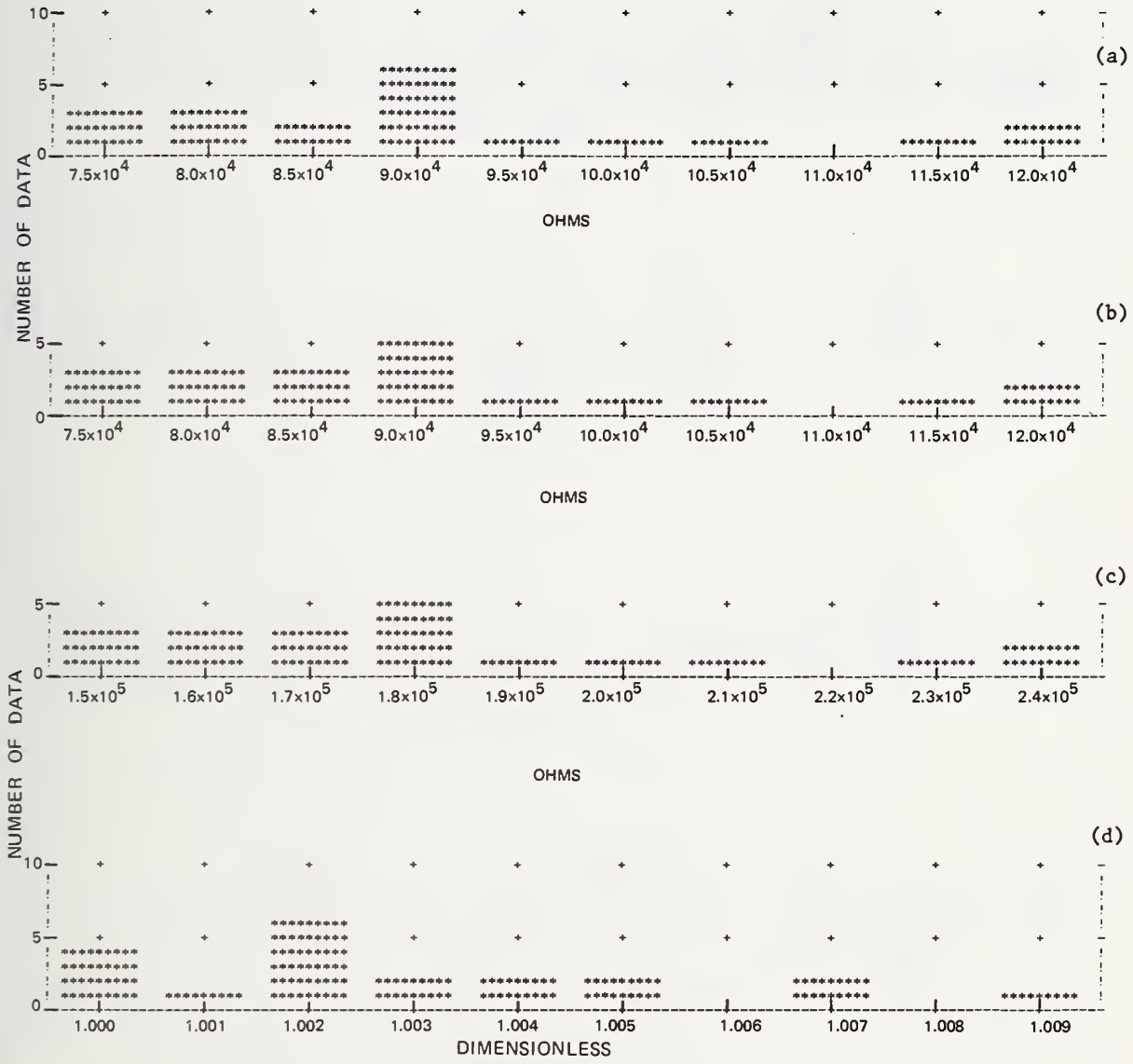


Figure 168.1. Histograms of data from a narrow n-channel structure. Scales are all self-determined.
(a) RGATE1 (ohm)
(b) RGATE2 (ohm)
(c) RGTTOT (ohm)
(d) TWLINR

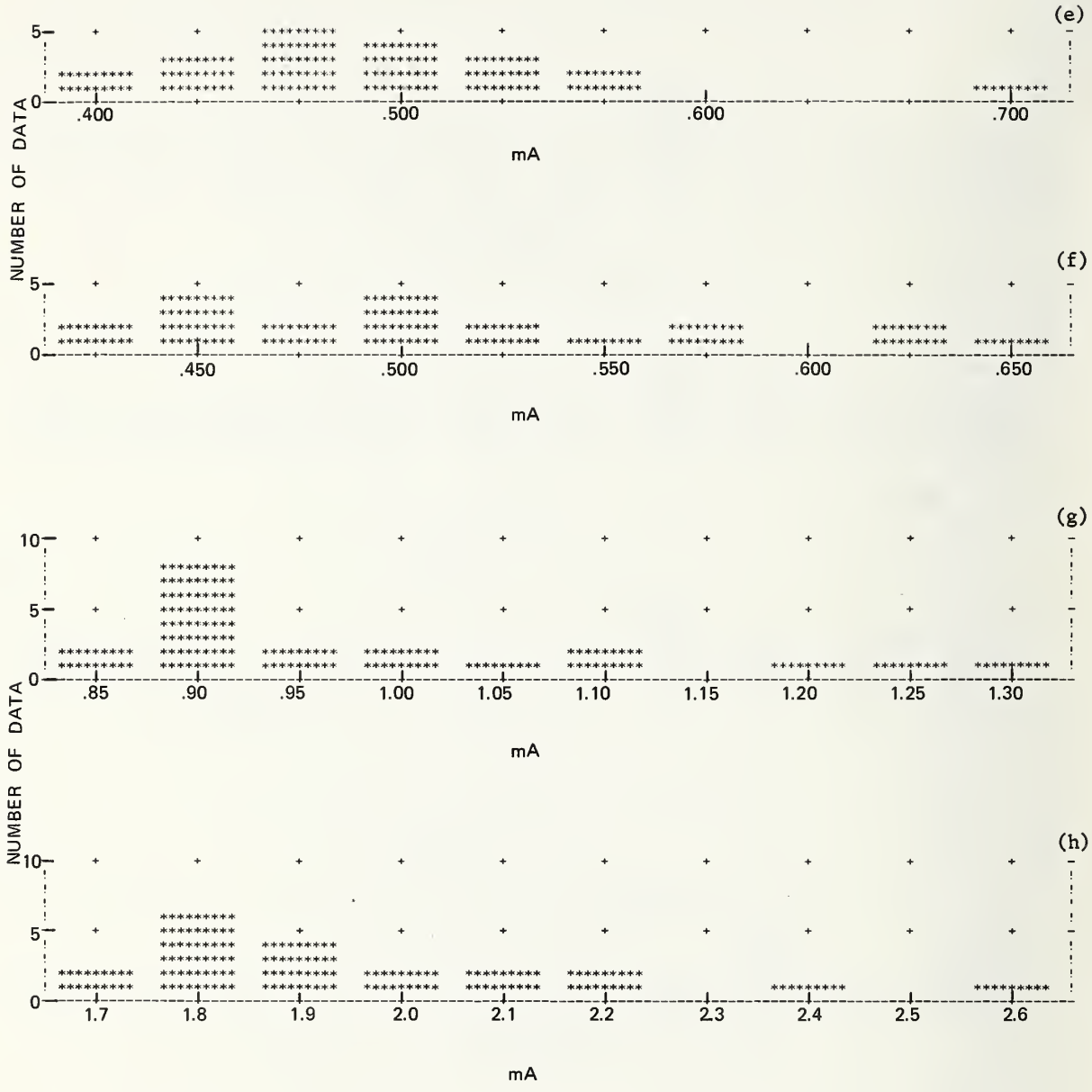


Figure 168.2. (Continued).
(e) ID621 (mA)
(f) ID622 (mA)
(g) ID125 (mA)
(h) IDTOTD (mA)

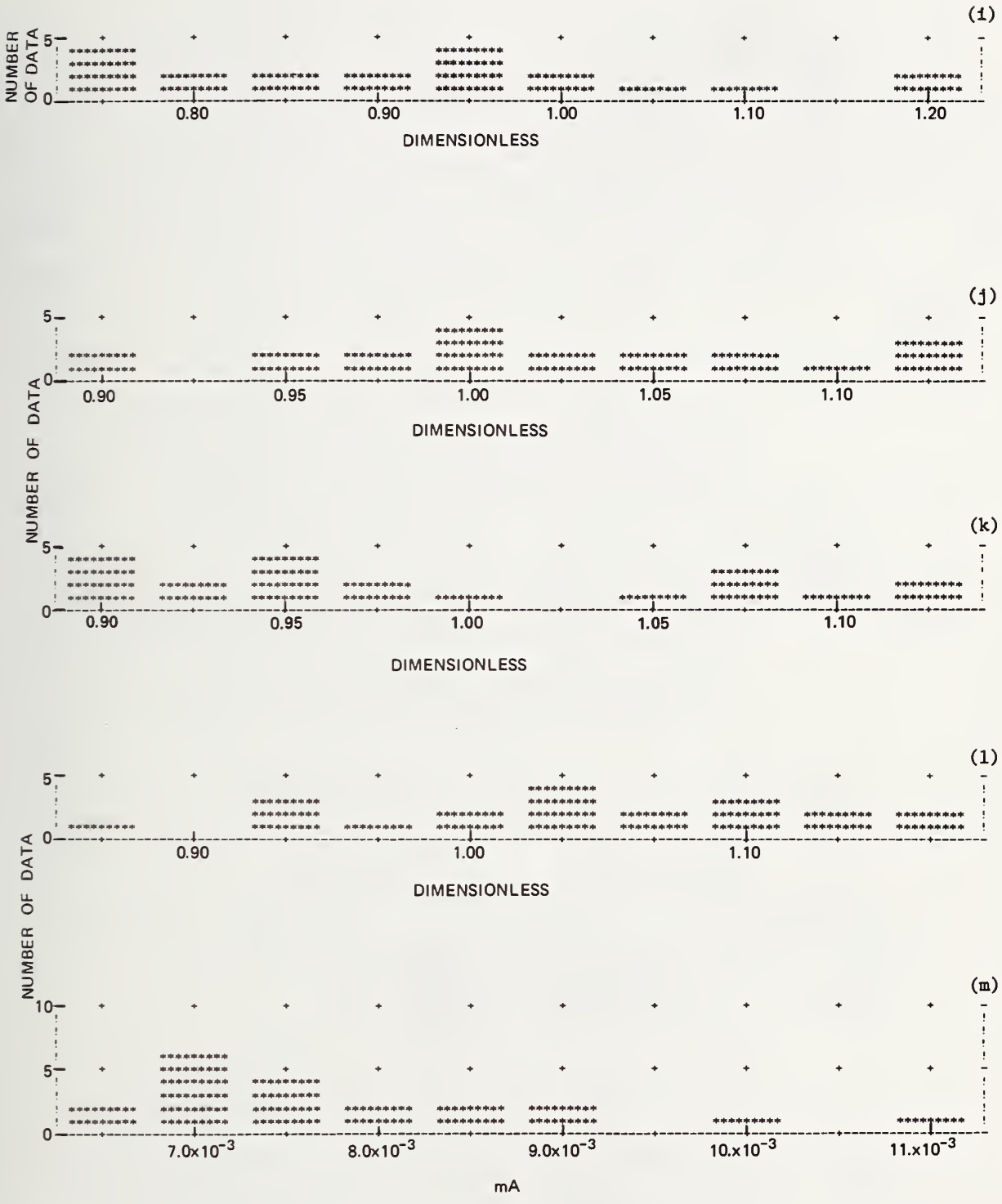


Figure 168.3. (Continued).
(i) DULIND
(j) TWLIND
(k) BILIND
(l) 4LIND
(m) 1DLIND (mA)

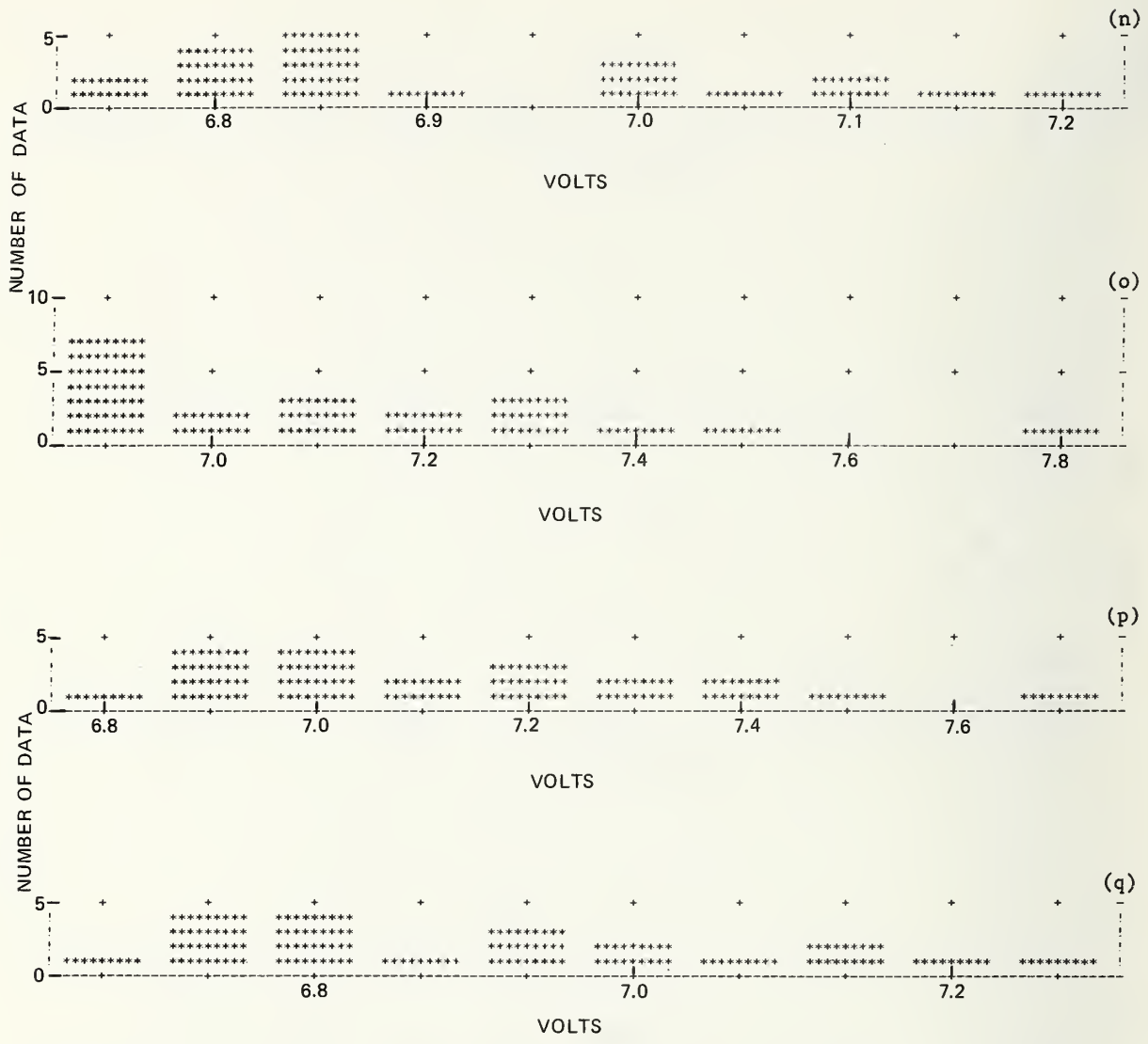


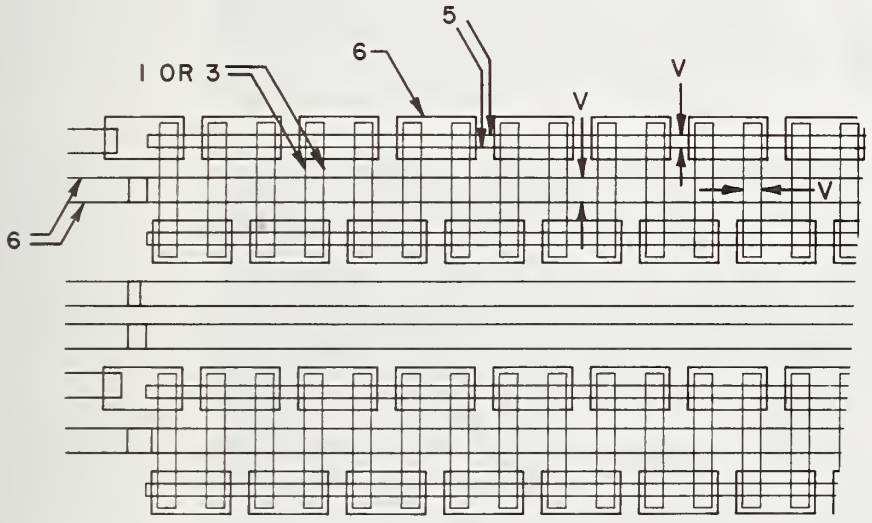
Figure 168.4. (Continued).
(n) BVD621 (V) (p) BVD125 (V)
(o) BVD622 (V) (q) BVDTOTL (V)

3.38 Contact; Crossover Test - IV-5, IV-6, IV-7, IV-8

Purpose - These test structures measure contact integrity on a variable large number of contacts and crossovers.

Verbal Description - This structure is a combination contact opening - diffused silicon resistance test and aluminum crossover test. The contact openings are 0.2 x 0.3 mil and the silicon bars are 0.3 x 2.2 mil long with an effective 4.66 squares per bar assuming no contact resistance. The structure is divided into two rows of 95 and 94 bars for a total of approximately 880 squares. The aluminum crossovers are 0.4 mil wide with taps at 46 and 48 on the 94 row and at the end of the 95 bar row. Contact taps are provided after 92 contacts and 96 contacts on the 94 bar row and after 190 contacts on the 95 bar row.

Line Drawing - The line drawings for this structure are shown in figures 169 and 170.



Layers are identified in figure 8, p. 23. Numbers refer to mask levels. Level 1 rectangles are 0.3 mil wide. See section 2.1c, pp. 20-25.

Figure 169. Contact-crossover test, test structures IV-5 through IV-8, computer line drawing.

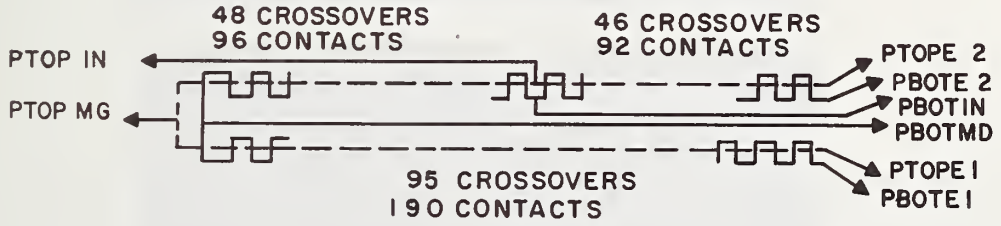


Figure 170. External connections, crossover test.

Halftone Photograph - The photomicrograph for this structure is shown in figure 171.

Electrical Access - This structure has eight electrical access points. Four of these are to the top conductor (the Al) and four of these are to the chain of silicon islands.

Top conductor end point 1	PTOPE1
Top conductor midpoint	PTOPMD
Top conductor intermediate point	PTOPIN
Top conductor end point 2	PTOPE2

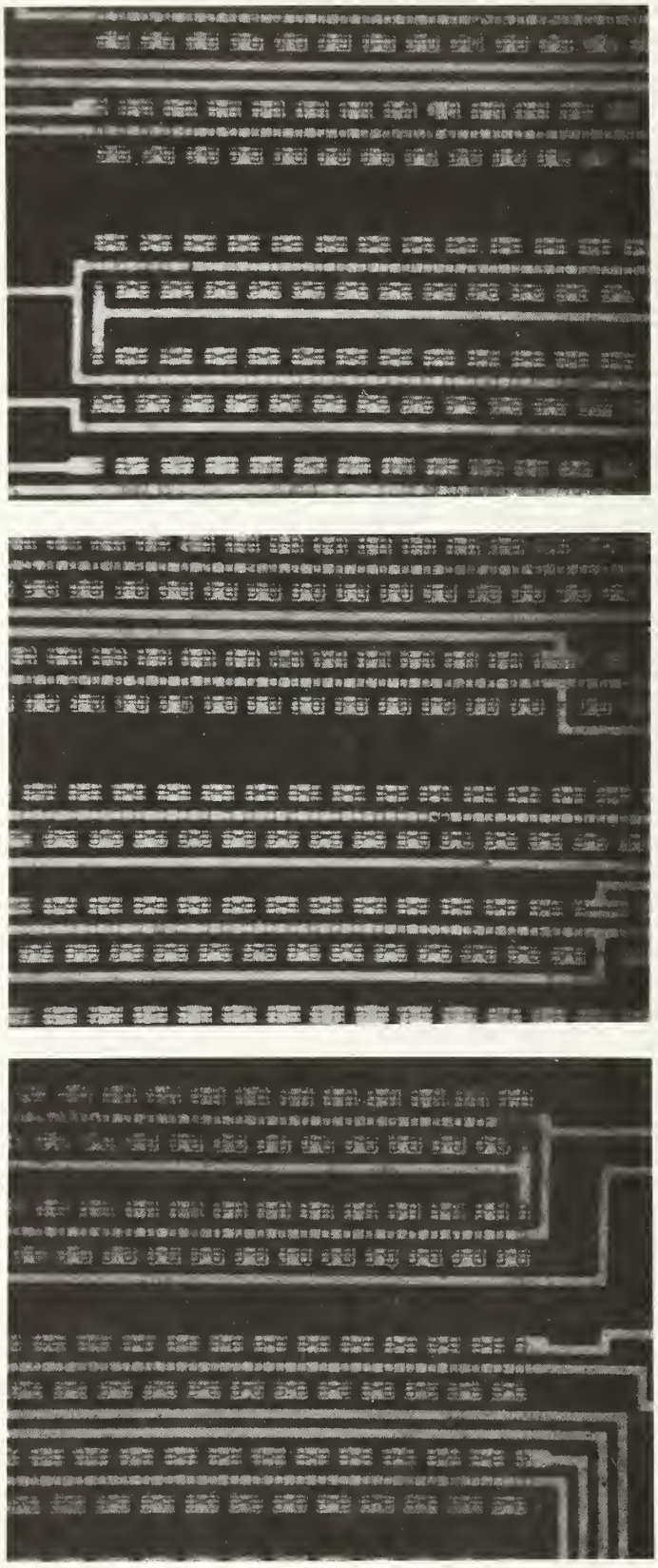


Figure 171. Photomicrographs, contact-crossover test, test structures IV-5 through IV-8. (a) Left section, (b) center section, and (c) right section.

End of island chain 1	PBOTE1
Midpoint of island chain	PBOTMD
Intermediate point of island chain	PBOTIN
End of island chain 2	PBOTE2

Testing Method - The general philosophy of testing crossovers was treated in subsection 3.3.

This basic philosophy holds here also, but additional insight can be gained with this structure if the problems are occurring only in a small number of devices. In other words the chances of finding a problem are greater here since there are many more devices. Successful operation of the structure means that there are no problems except possibly aluminum short-circuits between a few silicon bars. Unsuccessful operation of these structures, however, says very little by itself about the failures occurring. One can define a relative "yield" from a large number of measurements and this may provide an indication of the probability of success for this structure. This yield is of value only for relative comparisons and should certainly not be used to predict the yield for any other structure.

The first test is to measure the electrical separation between the top and bottom conductor. This is done by a single resistance measurement between all of the top conductor connections and all of the bottom conductor connections each connected together. This test is done first at a low voltage and next at a voltage at least as high as those to be used in the later tests. If this resistance is not sufficiently high, testing would normally be halted. There are situations, however, where this is of second-order interest and testing might proceed with the other conductors. If this is done, it must be recognized that continuity may appear to exist when in fact conduction is proceeding through the dielectric separating the two conductors.

The top metallization is used to provide information on continuity over steps. The absolute values of resistance may be measured to provide a comparison between samples, but the metal runs connecting to the steps are nearly as long as the metal runs over the steps and therefore contribute substantially to the total resistance. In this case open-circuits can be caused by opens in the metal over the steps and by opens in the metal not over the steps. It requires visual verification to determine which type of open is actually occurring. The structure provides the ability to determine (with diligent use of the microscope) whether a step coverage problem exists. The parametric output for top metallization is therefore given by the resistance between the pads:

PTOPIN, PTOPE2 = RT1

PTOPMD, PTOPE2 = RT2

PTOPE1, PTOPE2 = RT3

If any of these values are above a predetermined limit, an open is assumed. These resistance tests are accomplished using the TTRES2 approach described in subsection 3.3 where both a low voltage and an operating voltage are applied. The low voltage is applied to avoid burning out marginal connections. (This will be done during the operating voltage test.) If a continuing trend toward opens is observed as the number of crossovers is increased, one may suspect that something involving either the length of the metal runs or the number of steps crossed is causing the opens. As the area required for the structure increases, the chance of finding a defect increases. On the other hand, if a large number of open-circuits is found on one structure but not in another similar structure (with different silicon, for example), this would be a very strong indication of step coverage problems since the connecting lines should be similar in the two structures. This comparative power of nearly identical structures (the small-signal approach again) is another and perhaps the most important feature of these structures.

The lower portion is tested in a similar way to the top conductor by measuring the resistance between the following pins using first a low voltage and then an operating voltage.

PBOTIN	PBOTE2 = RB1
PBOTMD	PBOTE2 = RB2
PBOTE1	PBOTE2 = RB3
PBOTMD	PBOTIN = RB4

In this case the resistance measured is larger since transport through silicon is involved. There are several reasons for an open to occur here. In addition to the connecting lines mentioned above, closed contact holes and missing silicon can also produce opens. Again the microscope must be employed for diagnosis of the dominent problems, and "yield" predictions for other structures are unwise. Since the resistance is much larger in the silicon and contacts than in the connecting lines, parameters defining the ratios are again possible. We therefore define, in addition to the actual resistance, the following parameters:

DULINR = (RB4/RB1) * (46/48)

TWLINR = (RB1+RB4) /RB1) * (46/(46+48))

4LINR = (RB3/RB1) * (46/189)

If should be quite apparent from the above discussion that the primary uses of these structures are parametric in nature and not of a defect monitor nature. On the other hand these structures are very valuable for determining what type of defect causes the problem since the area occupied by a failed device is not too large to examine quickly and in detail using optical microscopes.

Since the tests performed here are basically resistance tests, and these have been described earlier, details of automatic testing will not be described here. The outputs have been described in this section.

Special Equipment - In addition to the relatively simple electrical equipment needed, a good quality microscope is strongly suggested for visual examination.

Samples of Data - These structures were tested on one wafer using a simplified testing procedure wherein only the resistances of the upper conductor and the lower conductor, and the isolation between conductors were measured. Each measurement used the total length of the structure and was done at a low and then at an operating voltage.

Figure 172 shows the results from structure IV-6 (n+ epi with Al top metal). The aluminum was measured with a low voltage of 1 mV and operating voltage of 50 mV. The bottom conductors were measured with a low voltage of 0.1 V and an operating voltage of 5 V. The isolation was measured with 0.1 and 9.9 V. No limits were used here to isolate good from bad.

It is particularly important to note the wafer position of the structure in order to interpret these data. The wafer position is noted by the symbol within the "box." These symbols correspond to data values listed below the box where the minimum values are noted. For example, in figure 172(a), the "B" category means any data above 0.198×10^2 while the "5" category means data between 0.1627×10^2 and 0.1686×10^2. Thus "B" category data are failures. Figures 172(a) and (b) show the upper conductor resistance. Notice that one negative value exists. This is due to the current reading being so low that the zero offset of the current meter caused a negative result. Most of the "bad" devices are on the extreme edges of the wafer and should not be considered as representative. On the other hand two hard failures are noted within the wafer. These are the "B's" in the third and sixth rows which are not on the wafer edges. By optical inspection these were found to be due to photoresist defects (one in the device and one in the connections).

CATEGORY MAP

```
-----+---
!0BBAAA !
!BA98766!
!B67B665!
+5554433+
!4444454!
!B224B47!
! B122B !
-----+---
```

(a)

LIN	CATEGORY	MINIMUM VALUE	POPULATION
	0	-.33333E.09	1
	1	.13904E 02	1
	2	.14496E 02	4
	3	.15089E 02	2
	4	.15681E 02	10
	5	.16273E 02	5
	6	.16865E 02	5
	7	.17457E 02	3
	8	.18049E 02	1
	9	.18641E 02	1
	A	.19233E 02	4
	B	.19825E 02	9

CATEGORY MAP

```
-----+---
!BBA755 !
!B986465!
!B87B563!
+8995455+
!6666567!
!B255B6B!
! B011B !
-----+---
```

(b)

LIN	CATEGORY	MINIMUM VALUE	POPULATION
	0	.19120E 02	1
	1	.19763E 02	2
	2	.20019E 02	1
	3	.20274E 02	1
	4	.20530E 02	2
	5	.20786E 02	10
	6	.21042E 02	9
	7	.21298E 02	3
	8	.21554E 02	3
	9	.21810E 02	3
	A	.22065E 02	1
	B	.22321E 02	10

Figure 172.1. Maps of crossover resistances (all values in ohms) for structure IV-6.
(a) Aluminum over n+ epi. V_{app} = 1 mV.
(b) Same as (a) with V_{app} = 50 mV.

The higher voltage test in figure 172(b) shows the same two failures but the negative value is removed because the system leakage caused the current meter to move to 0+. Also the resistance measurements are higher because of better accuracy of setting the higher voltage (50 mV compared with 1.0 mV). One device moved from a satisfactory state to an unsatisfactory state (right-hand edge of sixth row). This was probably caused by a marginal connection which failed at the higher current.

The lower conductor (n^+ epi in this case) is shown in figures 172(c) and (d). Here we see two classes of data (category 0 and category A) which deviate strongly from the main population. All of these structures except one (fifth row) were located on the periphery. We note that again one of the low voltage measurements changed completely at the higher voltage (second device - top row). In this case again an open was produced at the higher voltage. Visual inspection showed that the failures were nearly all due to open metal or missing silicon. Only one example was found where a contact hole was missing. The negative value has not been explained but is probably due to noise in the current meter.

CATEGORY MAP

```
-----+---
!AA4431 !
!A776132!
!8989854!
+7989864+
!0577074!
!A15A860!
! A002A !
-----+---
```

(c)

LIN	CATEGORY	MINIMUM VALUE	POPULATION
	0	.65019E 04	5
	1	.58720E 05	3
	2	.61011E 05	2
	3	.65594E 05	2
	4	.67885E 05	5
	5	.70176E 05	3
	6	.72467E 05	3
	7	.74758E 05	6
	8	.77050E 05	6
	9	.79341E 05	4
	A	.81632E 05	7

CATEGORY MAP

```
-----+---
!A04431 !
!A776142!
!7989854!
+7989864+
!0577074!
!A15A860!
! A002A !
-----+---
```

(d)

LIN	CATEGORY	MINIMUM VALUE	POPULATION
	0	-.22124E 10	6
	1	.60533E 05	3
	2	.62766E 05	2
	3	.67232E 05	1
	4	.69465E 05	6
	5	.71698E 05	3
	6	.73931E 05	3
	7	.76164E 05	7
	8	.78397E 05	5
	9	.80630E 05	4
	A	.82863E 05	6

Figure 172.2. (Continued). (c) Lower conductor (n^+ epi contacts) resistances V_{app} = 0.1 V.
(d) Same as (c), V_{app} = 5.0 V.
All values in ohms.

The isolation resistance is shown in figure 172(e) and (f). Here the failures are noted by category "0" since low resistances are the failures. The bad devices are largely confined to the edges but a significant population within the wafer was also found. This by far was the dominant failure observed for this structure. Many additional failures were noted at the higher applied voltage. One device changed from a bad state to a good state (right-hand device - top row) at the higher voltage. For this wafer the lower half was much worse than the upper half. Most of these failures were due to pinholes in the field oxide but not all could be accounted for visually.

When the upper and lower conductors are well isolated, the current flowing is well below the sensitivity of the current meter used here. Thus the values of isolation resistance shown are useful only for a lower bound on the resistance. These data are primarily used to determine the location of the poorly isolated devices. The higher values of resistance recorded at 9.9 V are due mainly to the use of the higher voltage in the calculation of resistance. The measured current was nearly the same at both 0.1 and 9.9 V.

CATEGORY MAP

```
-----+---
!800770 !
!8654542!
!2333333!
+0201101+
!0110011!
!1112010!
! 11010 !
-----+---
```

(e)

LIN	CATEGORY	MINIMUM VALUE	POPULATION
	0	-.10000E 12	13
	1	.62893E 09	14
	2	.87854E 09	4
	3	.11281E 10	6
	4	.13777E 10	2
	5	.18770E 10	2
	6	.26258E 10	1
	7	.28754E 10	2
	8	.31250E 10	2

CATEGORY MAP

```
-----+---
!300242 !
!0041456!
!2230113!
+0001700+
!0110007!
!1011010!
! 71010 !
-----+---
```

(f)

LIN	CATEGORY	MINIMUM VALUE	POPULATION
	0	-.63871E 11	19
	1	.34531E 10	12
	2	.56792E 10	4
	3	.10131E 11	3
	4	.12358E 11	3
	5	.16810E 11	1
	6	.23488E 11	1
	7	.25714E 11	3

Figure 172.3. (Continued). (e) Isolation resistance between aluminum and n^+ epi. V_{app} = 0.1 V.
(f) Same as (e), V_{app} = 9.9 V.
All values in ohms.

Potential Pitfalls - The most important pitfall in the use of this structure is to assume that it can be used to predict things which are dependent on defect densities. As a corollary one must not assume that the failures are due to any specific causes unless this is verified by optical or other physical examination. These structures should not be used to predict the "yield" of other structures although a relative measurement of the overall "yield" of these structures from different processes can provide an indication of the better overall process. This will only be true, however, if the process is bad enough to produce failures on these structures.

Overall Usefulness - This has been largely discussed in the sections above. It is clear that the sizes of interest to the process must be carefully chosen so that they represent minimum geometries of interest. These structures are most valuable as diagnostic tools for the effects of defects and for determining if the basic process was performed satisfactorily. They can also be used for determining the expected resistance from a long line of contact and silicon bars or metal runs such as might be found in a circuit. For example, the total aluminum resistance was measured to be ~20 ohm. This might not always be negligible.

Related Structures - The structures of subsection 3.3 are related to this structure as well as IV-9.

3.39 Continuity Test - IV-9

Purpose - This test structure measures total process electrical continuity.

Verbal Description - This structure combines all of the types of connections and crossover possible. All poly and epi is 0.3 mil wide and all contacts are 0.2 x 0.3 mil.

The following devices are connected in series:

- IV-9A, p^+ poly over (p^+ epi) - 25 islands
- IV-9B, p^- poly over (n^+ epi) - 25 islands
- IV-9C, p^+ poly contacts - 15 islands - 30 contacts ≈ 65 squares
- IV-9D, p^- poly contacts - 15 islands - 30 contacts ≈ 65 squares
- IV-9E, p^+ epi contacts - 15 islands - 30 contacts ≈ 65 squares
- IV-9F, n^+ epi contacts - 15 islands - 30 contacts ≈ 65 squares
- IV-9G, Al over p^+ poly - 25 islands
- IV-9H, Al over p^- poly - 25 islands
- IV-9I, Al over p^+ epi - 25 islands
- IV-9J, Al over n^+ epi - 25 islands

A tap is provided between each device.

Line Drawing - The line drawing for this structure is shown in figure 173.

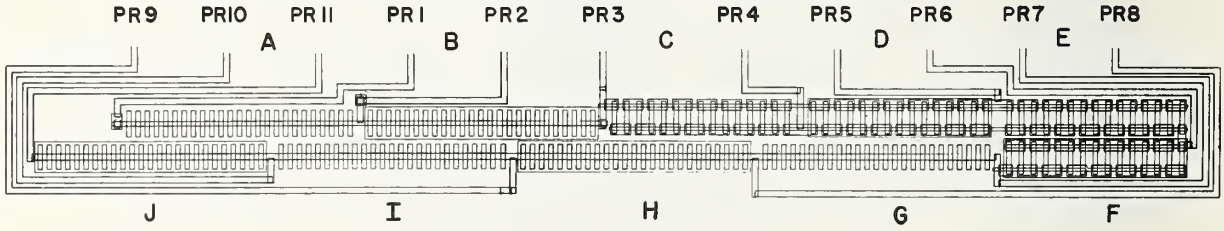
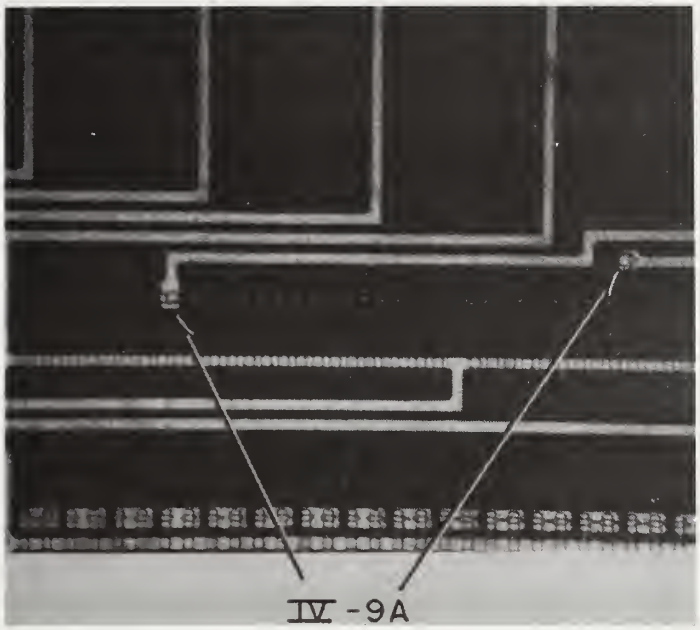


Figure 173. Continuity test, test structure IV-9, computer line drawing. The small rectangles are 0.3 mil wide.

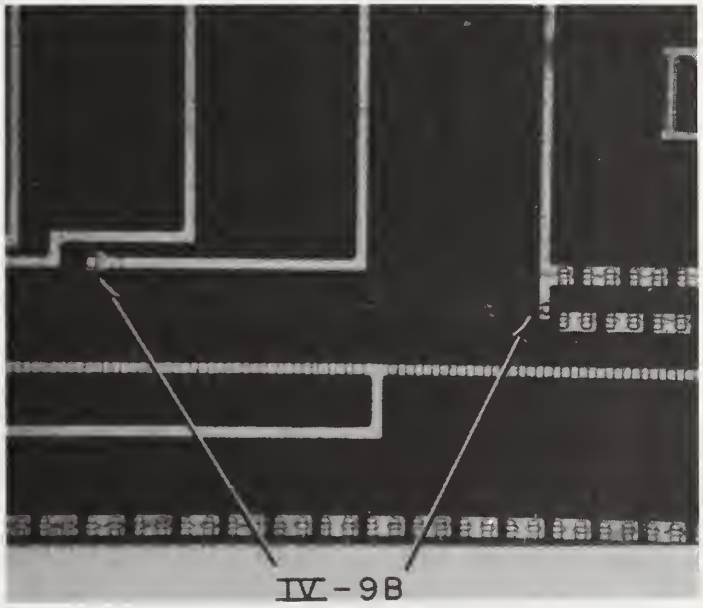
Halftone Photograph - The photomicrograph for this structure is shown in figure 174.

Electrical Access - This structure has eleven electrical access points:

END-A	PR1
A-B	PR2
B-C	PR3
C-D	PR4
D-E	PR5
E-F	PR6
F-G	PR7



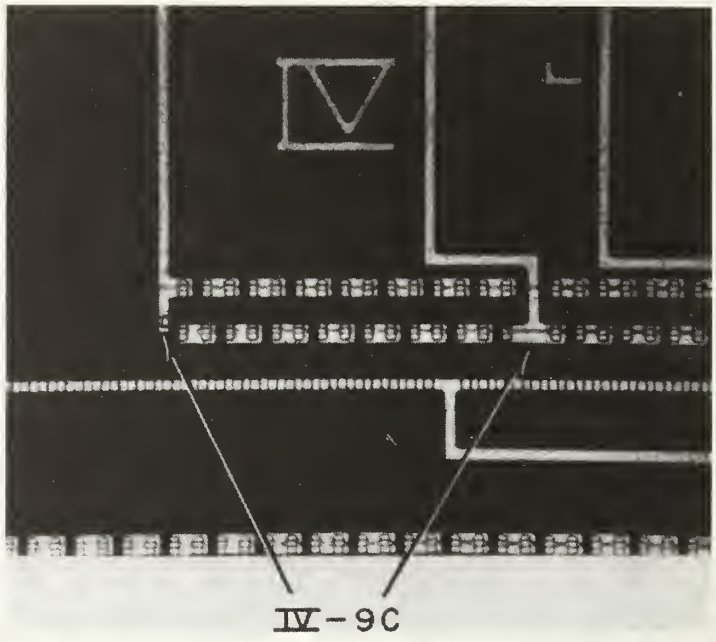
(a)



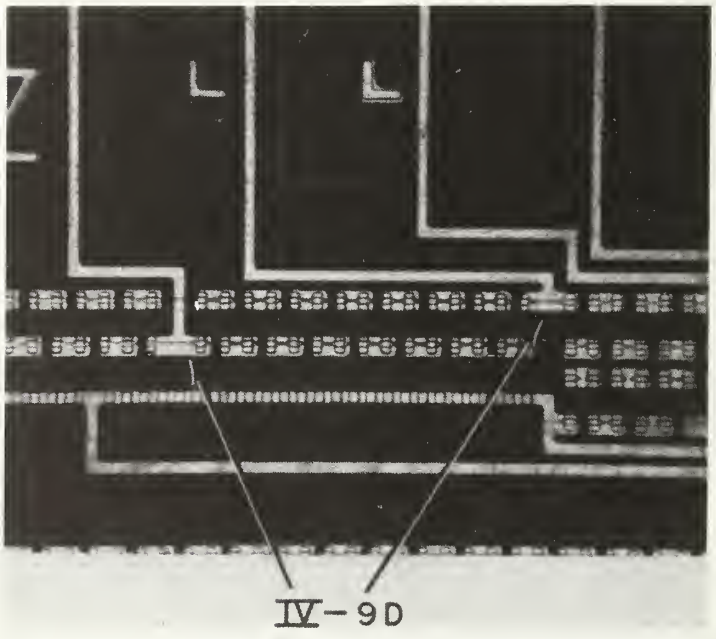
(b)

Figure 174.1. Photomicrographs, continuity test, test structure IV-9,
(a) p+ poly over epi steps and
(b) p⁻ poly over epi steps.

G-H	PR8
H-I	PR9
I-J	PR10
J-END	PR11



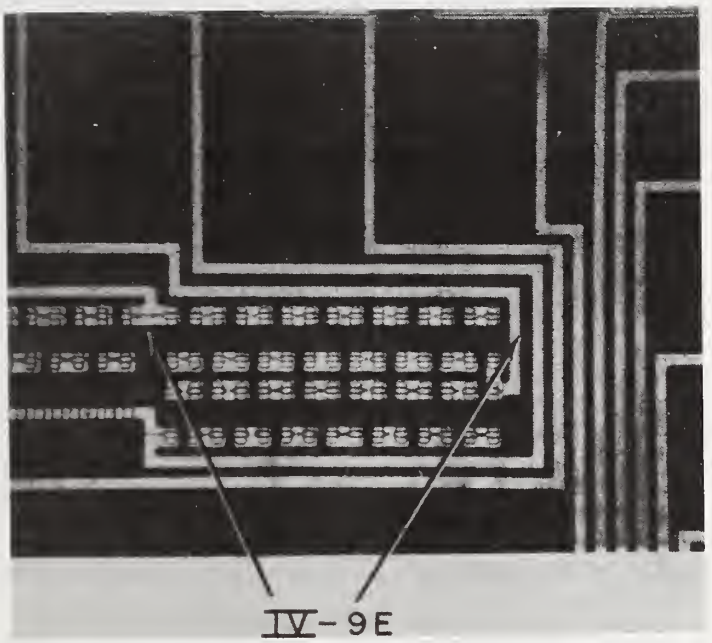
(c)



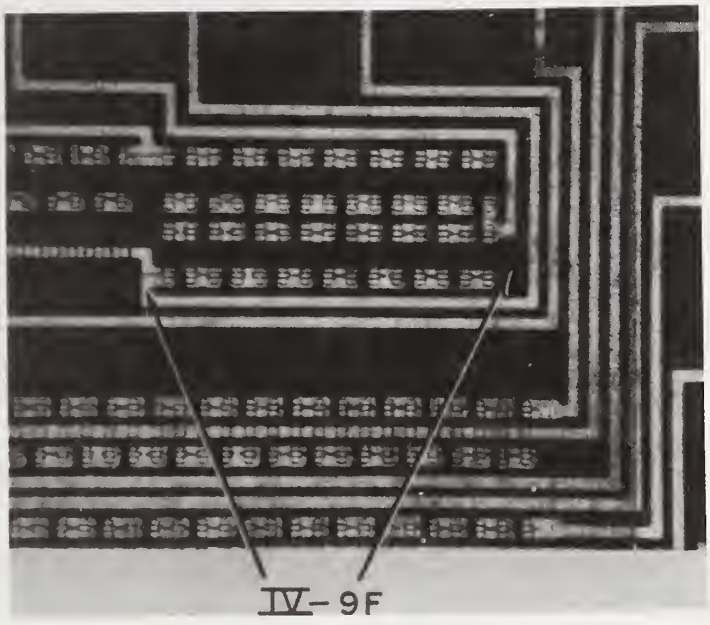
(d)

Figure 174.2. (Continued). (c) p+ poly contacts and (d) p^- poly contacts.

Testing Method - This structure is tested precisely the same way as described in subsection 3.18. There is a greater chance of finding a failure here since more devices are involved. It is especially important that visual confirmation be performed on failures before concluding a failure mechanism since there are many causes for opens other than the obvious ones being tested for. If many structures fail at the same test, there would be reasonable cause for suspecting the "obvious" as the failure. The main purpose of this structure is to determine if weaknesses in the connectivity exist for a moderate sample. If none or very few failures are detected, it must be concluded that the fundamental process was performed correctly and that the observed failures are probably due to type 1 defects (see Introduction, Section 1). We note that the use of the structure is entirely different from those of subsections 3.36, 3.37, and 3.38.



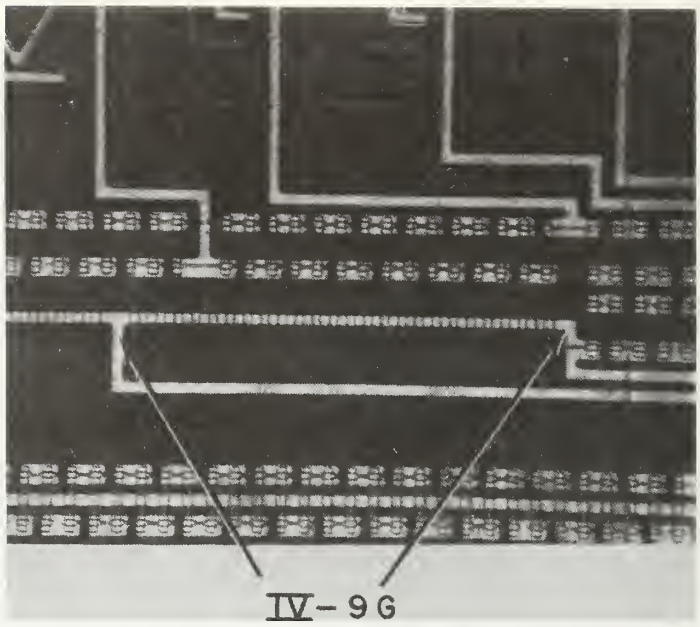
(e)



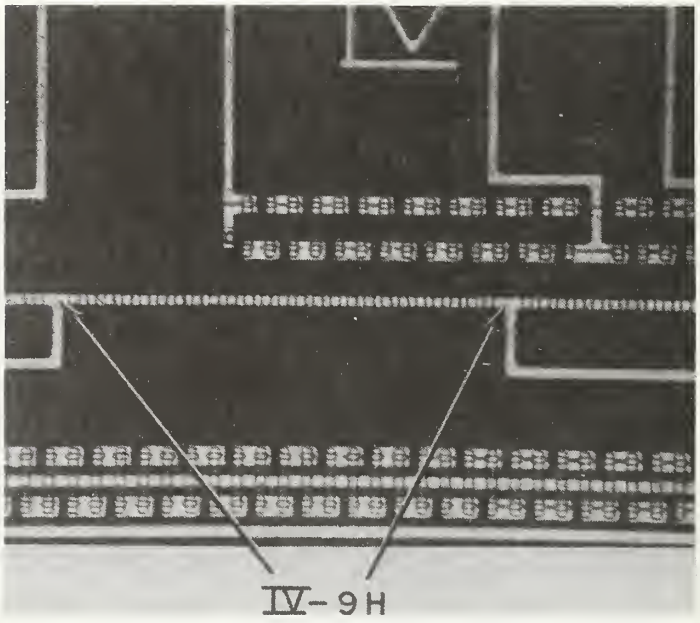
(f)

Figure 174.3. (Continued). (e) p+ epi contacts and (f) n+ epi contacts.

Samples of Data - The main data output from this structure is the diagnostic messages which tell clearly what types are open. An example of this output is shown in figure 175. Also data from those devices which were not open are shown in figure 176. These data are of secondary importance to the diagnostic messages. Most of the failures are due to the structure being partly on the wafer and partly off the wafer edge. Other failures are due to missing conductors or other visible defects. We note that the apparent difference between figures 176(j) and (k) is not due to the different type of steps but rather to the different length of connecting lines.



(g)

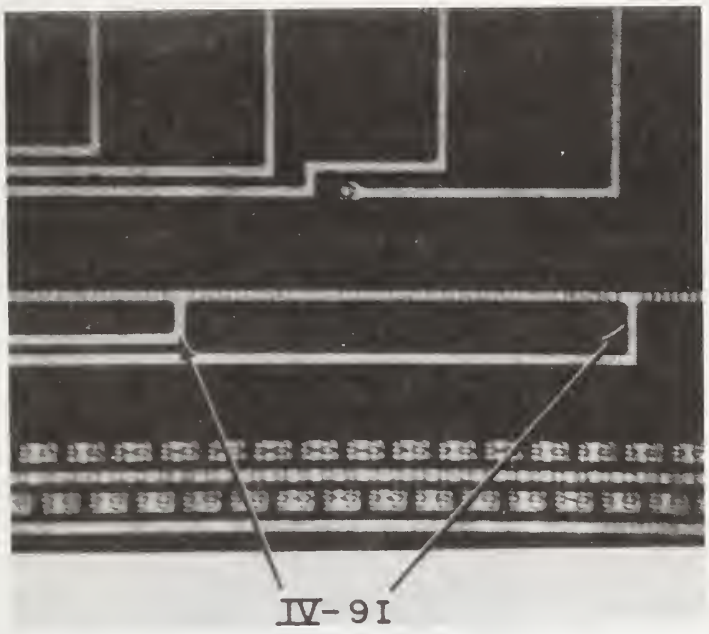


(h)

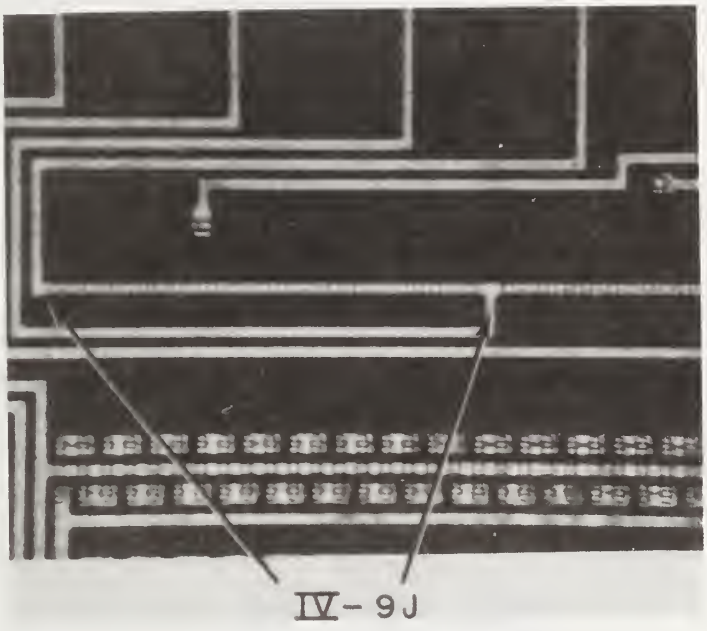
Figure 174.4. (Continued). (g) Al over p+ poly and (h) Al over p^- poly.

Potential Pitfalls - As mentioned above the major pitfall of this structure is assuming the cause of the failure from the electrical data alone.

Overall Usefulness - This structure can be used to "weed out" failures which are marginal on a single device basis if used very carefully. In general a failure on the single device represents a much more solid foundation on which to base a decision. A single device which does not work probably means that there is no reasonable chance of many working. On the other hand many devices not working only means that something is wrong, and that is a very tenuous foundation on which to base a decision. This philosophy is discussed briefly in subsection 1.2b.



(i)



(j)

Figure 174.5. (Continued). (i) Al over p+ epi
(j) Al over n+ epi.

No changes are suggested for this structure.

Related Structures - This structure is related to I-78.

```
TEST  21 =  .16900E-06
OPEN AT VLO IV9BPMPE  TTRES2
TEST  48 =  .23100E-06
OPEN AT VLO IV9EPPEC TTRES2
TEST  57 =  .15200E-06
OPEN AT VLO IV9FNPEC TTRES2
TEST  66 =  .14400E-06
OPEN AT VLO IV9GAPPP TTRES2
TEST  75 =  .13700E-06
OPEN AT VLO IV9HAPMP TTRES2
TEST   3 =  .15900E-06
OPEN AT VLO IV9TOTC TTRES2
TEST  12 =  .14100E-06
OPEN AT VLO IV9APPPE  TTRES2
TEST  21 =  .14900E-06
OPEN AT VLO IV9BPMPE  TTRES2
TEST   3 =  .14200E-06
OPEN AT VLO IV9TOTC TTRES2
TEST  12 =  .13200E-06
OPEN AT VLO IV9APPPE  TTRES2
TEST  75 =  .12700E-06
OPEN AT VLO IV9HAPMP TTRES2
TEST  84 =  .12200E-06
OPEN AT VLO IV9IAPPE  TTRES2
TEST  93 =  .12500E-06
OPEN AT VLO IV9JANPE  TTRES2
TEST   3 =  .14600E-06
OPEN AT VLO IV9TOTC TTRES2
TEST  12 =  .12400E-06
OPEN AT VLO IV9APPPE  TTRES2
TEST  21 =  .13400E-06
OPEN AT VLO IV9BPMPE  TTRES2
TEST  30 =  .13400E-06
OPEN AT VLO IV9CPPPC TTRES2
TEST  39 =  .12900E-06
OPEN AT VLO IV9DPMPC TTRES2
TEST  48 =  .12900E-06
OPEN AT VLO IV9EPPEC TTRES2
TEST  57 =  .13300E-06
OPEN AT VLO IV9FNPEC TTRES2
TEST  66 =  .12900E-06
OPEN AT VLO IV9GAPPP TTRES2
TEST  75 =  .11900E-06
OPEN AT VLO IV9HAPMP TTRES2
TEST  84 =  .11000E-06
OPEN AT VLO IV9IAPPE  TTRES2
TEST  93 =  .10900E-06
OPEN AT VLO IV9JANPE  TTRES2
```

Figure 175. Diagnostic messages indicating which structures are open.

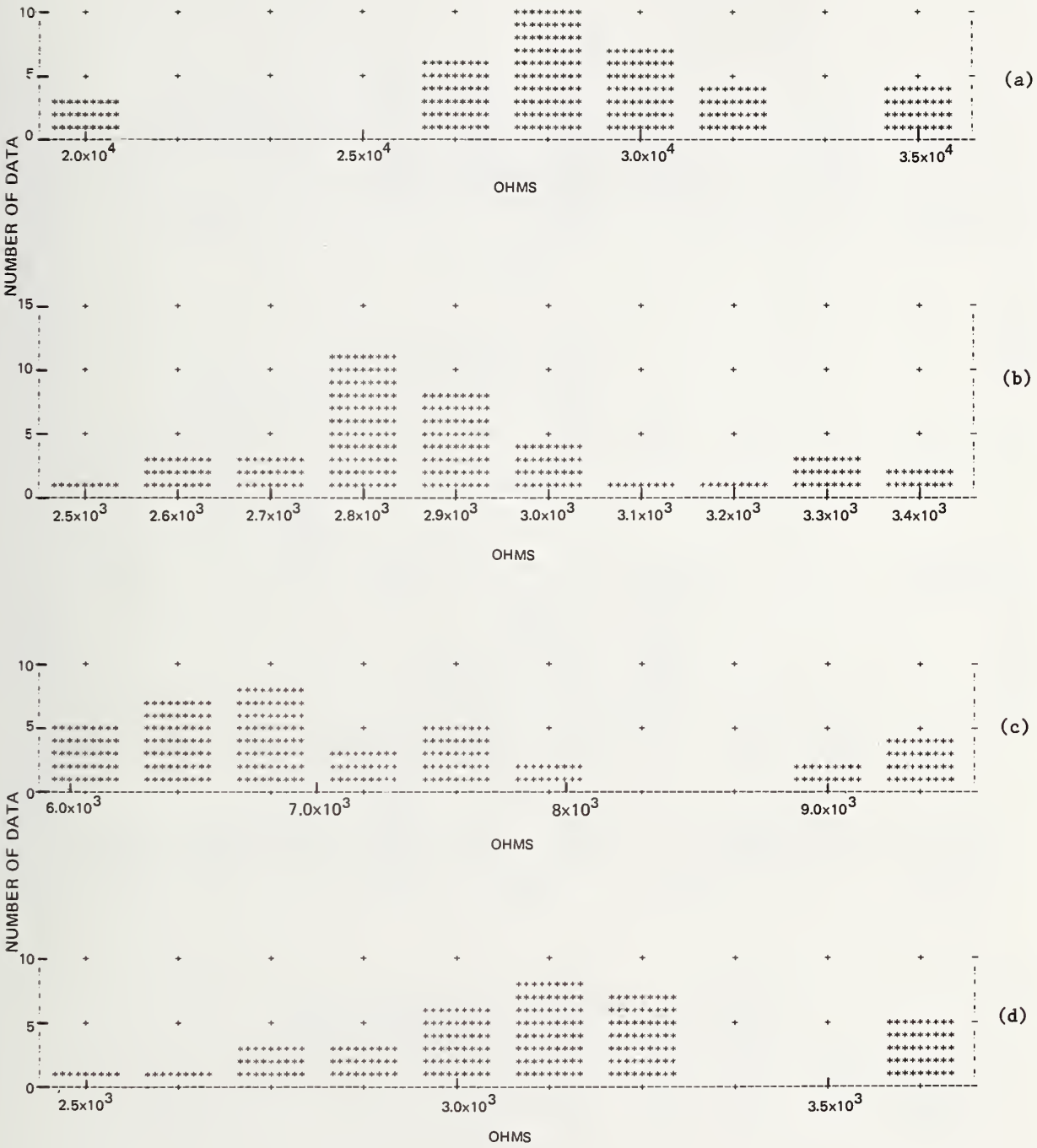


Figure 176.1. Autolimit histograms of the resistance of the various connections. All data in ohms.

(a) Total resistance
(b) IV-9A p+ poly over epi
(c) IV-9B p- poly over epi
(d) IV-9C p+ poly contacts.

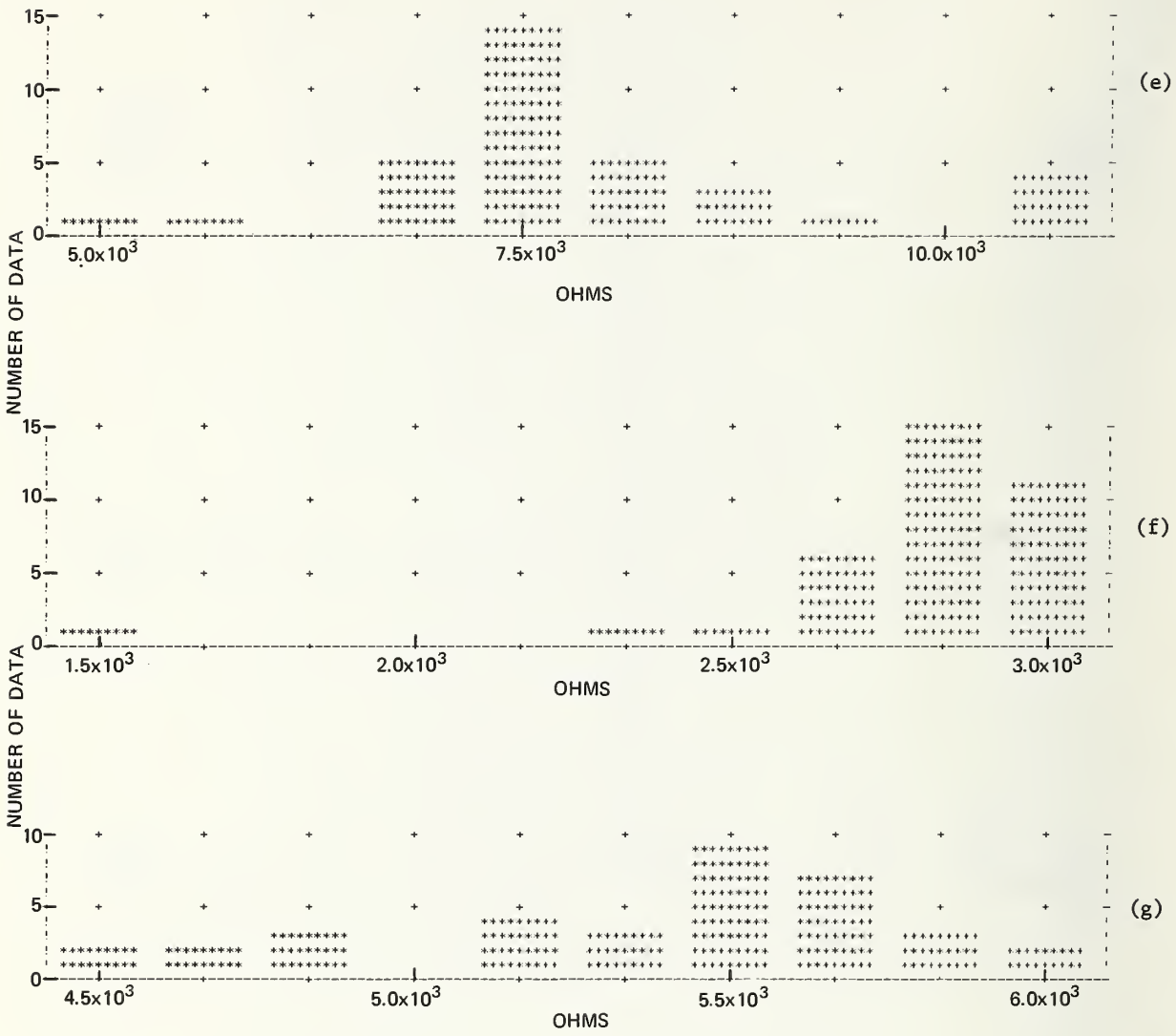


Figure 176.2. (Continued). (e) p- poly contacts
(f) p+ epi contacts
(g) n+ epi contacts.

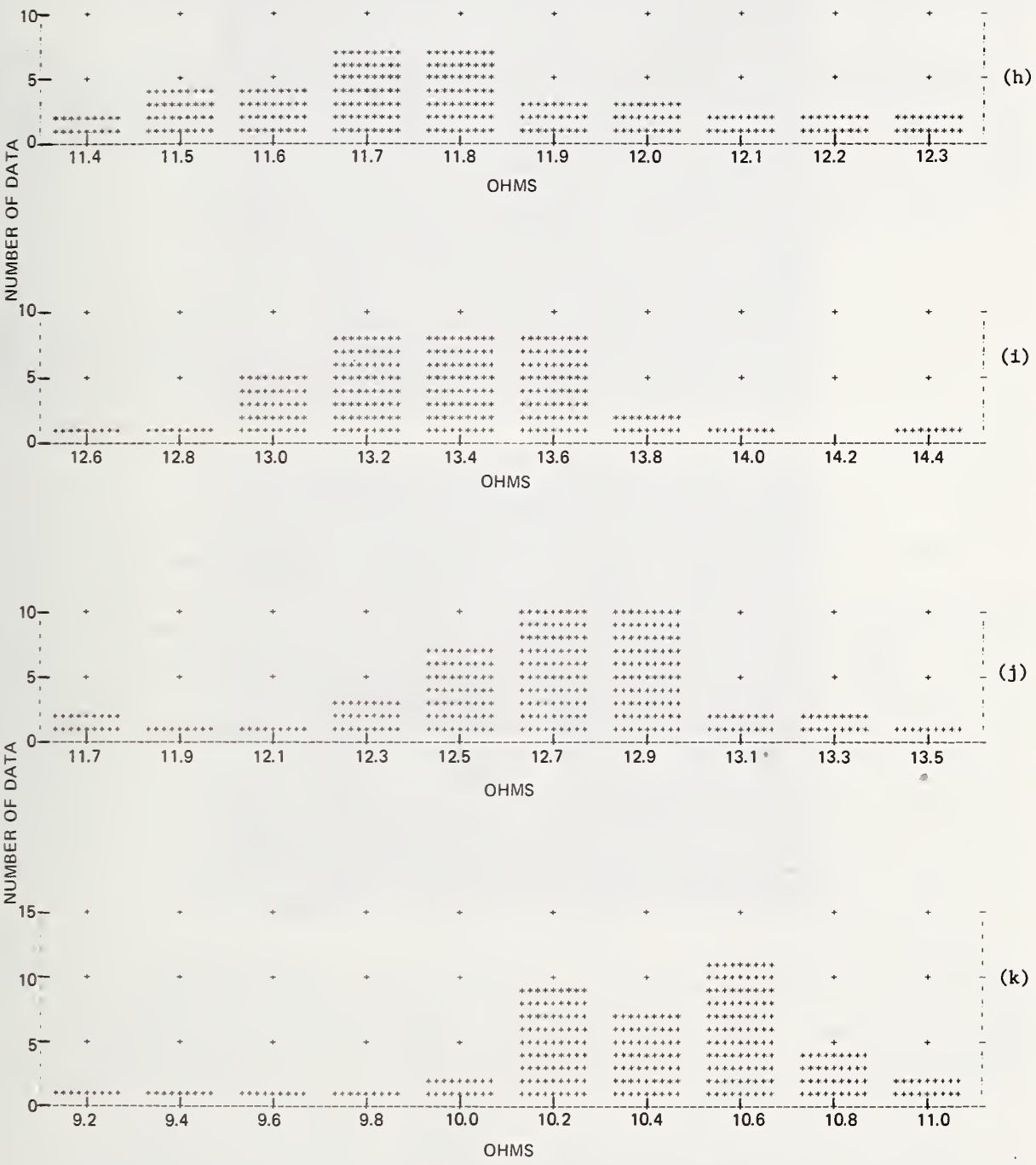


Figure 176.3. (Continued). (h) Al over p^+ poly
(i) Al over p^- poly
(j) Al over p^+ epi
(k) Al over n^+ epi.

3.40 Electrical Dimension Test - V-1, V-2, V-3

Purpose - Structures V-1, V-2, and V-3 electrically measure epi, poly, and aluminum dimensions, respectively.

Verbal Description - This structure is formed from uniformly conducting material and consists of two sections connected together but of different sizes. These sections are 1.0 and 0.3 mil wide, respectively, and are provided with potential probes whose center-to-center spacing is 10.0 mil. In order to minimize the photolithographic effects of changing the width of the narrow line at a corner, a small bevel was introduced at the point where the 0.2-mil-wide potential probe contacts the line.

Line Drawing - The line drawing for this structure is shown in figure 177.

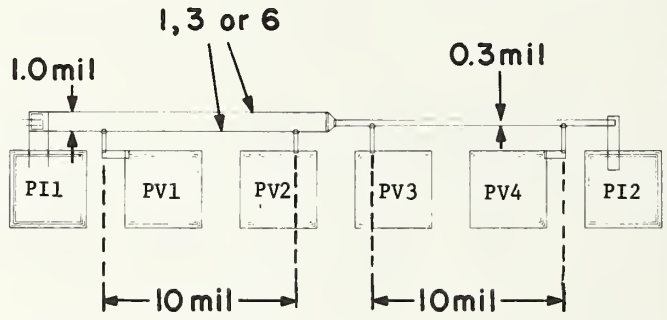


Figure 177. Electrical dimension test, test structures V-1, V-2, and V-3, computer line drawing.

Halftone Photograph - The photomicrograph for this structure is shown in figure 178.

Electrical Access - This structure has six electrical access points designated as:

Current Contact 1	PI1
Potential Contact 1	PV1
Potential Contact 2	PV2
Potential Contact 3	PV3
Potential Contact 4	PV4
Current Contact 2	PI2

Testing Method - Detailed operation of these structures was first presented in ref. 12. Basically these structures are tested as a bridge resistor except two sets of potential measurements are made. The ratio of the potential between PV1 and PV2, V_1, to that between PV3 and PV4, V_2, at the same current, I, yields the actual width according to the following formula:

$$W_{oe} = \frac{W_{1d} - \alpha W_{2d}}{2(1 - \alpha)}$$

where W_{1d} and W_{2d} are the designed dimensions in the wide and narrow regions, respectively. W_{oe} is the deviation of the actual dimensions, W_1 and W_2, from the designed dimensions. These notations are shown in figure 179. $\alpha = V_2/V_1$. The final dimension W_2 is then $W_{2d} - 2\ W_{oe}$ and W_1 is $W_{1d} - 2\ W_{oe}$.

It is, of course, necessary to ensure that the structure is not being heated by the current since this will preferentially change the resistance of the narrow section. This is

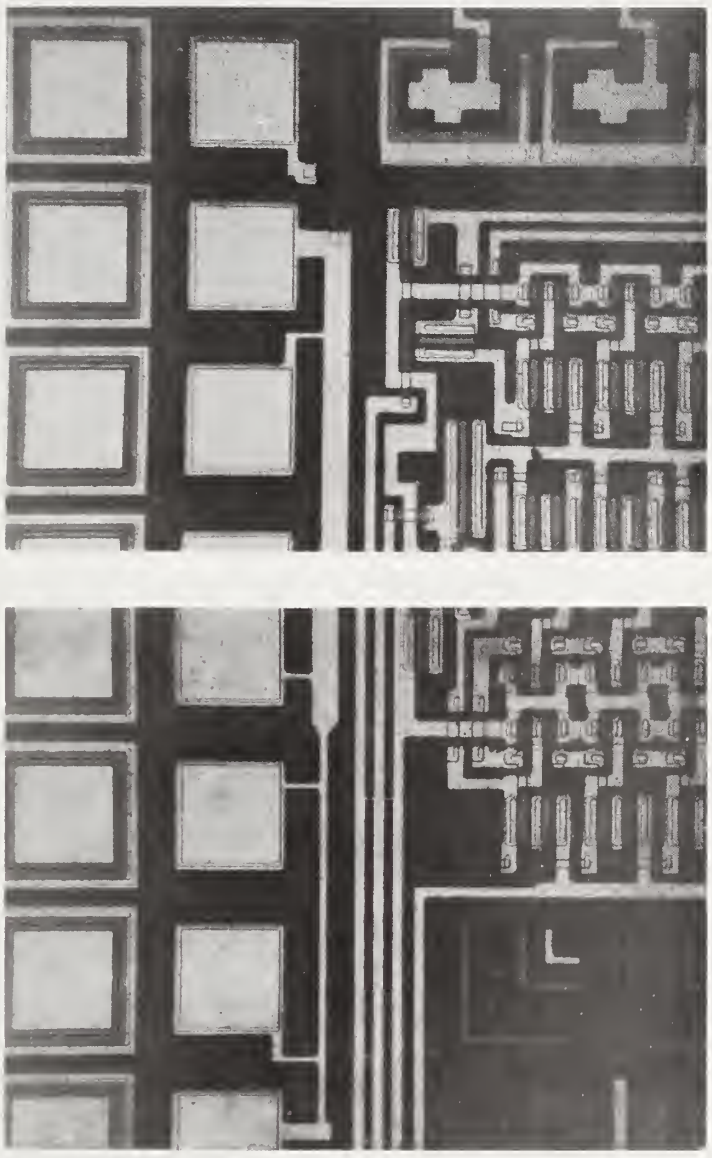


Figure 178. Photomicrographs, electrical dimension test, test structures V-1, V-2, and V-3.
(a) Interconnection of poly and Al,
(b) narrow section of Al.

tested by observing the linearity of the potential between PV3 and PV4 at different current levels. Since heating is by I^2R and over small temperature changes ΔR is proportional to ΔT, a nonlinearity test is suitable for detecting heating problems. As long as the widths of the sections were accurate as designated at the initial stages of the image formation process and any changes in the dimensions occurred independently of the opposite edge, the deviation in the actual width will be the same for both the narrow and wide sections. One can therefore measure the actual dimensions with no optical interaction at all. It is required that the resistivity be uniform across the entire length of the structure. This method is limited to conducting materials. Accuracies in the 1-μin. (250-Å) range have been obtained with this structure but physical verification of the measurements has not been performed.

Samples of Data - No data were acquired from this structure under this contract.

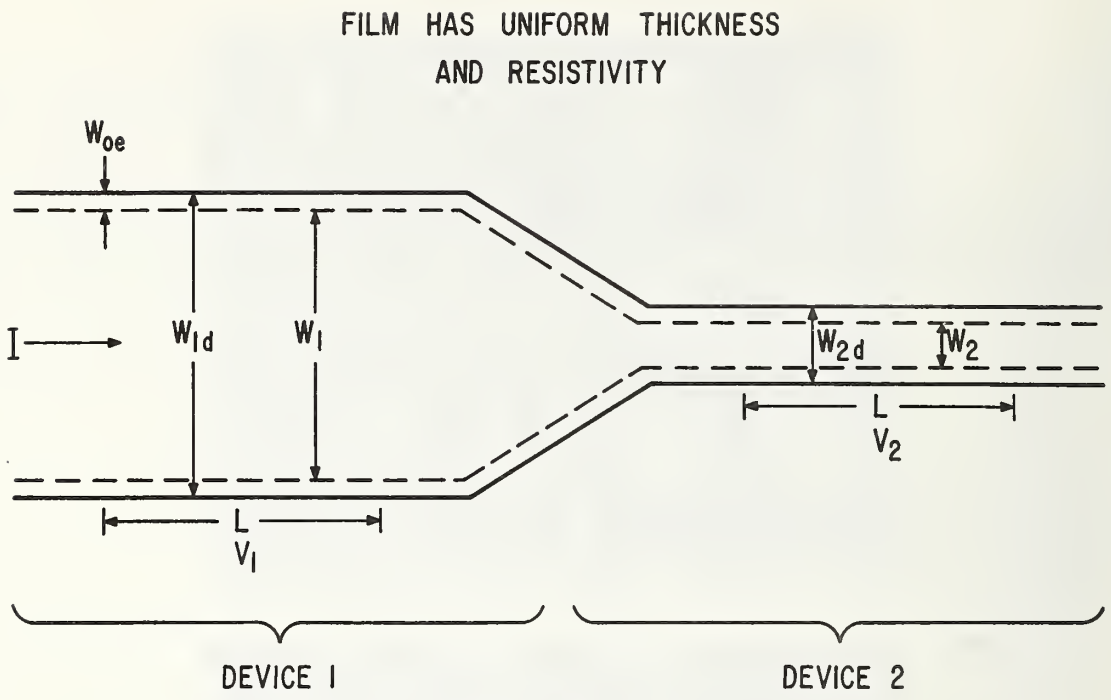


Figure 179. Definition of notation.

Potential Pitfalls - If the edge definition is poor, the structure will reflect this instead of the actual dimension. On the other hand if the edge definition is poor, what is the width in the first place? This measurement actually defines an electrical width which may not be exactly the same as the physical width.

Overall Usefulness - This structure has not been sufficiently evaluated to comment on the overall usefulness. One of the major advantages of this method is that dimension measurement can be acquired by existing hardware and does not require special optical interfaces to data handling equipment. Another advantage of this method is that precisely the same kind of measurement at precisely the same current level using precisely the same theory is done for both the thick and thin sections. One does not have to worry about cross-coupling between different types of measurement.

Related Structures - This structure is related to the bridge resistors I-57, I-59, I-61, and I-63.

3.41 Two-Level Interaction; Design Rule Test - V-4, V-5, V-6, V-7, V-8

Purpose - These test structures measure optimum spacings between mask levels.

Verbal Description - This structure consists of two lithographic levels which vary in their relationship to each other and to themselves. There are 70 different types of tests which are identified and many other non-specified observations which can be made. Only the orthogonal intersections are included. It is more expedient to refer to the line drawing (Fig. 180) than to try to describe each interaction verbally. In this figure each identified interaction is labeled with a number and an arrow. The arrow terminates on a heavy line on one side and a lighter line on the other side. The heavy line represents a "fixed" position and the length of the arrow is allowed to vary. Within any single test structure the length of all the arrows is the same. Some tests do not have heavy lines; these vary about the center of the arrow. In this particular test pattern the arrows are 0.5, 0.3, 0.2 and 0.1 mil long and the line drawing is drawn using 0.5-mil features.

Line Drawing - The line drawing for this structure is shown in figure 180.

Halftone Photograph - The photomicrograph for this structure is shown in figure 181.

Electrical Access - There is no electrical access.

Testing Method - This description is tested by optical observation only.

Samples of Data - A complete set of photomicrographs is shown in figures 181(a) through (ac) for one pattern on one wafer. We note that most of the photographs do not show anything of particular interest except that there is no problem with the interaction between the two levels at the characteristic size of the structure. Several of the structures, however, reveal totally unexpected results.

For example, structure V-4A (figure 181b) shows silicon left in the "hole" near the edges but only for the square hole, not the neighboring long one. This type of effect has been noticed also on V-4B and V-4C. It is confined to the epi layer only; it does not appear in the poly. This effect is probably related to the transparent substrate in some way. Other effects are seen in V-4D where some holes are missing and some edge interactions are seen. It is quite clear that 0.1 mil is too small for the poly-poly spacing, for example. The photograph of V-5C shows another example of an anomalous effect, V-6D shows poor aluminum definition near a silicon edge, and V-7A shows difficulty in maintaining definition for isolated photoresist islands on top of epi. The photographs of 8A, B, C, and D show progressive degradation in the contact geometry as the inside silicon edge is approached. The outside silicon edges are not affected.

Some of effects observed are unexpected and are due to relatively large geometries -- not the small geometries where one would expect to find the effects. The small geometry effects are also present of course, as expected. It requires a structure of this type to deduce the causes of the large geometry effects (which are tentatively identified as being due to constructive interference or diffraction effects through the transparent substrate).

Potential Pitfalls - None.

Overall Usefulness - This structure has not been extensively used to date. It is clear, however, that several large geometry effects have been observed which could be fatal to a circuit if present. A disadvantage of this device is that the data must be obtained in a subjective manner and are not easily put into a computer. On the other hand, specific problem areas such as metal definition near steps and missing holes or islands are almost immediately observable with very little effort. One can very quickly determine where the problem areas are and can choose from most of the geometries which are likely to exist in any circuit design at a glance (almost). The best example of unexpected behavior was the contact holes to bare sapphire near inside silicon corners. This is of little importance for most current applications but could be a consideration for new designs.

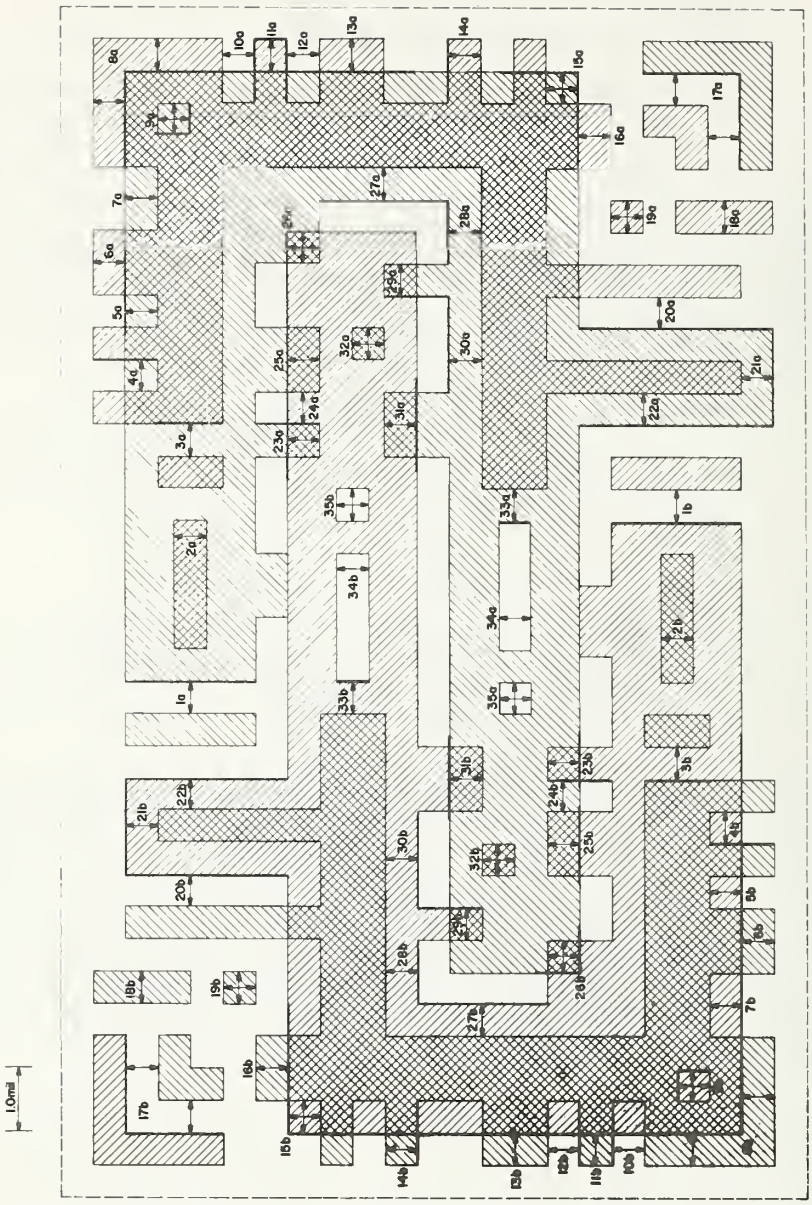
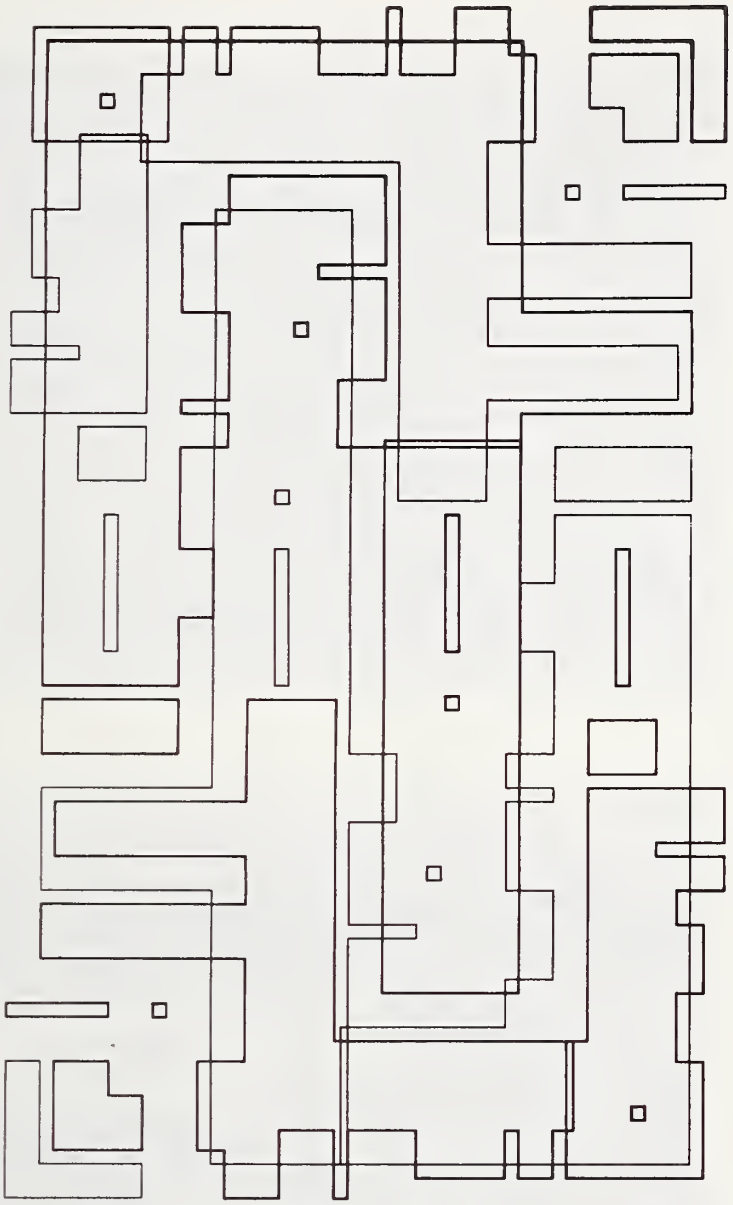


Figure 180.1. Two-level interaction; design rule tests, test structures V-4 through V-8. (a) Manual line drawing, each interaction is identified by its number; 0.5-mil spacings.

The most serious limitation with this structure is the space required for a single structure; 0.1 mil is a relatively crude feature for new lithographic methods. On the other hand, large area effects were seen at the 0.5-mil level. Furthermore, there are many dimensions between 0.1 and 0.2 mil, for example, which may prove to be the critical dividing line between success and failure. With only four characteristic dimensions available the resolution of the limits is clearly poor. We have taken a balance of the most important tests and the most likely dimensions for this pattern. The choice is not particularly for a structure redesign but rather for a careful consideration of the most important dimensions of interest. If we can have only four dimensions this author would still pick those used here. If a fifth were allowed, 0.05 mil would be added.

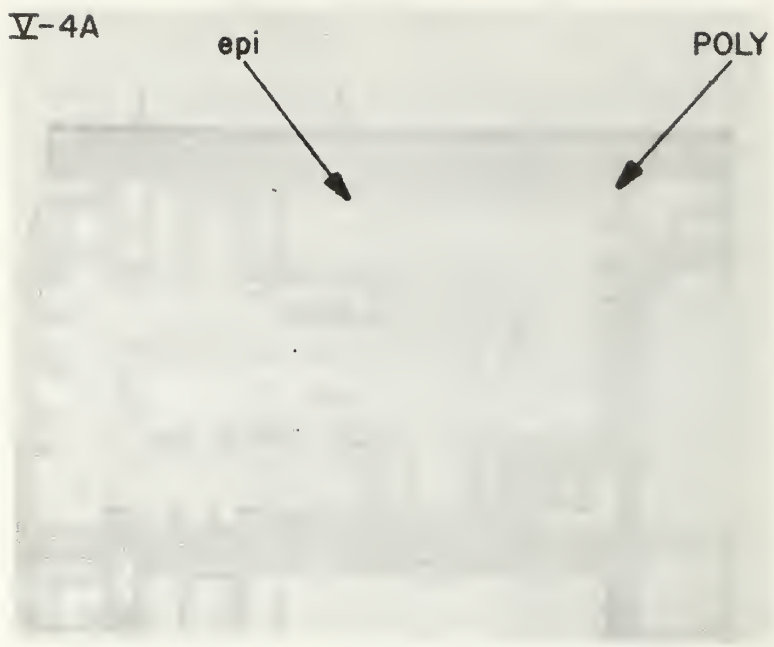


(b)

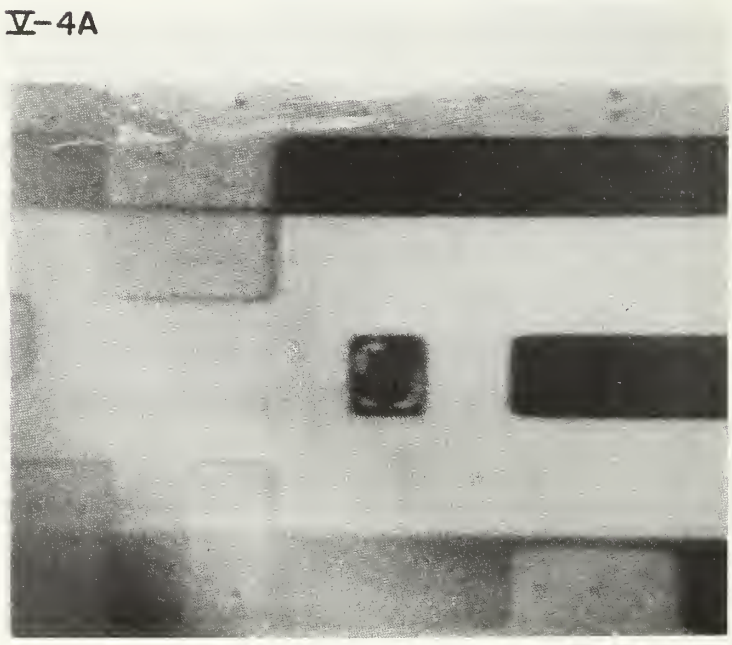
Figure 180.2. (Continued). (b) Computer line drawing of 0.2-mil spacings.

Not all the possible two-level interactions have been considered; only those deemed to be the most important have been included. Perhaps a dedicated test pattern using all possible interactions and many more characteristic dimensions would be a good approach for this very important area of process characterization. This, of course, defeats the fundamental principle of simultaneous fabrication of all structures.

We also note that some of the spacings depend on the precise alignment achieved between the two levels involved. This does not detract but rather adds to the usefulness of this structure. The precise alignment achieved can be measured with the structures of subsection 3.49 to determine the extent of the misalignment. Since the misalignment in general varies across a wafer (because of runout, etc), a quasi-continuous spectrum of spacings is therefore available for these tests. Furthermore, since the basic idea is to characterize the total process, any designed interaction must also satisfy the limitations of the lithographic process (including alignment). Therefore, when problems are observed, the actual spacing between levels can be determined and this may be the threshold level for failure with reasonable resolution. Similar statements can be made for the actual dimensions achieved (due to overetching, etc).



(a)

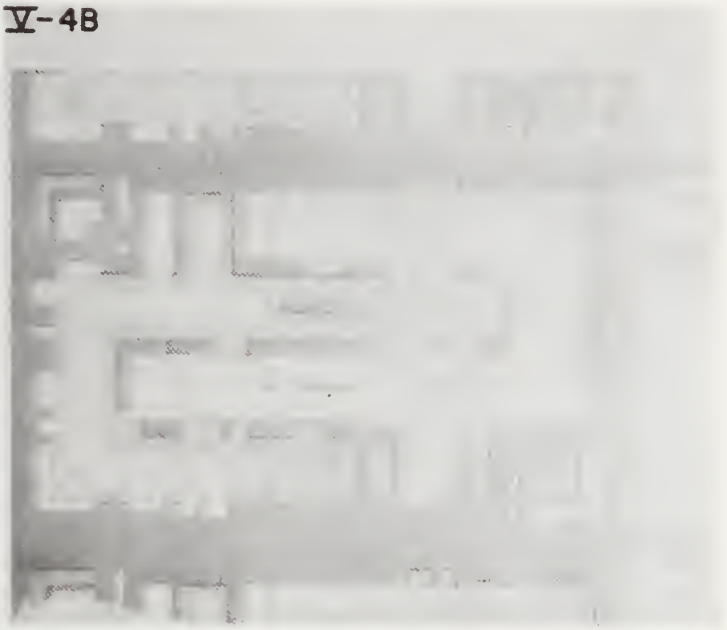


(b)

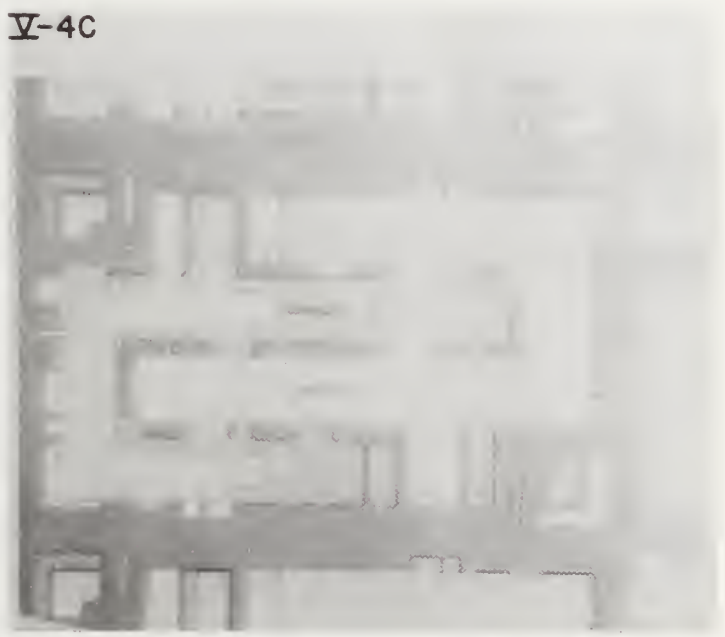
Figure 181.1. Photomicrographs, two-level interaction; design rule test, test structures V-4 through V-8;
(a) 0.5-mil epi-poly
(b) silicon left in 0.5-mil hole.

There are no recommended changes for these structures.

ther Related Structures - All structures on the pattern are related to these structures.



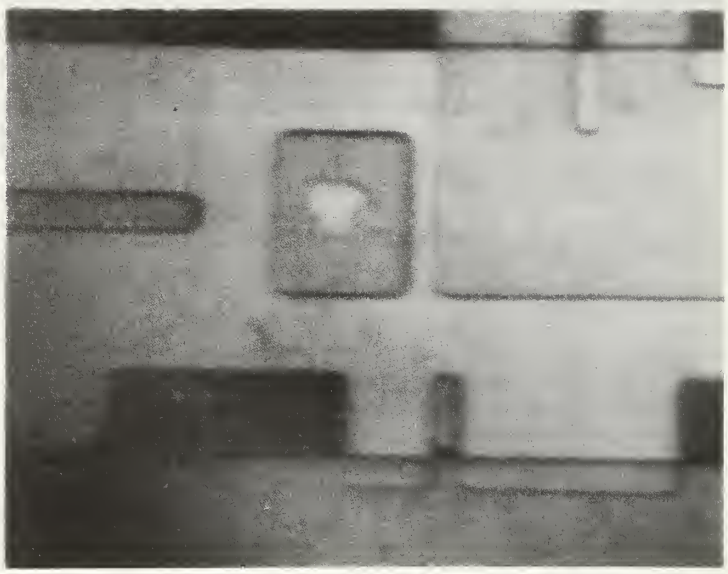
(c)



(d)

Figure 181.2. (Continued). (c) 0.3-mil poly-epi
(d) 0.2-mil poly-epi.

V-4C

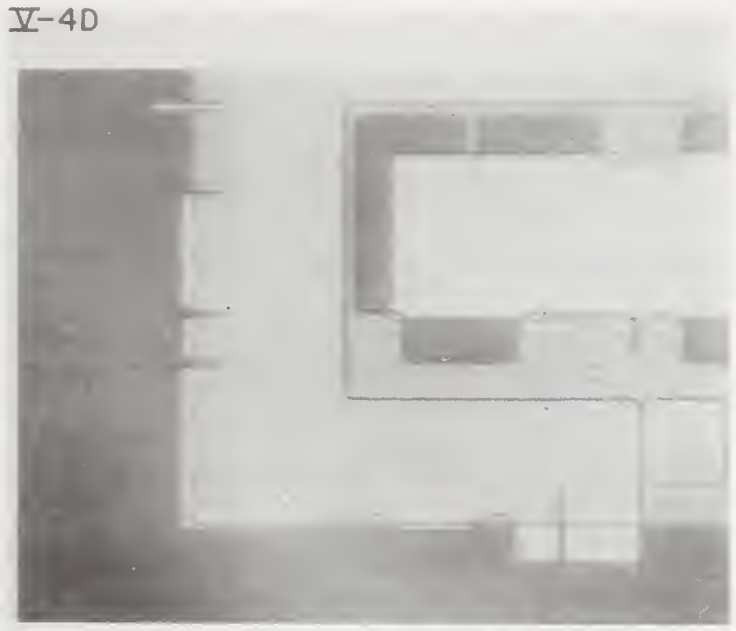


(e)

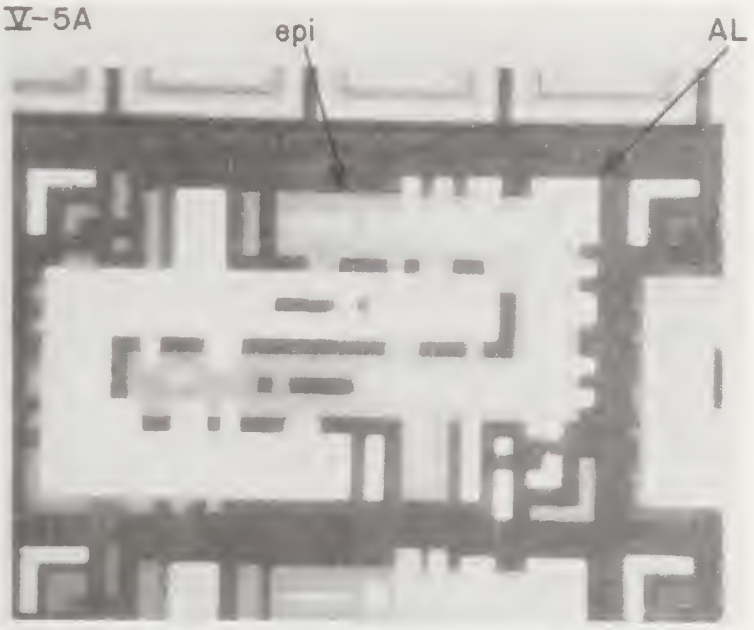
V-4D

(f)

Figure 181.3. (Continued). (e) 0.2-mil poly epi. Note epi left for certain geometries.
(f) 0.1-mil poly-epi.



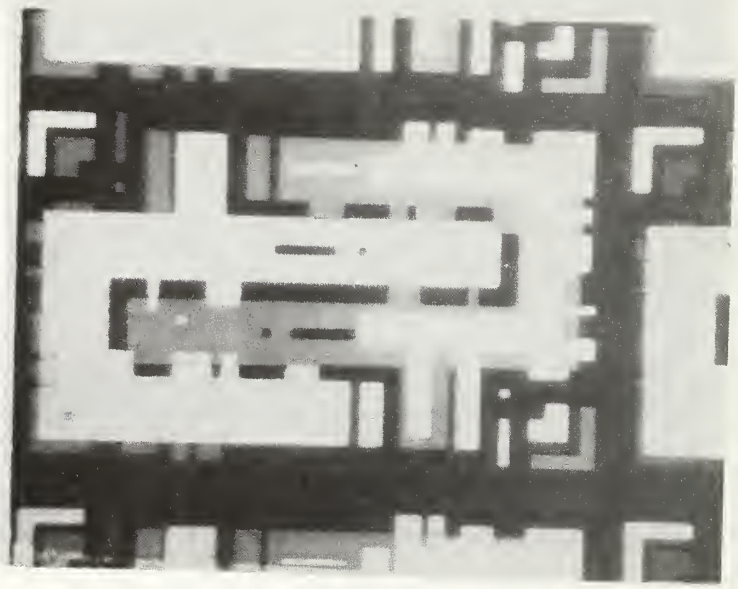
(g)



(h)

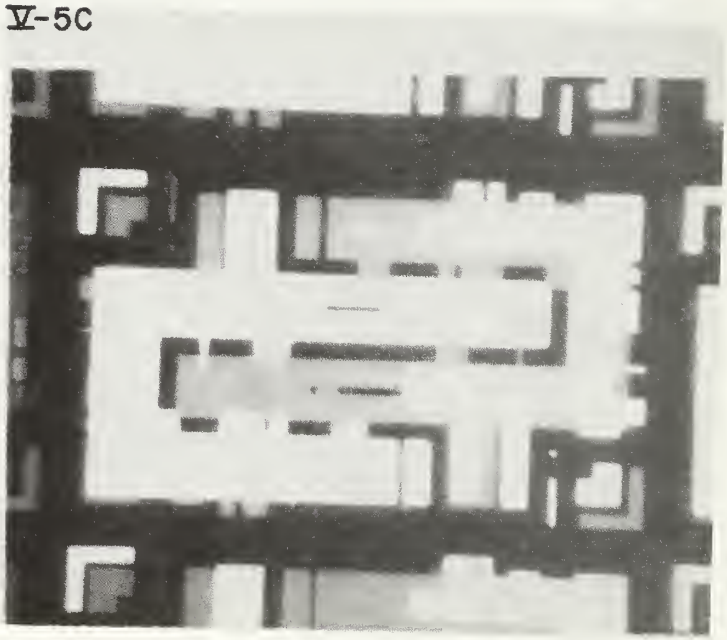
Figure 181.4. (Continued). (g) partially closed edge crossings.
(h) 0.5-mil epi-Al.

V-5B



(i)

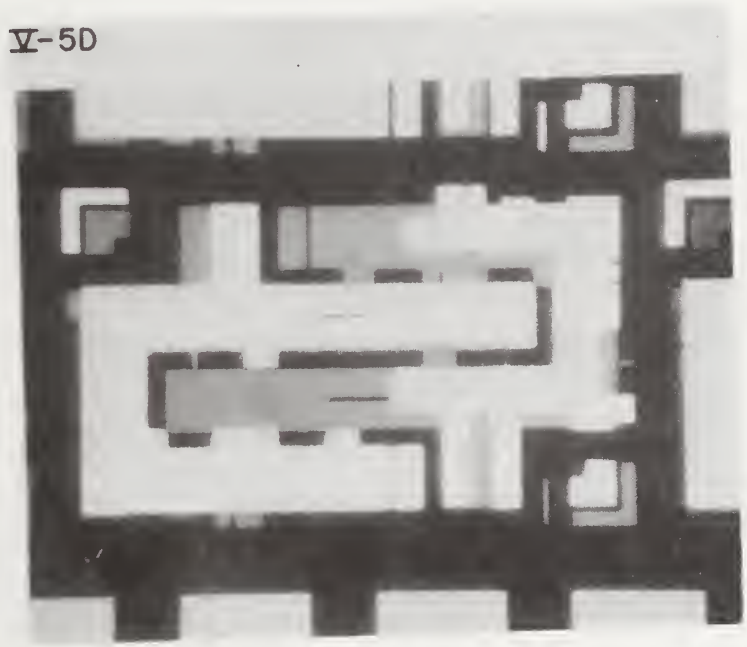
V-5C



(j)

Figure 181.5. (Continued). (i) 0.3-mil epi-Al
(j) 0.2-mil epi-Al.

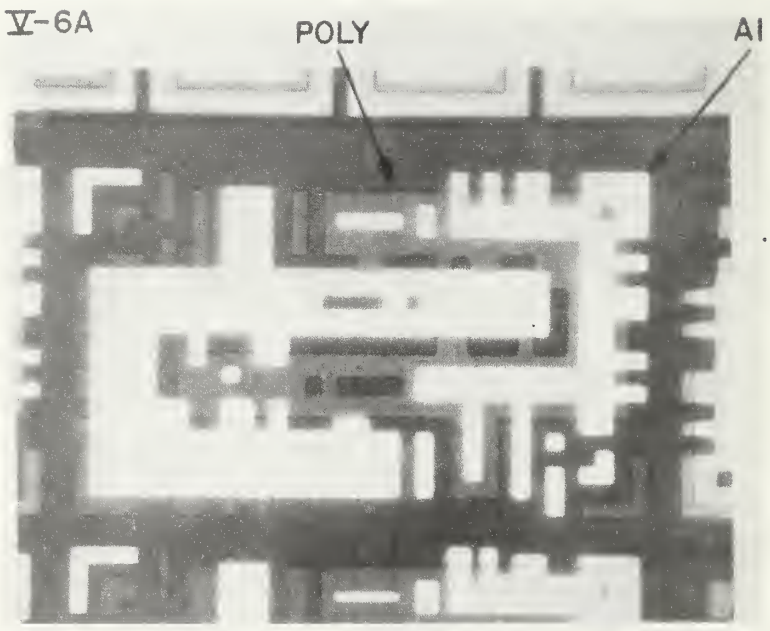
(k)



(l)

Figure 181.6. (Continued). (k) 0.2-mil epi-Al, silicon remaining in slit
(l) 0.1-mil epi-Al.

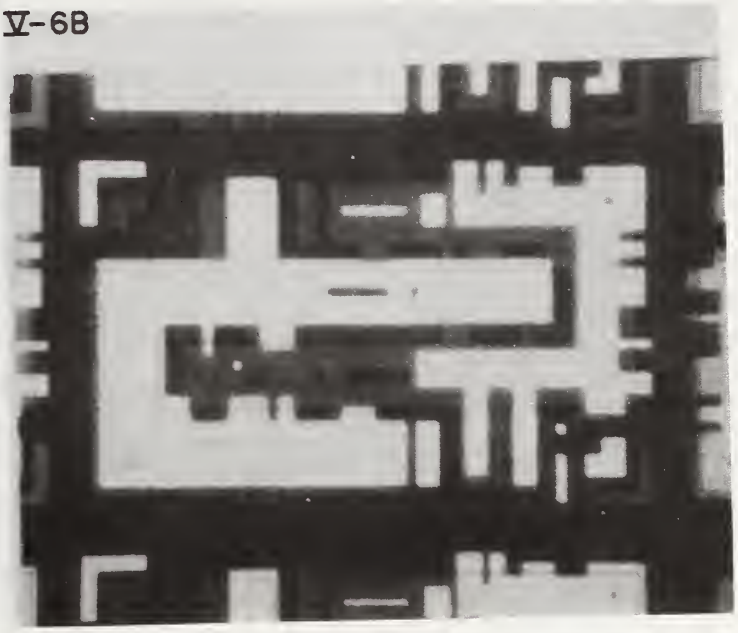
(m)



(n)

Figure 181.7. (Continued). (m) 0.1-mil epi-Al
(n) 0.5-mil poly-Al.

V-6B

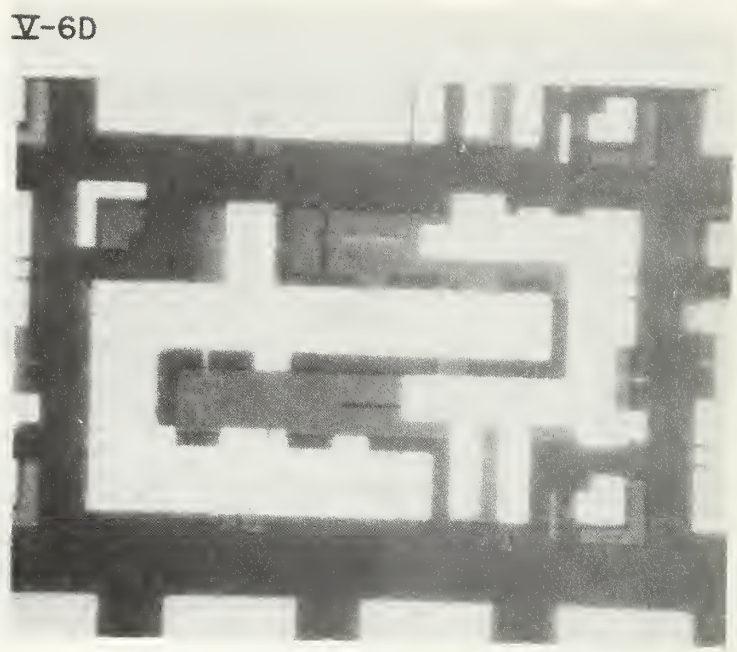


(o)

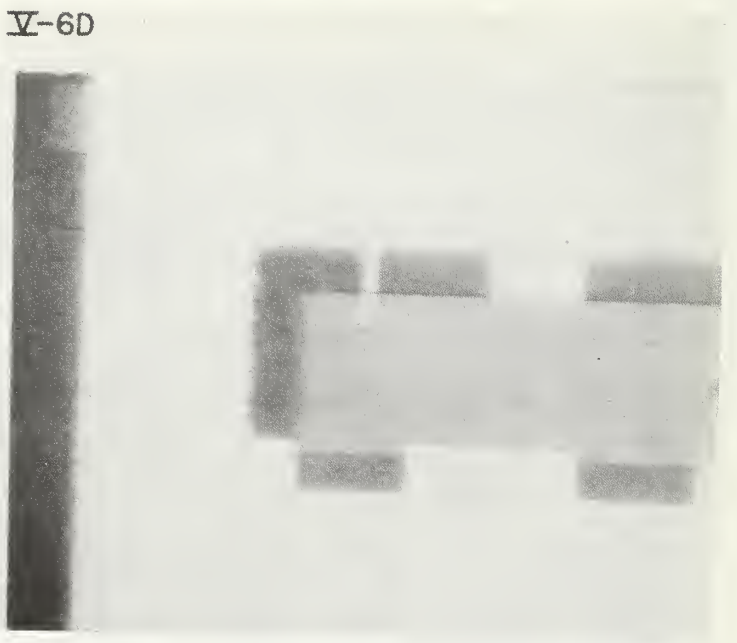
V-6C

(p)

Figure 181.8. (Continued). (o) 0.3-mil poly-Al
(p) 0.2-mil poly-Al.

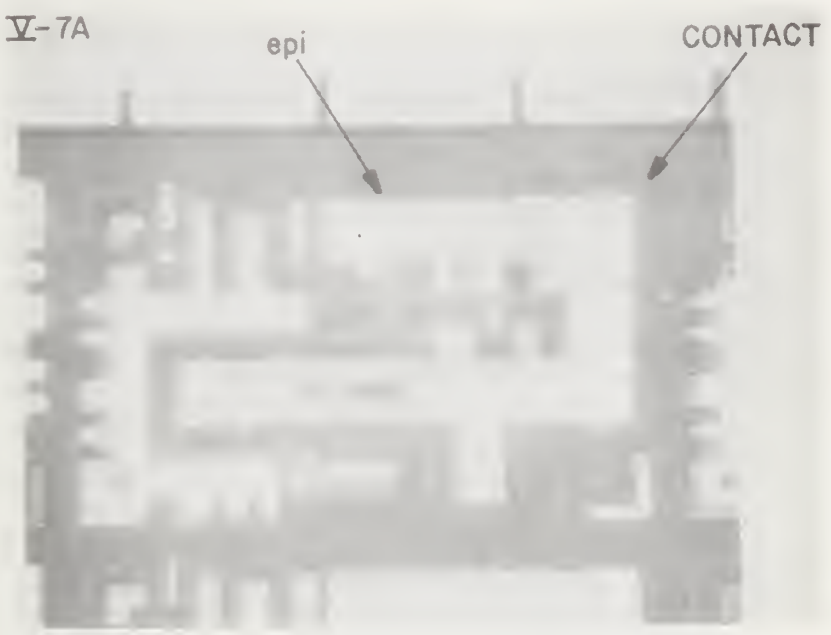


(q)



(r)

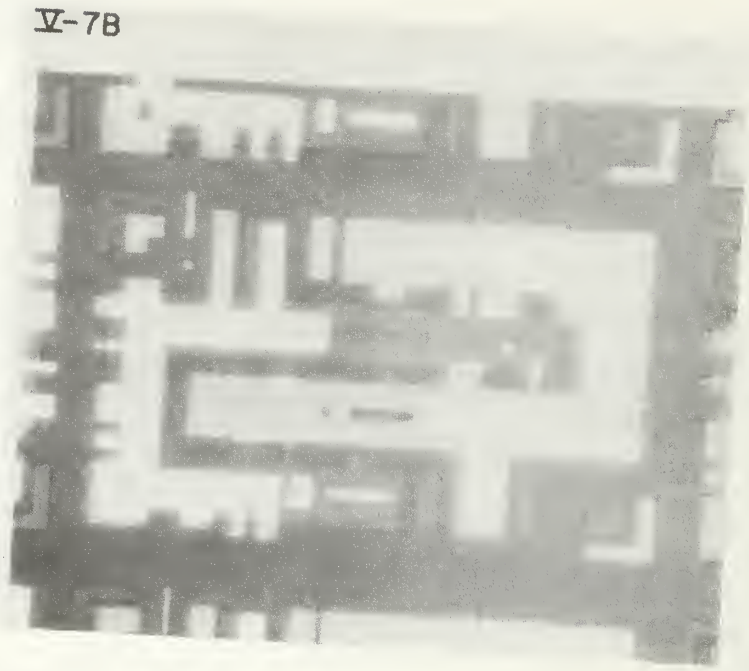
Figure 181.9. (Continued). (q) 0.1-mil poly-Al
(r) 0.1-mil poly-Al, spiking near edge.



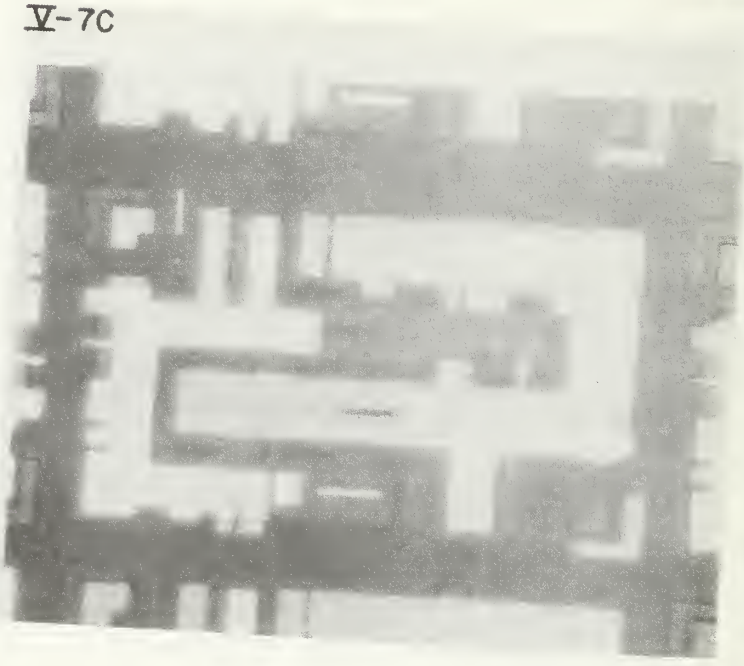
(s)

(t)

Figure 181.10. (Continued). (s) 0.5-mil contact-epi
(t) 0.5-mil contact-epi.

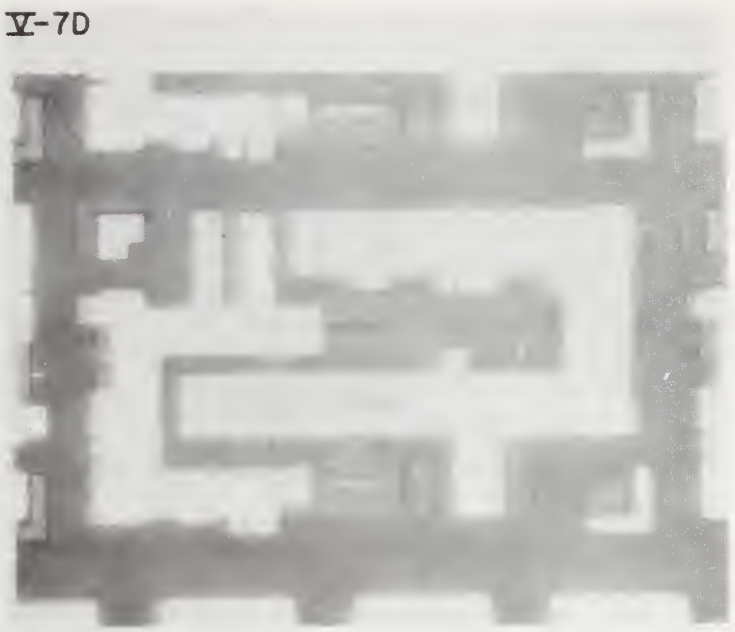


(u)

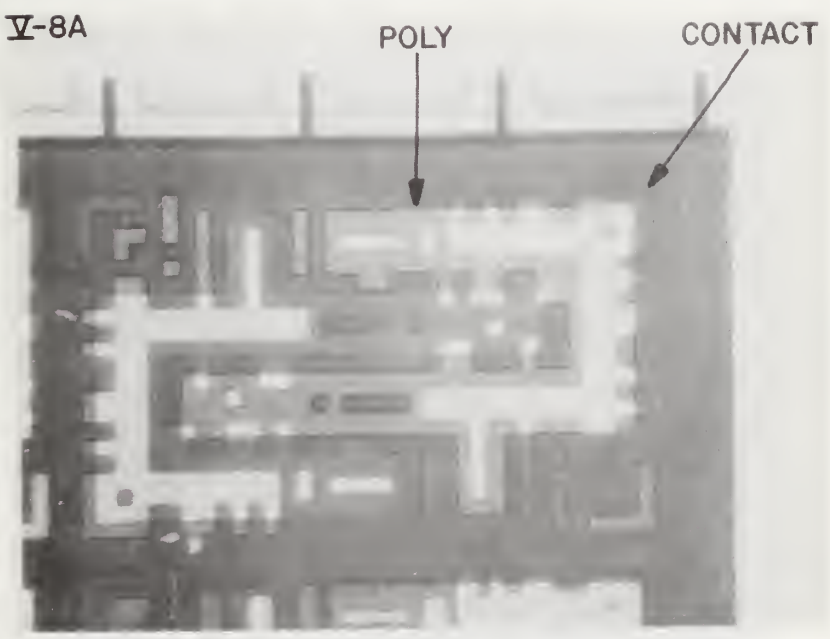


(v)

Figure 181.11. (Continued). (u) 0.3-mil epi-contact
(v) 0.2-mil epi-contact.

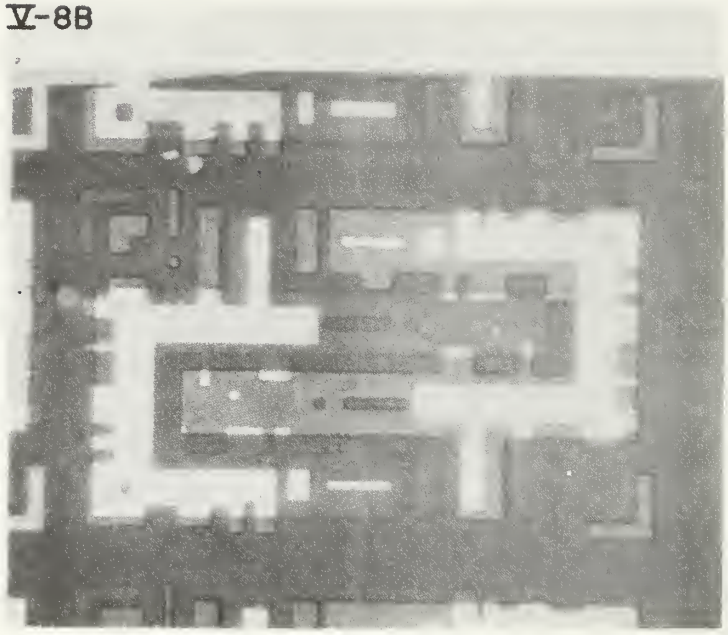


(w)

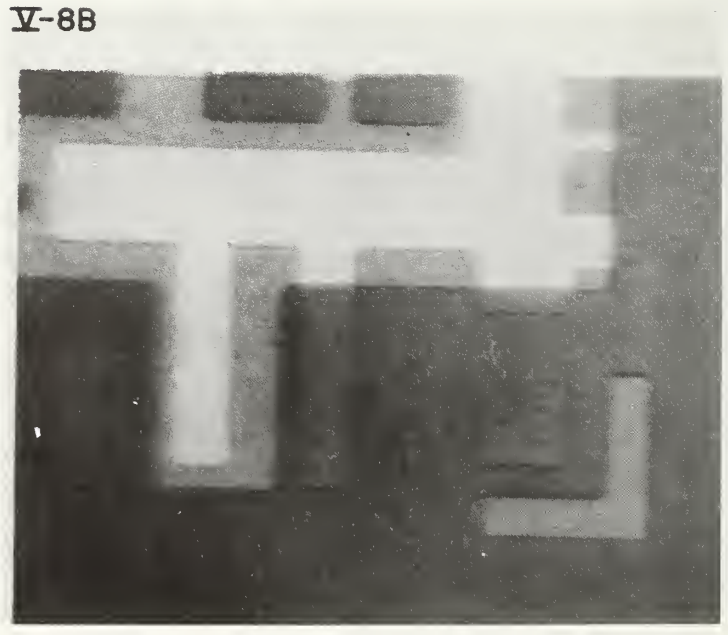


(x)

Figure 181.12. (Continued). (w) 0.1-mil epi contact
(x) 0.5-mil poly contact.



(y)



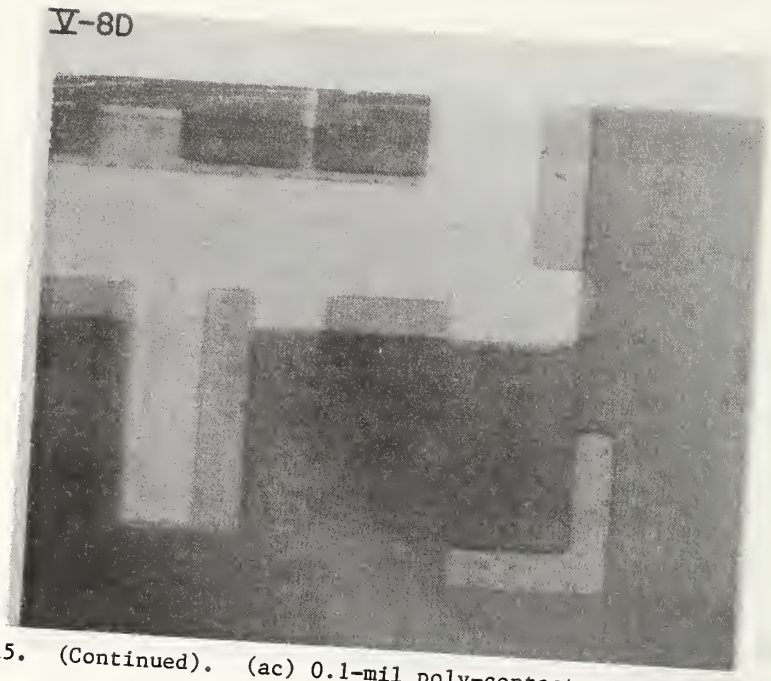
(z)

Figure 181.13. (Continued). (y) 0.3-mil poly contact
(z) 0.3-mil poly contact, poor definition near inside corners.

(aa)

(ab)

Figure 181.14. (Continued). (aa) 0.2-mil poly-contact
(ab) 0.1-mil poly-contact.



(ac)

Figure 181.15. (Continued). (ac) 0.1-mil poly-contact, poor definition on inside corner.

3.42 Electrical Alignment Test; Type 1 - V-9, V-11

Purpose - These test structures electrically measure the alignment between two mask levels.

Verbal Description - This structure consists of diffused silicon separated from metal by a small distance. The silicon is in the form of a rectangular doughnut with part of one side missing. The aluminum is contained within the hole in the form of a rectangle with the corners removed. The separation between the metal and the silicon is varied for each device but is constant within any given device. The separations chosen for this pattern are 0.3, 0.2, and 0.1 mil.

3.43 Electrical Alignment Test; Type 2 - V-10

Purpose - Same as structure in subsection 3.42.

Verbal Description - The structure is closely related to the structures of subsection 3.42. The aluminum is replaced with diffused polysilicon and the doughnut is diffused epi. The separations are 0.3, 0.2, and 0.1 mil.

3.44 Electrical Alignment Test; Type 3 - V-12, V-13

Purpose - Same as structure in subsection 3.42.

Verbal Description - This structure consists of squares of diffused silicon covered by metal with contact holes separated from the edge of the silicon by a small amount. This separation is the same on all sides of the square for each device and varies as 0.3, 0.2, and 0.1 mil.

3.45 Electrical Alignment Test; Type 4 - V-14

Purpose - Same as structure in subsection 3.42.

Verbal Description - This structure consists of an "L" of silicon partially covered by the n^+ mask. This structure is difficult to describe verbally, and the reader is referred to the line drawing. Separations of 0.3, 0.2, and 0.1 mil are included.

3.46 Electrical Alignment Test; Type 5 - V-15

Purpose - Same as structure in subsection 3.42.

Verbal Description - This structure consists of aluminum confined almost entirely to the top of silicon island with silicon dioxide under the metal. The silicon dioxide is removed near the aluminum edge. The oxide edge is spaced 0.3, 0.2, or 0.1 mil from the aluminum edge.

Line Drawing - The line drawings for these structures are presented as follows:

Structures V-9, V-11: figure 182

Structure V-10: figure 183

Structures V-12, V-13: figure 184

Structure V-14: figure 185

Structure V-15: figure 186

Halftone Photograph - The photomicrographs for these structures are shown as follows:

Structures V-9, V-11: figure 187

Structure V-10: figure 188

Structures V-12, V-13: figure 189

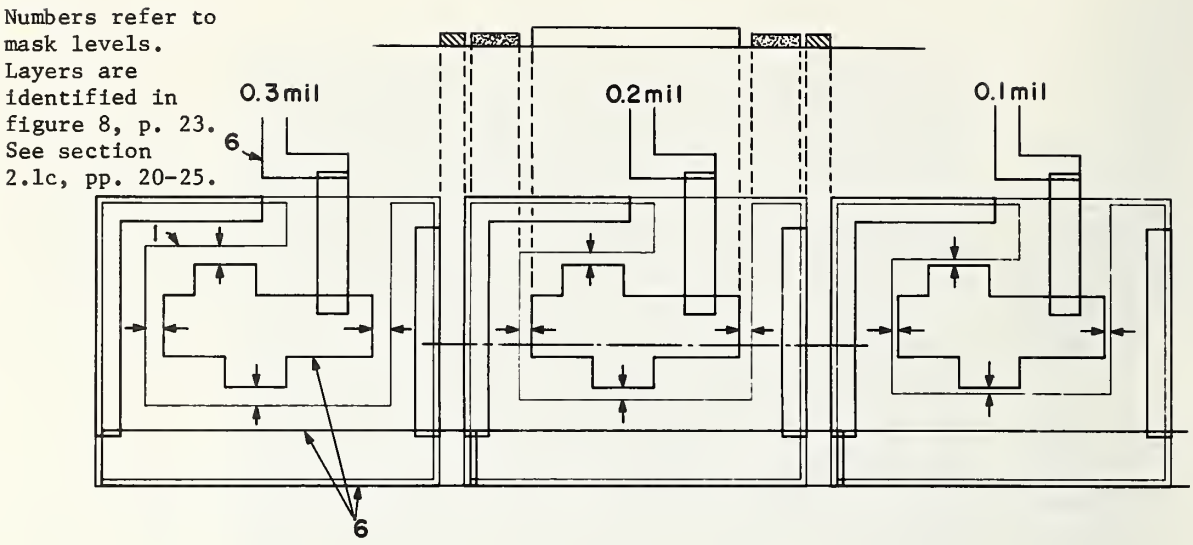


Figure 182. Electrical alignment test; type 1, test structures V-9, V-11, computer line drawing and cross section.

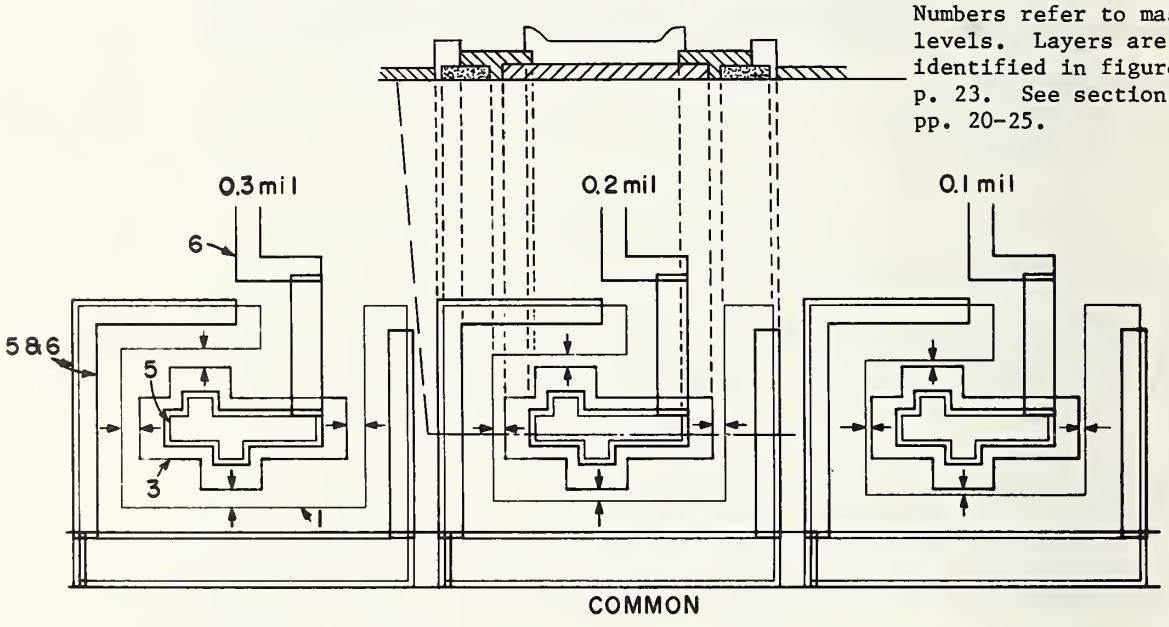


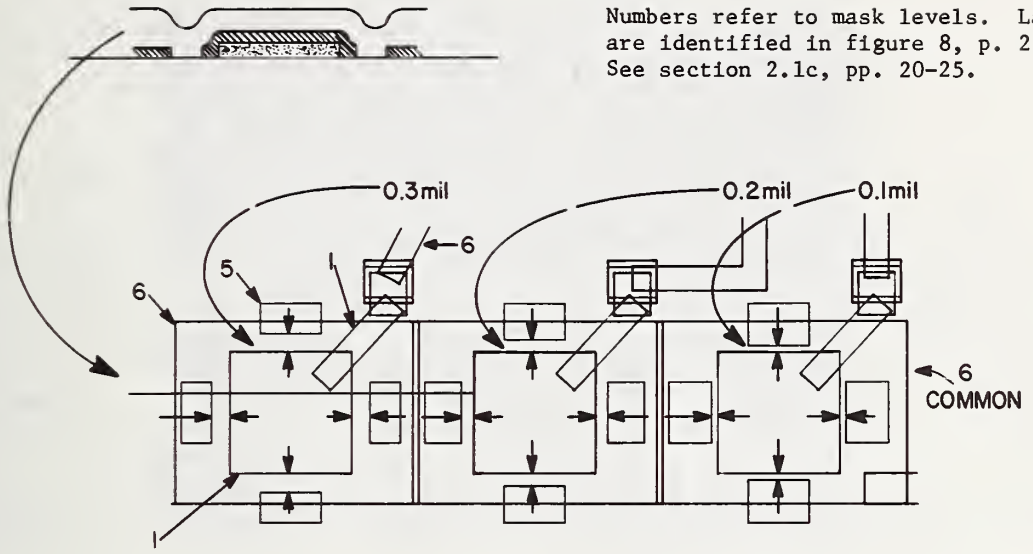
Figure 183. Electrical alignment test; type 2, test structure V-10, computer line drawing and cross section.

Structure V-14: figure 190

Structure V-15: figure 191

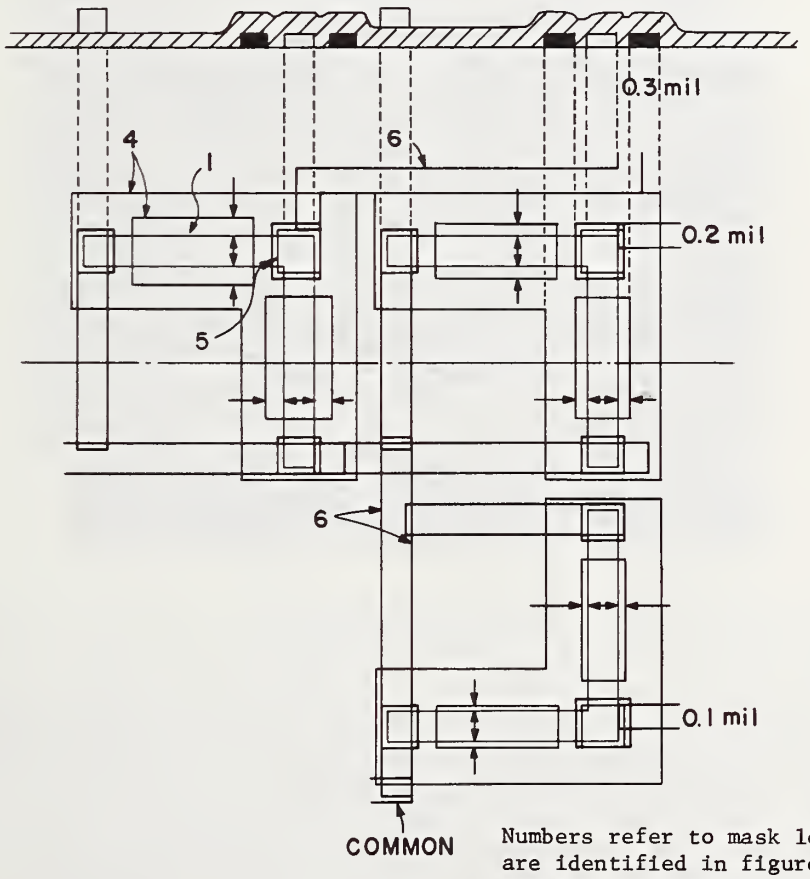
Electrical Access - All of the descriptions have four electrical access points designated

COMMON	PCOM
0.3-mil connection	PR3
0.2-mil connection	PR2
0.1-mil connection	PR1



Numbers refer to mask levels. Layers are identified in figure 8, p. 23. See section 2.1c, pp. 20-25.

Figure 184. Electrical alignment test; type 3, test structures V-12, V-13, computer line drawing and cross section.



Numbers refer to mask levels. Layers are identified in figure 8, p.23 See section 2.1c, pp. 20-25

Figure 185. Electrical alignment test; type 4, test structure V-14, computer line drawing and cross section.

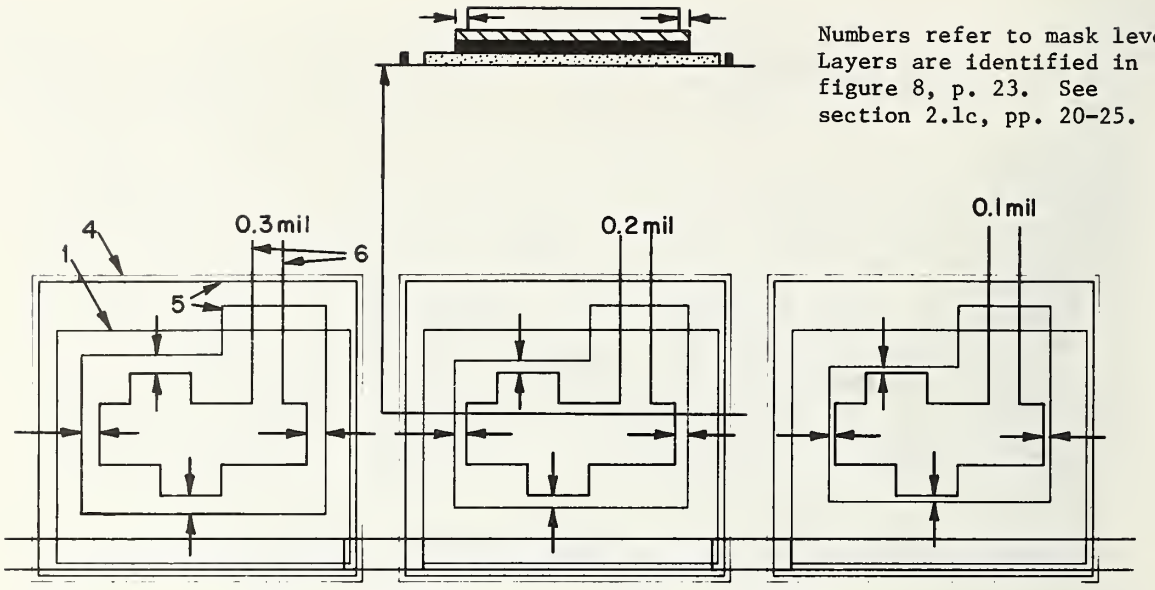


Figure 186. Electrical alignment test; type 5, test structure V-15, computer line drawing and cross section.

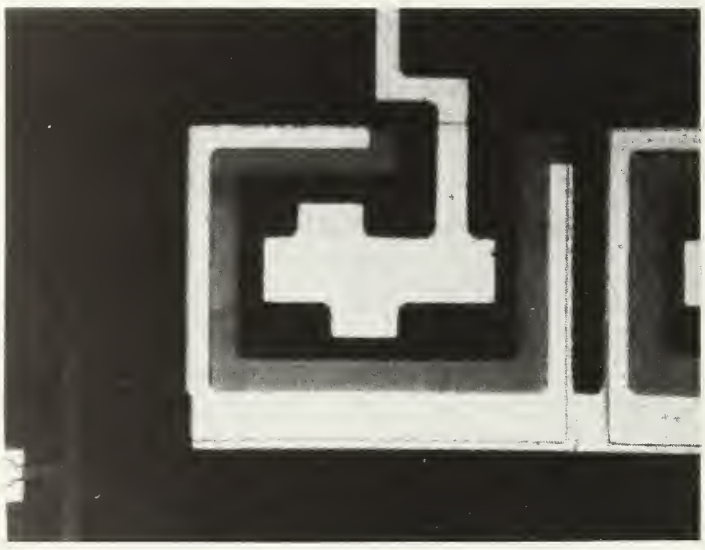
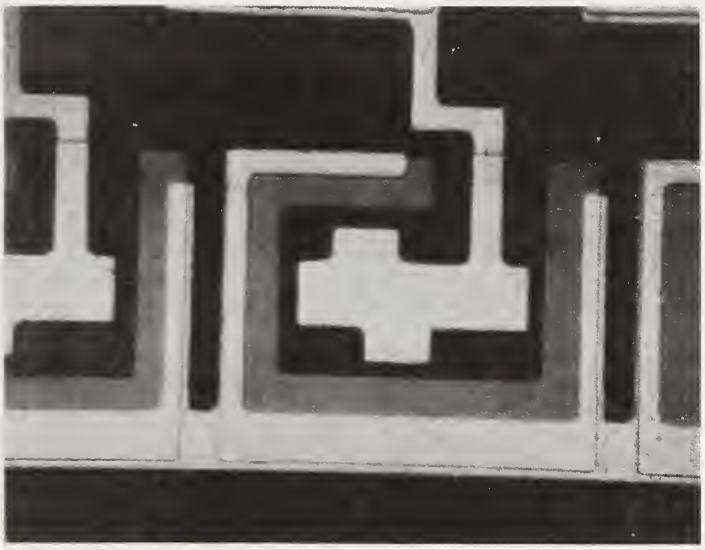
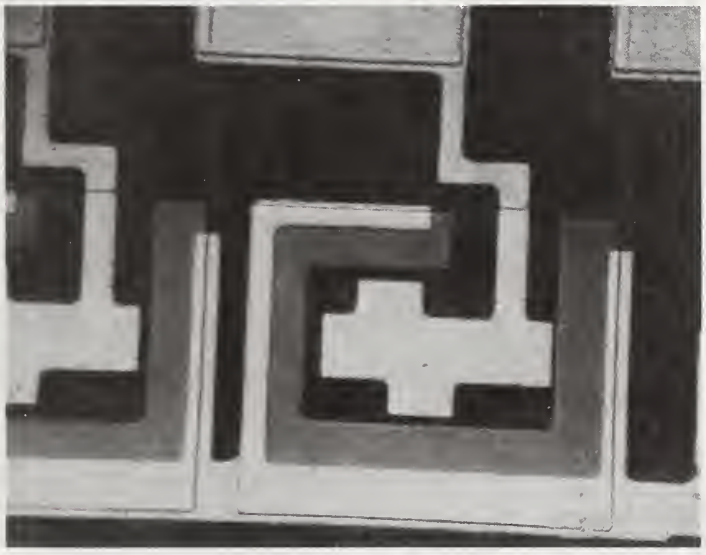


Figure 187.1. Photomicrographs, electrical alignment test; type 1, test structures V-9, V-11. (a) 0.3-mil Al-silicon.

Testing Method - All of these structures have the same basic operation. If the alignment is incorrect by more than the designed tolerance, the conductance between PRX and PCOM is much higher than when the alignment is correct. It is a general rule that the amount one knows about the details of the misalignment is directly proportional to the number of pads used for the test. In this case for a misalignment in any direction, a failure will occur. If one eliminates two of the sensitive points opposite each other, the failure indicates an x misalignment, for example. Two structures with two sensitive points each (3 pads) can distinguish between an x and a y misalignment. Four structures with one sensitive point each (5 pads) can distinguish between a positive or negative x or y misalignment. For complete information at three different sensitivities 4 x 3 + 1 = 13 pads are required. Therefore, with a complete set of all levels (10 possible alignments) 131 pads are required. This is



(b)



(c)

Figure 187.2. (Continued). (b) 0.2-mil Al-silicon and (c) 0.1-mil Al-silicon.

clearly prohibitive. We have chosen here to use seven different alignments at three different sensitivities for a total of 22 pads which is marginally acceptable. A failed structure simply says that the design sensitivity has been violated and says nothing about the direction. Usually this information is sufficient to determine the suitability of the alignment for alignment design rules; it says whether the total system is capable of 0.1-mil alignment. For example, the structure of subsection 3.42 creates a short between the Al and the silicon when they touch. Notice that the corners have been removed from the Al to avoid spurious contact at the inside silicon corners. Structure V-10 will conduct upon application of a voltage in excess of the dielectric strength of the oxide when the poly and the epi touch. Structures V-12, V-13 will conduct if the contact holes open the oxide over the silicon at the silicon edge. Structure V-14 normally has n+p+ junctions isolating the PRX from PCOM. If misalignment occurs, one edge of the silicon will be complete n+, thereby allowing a much higher conduction. Description 46 will allow the aluminum to contact diffused silicon if the aluminum crosses the contact hole edge.

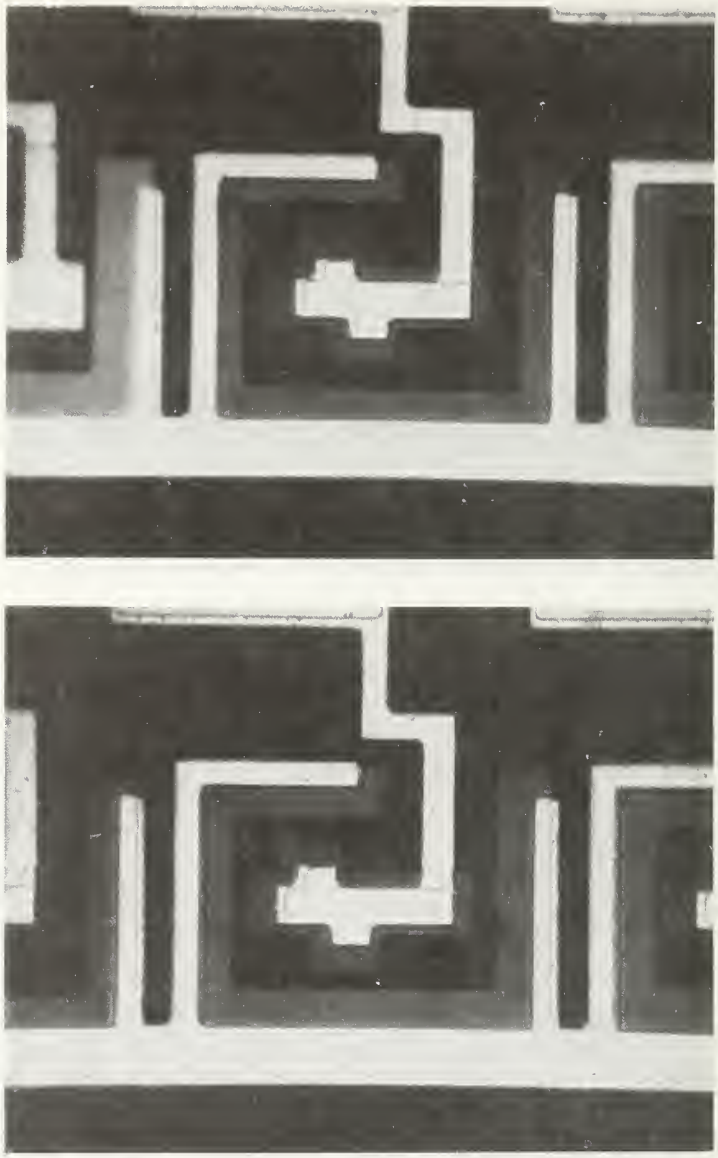


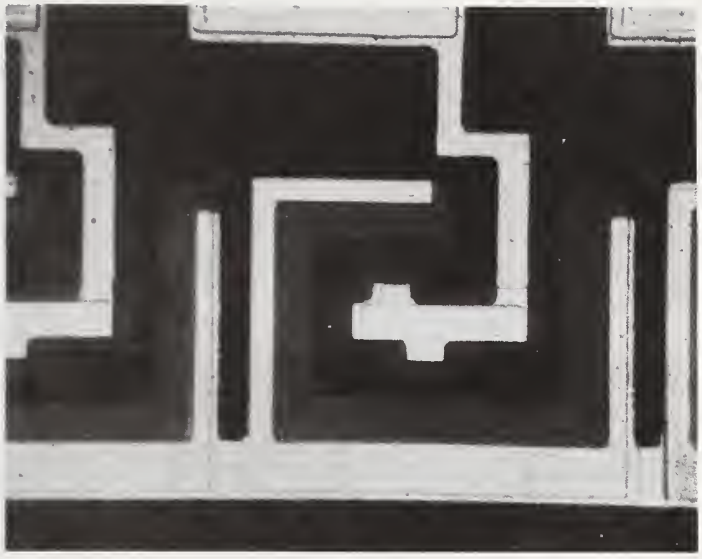
Figure 188.1. Photomicrographs, electrical alignment test; type 2, test structure V-10. (a) 0.3-mil poly-epi and (b) 0.2-mil poly-epi.

One of the most important features of these structures is that they reflect the success of the total process (including overetching and edge reflections, etc). More than just the misalignment is measured; the suitability of the process to produce a set of design rules is indicated.

Separation of the pure alignment component is done optically using the structures of subsection 3.49. With a very few exceptions the actual alignment should be measured optically.

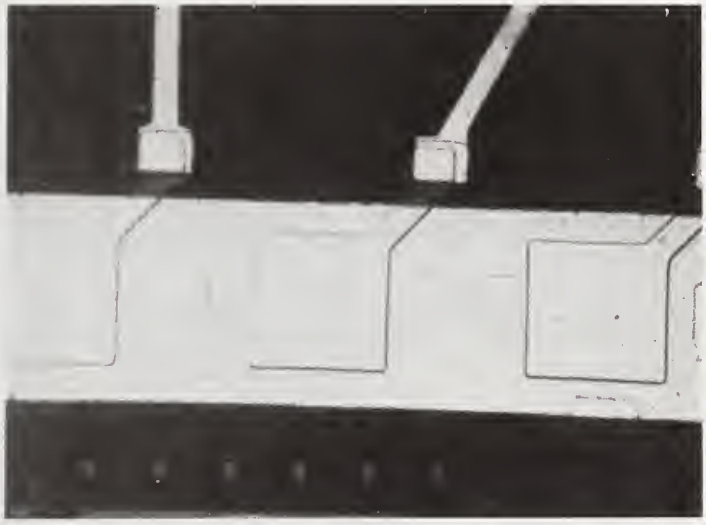
Samples of Data - No data have been acquired from these structures to date.

Potential Pitfalls - Some of the edges involved are not exactly as would appear in a typical circuit; therefore, edge reflections could affect the result slightly.



(c)

Figure 188.2. (Continued) (c) 0.1-mil poly-epi.

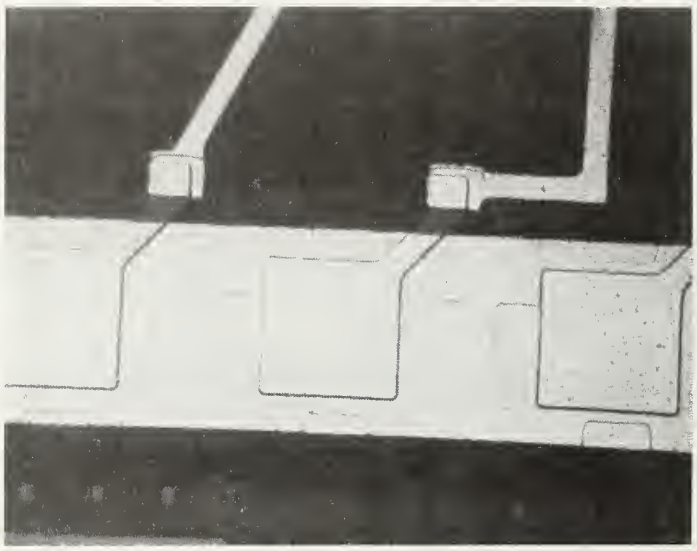


(a)

Figure 189.1. Photomicrographs, electrical alignment test; type 3, test structures V-12, V-13. (a) Good alignment for all spacings.

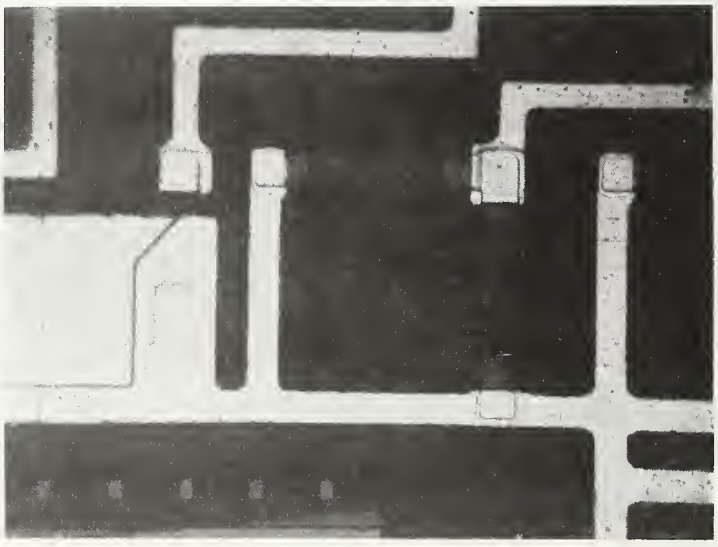
Overall Usefulness - Testing these structures can provide a very good idea of the capabilities of a process to produce the tolerance designed into the structures. Unfortunately most processes are capable of alignments much better than those allowed for here. Typically alignments of 0.05 mil are expected. These structures should be redesigned to have spacings of 0.1, 0.05, and 0.025 mil to be optimally useful. Currently testing should be limited to the 0.1-mil structure.

Other structures can be used for electrical alignment measurements on a continuous basis in some limited cases. For example, aluminum alignment to silicon can be detected by the capacitance ratio between the aluminum overlap onto one silicon edge and the overlap on a parallel silicon edge [16]. The greater the deviation of the ratio from 1.0, the greater the misalignment.



(c)

Figure 189.2. (Continued) (b) Failure at 0.1 mil.



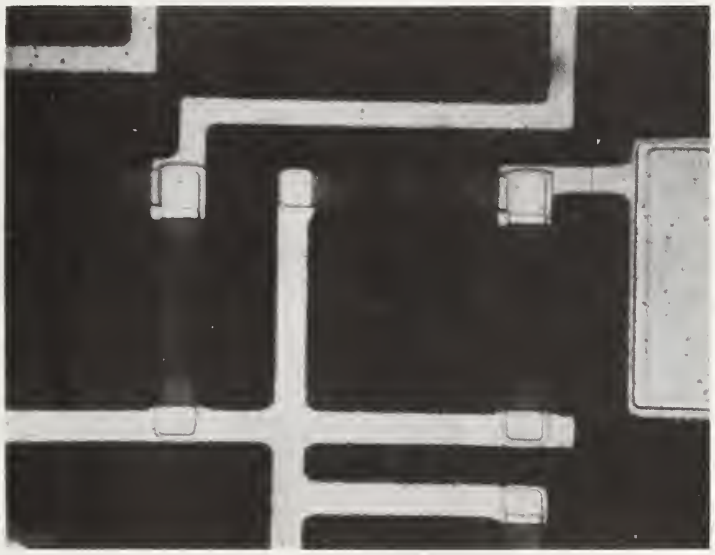
(a)

Figure 190.1. Photomicrographs, electrical alignment test; type 4, test structure V-14. (a) 0.3-mil n+ silicon (very hard to see).

A structure of this type requires only three terminals and gives continuous information and the direction of the misalignment for one direction only. A complete continuous representation of the alignment in both directions can be obtained from a perpendicular structure; a total of five pads is required. Similar continuous measurements between contacts and poly, diffusions, or silicon can be made by using a resistance ratio between nominally identical resistances defined by a contact in the center of a conductive strip.* The position of the contact is reflected in the resistance (or voltage) ratio. Both of these methods require assumptions of uniformity of other parameters such as oxide thickness or resistivity and are less direct than the methods used here.

Related Structures - The structures of subsections 3.41 and 3.49 are related to these devices.

*M.G. Buehler, private communication.



(b)

Figure 190.2. (Continued). (b) 0.2-mil n^+ silicon (very hard to see).

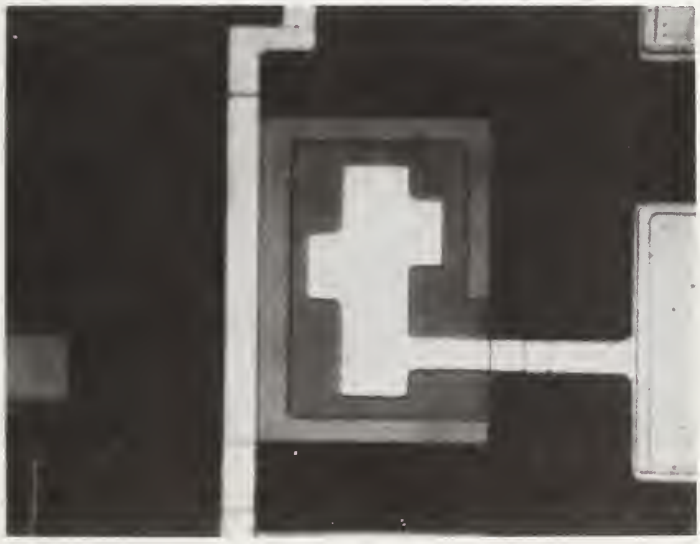
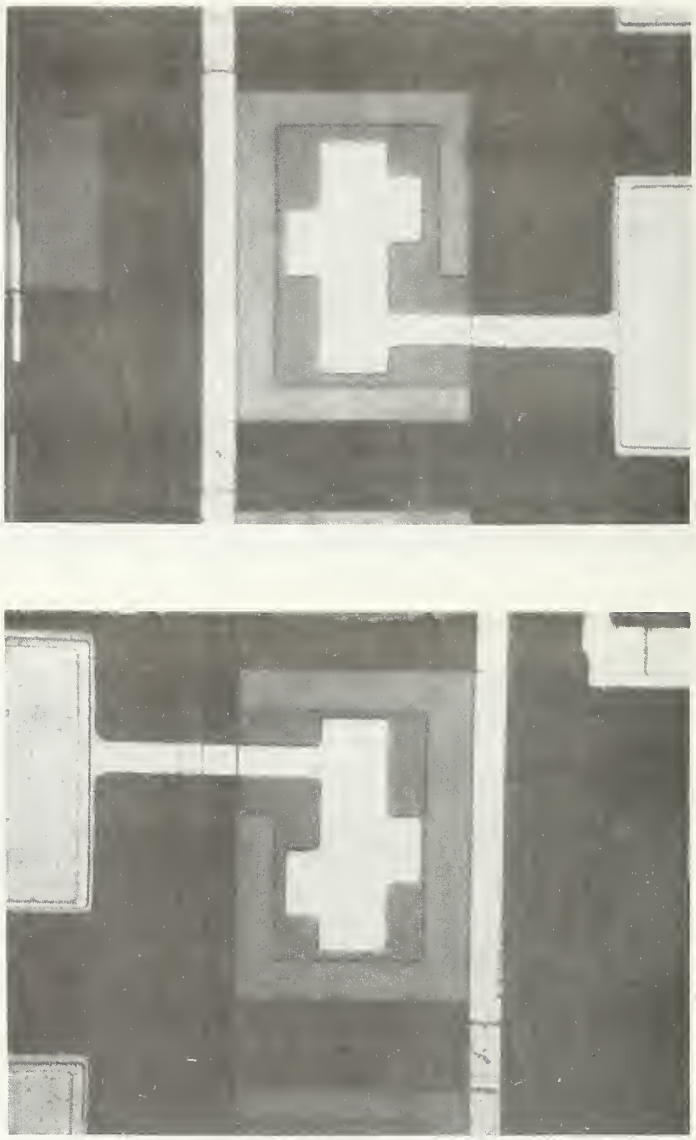


Figure 191.1. Photomicrographs, electrical alignment test; type 5, test structure V-15. (a) 0.3-mil Al-contact.



(b)

(c)

Figure 191.2. (Continued). (b) 0.2-mil Al-contact and (c) 0.1-mil Al-contact.

3.47 Two-Level Interaction; Sizes - V-16 through V-27

Purpose - These test structures measure the minimum size achievable and the actual size achieved.

Verbal Description - This structure contains strips of one level crossing the top of a slightly modified rectangle of another earlier level. These strips are of various sizes: 0.05, 0.1, 0.15, 0.2, 0.25, 0.3, 0.35, 0.4, 0.45, and 0.5. A length of at least 1.0 mil is included entirely on the top and on the supporting substrate. A device described in subsection 3.48 is also included as part of this structure.

3.48 Sizes; Single Level - V-28, V-29, V-30, V-31

Purpose - These test structures measure the actual size of the level achieved.

Verbal Description - This structure consists of four rectangles of material whose corners touch. The rectangles are 0.5 mil wide and 2.0 mil long. The center lines of the rectangles are 0.5 mil apart.

Line Drawing - The line drawings for the structures 3.47 and 3.48 are shown in figures 192 and 193, respectively.

Halftone Photograph - The photomicrograph is shown in figure 194.

Electrical Access - There is no electrical access.

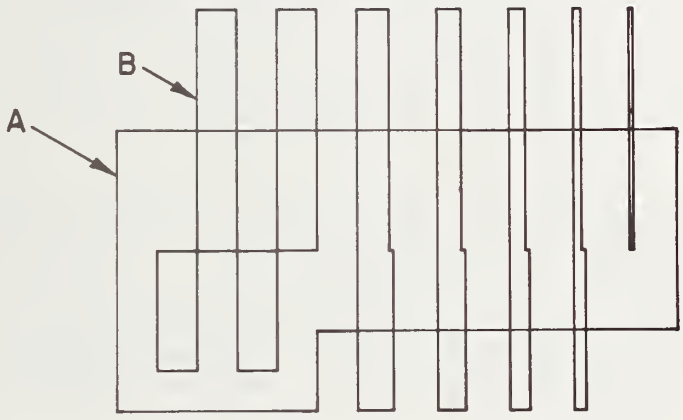


Figure 192. Two-level interaction; sizes, test structures V-16 through V-27, computer line drawing.

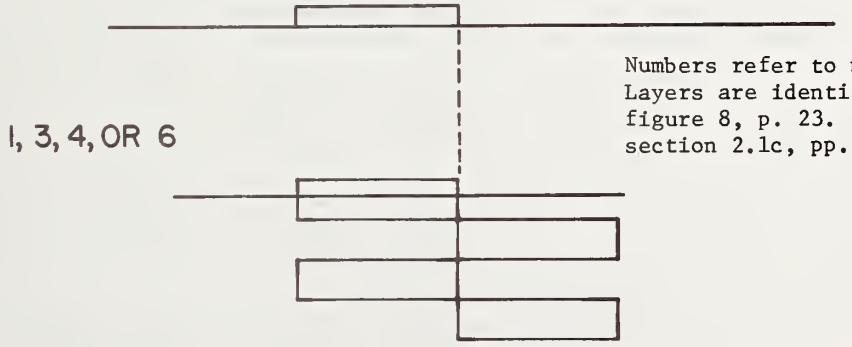


Figure 193. Sizes; single level, test structures V-28 through V-31, computer line drawing and cross section. Rectangles are 0.5 mil wide.

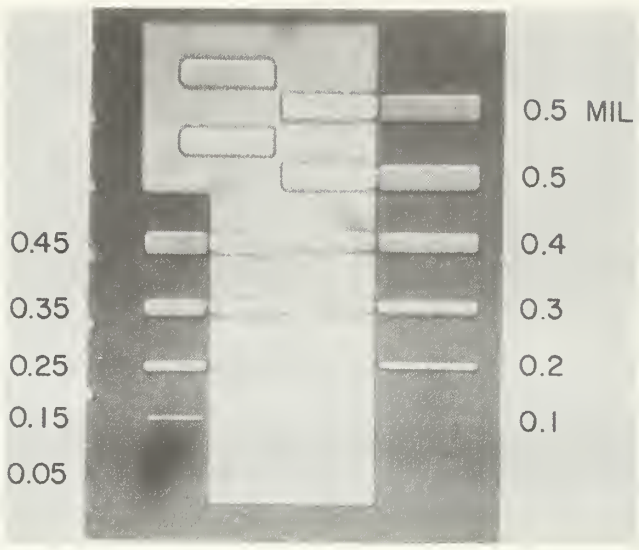


Figure 194. Photomicrograph, two-level interaction test structure.

Testing Method - These structures are tested by observing light reflected from the surface or transmitted through the substrate through an optical microscope. Structures V-16 through V-27 consist of two mask levels as illustrated in the line drawing. The strips are on top of the earlier mask level. A structure of the V-28 through V-31 type is seen at the top left of the line drawing; part of these structures extends across the earlier mask level of structures V-16 through V-27. The other part of structures V-28 through V-31 consists of strips of various width beginning with 0.05 mil and extending to 0.45 mil in 0.05-mil increments. These strips also cross the edge of the earlier mask level.

Structures V-28 through V-31 are intended to allow a quick but non-precise measurement of the dimensions of the later mask level. This measurement operates by using the fact that the center lines of the strips are a known distance apart. The deviation from perfect touching near the corners is compared with the known center-line distance to arrive at an estimate of the actual size achieved. This is shown in figure 195 for the case where the dimensions are smaller than the designed dimensions. Structures V-16 through V-27 also allow determination of the minimum dimensions in the three cases: (1) upper level confined entirely to lower level; (2) upper level confined entirely to substrate or background; and (3) upper level crossing lower level edge.

Samples of Data - Figure 194 shows a typical use of this structure. This photograph shows the two-level interaction test structure for p+ polysilicon over epitaxial silicon. Several points are quite clear and are immediately seen from this structure.

- The poly is smaller than its designed dimension by ∿0.05 mil on a side. (This is seen from the structure V-28 through V-31 segment.)
- The dimensions on top of the epi and on top of the sapphire are nearly identical.
- No poly remains for designed dimensions less than 0.1 mil.
- A severe distortion in the poly is seen at the edge of the epi silicon.
- A discontinuity in the poly at the edge of the epi silicon exists for poly less than or possibly equal to 0.3 mil.
- The sharp 0.05-mil step at the center of the strip is very "smeared out."

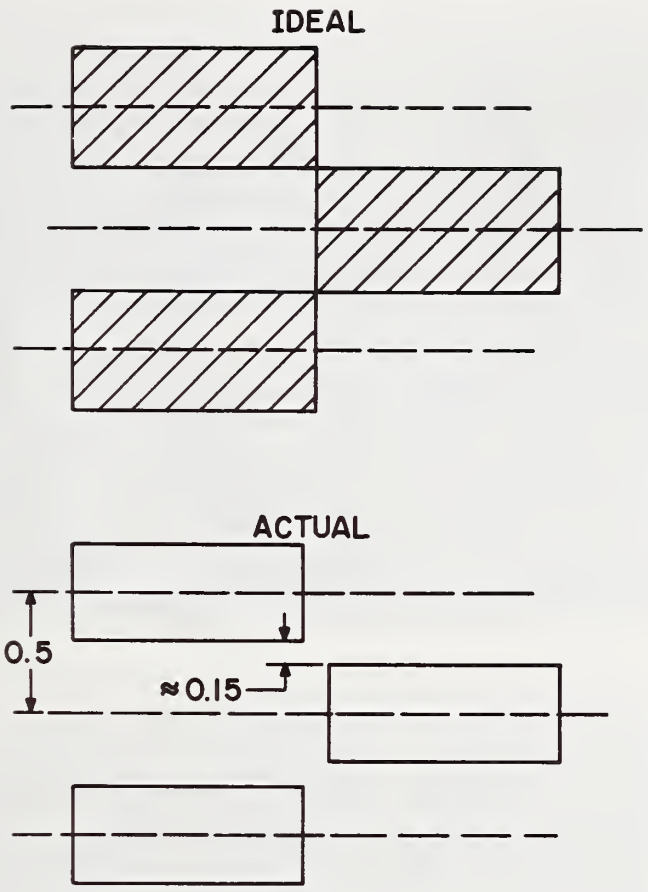


Figure 195. Operation of structures V-28 through V-31. Dimensions are in mil.

A complete set of data from one pellet is shown in figures 196 and 197. We notice in these figures that some types of strips are present at all sizes while other types are present only for the larger sizes. Perhaps the most noticeable effects are the blooming in structures V-17 and V-19 and the shrinking observed on the contact holes over bare sapphire. The aluminum on top of silicon is smaller than that on bare sapphire.

Potential Pitfalls - If strong effects are seen at the corners of structures V-28 through V-31, it may be difficult to use this structure as intended. In this case, actual measurement instead of visual estimation would be made.

Overall Usefulness - These structures are extremely useful for determining the absolute limits of line definition (with a 0.05-mil resolution). Any failures observed here would certainly cause failures in a circuit. Success here does not guarantee success in a circuit, but it provides a definite lower limit beyond which failure is certain. This structure is much more powerful than a simple line width measurement since it also takes into account the absolutely critical interactions between two levels, and the possibility of different line widths being obtained from the same mask and the same etching, etc, but on different surfaces. These are most strongly seen at the edge of the lower level. It would have been valuable to include some "spacing" interactions in addition to the "strip" interactions. These can be important for conductors crossing edges, for example. Some of these on various "spacings" can be obtained from the structure of subsection 3.41. A negative print of the upper level mask would form a "spacing" structure. This was omitted primarily because of space limitations, but the author now believes that these should have been included for completeness. Otherwise no changes are recommended.

Related Structures - The structures of subsections 3.41 and 3.49 are closely related to these structures.

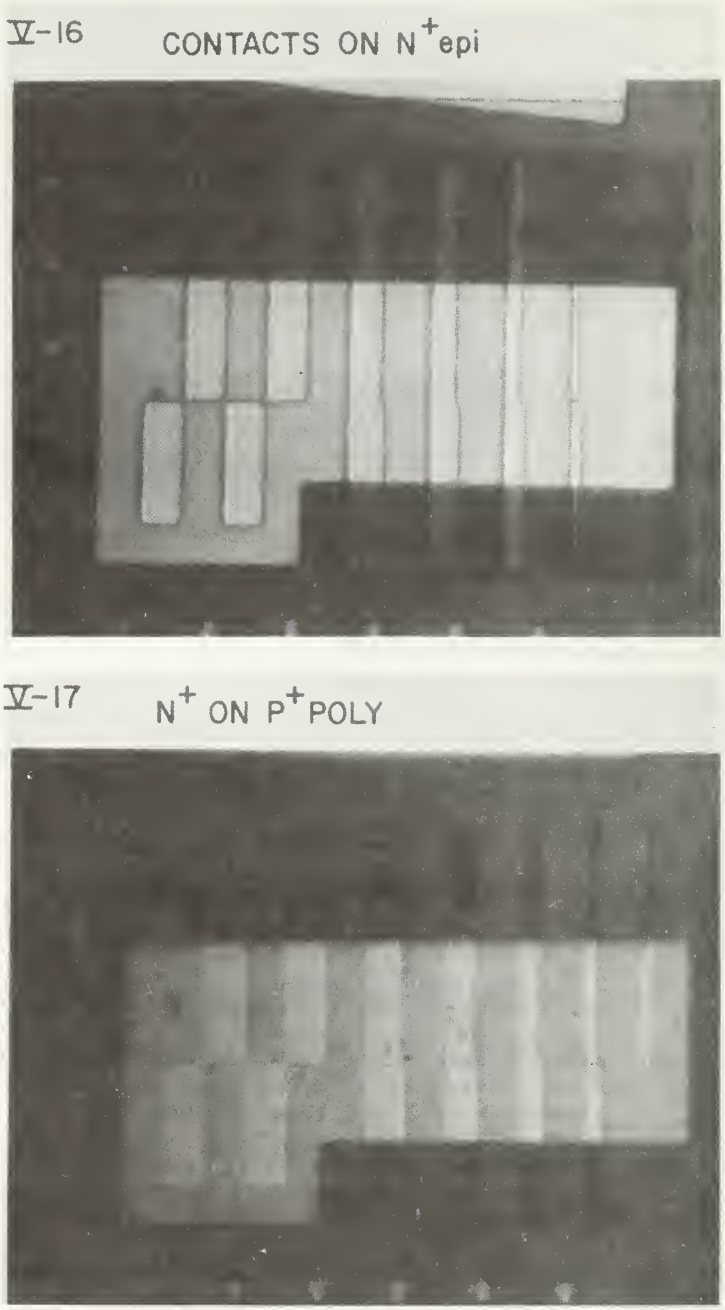
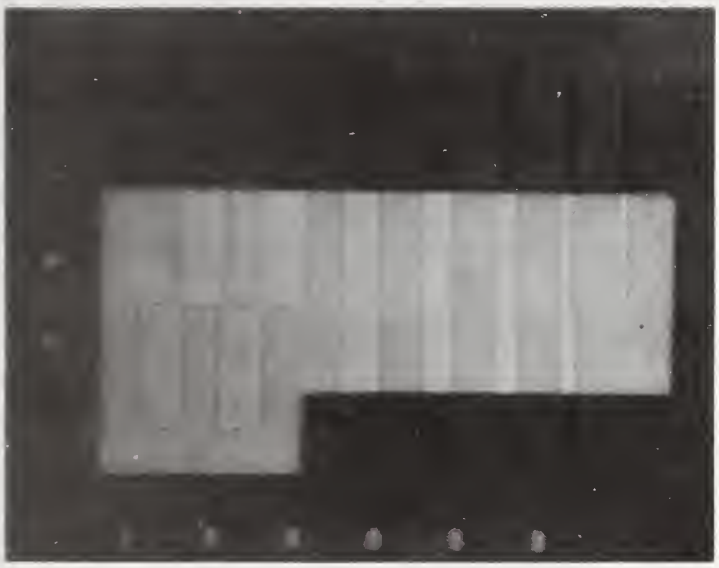


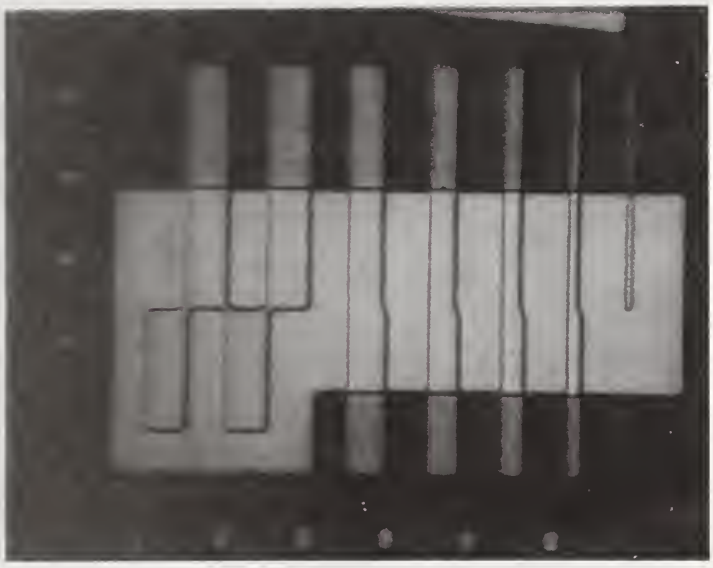
Figure 196.1. Photomicrographs, test structures V-16 through V-27, complete data. (a) Contacts on n+ epi and (b) n+ on p+ poly.

V-18 N^+ ON P^+epi



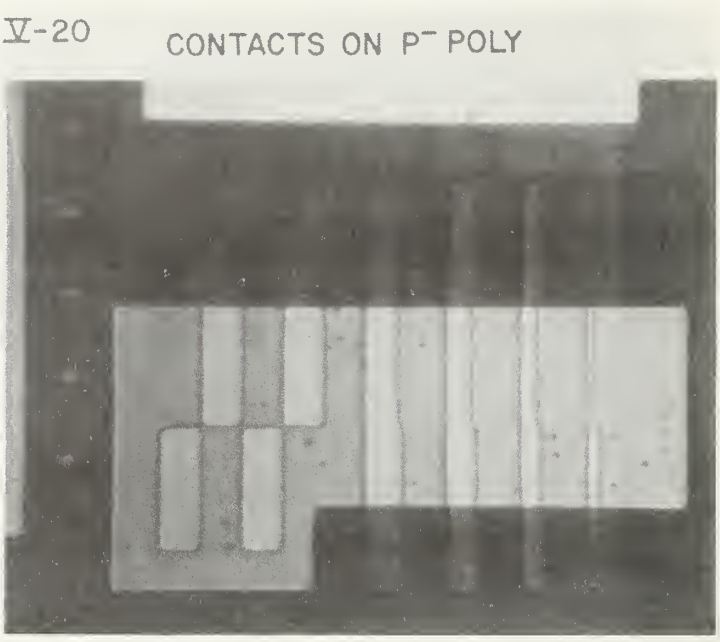
(c)

V-19 POLY ON epi

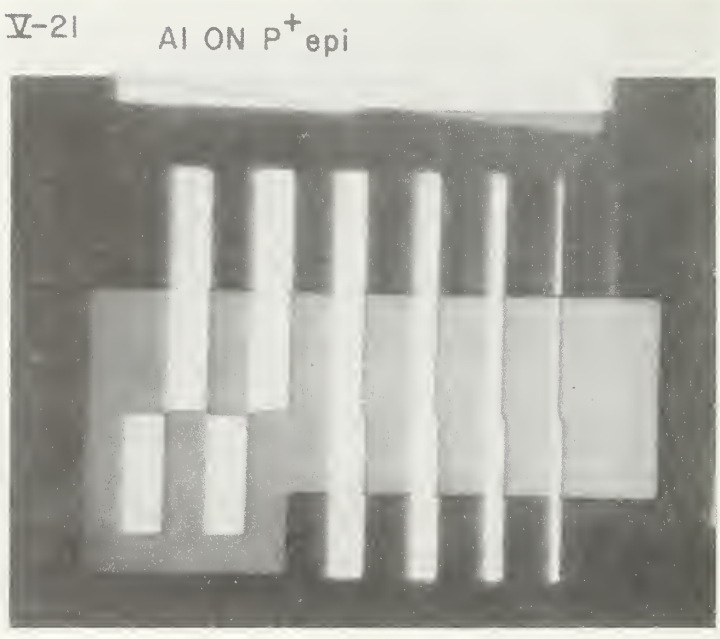


(d)

Figure 196.2. (Continued). (c) n+ on p+ epi and (d) poly on epi.

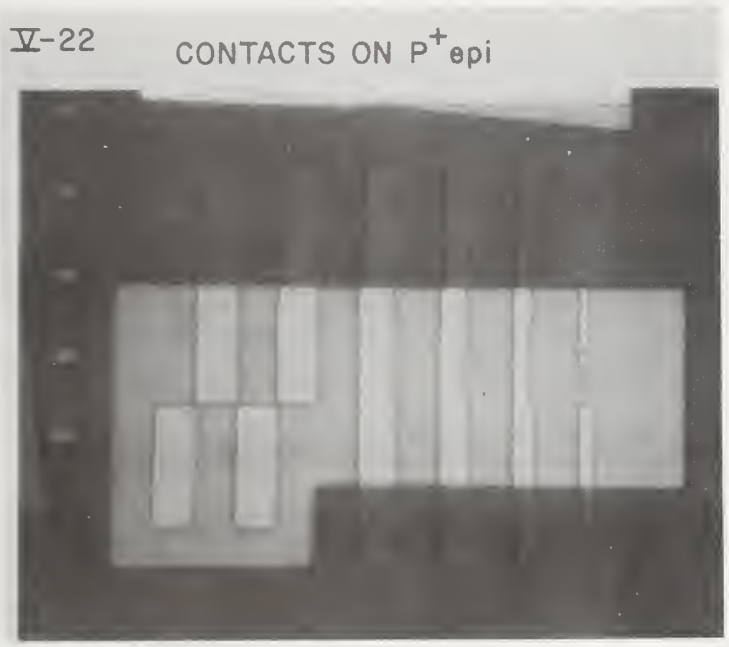


(e)

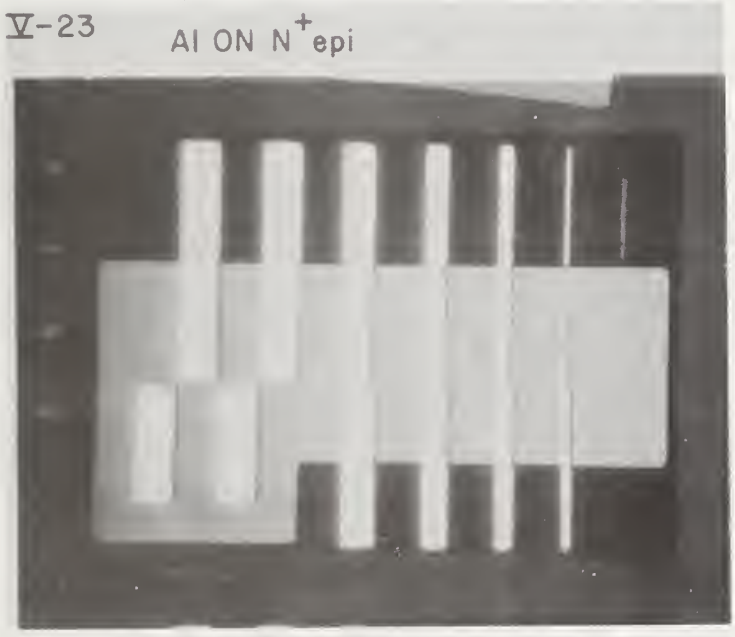


(f)

Figure 196.3. (Continued). (e) Contacts on p+ poly and (f) Al on p+ epi.

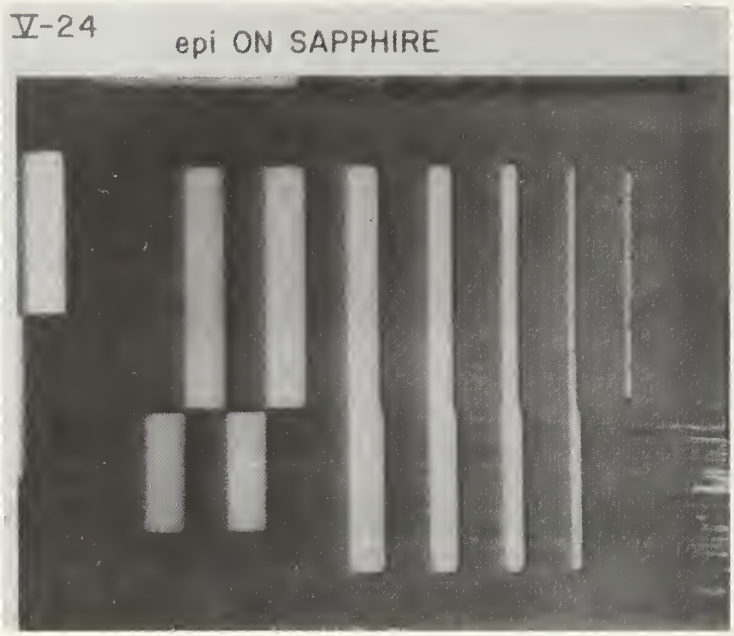


(g)

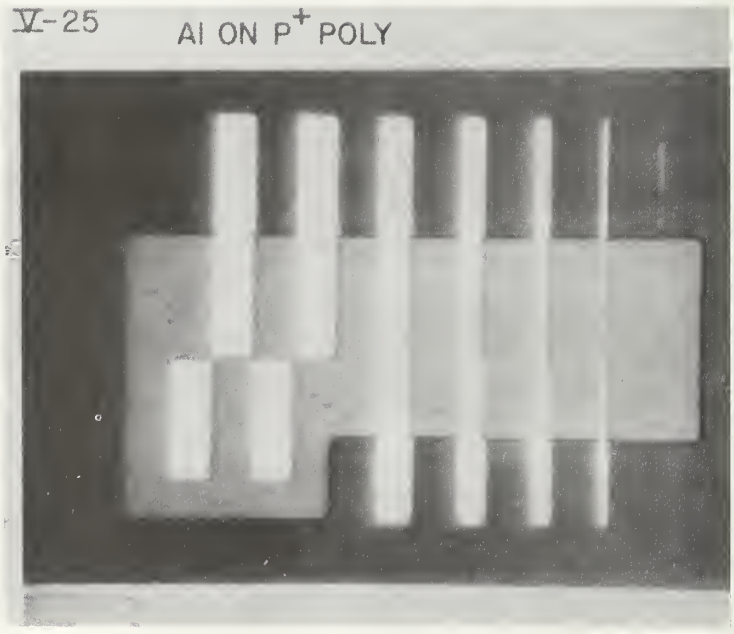


(h)

Figure 196.4. (Continued). (g) Contacts on p+ epi and (h) Al on n+ epi.

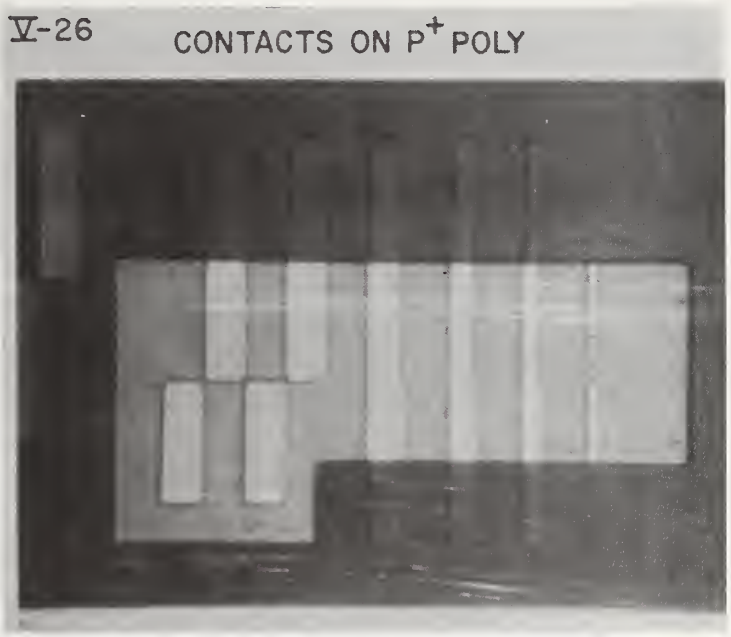


(i)

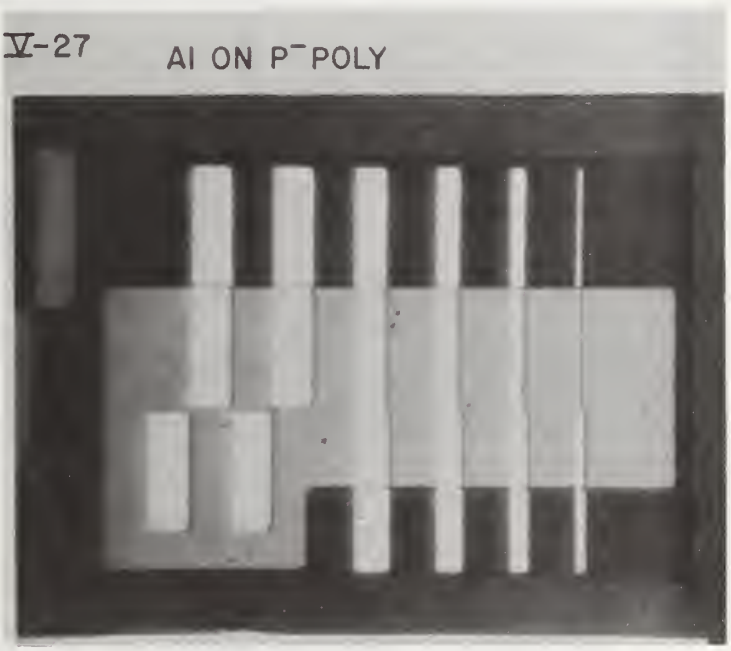


(j)

Figure 196.5. (Continued). (i) Epi on sapphire and (j) Al on p+ poly.



(k)



(l)

Figure 196.6. (Continued). (k) Contacts on p+ poly and (l) Al on p- poly.

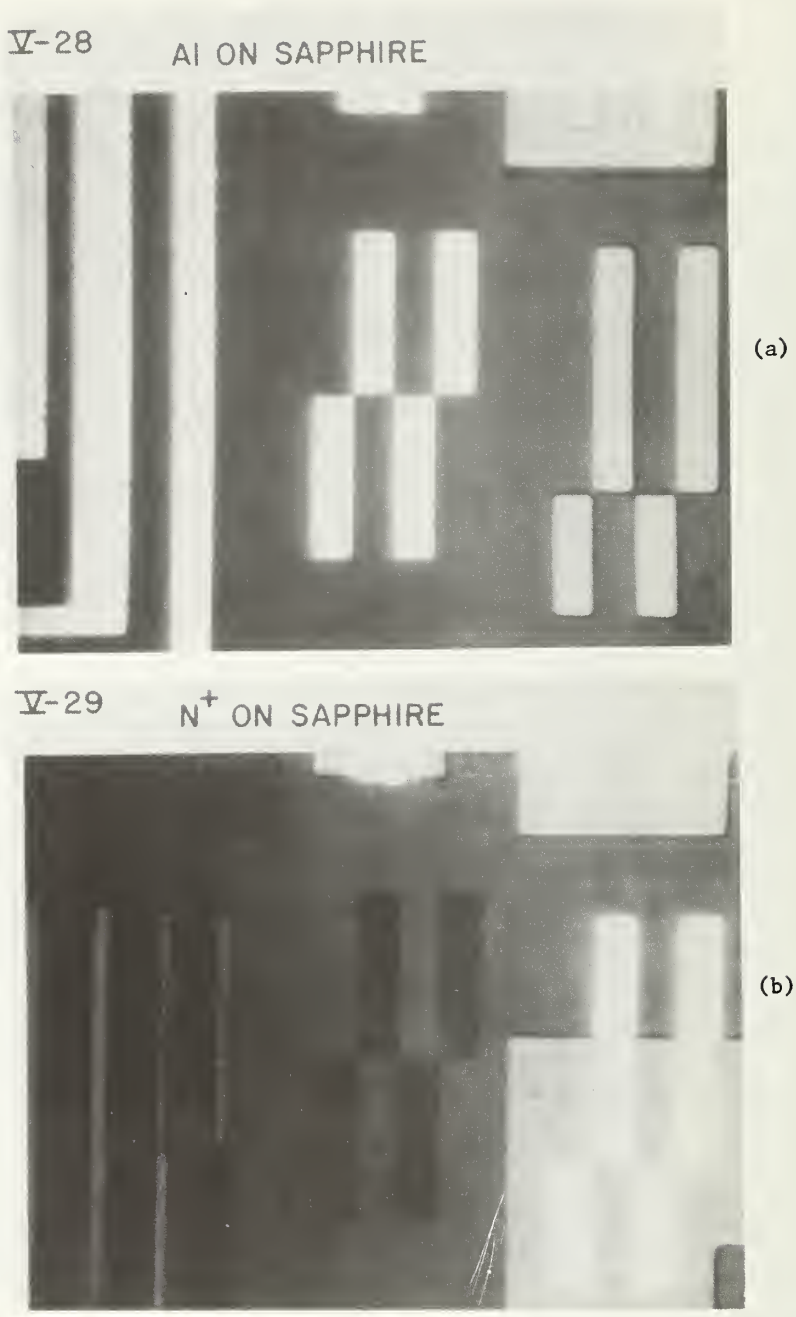


Figure 197.1. Photomicrographs, test structures V-28 through V-31, complete data. (a) Al on sapphire and (b) n+ on sapphire.

Figure 197.2. (Continued). (c) Poly on sapphire and (d) epi on sapphire.

3.49 Two-Level Interaction; Alignment - V-32 through V-39

Purpose - These test structures optically measure the alignment between two levels.

Verbal Description - This structure consists of a rectangle and a trapezoid overlaid on each other. The trapezoid has sides sloped at 5.71° off orthogonal. The rectangle is 1.0 x 6.0 mil. Small rectangles of silicon 0.2 x 0.3 mil are spaced at 1.0-mil intervals parallel to the major axis.

Line Drawing - The line drawings for this structure are shown in figures 198 and 199.

Halftone Photograph - The photomicrograph for this structure is shown in figure 200.

Electrical Access - There is no electrical access.

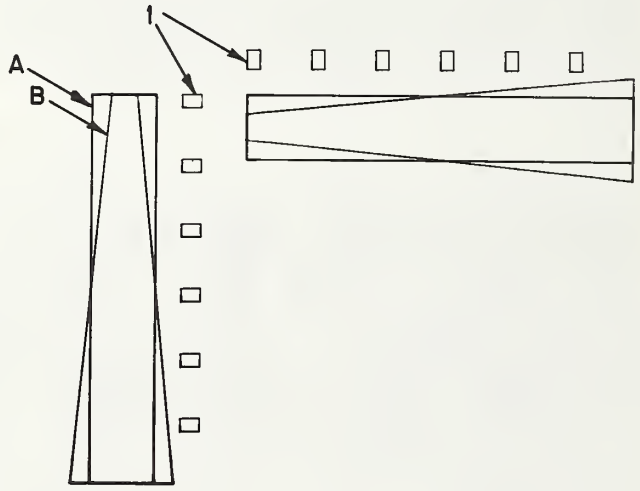


Figure 198. Two-level interaction; alignment, test structures V-32 through V-39, computer line drawing.

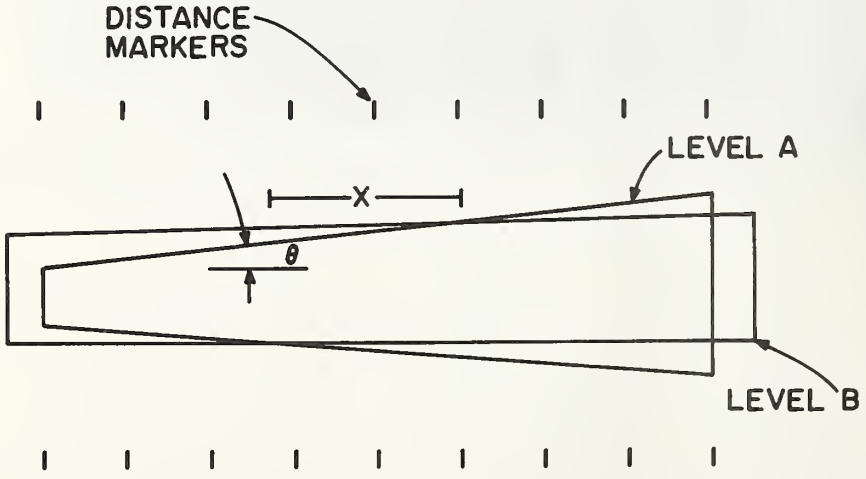


Figure 199. Operation of structures V-32 through V-39.

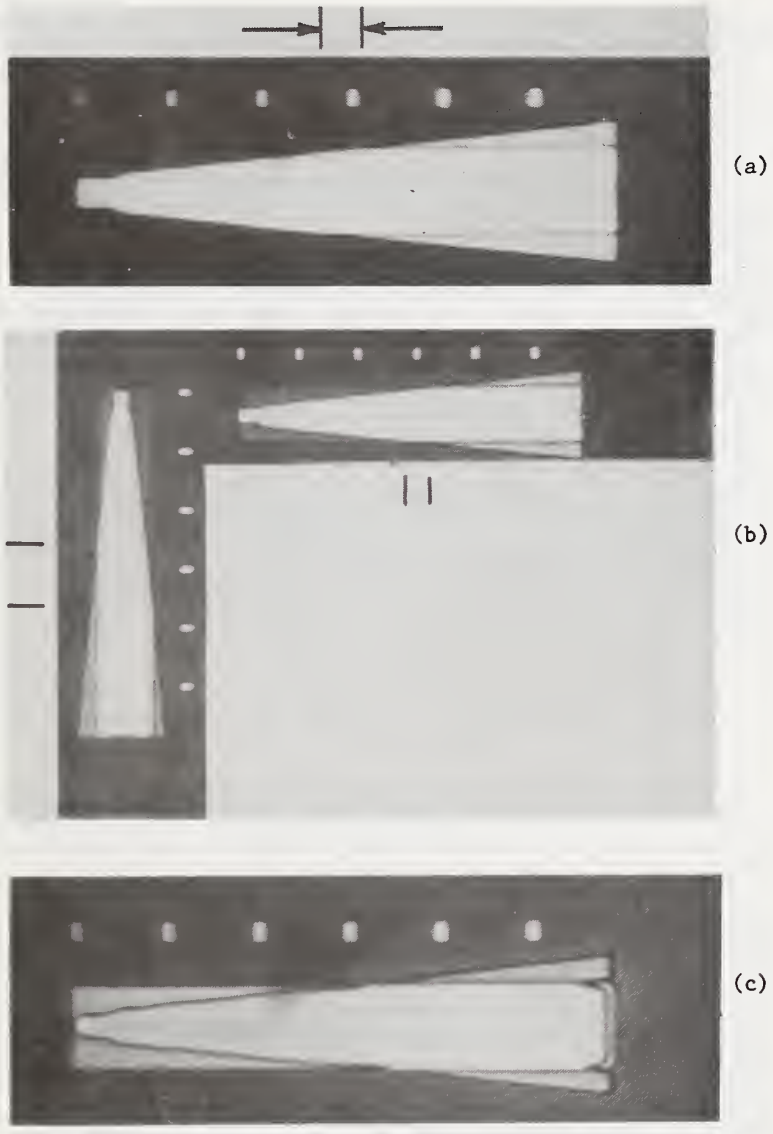


Figure 200. Photomicrographs, two-level test alignment structures V-32 through V-39. (a) Single structure, (b) orthogonal pair, and (c) two-level alignment structure where edge crossing is not ideal.

Testing Method - This structure is tested by observing reflected or transmitted light through an optical microscope (preferably with a filar eyepiece). The device operates by noting the intersection points of the upper level with respect to the lower level as shown in figure 199 and as described in ref. 20. The distance between the longitudinal axes of the rectangle (level B) and the trapezoid (level A) (which is the misalignment in the y direction) is given by:

$$\Delta = 2X/\tan\theta \qquad (48)$$

as a simple geometrical argument will show. Figure 200 shows an example of this structure. It is clear that no difficulty exists in determining the intersection point where the trapezoid crosses the rectangle. In figure 200(a) we note a difference of approximately 0.4 mil, which corresponds to an actual misalignment of 0.02 mil or 20 μin. Similar clarity persists when an orthogonal pair of structures for complete alignment measurement is used. The rotational misalignment between the two levels is usually negligible. The order of the

20. Ham, W. E., "Hetero-Geometrical Patterns and Method for Measuring Misalignment Between Two Integrated Circuit Masks Using Same," RCA Technical Notes No. 1166 (Sept 1976).

rotational misalignment can be seen from a rough calculation. Suppose a relatively gross misalignment of 1.0 mil existed across a 2.0-in.-diameter wafer. The rotational misalignment in this case is $\tan^{-1}$ (1/2000) = 0.0286°, which is obviously completely negligible.

Figure 200(c) shows this same structure where the edge crossing is not ideal. Since both sides of the structure deviate in precisely the same way, no loss of accuracy exists. In fact, it is even easier in this particular case to measure the crossing points than when the crossing is ideal.

It is also of interest that at least one order of magnitude smaller misalignment could be detected. This means that misalignments on the order of 1 μin. = (2.54×10^{-2} μm = 254 Å) are measurable with this structure using an ordinary microscope. This structure could also be used as a very accurate ruler to measure the change in the size of an object (such as a wafer) after some processing step or with temperature. In this case, the upper level would not necessarily be printed but could be simply observed. This is discussed more fully in "Overall Usefulness" below.

One of the most important features of this structure is that uniformly shrinking or expanding either level does not affect the accuracy of the alignment measurement. It changes the position of the crossing point but does not change the *difference* between the two crossing points. The structure is therefore independent of the method used to form the images. It is also independent of the slope of the edges of the films on the wafers.

Crude measurements can be made by comparing the intersection points with the distance markers on the wafer surface. This can provide perhaps 1.5 digits of accuracy for X values greater than one distance marker. A preferred method, though more time consuming, is to use a filar eyepiece to measure the intersection points. The hair line is placed perpendicular to the rectangle edges.

Samples of Data - Figure 201 shows a set of these alignment structures for all of the levels present on one pellet. We note that in several of the structures the edge crossing is not ideal. We also note that this structure provides a continuous variation of the edge-to-edge spacing and in a sense is a continuous design rule test.

Figure 202 shows how these structures can be used to characterize a process in terms of its alignment capabilities. Data are gathered across the major diameters of the wafer for both the structure perpendicular to the direction of travel and the structure parallel to the direction of travel. Those structures which are parallel to the direction of travel indicate "theta (θ)" errors while those perpendicular to the direction of travel indicate "runout (RO)" errors. Of course, simple translational errors may also exist. The actual theta and runout error is given by the difference between different points on the wafer. Thus, the slope of the curves of figure 202 indicate the theta error (top two curves) and the runout error (bottom two curves).

It is quite clear that more than simple theta, runout, and translational error exists for this data sample; the lowest curve particularly shows that the runout is not linear. This particular wafer suffers from all three types of error with the translational error being the most severe. If 0.050-mil design rules were being used, only the circuits on the bottom part of this wafer would have a good chance of working. This clearly illustrates the power of this type of investigation.

Potential Pitfalls - One must be careful to be consistent in the criteria used to determine the edge-crossing point. The same criteria must be used on both intersections for best results.

Overall Usefulness - This structure is extremely valuable for separating the pure alignment components of the process. It does not use any models or assumptions (other than *uniform* deviations from expected dimensions). Typical resolution is 1.0 μin. with some types producing perhaps 0.5 μin. This is well beyond the capabilities of normal filar eyepiece measurements.

The most serious drawback to this structure is that it is not directly connectable to a computer. This makes data acquisition relatively time-consuming.

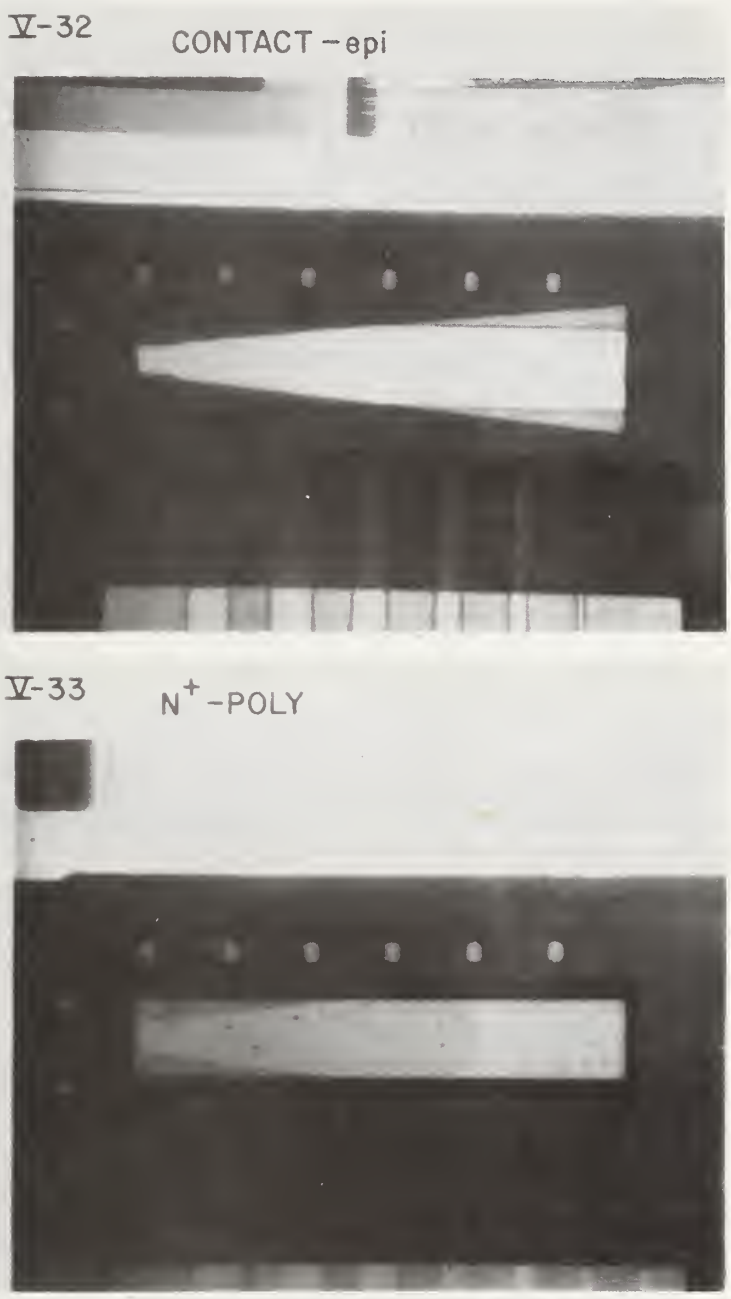


Figure 201.1. Photomicrographs, test structures V-32 through V-39, complete data. (a) Contact-epi and (b) n+-poly

Another use of this structure is as a very accurate ruler to measure the change in the actual sizes of wafers after processing steps. For example, when the epi is etched into islands, the substrate may change size due to the forces of the epi no longer being present. This can be measured by using the same mask (at exactly the same temperature, of course) that was used to form the first level. This might be implemented, for example, as follows:

- Etch rectangles in the epi.
- Expose and develop photoresist with the trapezoids in the same mask as used for the rectangles (these trapezoids should be placed as close as possible to the rectangles on the mask).

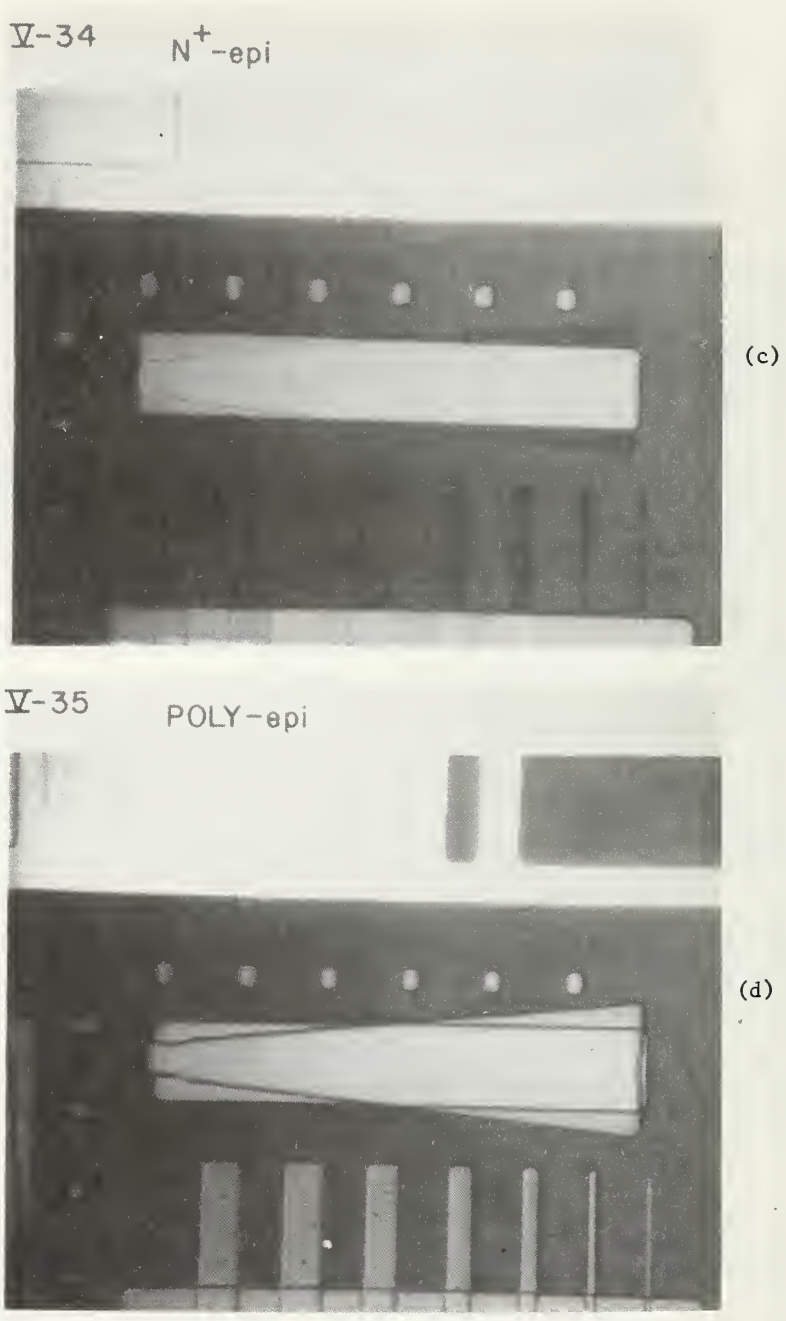


Figure 201.2. (Continued). (c) n+-epi and (d) poly-epi.

- Measure the misalignments. Since the rectangles were defined *before* the etch, they will move with the substrate during the etch.

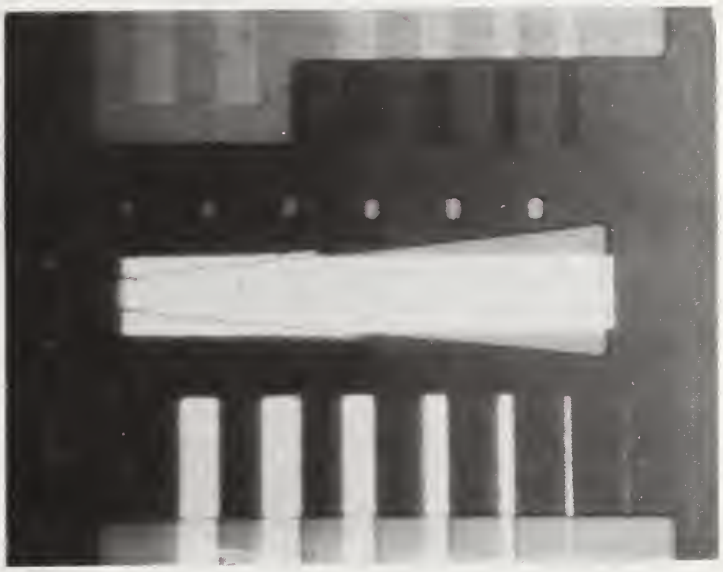
Any deviations between adjacent structures are then due to the wafer actually changing size during the processing step. This type of effect can be important at large wafer sizes.

Related Structures - This structure is related to those of subsection 3.41.

V-36 CONTACT-METAL

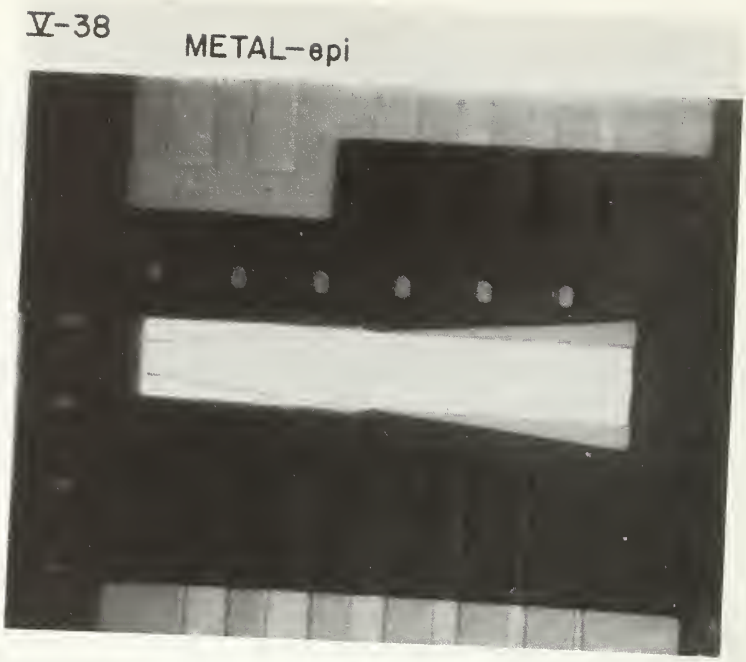
(e)

V-37 METAL-POLY

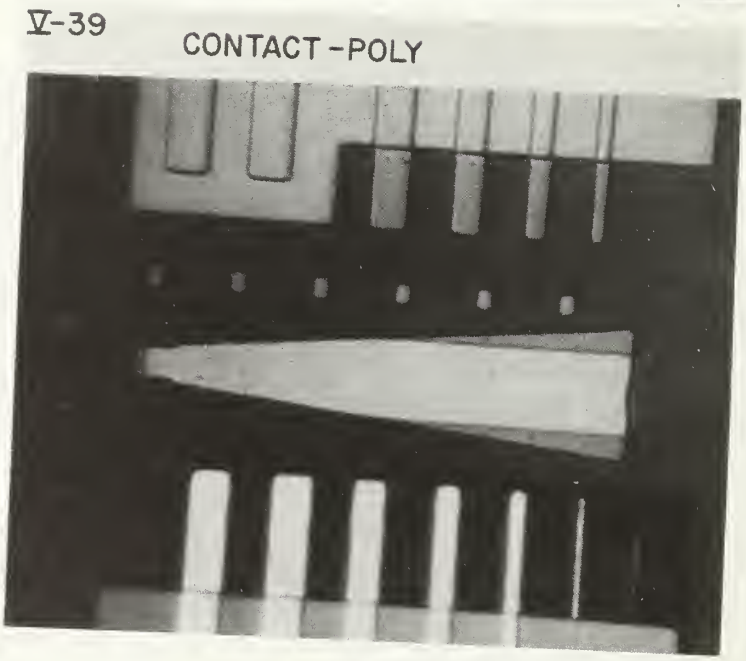


(f)

Figure 201.3. (Continued). (e) Contact-metal and (f) metal-poly.



(g)



(h)

Figure 201.4. (Continued). (g) Metal-epi and (h) contact-poly.

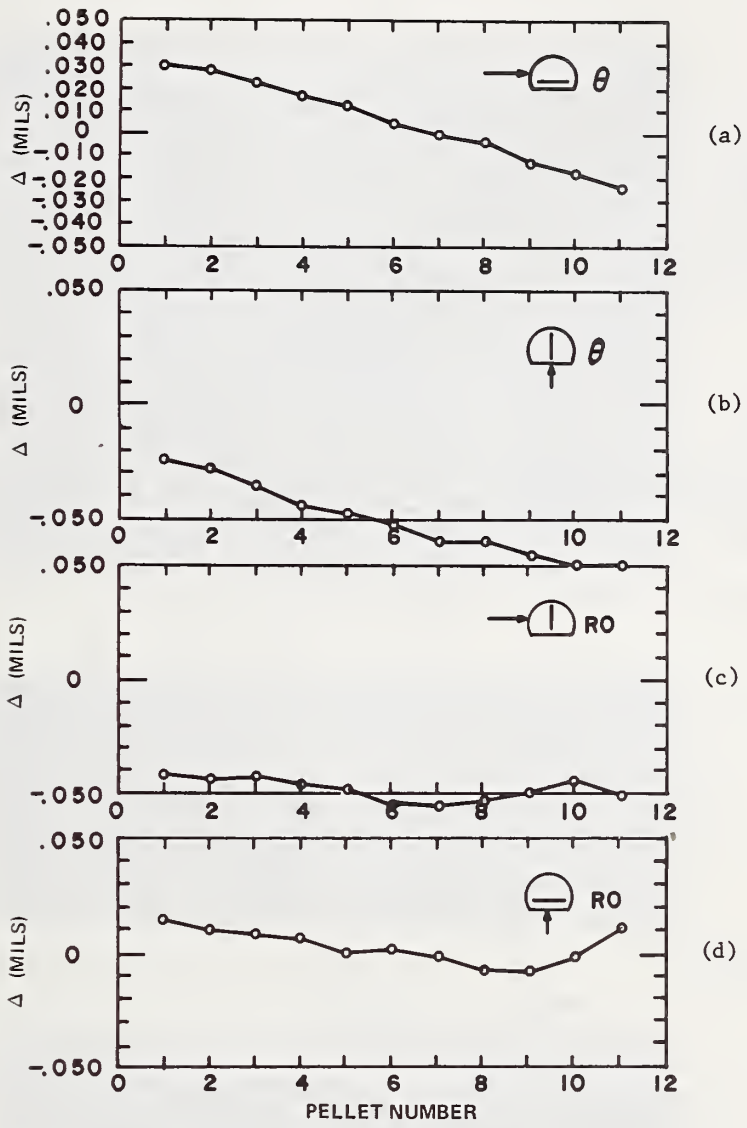


Figure 202. (a) Misalignment across a 3-in. wafer using the structure with the major axis of the structure parallel to the direction of travel of the probing machine; (b) Misalignment across a 3-in. wafer as in (a) but in a perpendicular direction of travel; (c) Misalignment across a 3-in. wafer using the structure with the major axis of the structure perpendicular to the direction of travel; (d) Misalignment across a 3-in. wafer as in (c) but in a perpendicular direction of travel. Δ is given in mil. See text for discussion.

3.50 Alignment Key; l-Shaped - V-40

Purpose - This test structure serves as an alignment key.

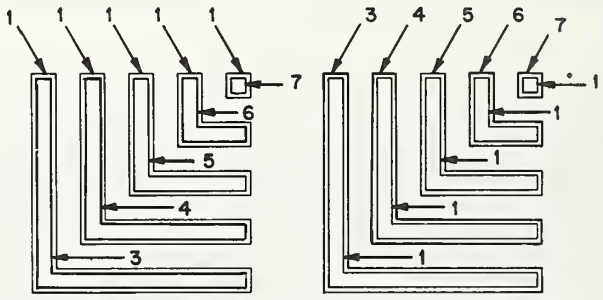
Verbal Description - This structure consists of "L's" of each level. All levels are referred to the first level. In one set of "L's" the first level is larger than the subsequent levels by 0.1 mil on all sides. In this set the first level is 0.5 mil wide and the subsequent levels are 0.3 mil wide. The "L's" are nested such that the earlier mask levels are largest (4.5 mil on a side). The other set is identical to the first except that the first level is smaller than the subsequent level by 0.1 mil.

3.51 Alignment Key; Squares - V-41

Purpose - As structure V-40, this test structure serves as an alignment key.

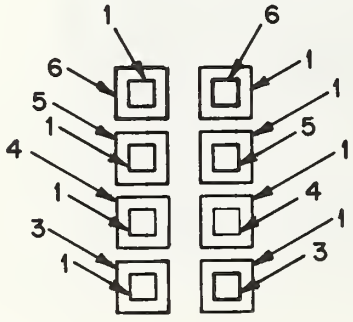
Verbal Description - This structure consists of squares of the various levels. All subsequent levels are referred to the first level. In one set the first level is larger than the subsequent levels (0.8 - 0.4 mil). In the other set the first level is smaller than the subsequent levels by 0.2 mil on a side (0.4 - 0.8 mil).

Line Drawing - The line drawings are shown in figures 203 and 204.



Layers are identified in figure 8, p. 23. Numbers refer to mask levels. See section 2.1c, pp. 20-25.

Figure 203. Alignment key; L-shaped, test structure V-40, computer line drawing.



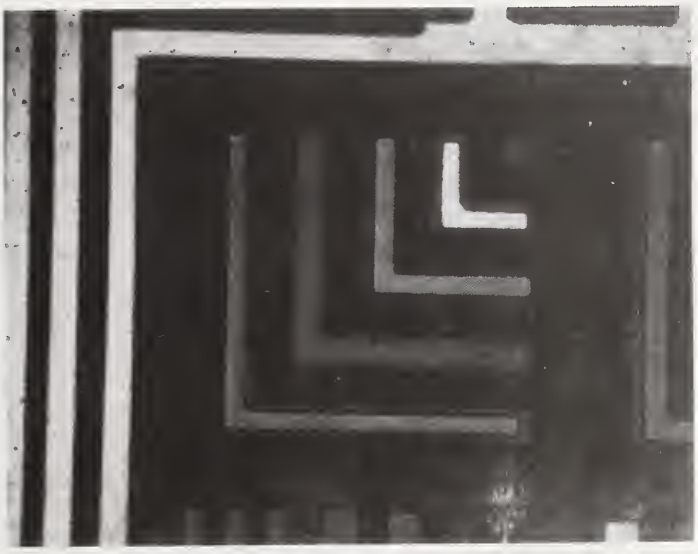
Layers are identified in figure 8, p. 23. Numbers refer to mask levels. Larger squares are 0.8 mil on a side. See section 2.1c, pp. 20-25

Figure 204. Alignment key; squares, test structure V-41, computer line drawing.

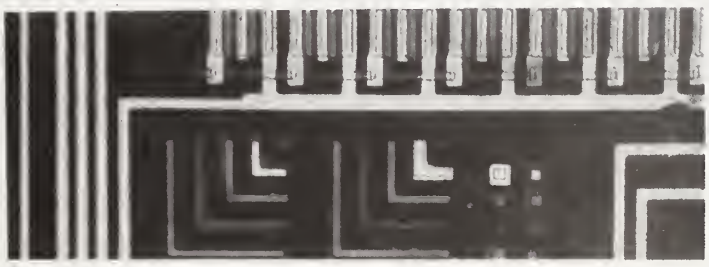
Halftone Photograph - The photomicrographs are shown in figures 205 and 206.

Electrical Access - There is no electrical access.

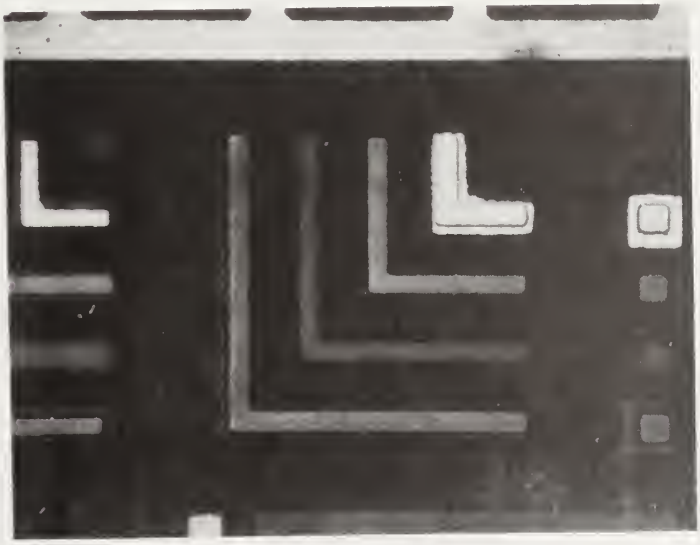
Testing Method - These structures are used for actually fabricating the test pattern. Both types can be used for either positive or negative working photoresist. The L-shaped keys are the most commonly used but require a somewhat larger area than the squares. When using the L-shaped keys, the eye must focus on each arm separately during the alignment while only one focus is needed for the squares. Also the space between levels is not always large



(a)



(b)



(c)

Figure 205. Photomicrographs, alignment key; L-shaped, test structure V-40,
(a) "L" alignment structure,
(b) complete structure, and
(c) opposite tone structure compared with (a).

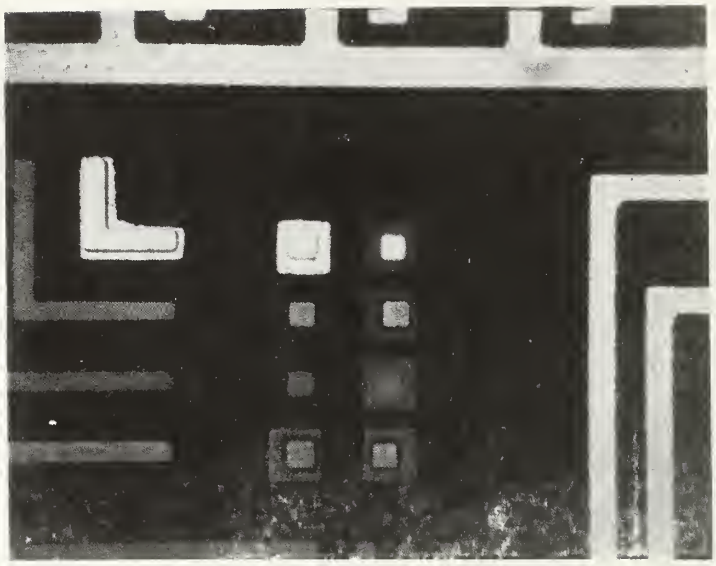


Figure 206. Photomicrograph, square alignment structure, V-41.

enough to see the alignment accurately with the L's. Examination of the photomicrographs shows that it is quite clear at a glance when the alignment is not correct from the squares, while the L's require some studying. Quantitative comparison of the alignment accuracies achieved can be obtained from structures V-32 through V-39 for a direct comparison of the relative effectiveness of the keys. The other items relevant to the documentation of structures do not seem to apply to these structures.

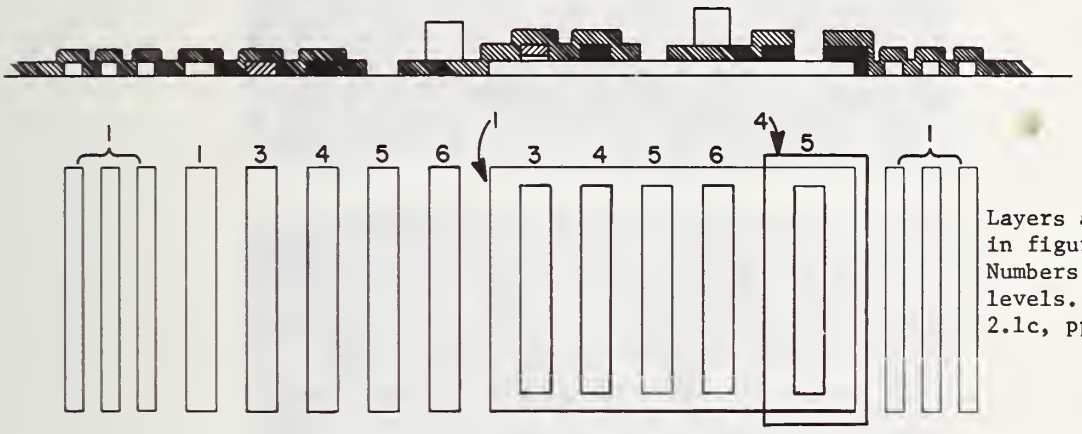
3.52 Surface Profilometer - V-42

Purpose - This test structure measures the actual film thickness achieved.

Verbal Description - This structure consists of rectangles of the various mask levels of 0.5 x 4.0 mil size spaced 0.5 mil apart. The structure consists of epi on sapphire, poly on sapphire, n^+ on sapphire, contact on sapphire, Al on sapphire, poly on epi, n^+ on epi, contact on p^+ epi, Al on epi, and contact on n^+ epi.

Three bars of epi precede and follow the structure. These bars are 0.3 x 4.0 mil.

Line Drawing - The line drawing for this structure is shown in figure 207.



Layers are identified in figure 8, p. 23. Numbers refer to mask levels. See section 2.1c, pp. 20-25.

Figure 207. Surface profilometer, test structure V-42, computer line drawing and cross section.

Halftone Photograph - The photomicrograph for this structure is shown in figure 208.

Electrical Access - There is no electrical access.

Testing Method - This structure is tested by drawing a fine-tipped stylus across the length of the structure. The three narrow silicon bars on either end of the structure act as coding signals that the beginning or end has been reached. In other words, when these closely spaced jumps are seen as the stylus is drawn from left to right, the next bump will be the wide silicon bar. It requires careful prepositioning of the stylus in order to avoid missing the entire structure. The coding humps and the regularly spaced edges are the best indication that the intended measurements are being made. It is sometimes difficult to see where the stylus is because the stylus must be observed from the side. The assumption is made here that the p+ oxide is the same thickness on top of the silicon and other oxide layers as on the sapphire. For example, we assume that the height of the p+ oxide step is the same as the height of the silicon step at the silicon edge. Not all of the possible steps are included in this structure. Data acquisition is slow and tedious with typical accuracy in the 100-Å range.

Special Equipment - This structure clearly requires a surface profilometer type of instrument. These instruments are commercially available. Special optics must be obtained, and special sample holders must be built in order to preposition the stylus and manipulate the sample. Typical outputs are traces of the surface of the structure. Identification of the peaks and actual measurement of the step height are all manual and are sometimes very subjective.

Samples of Data - No data have been acquired from this structure to date.

Potential Pitfalls - It is easy to misidentify peaks or to misread the step height. Also if the p+ oxide is not uniform for any reason, the step height read can be in error.

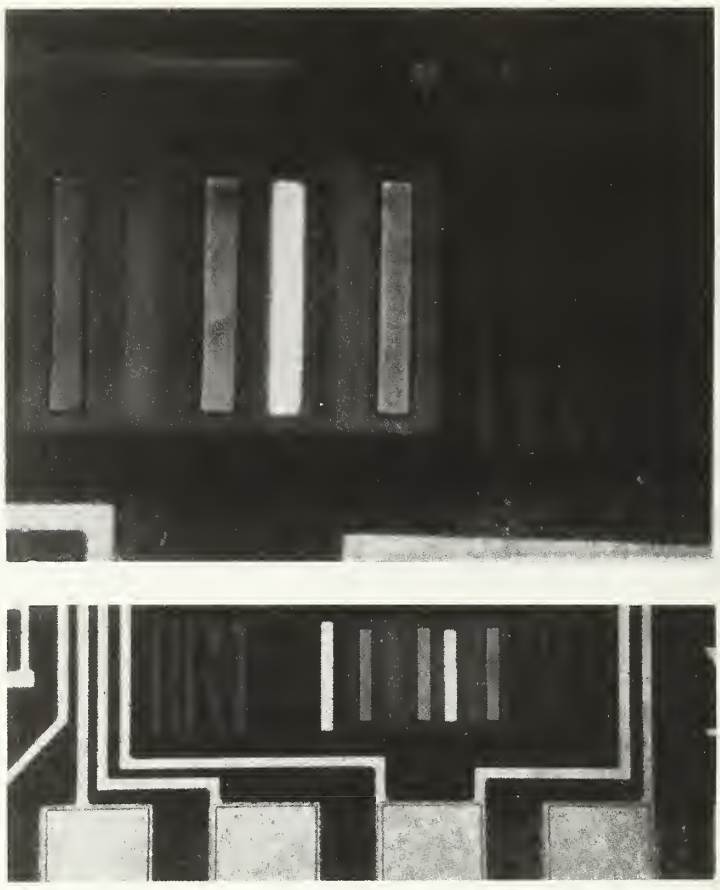


Figure 208. Photomicrographs, surface profilometer, test structure V-42,
(a) right end of structure and
(b) complete structure.

Overall Usefulness - This structure is typical of those used to measure actual film thickness. Such structures are difficult and time-consuming to measure, but they currently seem to be the best overall method available. An electrical means to do these measurements could open new doors to understanding and controlling IC processes. This structure should have been supplemented with a similar structure wherein the p+ oxide was removed from the top of the silicon layers both on the sapphire and on the epi and other missing steps were provided.

3.53 NOR Gate Ring Oscillator - V-43

Purpose - This test structure verifies the dynamic operation of a complicated device interconnection.

Verbal Description - This structure contains 32 stages of CMOS NOR gate connected in series. The basic NOR gate has a channel of 0.3 x 1.8 mil for the p-channel devices and 0.3 x 0.5 mil for the n-channel devices. Also included in this structure is the capability to disable the oscillation. This is accomplished by opening a gate line with a 0.3 x 2.0 mil p-channel device and also grounding this line with a 0.3 x 2.0 mil n-channel device. An output inverter with a 0.3 x 2.0 mil n-channel and a 0.3 x 4.0 mil p-channel device is included. A schematic diagram of two stages with the disabling scheme is illustrated in figure 209.

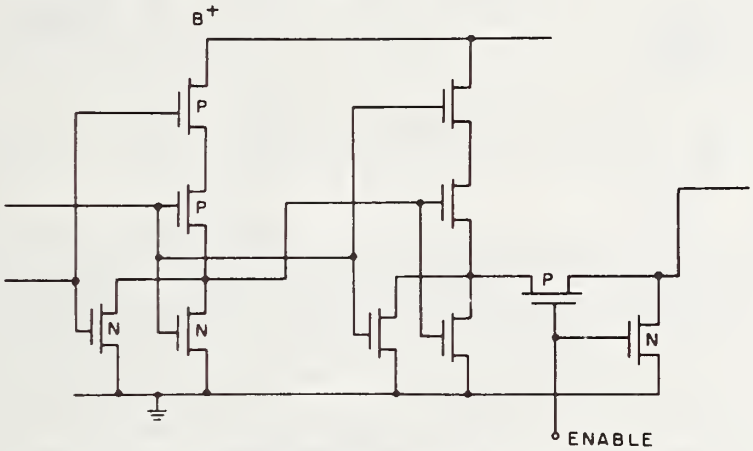


Figure 209. Schematic of NOR gate ring oscillator.

3.54 Inverter Ring Oscillator - V-44

Purpose - This test structure verifies the dynamic operation of a relatively simple device interconnection.

Verbal Description - This structure contains 18 stages of a CMOS inverter connected in series. The basic inverter has channel dimensions of 0.3 x 3.0 mil for both n- and p-channel. A two-stage output buffer is provided consisting of the first stage with 0.3 x 0.3 mil transistors and a second stage of 0.3 x 3.8 mil. No provision is made for disabling the oscillation. This structure is basically simpler than the NOR gate oscillator. A schematic diagram of the circuit is shown in figure 210.

Line Drawing - The line drawings are shown in figures 211 and 212.

Halftone Photograph - The photomicrographs are shown in figures 213 and 214.

Electrical Access - These structures have three basic access points and an optional fourth point:

Power supply + voltage	B+
Power supply ground	Ground
Output	Output
On structure V-43 only On-Off	ENABLE-DISABLE

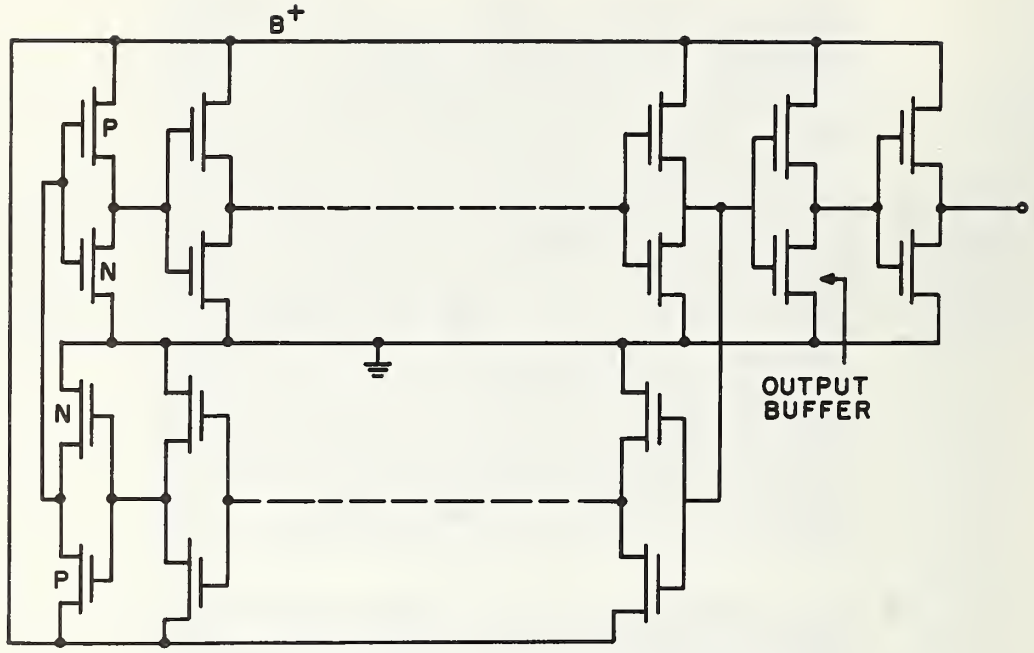


Figure 210. Schematic of inverter ring oscillator.

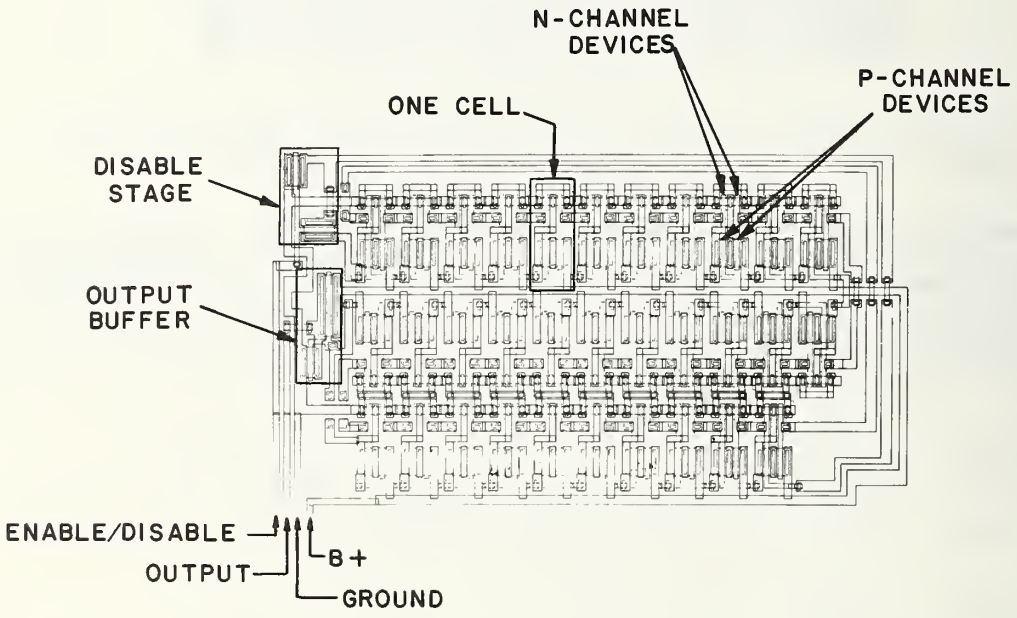


Figure 211. NOR gate ring oscillator, test structure V-43, computer line drawing.

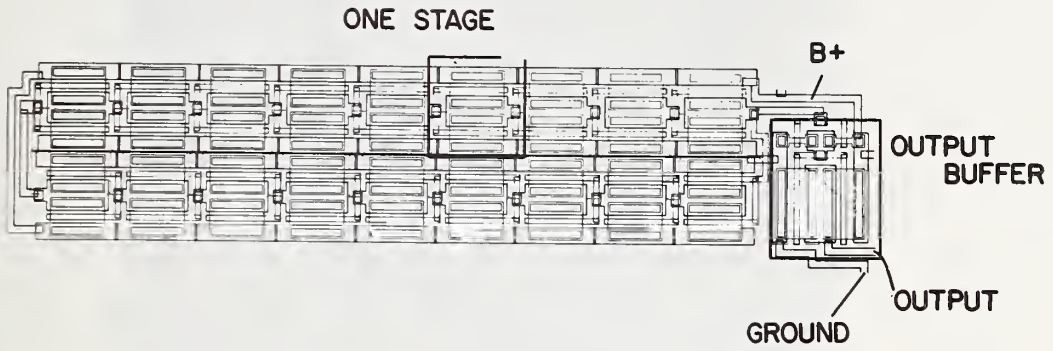
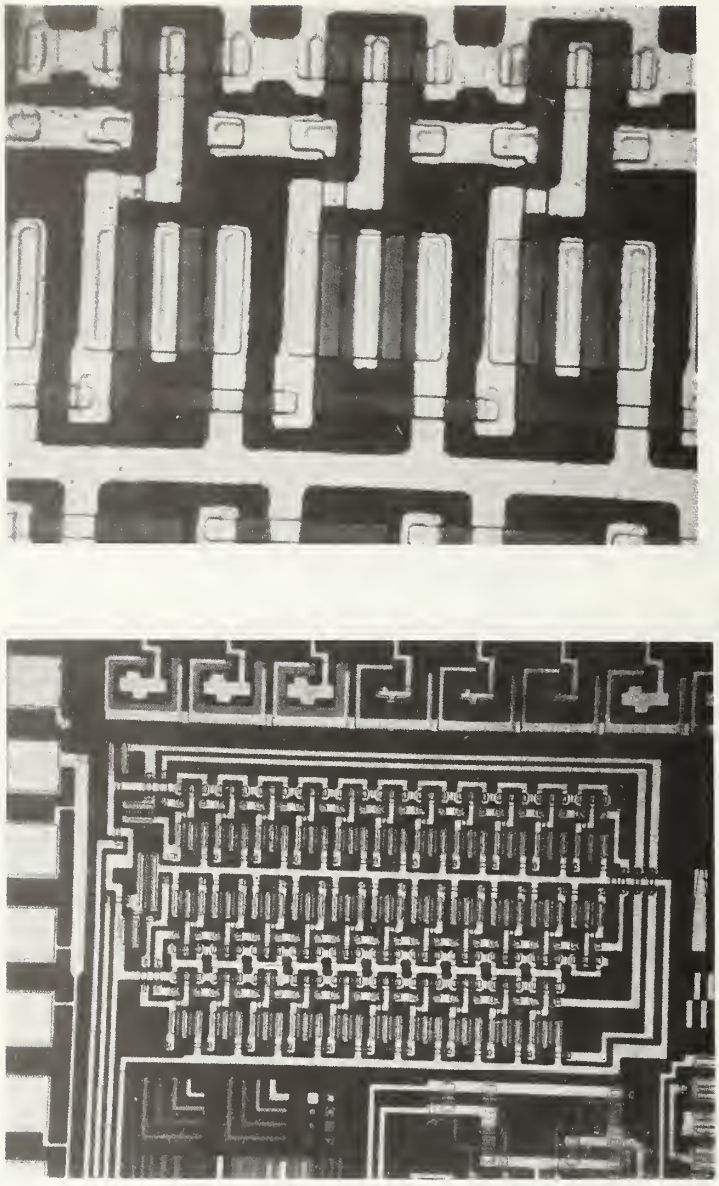


Figure 212. Inverter ring oscillator, test structure V-44, computer line drawing.

Testing Method - These structures oscillate with a characteristic frequency when the power supply to ground voltage (V_{DD}) is sufficiently high to overcome the threshold voltages of the transistors. Since an even number of stages is used and a phase reversal is experienced in each stage, a positive feedback results when the output of the last stage is connected to the input of the first. The waveform of the last stage is applied to the input of the first stage and is subsequently passed through to the output stage again and the process is repeated. It is clear therefore that not only is the frequency of these oscillations (f_o) self-determined but also the waveform. The primary reason to test these structures is to verify that they operate as a dynamic circuit. The frequency of oscillation is of secondary interest for the application here since it is very difficult to relate to any specific parameter or processing step. However, operation in a reasonable frequency range guarantees that the process is capable of relatively sophisticated operation and that the major factors concerning the processing were successful. Structure V-43 is much more complicated than structure V-44, and it is conceivable that both structures will not always operate at the same V_{DD}.

It is convenient to define the oscillation in terms of a stage delay, and therefore an attempt was made to make each stage as nearly identical to each other as possible. This also makes the difficult analysis easier since all elements and interfaces are the same. No analysis was performed here because the results would contain many parameters. While these parameters may be known from other structures, they are not determinable from a single measurement of oscillation frequency and therefore the structure does not measure anything which can be unambiguously related to the process. The measurement of these structures provides a relative comparison between wafers, etc, but it is not always true that higher frequency means better processing. For example, lower threshold voltages cause higher frequency and so do greater mobilities and reduced capacitances. The lower thresholds or reduced capacitances might also mean increased leakages or step coverage problems. In general, one would expect the oscillation frequency to increase with applied voltage and the parameters of the f_o vs V_{DD} curve can also be used as a parametric output for these structures. The minimum V_{DD} for which any nonzero f_o is obtained could provide another basis for comparison of these structures.

We note that the NOR gate oscillator (which was copied from a test circuit from a manufacturing operation) contains an enable-disable function (Fig. 209). This allows the oscillation to be quenched or started at will. (Gating V_{DD} also provides this same function.) When the enable gate is positive, the p-channel device is off, and the n-channel device is on, the output of the previous stage is therefore removed from the input to the next stage. A negative enable signal turns the p-channel device on and the n-channel device off, thereby connecting the two stages. While this provides better control of the operation of this structure, it makes analysis very difficult.



(a)

(b)

Figure 213. Photomicrographs, NOR gate ring oscillator, test structure V-43, (a) three stages and (b) entire structure.

The inverter oscillator is much more symmetrical than the NOR gate oscillator. If any analysis is done to relate the transistor parameters to the oscillation frequency, it should be done in the inverter oscillator. The inverter oscillator is designed such that the dominant capacitance seen by the output of each stage is due to the gate of the next stage. The buffer stage increases the capacitance loading by only ∿10% since the gate area of the first stage of the buffer is much smaller than the gate area of the stages. The output stage, however, is similar to one of the oscillator stages.

Operation is detected by measuring the frequency of oscillation at the output pad. Typically these frequencies are in the few megahertz range. An indication of the frequency can be obtained using dc techniques on an automatic tester with very simple special equipment.

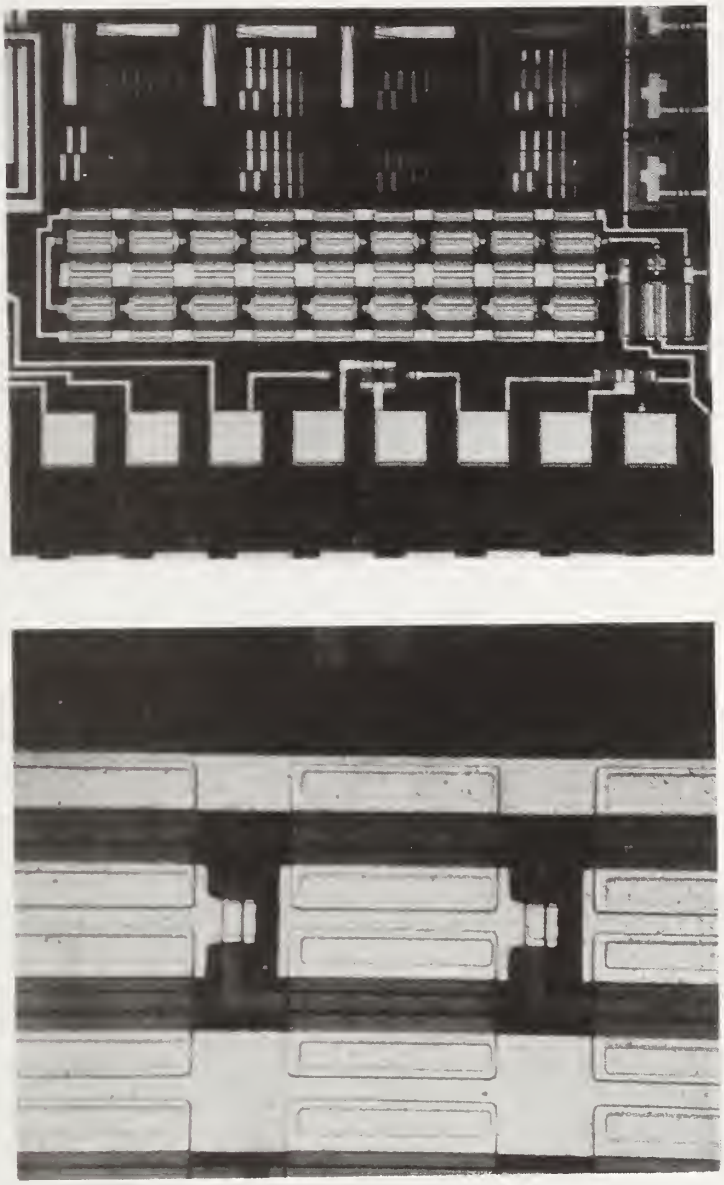


Figure 214. Photomicrographs, inverter ring oscillator, test structure V-44,
(a) entire structure and
(b) one stage.

Special Equipment - This structure requires an instrument capable of measuring frequency. Commercially available digital counters or a simple dc measurement from a clipped diode coupled RC network can be used. (The clipping is necessary to provide amplitude independence.) Since the main purpose of these structures is to verify the dynamic operation, high degrees of accuracy are not required. It is important that the sensing probe be of low capacitance so that the output buffer can drive the instrument. We note that only the frequency is of interest in general and that attenuation or waveform modification is not important as long as the signal is large enough to measure.

Samples of Data - No data have been acquired from these devices.

Potential Pitfalls - The main pitfall of this structure is to assume that higher frequency means better processing. This is not true in every case.

Overall Usefulness - Overall usefulness has been discussed in "Testing Method," above. One also may use these structures as a point defect (Type I) detector. This is perhaps the most important use of these structures since they are the only structures which contain all of the important elements in a single small area connected as in a circuit. Since the testing operation is very simple and the area involved is reasonably small, one can perform optical studies to determine the type of defect causing the failures without excessive expenditure of operator time. If an electrical failure exists, the general area of the failure is known to be confined to an area of 20 x 30 mil (the area of the NOR gate). Exhaustive examination even at 400X requires only a very few minutes. Identification of the defects causing failures is the first step to improving the process.

3.55 Inverter - V-45

Purpose - This test structure is the standard CMOS building block.

Verbal Description - This structure consists of an n-channel and a p-channel MOS transistor connected as an inverter. The transistors are 0.3 x 1.0 mil.

3.56 Transmission Gate - V-46

Purpose - This test structure is the standard CMOS building block.

Verbal Description - This structure consists of an n-channel and a p-channel MOS transistor connected as a transmission gate. Both transistors are 0.3 x 1.0 mil.

3.57 NAND Gate - V-47

Purpose - This test structure is the standard CMOS building block.

Verbal Description - This structure consists of two n-channel and two p-channel transistors connected as a CMOS NAND gate. The transistors are 0.3 x 1.0 mil.

3.58 NOR Gate - V-48

Purpose - This test structure is the standard CMOS building block.

Verbal Description - This structure consists of two n-channel and two p-channel transistors connected as a CMOS NOR gate. The transistors are 0.3 x 1.0 mil.

Line Drawing - The line drawings are presented as follows:

Structure V-45: figure 215

Structure V-46: figure 216

Structure V-47: figure 217

Structure V-48: figure 218

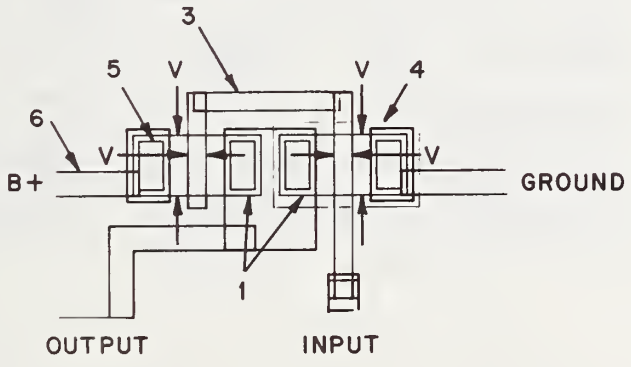


Figure 215. Inverter, test structure V-45, computer line drawing. Level 4 covers the n-channel device.

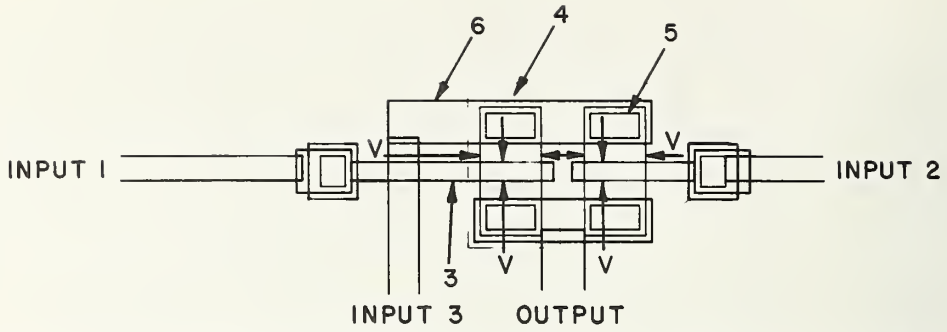


Figure 216. Transmission gate, test structure V-46, computer line drawing. Level 4 covers the n-channel device.

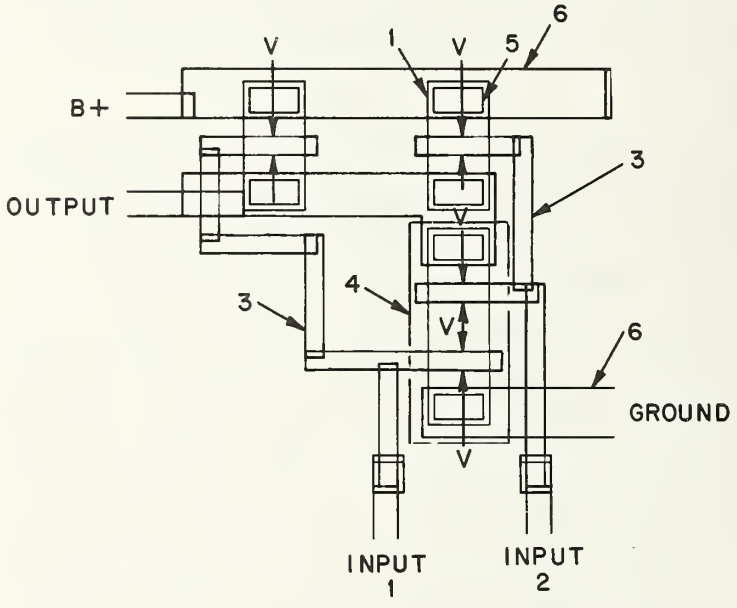


Figure 217. NAND gate, test structure V-47, computer line drawing. Level 4 covers the n-channel devices.

Halftone Photograph - The photomicrographs are shown as follows:

Structure V-45:	figure 219
Structure V-46:	figure 220
Structure V-47:	figure 221
Structure V-48:	figure 222

Electrical Access - All structures have an output pad (Output); V-55, V-57 and V-58 have (B+) and (ground) connections; V-55 has one input (Input); V-57 and V-58 have two inputs (Input 1) and (Input 2); V-56 has three inputs (Input 1), (Input 2), and (Input 3).

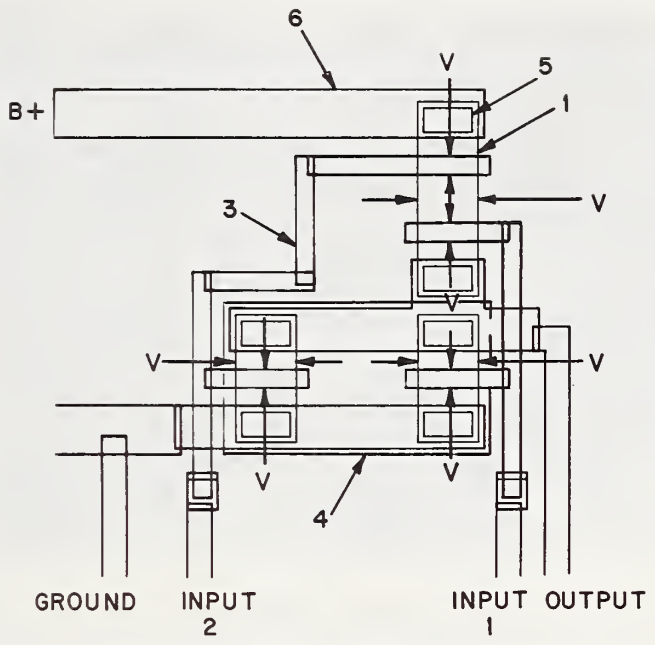


Figure 218. NOR gate, test structure V-48, computer line drawing. Level 4 covers the n-channel devices.

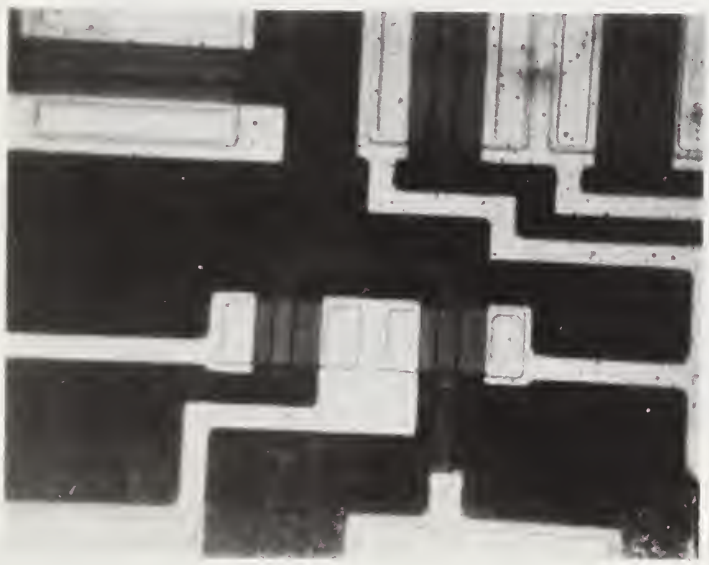


Figure 219. Photomicrograph, inverter, test structure V-45.

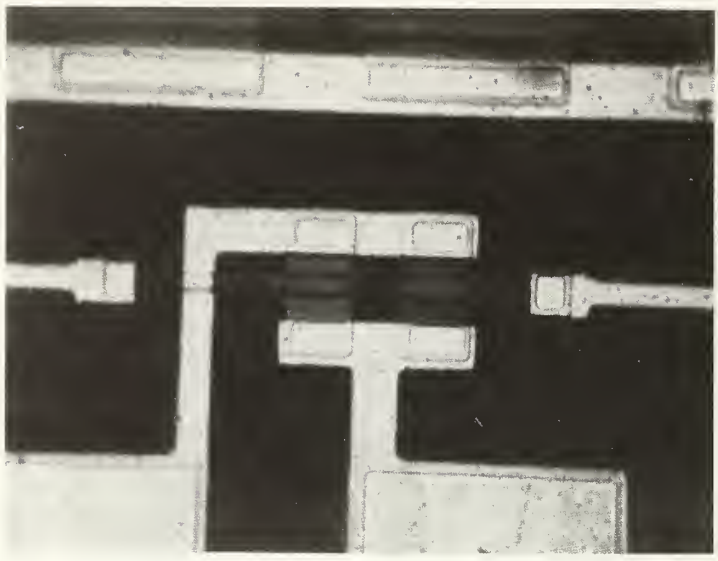


Figure 220. Photomicrograph, transmission gate, test structure V-46.

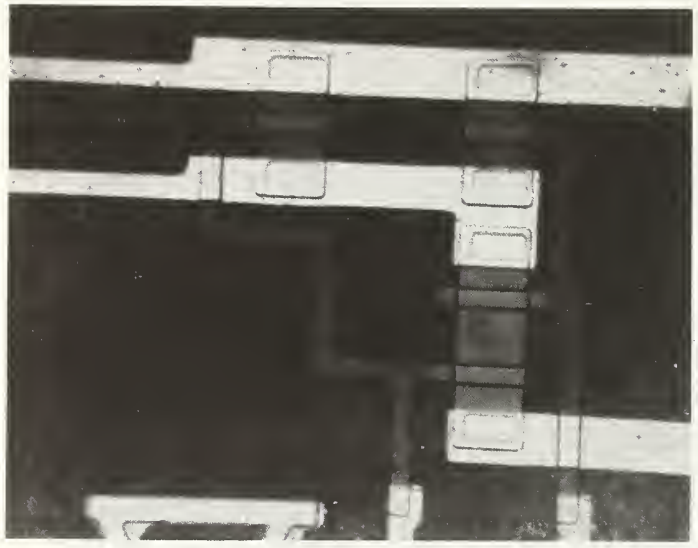


Figure 221. Photomicrograph, NAND gate, test structure V-47.

Testing Method - The detailed testing of these structures has not been considered here. Basically these are provided to eliminate the necessity to "wire" the individual elements together to form the test cell. Operation of cells of this type is described, for example, in ref. 21. We are currently not in a position to comment on the equipment required, overall usefulness, etc. We note, however, that by using these structures either as part of a total test program or separately we can obtain most of the information of first-order interest for CMOS circuits as far as the compatibility of n-channel and p-channel transistors is concerned. Of course, the channel geometry ratios will not be optimum for every application. Equal channel geometries were chosen for both n- and p-channel devices for lack of more generally useful and model independent guidelines.

21. "Basic COS/MOS Circuits," *RCA COS/MOS Integrated Circuits Manual*, pp. 14-26, RCA Solid State Division, Somerville, NJ (1971).

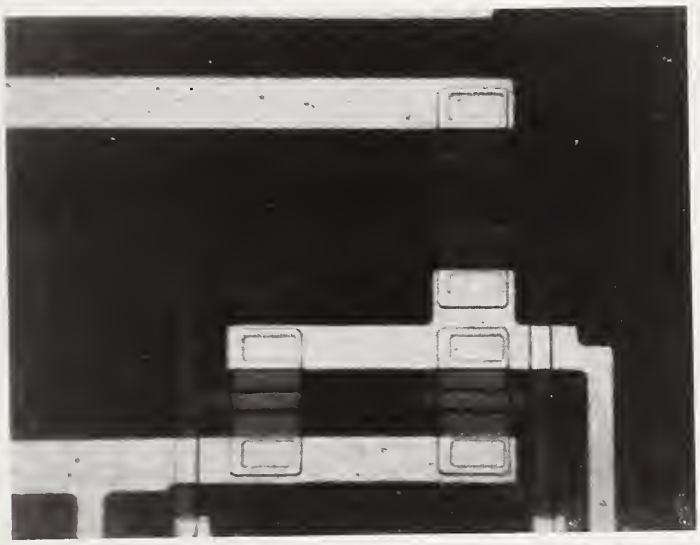


Figure 222. Photomicrograph, NOR gate, test structure V-48.

4. IMPLEMENTATION AND ASSESSMENT OF RESULTS

The basic method of implementation of this vehicle was discussed in section 1. The details of the implementation, especially the automatic testing considerations, are discussed in this section. In addition, a brief assessment of the results obtained is presented.

4.1 IMPLEMENTATION

It is obvious that only pieces of this pattern can be tested at any given time. A family of testing philosophies was therefore created to look at some possible fields of interest. A specific set of probes is required for each of these. It has been found that a reasonable number of probes to use at any given time is ∿40 or less. There are several reasons for limiting the number to this level:

(1) Probe card maintenance can become a significant part of the overall effort if too many probes are used.

(2) The size of the test program needed for many probes is frequently proportional to the number of probes. This can place severe limitations on the type of testing one can perform on his machine. For example, if one wants to perform detailed studies on all of the devices for one probe card, he will usually find that there is simply not enough core available in the tester to hold the required test program.

(3) The number of output variables is also approximately proportional to the number of probes. If an excessive amount of output is obtained, it will, in fact, never be used.

(4) The number of relays, lines, and connections which must operate is directly proportional to the number of probes used. This, again, can cause a possible maintenance problem.

For the limited testing of this pattern which has been accomplished to date, a family of probe cards was created. In all, twenty different designs were used to handle the various types of automatic testing desired. Many of these are highly specialized and would not normally be needed. We note that no special effort was needed for fabrication of the probe cards since all were obtained at regular (i.e., nonpremium) prices from commercial suppliers. The specific designs used are not included in this report, but the general areas considered and the number of required probes are listed in Table 4. These designs may of course change for different applications.

It was realized from the outset that the total number of structures which could be included in the pattern might be severely limited if the pad layout were constrained to match any particular probe card configuration. Also a great deal of *in*flexibility in the *collections* of devices which could be tested *together* can result from designing for only one probe card configuration. Therefore, in general a different probe card is needed for every different collection of devices to be tested. If one cannot use *exactly* the same probe card for different collections of devices, there is little point in laying out a pattern to accommodate a particular configuration of probes. The effort involved in changing probe cards is no greater than that usually required to change test programs (which obviously must be done somehow for different test structures). Some other test patterns used in the industry are laid out in quadrant form where the pad locations are all the same for each quadrant. This method does produce a savings in testing effort and should be used where possible. It was not possible to use such a layout for this pattern due to the very large number of pads involved.

For types I, III, and IV, a probe card which gives a cursory overview for a sampling of some of the structures was used and is called the primary card for that quadrant. Other cards address more specific areas. The type II section is completely testable with a single card.

TABLE 4. PROBE CARDS USED FOR INITIAL EVALUATION

Probe Card Type & Name	Purpose	Number of Probes
I-1 Primary	For general testing of a sampling of important structures from quadrant I	37
I-2 Epi Resistance	For gated bridge and gated van der Pauw measurements	20
I-3 Complete Transistor and Complete Continuity	For analysis of contact properties and their effect on transistors	25
I-4 Sheet Resistance - Contact Resistance - Epi Resistance	For detailed analysis of contacts and diffusions and, particularly, for field effect mobility measurements	18
I-5 Diodes	For detailed analysis of all types of diodes - n+ p+ - gated floating gate	18
I-6 Epi Capacitors	For two-terminal MOS measurements on different structures involving conductors over epi	10
I-7 Poly Capacitors	For two-terminal MOS measurements on different structures involving metal over poly	10
I-8 Ungated van der Pauw	For measurement of diffused layers by van der Pauw method	16
II-X	For type II pattern in X direction	8
II-Y	For type II pattern in Y direction	8
III-1 Primary	For measurement of transistors of various lengths and widths	32
III-2 Contacts and Substrate Contact Transistors	For measurement of different sizes of contact hole and of substrate contact transistors	22
III-3 Transistors Small Width and Length	For measurement of transistors with a selection of small channel lengths or widths	38
III-4 Transistors Large Width and Length	For measurement of transistors with a selection of large channel lengths or widths	28
III-5 Transistors Angular Variation 1	For measurement of transistor properties for different orientations	30
III-6 Transistors Angular Variation 2	For measurement of transistor properties for different orientations (different set of angles from card III-5)	28
IV-1 Primary	Measure partial characteristics of all types of crossover and transistors	38
IV-2 Transistors and Continuity	Measure complete properties of strings of transistors and all types of connections used	32
IV-3 Complete Crossovers	Measure all properties of the crossover test structures	32

TABLE 4. (Continued)

Probe Card Type & Name	Purpose	Number of Probes
V-1 Dimensions and Alignment	For measuring all the electrical structures used for alignment and dimension measurement	38
V-2 Ring Oscillators and Building Blocks	For measuring the characteristics of CMOS building blocks and interconnections thereof	19

The primary card for the type I quadrant, for example, is intended to test for all of the phenomena which are usually of first-order importance to the process, namely, connectivity, contact properties, diffused layer properties, transistor properties, diode characteristics, and epi edge phenomena.

Once the set of test structures has been chosen and the probe card has been obtained, a test program is then written (using the test block approach discussed in section 1 if possible). The wafers are then tested, and the results are stored in the tester memory or elsewhere for further use later. It is very important for nearly every kind of test that the wafer position be recorded automatically and stored with the data. Further, specification of the testing details requires specification of the testing hardware to be used. Such details are clearly beyond the scope of this work since the testers available are widely different in their abilities and configurations.

For the particular testing system used to obtain the data in section 3, data are stored directly on a disk shortly after being acquired. Each data point is carefully identified by a number of parameters, including the position. In addition, the system has the ability to print messages on the console during test execution to give a real-time indication of faulty test structures. They can also be used to give a real-time indication of testing-related parameters such as probe contact resistance. These messages are written as part of the test program and execute when certain limits are exceeded.

A typical set of messages describing the faults, structure, and the test block used for the test is shown in figure 223. This represents the total from approximately one-half of a 2-in. wafer. (The "I TOO LOW" messages were obtained when the probes attempted to probe off the wafer.)

Thus if many error messages are obtained, it may be futile to continue to test the wafer. These messages may allow real-time correction of testing problems (such as too little pressure on the probes) and in general make the entire data acquisition procedure much more reliable and efficient.

After the wafer is entirely tested, one has the option of performing other tests on the same wafer, the same tests on another wafer, or performing an analysis on the data which were acquired.

Once the data are stored in the system, they must be reduced in order to be useful. Some of the philosophy involved in this area was recently discussed [22]. The method of data output is at least as important as the testing methods in determining the actual effective transfer of an accurate impression of the situation to the user. This constitutes an entire field of study in itself and will not be discussed here except to list some of the ways that data output was handled for the testing of the vehicle described in this report.

The data output consists of:

1. List of identification parameters defined by:

    A. Test name

    B. Structure name

22. Ham, W. E., "Test Data Reduction," IEEE Trans. Manuf. Technol. MFT-5, No. 1, 24-29 (1976).

```
TEST    1 =  .70504E-04          <-- Test value
I TOO LOW I50 1                  <-- Fault, structure number,
TEST   32 =  .62935E-05              test program version used
I TOO LOW I51 1
TEST  102 =  .84170E 00
BAD CONTACT 42 I53 1
TEST   63 =  .66363E-04
I TOO LOW I52 1
TEST   70 =  .17574E-03
SPURIOUS CURRENT I52 1
TEST  101 =  .17576E-03
SPURIOUS CURRENT I53 1
TEST    9 =  .78780E 00
BAD CONTACT 42 I50 1
TEST   32 =  .12455E-03
I TOO LOW I51 1
TEST   94 =  .67899E-04
I TOO LOW I53 1
```

NOTE: "Spurious Current" means that the structure is not suitably isolated for valid measurements. "I TOO LOW" means that the system is not capable of delivering the current needed for the measurements. "Bad Contact 21" means that one (or both) of the voltage contacts, 2 or 1, are not suitable. Note also that the exact structure and the test program form being tested are automatically identified. Many other error messages are also built into the testing program.

Figure 223. Diagnostic messages indicating why certain structures are not suitable for further testing.

C. Test block used

D. Wafer used

E. Position on wafer

F. Number of times device has been probed

G. Date and time of data acquisition

H. Test program used

I. Other appropriate comments

2. Data reduction considering:

A. Numerical properties

1. List of numbers

2. Histograms and standard statistical analysis

B. Spatial properties

1. List of numbers with position

2. Special statistical analysis on neighboring devices, one line at a time (X or Y) (type II data). See next section

3. Relative positional information

   A. Category maps

   B. Density maps

   C. 3D plots

   D. Contour maps

C. Correlative properties

   1. With other results from the same wafer

   2. With other samples

An example of the importance of using both numerical and wafer position plots is shown in figures 224 and 225. The interpretation of the histogram would very likely be incorrect if the wafer map were not also available. The above methods for data reduction are commonly available and are more or less standard, except for the analysis of type II data. Data from the type II section of the test vehicle is different from that usually available and requires some discussion.

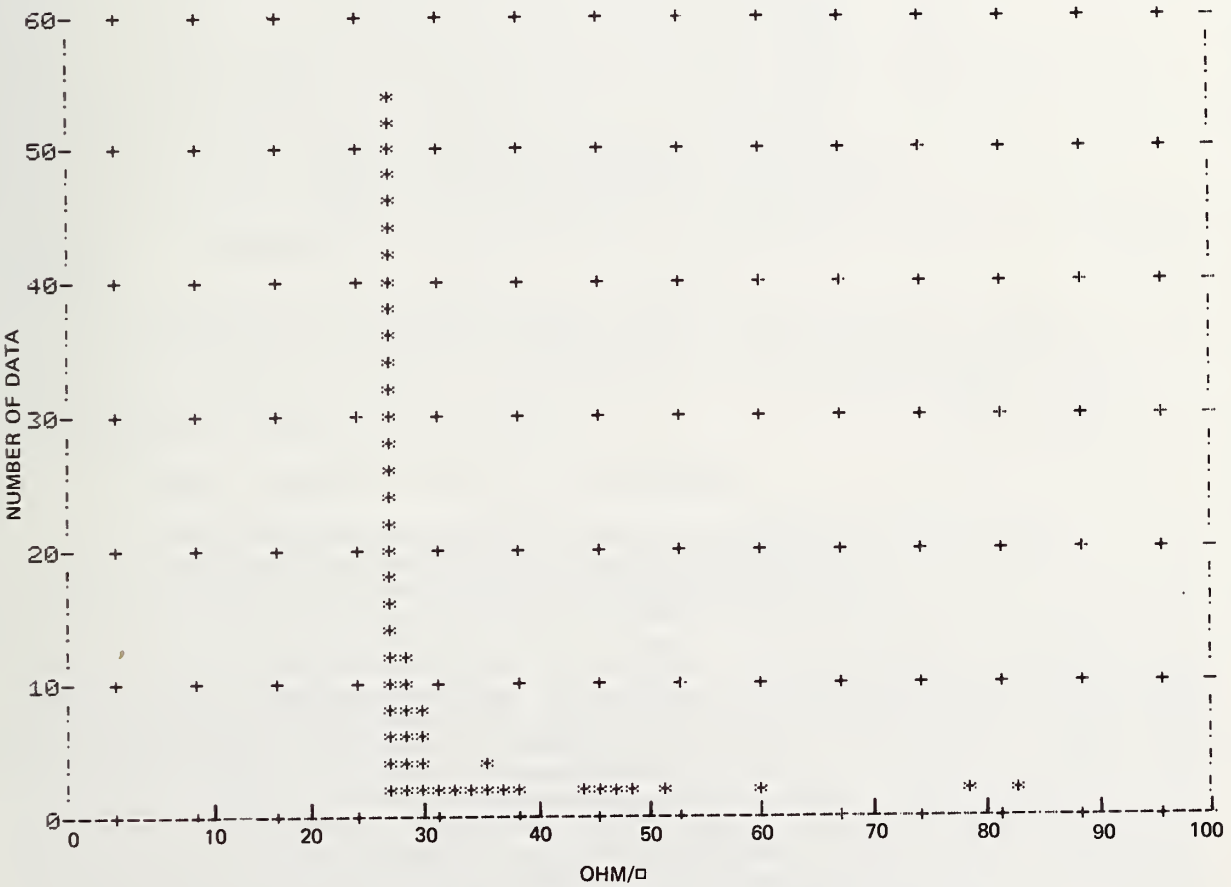


Figure 224. Histogram of sheet resistance data. The limits are fixed at 0 and 100 ohm/□.

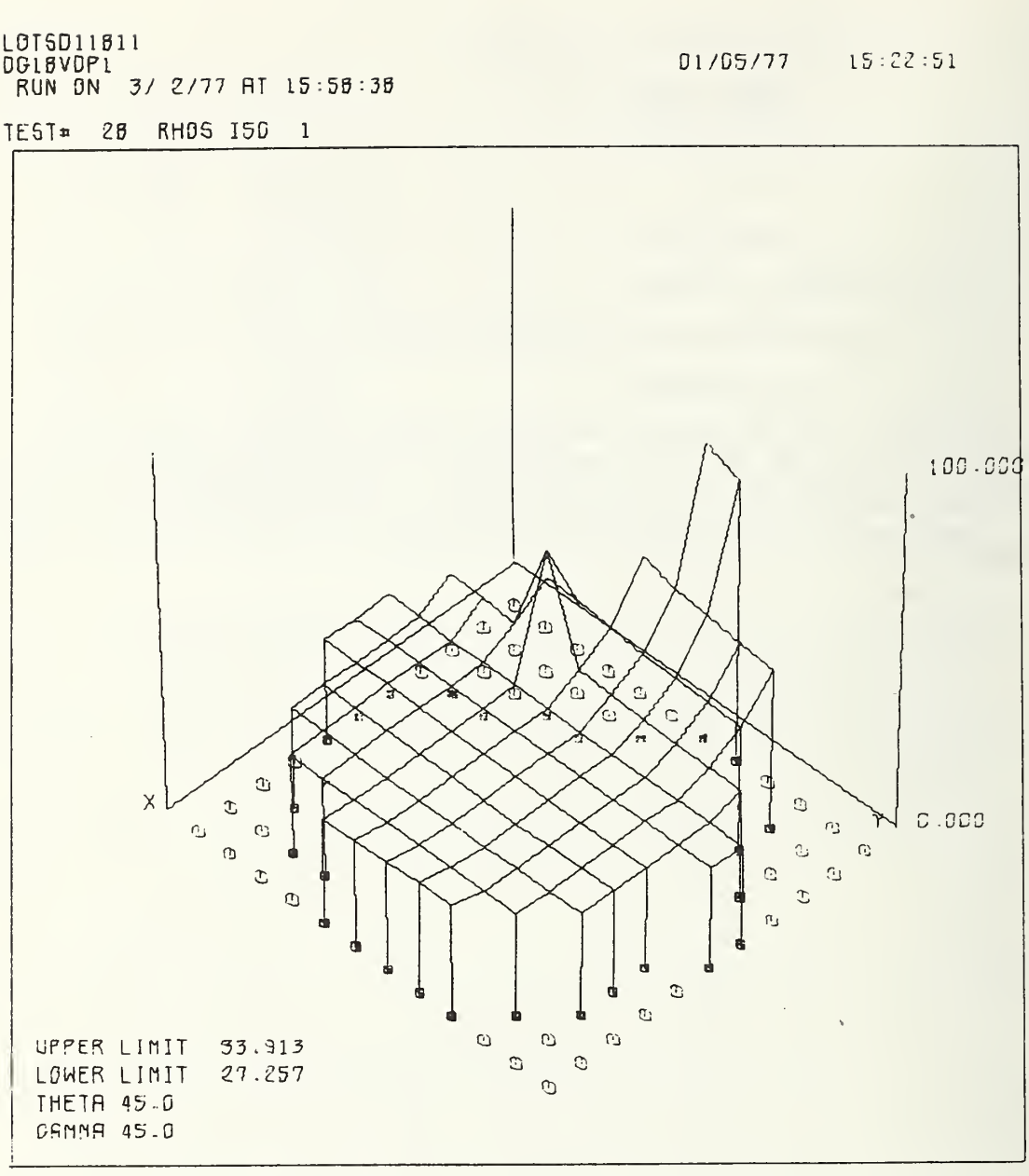


Figure 225. Three dimensional plot of the same data in figure 224. The limits are fixed at 0 and 100 ohm/□. The upper and lower limits are the extreme data values in the 0-100 ohm/□ range.

The most revealing output for type II data is a plot of the data vs position. This method, although highly preferred if available, is somewhat cumbersome in that an entire plot must be used. There is therefore some motivation for creating a method for parametizing the plot. It is obvious that a set of data having the complexity of that shown in figure 226 cannot be reduced to a single parameter without *severe* loss of information content. On the other hand many sets of type II data have been acquired which would lend themselves to parameterization without severe loss of information content. In fact the wafers which have "homogeneous" behavior across the wafer can be reasonably well described by two or three parameters. Several parameters can be defined which reflect the important features of the data set. The following discussion shows how four of these parameters have been defined. It may be useful to refer to figure 226 when reading these definitions.

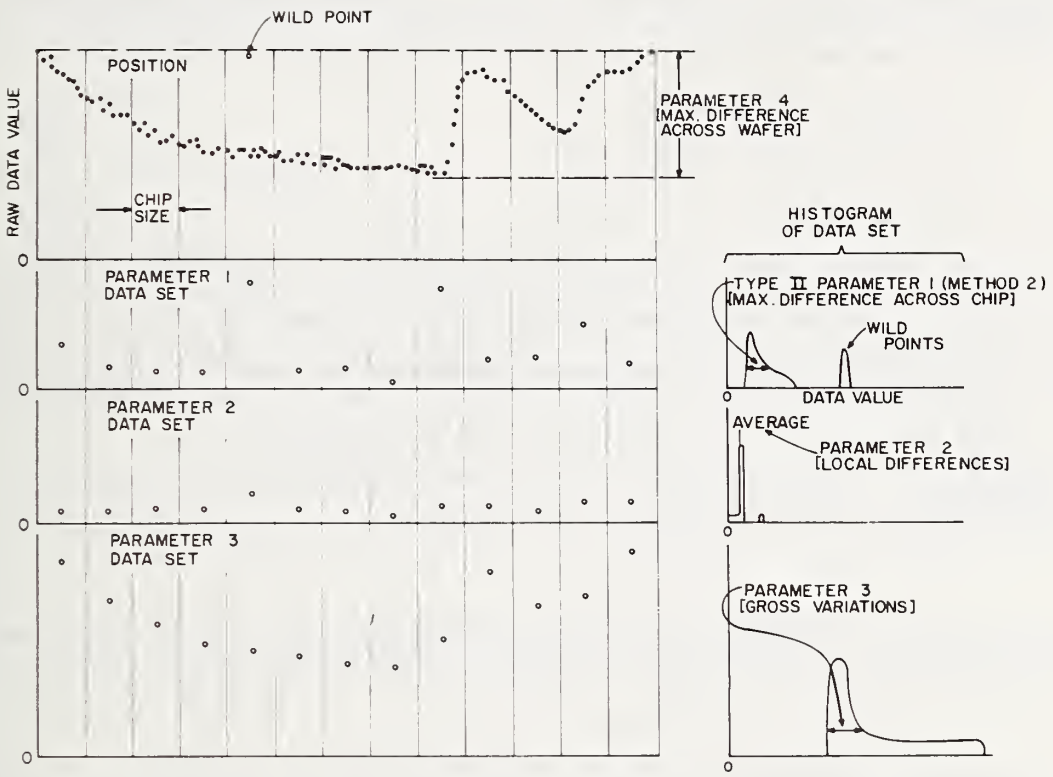


Figure 226. Illustration of four parameters which can be created from a hypothetical set of type II data. See text.

(1) *Type II - Parameter 1 - Maximum difference across a distance typical of the circuit of interest.*

This parameter is calculated by examining all the data in a block of size ΔN (= chip edge length/6.0 mil + 1). There are several ways of calculating this parameter.

Method (1) assumes the data is of the form $Z(N_x)$ where Z is the data value and N_x is the integer associated with the x position.

$$\text{PARM 11} \equiv \text{MAX}\left|Z(N_x) - Z(N_x + 1)\right| : N_x : 1, N_x\text{MAX}.$$

This notation is used throughout this section. The above statement reads "PARM 11 is defined as the maximum member of the set of data consisting of the absolute value of the difference between $Z(N_x)$ and $Z(N_x + 1)$ where N_x takes the value 1 to N_xMAX in steps of 1." Steps of 1 are assumed unless otherwise specified. In this method N_xMAX is the number of points in the type II data across the entire wafer. The parameter is the absolute maximum difference that exists between any two adjacent points. Note that it does not depend on ΔN. Although this parameter is very easy to calculate, it does not reflect the desired quality of the data in the general case. This is because it only takes one "wild" data point to completely dominate this parameter. Whereas this may indeed be a valid data point, a strong possibility exists that a defect in the test structure may be the underlying cause of the wild point. We are generally not interested in parametric shifts caused by visible point defects, as discussed in the introduction and, therefore, choose to de-emphasize this approach. It is, of course, possible to eliminate these wild points from the computation (using external criteria), thereby providing a reasonable parametric interpretation.

Method (2). With the above notation, a second method is given by the following.

PARM 12 ≡ The characteristic value of the data set defined by:

$$\text{MAX}\ (Z(N_x):N_x:N_xMIN,\ N_xMIN + \Delta N) -$$

$$\text{MIN}\ (Z(N_x):N_x:N_xMIN,\ N_xMIN + \Delta N)$$

and N_xMIN takes the values $1,\ \Delta N + 1,\ 2\Delta N + 1,\ \cdots\ N_xMAX - \Delta N$.

In other words the wafer is divided into blocks the size of the chip, and *each* block is examined for the maximum and minimum values existing in that block. In this case, a wild point will cause only one of the data set to be "wild" and computation of a characteristic value of the data set without the wild point(s) provides an intelligent parametric output. An example of this characteristic value would be the standard deviation of the data set without the wild points. This method fails to detect a discontinuity at the chip edge whereas method (1) would not fail to detect this discontinuity.

Method (3). This method is similar to Method (2) except that the edge discontinuity is accounted for. In this method

$$N_xMIN = 1,2,3,\ \cdots\ N_xMAX - \Delta N$$

In this case, every possible situation is accounted for and one wild point causes $\sim\Delta N$ wild data set values. The data set is much larger, however, and provides a more statistically significant data set.

One can clearly define other methods where

$$N_xMIN = 1,\alpha 2,\alpha 3,\alpha 4,\ \cdots$$

where α is any integer. Method (1), in fact, is just a special case where $\alpha \approx N_xMAX/2$.

Method (2) is preferred for most applications since one does not have to worry about interpreting effects of multiple wild points, and computation time is somewhat less. Furthermore, discontinuity at chip edges usually would not cause a circuit problem. Implementation of this method is shown in figure 226.

In a typical case, for a 3-in.-diam wafer, there will be approximately 15 to 30 points for any application of Method (2) above for chips 100 to 200 mil on a side. For a data set of this size, a very few defective test structures can significantly alter the complexion of the data set. This leads us to define another parameter which is less sensitive to the effects of wild points.

(2) *Type II - Parameter 2 - Local Differences.*

This parameter considers the difference between adjacent points as the data set. Although the maximum difference to be expected across a chip is given by Parameter 1, and for many circuit applications the maximum difference may be the important feature, this does not say anything about the behavior of closely spaced devices.

Method (1). The local differences are more important than the maximum differences, if parametric matching is the issue. The local "fuzziness" is given by PARM 21 ≡; the characteristic value (usually the average) of the data set defined by:

$$(|Z(N_x) - Z(N_x + 1)|:N_x:1,\ N_xMAX - 1)$$

In other words the data set consists of the absolute value of the difference between neighboring devices including those which are on the chip edges.

Method (2). Since discontinuties at the chip edge can be largest local differences and since it is mainly the local differences within a chip that are most important, it is convenient to define another method for parametizing the local differences. This can be

done by considering only those points within a chip in essentially the same manner as used in PARM 12. In this case PARM 22 = characteristic value (usually the average in this case) of the data set defined by:

$$\frac{\sum_{N_x MIN}^{N_x MIN + \Delta N} \left| Z(N_x) - Z(N_x+1) \right|}{\Delta N}$$

where $N_x MIN$ takes the values 1, $\Delta N + 1$, $2\Delta N + 1$, . . . $N_x MAX - \Delta N$. In most cases this second method is preferred.

Parameter 2 provides an indication of the "fuzziness" across the wafer. In this parameter, wild points have an effect but they are only counted twice - once for each data point on either side of the wild point. In the type II - parameter 1 they "wiped out" all the "good" data points in the chip. In effect, they were counted up to, perhaps, 40 times. It is again possible to eliminate any wild points by specifying a maximum acceptable data set range.

Another feature of the original type II data which is not included in Parameters 1 or 2 is the slow charges sometimes observed over larger areas of the wafer than a single chip. It is possible for the data to exhibit slow changes across a wafer while maintaining essentially the same local fuzziness.

Whereas it is possible to represent these slow changes by non-type II data (that is, an indication of the gross changes existing can be obtained from test structures located far apart), the value of the data which represent that particular area of the wafer is much more likely to be correct if many measurements are used instead only one. Furthermore, the effect of wild points can be drastically reduced by using type II data. There is, therefore, considerable value in creating a third parameter which represents these large distance changes.

(3) *Type II - Parameter 3 - Gross Variations.*

This parameter is defined by considering the average of the parameter over a distance representative of the circuit as the data set

$$\frac{\sum_{N_x MIN}^{N_x MIN + \Delta N} Z(N_x)}{\Delta N}$$

where $N_x MIN$ again takes the values 1, $\Delta N+1$, $2\Delta N+1$,...

In other words the raw data within each chip are averaged over the chip and this data set constitutes a reasonable representation of the *systematic* gross variations existing across the wafer. The average and especially the standard deviation of this data set provide a reasonable parameterization of the gross variations. We note that this average is the same as that obtained without dividing the wafer into chips.

One further parameter is needed to characterize a feature of the data which is not effectively handled by those parameters previously discussed. This is simply the maximum difference existing across the wafer between any two points existing *anywhere*. This is not the same as Parameter 1 because the gross variations were not considered. This parameter is perhaps the most useful of all since it defines the limits which must be satisfied if

all the circuits on the wafers are to perform properly. This parameter can be dominated by a single wild point. If the "wild" data are acquired from test devices which are operating properly as test devices, it is quite likely that circuits will in fact encounter such values on the wafer. Therefore, this effect may not be severe.

The fourth parameter describes the total spread of data values across the wafer.

(4) *Type II - Parameter 4 - Total Spread.*

This parameter is defined by

$$\text{PARM } 4 \equiv \text{MAX } (Z(N_x):N_x:1,N_xMAX) - \text{MIN } (Z(N_x):N_x:1,N_xMAX)$$

Thus many of the essential features of a set of type II data can be represented by parameters. These parameters (listed in table 5 for convenience) provide a good set of design guidelines for anyone using the process and are generally applicable to any set of raw type II data.

TABLE 5. SUMMARY OF TYPE II PARAMETERS

Parameter	Name
1	Maximum difference across a distance typical of a circuit
2	Local difference (fuzziness)
3	Gross variations (large distance effects)
4	Total spread (maximum differences across the wafer)

These four parameters are represented schematically in figure 226, for a presumed data set. It is apparent by examining this figure that even with the calculation of four carefully considered parameters, that some of the information contained in the raw data is lost. This is due primarily to the fact that the data set shown is very complicated (purposely for illustrative purposes). This degree of complexity is not usually found in typical wafers. However, for the presumed data set the parametric representation does not indicate:

- That the local differences are scattered above and below a mean curve on the left-half and are located almost on a mean curve on the right-half.
- Only with very careful study of the parameters in their *histogram form* is it found that a strong gradient exists across a single chip.
- The total change of character between the right and left sides.
- The range of applicability of a single measurement in terms of a "critical local distance."
- The nature of the parameters for other chip sizes.

Reducing a complicated type II data plot to a small set of parameters can be similar to trying to represent a full color photograph of the Grand Canyon by a small list of numbers. Nevertheless, for most of the cases typically encountered, the parametric reduction suggested above provides a method for comparing the type II data from many wafers and can be very valuable for performing optimum circuit designs. If possible, the actual data plot should be inspected before assuming the meaning of the parameters. This is only necessary on a sampling basis. During the course of this writing a publication has appeared which shows many examples of type II data and further discusses its use [23].

23. Ham, W. E., "Intrachip and Spatial Parametric Integrity - an Important Part of IC Process Characterization," Technical Digest IEDM, Cat No. 77 CH1275-7ED, Abstract No. 19.6, pp. 406-409, Washington, DC (Dec 1977).

Thus, an outline of the methods of implementation of a comprehensive test vehicle have been briefly discussed. The specific use of the data and of the data reductions will depend entirely on the area of the process being measured. The next section briefly discusses the highlights of the very limited use that this vehicle has had to date.

4.2 Assessment of Results

A total of five or six wafers from four different processing lots (total of five or six wafers) were examined; the results were not representative of SOS technology in general. The use of this pattern in volume is beginning at the present time to evaluate three different SOS processing facilities and to evaluate the use of various surface finishes on the sapphire and the use of different kinds of sapphire growth techniques. The results obtained to date are primarily from the testing of new test programs. Once satisfactory operation was achieved, no further data were acquired. It is therefore difficult to be sure where the main emphasis will be placed after volume testing has been completed. It is almost certain that the type II tests will be useful.

The parameters listed below are those which seemed to be the most important on the few wafers which were examined. (See section 3.) These lists could change considerably for specific applications.

Structures:	Test Structure Class (Section 3)
• Ordinary MOS transistor	1, 13, 26
• Variable geometry MOS capacitors	4, 5, 7
• van der Pauw sheet resistors	8, 9, 10
• Gate-controlled bridge resistors	2
• Four-terminal contact resistance structures	12
• Total process connectivity test	18, 39
• Trapezoid - rectangle alignment test	49
• Electrical dimension test	40
• Electrical alignment tests	42, 43, 44, 45, 46
• Edgeless devices	1, 31
• Design rule tests	41, 47, 48
• Type II concept tests	24, 25, 26, 27
• Strings of identical devices when used as a test for parametric properties (not for defect studies)	35, 36, 37, 38
• Probe resistance tests	27
• MOS capacitors with both diffusion types	6

Parameters:

- Contact characteristics particularly to n^+ layers
- Field effect mobility (dependence on gate voltage)
- Dielectric strength of channel oxide particularly on edges
- Field oxide pinholes

- Distribution of diffused sheet resistances across wafers
- Local variations of threshold voltages and channel current
- Value of low current threshold voltages
- Stability of threshold voltage at room temperature
- Alignment tolerances achieved
- Values of minimum currents on transistors
- Line width control of poly particularly at silicon edges
- Large geometry photoresist effects
- Aluminum edges near silicon edges
- "Linearity" of type IV transistor measurement
- Critical channel length below which leakage and drain breakdown are severe
- Mobility dependence on orientation
- Stability of edge currents under high fields and high temperatures

In general the results from the test vehicle have been very encouraging. The understanding and control of IC processing phenomena as a whole will be vastly improved by use of this vehicle and similar vehicles designed and tested using the comprehensive features discussed in this report.

The vast power of the "small-signal" approach, that is, looking for changes in results due to small known changes from a known state, was demonstrated. This approach is also referred to as a perturbation method and is not original to this work. This "small-signal" approach is also useful when comparing reduced data.

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APPENDIX A

MASK LEVELS

This appendix shows photomicrographs (figures A-2 through A-7) of the six mask levels used to form the test structures using the process discussed in section 2. As discussed there, level 2 does not exist for this process. The masks shown are for use with positive photoresist (the photoresist is removed during development where the light hits during exposure). The opposite polarity mask is also available, of course. These masks (designated TA10068) are available from the RCA Solid State Technology Center, Somerville, NJ 08876. As discussed in section 2, many different processes are compatible with the mask set.

In addition to the levels shown here, masks will soon be available which allow gate lengths other than 0.3 mil to be used (0.1, 0.125, 0.15, 0.175, 0.2, 0.25, and 0.4 mil). Also level 5 (contacts) will soon be available where the contact opening over the contact pads does not exist. This allows much better compatibility with bulk silicon processing. (We again note that level 4 can be used in place of level 2 for some processes.)

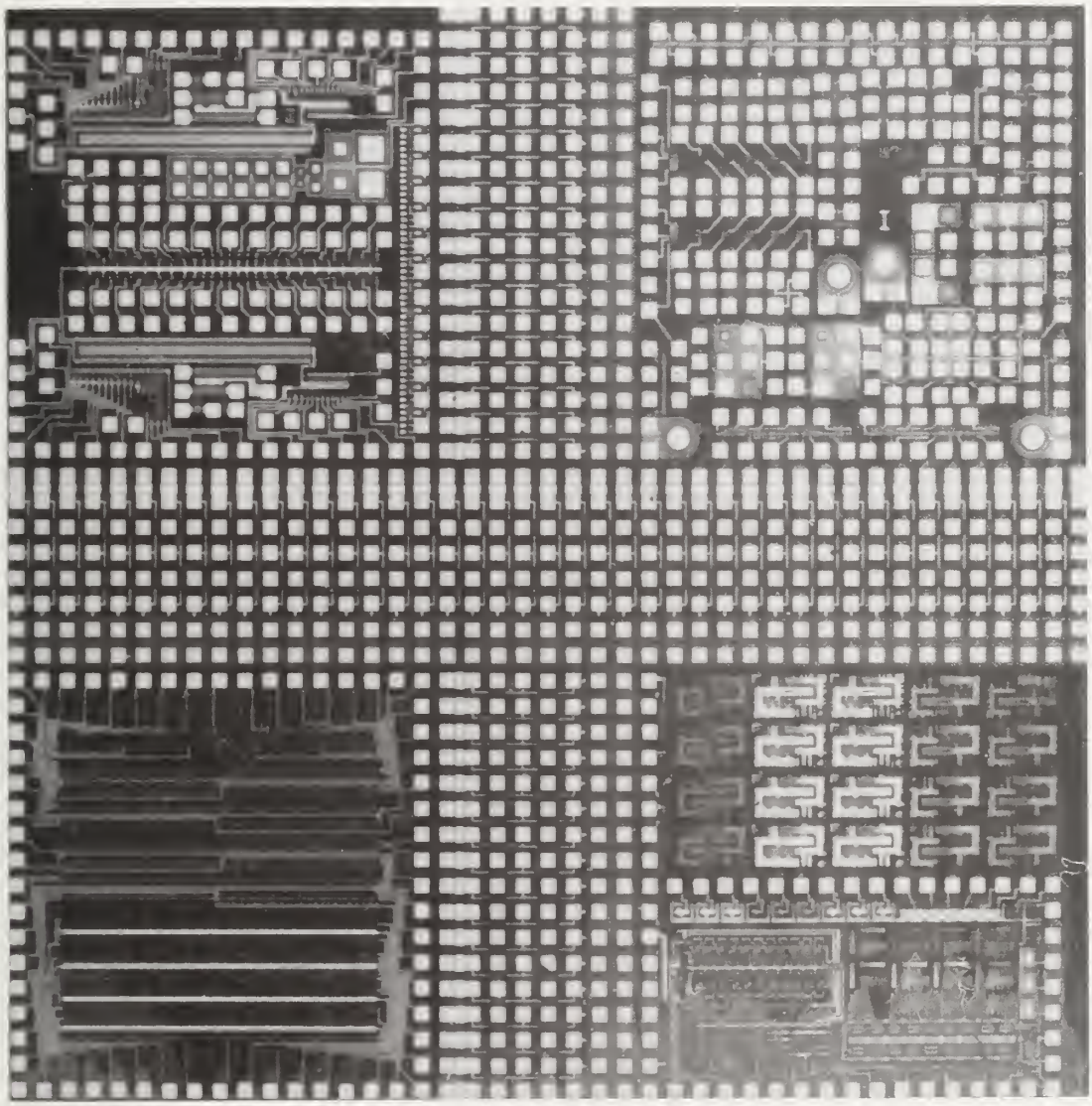

Figure A-1. Composite of all mask levels - completed chip.

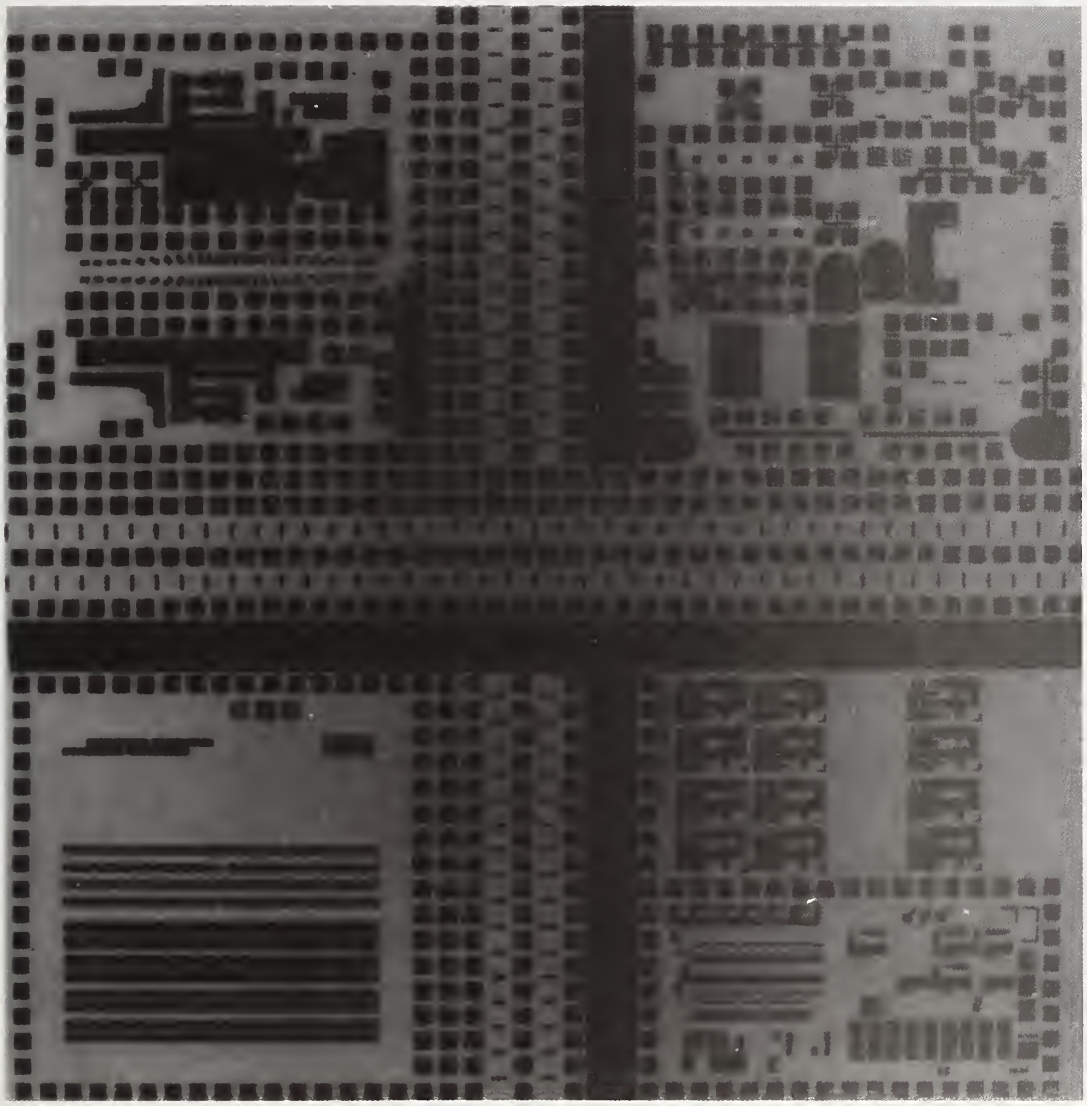

Figure A-2. Level 1, Silicon Islands.

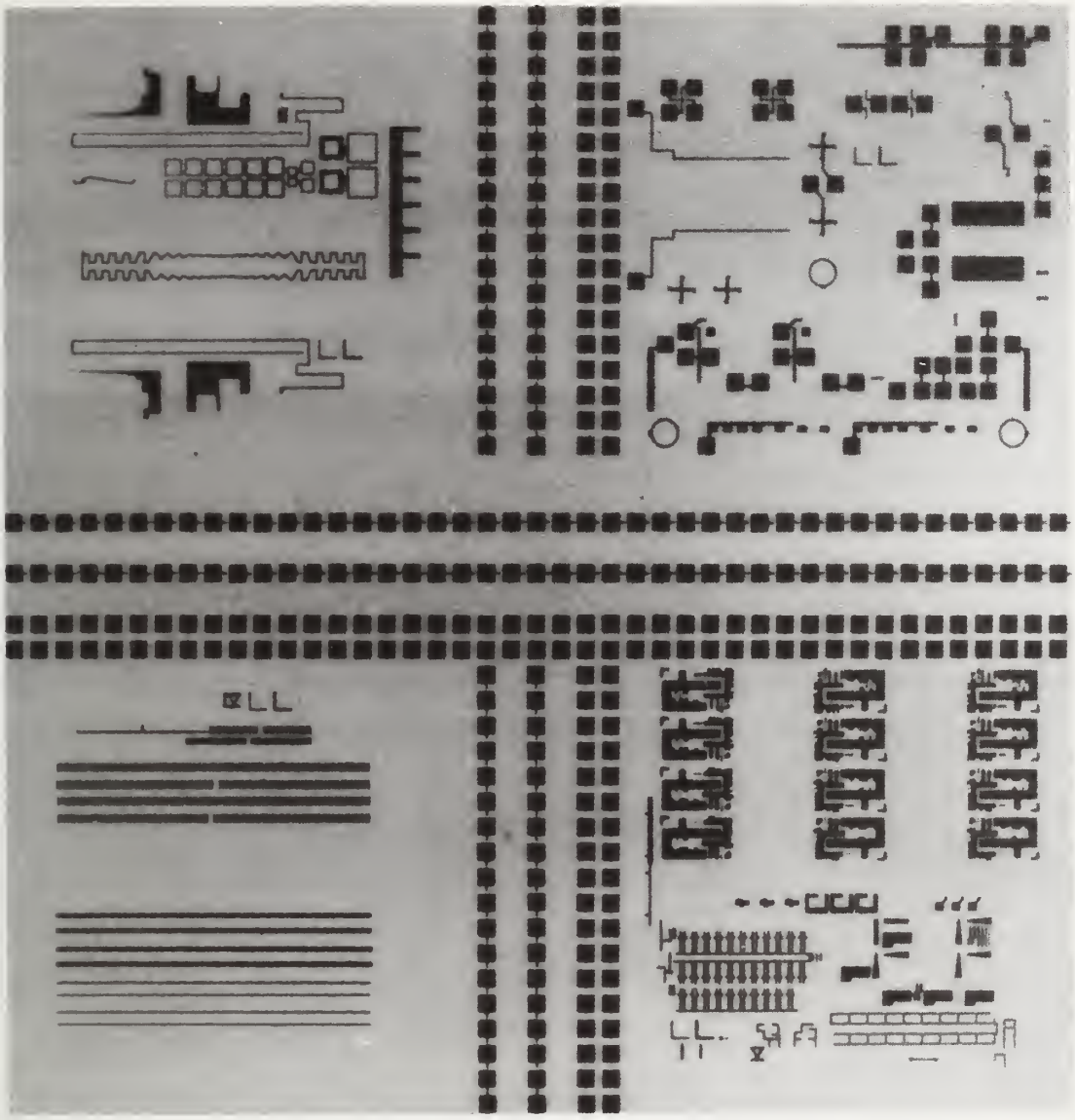

Figure A-3. Level 3, poly gates.

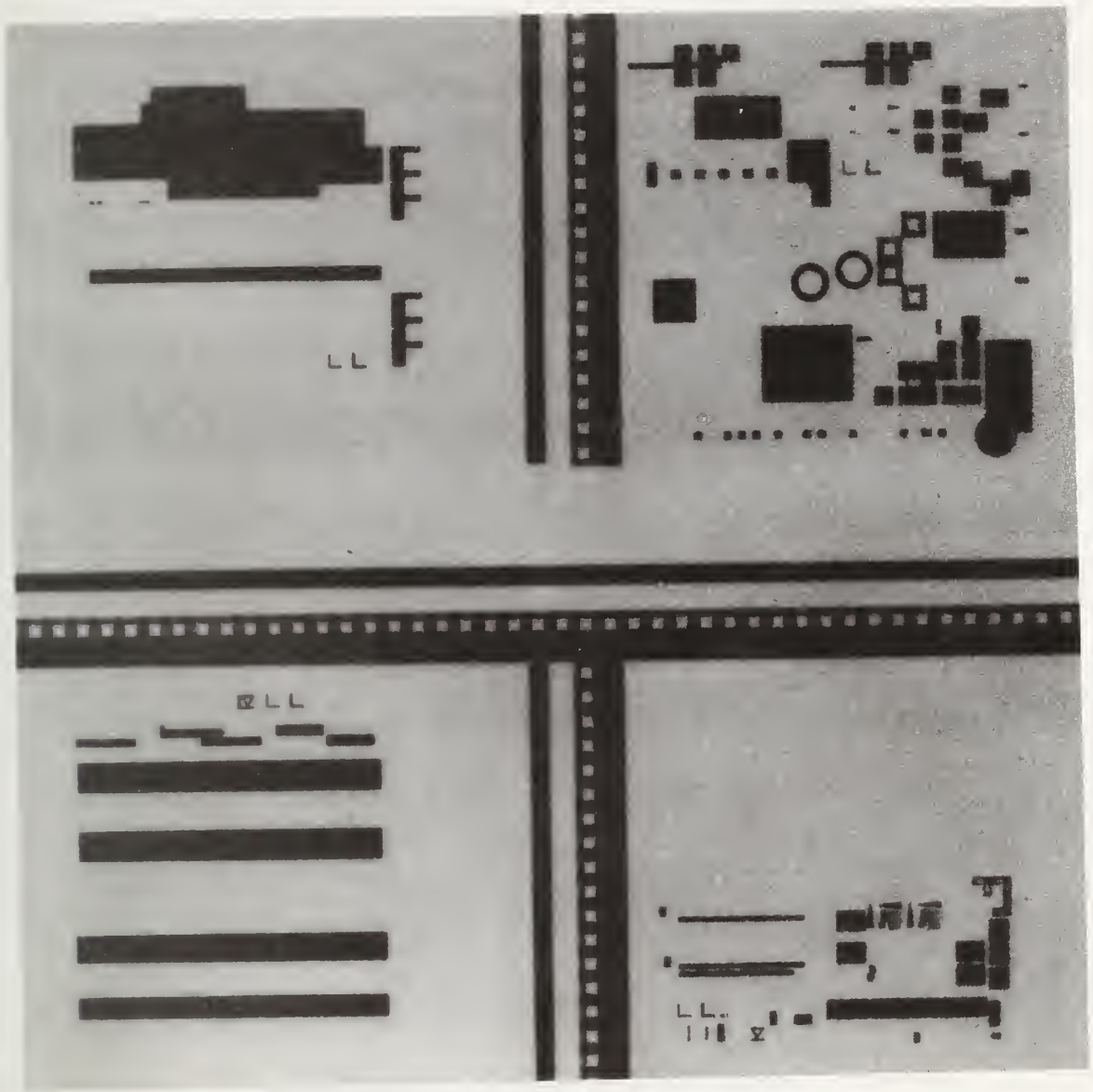

Figure A-4. Level 4, n+ doped oxide.

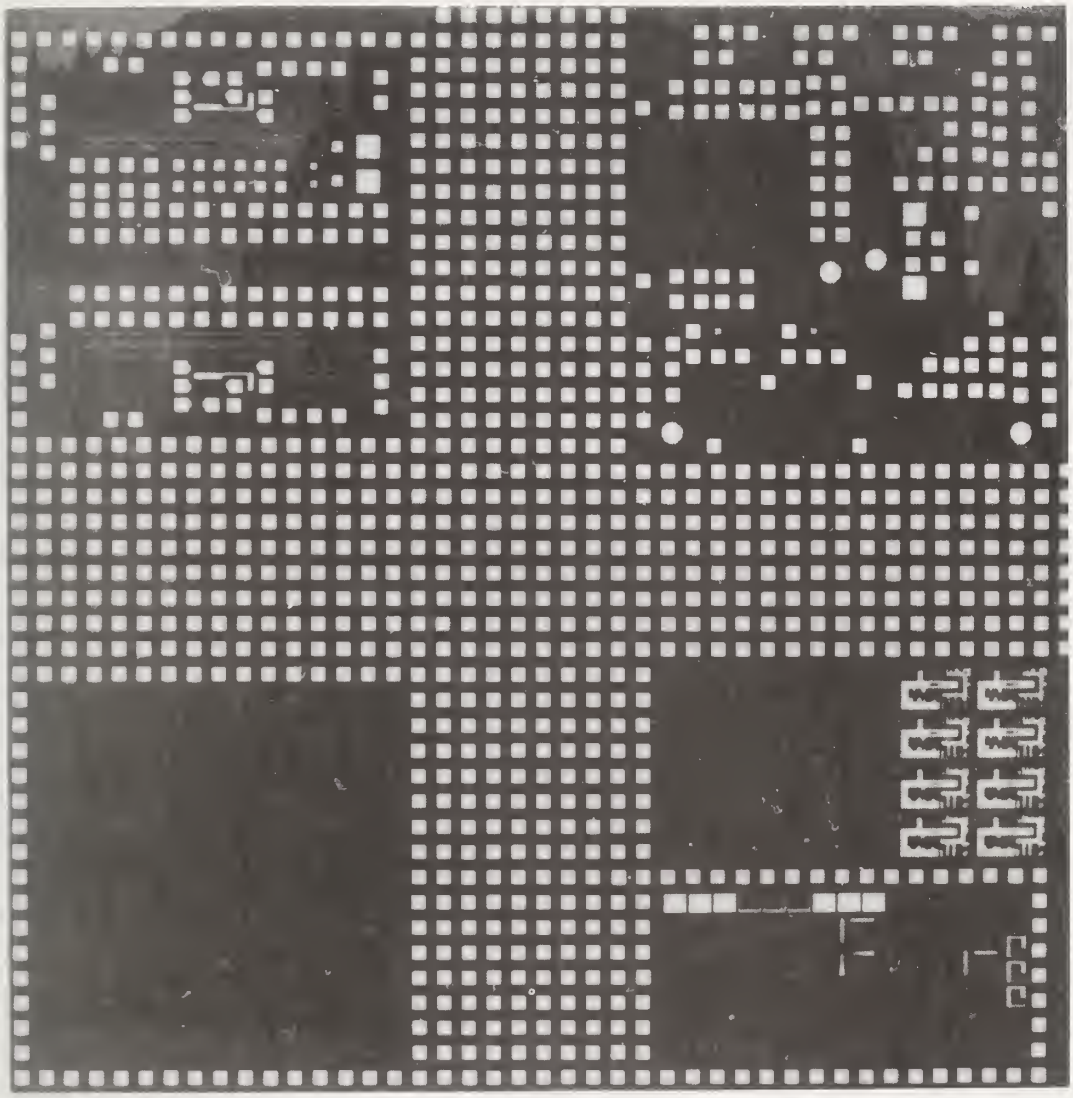

Figure A-5. Level 5, contact openings.

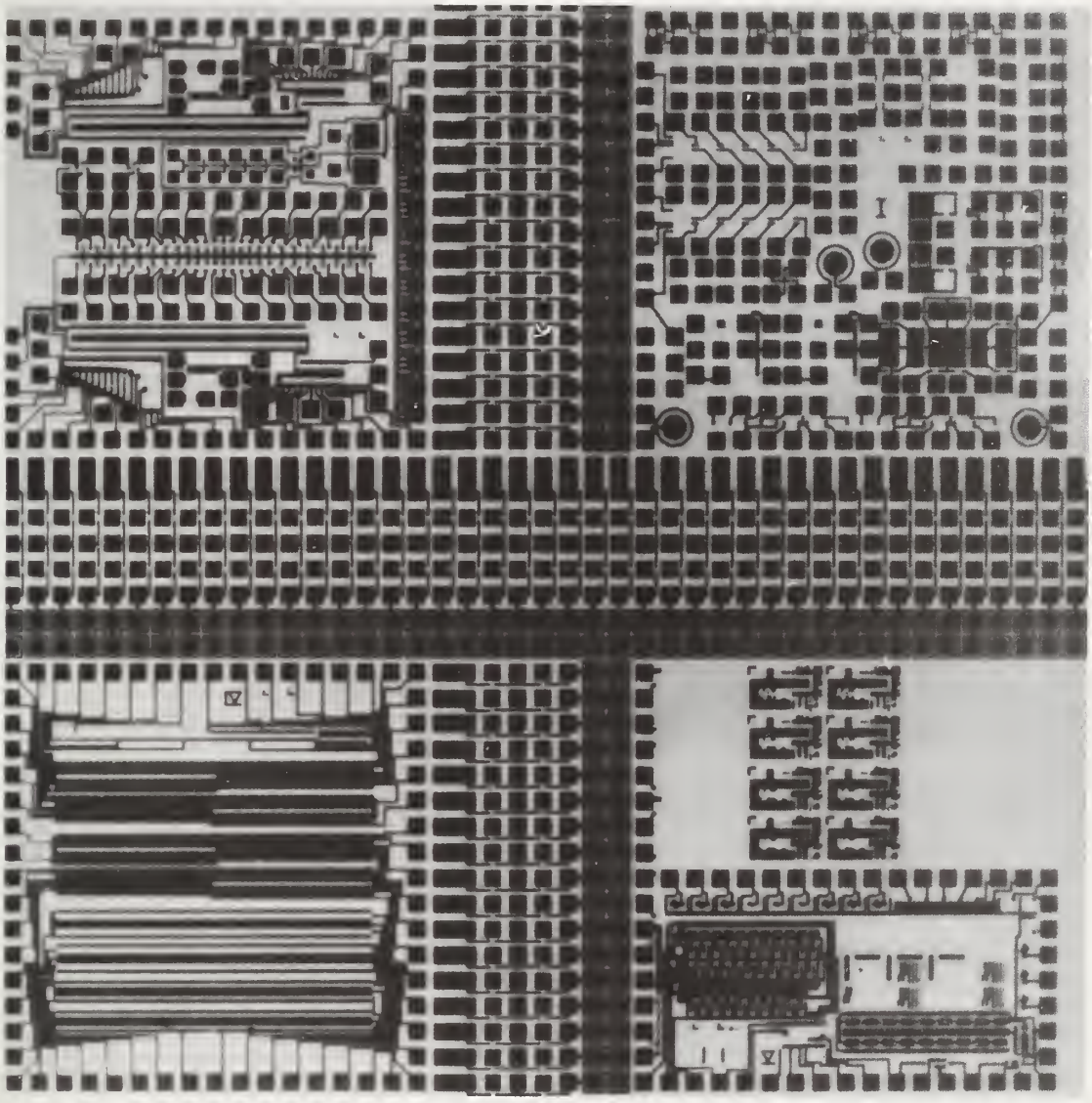

Figure A-6. Level 6, metal.

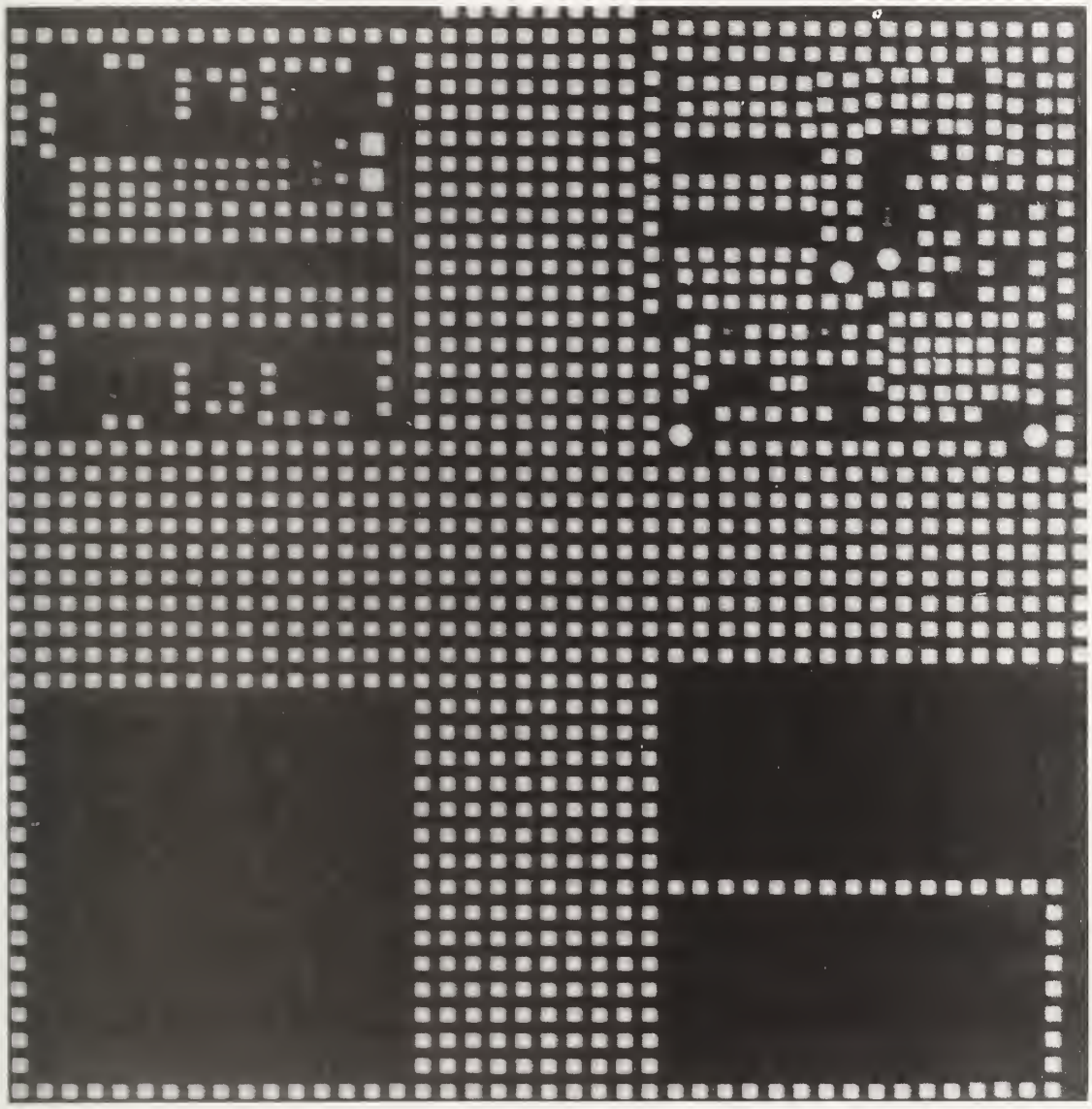

Figure A-7. Level 7, bond pad - overcoat.

APPENDIX B

OTHER USES OF STRUCTURES

It may be readily appreciated that the ideas and concepts developed during the creation and testing of this pattern have produced other uses for some of the structures or for the pattern itself. One version which was created eliminated the type II cross and left only the quadrants. This allowed a higher magnification lens to be used during the final reduction. Another version was created from the type III quadrant, two structures from the type I quadrant and half of each direction of the type II cross. This version was used for SOS material characterization along with other very large geometry structures on the same wafer. The very large geometry structures were for use with instruments such as TEM, SIMS, etc so that direct comparisons of physical performance with electrical performance could be achieved. It is of course clear that any structure on the pattern can be repeated many times to produce a structure of a type II class or to provide more sensitivity to defects. An example of this is shown in figure B-1 where structure IV-3 was repeated many times to provide up to 11,750 nominally identical transistors. These are available as 250, 500, 1000, 2000, 3000, or 5000 or as any combination thereof by the testing method. This pattern is particularly useful for gate dielectric studies. It can also be used for detecting open poly or metal lines over silicon steps and for measurement of circuit leakage.

Many other uses will no doubt appear in the future.

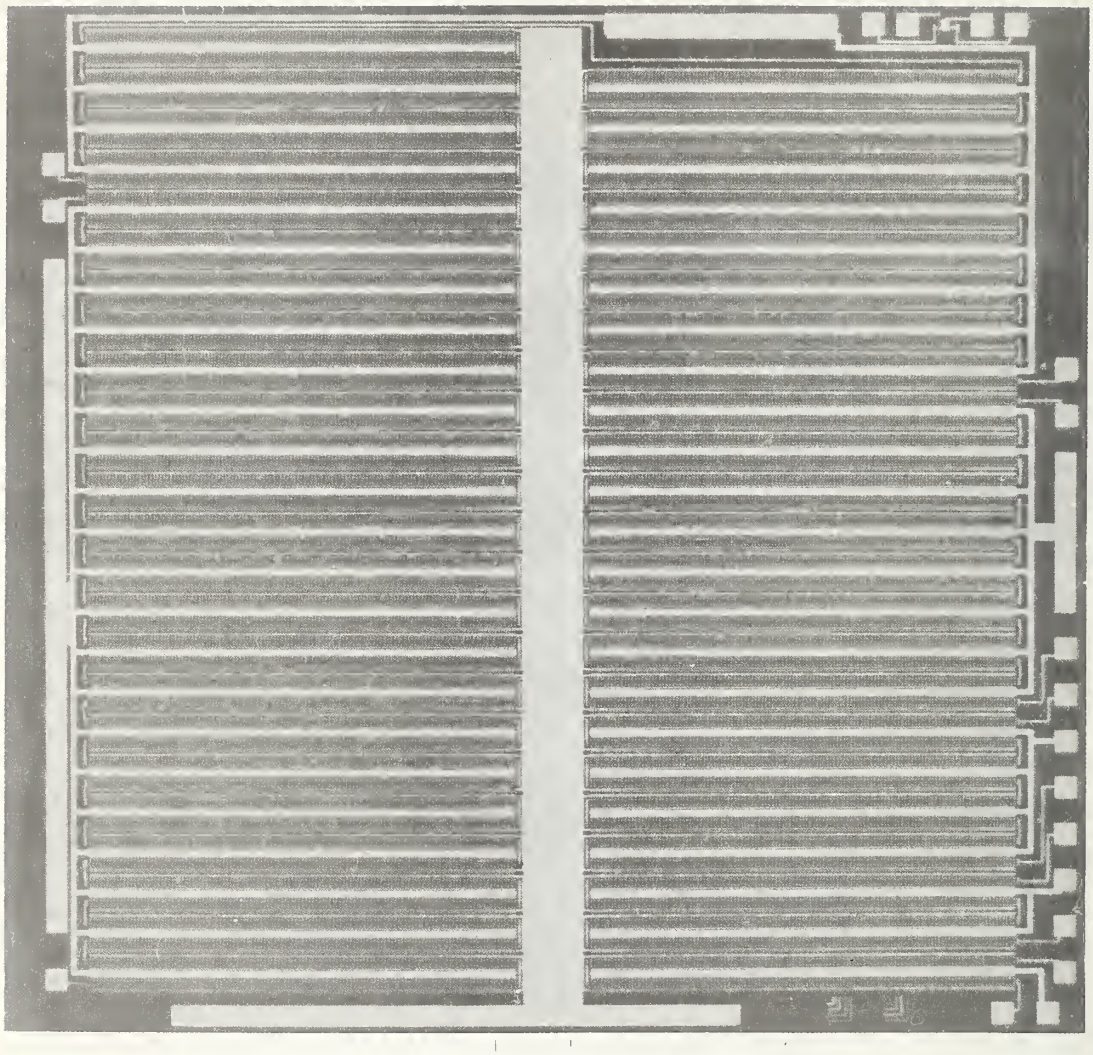

Figure B-1. Defect-sensitive pattern created from structures in main pattern.

APPENDIX C

CROSS REFERENCE LIST

	Item	Primary Structure Nos.	Secondary Structure Nos.	Other Possible Structures
1.	Film Thickness	V-42	I-18,20,27,29,33,37 (using capacitance)	I-21,I-30,III-11, III-12,I-42,43 (using capacitance)
2.	Undoped or Lightly Doped Epi Resistance	I-4,I-5,III-11, II-12	I-48,I-49	any junctionless MOS transistor
3.	Epi Doping	I-29,I-20,II-1	I-24,I-30,III-11 III-12,II-2,I-41-44	I-4,I-5 for Hall measurements
4.	Epi Mobility (Field Effect)	I-4,I-5	I-48,I-49,III-11, III-12	any MOS transistor
5.	Epi Mobility (Hall)	I-4,I-5	I-48,I-49	
6.	Heavily Doped Epi Resistance n+	I-52,I-57	I-56,I-72	
7.	Heavily Doped Poly Resistance p+	I-53	I-62	
8.	Heavily Doped Poly Resistance p-	I-51,I-64	I-60	
9.	Contact Resistances			
	p+ Epi	I-58	I-74,III-15	IV-5,IV-9,I-78
	n+ Epi	I-56	I-71,III-14	IV-6,IV-9,I-78
	p+ Poly	I-62	III-17	IV-7,IV-9,I-78
	p- Poly	I-60	III-16	IV-8,IV-9,I-78

	Item	Primary Structure Nos.
10.	Metal Resistance	I-45,I-3
11.	Probe Resistance	II-5
12.	Single Crossovers	
	Al Over n+ Epi	I-7,I-78
	Al Over p+ Epi	I-8,I-78
	Al Over p+ Poly	I-11,I-78
	Al Over p- Poly	I-9,I-78
	p+ Poly Over (p+ Epi)	I-14,I-78
	p- Poly Over (n+ Epi)	I-12,I-78
13.	Multiple Crossovers	
	Al Over n+ Epi	IV-6,IV-9
	Al Over p+ Epi	IV-5,IV-9
	Al Over p+ Poly	IV-8,IV-9
	Al Over p- Poly	IV-8,IV-9
	p+ Poly Over (p+ Epi)	IV-2,IV-9
	p- Poly Over (n+ Epi)	IV-1,IV-9
14.	Ungated p-n Junction Properties	I-4,I-83,I-92
15.	Gate-Controlled p-n Junction	I-3,I-79,I-80,I-85 I-88,I-89,I-94
16.	Channel Oxide Dielectric Properties	
	Top Only	
	(p+ Epi)	I-29,I-30,
	(n+ Epi)	I-20,I-21,II-1
	(n+ -p Epi)	I-43,I-42,II-2
	Top Mostly	
	(p+ Epi)	I-24

Item	Primary Structure Nos.
(n+ Epi)	I-15
(n+ Epi)	I-15
n+ -p Epi	I-41,I-44
Edge Mostly	
(p+ Epi)	I-31
(n+ Epi)	I-22
Corner	
(p+ Epi)	I-32
(n+ Epi)	I-23
Spatial Distribution	
(p+ Epi) With Edges	II-4
(n+ Epi) No Edges	II-1
(n+ Epi) With Edges	II-3
(n+ -p+ Epi) No Edges	II-2
Large Numbers of Edges	
(p+ Epi)	IV-2
(n+ Epi)	IV-1
Large Area With Large Number of Edges	
(p+ Epi)	IV-4
(n+ Epi)	IV-3
17. Field Oxide Dielectric Properties	
Top Only	
n+ Epi	I-18
p+ Epi	I-27
p- Poly	I-37
p+ Poly	I-33
Top Mostly	
n+ Epi	I-19
p+ Epi	I-28
p- Epi	I-38
p+ Poly	I-34
Edge Mostly	
n+ Epi	I-16
p+ Epi	I-25
p- Poly	I-39
p+ Poly	I-35
Corner	
n+ Epi	I-17
p+ Epi	I-26
p- Poly	I-40
p+ Poly	I-36
Large Number of Edges	
n+ Epi	IV-6
p+ Epi	IV-5
p- Poly	IV-8
p+ Poly	IV-7

Item	Primary Structure Nos.
18. MOS Transistor Properties	
Single Ordinary	
n-Channel	I-70,II-3
p-Channel	I-73,II-4
Spatial Distribution Ordinary	
n-Channel	II-3
p-Channel	II-4
Smooth Edgeless	
n-Channel	I-2
p-Channel	I-1
Sharp Corners Edgeless	
n-Channel	III-7
p-Channel	III-8
Variable Channel Length With Edges	
n-Channel	III-1
p-Channel	III-2
Variable Channel Length With No Edges	
n-Channel	III-7
p-Channel	III-8
Variable Channel Width With Edges	
n-Channel	III-3
p-Channel	III-5
Variable Channel Width With No Edges	
n-Channel	III-7
p-Channel	III-8
Variable Orientation	
n-Channel	III-9
p-Channel	III-10
Large Channel Areas	
n-Channel	III-11
p-Channel	III-12
Large Numbers of Parallel Devices With Short Channels	
n-Channel	IV-1
p-Channel	IV-2
Large Numbers of Parallel Devices With Long Channels	
n-Channel	IV-3
p-Channel	IV-4
Six Identical Ordinary Devices for Reliability,	

Item	Primary Structure Nos.
18. Continued	
Radiation, or Bias Temperature Testing Under Different Bias Conditions (simultaneous)	
n-Channel	I-76
p-Channel	I-77
19. Floating-Gate Devices Transistors	
n-Channel	I-82,I-87,I-95
p-Channel	I-86,I-91,I-96
Diodes	
p+n	I-84,I-93
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van der Pauw	
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n+ Contacts	I-47
20. Dimensions Electrical Measurements	
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Poly	V-2
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Optical	
Epi On Sapphire	V-31
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n+ On Sapphire	V-29
Contacts on n+ Epi	V-16
Metal On Sapphire	V-28
Contacts On p+ Epi	V-22
Contacts On p- Poly	V-20
Contacts On p+ Poly	V-26
Poly Epi	V-19
n+ On p+ Epi	V-18
n+ On p+ Poly	V-17
Al On p+ Epi	V-21
Al On n+ Epi	V-23
Al On p+ Poly	V-25
Al On p- Poly	V-27
21. Visible Interactions Between Two Levels	
Epi-Poly	V-4,V-19
n+-Epi	V-18
n+-Poly	V-17
Contact -Epi	V-7,V-16,V-22
Metal-Epi	V-5,V-21,V-23
Contact-Poly	V-8,V-20,V-26
Metal-Poly	V-6,V-25,V-27
22. Alignment Between Two Levels Electrical	
Poly-Epi	V-10
Poly-Metal	V-11
Poly-Contact	V-13
n+ -Epi	V-14
Metal-Contact	V-15
Epi-Contact	V-12
Epi-Metal	V-9
Optical	
Poly-Epi	V-35,V-40,V-41
n+ Epi	V-34,V-40,V-41
Contact-Epi	V-32,V-40,V-41
Metal-Epi	V-38,V-40,V-41
n+ Poly	V-33
Contact-Poly	V-39
Metal-Poly	V-37
Contact-Metal	V-36
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7.	Aluminum-Gate MOS Capacitors on poly-single contact type	I-33, 34, 35, 36, 37, 38, 39, 40	113
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16. ABSTRACT *(A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.)*

This report contains detailed information concerning a comprehensive approach to parametric process characterization for IC processes. This includes defining the general areas of importance, devising structures which are sensitive to these areas, devising methods for testing the structures, documenting the structures, tests, and results, producing suitable data reduction and presentation schemes, and considering the implementation of the methods in a practical sense. Proper methods for automatically testing some of these structures are explored. Seven divisions were created for the general types of test structure: (1) individual structures of nominal dimensions, (2) closely spaced identical structures, (3) structures of various sizes, (4) series and parallel combinations of structures, (5) structures especially sensitive to lithographic properties, (6) basic circuit building blocks, and (7) small area test circuits.

A test pattern, compatible primarily with silicon on sapphire technology, which integrates into a single mask set (6 levels) test structures to measure the properties of each of these basic divisions, was created and partially tested. This concept of total integration is shown to be valuable for determining causes and effects of many kinds with the use of only a small number of test wafers. An attempt was made to use computer-aided techniques as much as possible. These found application in mask making (the masks would have been much more difficult to create without the computer), docu-

(continued)

17. KEY WORDS *(six to twelve entries; alphabetical order; capitalize only the first letter of the first key word unless a proper name; separated by semicolons)* Comprehensive process characterization; design rules; intradie parametric integrity; LSI circuits; mask alignment tolerances; modular test programs; parametric yield limitations; performance limitations; photomask performance; process control; test patterns; test structures; total process integration.

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mentation (where computer line drawings were used as the basic drawings), testing (where a standardizable building block approach was implemented), and finally, the traditional use of the computer for data reduction and presentation. The test pattern contains 175 individually identified test structures and has approximately 1250 electrical access pads for each chip. The chip dimensions are 258 by 258 mil (6.553 x 6.553 mm). All of these structures are documented with cross sections and line drawings. A discussion of the intended uses of the structures, of their peculiarities, and samples of actual test results for many of the structures are included. A "small-signal" approach to testing, data analysis, and test structure design was used in several cases. For the test structure design, the small-signal approach is particularly useful with respect to physical structure sensitivity. For the testing, it finds traditional applications in the measurement of slopes while in the data analysis differences in identically acquired data from different wafers are frequently the desired information.

Results from a limited use of the pattern on a sampling of wafers from a few lots indicated that contact resistance effects and deposited oxide pin holes were much more important than previously thought. Alignment measurements between photomasking levels were obtained with an accuracy of $\pm$250 Å. The closely spaced and nominally identical structures are shown to be especially valuable for determining the nature of the individual measurements and for providing some of the best clues to the causes of the observed variations.

The uses of the overall approach include processing facility comparisons using structures with understandable outputs, detecting the least controlled parts of the process, providing a solid base on which to define circuit design rules, and predicting parametric yield loss to be expected due to circuit design-process incompatibility.

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