Semiconductor Measurement Technology:

Safe Operating Area Limits for Power Transistors

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PREFACE

This is the script for the third in a series of videotape presentations being
distributed on loan without charge in order to disseminate more effectively to the
semiconductor community the measurement technology improvements developed under the
Semiconductor Technology Program in the Electronic Technology Division of the National
Bureau of Standards (NBS).

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materials and devices in national and international commerce and for use by industry in
controlling device fabrication processes. Its major thrusts are the development of care-
fully evaluated and well documented test procedures and associated technology and the
dissemination of such information to the electronics community. Application of the output
by industry will contribute to higher yields, lower cost, and higher reliability of semi-
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government agencies which will lead to greater economy in government procurement. In
addition, improved measurement technology will provide a basis for controlled improvements
in fabrication processes and in essential device characteristics.

The Program receives direct financial support principally from two major sponsors:
The Defense Advanced Research Projects Agency (ARPA), and the National Bureau of Standards.

The ARPA-supported portion of the Program addresses critical Defense Department problems in
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Program emphasize aspects of the work which relate to the specific needs of the supporting
agency. Measurement oriented activity appropriate to the mission of NBS is an essential
aspect in all parts of the Program. Support for the work reported here came solely from
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Semiconductor Measurement Technology:

Safe Operating Area Limits for Power Transistors

Videotape Script

by

David L. Blackburn

This is a script of a videotape presentation which addresses deficiencies of present methods for measuring and specifying the power dissipation capabilities and safe operating area (SOA) limits for power transistors. These deficiencies result from not including adequately the effects of significant temperature nonuniformities which occur, primarily for high-voltage, low-current conditions. Firstly, the specified thermal resistance of a transistor can be applied strictly only when the junction temperature is relatively uniform, otherwise the power capability of the device can be grossly overestimated. Secondly, the use of the standard method for measuring junction temperature can lead to a serious underestimate of the peak junction temperature if the temperature distribution is not uniform. Finally, the traditional SOA limits do not consider the phenomenon of thermal instability and the hot spots that ensue. As a result, devices can operate with potentially dangerous hot spots within operating limits that traditionally have been considered to be safe. It is proposed that the SOA limits be revised to exclude operating conditions where thermal instability and hot spots can occur. A method for detecting the onset of thermal instability and triggering a circuit to turn-off the transistor under test is described. This approach can be used to develop the revised SOA limits in a nondestructive way.

Key Words: Hot spots; junction temperature; measurement technology; nondestructive test; reliability; safe operating limits; second breakdown; semiconductor devices; thermal characterization; thermal instability; thermal resistance; transistors.

Thermal resistance and junction temperature are parameters which are widely used to determine how much power a transistor may dissipate. They are also used to help to determine the safe operating area limits of power transistors.

Unless we know how to interpret these parameters and limits, we may reduce the performance, reliability, and life of the transistors we use. There are several problems we should be aware of. First, the concept of thermal resistance can be applied for only certain operating conditions. Second, the measurement of junction temperature as commonly performed can lead to serious underestimates of the actual temperatures. Finally, the forward-bias safe operating area limits of power transistors are frequently inadequate. Even if the transistor operates within its specified safe operating area, the peak junction temperature may be far in excess of the maximum rated junction temperature.

We have developed what we believe to be an improved nondestructive method for specifying safe operating area limits for transistors. By using this method, the region of excessively high temperatures is excluded from the safe operating area.
Before we discuss this method, let us review the concept of thermal resistance and the measurement of junction temperature – first for the ideal world and then for the real world where temperature non-uniformities and hot spots can occur.

The concept of thermal resistance provides a simplistic way of indicating the power dissipation capability of a transistor. It can be understood by analogy between thermal and electrical characteristics. [Graphic 1] Temperature difference, \( T_J - T_R \), is analogous to voltage difference, \( V_1 - V_2 \); heat flow, \( Q \), corresponds to electrical current, \( I \); and thermal resistance, \( R_\theta \), to electrical resistance, \( R \). By measuring the junction temperature for a given power dissipation, we can calculate the thermal resistance of the transistor. We then have a number which can be used as a measure of the power dissipation handling capability of the transistor. For a given maximum allowed junction temperature, the lower the thermal resistance, the higher the power which can be dissipated in the transistor.

Implicit in the use of thermal resistance is the assumption that we have a method for accurately measuring the junction temperature. If the temperature is uniform across the device, a number of electrical parameters of the transistor can be used to measure the temperature. They are the forward junction voltages (which are measured at a particular current), the junction leakage currents, and the current gain. We have found that the best one to use is the forward voltage of the emitter-base junction.

The basis for using the emitter-base forward voltage as a thermometer can be seen by this relationship. [Graphic 2] For a constant forward current density, the magnitude of the emitter-base forward voltage decreases linearly with increasing temperature. If we increase the current density, the curve shifts upward but the slope does not change significantly.

The temperature coefficient of the forward voltage is determined for a device
type by selecting an appropriately small forward current and measuring the forward voltage for different ambient temperatures. These ambient temperatures can be generated with a hot plate or an oven. This is the procedure that is used in the calibration step of a standard method to measure junction temperature.

This standard was developed by NBS in cooperation with the Joint Electron Device Engineering Councils Committee on Power Transistors. The standard was published by the Electronic Industries Association in 1975 [1].

The measuring circuit used with the standard method is called the emitter-only switching circuit; the only switching that occurs is at the emitter of the device being tested. [Graphic 3] The collector voltage is maintained at a constant value during both the heating and measurement cycles. This voltage is the same as used in the calibration step.

To measure the junction temperature for a given power level, heating power, which is controlled by $V_{EE}$, is applied to the device under test. The power dissipation is equal to the product of the collector current and the collector-emitter voltage. After the transistor reaches a steady-state temperature, the heating current is switched from the device by diverting it to ground through transistor Q which has been turned on by the clock pulse. Now only the small measuring current, $I_M$, is applied to the device under test. Its magnitude is controlled by $V_{MM}$.

The emitter-base voltage is sensed by the sample-and-hold unit as quickly as possible after the heating current has been removed and its value displayed on the digital

voltmeter. The junction temperature can be calculated using the temperature coefficient of the forward voltage that was obtained in the calibration part of the procedure, where the same measuring current $I_m$, and the same collector voltage were used. The thermal resistance of the transistor is then calculated from the measured power and the measured junction temperature.

Until now we have tacitly been in the ideal world of uniform current and temperature distributions in transistors. The junction voltage can be uniquely related to temperature only when the entire junction is at the same temperature. The real world, though, is usually not like that.

Let us see why. This power transistor has had its cap removed so that we can look directly at the transistor chip. Let us take a closer look. Under the microscope we can see that the emitter and base regions are interdigitated. [Graphic 4A] I took a similar transistor and coated the surface of the chip with a thermographic phosphor to display its temperature distribution while it dissipates power [2]. This phosphor fluoresces when it is illuminated with near ultraviolet radiation. The intensity of the fluorescence decreases as the temperature increases. Hotter areas of the phosphor appear darker than cooler ones.

This is how the coated chip looks when illuminated with ultraviolet radiation for a high-current, low-voltage operating condition. [Graphic 4B] There is not much variation in the intensity of the fluorescence. This indicates a relatively uniform temperature across the transistor chip, and implies that the power dissipation and therefore the collector current density are also relatively uniform. Now, let us increase the collector-emitter voltage and decrease the collector current in a way that keeps the power dissipation constant. [Graphic 4C] The fluorescence is no longer uniform. In fact there is a well defined dark spot which tells us that this area is much hotter than the surrounding area. This is a stable hot spot. Nearly all of the collector current passes through this spot. So we see that severe temperature nonuniformities can and do occur in transistors. We expect to see the most severe nonuniformities for low-current, high-voltage operations.

This shows that the thermal resistance of the transistor is not constant. We have not changed the power dissipation in the transistor by changing the current and voltage. Yet, the peak junction temperature in the transistor has changed dramatically. In this case it has changed by about 150°C.

Usually a thermal resistance value for the transistor is calculated from measurements made under high-current, low-voltage conditions. But if we do this, we can seriously underestimate the peak junction temperature which exists for other operating conditions.

There is yet another problem. If we do have a nonuniform temperature distribution over the junction, what temperature do we measure when we use the electrical method that I have just described? Let us take a look at this problem in a little more detail using this cutaway view of a transistor, which shows the base metallization and diffusion,
the emitter metallization and diffusion, and the collector region. [Graphic 5A]

During calibration to determine the temperature coefficient of the forward voltage, the transistor is in a uniform temperature environment. It is conducting the small measuring current, represented by these few vertical lines. [Graphic 5B] The power dissipation is extremely small so the junction temperature is essentially uniform as indicated by the horizontal line.

With heating power applied to the transistor, the steady-state temperature and current distribution might be represented in this way for a high-current, low-voltage operating condition. [Graphic 5C] We do not expect appreciable nonuniformities, even though there may be some small ripples in the temperature distribution; these ripples result from the effect of the emitter fingers.

To measure the forward voltage, the heating current is diverted from the device leaving only the measuring current which has assumed the uniform distribution of the heating current. [Graphic 5D] Therefore, the measuring current will have essentially the same distribution it had during calibration. Because the measurement and calibration conditions are very similar, an accurate measurement of the junction temperature can be obtained.

Consider, though the case where we try to measure the junction temperature when the heating current is constricted as we have seen for low-current, high-voltage conditions. [Graphic 5E] When we divert the heating current, the measuring current, which essentially takes the
distribution of the heating current, is very much different from the relatively uniform distribution we had during calibration. [Graphic 5F] The critical difference is that the density of the measuring current is much higher than that during calibration! We are no longer on the calibration curve we developed earlier to obtain the temperature coefficient of the forward voltage. We are on some higher one.

But we must know what the measurement current density is in the hot spot to know how to shift the calibration curve. This can be determined from the cooling response of the transistor [3]. Doing this we can obtain estimates of the peak junction temperature which are only about 10 percent below the value obtained from direct infrared measurements. But if we ignore the change in current density, we can underestimate the peak junction temperature by as much as 40 percent or even more.

So, in the real world we have to realize that the thermal resistance is not constant, the junction temperature is not a unique quantity, and significant underestimates of the peak junction temperature are possible.

I have talked about hot spots and temperature nonuniformities. What causes the current in the transistor to constrict to generate these hot spots? The answer, in brief, is thermal instability. In 1963,

Scarlett, Shockley, and Haitz [4] first wrote about the nature of thermal instability. In 1976 we, with Dr. Philip Hower of the Westinghouse Research Labs, were able to show that it is possible to predict quite accurately operating conditions where thermal instability will begin [5], [6], [7].

This thermal instability can lead to a runaway condition which ends in second breakdown and, generally, device failure. For some operating conditions, however, internal processes act degeneratively on the increasing current density to check this instability. If the instability is checked, a stable hot spot will be formed. Temperatures in such hot spots are typically greater than 200°C and often in excess of 300°C. The dominant process that works to stabilize the current density is the base widening effect which occurs at high current densities [5], [7]. This occurs in nearly all transistors except for single-diffused structures where no stable hot spots have been found [5].

There are several ways for measuring the onset of thermal instability. Let us look at two of them. When stable hot spots occur, the common emitter gain of the transistor decreases suddenly. We can see the development of a hot spot while we monitor the transistor gain. [Video Insert] This phosphor-coated transistor chip is illuminated with near ultraviolet light so that we can observe the temperature distribution over the surface of the chip. On the cathode ray screen we plot the collector voltage, on the horizontal axis, and the base current, on the vertical axis. We keep the collector current constant so the base current varies inversely with transistor gain. As the collector voltage is increased, the base current decreases slightly until suddenly the hot spot occurs. The voltage has to be decreased considerably before the hot spot suddenly disappears and the base current decreases abruptly. This is what we call thermal hysteresis [8]. We can cycle the applied voltage a number of times to show it is quite repeatable.

You would not ordinarily be aware that the transistor is in such a hot-spot mode unless you were specifically trying to detect it. However, the switching time, gain, and linearity of the transistor are affected by the presence of the hot spot. Both


switching time and gain are reduced and nonlinear amplification is increased [9] by the hot spot.

A simpler way to detect the onset of thermal instability is by measuring the emitter-base voltage, which is temperature sensitive [10], [11], [12]. If we apply a pulse of power to the transistor and monitor the emitter-base voltage as the transistor heats, the voltage decreases.

[Graphic 6] A continuous concave upward curve such as this would indicate no instability. If a hot spot forms, we would see a step in the curve. This step is caused by the sudden increase in the rate of heating of the transistor caused by the thermal instability. Sometimes this step is clearly evident, but sometimes it is difficult to discern. To accent the step we can take the time derivative of the emitter-base voltage. [Graphic 7] Instead of looking for a step, we need only look for a pulse.

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In the laboratory, [Video Insert] an oscilloscope is used to monitor the derivative of the emitter-base voltage. We keep the emitter current constant and progressively increase the collector voltage with each successive power application. At first we see no pulse. Then when the voltage is great enough for thermal instability to occur, a pulse appears. As the voltage increases, the pulse moves to the left. The thermal instability occurs sooner after the application of power for greater values of applied voltage.

We can also connect a protective turn-off circuit which is activated when the pulse begins. It senses the leading edge of the pulse and turns off the transistor before it can enter into a fully developed hot-spot mode and reach any significant temperature extremes.

I have talked about thermal instability being stabilized by internal processes. For many operating conditions these processes are not capable of checking the instability. For these conditions, second breakdown occurs. Very high localized currents and temperatures are present when the transistor goes into second breakdown. Usually the transistor is either degraded or destroyed.

Here is an extreme case of what second breakdown can do to a transistor. [Video Insert] The current and temperature at the outer edges of these two emitter fingers became so great during second breakdown that two holes were formed extending completely through the die to form a collector-to-emitter short circuit. [Excerpt From Video Insert] This is a common failure mode of second breakdown.

The possibility of destruction through second breakdown is a primary reason for the use of safe operating area limits in transistor data and specification sheets. But these safe operating area limits are dictated not only by the limits imposed by second breakdown; they are also determined by the limits imposed by the thermal resistance as well as the maximum current and voltage limits.

The maximum safe operating area limits for transistors are usually plotted as the log of the collector current against the log of the collector-emitter voltage.
The maximum current is determined by such considerations as the size of the chip and interconnecting wires, the metallization, and the minimum allowable transistor gain. The maximum voltage is set by the breakdown characteristics of the collector-base junction. The establishment of these two limits is generally straightforward.

Continuing to fill in the gap between these two limits, we have the thermal limit. [Graphic 8B] In this region, the temperature distribution over the device is still relatively uniform so that the thermal resistance for the transistor can be used. For a maximum safe junction temperature, set by the manufacturer, a maximum allowed power can be calculated using the thermal resistance of the transistor. This power is constant and translates as a line with a slope of minus one.

The maximum safe operating area limit specification is completed with the second-breakdown limit. [Graphic 8C] The traditional way of determining the second-breakdown limit for a transistor type is to submit many devices to a destructive second breakdown test. They are operated in successively more stressful conditions until second breakdown occurs. The voltage and current are noted. By doing this for enough transistors over the voltage-current area of interest, a line can be drawn which is safely below all of the points at which second breakdown would be expected to occur.
This then completes the traditional maximum safe operating area limits that are usually specified. They do not take into consideration the existence of hot spots. Yet hot spots may actually appear within these limits, usually in this region.

Let us take a closer look at the region where hot spots do occur. In our work with Dr. Hower, we found that very specific relationships exist between thermal instability, stable hot spots, and second breakdown [5].

Thermal instability always precedes second breakdown. Stable hot spots exist in this region. Slightly to the left of the thermal instability limit, the junction temperature is relatively uniform and may be only 30°C to 40°C above the case temperature. A fraction of a volt to the right, the transistor is in a hot-spot mode. The temperature is nonuniform with the peak temperature often above the maximum allowed junction temperature for the transistor. If while in the hot-spot mode the voltage is increased sufficiently, the transistor will go into second breakdown. At lower currents and higher voltages, hot spots may not be stable and thermal instability will continue directly into second breakdown.

Superimposing this relationship on the traditional safe operating area [Graphic 8F]
we can see that hot spots can appear within the maximum safe operating area limits as they are presently specified. Therefore we propose that the safe operating area for transistors be revised to include protection against operation in the hot-spot mode. [Graphic 8G] Within this revised safe operating area, we can be assured that the transistor will be operated so that the junction temperature will be relatively uniform and below its maximum rated junction temperature.

While hot spots may not be immediately destructive, the very high localized temperatures can be expected to be degrading to the transistor with time. In this vein, recent work by Gaur and others [13] at IBM has shown crystal damage in transistors operating repeatedly under hot-spot-like conditions. Furthermore, the hot spots degrade gain and switching speed, and introduce nonlinear amplification. Therefore, the revised safe operating area represents a realistic limit for achieving the maximum reliability, performance, and life of transistors for operation under forward base drive conditions.

The limits of this area for a given device type can be determined nondestructively without sacrificing any transistors. This can be done by using the method I described involving the derivative of the emitter-base voltage to detect the onset of thermal instability. The derivative pulse can trigger a circuit to turn off the transistor under test before it is damaged by high, localized temperatures. This method is easily implemented not only by the device manufacturer who generates and verifies the safe operating area specifications of his product but also by the device user as a check of the products he buys.

Our discussion has centered around DC operation. For pulsed operation these limits move out and shift somewhat relative to each other. Depending on operating points, thermal instability and second breakdown can be initiated in times that range from milliseconds to microseconds. But the concepts developed for establishing these limits can also be applied in the case of pulsed operation.

Let me briefly review the points I made about the thermal characterization of power transistors.

First, the concept of thermal resistance cannot be used indiscriminately to define the maximum power the transistor can dissipate. To do so may grossly overestimate the power capability of the transistor.

Second, accurate measurement of the junction temperature is not straightforward. Temperature nonuniformities that can occur will result in serious underestimates of the actual peak junction temperature, if current density differences are not taken into account.

Third, the traditional way of developing safe operating areas of transistors may allow potentially dangerous hot spots to occur within the safe operating areas.

Finally, a method is now available which can be used to develop a revised safe operating area which avoids conditions where hot spots can occur.

CREDITS

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Semiconductor Measurement Technology: Safe Operating Area Limits for Power Transistors: Videotape Script

This is a script of a videotape presentation which addresses deficiencies of present methods for measuring and specifying the power dissipation capabilities and safe operating area (SOA) limits for power transistors. These deficiencies result from not including adequately the effects of significant temperature nonuniformities which occur, primarily for high-voltage, low-current conditions. Firstly, the specified thermal resistance of a transistor can be applied strictly only when the junction temperature is relatively uniform, otherwise the power capability of the device can be grossly overestimated. Secondly, the use of the standard method for measuring junction temperature can lead to a serious underestimate of the peak junction temperature if the temperature distribution is not uniform. Finally, the traditional SOA limits do not consider the phenomenon of thermal instability and the hot spots that ensue. As a result, devices can operate with potentially dangerous hot spots within operating limits that traditionally have been considered to be safe. It is proposed that the SOA limits be revised to exclude operating conditions where thermal instability and hot spots can occur. A method for detecting the onset of thermal instability and triggering a circuit to turn-off the transistor under test is described. This approach can be used to develop the revised SOA limits in a nondestructive way.

**ABSTRACT**

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**KEY WORDS**

Hot spots; junction temperature; measurement technology; nondestructive test; reliability; safe operating limits; second breakdown; semiconductor devices; thermal characterization; thermal instability; thermal resistance; transistors.
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