NBS SPECIAL PUBLICATION 400-44

U.S. DEPARTMENT OF COMMERCE / National Bureau of Standards

Semiconductor Measurement Technology:

Safe Operating Area Limits for Power Transistors

Videotape Script

NATIONAL BUREAU OF STANDARDS

The National Bureau of Standards[1] was established by an act of Congress March 3, 1901. The Bureau's overall goal is t strengthen and advance the Nation's science and technology and facilitate their effective application for public benefit. To thi end, the Bureau conducts research and provides: (1) a basis for the Nation's physical measurement system, (2) scientific an technological services for industry and government, (3) a technical basis for equity in trade, and (4) technical services to pro mote public safety. The Bureau consists of the Institute for Basic Standards, the Institute for Materials Research, the Institut for Applied Technology, the Institute for Computer Sciences and Technology, the Office for Information Programs, and th Office of Experimental Technology Incentives Program.

THE INSTITUTE FOR BASIC STANDARDS provides the central basis within the United States of a complete and consist ent system of physical measurement; coordinates that system with measurement systems of other nations; and furnishes essen tial services leading to accurate and uniform physical measurements throughout the Nation's scientific community, industry and commerce. The Institute consists of the Office of Measurement Services, and the following center and divisions:

Applied Mathematics — Electricity — Mechanics — Heat — Optical Physics — Center for Radiation Research — Lab oratory Astrophysics[2] — Cryogenics[2] — Electromagnetics[2] — Time and Frequency[2].

THE INSTITUTE FOR MATERIALS RESEARCH conducts materials research leading to improved methods of measure ment, standards, and data on the properties of well-characterized materials needed by industry, commerce, educational insti tutions, and Government; provides advisory and research services to other Government agencies; and develops, produces, an distributes standard reference materials. The Institute consists of the Office of Standard Reference Materials, the Office of Ai and Water Measurement, and the following divisions:

Analytical Chemistry — Polymers — Metallurgy — Inorganic Materials — Reactor Radiation — Physical Chemistry.

THE INSTITUTE FOR APPLIED TECHNOLOGY provides technical services developing and promoting the use of avail able technology; cooperates with public and private organizations in developing technological standards, codes, and test meth ods; and provides technical advice services, and information to Government agencies and the public. The Institute consists o the following divisions and centers:

Standards Application and Analysis — Electronic Technology — Center for Consumer Product Technology: Produc Systems Analysis; Product Engineering — Center for Building Technology: Structures, Materials, and Safety; Building Environment; Technical Evaluation and Application — Center for Fire Research: Fire Science; Fire Safety Engineering.

THE INSTITUTE FOR COMPUTER SCIENCES AND TECHNOLOGY conducts research and provides technical service designed to aid Government agencies in improving cost effectiveness in the conduct of their programs through the selection, acquisition, and effective utilization of automatic data processing equipment; and serves as the principal focus wthin the exec utive branch for the development of Federal standards for automatic data processing equipment, techniques, and computer languages. The Institute consist of the following divisions:

Computer Services — Systems and Software — Computer Systems Engineering — Information Technology.

THE OFFICE OF EXPERIMENTAL TECHNOLOGY INCENTIVES PROGRAM seeks to affect public policy and process to facilitate technological change in the private sector by examining and experimenting with Government policies and prac tices in order to identify and remove Government-related barriers and to correct inherent market imperfections that impede the innovation process.

THE OFFICE FOR INFORMATION PROGRAMS promotes optimum dissemination and accessibility of scientific informa tion generated within NBS; promotes the development of the National Standard Reference Data System and a system of in formation analysis centers dealing with the broader aspects of the National Measurement System; provides appropriate services to ensure that the NBS staff has optimum accessibility to the scientific information of the world. The Office consists of the following organizational units:

Office of Standard Reference Data — Office of Information Activities — Office of Technical Publications — Library — Office of International Standards — Office of International Relations.

---

[1] Headquarters and Laboratories at Gaithersburg, Maryland, unless otherwise noted; mailing address Washington, D.C. 20234.
[2] Located at Boulder, Colorado 80302.

Semiconductor Measurement Technology:

Safe Operating Area Limits for Power Transistors

David L. Blackburn

Electronic Technology Division
Institute for Applied Technology
National Bureau of Standards
Washington, D.C. 20234

U.S. DEPARTMENT OF COMMERCE, Juanita M. Kreps, Secretary

Dr. Sidney Harman, Under Secretary

Jordan J. Baruch, Assistant Secretary for Science and Technology

NATIONAL BUREAU OF STANDARDS, Ernest Ambler, Acting Director

Issued September 1977

Library of Congress Cataloging in Publication Data

Blackburn, David L.

Safe operating area limits for power transistors.

(Semiconductor measurement technology) (National Bureau of Standards special publication ; 400-44)

Supt. of Docs. Cat. no.: C13.10:400-44.

1. Power transistors—Testing. I. Title. II. Series. III. Series: United States. National Bureau of Standards. Special publication ; 400-44.

QC100.U57 no. 400-44 [TK7871.92] 602'.1s [621.31'7] 77-608172

National Bureau of Standards Special Publication 400-44

Nat. Bur. Stand. (U.S.), Spec. Publ. 400-44, 20 pages (Sept. 1977)

CODEN: XNBSAV

For sale by the Superintendent of Documents, U.S. Government Printing Office, Washington, D.C. 20402

Price $1—Stock No. 003-003-01833-3

☆ U.S. GOVERNMENT PRINTING OFFICE : 1977 O—244-870

PREFACE

This is the script for the third in a series of videotape presentations being distributed on loan without charge in order to disseminate more effectively to the semiconductor community the measurement technology improvements developed under the Semiconductor Technology Program in the Electronic Technology Division of the National Bureau of Standards (NBS).

The Semiconductor Technology Program serves to focus NBS efforts to enhance the performance, interchangeability, and reliability of discrete semiconductor devices and integrated circuits through improvements in measurement technology for use in specifying materials and devices in national and international commerce and for use by industry in controlling device fabrication processes. Its major thrusts are the development of carefully evaluated and well documented test procedures and associated technology and the dissemination of such information to the electronics community. Application of the output by industry will contribute to higher yields, lower cost, and higher reliability of semiconductor devices. The output provides a common basis for the purchase specifications of government agencies which will lead to greater economy in government procurement. In addition, improved measurement technology will provide a basis for controlled improvements in fabrication processes and in essential device characteristics.

The Program receives direct financial support principally from two major sponsors: The Defense Advanced Research Projects Agency (ARPA),* and the National Bureau of Standards.+ The ARPA-supported portion of the Program addresses critical Defense Department problems in the yield, reliability, and availability of integrated circuits. Other portions of the Program emphasize aspects of the work which relate to the specific needs of the supporting agency. Measurement oriented activity appropriate to the mission of NBS is an essential aspect in all parts of the Program. Support for the work reported here came solely from NBS.

Essential assistance to the Program is also received from the semiconductor industry through cooperative experiments and technical exchanges. NBS interacts with industrial users and suppliers of semiconductor devices through participation in standardizing organizations; through direct consultations with device and material suppliers, government agencies, and other users; and through periodically scheduled symposia and workshops. In addition, progress reports are regularly prepared for issuance in the NBS Special Publication 400 sub-series. More detailed reports such as state-of-the-art reviews, literature compilations, and summaries of technical efforts conducted within the Program are issued as these activities are completed. Reports of this type which are published by NBS also appear in the Special Publication 400 sub-series. Announcements of availability of all publications in this sub-series are sent by the Government Printing Office to those who have requested this service. A request form for this purpose may be found at the end of this report.

---

*Through ARPA Order 2397, Program Code 7D10 (NBS Cost Center 4257555).

+Principally through the Electronic Technology Program (Cost Center 4257100).

Semiconductor Measurement Technology:

Safe Operating Area Limits for Power Transistors

Videotape Script

by

David L. Blackburn

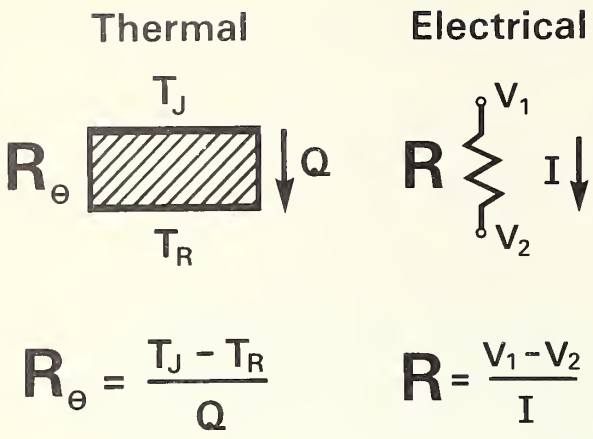
This is a script of a videotape presentation which addresses deficiencies of present methods for measuring and specifying the power dissipation capabilities and safe operating area (SOA) limits for power transistors. These deficiencies result from not including adequately the effects of significant temperature nonuniformities which occur, primarily for high-voltage, low-current conditions. Firstly, the specified thermal resistance of a transistor can be applied strictly only when the junction temperature is relatively uniform, otherwise the power capability of the device can be grossly overestimated. Secondly, the use of the standard method for measuring junction temperature can lead to a serious underestimate of the peak junction temperature if the temperature distribution is not uniform. Finally, the traditional SOA limits do not consider the phenomenon of thermal instability and the hot spots that ensue. As a result, devices can operate with potentially dangerous hot spots within operating limits that traditionally have been considered to be safe. It is proposed that the SOA limits be revised to exclude operating conditions where thermal instability and hot spots can occur. A method for detecting the onset of thermal instability and triggering a circuit to turn-off the transistor under test is described. This approach can be used to develop the revised SOA limits in a nondestructive way.

Key Words: Hot spots; junction temperature; measurement technology; nondestructive test; reliability; safe operating limits; second breakdown; semiconductor devices; thermal characterization; thermal instability; thermal resistance; transistors.

Thermal resistance and junction temperature are parameters which are widely used to determine how much power a transistor may dissipate. They are also used to help to determine the safe operating area limits of power transistors.

Unless we know how to interpret these parameters and limits, we may reduce the performance, reliability, and life of the transistors we use. There are several problems we should be aware of. First, the concept of thermal resistance can be applied for only certain operating conditions. Second, the measurement of junction temperature as commonly performed can lead to serious underestimates of the actual temperatures. Finally, the forward-bias safe operating area limits of power transistors are frequently inadequate. Even if the transistor operates within its specified safe operating area, the peak junction temperature may be far in excess of the maximum rated junction temperature.

We have developed what we believe to be an improved nondestructive method for specifying safe operating area limits for transistors. By using this method, the region of excessively high temperatures is excluded from the safe operating area.

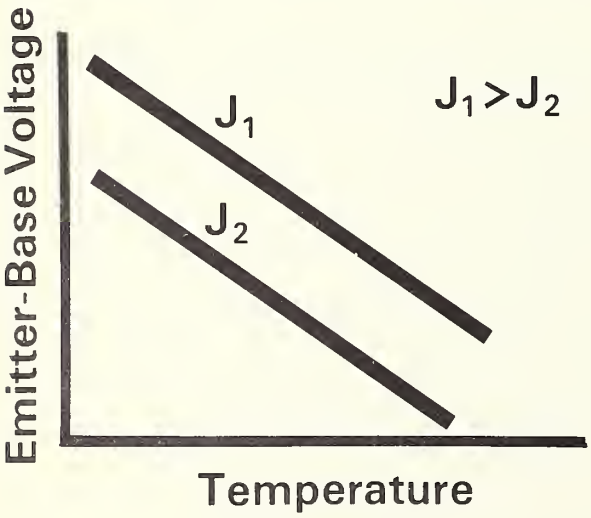


Graphic 1

Before we discuss this method, let us review the concept of thermal resistance and the measurement of junction temperature — first for the ideal world and then for the real world where temperature non-uniformities and hot spots can occur.

The concept of thermal resistance provides a simplistic way of indicating the power dissipation capability of a transistor. It can be understood by analogy between thermal and electrical characteristics. [Graphic 1] Temperature difference, $T_J - T_R$, is analogous to voltage difference, $V_1 - V_2$; heat flow, Q, corresponds to electrical current, I; and thermal resistance, R_θ, to electrical resistance, R. By measuring the junction temperature for a given power dissipation, we can calculate the thermal resistance of the transistor. We then have a number which can be used as a measure of the power dissipation handling capability of the transistor. For a given maximum allowed junction temperature, the lower the thermal resistance, the higher the power which can be dissipated in the transistor.

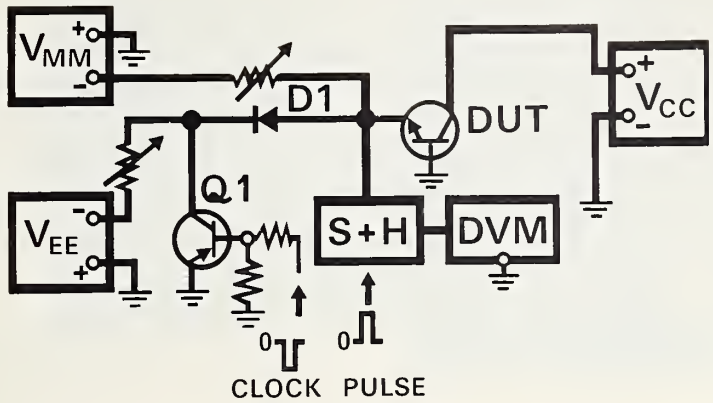
Implicit in the use of thermal resistance is the assumption that we have a method for accurately measuring the junction temperature. If the temperature is uniform across the device, a number of electrical parameters of the transistor can be used to measure the temperature. They are the forward junction voltages (which are measured at a particular current), the junction leakage currents, and the current gain. We have found that the best one to use is the forward voltage of the emitter-base junction.



Graphic 2

The basis for using the emitter-base forward voltage as a thermometer can be seen by this relationship. [Graphic 2] For a constant forward current density, the magnitude of the emitter-base forward voltage decreases linearly with increasing temperature. If we increase the current density, the curve shifts upward but the slope does not change significantly.

The temperature coefficient of the forward voltage is determined for a device



Graphic 3

type by selecting an appropriately small forward current and measuring the forward voltage for different ambient temperatures. These ambient temperatures can be generated with a hot plate or an oven. This is the procedure that is used in the calibration step of a standard method to measure junction temperature.

This standard was developed by NBS in cooperation with the Joint Electron Device Engineering Councils Committee on Power Transistors. The standard was published by the Electronic Industries Association in 1975 [1].

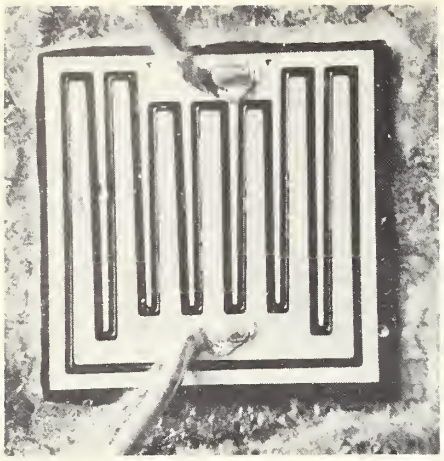
The measuring circuit used with the standard method is called the emitter-only switching circuit; the only switching that occurs is at the emitter of the device being tested. [Graphic 3] The collector voltage is maintained at a constant value during both the heating and measurement cycles. This voltage is the same as used in the calibration step.

To measure the junction temperature for a given power level, heating power, which is controlled by V_{EE}, is applied to the device under test. The power dissipation is equal to the product of the collector current and the collector-emitter voltage. After the transistor reaches a steady-state temperature, the heating current is switched from the device by diverting it to ground through transistor Q which has been turned on by the clock pulse. Now only the small measuring current, I_M, is applied to the device under test. Its magnitude is controlled by V_{MM}.

The emitter-base voltage is sensed by the sample-and-hold unit as quickly as possible after the heating current has been removed and its value displayed on the digital

---

[1] Thermal Resistance Measurements of Conduction Cooled Power Transistors, EIA Recommended Standard, RS - 313 - B (Revision of RS-313-A), October 1975 (Electronic Industries Association, 2001 Eye Street, N.W., Washington, DC 20006).



Graphic 4A

voltmeter. The junction temperature can be calculated using the temperature coefficient of the forward voltage that was obtained in the calibration part of the procedure, where the same measuring current I_M, and the same collector voltage were used. The thermal resistance of the transistor is then calculated from the measured power and the measured junction temperature.

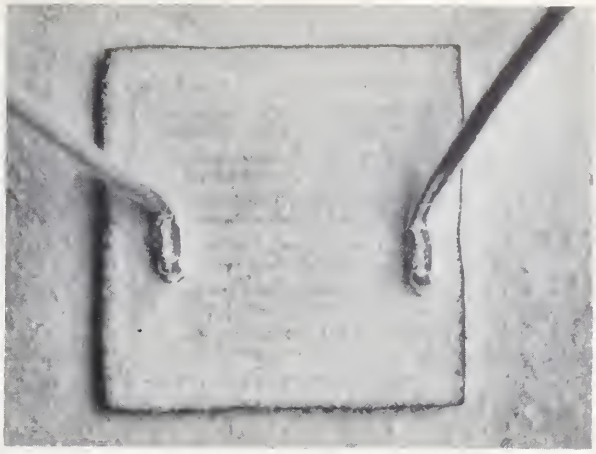
Until now we have tacitly been in the ideal world of uniform current and temperature distributions in transistors. The junction voltage can be uniquely related to temperature only when the entire junction is at the same temperature. The real world, though, is usually not like that.

Let us see why. This power transistor has had its cap removed so that we can look directly at the transistor chip. Let us take a closer look. Under the microscope we can see that the emitter and base regions are interdigitated. [Graphic 4A] I took a similar transistor and coated the surface of the chip with a thermographic phosphor to display its temperature distribution while it dissipates power [2]. This phosphor fluoresces when it is illuminated with near ultraviolet radiation. The intensity of the fluorescence decreases as the temperature increases. Hotter areas of the phosphor appear darker than cooler ones.

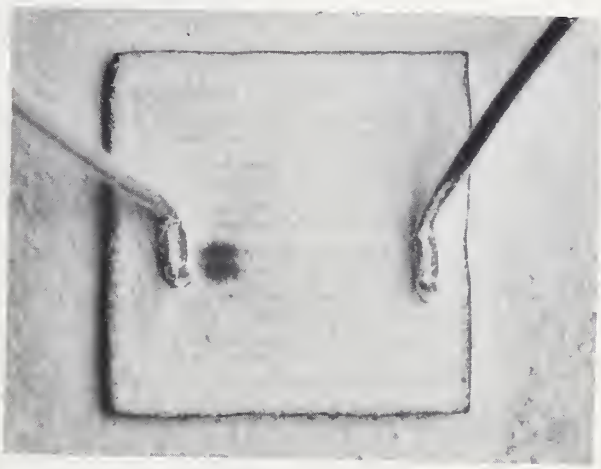
This is how the coated chip looks when illuminated with ultraviolet radiation for a high-current, low-voltage operating condition. [Graphic 4B] There is not much variation in the intensity of the fluorescence. This indicates a relatively uniform temperature across the transistor chip, and implies that the power dissipation and therefore the collector current density are also relatively uniform. Now, let us increase the collector-emitter voltage and decrease the collector current in a way that keeps the power dissipation constant. [Graphic 4C] The fluorescence is no longer uniform. In fact there is a well defined dark spot which tells us that this area is much hotter than the surrounding area. This is a stable hot spot. Nearly all of the collector current passes through this spot. So we see that severe temperature nonuniformities can and do occur in transistors. We expect to see the most severe nonuniformities for low-current, high-voltage operations.

---

[2] Brenner, D.J., A Technique for Measuring the Surface Temperature of Transistors by Means of Fluorescent Phosphors, NBS Tech. Note 591, July 1971.



Graphic 4B

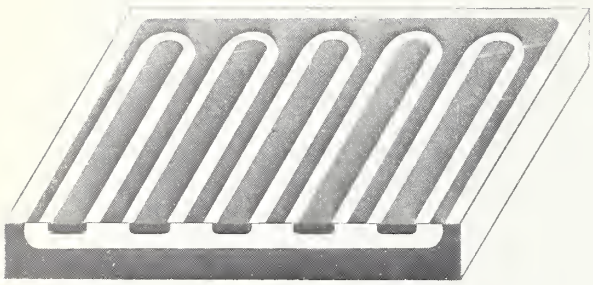


Graphic 4C

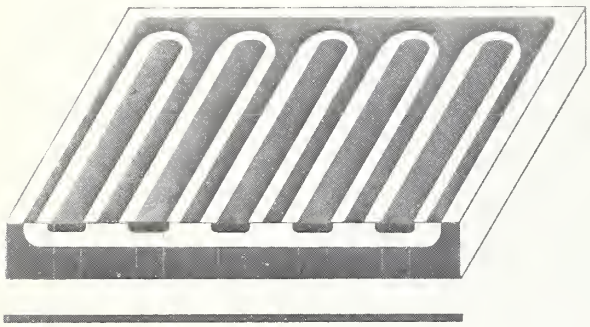
This shows that the thermal resistance of the transistor is not constant. We have not changed the power dissipation in the transistor by changing the current and voltage. Yet, the peak junction temperature in the transistor has changed dramatically. In this case it has changed by about 150°C.

Usually a thermal resistance value for the transistor is calculated from measurements made under high-current, low-voltage conditions. But if we do this, we can seriously underestimate the peak junction temperature which exists for other operating conditions.

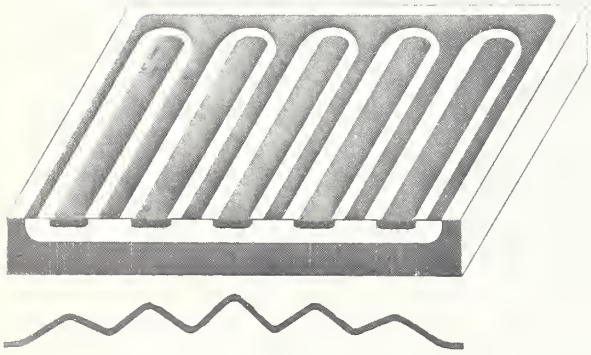
There is yet another problem. If we do have a nonuniform temperature distribution over the junction, what temperature do we measure when we use the electrical method that I have just described? Let us take a look at this problem in a little more detail using this cutaway view of a transistor, which shows the base metallization and diffusion,



Graphic 5A



Graphic 5B



Graphic 5C

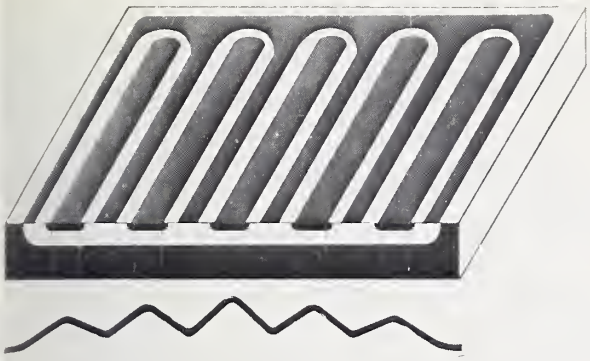
the emitter metallization and diffusion, and the collector region. [Graphic 5A]

During calibration to determine the temperature coefficient of the forward voltage, the transistor is in a uniform temperature environment. It is conducting the small measuring current, represented by these few vertical lines. [Graphic 5B] The power dissipation is extremely small so the junction temperature is essentially uniform as indicated by the horizontal line.

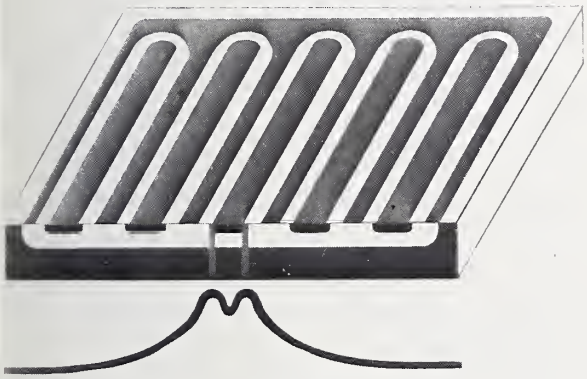
With heating power applied to the transistor, the steady-state temperature and current distribution might be represented in this way for a high-current, low-voltage operating condition. [Graphic 5C] We do not expect appreciable nonuniformities, even though there may be some small ripples in the temperature distribution; these ripples result from the effect of the emitter fingers.

To measure the forward voltage, the heating current is diverted from the device leaving only the measuring current which has assumed the uniform distribution of the heating current. [Graphic 5D] Therefore, the measuring current will have essentially the same distribution it had during calibration. Because the measurement and calibration conditions are very similar, an accurate measurement of the junction temperature can be obtained.

Consider, though the case where we try to measure the junction temperature when the heating current is constricted as we have seen for low-current, high-voltage conditions. [Graphic 5E] When we divert the heating current, the measuring current, which essentially takes the



Graphic 5E



Graphic 5D

Graphic 5F

distribution of the heating current, is very much different from the relatively uniform distribution we had during calibration. [Graphic 5F] The critical difference is that the density of the measuring current is much higher than that during calibration! We are no longer on the calibration curve we developed earlier to obtain the temperature coefficient of the forward voltage. We are on some higher one.

But we must know what the measurement current density is in the hot spot to know how to shift the calibration curve. This can be determined from the cooling response of the transistor [3]. Doing this we can obtain estimates of the peak junction temperature which are only about 10 percent below the value obtained from direct infrared measurements. But if we ignore the change in current density, we can underestimate the peak junction temperature by as much as 40 percent or even more.

So, in the real world we have to realize that the thermal resistance is not constant, the junction temperature is not a unique quantity, and significant underestimates of the peak junction temperature are possible.

I have talked about hot spots and temperature nonuniformities. What causes the current in the transistor to constrict to generate these hot spots? The answer, in brief, is thermal instability. In 1963,

---

[3] Blackburn, D.L., An Electrical Technique for the Measurement of the Peak Junction Temperature of Power Transistors. *Thirteenth Annual Proceedings, Reliability Physics 1975*, pp. 142-150, 1975.

Scarlett, Shockley, and Haitz [4] first wrote about the nature of thermal instability. In 1976 we, with Dr. Philip Hower of the Westinghouse Research Labs, were able to show that it is possible to predict quite accurately operating conditions where thermal instability will begin [5], [6], [7].

This thermal instability can lead to a runaway condition which ends in second breakdown and, generally, device failure. For some operating conditions, however, internal processes act degeneratively on the increasing current density to check this instability. If the instability is checked, a stable hot spot will be formed. Temperatures in such hot spots are typically greater than 200°C and often in excess of 300°C. The dominant process that works to stabilize the current density is the base widening effect which occurs at high current densities [5], [7]. This occurs in nearly all transistors except for single-diffused structures where no stable hot spots have been found [5].

There are several ways for measuring the onset of thermal instability. Let us look at two of them. When stable hot spots occur, the common emitter gain of the transistor decreases suddenly. We can see the development of a hot spot while we monitor the transistor gain. [Video Insert] This phosphor-coated transistor chip is illuminated with near ultraviolet light so that we can observe the temperature distribution over the surface of the chip. On the cathode ray screen we plot the collector voltage, on the horizontal axis, and the base current, on the vertical axis. We keep the collector current constant so the base current varies inversely with transistor gain. As the collector voltage is increased, the base current decreases slightly until suddenly the hot spot occurs. The voltage has to be decreased considerably before the hot spot suddenly disappears and the base current decreases abruptly. This is what we call thermal hysteresis [8]. We can cycle the applied voltage a number of times to show it is quite repeatable.

You would not ordinarily be aware that the transistor is in such a hot-spot mode unless you were specifically trying to detect it. However, the switching time, gain, and linearity of the transistor are affected by the presence of the hot spot. Both

---

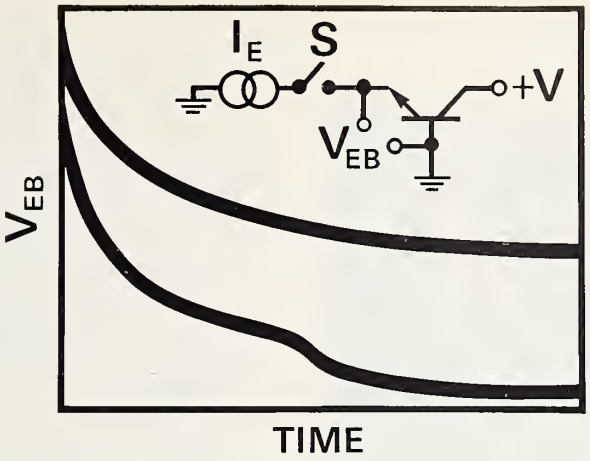
[4] Scarlett, R.M., Shockley, W., Haitz, R.H., Thermal Instabilities and Hot Spots in Junction Transistors, *Physics of Failure in Electronics*, M.E. Goldberg and J. Vaccaro, Eds., Spartan Books, Baltimore, Md, 1963, pp 194-203.

[5] Hower, P.L., Blackburn, D.L., Rubin, S., and Oettinger, F.F., Stable Hot Spots and Second Breakdown in Power Transistor, *PESC '76 Record, 1976 Power Electronics Specialists Conference*, pp 234-246.

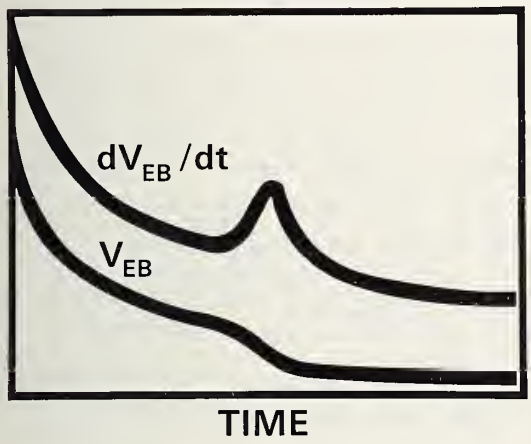
[6] Blackburn, D.L., Rubin, S., and Rogers, G.J., Measurements of Power Transistor Thermal Instabilities, Stable Hot Spots, and Second Breakdown, *IEDM Technical Digest, 1976 International Electron Device Meeting*, pp. 151-154.

[7] Hower, P.L., A Model for Stable Hot Spots in Transistors, *IEDM Technical Digest, 1976 International Electron Devices Meeting*, pp. 147-150.

[8] Oettinger F.F., and Rubin, S., The Use of Current Gain as an Indicator for the Formation of Hot Spots due to Current Crowding in Power Transistors, *Tenth Annual Proceedings, Reliability Physics 1972*, pp. 12-18.



Graphic 6



Graphic 7

switching time and gain are reduced and nonlinear amplification is increased [9] by the hot spot.

A simpler way to detect the onset of thermal instability is by measuring the emitter-base voltage, which is temperature sensitive [10], [11], [12]. If we apply a pulse of power to the transistor and monitor the emitter-base voltage as the transistor heats, the voltage decreases. [Graphic 6] A continuous concave upward curve such as this would indicate no instability. If a hot spot forms, we would see a step in the curve. This step is caused by the sudden increase in the rate of heating of the transistor caused by the thermal instability. Sometimes this step is clearly evident, but sometimes it is difficult to discern. To accent the step we can take the time derivative of the emitter-base voltage. [Graphic 7] Instead of looking for a step, we need only look for a pulse.

---

[9] Sawyer, D.E., and Berning, D.W., Mapping Nonlinearities Over the Active Region of Semiconductors Devices, *Proc IEEE*, vol. 64, pp. 1636-1637, November 1976.

[10] Oettinger, F.F., Blackburn, D.L., and Rubin, S., Thermal Characterization of Power Transistors, *IEEE Trans. Electron Devices*, vol. ED-23, pp. 831-838, August 1976.

[11] Blackburn, D.L., and Rubin, S., A Nondestructive Method for the Determination of Forward-Biased Safe-Operating-Area Limits for Power Transistors, *PESC '77 Record, 1977 Power Electronics Specialists Conference*, (to be published).

[12] Rubin, S., and Blackburn, D.L., A Test Unit for the Nondestructive Determination of Forward-Biased Safe-Operating-Area Limits of Power Transistors, *Proceedings of 1977 Industrial Applications Society Annual Meeting*, (to be published).

Excerpt From Video Insert

In the laboratory, [Video Insert] an oscilloscope is used to monitor the derivative of the emitter-base voltage. We keep the emitter current constant and progressively increase the collector voltage with each successive power application. At first we see no pulse. Then when the voltage is great enough for thermal instability to occur, a pulse appears. As the voltage increases, the pulse moves to the left. The thermal instability occurs sooner after the application of power for greater values of applied voltage.

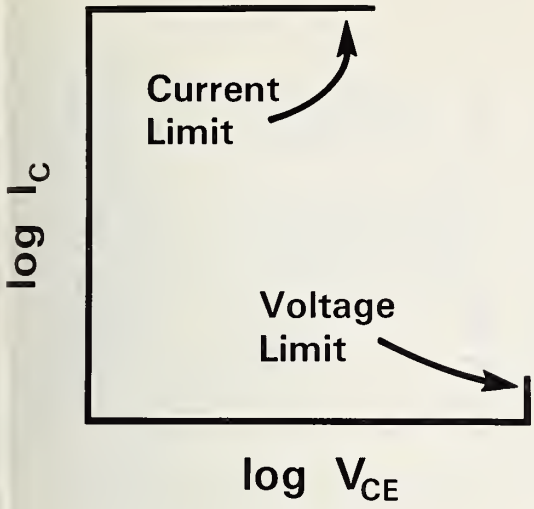
We can also connect a protective turn-off circuit which is activated when the pulse begins. It senses the leading edge of the pulse and turns off the transistor before it can enter into a fully developed hot-spot mode and reach any significant temperature extremes.

I have talked about thermal instability being stabilized by internal processes. For many operating conditions these processes are not capable of checking the instability. For these conditions, second breakdown occurs. Very high localized currents and temperatures are present when the transistor goes into second breakdown. Usually the transistor is either degraded or destroyed.

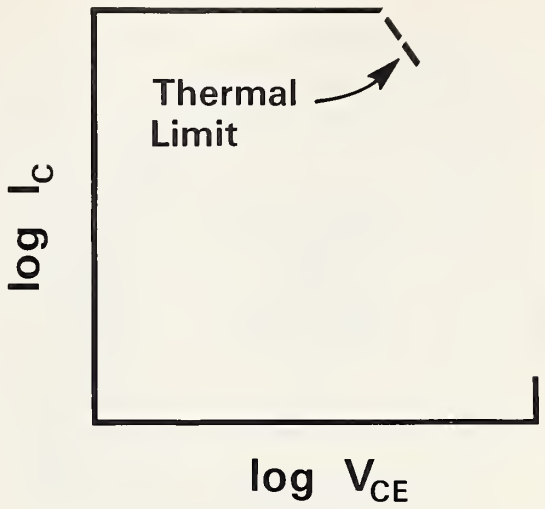
Here is an extreme case of what second breakdown can do to a transistor. [Video Insert] The current and temperature at the outer edges of these two emitter fingers became so great during second breakdown that two holes were formed extending completely through the die to form a collector-to-emitter short circuit. [Excerpt From Video Insert] This is a common failure mode of second breakdown.

The possibility of destruction through second breakdown is a primary reason for the use of safe operating area limits in transistor data and specification sheets. But these safe operating area limits are dictated not only by the limits imposed by second breakdown; they are also determined by the limits imposed by the thermal resistance as well as the maximum current and voltage limits.

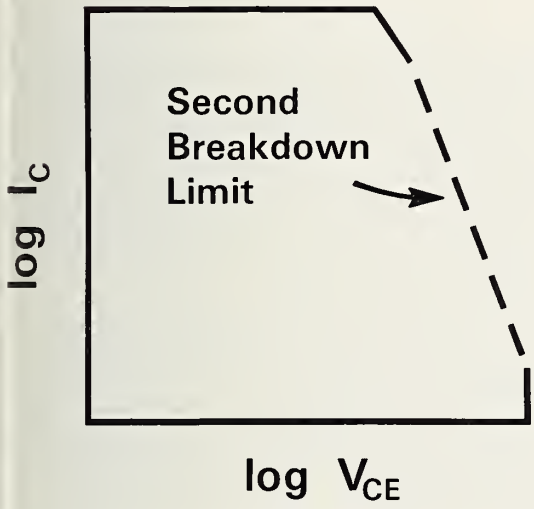
The maximum safe operating area limits for transistors are usually plotted as the log of the collector current against the log of the collector-emitter voltage.



Graphic 8A



Graphic 8B

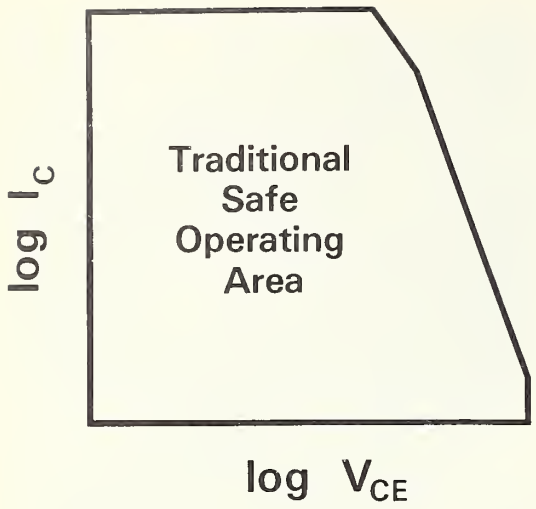


Graphic 8C

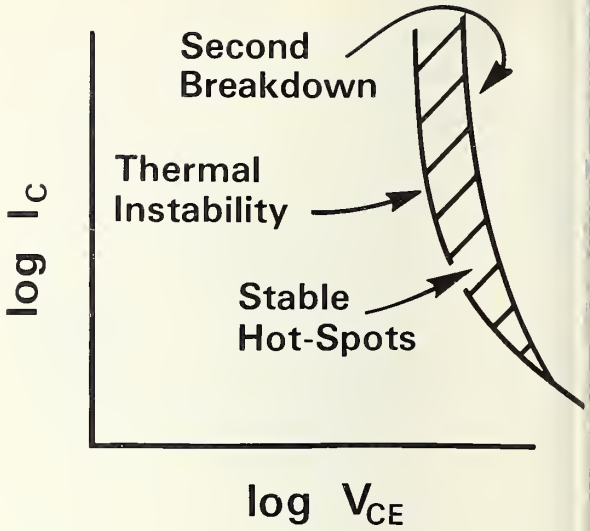
[Graphic 8A] The maximum current is determined by such considerations as the size of the chip and interconnecting wires, the metallization, and the minimum allowable transistor gain. The maximum voltage is set by the breakdown characteristics of the collector-base junction. The establishment of these two limits is generally straightforward.

Continuing to fill in the gap between these two limits, we have the thermal limit. [Graphic 8B] In this region, the temperature distribution over the device is still relatively uniform so that the thermal resistance for the transistor can be used. For a maximum safe junction temperature, set by the manufacturer, a maximum allowed power can be calculated using the thermal resistance of the transistor. This power is constant and translates as a line with a slope of minus one.

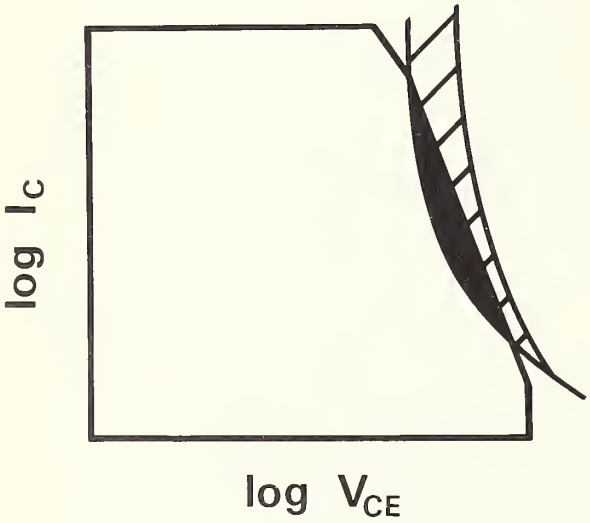
The maximum safe operating area limit specification is completed with the second-breakdown limit. [Graphic 8C] The traditional way of determining the second-breakdown limit for a transistor type is to submit many devices to a destructive second breakdown test. They are operated in successively more stressful conditions until second breakdown occurs. The voltage and current are noted. By doing this for enough transistors over the voltage-current area of interest, a line can be drawn which is safely below all of the points at which second breakdown would be expected to occur.



Graphic 8D



Graphic 8E

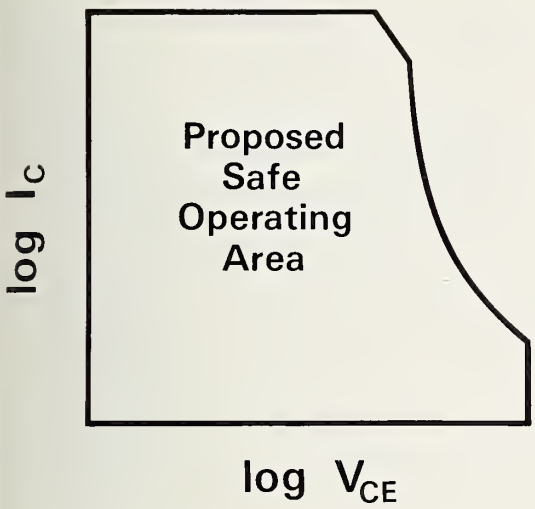


Graphic 8F

This then completes the traditional maximum safe operating area limits that are usually specified. [Graphic 8D] They do not take into consideration the existence of hot spots. Yet hot spots may actually appear within these limits, usually in this region.

Let us take a closer look at the region where hot spots do occur. In our work with Dr. Hower, we found that very specific relationships exist between thermal instability, stable hot spots, and second breakdown [5]. [Graphic 8E] Thermal instability always precedes second breakdown. Stable hot spots exist in this region. Slightly to the left of the thermal instability limit, the junction temperature is relatively uniform and may be only $30^{\circ}C$ to $40^{\circ}C$ above the case temperature. A fraction of a volt to the right, the transistor is in a hot-spot mode. The temperature is nonuniform with the peak temperature often above the maximum allowed junction temperature for the transistor. If while in the hot-spot mode the voltage is increased sufficiently, the transistor will go into second breakdown. At lower currents and higher voltages, hot spots may not be stable and thermal instability will continue directly into second breakdown.

Superimposing this relationship on the traditional safe operating area [Graphic 8F]



Graphic 8G

we can see that hot spots can appear within the maximum safe operating area limits as they are presently specified. Therefore we propose that the safe operating area for transistors be revised to include protection against operation in the hot-spot mode. [Graphic 8G] Within this revised safe operating area, we can be assured that the transistor will be operated so that the junction temperature will be relatively uniform and below its maximum rated junction temperature.

While hot spots may not be immediately destructive, the very high localized temperatures can be expected to be degrading to the transistor with time. In this vein, recent work by Gaur and others [13] at IBM has shown crystal damage in transistors operating repeatedly under hot-spot-like conditions. Furthermore, the hot spots degrade gain and switching speed, and introduce nonlinear amplification. Therefore, the revised safe operating area represents a realistic limit for achieving the maximum reliability, performance, and life of transistors for operation under forward base drive conditions.

The limits of this area for a given device type can be determined nondestructively — without sacrificing any transistors. This can be done by using the method I described involving the derivative of the emitter-base voltage to detect the onset of thermal instability. The derivative pulse can trigger a circuit to turn off the transistor under test before it is damaged by high, localized temperatures. This method is easily implemented not only by the device manufacturer who generates and verifies the safe operating area specifications of his product but also by the device user as a check of the products he buys.

Our discussion has centered around DC operation. For pulsed operation these limits move out and shift somewhat relative to each other. Depending on operating points, thermal instability and second breakdown can be initiated in times that range from milliseconds to microseconds. But the concepts developed for establishing these limits can also be applied in the case of pulsed operation.

---

[13] Gaur, S.P., Lowe, G., and Thorpe, W., Power Transistor Crystal Damage in Inductive Load Switching: A Reliability Concern, *Fifteenth Annual Proceedings, Reliability Physics 1977*, (to be published).

Let me briefly review the points I made about the thermal characterization of power transistors.

First, the concept of thermal resistance cannot be used indiscriminately to define the maximum power the transistor can dissipate. To do so may grossly overestimate the power capability of the transistor.

Second, accurate measurement of the junction temperature is not straightforward. Temperature nonuniformities that can occur will result in serious underestimates of the actual peak junction temperature, if current density differences are not taken into account.

Third, the traditional way of developing safe operating areas of transistors may allow potentially dangerous hot spots to occur within the safe operating areas.

Finally, a method is now available which can be used to develop a revised safe operating area which avoids conditions where hot spots can occur.

CREDITS

Presented by: The National Bureau of Standards

Graphics: Eugene P. Ralston and Raymond W. Gates

Producer: Susan Lieberman

Executive Producer: Harry A. Schafft

Videotaped by: Video Electronics Branch
Division of Administrative Services,
Energy Research and Development Administration

Teleprompter script typed by E. Jane Walters

Camera copy of script typed by Valerie Claggett

NBS-114A (REV. 7-73)

U.S. DEPT. OF COMM. BIBLIOGRAPHIC DATA SHEET	1. PUBLICATION OR REPORT NO. NBS Spec. Publ. 400-44	2. Gov't Accession No.	3. Recipient's Accession No.

4. TITLE AND SUBTITLE

Semiconductor Measurement Technology: Safe Operating Area Limits for Power Transistors: Videotape Script

5. Publication Date: September 1977

6. Performing Organization Code

7. AUTHOR(S)

David L. Blackburn

8. Performing Organ. Report No.

9. PERFORMING ORGANIZATION NAME AND ADDRESS

NATIONAL BUREAU OF STANDARDS
DEPARTMENT OF COMMERCE
WASHINGTON, D.C. 20234

10. Project/Task/Work Unit No.

11. Contract/Grant No.

12. Sponsoring Organization Name and Complete Address *(Street, City, State, ZIP)*

Same as 9.

13. Type of Report & Period Covered

14. Sponsoring Agency Code

15. SUPPLEMENTARY NOTES

Library of Congress Catalog Card Number: 77-608172

16. ABSTRACT *(A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.)*

This is a script of a videotape presentation which addresses deficiencies of present methods for measuring and specifying the power dissipation capabilities and safe operating area (SOA) limits for power transistors. These deficiencies result from not including adequately the effects of significant temperature nonuniformities which occur, primarily for high-voltage, low-current conditions. Firstly, the specified thermal resistance of a transistor can be applied strictly only when the junction temperature is relatively uniform, otherwise the power capability of the device can be grossly overestimated. Secondly, the use of the standard method for measuring junction temperature can lead to a serious underestimate of the peak junction temperature if the temperature distribution is not uniform. Finally, the traditional SOA limits do not consider the phenomenon of thermal instability and the hot spots that ensue. As a result, devices can operate with potentially dangerous hot spots within operating limits that traditionally have been considered to be safe. It is proposed that the SOA limits be revised to exclude operating conditions where thermal instability and hot spots can occur. A method for detecting the onset of thermal instability and triggering a circuit to turn-off the transistor under test is described. This approach can be used to develop the revised SOA limits in a nondestructive way.

17. KEY WORDS *(six to twelve entries; alphabetical order; capitalize only the first letter of the first key word unless a proper name; separated by semicolons)*

Hot spots; junction temperature; measurement technology; nondestructive test; reliability; safe operating limits; second breakdown; semiconductor devices; thermal characterization; thermal instability; thermal resistance; transistors.

18. AVAILABILITY

[X] Unlimited

[ ] For Official Distribution. Do Not Release to NTIS

[X] Order From Sup. of Doc., U.S. Government Printing Office Washington, D.C. 20402, SD Cat. No. C13.10:400-44

[ ] Order From National Technical Information Service (NTIS) Springfield, Virginia 22151

19. SECURITY CLASS (THIS REPORT): UNCLASSIFIED

21. NO. OF PAGES: 20

20. SECURITY CLASS (THIS PAGE): UNCLASSIFIED

22. Price

NBS TECHNICAL PUBLICATIONS

PERIODICALS

JOURNAL OF RESEARCH reports National Bureau of Standards research and development in physics, mathematics, and chemistry. It is published in two sections, available separately:

• Physics and Chemistry (Section A)
Papers of interest primarily to scientists working in these fields. This section covers a broad range of physical and chemical research, with major emphasis on standards of physical measurement, fundamental constants, and properties of matter. Issued six times a year. Annual subscription: Domestic, $17.00; Foreign, $21.25.

• Mathematical Sciences (Section B)
Studies and compilations designed mainly for the mathematician and theoretical physicist. Topics in mathematical statistics, theory of experiment design, numerical analysis, theoretical physics and chemistry, logical design and programming of computers and computer systems. Short numerical tables. Issued quarterly. Annual subscription: Domestic, $9.00; Foreign, $11.25.

DIMENSIONS/NBS (formerly Technical News Bulletin)—This monthly magazine is published to inform scientists, engineers, businessmen, industry, teachers, students, and consumers of the latest advances in science and technology, with primary emphasis on the work at NBS. The magazine highlights and reviews such issues as energy research, fire protection, building technology, metric conversion, pollution abatement, health and safety, and consumer product performance. In addition, it reports the results of Bureau programs in measurement standards and techniques, properties of matter and materials, engineering standards and services, instrumentation, and automatic data processing.

Annual subscription: Domestic, $12.50; Foreign, $15.65.

NONPERIODICALS

Monographs—Major contributions to the technical literature on various subjects related to the Bureau's scientific and technical activities.

Handbooks—Recommended codes of engineering and industrial practice (including safety codes) developed in cooperation with interested industries, professional organizations, and regulatory bodies.

Special Publications—Include proceedings of conferences sponsored by NBS, NBS annual reports, and other special publications appropriate to this grouping such as wall charts, pocket cards, and bibliographies.

Applied Mathematics Series—Mathematical tables, manuals, and studies of special interest to physicists, engineers, chemists, biologists, mathematicians, computer programmers, and others engaged in scientific and technical work.

National Standard Reference Data Series—Provides quantitative data on the physical and chemical properties of materials, compiled from the world's literature and critically evaluated. Developed under a world-wide program coordinated by NBS. Program under authority of National Standard Data Act (Public Law 90-396).

NOTE: At present the principal publication outlet for these data is the Journal of Physical and Chemical Reference Data (JPCRD) published quarterly for NBS by the American Chemical Society (ACS) and the American Institute of Physics (AIP). Subscriptions, reprints, and supplements available from ACS, 1155 Sixteenth St. N.W., Wash. D. C. 20056.

Building Science Series—Disseminates technical information developed at the Bureau on building materials, components, systems, and whole structures. The series presents research results, test methods, and performance criteria related to the structural and environmental functions and the durability and safety characteristics of building elements and systems.

Technical Notes—Studies or reports which are complete in themselves but restrictive in their treatment of a subject. Analogous to monographs but not so comprehensive in scope or definitive in treatment of the subject area. Often serve as a vehicle for final reports of work performed at NBS under the sponsorship of other government agencies.

Voluntary Product Standards—Developed under procedures published by the Department of Commerce in Part 10, Title 15, of the Code of Federal Regulations. The purpose of the standards is to establish nationally recognized requirements for products, and to provide all concerned interests with a basis for common understanding of the characteristics of the products. NBS administers this program as a supplement to the activities of the private sector standardizing organizations.

Consumer Information Series—Practical information, based on NBS research and experience, covering areas of interest to the consumer. Easily understandable language and illustrations provide useful background knowledge for shopping in today's technological marketplace.

Order **above** *NBS publications from: Superintendent of Documents, Government Printing Office, Washington, D.C. 20402.*

Order **following** *NBS publications—NBSIR's and FIPS from the National Technical Information Services, Springfield, Va. 22161.*

Federal Information Processing Standards Publications (FIPS PUBS)—Publications in this series collectively constitute the Federal Information Processing Standards Register. Register serves as the official source of information in the Federal Government regarding standards issued by NBS pursuant to the Federal Property and Administrative Services Act of 1949 as amended, Public Law 89-306 (79 Stat. 1127), and as implemented by Executive Order 11717 (38 FR 12315, dated May 11, 1973) and Part 6 of Title 15 CFR (Code of Federal Regulations).

NBS Interagency Reports (NBSIR)—A special series of interim or final reports on work performed by NBS for outside sponsors (both government and non-government). In general, initial distribution is handled by the sponsor; public distribution is by the National Technical Information Services (Springfield, Va. 22161) in paper copy or microfiche form.

BIBLIOGRAPHIC SUBSCRIPTION SERVICES

The following current-awareness and literature-survey bibliographies are issued periodically by the Bureau:

Cryogenic Data Center Current Awareness Service. A literature survey issued biweekly. Annual subscription: Domestic, $25.00; Foreign, $30.00.

Liquified Natural Gas. A literature survey issued quarterly. Annual subscription: $20.00.

Superconducting Devices and Materials. A literature survey issued quarterly. Annual subscription: $30.00. Send subscription orders and remittances for the preceding bibliographic services to National Bureau of Standards, Cryogenic Data Center (275.02) Boulder, Colorado 80302.

U.S. DEPARTMENT OF COMMERCE
National Bureau of Standards
Washington, D.C. 20234

OFFICIAL BUSINESS

Penalty for Private Use, $300

POSTAGE AND FEES PAID
U.S. DEPARTMENT OF COMMERCE
COM-215

SPECIAL FOURTH-CLASS RATE
BOOK