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U.S. DEPARTMENT OF COMMERCE / National Bureau of Standards

Semiconductor Measurement Technology:

**A Versatile
High-Voltage Bias Supply for
Extended Range MIS
C(V) and G(V) Measurements**

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PREFACE

This study was carried out at the RCA Laboratories as a part of the Semiconductor Technology Program in the Electronic Technology Division at the National Bureau of Standards. The Semiconductor Technology Program serves to focus NBS efforts to enhance the performance, interchangeability, and reliability of discrete semiconductor devices and integrated circuits through improvements in measurement technology for use in specifying materials and devices in national and international commerce and for use by industry in controlling device fabrication processes. The work was supported by the Defense Advanced Research Projects Agency* through the National Bureau of Standards' Semiconductor Technology Program, Contract 5-35912. The contract was monitored by R. L. Raybold as the Contracting Officer's Technical Representative (COTR) and R. Y. Koyama as Assistant COTR.

DISCLAIMER

Certain commercial equipment, instruments, or materials are identified in this report in order to adequately specify the experimental procedure. In no case does such identification imply recommendation or endorsement by the National Bureau of Standards, nor does it imply that the material or equipment identified is necessarily the best available for the purpose.

Larger scale drawings of the mechanical parts and full-scale negatives of the custom circuit boards are available on request from the COTR, Tech-A-361, National Bureau of Standards, Washington, DC 20234.

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SEMICONDUCTOR MEASUREMENT TECHNOLOGY: A Versatile High-Voltage Bias Supply for Extended Range MIS C(V) and G(V) Measurements

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Abstract: Recently developed technology has enabled the measurement of MIS C(V) and G(V)* at bias-voltage magnitudes as large as 25 kV. This report describes a versatile high-voltage power supply intended for use as a bias source in carrying out such measurements.

The design allows the user a wide variety of options in the selection of the sweep function (waveform), sweep time, initial bias voltage, and the amplitude of the bias sweep. There are six possible sweep functions: (i) increasing ramp, (ii) decreasing ramp, (iii) positive polarity half-wave sawtooth (increasing ramp followed by decreasing ramp), (iv) negative polarity half-wave sawtooth (decreasing ramp followed by increasing ramp), (v) full-wave sawtooth starting with increasing ramp, and (vi) full-wave sawtooth starting with decreasing ramp. Either single or repetitive sweeps may be selected. The sweep time from the initial value to the end of the first ramp segment may be varied from 1 to 2000 s. Operator convenience is enhanced by certain features of the design; among these are light-emitting diodes which display the state of the sweep and automatic pen control if the sweep is used with an x-y recorder.

Key Words: High-voltage bias supply; high-voltage C(V) and G(V) measurements; high-voltage function generator; high-voltage sweep; semiconductor devices; silicon-on-sapphire measurements.

1. INTRODUCTION

A recently developed modification of the MIS C(V) measurement technique [1] has extended its useful range, allowing it to be used for the measurement of samples with insulating layers more than two orders of magnitude greater in thickness than was previously possible. This use, however, often requires the application of a very large bias voltage to the capacitor sample being measured. In the first high-voltage MIS C(V) measurements of Al-sapphire-Si capacitors [2], the bias voltage was controlled manually and an attempt was made to keep the rate of change of bias as uniform as possible. It was clear, however, that the measured capacitance, C, depended to some extent upon the rate of change of the bias voltage, V, and that manual control of

*The following abbreviations are used: MIS for metal-insulator-semiconductor; C(V) for capacitance as a function of voltage; G(V) for conductance as a function of voltage.

the bias voltage would be unsatisfactory for general use. Since the extended-range modification of the measurement technique was relatively new, and there existed very little experience on which to base a set of requirements for a suitable bias supply, we decided to design and construct an extremely versatile supply that would lend itself to a variety of possible future applications. The bias supply which resulted from that work is described in this report. It was intended for use with other equipment developed concurrently and described in references 3-5.

2. GENERAL DESCRIPTION OF EQUIPMENT, OPERATION, AND PERFORMANCE

The high-voltage bias supply is constructed in the form of two modules: (1) a control module with digital logic, a D/A (digital to analog) converter, and amplifiers to provide the required waveforms at low- and medium-voltage levels, and (2) a high-voltage amplifier module (HVAM).

2.1 Control Module

The control module is designed to allow the user a wide variety of options in the selection of the (1) sweep function (waveform), (2) sweep time, (3) initial bias voltage, and (4) amplitude of the bias sweep. The front panel of the control module (illustrated in fig. 1) shows the location of all of the user-operated controls.

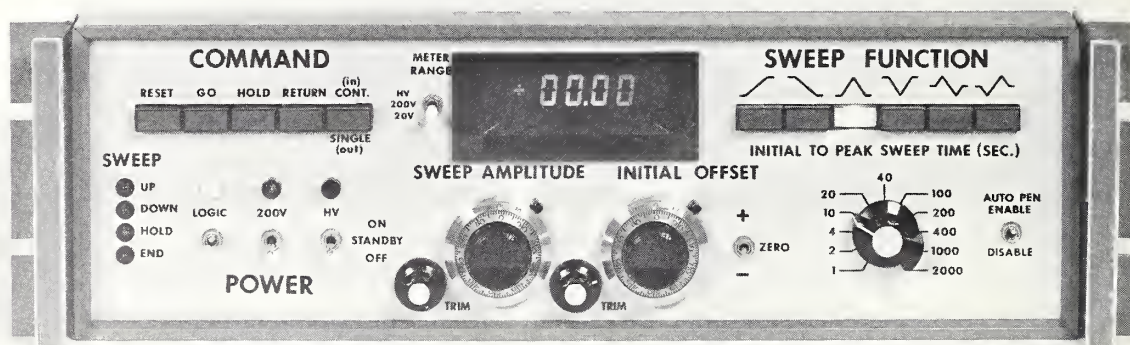


Figure 1. Control module front panel.

Operating power for the digital logic and low-voltage analog circuitry is controlled by the switch marked LOGIC* located above the POWER label. The function of the two adjacent switches will be discussed later.

Any one of six basic sweep functions may be selected by depressing (to its latched position) the appropriate pushbutton under the heading SWEEP FUNCTION. Each sweep function is composed of one or more "ramp" segments. The term ramp is understood here to mean a voltage which varies linearly with time.

The time, T , required for the sweep is controlled by selection of the INITIAL TO PEAK SWEEP TIME; i.e., the time required for the sweep voltage to change from its initial value to the first maximum excursion from that initial value.

If a single sweep is desired the CONT.-SINGLE pushbutton under the COMMAND heading should be in the released (out) position. If continuous operation is desired, this pushbutton should be in the depressed (in) position.

The magnitude of the starting value of the sweep is set by adjusting the INITIAL OFFSET control and the adjacent TRIM control. The polarity of the initial offset voltage is selected by setting the adjacent three-position toggle switch to the appropriate + or - position or to ZERO if no initial offset is desired.

The maximum one-way excursion of the sweep voltage from its initial value is set by adjusting the SWEEP AMPLITUDE control and the adjacent TRIM control.

Before initiating a sweep, the digital control circuits must be reset by momentarily depressing the RESET pushbutton. The sweep may then be initiated by depressing the GO pushbutton. The resulting sweep voltage as a function of time will be one of the waveforms shown in figure 2. If the sweep has been started in the continuous operation mode, the sweep will continue indefinitely until it is ended in one of two ways: (1) the continuous sweep may be ended by depressing the RESET pushbutton; this will bring the sweep voltage back to its initial value almost instantaneously, i.e., at slewing speed. (2) Alternatively, the continuous sweep may be ended by releasing the CONT.-SINGLE pushbutton to its out position. This causes a reversion to single sweep operation, which ends with the completion of the sweep function then in progress.

The sweep may be stopped at any time by pressing the pushbutton marked HOLD. The output voltage will then remain constant until the GO, RETURN or RESET pushbutton is pressed. If the GO pushbutton is pressed,

*Words corresponding to labels, callouts, or titles in the figures are capitalized in the text.

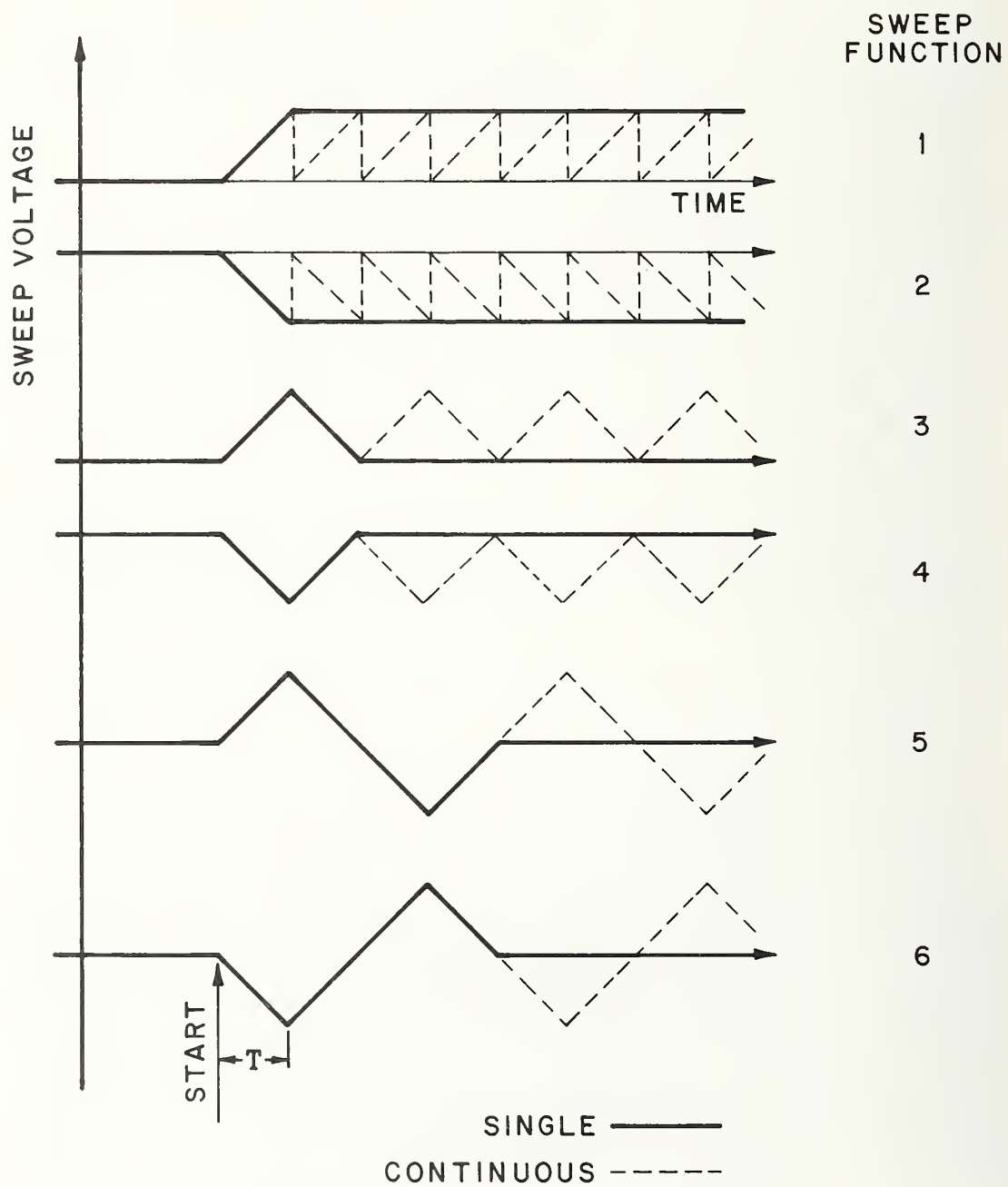


Figure 2. Sweep function waveforms.

the sweep will continue from the point at which it had been stopped. If the RETURN pushbutton is pressed the sweep voltage will return to the initial value by the shortest possible path (single ramp) at a sweep rate corresponding to the selected SWEEP AMPLITUDE and INITIAL TO PEAK SWEEP TIME. If the RESET pushbutton is pressed, the sweep voltage will return to its initial value almost instantaneously, i.e., at slewing speed.

The operating state of the sweep is indicated by four monitor lights (light-emitting diodes) located under the label SWEEP. The UP or DOWN light will be on if the sweep is on an up or down ramp, respectively. The HOLD light indicates that the sweep has been stopped by pressing the HOLD pushbutton. The END light indicates completion of a sweep. The absence of any light indicates that the RESET pushbutton has been pressed.

The sweep waveforms generated in the control module are available from connectors on the rear panel (see fig. 3) at three different voltage levels. The nominal low voltage output of the control module has a maximum magnitude of about 10 V with respect to ground. The output is "antisymmetric" with respect to ground. That is, the voltages which appear at the two output terminals (BNC connectors labeled +10 V and -10 V) have equal magnitudes but are of opposite polarity with respect to ground. Thus, when one terminal is at +10 V, the other is at -10 V and the total output magnitude is 20 V. The voltage at each output terminal is also bipolar; i.e., it can have

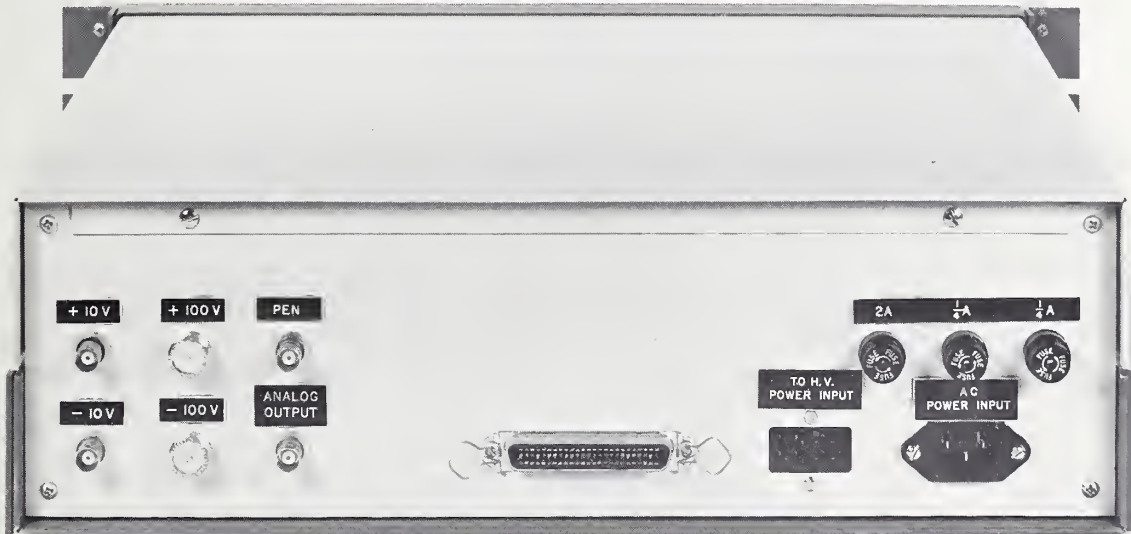


Figure 3. Control module rear panel.

either polarity with respect to ground. When the +10 V terminal is positive with respect to ground, the output polarity is said to be positive or normal; if the +10 V terminal is negative with respect to ground, the output polarity is said to be negative or reversed. This total voltage is indicated on the digital voltmeter when the METER RANGE switch is in the 20-V position.

There are two additional outputs available from the control module.

(1) A single-ended output proportional to the previously described bipolar output, but equal to one-half of its magnitude. This voltage appears at a single BNC connector labeled ANALOG OUTPUT and is intended for use with grounded instruments to monitor the bipolar output. (2) A medium level bipolar output equal to ten times the low-voltage bipolar output. This voltage appears at two terminals (UHF connectors) labeled +100 V and -100 V. The total voltage between these terminals is indicated on the digital voltmeter when the METER RANGE switch is in the 200-V position. Operating power for this medium level analog circuitry is controlled by the switch marked 200 V located above the POWER label.

A BNC connector (labeled PEN) located on the rear panel provides a connection to the contacts of a pen-control relay. When the AUTO PEN switch on the front panel is in the ENABLE position, the pen relay is energized during sweep operation; this provides a closed circuit at the PEN connector. If the AUTO PEN switch is in the DISABLE position the relay cannot be energized and the PEN control circuit remains open.

The operating power for the digital logic and all levels of analog circuitry is provided through the connector labeled AC POWER INPUT.

The operating power for the high-voltage amplifier module is provided through the connector labeled TO HV POWER INPUT and is controlled by the switch marked HV located above the POWER label. This connector also provides a circuit connection between the control and high-voltage modules that may be used for monitoring the voltage level (attenuated 1000:1) at the output of the HV amplifier module. This voltage may be read on the digital voltmeter of the control module when the METER RANGE switch is in the HV position.

There is an unlabeled connector in the rear panel of the control module. It was originally intended for interfacing digital logic signals in the control module with a data acquisition system for extended-range MIS C(V) measurements. This system has not yet been developed and the connector is, at present, unused.

2.2 High-Voltage Amplifier Module

The high-voltage amplifier module (HVAM) is designed to accept the nominal low-voltage bipolar output of the control module at its input, and to produce a high-voltage bipolar output at levels up to ~ 25 kV (~ 12.5 kV between each output terminal and ground). The front and

rear panels are shown in figures 4 and 5, respectively. The input terminals are located on the rear panel and labeled +10 V DRIVE and -10 V DRIVE. The output terminals are located on the front panel and are labeled + and -.

The gain of the HVAM is controlled by a switch located on the front panel and labeled HIGH VOLTAGE RANGE (kV). There are five positions of this switch, +1, +2.5, +5, +10, +25 each indicating the nominal maximum output voltage magnitude in kilovolts corresponding to that switch position with the maximum nominal input voltage. The corresponding amplifier gain figures are 50, 125, 250, 500, and 1250.

Operating power is supplied through a connector labeled POWER INPUT and located on the rear panel. The operating power is controlled by the switch on the control module labeled HV. This switch has three positions. The OFF position indicates that all power to the HVAM is shut off. The STANDBY position indicates that power is connected to all of the low-voltage control circuitry, the regulator tube heaters, and a time-delay relay, but not to the plate supplies for the regulator tubes. The regulator tube plate supplies are powered only when the time-delay (~ 8 s) relay has closed. High voltage can reach the output terminals only if the time-delay relay has closed, the HV switch is in the ON position, and the safety interlock circuit [4] is complete. The latter occurs when a low resistance is connected across the insulated BNC connector marked SAFETY INTERLOCK.

Three pilot lights on the front panel of the HVAM and one on the front panel of the control module monitor the status of operating power for the HVAM. When the HV switch is in the OFF position, all pilot lights should be off. When the HV switch is in the STANDBY position, the pilot light above the HV switch and the one marked CONTROL POWER should be on. The pilot light marked STANDBY will be on only after the time-delay relay has closed. When the HV switch is in the ON position, the OUTPUT pilot light on the HVAM will be on if the safety interlock circuit is complete. Note that it is possible for the OUTPUT light to be on when the STANDBY light is off during the ~ 8 s waiting period of the time-delay relay; there will be no voltage at the output terminals during this time.

3. CIRCUIT DETAILS OF CONTROL MODULE

A functional block diagram of both modules of the high-voltage bias supply is shown in figure 6. This section deals with the circuits comprising the control module portion of that figure. These circuits are described in five schematic diagrams, one for each of the blocks in the digital portion (figs. 7 to 10) and a fifth (fig. 11) for the three blocks representing the analog portion. The circuit elements shown in these figures are described in table 1.

In brief, a crystal-oscillator-derived square wave (clock) is fed to an up/down counter producing a binary number which varies linearly

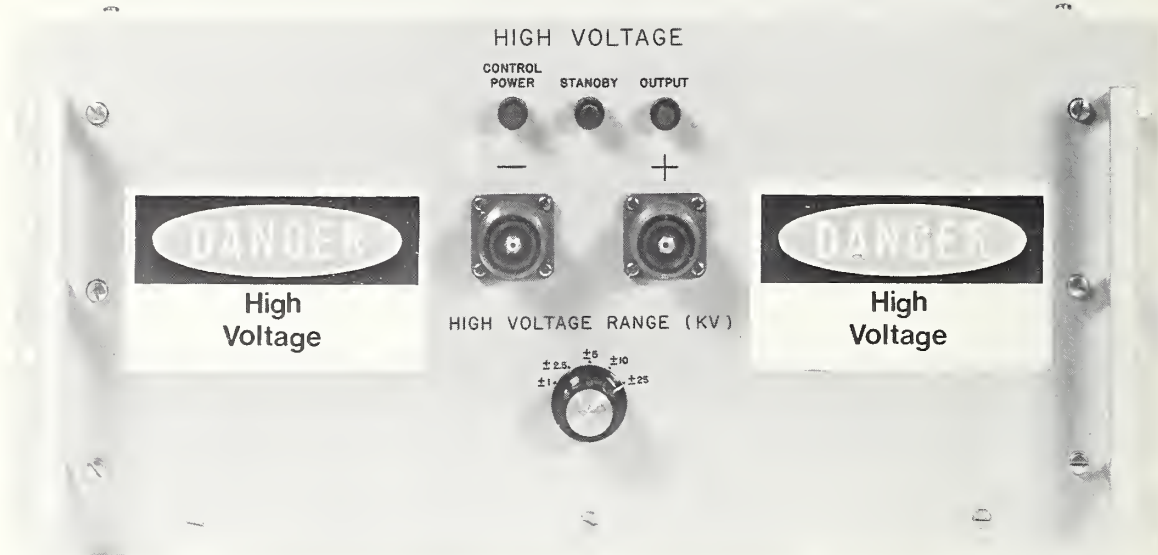


Figure 4. High-voltage amplifier module front panel.



Figure 5. High-voltage amplifier module rear panel.

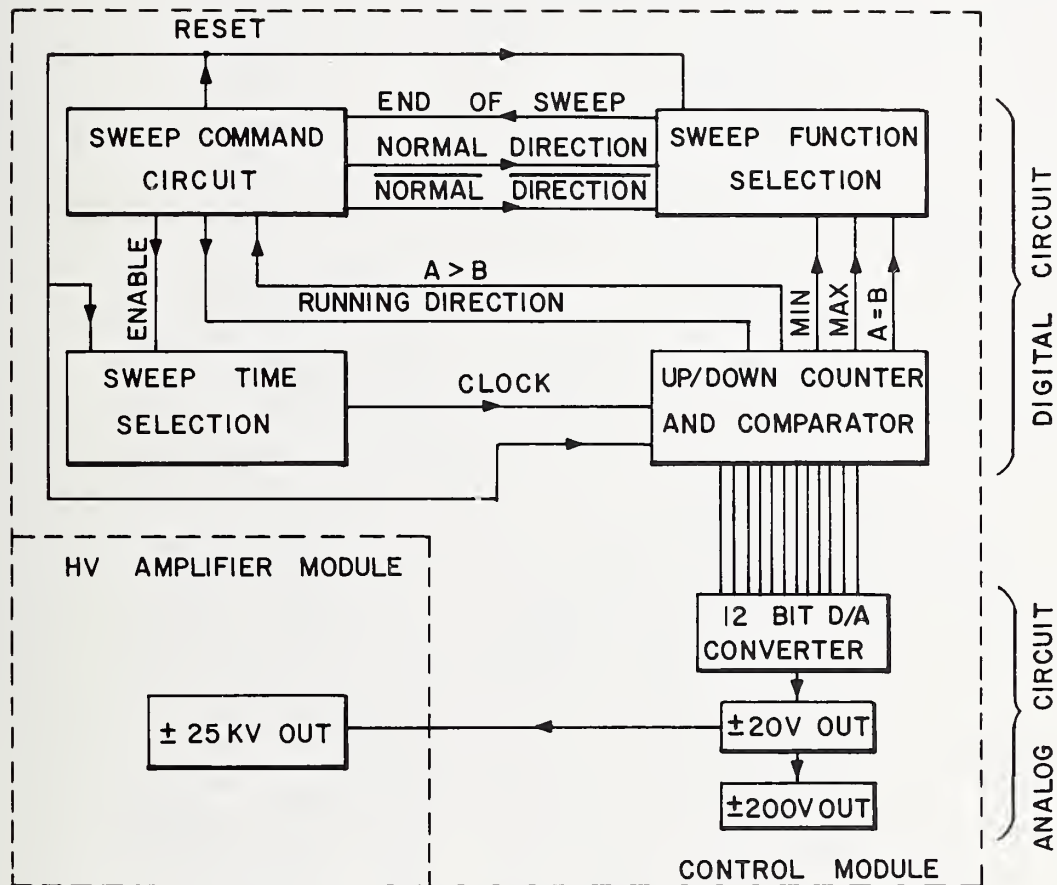


Figure 6. Functional block diagram of high-voltage bias supply.

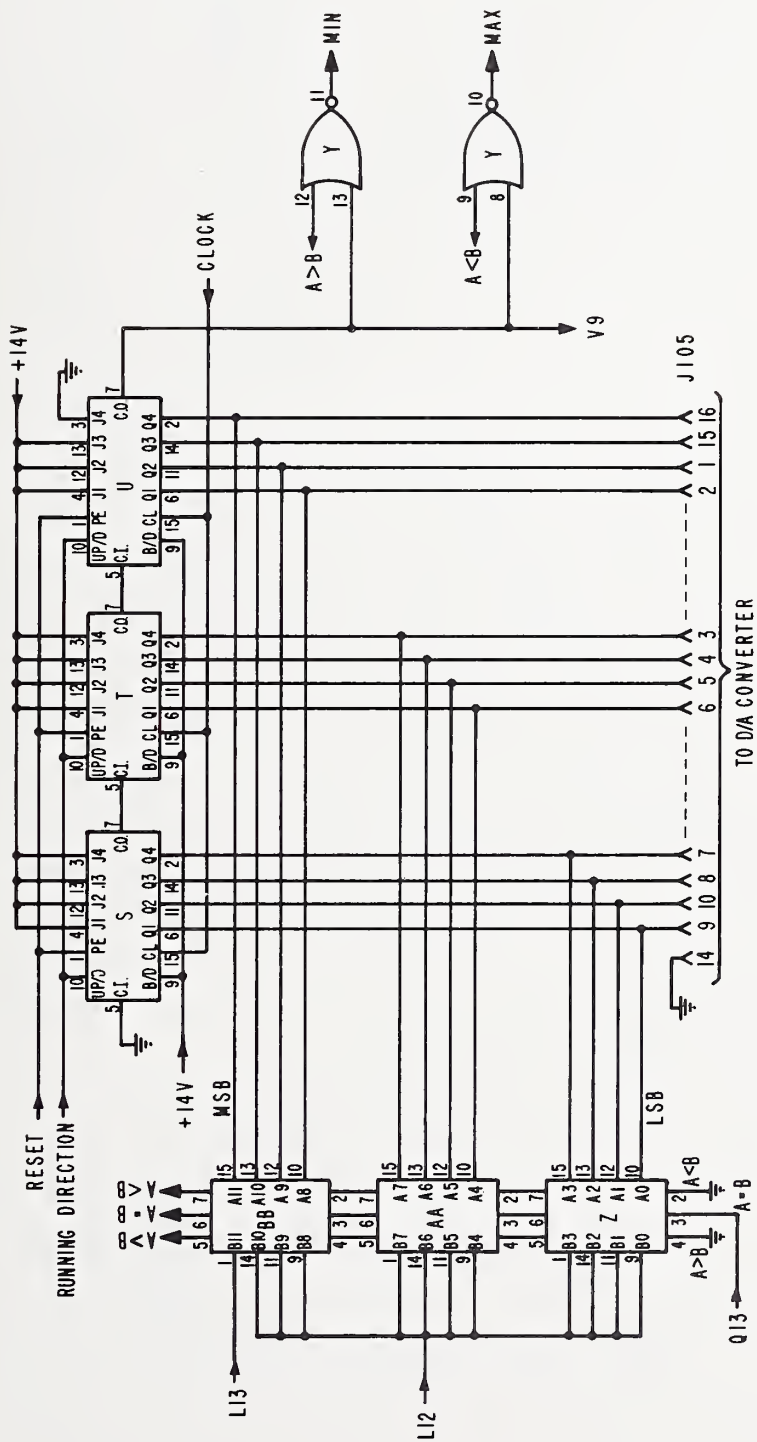


Figure 8. Up/down counter and comparator circuit.

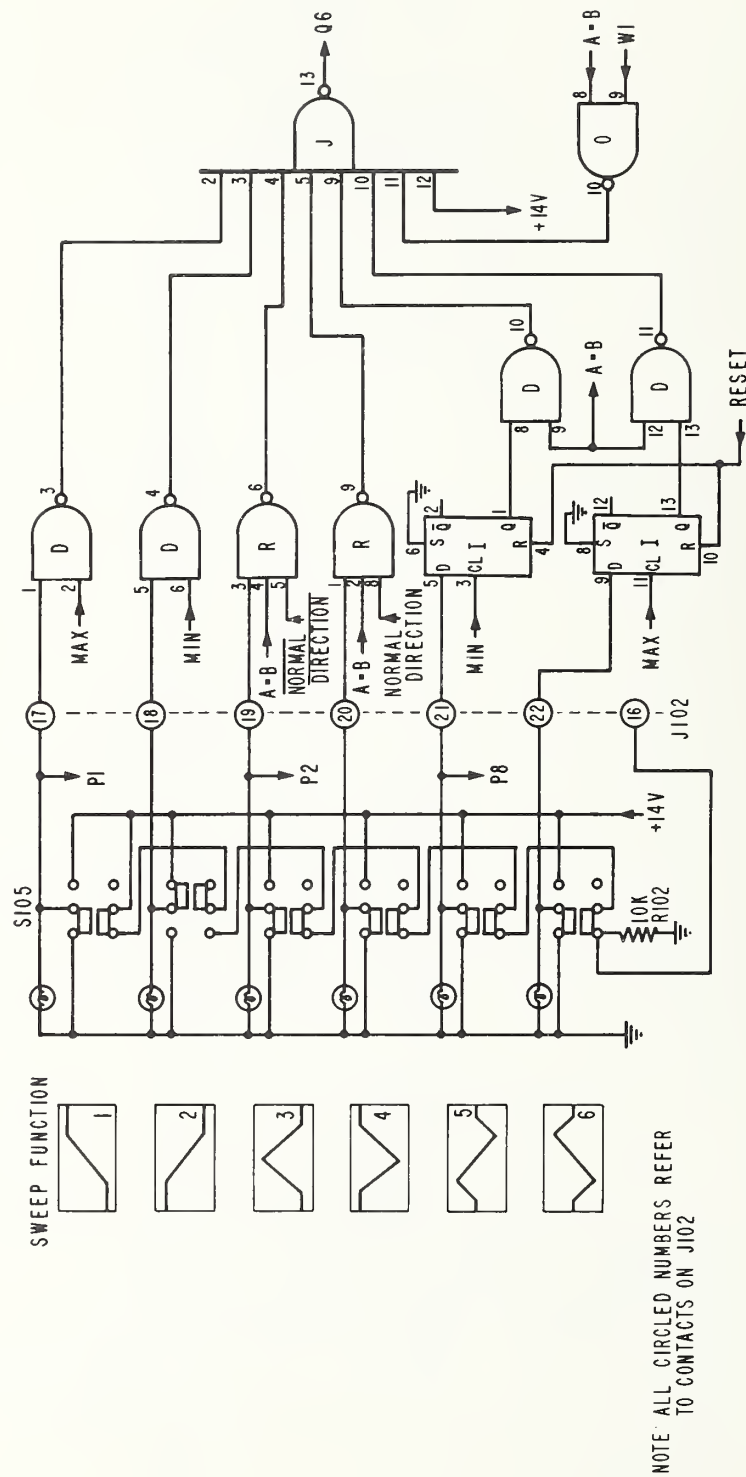


Figure 9. Sweep function selection circuit.

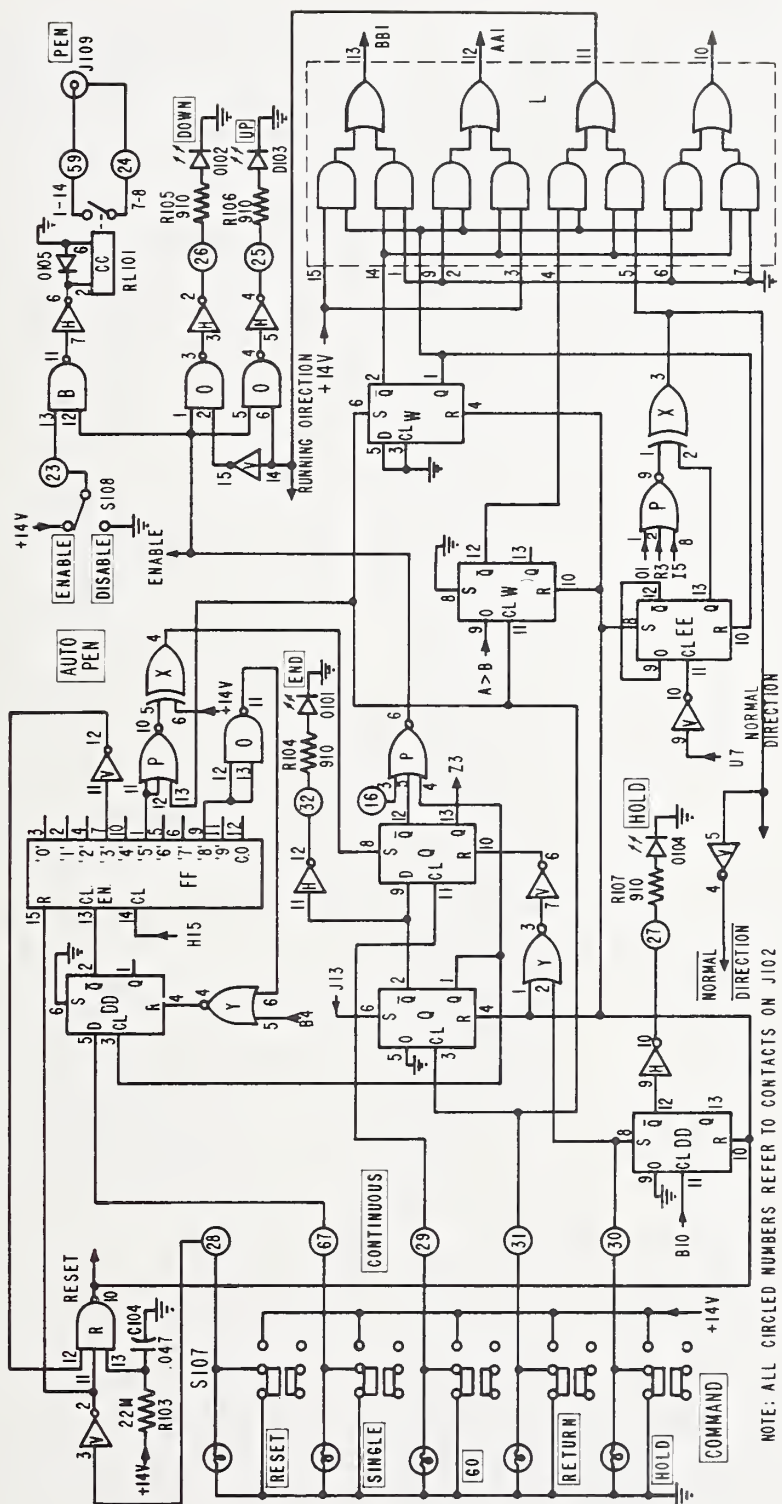


Figure 10. Sweep command circuit.

Table 1. Electrical Parts List for Bias Supply Control Module

<u>Schematic Reference</u>	<u>Description (Commercial description,* if appropriate, shown in parentheses)</u>
AR A, AR B, AR D, AR F	General purpose FET operational amplifier. (Teledyne Philbrick, Type 1421).
AR C	Digital to analog converter (Analog De- vices, Type AD562 KD/BIN)
AR E	Precision instrumentation amplifier (Analog Devices Type AD 521)
AR G, AR H	High-voltage FET operational amplifier (Teledyne Philbrick, Type 1022).
B	CD4011AE
C	CD4068AE
D	CD4011AE
E	MC14522
F	MC14522
G	MC14522
H	CD4049AE
I	CD4013AE
J	CD4068AE
K	CD4024AE
L	CD4019AE
M	Dual-In-line, 10 k Ω resistor network [contains 15 resistors; 12 used in circuit, figure 7].
N	MC14522
O	CD4011AE
P	CD4025AE
Q	CD4013AE
R	CD4023AE
S	CD4029AE
T	CD4029AE
U	CD4029AE
V	CD4049AE
W	CD4013AE
X	CD4013AE
Y	CD4001AE
Z	CD4063AE
AA	CD4063AE
BB	CD4063AE
CC	12 V Relay SPST [RL101]
DD	CD4013AE
EE	CD4013AE
FF	CD4017AE
C101	0.22 μ F, 50 V, mylar capacitor
C102, C103	0.1 μ F, 50 V, mylar capacitor
C104	0.047 μ F, 25 V, ceramic capacitor
C105	100 pF, silvered mica capacitor
C106	200 pF, silvered mica capacitor

*See disclaimer on p. vii.

Table 1. (Continued)

<u>Schematic Reference</u>	<u>Description (Commercial description,* if appropriate, shown in parentheses)</u>
C107, C108, C109, } C110, C111, C112, C113 } C114, C115, C116, C117 C118, C119	1.5 μ F, 50 V, ceramic capacitor 200 pF, silvered mica capacitor 22 μ F, 15 V, tantalum capacitor
D101, D102, D103, D104 D105 DS101	Light-Emitting Diode (Hewlett-Packard 4655) IN914 Panel lamp, neon, clear (Leecraft type 44N-0117)
DS102	Panel lamp, neon, amber (Leecraft type 44N-0113)
DS103	Panel lamp, neon, red (Leecraft type 44N-0111)
F101, F102 F103	1/4 A. SB, 3 AG Type 2A. SB, 3 AG Type
J101	22/44 PCB connector 0.156 contact centers (Amphenol 225-22221-101)
J102	35/70 PCB connector 0.100 contact centers (Stanford Applied Engineering CPH 7000-70)
J103	"Jones" plug (Cinch P-308-AB)
J104	15/30 PCB connector 0.156 contact centers (Amphenol 225-21521-101)
J105, J106	16-pin dual-in-line socket
J107, J108, J109	Insulated BNC chassis connector
J110, J111	UHF chassis connector
J112, J113	"Grabber" clip (Pomona Electronics Type 3925)
M101	4 1/2 digit panel meter (Ballantine 8310-05)
P101	16-pin dual-in-line plug
P102, P103	8-pin cable male connector, "Jones" type (Cinch Type P308-CCT)
PS101	Power supply, regulated with 14 V @ 0.5A (Power One Type HA15-5)
PS102	Power supply, regulated with +15 V and -15 V outputs @ 10 mA (Acopian type D15-10A)
PS103	Power supply, regulated with +120 V and -120 V outputs @ 40 mA (Teledyne-Philbrick type 2217)
R101, R102	10 k Ω , 5%, 1/2 W
R103	22 M Ω , 5%, 1/4 W
R104, R105, R106, R107	910 Ω , 5%, 1/2 W
R108	162 Ω , 1%, 1/2 W
R109	30.1 k Ω , 1%, 1/2 W
R110, R111, R112, R113, R114	100 k Ω , 1%, 1/2 W
R115, R116, R117	50 k Ω , 1/2 W
R118	33 k Ω , 1/2 W
R119	

*See disclaimer on p. vii.

Table 1. (Continued)

<u>Schematic Reference</u>	<u>Description (Commercial description,* if appropriate, shown in parentheses)</u>
R120, R121	10 k Ω , 1/2 W
R122, R123	9.1 k Ω , 1/2 W
R125	Optional. Can be used to calibrate initial offset dial, if desired.
R126	90.9 k Ω
R127, R128, R129, R130, R131	1 k Ω , 1/4 W, trim-pot.
R124, R132, R134, R135	10 k Ω , 1/4 W, trim-pot.
R136, R137	200 Ω , 1/4 W, trim-pot.
R138	20 k Ω , 1/4 W, trim-pot.
R133	10 k Ω , 2 W, 15-turn, potentiometer
R139, R140	1 k Ω , 2 W, 10-turn, potentiometer
R141	5 k Ω , 2 W, 10-turn, potentiometer
R142	2 k Ω , 2 W, 10-turn, potentiometer
R152	22 M Ω , 1/4 W, 5%
RL101	Dual-in-line reed relay, contact rating 10 VA (MRR1AD 12 VDC Struthers-Dunn, Inc.)
S101, S102	Double-pole, double-throw, 3-A @ 125 VAC toggle switch
S103, S104, S109	4 P 3-pos. toggle switch (Alco MTA406A) [S104 wired to form 2-pole, 3-pos. switch].
S105	6-section, reciprocal release, pushbutton switch. (LEDEX Series 1400 pushbutton switch) [The contacts operate when the pushbutton is depressed, contacts remaining operated and the button depressed until any other button is pressed, which causes release. The first button resets before the second button has been pressed far enough to operate its own contacts.]
S106	1-pole, 12-pos. shorting type rotary switch
S107	5-section pushbutton switch. (LEDEX Series 1400 pushbutton switch.) [4-sections: momentary interlock, normal pushbutton action. Contacts operate only for the time the pushbutton is depressed. Interlock is incorporated so that only one pushbutton can be depressed at a time. 1-section: push-push. Two-step action. When this button is pressed once, the con- tacts operate and the button remains in. When the button is pressed a second time, the contacts and the button reset. No inter- lock.]
S108	SPDT toggle switch
VR 101	Constant voltage source (Analog Devices, Type AD580).

*See disclaimer on p. vii.

Table 1. (Continued)

<u>Schematic Reference</u>	<u>Description (Commercial description,* if appropriate, shown in parentheses)</u>
W101	2 ft. long, 8-conductor, shielded cable. (Shield is used as one of the conductors.)
W102, W103	RG58 coax cable, 2 ft. long, male BNC connector on both ends.
W104	16-pin, ribbon cable, male plugs on both ends.
W105	Adapter cable for use with DVM (M101) as a calibration instrument. This cable can also be used to check the DVM for accuracy. Cable is RG174 coax, 3 ft. long.
Y101	Crystal, specifications: AT cut, 32 pf load capacity, parallel resonant, 512.000 kHz.
Enclosure	(Optima Type K051716R, beige w/bronze trim, Scientific Atlanta, Inc.)
Digital circuit board	(Cambion Type 715-1115-01, Cambridge Thermionic Corporation)

with time. A digital-to-analog (D/A) converter uses this number to produce a ramp voltage which varies linearly with time. The details of these circuits, the digital control circuits and the analog circuits necessary to produce the desired output levels are described in the remainder of this section.

3.1 Sweep Time Selection

The initial-to-peak sweep time, T , is the time necessary for a CLOCK output of the SWEEP TIME SELECTION circuit (see fig. 7) to accumulate 2048^{+0}_{-1} counts on the UP/DOWN COUNTER to be described in section 3.2.

The functions of the SWEEP TIME SELECTION circuit are to produce a stable high-frequency clock signal and to modify it using "divide by n " circuits to produce the appropriate CLOCK output.

The heart of the circuit is a crystal-controlled oscillator which can be seen as gate† B3 in figure 7. The output is buffered by an inverter (H15) which, in turn, feeds a "divide-by-125" circuit through a NAND gate (B4). The "divide-by-125" circuit employs a 7-stage binary counter (K) and two NAND gates (C13 and B10). Gate C13 detects the count of 125 (all inputs "high"††) and resets the counter through inverter B10. The 4.096-kHz clock signal is obtained from pin K3 because the signal there (MSB output) is most nearly symmetrical. Note that

*See disclaimer on p. vii.

†Gates and inverters will be designated by their output terminals.

††Positive logic is assumed.

the gate B4 will pass the oscillator output signal only when the level at pin B6 (marked ENABLE) is "high"; a "low" ENABLE level will terminate the sweep.

The 4.096-kHz clock signal is further modified by four programmable stages of frequency division (E, F, G, and N) and a "divide by 2" flip-flop (EE) to produce the desired CLOCK output at pin EE2. Switch S106 is used to program E, F, G, and N; i.e., to select the frequency division factor necessary to produce the desired value of T.

3.2 Up/Down Counter and Comparator

In this circuit an up/down counter is used to convert the CLOCK output to a binary number which will be the input for the D/A converter to be described in section 3.5. A binary number comparator is used to determine the points at which the counter reaches "critical numbers," i.e., numbers corresponding to sweep maxima, sweep minima, or end of sweep.

The UP/DOWN COUNTER AND COMPARATOR circuit is shown in figure 8. Three stages of presettable 4-bit up/down counters (S, T, and U) are used to generate a 12-bit binary number. The starting point for all sweeps is the number 2047₍₁₀₎. This is illustrated in figure 12 which shows the counter number sequences for the six sweep functions in the single sweep mode. In the continuous mode of operation, the selected sweep function is automatically and continuously repeated.

Three 4-bit binary comparators (Z, AA, and BB) are cascaded to form a 12-bit comparator which monitors the magnitude of the counter output (A inputs) relative to a reference number (B inputs). The truth table for the comparator is shown in table 2.

Table 2. Truth Table for UP/DOWN Comparator.

<div style="text-align: center;"> <div style="transform: rotate(-45deg); display: inline-block;">OUTPUT LINE AND LOCATION</div> <div style="display: inline-block;">CONDITION</div> </div>	"A>B"	"A=B"	"A<B"
	pin 5 of BB	pin 6 of BB	pin 7 of BB
A>B	1	0	0
A=B	0	1	0
A<B	0	0	1

During sweep operation, Q13 (A=B input to comparator Z) is "high." At all other times it is "low." This inhibits an A=B output that might otherwise occur during the switching associated with selection of the sweep function. Under certain switching conditions, if there were an

SWEEP FUNCTION	SEQUENCE
1	A TO B, STOP
2	C TO D, STOP
3	A TO B TO C, STOP
4	C TO D TO E, STOP
5	A TO B TO C TO D TO E, STOP
6	C TO D TO E TO F TO G, STOP

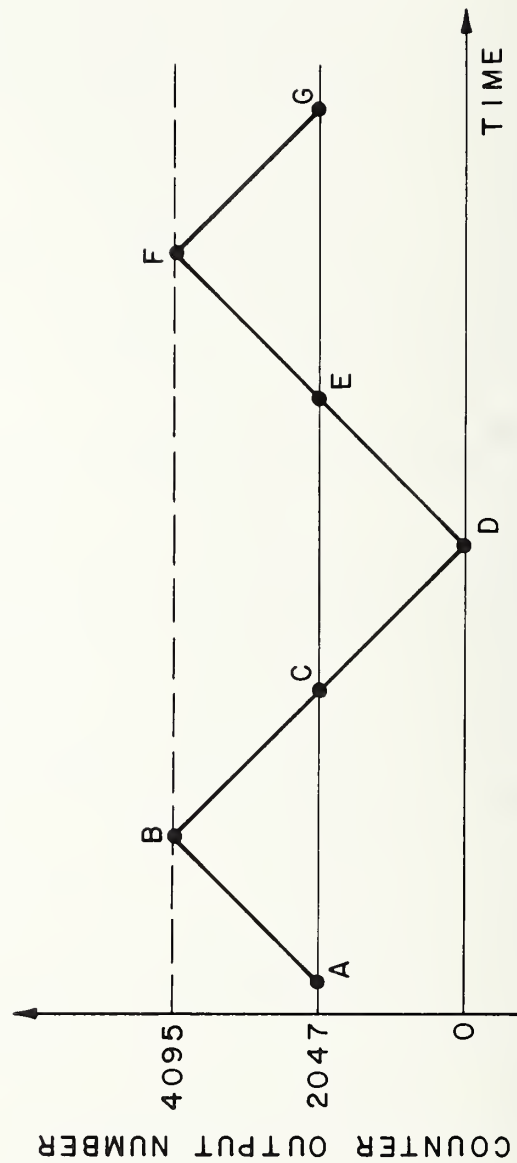


Figure 12. Counter number sequences for the six sweep functions (single sweep).

A=B output, the end of sweep light would go on, signaling that the sweep had ended before it had begun.

Two additional gates are used to monitor the state of the 12-bit output. NOR gate Y11 detects a minimum count of zero (all 12 outputs "low") in the following manner. The carry-out signal at pin 7 of counter U is normally "high" and goes "low" only when the counter reaches its maximum count in the up mode, or its minimum count in the down mode. Since a low at the carry-out terminal indicates *either* a minimum or a maximum count, additional information is required to resolve the ambiguity. A "low" at the A>B output indicates that the counter is below the starting count of 2047(10). A "high" output at gate Y11 (labeled MIN) indicates that both of its inputs are "low" and that the counter output is at a minimum. A maximum count of 4095 (10) (all twelve outputs "high") is detected in a similar manner by gate Y10. A "low" at the A<B output indicates that the counter is above the starting count of 2047(10). A "high" output at gate Y10 (labeled MAX) indicates that both of its inputs are low and that the counter is at a maximum.

3.3 Sweep Function Selection

The selection of the SWEEP FUNCTION is made by depressing one of the pushbuttons of S105 as indicated in figure 9. A mechanical interlock prevents the depression of more than one pushbutton at a time. Figure 9 also contains the logic circuitry that determines when a single sweep is terminated (assuming that it is *not* terminated by pressing the RESET button). The termination of a single sweep will occur when any of the 8 inputs to NAND gate J13 becomes "low." The required conditions for this to occur for each of the sweep functions is shown in table 3. They may be checked by referring to figure 9. The first six entries in the table are termination conditions for single sweeps during which neither the RETURN nor RESET buttons have been depressed. The 7th entry describes the termination conditions after the RETURN button has been pushed.

3.4 Sweep Command Circuit

The SWEEP COMMAND CIRCUIT in figure 10 comprises five subcircuits which can be considered according to the purpose served by each: (a) COMMAND pushbutton switches and associated circuitry, (b) DIRECTION circuit (c) SWEEP STATUS indicators, (d) AUTO PEN control circuit, and (e) CONTINUOUS restart circuit.

(a) Command Pushbutton Switches and Associated Circuitry

To initiate a sweep, all inputs to gate P6 must be "low"; this will produce a "high" on the ENABLE line. A "low" at input pin 3 of gate P6 indicates that one of the SWEEP FUNCTION pushbuttons is depressed. When the RESET button is depressed, the flip-flop Q1 is reset producing a "low" at input pin 4 and a "high" at input pin 5 of gate P6. This "high" at input pin 5 is changed to a "low" by depressing the GO pushbutton.

Table 3. Conditions Required for the Termination of a Single Sweep

<u>Sweep Function</u>	<u>Required Conditions</u>
1	(a) S105-1 depressed (b) MAX level "high"
2	(a) S105-2 depressed (b) MIN level "high"
3	(a) S105-3 depressed (b) <u>NORMAL DIRECTION</u> level "high" (c) A=B level "high"
4	(a) S105-4 depressed (b) <u>NORMAL DIRECTION</u> level "high" (c) A=B level "high"
5	(a) S105-5 depressed (b) MIN level "high" (c) A=B level "high"
6	(a) S105-6 depressed (b) MAX level "high" (c) A=B level "high"
Any	(a) RETURN button previously depressed (b) A=B level "high"

The HOLD pushbutton stops the sweep by resetting Q13, thereby changing the previous "low" at input pin 5 of P6 to a "high."

The RETURN pushbutton unconditionally returns the sweep to its starting point at its previous rate. Here, flip-flop Q1 is "clocked" to its reset state and flip-flop Q13 is set through gates P10 and X4.

The RESET command may be generated in three ways:

- (1) When the LOGIC POWER switch is initially turned on, the charging time constant of (R103) x (C104) produces a low at input pin 13 of gate R10 for a time sufficient to insure reset.
- (2) From the continuous restart circuit gate V12.
- (3) From the RESET pushbutton switch.

(b) Direction Circuit

The direction of the UP/DOWN COUNTER is determined by the level of the RUNNING DIRECTION line; a "high" corresponds to UP, a "low" corresponds to DOWN. When the RESET pushbutton is depressed, RUNNING DIRECTION control is transferred to gate X3 by flip-flop W1. At this time the output W1 is "high" and the output X3 is gated to the RUNNING DIRECTION line through AND/OR-select gate L11. The RUNNING DIRECTION at the start of a sweep is controlled by the gate P9; for SWEEP FUNCTIONS 1, 3, and 5 it is UP; for 2, 4, and 6 it is DOWN. When the maximum or minimum count is reached, the RUNNING DIRECTION is reversed by flip-flop EE13 and exclusive-OR gate X3. Pin 2 of gate X3 determines whether the level at pin 1 becomes inverted at the output or not; i.e., a "high" level at pin 2 causes inversion, a "low" level does not. During a sweep in which the RETURN pushbutton is *not* depressed, the NORMAL DIRECTION and RUNNING DIRECTION are the same.

If the RETURN pushbutton is depressed, the NORMAL DIRECTION level is not altered, but the RUNNING DIRECTION level *may* be altered through flip-flop W13, depending upon the levels of the A>B and NORMAL DIRECTION lines. If the levels of A>B and NORMAL DIRECTION are *both* "high" or *both* "low," the RUNNING DIRECTION level will be changed; if the A>B level is "high" and the NORMAL DIRECTION level is "low" (or vice versa), the RUNNING DIRECTION will not be changed.

It should be noted that although pressing the RESET pushbutton sets the COMPARATOR reference number to 2047 (10), pressing the RETURN pushbutton changes the COMPARATOR reference number to 2048 by setting flip-flop W1, which, in turn, changes the output levels of the AND-OR gates L12 and L13. This is done for the following reason. In the RESET condition, A=B and the A>B level is "low." This would cause the COUNTER to immediately start to count up if the RETURN pushbutton were pressed after RESET. In this case, the SWEEP is forced to end after one count by the change of reference number just described. This results in an offset of the output voltage at any END of SWEEP caused by pressing the RETURN pushbutton. The amount of this offset (1 part in 2047) is undetectable in normal use.

(c) Sweep Status Indicators

Four LEDs (light-emitting diodes) are used to indicate the operating state of the SWEEP. Only one LED (at most) can be on at a given time during a normal sequence of COMMANDs. When the ENABLE level from

gate P6 is "high," either the UP or DOWN LED will be on, depending upon whether the RUNNING DIRECTION level is "high" or "low." Depressing the HOLD pushbutton sets flip-flop DD13, which turns on the HOLD LED through inverter H10. If the sweep is resumed by pressing the GO pushbutton, flip-flop DD13 is clocked to its "reset" state. The END LED turns on at termination of the SWEEP when flip-flop Q1 is set by a "high" level at J13. When the RESET pushbutton is depressed, any previously turned-on LED is turned off. Thus, if all LEDs are off, it signifies that RESET has taken place.

(d) Pen Control Circuit

Both inputs to NAND gate B11 must be "high" to energize the PEN relay RL101. Thus, the PEN control circuit will be closed only when the AUTO PEN switch is in the ENABLE position *and* the ENABLE level is "high."

(e) Continuous Restart Circuit

A decade counter, FF, is used to generate (1) a RESET pulse via inverter V12 and NAND gate R10; (2) a "start" pulse via NOR gate P10 and exclusive-OR gate X4; and (3) a "self-turnoff pulse: via NAND gate O11 and NOR gate Y4 in the following manner. A "high" from NAND gate J13 signifies the end of a sweep and sets flip-flop Q1. A "high" from pin Q1 clocks flip-flop DD1 to its "set" state when the SINGLE-CONTINUOUS switch is in the CONTINUOUS position. This causes a "low" level at the clock enable line FF13 of the counter* FF, allowing it to start counting 512 kHz pulses from the oscillator buffer-inverter H15. First, the RESET pulse is generated from gate V12; next, the "start" pulse from X4 sets Q13 (this is equivalent to a GO command), and finally, the counter is "disabled" by the "self-turnoff pulse" from Y4, which resets flip-flop DD1, bringing the clock enable line of the counter "high" preventing further counts. This sequence is repeated continuously if the SINGLE-CONTINUOUS switch remains in the CONTINUOUS position.

If, at the end of the sweep, this switch is in the SINGLE position, flip-flop DD1 is clocked to its "reset" state, in which case, the counter-clock enable level is "high," and counting is inhibited.

3.5 Analog Circuit

The digital circuit produces a 12-bit binary number which varies linearly with time. The heart of the analog circuit is a digital to analog (D/A) converter which uses this time-varying binary number to produce a voltage which varies linearly with time. A series of dc amplifiers is used to make this voltage bipolar and to obtain the desired amplitude and offset levels.

*For this counter, the "clock enable level" must be "low" to enable counting; a "high" level disables or inhibits counting.

Current from the D/A converter AR C (fig. 11) develops a voltage across an internal load resistor. This voltage is passed through amplifier AR B to provide a basic single-ended sweep signal. A portion of this is selected by adjusting the SWEEP AMPLITUDE and TRIM potentiometers and then summed with an INITIAL OFFSET voltage through amplifier AR D to produce the -10 V output. This output is inverted by amplifier AR F to produce the +10 V output. Amplifiers AR G and AR H are used to raise these levels to provide the +100 V and -100 V outputs, respectively. The voltage regulator VR101 provides a stable 2.5-V (nominal) level which is used as a reference for the D/A converter and a source of INITIAL OFFSET voltage. An INITIAL OFFSET voltage of opposite polarity is obtained by using an inverter, AR A. The instrumentation amplifier AR E is used to provide a single-ended output labeled ANALOG OUTPUT which is equal to one-half the difference between that at the +10 V and -10 V output terminals. It is intended for monitoring the sweep generator output with an instrument having one input terminal grounded.

3.6 Power Supplies and Metering

The schematic circuit diagram of the POWER SUPPLIES AND METERING for the control module is shown in figure 13.

4. CIRCUIT DETAILS OF HIGH-VOLTAGE AMPLIFIER MODULE

A schematic diagram of the power supplies and switching for the HVAM is shown in figure 14. The high-voltage amplifier consists of two substantially identical amplifiers, one of which is driven in the positive direction while the other is driven in the negative direction, and vice versa. The two amplifiers are represented schematically in the right and left halves of figure 15. The electrical components shown in figures 14 and 15 are described in table 4. The circuit description which follows refers only to the right side of figure 15, the amplifier which produces the "+" output. Overall feedback from the output to the input of the driver section linearizes the transfer function and "regulates out" power supply variations.

4.1 General Specifications

Each amplifier, when driven by a signal in the range -10 to +10 V, produces a signal proportional to the negative of the input signal. The proportionality constant (gain) is selectable such that -10 V input will produce outputs of 0.5, 1.25, 2.5, 5.0, and 12.5 kV. The circuit is such that +10 V input produces the negatives of the voltages indicated above. The amplifiers can drive a 50-M Ω external load. The anticipated voltage sweep rates are low so that capacitive loading of the output is not a problem.

4.2 Output Stage

The output stage is the most challenging design, having to be constructed within the capabilities of available tubes, and controls what

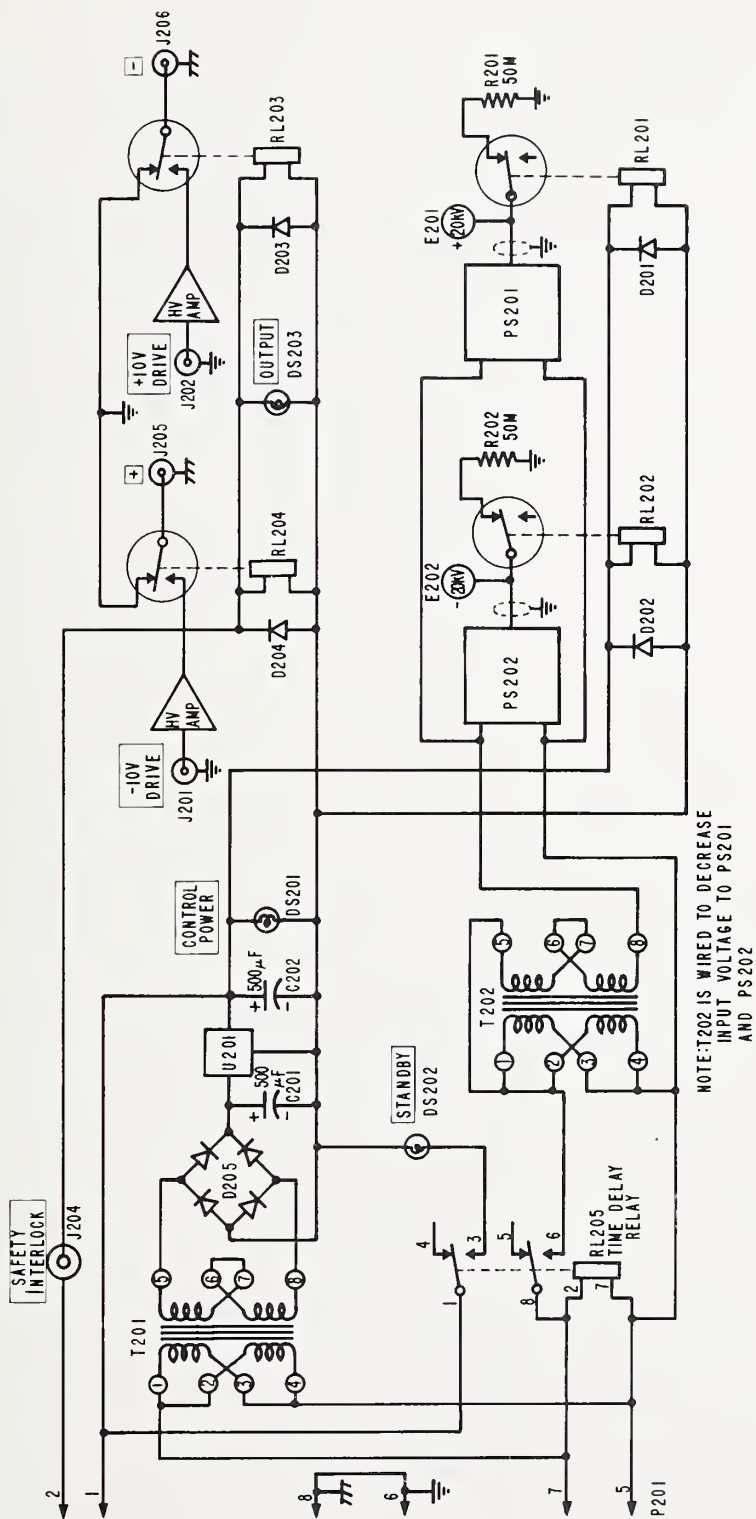


Figure 14. Power supplies and switching for high-voltage amplifier module.

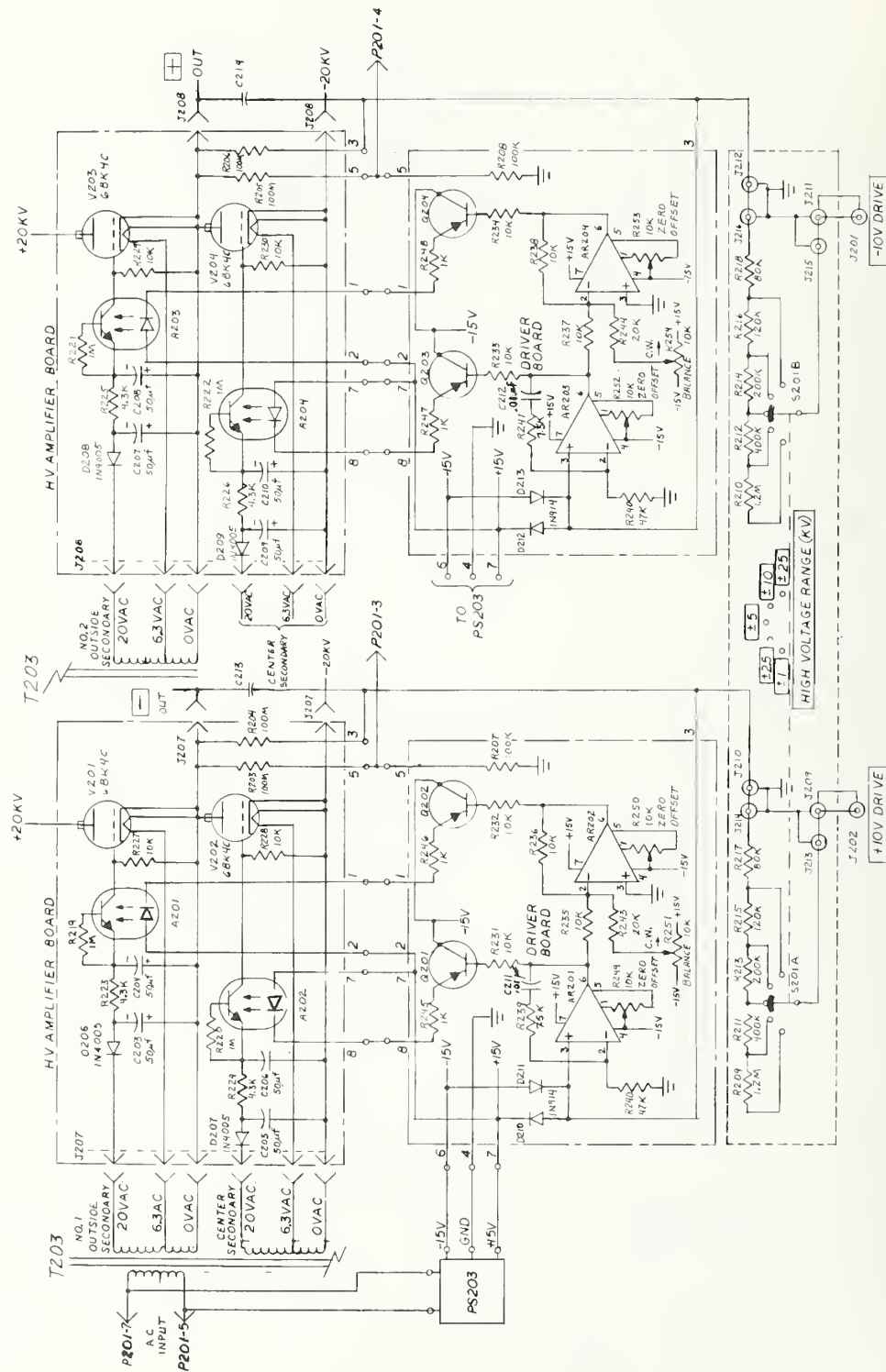


Figure 15. High-voltage amplifier schematic.

Table 4. Electrical Parts List for HV Amplifier Module

<u>Schematic Reference</u>	<u>Description (Commercial description,* if appropriate, shown in parentheses)</u>
A201, A202, A203, A204	50 kV optical coupler (Optron, Type OPI-150)
AR201, AR202, AR203, AR204	General purpose FET operational amplifier (Teledyne Philbrick, type 1421).
C201, C202	500 μ F, 50 VDC, electrolytic capacitor
C203, C204, C205, C206 } C207, C208, C209, C210 }	50 μ F, 50 VDC electrolytic capacitor
C211, C212	0.01 μ F, 50 V, ceramic capacitor
C213, C214 (Gimmick capacitor)	3/4" length of copper braid around output cable covered with shrinkable tubing.
D201, D202, D203, D204	IN4005 diode
D206, D207, D208, D209	IN4005 diode
D205	18DB6A bridge rectifier
DS201, DS202, DS203	24 V indicator lights
E201, E202	Corona ring, high-voltage terminal
J201, J202, J204	Insulated BNC coaxial chassis connector (Amphenol type 31-010)
J203	8-pin cable female connector, "Jones" type (Cinch type S-308-CCT)
J205, J206	High-voltage coaxial chassis connector (Amphenol type 97-3102A-18-420S)
J207, J208	HV connector assembly
J209, J210, J211, J212	Sub-minax coax cable connector (Amphenol type 27-7)
J213, J214, J215, J216	Sub-minax receptacle (Amphenol type 27-9).
P201	8-pin chassis male connector, "Jones" type (Cinch type P-308-AB)
PS201, PS202	Power supply, 20 kV, dc, @ 1 mA (Del, type 20-1-4)
PS203	Power supply, regulated with +15 V and -15 V outputs @ 100 mA (Acopian type D15-10A).
Q201, Q202, Q203, Q204	2N4036 transistor.
R201, R202	50 M Ω , 5 W, 5%. (IRC Type MVP)
R203, R204, R205, R206	100 M Ω , 15 W, 1%. (Caddock Type MG815)
R209, R210	1.2 M Ω , 1/4 W, 1%. (Caddock Type MG650)

*See disclaimer on p. vii.

Table 4. (Continued)

<u>Schematic Reference</u>	<u>Description (Commercial description,* if appropriate, shown in parentheses)</u>
R211, R212	400 k Ω , 1/4 W, 1%.
R213, R214	200 k Ω , 1/4 W, 1%.
R215, R216	120 k Ω , 1/4 W, 1%.
R217, R218	80 k Ω , 1/4 W, 1%.
R219, R220, R221, R222	1 M Ω , 1/2 W, 5%.
R223, R224, R225, R226	4.3 k Ω , 1/2 W, 5%.
R227, R228, R229, R230	10 k Ω , 1/2 W, 5%.
R231, R232, R233, R234	10 k Ω , 1/2 W, 5%.
R235, R236, R237, R238	10 k Ω , 1/2 W, 5%.
R239, R241	7.5 k Ω , 1/2 W, 5%.
R240, R242	47 k Ω , 1/2 W, 5%.
R243, R244	20 k Ω , 1/2 W, 5%.
R245, R246, R247, R248	1 k Ω , 1/2 W, 5%.
R249, R250, R251, R252, R253, R254	10 k Ω , 1/4 W, 15-turn trim-pot
RL201, RL202, RL203, RL204	High-voltage relay (ITT Jennings, Type RE6B-26-N300).
RL205	Time-delay relay (Guardian TD062C30-115A).
S201	2-pole, 5-position, shorting type rotary switch
T201, T202	Transformer (Stancor, Type P6377).
T203	High-voltage isolation transformer. (NWL Model 24543).
U201	24 V dc regulator.
V201, V202, V203, V204	Vacuum tube 6BK4C/6EL4A.
Miscellaneous	
4 - Tube sockets (Amphenol, Type 78S8-1M-0125)	
4 - Cap and lead assembly for V101-V104 (RCA 114048)	

*See disclaimer on p. vii.

the drivers must do. Therefore, the output stage is the starting point of the description. The 6BK4C tube is rated to withstand 27 kV plate to cathode and has maximum power and current ratings of 40 W and 1.6 mA, respectively. With the effective load resistance of 25 M Ω (50-M Ω external load in parallel with 50-M Ω internal load) the current limitation is more restrictive than the power limit. The 6BK4C is intended as a shunt regulator tube so it is not designed to have a low voltage drop at zero grid bias. With a 20-kV power supply and 25-M Ω load the zero-bias plate voltage is about 5 kV. With a ± 20 kV power supply, the swing is thus limited to ± 15 kV. With the usual 20% tolerance on tube specifications the actual limits may be as low as ± 13 kV. When one tube is zero-biased, the other one is cut off and has approximately 35 kV across it. The rated voltage is then exceeded substantially at the limits of the swing. This undesirable condition is accepted because no higher-rated tube is available; there is no other choice. However, the rating is based on leakage developing due to glass electrolysis when the voltage is maintained constant as it is in shunt regulator service. In the present service, the time the tube spends under maximum voltage stress is much less than 100% of the operating time, so electrolysis will proceed more slowly. Also, the temperature of the bulb is low since the dissipation is much less than the allowed 40 W. Electrolysis rate increases as an exponential of the absolute temperature. Life of the 6BK4C's is expected to be reasonable, and the chance of having to replace tubes was taken as a calculated risk. Although our use experience is limited (several hundred hours over a period of approximately one year), no failures have occurred thus far.

Each tube has a floating 28-V negative-bias supply which is derived from a 20-V winding of T203. The 6.3-V tap on the same winding provides heater current. V204 and V202 (of the other amplifier) share the winding which is connected to the -20 kV power supply. The 10-k Ω grid resistors (R229 for V203, and R230 for V204) bias the grids to 0 V when the transistors of the optical couplers, A203 and A204, are cut off. The high-voltage power supplies should not be turned on with the driver circuits disconnected since approximately 3 mA per tube would flow, exceeding both the current and power ratings of the tubes. With properly adjusted drivers connected, tubes are not both biased on simultaneously. When the light-emitting diode of A203 is turned on, the transistor of A203 conducts, biasing V203 toward cutoff. When A203 is driven on, A204 is driven off so that V203 is turned off as V204 is turned on, and the output voltage swings in a negative direction. The maximum negative bias for the tubes is about 20 V when the optical coupler transistors are full on. R225 and R229 form a voltage divider with a ratio of approximately 0.7. Thus, 20 V should be enough to cut the tubes off at 35-kV plate voltage based on an extrapolation of published curves. Tubes at the limit of the allowable $\pm 20\%$ tolerances might not cut off. In our experience, however, none of the ten tubes tried failed to operate as desired.

The optical couplers, A203 and A204, have a transfer ratio of about 0.7. About 2 mA must flow to bias the tube off, which means about 3 mA in the LED.

The bias supplies are typical half-wave RC-filtered power supplies and are unregulated. Bias variations are taken out by the overall feedback.

4.3 Driver Circuit

The dividing line between the output circuit and the driver circuit bisects the optical couplers and the feedback resistors. All parts of the driver circuits are within ± 15 V of ground.

Transistors Q203 and Q204 drive the LED's of the optical couplers. The LED currents are limited by series resistors R247 and R248 to less than 30 mA. R233 and R234 limit the base currents of Q203 and Q204 to conservative values; these values allow adequate drive and also avoid loading the outputs of AR203 and AR204.

AR204 is operated as a unity-gain inverter to provide the inverted drive for V203. Additional current is injected into the node at pin 2 to provide a dc offset in the output. This offset is used to establish the quiescent current in the output tubes at 0 V output. See Section 5.2 for a discussion of how the quiescent point is established.

AR203 is operated locally open-loop at dc to provide a high gain near the overall amplifier summing point. The local feedback provided by R240, R241 and C212 produces a high-frequency roll-off to stabilize the overall feedback amplifier. The overall feedback summing point is at the + input of AR203, which is the - input if the whole amplifier is considered as a unit. Diodes D212 and D213 protect this input from the inevitable surges which occur in high-voltage equipment. R206 and C214 in parallel provide the overall feedback path and establish main frequency roll-off of the whole amplifier. C214 is about 2.5 cm of braid around the output cable which produces a capacitance of about 2 pF.

The overall gain is established by choosing the input resistor with S201B (a make-before-break selector switch). The input resistance is varied from 80 k Ω to 2 M Ω .

5. CALIBRATION AND ADJUSTMENTS

5.1 Bias Supply Control Module

a. Digital Circuit

No adjustments are necessary or possible.

b. Analog Circuit

Either the digital voltmeter (DVM) in the control module or a separate DVM may be used for calibration and adjustment of the ANALOG CIRCUIT. If the internal DVM is to be used, it will be necessary to install an

adaptor cable (W105) to receptacle J103 at the rear of the control module; the leads will be connected to the DVM when the METER RANGE switch is in the HV position. The internal DVM should be checked for accuracy before proceeding with the ANALOG CIRCUIT calibration.

(1) Initial Offset Calibration

- (i) Remove VR101 from its socket and connect a short jumper wire between the output and ground terminals on the socket. This will provide 0.00 V input to AR A.
- (ii) Measure the output of AR A with a DVM and adjust trim-pot A-ZERO for 0.00 V output.
- (iii) Remove the jumper wire and reinstall VR101.
- (iv) Measure the output from VR101 and record the value.
- (v) Reverse the meter leads*, measure the output of AR A, and adjust trim-pot A-TRIM to obtain the same reading as that previously obtained from the output of VR101.

(2) Zero adjustment of AR B

- (i) Connect the DVM to the output of AR B (pin 6).
- (ii) Momentarily depress the RESET button; then adjust B-ZERO for 0.00 V output.

(3) Zero adjustments of AR D, AR E, AR F, AR G, and AR H

- (i) Set SWEEP AMPLITUDE and associated TRIM completely counterclockwise (CCW). Set INITIAL OFFSET and associated TRIM completely CCW; set INITIAL OFFSET switch to ZERO. Carry out following steps *in sequence*.
- (ii) Connect DVM to AR D output at -10 V BNC connector (J108) or pin 6 of AR D and adjust D-ZERO for 0.00 V meter reading.
- (iii) Connect DVM to AR F output at +10 V BNC connector (J107) or pin 6 of AR F and adjust F-ZERO for 0.00 V meter reading.
- (iv) Connect DVM to AR E output at ANALOG OUTPUT connector (J109) or pin 7 of AR E and adjust E-ZERO for 0.00 V meter reading.
- (v) Connect DVM to AR G output at +100 V UHF connector (J110) and adjust G-ZERO for 0.00 V meter reading.
- (vi) Connect DVM to AR H output at -100 V UHF connector (J111) and adjust H-ZERO for 0.00 V meter reading.

*For best results (greatest accuracy) the polarity of the DVM should be the same for all measurements.

(4) Amplifier tracking (gain) adjustments

- (i) Adjust D-TRIM to approximate center of rotational range.
- (ii) Select SWEEP FUNCTION 1 (Ascending single ramp) and a low INITIAL TO PEAK SWEEP TIME. Momentarily depress the RESET pushbutton and then the GO pushbutton. After the END of SWEEP light comes on, adjust the SWEEP AMPLITUDE CONTROL for exactly -5.00 V at the -10 V output connector. Carry out the following steps *in sequence*.
- (iii) Connect DVM to AR F output and adjust F-TRIM for a +5.00 meter reading.
- (iv) Connect DVM to AR G output and adjust G-TRIM for a +50.00 meter reading.
- (v) Connect DVM to AR H output and adjust H-TRIM for a -50.00 V meter reading.
- (vi) Connect DVM to ANALOG OUTPUT and adjust E-TRIM for a +5.00 V meter reading.

This completes the ANALOG CIRCUIT calibration.

5.2 High-Voltage Amplifier Module

Only 3 adjustments are provided. The zero-offset adjustments provided on AR203 and AR204 by R252 and R253 respectively are noncritical and need adjustment only if the associated amplifier is replaced. The quiescent point adjustment may be needed if the replacement of one or more tubes is required. The overall feedback maintains the amplifier performance quite well even if these adjustments are not optimized.

Remove time-delay relay from its socket. This will prevent accidental high-voltage turn-on.

a. Zero-Offset Adjustment

1. Remove both operational amplifiers from high-voltage driver board.
2. Measure the slider voltage of R254 (it can be accessed at the end of R244 that is nearer the center of R254) with an external DVM and adjust the center trim-pot, R254, for 0.00 V.
3. Temporarily connect a 10-M Ω resistor between pin 2 and 6 of operational amplifier AR203. Switch high-voltage range switch to 25 kV and install both operational amplifiers.
4. Short the -10 V driver connector, J201. Turn power switch to standby and adjust zero-offset trim-pot, R252, near operational amplifier AR203 for 0.00 V reading on operational amplifier output pin 6.
5. Measure the output of operational amplifier AR204 pin 6 and adjust the trim-pot nearest AR204 for 0.00 V. Remove short across -10 V drive and 10-M Ω resistor. Reinsert the time delay relay.

As mentioned in section 4.3, the balance potentiometer R254 is used to establish the quiescent operating current in V203 and V204. With zero volts input the overall feedback will cause the intermediate signal voltages in the amplifier to assume values which will bring the output voltage to zero. When the output voltage is zero equal currents flow in V203 and V204. Producing an offset voltage in *that portion of the circuit which drives V203 but does not affect the drive to V204* will change the quiescent current. The adjustments described above reduced this offset to zero.

b. Quiescent Point Adjustment

While the voltages and currents in the high-voltage amplifier may not be lethal, contact with them would certainly be unpleasant. Before starting the following procedure, power must be off and grounds connected to the output and both power supply corona caps. Remove the connector from the plate V204 and connect a 200- μ A meter from the connector to the cap. The + of the meter goes to the connector. The meter must be insulated so there is at least 2 or 3 cm between it and the nearest conductors. The measurement will be made with the meter near ground but transients may occur during turn-on. With the meter securely in place where it can be read easily, remove the grounds and go through normal turn-on procedure. With the input at 0.00 V, check that the output is also 0.00 V. Then, adjust R254 for a quiescent current between 5 and 50 μ A. The output should still be 0.00 V. Shut off the power, ground the output and power supplies, remove the meter, and replace the plate cap.

The procedure for adjusting the amplifier on the left side of figure 15 is exactly the same except, of course, that the component designation numbers are different.

ACKNOWLEDGMENT

The authors acknowledge with gratitude many helpful suggestions contributed by Jeremiah Avins during the development of the equipment described in this report.



APPENDIX A

This appendix contains information which is intended for use by anyone who wants to duplicate the Bias Supply Control Module described in the body of the report. It consists of:

- (i) A list of the mechanical parts which are not commercially available, (table 5)
- (ii) detailed drawings of those parts, and
- (iii) Drawings and photographs showing the placement of the mechanical parts and electrical components identified in tables 1 and 5.

Table 5. List of Mechanical Parts in Bias Supply Control Module (not commercially available)

<u>Part No.</u>	<u>Part Description</u>	<u>Drawing No.</u>
1	Front panel	MA1
2	Rear panel	MA2
3	Base panel	MA3
4	Clamp for power supply PS102	MA3
5	Clamp for power supply PS103	MA3
6	Analog printed-circuit board	MA7



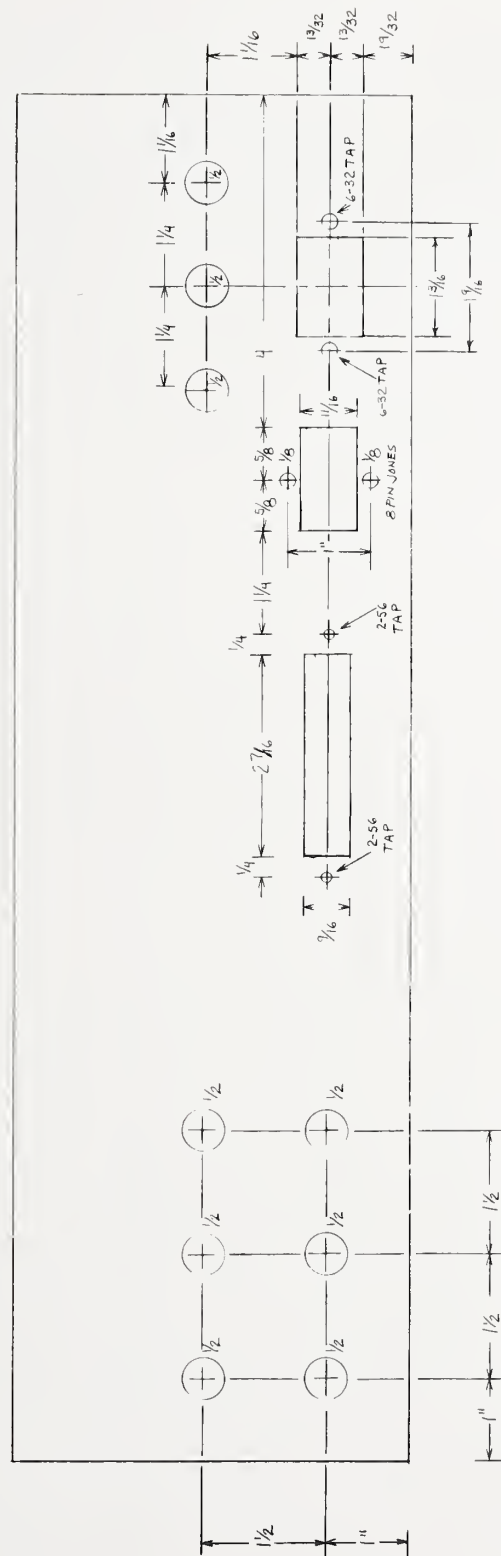


Figure MA2. Rear panel, bias supply control module.

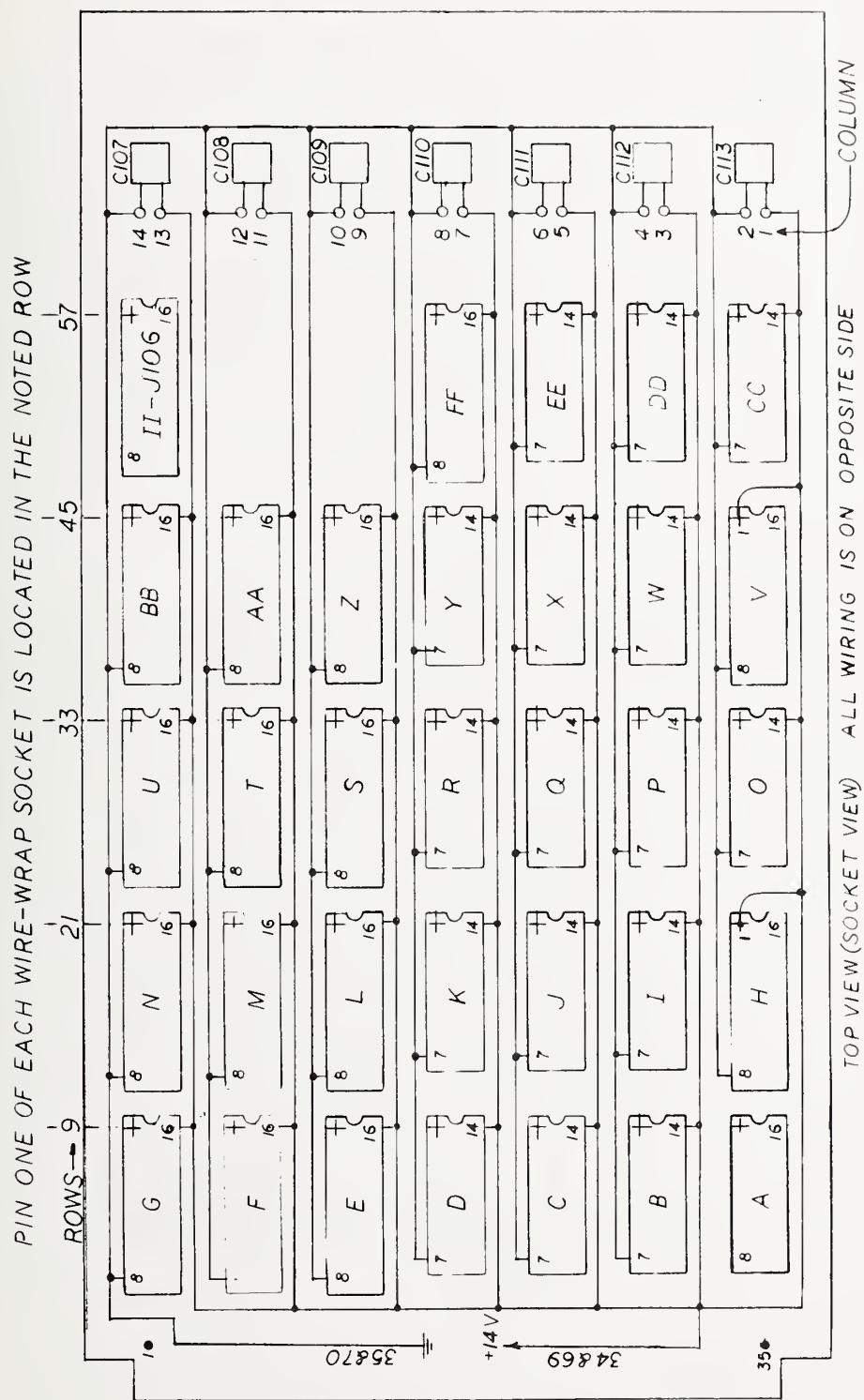


Figure MA4. Digital logic board layout, bias supply control module.

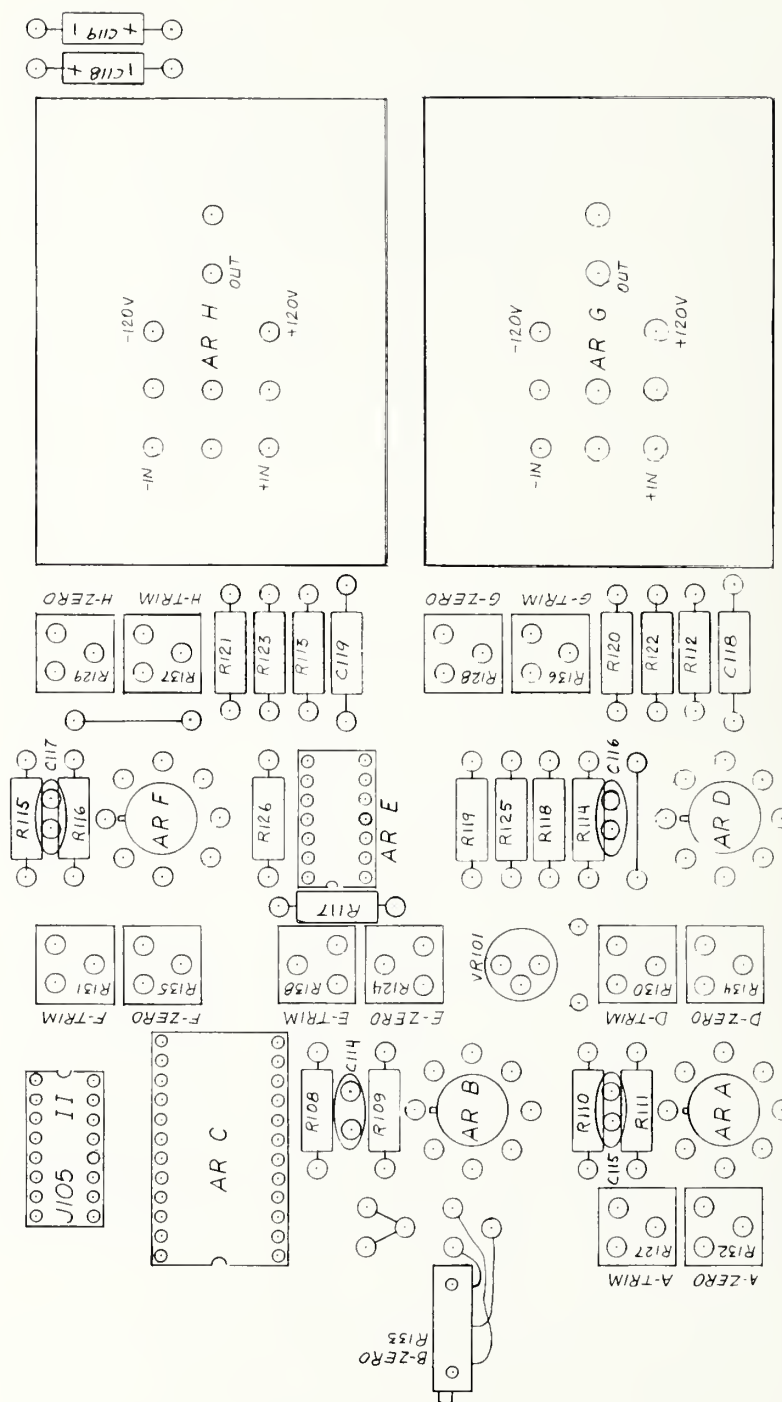


Figure MA5. Analog circuit board component side, bias supply control module.

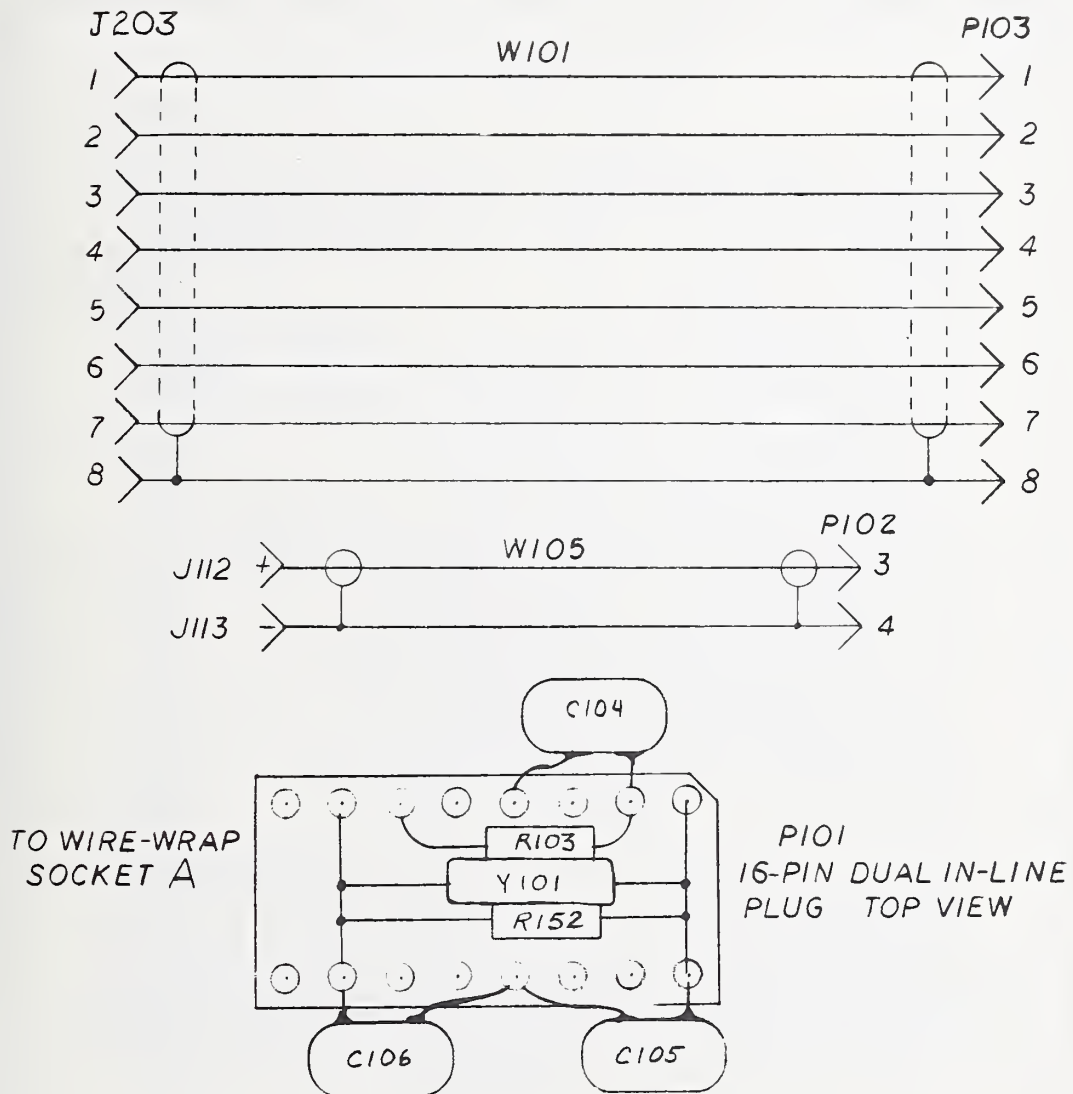


Figure MA6. Cables W101, W105, and crystal circuit subassembly, bias supply control module.

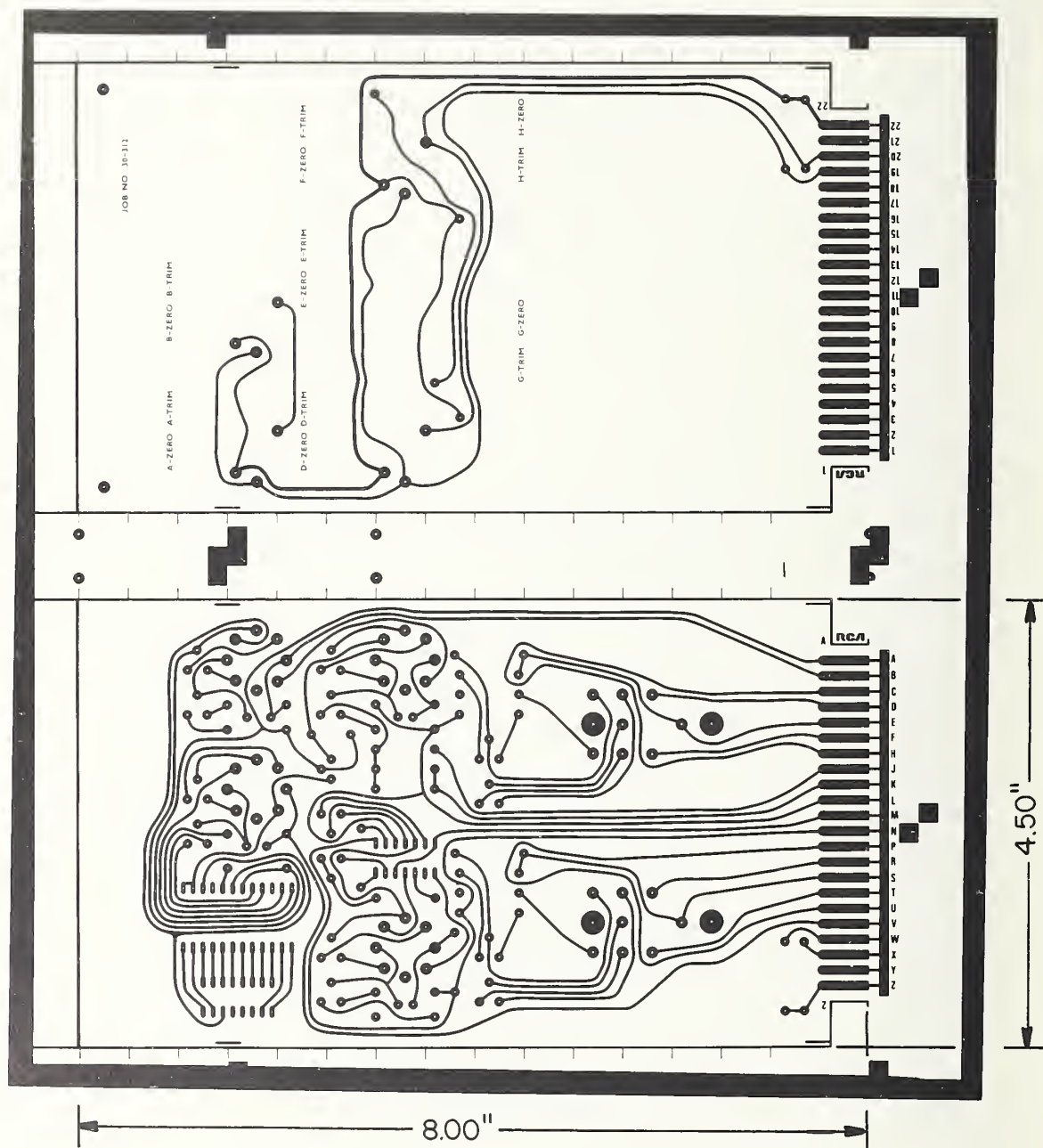


Figure MA7. Analog printed-circuit board, bias supply control module.

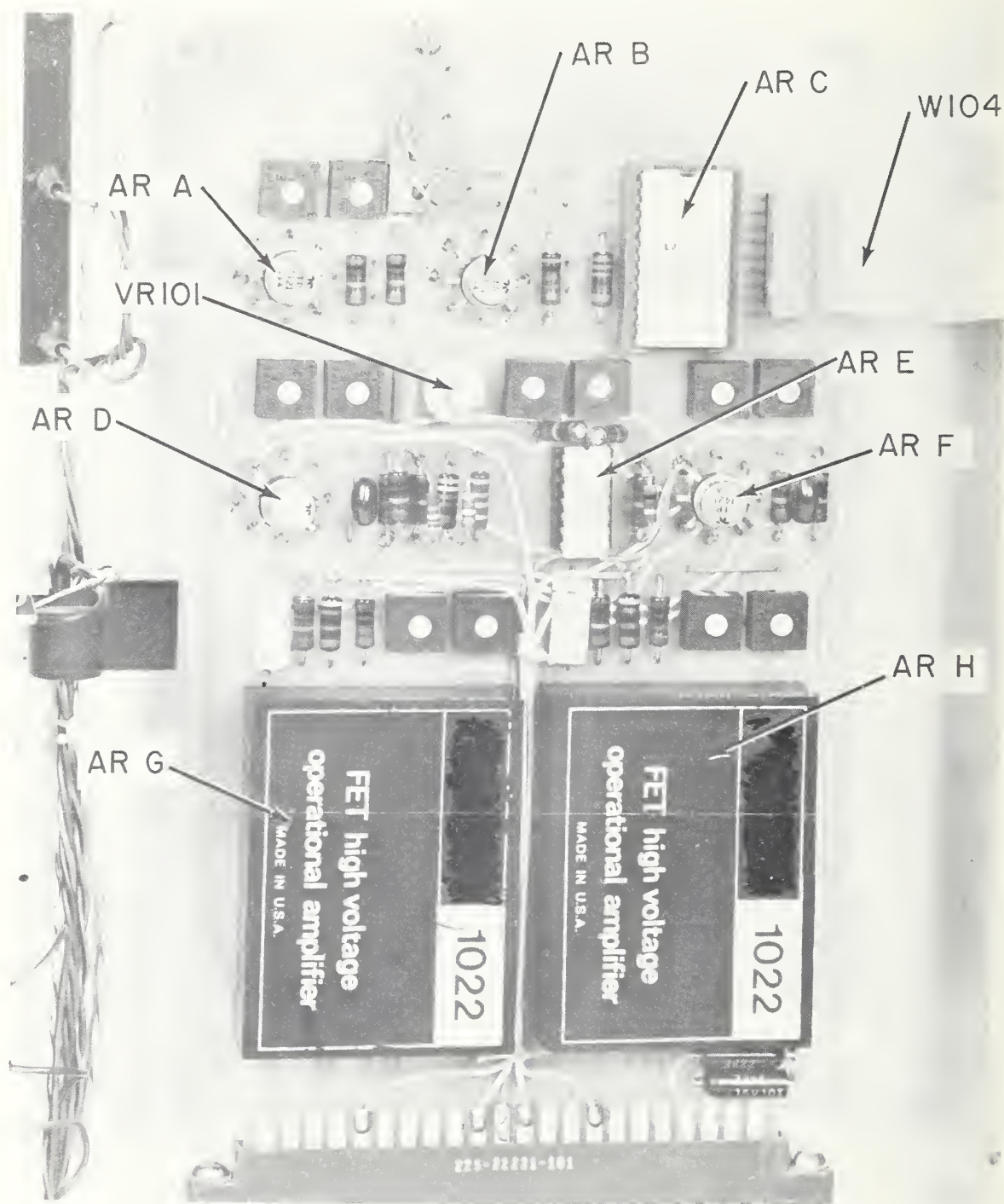


Figure A2. Top view of analog circuit board, bias supply control module.

APPENDIX B

This appendix contains information which is intended for use by anyone who wants to duplicate the High Voltage Amplifier Module described in the body of the report. It consists of:

- (i) A list of the mechanical parts which are not commercially available, (table 6)
- (ii) detailed drawings of those parts, and
- (iii) a drawing and photographs showing the placement of the mechanical parts and electrical components identified in tables 4 and 6.

Table 6. List of Mechanical Parts in High-Voltage Amplifier Module (not commercially available)

<u>Part No.</u>	<u>Part Description</u>	<u>Drawing No.</u>
1	Front Panel	MB1
2	Rear Panel	MB2
3	Base Panel	MB3
4	Left Side Panel	MB4
5	Right Side Panel	MB4
6	Chassis Top Cover	MB5
7	Chassis Bottom Cover	MB5
8	HV Connector Assembly	MB6
9	Driver Printed-Circuit Board	MB7
10	HV Amplifier Printed-Circuit Board	MB8
11	Clamp For Power Supply PS203	MB11

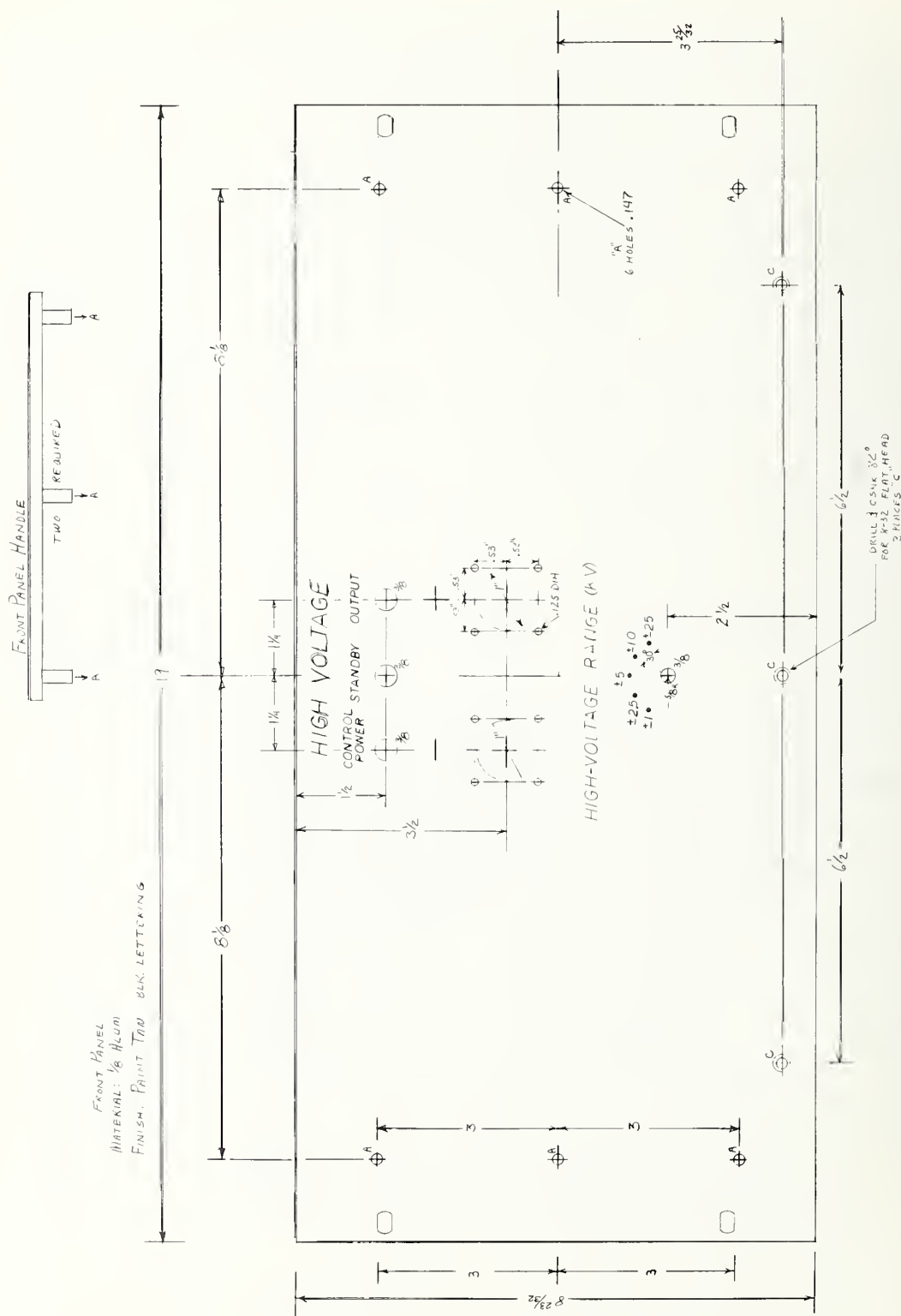
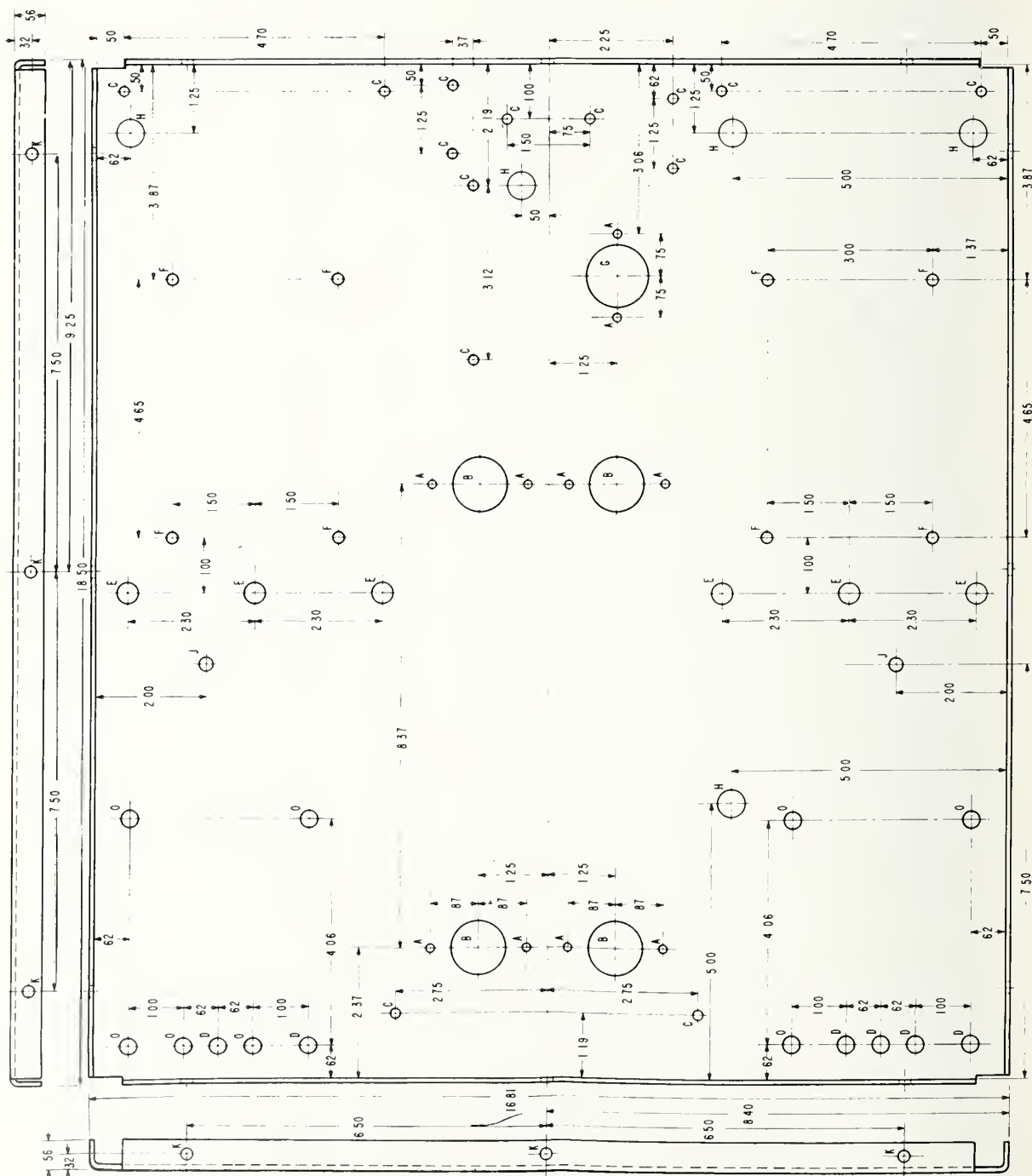


Figure MB1. Front panel, HV amplifier module.



LETTER	HOLE DIA
A	147
B	100
C	173
D	31
E	37
F	204
G	1125
H	50
J	25
K	213

Figure MB3. Base panel, HV amplifier module.

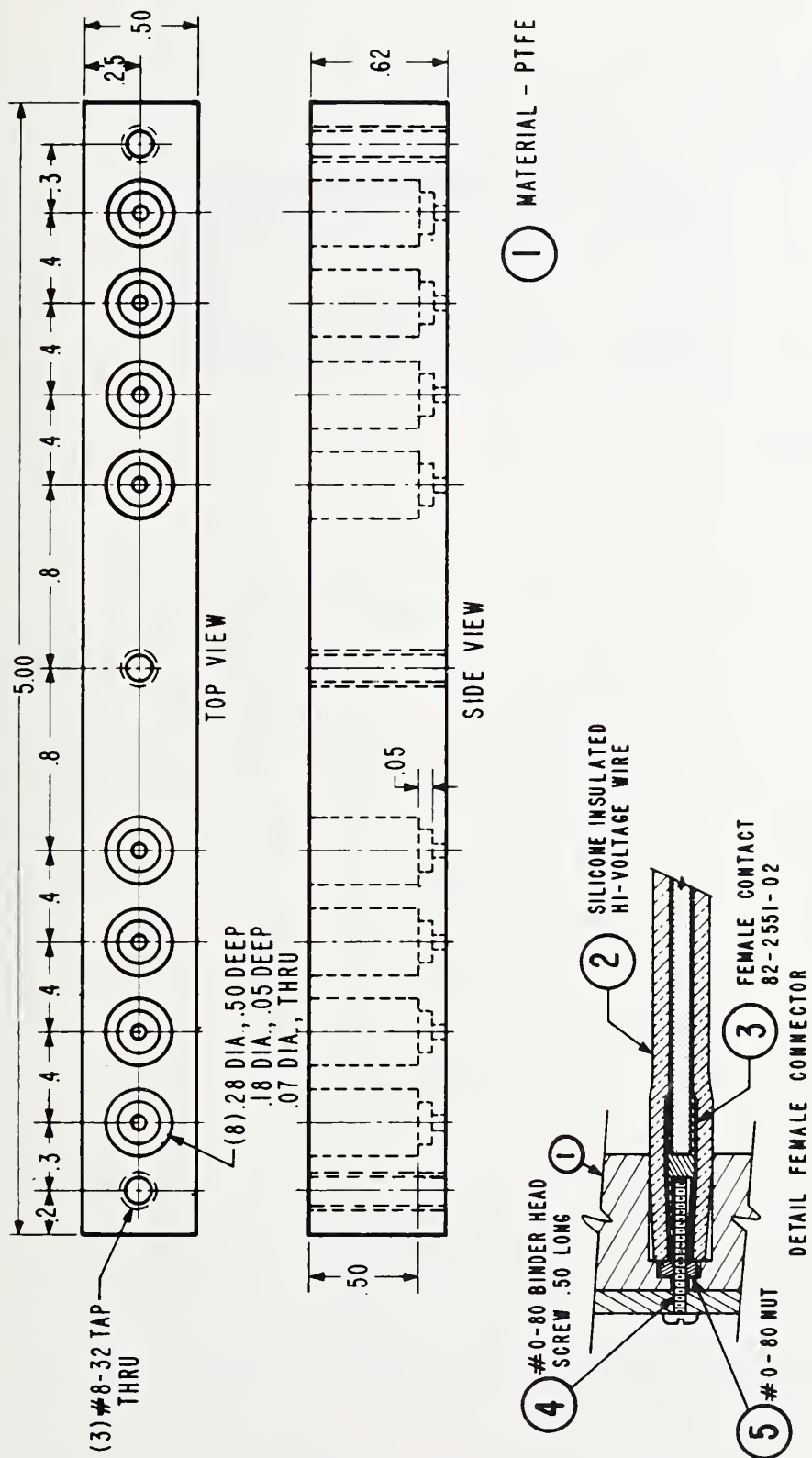


Figure MB6. HV connector assembly, HV amplifier module.

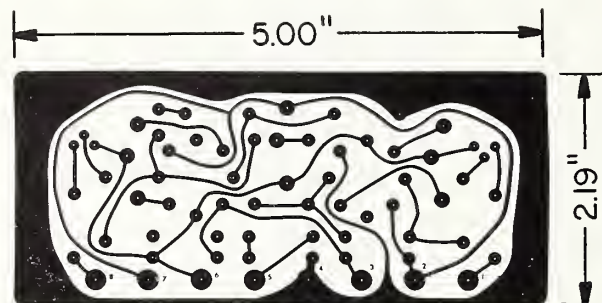


Figure MB7. Driver printed-circuit board, HV amplifier module.

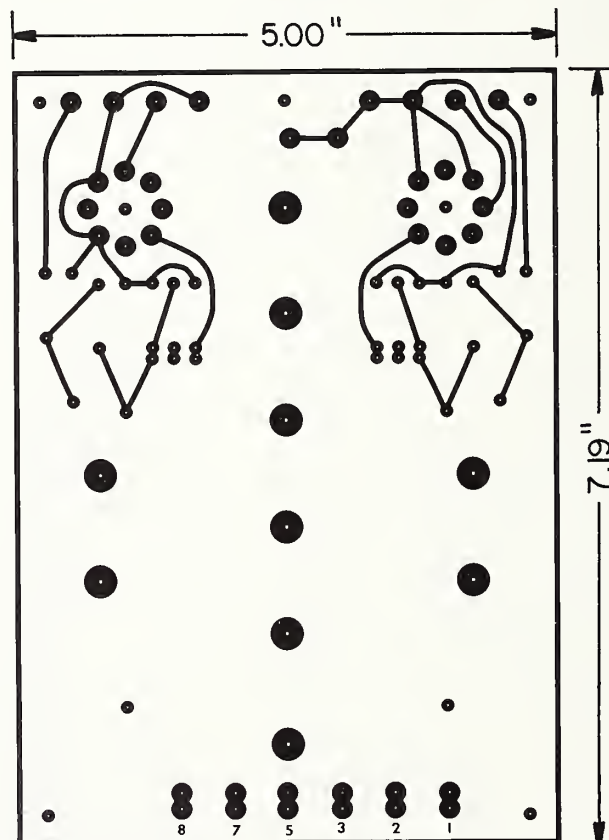
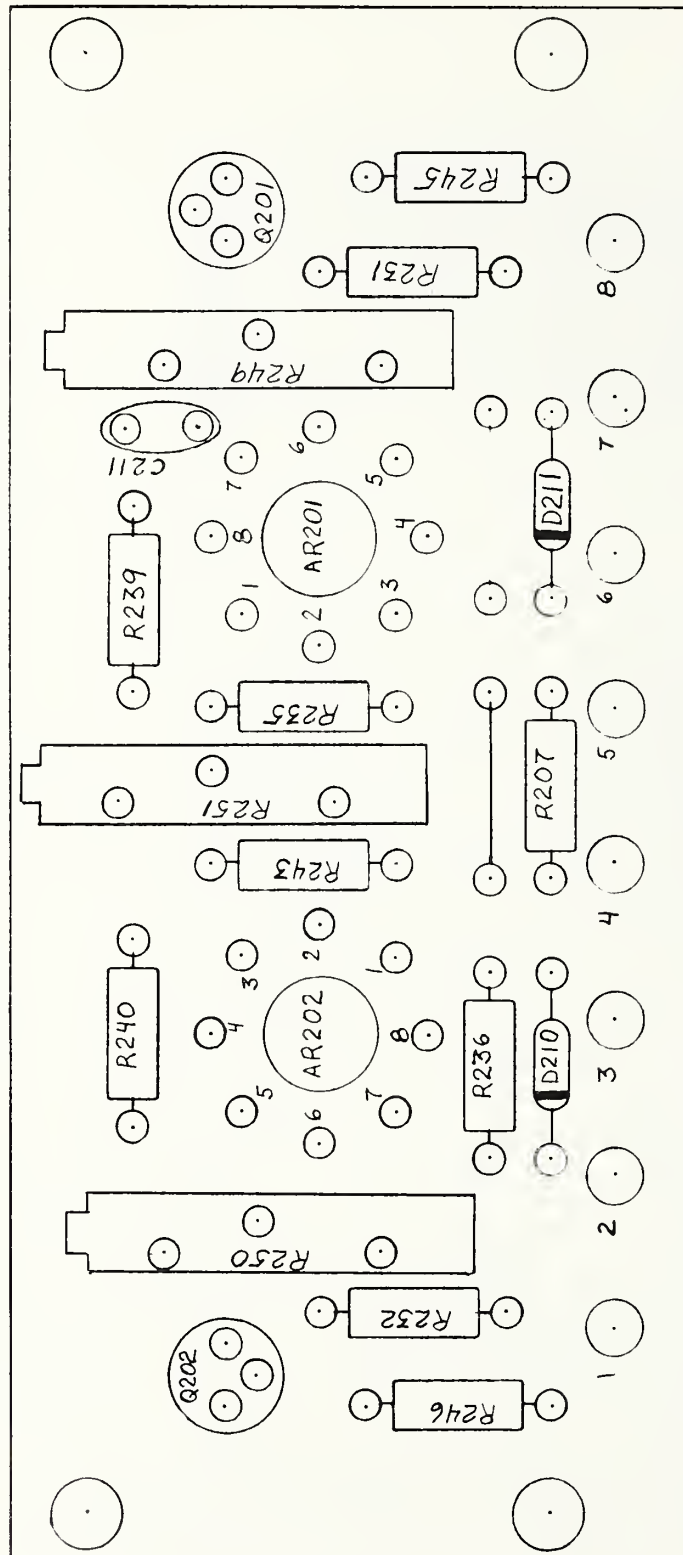


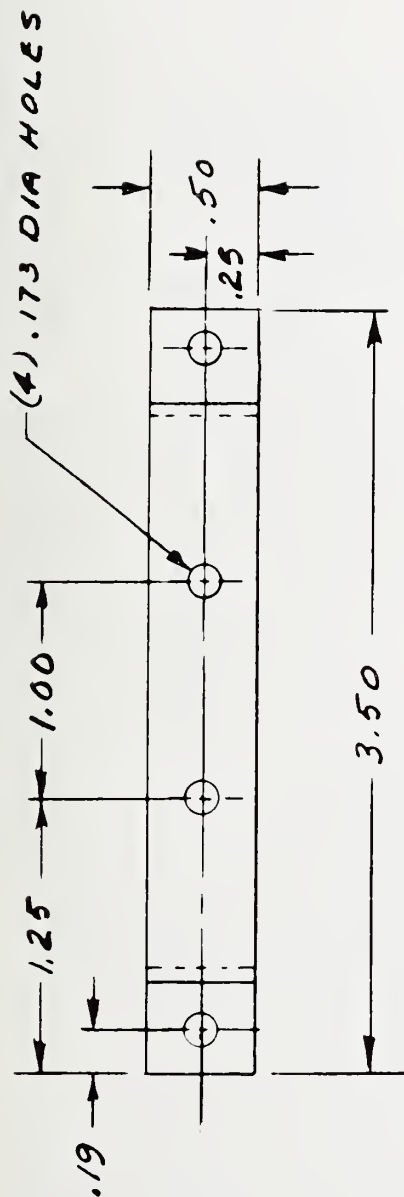
Figure MB8. HV amplifier printed-circuit board, HV amplifier module.



COMPONENT SIDE

NOTE: OTHER DRIVER BOARD IS IDENTICAL

Figure MB10. Driver board, HV amplifier module.



1 MATERIAL - $\frac{1}{16}$ " ALUMINUM

Figure MB11. Clamp for power supply PS 203

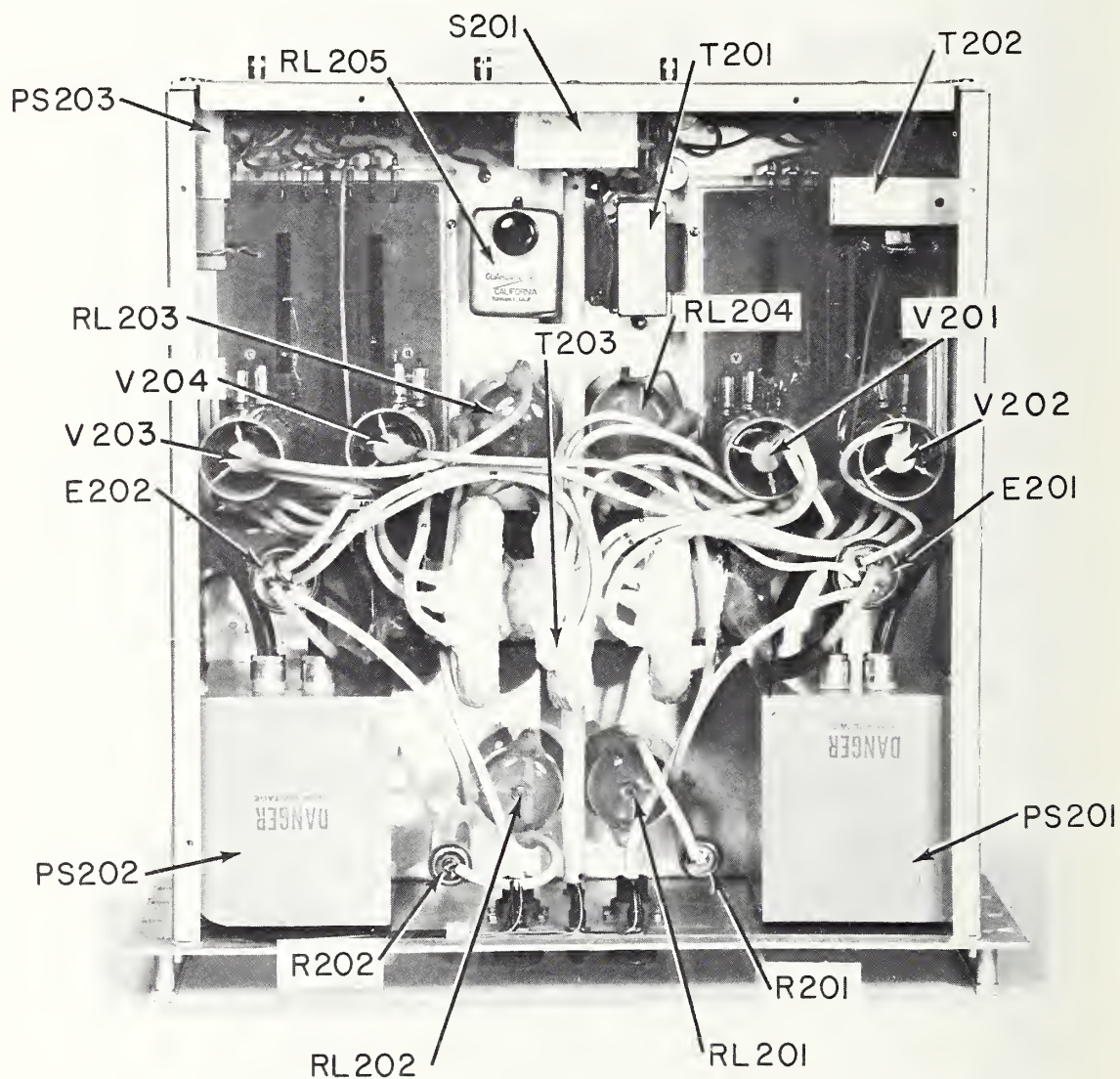


Figure B1. Top view of HV amplifier module with top cover removed.

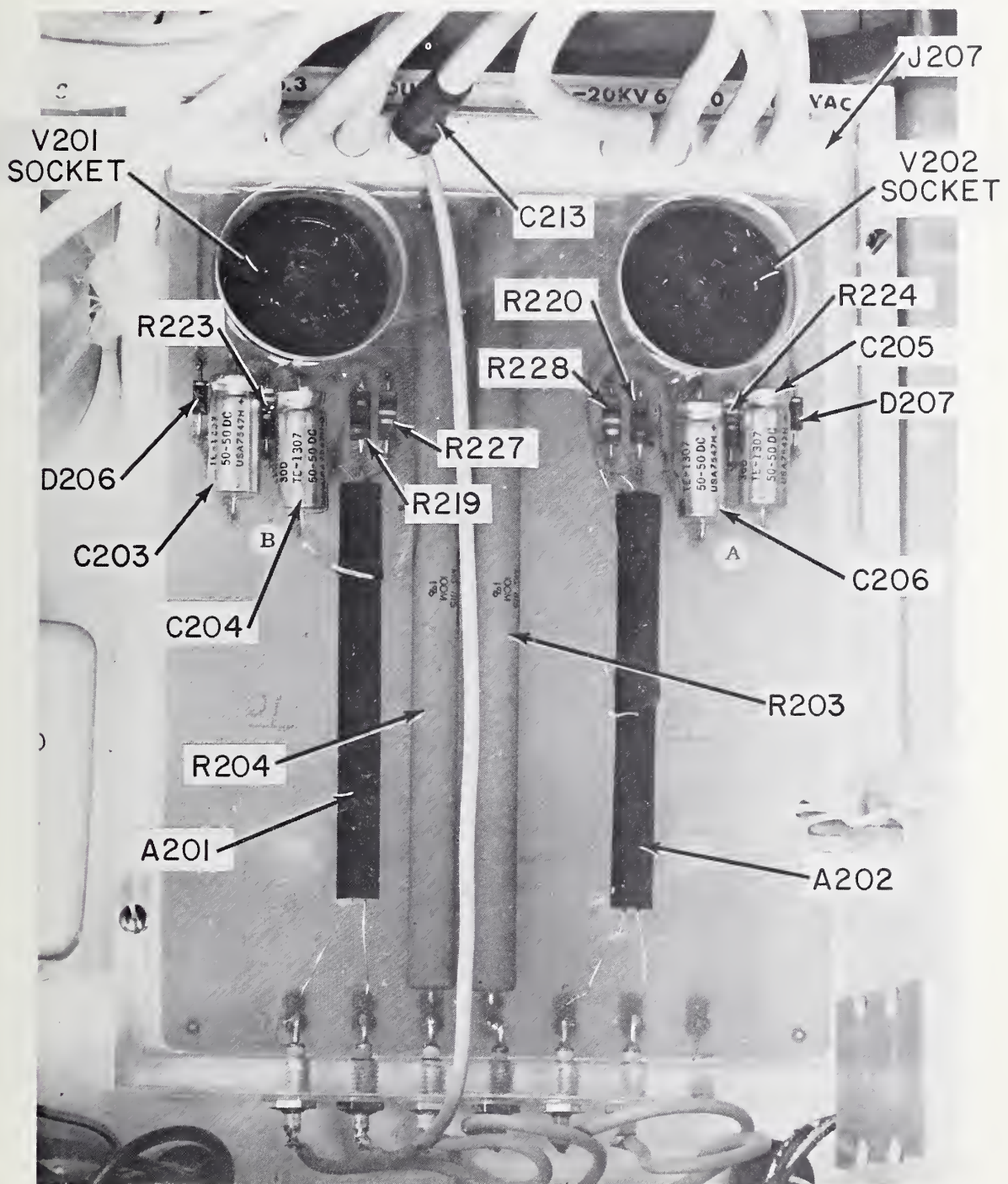


Figure B2. Top view of HV amplifier board.

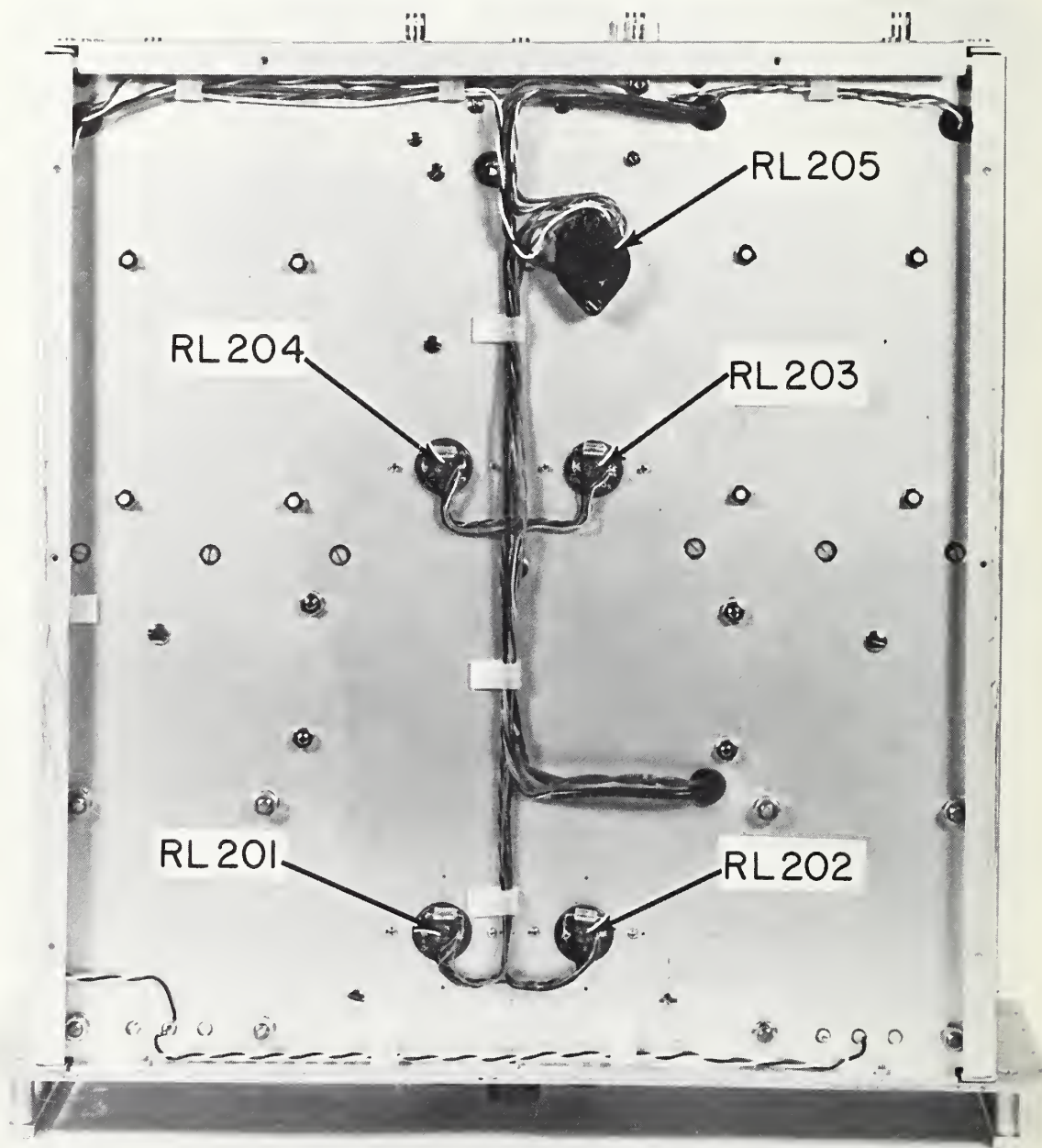


Figure B3. Bottom view of HV amplifier module with bottom cover removed.

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