NBS SPECIAL PUBLICATION 400-4

U.S. DEPARTMENT OF COMMERCE / National Bureau of Standards

Semiconductor Measurement Technology

Combined Quarterly Report

October 1, 1973 to March 31, 1974

NATIONAL BUREAU OF STANDARDS

The National Bureau of Standards [1] was established by an act of Congress March 3, 1901. The Bureau's overall goal is to strengthen and advance the Nation's science and technology and facilitate their effective application for public benefit. To this end, the Bureau conducts research and provides: (1) a basis for the Nation's physical measurement system, (2) scientific and technological services for industry and government, (3) a technical basis for equity in trade, and (4) technical services to promote public safety. The Bureau consists of the Institute for Basic Standards, the Institute for Materials Research, the Institute for Applied Technology, the Institute for Computer Sciences and Technology, and the Office for Information Programs.

THE INSTITUTE FOR BASIC STANDARDS provides the central basis within the United States of a complete and consistent system of physical measurement; coordinates that system with measurement systems of other nations; and furnishes essential services leading to accurate and uniform physical measurements throughout the Nation's scientific community, industry, and commerce. The Institute consists of a Center for Radiation Research, an Office of Measurement Services and the following divisions:

Applied Mathematics — Electricity — Mechanics — Heat — Optical Physics — Nuclear Sciences [2] — Applied Radiation [2] — Quantum Electronics [3] — Electromagnetics [3] — Time and Frequency [3] — Laboratory Astrophysics [3] — Cryogenics [3].

THE INSTITUTE FOR MATERIALS RESEARCH conducts materials research leading to improved methods of measurement, standards, and data on the properties of well-characterized materials needed by industry, commerce, educational institutions, and Government; provides advisory and research services to other Government agencies; and develops, produces, and distributes standard reference materials. The Institute consists of the Office of Standard Reference Materials and the following divisions:

Analytical Chemistry — Polymers — Metallurgy — Inorganic Materials — Reactor Radiation — Physical Chemistry.

THE INSTITUTE FOR APPLIED TECHNOLOGY provides technical services to promote the use of available technology and to facilitate technological innovation in industry and Government; cooperates with public and private organizations leading to the development of technological standards (including mandatory safety standards), codes and methods of test; and provides technical advice and services to Government agencies upon request. The Institute consists of a Center for Building Technology and the following divisions and offices:

Engineering and Product Standards — Weights and Measures — Invention and Innovation — Product Evaluation Technology — Electronic Technology — Technical Analysis — Measurement Engineering — Structures, Materials, and Life Safety [4] — Building Environment [4] — Technical Evaluation and Application [4] — Fire Technology.

THE INSTITUTE FOR COMPUTER SCIENCES AND TECHNOLOGY conducts research and provides technical services designed to aid Government agencies in improving cost effectiveness in the conduct of their programs through the selection, acquisition, and effective utilization of automatic data processing equipment; and serves as the principal focus within the executive branch for the development of Federal standards for automatic data processing equipment, techniques, and computer languages. The Institute consists of the following divisions:

Computer Services — Systems and Software — Computer Systems Engineering — Information Technology.

THE OFFICE FOR INFORMATION PROGRAMS promotes optimum dissemination and accessibility of scientific information generated within NBS and other agencies of the Federal Government; promotes the development of the National Standard Reference Data System and a system of information analysis centers dealing with the broader aspects of the National Measurement System; provides appropriate services to ensure that the NBS staff has optimum accessibility to the scientific information of the world. The Office consists of the following organizational units:

Office of Standard Reference Data — Office of Information Activities — Office of Technical Publications — Library — Office of International Relations.

---

[1] Headquarters and Laboratories at Gaithersburg, Maryland, unless otherwise noted; mailing address Washington, D.C. 20234.
[2] Part of the Center for Radiation Research.
[3] Located at Boulder, Colorado 80302.
[4] Part of the Center for Building Technology.

Semiconductor Measurement Technology

Combined Quarterly Report, October 1, 1973 to March 31, 1974

W. Murray Bullis, Editor

Electronic Technology Division
Institute for Applied Technology
National Bureau of Standards
Washington, D.C. 20234

Jointly Supported by:
The National Bureau of Standards,
The Defense Nuclear Agency, and
The Defense Advanced Research Projects Agency

U.S. DEPARTMENT OF COMMERCE, Frederick B. Dent, *Secretary*
NATIONAL BUREAU OF STANDARDS, Richard W. Roberts, *Director*

Issued November 1974

National Bureau of Standards Special Publication 400-4

Nat. Bur. Stand. (U.S.), Spec. Publ. 400-4, 101 pages (Nov. 1974)

CODEN: XNBSAV

U.S. GOVERNMENT PRINTING OFFICE
WASHINGTON: 1974

For sale by the Superintendent of Documents, U.S. Government Printing Office, Washington, D.C. 20402
(Order by SD Catalog No. C13.10:400-4). Price $1.70

TABLE OF CONTENTS

SEMICONDUCTOR MEASUREMENT TECHNOLOGY

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF FIGURES

PAGE

LIST OF FIGURES

LIST OF TABLES

PREFACE

The Semiconductor Technology Program serves to focus NBS efforts to enhance the performance, interchangeability, and reliability of discrete semiconductor devices and integrated circuits through improvements in measurement technology for use in specifying materials and devices in national and international commerce and for use by industry in controlling device fabrication processes. Its major thrusts are the development of carefully evaluated and well documented test procedures and associated technology and the dissemination of such information to the electronics community. Application of the output by industry will contribute to higher yields, lower cost, and higher reliability of semiconductor devices. The output provides a common basis for the purchase specifications of government agencies which will lead to greater economy in government procurement. In addition, improved measurement technology will provide a basis for controlled improvements in fabrication processes and in essential device characteristics.

The Program receives direct financial support principally from three major sponsors: the Defense Advanced Research Projects Agency (ARPA),* the Defense Nuclear Agency (DNA),† and the National Bureau of Standards (NBS).× The ARPA-supported portion of the Program, Advancement of Reliability, Processing, and Automation for Integrated Circuits with the National Bureau of Standards (ARPA/IC/NBS), addresses critical Defense Department problems in the yield, reliability, and availability of integrated circuits. The DNA-supported portion of the Program emphasizes aspects of the work which relate to radiation response of electron devices for use in military systems. There is considerable overlap between the interests of DNA and ARPA. Measurement oriented activity appropriate to the mission of NBS is a critical element in the achievement of the objectives of both other agencies.

Essential assistance to the Program is also received from the semiconductor industry through cooperative experiments and technical exchanges. NBS interacts with industrial users and suppliers of semiconductor devices through participation in standardizing organizations; through direct consultations with device and material suppliers, government agencies, and other users; and through periodically scheduled symposia and workshops. In addition, progress reports, such as this one, are regularly prepared for issuance in the NBS Special Publication 400 sub-series. More detailed reports such as state-of-the-art reviews, literature compilations, and summaries of technical efforts conducted within the Program are issued as these activities are completed. Reports of this type which are published by NBS also appear in the Special Publication 400 sub-series. Announcements of availability of all publications in this sub-series are sent by the Government Printing Office to those who have requested this service. A request form for this purpose may be found at the end of this report.

---

* Through ARPA Order 2397, Program Code 4D10 (NBS Cost Center 4259555).

† Through Inter-Agency Cost Reimbursement Order 74-811 (NBS Cost Center 4259522).

× Through Scientific and Technical Research Services Cost Centers 4251126, 4252128, and 4254115.

SEMICONDUCTOR MEASUREMENT TECHNOLOGY

COMBINED QUARTERLY REPORT
October 1, 1973 to March 31, 1974

Abstract: This combined quarterly progress report describes NBS activities directed toward the development of methods of measurement for semiconductor materials, process control, and devices. The emphasis is on silicon device technologies. Principal accomplishments during this reporting period include (1) identification of major problem areas in connection with measuring and inspecting photomasks, (2) development of a mathematical model suitable for interpreting thermally stimulated current and capacitance measurements on junction diodes and metal-oxide-semiconductor (MOS) capacitors, (3) completion of a preliminary evaluation of a method, based on the transient capacitance-voltage characteristic of an MOS capacitor, for measuring thickness of epitaxial layers up to 2 μm thick, and (4) development of criteria for use in nondestructive wire bond pull tests. Results are also reported on spreading resistance, capacitance-voltage, and carrier mobility measurements; polynomial fits for energy band gap and hole and electron effective masses in silicon; methods for characterizing oxide films; evaluation of sheet resistance and collector resistor test structures; evaluation of a photoresist spinner test; scanning electron microscopy; bonding of aluminum ribbon wire to thick film copper; bonding of platinum wire to thin film aluminum; leak rate calculations in the transition flow regime; transistor thermal response measurements; and radiation response of microwave mixer diodes. Supplementary data concerning staff, publications, workshops and symposia, standards committee activities, and technical services are also included as appendices.

Key Words: Boron redistribution; collector resistor; dopant profiles; effective mass; electrical properties; electron beam induced current mode; electronics; epitaxial layer thickness; flying spot scanner; gold-doped silicon; hermeticity; ion microprobe mass analysis; methods of measurement; microelectronics; microwave diodes; mobility; MOS devices; oxide films; photomasks; photoresist; platinum wire; resistivity; resistivity standards; ribbon wire; scanning electron microscopy; semiconductor devices; semiconductor materials; semiconductor process control; sheet resistance; silicon; spreading resistance; test patterns; thermal response; thermally stimulated capacitance; thermally stimulated current; thick film copper; voltage contrast mode; wire bonds; X-ray photoelectron spectroscopy.

1. INTRODUCTION

This is a report to the sponsors of the Semiconductor Technology Program on work during the twenty-second and twenty-third quarters of the Program. It summarizes work on a wide variety of measurement methods for semiconductor materials, process control, and devices that are being studied at the National Bureau of Standards. The Program, which emphasizes silicon-based device technologies, is a continuing one, and the results and conclusions reported here are subject to modification and refinement.

The work of the Program is divided into a number of tasks, each directed toward the study of a particular material or device property or measurement technique. This report is subdivided according to these tasks. Highlights of activity during the quarter are given in section 2. Subsequent sections deal with each specific task area. References cited are listed in the final section of the report.

INTRODUCTION

The report of each task includes a narrative description of progress made during this reporting period. Additional information concerning the material reported may be obtained directly from individual staff members identified with the task in the report. The organization of the Program staff and telephone numbers are listed in Appendix A.

Background material on the Program and individual tasks may be found in earlier quarterly reports as listed in Appendix B. From time to time, publications are prepared that describe some aspect of the program in greater detail. Current publications of this type are also listed in Appendix B. Reprints or copies of such publications are usually available on request to the author.

Communication with the electronics community is a critical aspect both as input for guidance in planning future program activities and in disseminating the results of the work to potential users. Formal channels for such communication occur in the form of workshops and symposia sponsored or co-sponsored by NBS. Currently scheduled seminars and workshops are listed in Appendix C. In addition, the availability of proceedings from past workshops and seminars is indicated in the appendix.

An important part of the work that frequently goes beyond the task structure is participation in the activities of various technical standardizing committees. The list of personnel involved with this work given in Appendix D suggests the extent of this participation. In most cases, details of standardization efforts are reported in connection with the work of a particular task.

Technical services in areas of competence are provided to other NBS activities and other government agencies as they are requested. Usually these are short-term, specialized services that cannot be obtained through normal commercial channels. To indicate the kinds of technology available to the Program, such services provided during the period covered by this report are listed in Appendix E.

2. HIGHLIGHTS

Particularly significant accomplishments during this reporting period include (1) identification of major problem areas in connection with measuring and inspecting photomasks, (2) development of a mathematical model suitable for interpreting thermally stimulated current and capacitance measurements on junction diodes and metal-oxide-semiconductor (MOS) capacitors, (3) completion of a preliminary evaluation of a method, based on the transient capacitance-voltage characteristic of an MOS capacitor, for measuring thickness of epitaxial layers up to 2 μm thick, and (4) development of criteria for use in nondestructive wire bond pull tests.

In addition, the second ARPA/NBS Workshop, on hermeticity, was held at NBS Gaithersburg. This workshop focussed on problems with correlation between various methods for testing semiconductor device packages for fine leaks, the lack of correlation between device failure and leaks in the fine leak range, and the need for an objective, quantitative test procedure for measuring leaks in the gross leak range. A separate report is being prepared on the discussions and conclusions of the workshop.

The following are highlights of these and other activities during this reporting period.

Resistivity; Dopant Profiles — An investigation was initiated to determine the relationships, if any, which exist between the surface morphology of the probe tips used for spreading resistance measurements and their electrical behavior. The junction capacitance-voltage technique was successfully applied to gated diodes formed by diffusing an n^+ layer into a uniformly doped p-type silicon wafer or epitaxial film. Mathematical analysis of the boron redistribution problem continued with the development of procedures for solving the appropriate equations by the method of heat potentials. Curves were calculated to relate the surface dopant density of a diffused layer to the sheet resistance-junction depth product, taking into account the penetration of the zero-bias space charge region into the diffused layer; this correction is important for films with sheet resistance in excess of 0.8 kΩ/□. In cooperation with ASTM Committee F-1 on Electronics, experimental work was undertaken to redetermine the relationships between resistivity, carrier density, and carrier mobility in silicon. In response to a request from the industry, a computer program was written to calculate dopant density as a function of silicon resistivity using empirical expressions for the relationship between carrier mobility and dopant density found in the literature. Polynomials were developed which describe the temperature dependence of the hole and electron masses and the energy band gap of silicon. An analysis was completed of procedures which can be used to eliminate misalignment or magnetoresistance voltages when calculating the Hall coefficient from measured values of the Hall voltage when the forward and reverse magnetic flux densities are not equal. A small-scale experiment, designed to test the ability of various laboratories to measure the probe force of pins mounted in a four-probe head, showed that for probe forces near 0.30 N the variability was in excess of that permitted by the requirements of the ASTM method for measuring sheet resistance on epitaxial silicon wafers.

Crystal Defects and Contaminants — A physical model has been developed and applied to the experimental results obtained for the dynathermal current and capacitance response of the gold acceptor center in silicon. This model satisfactorily predicts the shift in the thermally stimulated current characteristics with heating rate for the single peak in the case of a p-n junction and both peaks in the case of an n-MOS capacitor.

Oxide Film Characterization — An analysis was made of the errors which could arise in the capacitance measurement as a result of excessive loss due to high contact resistance on the backside, high series body resistance, or capacitance and conductance of a backside oxide in an MOS capacitor when measuring the capacitance-voltage characteristics. Studies of the bias-temperature stress test were begun; a prototype apparatus has been constructed and preliminary measurements made on an oxide layer fabricated in-house. Several techniques were examined for creating a shallow, uniformly sloped region through the oxidized surface of a silicon wafer; such a slope is necessary to make depth profile measurements with the ion microprobe mass analyzer. Preliminary study of the silicon-oxygen system by means of x-ray photoelectron spectroscopy (also known as electron spectroscopy for chemical analysis) revealed the presence of carbon near the surface. The origin of this carbon is being investigated in some detail in order to establish whether it is an artifact of the measurement or whether it comes from the specimen itself; should it be found to come from the surface or bulk of the specimen, it would be of considerable interest in connection with the operation of MOS devices.

HIGHLIGHTS

Test Patterns — The process previously used to fabricate gated p^+n junctions and n-MOS capacitors was modified by interchanging the emitter and base diffusions in order to fabricate gated n^+p junctions and p-MOS capacitors. A detailed analysis of the collector resistor test structure on test pattern NBS-2 revealed several possible limitations; five new structures have been designed and incorporated into a new test pattern in order to permit additional experiments which are expected to lead to a fuller understanding of the current patterns in collector resistor structures to be undertaken. A preliminary analysis was made of various four-terminal test structures for measuring sheet resistance of thin layers; a gated van der Pauw structure is being included in the new test pattern. Design work is nearing completion on another test pattern which includes a variety of charge-coupled devices as well as more conventional test structures.

Photolithography — In connection with the definition of a program to be undertaken in this area, visits were made to 26 device manufacturers, photomask and photoresist suppliers, and manufacturers of mask alignment or inspection equipment. Indications are that major problems exist in connection with standards for line width measurement and with procedures for edge definition, inspection of both masks and unexposed photoplates for defects, and alignment of a series of photomasks. Preliminary results of an analysis of the usefulness of absolute radiometric measurements to standardize and control photoresist exposure suggest that exposure control can be improved by the use of a light integrator, but that use of absolute radiometry would not be necessary. An evaluation was made of the repeatability of a method for measuring the rotational acceleration and velocity of a wafer during the spinning process used in photoresist coating; this method is being considered for adoption by ASTM Committee F-1 on Electronics.

Epitaxial Layer Thickness — To address a need expressed by the semiconductor device industry for methods of measuring the thickness of epitaxial layers less than 2 μm thick, a new method which makes use of the transient high-frequency capacitance-voltage characteristic of an MOS capacitor is being evaluated. This method, with some limitations, is applicable to the measurement of such thin layers when the layer and substrate are of the same conductivity type and when the substrate is much more heavily doped than the layer.

Wafer Inspection and Test — To prepare for the study of the extent of damage to microelectronic devices when examined in a scanning electron microscope, in connection with work toward non-contacting measurements on finished devices at the wafer level, measurements of the total electron beam current of the scanning electron microscope were made as a function of accelerating potential, condenser lens current, and objective lens current. In addition, a flying spot scanner is being assembled to evaluate electrical properties of devices before and after exposure to the electron beam. A cylindrical detector intended to increase the sensitivity of the scanning electron microscope in the voltage contrast mode was assembled and installed. Relatively simple relationships were developed between the carrier generation rate in an aluminum-silicon dioxide-silicon structure and the accelerating potential and the beam current of the scanning electron microscope to assist in predicting the magnitude of signals to be expected when examining MOS and bipolar devices in the electron beam induced current mode.

Interconnection Bonding — Experiments were completed which demonstrate that aluminum ribbon wire can be satisfactorily bonded to thick film copper conductors and used in typical hybrid circuit processing environments; thus, for many hybrid circuit applications it may be possible to replace gold thick films with less expensive copper thick films. On further investigation, it was found that the use of small diameter platinum wire in ultrasonic bonding to silicon device metallization is not likely to be satisfactory because of the occurrence of severe damage to the silicon wafer under the bond. A versatile instrument was built to pull beam lead devices or wire bonds made by either thermocompression or ultrasonic bonding techniques. Work was completed on the development of the metallurgical and statistical rationales for a nondestructive wire bond pull test and the determination of maximum permissible force limits applicable for a wide variety of wire sizes, both hard drawn and annealed. Destructive double-bond pull tests, conducted on a number of power devices bonded with large diameter annealed aluminum wire, revealed that the principal failure mode is breakage in the wire span and that the electrical discharge weld made to the gold plated post often forms at the perimeter of the bond in the same manner as was observed previously for ultrasonic bonds made with small diameter aluminum wire. A preliminary evaluation was made of a technique

for directly observing the bond formed between small diameter aluminum wire and aluminum metallization deposited on glass slides. Mathematical modeling of the motion of an ultrasonic wire bonding tool was undertaken to determine the mechanisms by which the metallurgical weld is formed and to lay the basis for a quantitative in-process bond monitoring scheme.

Hermeticity — ASTM Committee F-1 on Electronics was assisted in prepairing a final draft procedure and schedule for the interlaboratory evaluation of the helium mass spectrometer method for testing fine capillary leaks in large volume containers. A sensitive mass spectrometer was designed and is being constructed to evaluate the use of this type of instrumentation for the measurement of trace elements in the semiconductor processing environment and on wafer surfaces as well as for the investigation of gas flow mechanisms in leaks in hermetic packages. Initial calculations were made of gas flow in leaks of a size likely to be encountered in semiconductor device packages; these calculations, which took into account both the molecular flow and laminar viscous flow mechanisms, verified the need for more realistic examination of flow mechanisms and their effect on the relationship between indicated leak rate and true leak rate. A novel procedure for a dry, quantitative gross leak test was conceived and is being evaluated.

Thermal Properties of Devices — The transient thermal response of power semiconductor devices as measured by both the pulsed heating curve technique and the cooling curve technique was studied. It was found both experimentally and theoretically that the cooling curve technique, which is more widely used because of its simplicity, is equivalent to the pulsed heating curve technique, which more closely simulates the response of interest in an application, only under idealized conditions. In general, the cooling curve technique was found to give a larger value for thermal impedance than that which would be obtained under actual single pulse operating conditions.

Microwave Diodes — As an outgrowth of the development of precise methods for characterizing the properties of X-band mixer diodes, a preliminary assessment was made of the response to gamma and neutron irradiation of Schottky-barrier diodes designed as direct replacements for military grade 1N23 point-contact diodes. No significant permanent damage effects were observed at gamma dosages up to 10^7 rads (Si) and neutron fluences up to 10^{15} cm^{-2}. Small effects were observed at neutron fluences of about 5×10^{-15} cm^{-2}.

Dissemination Activities — Organizational activities were completed for the Workshop on Radiation Effects in MOS Technology. This workshop co-sponsored the IEEE Nuclear and Plasma Sciences Society, the IEEE Electron Devices Group, and NBS, was held December 6 and 7, 1973 in Washington. No proceedings of this workshop were printed.

Planning activity was completed for the Spreading Resistance Symposium, scheduled for June 13 and 14, 1974, at NBS Gaithersburg. This symposium is being jointly sponsored by ASTM Committee F-1 on Electronics and NBS. The proceedings, which will include summaries of discussion at the meeting, will be made available as an NBS Special Publication.

Test patterns were selected as the subject of the third ARPA/NBS Workshop scheduled for September 6 in Scottsdale, Arizona following the fall meeting of ASTM Committee F-1. This workshop, which is a logical follow-on to a mini-symposium on test patterns held as part of the January meeting of the Committee, will discuss MOS and bipolar test structures and acquisition systems for test structure data from both production and laboratory view points.

3. RESISTIVITY; DOPANT PROFILES

3.1. Spreading Resistance Methods

While continuing the development of a calibration curve for the spreading resistance instrument on *p*-type silicon slices (NBS Tech. Note 806, pp. 9-10) erratic behavior was encountered in the instrument. This behavior was manifested by variability greater than 10 percent in the spreading resistance during periodic tests on a 2-Ω•cm, chem-mechanically polished, *p*-type reference slice. Although this variability was thought to be due to changes in the operating characteristics of the probe tips, it could not be remedied by running about 1000 probe impressions on a lapped silicon surface, a simple technique which had previously proven successful in clearing up erratic probe behavior. Consequently, a variety of probe tips was examined microscopically and electrically to determine the nature of both good and bad tips and the relationships, if any, between tip surface morphology and electrical behavior.

In the initial investigation, styli consisting of various osmium or tungsten carbide alloys, acquired from various suppliers, and having radii of curvature from about 19 to about 250 μm were mounted for use as spreading resistance probes. Most styli were tested as supplied by the manufacturer with the exception of two which had been conditioned by running 2000 to 4000 impressions on a lapped silicon surface to yield stable spreading resistance measurements and two on which such conditioning had been attempted but which failed to yield probes adequate for spreading resistance measurements.

To test the electrical characteristics of the probes, spreading resistance measurements were made on the *p*-type reference slice used in the calibration curve development effort to verify probe stability. A range of 600 to 1000 Ω has been found previously to be typical of the response of a good probe on this reference slice. The probes tested yielded values from about 500 Ω to values between 10^6 and 10^8 Ω. This latter range of response included one stylus with a nominal radius of 25 μm, two with a nominal radius of 125 μm, and one with a nominal radius of 250 μm. On these four probes, no conditioning had been attempted.

Scanning electron micrographs were then taken of the various probe tips at a magnification of about 1000 X and of the damage tracks left in a polished silicon surface by these probes at a magnification of about 4000 X. Also differential interference optical photomicrographs were taken of the probe damage tracks. No damage mark was visible on a polished silicon surface under either scanning electron or differential interference optical microscopy for any of the four probes which yielded electrical resistance values above 10^6 Ω. In most cases the surface of the stylus tip was rather flat, perhaps 80 percent consisting of the alloy and 20 percent being small voids. A typical example is the scanning electron micrograph of one of the 125 μm radius tips shown in figure 1.

With exception of one osmium stylus with a radius of 50 μm which had a relatively smooth surface and reasonably low resistance, the rougher or more granular the surface of the probe, the lower was the measured spreading resistance. The ability of a rougher probe to form a number of individual microcontacts appears to enhance its ability to make a relatively low resistance contact. In fact after a very light abrasion of the other 125 μm radius tip with fine aluminum oxide paper, the surface was greatly roughened as shown in figure 2 and the contact resistance dropped to the range 650 to 800 Ω.

In addition to low contact resistance, it is also desirable to have a contact with well defined geometry, preferably circular and compact, to aid in analytical modeling of the potential distribution beneath the contact. Furthermore, under some conditions a probe can fracture and otherwise damage the silicon surface to a depth which can complicate the interpretation of measurements of depth profiles in thin layers or in multilayered structures. Differences in probe impression characteristics are frequently not visible in Nomarski optical photomicrographs of the probe imprint but they can be seen in scanning electron micrographs under much greater magnification. Imprints of two probes with about the same contact resistance are shown in figure 3. The Nomarski optical photomicrographs of the imprints are quite similar while the scanning electron micrographs shown significant differences. The conchoidal fracture and related damage in the scanning electron micrograph of figure 3d may cause electrical punch through of thin layers and may complicate or even invalidate the results of measurements of depth profiles of thin layers or of multilayered structures. Sin damage of this type is not visible optically, it may be necessary to develop a thin film reference structure for use in verifying that a given set of probes is making electrical con tact only to the surface layer of the specimen. (J. R. Ehrstein)

Figure 1. Scanning electron micrograph of tip of an unconditioned tungsten carbide spreading resistance probe with a nominal radius of 125 μm. (Magnification: ∿ 1000 X).

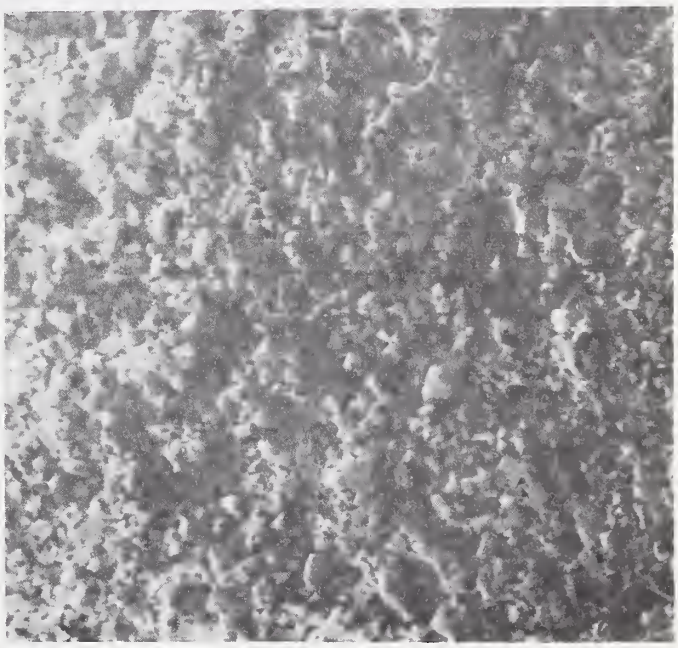
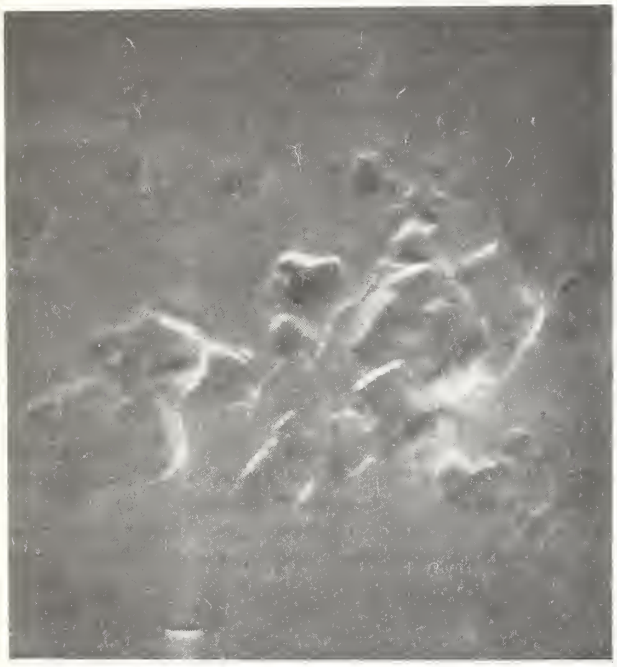


Figure 2. Scanning electron micrograph of a lightly abraded tungsten carbide spreading resistance probe with a nominal radius of 125 μm. (Magnification: ∿ 1000 X).

a. Nomarski photomicrograph, Probe MSF, Magnification: ∿ 850 X.

b. Nomarski photomicrograph, Probe 1WKA-1, Magnification: ∿ 850 X.



c. Scanning electron micrograph, Probe MSF, Magnification: ∿ 6400 X.

d. Scanning electron micrograph, Probe 1WKA-1 Magnification: ∿ 6400 X.

Figure 3. Imprints of two spreading resistance probes with about the same contact resistance.

3.2. Junction Capacitance-Voltage Method

Experimental investigation of the junction capacitance-voltage (C-V) method, previously directed toward understanding of measurements on n-type silicon (NBS Tech. Note 788, pp. 9-11), was extended to measurements on p-type silicon wafers. Measurements on p-type silicon are generally more difficult because the surface of the wafer can be inverted due to positive charge in the oxide. In addition, the surface region is frequently depleted of dopant because of boron redistribution during oxidation.

Gated n^+p diodes were fabricated (see sec. 6.1.) in 11 p-type bulk or epitaxial wafers using test pattern NBS-2 (NBS Tech. Note 788, pp. 15-17). The diodes were about 0.5 mm (20 mils) in diameter, the diffused layer sheet resistance was about 3.5 Ω/□, and the junction depth was about 2.7 μm. Capacitance-voltage measurements were made on one diode on each wafer with the gate biased at the flat band potential as determined from C-V measurements on an MOS capacitor located near the n^+p diode. The diodes measured were located near the center of the wafer except that an off-center diode was measured on wafer 3001 which had been broken.

The junction capacitance was measured in the dark at room temperature with a capacitance meter having a test signal of 15 mV rms at 1 MHz at reverse biases ranging from about 2 V to

a maximum value V_{max} limited by the junction breakdown voltage. Each succeeding voltage was chosen to cause the capacitance to decrease by about 10 percent from the preceding value. Dopant density profiles were then calculated from adjacent C-V pairs, taking into account both peripheral and diffused layer effects [1].

The results of these measurements are shown in table 1 where $\bar{N}$ is the average dopant density and s is the relative sample standard deviation of each profile. Also shown in table 1 are the number of C-V pairs used in the computation, the maximum applied reverse bias, V_{max}, and the flat-band voltage, V_{fb}. The dopant profiles for the wafers are quite flat; only one of the profiles had a relative sample standard deviation greater than 2 percent. The gold-doped wafers had a gold density of only about 10^{13} cm^{-3} which is small enough that it did not affect the profiles. It should be noted that flat profiles were achieved even though the flat-band voltage ranged from -0.5 to -12.6 V.

(R. L. Mattis and M. G. Buehler)

3.3. Mathematical Models of Dopant Profiles

A mathematical model was developed for use in solving the problem of redistribution of boron in silicon during thermal oxidation and diffusion. Mathematically stated, the redistribution problem consists of finding the solution to a pair of partial differential equations which are coupled through their boundary conditions. A reformulation of this mathematical problem was effected by using the method of heat potentials [2,3], so that instead of solving the partial differential equations one need only solve a more tractable system of integral equations.

The mathematical model is built on an extension of the physical model described previously (NBS Spec. Publ. 400-1, pp. 9-11). In the physical model, two domains, the oxide and the silicon, were defined. In the extension, the oxide thickness before oxidation ($t<0$) may be either zero or nonzero. The oxide domain covers the region $0<z<z_0(t)$, $t\geq 0$, where z is a moving coordinate system referenced to the front surface of the oxide and $z_0(t)$ is the total oxide thickness. The silicon domain in the extension of the physical model is bounded, $y_0(t)<y<L$, $t\geq 0$, where y is the laboratory coordinate system referenced to the original front surface of the silicon (i.e., $y_0(0) = 0$), $y_0(t)$ is the oxide-silicon interface, and L is the thickness of the silicon wafer (assumed in the previous formulation to be semi infinite, i.e., $L\to\infty$). The oxide thickness is assumed to increase parabolically with time: $z_0(t) = z_0(0) + At^{1/2}$. The ratio of the thickness of silicon consumed during oxidation to the increase in oxide thickness is assumed constant: $y_0(t)/[z_0(t) - z_0(0)] = \alpha$. The two coordinate systems are related by: $z - z_0(t) = y - y_0(t)$, and the origin of the z-axis is convected away from the original silicon surface with a time dependent velocity, $(1 - \alpha)A/2t^{1/2}$. In a third extension of the original model the initial boron distribution in both the oxide and the silicon may vary with position.

Following the method of heat potentials, the density of boron in the oxide, $C_1(z,t)$, and the density of boron in the silicon, $C_2(y,t)$ are defined by sums of four integral expressions. These expressions contain only two unknown functions, $Q(\tau)$ and $R(\tau)$. When $Q(\tau)$ and $R(\tau)$ satisfy two appropriate Volterra-type integral equations, it can be shown that $C_1(z,t)$ and $C_2(y,t)$ satisfy the diffusion equations

$$\frac{\partial C_1(z,t)}{\partial t} = D_1 \frac{\partial^2 C_1(z,t)}{\partial z^2} \qquad \text{(in the oxide)}$$

and

$$\frac{\partial C_2(y,t)}{\partial t} = D_2 \frac{\partial^2 C_2(y,t)}{\partial y^2} \qquad \text{(in the silicon)}$$

with the initial conditions

Table 1 — Summary of p-Type Dopant Density Profiles, Run No. 2.5

Specimen No.	Wafer	$\bar{N}$, cm^{-3}	s, %	Number of CV Pairs	V_{max}, V	V_{fb}, V
3001	Bulk	1.41×10^{15}	0.86	14	46.6	-6.0
3002	Bulk	1.56	0.84	13	41.5	-12.6
3003	Bulk	1.44	0.67	13	40.5	-10.4
3004	Bulk Au-doped	1.39	1.06	14	48.5	-7.4
3005	Bulk Au-doped	1.50	1.31	14	43.3	-4.0
3006	Bulk Au-doped	1.41	1.49	14	43.3	-2.5
4001	Epi	0.73	1.82	12	27.0	-6.5
4002	Epi	0.79	1.85	12	30.4	-6.3
4003	Epi	1.47	2.60	14	41.0	-5.0
4004	Epi Au-doped	1.43	1.06	14	51.9	-1.9
4006	Epi Au-doped	1.42	1.17	15	55.5	-0.5

$$C_1(z,0) = C_{b1}(z), \quad (0 \leq z \leq z_0(0))$$

and

$$C_2(y,0) = C_{b2}(y), \quad (y_0(0) \leq y \leq L)$$

and, for $t>0$, the boundary conditions

$$C_1(0,t) = C_s(t)$$

$$C_2(y_0(t),t) = m\, C_1(z_0(t),t)$$

$$(m\alpha - 1)\, C_1(z_0(t),t)\, \frac{\partial z_0(t)}{\partial t} = D_1 \left.\frac{\partial C_1(z,t)}{\partial z}\right|_{z = z_0(t)} - D_2 \left.\frac{\partial C_2(y,t)}{\partial y}\right|_{y = y_0(t)}$$

$$C_2(L,t) = C_L(t)$$

where D_1 and D_2 are the diffusion coefficients of the boron in silicon dioxide and silicon, respectively; C_s is the density of boron at the front surface of the oxide, C_{b1} and C_{b2} are the initial densities of boron in the oxide and in the silicon, respectively, and m is the segregation coefficient of boron.

The two Volterra-type integral equations are too complicated to solve analytically in situations of practical interest, so they are being solved numerically [4]. First, the continuous variable τ is replaced by n uniformly spaced grid points $\{\tau_j\}$ with $j = 1, 2, 3, \ldots, n$. One then evaluates each integral equation at each grid point, τ_j. The indefinite integrals in the equations are replaced by finite sums by employing a quadrature rule, using the set $\{\tau_j\}$ as node points. In the usual case, the result is a solvable system of 2n equations in the 2n unknowns $Q(\tau_j)$ and $R(\tau_j)$.

However, these Volterra-type equations differ in two significant ways from the type of equations usually encountered. The first difference is that the kernels of the present

equations are singular. Special care must be taken when quadrature techniques are applied to integrals with such kernels. In the present case, product integral quadrature techniques [5] are being used.

The other unusual aspect of these integral equations occurs because the time derivative of $Q(\tau)$ appears in an integral in addition to the functions $Q(\tau)$ and $R(\tau)$. Consequently, it is more convenient to use Haber's method [6] to solve the system of integral equations. In Haber's method one does not solve directly for the $Q(\tau_j)$ and $R(\tau_j)$. Instead it is assumed that $Q(\tau)$ and $R(\tau)$ are piecewise linear in each interval $[\tau_j, \tau_{j+1}]$ for $j = 1, 2, 3, \ldots, n\ 1$. Thus, for the interval $\tau_j \geq \tau \geq \tau_{j+1}$,

$$Q(\tau) \equiv Q(\tau_j) + A_Q(\tau_j)(\tau - \tau_j) \tag{1}$$

and

$$R(\tau) \equiv R(\tau_j) + A_R(\tau_j)(\tau - \tau_j), \tag{2}$$

where the slopes $A_Q(\tau_j)$, $A_R(\tau_j)$, $j = 1, 2, 3, \ldots, n - 1$ are unknown. When these piecewise linear approximations are substituted for $Q(\tau)$ and $R(\tau)$ in the integral equations and these integral equations are then made discrete, as described above, there results a solvable, linear algebraic system of equations in the $2(n - 1)$ unknown slopes $A_Q(\tau_j)$ and $A_R(\tau_j)$. Once the values of these slopes are known the originally sought after values of $Q(\tau_j)$ and $R(\tau_j)$ can be recovered from eqs (1) and (2). The initial values, $Q(\tau_1)$ and $R(\tau_1)$, follow immediately from evaluating the Volterra equations at $\tau = \tau_1$. A computer program employing these procedures has been written in FORTRAN IV. (S. R. Kraft* and M. G. Buehler)

3.4. Diffused Layer Sheet Resistance

In the fabrication of semiconductor devices it is common practice to obtain the surface dopant density, N_0, of a diffused layer from the measurement of the diffused layer sheet resistance, R_s; the junction depth, X_j; the background dopant density, N_b; and an assumed functional form for the diffused layer. Previously (NBS Spec. Publ. 400-1, pp. 11-14) curves of N_0 as a function of $R_s X_j$ were developed for both *p*- and *n*-type Gaussian diffused layers with various values of N_b. In developing these curves the entire diffused layer was assumed to be conducting; restricted conduction due to the penetration of the space-charge region into the layer was not considered. It is shown here that this effect becomes important for shallow junction depths and high sheet resistance values.

The problem is illustrated in figure 4 where the true surface dopant density, $N_0(A_0 \neq 0)$, takes into account the penetration of the zero-bias space charge region A_0 into the diffused layer. In a usual calculation, A_0 is taken to be zero, and the apparent surface dopant density, $N_0(A_0=0)$, is calculated. The ratio $N_0(A_0 \neq 0)/N_0(A_0=0)$, calculated at various R_s and N_b values, is shown in figure 5 for a *p*-type Gaussian layer with a 0.1 μm junction depth.

The procedure for computing the values shown in figure 5 is as follows. First, values for X_j, N_b, and N_0 are assumed for a Gaussian diffusion. Then A_0 is found numerically [1] by equating the total junction potential (eq (12), ref 1) to the Boltzmann relation for the built-in voltage (eq (13), ref 1) while satisfying Gauss' law for the junction (eq (5), ref 1). Next, the true sheet resistance is calculated from the surface to A_0 from the expression:

---

*NBS Applied Mathematics Division

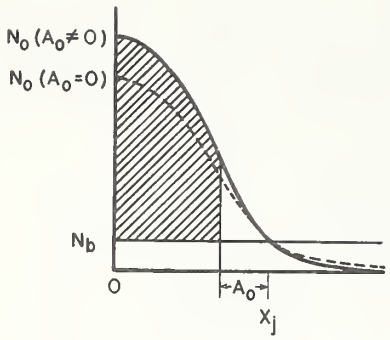


Figure 4. Dopant density profile of a diffused layer showing true $[N_0(A_0 \neq 0)]$ and apparent $[N_0(A_0 = 0)]$ surface dopant density.

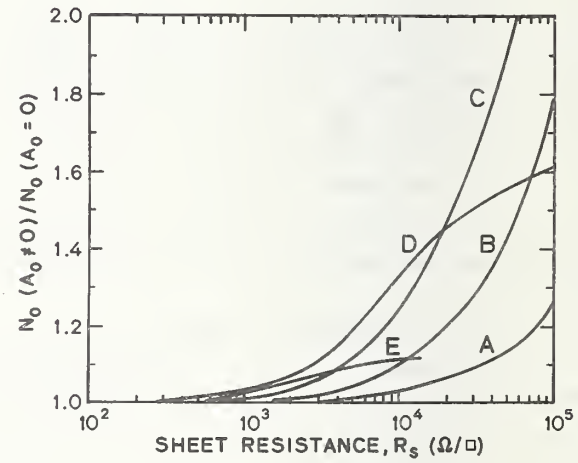


Figure 5. Ratio of true to apparent surface dopant density of a p-type Gaussian diffused junction, 0.1 μm deep, as a function of sheet resistance, for various values of background dopant density, N_b. (A: $N_b = 10^{14}$ cm^{-3}; B: $N_b = 10^{15}$ cm^{-3}; C: $N_b = 10^{16}$ cm^{-3}; D: $N_b = 10^{17}$ cm^{-3}; E: $N_b = 10^{18}$ cm^{-3}).

$$R_s^{-1} = q \int_0^{A_0} \mu(N - N_b)dx \ , \tag{3}$$

where q is the electronic charge, μ is given by [7]:

$$\mu = 47.7 + \left\{ 447 \Big/ \left[1 + \left(\frac{N + N_b}{1.9 \times 10^{17}} \right)^{0.76} \right] \right\}$$

(in square centimetre per volt second with dopant density given in inverse cubic centimetre), $N = N_0 \exp(-x^2/L^2)$, and $L = X_j[\ell n(N_0/N_b)]^{1/2}$. Finally the apparent surface dopant density is computed numerically from eq (3) using the true sheet resistance as calculated above but now assuming $A_0=0$.

The curves shown in figure 5 indicate that the effect on the surface dopant density is greater than 4 percent for sheet resistances above 1 kΩ/□. This range of values is important for high value resistors which have sheet resistance values ranging from 0.8 to 11 kΩ/□ [8]. Other junction depth values have been studied namely, 0.05 and 0.2 μm. For these values the curves are similar to figure 5, for the curves are not strongly dependent on X_j values.

(T. E. Griffin and M. G. Buehler)

3.5. Reevaluation of Irvin's Curves

Irvin's curves [9], which relate the resistivity of both *n*- and *p*-type silicon to the density of dopant atoms, have been been widely used by the semiconductor industry during the past decade. There are various reasons to believe that the relationships for present day silicon deviate significantly from these curves in some regions (NBS Tech. Note 806, pp. 20-23). In particular, recent data on boron-doped silicon [7] are different from the data, mostly developed from measurements on gallium-doped silicon, used by Irvin to derive his curve for *p*-type silicon. In addition, uncertainties still remain in connection with the degenerate (heavily-doped) region for silicon of both conductivity types.

In conjunction with the Mobility Section of ASTM Committee F-1 on Electronics, a plan to reevaluate Irvin's curves has been established. Preliminary junction C-V*, Hall effect, and four-probe resistivity measurements were made on a group of boron-doped silicon wafers under the auspices of the Mobility Section. The data are plotted in figure 6 with the curves of Irvin [9] and Wagner [7]. All of the experimental measurements were made at a temperature of 25 ± 2°C; the curves are for a temperature of 300 K (26.9°C). The resistivity, directly measured by the four-probe method is plotted as a function of ionized dopant density as determined by junction C-V (circles) or Hall effect (squares) measurements. In the latter, the scattering factor r, used to obtain the ionized doping density from the Hall coefficient, was taken from Runyan [10]. Care was taken to cut Hall bars from the center of a wafer where the four-probe resistivity measurement was made. Uniformity of the resistivity was checked by four-probe measurements at one-half radius positions; radial variations of less than 2 percent were observed in all cases. The resistivity was also measured on the Hall bar and the values were within 2 percent of those obtained by the four-probe technique. Several of the wafers from which Hall bars were cut were from the same lot as those used for the capacitance-voltage measurements.

The abscissa for the curves of Irvin and Wagner is the total dopant density rather than the ionized density. At high impurity densities some of the impurity atoms may not be ionized so that a departure of the data points from the curves would not be surprising. Nevertheless, at present it must be concluded that the experimental data are in much better agreement with Wagner's curve than with Irvin's. (W. R. Thurber and M. G. Buehler)

3.6. Computer Program to Calculate Dopant Density from Resistivity

Frequently it is desired to know the dopant density corresponding to a given value of silicon resistivity. The conversion can be done graphically by reference to the curves of Irvin [9] which have traditionally been used to relate resistivity to dopant density. However, for greater precision and convenience, it is useful to have an analytical procedure for the conversion which can be used in computer calculations. To meet this need a BASIC language [11] program was written to solve the equation which relates dopant density to resistivity. This equation can be written as follows:

$$N - \frac{1}{\rho q \mu(N)} = 0 \qquad (4)$$

where N is the dopant density, ρ is the resistivity, q is the electron charge, and $\mu(N)$ is the carrier mobility which is a function of the dopant density. The mobility equation used for *n*-type silicon is an empirical expression obtained by Caughey [12] to fit Irvin's curve. It is

$$\mu = \mu_{min} + (\mu_{max} - \mu_{min})/[1 + (N/N_{ref})^{\alpha}] \qquad (5)$$

where $\mu_{min} = 65$ cm^2/V·s, $\mu_{max} = 1330$ cm^2/V·s, $N_{ref} = 8.5 \times 10^{16}$ cm^{-3}, and $\alpha = 0.72$.

---

*The junction C-V and some of the four-probe measurements were made by B. L. Morris, Bell Telephone Laboratories, Allentown, Pa. 18103.

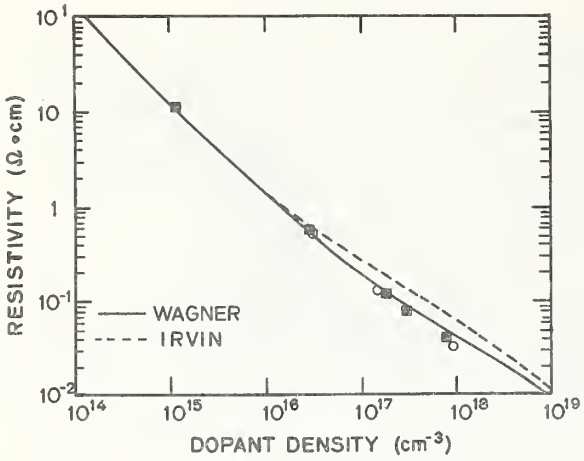


Figure 6. Resistivity as a function of dopant impurity density for p-type silicon. (The data points shown as circles were obtained from capacitance-voltage and four-probe resistivity measurements and the points shown as squares were derived from Hall effect and four-probe resistivity measurements. The curves are taken from the work of Irvin [9] and Wagner [7].)

The mobility equation for p-type silicon is from the work of Wagner [7] on boron-implanted implanted silicon. The expression is of the same form as eq (5), with the constants $\mu_{min} = 47.7$ cm^2/V•s, $\mu_{max} = 495$ cm^2/V•s, $N_{ref} = 1.9 \times 10^{17}$ cm^{-3}, and $\alpha = 0.76$.

The mobility equations were derived with the assumption that the carrier density is the same as the dopant density. This may not be the case at high dopant densities because of incomplete ionization of the dopant. This is a problem which is being studied as part of a project to reevaluate Irvin's curves (see sec. 3.5.). If new expressions for mobility result from this study, the present equations can simply be replaced with new ones.

Because of the nature of the mobility expressions it is necessary to solve a transcendental equation to obtain the dopant density. An iterative method is commonly used to solve this type of equation and the computer program to be described has been written using Newton's method of iteration. The desired solution is that value of N which satisfies eq (4) for a given value of ρ.

Before solving a transcendental equation it is instructive to examine a graph of the function in order to arrive at a method of solution which will give convergence. Plots of the left hand side of eq (4), multiplied by ρ for scaling purposes, as a function of ρN are shown in figure 7 for both n- and p-type silicon with resistivity from 0.0001 to 100 Ω•cm. Because of the minimum to the left of the zero crossing point in the curves for the low resistivities, it is necessary that the initial choice of N for Newton's method be on the right hand side of the minimum in order to obtain convergence. The plots in figure 7 indicate that an initial choice of N by the equation $N = 1 \times 10^{17}/\rho$ will give convergence for resistivities above 10^{-4} Ω•cm for both types of silicon. For high values of resistivity there is no minimum in the curves, but it is still prudent to approach the zero crossing point from large N values.

A flowchart of the program written in extended BASIC [13] is shown in figure 8 and a list of the statements follows in table 2. The program has two parts, the main program and the iteration subroutine. It was written to be simple to implement from the user's point of view. The inputs needed are called for by print statements which end with an equal sign. The user then types in the appropriate data. The variables used in the program are identified in table 3. The first input, N1, is the number of resistivity values of the same type. The program is expecting this number of values to be typed one to a line in response to "RESISTIVITY VALUES =". Since the resistivity R is a subscripted variable, it is necessary to have a dimension statement at the beginning of the program to set aside space to accommodate all of the values. The statement DIM R(50) reserves locations for up to 50 resistivity values of one type. The last input is the conductivity type, n or p. A logical variable, T$, is used for the type as it can be readily tested to determine if its value is "N" or "P".

In the execution phase of the program a heading for the output is printed, a DO loop is set up which calculates the dopant density for each of the resistivity values, and the results are printed. The parameter K, initially set to zero, is used by the subroutine to indicate to the main program whether or not a solution to eq (4) has been found within the specified tolerance. At line 45 a test is made to determine the conductivity type and the program branches accordingly. The left hand side of eq (4), F1, and its derivative, F2, are calculated for use by the subroutine which is called at line 60. The subroutine, starting at line 80, first determines if this is the initial iteration for this resistivity. If yes, then K is set to 1 and the counter for the number of iterations, N7, is set to 0.

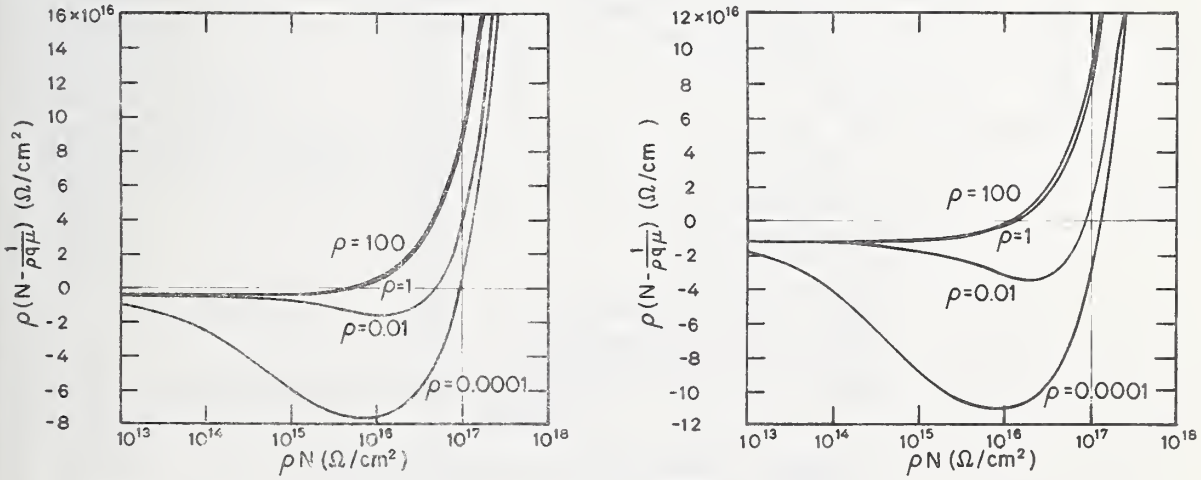
Then a test is made to see if the value of F1 is zero within a tolerance of 10^{-4} N. If so, the equation is considered solved, K is set to 2, and a return to the main program occurs. If more iterations are needed to solve the equation, then the new N is calculated by Newton's method:

$$N = N - \frac{F1}{F2}$$

where the N on the left side of the equation is the new value and the N on the right side is the previous value. The iteration count is incremented by one and control returns to the main program at line 62. Here branching, based on the value of K, occurs. If K is 1, control goes to line 45 for another iteration cycle. If K is 2, control goes to line 70 for computation of the carrier mobility from the given resistivity R(I) and the just calculated dopant density. Then the various quantities are printed and the loop continues with the next value of R(I). After all values of R(I) have been computed, control goes to line 20 for either input of more data or termination of the run. Termination is accomplished by typing 0 for the number of resistivity values. A teletypewriter printout of a run is shown in table 4. Note that convergence is very fast as usually only 2 or 3 iterations are needed to determine N to within an uncertainty of ±0.01 percent. The values presented in the table may also be used in checking programs which have been modified by other users to meet particular machine requirements. (W. R. Thurber and M. G. Buehler)

3.7. Effective Masses and Band Gap of Silicon

When developing various physical models for phenomena observed in silicon, the effective masses of electrons and holes and the energy band gap are often needed parameters. Such needs arise when computing the density of electrons and holes, the intrinsic carrier density,



a. *n*-type silicon.

b. *p*-type silicon.

Figure 7. Plots to show region of convergence for solution to the carrier density equation. (The resistivity, ρ, in Ω·cm is shown on each curve.)

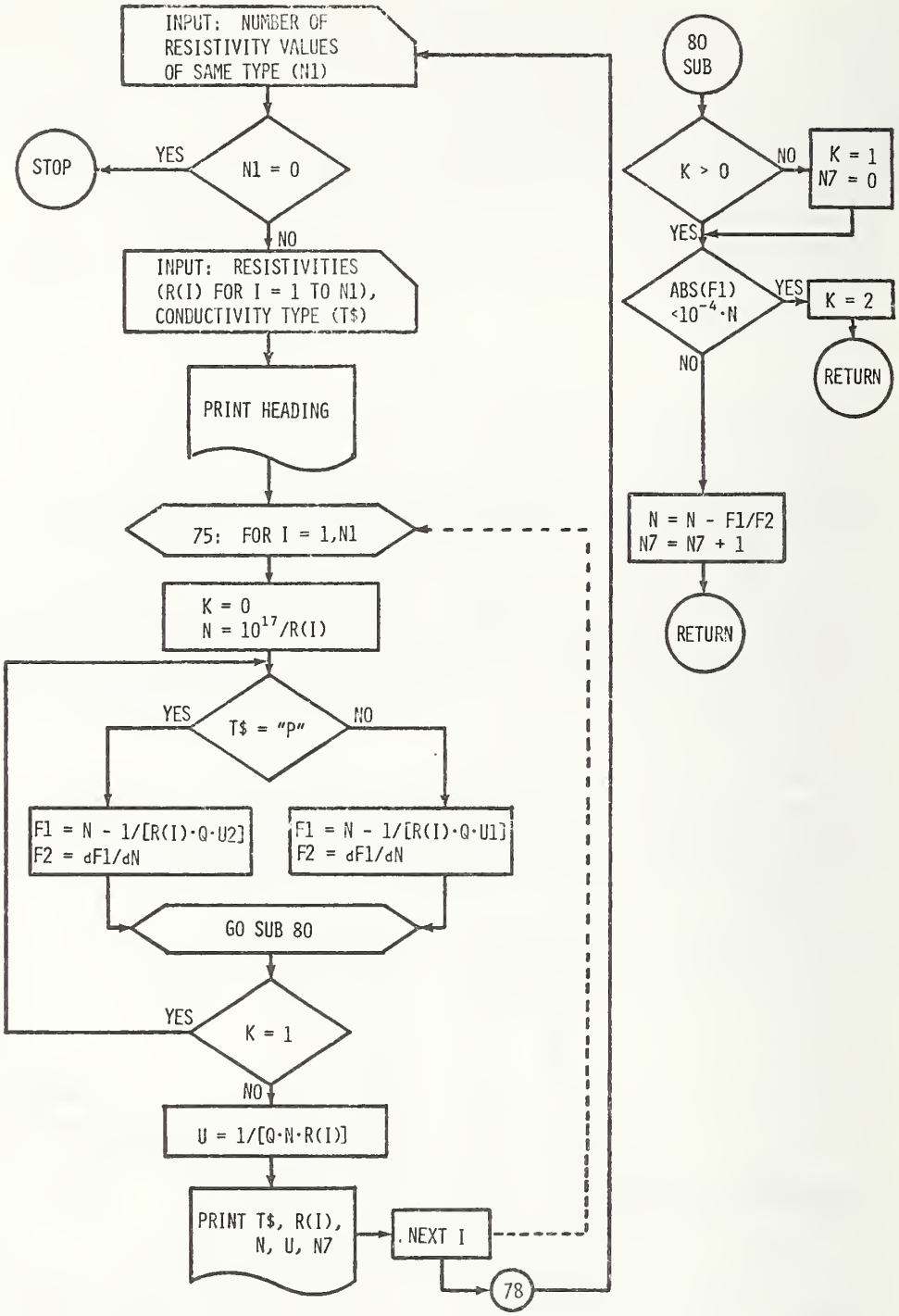


Figure 8. Flow chart for extended BASIC DOPDEN program.

Table 2 — Listing of Extended BASIC DOPDEN Program

```
10 DIM R(50)
11 Q=1.6022E-19
12 U3=65
13 U5=1330
14 A5=0.72
15 N5=8.5E16
16 U4=47.7
17 U6=495
18 A6=0.76
19 N6=1.9E17
20 PRINT "NUMBER OF RESISTIVITY VALUES OF SAME TYPE = ";
21 INPUT N1
23 IF N1>0 GO TO 25
24 STOP
25 PRINT "RESISTIVITY VALUES = ";
26 FOR I=1,N1
27 INPUT R(I)
28 NEXT I
30 PRINT "CONDUCTIVITY TYPE (N OR P) = ";
31 INPUT T$
32 PRINT
33 PRINT "TYPE   RESISTIVITY   DOPANT DENSITY   MOBILITY   ITERATIONS"
38 FOR I=1,N1
40 K=0
41 N=1E17/R(I)
45 IF T$="P" THEN 54
46 U1=U3+(U5-U3)/(1+(N/N5)**A5)
47 F1=N-1/(R(I)*Q*U1)
48 F2=(U3-U5)*A5/(R(I)*Q*U1**2)
49 F2=1+F2/((1+(N/N5)**A5)**2*N5*(N/N5)**(1-A5))
50 GO TO 60
54 U2=U4+(U6-U4)/(1+(N/N6)**A6)
55 F1=N-1/(R(I)*Q*U2)
56 F2=(U4-U6)*A6/(R(I)*Q*U2**2)
57 F2=1+F2/((1+(N/N6)**A6)**2*N6*(N/N6)**(1-A6))
60 GO SUB 80
62 IF K=1 GO TO 45
65 U=1/(R(I)*Q*N)
71 PRINT TAB(2);T$;
72 PRINT,73,R(I),N,U,N7
73 FMT X4,E10.4,X5,E10.4,X6,F7.1,X7,I2
75 NEXT I
76 PRINT
77 PRINT
78 GO TO 20
80 IF K>0 GO TO 84
81 K=1
82 N7=0
84 IF ABS(F1)<1E-4*N GO TO 90
86 N=N-F1/F2
88 N7=N7+1
89 RETURN
90 K=2
91 RETURN
99 END
```

Table 3 — Variables for Extended BASIC DOPDEN Program

Variable	Value	Description
Q	1.6022×10^{-19}	electron charge
U3	65	μ_{min} for *n*-type, see eq (5)
U5	1330	μ_{max} for *n*-type, see eq (5)
A5	0.72	α for *n*-type, see eq (5)
N5	8.5×10^{16}	N_{ref} for *n*-type, see eq (5)
U4	47.7	μ_{min} for *p*-type, see eq (5)
U6	495	μ_{max} for *p*-type, see eq (5)
A6	0.76	α for *p*-type, see eq (5)
N6	1.9×10^{17}	N_{ref} for *p*-type, see eq (5)
U1	computed	μ for *n*-type
U2	computed	μ for *p*-type
N1	input	number of resistivity values
R(I)	input	resistivity value
T$	input (*N* or *P*)	conductivity type
N	computed	dopant density
F1	computed	left hand side of eq (4)
F2	computed	derivative of eq (4)
K	set (0,1, or 2)	parameter for status of solution
N7	set	number of iterations
U	computed	μ for print-out, *n*- or *p*-type

and the Fermi energy level. Low order polynomials were fitted to published data so that the expressions can be used in future computations. Because of changes in the above parameters as dopant density increases, the equations derived here are suitable only for low to moderate doping levels.

Polynomial fits for the energy band gap and electron and hole density-of-states effective masses of silicon were determined as a function of temperature for the range 0 to 600 K using the algorithms available in the OMNITAB computing system [14]. The polynomials are of the form

$$F = \sum_{n=0}^{N} a_n T^n ,$$

where T is the temperature in Kelvin, a_n is the coefficient of the n^{th} term in the summation, and N is the order of the polynomial. The polynomials for the electron density-of-states mass, m_e^*, and the hole density-of-states mass, m_h^*, are expressed in units of the electron rest mass, m_o, and that for the energy band gap, E_g, in electron volts. The coefficients for the polynomial fits are given in table 5.

The data for the energy gap in the range 4 to 415 K were taken from the work of MacFarlane, *et al.* [15] and are reproduced in table 6. The values beyond 415 K were generated by computing a linear extrapolation of MacFarlane's three highest temperature points by

Table 4 — Typical Output of Extended BASIC DOPDEN Program

```
?XBASIC DOPDEN
RUN
NUMBER OF RESISTIVITY VALUES OF SAME TYPE = !3
RESISTIVITY VALUES = !0.001
!0.1
!10
CONDUCTIVITY TYPE (N OR P) = !N

TYPE   RESISTIVITY   DOPANT DENSITY   MOBILITY   ITERATIONS
  N     .1000E-02      .8467E 20         73.7        2
  N     .1000E 00      .9179E 17        680.0        3
  N     .1000E 02      .4800E 15       1300.3        2


NUMBER OF RESISTIVITY VALUES OF SAME TYPE = !4
RESISTIVITY VALUES = !0.01
!0.1
!1
!10
CONDUCTIVITY TYPE (N OR P) = !P

TYPE   RESISTIVITY   DOPANT DENSITY   MOBILITY   ITERATIONS
  P     .1000E-01      .8837E 19         70.6        2
  P     .1000E 00      .2524E 18        247.3        3
  P     .1000E 01      .1417E 17        440.4        2
  P     .1000E 02      .1286E 16        485.2        2


NUMBER OF RESISTIVITY VALUES OF SAME TYPE = !0

   24 EXIT
```

a least squares procedure as the band gap is known to be linear above room temperature. The temperature coefficient found was -2.786×10^{-4} eV/K. To fit the data from 0 to 600 K polynomials of various degrees were tried. One of fourth degree was chosen as it fitted a smooth curve through the data points within ±0.001 eV and had a smaller standard deviation than one of third degree. A fifth degree polynomial was considered to be unnecessary as its standard deviation was insignificantly better than that for the fourth degree fit. A computer plot of the polynomial fit to the data points is shown in figure 9 where the polynomial fit was computed at intervals of 2 K and connected by straight line segments.

Electron density-of-states masses up to 625 K were taken from the work of Barber [16], who kindly supplied an original graph from which values could be read as accurately as they are known. As discussed by Barber, the effective mass is dependent on donor density; the data tabulated in table 7 are valid for densities of less than 5×10^{17} cm^{-3}. A sixth degree polynomial was selected for use as the computed values of effective mass were within ±0.002 of the data over the entire temperature range. A computer plot of the fit is shown in figure 10.

Hole density-of-states mass data were taken from a table supplied by Barber as listed in table 8. A sixth degree polynomial fits the data within ±0.005. A computer plot of the fit is shown in figure 11. The hole mass also depends on dopant density; the mass values given by the polynomial are valid for acceptor density less than 1×10^{18} cm^{-3}.

The intrinsic density, n_i, in cubic centimetre is given by

$$n_i = 4.829 \times 10^{15} \, (m_e^* \, m_h^*)^{3/4} \, T^{3/2} \exp(-5802.4 \, E_g/T)$$

where T is in kelvin. From this equation values of n_i were calculated using for E_g, m_e^*, and

Table 5 — Coefficients of the Polynomial Fits to the Energy Band Gap, Electron Mass, and Hole Mass of Silicon

	E_g	m_e^*	m_h^*
a_0	1.15556	1.06270	0.590525
a_1	3.23741×10^{-5}	-1.61708×10^{-4}	-5.23548×10^{-4}
a_2	-8.70110×10^{-7}	6.83008×10^{-6}	1.85678×10^{-5}
a_3	9.95402×10^{-10}	3.32013×10^{-8}	-9.67212×10^{-8}
a_4	-3.80977×10^{-13}	8.04032×10^{-11}	2.30049×10^{-10}
a_5		-9.66067×10^{-14}	-2.59673×10^{-13}
a_6		4.54649×10^{-17}	1.11997×10^{-16}
Residual std. dev.	0.00032	0.00087	0.0019

Table 6 — Data used for the Polynomial Fit of the Energy Band Gap of Silicon

Temperature	Energy Band Gap
4.2 K	1.1558 eV
20.	1.1558
77.	1.1532
90.	1.1522
112.	1.1494
170.	1.1407
195.	1.1355
249.	1.1237
291.	1.1135
363.	1.0930
415.	1.0790
500.	1.0551
600.	1.0273

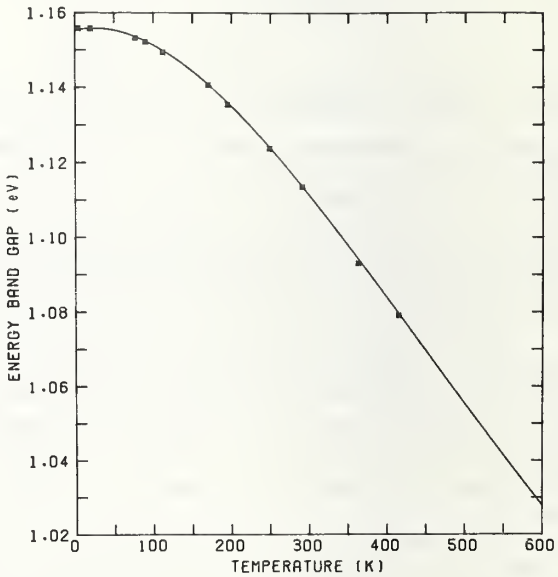


Figure 9. Energy band gap of silicon as a function of temperature. (⊠, data from MacFarlane, et al. [15]; ——— , polynomial fit.)

Table 7 — Data used for the Polynomial Fit of the Electron Density-of-States Effective Mass in Silicon

Temperature	Electron Mass
0. K	1.0625 m_o
10.	1.0626
20.	1.0628
30.	1.0631
40.	1.0642
50.	1.0662
60.	1.0703
75.	1.0780
100.	1.0905
125.	1.1025
150.	1.1140
175.	1.1265
200.	1.1380
225.	1.1490
250.	1.1608
275.	1.1713
300.	1.1822
325.	1.1928
350.	1.2028
375.	1.2122
400.	1.2215
425.	1.2305
450.	1.2392
475.	1.2472
500.	1.2555
525.	1.2628
550.	1.2700
575.	1.2767
600.	1.2828
625.	1.2887

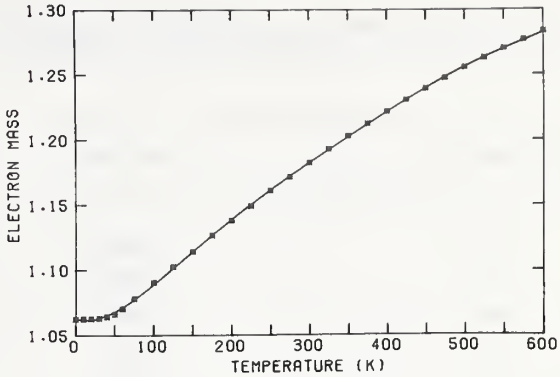


Figure 10. Electron density-of-states effective mass in silicon with donor density less than 5×10^{17} cm^{-3} as a function of temperature. (⊠, data from Barber [16]; ——— , polynomial fit.)

m_h^* the respective polynomial fits. Table 9 gives a listing of computed results for selected temperatures. (W. R. Thurber and M. G. Buehler)

3.8. Hall Effect Measurements

In Hall effect measurements the calculation of the Hall coefficient is unambiguous whenever the forward and reverse magnetic flux densities are the same. However, in most automatic data collection systems, including the one in use at NBS, the flux density is reversed simply by reversing the current through the magnet coils, and because of residual fields, the forward

Table 8 — Data used for the Polynomial Fit of the Hole Density-of-States Effective Mass in Silicon

Temperature	Hole Mass
0.0 K	0.5902 m_0
26.0	0.5904
30.0	0.5906
35.0	0.5914
40.0	0.5929
50.5	0.5981
61.1	0.6063
68.3	0.6132
77.37	0.6230
82.9	0.6291
89.3	0.6360
96.7	0.6450
105.5	0.6550
116.	0.6672
129.	0.6814
145.	0.6975
166.	0.7181
193.	0.7398
232.	0.7674
258.	0.7838
290.	0.8025
332.	0.8230
387.	0.8479
464.	0.8765
580.	0.9154
774.	0.9706

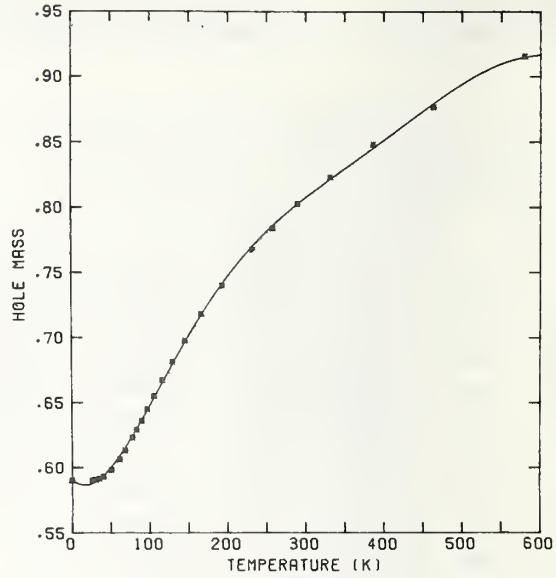


Figure 11. Hole density-of-states effective mass in silicon with acceptor density less than 10^{18} cm^{-3} as a function of temperature. (⊠, data from Barber [16]; ——— , polynomial fit.)

and reverse flux densities are slightly different. In this situation the sequence of steps to be followed in data reduction is not obvious; the optimal procedure depends on whether it is more important to eliminate misalignment or magnetoresistance voltages.

For a Hall bar of parallelepiped shape [17] the voltage which is measured across the width of the bar has three significant components: (1) the misalignment voltage arising because of a slight offset between the contacts on either side of the bar, (2) the Hall voltage, and (3) the magnetoresistance voltage which is proportional to the misalignment of the contacts and the square of the flux density. Two other components, the thermomagnetic and thermoelectric voltages, are small for semiconductors measured in a specimen holder designed to minimize thermal gradients. Consequently they do not influence the choice of a data reduction procedure. For most specimens the main reason for reversing the magnetic field is to eliminate the effect of the misalignment voltage which is usually much larger than the magnetoresistance voltage. However, for high mobility materials, such as indium antimonide, the magnetoresistance effect may dominate, especially at low temperatures.

As discussed in ASTM Method F 76 [17] the voltage from which the Hall coefficient is obtained is measured for both directions of specimen current. The first step in the data

Table 9 — Band Gap, Electron Mass, Hole Mass, and Intrinsic Carrier Density of Silicon at Selected Temperatures Calculated from the Polynomial Fits

T	E_g	m_e^*	m_h^*	n_i
0 K	1.1556 eV	1.063 m_o	0.591 m_o	
50	1.1551	1.068	0.600	
100	1.1511	1.089	0.648	3.67×10^{-11} cm^{-3}
150	1.1440	1.114	0.701	4.45×10^{-1}
200	1.1346	1.139	0.747	6.13×10^{4}
250	1.1233	1.161	0.781	8.43×10^{7}
300	1.1108	1.182	0.807	1.13×10^{10}
350	1.0973	1.202	0.829	3.97×10^{11}
400	1.0832	1.221	0.851	5.96×10^{12}
450	1.0690	1.239	0.873	5.05×10^{13}
500	1.0548	1.256	0.894	2.84×10^{14}
550	1.0409	1.270	0.910	1.18×10^{15}
600	1.0274	1.282	0.917	3.88×10^{15}

reduction procedure is to normalize all voltages with respect to specimen current so the equations can be written in units of resistance.

The resistance between the side contacts is given by:

$$R = R_a + cR_H B + MB^2 \ ,$$

where R is the measured (algebraic) resistance, R_a is the misalignment resistance, c is a constant which includes the thickness of the Hall bar, R_H is the Hall coefficient which is assumed to be independent of the flux density, M is the effective magnetoresistance coefficient, and B is the magnetic flux density. When the flux density is the same in the forward and reverse directions the calculation for the Hall coefficient is:

$$\frac{R_f - R_r}{2B} = \frac{R_a + cR_H B + MB^2 - (R_a - cR_H B + MB^2)}{2B} = cR_H \ ,$$

where R_f and R_r are the measured resistances for forward and reverse magnetic flux densities, respectively.

When the magnitude of the magnetic flux density in the forward direction, B_f, differs from that in the reverse direction, B_r, the misalignment contribution can be eliminated as follows:

$$\frac{R_f - R_r}{B_f + B_r} = \frac{R_a + cR_H B_f + MB_f^2 - (R_a - cR_H B_r + MB_r^2)}{B_f + B_r} = cR_H + M(B_f - B_r).$$

The calculated R_H is in error only by a magnetoresistance component.

Another possible data reduction procedure involves dividing R_f and R_r by the respective flux densities before combining:

$$\frac{R_f}{2B_f} - \frac{R_r}{2B_r} = \frac{(R_a + cR_H B_f + MB_f^2)}{2B_f} - \frac{(R_a - cR_H B_r + MB_r^2)}{2B_r} = cR_H + \frac{R_a(B_r - B_f)}{2B_f \cdot B_r} + \frac{M(B_f - B_r)}{2}.$$

This procedure results in one-half the magnetoresistance error of the previous method, but the misalignment contribution has not been completely eliminated.

It is possible to cancel the magnetoresistance by dividing R_f and R_r by the respective flux density square:

$$\frac{R_f}{B_f^2} - \frac{R_r}{B_r^2} = \frac{(R_a + cR_H B_f + MB_f^2)}{B_f^2} - \frac{(R_a - cR_H B_r + MB_r^2)}{B_r^2} = \frac{cR_H(B_f + B_r)}{B_f \cdot B_r} + \frac{R_a(B_r^2 - B_f^2)}{B_f^2 \cdot B_r^2}.$$

Since B_f and B_r are measured following a flux density reversal, it is simple to multiply by the quantity $B_f \cdot B_r/(B_f + B_r)$ and obtain a value for cR_H, within a misalignment error, as follows:

$$\left[\frac{R_f}{B_f^2} - \frac{R_r}{B_r^2}\right]\left[\frac{B_f \cdot B_r}{(B_f + B_r)}\right] = cR_H + \frac{R_a(B_r - B_f)}{B_f \cdot B_r}.$$

No data reduction procedure eliminates both contributions simultaneously so it is necessary to determine which effect is dominant and choose the procedure which minimizes it. Also the magnitude of the flux density may dictate the choice of procedures. For the same specimen, the misalignment error may be the one to eliminate at low flux densities whereas at high densities the magnetoresistance effect should be eliminated. (W. R. Thurber)

3.9. Probe Force Measurements

A small-scale experiment to test the ability of various laboratories to measure the probe force of pins mounted in a four-probe head was completed. The purpose of the test, which involved seven laboratories was to test the adequacy of a proposed ASTM Recommended Practice [18] for making such measurements (NBS Tech. Note 773, p. 7). For the test, a four-probe head was selected and each pin was individually tensioned to a different value. The range covered included the ranges specified in ASTM methods of test for four-probe resistivity measurements on bulk silicon and sheet resistance measurements on epitaxial silicon [19, 20]. Method F 84 [19] calls for a probe force of 1.75 ± 0.25 N for measuring bulk silicon slices while Method F 374 [20] calls for 0.30 ± 0.03 N for measuring epitaxial silicon wafers.

Each laboratory was asked to measure probe force on each pin five times. Analysis of the results, displayed in figure 12, showed that all but the lowest force level could be measured with a multilaboratory relative sample standard deviation of 4 to 7 percent of the multilaboratory mean which is compatible with the requirements of Method F 84. However, the multilaboratory relative sample standard deviation for the lowest force was about 17 percent of the multilaboratory mean. This variability is far greater than is permitted by the requirements of Method F 374.

Two possible explanations may be offered. The first is that the friction forces in the mechanical linkages of the various instruments used for this measurement might have different

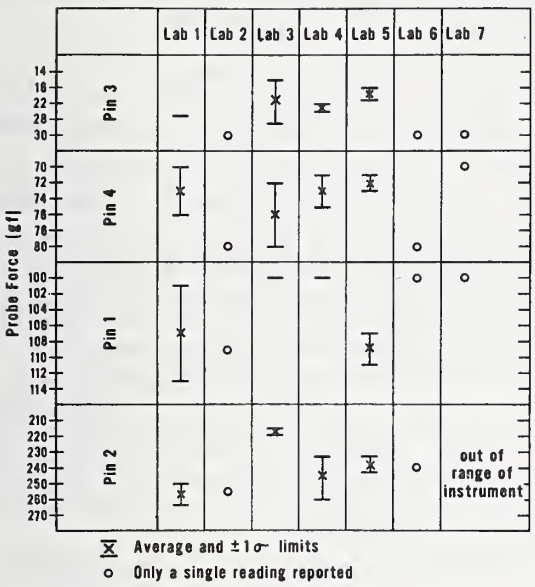


Figure 12. Restoring force of the pins of a four-probe array for measuring resistivity as measured by seven laboratories. (Note 1 gf = 9.8 mN.)

values. The errors caused by these friction forces would be expected to cause larger percentage errors when measuring smaller probe forces. The second possibility is that the use of gauges of improper range for measuring a given force value resulted in erroneous readings. It is to be noted that three laboratories reported values of 30 gf (0.29 N) for Pin 3. Similarly, four laboratories reported values of 100 gf (0.98 N) for Pin 1. The probability of such high level agreement is very small for seven participants whatever the force level. That these coincidences occurred at such round measurement values suggests that gauges were used beyond their designated range for these measurements and that the extremum value of the gauge used was reported. Even excluding the three 30 gf readings, however, is not adequate to reduce the multilaboratory relative sample standard deviation to 10 percent of the multilaboratory mean.

The results of this experiment suggest that an adequate procedure for probe force measurement should require that the frictional forces in the measuring instrument be minimized and that the gauge used for the measurement be chosen so that the limits of its range are at least 15 percent above and below the force level to be measured.

(J. R. Ehrstein and F. H. Brewer)

3.10. Standard Reference Materials

Silicon resistivity wafer standards were released for sale in early November as SRM 1520 (NBS Tech. Note 806, p. 66). As a convenience for purchasers of this standard, values of voltage to current ratio (V/I) as measured during the calibration process were given on the individual calibration certificates in addition to the calculated resistivity values. Use of V/I values is a convenience which omits the application of correction factors for the geometrical conditions of measurement. However, to compare the quoted NBS values for V/I to those measured by an individual user of the SRM's, the same geometrical conditions must apply as were used during calibration.

Discrepancies found by one user of SRM 1520 between his V/I values and those of NBS were traced to use of a probe of different spacing than that used during certification. A four-probe array with probe spacing of 1.6 mm (0.63 in.) as specified in ASTM Method F 84 [19] was used during the certification procedure. If a different probe spacing is used differences in the V/I ratio are introduced because of differences in the ratio of specimen thickness to probe spacing, differences in volume of material sampled by the measurement,

and differences in the ratio of specimen diameter to probe spacing. For SRM 1520, the relative importance of these factors for probes with spacing smaller than that used for certification is in the order listed; since the wafers used for the SRM are quite uniform and are of large diameter compared to the probe spacing.

By extension, use of the voltage-current ratio as a short cut to gauge resistivity values, whether for comparing the resistivities of a sequence of wafers, or for comparing the values measured on a common wafer at two different measurement stations is valid only to the extent that all geometric conditions of the specimen — shape, size, and probe spacing — are held constant. To the extent that geometric conditions are not held constant, accurate comparisons can be made only by applying the geometric factors, $F(w/s)$, F_2, and w, as detailed in Method F 84 [19]. Use of these factors gives the resistivity value at the temperature of measurement, the resistivity being the only measurement constant obtainable (within the limits of specimen uniformity) when the measurement geometry changes. All other factors pertinent to silicon resistivity measurement such as photovoltage, excess carrier generation, resistive heating at the probes and electrical noise interference are not considered here. These and the effect of temperature on the measurement are considered in some detail in Method F 84 [19]. (J. R. Ehrstein)

The simple multipass round-robin experiment to study the stability and the multilaboratory precision to be expected of SRM 1520 (NBS Spec. Publ. 400-1, p. 12) was initiated. NBS and five other laboratories are to participate in this experiment during the next 18 months. In addition to data on the SRM sets retained at each participating laboratory, data are being collected on two SRM sets circulated regularly among the participants.

(F. H. Brewer, J. Mandel*, and J. R. Ehrstein)

3.11. Other Standards Activities

NBS participated in a pilot study of the junction capacitance-voltage (C-V) method conducted by the Epitaxial Resistivity Section of ASTM Committee F-1 on Electronics. The object of the study was to establish the repeatability of the dopant density values derived from junction C-V measurements on planar metallized diodes. In this study neither the specimens nor the measurement procedures were optimized with respect to obtaining accurate measurements. Rather, the emphasis was on intermediate term, single laboratory repeatability. Each pilot study participant was given an n/p epitaxial wafer in which n^+ buried layers had been diffused and on which an array of 0.76-mm (30-mil) diameter, diffused, metallized, ungated p^+n diodes had been fabricated. The capacitance between the p^+ and p layers was measured on one diode on this slice with the n layer floating electrically. Seven reverse bias voltage levels which ranged from 2 to 40 V were applied. These measurements were repeated 14 times in 33 days. The capacitance readings at the seven voltage levels had relative sample standard deviations ranging from 0.93 percent at 2 V (capacitance about 54 pF) to 0.41 percent at 40 V (capacitance about 15 pF). A dopant density profile and an average dopant density were calculated for each of the 14 sets of capacitance-voltage pairs. The relative sample standard deviation of the average dopant density was 0.82 percent. Other laboratories who participated in the pilot study reported relative sample standard deviations for this average which ranged from 0.56 to 1.28 percent. This indicates the degree of single-laboratory repeatability that can be expected from this measurement. (R. L. Mattis and M. G. Buehler)

---

*NBS Institute for Materials Research

4. CRYSTAL DEFECTS AND CONTAMINANTS

4.1. Thermally Stimulated Current and Capacitance Measurements

A physical model has been applied to the experimental results (NBS Spec. Publ. 400-1, pp. 16-19) obtained for the dynathermal current and capacitance response of the gold acceptor in silicon in which the gold density, N_t, is less than the background donor dopant density, N_d. This model effectively predicts the shift in the thermally stimulated current characteristics with heating rate for both the majority carrier, phase I response, and the minority carrier, phase II response in an *n*-MOS capacitor.

The model is based on the charge distribution of an ideal MOS capacitor*, of area A and oxide thickness X_o, biased in the region of strong inversion as illustrated in figure 13. Initially (fig. 13a) the applied gate voltage, V_{g1}, is just sufficient to drive the depletion width to its steady state value, W_{IIf}, and to create a slight inversion layer of holes at the oxide-silicon interface. The sum of the positive charge per unit area in the depletion region, $q(N_d - n_{tf})W_{IIf}$, and the positive charge per unit area in the inversion region, qp_{sA}, is balanced by a negative charge per unit area, $-Q_{mA}$, at the metal-oxide interface:

$$-Q_{mA} = qp_{sA} + q(N_d - n_{tf})W_{IIf} ,$$

where q is the electronic charge and n_{tf} is the density of negatively charged gold centers in the steady state. The capacitance, C_{IIf}, associated with this charge distribution is denoted by point A on the C-V plot of figure 14 and is given by:

$$C_{IIf} = \left(C_o^{-1} + \frac{W_{IIf}}{\varepsilon_s A} \right)^{-1} ,$$

where $C_o = \varepsilon_o A/X_o$, ε_o is the dielectric constant of the oxide, and ε_s is the dielectric constant of silicon.

The hole density p_{sA} at the oxide-silicon interface is sufficient to supress the generation action of fast interface states. In the depletion region in steady state conditions the density, n_{tf}, of gold acceptor centers which contain electrons is governed by the electron and hole emission rates, e_n and e_p, respectively:

$$n_{tf} = \frac{e_p N_t}{e_n + e_p} .$$

Similarly in the steady state the density of neutral gold acceptor centers, p_{tf}, is given by:

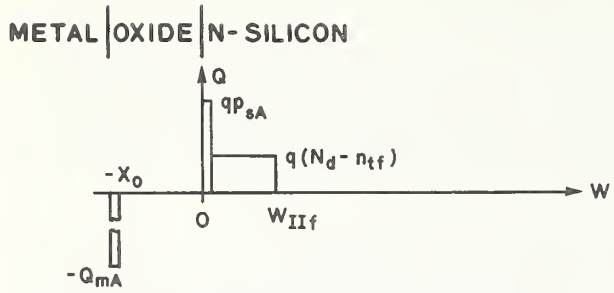
$$p_{tf} = N_t - n_{tf} = \frac{e_n N_t}{e_n + e_p} .$$

The emission rates for impurity centers lying deep in the forbidden energy gap have been shown to have the following temperature dependence [21]:

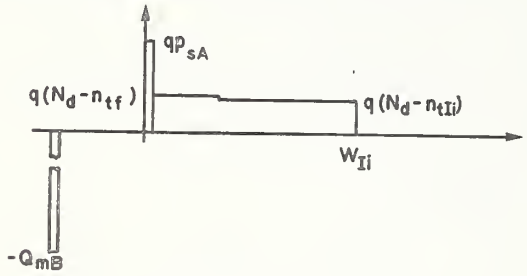
$$e_n = B_n T^2 \exp(-\Delta E_n/kT) \qquad (6)$$

---

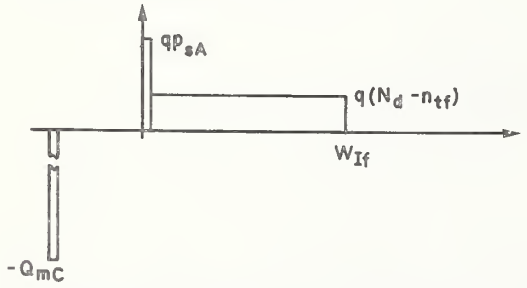
*Charge in the oxide and differences in work function do not affect the results to be obtained.



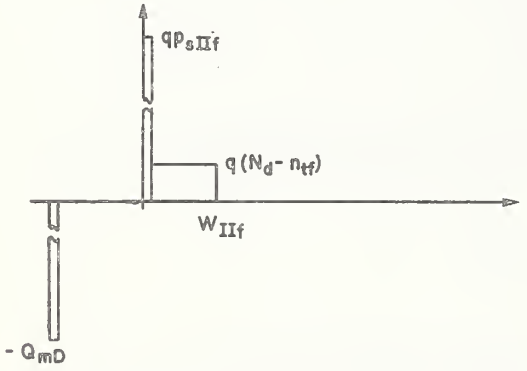
a. Initial condition before charging.



b. Initial charged condition.



c. After majority carrier emission (End of phase I response).



d. After minority carrier emission (End of phase II response).

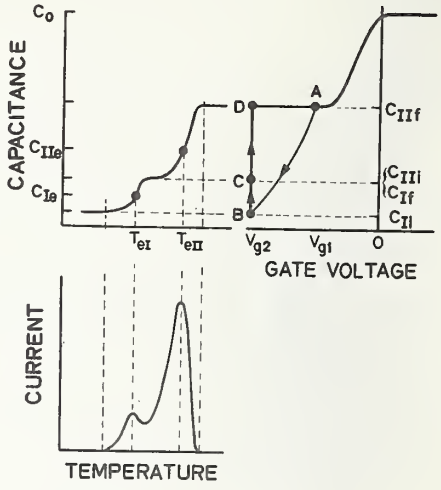


Figure 14. Capacitance-voltage characteristi and dynathermal current and capacitance respo of an ideal, gold-doped n-MOS capacitor. (The points A, B, C, and D correspond to charge distributions a, b, c, and d, respectively, in fig. 13. The capacitance-temperatu and current temperature curves are for a gate voltage of V_{g2}.)

Figure 13. Charge density distribution in an ideal, gold-doped n-MOS capacitor during dynathermal response measurement. (The hole density, p_s, at the oxide-silicon interface and the electron charge density, $-Q_m$, at the metal-oxide interface are given per unit area since they occur in very narrow sheets at the interface.)

and

$$e_p = B_p T^2 \exp(-\Delta E_p/kT) \tag{7}$$

where ΔE_n and ΔE_p are the energy differences between the gold acceptor and the conduction and valence band edges, respectively, k is Boltzmann's constant (=8.617 × 10^{-5} eV/K), T is the absolute temperature, and B_n and B_p are coefficients. The constants ΔE and B for the gold acceptor in silicon [22] are listed in table 10. At room temperature, $n_{tf} \approx 0.05\ N_t$. In the neutral region of the semiconductor, to the right of the depletion region, the occupancy of the gold acceptors is governed by the position of the Fermi energy. For the case considered here, $N_d > N_t$, the Fermi energy lies above the gold acceptor energy so that essentially all the gold acceptors in the neutral region are filled with electrons, $n_{tIi} \approx N_t$.

With gate voltage V_{g1} applied, the MOS capacitor is then rapidly cooled to a temperature near 77 K after which the applied gate voltage is increased to V_{g2}. Additional free electrons are swept out and the space charge region widens to a new value, W_{Ii}, as shown in figure 13b. The electrons on the gold acceptor, however, remain trapped at this low temperature so that only $N_d - n_{tIi}$ positive charges are available in each unit volume of this region. The positive hole charge at the oxide-silicon interface remains unchanged, but the negative charge per unit area at the metal-oxide interface increases to compensate for the added positive charge:

$$-Q_{mB} = qp_{sA} + q(N_d - n_{tf})\ W_{IIf} + q(N_d - n_{tIi})\ W_{Ii}\ .$$

The capacitance, C_{Ii}, associated with this charge distribution is denoted by point B on the C-V plot of figure 14 and is given by:

$$C_{Ii} = \left(C_o^{-1} + \frac{W_{Ii}}{\varepsilon_s A}\right)^{-1}\ .$$

This condition is known as deep depletion.

With gate voltage V_{g2} applied, the capacitor is heated. At some temperature, the gold acceptor centers begin to emit the trapped electrons. The rate of change of the electron density at a defect center in a space-charge region is [23]:

$$\frac{dn_t}{dt} = e_p p_t - e_n n_t\ , \tag{8}$$

where p_t and n_t are the hole and electron densities, respectively, at the defect center. In addition, some holes are emitted from the gold acceptor centers; these are immediately swept to the inversion layer at the oxide-silicon interface. The rate per unit area at which holes are generated at this interface, dp_s/dt, is given by the difference between the hole generation rate in the space-charge region and the hole capture rate at the interface [24]:

$$\frac{dp_s}{dt} = e_p p_t (W - W_{IIf})\ , \tag{9}$$

where W is the width of the space charge region at time t. During most of this period, the hole emission from the gold acceptor centers is substantially lower than the electron emission so the response during this period is called the majority carrier, phase I response. During this phase, the capacitance changes and a small current can be observed in the external circuit; these are the left hand features of the capacitance-temperature and

Table 10 — Constants for Emission Rates for Gold Acceptor in Silicon

	B, $K^{-2} \cdot s^{-1}$	E, eV
electrons	1.97×10^7	0.547
holes	5.82×10^6	0.590

current-temperature plots in figure 14. Phase I is complete when the gold acceptor centers have been discharged to their steady state value, $n_t = n_{tf}$. At this time, $e_p p_t = e_n n_t$ so dn_t/dt becomes zero. At the end of phase I, the charge distribution is as given in figure 13c. Compared with the previous distribution (fig. 13b), the space charge width is slightly less and the total positive charge in the semiconductor is slightly greater. The capacitance, $C_{If} = C_{IIi}$, associated with this charge distribution is denoted by point C on the C-V plot of figure 14 and is given by:

$$C_{If} = C_{IIi} = \left(C_o^{-1} + \frac{W_{If}}{\epsilon_s A} \right)^{-1} .$$

As the capacitor is heated further, the gold acceptors act predominately as hole generation sites; as holes are generated they are swept to the oxide-silicon interface to increase the inversion layer charge. At the same time electrons, which enter the gold acceptors as a consequence of the emission of the holes, are emitted rapidly and move toward the neutral region of the semiconductor. Some of these electrons neutralize the charge in the space charge region, shrinking its width. During this period, the current and capacitance charges are dominated by the hole emission; hence the response during this period is called the minority carrier, phase II response. The phase II current and capacitance response are shown as the right hand features of the capacitance-temperature and current-temperature plots of figure 14. When the depletion width has returned to its steady state value, sufficient charge has gone to the interface and the current ceases. The charge distribution is as given in figure 13d and the capacitance, denoted by point D on the C-V plot of figure 14, has returned to its original value.

To apply the model quantitatively it is convenient to consider the current through the MOS capacitor which can be found by evaluating the displacement current through the oxide while the constant gate voltage V_{g2} is applied. The electric field in the oxide is given by the first integral of Poisson's equation:

$$E_o = - \frac{q}{\epsilon_o} \left[(N_d - n_{tf}) W_{IIf} + (N_d - n_t)(W - W_{IIf}) + p_s \right].$$

The displacement current through the oxide is given by:

$$I = \epsilon_o A \frac{dE_o}{dt} = -qa \left[(N_d - n_t) \frac{dW}{dt} - (W - W_{IIf}) \frac{dn_t}{dt} + \frac{dp_s}{dt} \right]. \qquad (10)$$

In order to evaluate this expression, an expression for dW/dt must be found. The voltage drop across the capacitor, which can be found by double integration of Poisson's equation:

$$V_{g2} = -\frac{qX_o}{\varepsilon_o}\left[(N_d - n_{tf})W_{IIf} + (N_d - n_t)(W - W_{IIf}) + p_s\right]$$

$$+\frac{q}{2\varepsilon_s}\left[(N_d - n_{tf})W_{IIf}^2 + (N_d - n_t)(W^2 - W_{IIf}^2)\right],$$

is constant so that $dV_{g2}/dt = 0$. By equating the time derivative of the right hand side of this equation to zero it is found that:

$$\frac{dW}{dt} = \frac{\frac{dn_t}{dt}\left[\frac{X_o}{\varepsilon_o}(W - W_{IIf}) + \frac{(W^2 - W_{IIf}^2)}{2\varepsilon_s}\right] - \frac{X_o}{\varepsilon_o}\frac{dp_s}{dt}}{(N_d - n_t)\left(\frac{X_o}{\varepsilon_o} + \frac{W}{\varepsilon_s}\right)} \quad . \tag{11}$$

On substituting eqs (11), (8), and (9) into eq (10) one finds that:

$$I = -\frac{qA}{2\varepsilon_s}\frac{e_n n_t(W - W_{IIf})^2 + e_p p_t(W^2 - W_{IIf}^2)}{\frac{X_o}{\varepsilon_o} + \frac{W}{\varepsilon_s}} \quad . \tag{12}$$

The majority carrier, phase I current response has a maximum if $e_n >> e_p$, as is the case for the gold acceptor in silicon. As a first approximation, put $e_p = 0$ in eq (12) so that the current becomes:

$$I = -\frac{qAe_n n_t}{2\varepsilon_s}\frac{(W - W_{IIf})^2}{\left(\frac{X_o}{\varepsilon_o} + \frac{W}{\varepsilon_s}\right)} \quad .$$

During phase I, W is approximately constant so that the maximum current can be found by evaluating $dI/dt = d(e_n n_t)/dt = 0$. This, with eq (8) and $e_p = 0$, leads to

$$\frac{de_n}{dt} = e_n^2 \quad ,$$

which can be evaluated by means of eq (6) to yield for the temperature at which the current is a maximum

$$T_{eI} = \frac{\Delta E_n}{k} \Big/ \ell n\left[\frac{B_n k T_{eI}^4}{\beta_{eI}\,\Delta E_n}\left(\frac{2kT_{eI}}{\Delta E_n} + 1\right)^{-1}\right] \tag{13}$$

where β_{eI} is the heating rate, dT/dt, at T_{eI}. As explained elsewhere [23], the heating rate need not be linear in time. This expression is identical to the p^+n junction expression [21] indicating that the current peaks at the same temperature in both p^+n junctions and n-MOS capacitors for the same defect evalauted at the same heating rate. Equation (13) was evaluated using B_n and ΔE_n values as given in table 10 to obtain the curve labeled $de_n/dt = e_n^2$ in figure 15.

If the inequality $e_n >> e_p$ cannot be assumed, then the current peak can be found by assuming $W >> W_{IIf}$ and $dW/dt = 0$. Now eq (12) evaluated at $dI/dt = 0$ yields $d(e_n n_t + e_p p_t)/dt = 0$. An analytic expression has not been found for this relation. Values for the current peak were found by evaluating $e_n n_t + e_p p_t$ numerically as a function of temperature using the emission rates given in table 10 and n_t and p_t expressions given elsewhere (see eqs (7a) and (7b), ref. [21]). Values for β_{eI} and T_{eI} derived in this manner, form the curve labeled $d(e_n n_t + e_p p_t)/dt = 0$ in figure 15.

Experimental points plotted in figure 15 as circles resulted from dynathermal measurements of the gold acceptor on the n-side of a p^+n junction (Device No. 2107.1) as previously reported (NBS Tech. Note 806, pp. 14-16). The experimental points plotted as squares resulted from dynathermal measurements of an n-MOS capacitor (Device No. 2107.7) fabricated on the same wafer as the p^+n junction (NBS Spec. Publ. 400-1, pp. 16-19). The error bars are estimated limits of one standard deviation, based on the range of data obtained in a series of repetitive runs.

The minority carrier, phase II current response always has a peak irrespective of the asymmetry in the emission rates of a defect center. This peak occurs as minority carriers begin to satisfy the inversion layer requirements at the oxide-silicon interface.

The physical model for phase II assumes that steady state conditions prevail; that is, $dn_t/dt = dp_t/dt = 0$. Because the densities n_t and p_t are both time and temperature dependent, this assumption must be examined for each defect center. For the gold acceptor the temperature can be swept slowly enough so that at each temperature n_t and p_t are at their steady state values, n_{tf} and p_{tf}, respectively.

With use of the steady state condition, $e_n n_{tf} = e_p p_{tf}$, eq (12) becomes:

$$I = -\frac{qAW}{\varepsilon_s} e_p p_{tf} \frac{(W - W_{IIf})}{\frac{X_o}{\varepsilon_o} + \frac{W}{\varepsilon_s}}$$

The peak in the current is found by evaluating $dI/dt = 0$. This leads to

$$de_p dt = e_p^2 F \ , \qquad (14)$$

where

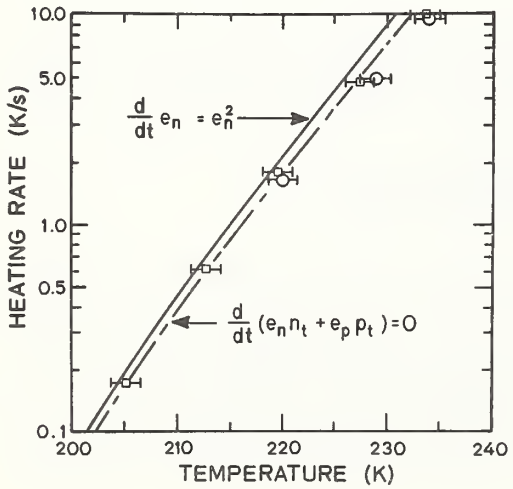


Figure 15. Emission temperature of the phase I response of the gold acceptor in silicon at various heating rates. (Solid curve: theory with $e_p = 0$ [eq (13)]; dashed curve: theory with $e_p \neq 0$; ○: experimental data on gold-doped p^+n junction; □: experimental data on n-MOS capacitor.)

$$F = \left(\frac{p_{tf}}{N_d - n_{tf}}\right)\left(\frac{C_{IIe}\,(C_{IIf}C_o - C_{IIe}^2)}{C_o C_{IIf}\,(C_o - C_{IIe})}\right),$$

$$C_{IIe} = \left(C_o^{-1} + \frac{W_{IIe}}{\varepsilon_s A}\right)^{-1}, \text{ and}$$

the subscript e designates a quantity taken at the emission temperature, defined by the phase II current peak. The solution of eq (14) by use of eq (7) leads to an expression for the phase II emission temperature:

$$T_{eII} = \frac{\Delta E_p}{k} \Big/ \ln\left[\frac{FB_p kT_{eII}^4}{\beta_{eII}\,\Delta E_p}\left(\frac{2kT_{eII}}{\Delta E_p} + 1\right)^{-1}\right]$$

where β_{eII} is the phase II heating rate evaluated at the emission temperature. This expression, which is identical in form to the expression derived for phase I, eq (13), except for the factor F, was evaluated using B_p and ΔE_p values as given in table 10 to obtain the curve in figure 16.

The factor F can be written in terms of measurable capacitances if it is assumed that the defect centers are initially fully charged:

$$F = \frac{C_{IIf}C_{IIe}(C_{IIf}C_o - C_{IIe}^2)(C_{If}^2 - C_{Ii}^2)}{C_o C_{If}^2 (C_o - C_{IIe})(C_{IIf}^2 - C_{Ii}^2)}$$

This equation and values of capacitance heating rate, and emission temperature, experimentally determined on the *n*-MOS capacitor (Device No. 2107.7) were used in locating the data points shown in figure 16. (W. E. Phillips and M. G. Buehler)

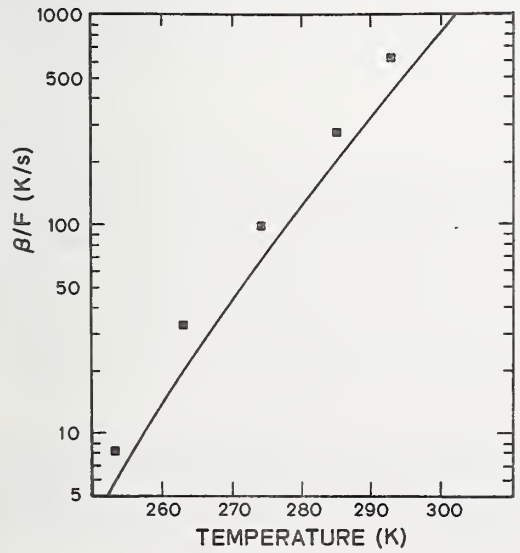


Figure 16. Emission temperature of the phase II response of the gold acceptor in a silicon *n*-MOS capacitor at various normalized heating rates. (Solid curve: theory; ■: experimental data.)

5. OXIDE FILM CHARACTERIZATION

5.1. MOS Capacitance-Voltage Method

A commonly used technique for characterizing metal-oxide-semiconductor (MOS) structures is the measurement of the capacitance-voltage (C-V) characteristic. Ordinarily this measurement is straightforward and can be simply interpreted. However, there are situations which can lead to error; several such cases arising from excessive loss in the MOS structure were analyzed in detail.

In the accumulated condition, the capacitance of an MOS device consists only of the oxide contribution. The oxide capacitance can be calculated from the gate area and the oxide thickness, both of which may be measured independently. If the measured and calculated values of capacitance do not agree, there is reason to suspect errors in the measurement due to excessive loss in the structure. This loss can be caused by one or more of the following possibilities: 1) high contact resistance on the backside, 2) high series body resistance, or 3) capacitance and conductance of any backside oxide which may be present.

Two typical MOS structures and their equivalent circuits are shown in figures 17 and 18. The MOS capacitor, C, consists of the series combination of the oxide capacitance, C_o, and the semiconductor depletion capacitance, C_s. The series resistance, R, is comprised of the body resistance of the semiconductor, R_b, and the backside contact resistance, R_c. In an MOS structure which has had its backside metal applied without oxide removal (fig. 18) an additional capacitance, C_B, and a resistance, R_B, which accounts for pin holes and other leakage paths are introduced.*

In the case of the structure without a backside oxide film (fig. 17) there are four cases to consider: I) $R_b = R_c = 0$, II) $R_b > 0$, $R_c = 0$, III) $R_b = 0$, $R_c > 0$, IV) $R_b > 0$, $R_c > 0$. Case I is the ideal situation and presents no problems. Depending on the magnitude of the resistances, the other three cases could lead to errors. To analyze these cases, consider the equivalent parallel circuit† whose elements are given by:

$$C_p = \frac{C}{1 + \omega^2 R^2 C^2}$$

and

$$R_p = R \frac{(1 + \omega^2 R^2 C^2)}{\omega^2 R^2 C^2} \quad ,$$

where ω is the angular frequency of the test voltage source. Evidently, the measured capacitance, C_p, differs from the actual capacitance by the factor $(1 + \omega^2 R^2 C^2)^{-1}$. The circuit Q is given by:

$$Q = \frac{1}{\omega RC} = \omega R_p C_p \quad . \tag{15}$$

Therefore, if the error in the capacitance measurement is defined as:

---

*In the present analysis, the oxide and semiconductor depletion regions are assumed to be accurately represented by capacitive elements; other physical mechanisms (e.g., interface states), which could cause additional losses, are ignored.

†The parallel equivalent is considered because of instrumental considerations. Typically, the measurement is made with a constant voltage, high frequency a-c source and a locked phase, synchronous detection system. Hence, the experiment consists of measuring a current proportional to the equivalent parallel capacitance under conditions of a constant applied test voltage.

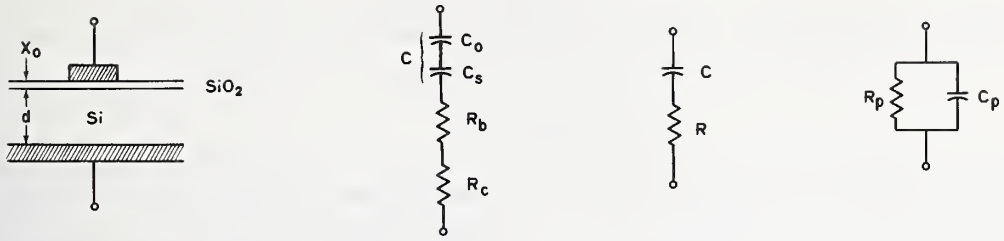


Figure 17. MOS capacitor and its equivalent circuit representations. (See text for meaning of symbols. It is assumed that the area of the gate, A, is less than the area of the backside contact, A_B.)

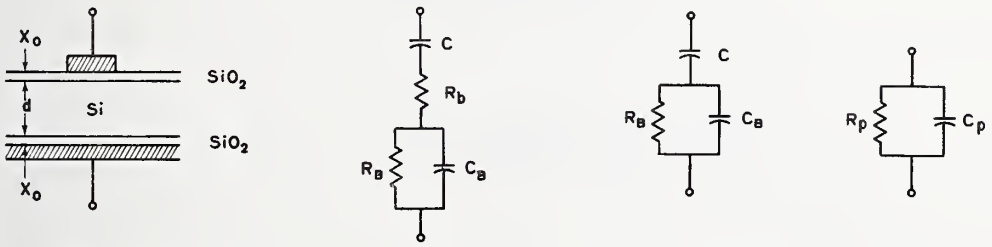


Figure 18. MOS capacitor with backside oxide film and its equivalent circuit representations. (See text for meaning of symbols. It is assumed that the area of the gate, A, is less than the area of the backside contact, A_B. In developing the parallel circuit model it is assumed that $R_b = 0$.)

$$e = \frac{C - C_p}{C} = \frac{1}{1 + Q^2} \quad ,$$

the Q of the capacitor is given by:

$$Q = \left(\frac{1 - e}{e}\right)^{1/2} \tag{16}$$

Thus, for a measurement frequency of 1 MHz and an MOS capacitance of 10 pF, the error in the measurement of C will be 1 percent or less if the series resistance is 1.6 kΩ or less.

To obtain a relationship between the error in the capacitance measurement and the material parameters of the elements of the MOS structure, consider as an example, case II above. The largest error (worst case analysis) will occur for the largest values of R_b and C. Since $C \leq C_o$, the largest value of C is given by the oxide capacitance:

$$C_o = \frac{\varepsilon_o A}{X_o} \quad , \tag{17}$$

where ε_o is the dielectric constant of the oxide film, A is the gate metal area, and X_o is the oxide thickness. The largest value of R_b results when the current is confined to a cylinder of area A:

$$R_b = \frac{\rho d}{A} , \tag{18}$$

where ρ is the bulk resistivity and d is the wafer thickness. By combining eq (15) (with $R = R_b$ and $C = C_o$) with eqs (16), (17), and (18) one obtains:

$$d = \frac{X_o}{\varepsilon_o \rho \omega} \left(\frac{e}{1 - e} \right)^{1/2} . \tag{19}$$

Figure 19 shows plots of eq (19) for an error of 1 percent and a frequency $f = \omega/2\pi = 10^6$ Hz for three different oxide thicknesses, X_o. For a given X_o, the region above the curve signifies combinations of ρ and d which result in a measurement error greater than 1 percent whereas below the curve, the error would be less than 1 percent.

For the situation when an oxide film is present on backside of the structure (fig. 18), the analysis is more complex. If it is assumed that the body resistance of the semiconductor can be neglected ($R_b = 0$), the elements of the equivalent parallel circuit are:

$$C_p = C \frac{[1 + \omega^2 R_B{}^2 C_B (C + C_B)]}{[1 + \omega^2 R_B{}^2 (C + C_B)^2]}$$

and

$$R_p = R_B \frac{[1 + \omega^2 R_B{}^2 (C + C_B)^2]}{\omega^2 R_B{}^2 C^2}$$

and the capacitor Q [eq (15)] is:

$$Q = \frac{1}{\omega R_B C} + \omega R_B C_B \left(1 + \frac{C_B}{C}\right) .$$

The measured capacitance C_p is equal to C if $R_B = 0$ or if $C_B >> C$. However, error is introduced if R_B is finite and C_B is not much greater than C. The area contributing to C_B depends on the bulk resistivity, ρ, the gate metal area, A, and the slice thickness, d. Depending on these parameters, the backside capacitance can fall in the range from:

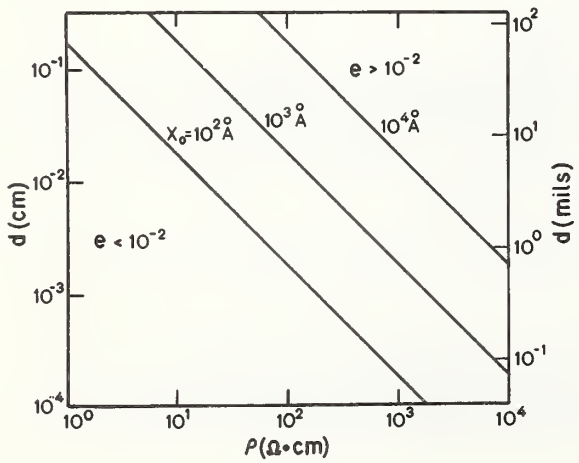


Figure 19. Worst case error plot for capacitance measurements on an MOS capacitor with zero backside contact resistance, steam grown silicon dioxide of three thicknesses, X_o, and a measurement frequency of 1 MHz.

$$\frac{\varepsilon_o A}{X_o} \leq C_B \leq \frac{\varepsilon_o A_B}{X_o},$$

where A_B is the area of the wafer. If the entire backside contributes to C_B, then $C_B >> C$; this should allow a satisfactory measurement. However, because of the spreading resistance effect, it is unlikely that the entire backside is involved. The value of C_B tends toward the lower limit for high resistivity material; this compounds the measurement problem along with introducing additional error through the increased series body resistance. In such cases, it is not clear, without a separate measurement, that one could assume that C_B is large enough not to effect the measurement.

It is evident from the preceding discussion that there are circumstances that could lead to measurement error in a C-V experiment. Obviously, if a measurement is suspected to be in error, it would be necessary to make additional measurements to determine the loss factor. Knowing the Q of the capacitor, one could make the appropriate corrections to derive the actual capacitance. (R. Y. Koyama)

5.2. MOS Bias-Temperature Stress Test

The MOS bias-temperature stress test is a widely used technique to determine the quality of thermally grown silicon dioxide films with particular application to detection of ionic contamination and the presence of interface states. There is, however, wide variation in the stress conditions of bias, temperature, and time used in carrying out the test. An extensive study of the technique has been initiated to survey and evaluate these differences in stress on the measured characteristics of oxide films grown by different process procedures.

To gain familiarity with the technique, preliminary measurements were made on *n*-MOS capacitors fabricated in an early process run (No. 2.1) with the NBS-2 test pattern mask set (NBS Tech. Note 788, pp. 15-17). The capacitors measured were structure 11 of the test pattern. They were fabricated on a (111)-oriented, 10 Ω·cm, *n*-type epitaxial silicon film on an n^+ substrate wafer. Approximately 660 nm of oxide was grown in steam at 1000°C. The capacitor was formed by E-gun evaporating a 0.51-mm (20-mil) diameter aluminum gate to a thickness of about 800 nm over the oxide. The MOS capacitor was annealed in nitrogen at 500°C for 30 min to suppress interface states.

The general procedure for the MOS bias-temperature stress test followed that described in the literature [25, 26]. First, the high-frequency, equilibrium C-V characteristics were measured at room temperature. Because the surface of the wafer was accumulated, it was not necessary to bias the guard ring surrounding the gate during these and subsequent C-V measurements. Next, the MOS capacitor was heated to 300°C for a certain time under bias after which it was cooled, and its C-V characteristics remeasured at room temperature. The hot stage used in this work was specially designed for the purpose (see sec. 5.3.).

The results of measurements on one particular MOS capacitor which has an oxide capacitance, C_o, of 10.5 pF are shown in figure 20. To interpret these curves it is first appropriate to consider the characteristics of an ideal MOS capacitor [26, 27]. If the work function difference between gate metal and semiconductor, ϕ_{ms}, is taken into account, the energy bands of the semiconductor are not bent when the gate voltage $V_g = \phi_{ms}$. The capacitance of the semiconductor for this flat-band condition is [27]:

$$C_{sfb} = A\left(\frac{q^2 \varepsilon_s N}{kT}\right)^{1/2}$$

where A is the area of the MOS capacitor, q is the electronic charge, ε_s is the dielectric constant of the semiconductor, k is Boltzmann's constant, T is the absolute temperature, and N is the dopant density. The measured capacitance, C, is the series sum of the oxide capacitance, C_o, and the semiconductor capacitance, C_s:

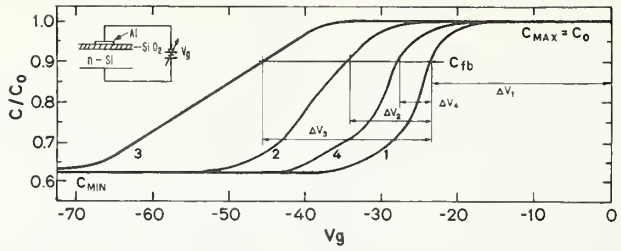


Figure 20. Capacitance-voltage characteristics of an MOS capacitor with poor oxide quality after various bias-temperature stresses. (The capacitance, normalized to the oxide capacitance, C_o = 10.5 pF, is plotted against gate voltage. Curve 1: initial characteristic. Curve 2: characteristic after stress at 300°C for 30 min with V_g = +60 V. Curve 3: characteristic after additional stress at 300°C for 30 min with V_g = +80 V. Curve 4: characteristic after additional stress at 300°C for 20 min with V_g = -80 V. Inset: schematic of MOS capacitor and bias circuit. See text for discussion of curves. Wafer 2105.)

$$C^{-1} = C_o^{-1} + C_s^{-1}. \tag{20}$$

For an n-type semiconductor at very large positive gate voltage, the semiconductor surface becomes heavily accumulated and metallic in nature so that $C \approx C_o$. At very large negative gate voltage, the semiconductor becomes strongly inverted, the depletion layer width in the semiconductor reaches a maximum value, $2\{[\varepsilon_s kT\ \ell n(N/n_i)]/q^2N\}^{1/2}$, and the semiconductor capacitance becomes [27]:

$$C_{s,min} = \frac{A\left(q^2\varepsilon_s N\right)^{1/2}}{2\left(kT\ \ell n(N/n_i)\right)}, \tag{21}$$

where n_i is the intrinsic carrier density. Thus the dopant density can be found by iterati from the measured minimum capacitance by using eqs (20) and (21). This value of dopant den can then be used to calculate C_{sfb} and, in turn, C_{fb}, the total capacitance at the flat ban condition. The difference of the voltage for the flat band condition from its ideal value, ΔV, is interpreted as being due to charge in the oxide. The density of this charge (per un area) is given by:

$$Q_{ss} = \frac{C_o \Delta V}{qA}.$$

Curve 1 in figure 20 is the initial C-V characteristic of the MOS capacitor. In this case the flat-band capacitance is offset by -23.4 V from the ideal value (neglecting the wo function difference) which indicates a fixed oxide charge density near the silicon-oxide interface of 7.7×10^{11} cm^{-2}. This value is in reasonable agreement with results obtained earlier using structure 12 of the test pattern processed on the same wafer (NBS Tech. Note 806, pp. 39-41).

Following the application of +60 V on the gate for a period of 30 min while holding th wafer at 300°C, the C-V characteristic shifted further to result in the curve marked 2. Th shift of -10.7 V from the original curve indicates that an additional 3.5×10^{11} cm^{-2} posit charges moved to the interface. This is due primarily to ion drift in the oxide during the period of the bias-temperature stress. Following an additional stress of +80 V for 30 min

at 300°C resulted in curve 3. In addition to a further shift of the characteristic, there is also the increased dispersion of the curve which is usually attributed to the presence of fast interface states.

A stress of -80 V for 20 min at 300°C resulted in curve 4 which shows partial recovery of the C-V characteristic. These results demonstrate the application of the bias-temperature test to a poor quality oxide such as that obtained in an initial processing run.

(R. Y. Koyama and M. G. Buehler)

5.3. Hot/Cold Stage Development

A hot/cold stage is being developed for use in electrically characterizing planar test structures in wafer form at temperatures other than room temperature. Such a stage is essential for conducting measurements such as the bias-temperature stress test on MOS capacitors (see sec. 5.2.) and thermally stimulated current and capacitance measurements on *p-n* junctions [21] and MOS capacitors (see sec. 4.1.).

The first prototype apparatus for this purpose has been designed and constructed. This apparatus, shown in figure 21, is capable of testing wafers over a temperature range from -182 to 300°C. Both capacitance-voltage and current-voltage characteristics can be measured. The wafer is held on a fixed cold plate/vacuum chuck which also serves as the contact medium for the backside of the wafer. A single-point probe can be positioned within a 5-cm square on the chuck by means of a three-axis manipulator. A stereo microscope (5X eyepiece, 10X objective), mounted on a second three-axis manipulator to allow positioning and focussing, is provided for viewing the probe and wafer during positioning of the probe on the wafer. A fixed hot plate is located below and is electrically isolated from the cold plate/vacuum chuck. The electrical isolation between the chuck and the rest of the system is greater than 10^{13} Ω over the operating temperature range.

Cooling is accomplished by circulating liquid nitrogen through the cold plate; heating is achieved by a 400-W resistive element in the hot plate. The entire stage is housed in a metal box (approximately a six inch cube) which serves as an optical and electrical shield. The box is continuously flushed with dry nitrogen to minimize condensation on the cold parts and to maintain a known ambient over the wafer. An electrically isolated thermocouple attached to the stage is used as the sensing element for an electronic servo-control on the temperature. Maximum heating and cooling rates of 0.50 and -0.45°C/s, respectively, have been achieved. This means that it takes about 10 min to go from room temperature to 300°C and another 10 min to return to room temperature.

The box (or shield), the probe, and cold plate/vacuum chuck are each electrically isolated from each other. This allows a three-terminal capacitance measurement which eliminates the effect of stray capacitance. In addition, both capacitance and current measuring instruments are located as close to the wafer as possible. In operation, the microscope viewing port is covered to prevent errors due to photoconductivity of the specimen.

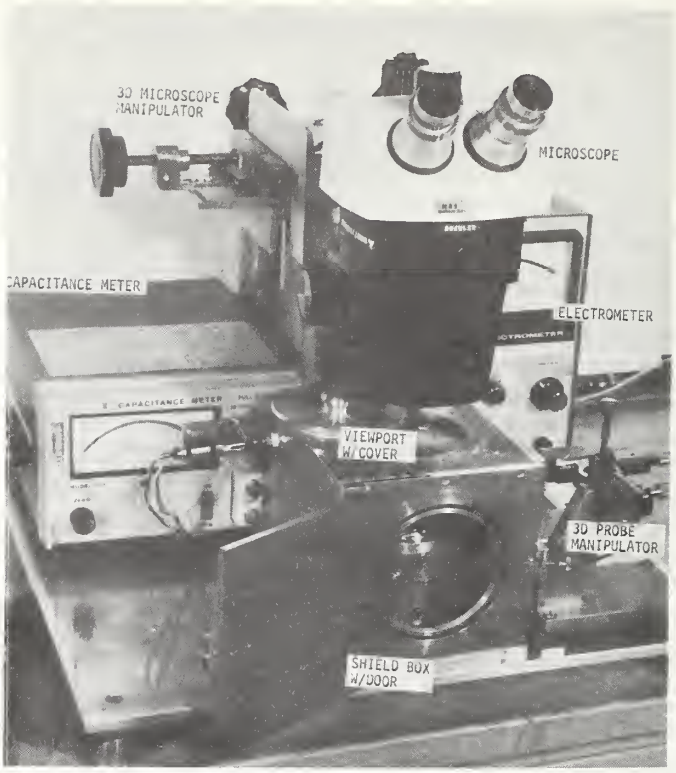
Although this apparatus was successfully used to conduct the bias-temperature tests reported in section 5.2., a faster heating rate and better control of the ambient atmosphere are desired. A second apparatus designed to meet these needs is presently being constructed.

(A. W. Stallings, R. Y. Koyama, and M. G. Buehler)

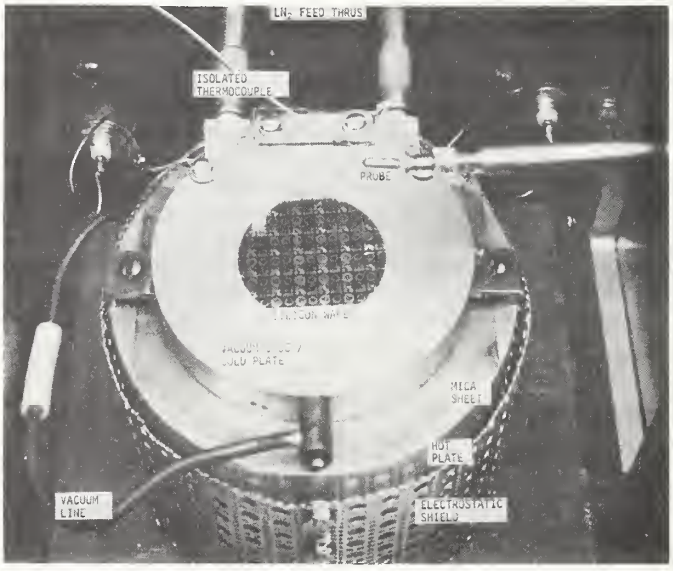
5.4. Ion Microprobe Mass Analysis

Techniques were examined for creating a shallow, uniformly sloped region through the oxidized surface of a silicon wafer. Such a slope is necessary to provide a depth profile measurement because the depth dimension is expanded along the length of the slope. This, however, assumes that the method employed to slope the surface does not alter the impurity distribution. Ion sputter etching is known to redistribute mobile impurities, such as sodium ions, in the oxide. Chemical etching tends to leach or introduce additional impurities at the surface or to do both. Mechanical lapping can damage the surface structure, smear the profile over the taper, and introduce additional contaminants from the slurry. Oxide removal by means of a diamond microtome appears, under examination with a scanning electron microscope, to produce a relatively unharmed surface, but it has not been possible to achieve a slope of less than 30 deg.

None of the above alternatives is completely satisfactory; however, the convenience and cleanliness of ion sputter etching within the microprobe vacuum chamber have been cause for



a. Overall view.



b. Close up of stage with shield box partially removed.

Figure 21. Hot-cold stage for wafer characterization.

it to be further studied. A technique for eroding a symmetrical vee-shaped cut in the wafer specimen was subsequently developed. The specimen was mounted on a stage which is stepped parallel to the ion sputter raster. The rate of translation is adjusted so that the total travel is equal to the raster length in the time required to dig the desired pit depth.

Various pits were sputter-eroded. When the specimen stage was held stationary under either a positive or a negative oxygen ion raster, flat bottomed pits with rounded walls were obtained as a consequence of the Gaussian intensity profile of the primary ion beam. When the specimen stage was translated beneath a positive oxygen ion raster, a characteristic vee-shaped pit was produced. Sides sloping at an angle as low as 10^{-4} radians (10 nm in depth with 100 μm lateral travel) could be obtained.

A series of spot analyses, made by stepping a finely focussed (less than 10 μm diameter) negative oxygen ion beam across the pit, provides the depth profile. In addition to spreading out the depth profile, the shallow pits are useful in reducing the effects of redeposited secondary ions contributed during microprobe spot analysis; this is the so-called "crater-wall effect".

Pits were eroded in a sodium implanted oxidized silicon wafer specimen, obtained from another government research laboratory, (NBS Spec. Publ. 400-1, p. 20) using both a stationary $^{32}O^{+}$ raster and a stationary $^{16}O^{-}$ raster. The sodium depth profiles showed very similar distributions which suggests that migration was not a substantial problem, probably because the peak sodium density was so close to the silicon oxide interface.

Several vee-shaped pits of various maximum depths were eroded into an aluminum implanted oxidized wafer, obtained from a commercial firm, using a translated $^{32}O^{+}$ raster. These pits are symmetrical with respect to depth, and a spot analysis across such a pit should reveal this symmetry in the signal intensity provided no redistribution of material occurs during pit erosion. The aluminum depth profiles obtained were not, however, symmetrical. The asymmetry may be an indication of material redistribution during pit erosion or may result from lateral inhomogeneities introduced during the implantation.

(A. G. Lieberman, D. C. Lewis, and D. E. Newbury*)

5.5. X-Ray Photoelectron† and Auger Electron Spectroscopy

The initial focus of the XPS/AES study of the silicon-oxygen system is directed at the electron density of states and at the core level binding energies of atomically clean silicon under ultrahigh vacuum conditions. As an initial step, the spectrometer was modified to produce ultrahigh vacuum conditions (NBS Spec. Publ. 400-1, p. 20); the residual background pressure in the vacuum system was reduced to approximately 3.5×10^{-10} Torr. A port and a quadrupole mass spectrometer were then added to study the residual gas composition and follow gas phase-solid chemical reactions. The x-ray gun supplied with the instrument was also redesigned and rebuilt to run trouble-free at higher power levels.

Experimentation commenced upon completion of a joule-heated specimen holder for in-situ silicon oxidation. To prevent thermal runaway during oxidation, the alternating heating current through the silicon specimen was also passed through the filaments of several series-connected light bulbs. It was observed at 900°C and 2×10^{-5} Torr pressure that oxygen failed to stick to the clean silicon surface. This situation persisted up to 1150°C; higher temperatures were not attempted because of the problems introduced by the rapid rise in silicon vapor pressure with increasing temperature (10^{-8} Torr at 1265°C; 10^{-6} Torr at 1420°C). A possible explanation for the inhibited oxidation of silicon at reduced pressures may be that silicon monoxide, not silicon dioxide, is formed and immediately sublimated. (The vapor pressure of silicon monoxide is 10^{-8} Torr at only 870°C).

---

*NBS Surface Microanalysis Section, Analytical Chemistry Division.

†X-ray photoelectron spectroscopy (XPS) is also known as electron spectroscopy for chemical analysis (ESCA).

To avoid the sublimation of silicon monoxide from the surface, several runs at about 700°C (2×10^{-5} Torr oxygen) were attempted. An oxygen signal was obtained from the surface which grew, at first, rapidly, but then more slowly. Also, at room temperature, both oxygen and water on silicon were separately adsorbed. The oxygen signals were noted not to occur at identical energies, indicating that different oxygen containing species were formed. As yet the silicon has not been heated in an atmosphere of water vapor to determine whether at high temperatures this difference persists.

Another complication is the formation of silicon carbide over the surface. Air exposed specimens are invariably coated with carbon from absorbed carbon dioxide, carbon monoxide, or pump oil vapors. Such a film does not appear to be an integral part of the silicon or the native silicon dioxide layer. A scan taken immediately after placing the specimen in the spectrometer contained lines due to silicon, oxygen, and carbon, but the sort of spectral structure clearly evident for the silicon and oxygen peaks was not displayed by the carbon 1s line. Most of the carbon and the oxygen were removed by 5 min of bombardment with an 8.5 μA current of 1 keV argon ions. Traces of argon imbedded in the silicon by the sputtering process were also evident in the scan taken after bombardment. Carbon and oxygen reappeared upon heating the silicon specimen to 850°C at 1.5×10^{-9} Torr. At 980°C virtually all of the oxygen was released with a concomitant rise in spectrometer pressure to 6×10^{-7} Torr, and a doubling of the carbon 1s peak intensity. The carbon 1s line now also had a pronounced satellite structure suggesting union with the silicon.

Digital scans over the silicon 2p region revealed the following details. The initial silicon 2p peak (after argon cleaning, but no heating) was fairly symmetrical. After heating to 825°C this peak moved toward lower energies and definite signs of structure began to appear on its lower energy side. At 980°C a second peak became evident, which upon further heating of the specimen to about 1150°C, dominated the now barely detectable silicon 2p substrate signal. Furthermore, no impurity elements other than carbon were noted after these heating experiments, and three hours of argon ion bombardment were required to reduce the carbon to a negligible level. Hence, it may be concluded that some form of silicon carbide was formed having a thickness of at least 5 nm. Whether this carbon is of an external origin, or already present in the silicon and brought to the surface by heating has yet not been resolved.

The specimen surface in each of the runs described above was oriented parallel to the x-ray beam. Under this condition of grazing incidence, the x-rays were likely to become trapped by anomalous refraction in a thin surface layer, neither penetrating into the specimen nor being reflected back out. The trapping should enhance the photo-effectiveness of the x-ray flux and therefore result in greater spectral intensities. This condition of grazing incidence is expected to provide the truest measure of surface composition.

At other angles of incidence, the data are biased in favor of the very outermost surface atoms. Electrons originating from lower strata would have to traverse a greater thickness of material to escape from the surface and enter the spectrometer aperture located at right angles to the x-ray flux. The areas of the XPS peaks and the various area ratios might also be expected to vary smoothly with changing incidence angle, except, perhaps, near the normal angle of x-ray incidence where the specimen shadows itself and electron emission from the specimen edge could occur. This conjectured angular dependence of the XPS spectrum for the silicon-oxygen-carbon system was qualitatively verified by experiment.

It should be emphasized that all of the above results are limited and preliminary in nature. However, methods to obtain clean silicon surfaces have been found, rather large amounts of carbon have been observed in the silicon specimens, and approximate temperature regions permiting oxide growth for the pressures available in the spectrometer chamber have been determined. (N. E. Erickson*, J. T. Yates*, T. E. Madey*, and A. G. Lieberman)

---

*NBS Surface Chemistry Section, Physical Chemistry Division.

6. TEST PATTERNS

6.1. Process Development

The process used previously to fabricate gated p^+n junctions and n-MOS capacitors was modified by interchanging the emitter and base diffusions in order to fabricate n^+p junctions and p-MOS capacitors.* Using this process, test pattern NBS-2 was fabricated on a group of 11 p-type wafers. In the group were six bulk wafers and five p/p^+ epitaxial wafers each having a nominal bulk or layer resistivity of 10 Ω·cm at room temperature. Three of the bulk and two of the epitaxial wafers were lightly gold doped. Wafers 3005 (bulk) and 4006 (epitaxial) were selected as representative of this run and characterized with the results shown in table 11.†

The results in the table indicate that acceptable values of the desired parameters were achieved. The oxide charge was low in these two wafers; however, in some wafers in the group it was as high as 5×10^{11} cm^{-2}. The MOS doping density is lower than the junction doping density. This indicates that the surface (where the MOS capacitor measures) was depleted of boron during oxidization. (J. Krawczyk, R. L. Mattis, T. F. Leedy, and M. G. Buehler)

6.2. Test Structure: Collector Resistor

As a part of a continuing study of the structures on test pattern NBS-2 (NBS Tech. Note 788, pp. 16-17), an analysis was undertaken of the collector resistor, structure number 18

---

*No emitter resistor or transistor structures were formed because the surface dopant densities of the two diffusions were not readjusted to permit the boron density to over compensate the phosphorus density at the surface.

†Dopant densities obtained from junction C-V measurements on other wafers of this group are reported in section 3.2.

Table 11 — Measurements from Two p-Type Wafers Fabricated with *pnp* Process and Test Pattern NBS-2; Run No. 2.5

Test Structure	Quantity Measured	Measured Value		Target Value
		Bulk (3005)	Epitaxial (4006)	
14	Base sheet resistance, Ω/□	3.50	3.45	10 ± 5
16	Metal-to-base contact resistance, μΩ·cm^2	0.057	0.057	< 5
18	Back side contact resistance, Ω	26.2	0.33	< 1
12	Fixed oxide charge density, cm^{-2}	2.2×10^{11}	0.63×10^{11}	$<2 \times 10^{11}$
12	Collector oxide thickness, nm	473.	483.	500 ± 50
12	Dopant density, cm^{-3} (MOS C-V)	1.26×10^{15}	1.21×10^{15}	
6	Dopant density, cm^{-3} (Junction C-V)	1.51×10^{15}	1.43×10^{15}	

on the test pattern. This structure is intended to measure both bulk resistivity, ρ, and backside contact resistance. When combined with dopant densities determined from junction capacitance-voltage (C-V) measurements made on structure 6 of the test pattern, values of resistivity can be plotted against dopant density, and the resulting curves compared with Irvin's curves [9].

A photograph of the collector resistor is shown in figure 22, and the cross-section is shown schematically in figure 23. Not shown in figure 23 is the oxide on the top surface, the thickness of which depends on whether it is over the undiffused n region, the n^+ region, or the p^+ region. These different oxide thicknesses appear as different gray tones in figure 22.

The intended operation of the device involves passing a current I into the top inner ring contact and out the back contact then measuring voltages V_b and V_c as shown in figure 23. The p^+ region serves to prevent conduction between the two n^+ regions in the event that the surface is accumulated. The gold microalloyed back contact acts to form an equipotential surface at ground potential. It was originally expected that the bulk and contact resistances could be separately determined from measurements of V_b and V_c. Experiments have shown, however, that the bulk and contact resistances cannot be so readily separated and that the measurement of homogeneous and epitaxial specimens involve two different types of problems.

When measuring homogeneous specimens, the geometry is such that a three-dimensional model must be employed to accurately determine the resistivity ρ from the resistance R where R is given by $(V_b + V_c)/I$ and is measured between the center contact and the backside contact in figure 23. For the case of an infinite conducting sheet of thickness, W, with a back plane at ground potential and a top circular contact of radius, a, which is also an equipotential surface, R is related to the bulk resistivity, ρ, of the conducting sheet by [28]:

$$\frac{Ra}{\rho} = \frac{1}{4\int_0^\infty \frac{\sin x}{x} J_1(x) \coth \frac{Wx}{a}\, dx} ,$$

where x is a variable of integration and $J_1(x)$ is a first order Bessel function. This equation was solved in the suggested manner [28] to obtain the plot of (Ra/ρ) as a function of W/a shown as the solid line in figure 24. For very thick specimens, for which $W>>a$, (Ra/ρ) approaches the constant value 0.25. For very thin specimens such as epitaxial specimens for which $w<<a$, the one-dimensional model becomes valid such that $R = \rho W/\pi a^2$.

The collector resistors and junction C-V characteristics of two bulk specimens, wafer 306 (3 $\Omega\cdot$cm n-type) and wafer 3006 (10 $\Omega\cdot$cm p-type), were measured. The resistivity was determined by means of Irvin's curves [9] from the dopant density calculated from the junction C-V measurements. The value of a was assumed to be 0.18 mm (7 mils), the radius of the center n^+ diffused region in figure 23. Each specimen is represented by a solid point as indicated on the plot of figure 24. Note that the two points lie substantially below the solid line. The collector resistors and junction C-V characteristics of two epitaxial specimens, slice 2108 (10 $\Omega\cdot$cm n/n^+) and slice 4006 (10 $\Omega\cdot$cm p/p^+) were also measured. As with the homogeneous specimens, the results for each epitaxial specimen was plotted as a point on figure 24. Note that again the data points lie below the solid curve.

There are several possible explanations as to why the four experimental points lie as they do in relation to the theoretical curve. First, shunting by surface currents may be present. This has been observed on some specimens by noting that the potential on the top surface approaches zero less rapidly than expected as the distance from the center n^+ diffused region is increased. Such shunting resistance would cause R to appear to be less than it should be and move the data points down from the theoretical curve.

Second, contact resistance at either the top or back contact may be present. If present, contact resistance would cause R to appear larger than it actually is, thereby moving the data points up from the theoretical curve.

Third, in the measurement of epitaxial specimens, the layer thickness must be accurately known. This is a problem since measurement by infrared reflectance [29], angle-lap-and-stain

Figure 22. Photomicrograph of collector resistor, test structure 18 of test pattern NBS-2. (The wide white circles are the aluminum metallization, the dark gray circles are oxide over the n^+ diffused regions, the light gray circle is oxide over the p^+ diffused channel stop, and the medium gray circles are oxide over the undiffused n-type substrate. Magnification: ∿ 116 X.)

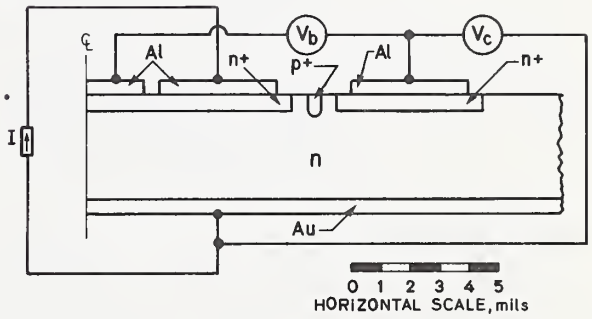


Figure 23. Cross sectional diagram of collector resistor structure with a schematic of the measuring circuit. (1 mil ≃ 25 μm.)

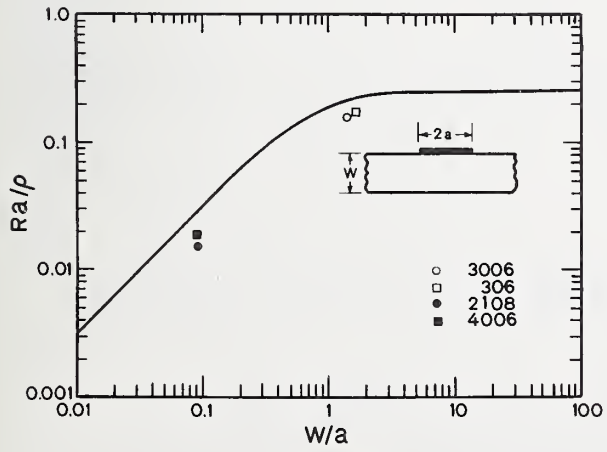


Figure 24. Normalized resistance-resistivity ratio as a function of normalized sheet thickness. (Solid curve: theory; open points: experimental data on bulk wafers; closed points: experimental data on epitaxial wafers.)

[30], and spreading resistance [31] often give differing results. Any error in thickness would result in a horizontal displacement of the data points from the theoretical curve.

Fourth, the model assumes that the top contact is an equipotential surface. In fact the potential is applied by means of a probe which contacts thin aluminum film and an n^+ diffusion both of which have finite sheet resistance. If the top contact is not an equipotential, the current would be crowded into the region under the probe tip. Such current crowding would cause R to appear larger than it actually is, thereby moving the data points up from the theoretical curve.

Fifth, since the resistivity was calculated using Irvin's curves [9], any error in these curves would cause the data points to shift up or down with respect to the theoretical curve.

It cannot be determined to what extent each of these five sources of error was present from measurements on the collector resistor in test pattern NBS-2. A new test pattern is being designed which includes five structures which are modifications of the present collector resistor. The study of these five structures is expected to lead to a fuller understanding of the current patterns in such devices. This in turn is expected to permit adequate control of all the sources of error so that the relation between dopant density and resistivity can be established over a wide range of resistivities.

(R. L. Mattis, A. G. Lieberman, R. Y. Koyama, and M. G. Buehler)

6.3. Test Pattern: Charged-Coupled Device

The charge coupled device (CCD) was chosen for study, because it is very sensitive to fixed oxide charge Q_{ss} and fast interface states N_{ss}. The object of this study is to explore the use of the CCD as a process control test structure by intercomparing the results obtained from it and a variety of other conventional test structures.

The test pattern includes a variety of test structures on two rectangular dice. One of the dice is devoted to four charge-coupled devices of different size. The other die contains n-channel IGFETs with either thin (gate) or thick (field) oxides, MOS capacitors over gate and field oxides, a gated n^+p diode, a metal to n^+ contact resistor (NBS Spec. Publ. 400-1, pp. 22, 24-25), a gated n^+ van der Pauw resistor (see sec. 6.4.), and a bulk and backside contact (substrate) resistor.*

The CCDs were designed with a 2.5 μm interelectrode gap. Layouts for masks for both dice are being computer generated. The full composite layout of the die containing the structures other than the CCDs was completed; the layout of the CCD die, delayed by software inconsistencies in the computer aided design system, is nearing completion. Six different masks are required to fabricate the test pattern wafers. It is intended to employ aluminum gate technology technology.

The correlation of results obtained from the CCDs with results obtained from other test structures is intended to take the following form. The interface state density can be determined from the CCDs [32] and compared to values obtained from the IGFETs [33], the MOS capacitors [34], and the gated n^+p junction [35]. Likewise, the fixed oxide charge can be obtained from the CCDs [36] and compared to values obtained from the IGFETs [37] and the MOS capacitors (see sec. 5.1.). In addition, a CCD structure can be operated as a long channel IGFET, a gated diode, and an MOS capacitor and the results of measurements on the CCD structure compared with those on conventional test structures of the same family.

(I. Lagnado† and M. G. Buehler)

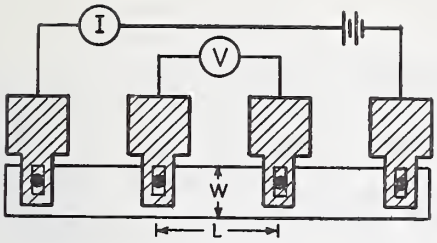
6.4. Test Structures: Sheet Resistors

Various four-terminal test structures for measuring the sheet resistance of layers diffused into opposite type substrates are depicted schematically in figure 25. The structure

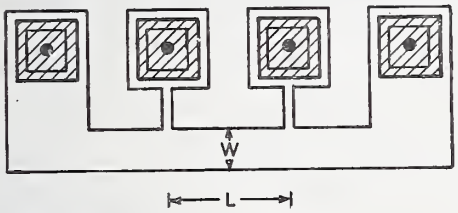
---

*This structure is a slightly improved version of the collector resistor on test pattern NBS-2 but not as advanced as the five structures referred to in section 6.2.

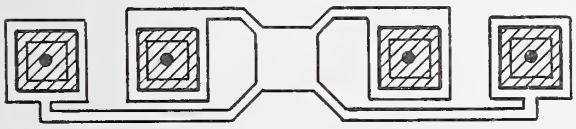
†Naval Electronics Laboratory Center, San Diego, California 92152.



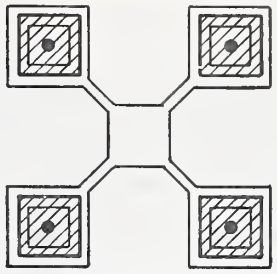
a. Rectangular bar with metal contacts.



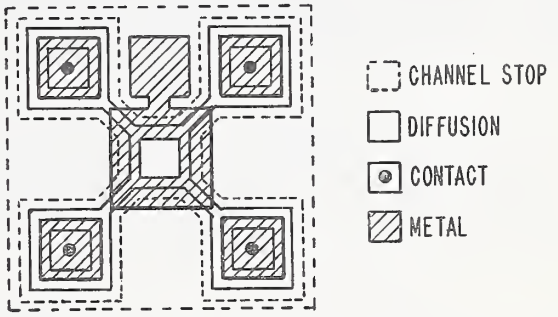
b. Rectangular bar with diffused contacts.



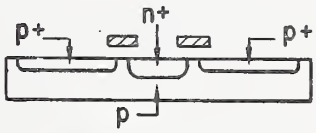
c. van der Pauw structure with linear contact array.



d. van der Pauw structure with square contact array.



e. Gated van der Pauw structure (top view).



f. Gated van der Pauw structure (sectional view).

Figure 25. Diffused layer sheet resistors with Kelvin contact schemes.

with metal contacts (fig. 25a) suffers because the metal taps act as shorting bars giving too low a voltage-current ratio. In addition, to calculate the sheet resistance, R_s, it is necessary to determine the ratio of the contact spacing, L, to the resistor width, W, from direct measurement of L and W. This ratio is affected by variations in the etching of the diffusion window. The structure with diffused contacts (fig. 25b) is an improvement in that the voltage-current ratio is measured by a true four terminal method, but the sheet resistance calculation again depends on the L/W ratio. The van der Pauw structure (fig. 25c) is a further improvement for the surface geometry need not be measured to find the resistivity [38]. Another advantage of this structure is that the main diffused region can be made the same size as that found in actual devices. For this reason the structure can be used to obtain a precise sheet resistance measurement of a device region such as a transistor base.

An additional effect must be taken into account if, as is frequently the case with *n*-type diffusions into *p*-type substrates, the surface of the substrate is inverted (channeled) due to positive charge in the oxide and boron depletion effects during oxidization. Channeling, which tends to increase the effective surface area of the diffused region, is not usually important for *p*-type diffusions into *n*-type substrates because the surface of the *n*-type substrate is usually accumulated due to positive charge in the oxide and phosphorus pile-up effects during oxidization. To overcome the effects of channeling, gates and channel stops are required. These may be most conveniently added to the van der Pauw structure if it is

first rearranged (fig. 25d). The gated van der Pauw structure with channel stops is shown in figure 25e. The cross sectional view through the center of this structure (fig. 25f) shows the p^+ diffusions which act as channel stops and the gate electrode which rests over an oxide film (not shown) and which can be biased to accumulate the surface of the p-type substrate between the n^+ diffusion and the channel stops.

When monitoring a production process, the diffused contact structure (fig. 25b) and the van der Pauw structure (fig. 25c) can be used together to separate sheet resistance changes from variation in the etching of the diffusion window. The voltage-current ratio of the former structure is equal to $R_s L/W$, while geometrical factors can be excluded in the latter structure. Thus a comparison of measurements made with these two structures can resolve etching variations (W changes) from sheet resistance changes. It should be noted that these two test structures are also useful for measurements on other types of resistors such as nichrome or other thin film resistors. (M. G. Buehler)

7. PHOTOLITHOGRAPHY

7.1. Photomask Metrology

A program was initiated to determine the optical and metrological requirements and problems associated with the manufacture and use of photomasks for semiconductor processing. In addition to a review of the pertinent scientific and report literature on photomask technology, visits are being made to technical personnel responsible for research and production of both photomasks and integrated circuits. So far 12 companies have been visited. From these first visits it was tentatively concluded that there are several optical and measurement problems common to both photomask and integrated circuit manufacturers:

1. the inability to measure line widths in the 1 to 5 μm region with an associated accuracy of better than ±0.25 μm,

2. the lack of an objective method of defining and locating a physical edge of a line or other photomask pattern geometry, and

3. differences of line width measurements obtained using the image shearing and filar attachments to conventional microscopes.

The conclusions reached were that before 1 μm lines can be manufactured uniformly over a 2 or 3 in. (51 or 76 mm) diameter wafer, line width measurement standards must be established in the 1 μm range. Because of the large investment already made by the industry in optical measurement equipment these standards must be compatible with the existing measurement equipment. (J. M. Jerke* and D. B. Novotny)

7.2. Automated Photomask Inspection

A study was undertaken to review and assess the state-of-the-art of available technologies for automated photomask inspection and to assess the feasibility of applying these technologies to wafer surface inspection. To carry out the study, visits are being made to representative integrated circuit facilities, photomask manufacturers, inspection equipment manufacturers, hard surface photomask blank suppliers, and photomask aligner manufacturers. To date 22 organizations have been visited.

Preliminary indications are that major problems exist in the manufacture of acceptable photomasks as a result of the presence of visual defects such as pinholes, bridgings, scratches, cracks, and glass chips; difficulty in achieving sufficient registration between photomasks in a series; difficulty in maintaining critical device dimensions within specified tolerances; and inconsistancies in the quality of blank photoplates.

Five systems under development or potentially useful for automated photomask inspection have been identified. One, most suitable for dimensional metrology, utilizes a laser-produced diffraction pattern to measure line widths or gaps in an opaque area 1.5 to 25 μm in size with a claimed repeatability of ±0.012 μm. This system appears to be as fast as the methods, such as those based on use of an image shearing or filar eyepiece in an optical microscope, now used to measure critical dimensions and has the advantage of removing the operator subjectivity found in these methods (see sec. 7.1.). However, the system is not suited for scanning a photomask for defects.

The other four systems utilize various comparative techniques to inspect for dimensional errors, defects, or registration. The most rapid is based on a spatial filtering technique. A filter is made of the optical Fourier transform of an array pattern. This filter is then used in the Fourier image plane to subtract all the correct information from the transform of a second array allowing only the defects to be present in the reconstructed image.

In another rapid system, the photomask patterns are scanned with a microdensitometer. The information is digitized and stored in a computer memory. Differences between patterns are identified by data comparison. This system appears to be most suited for analyzing registration of successive mask layers.

In a third system, the photomask is scanned with a split laser beam so that two different arrays are scanned simultaneously. The two signals are compared and differences in the array patterns register as defects.

---

*NBS Optics and Micrometrology Section, Optical Physics Division.

In the fourth system an image dissection camera views the array pattern through a microscope. The photomask is stepped across the field of view of the microscope in very small (∿10 μm) increments. The image information is digitized and stored in a computer memory. The digitized information from successive arrays is compared with the stored data to check for dimensional errors or defects. (D. R. Ciarlo*, P. A. Schulz*, and D. B. Novotny)

7.3. Photoresist Illumination

An analysis of the usefulness of absolute radiometric measurements to standardize and control photoresist exposures was made. The data used in this analysis were approximate values for parameters such as the temperature and temperature fluctuation of a high pressure mercury lamp, the effect of aging of such a lamp, the possible skewing of the relative line intensities of the actinic radiation, the relative absorbancies of photoresists, and the spectral sensitivities of commercially available radiometers used to measure the lamp outputs. It was concluded from this brief study that absolute radiometry would offer little help in solving photoresist exposure problems and that exposure problems can be reduced by the use of a light integrator to regulate the exposure. (E. Zalewski† and D. B. Novotny)

7.4. Photoresist Spinner Dynamics

The repeatability of a method [39] for measuring the rotational acceleration and velocity of a wafer during the spinning process used in photoresist coating, being considered for adoption by ASTM Committee F-1 on Electronics, was tested. This method consists of etching a radially segmented pattern onto an oxidized silicon wafer. This pattern is similar to the pattern previously described (NBS Tech. Note 592, pp. 46-47) with the addition of several concentric bands on the periphery of the wafer. The patterned object is aligned on the spinner chuck such that the center of the pattern coincides with the center of rotation of the chuck; the alignment is made using the circular bands on the periphery of the wafer. A small spot of light is then focussed on the wafer near the periphery of the segmented portion of the wafer. A photosensor detects the passage of each segment boundary as the spot of light is alternately reflected and absorbed. The output of the photosensor is displayed on one channel of a two-channel oscilloscope. The other channel is connected to a time-mark generator. The oscilloscope display is photographed and the times required for the pattern to rotate through arcs corresponding to successive segments are measured. From these times, the acceleration is calculated. A second photograph of the oscilloscope display is taken after the spinner attains final velocity. From this photograph the final angular velocity is calculated.

The procedure of this method was repeated several times with a photoresist spinner that was spinning at a constant velocity. The oscilloscope signals were photographed and measured with a traveling microscope. The single instrument, single operator relative sample standard deviation of the velocity measurements was found to be less than 4 percent of the calculated average velocity. It was also shown that failure to align the wafer pattern center with the axis of rotation of the spinner chuck results in measured instantaneous velocities that have a sinusodial variation with a period corresponding to one revolution of the patterned wafer. (D. B. Novotny)

---

*Lawrence Livermore Laboratory, Livermore, California 94550.

†NBS Optical Radiation Section, Heat Division.

8. EPITAXIAL LAYER THICKNESS

8.1. MOS Capacitance Methods

The need for methods for measuring epitaxial layer thicknesses in the range $\lesssim 2$ μm was identified at a recent workshop on measurement problems in integrated circuit processing and assembly [40]. As a means of addressing this need, two MOS measurement methods are being evaluated and, in the range of layer thicknesses where such comparisons are possible, compared with existing methods. These methods, with some limitations, are applicable to layer thicknesses in the above range when the layer and the substrate are of the same conductivity type and when the substrate is much more heavily doped than the layer.

The MOS methods make use of the high-frequency capacitance-voltage (C-V) characteristic of a metal-oxide-semiconductor capacitor as shown in figure 26 for an *n*-MOS capacitor. Under quasi-static conditions the capacitance consists only of the oxide capacitance C_o, at large positive voltages (point B) and of a series combination of the oxide and semiconductor depletion layer capacitances, C_∞, at large negative voltages (point F). If the voltage is changed rapidly from a large positive value (point B) to a large negative value (point D) the semiconductor is driven into deep depletion and the capacitance becomes lower than C_∞ [41]. If the voltage is fixed at a large negative value after such a rapid change, the capacitance relaxes slowly to the steady-state value C_∞, following the path from D to F. If the space charge region in deep depletion is wider than the thickness of the epitaxial layer, there is a pronounced discontinuity in moving from point B to point D on the C-V characteristic as the depletion layer passes into the substrate at a transition capacitance, C_t (point E'). In addition there is a pronounced discontinuity (also at C_t) in the capacitance-time (C-t) relaxation characteristic (equivalent to point E on the path from D to F on the C-V plot of fig. 26).

The latter discontinuity is employed in the step-relaxation method. The capacitor is driven into deep depletion by applying a voltage step (point B to point D) and the relaxation (point D to point F) is monitored on an x-t recorder. A typical C-t relaxation characteristic is shown in figure 27. Following a step in applied bias from +100 V (point B) to -100 V (point D) at time t = 30 s, the capacitance relaxes to the transition value, C_t, and then, with a different rate, relaxes to the steady-state value, C_∞. The epitaxial thickness, t_{epi}, is determined from the capacitance at the transition, C_t; the oxide capacitance, C_o; and the device area, A:

$$t_{epi} = \varepsilon_s A\left(\frac{1}{C_t} - \frac{1}{C_o}\right) \tag{22}$$

where ε_s is the dielectric constant of silicon.

An alternative method, the ramp-voltage method, involves driving the MOS capacitor into deep depletion using a rapid voltage ramp rather than a voltage step. In this case the C-t plot, monitored on an x-t recorder, is equivalent to the C-V plot of figure 26 and the transition at point E' is used to determine C_t. From the corresponding C_t value, t_{epi} can be calculated from eq (22). A typical C-t plot for this method is shown in figure 28 for the same capacitor as was used to obtain the relaxation characteristic (fig. 27). Note that the value for C_t in the two cases is the same and also that the time scale in the ramp-voltage method is much shorter than that in the step relaxation method.

As a preliminary test of the consistency of the MOS methods, measurements were made on guarded 0.51-mm (20-mil) diameter MOS capacitors on 5.1-mm (200-mil) centers. The capacitors were formed on six oxidized *n*-type epitaxial layers deposited on n^+ substrates by metallizing the topside with aluminum, using the metal mask from test pattern NBS-2 (NBS Tech. Note 788, pp. 15-17), and the entire backside with gold. On each wafer devices along the diameter perpendicular to the flat were designated devices 1 through 8. Epitaxial thickness was measured by the step-relaxation method on several selected devices on each wafer with results as given in table 12. The values are seen to be consistent within each wafer. A measurement on a single device on each wafer by the ramp-voltage method confirmed that the two methods

generally agreed to 8 percent or better although in some instances it was necessary to slow down the capacitance transient by cooling the slice to about 0°C.

A fundamental limitation of these methods is imposed by the breakdown voltage and the consequent limit on depletion depth which can be achieved. Sze gives a plot of maximum depletion depth as a function of dopant density for one-sided abrupt junctions [42]. It appears that the MOS methods should be applicable for layers up to 2 μm thick (beyond which other methods are applicable) with dopant densities of 1.2×10^{16} cm^{-3} or less. For layers with larger dopant densities, the maximum thickness which can be measured is limited by the breakdown voltage to values less than 2 μm. (R. L. Mattis)

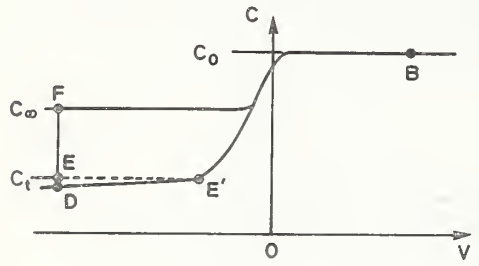


Figure 26. High-frequency capacitance-voltage characteristic of an *n*-MOS capacitor. (See text for discussion of marked points.)

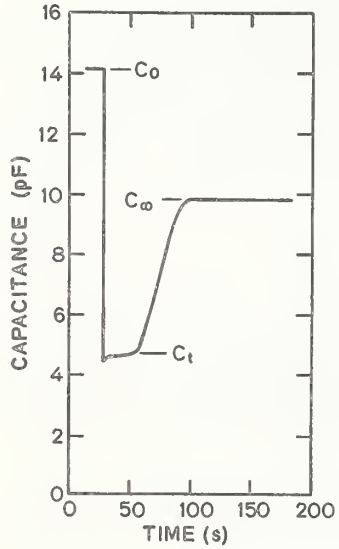


Figure 27. Relaxation characteristic of an MOS capacitor formed on a thin epitaxial layer illustrating the step-relaxation method for measuring epitaxial layer thickness.

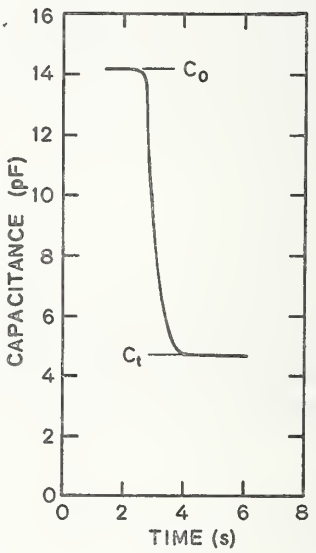


Figure 28. Deep depletion characteristic of an MOS capacitor formed on a thin epitaxial layer illustrating the ramp-voltage method for measuring epitaxial layer thickness.

Table 12 — Epitaxial Layer Thickness in Micrometres Measured on MOS Capacitors Along Slice Diameters by the Step-Relaxation Method

Device No.	Slice Number					
	2301	2302	2351	2352	2203	2204
1		2.80	1.49		5.03	
2		2.87		1.47		5.17
3			1.47	1.47	4.86	5.14
4	2.03	2.95	1.47			
5	2.12			1.45	4.52	
6	2.03	3.13	1.40			
7				1.42	4.98	
8	1.93	3.08	1.29	1.36	4.51	

9. WAFER INSPECTION AND TEST

9.1. Flying-Spot Scanner Development

Assembly of the optical flying-spot scanner (NBS Spec. Publ. 400-1, p. 31) is continuing. Almost all of the commercially available components required have been received, and the necessary special jigs and fixtures have been designed and constructed.

The design of the scanner has been modified to allow the scanning light reflected from the surface of the integrated circuit to be detected. This will allow the operator to mix this signal with that resulting from photoexcitation of the integrated circuit and present on the viewing screen a composite image useful for locating the electrical response of the integrated circuit relative to its surface topology.

The helium-neon laser and the scanning mirror assembly have been mounted on an optical bench and adjusted to produce a raster with the mirrors driven by triangular waveforms. The triangular waves are supplied by variable-frequency signal generators which also produce square waves in synchronism. The negative halves of the square waves are used for oscilloscope blanking: they are mixed and inverted by a simple transistor OR circuit and then applied to the blanking input of the oscilloscope monitor screen. Rudimentary images were displayed on the monitor screen when transparencies were placed between the unfocussed scanning laser beam and a photocell, with the photocell connected to the Z-axis input of the monitor.

(G. J. Rogers and D. E. Sawyer)

9.2. Scanning Electron Microscope Damage Study

Microelectronic devices when viewed in a scanning electron microscope (SEM) can undergo damage due to exposure to the electron beam. To initiate a study of this type of damage, measurements were made to determine the total electron beam current as a function of the various machine settings. Due to the design of the electron optics of an SEM, beam current is a function of accelerating voltage and of the currents in the condenser and objective lenses.

Figure 29 shows a schematic of the circuit which was used to collect and measure the beam current. The beam was directed at a standard specimen support which was electrically separated from the main part of the machine fixtures by an insulated holder. In order to insure collection of the entire beam, a Faraday cage was added to the stub but electrically isolated from it. The magnitude of the negative bias voltage applied to this cage was such that an increase in bias voltage did not produce an increase in measured current.

For each of five accelerating voltages (30, 20, 10, 5, and 2.5 kV) the beam current was measured as a function of objective lens current at various settings of condenser lens current. These were plotted as a family of curves at each accelerating voltage. Figure 30 shows the curves for an accelerating voltage of 20 kV. It should be noted that the lens current ranges shown represent the limits of adjustment on this particular SEM. For other accelerating voltages, the curves were similar except that at lower accelerating voltages, the range of beam currents was smaller. Not plotted are certain anomalous values of beam current which were as high as several microamperes. These were found at the lowest lens current settings and appear to correspond to a case of an almost uncontrolled beam.

(W. J. Keery and K. O. Leedy)

9.3. Scanning Electron Microscopy - Voltage Contrast Mode

Investigations were made into possible means of extending the voltage contrast capabilities of the SEM. As a result of conversations with other operators and a survey of several articles, the consensus would appear to be that voltage differences of one to a few tenths of a volt are generally about the present usable limits of resolution. These differences are between parts of a circuit, not along a single conductor or resistor. Some articles have shown more sensitive results but usually for rather specialized cases and geometries.

One approach which offers some promise of increasing the detectability of small voltage differences is that described in a paper by Yakowitz, *et al.* [43]. Plans for a cylindrical detector based on the design described in the paper were drawn up* and the detector fabricated.

*The assistance of H. Yakowitz, NBS Metallurgy Division, in developing the detector for this study is gratefully acknowledged.

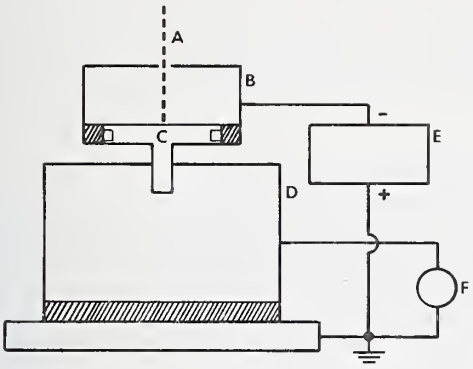


Figure 29. Configuration of the beam current measuring equipment. (The shaded regions are electrical insulation.)

A Electron beam
B Faraday cage
C Specimen support
D Stub base
E Power supply
F Current meter

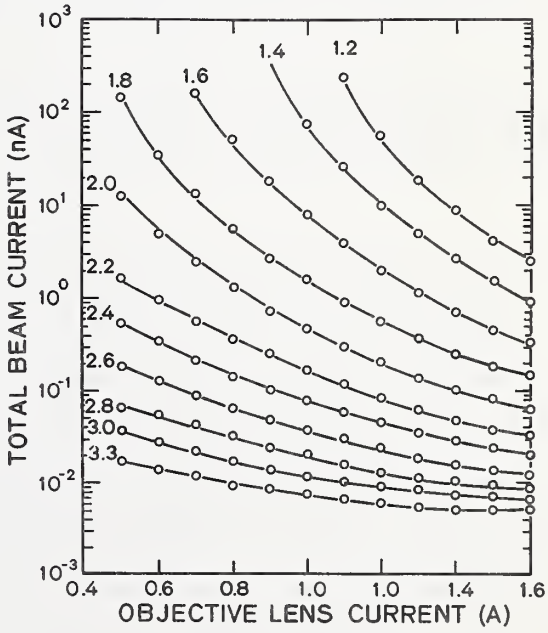


Figure 30. Beam current as a function of objective lens current for an accelerating voltage of 20 kV and various values of condenser lens current. (The number on each curve is the condenser lens current in amperes.)

Among the modifications made to the original design were those necessitated by the very different design of the specimen chamber and stage of the SEM used in the present study from the SEM used in the original work. The present design includes a mounting bracket which will permit rather easy removal and replacement of the detector to permit regular SEM observations as required. The mounting also permits the specimen being investigated to be oriented with respect to the detector through the use of the regular X, Y, and rotation controls on the stage. (W. J. Keery and L. M. Smith)

9.4. Scanning Electron Microscopy - Electron Beam Induced Current Mode

Analytic work on electron-hole pair generation in silicon structures has been initiated to complement observations of electron beam induced current (EBIC) signals which can be obtained from some semiconductor devices scanned in the SEM. Such signals can reveal a wealth of information about the efficacy of device fabrication and about localized device operation. As the first step in the work, a search of the EBIC literature has been made. From the search it appears that one may derive simple, yet useful, graphical relationships between the shape and magnitude of the electron-hole generation rate function within an aluminum-silicon dioxide-silicon sandwich of arbitrary constituent-layer thicknesses, and the SEM accelerating voltage and beam current. (D. E. Sawyer)

Preliminary experimental work with the scanning electron microscope operating in the EBIC mode illustrated a need to extend the usable current range of the standard instrument module. These modifications have been completed. (W. J. Keery)

10. INTERCONNECTION BONDING

10.1. Ultrasonic Bonding to Thick Film Copper with Aluminum Ribbon Wire

Several power series were run to determine the bondability of 38 by 13 μm (1.5 by 0.5 mil) aluminum (1% silicon) ribbon wire to thick film copper on a ceramic substrate. All bonds in the power series were made on a single level substrate with a bond-to-bond spacing of 1.5 mm (60 mils) and a loop height of 0.38 mm (15 mils). A statistical set-up procedure [44] was used for the evaluation; the bonding force ranged from 25 to 30 gf (0.24 to 0.29 N) and bonding times ranged from 45 to 55 ms. The tool tip vibration amplitude was varied from 0.6 to 2.5 μm (25 to 100 μin.) for the first bond and held constant at 1.3 μm (50 μin.) for the second bond by appropriate settings of the bonder power. The bonding tool had a foot length of 0.11 mm (4.5 mil). The pull strength of bonds made with a typical set of bonding parameters which produced satisfactory bonds on unetched substrates is shown in figure 31. In this series, the bonding force and time were 29 gf (0.28 N) and 45 ms for the first bond and 25 gf (0.24 N) and 50 ms for the second bond. The wire broke or lifted off at the first bond in all cases. The thick film copper substrates had been stored for four months in air before bonding. One substrate showed a dark color typical of oxidation or other contamination of the copper film. However, only a small difference in bonding characteristics or resulting pull strength was observed between the discolored substrate and a substrate which showed no discoloration.

An experiment was made to determine whether oxidation of the thick film copper after bonding results either in undercutting of the bonded region, causing lift off at low stress, or in the formation of weak intermetallic compounds. One substrate was cleaned in detergent and etched in a ferric chloride solution for 10 s. Bonding was done immediately after etching. A bonding time of 45 ms and a bonding force of 29 gf (0.28 N) were used. First bonds were made with three different power settings. After bonding to the etched surface, every second bond was pulled to destruction. The substrate was then heated for 168 h at 155°C in air. The copper surface showed a dark brown color, typical of oxide formation. The remaining bonds were pulled. The pull strength decreased slightly as a result of wire annealing and the standard deviation improved as seen in figure 32. After the heat treatment, typical bonds were examined with a scanning electron microscope to search for intermetallic compounds which might have formed during the heat treatment. Scanning electron micrographs of a first bond made with large tool tip vibration amplitude and a second bond made with intermediate tool tip vibration amplitude are shown in figures 33 and 34 respectively. No evidence was found of intermetallic compound formation.

These experiments suggest that aluminum wire can be satisfactorily bonded to thick film copper and used in typical hybrid circuit processing environments. Thus, for many hybrid circuit applications it may be possible to replace gold thick films with less expensive copper thick films. (H. K. Kessler, C. A. Main, and K. O. Leedy)

10.2. Ultrasonic Bonding of Small Diameter Platinum Wire

The ultrasonic bondability of 25 μm (1-mil) diameter platinum wire was further investigated. Bonds of reasonable strength could be made to a number of thick and thin film substrates using bonding parameters similar to those for gold wire (NBS Spec. Publ. 400-1, p. 35). However, when bonding to thin-film aluminum integrated-circuit type metallization, about 800 nm thick, the bonds often failed in a pull test by pulling a piece of silicon out of the substrate. This indicated severe damage to the substrate that is rarely seen in small diameter aluminum or gold wire bonds. In addition it was observed that the ultrasonic energy could be applied to a bond for several seconds (*vs.* about 50 ms for a normal bond) without greatly increasing the wire deformation past about 1.5 wire diameters. Some erratic variation in the wire bondability also appeared from time to time. A discussion of the metallurgical properties of this wire with the manufacturer revealed that platinum is known to work harden very rapidly. This would explain most of the above observations. Later, very soft platinum wire, annealed in burn-out tests, was used to repeat the experiments. This wire was very difficult to handle and occasionally broke in or near the wire clamp, requiring the operator to rethread the tool. Although some improvement in bonding to metallization over silicon was noted, silicon chunks were still occasionally pulled out with the bond. This suggests that application of platinum wire in ultrasonic bonding to silicon device metallization is not likely to be satisfactory. (G. G. Harman and C. A. Main)

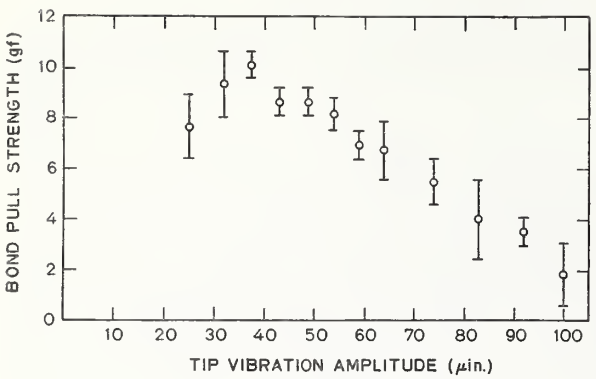


Figure 31. Pull strength of aluminum (1% silicon) ribbon wire bonded to thick film copper. (The variable is the bonder power, expressed in terms of tool tip vibration amplitude used in making the first bond (1 μin. ≈ 25 nm). Other bonding parameters were held constant; see text for values. The error bars represent one sample standard deviation above and below the mean for each group of 10 to 15 bonds.)

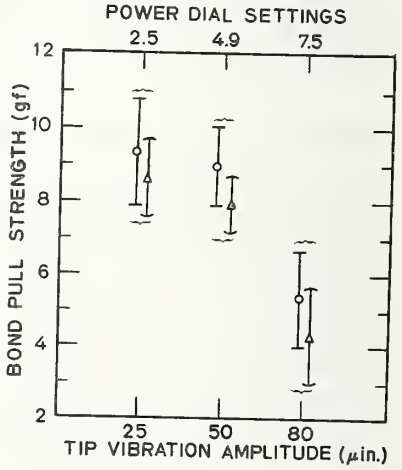


Figure 32. Pull strength of aluminum (1% silicon) ribbon wire bonded to etched thick film copper before (O) and after (Δ) heating in air at 155°C for 168 h. (The error bars represent one sample standard deviation above and below the mean for each group of 10 to 15 bonds. The data points have been displaced horizontally for clarity.)

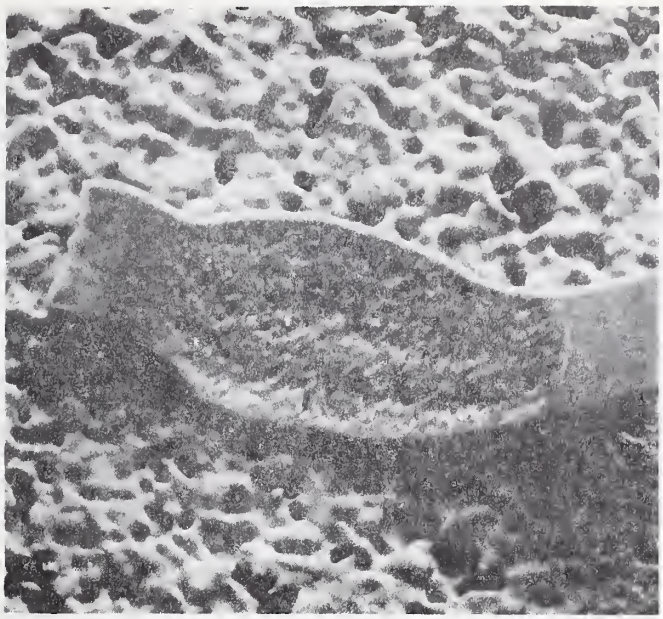


Figure 33. Scanning electron micrograph of first bond of aluminum (1% silicon) ribbon wire made to etched thick film copper with high power after heating in air at 155°C for 168 h. (Magnification: ∿ 400 X).

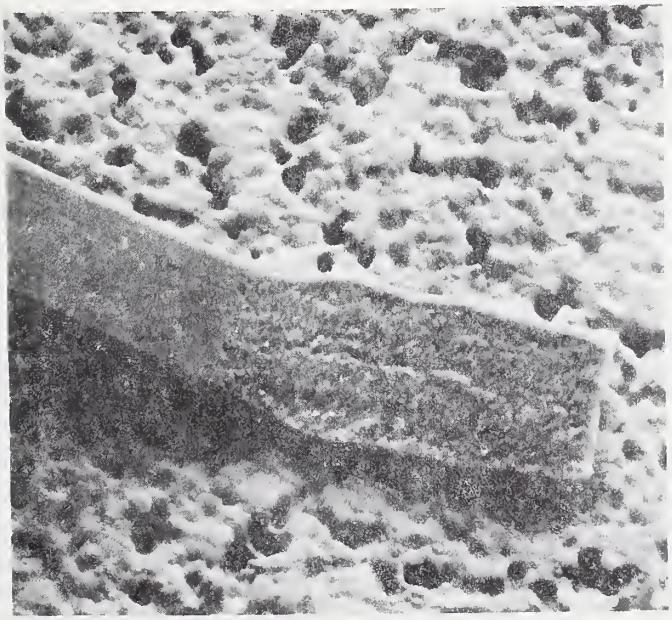


Figure 34. Scanning electron micrograph of second bond of alumimum (1% silicon) ribbon wire made to etched thick film copper with intermediate power after heating in air at 155°C for 168 h. (Magnification: ∿ 400 X).

10.3. Automatic Puller for Beam Lead Bonds

An instrument was built to pull beam lead bonds made by either thermocompression or ultrasonic bonding techniques. The puller was designed to pull bonds over a wide range of force in a series of steps.

Beam lead devices are pulled by means of the hot-melt-glue technique (NBS Tech. Note 488, pp. 22-24). A wire loop is heated to melt a thermoplastic resin which is then brought into contact with the beam lead device. Upon cooling, the wire loop is firmly attached to the beam lead device and a pull test may then be performed. The pull strength in grams force is recorded by amplifying and then plotting the signal from a strain gauge on an x-y recorder. The length of the straight line in the y direction is proportional to the output signal and hence to the pull strength. After each bond is pulled and the result recorded, the recorder is advanced along the x-axis for the next bond to be tested. The instrument may also be used to pull wire bonds, if the wire loop is replaced by a wire hook.

The bond puller is shown in figure 35 with its associated electronic equipment except for the x-y recorder. To operate the bond puller, the slide drive motor (F) is started. The slide with the transducer (G) moves down and presses against the leaf spring (I) attached to a beam (D) which transmits the force to the pulling head (A). After the bond breaks on the device tested, the slide with the transducer returns to the reset position and is then ready for pulling the next bond or beam lead device. The carrier (E) and the leaf spring (I) can be moved to vary the force transmitted to the bond by a factor of 2. The basic instrument has a force range of 0 to 15 gf (0 to 0.15 N). By mounting adaptors on the botton of the load cell transducer, force ranges up to 0 to 2,200 gf (0 to 21.6 N) can be achieved. With a larger cross-sectional area beam, the applied force could be increased still more.

Since it is frequently desirable to conduct pull test experiments at pull angles other than normal to the substrate, a two axis, variable angle substrate holder, illustrated in figure 36, was designed. The basic component was the gear mechanism of an astrocompass. With this holder, the device or bonding substrate may be positioned accurately so that bonds can be pulled in a consistent, reproducible manner. (H. K. Kessler)

10.4. Non-Destructive Wire Bond Pull Test

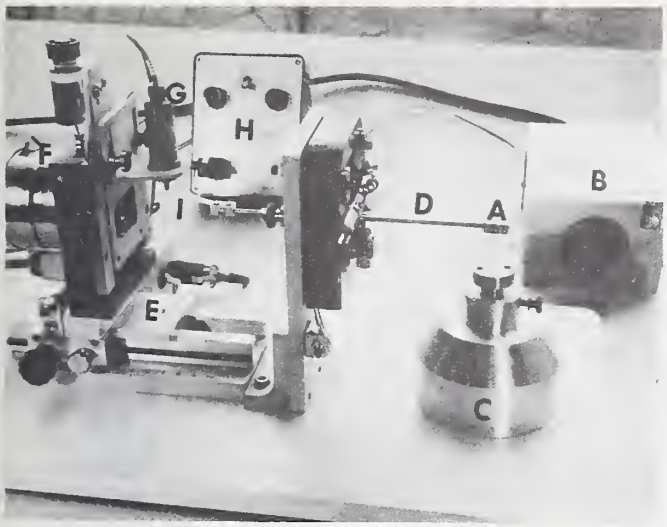
In view of the fact that non-destructive bond pull (NDP) tests are often used in high-reliability production lines, the metallurgical and statistical rationales for the test developed, and maximum permissible NDP force limits applicable for a wide variety of wire sizes, both hard drawn and annealed, were determined. [45]. Previous work [46-49] on the subject has been restricted to small diameter wire having relatively low elongation under tensile stress.

The NDP test consists of pulling bonds at force levels below those necessary to cause breakage of the bond-loop system. In order for the NDP test to be truly non-destructive and hence prevent metallurgical defects in the bond-loop system, no part of the bond-loop system should be subjected to stresses greater than the metallurgical elastic limits.

For the NDP test to be statistically meaningful, it must be carried out in conjunction with a destructive bond pull test. The results of both the destructive bond pull test and the NDP test depend upon the same variables, including wire metallurgical properties, bonding technique, bond geometry, and bond deformation. Hence the mean and the standard deviation of the destructive bond pull test are significant factors in developing criteria for the NDP test.

In relating the results of a destructive pull test to criteria for a non-destructive pull test the stress-strain relationship of the wire is a significant factor. The effect of the state of hardness on the stress-strain relation is exemplified in figure 37. In this figure stress-strain curves are shown for the same aluminum wire in two states of hardness. The annealed wire has a large elongation typical of large diameter aluminum wire used in bonding power devices (see sec. 10.5.). Hard-drawn or stress-relieved wire has a small elongation and is typical of that of small diameter aluminum wire used in bonding integrated circuits.

Bonds made with small diameter aluminum wire are typically ultrasonically welded which work hardens the bond heel and causes it to be the weakest part of the bond-loop system. Hence, the strength of the heel determines the maximum safe NDP force. The heel strength depends upon the bond deformation which in turn depends upon the bonding schedule. Hence, a safe NDP force may be determined only if a destructive bond pull test is performed on bonds



A Beam lead head with heater wire loop
B Power supply for heater loop
C Substrate holder
D Beam
E Carrier for adjusting force settings
F Drive motor
G Load cell transducer
H Load cell transducer amplifier
I Leaf spring

Figure 35. Automatic puller for beam lead bonds.

Figure 36. Two-axis, variable-angle substrate holder.

made under the same conditions. The results of a destructive bond pull test are assumed to follow a normal distribution for which $\bar{X}$ is the mean breaking force and s is the sample standard deviation of the distribution. For normal assembly lines, where s can be expected to lie in the range 0.15 $\bar{X}$ to 0.25 $\bar{X}$, the recommended maximum safe NDP force is $0.9(\bar{X} - 3s)$. For high-reliability lines, s may be equal to or less than 0.15 $\bar{X}$. For this case, the recommended maximum safe NDP force is $0.9(\bar{X} - 4s)$. No NDP testing is recommended for cases where s is greater than 0.25 $\bar{X}$ since this indicates that some aspect of the bonding procedure is out of control and either a low, meaningless NDP force would be used or too many bonds would be stressed beyond their elastic limits.

The large diameter aluminum wire used in power devices typically has an elongation up to 20 percent before breaking. Also, this wire is usually ultrasonically bonded with a grooved capillary-type tool which limits the maximum bond deformation and hence does not produce a weak bond heel. In this case, the stress-strain relation for the wire span determines the maximum safe NDP force. Due to the differences in the stress-strain relation from that of small diameter wire, a different NDP force is necessary. For a wire elongation up to 20 percent and an s of 0.25 $\bar{X}$ or less the recommended maximum safe NDP force is $(\bar{X} - 3s)/2$. For an elongation greater than 20 percent, the maximum NDP force must be reduced to $(\bar{X} - 3s)/3$ in order to avoid significant inelastic wire elongation during the test.

Gold wire bonds formed by thermocompression or ultrasonic techniques do not have weak, overworked bond heels. Hence, the stress-strain relation for wire span determines the NDP force. These relations for small diameter grain-stabilized gold wire used in both ultrasonic

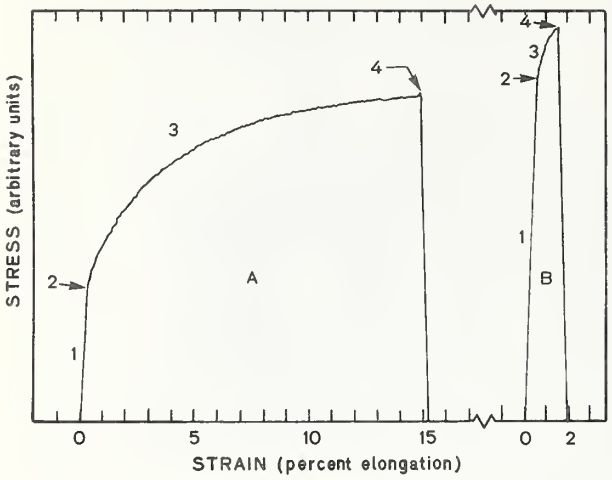


Figure 37. Stress-strain curves for annealed (A) and hard-drawn or stress-relieved (B) aluminum wire. (This figure was made up from individual stress-strain charts reversed in direction for clarity of presentation. In order to display both curves on the same chart the stress axis was made relative, since the breaking load of the annealed wire was approximately one-half that of the hard-drawn wire. On both curves region 1 is the elastic region where the stress is proportional to the strain, point 2 is the proportional or elastic limit, region 3 is the region of inelastic or plastic deformation, and point 4 is the breaking load of the wire.)

and thermocompression bonding show that this type of gold wire typically experiences most of its elongation above 85 to 90 percent of its breaking load. However, some other gold wires may begin to elongate as low as 70 percent of their breaking load. Considering this and the high pull strength, even with large bond deformation, the recommended maximum safe NDP force control limit to include all small diameter gold wire is $0.7(\bar{X} - 3s)$ or $0.7(\bar{X} - 4s)$ for $0.15\ \bar{X} < s \leq 0.25\ \bar{X}$ or $s \leq 0.15\ \bar{X}$, respectively.

Table 13 summarizes these recommendations. It must be noted that the NDP test ensures the reliability of a bond at the time of the test but does not prevent the later failure of the bond from intermetallic compound formation or post-production stresses [50].

(G. G. Harman)

Table 13 — Summary of NDP Force Recommendations

Type of Production Line	Wire		Relation Between $\bar{X}$ and s on the Bond Pull Test	Recommended Maximum Safe NDP Force
	Composition	Elongation		
Normal	Aluminum	<3%	$0.15\bar{X} < s \leq 0.25\bar{X}$	$0.9(\bar{X} - 3s)$
High Rel	Aluminum	<3%	$s \leq 0.15\bar{X}$	$0.9(\bar{X} - 4s)$
All	Aluminum	~5 to 20%	$s \leq 0.25\bar{X}$	$(\bar{X} - 3s)/2$
	Aluminum	>20%	$s \leq 0.25\bar{X}$	$(\bar{X} - 3s)/3$
All	Gold	Any	$0.15\bar{X} < s \leq 0.25\bar{X}$	$0.7(\bar{X} - 3s)$
	Gold	Any	$s \leq 0.15\bar{X}$	$0.7(\bar{X} - 4s)$

10.5. Bonds in Power Devices

Destructive double-bond pull tests were conducted on a number of power devices bonded with large diameter annealed aluminum wire [50]. Most such wire has a high elongation and breaks in the span after necking down at the weakest point as shown in the scanning electron micrograph of figure 38. As illustrated in the figure, the bond to the die is made ultrasonically and the bond to the gold-plated post is made by an electrical-discharge tweezer weld. In a few cases, the ultrasonic bond at the die was observed to fail by lift off at very low pull force. These "freaks" or "sports" would normally be eliminated by a nondestructive bond pull test (see sec. 10.4.).

Other failures occured at the post bond. In the process of investigating these failures, it was found that the electrical discharge weld often forms at the perimeter of the bond in the same manner as was observed previously (NBS Tech. Note 560, p. 34) for 25-μm (0.001-in.) diameter aluminum ultrasonic wire bonds (see also sec. 10.6). Scanning electron micrographs of lifted off or peeled back post bonds, such as those shown in figures 39 and 40, illustrate the bond formation. The upper post bond shown in figure 39 lifted off at very low pull force; the wire material left on the post reveals that welding only occured around the bond perimeter. The lower bond in the figure has more welded area and apparently was made by increasing either the weld energy or the clamp force. During a pull test the wire broke in the span leaving the partially peeled region. Later the wire was bent outward to reveal a completely unwelded area in the center of the bond. The very strong post bond illustrated in figure 40 was difficult to peel back. However, again the center region was unwelded. Similar observations have been made on a number of devices made by different manufacturers.

These observations indicate that the electrical discharge post bond is a deformation-type weld, as has been previously described for both thermocompression [51] and ultrasonic bonds [52]. In the latter case the aluminum wire is softened by the ultrasonic energy without significant temperature rise [53], and the bond is then deformed by the clamping force. In the case of the post welds, the wire is heated, and thus softened, by the electrical energy and again deformed by the clamping force. As deformation progresses, the wire is forced laterally over the gold metallization of the post, and both weldment surfaces are cleaned. As this happens a deformation-type weld takes place. In rare cases there may be molten aluminum around the bond. However, generally the only evidence of heat is an occasional very fine ring of purple plague around the outside perimeter of the bonds, as is indicated by the arrow on figure 41, a close up of the lower bond illustrated in figure 39. Only occasionally is plague observed in the bond interface region when the wire is peeled back. This is believed to result from an excessive electrical discharge energy and a clamping force that is too small. Contrary to this, in ultrasonic aluminum wire-bonding, where only a small amount of heat is thought to be generated, purple plague is never observed for bonds made to either thick- or thin-film gold metallizations, unless there is a subsequent heat treatment.

(G. G. Harman and K. O. Leedy)

10.6. Direct Observation of Ultrasonic Aluminum Wire Bonds

Experiments were initiated to investigate the feasibility of directly observing the bond formed between small diameter aluminum (1% silicon) wire and aluminum metallization. For this purpose, aluminum wire was bonded to aluminum thin films deposited onto slides composed of 96 percent silica glass.* The wire-film interfaces were then observed directly through the transparent slide.

The slides used in the study were first cleaned in polypropanol to remove any surface contaminants. The slides were then dried and sprayed with fluorocarbon liquid to remove airborne dust which, if present on the surface, might cause localized irregularities in the aluminum metallization. Varying thicknesses of aluminum were then evaporated onto the glass surface and allowed to age for several days at room temperature. This aging could equally well have been realized by sintering at elevated temperatures for about 20 min. The purpose of this aging was to improve the metallization-glass adhesion to the point where the aluminum film would not peel off the substrate. For purposes of visual inspection, it was found that

*This glass was chosen to simulate silicon dioxide over silicon as is used in integrated circuit fabrication.

Figure 38. Scanning electron micrograph showing the typical failure mode of well-made, 200-μm (0.008-in.) diameter, aluminum wire bonds subjected to a destructive double-bond pull test. (For clarity, the wires were carefully bent back into their approximate positions at rupture. Magnification: ∿ 13 X).

Figure 39. Scanning electron micrograph of the emitter post of a power transistor showing the imprint of a weak electrical discharge weld (A) that lifted off at low pull force and a partially peeled back 300-μm (0.012-in.) diameter aluminum wire bond (B). (Magnification: ∿ 36 X).

Figure 40. Scanning electron micrograph of a partially lifted, very strong electrical discharge weld to a gold-plated post showing the absence of welding in the center of the bond. (Magnification: ∿ 72 X).

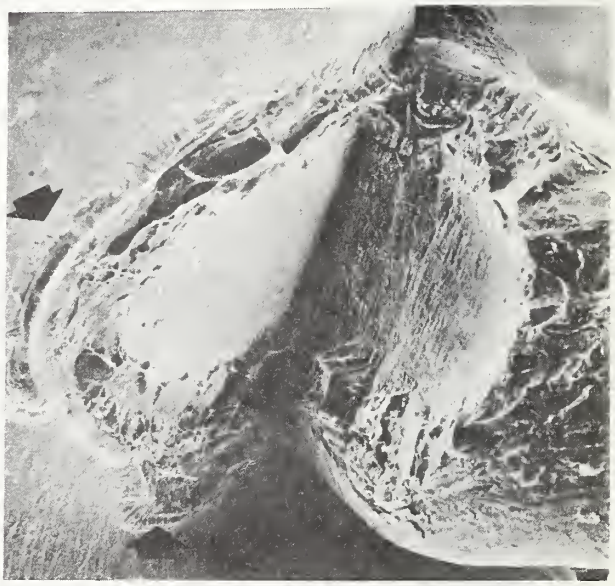


Figure 41. Scanning electron micrograph of the lower emitter post bond of figure 39 at greater magnification to show absence of deformation or welding in the center region of the bond and purple plague regions (arrows) around the outer perimeter of the weld. (Magnification: ∿ 130 X).

an aluminum film thickness less than about 400 nm gave the clearest results. For the examples reported, a thickness of 317 nm was used. For thicknesses greater than about 700 nm the metallization was sufficiently opaque to preclude clear observation.

After preparation of the metallized slides, 25-μm (1-mil) diameter aluminum (1% silicon) wire was ultrasonically bonded to the aluminum metallization. The bonding force and time were set at 25 gf (0.24 N) and 50 ms for both the first and second bonds. The power setting used in making the first bond was varied from a lower than normal value of 4 to a higher than normal value of 10, while that for the second bond was held constant at an intermediate value. A sequence of three bond loops was formed in accordance with this bonding schedule and the bond patterns of the first bonds in this sequence were observed with an optical microscope through the transparent slide.

Photomicrographs of the three patterns are shown in figure 42. The bond formed at the low power setting (fig. 42a) is in its nascent stages but not fully formed. The beginnings of a metallurgical weld are evident around portions of the perimeter of the contact area. In the bond formed at an intermediate power setting (fig. 42b) the weld extends around the entire perimeter of the contact area and the deformation is in the desirable intermediate range. For the bond formed at the high power setting (fig. 42c) an overbonded condition clearly prevails; the wire deformation was greater than two wire diameters.

These results confirm that the bond is initially formed at the perimeter of the wire-metallization contact area. This had previously been shown to be the case by means of very carefully peeling back the bond and observing the bond lift-off pattern with a scanning electron microscope (NBS Tech. Note 527, pp. 42-44). Also, poor bond quality was readily seen at extremes of the ultrasonic power settings studied in this series. This is particularly important at low ultrasonic power. In this region, the wire may look properly deformed and, hence, satisfactorily bonded but it may lift-off at a low bond pull force revealing only a partially welded region. This technique is simple and yet elegent. It provides an inexpensive window through which ultrasonic bonds may be viewed directly. (C. A. Main)

10.7. In-Process Bond Monitor

This joint theoretical and experimental project addresses itself to a number of rather important problems associated with ultrasonic bonding. The central problem focuses upon the possibility of using the bonding tool modal pattern in a feed-back set-up to identify and correct possible bad bonds and hence ensure consistent high-reliability bonds. In order to properly understand and treat this problem, several topics must be addressed. These include the basic mechanism or mechanisms through which applied ultrasonic energy gives rise to the formation of metallurgical welds, the motion of the bonding tool as a function of time and position along the tool for the tool in both the unloaded and loaded phases of operation, and the mixing phenomenon whereby higher harmonics are mixed with the fundamental during the formation of bad bonds [54].

For the purpose of mathematical modeling, consideration is being given only to the transverse motion of the ultrasonic tool. This is a rather good approximation since scanning electron micrographs of ultrasonic bonds formed with wedge tip tools show very little, if any, effects of torsional motion of the tool relative to those of the transverse motion. Further, vibration amplitudes of the tool tip (where the amplitude is usually the maximum) lie typically between 0.5 to 2.5 μm (20 to 100 μin.) and these are in the small oscillation region. Under these conditions, the motion of the tool may be modeled by the beam equation [55].

If $y(x,t)$ is the transverse displacement of the tool at the position x along its length at a time t, then $y(x,t)$ satisfies the equation:

$$\rho A(x) \frac{\partial^2 y(x,t)}{\partial t^2} + \frac{\partial^2}{\partial x^2} EI(x) \frac{\partial^2 y(x,t)}{\partial x^2} = F(x,t), \tag{23}$$

where ρ is the volume density of tool material, $A(x)$ and $EI(x)$ are the cross-sectional area and the flexural rigidity at the position x along the length of the tool, respectively, and $F(x,t)$ is the time-dependent applied force acting at the position x along the length of the tool. The functional form of $A(x)$, $EI(x)$, and $F(x,t)$, two initial conditions (in time), and four boundary conditions (in space) deterministically specify the solution, $y(x,t)$, of eq (23). The quantities ρ, $A(x)$ and $EI(x)$ may be determined directly from the material and geometrical

a. Low power. b. Normal power. c. High power.

Figure 42. Photomicrographs of patterns of ultrasonic aluminum wire bonds made with various power settings to a thin aluminum film of a 96-percent silica glass slide viewed through the glass slide. (Magnification: ∿ 300 X).

properties of the tool. This leaves the tool amplitude $y(x,t)$ in terms of the unknown applied force $F(x,t)$ only.

As a first step in the analysis of this problem, the uniform beam prototype (in which $A(x)$ and $EI(x)$ are taken to be constant and equal to A and EI, respectively) is being studied.

(J. H. Albers)

11. HERMETICITY

11.1. Helium Mass Spectrometer Method for Leak Detection

ASTM Committee F-1 on Electronics was assisted in preparing a final draft procedure and schedule for the interlaboratory evaluation of the helium mass spectrometer method for testing fine capillary leaks in large volume containers [56]. Each of the test objects consists of a capillary leak drawn in one end of a small glass tubulation and a prepared seal-off stem at the opposite end of the tubulation. The evaluation is to be conducted in three stages. The first stage requires the direct measurement of the capillary leak with the open seal-off stem inserted into the helium leak detector. The second stage requires pressurization and measurement on the capsule after seal-off. The third stage requires measurement of the leak after the seal-off is broken open. Interlaboratory measurements of the prepared test objects are scheduled at each stage.

Several sets of ancillary apparatus were fabricated to enable uniform, ambient pressure flooding of the capillary leak with helium for the first and third stages of the test. Enclosures for use in the second stage have been designed and fabricated.

Major delays in conducting the interlaboratory experiment were encountered, especially in laboratories equipped only with special purpose instruments for production testing where it has been necessary to fabricate custom adapters to connect the test objects. Nevertheless, the first stage has been completed in three of the five installations participating in the experiment. (S. Ruthberg)

11.2. ARPA/NBS Workshop II

A workshop on Hermeticity Testing of Integrated Circuits was held on March 29 at NBS Gaithersburg. Sixty-five engineers and scientists representing 36 organizations participated in the workshop which comprised six invited talks and two discussion periods.

Several relevant factors were underscored as a result of the workshop. The lack of correlation experienced to date between the radioisotope [57] and helium leak detection [56,58] methods of testing by the back pressurization technique is due in large part to discrepancies in existing standards procedures and in leak flow calculations. Data were given which showed limited correlation as a function of leak size and package internal volume after appropriate preconditioning of the test package.

While both the radioisotope and helium leak detector methods are capable of quantitative measurements and are inherently for the fine leak range ($\leq 10^{-5}$ atm·cm^3·s^{-1}), it was pointed out that the correlation of device failure to leaks in this range is not clear. In contrast, the correlation of device failure to leaks in the gross range ($>10^{-5}$ atm·cm^3·s^{-1}), is considered as well founded, but no test method of an objective, quantitative nature is in prevalent use.

Reported data substantiated the weight gain method [59] as a sensitive, quantitative measurement procedure particularly for high reliability selection; however, reservations with this method exist because of past experiences with delayed device failure as related to residual contamination from liquid test media and because of false rejection caused by irregular surface conditions which tend to entrap the test medium.

Extension of the gas tracer back pressurization methods into the gross leak range can be accomplished but is limited by internal volume and is dependent upon double valued, nonlinear functional relationships for flow modeling (see sec. 11.4.). Mass spectrometer analyses of the internal ambients of failed devices show a high incidence rate for included water, but the relationship of water leakage to measured leak rates is obscure. Tests at temperatures of 65°C or more showed increased occurrence of leakage which was reversible with return to room temperatures. (H. A. Schafft, K. O. Leedy, and S. Ruthberg)

11.3. Mass Spectrometer Application

A sensitive mass spectrometer has been designed and is being constructed to evaluate the use of this type of instrumentation for the measurement of trace elements in the semiconductor processing environment and on wafer surfaces as well as for the investigation of gas flow mechanisms in leaks in hermetic packages.

The apparatus comprises a quadrupole mass analyzer and an extremely high vacuum system with orifice limited pumping speeds at the manifold. Pumping is by a cascaded mercury

diffusion pump array with a ballasted sorption-mechanical forepump. High gas load capability, maximum sensitivity, and minimum hydrocarbon contamination are expected. (S. Ruthberg)

11.4. Gas Flow Mechanisms

The relationship of the true leak rate of a hermetic package to that measured in the back pressurization procedure [60] with a tracer gas is deduced, in practice, from either the molecular flow or the laminar viscous flow equations. Calculations obtained from the two types of flow mechanisms may show agreement in a narrow range of conditions or may differ by one to two orders of magnitude depending upon parameter values [60,61]. The molecular flow equations are usually used for the helium leak detector method, while the laminar viscous flow equations are used for the radioisotope method.

In reality, actual flow is more likely to be in the transition range with perturbing factors such as compressibility and diffusion playing some role. Complete solution of the problem requires consideration of the integrated effects of the pressurization, leakage, and detection phases. Initial calculations have been made for steady state conditions in air at 25°C for channel leaks, 1 mm long, and for channel radii in the range 10 to 0.1 μm using the semi-empirical formulation of Knudsen [62]. Onset limits for compressible, turbulent, and sonic flows have also been determined. In this approach the flow conductance of a long tube is taken as a linear combination of the laminar viscous flow and the free molecular flow conductances.

The results for three pressure conditions are summarized in table 14. In the table P_1 is the upstream pressure, P_2 is the downstream pressure, $\bar{\lambda}$ is the average mean free path for intermolecular collision distances at the mean pressure in the channel, R is the channel radius, Q_T is the calculated total flow rate, and Q_m is the calculated molecular flow rate. The transition length L_e is a characteristic length of viscous flow and is the distance from the mouth of the channel at which uniform laminar flow first sets in. The values of flow rate at which compressibility sets in are listed as Q_{comp}, for which the flow velocity becomes equal to Mach 1/3. Turbulent flow may occur above the flow rates listed as Q_{turb}, above which the pressure drop across the channel must be increased over that calculated for laminar flow. The maximum continuum flow which a channel entrance can pass is the critical flow rate, Q_{crit}, which is reached at a flow velocity of Mach 1 at the throat.

Consider first an upstream pressure of 1 atm and a downstream pressure of zero, conditions corresponding to the definition of leak rate. For a range in radius of two orders of magnitude, leak rates range from 10^{-2} to 10^{-9} atm·cm^3·s^{-1}. A channel with a 10 μm radius gives rise to a leak rate evidencing nearly 95 percent laminar flow, a channel with a 1 μm radius corresponds approximately to half molecular, half laminar flow, and a channel with a 0.1 μm radius exhibits complete molecular flow.

Upon upstream pressurization to 5 atm, flow is shifted toward the viscous range. Even the 0.1 μm radius channel exhibits about half molecular, half laminar flow, and the 1 μm radius channel has a 90 percent viscous flow characteristic. Transition length is significant and compressible flow is evidenced in the two larger leaks.

At upstream pressurization of 10 atm, viscous flow predominates but is modified in the two larger leaks to values less than that calculated by the Poiseuille equation because of compressibility and turbulence.

Under actual test conditions, tracer gases other than air are usually used. The values for Q_{crit}, Q_{turb}, L_e, and Q_T (for P_1 = 1 atm and P_2 = 0) in the table can be modified for the particular tracer gas used by multiplying the appropriate value for air by the relative values listed in table 15.

The results of these calculations verify the need for more realistic examination of flow mechanisms and the effect on the relationship between indicated leak rate and true leak rate. Failure to consider such factors could lead to calculation of oversize leak rates from the indicated value with molecular flow equations as compared with viscous flow equations. In the fine leak regime where both flow mechanisms are significant, an oversize leak would result from calculation with either type of equation alone. In addition, errors can result in larger leaks if the effects of compressibility or turbulance are neglected. (S. Ruthberg)

Table 14 — Flow and Flow Rate Characteristics for Channel Leaks of 1-mm Length for Air at 25°C

	R, μm	10	5	1	0.1
P_1=1 atm,	$R/\bar{\lambda}$	100	50	10	1
P_2=0,	Q_T/Q_m	15.5	8.2	2.3	1
$\bar{\lambda}$=0.1 μm	Q_T, atm·cm³·s⁻¹	1.2×10^{-2}	9.5×10^{-4}	2.1×10^{-6}	1.1×10^{-9}
	L_e, mm	5.0×10^{-2}	4.4×10^{-4}	1.0×10^{-5}	
	Q_{crit}, atm·cm⁷·s⁻¹	1.3×10^{-1}	3.3×10^{-2}	1.3×10^{-3}	
P_1=5 atm,	$R/\bar{\lambda}$	600	300	60	6
P_2=1 atm,	Q_T/Q_m	89	45	9.6	1.7
$\bar{\lambda}$=0.016 μm	Q_T, atm·cm³·s⁻¹	3.3×10^{-1}	2.1×10^{-2}	3.9×10^{-5}	6.3×10^{-9}
	L_e, mm	1.3	9.7×10^{-3}	2.4×10^{-4}	
	Q_{crit}, atm·cm³·s⁻¹	6.5×10^{-1}	1.6×10^{-1}	6.5×10^{-2}	
P_1=10 atm,	$R/\bar{\lambda}$	1100	550	110	11
P_2=1 atm,	Q_T/Q_m	163	82	17	2.4
$\bar{\lambda}$=0.009 μm	Q_T, atm·cm³·s⁻¹	1.4	7.3×10^{-2}	1.4×10^{-4}	1.8×10^{-8}
	L_e, mm	6.1	3.4×10^{-1}	6.5×10^{-4}	
	Q_{crit}, atm·cm³·s⁻¹	1.3	3.3×10^{-1}	1.3×10^{-2}	
	Q_{comp}, atm·cm³·s⁻¹ [a]	0.04	0.01	0.0004	
	Q_{turb}, atm·cm³·s⁻¹	0.49	0.24	0.049	

[a]The onset of compressible flow depends on the pressure at the point, here taken as 1 atm.

Table 15 — Channel Leak Flow Rate Limits and Leak Rates Relative to Air for Gases other than Air

Gas	Limiting Flow			Rel. Leak Rate Radius (μm)		
	Q_{comp}	Q_{turb}	L_e	10	1	0.1
Air	1	1	1	1	1	1
Ar				0.83	0.84	0.85
He	2.8	8.1	0.11	1.09	1.77	2.7
H_2				2.22	2.90	3.62
Kr^{85}	0.62	0.65	1.5	0.74		0.59

11.5. Dry, Quantitative Gross Leak Test

It has become increasingly clear that the principal problem area in hermetic testing is the gross leak range and that the development of a dry gas test procedure is desirable. The limiting factor in presently used procedures lies in the delay between the removal of pressurization and the detection of the tracer gas. This delay allows rapid depletion of the gas from the package interior with consequent nondetection of large leaks. A new method which eliminates this factor is being evaluated.

The procedure employs gas expansions in two similar and parallel systems. A differential pressure measurement is made after expansion. The device to be tested is placed in the first small test chamber of dimensions just sufficient to contain the specimen. A similar but solid artifact of the same external volume is placed in a parallel reference chamber of the same volume as the test chamber. Both chambers are pressurized to a desired pressure for the same time. After pressurization, the quantity of gas in the test and reference chambers will be the same if there is no leak in the device under test. However, if the device leaks, the quantity of gas introduced into the test chamber will be greater by the amount driven into the test device interior.

The gas in the small volumes is then allowed to expand into associated larger and previously evacuated chambers of the same size connected by a differential pressure meter. A difference in quantity of gas in the two volumes causes an indication on the meter. The rate of change of meter indication is a measure of the leak rate and the amplitude is a measure of device internal volume.

The major factors limiting the leak range and application are the sensitivity of the differential pressure gauge and the temperature stability of the system. The limiting physical difficulties are the minimization of dead volume in the pressure chambers and the precision of closure of valves between the various chambers.

The use of a parallel reference chain eliminates the need for absolute measurement, minimizes the effects of adsorption and variation in valve closure, and allows a wide range of test object volumes and materials by adjustment of the tare. Any test gas may be used.

A system to implement this method is being designed. A more detailed description of the operating procedures and a discussion of sensitivity and stability requirements have been prepared to provide preliminary information for the consideration of and discussion by potential users of the method; copies are available on request to the author. (S. Ruthberg)

12. THERMAL PROPERTIES OF DEVICES

12.1. Transient Thermal Response

The transient thermal response of power semiconductor devices to a single pulse or a series of power pulses is an important characteristic for many device applications because it determines by how much and for how long the dissipation-limited d-c power level of the device can safely be exceeded. Either the pulsed heating curve technique or the cooling curve technique [63,64] may be used to measure the transient thermal response.

The pulsed heating curve technique involves the measurement of the device junction temperature, T_{Jh}, at the conclusion of a power pulse of amplitude P which has been applied for a time, t, to a device, initially at a reference temperature, T_{ref}. The device is allowed to cool to the reference temperature before the next pulse is applied. The pulsed heating curve is generated by repeating this procedure for pulses of the same amplitude but of increasing width until steady state is reached. This technique can also be used to generate the heating response for single pulses of power in excess of the permissible d-c level. The pulse width is set and maintained constant. Pulses of increasing power level are applied until the maximum safe operating junction temperature is reached. This sequence must be repeated for each pulse width of interest.

The measurement of the cooling curve is made by heating the device to a steady state temperature, T_{Js}, switching the power off, and monitoring the junction temperature, T_{Jc}, as the device cools. Because the device must first be heated to steady state, the dissipation limited d-c power level cannot be exceeded. Thus the cooling curve cannot be generated for operating conditions which simulate power pulses in excess of the d-c limit. Application of the technique in this range therefore requires the assumption that the device thermal response to a power pulse in excess of the d-c limit is equivalent to the device cooling response for a time (equal to the pulse width) after cessation of power at or below the d-c limit.

Both techniques require the use of a temperature sensitive parameter to measure the junction temperature. In the present work the emitter-base voltage, V_{EB}, was measured at a small, constant forward current in an emitter-only switching circuit as shown in figure 43. Thermal impedance, $Z_{\theta}(t)$, is the parameter employed by device users to characterize the thermal response of a device for particular pulsed applications. The heating curve or the cooling curve can be used to determine the thermal impedance for devices. The thermal impedance derived from the heating curve is:

$$Z_{\theta(h)}(t) = \frac{T_{Jh}(t) - T_{ref}}{P} \quad , \tag{24}$$

while that derived from the cooling curve is:

$$Z_{\theta(c)}(t) = \frac{T_{Js} - T_{Jc}(t)}{P} \quad . \tag{25}$$

Because it is the heating response which is of interest, the pulsed heating curve technique would seem to be the obvious technique to use to obtain the thermal impedance or transient thermal response. The cooling curve technique is generally used, however, because it is easier and faster to generate the cooling curve than the pulsed heating curve, particularly if a large number of points must be generated to obtain the heating curve. When applying the cooling curve technique, it is assumed that the cooling curve is the conjugate of the heating curve as shown in figure 44. It has been found, however, that the cooling response is generally not the conjugate of the heating response for power transistors.

Examination of the heat flow equations [65] shows that the heating curve is the conjugate of the cooling curve only when the thermal conductivity of the device, k, the thermal diffusivity of the device, D, and the power density distribution (and therefore the current density distribution) within the device are all independent of temperature. These conditions are violated because both k and D are functions of temperature [66] and, because of the

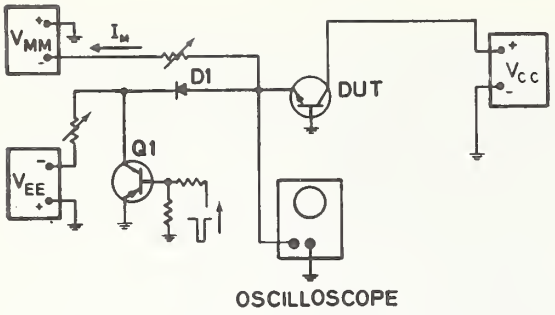


Figure 43. Emitter-only switching circuit for measuring thermal response of transistors using the emitter-base voltage as the temperature sensitive parameter.

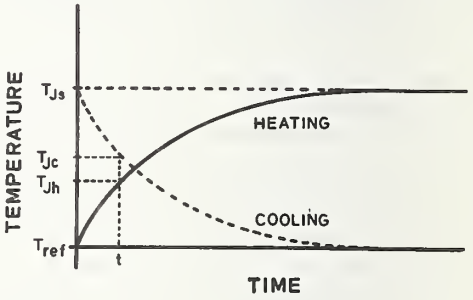


Figure 44. Illustrative heating and cooling curves of a semiconductor device. (See text for definition of symbols.)

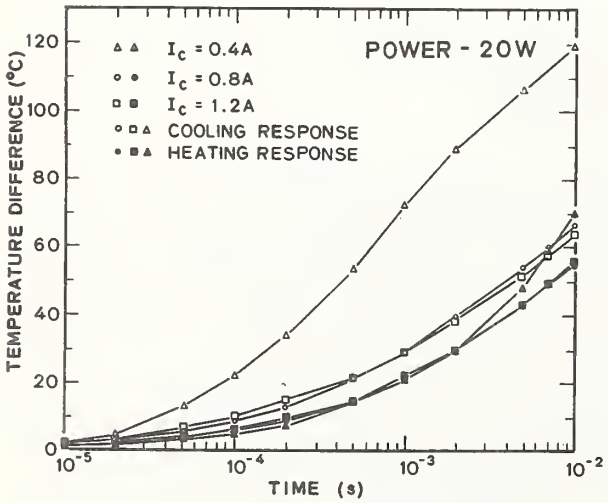


Figure 45. Electrically measured heating and cooling curves for constant power at three different current-voltage operating conditions. (The ordinate axis for the cooling curve is $T_{Js} - T_{Jc}(t)$ and for the heating curve is $T_{Jh}(t) - T_{ref}$. The heating and cooling curves for a particular value of collector current would coincide in this presentation if the curves were the conjugate of each other.)

thermal-electrical feedback mechanisms of power transistors [67], the power density distribution within a device changes with time as the device heats.

To show experimentally that the heating and cooling curves are not conjugate to each other, the heating and cooling responses were generated for numerous TO-3 and TO-66 encased planar and mesa power transistors. Both wire and clip lead bonded devices were included. As an illustration consider the results of measurements by both techniques on a typical device under three different operating conditions as shown in figure 45. The power dissipation for all three operating conditions is the same, but it was achieved by different combinations of collector-emitter voltage, V_{CE}, and collector current, I_C. If the heating curve were the conjugate of the cooling curve, the heating and cooling curves generated for the same combinations of values of I_C and V_{CE} would coincide.

It can also be seen in the figure that the cooling response is a strong function of the device operating conditions. The rate of cooling is most rapid for the 0.4 A collector current because the power density distribution at steady state is more constricted for this case than for the other two cases illustrated. However, the heating response for this device is not significantly dependent upon operating conditions until after about 2 ms of heating. For pulses longer than 2 ms the heating curve for the 0.4 A collector current deviates from the other two suggesting that the power density distribution is becoming more non-uniform as the device heats. This is expected because low current, high voltage operating conditions are favorable to the formation of current constrictions (NBS Tech. Note 475, pp. 27-28).

The curves in figure 45 were all generated for a power level less than the d-c limit of the device. This was necessary because the cooling curves were generated for the same operating conditions as the heating curves. When this is done, the cooling curve always lies above the heating curve because, for a given operating condition, the power density distribution for power transistors is less uniform at steady state than at any time during device heating. Thus, the device cools from the most non-uniform power density distribution, while it heats from a more uniform distribution. Consequently, the thermal impedance, $Z_\theta(t)$, as determined from the cooling curve (eq 25), is larger for all times than that determined from the heating curve (eq 24), if the two curves are generated for the same device operating conditions.

Because thermal impedance is often used to determine device temperature for power pulses in excess of the d-c dissipation limit, comparisons were made between the actual thermal impedance for such pulses and the thermal impedance determined from cooling curves. The cooling curves were generated for a condition of maximum d-c power and maximum voltage because this condition usually produces the most severe thermal non-uniformity at steady state. Thermal impedance for power pulses in excess of the d-c limit was determined by fixing the pulse width, setting the voltage at the maximum allowed value and then increasing the collector current until the junction temperature reached the same value at the conclusion of the pulse as was measured at steady state for maximum d-c power dissipation and maximum voltage. These measurement conditions were chosen because they were expected to produce the largest values of thermal impedance under pulse conditions.

The thermal impedance derived from the cooling curve of a device which was determined to have a severe current constriction for the maximum voltage, maximum power operating condition from measurements of device current gain [68] is shown in figure 46. The values of thermal impedance determined for pulses of width 0.2, 1, 10, and 100 ms and magnitude in excess of the d-c limit are also shown in the figure. The first two of these fall well below the cooling curve because the severe current constriction does not form until after the first millisecond of heating. By 10 ms after the initiation of the heating pulse, the constriction has formed and the power density distribution for the remainder of the heating is more nearly the same as that for which the cooling curve was generated, and after this time the heating and cooling curves are more nearly the conjugate of each other.

The cooling curve of a second device, which had a more uniform thermal distribution at steady state than the device previously discussed, is shown in figure 47. The values of thermal impedance for pulses of magnitude in excess of the d-c limit and width 1, 10, and 100 ms, which are also shown in the figure, also lie below the thermal impedance obtained from the cooling curve. The two determinations of thermal impedance do not approach each other as rapidly as for the previous device when the pulse width is increased above 10 ms because no sudden non-uniformity in power density occurs for this device. Rather, the power density only gradually becomes non-uniform as the device heats.

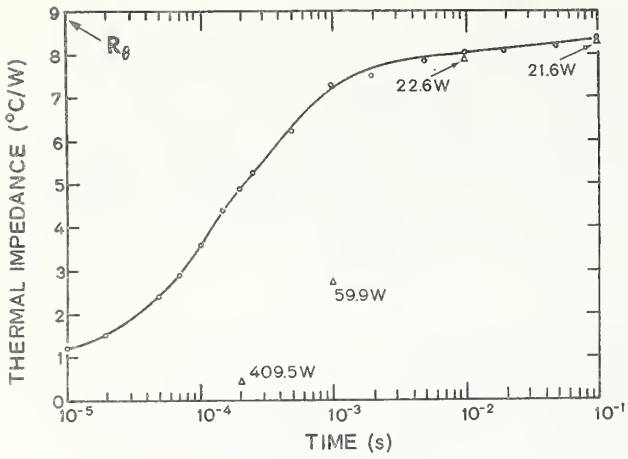


Figure 46. Thermal impedance derived from the electrically measured cooling curve of a device which has a severe current constriction at the steady-state operating conditions for which the cooling curve was generated compared with thermal impedance determined for pulsed power in excess of the dissipation limited d-c power where the peak temperature for the pulse was the same as the steady-state temperature. (Cooling curve for a steady-state power dissipation of 17.5 W: O; pulsed power: Δ. The instantaneous power for each pulse width is indicated beside each triangle. The thermal resistance of the device is denoted as R_θ.)

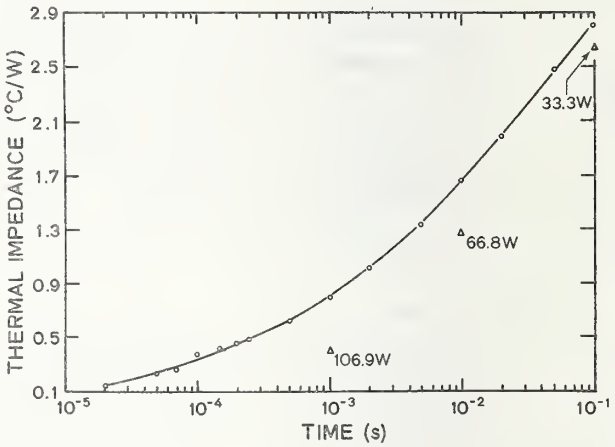


Figure 47. Thermal impedance derived from the electrically measured cooling curve of a device which has a relatively uniform current distribution at the steady-state operating conditions for which the cooling curve was generated compared with thermal impedance determined for pulsed power in excess of the dissipation limited d-c power where the peak temperature for the pulse was the same as the steady-state temperature. (Cooling curve: O; pulsed power: Δ.)

The cooling curve technique, then, because it is initiated from the most non-uniform thermal distribution, gives a more conservative (larger) value for thermal impedance than that which would be obtained under actual single pulse operating conditions, even for pulses in excess of the d-c level. Furthermore, for the transistors examined, the cooling response is shown to be very dependent upon device operating conditions, whereas the heating response for pulse widths up to a few milliseconds is only slightly dependent upon the operating conditions. (D. L. Blackburn and F. F. Oettinger)

12.2. Standardization Activities

In connection with assistance provided to EIA-JEDEC committees, comments were received on a proposed revision of EIA Standard RS-313-A, Thermal Resistance Measurements of Conduction Cooled Power Transistors, recently letter balloted in JEDEC Committee JC-25 on Power Transistors, and modifications are being made to incorporate these comments. A final revision of the document, Thermal Resistance Test Methods for Signal Diodes, previously letter balloted in EIA JEDEC Committee JC-20 on Signal and Regulator Diodes, was completed in response to JEDEC Solid State Products Council comments. Comments on Letter Ballot JC-11.3-73-36, Accepted Practices for Making Microelectronic Device Thermal Characteristics Tests - A Users Guide, were resolved, and the revised document sent to the JEDEC Solid State Products Council for review. (F. F. Oettinger and S. Rubin)

13. MICROWAVE DIODES

13.1. Radiation Response of Schottky-Barrier X-Band Mixer Diodes

A preliminary indication of the permanent damage induced by nuclear radiation in silicon Schottky-barrier X-band microwave mixer diodes was obtained by subjecting separate groups of diodes to ^{60}Co gamma rays and fast neutrons (E>10 keV) of progressively higher levels, reaching a cumulative gamma dose of 1.7×10^8 rads(Si) and a neutron fluence of 5.5×10^{15} cm^{-2}. Measurements were made after each irradiation to determine changes in conversion insertion loss, local oscillator return loss and standing wave ratio, i-f output conductance, self-bias (rectified current), and forward current at one d-c bias voltage (with no local oscillator drive).

The diodes were divided into three equal-sized groups: a gamma group, a neutron group, and a control group. This equality of division also extended to the diode supplier, type, and grade. The gamma and neutron groups were irradiated according to the schedule in table 16; the control group was not irradiated. To reduce the effect of systematic shifts in measurement error, the three groups were interleaved during measurements: a diode from the gamma group, a diode from the control group, a diode from the neutron group, a diode from the gamma group, etc., with interuptions permitted only after a neutron-group diode measurement, so that every irradiated diode was measured at approximately the same time as an unirradiated (control) diode.

Figures 48, 49, and 50 show the behavior of conversion insertion loss for the diodes in the gamma, control, and neutron groups respectively of the first lot of 27 diodes for the radiation levels shown in table 16. Note that each radiation shown preceded the measurement number cited on the same line. Measurements 1 and 2 were pre-irradiation measurements used to establish diode stability (NBS Spec. Publ. 400-1, pp. 44-46). The letter in the diode serial is a brand code for the diode manufacturer. Diodes of two grades were used, based on the manufacturer's specified limit on standard overall average noise figure. Diodes with primed serial numbers were specified to have a standard overall average noise figure limit of 6.5 dB while those with unprimed serial numbers had a specified limit of 6.0 dB.

The following conclusions can be drawn from the results of the conversion insertion loss measurements described above, other measurements on the first lot of diodes, and measurements on a second mixed lot of 24 diodes [69]:

1. Gamma radiation up to 1.7×10^8 rads(Si) has no discernible effect.

2. Fast neutrons up to a fluence of 1.0×10^{15} cm^{-2} generally cause only barely perceptible changes at most, comparable to the measurement repeatability.

3. Fast neutrons at a fluence of 5.5×10^{15} cm^{-2} generally cause a definite but small increase in conversion insertion loss. The largest, 0.69 dB between measurements 4 and 6, was a significant amount but is probably tolerable in most systems as a one-time occurrence until the diodes can be replaced. The average change (also between measurements 4 and 6) was only 0.20 dB, which is generally negligible considering the wide variability in initial

Table 16 — Cumulative Radiation Levels for Lot 1 Diodes

Designation of Measurement Following Irradiation	^{60}Co Gamma Ray Dose, rads(Si)	Fast Neutron Fluence, cm^{-2}
3	1.0×10^6	1.0×10^{13}
4	1.1×10^7	1.1×10^{14}
5	5.1×10^7	1.0×10^{15}
6	1.7×10^8	5.5×10^{15}

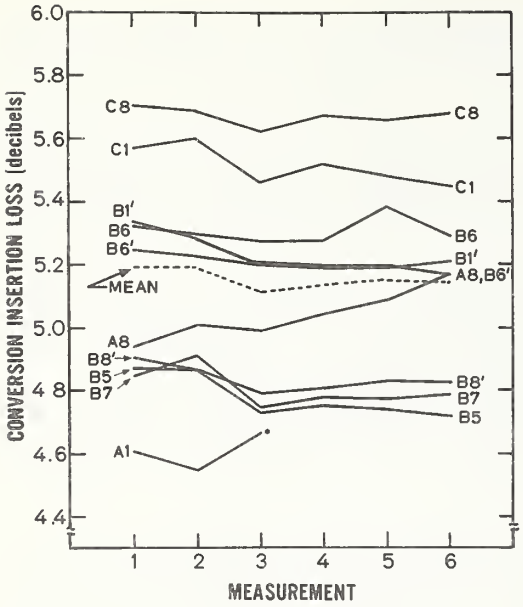


Figure 48. Conversion insertion loss for first-lot gamma-group diodes. (Diode A1 was accidently destroyed after the third measurement; data from this diode are not included in the mean.)

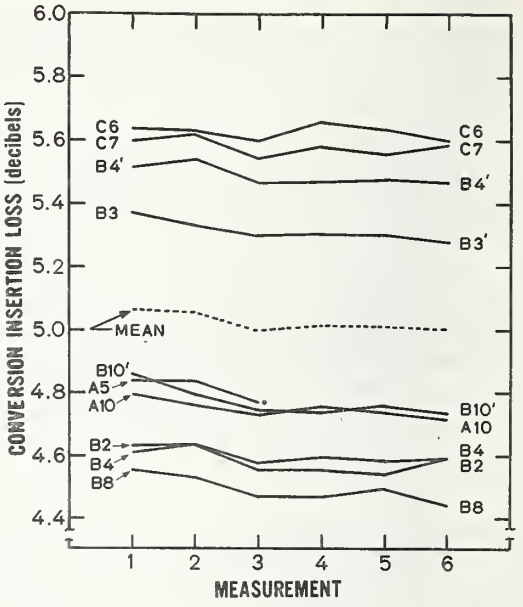


Figure 49. Conversion insertion loss for first-lot control-group diodes. (Diode A5 was accidently destroyed after the third measurement; data from this diode are not included in the mean.)

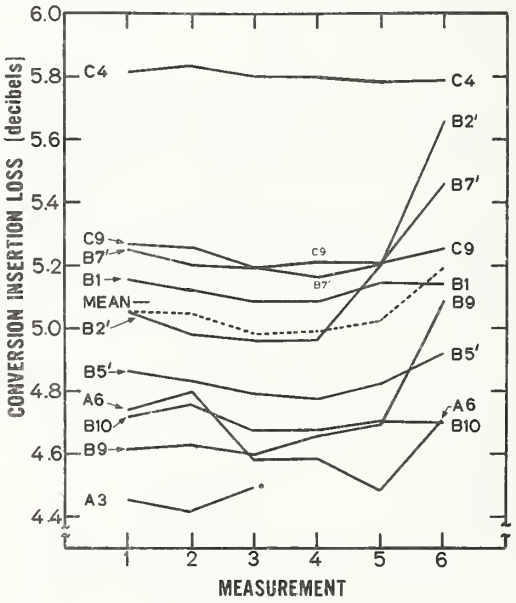


Figure 50. Conversion insertion loss for first-lot neutron-group diodes. (Diode A3 was accidently destroyed after the third measurement; data from this diode are not included in the mean.)

performance. The return loss, standing wave ratio, and self-bias voltage of most diodes were distinctly altered at this level, and the forward current of all diodes decreased. The i-f output conductance was not significantly altered.

4. There is a wide variation in neutron hardness, some diodes showing little or no effect while others were degraded in conversion insertion loss by several tenths of a decibel after a neutron fluence of 5.5×10^{15} cm^{-2}. The sample standard deviation of the conversion insertion loss changes (between measurements 5 and 6) was 0.178 dB, as compared with only 0.034 dB for the control group and 0.047 dB for the gamma group. A similar variability was observed in most of the other measured characteristics. There seem to be brand-correlated differences in hardness, but the limited number of specimens prevents any firm conclusion.

5. There are significant differences in mechanical shock sensitivity between brands; few brand-A diodes could be used for this reason. Several brand-A diodes were rejected for excessive conversion insertion loss on the first measurement, and many more became unmeasurable due to gross instability despite careful handling. Operating a waveguide switch audibly against its stop was sufficient to significantly change the characteristics of some of these diodes, despite clamping of the waveguide between the switch and the diode holder. In this respect, they resemble point-contact diodes.

6. There was a considerable spread in conversion insertion loss between diodes of the same grade. Values of conversion insertion loss for diodes of the 6.0-dB grade are spread over a range of more than 1 dB, some being significantly higher than those of 6.5-dB grade diodes of a different brand. Overall average noise figure is proportional to conversion insertion loss, and the output noise ratio for Schottky diodes tends to be low. If the output noise ratio were unity, the standard overall average noise figure would be higher than the conversion insertion loss by the amount of the standard i-f average noise figure, 1.5 dB for these types. The 6.0-dB grade diodes should therefore have conversion losses close to 0.5 dB lower than those of the 6.5-dB grade diodes; from the plots it can be seen that this is not the case, even for diodes from the same supplier. Lack of specification compliance for many of the diodes tested is therefore strongly suspected, although absolute measurements were not attempted.

7. The repeatability of the conversion insertion loss measurements was established by computing the sample standard deviations of the six data for each control-group diode, after correcting the data for systematic shifts. The sample standard deviations ranged from 0.007 dB to 0.030 dB, with a median of 0.019 dB and a mean of 0.018 dB. How much of these deviations is due to diode changes and how much to measurement precision (equipment plus operator) is unknown, but a three-sigma uncertainty of 0.05 dB can be assigned to the latter as a reasonable estimate. An additional 0.05 dB can be assigned as a tentative limit on a several-month systematic drift where the system calibrations are unchanged. A systematic uncertainty of about 0.1 dB is due to calibration uncertainty, but this is not relevant to the hardness study.

Since this experiment was intended to be exploratory, only a small number of specimens was employed. The scope of the experiment was not intended to be sufficient to provide a definitive evaluation of diode brands or grades. With this qualification, it can be concluded that the diodes appear to be reasonably hard to radiation, but that there may be serious threats to system performance from inadequate quality control and mechanical instability of the diodes used in this experiment are representative of those employed in the system.

This experiment concludes the laboratory phase of the investigation of measurement technique for characterizing microwave mixer diodes. Results obtained to date are being collected and analyzed for inclusion in a final report. (J. M. Kenney)

14. REFERENCES

1. Buehler, M. G., Peripheral and Diffused Layer Effects on Doping Profiles, *IEEE Trans. Electron Devices* ED-19, 1171-1178 (1972).

2. Klaber, E., A Survey of Stefan Type Problems, PhD. Thesis, Carnege-Mellon Univ. (University Microfilms, Ann Arbor, Michigan, 1972).

3. Rubinstein, L. I., The Stefan Problem, *Trans. Amer. Math. Soc.* (Translation) 27, (1971).

4. Hildebrand, F. B., *Methods of Applied Mathematics*, pp. 444-448 (Prentice-Hall, Inc., New York, 1956).

5. Linz, Peter, Numerical Methods for Voterra Integral Equations with Singular Kernels, *Siam Journal of Numerical Analysis* 6, 365-374 (1969).

6. Nicholson, R. S., and Olmstead, M. L., Numerical Solution of Integral Equations, *Electrochemistry*, J. Mattson and H. Mark, eds., pp. 120-137 (Marcel Dekker, Inc., New York, 1972).

7. Wagner, S., Diffusion of Boron from Shallow Ion Implants in Silicon, *J. Electrochem. Soc.* 119, 1570-1576 (1972).

8. MacDougall, J. D., Manchester, K. E., and Roughan, P. E., High Value Implanted Resistors for Microcircuits, *Proc. IEEE* 57, 1538-1542 (1969).

9. Irvin, J. C., Resistivity of Bulk Silicon and of Diffused Layers in Silicon, *Bell System Tech. J.* 41, 387-410 (1962).

10. Runyan, W. R., *Silicon Semiconductor Technology*, p. 180 (McGraw-Hill, New York, 1965).

11. Farina, M. V., *Programming in BASIC, The Time-Sharing Language* (Prentice-Hall, Inc., Englewood Cliffs, New Jersey, 1968).

12. Caughey, D. M., and Thomas, R. E., Carrier Mobilities in Silicon Empirically Related to Doping and Field, *Proc. IEEE* 55, 2192-2193 (1967).

13. Farina, M. V., *op. cit.*, pp. 134-135, 138.

14. Hogben, D., Peavy, S. T., and Varner, R. N., OMNITAB II - User's Reference Manual, NBS Technical Note 552 (October 1971).

15. MacFarlane, G. G., McLean, T. P., Quarrington, J. E., and Roberts, V., Fine Structure in the Absorption-Edge Spectrum of Si, *Phys. Rev.* 111, 1245-1254 (1958).

16. Barber, H. D., Effective Mass and Intrinsic Concentration in Silicon, *Solid-State Electronics* 10, 1039-1051 (1967).

17. Standard Method for Measuring Hall Mobility and Hall Coefficient in Extrinsic Semiconductor Single Crystals, ASTM Designation F 76, *Annual Book of ASTM Standards*, Part 8 (November 1973). (Available as a separate reprint from American Society for Testing and Materials, 1916 Race Street, Philadelphia, Pa. 19103.)

18. Draft Method of Test for Probe Force on Four-Probe Arrays, ASTM Committee F-1 Draft 6D28 (unpublished).

19. Standard Method for Measuring Resistivity of Silicon Slices with a Collinear Four-Probe Array, ASTM Designation F 84, *Annual Book of ASTM Standards*, Part 8 (November 1973). (Available as a separate reprint from American Society for Testing and Materials, 1916 Race Street, Philadelphia, Pa. 19103.)

20. Tentative Method of Test for Sheet Resistance of Silicon Epitaxial Layers using a Collinear Four-Probe Array, ASTM Designation F 374, *Annual Book of ASTM Standards*, Part 8 (November 1973). (Available as a separate reprint from American Society for Testing and Materials, 1916 Race Street, Philadelphia, Pa. 19103.)

21. Buehler, M. G., Thermally Stimulated Measurements: The Characterization of Defects in Silicon *p-n* Junctions, *Semiconductor Silicon/1973*, H. R. Huff and R. R. Burgess, eds., pp. 549-560 (The Electrochemical Society, Princeton, N. J., 1973).

22. Sah, C. T., Forbes, L., Rosier, L. I., Tasch, Jr., A. F., and Tole, A. B., Thermal Emission Rates of Carriers at Gold Centers in Silicon, *Appl. Phys. Letters* 15, 145-148 (1969).

23. Buehler, M. G., Impurity Centers in *p-n* Junctions Determined from Shifts in the Thermally Stimulated Current and Capacitance Response with Heating Rate, *Solid-State Electronics* 15, 69-79 (1972).

24. Heiman, F. P., On the Determination of Minority Carrier Lifetime from the Transient Response of an MOS Capacitor, *IEEE Trans. Electron Devices* ED-14, 781-784 (1967).

25. Zaininger, K. H., Automatic Display of MIS Capacitance Versus Bias Characteristics, *RCA Review* 27, 341-359 (1966).

26. Grove, A. S., Deal, B. E., Snow, E. H., and Sah, C. T., Investigation of Thermally Oxidized Silicon Surfaces Using Metal-Oxide-Semiconductor Structures, *Solid-State Electronics* 8, 145-163 (1965).

27. Sze, S. M., *Physics of Semiconductor Devices*, Chapter 9 (John Wiley and Sons, New York, 1969).

28. Brooks, R. D., and Mattes, H. G., Spreading Resistance Between Constant Potential Surfaces, *Bell System Tech. J.* 50, 775-784 (1971).

29. Standard Method of Test for Thickness of Epitaxial Layers of Silicon in Substrates of the Same Type by Infrared Reflectance, ASTM Designation F 95, *Annual Book of ASTM Standards*, Part 8 (November 1973). (Available as a separate reprint from American Society for Testing and Materials, 1916 Race Street, Philadelphia, Pa., 19103.)

30. Standard Method of Test for Thickness of Epitaxial or Diffused Layers in Silicon by the Angle Lapping and Staining Technique, ASTM Designation F 110, *Annual Book of ASTM Standards*, Part 8 (November 1973). (Available as a separate reprint from American Society for Testing and Materials, 1916 Race Street, Philadelphia, Pa., 19103.)

31. Morris, B. L., Some Device Applications of Spreading Resistance Measurements on Epitaxial Silicon, *J. Electrochem. Soc.* 121, 422-426 (1974).

32. Carnes, J. E., and Kosonocky, W. F., Fast-Interface-State Losses in Charge-Coupled Devices, *Appl. Phys. Letters* 20, 261-263 (1972).

33. Kooi, E., Influence of Heat Treatments and Ionizing Irradiations on the Charge Distribution and the Number of Surface States in the $Si-SiO_2$, *IEEE Trans. Electron Devices* ED-13, 238-245 (1966).

34. Sze, S. M., *op. cit.*, pp. 447-459.

35. Grove, A. S., *Physics and Technology of Semiconductor Devices*, (John Wiley and Sons, Inc., New York, 1967), p. 302.

36. Brodersen, R. W., Buss, T. D., and Tasch, Jr., A. F., Experimental Characterization of Charge Transfer Efficiency in Surface Channel Charge-Coupled Devices, *Proc. CCD Applications Conference*, San Diego, California, 18-20 September 1973, pp. 169-178.

37. Gosney, W. M., Subthreshold Drain Leakage Currents in MOS Field-Effect Transistors, *IEEE Trans. Electron Devices* ED-19, 213-219 (1972).

38. van der Pauw, L. S., A Method of Measuring the Resistivity and Hall Coefficient on Lamella of Arbitrary Shape, *Phillips Research Reports* 13, 1-9 (1958).

39. Draft Recommended Practice for Rotational Acceleration and Rotational Velocity of a Wafer During Photoresist Coating, ASTM Committee F-1 Draft 5D31 (unpublished).

40. Schafft, H. A., *Semiconductor Measurement Technology:* ARPA-NBS Workshop I. Measurement Problems in Integrated Circuit Processing and Assembly, NBS Spec. Publ. 400-3 (February 1974).

41. Zaininger, K. H., and Heiman, F. P., The C-V Technique as an Analytical Tool, Part II, *Solid State Technology* 13, No. 6, 46-55 (1970).

42. Sze, S. M., *op. cit.*, p. 117.

43. Yakowitz, H., Ballantyne, J. P., Munro, E., and Nixon, W. C., The Cylindrical Secondary Electron Detector as a Voltage Measuring Device in the Scanning Electron Microscope, *Proc. 5th Annual Scanning Electron Microscope Symposium,* Chicago, Illinois, April 1972, pp. 33-40.

44. Harman, G. G., Ed., *Semiconductor Measurement Technology:* Microelectronic Ultrasonic Bonding, NBS Spec. Publ. 400-2 (January 1974) pp. 23-28.

45. Harman, G. G., A Metallurgical Basis for the Non-Destructive Wire-Bond Pull Test, *12th Annual Proceedings, Reliability Physics 1974,* Las Vegas, Nevada, April 2-4, to appear.

46. Ang, C. Y., Eisenberg, P. H., and Matraw, H. C., Physics of Control of Electronic Devices, *Proc. 1969 Annual Symposium on Reliability,* Chicago, Illinois, January 1969, pp. 73-85.

47. Slemmons, J. W., The Microworld of Joining Technology, *Proc. American Welding Society 50th Annual Meeting,* Philadelphia, Pennsylvania, April 1969, pp. 22-27, 35, 56, 72.

48. Polcari, S. M., and Bowe, J. J., Evaluation of Non-Destructive Tensile Testing, DOT-TSC-NASA-71-10 (1971). Avaiable from National Technical Information Service, Springfield, Virginia 22151, Accession No. N71-37516.)

49. Bertin, A. P., Development of Microcircuit Bond-Pull Screening Techniques, RADC-TR-73-123 (April 1973). (Available from National Technical Information Service, Springfield, Virginia 22151, Accession No. AD 762333.)

50. Harman, G. G., Metallurgical Failure Modes of Wire Bonds, *12th Annual Proceedings, Reliability Physics 1974,* Las Vegas, Nevada, April 2-4, 1974, to appear.

51. English, A. T., and Hokanson, J. L., Studies of Bonding Mechanisms and Failure Modes in Thermocompression Bonds of Gold Plated Leads to Ti-Au Metallized Substates, *9th Annual Proceeding, Reliability Physics 1971,* Las Vegas, Nevada, March 31-April 2, 1971, pp. 178-186. (Available from Publications Sales Dept., The IEEE, 345 E. 47th Street, New York, New York 10017, Catalog No. 71-C-9-PHY.)

52. Harman, G. G., and Leedy, K. O., An Experimental Model of the Microelectronic Ultrasonic Wire Bonding Mechanism, *10th Annual Proceedings, Reliability Physics 1972,* Las Vegas, Nevada, April 5-7, 1972, pp. 49-56. (Available from Publication Sales Dept., The IEEE, 345 E. 47th Street, New York, New York 10017, Catalog No. 72CH0628-8-PHY.)

53. Langenecker, B., Effects of Ultrasound on Deformation Characteristics of Metals, *IEEE Trans. Sonics Ultrasonics* SU-13, 1-8 (1966).

54. Harman, G. G., Ed., *op. cit.*, pp. 58-73.

55. Chen, Yu, *Vibrations: Theoretical Methods*, pp. 204-229 (Addison-Wesley Publishing Company, Inc., Reading, Mass., 1966).

56. Tentative Recommended Practices for Determining Hermeticity of Electron Devices with a Helium Mass Spectrometer Leak Detector, ASTM Designation F 134, *Annual Book of ASTM Standards*, Part 8 (November 1973). (Available as a separate reprint from American Society for Testing and Materials, 1916 Race Street, Philadelphia, Pennsylvania 19103.)

57. MIL-STD-883, Test Methods of Procedures for Microelectronics, Method 1014, Seal, Test Condition B; MIL-STD-750, Test Methods for Semiconductor Devices, Method 1071, Hermetic Seal, Test Condition G.

58. MIL-STD-883, Method 1014, Seal, Test Condition A; MIL-STD-750, Method 1071, Hermetic Seal, Test Condition H.

59. Stinnett, D., Der Marderosian, A., and Nelson, P., Weight Test Method Detects Gross Leaks in Components, *Evaluation Engineering*, p. 11 (Sept.-Oct. 1970).

60. Howl, D. A., and Mann, C. A., The Back-pressurization Technique of Leak Testing, *Vacuum* 15, 347-352 (1965).

61. Maurer, D. W., Comparison of Standard Leak Rates Measured by Viscous and Molecular Flow Techniques, *Materials and Electron Device Processing*, ASTM Special Technical Publication No. 300, pp. 187-192 (American Society for Testing and Materials, Philadelphia, 1961).

62. Dushman, S., and Lafferty, J. M., *Scientific Foundations of Vacuum Technique*, 2nd ed., pp. 104-111 (John Wiley and Sons, New York, 1972).

63. Lockett, R. A., Bell, H. A., and Priston, R., Thermal Resistance of Low Power Semiconductor Devices under Pulse Conditions, *Mullard Technical Communications* 8, 146-169 (1965).

64. Gutzwiller, F. W., and Sylvan, T. P., Power Semiconductor Ratings Under Transient and Intermittent Loads, *AIEE Transations, Part I, Communications and Electronics* 79, 699-706 (January 1961).

65. Blackburn, D. L., and Oettinger, F. F., Transient Thermal Response Measurements of Power Transistors, *Proc. 1974 IEEE Power Electronics Specialists Conference (PESC)*, Murray Hill, New Jersey, June 10-12, 1974, to appear.

66. Shanks, H. R., Maycock, P. D., Sidles, P. H., and Danielson, G. C., Thermal Conductivity of Silicon from 300 to 1400°K, *Phys. Rev.* 130, 1743-1748 (1963).

67. Scarlett, R. M., and Shockley, W., Secondary Breakdown and Hot Spots in Power Transistors, *IEEE International Conv. Record* 11, Part 3, 3-13 (1963).

68. Oettinger, F. F., and Rubin, S., The Use of Current Gain as an Indicator for the Formation of Hot Spots Due to Current Crowding in Power Transistors, *Tenth Annual Proceedings, Reliability Physics 1972*, Las Vegas, Nevada, pp. 12-18. (Available from Publication Sales Dept., The IEEE, 345 E. 47th Street, New York, New York 10017, Catalog No. 72CH0628-8-PHY).

69. Kenney, J. M., *Semiconductor Measurement Technology:* Permanent Damage Effects of Nuclear Radiation on the X-Band Performance of Silicon Schottky-Barrier Microwave Mixer Diodes, NBS Spec. Publ. 400-7 (in preparation).

APPENDIX A

SEMICONDUCTOR TECHNOLOGY PROGRAM STAFF

Coordinator: J. C. French*
Secretary: Miss B. S. Hope*
Consultant: C. P. Marsden¶†

Semiconductor Characterization Section

(301) 921-3625

Dr. W. M. Bullis, Chief

F. H. Brewer
Dr. M. G. Buehler
Miss F. C. Butler+
M. Cosman
Mrs. K. E. Dodson+
Dr. J. R. Ehrstein
T. E. Griffin×
Dr. R. Y. Koyama
Mrs. K. O. Leedy
Dr. D. C. Lewis
R. L. Mattis
Dr. A. G. Lieberman
Dr. W. E. Phillips
Miss D. R. Ricks
S. Ruthberg
H. A. Schafft
A. W. Stallings
Mrs. M. L. Stream+
W. R. Thurber

Semiconductor Processing Section

(301) 921-3541

Dr. A. H. Sher, Chief

H. E. Dyson
G. G. Harman
W. J. Keery
H. K. Kessler
J. Krawczyk
T. F. Leedy
Y. M. Liu
Miss C. A. Main§
Dr. D. B. Novotny
R. L. Raybold
L. M. Smith
Mrs. E. Y. Trager+

Electron Devices Section

(301) 921-3622

F. F. Oettinger, Acting Chief

D. L. Blackburn
Mrs. A. D. Glover+
J. M. Kenney
Mrs. B. A. Oravec¶+
M. K. Phillips
M. C. Rhodes¶
G. J. Rogers
S. Rubin
D. E. Sawyer
L. R. Williams

¶ Part Time
+ Secretary
× Summer
* Telephone: (301) 921-3357
† Telephone: (301) 921-3621
§ Telephone: (301) 921-3625

APPENDIX B

SEMICONDUCTOR TECHNOLOGY PROGRAM PUBLICATIONS

B.1. Prior Reports

A review of the early work leading to this Program is given in Bullis, W. M., Measurement Methods for the Semiconductor Device Industry — A Review of NBS Activity, NBS Tech. Note 511, December, 1969.

Quarterly reports covering the period July 1, 1968, through June 30, 1973, were published as NBS Technical Notes with the title, Methods of Measurement for Semiconductor Materials, Process Control, and Devices:

Quarter Ending	NBS Tech. Note	Date Issued	NTIS Accession No.
September 30, 1968	472	December 1968	AD 681330
December 31, 1968	475	February 1969	AD 683808
March 31, 1969	488	July 1969	AD 692232
June 30, 1969	495	September 1969	AD 695820
September 30, 1969	520	March 1970	AD 702833
December 31, 1969	527	May 1970	AD 710906
March 31, 1970	555	September 1970	AD 718534
June 30, 1970	560	November 1970	AD 719976
September 30, 1970	571	April 1971	AD 723671
December 31, 1970	592	August 1971	AD 728611
March 31, 1971	598	October 1971	AD 732553
June 30, 1971	702	November 1971	AD 734427
September 30, 1971	717	April 1972	AD 740674
December 31, 1971	727	June 1972	AD 744946
March 31, 1972	733	September 1972	AD 748640
June 30, 1972	743	December 1972	AD 753642
September 30, 1972	754	March 1973	AD 757244
December 31, 1972	773	May 1973	AD 762840
March 31, 1973	788	August 1973	AD 766918
June 30, 1973	806	November 1973	AD 771018

After July 1, 1973 quarterly reports were issued in the NBS Special Publication 400 subseries with the title, Semiconductor Measurement Technology:

Quarter Ending	NBS Spec. Publ.	Date Issued	NTIS Accession No.
September 30, 1973	400-1	March 1974	AD 775919

B.2. Current Publications

As various phases of the work are completed, publications are prepared to summarize the results or to describe the work in greater detail. Publications of this kind which have been issued recently are listed below:

Sawyer, D. E., Rogers, G. J., and Huntley, L. E., Measurement of Transit Time and Related Transistor Characteristics, Air Force Weapons Laboratory Report AFRL-TR-73-54 (October 1973). Available from National Technical Information Services, Springfield, Virginia 22151, Accession No. AD 914258.

Oettinger, F. F., and Gladhill, R. L., Thermal Response Measurements for Semiconductor Device Die Attachment Evaluation, *Technical Digest, 1973 International Electron Devices Meeting*, Washington, D. C., December 3-5, 1973, pp. 47-50. (Available from Publications Sales Dept., The IEEE, 345 E. 57th Street, New York, New York 10017, Catalog No. 73CH0731-5ED.)

Harman, G. G., Ed., *Semiconductor Measurement Technology:* Microelectronic Ultrasonic Bonding, NBS Spec. Publ. 400-2 (January 1974).

Schafft, H. A., *Semiconductor Measurement Technology:* ARPA/NBS Workshop I. Measurement Problems in Integrated Circuit Processing and Assembly, NBS Spec. Publ. 400-3 (January 1974).

Sandow, P. M., A Transistor with Simultaneously Diffused Emitter and Base, *Solid-State Electronics* 17, 404-406 (April 1974).

Harman, G. G., A Metallurgical Basis for the Non-Destructive Wire Bond Pull Test, *12th Annual Proceedings, Reliability Physics 1974,* Las Vegas, Nevada, April 2-4, 1974, to appear.

Harman, G. G., Metallurgical Failure Modes of Wire Bonds, *12th Annual Proceedings, Reliability Physics 1974,* Las Vegas, Nevada, April 2-4, 1974, to appear.

Forman, R. A., Thurber, W. R., and Aspnes, D. E., The Second Indirect Band Gap in Silicon, *Solid-State Communications* 14, 1007-1010 (May 1974).

Blackburn, D. L., and Oettinger, F. F., Transient Thermal Response Measurements of Power Transistors, *Proc. 1974 IEEE Power Electronics Specialists Conference (PESC),* Murray Hill, New Jersey, June 10-12, 1974, to appear.

Buehler, M. G., *Semiconductor Measurement Technology:* Microelectronic Test Patterns: An Overview, NBS Spec. Publ. 400-6 (August 1973).

Lewis, D. C., On the Determination of the Minority Carrier Lifetime from the Reverse Recovery Transient of *pn*R Diodes, *Solid-State Electronics,* to appear.

Ciarlo, D. R., Schultz, P. A., and Novotny, D. B., Automated Inspection of IC Photomasks, *Proceedings 18th Annual Technical Meeting,* Society of Photo-Optical Instrumentation Engineers, San Diego, California, August 19-23, 1974, to appear.

B.3. Availability of Publications

In most cases reprints of articles in technical journals may be obtained on request to the author. NBS Technical Notes and Special Publications are available from the Superintendent of Documents, U.S. Government Printing Office, Washington, D. C. 20402, or the National Technical Information Service, Springfield, Virginia 22151, or both. Current information regarding availability of all publications issued by the Program is provided in the latest edition of NBS List of Publications No. 72 which can be obtained on request to Mrs. K. O. Leedy, Room B346, Technology Building, National Bureau of Standards, Washington, D. C. 20234.

APPENDIX C

WORKSHOP AND SYMPOSIUM SCHEDULE

C.1. Proceedings or Reports of Past Events:

Symposium on Silicon Device Processing, Gaithersburg, Maryland, June 2-3, 1970. (Cosponsored by ASTM Committee F-1 and NBS). Proceedings: NBS Spec. Publ. 337 (November 1970).

ARPA/NBS Workshop I. Measurement Problems in Integrated Circuit Processing and Assembly, Palo Alto, California, September 7, 1973. Report: NBS Spec. Publ. 400-3 (January 1974).

ARPA/NBS Workshop II. Hermeticity Testing for Integrated Circuits, Gaithersburg, Maryland, March 29, 1974. Report: NBS Spec. Publ. 400-9 (to appear).

Spreading Resistance Symposium, Gaithersburg, Maryland, June 13-14, 1974. (Cosponsored by ASTM Committee F-1 and NBS). Proceedings: NBS Spec. Publ. 400-10 (to appear).

C.2. Calendar of Future Events:

ARPA/NBS Workshop III. Test Patterns, Scottsdale, Arizona, September 6, 1974. For information, contact K. O. Leedy or M. G. Buehler (301) 921-3625.

APPENDIX D

STANDARDS COMMITTEE ACTIVITIES

ASTM Committee F-1 on Electronics

M. G. Buehler, Semiconductor Measurements Subcommittee; Process Controls Section
W. M. Bullis, Editor, Semiconductor Crystals Subcommittee; Secretary, Editorial Subcommitee, Semiconductor Measurements, Semiconductor Processing Materials, Hybrid Microelectronics, and Quality and Hardness Assurance Subcommittees; Insulating Materials Section; Advisory Committee
J. R. Ehrstein, Chairman, Resistivity Section; Semiconductor Crystals, Semiconductor Processing Materials, Semiconductor Measurements and Hybrid Microelectronics Subcommittees
J. C. French, Chairman, Editorial Subcommittee; Secretary, Advisory Committee; Semiconductor Crystals, Semiconductor Processing Materials, Semiconductor Measurements, Hybrid Microelectronics and Quality and Hardness Assurance Subcommittees
G. G. Harman, Secretary, Interconnection Bonding Section
B. S. Hope, Committee Assistant Secretary
K. O. Leedy, Chairman, Interconnection Bonding Section
T. F. Leedy, Dielectrics Section
D. C. Lewis, Semiconductor Crystals, Semiconductor Processing Materials, Semiconductor Measurements, Hybrid Microelectronics and Quality and Hardness Assurance Subcommittees
C. P. Marsden, Committee Secretary; Advisory Committee
R. L. Mattis, Semiconductor Crystals, Semiconductor Measurements, and Editorial Subcommittees
D. B. Novotny, Editor, Semiconductor Processing Materials Subcommittee
W. E. Phillips, Chairman, Lifetime Section; Secretary, Semiconductor Crystals Subcommittee; Semiconductor Processing Materials, Semiconductor Measurements, and Hybrid Microelectronics Subcommittees
G. J. Rogers, Quality and Hardness Assurance Subcommittee
S. Ruthberg, Semiconductor Processing Materials, Hybrid Microelectronics, and Quality and Hardness Assurance Subcommittees
A. H. Sher, Semiconductor Crystals, Semiconductor Processing Materials, and Hybrid Microelectronics Subcommittees
W. R. Thurber, Semiconductor Crystals and Semiconductor Measurements Subcommittees

ASTM Committee E-10 on Radioisotopes and Radiation Effects

W. M. Bullis, Subcommittee 7, Radiation Effects on Electronic Materials
J. C. French, Subcommittee 7, Radiation Effects on Electronic Materials
D. C. Lewis, Subcommittee 7, Radiation Effects on Electronic Materials

Electronic Industries Association: Solid State Products Division, Joint Electron Device Engineering Council (JEDEC)

F. F. Oettinger, Chairman, Task Group JC-11.3-1 on Thermal Considerations for Microelectronic Devices, Committee JC-11.3 on Mechanical Standardization for Microelectronic Devices; Chairman, Task Group JC-25-5 on Thermal Characterization of Power Transistors, Committee JC-25 on Power Transistors; Technical Advisor, Thermal Properties of Devices, Committees JC-22 on Rectifier Diodes and Thyristors, JC-20 on Signal and Regulator Diodes, and JC-30 on Hybrid Integrated Circuits
S. Rubin, Chairman, Council Task Group on Galvanomagnetic Devices
D. E. Sawyer, Task Group JC-24-5 on Transistor Scattering Parameter Measurement Standard, Committee JC-24 on Low Power Transistors
H. A. Schafft, Technical Advisor, Second Breakdown and Related Specifications Committee JC-25 on Power Transistors

Electronic Industries Association: Government Products Division

F. F. Oettinger, Chairman, Task Group G-12-08-74 on Recommendations for Military Usage of Proposed Standards and Test Methods for Thermal Resistance, Committee G-12 on Solid State Devices

APPENDIX D

IEEE Electron Devices Group

J. C. French, Standards Committee
J. M. Kenney, Chairman, Standards Committee Task Force on Microwave Solid-State Devices II (Mixer and Video Detector Diodes)
H. A. Schafft, Standards Committee Task Force on Second Breakdown Measurement Standards

IEEE Magnetics Group

S. Rubin, Chairman, Galvanomagnetic Standards Subcommittee

Society of Automotive Engineers

J. C. French, Subcommittee A-2N on Radiation Hardness and Nuclear Survivability
W. M. Bullis, Planning Subcommittee of Committee H on Electronic Materials and Processes

IEC TC47, Semiconductor Devices and Integrated Circuits

S. Rubin, Technical Expert, Galvanomagnetic Devices; U.S. Specialist for Working Group 5 on Hall Devices and Magnetoresistive Devices

APPENDIX E

SOLID-STATE TECHNOLOGY & FABRICATION SERVICES

Technical services in areas of competence are provided to other NBS activities and other government agencies as they are requested. Usually these are short-term, specialized services that cannot be obtained through normal commercial channels. Such services provided during the last two quarters, which are listed below, indicate the kinds of technology available to the program.

E.1. Thin Metal Films (J. Krawczyk)

Thin films of a gold-germanium alloy and nickel were evaporated onto gallium-arsenide substrates for the Harry Diamond Laboratories.

Patterned thin films of gold were evaporated onto silicon substrates for the Harry Diamond Laboratories.

Thin films of aluminum and gold were evaporated onto the front and back sides, respectively, of silicon wafers intended for MOS device production for the Harry Diamond Laboratories.

Thin films of aluminum were evaporated onto the tapered edges of laser reflecting mirrors for the Harry Diamond Laboratories.

E.2. Semiconductor Device Assembly (J. Krawczyk)

Silicon wafers containing arrays of transistors were scribed, the resulting dice attached to TO-5 headers, and the devices bonded with gold wire leads for the Harry Diamond Laboratories.

E.3. Silicon Nuclear Radiation Detectors (Y. M. Liu)*

Four *p*-type silicon surface barrier detectors were thermally cycled between room temperature and 35°C under high vacuum. All four detectors exhibited excess noise and increased reverse leakage current after the test. Two detectors recovered to their pre-test levels after storage over night at room temperature and ambient and were then irradiated with 1-MeV electrons at fluences of 1×10^{13} and 1×10^{15} cm^{-2}. Analysis of the results of the irradiation are underway.

E.4. Ribbon Wire Technology (H. K. Kessler)†

Assistance to the Naval Electronics Laboratory Center, San Diego, in the implementation of NBS-developed ribbon wire technology on their pilot production line continued. Information on bonding equipment was compiled and sent to NELC, and a final report was prepared.

E.5. Scanning Electron Microscopy (W. J. Keery)

Scanning electron micrographs of micrometer diameter glass fibers were taken for both the NBS Surface Microanalysis Section and the NBS Spectrochemical Analysis Section.

Specimens of marble and various cements were examined for the NBS Materials and Composites Section.

Scanning electron micrographs of smoke particles were taken for the NBS Fire Technology Division.

---

*NBS Cost Center 4254429

†NBS Cost Center 4254448.

INDEX

NBS-114A (REV. 7-73)

U.S. DEPT. OF COMM. BIBLIOGRAPHIC DATA SHEET	1. PUBLICATION OR REPORT NO. NBS Spec. Publ. 400-4	2. Gov't Accession No.	3. Recipient's Accession No.

4. TITLE AND SUBTITLE

Semiconductor Measurement Technology: Quarterly Report
October 1, 1973 to March 31, 1974

5. Publication Date November 1974

6. Performing Organization Code

7. AUTHOR(S) W. Murray Bullis, Editor

8. Performing Organ. Report No.

9. PERFORMING ORGANIZATION NAME AND ADDRESS

NATIONAL BUREAU OF STANDARDS
DEPARTMENT OF COMMERCE
WASHINGTON, D.C. 20234

10. Project/Task/Work Unit No. See Item 15

11. Contract/Grant No. ARPA Order 2397, Pgm Code 4D10; DNA IACRO 74-811

12. Sponsoring Organization Name and Complete Address (Street, City, State, ZIP)

NBS — Washington, D. C. 20234
ARPA — 1400 Wilson Blvd., Arlington, Va. 22209
DNA — Washington, D. C. 20305

13. Type of Report & Period Covered Interim October 1 to March 31, 1973.

14. Sponsoring Agency Code

15. SUPPLEMENTARY NOTES 4251126, 4252128, 4254115, 4259522, 4259555.

16. ABSTRACT (A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.)

This combined quarterly progress report describes NBS activities directed toward the development of methods of measurement for semiconductor materials, process control, and devices. The emphasis is on silicon device technologies. Principal accomplishments during this reporting period include (1) identification of major problem areas in connection with measuring and inspecting photomasks, (2) development of a mathematical model suitable for interpreting thermally stimulated current and capacitance measurements on junction diodes and metal-oxide-semiconductor (MOS) capacitors, (3) completion of a preliminary evaluation of a method, based on the transient capacitance-voltage characteristic of an MOS capacitor, for measuring thickness of epitaxial layers up to 2 μm, and (4) development of criteria for use in nondestructive wire bond pull tests. Results are also reported on spreading resistance, capacitance-voltage, and carrier mobility measurements; polynomial fits for energy band gap and hole and electron effective masses in silicon; methods for characterizing oxide films; evaluation of sheet resistance and collector resistor test structures; evaluation of a photoresist spinner test; scanning electron microscopy; bonding of aluminum ribbon wire to thick film copper; bonding of platinum wire to thin film aluminum; leak rate calculations in the transition flow regime; transistor thermal response measurements; and radiation response of microwave mixer diodes. Supplementary data concerning staff, publications, workshops and symposia, standards committee activities, and technical services are also included as appendices.

17. KEY WORDS (six to twelve entries; alphabetical order; capitalize only the first letter of the first key word unless a proper name; separated by semicolons)

Boron redistribution; collector resistor; dopant profiles; effective mass; electrical properties; electron beam induced current mode; electronics; epitaxial layer thickness; flying spot scanner; gold-doped silicon; hermeticity; ion microprobe mass analysis; methods of measurement; microelectronics; microwave diodes; mobility; MOS devices; oxide films; photomasks; photoresist; platinum wire; resistivity; resistivity standards; ribbon wire; scanning electron microscopy; semiconductor devices; semiconductor materials; semiconductor process control; sheet resistance; silicon; spreading resistance; test patterns; thermal response; thermally stimulated capacitance; thermally stimulated current; thick film copper; voltage contrast mode; wire bonds; X-ray photoelectron spectroscopy.

18. AVAILABILITY

[XX] Unlimited

[ ] For Official Distribution. Do Not Release to NTIS

[XX] Order From Sup. of Doc., U.S. Government Printing Office Washington, D.C. 20402, SD Cat. No. C13.10:400-4

[XX] Order From National Technical Information Service (NTIS) Springfield, Virginia 22151 (Microfiche only)

19. SECURITY CLASS (THIS REPORT) UNCLASSIFIED

21. NO. OF PAGES 101

20. SECURITY CLASS (THIS PAGE) UNCLASSIFIED

22. Price 1.70

USCOMM-DC 29042-P74

Announcement of New Publications on Semiconductor Measurement Technology

Superintendent of Documents,
Government Printing Office,
Washington, D.C. 20402

Dear Sir:

Please add my name to the announcement list of new publications to be issued in the series: National Bureau of Standards Special Publication 400–.

Name _____

Company _____

Address _____

City _____ State _____ Zip Code _____

(Notification Key N-413)

U.S. DEPARTMENT OF COMMERCE
National Bureau of Standards
Washington, D.C. 20234

OFFICIAL BUSINESS

Penalty for Private Use, $300

POSTAGE AND FEES PAID
U.S. DEPARTMENT OF COMMERCE
COM-215