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Semiconductor Measurement Technology:

Techniques for Measuring the Integrity of Passivation Overcoats on Integrated Circuits

400-31

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Werner Kern

and

Robert B. Comizzoli

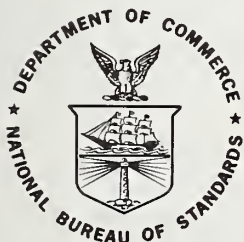
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PREFACE

This Final Report describes work performed from April 24, 1975 to April 30, 1976 in the Process and Applied Materials Research Laboratory of RCA Laboratories, Princeton, NJ, under Contract No. NBS5-35913. Paul Rappaport is the Laboratory Director, George L. Schnable is the Project Supervisor and Group Head, and Werner Kern, Member of the Technical Staff, is the Project Scientist. Additional members of the research team are Robert B. Comizzoli, Member of the Technical Staff; Edward C. Tracy, Research Associate; Ruth E. Allen and Robert D. Vibronek, Research Technicians.

The contract has been administered under Richard L. Raybold, Government Project Monitor, National Bureau of Standards, Department of Commerce, Washington, D.C. Thomas F. Leedy has been Assistant to the Government Project Monitor.

It is a pleasure to acknowledge the help of a number of individuals who have contributed to this work by the performance of specific research tasks, several analytical techniques, and sample preparation: E. C. Tracy - photomicrography, chemical etching, and uv fluorescence studies; R. E. Allen - electrical technology and photo-resisting; R. D. Vibronek and A. W. Fisher - film deposition technology; B. J. Seabury - scanning electron microscopy; and G. R. Auth - profilometric measurements.

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In some cases, for the sake of completeness or to provide desirable background information, this report contains results generated during RCA-supported research programs related to thin-film dielectrics, analytical method development, silicon device failure mechanisms and device processing.

It should be pointed out that most of the ICs shown are not standard products but were specially processed by CVD techniques and/or heat treatments to generate high densities of defects for the purpose of testing and demonstration of the analytical techniques.



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"Techniques for Measuring the Integrity of Passivation Overcoats on Integrated Circuits"

by

Werner Kern and Robert B. Comizzoli

Conventional test methods to evaluate the quality of glass passivation overcoats on semiconductor devices are generally inadequate and/or destructive. Three new methods have been devised that overcome these problems: (1) Sequential selective chemical etching of metal/dielectric structures to detect buried, latent, or partial defects as a function of dielectric layer depth. (2) Electrophoretic cell decoration with uv phosphor particles suspended in an insulating liquid, the sample forming one electrode of the cell. (3) Electrostatic corona charging to selectively deposit surface ions from a high voltage dc discharge on the insulating surfaces of the sample, followed by placing of the charged sample in a suspension of charged carbon black particles in an insulating liquid; depending on the polarity of the ions the particles can be deposited on the insulator surface or at the defect sites. The etching method is most suitable in process research studies, and the electrophoretic technique for demarcating relatively large defects. The corona decoration method, coupled with automated instrumental read-out based on measuring the reflected light intensity, is ideal for routine testing of devices because it is fast, simple, sensitive, and nondestructive to devices such as glass passivated bipolar and MOS ICs. The practical benefits of the new test methods can be considerable in production and product control, with cost savings through early detection of production line defects and rapid corrective action.

Key words: Corona charging decoration; dielectric defect detection; electrophoretic decoration; integrated circuit quality control; selective chemical etching; and semiconductor device reliability.

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1. SUMMARY

Most integrated circuits now on the market are metallized with aluminum and passivated with an overcoat of phosphosilicate glass (PSG) and/or silicon dioxide. The quality of present-day overcoats is highly variable, indicating that more effective quality control measures are needed to improve the product and its reliability. However, test methods available for evaluating the quality of glass passivation overcoats have been inadequate and/or destructive. The objective of this research program has been the development of analytical test methods that do not suffer from these shortcomings. This goal has been accomplished successfully. We have demonstrated the applicability of the new methods to the specific requirements of this contract, as well as to the evaluation of insulating coatings in general.

The experimental approaches chosen to solve these problems were based on the following basic methods: (1) *Selective chemical etching, intended primarily as an absolute standard for comparing other test methods;* (2) *electrophoretic cell decoration with uv phosphor particles;* and (3) *electrostatic corona charging to deposit surface charge followed by decoration.* Techniques for quantifying the defect density were examined in conjunction with these detection and decoration methods. The major results and conclusions for each are summarized below.

The method of selective metal etching underneath the glass overcoat to demarcate localized structural defects in the overcoat has been demonstrated to be simple, fast, effective, and sensitive. It is an absolute method but has the disadvantage of being destructive. It is used primarily when the sample can be sacrificed in the test, or when an absolute standard is desired for comparison with other techniques. Microcracks in typical glass layers over aluminum can be detected down to widths of less than 500 Å.

Sequential etching of metal/insulator structures is useful for detecting buried, latent, or partial defects within the dielectric overcoat. Determination of the defect density after each pair of etching treatments then provides the defect density as a function of dielectric or insulator layer depth. The method is reliable but time-consuming; it is recommended for applications in process research. Numerous examples are presented, illustrating specific and general applications of the two selective etching methods.

In the electrophoretic method, the sample to be decorated is placed in the suspension, and a voltage is applied between it and an opposite electrode to move the decorating particles to the defects. A rectangular stainless-steel tank is used to hold the decorating suspension. The tank is also used as one electrode. In some cases, a glass beaker is used and a stainless-steel electrode is placed opposite the sample. This method was found suitable for decoration of relatively large defects and cracks with white or uv phosphor powders. The use of insulating liquids was found to give superior results in terms of adhesion and nondestructiveness. The deposition mechanism, basically a

capacitor-charging phenomenon, was investigated in some detail. This technique is useful but less attractive than the corona-charging methods.

In the corona-charging method of decoration, surface ions from a corona discharge are deposited on the insulating surfaces of the sample. At a defect in the insulator, ions flow to the grounded substrate. After the charging step, the sample is placed in a suspension of charged decorating particles in an insulating liquid. If the electrical polarities of the ions on the sample insulating surfaces and of the charged decorating particles are opposite, then the particles are deposited on the insulating surfaces and not at the defects, resulting in reverse defect decoration. If the electrical polarities of ions and particles are the same, then the particles are deposited on the defects, resulting in direct decoration.

For the corona charging, a plane array of 40- μ m-diameter wires is used, spaced 2 cm from the sample, which rests on a grounded plate. For certain samples, it is necessary to place a grounded grid over the sample to limit the surface voltage of the passivating layer during the corona charging. The principles of the corona-charging mechanism were studied and related to the process; in particular, the basis for the nondestructive nature of the process is well understood.

In general, the corona-charging techniques are nondestructive, rapid, and simple. Various decorating powders were tested including silicate glasses, uv phosphors, and carbon black. The corona-charging methods are very sensitive; e.g., the carbon black reverse decoration method can detect defects not found by aluminum etching, nor by scanning electron microscopy (SEM), unless glass etching is first used to enlarge the defect. By comparison with etching, this technique has been shown to be very selective. These techniques are also capable of detecting certain partial or latent defects.

The carbon black reverse decoration by corona charging results in a very high contrast sample when viewed by reflectance microscopy. This is a particular advantage for process automation and was explored using a photocell mounted on the microscope to measure reflected light intensity, which was related to sample quality. The population density of decorated defects can thus be quantified. It is possible to automate this type of read-out technique on a step-and-repeat basis, using automatic and computerized instrumental recording of the data.

Post-decoration device recovery procedures have been developed and proven to be effective. It has been shown that device yield is not decreased by this procedure.

A good correlation has been shown to exist among the various methods developed on this contract. Advantages, disadvantages, limitations, sensitivity limits, and applicability of each have been pointed out and demonstrated experimentally in many instances.

The described methods were developed and refined specifically for the evaluation of dielectric overcoats on aluminum-metallized ICs. We have shown, however, that these methods are also applicable to analyzing other metal/dielectric structures and devices and, in fact, to evaluating insulator coatings in general.

The availability of a well-defined practical test method for evaluating the integrity of IC passivating overcoats now offers device manufacturers a much needed tool for controlling their products during fabrication. Since the recommended techniques are nondestructive, a 100 percent quality control is feasible at the device wafer level. It will be possible to reprocess defective wafers at this point rather than continue their processing, thus eliminating very large potential losses that would be caused by completing defective materials into finished IC devices. Even more important, these expedient, sensitive, and non-destructive test methods allow rapid information feedback of the test results to the production line and, thus, immediate correction of faulty processing conditions. In addition to being an early, rapid detection system for defects occurring on the production line, the new test methods are a valuable tool for assessing developmental studies for improving materials and processes.

The methods developed and perfected during this program also make it possible to test finished IC devices by the manufacturer (or by the procurement agency or individual customer), and allow a reasonable degree of presently nonexistent standardization of the integrity of overcoat passivation layers on finished IC products. In summary, the practical benefits of the new test methods are very considerable, when applied to production and product control, in terms of both cost savings due to early detection of production line defects and rapid information feedback for corrective action. Batch removal and batch reprocessing of defective material in wafer form will be an additional cost-saving factor.

2. INTRODUCTION

2.1 Background and Definitions

Most types of silicon integrated circuits (ICs) require a passivation overcoat layer to afford scratch resistance of the metallization interconnects during processing; to prevent alkali ions and other impurities from contaminating the device, especially with plastic-encapsulated devices; and to provide protection against the effects of loose particles in the case of hermetically sealed packages. Rf-sputtered or, more commonly, chemical vapor-deposited (CVD) films of silicon dioxide or phosphosilicate glass (PSG) are generally used as the passivation layer. Both bipolar- and MOS-type ICs used in recent years have been fabricated using passivation layers which, in some cases, have cracks, pinholes, or inadequate coverage of the edges of delineated lines of aluminum conductors (the metallization material most frequently used in ICs), or thin-film resistors. These defects can result in device failure as a result of corrosion of aluminum metal conductors or of oxidation of thin-film resistors. Defects of this type can clearly give rise to serious reliability problems of ICs, and must therefore be controlled and minimized.

Although specifications for high-reliability ICs generally require passivation coatings, they do not provide methods for evaluation of the integrity of these coatings or for rejection of unsuitable coatings that have the specified thickness. Known methods for defect detection and measurement have many drawbacks, which will be discussed. The purpose of this research contract was to devise and to refine suitable analytical control methods for this purpose that do not suffer from such drawbacks. This has been successfully achieved, as demonstrated in this report.

2.2 Objective, Scope, and Approach

One objective of this program was to innovate and develop techniques for evaluating the integrity of passivation overcoats on metallized ICs, and, specifically, for devising practical techniques to detect localized structural defects and to measure their population density.

The techniques to be developed should be suitable for routine quality control by manufacturers, be applicable both to IC devices in wafer form and to individual pellets, and allow estimation or quantization of the number of localized structural defects (such as pinholes and microcracks) per unit area in the oxide or glass overcoat. Preferably, the method should be essentially nondestructive; that is, not damage areas that are defect-free.

Our experimental approach consisted of three main types of promising methods to be explored, developed, and assessed to allow comparison: (1) selective chemical etching of metal to make defects readily visible; (2) electrophoretic defect decoration; and

(3) electrostatic corona-charge decoration of defects. The method selected was expected to be one of these methods (or a combination) to offer the maximum amount of reliable information that can be gained with the simplest, most direct technique. A further task was to explore techniques for quantitative automated measurements of the defect density per unit area on samples where the defects had been made visible by the three methods outlined above.

2.3 Organization of Report and Related References

The main sections consist of: (1) brief review of dielectric defects and methods for their detection; (2) presentation of experimental results of the new analytical methods developed and optimized; (3) critical comparison of the performance of the new methods; (4) examples of applications; and (5) recommended methods, techniques, and test procedures.

For the purpose of brevity, and to avoid duplication, extensive use is made of references to the following related basic papers we have recently published: Survey of methods for detecting and characterizing localized defects in dielectric films [1]*, and their relation to device reliability [2]; origin of such defects [3] and their relation to electrical film properties [4]; analysis of glass passivation overcoats by selective etching techniques [5]; improved techniques for depositing and testing CVD passivation layers [6]; and, finally, survey of electrostatic and electrophoretic principles and processes [7].

In some cases, for the sake of completeness or to provide desirable background information, this report contains results generated during RCA-supported research studies.

*Bracketed numbers pertain to citations shown on pages 103 to 105.

3. DEFECTS IN GLASS PASSIVATION LAYERS AND METHODS FOR DEFECT TESTING

3.1 Types and Causes of Defects and Their Effects on IC Reliability

Defects in the glass passivation overcoat of ICs can give rise to several types of failure mechanisms that may seriously impair the reliability of the device. Such defects can be classified into the following major groups: (1) localized structural and compositional defects; (2) nonlocalized chemical and physical defects; (3) defects due to chemical interactions of dielectric with metallization and moisture; (4) defects due to ionic and electronic charge motion and conductivity in glass and oxide films, on their surfaces, and along their various interfaces; and (5) assorted defects introduced during passivation processing. Each of these groups has been discussed in detail [6].

Of primary concern in the present work are the localized structural glass defects [1-6] that can originate from several sources. Particulate contaminants (dust or reaction products) in the gas or vapor streams or on the substrate surface during chemical vapor deposition interfere with film nucleation and proper growth, resulting in voids, thin spots, partial or complete pinholes, or hillocks. Particulate impurities that become embedded in the film constitute a potential device failure due to local weakening of the dielectric strength.

Pinholes in the films can also be caused by problems in photolithographic processing if the photoresist protects the film incompletely, if the photomask causes mechanical damage during the contact printing step [3], or if the etchants used in the chemical patterning process penetrate through pinholes or thin spots in the resist coating itself. Pinholes in the glass overcoat may also be caused by aluminum grain growth during CVD [8,9] or by impact during chip handling [1,9,10]. Cracks in the CVD oxide or glass passivation over aluminum in linear bipolar ICs seem to be the cause of increased susceptibility of metal corrosion during device operation, which led to serious field failure [11,12]. Localized structural defects, in general, often open the way to migrating ionic contaminants [13] that are always present in plastic encapsulants or on the device surfaces after chip mounting, bonding, and normal processing operations.

Next to pinholes, microfractures are a very common and important mode of a localized defect often caused by excessive stress in the glass layer covering the metallization interconnects. Microfractures can also be caused by differences in the coefficients of thermal expansion between the dielectric film and the substrate or between different types of films. Stress in films may develop during growth, deposition, pattern etching or heat treatments, especially if the linear thermal expansions of the components are mismatched. Cracks may form, particularly during thermal shock preceding or following high-temperature processing, excessive thermal contraction on cooling, or temperature stress cycling and life-testing of devices. Silicon ICs packaged in frit-sealed ceramic packages have been particularly susceptible to microcracks in

the silicon dioxide or PSG overcoat, mostly over large areas of aluminum such as those used as the counterelectrodes of capacitors [1]. The cause of this failure is the relatively high temperature (530°C) needed for fusion of the glass frit sealing the ceramic package. The stress in the glass overcoat passivation becomes so great that stress release occurs by cracking, especially over large metal areas and along their edges. Device failure may occur subsequently, due to penetration of sodium ions through the cracks and lateral penetration along the metal/glass interface or in the field oxide. The sodium originates from the glass frit and cannot be avoided in the atmosphere of the package; it is normally gettered by the PSG. Similarly, tensile cracks can occur during eutectic bonding of devices, particularly when chip bonding temperature exceeds the glass deposition temperature. This may occur when gold-silicon eutectic bonding is used, and is chiefly true when aluminum-germanium eutectic alloy with a melting point of 424°C is used to achieve a hard-solder joint containing no elements of high atomic number. During the bonding operation, internal tension in the CVD film combined with stress caused by mismatch in linear coefficients of thermal expansion of silicon dioxide (or PSG) and aluminum (or thin-film resistor alloy), can cause cracking of the passivation layer, often along the edges of delineated patterns of conductors.

Uneven topography of the substrate being coated with a dielectric film may result in thin spots over sharp edges or film discontinuities in corners at the base of steep steps, thereby leading to electrical short-circuits. Unacceptable topographical defects, such as excessive surface roughness, may also arise during film deposition under incorrect process conditions. Recent analytical results on localized structural defects in various types of glass overcoats on bipolar and CMOS devices have shown that, in addition to pinholes [5] and microcracks [9], defects frequently encountered are due to improper glass coverage of metal lines [9].

Gas bubbles that weaken the dielectric strength in an insulator may form during chemical vapor deposition in the presence of nucleating particulate contaminants. Other localized defects include embedded foreign particles, microcrystallites, or precipitates caused by reactions in the solid state. Oxides and glasses may devitrify in local regions under certain conditions, and may deleteriously affect film integrity and dielectric strength.

3.2 Conventional Methods for Defect Testing

Methods for testing dielectric films for the presence of localized structural defects may simply detect the defects by observation without altering them, or may make them more readily visible by decoration, by reaction, or by etching of the substrate.

Typical examples of direct detection methods are: optical microscopy, light-scattering techniques, scanning electron microscopy, transmission electron microscopy, and replica electron microscopy [1].

Examples of decoration methods are: electrophoretic particle transport techniques [1] and electrolytic decoration with copper oxysalts [14,15]. Methods based on reaction at the defect sites are nematic liquid-crystal light-scattering in an electric field to produce readily visible vortices above the defects [8,16]; formation of trains of hydrogen gas bubbles rising from the defect sites [14]; electroautographic techniques [14]; and self-limiting dielectric breakdown [17] where a deposited thin-metal film electrode disrupts, indicating the location of a defect.

Selective etching of the substrate to produce a readily visible pit or enlarged demarcation area is one of the earliest techniques used for revealing defects in dielectric films. In the case of silicon dioxide films on silicon, the etchant can be hot chlorine gas [18,19], pyrocatechol - ethylene diamine - water mixtures [20,21], catechol-hydrazine reagent [22], aqueous 10% sodium hydroxide solution at 70°C [23], or a common silicon etchant such as 70% nitric acid with 4 to 6 % volume of 49% hydrofluoric acid. Silicon dioxide films on metal substrates require different treatments. Anodization or ceric sulfate etching have been described for nickel-chromium [24]; alkaline etchants [24], concentrated acid solution [25], or phosphoric acid-based etchants [1] for aluminum; and extended hot water treatments for molybdenum [25].

The defect detection methods enumerated above have been reviewed in detail and illustrated in a recent survey [1] and therefore will not be further discussed here.

3.3 Shortcomings of Conventional Methods

Critical evaluation has shown great merit in most of these methods for specific applications. However, each of the methods available at the time we started our investigation under the present contract suffered from several or all of the following shortcomings: (1) destructive, and hence, expensive; (2) not sensitive to latent or partial defects (such as thin spots); (3) inadequate for production control; (4) slow and not suitable for automation; (5) subjective, because read-out by operator is required; (6) not standardized in present form and, hence not comparative on an absolute basis; (7) results ambiguous: not reproducible consistently or not reliable; and (8) applicable only to very specific problems, rather than generally applicable for testing any dielectric.

3.4 Methods Investigated and Developed During This Research Contract

The methods developed for evaluating the integrity of glass passivation overcoats on metallized ICs were to be based on measurements of density of pinholes, microcracks, and thin spots in dielectric by suitable techniques. The methods were to be applicable for the analysis and process control of both device wafers and single IC pellets and, furthermore, for detection of localized structural defects in dielectric layers on conductive substrates in general. The shortcomings of present methods listed in the previous sections were to be eliminated or, at least, minimized as much as possible.

From exploratory research performed prior to this contract we felt that a developmental research program based on the following methods would be most promising:

- (1) Metal demarcation etching.
- (2) Metal/Insulator sequential etching.
- (3) Electrophoretic decoration with intensely uv-luminescing phosphor or powder particles.
- (4) Electrostatic charging followed by direct or reverse decoration with phosphors or carbon black particles.
- (5) Techniques for quantifying the defects found by the above techniques.

Method (1) is a conventional selective etching technique that would be optimized primarily as a baseline standard for comparing the performance of new techniques. Method (2) was intended to provide unique information on defect density as a function of dielectric layer depth. The electrophoretic method (3) had been previously demonstrated to be feasible [1], but had not been optimized in any way. The electrostatic method (4) had also been outlined and demonstrated as feasible [1] and appeared to offer remarkable possibilities. Indeed, this method has proven to be the most useful and sensitive technique for dielectric defect detection now available, as will become apparent in the course of the presentations to follow. The measuring technique (5) was intended for rapid and quantitative read-out, preferably by optical techniques and suitable for automation. Standard optical and electron microscopic methods were to be used extensively for direct examination of defect sites. Finally, the best method(s) and techniques were to be formulated into one practical and reliable procedure suitable for routine device wafer quality control by manufacturers, as well as for acceptance testing and reliability analysis of single IC pellets.

4. EXPERIMENTAL STUDIES AND METHOD DEVELOPMENT

4.1 Metal Demarcation Etching

4.1.1 Principle

Structural localized defects, such as pinholes and microcracks, in dielectric layers over a substrate can be seen with a microscope by exposing the sample to a selective etchant that attacks the substrate but not the coating; examples have been noted in the previous section. In a thick substrate the selective etchant produces a pit; in a thin substrate film, such as a metal film on a thick support, the selective metal etchant dissolves the metal where a defect in the coating exists. In either case, to be effective, the opening of the defect must be wide enough for the etchant to penetrate, and the interfacial tension of the etchant at the dielectric interface must be such that it facilitates penetration. Furthermore, the etching time must be adequate to achieve reasonable demarcation by allowing the etchant to attack and dissolve a sufficiently large quantity of the substrate laterally underneath the intact areas of the coating, so that a demarcation many times the diameter of the defect in the dielectric results.

4.1.2 Materials and Equipment

Sample material for systematic etching methodological studies consisted of both planar test samples and glassed ICs.

Test samples were polished silicon wafers that had been thermally oxidized to have silicon dioxide thicknesses of 0.5 to 1.2 μm . Films of pure aluminum, 0.5 to 1.8 μm thick, were deposited by vacuum evaporation. Overcoats of silicon dioxide or PSG films were deposited by CVD techniques at 450°C [3]. The overcoat thicknesses ranged from 0.2 to 1.8 μm , depending on the defect type and density desired. In general, the pinhole density decreased with increasing glass thickness or higher phosphorus content, while the density of microcracks increased with increasing glass thickness and lower phosphorus content due to higher film stress. Device wafer samples consisted of bipolar linear ICs with large aluminum-metallized capacitors that are especially sensitive to stress cracking of the glass coating. The aluminum thickness ranged from 1.3 to 1.8 μm . In addition to aluminum-metallized samples, several other types of metallizations were briefly explored (see section 4.1.6).

A phosphoric acid-based mixture (table 1) was used as a selective aluminum standard etchant. Hydrochloric acid-based and sodium hydroxide-based etchants were used in initial exploratory tests to be noted. A regulated constant temperature bath was used to maintain the agitated etch bath at a constant temperature ($\pm 0.5^\circ\text{C}$).

Binocular stereo-microscopes as well as research microscopes were used, each set up for a particular optical mode of observation and photographic recording. Selected samples were examined by scanning electron

TABLE 1. CHARACTERIZATION OF VARIOUS ALUMINUM ETCHANT COMPOSITIONS AT 50°C.

Etchant Composi- tion, #	Components, Vol. %				Surfactant		H ₃ PO ₄ /HNO ₃ Ratio	Aluminum		Sample Etch Time (2) Used, (s)	Relative Defect Density (3)
	H ₃ PO ₄	HNO ₃	C ₂ H ₅ CO ₂ H	H ₂ O	Wt/ Vol %			Etch Time, (s)	Etch Rate, (Å/s)		
	85%	70%	100%	Dist.	Type						
1 (Standard)	74.1	7.4	-	18.5	none		10.1	120	150	150	standard
2	70.0	15.0	15.0	-	none		4.67	80	235	100	same
3	57.5	12.5	30.0	-	none		4.60	100	180	125	same
4	78.5	16.5	5.0	-	none		4.76	75	191	94	same
5	77.0	3.0	15.0	5.0	none		25.3	105	171	131	same
6			standard		A	0.05	10.1	107	168	134	same
7			standard		B	0.05	10.1	95	189	109	same
8			standard		C	0.05	10.1	100	180	125	same
9			standard		D	1.0	10.1	107	168	134	same

A : An anionic ammonium perfluoroalkyl sulfonate.

B : An anionic potassium perfluoroalkyl sulfonate.

C : An anionic potassium perfluoroalkyl sulfonate.

D : A non-ionic polyalkylene glycol ether.

(1) Vertical etch time based on a pure aluminum thickness of 18,000 Å.

(2) Based on an etch time factor of 1.25.

(3) Microcrack density in 12,000 Å-thick CVD SiO_2 glass over aluminum with respect to etchant No. 1 (standard).

microscopy (SEM) at various angles of incidence, including cross-sectional viewing.

4.1.3 General Test Procedure for Demarcation Etching

The procedure consists simply of immersing the sample piece on a plastic holder (such as a slotted, soft plastic tubing) in the agitated etch solution, typically at 50°C, for a predetermined period of time. This period (usually 1 to 3 min) depends on the aluminum thickness, the size range of the defect openings, and the degree of demarcation desired, as will be discussed in section 4.1.5 on etching parameters. Following the etching, the sample is thoroughly rinsed in deionized water, blotted dry between filter paper, and examined under the microscope.

4.1.4 Examination of Glass Defects by Optical and Scanning Electron Microscopy

Typical localized structural defects encountered in relatively thick (0.7 to 1.8 μm) glass layers over aluminum films on oxidized silicon were examined more closely by microscopy before and/or after selective demarcation etching. A selection of representative photomicrographs is presented in this initial experimental section.

Simple microcracks (but not pinholes) in glass layers over aluminum are usually visible with difficulty under a carefully focused optical microscope without special treatments, as shown in figure 1. Demarcation etching of the aluminum film substrate of the sample shown in figure 1 marks the area under the glass crack as seen in figure 2 at the same magnification (385X)*, making it more readily visible. The dark band is the oxidized silicon substrate from which the aluminum film was etched away. The glass film covers the hollow groove except for the center region where the glass crack is visible as a thin double line. Continued aluminum etching widens the dark band further.

Scratch-induced glass defects as seen after aluminum etching are shown in figures 3 and 4. A microcrack formation of strange appearance is shown in figures 5(a) and (b) at a magnification of 500 diameters after 20 and 30 min of aluminum etching, respectively. The thickness of the aluminum region of this sample was 1.8 μm , and that of the CVD PSG overcoat, 1.4 μm . Scratch-induced line cracks and pinholes in similar types of samples are shown in figure 6, and self-terminating loop-cracks in figure 7.

Severe stress cracks formed in a 1- μm -thick CVD silicon dioxide layer deposited over aluminum squares on oxidized silicon are shown in figure 8. The cracks were made easily visible by selective aluminum etching. Most of the edges over the metal patterns are seen to be cracked, and there are numerous cracks within the metallized areas.

*All magnifications cited refer to actual diameters as seen in the figures.

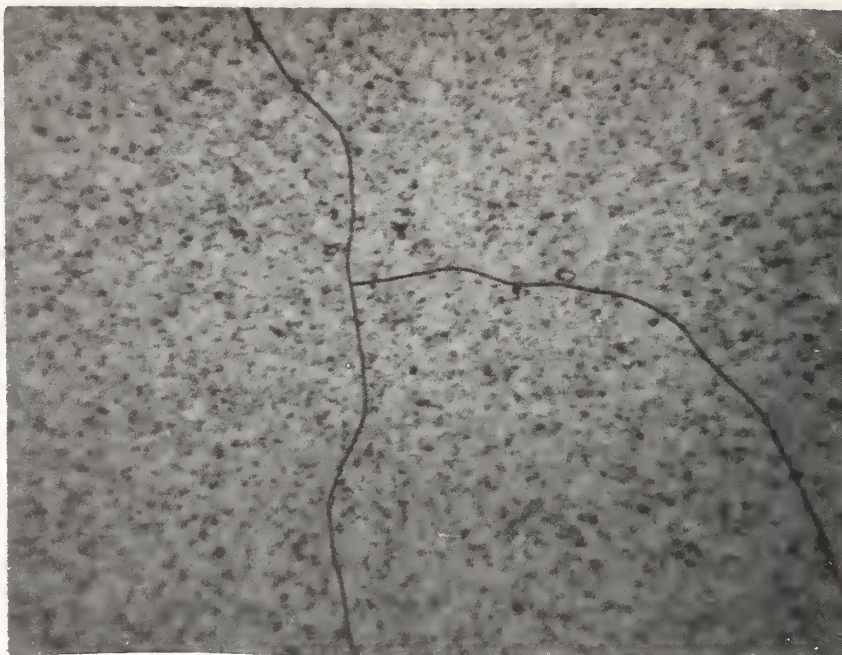


Figure 1. Optical photomicrograph of untreated cracks in a 1.4- μm -thick CVD PSG layer over a continuous 1.8- μm -thick layer of aluminum on oxidized silicon. Pinholes (if present) would be invisible because of metal grain structure (385X, bright-field).



Figure 2. Etching-demarcated microcracks in sample shown in figure 1. Dark bands are substrate from which aluminum was removed from underneath glass layer in 10 min selective metal etching at 50°C. Glass crack is dark line in center of 15-18- μm -wide bands. No pinholes are present in this sample area (385X, Nomarski differential interference contrast).



Figure 3. Scratch-induced heavy damage in glass layer made visible by 20-min aluminum etching. Scribe direction was apparently downward with increasing pressure. Sample structure as noted in figure 1 (385X, brightfield).



Figure 4. Scratch-induced microcracks in glass layer similar to figure 3. Most damage occurs in V-shaped part of pattern. Maximum spread of demarcation is 80 μm (385X, brightfield).



(a)



(b)

Figure 5. Optical photomicrograph of microcrack structure in 1.4- μm -thick PSG layer on a 1.8- μm -thick aluminum layer on oxidized silicon. (a)-incompletely demarcated by selective etching for 20 min. (b)-completely demarcated by additional 10 min of aluminum etching (500X, brightfield).

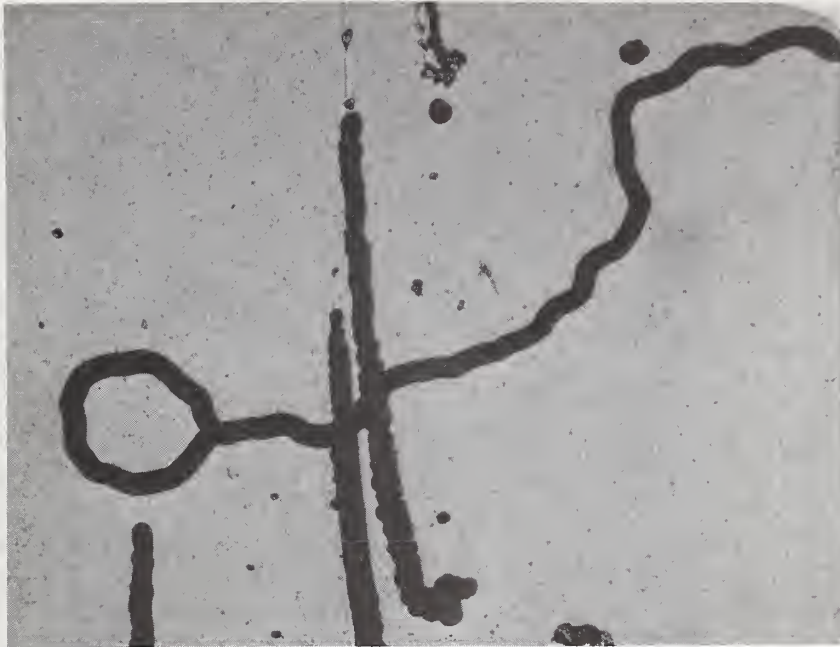


Figure 6. Stress- and scratch-induced cracks and several pinholes in 0.7- μm -thick PSG layer on 1.8- μm -thick aluminum layer on oxidized silicon. Demarcation-etched for 20 min. Width of circular band is 25 μm (200X, brightfield).

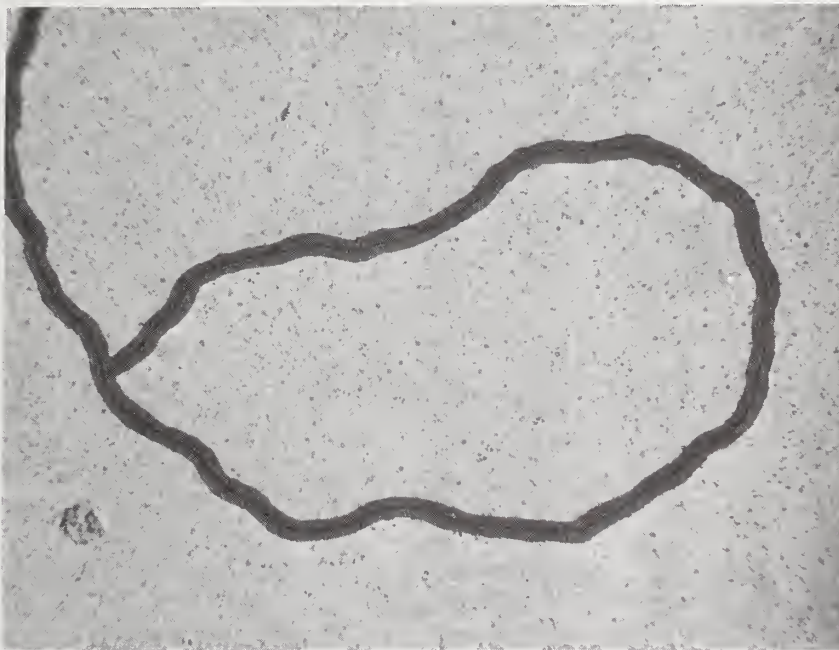


Figure 7. Circular, self-terminating crack pattern in glass layer as in figure 6 except that PSG is 1.4 μm thick (200X).



Figure 8. Optical photomicrograph of stress cracks of a CVD silicon dioxide film of 1- μm thickness deposited over oxidized silicon with squares of 105 x 105 μm of evaporated aluminum. Demarcation was achieved by 10-min aluminum etching. Cracks surround most of pattern along edge of aluminum. Differences in the width of the inside area are most probably caused by differences in the width of the cracks (150X, brightfield).

Selected samples were examined by SEM at various angles and magnifications to provide high-magnification micrographic records of glass defects for comparison with optical photomicrographs, to measure the width of typical glass cracks, and to demonstrate the predicted cross-sectional shape of demarcation etched structures. Representative results are presented pictorially in figures 9 to 13.

4.1.5 Parameters of Selective Aluminum Etching

The results of a systematic investigation aimed at optimizing the selective chemical etching technique for detecting localized structural defects in glass layers over aluminum-metallized ICs are summarized in this subsection. Variables examined include etchant composition, addition of surfactants, etching temperature and time, use of ultrasonic agitation, and vacuum impregnation to enhance penetration. The development of demarcation areas for microcracks in silicon dioxide layers over aluminum capacitors of IC test wafers with a high density of uniformly distributed microcracks was employed as a criterion for quality of resolution.

4.1.5.1 Optimum Etchant Composition - Nine different compositions, with and without surfactants, were formulated and tested at 50°C on a comparative basis. The etch rate of each composition was first determined for pure aluminum. On this basis the etch times to be used for evaluating the various compositions were then calculated using a constant etch time factor of 1.25, the factor for just etching through the aluminum being 1.00. The experimental data presented in table 1 (section 4.1.2) show that the defect detection sensitivity is the same for all compositions. One may therefore continue to use our "standard composition" defined in table 1.

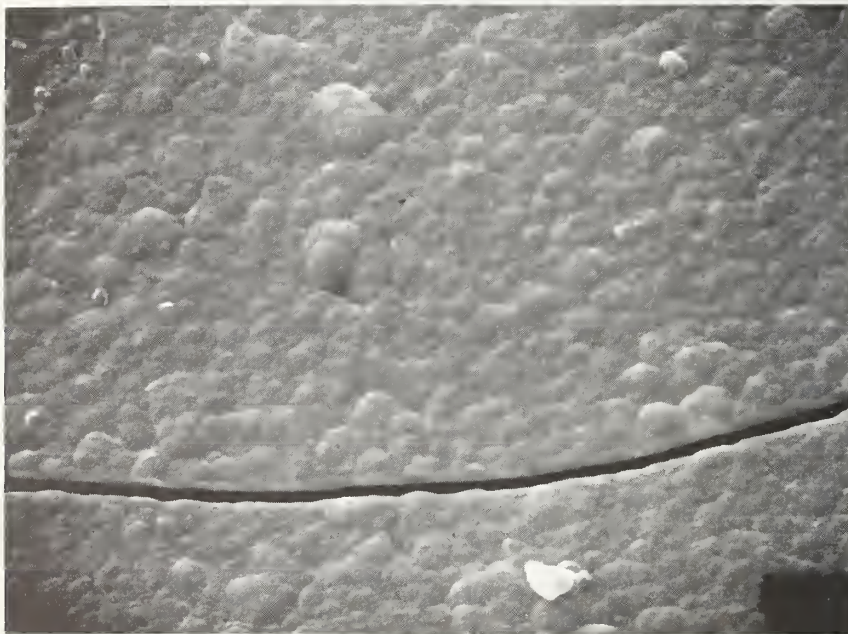
4.1.5.2 Optimum Etching Temperature - Using the standard etchant, effects of 10°C above and below the normal temperature of 50°C were tested by the technique described above. The data presented in table 2 show no difference in defect detection sensitivity, so that we have continued to use the temperature of 50°C, which affords a convenient etch time.

4.1.5.3 Optimum Etching Duration and Etch Time Factor - Using the same type of IC samples as above, we tested the optimum etch time at 50°C in standard etchant with respect to completeness of detection of all structural defects in the dielectric that penetrate down to the aluminum, to sharpness and definition of demarcated defects, and to rate of undercut-etching.

Etch time was normalized and expressed in terms of the "etch time factor," defined as the actual etch time used for a sample over the etch time required to just etch through the aluminum. The half-widths of the aluminum removed under the glass served as a convenient measure of the lateral etch rate.



(a)



(b)

Figure 9. Scanning electron micrographs at 5000X of untreated microcrack in 1.4- μm -thick PSG over 1.8- μm -thick evaporated aluminum on oxidized silicon substrate wafer. Width of crack is about 0.4 μm . (a)-45° view and (b)-25° view from perpendicular.

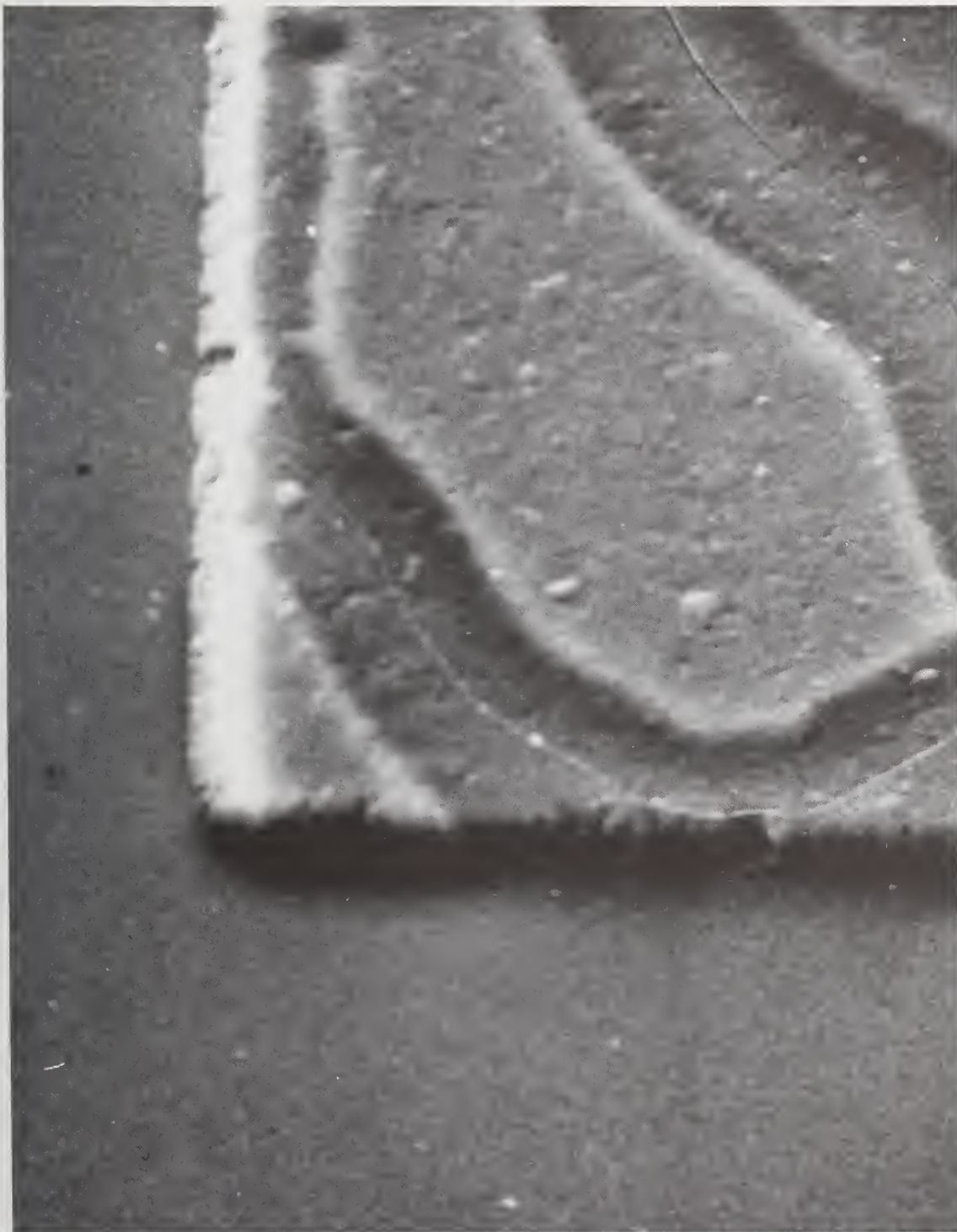


Figure 10. Scanning electron micrograph (2400X, 30°) of demarcation-etched stress cracks. Sample as defined in figures 8 and 9. No cracks exist in overcoated oxide layer between aluminum patterns.

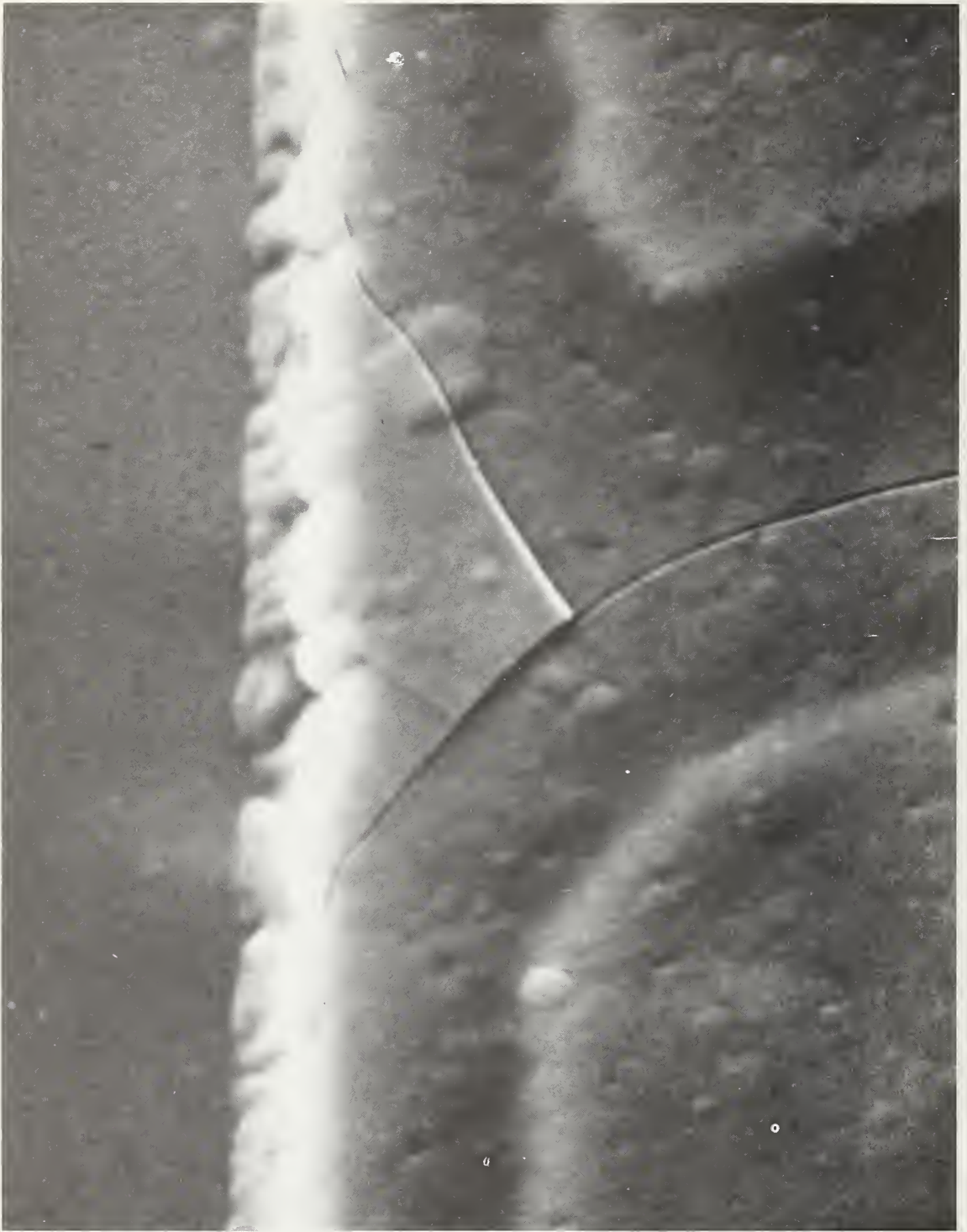


Figure 11. Scanning electron micrograph (4800X, 30°) showing a different area of sample from figure 10. Gray channel areas are caused by differences in charging due to etched-out aluminum under glass.



Figure 12. Glass microcracks in sample shown in figures 8, 10 and 11 as observed by SEM at 4800X and 30° from the perpendicular. Width of crack from this high-magnification photograph is approximately 0.2 μm .

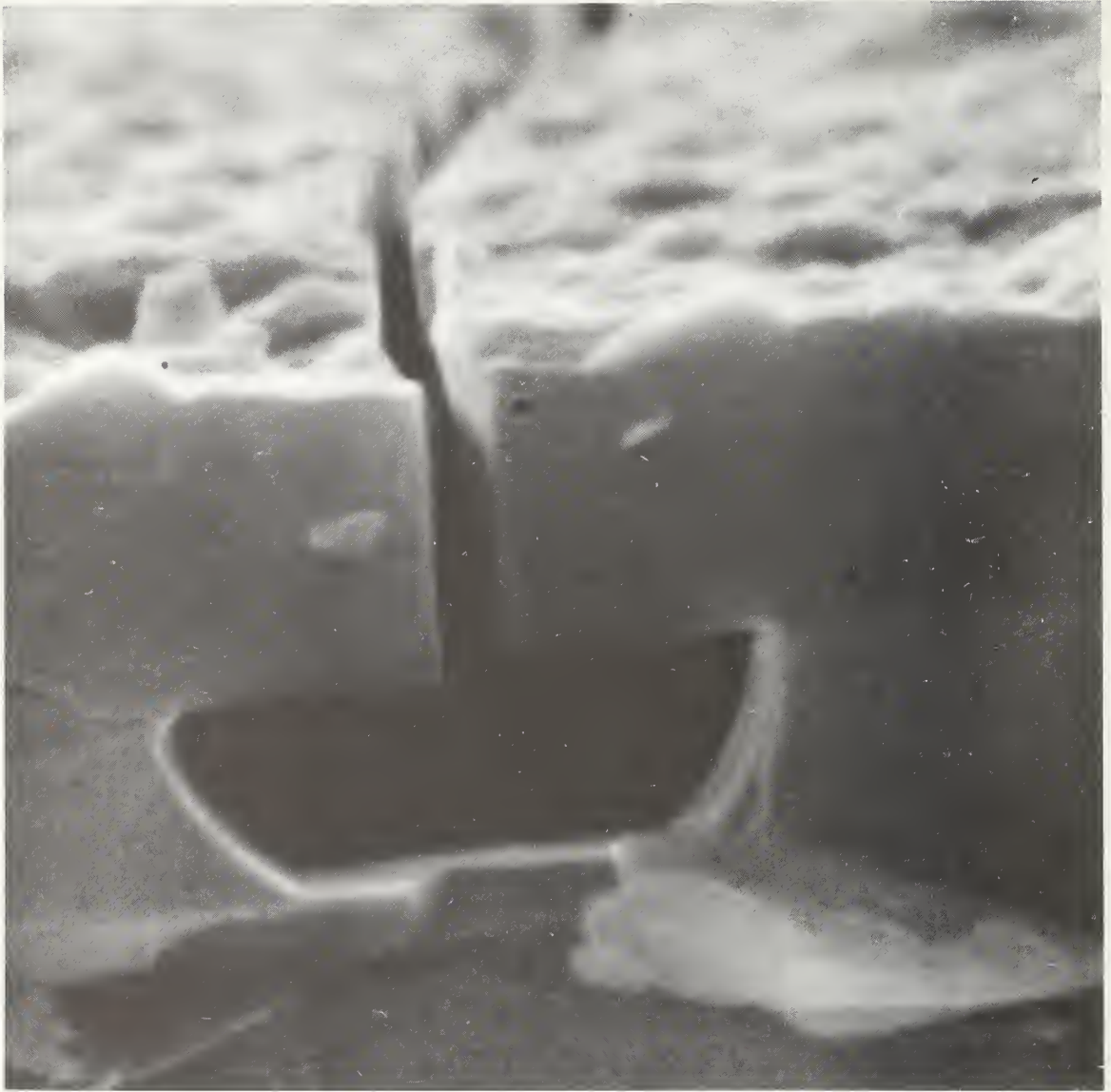


Figure 13. Cross section SEM of a demarcation-etched structure. Sample consisted of a stress-cracked CVD PSG passivation layer over aluminum on oxidized silicon. Cavity formed in aluminum by selective etching underneath glass exhibits curved side walls caused by normal isotropic etching.

SEM magnification: 23,500X
Thickness of glass coating: 1.8 μm (top layer)
Width of glass crack: 0.4 μm
Thickness of aluminum: 1.2 μm (center layer with cavity)
Thickness of thermal oxide: 0.7 μm (bottom layer on silicon)

TABLE 2. EFFECTS OF TEMPERATURE AND TIME ON ALUMINUM ETCHING

Variable Parameters	Temp. of Etchant (°C)	Al Etch Time (1) (min)	Al Etch Rate (Å/s)	Etch Time Factor	Sample Total Etch Time (2) (min)	Al Etch Half-Width (μm)	Defect Resolution (3) (150X)	Relative Defect Density (4)
Temperature Variation	40	4.25	71	1.25	5.33	3.0	very good	same
	50	2.0	150	1.25	2.50	3.0	very good	standard
	60	0.83	360	1.25	1.06	3.0	very good	same
Time Variation	50	2	150	1.25	2.5	3.0	very good	standard
	50	2	150	2.50	5.0	5.5	excellent	same
	50	2	150	5.0	10.0	7.5	poor	same
	50	2	150	10.0	20.0	11	poor	same
	50	2	150	15.0	30.0	15	poor	same

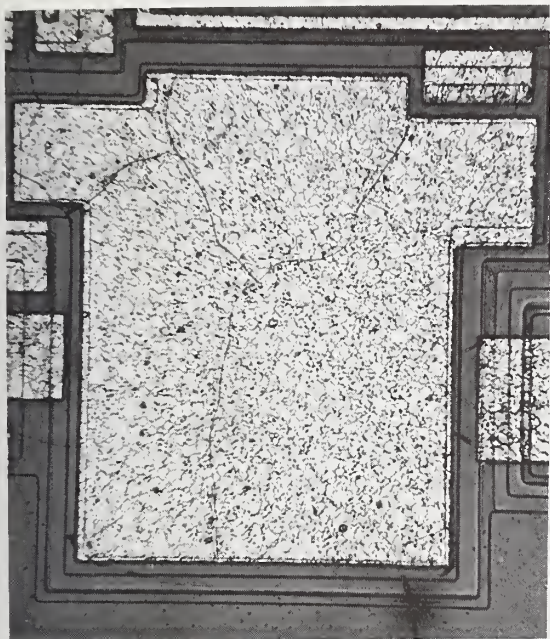
(1) Vertical etch time based on a pure aluminum thickness of 18,000 Å.

(2) Based on an etch time factor of 1.25.

(3) "Poor" rating was given to etch widths 15 μm and above, since closely adjacent defects could be masked by overetching.

(4) Microcrack density in 12,000 Å CVD SiO₂ glass over aluminum with respect to standard etch conditions.

- Figure 14. Optical photomicrographs of microcrack in a continuous 1.2- μm -thick silicon dioxide film over aluminum-metallized linear bipolar IC wafer. Large light area is a metallized capacitor of 430 μm length (150X, brightfield).
- (a)-Untreated sample; fine microcracks are just barely visible.
 - (b)-Demarcation-etched in aluminum etch at 50°C by an etch time factor of 1.25; crack pattern over aluminum areas is now readily visible. Previously non detectable defects in smaller metal areas can now be seen.
 - (c)-Additionally etched sample corresponding to an etch time factor of 2.5; cracks along the periphery of the metal areas have now become visible.
 - (d)-Etch time factor of 5.0; peripheral crack demarcations are seen to be 1/2 the width of the inside area bands, indicating that they occur exactly along edge of pattern. Portions of one interconnect line are seen to be the only undamaged parts in this sample area. Differences in the width of the inside demarcation bands in various areas seem to indicate differences in width of the crack, affecting the rate of demarcation etching.



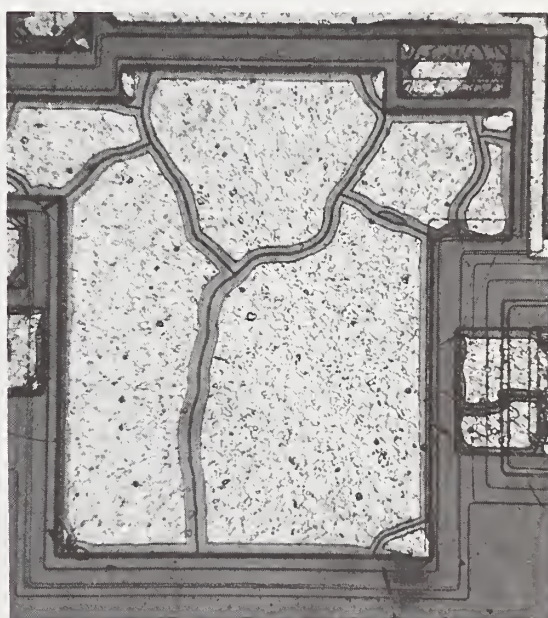
(a)



(b)



(c)



(d)

Etch time factors of 0, 1.25, 2.50, 5.0, 10.0, and 15.0 were tested by photographing the same sample position under the microscope at several magnifications after each etching treatment. The first four consecutive steps are shown in figures 14(a) to (d); detailed explanations are presented with each photomicrograph. The lateral etch rate for etch time factors greater than one can be expressed by a linear curve. For the samples shown, the lateral etch rate is $0.4 \mu\text{m}/\text{min}$, but the rate depends on crack width.

From the photographs and the data presented in table 2, we concluded that an etch time factor of 1.25 is best for maximum planar resolution on samples with a high density of defects. A factor of 2.5 widens the defect site considerably, making it more readily visible; also, edge defects not previously noticeable become clearly visible along the periphery of the aluminum pattern. Larger etch time factors have little merit since they decrease the detection resolution.

Figures 15(a) and (b) are the samples from figures 14(c) and (d) shown at a higher magnification. They show clearly that the glass over the large aluminum areas, but not over the line interconnects, had cracked along the edges.

The series of photomicrographs presented in figures 16(a) to (d) shows the growth of demarcation areas around pinholes for etch time factors of 0, 1.25, 2.5, and 5.0. Note that the pinhole density remains constant on prolonged etching. Again, the lateral etch rate depends on the defect size.

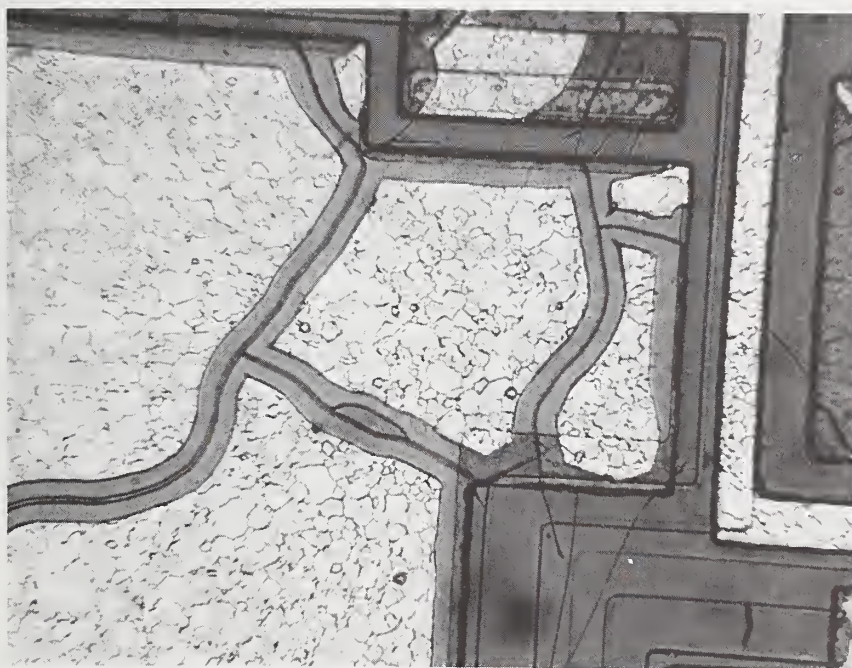
4.1.5.4 Ultrasonic Etching - The effect of ultrasonic agitation on the etching at 50°C of aluminum under cracked glass was investigated by using IC samples that had been etched under normal conditions with an etch time factor of 1.25. No new defects became visible as a result of continued etching with ultrasonic agitation. However, the protruding glass film overhang above the etched-out aluminum was removed by this treatment, leading to irregularly tapered aluminum edges. The aluminum etch rate increased by a factor of approximately three. No advantage was found by this technique.

4.1.5.5 Vacuum Impregnation - Impregnation with etchant under reduced pressure (0.3 torr) was tested to see whether removal of air from the defects prior to etching could increase the defect detection sensitivity. A pre-etched sample was used, as above. No new defects could be discovered by this technique. The aluminum etch rate increased three-fold, probably due to increased speed of penetration of the etchant.

4.1.5.6 Defect Detection Sensitivity - We have clearly shown that the rate of lateral etching during metal demarcation is dependent on the size of the defect opening in the dielectric layer, regardless of whether the defect site is a pinhole or a microcrack. The smaller this opening, the slower the penetration, and hence, the lower the rates of mass transport and etching. It follows that at a certain limiting dimension the penetration should become nil. SEM studies of microcracks at their

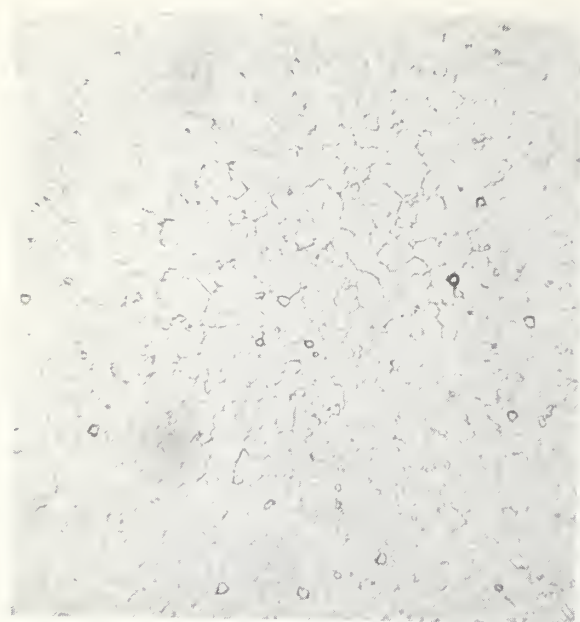


(a)



(b)

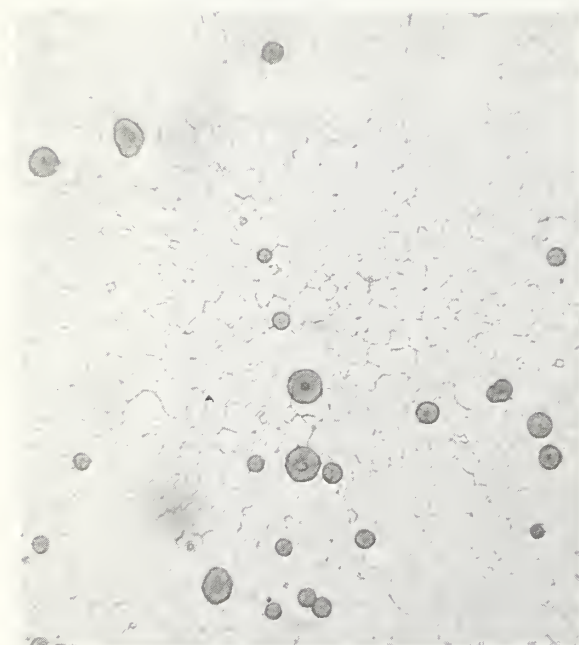
Figure 15. Detailed optical photomicrographs of demarcation-etched glass cracks. (a)-same as figure 14c but at 2.6X higher magnification. (b)-same as figure 14d but at 2.6X higher magnification.



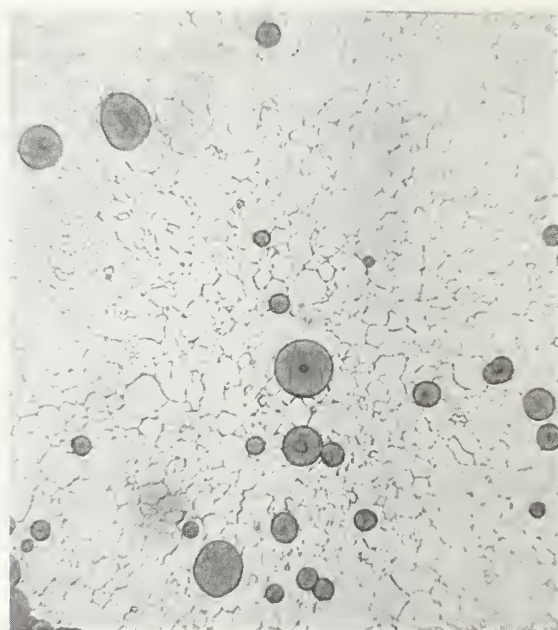
(a)



(b)



(c)



(d)

Figure 16. Optical photomicrograph of pinholes in a PSG layer over aluminum as a function of increasing etch time factor: (a)-0; (b)-1.25; (c)-2.5, and (d)-5.0. It is seen that no new pinholes become demarcated beyond a factor of 1.25. Small size demarcations (indicating small pinholes) increase much more slowly in size on continued etching than longer ones, indicating that the rate of demarcation growth depends on the defect size, as noted for microcracks (385X, bright-field).

terminal thinning-out ends have shown that the limiting crack width for a 1- μ m-thick PSG layer over aluminum interconnects is below 500 Å. In other words, a crack width of 500 Å still allows the aluminum etchant to penetrate and etch laterally at a sufficient rate to demarcate the defect under the typical conditions of selective etching. Extending the etching time to correspond to etch time factors of 5 to 15 should aid in further increasing the detection sensitivity, if this should be necessary.

4.1.5.7 *Other Aluminum Etchants* - Several other selective etchants for aluminum were tested at 50°C including sodium hydroxide solutions containing high-pH stable and active surfactants, and aqueous hydrochloric acid solutions containing low-pH stable and active surfactants. The sodium hydroxide etchants behaved similarly to the standard phosphoric acid-based aluminum etchant but were not superior to it, whereas the hydrochloric acid etchants operated erratically and etched nonuniformly.

4.1.6 Selective Demarcation Etching of Other Metal/Insulator Structures

The metal demarcation etching technique is applicable for testing other types of metallization and insulator systems as long as the metal etchant is selective in not attacking the insulator coating or the substrate.

Using the principle of this method, we have successfully analyzed structural localized defects in layers of silicon dioxide, PSG, borosilicate glasses, aluminum oxide, and silicon nitride over numerous metal substrates or delineated metal film. These metals and their etchants used include the following: tungsten and molybdenum etched with an aqueous solution of potassium ferricyanide and potassium hydroxide; platinum etched with aqua regia, gold etched with an aqueous solution of potassium iodide and iodine; chromium etched in a mixture of saturated ceric sulfate solution and concentrated nitric acid; copper with ferric chloride solution; and nickel with diluted nitric acid. (It should be noted in this connection that a nickel etchant consisting of nitric acid, acetic acid, and acetone must never be used because mixing nitric acid with acetone causes a violent reaction.) These etchants, used at appropriate concentrations, temperature, and time are suitable for defect demarcation testing. A brief summary is presented in table 3.

4.2 Metal/Insulator Sequential Etching

4.2.1 Principle

The method of demarcation by selective metal etching described in section 4.1 is capable of detecting only defects that locally expose the sublayer of metal. It would be highly desirable to have an additional method available for determining the density of buried or partial defects that extend only partially into the insulator layer, because such defects can seriously weaken the dielectric strength and protective properties

TABLE 3. SELECTIVE DEMARCATION ETCHING OF COMMONLY USED METAL FILMS COATED WITH OXIDE, GLASS, OR NITRIDE LAYERS.

<u>Metal to be Demarcated</u>	<u>Recommended Etchants and Conditions</u>		
	<u>Reagent</u>	<u>Quantity</u>	<u>Temperature (°C)</u>
Aluminum	H ₃ PO ₄ (85%)	20 vol	50
	H ₂ O (dist.)	5 vol	
	HNO ₃ (70%)	2 vol	
Chromium	K ₃ Fe(CN) ₆ (25%)	3 vol	23
	NaOH (33%)	1 vol	
Copper	FeCl ₃ (33%)		35
Gold	H ₂ O (dist.)	2400 ml	50
	KI (99.5%)	60 g	
	I ₂ (99.8%)	15 g	
Molybdenum	H ₂ O (dist.)	3 vol	23
	H ₂ SO ₄ (96%)	1 vol	
	HNO ₃ (70%)	1 vol	
Nickel	FeCl ₃ (33%)		50
Platinum	HCl (37%)	3 vol	23
	HNO ₃ (70%)	1 vol	
Tantalum	NaOH (30%)	19 vol	90
	H ₂ O ₂ (30%)	1 vol	
Tungsten	KOH (10%)	1 vol	35
	K ₃ Fe(CN) ₆ (10%)	1 vol	

of the insulator. Similar considerations hold for latent defects [26], such as structurally weak regions in the dielectric.

The examination of ICs for thinned-out insulator regions is another important aspect. Vapor-deposited dielectric layers over delineated metal steps are well known to constitute a serious reliability problem [2]. A reliable technique for determining the quality of metal or polysilicon edge coverage would therefore be of considerable practical interest.

The new test method described in this section is destructive and time-consuming, but is capable of solving these special problems of defect detection. It is based on first metal etching followed by sequential selective etching of the dielectric layer in steps of typically 20 or 25% of the total film thickness each, followed by the selective demarcation metal etching described in section 4.1. Microscopic examination of the same sample areas after each pair of etch treatments provides a quantitative measure of the increase in defects as a function of dielectric layer depth.

4.2.2 Test Samples and Materials

The same test samples, equipment, and metal etching techniques described in section 4.1 were used in these studies. Ammonium fluoride-buffered hydrofluoric acid solution as defined in table 4 was chosen as the room-temperature etchant for CVD layers of silicon dioxide and PSG because of its nonselectivity for phosphorus and its relative non-aggressiveness toward aluminum in the interconnect metallization. Aqueous 20 wt% hydrofluoric acid was used as a selective etchant for silicon nitride layers over gold or tungsten metallization, and for CVD borosilicate glass over tungsten, molybdenum, chromium, or nickel metallization on silicon.

4.2.3 Test Procedure

The average layer thickness of the metal and the dielectric overcoat are first determined by step etching and stylus-type profilometric measurements [5]. The respective minimum etching time for completely removing each layer in the selective etchants is then determined. From these data the demarcation etching time is calculated, usually for an etch time factor of 2.5. The etching time for removing passivation layer fractions of fourths or fifths is calculated from the etching time for removing the entire layer of measured thickness. Appropriate corrections may be necessary in the case of certain multilayer dielectric structures where components have significantly different etch rates.

The sequence of metal demarcation etching and dielectric section etching begins with the normal metal etching described in section 4.1. The sample is examined and photographed under the microscope for determining the defect density within well-defined areas, as will be discussed in detail in section 4.5. The first dielectric etching followed by a

TABLE 4. DEMONSTRATION OF SEQUENTIAL METAL-GLASS ETCHING METHOD.

Sample	Thickness (1)		Etch Time (2) (s)			PSG Etch Step	Residual PSG (Å)	Pinhole Density (3) (x 10 ² cm ⁻²) (Total)
	Thicknss (Å)		Total	1/5	1.25 Factor for Al			
	PSG	Al						
A	13,000	17,600	107	93	21	0	13,000	0.37
						1	10,400	0.74
						2	7,800	3.3
						3	5,200	10
						4	2,600	240
B	7,000	14,000	45	120	9	0	7,000	3.3
						1	5,600	3.7
						2	4,200	3.3
						3	2,800	9.6
						4	1,750	44
C	13,400	18,000	100	130	20	0	13,400	0.37
						1	10,700	1.5
						2	8,000	11
						3	5,400	28
						4	2,700	27

(1) Stylus type profilometric measurements.

(2) Etchants: a) HF-buffer, 25°C, for PSG layer [5]

b) Al-etch, 50°C for Al layer (table 1) [5];

Al-etch time factor = 1.25.

(3) Density determined by averaging five areas under 150X (brightfield illumination).

second metal etching is then carried out, and the same sample areas are re-examined under the microscope to determine the number of new defect sites. Additional pairs of dielectric/metal etching steps are carried out to obtain defect density as a function of dielectric layer depth.

4.2.4 Examples

A few typical examples presented to illustrate the technique are selected from methodical studies conducted to establish the capabilities of this analytical technique. The system PSG with or without silicon dioxide over aluminum on oxidized wafers of polished silicon is used because of its prime importance to the contract objectives. However, the method is equally applicable to other insulator/metal structures.

An analysis of three different samples is presented in table 4. It shows the increase in pinhole density as a function of layer depth in 20% steps, and indicates a drastic increase of pinhole density after 60% of the dielectric layer has been removed. A detailed interpretation of the results from this example is beyond the scope of the present objective.

Figure 17 shows the appearance of sequentially etched typical latent pinholes in an aluminum-metallized linear bipolar IC glassed with 1 μm of PSG after 50% of the glass overcoat was etched off. Very few pinholes existed in the initial sample. It can be seen that pinholes above the thermally grown silicon dioxide bottom layer are visible also by this sequential etching technique.

It may be mentioned in this connection that the vast majority of complete and latent pinholes in glassed aluminum-metallized ICs is always located above the aluminum, due to the roughness, spikes, and hillocks of typical evaporated aluminum layers. We determined by profilometric precision measurements that such localized high points in samples of the type treated in table 4 often measure up to 2800 Å before glassing, and up to typically 4200 Å after glass overcoating.

The quality - both integrity and layer thickness - of dielectric overcoats on the steps and edges of photolithographically delineated metal patterns is readily determined, as can be seen from the photomicrograph of a glassed IC shown in figure 18. Selective metal demarcation etching showed good edge coverage quality. Removal of 25% of the dielectric overcoat by section etching still showed no edge defects. However, severe defects developed after 50% of the glass layer thickness (measured in the planar areas of the sample) had been removed, as shown in figure 18. This result indicated that edge coverage had (a) good integrity and (b) an edge coating thickness between 50 and 75% of the average dielectric overcoat thickness, if one assumed that edges etch at the same rate as planar areas.

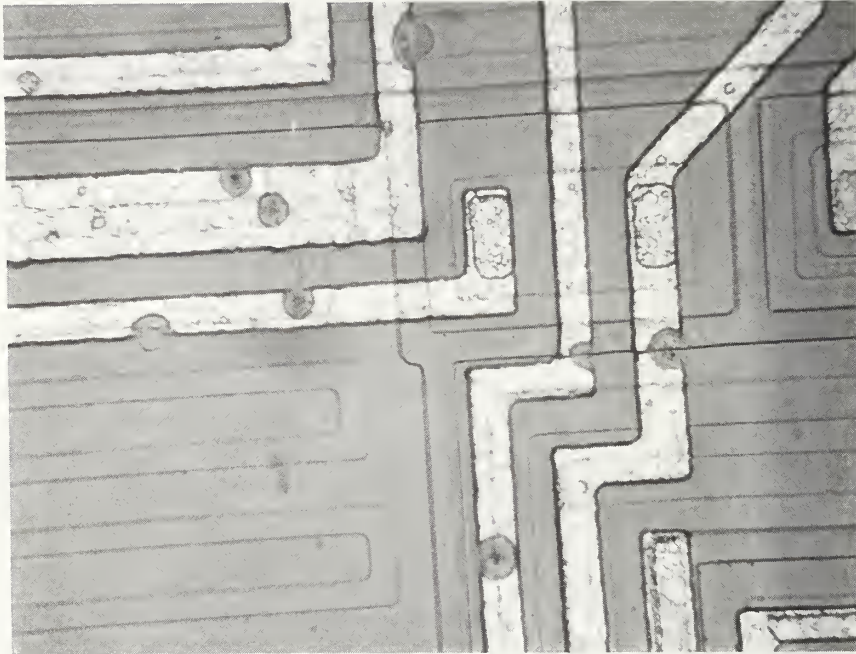


Figure 17. Developed partial pinholes in PSG passivation layer over aluminum interconnect pattern of an IC. These latent pinholes exposed the aluminum after 50% of the glass coating was removed by selective etching (385X, brightfield).



Figure 18. Developed thin edge coverage of PSG over edges of aluminum interconnect of an IC. The aluminum line edges became exposed in many places after 50% of the glass coating was removed by selective etching (385X, brightfield).

4.3 Electrophoretic Decoration

In this section conventional or cell electrophoresis for decoration of defects is discussed. A general introduction to electrophoretic principles is presented, followed by a discussion of the specific application to defect decoration on ICs. Finally, both the advantages and the limitations of the method are pointed out.

4.3.1 General Principles

In order to combine various powders and liquid vehicles most advantageously for useful decorating dispersions, an understanding of electrophoresis and electrodeposition is required. Electrophoresis is the motion of a charged particle suspended in a liquid in an electric field between two electrodes. Deposition of the particles on one electrode can occur as shown in the schematic in figure 19. Thus, the processes of electrophoresis and electrodeposition involve the mechanisms of particle charging, particle mobility and transport in an electric field, and the mechanism of deposition. Depending on the carrier liquid (aqueous or nonaqueous), different mechanisms of charging have been proposed. Basically, however, in both liquid systems there exists an electrical double layer surrounding each suspended particle. Upon application of an electric field, the force acting on the particle and on the inner portion of the double layer causes it to move in one direction, while the oppositely charged outer portion of the double layer moves in the opposite direction. Thus, a shear surface exists which separates the double layer. The charges in the double layer give rise to an electrical potential, the value of which at the shear surface is commonly called the zeta potential. Among other properties, the zeta potential affects the stability of dispersions and the electrophoretic mobility. For general discussions, one may consult various publications [7,27-30].

In water, many particle dispersions achieve a charge spontaneously, and the size and magnitude of the charge (or zeta potential) depend strongly on the pH. In organic liquids, especially in insulating liquids such as hydrocarbons, it is necessary to add a surfactant or charging agent to achieve high zeta potential; this is due to the low dissociation power of the nonpolar liquids. As will be described later, various organic liquids and charging agents have been found which can be used to deposit decorating powders on silicon wafers.

In addition to the particle charging and mobility effects, attention must be paid to the deposition process. We have found that with low conductivity liquids it is relatively easy to form an adhering deposit with properly charged particles. Once the particle is moved to the surface, an image charge on the surface acts to hold the particle in place. With conducting liquids, however, this image force is short-circuited and adhesion is not good unless certain resins are added. This is a particular problem with water or with large particle sizes. With smaller particle sizes ($\lesssim 1 \mu\text{m}$), there are ample short-range surface forces available because of the larger surface-to-volume ratio. For

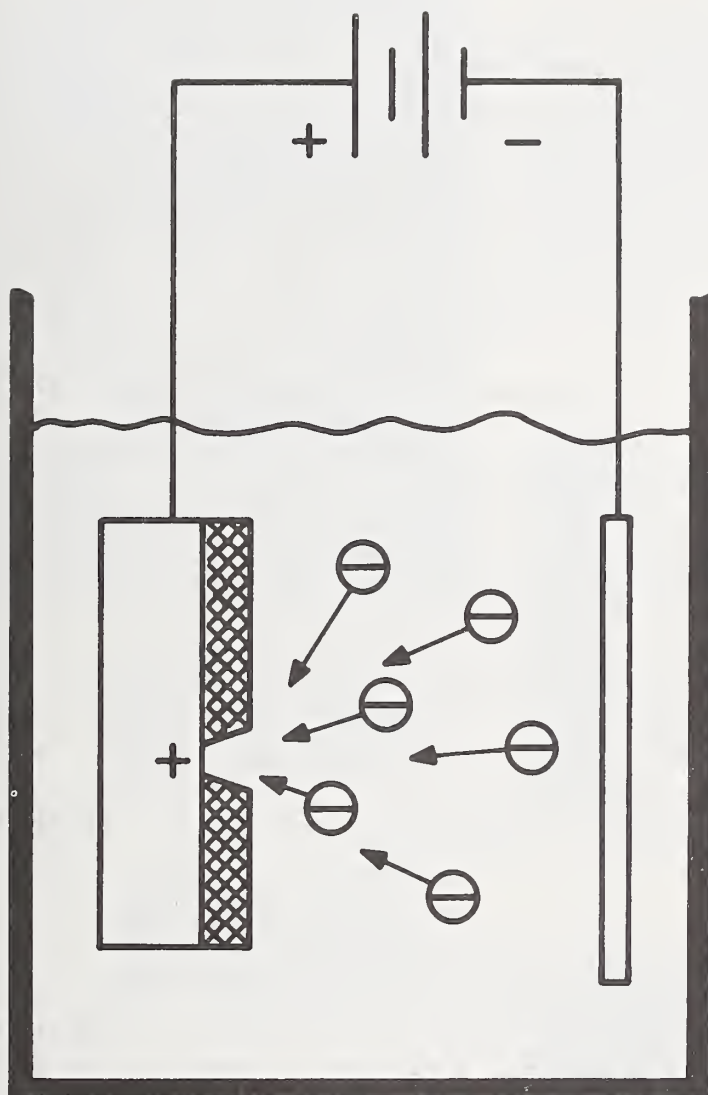


Figure 19. Schematic of electrophoretic decoration apparatus.

these reasons, we prefer the use of small particles and organic liquids. In addition to the advantages stated, the use of organic liquids limits the possibility of damage to the wafer or device being decorated. This is due to the current-limiting properties and to the smaller possibility of electrode reactions or impurity dissolution. Also, most organic liquids which were used dry much faster than water.

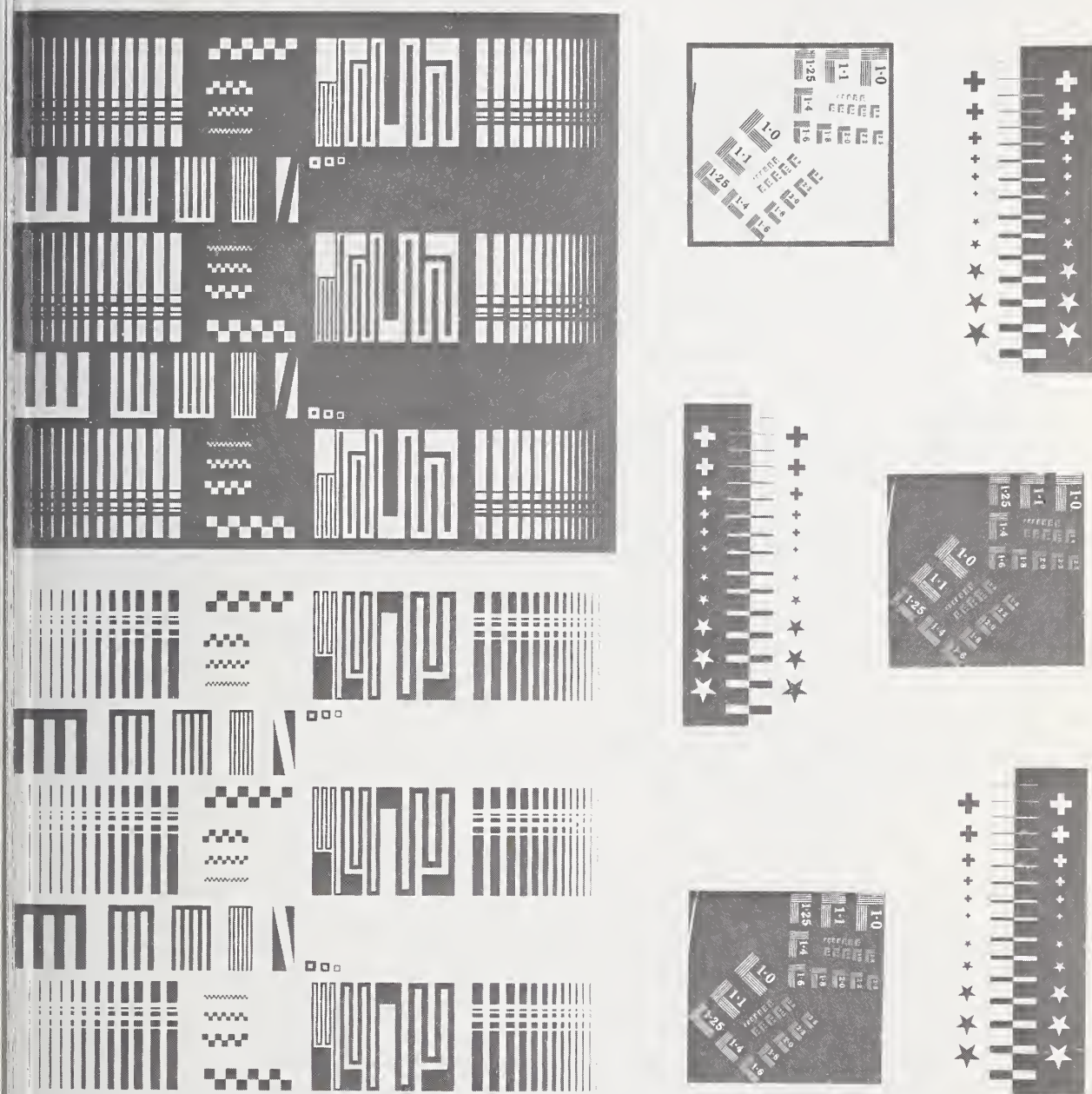
An important advantage of insulating liquids for this application is that the nondestructive decoration of partial pinholes (oxide regions thinner than the surrounding area) may be achieved. With conducting liquids this is possible only by applying voltage high enough to break down the thin oxide region. With an insulating liquid, however, the particles will deposit on the insulator, charging it as a capacitor. The capacitor will charge to the applied potential, and the area density of particles on the surface will be inversely proportional to the oxide thickness. Thus, partial pinholes (thinner oxide) will have a greater particle density than the surrounding areas.

4.3.2 Equipment and Materials

For the conventional electrophoresis, a stainless-steel tank (10 cm x 3.5 cm x 9 cm deep) was used, which can accommodate 5-cm-diameter wafers. It acts as one electrode in the system and rests in an acrylic holder for operator safety. The acrylic holder also incorporates a small motor to stir the electrophoretic suspension with a magnetic bar. In some tests, a single stainless-steel electrode (9 cm x 9 cm) was used in a glass beaker. In both cases, the sample was held in a tweezer clip attached to a vertically sliding bar for insertion of the sample into and removal from the liquid. The clip also acted as the electrical contact to the sample. Voltages were obtained from a well-regulated power supply capable of providing ± 1200 V. For operator safety, currents were limited to 10 mA. Current during particle deposition, measured with a sensitive electrometer (1×10^{-14} A), was recorded on a strip chart.

The samples used in the tests included IC wafers, bare silicon wafers, thermally oxidized wafers (patterned and unpatterned), wafers with deposited oxides, and metal foils or plates. For wafer samples covered with insulators, provisions were made for electrical contact. Usually, samples were cleaned by rinsing in distilled water followed by acetone and $C_2Cl_3F_3$ (1,1,2 - trichloro - 1,2,2 - trifluoroethane) rinses.

A positive/negative test pattern was selected which features lines, squares, rectangles, triangles, crosses, stars, dots, and serpentine lines of a large variety of sizes (figure 20). Photolithographic masks were generated by step-and-repeat processing of this pattern. This mask was utilized for fabricating high-precision patterns in oxide layers to measure the resolution capability of decoration techniques.



The microscopes have already been noted in section 4.1.2 on aluminum etching. Several uv sources were tested for the uv phosphors. The most useful were pairs of pencil-type, short- and long-wave lamps mounted just above the stage of the microscope. This places the source in immediate proximity to the sample, furnishing the maximum uv flux to the sample surface.

Various particulate materials for decoration were evaluated. Criteria to be met for selection were as follows: (1) dielectrics of well-defined chemical composition (no mixtures); (2) insolubility in vehicular suspending liquids used in electrophoresis or corona-charging decoration; (3) materials exhibiting intense luminescence in uv light or good white on black contrast in metallurgical microscopy; (4) availability in powder form of suitable particle size; (5) nontoxicity; and (6) preferably, low cost.

An important class of materials are the uv luminescing agents. Twelve TV phosphors, lamp phosphors, and fluorescing compounds were tested and rated on the basis of their uv fluorescence intensity, fluorescence color, and sensitivity to visual detection under the microscope. Based on these criteria, these materials were classified in order of preference as shown in table 5 (the first six being especially preferred candidates):

TABLE 5. UV-LUMINESCING POWDER MATERIALS (CLASSIFIED IN ORDER OF PREFERENCE FOR ELECTROPHORETIC DEFECT DECORATION).

<u>No.</u>	<u>Material</u>	<u>Short Wavelength UV Fluorescence Color</u>
A	Zinc silicate: Mn ¹	Yellow
B	Zinc silicate: Mn ²	Yellow
2	Zinc silicate: Mn ³	Green
D	Cerium, terbium, magnesium- aluminate: Tb	Light Yellow
7	Yttrium vanadate: Eu	Red
C	Magnesium, aluminum-gallate: Mn	Pale Green
F	Barium, magnesium - aluminate: Mn	Pale Green ⁴
1,5	Zinc, cadmium-sulfide: Cu: Al	Yellow ⁴
4	Yttrium oxide: Eu	Red
3	Zinc sulfide: Ag: Cl	Blue
E	Magnesium-gallate: Mn	Pale Green
6	Uranyl ion silicate glass	Pale Yellow

¹Large particle size; lamp phosphor.

²Small particle size; lamp phosphor.

³TV phosphor with very good contrast.

⁴Long wavelength exhibits greater intensity.

In addition to the phosphors, various types of white powders including powdered glasses (such as lead borosilicates, zinc aluminosilicates, lead boro-aluminosilicates), metal oxides (such as zinc oxide and titanium dioxide), and carbon blacks were evaluated. Liquid vehicles included isopropyl alcohol, Isopar G (a narrow cut, high-purity hydrocarbon, Exxon), and $C_2Cl_3F_3$.

Various materials used to provide net electrical charge on the decorating particles in the liquid vehicle include: zirconium octoate, zinc octoate, petroleum magnesium sulfonate, petroleum barium sulfonate, OLOA 1200 (Chevron), anhydrous ammonia, petroleum ammonium sulfonate, Lubrizol 894 (Lubrizol Corp.), and A-C Copolymer 430 (Allied Chemical). The most useful materials have been OLOA 1200, Lubrizol 894, and A-C Copolymer 430. The first two are low-ash, heavy-duty motor oil dispersants. These are chosen for their excellent particle charging ability and absence of metal content. The A-C Copolymer 430 is an ethylene copolymer with about 28% vinyl acetate.

4.3.3 Test Procedure

As shown in figure 19, the sample is spaced about 1.2 cm from the opposite electrode. After immersing the wafer, a constant voltage of 5 to ~300 V is applied for times varying from 2 to ~200 s. The voltages and times used depend on the particle density in the liquid, the particle mobility, and the degree of decoration desired. It has been found that with certain particle dispersions, it is advantageous to remove the wafer from the liquid with the voltage applied in order to avoid lateral motion of the deposit. The decorated device wafer is allowed to dry in air at room temperature and can then be examined under a microscope.

When metal foils are used for correlating charge transport with deposited particle weight, the foil is placed in the center of the stainless-steel tank. Thus, the spacing to the electrode (the tank body) is 1.7 cm on each side.

4.3.4 Selection of Best Materials

Preliminary tests were made to select the best candidate materials from the wide variety of powders, liquid vehicles, and charging agents available. The criteria in these initial screening tests were deposition, adhesion, selectiveness, and ease of observation. Based on these tests, the best powders for the conventional cell electrophoresis were found to be a lead aluminosilicate glass powder and the small-particle zinc silicate: Mn (phosphor B) with intense yellow fluorescence as noted in table 4.

The lead aluminosilicate glass has the composition 50% PbO , 10.1% Al_2O_3 , and 39.9% SiO_2 by weight. The glass powder has about 75% by weight of particles below 12 μm in size, and about 25% below 3 μm in size. Best suspensions were obtained with $C_2Cl_3F_3$ as the vehicle. The

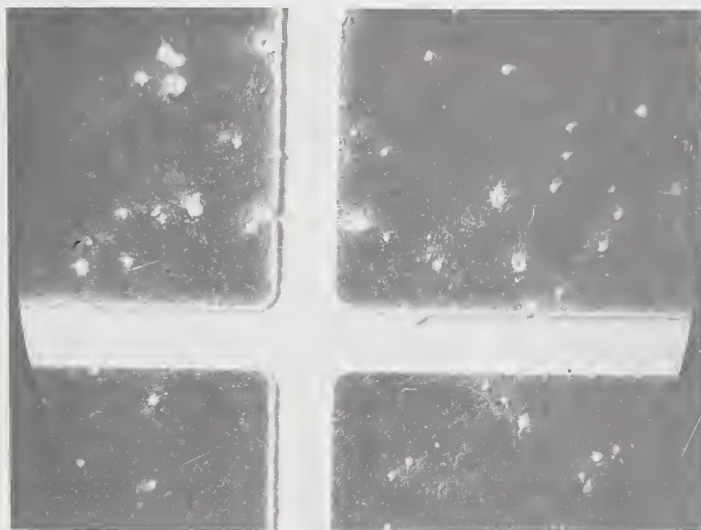
charging agent was either petroleum barium sulfonate or OLOA 1200. Typical suspensions consisted of 20 g of the glass in 400-ml $C_2Cl_3F_3$ with 2-ml petroleum barium sulfonate or 0.4 g of OLOA 1200. The glass particle charge is negative for both charging agents. In both cases, the charging agent is first added to the liquid and then the glass is added, followed by two minutes of shaking. Because of the relatively large particle size of this glass, these dispersions are suitable for decoration of large defects, as are sometimes found in the oxide layers of mesa-type power devices. Such large defects, deliberately induced in thermal oxide by excessively long etching, were decorated with the above glass suspension. The result is shown in figure 21 for two deposition voltages and times, and the defects are clearly visible in both cases. However, in the 200 V condition, it is evident that a general deposition over the entire oxide has occurred. To some extent, this occurs at all voltages and is a consequence of the insulating nature of the liquid vehicle ($\sim 10^{13} \Omega\text{-cm}$). Another example of the background deposition is shown in figure 22 for 0.3- μm zinc oxide powder deposited on 1- μm thermal silicon dioxide from a $C_2Cl_3F_3$ suspension with OLOA 1200 as the charging agent. There is heavy deposition at the pinholes, but a low-density background deposit is also evident. Two criteria for selection, adhesion and nondestructiveness of the process, are satisfied by the use of insulating liquids. However, background deposition does take place, and the reason for this is described in detail later.

The phosphor suspension consisted of 1 g of phosphor in 400-ml $C_2Cl_3F_3$. One ml of a stock solution of OLOA 1200 was used as the charging agent. The stock solution of OLOA 1200 consists of 8 ml of a 100-g OLOA 1200/100-ml $C_2Cl_3F_3$ solution added to 392 ml of $C_2Cl_3F_3$. The voltages used were 10 to 500 V for times ranging from 30 s to 5 min. Again, there was a general background deposition over the insulator, in addition to the defect decoration, and the background deposit increased with voltage. A typical example is shown in figure 23 where a line defect is heavily decorated. Many of the phosphor particles in the surrounding area are not associated with defects, but represent capacitive charging of the insulator. The best results are obtained at low voltages such as 25 V, which minimizes background deposition.

Using a wafer patterned with the special test mask (figure 20), we were able to decorate pinholes as small as 1 μm in diameter with the phosphor. These were the smallest pinholes available in the test pattern used. With the glass powder, pinholes could only be decorated if their diameters were greater than about 2 μm , presumably due to the greater particle size.

4.3.5 Investigation of Deposition Mechanism

As discussed previously, the problem of adhesion and the possibility of destructive dielectric or junction breakdown with conducting liquids favors the use of insulating liquids. With these, however, unwanted deposition occurs on insulator areas which lowers the contrast ratio of decorated defects to background. In order to understand this background deposition and reduce it to a minimum, measurements



(a)



(b)

Figure 21. Micrograph of glass particles deposited on mesa-type wafer. The thermal oxide is $1.2 \mu\text{m}$ thick, and the groove width is 0.4 mm . (a) Deposition at 50 V for 8 min. (b) Deposition at 200 V for 2 min (20X).

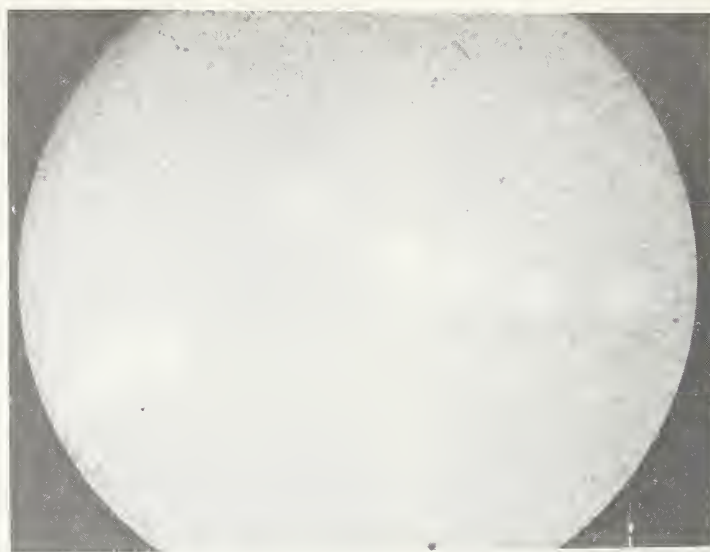


Figure 22. Zinc oxide powder deposited by electrophoresis on thermal silicon dioxide showing pinhole decoration and background deposition. The deposition was done at 10 V for 30 s. The deposits decorating the pinholes are about 10 μm in diameter (400X).

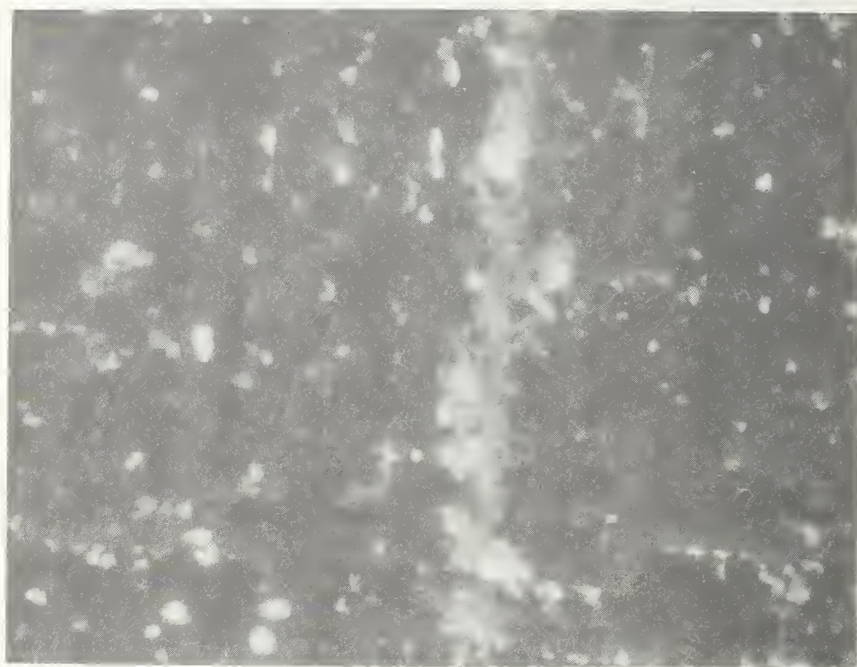


Figure 23. Micrograph of zinc silicate phosphor deposited on defect on IC wafer. Deposition was done at 25 V for 10 min (100X, brightfield).

of current and charge transported were correlated with sample capacitance and the weight of decorating powder deposited on unpatterned silicon wafers.

The current was measured during voltage application between the tank electrode and a silicon wafer. The time dependence of this current is determined by the wafer being bare silicon or covered with an insulator such as thermal silicon dioxide or CVD glass. This effect is shown in figure 24, where current vs time is plotted for three cases for lead aluminosilicate glass in $C_2Cl_3F_3$ with petroleum barium sulfonate as the charging agent. Deposition on bare silicon results in a decaying current. Note that the decay is less steep after allowing the glass particles to settle out, indicating that at least part of the decay is due to the build-up of an insulating layer of glass powder. The initial current is lower after the glass particles have settled, demonstrating that a measurable fraction of the current is carried by the glass particles. When the glass is deposited on a silicon dioxide-coated wafer, the current decays very rapidly. This is presumably due to capacitive charging of the silicon dioxide by the glass particles and other current carriers deposited on the silicon dioxide.

To confirm this capacitor-charging effect, measurements of total charge transported during glass deposition on silicon dioxide-coated wafers were correlated with the calculated capacitance. As shown in figure 25, the agreement is good; and the linear dependence on voltage is a further confirmation. In the figure, the upper line is for 1.5×10^{-4} cm silicon dioxide, and the lower line is for 2.0×10^{-4} cm silicon dioxide.

As shown in figure 24, only a fraction of the current is carried by the glass particles. Other unknown ions or charge carriers transport the bulk of the current, as established by the current measurement after the glass is allowed to settle. Thus, it is possible to increase the density of these other charge carriers so that relatively more of the capacitor charging on the insulating regions is done by the nonvisible charged particles rather than by the glass particles. This will reduce glass or phosphor deposition on the "good" insulating region, and increase the contrast of the glass or phosphor deposited at defects. The addition of these charge carriers can be done conveniently by introducing small amounts of acetone, another polar solvent, or a charging agent to the $C_2Cl_3F_3$ to increase conductivity and decrease the glass or phosphor deposition on the insulating regions. Figure 26 shows the result of addition of petroleum barium sulfonate to a decorating suspension of lead aluminosilicate glass in $C_2Cl_3F_3$. In this experiment the weight of glass deposited at 1000 V in 1 min on silicon dioxide-coated wafers was determined as a function of charging agent concentration. There is a decrease of about a factor of five in glass weight for a fourfold increase in concentration of charging agent. Thus, improvements in contrast can be made. Over the concentration range in figure 26 the glass deposited on bare silicon decreases only about 10%, so that a true contrast improvement is obtained. Additions of still more surfactant will result in too high a conductivity, and adhesion problems

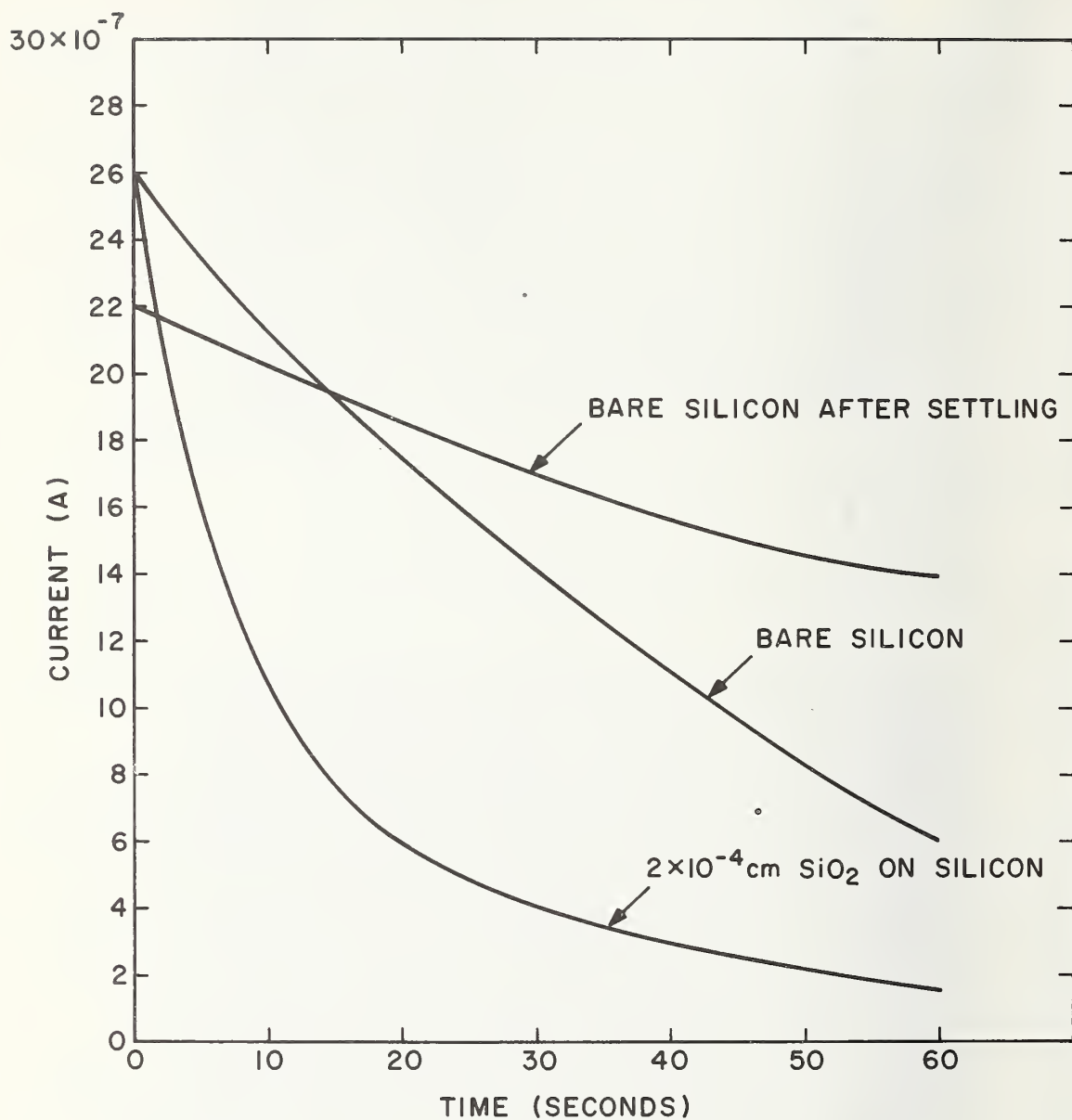


Figure 24. Plot of current vs time for bare silicon wafer and silicon dioxide-coated wafer, for a suspension of lead alumino-silicate glass particles with petroleum barium sulfonate in $\text{C}_2\text{Cl}_3\text{F}_3$. Also shown is the time dependence for bare silicon after the glass has settled out.

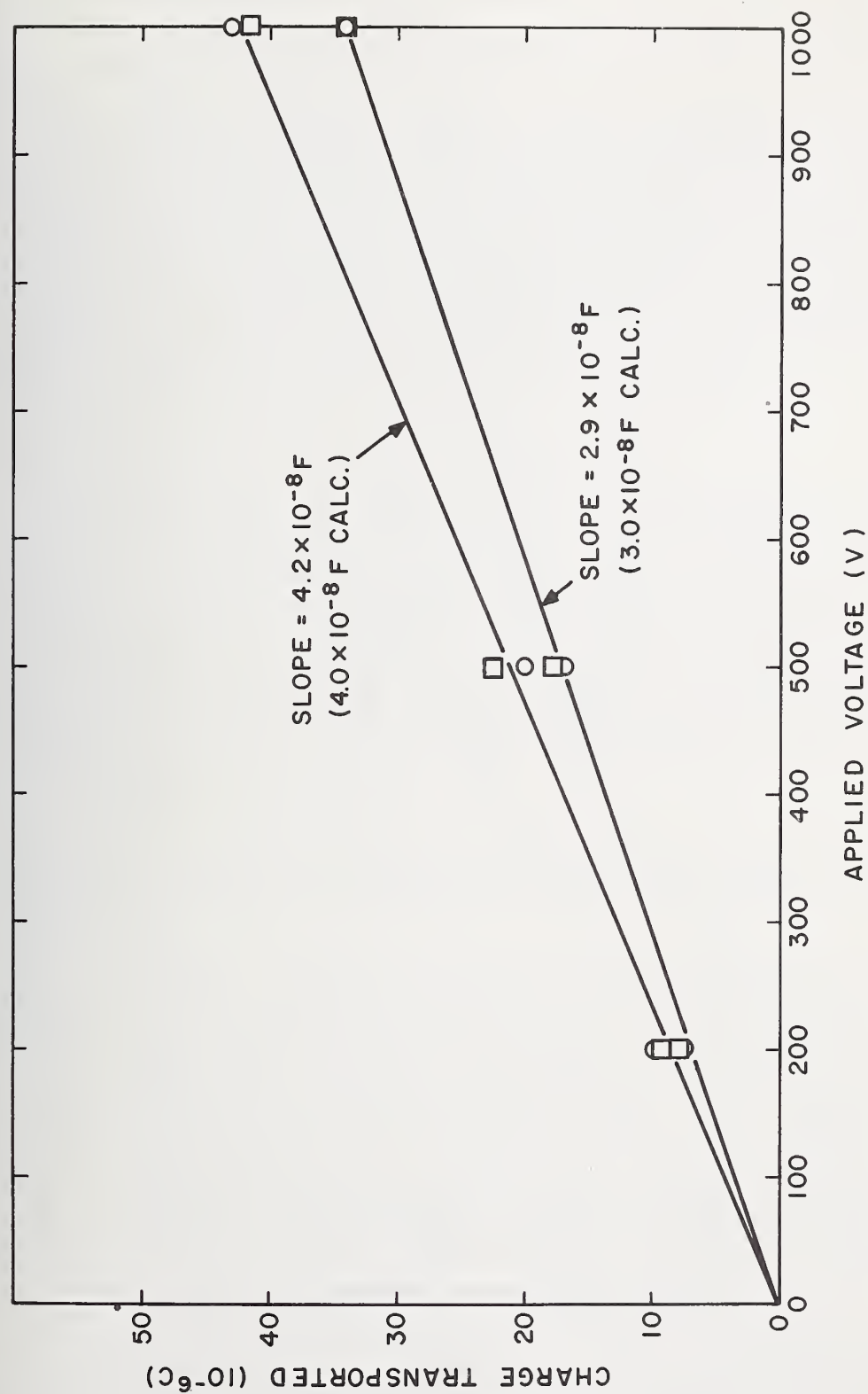


Figure 25. Plot of charge transported vs applied voltage for silicon dioxide-coated wafer. The suspension is the same as for figure 24. Sulfonate content was 0.1% to C2Cl3F3 by volume for the \odot points and 0.2% for the \square points.

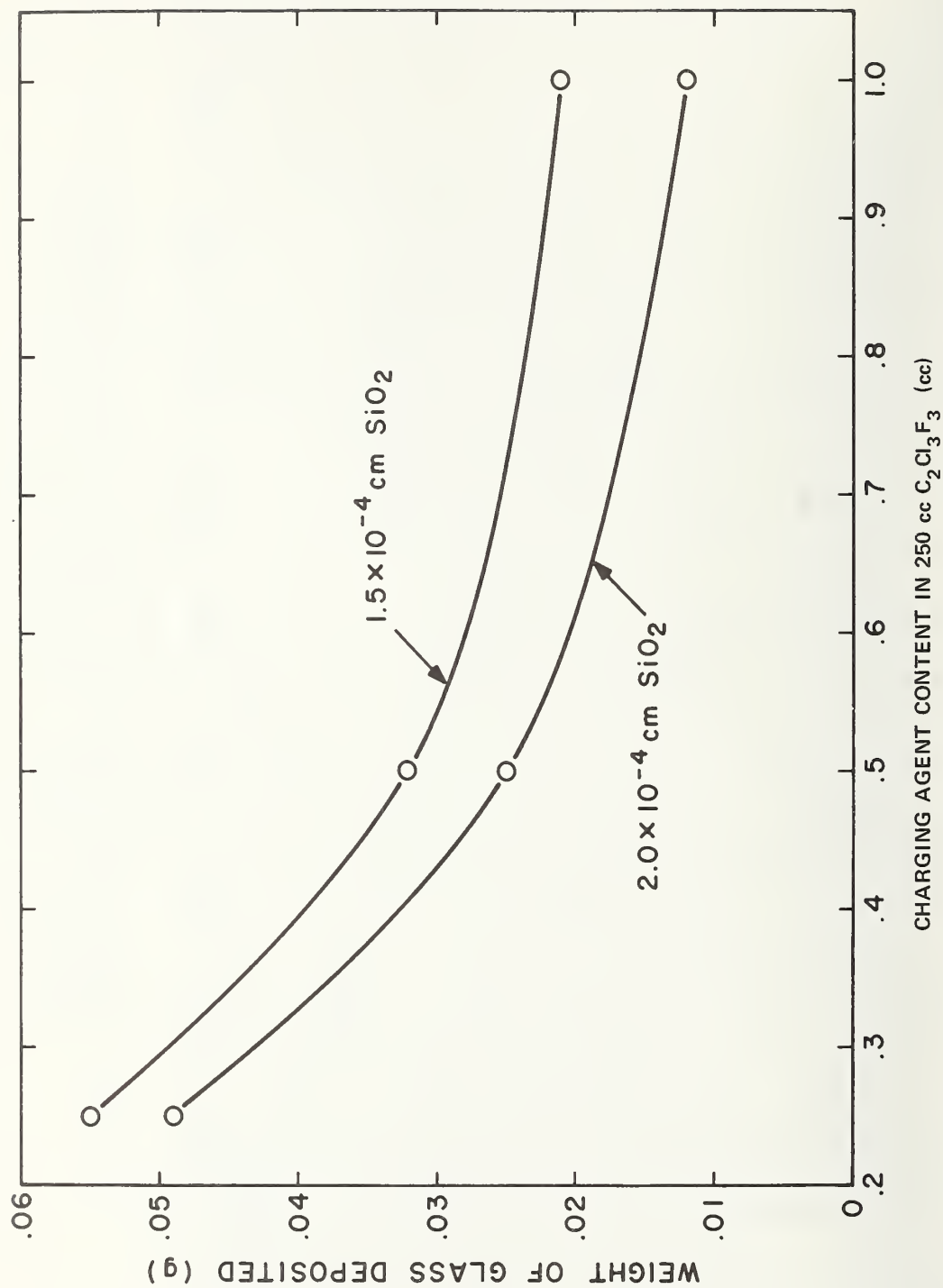


Figure 26. Plot of glass deposited on silicon dioxide-coated wafers as function of concentration of petroleum barium sulfonate.

develop. The addition of acetone results in qualitatively the same behavior.

4.3.6 Summary

It has been possible to obtain useful decoration of defects in insulating passivation layers on device wafers by deposition of particles such as glass or phosphor (zinc silicate) from insulating liquids by a conventional cell electrophoretic technique. The use of conducting liquids involves adhesion problems with the decorating particles, and the possibility of destructive breakdown because of the low impedance of the system. The contrast ratio of the process can be optimized by the addition of conductivity-increasing agents. At best, however, the defect detectability, ease of observation, and contrast ratio are inferior to the methods described in the next section.

4.4 Decoration by Electrostatic Charging

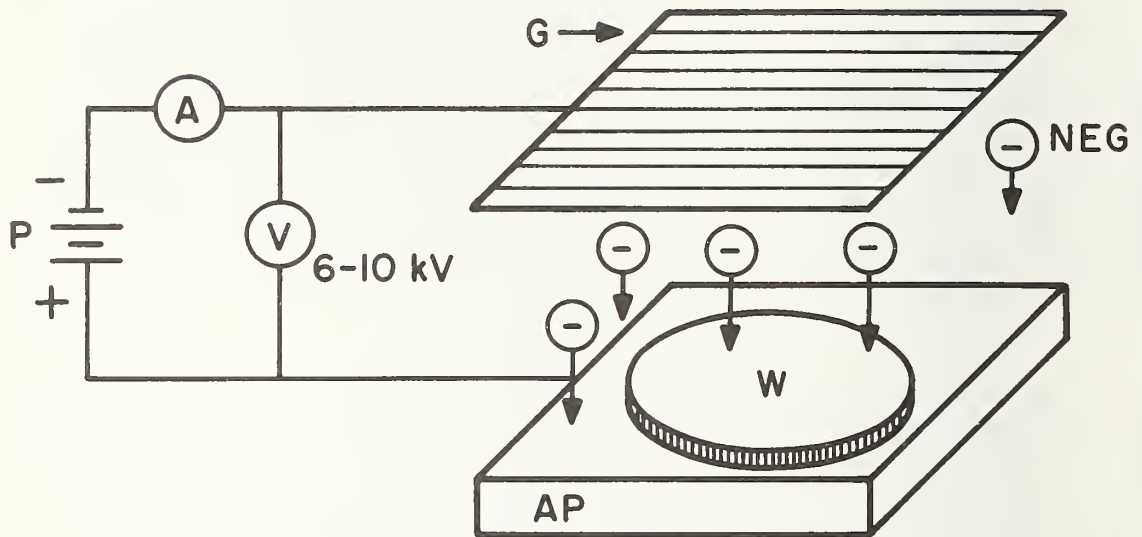
In this section the decoration method of electrostatic charging of the sample followed by immersion in an insulating liquid containing charged decorating particles is described. Basic principles of the processes have been discussed [7]. In the first step, ions from an atmospheric pressure glow discharge (corona) are deposited on the insulating regions of the sample. Then the sample is immersed in a suspension of charged particles. Depending on the relative signs of the charged particles and the deposited surface ions, the charged particles are attracted to the charged insulating regions, resulting in reverse decoration, or to the defects, resulting in direct decoration.

4.4.1 Corona-Charging Process

The first step for either direct or reverse decoration is the deposition of ions on the insulating regions of the sample as shown in figure 27.

4.4.1.1 *Equipment* - The source of ions deposited on the sample is a plane array of 40- μ m-diameter nickel alloy wires. This wire grid consists of seven parallel wires 1.8 cm apart, held in an acrylic frame in a horizontal plane. The wires are commonly connected to a high-voltage dc power supply capable of $\pm 10,000$ V and 6 mA. It is recommended that only rf-type dc power supplies with current limitation of no more than 10 mA be used for operator safety. A grounded plate is placed 3 cm above the wires to provide greater current uniformity and to protect the wires from mechanical damage. The sample is placed on a grounded plate about 2 cm below the wire array. The power supply is operated from a foot switch. The process is carried out at relative humidity below 30% in a glove box in flowing nitrogen.

4.4.1.2 *Parameter Study of Charging* - In order to understand the surface charge deposition process on device wafers, measurements of surface voltage of charged wafers were done as functions of sample geometry, passivating layer thickness, corona voltage, relative



P = power supply,
 A = ammeter,
 V = voltmeter,
 G = corona grid wire array,
 NEG = negative ions,
 W = sample wafer,
 AP = anode plate

Figure 27. Schematic of corona charging process.

humidity, and corona wire-to-sample spacing. For these tests, IC wafers were not used because we wanted results to be independent of metallization patterns and bonding pad arrangements. To simulate an IC wafer, a square grid pattern was etched into thermal silicon dioxide on silicon, yielding a pattern of square islands of silicon dioxide surrounded by grid lines of bare silicon. Several islands of different sizes and grid line widths were used.

Charging properties of wafers are studied by measuring the surface potential of the charged wafers. This is done with an electrostatic voltmeter that uses a noncontacting probe with feedback to make absolute (independent of spacing) voltage measurements. The probe-to-wafer spacing is adjusted so that the geometry of the ground potential (bare silicon grid lines) and charged silicon dioxide islands is not resolved, to avoid lateral positioning errors. In this case, the probe detects an area average of the surface potential. In the following discussion, the voltage values have been corrected to take into account the area ratios of charged insulator and ground potential silicon. Thus, the voltage is that of the surface oxide of the square islands. All measurements were done in nitrogen ambient at a relative humidity (RH) of about 25%.

The oxide surface voltage reaches a steady-state value within about 5 s, when the corona charge is set just below sparking voltage. For lower voltages, the time to steady state is greater. In the actual process used for decoration, the surface voltage reaches steady state in about 10 s. The standard charging time used in the decoration process is set at 18 s.

The magnitude of the oxide surface voltage at steady state depends mainly on the grid line geometry and is greater for higher ratios of oxide area to bare silicon area for a square geometry. This is shown in figure 28 where the oxide surface voltage, corrected for the area measurement effect, is plotted vs the area of the oxide covered surface. There is little dependence on oxide thickness. This is shown in figure 29 for three oxide thicknesses of the same square geometry.

The observations indicate that the charging of a surface containing closely spaced insulator and conductor regions is limited mainly by the conducting areas. As the ions collect on the insulator they generate an electric field in the gas ambient which causes subsequent ions to move toward the ground potential regions before arriving at the wafer surface. Thus, for the geometries of interest, the oxide surface voltage is not determined by the oxide breakdown potential (except for very thin oxides or very large insulator areas).

Further support for the above is gained from the dependence of oxide steady-state voltage on corona voltage, shown in figure 30, and on corona wire-to-sample spacing, shown in figure 31. Based on the geometry-limited model of charging, the decrease in voltage for decreasing corona voltage or increasing spacing is related to deflection of incident ions from the charged oxide.

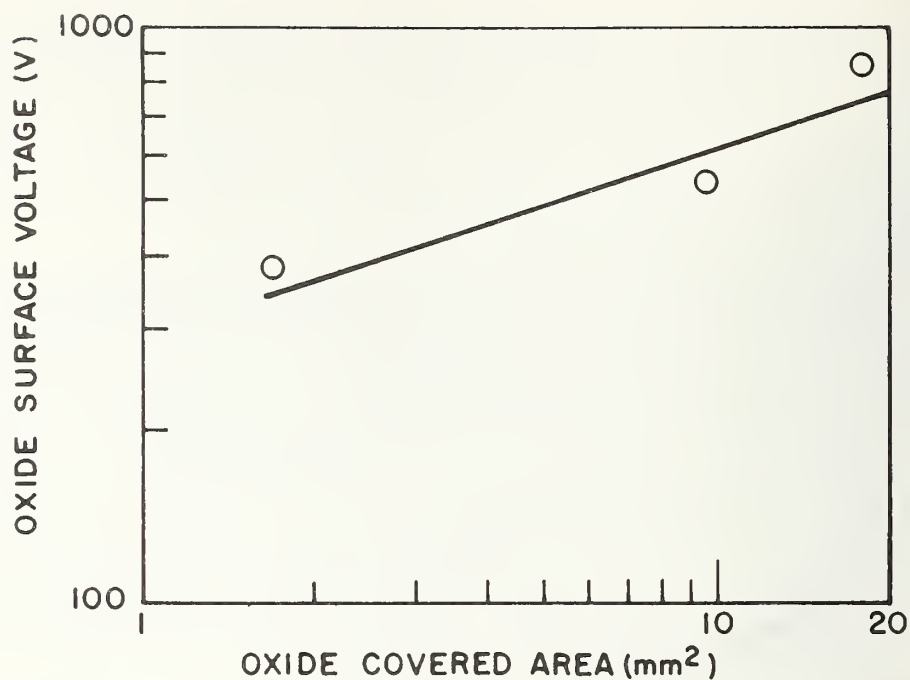


Figure 28. Oxide surface voltage charged to saturation vs area of oxide-covered surface. Oxide thickness is 10,000 Å.

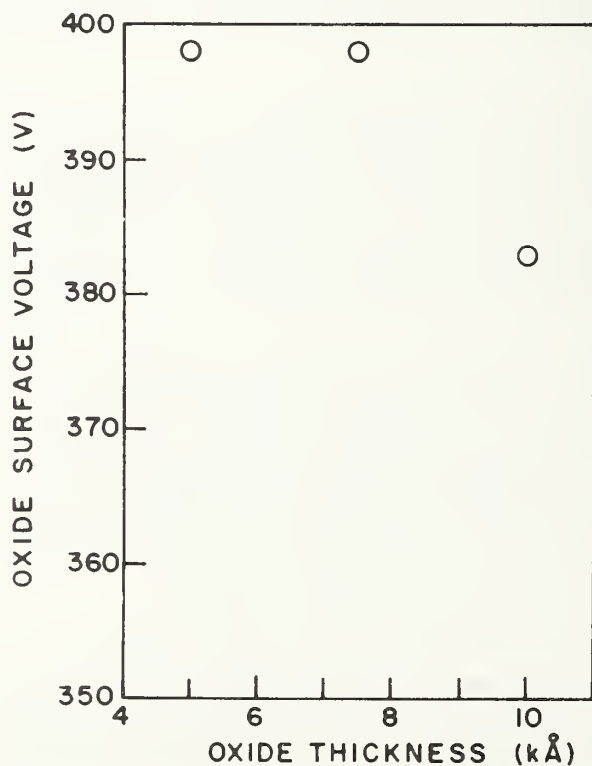


Figure 29. Oxide surface voltage charged to saturation vs oxide thickness for oxide-covered area of 1.7 mm².

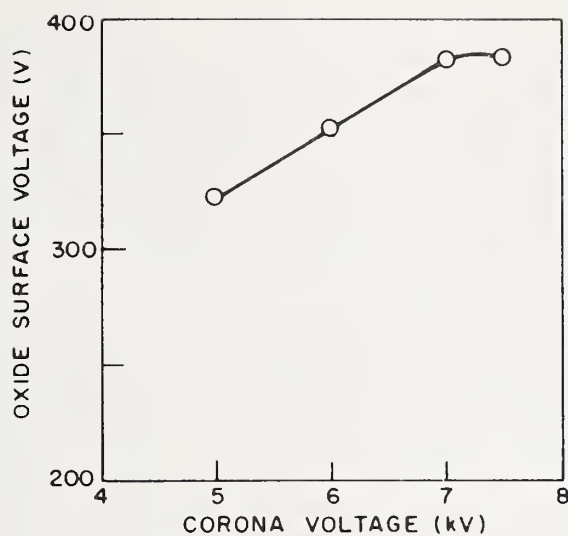


Figure 30. Oxide surface voltage charged to saturation vs voltage of corona wires for oxide $10,000 \text{ \AA}$ thick and area of 1.7 mm^2 .

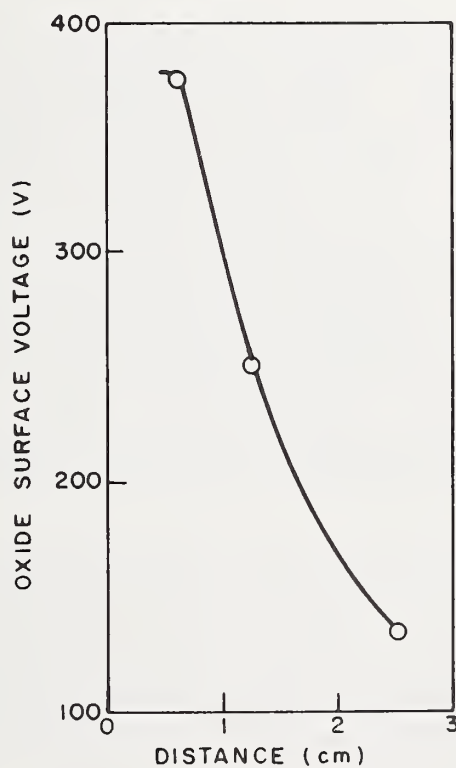


Figure 31. Oxide surface voltage charged to saturation vs distance from wafer to corona wires at 10 kV for oxide $10,000 \text{ \AA}$ thick and area of 1.7 mm^2 .

The ambient relative humidity must be controlled to prevent lateral current flow on the oxide surface. The oxide surface voltage decay rate after charging increases greatly above 30% RH for thermal silicon dioxide, CVD silicon dioxide, and CVD PSG, as shown in figure 32. The surface voltage will also decay rapidly if the bulk conductivity of the oxide is high due to the presence of moisture. Thus, it is best to remove adsorbed or absorbed water before charging by heating at 200°C for 5 min in air. This has been made the first step in the standard process to ensure retention of surface charge on the sample.

4.4.1.3 *Discussion* - The fact that the surface voltage of the sample insulator regions depends on the geometry of insulator and conductor regions is very important for the process implementation. Since the surface voltage depends on this geometry, it does not depend on the insulator thickness, except for very thin insulators not used for passivation. Thus, the surface voltage is not set by insulator dielectric breakdown (except at latent or partial defects, as will be described later). If the surface voltage were set by dielectric breakdown, then the insulator regions over metal would have a lower voltage than those over the primary silicon oxide. In this case, a decoration conforming to the metal interconnects would result after charging and decoration. This is not normally desired for defect detection.

In the above discussion, we have assumed that the sample is a chip or a wafer with the passivating layer etched open at the contact pads or at the grid lines. These etched-open regions furnish the closely spaced geometry of insulator-conductor required so that the surface voltage does not depend on whether the passivating layer is over metal or over insulator. It is also possible to decorate wafers with a uniform insulator (before the passivation layer is etched open). This can be done if a grounded conducting grid is placed over the wafer during the charging. A convenient grid consists of an aluminum sheet (0.8 mm thick) with 3.5-mm-diameter holes on 5.0-mm centers. This grid, placed over the wafer, furnishes the closely spaced insulator - conductor geometry required for the proper charging. When the grid is used, charge is deposited only at openings in the grid. The entire sample can be charged if the grid is moved laterally over the sample during the charging, while in close proximity to the sample (~0.3-mm spacing).

An important consequence of the charging properties is that the surface charge and potential around a defect decrease laterally as the defect is approached due to ion deflection during charging and to surface conduction. Thus, there is a margin around a crack or pinhole of lower surface potential than the potential in nondefect areas. This effect increases detectability since it magnifies the defects as far as charged particle deposition is concerned. The margin is of the order of 25 μm in lateral dimension.

For the process implementation it is necessary that the surface charge remain on the passivating layer for a time equal to the delay between charging and deposition, plus the deposition time. This total time is about 20 s and it is required that the dielectric relaxation

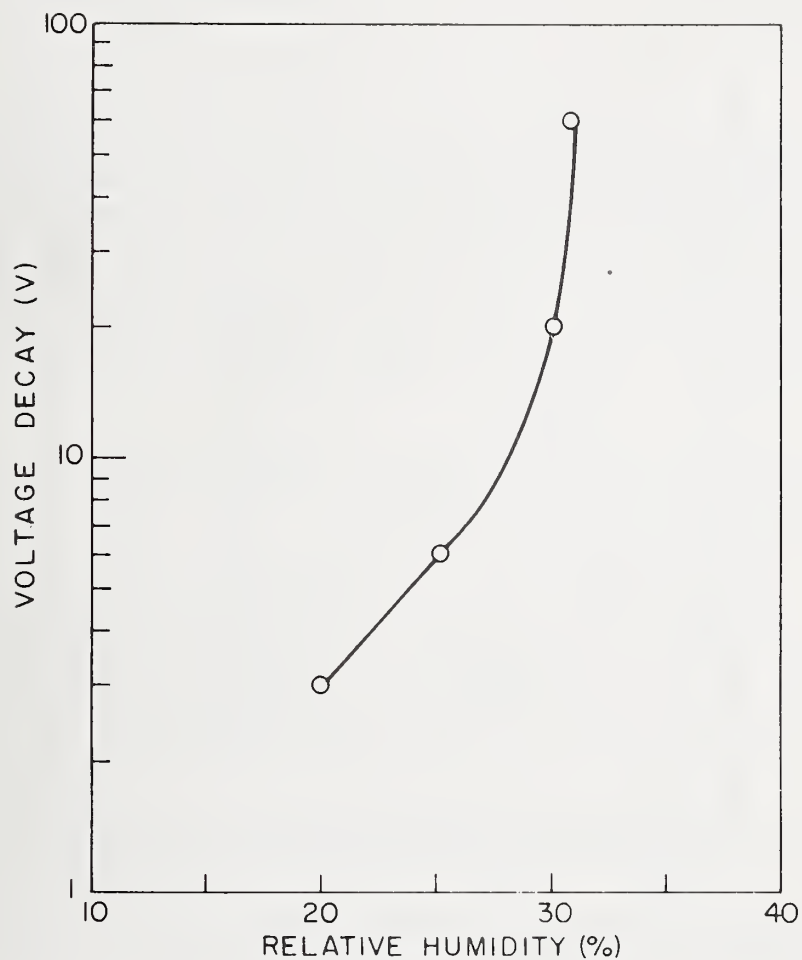


Figure 32. Oxide surface voltage decay in first minute after charging vs relative humidity.

time of the passivation layer be about 20 s or greater. Thus, a bulk resistivity of about $10^{13} \Omega\text{-cm}$ or greater (at room temperature) is needed. By cooling the sample during charging, and by the use of cooled particle suspensions, it is possible to decorate defects on layers of lower resistivity.

4.4.2 Direct Decoration of Defects by Corona Charging

The sign of the corona discharge is chosen to be the same as that of the particles suspended in the insulating liquid. Thus, upon immersion of the sample, the particles are repelled from the charged insulator regions and directed to the conducting, uncharged regions such as cracks and pinholes (and including etched-open bond pads and grid lines). Also, particles are directed to regions of substantially lower surface voltage, as found at partial pinholes. The latter effect will be discussed later. A schematic of the deposition process for direct decoration is shown in figure 33.

4.4.2.1 Particle Suspensions - Several particle suspensions were used successfully in direct decoration tests. These included zinc oxide ($0.3 \mu\text{m}$), lead aluminosilicate glass (2 to $8 \mu\text{m}$), and the zinc silicate phosphor (manganese-doped, $1 \mu\text{m}$) used for the electrophoretic cell decoration discussed previously. In all cases, the charging agent was OLOA 1200 in $\text{C}_2\text{Cl}_3\text{F}_3$, made up into a stock solution as described in section 4.3.4. The charged particle suspensions were made by adding the following to 400 ml of $\text{C}_2\text{Cl}_3\text{F}_3$: 1-g zinc oxide or silicate and 1-ml stock solution; and 4-g lead aluminosilicate glass and 4-ml stock solution. The particles are charged negatively in these three cases. These choices represent the three materials giving the best results in direct decoration of about ten which were tested. The criteria were selectivity, amount of deposit, adhesion, and contrast available in microscopic observation. Of the three, the phosphor was the best, primarily because of the enhanced ease of observation under uv illumination. The remaining discussion of direct decoration will concentrate on the zinc silicate (manganese) phosphor B.

4.4.2.2 Procedure - The best procedure for pinhole or microcrack decoration by the phosphor is to charge the wafer for 18 s at 7000 V dc at a wafer-to-wire spacing of 2 cm. The sample is then immersed in the suspension for 5 s. At higher voltages, very heavy phosphor deposits are formed at large defects, which are sometimes disturbed by the liquid, and a scatter deposit over the sample not correlated with defects is obtained. A small fraction (~5%) of the smaller pinholes is missed at 7000 V dc, but a clean deposition with little scatter is obtained. Examples of pinhole and crack decoration and correlation with etching are shown in figures 34, 35, and 36. Figure 35 shows an example of a pinhole not detected by the phosphor that was found by aluminum etching. In general, the correlation between phosphor decoration and etching is very good.

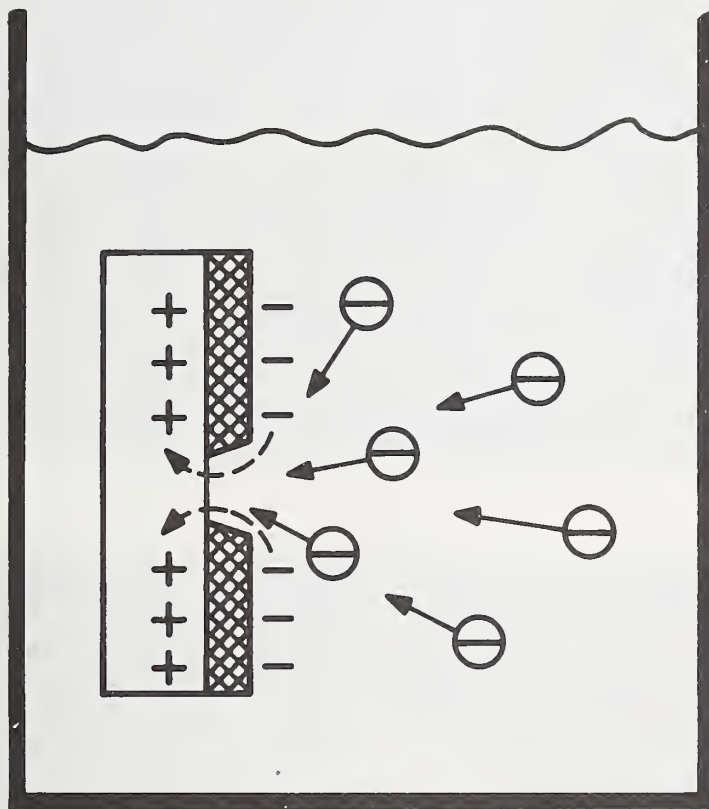
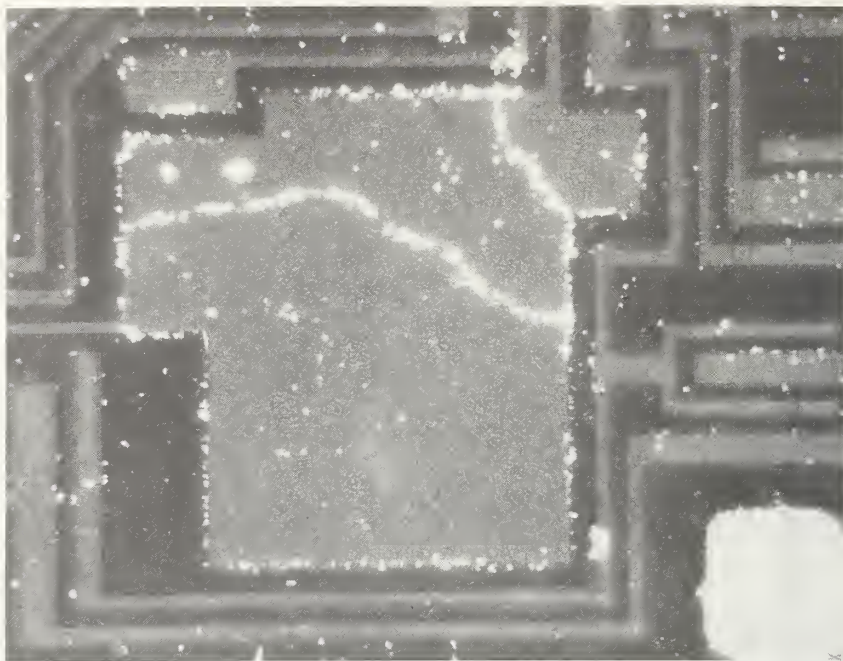
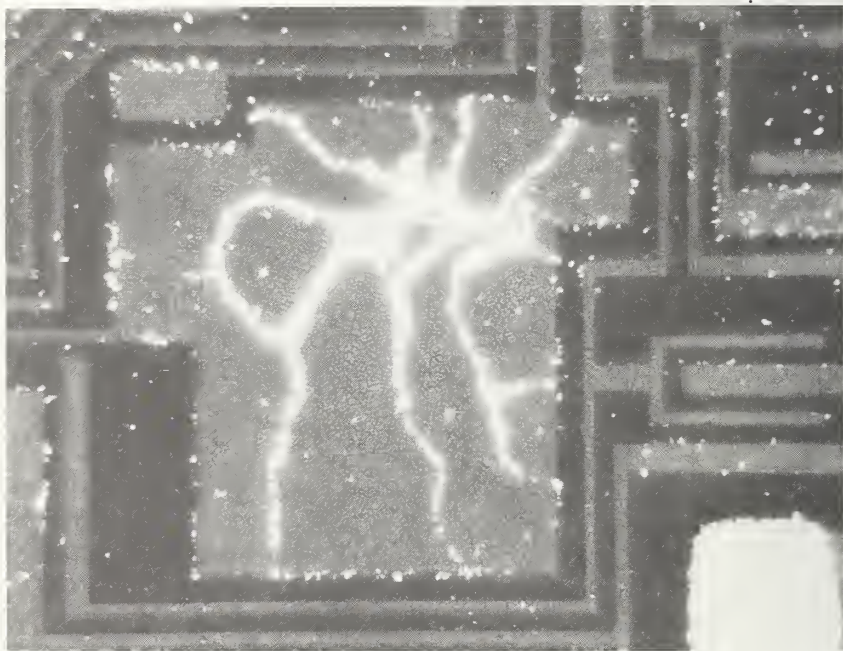


Figure 33. Direct decoration of defects after corona charging of insulator regions with ions of same sign as decorating particles in suspension.

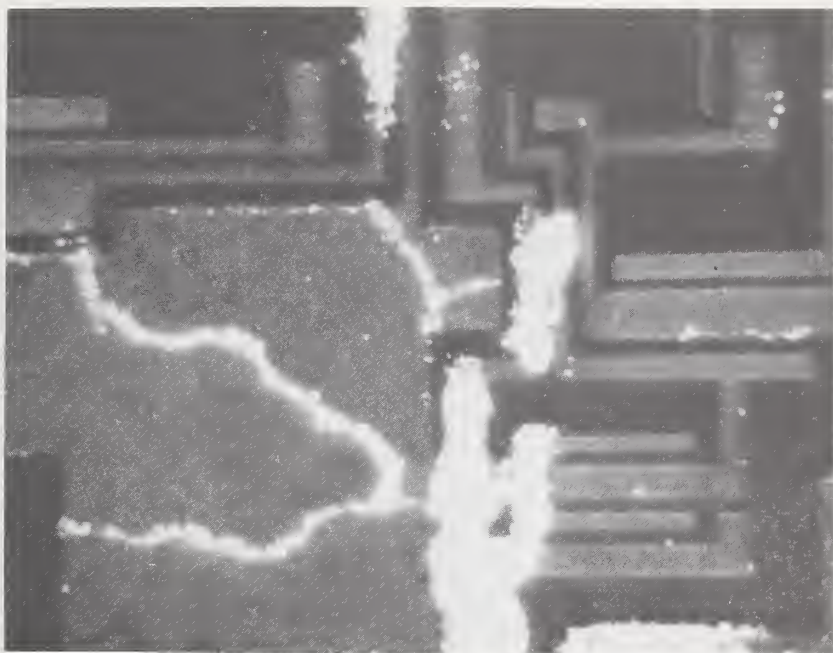


(a)

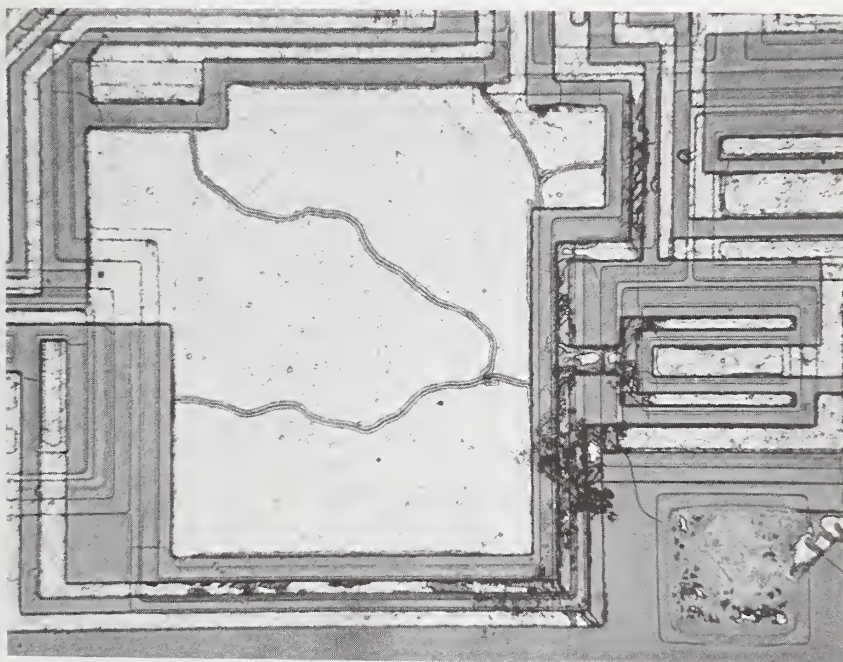


(b)

Figure 34. (a) and (b)-Phosphor deposition at 10,000 V charging voltage showing excellent crack detection. Not all isolated phosphor deposits correspond to pinholes at this high voltage. (150X, uv and brightfield).

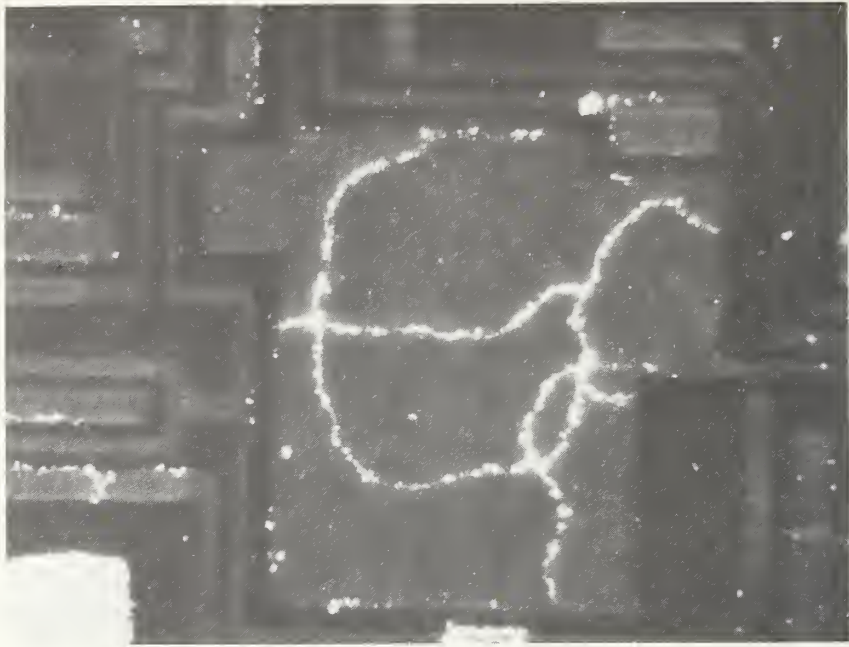


(c)

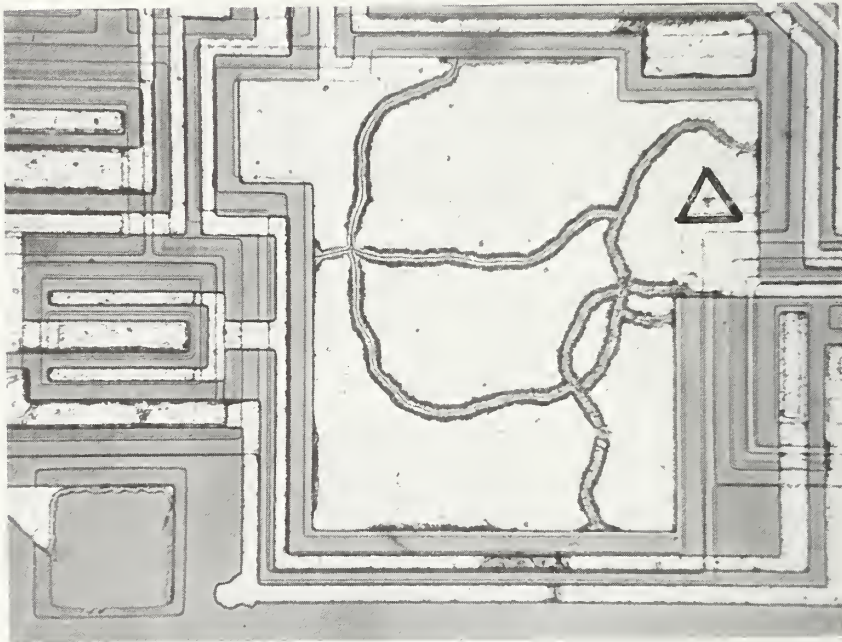


(d)

Figure 34. (c)-Phosphor deposition at relatively low charging voltage (6000 V). Note that cracks and large defects are detected by the phosphor (150X, uv and brightfield illumination). (d)-Sample from (c) after phosphor stripping followed by selective aluminum etching (15 min 50°C), (150X, bright-field).



(a)



(b)

Figure 35. (a)-Phosphor decoration at a charging potential of 6000 V prior to aluminum etching (150X, uv and brightfield illumination).
 (b)-Sample from (a) after phosphor stripping followed by aluminum etching (5 min 80°C). The triangle encloses a defect detected by etching which had not been decorated by the phosphor.

4.4.2.3 *Partial Pinhole Detection* - By using the special test pattern to etch thermal silicon dioxide and then regrowing oxide on the etched wafer, partial pinholes were simulated. Phosphor decoration of these test patterns indicated that partial pinholes in 7000-Å oxide with 2000 Å of oxide at the bottom of the hole (total partial pinhole depth of 5000 Å) could be detected if the pinhole diameter was greater than about 2 μm. This geometry represents an extreme and limiting case. Thinner bottom layers were also prepared and tested with good results, as illustrated in the two photomicrographs of figure 37. In the decoration of actual device wafers and comparison with etch detection methods, no partial pinholes could be found. Thus, we conclude that if partial pinholes exist in the passivating layers of these device wafers they are smaller than ~2 μm in diameter. This is certainly not surprising since one might expect a defect as large as 2 μm in diameter to penetrate the passivation layer completely. It is possible to enhance somewhat the detection of small partial pinholes by heating the sample at 100°C for 10 s between charging and phosphor deposition. It is believed that partial pinholes can be detected because, upon cessation of charging, the partial pinhole and the surrounding insulator are at the same surface potential. Immediately upon the cessation of charging, the surface potential begins to decay. This decay is very slow for the normal PSG or silicon dioxide layer but at the partial pinhole it is more rapid since the field across the insulator of partial thickness is greater. Thus, during the delay between charging and immersion, a voltage difference is formed which leads to decoration of partial pinholes. The 10-s heating at 100°C increases the decay rate and amplifies the potential difference.

4.4.2.4 *Effect of Surface Conduction* - The amount of phosphor deposited at cracks and pinholes can be markedly increased by exposing the sample to humid ambient for several seconds between charging and phosphor deposition. The moisture increases the surface conductivity of the insulators, and the surface charge in the proximity of a crack or pinhole leaks away. Thus, the defect is, in effect, expanded and more phosphor is deposited since the "defect" area is greater. An example is shown in figure 38.

4.4.3 Reverse Decoration of Defects by Corona Charging

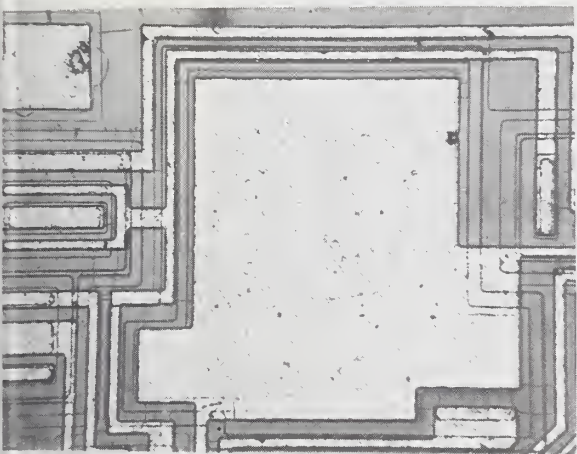
In this process the corona voltage polarity is chosen opposite that of the decorating particles so that deposition occurs on the insulator regions and not on the defects, as shown schematically in figure 39. As previously discussed, there is a relatively large margin of nondecoration around each defect due to ion deflection and surface current effects. Various decorating powders have been used, including phosphors, zinc oxide, and lead aluminosilicate glass, but the superior results in terms of sensitivity and contrast were obtained using carbon black suspensions.

Figure 36. Corresponding photomicrographs of a glass-overcoated linear bipolar IC with stress induced microcracks depicting two aluminum-metallized capacitor areas (a) and (b):

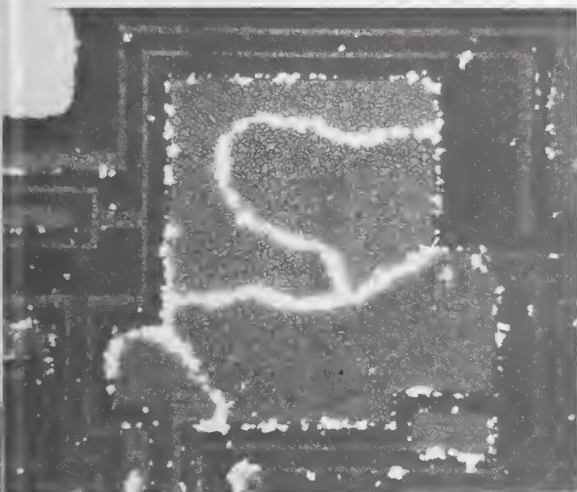
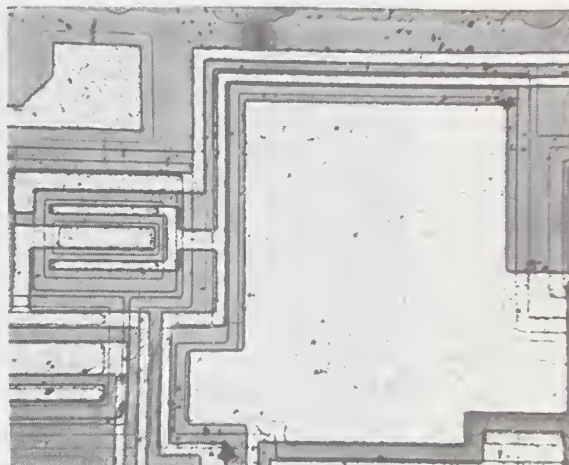
- (1) Samples before treatments, as seen under bright-field illumination ($\sim 100\times$).
- (2) Same samples electrophoretically decorated with $\text{ZnSiO}_4\text{:Mn}$ phosphor B, as seen in uv and bright-field illumination ($\sim 100\times$).
- (3) Same sample after stripping phosphor followed by 5-min aluminum etching at 50°C ($\sim 100\times$).

(a)

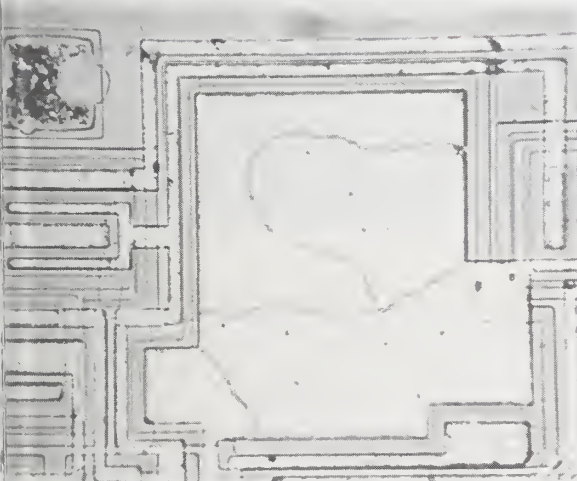
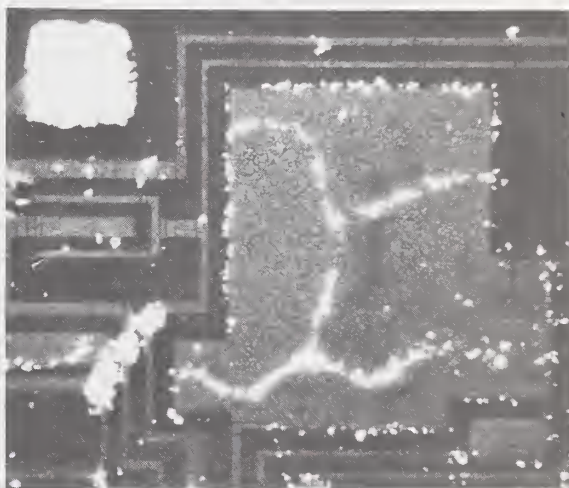
(b)



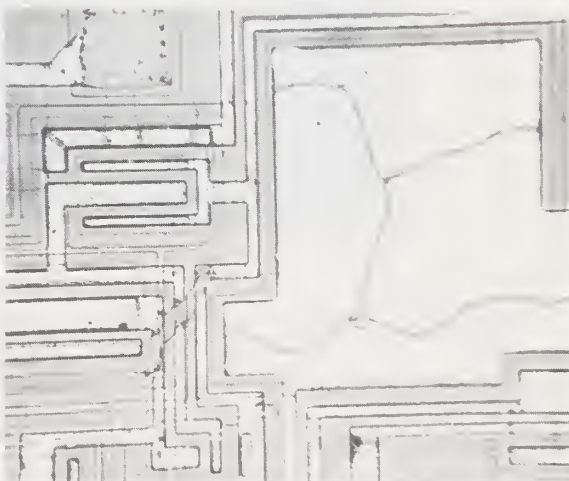
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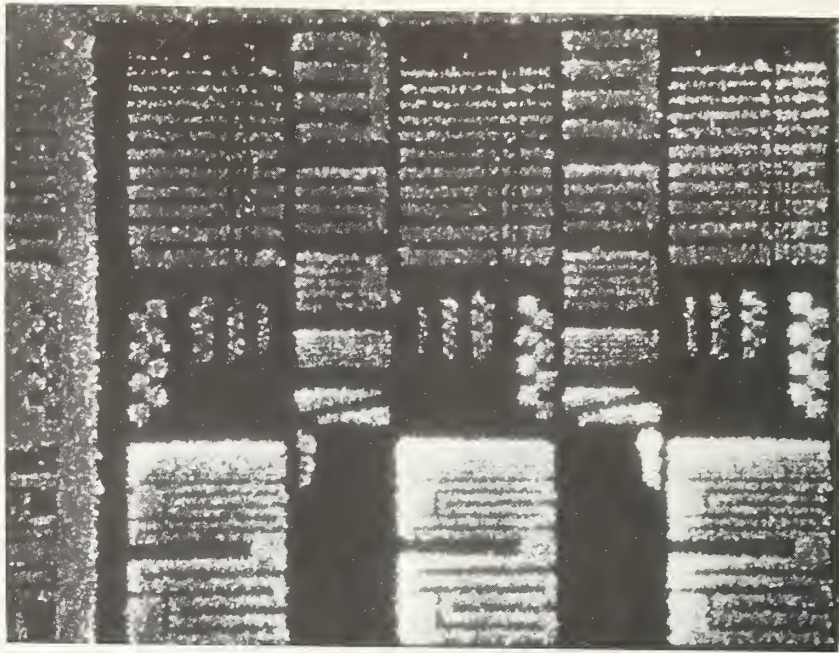


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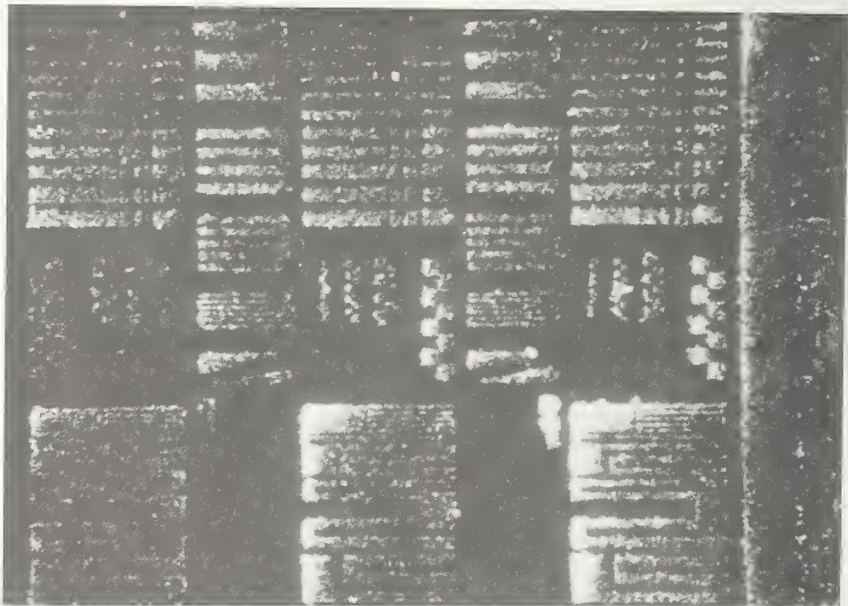


3





(a)



(b)

Figure 37. (a)-Electrophoretic phosphor decoration of negative/positive precision test pattern etched into 5000 Å of thermally grown SiO₂ on silicon. Thinnest line width is 1 μm (78.5X, uv illumination).

(b)-Same pattern as (a), showing feasibility of decorating "partial" pinholes or thin spots. In this case, 1000 Å of CVD SiO₂ was deposited over the same etched pattern used for (a) to simulate 1000-Å-thick-thin spots over silicon. The pattern (except the narrowest line) has become decorated, but with a lower quantity of phosphor.

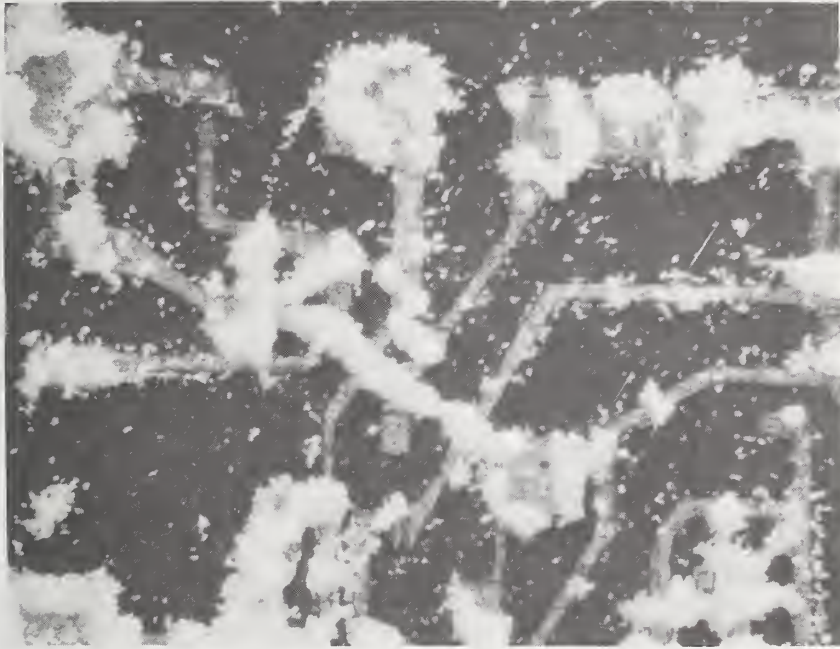


Figure 38. $\text{ZnSiO}_4\text{:Mn}$ phosphor deposited along cracks in $15,000\text{-}\text{\AA}$ CVD SiO_2 layer over IC wafer exposed to humid ambient ($\text{RH} = 62\%$) for 2 s between charging and deposition (150X, brightfield with uv irradiation).

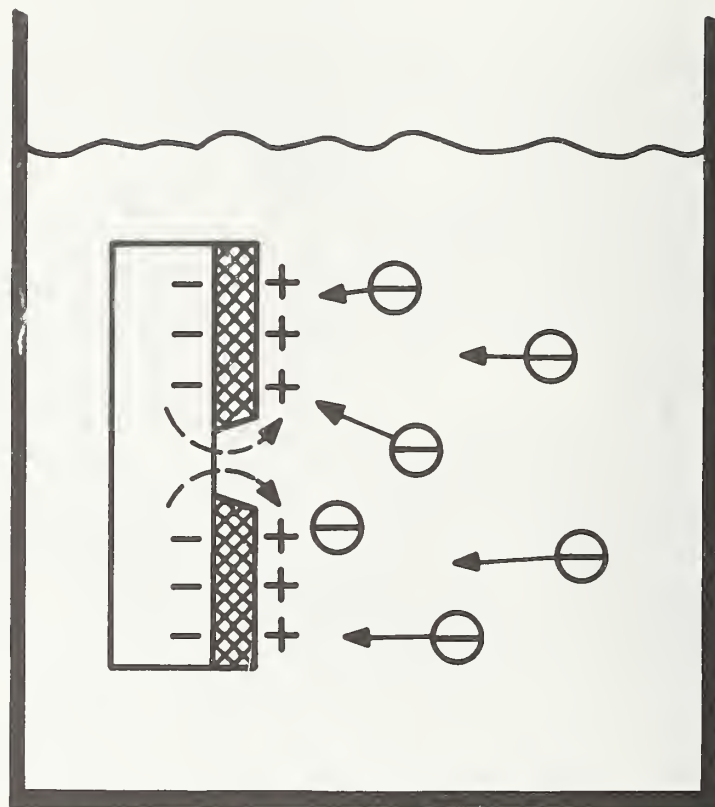


Figure 39. Reverse decoration of defects after corona charging of insulator regions with ions of opposite sign to that of decorating particles in suspension.

4.4.3.1 *Deposition Process* - Various carbon black suspensions were tested that included commercially available electrophotographic toner concentrates and formulations prepared in our laboratory. Best results were obtained with a carbon black suspension [31] prepared in the following way. First, a concentrate is made from:

- 17.0 g Raven 1255 carbon black (Columbian Division, Cities Service Co.)
- 100.0 ml toluene
- 10.0 ml of 50 g/50 ml toluene dilution of Lubrizol 894 (Lubrizol Corp.)
- 10.0 ml of 50 g/90 ml toluene dilution of AC Polyethylene-grade 430 (Allied Chemical)

These ingredients are agitated for about 5 min with an ultrasonic probe at 100-W power level to disperse the carbon black.

The materials used are readily available. The carbon black has an arithmetic mean particle diameter of 220 Å and a nitrogen absorption surface area of 130 m²/g. The surface of the carbon black as supplied is acidic by addition of volatiles [32]. Lubrizol 894 is an ashless dispersant additive for heavy-duty engine oils. Weight percent of nitrogen ranges from 1.65 to 1.95% [33]. AC Polyethylene-grade 430 is a polyethylene-vinyl acetate copolymer (30% vinyl acetate). Its softening point is 60°C [34]. This concentrate is added at a proportion of 0.75 to 1.00 ml to 400-ml C₂Cl₃F₃ and stirred to produce the suspension. The concentrate and dilute suspension are stable for long periods (months). The carbon black in this suspension is negatively charged so that positive corona potentials are used for reverse decoration. .

The charging process is done as described in section 4.4.1 using +7000 V dc at a sample-to-wire spacing of 2 cm for 18 s. After a 10-s standard delay, the sample is immersed in the suspension for 6 to 12 s, depending on type. Generally, for wafers and single chips we have used 12 s, while for opened packaged devices 6 s has been used. As described previously, a standard precharging bake is used and the charging and deposition are done in nitrogen ambient with RH ≤ 25%.

4.4.3.2 *Suspension Properties* - Measurements were conducted to characterize the electrical state of the carbon particles in the dilute suspension by depositing the carbon black on metal foils while recording the current, and then weighing the deposited carbon by difference. This was done as a function of applied voltage and time. The weight of carbon black deposited and the charge transported varied almost linearly with voltage and time. For electrode spacings of 1.7 cm on each side of a metal foil, an applied voltage of 100 V for 4 min resulted in a deposition of 3.2 x 10⁻⁴ g carbon black per cm². Tests such as these are convenient for monitoring the electrical properties of the suspension and ensuring reproducibility of these properties.

Combined charge flowing and weight measurements resulted in a charge per single carbon black particle of 5×10^{-2} electronic charge per particle, assuming all particles to be 220 Å in diameter, and singly dispersed. Since the minimum charge can be no less than 1 electronic charge per particle, the carbon black is not monodispersed but is aggregated at least by a factor of 20. Indeed, this aggregation is essential to obtaining dense black on the charged insulator surface since the surface charge after corona charging is only about 4×10^{11} electronic charges per cm^2 . This would result in somewhat less than monolayer coverage if the carbon were monodispersed with one electronic charge per particle. Actually, the layer deposited is many particles thick. Thick layers are an advantage since the optical density is saturated, and relatively large variations in thickness can be tolerated without affecting the percentage of light reflected.

The recommended ratio of 1 ml of the concentrate in 400 ml of $\text{C}_2\text{Cl}_3\text{F}_3$ results in a suspension containing 0.1 g of carbon black; at least ten IC wafers (75-mm diameter) can be decorated with it.

4.4.3.3 Deposition Properties - The detection of cracks and pinholes is carried out quite conveniently by microscopic observation. An example is shown in figure 40. Extensive comparison tests confirmed that every defect detected by etching of the underlying aluminum through the defects was detected by the carbon black reverse-decoration. This was done in two ways. Wafers and chips were decorated with carbon black, and photomicrographs were taken of crack and pinhole patterns. The carbon black was then removed, and aluminum etching at 50°C for 5, 7, 10, and 15 min was done. The samples were again photomicrographed and the results compared. Hundreds of micrographs from many different sample types were compared and, in every case, all defects detected by etching were also clearly outlined by the carbon black. In the second method, samples were decorated with carbon black and then aluminum-etched with the carbon black in place. Again, the correlation was excellent. An example of the latter test is shown in figure 41.

Various carbon black dispersions have different voltage thresholds for deposition [35]. The voltage threshold is that surface voltage on the insulator below which the carbon black will not deposit. For a given surface charge density, it is a function of the carbon black dispersion and of the insulator properties. Since the surface voltage profile decreases to zero voltage rapidly around a pinhole, and laterally at a crack, a clear margin, in which no carbon black is deposited, is found around defects. The extent of this clear area is a function of the threshold voltage for deposition and the surface conductivity. To avoid excessive width of clear areas, a carbon black dispersion formulated to have low threshold voltage was used, as described previously. This may be compared with a high threshold formulation in figures 42(a) and (b), where the differing margins are clearly evident.

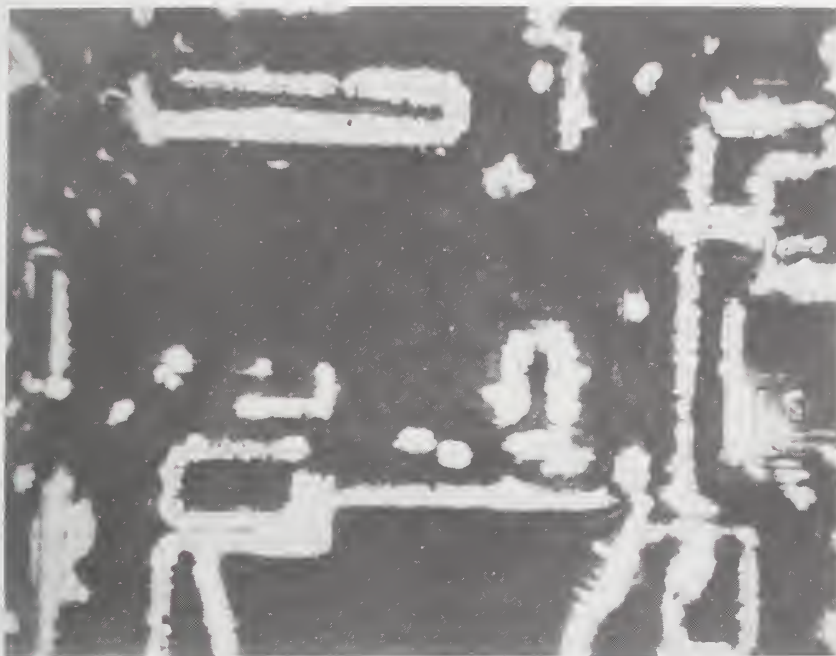
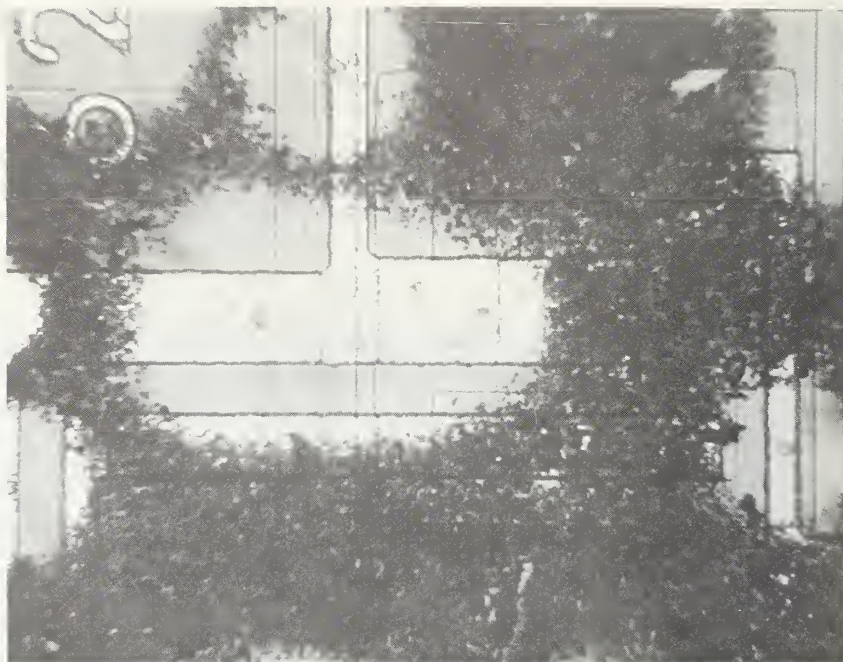


Figure 40. Carbon black deposited on device to reverse-decorate the defects. High contrast renders microscopic evaluation fast and sensitive. Width of narrowest aluminum lines (visible at right) is about $12\text{ }\mu\text{m}$ (150X).

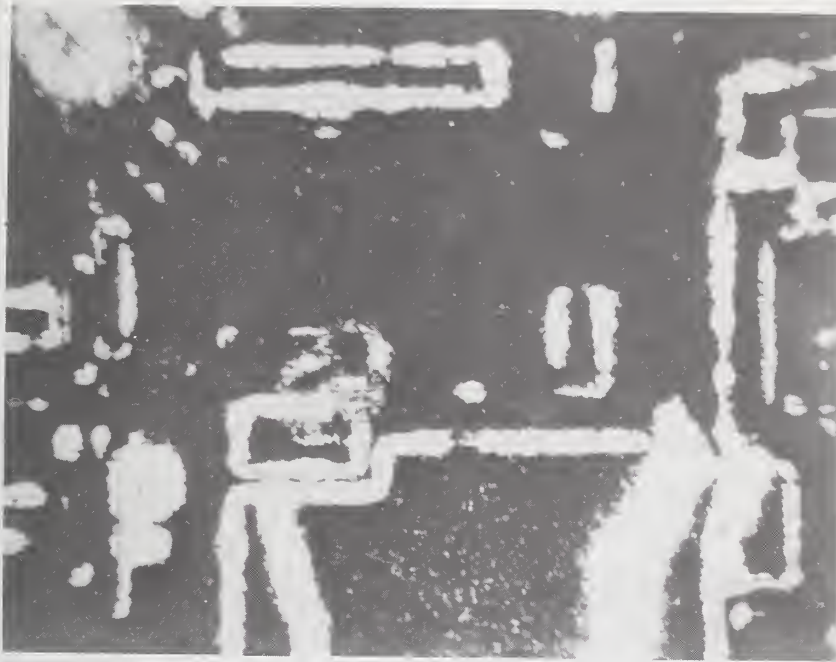


(a)

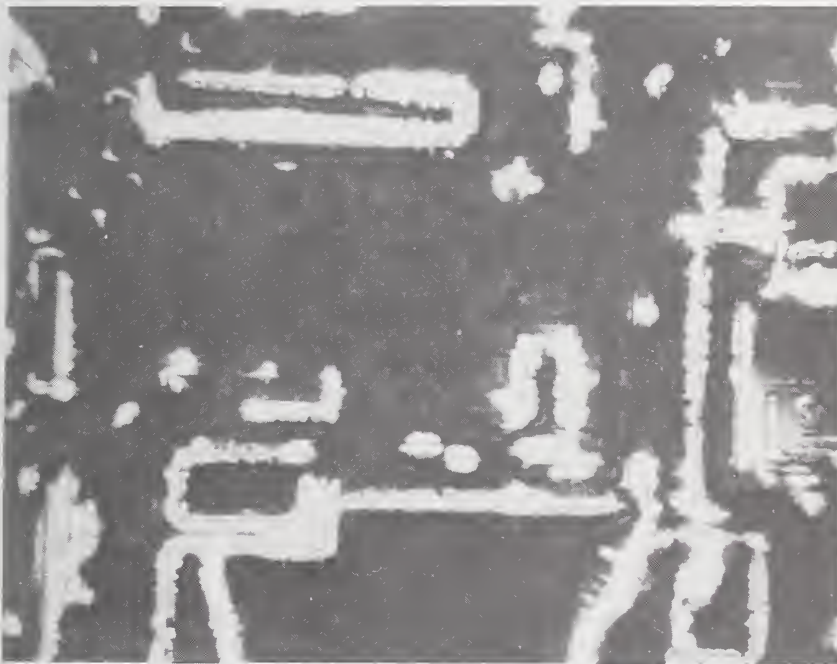


(b)

Figure 41. Confirmation of defect detection by the reverse-decoration method. Sample was aluminum-etched at 50°C for 5 min without removing carbon black. (a) 385X, (b) 760X.



(a)



(b)

Figure 42. Carbon black deposition with high threshold voltage in (a) compared to one with low threshold voltage in (b); (150X, brightfield).

As noted, the decrease in surface voltage near a defect leads to a clear margin around defects. Two effects contribute to the voltage decrease: (1) During charging, ions are deflected to the defect area by the fringing fields; and (2) finite surface conduction results in surface charge motion which modifies the charge distribution. At high corona potentials (10,000 V), the ion deflection is a relatively small factor and, in this case, surface ion motion results in a nondeposited area which increases with time between charging and carbon deposition. For the lower voltage normally used (7000 V), ion deflection effects are much greater, and in this case surface ion motion tends to shrink the nondeposited area for the first few seconds between charging and deposition. These effects are shown in figures 43(a), (b), and (c). In (a), deposited 4 s after charging, there is a wide margin due to ion deflection during the charging. In (b), deposited 10 s after charging, the margin has decreased due to surface ion motion. In (c), deposited 120 s after charging, the margin has increased due to surface charge leaking off. Because of these effects, a standard delay of 10 s is used between the cessation of charging and the deposition of carbon black.

The width of clear, undeposited margin can be varied also by varying the temperature of the sample during charging and deposition. Using a thermoelectric cold plate, samples were cooled to -7°C during charging and then immersed in the carbon suspension held at -7°C . The defect margin was only about one third of that found for the same sample decorated at 23°C .

Detection of partial pinholes is also possible with the reverse technique. Partial pinholes of $5000\text{-}\text{\AA}$ depth in $7000\text{-}\text{\AA}$ total thickness of thermally grown silicon oxide and $1.5\text{-}\mu\text{m}$ diameter could be detected by heating the sample for 10 s at 100°C between charging and deposition.

4.4.4 Sample Cleaning After Decoration

Methods of removing the various decorating particles were investigated. For the phosphors, glass powders, and other inorganic powders, removal is quite simple with ultrasonic agitation in a 50/50 volume mixture of $\text{C}_2\text{Cl}_3\text{F}_3$ /acetone or $\text{C}_2\text{Cl}_3\text{F}_3$ /isopropanol, followed by rinsing without ultrasonic agitation in a fresh quantity of one of the previous solutions. A final rinse in $\text{C}_2\text{Cl}_3\text{F}_3$ results in rapid drying.

The carbon black can be removed by soaking the samples in toluene for 15 min, followed by ultrasonic agitation in toluene and $\text{C}_2\text{Cl}_3\text{F}_3$ rinsing. Another procedure is to use a commercial photoresist developer spray machine which cleans the sample in one pass [36].

When ultrasonic energy is used, care must be taken to avoid sample damage. Contact of the wafer with hard surfaces, such as beaker sides or bottom, should be avoided. We have found that careless use of the ultrasonic bath has actually caused pinholes in previously good passivating layers.

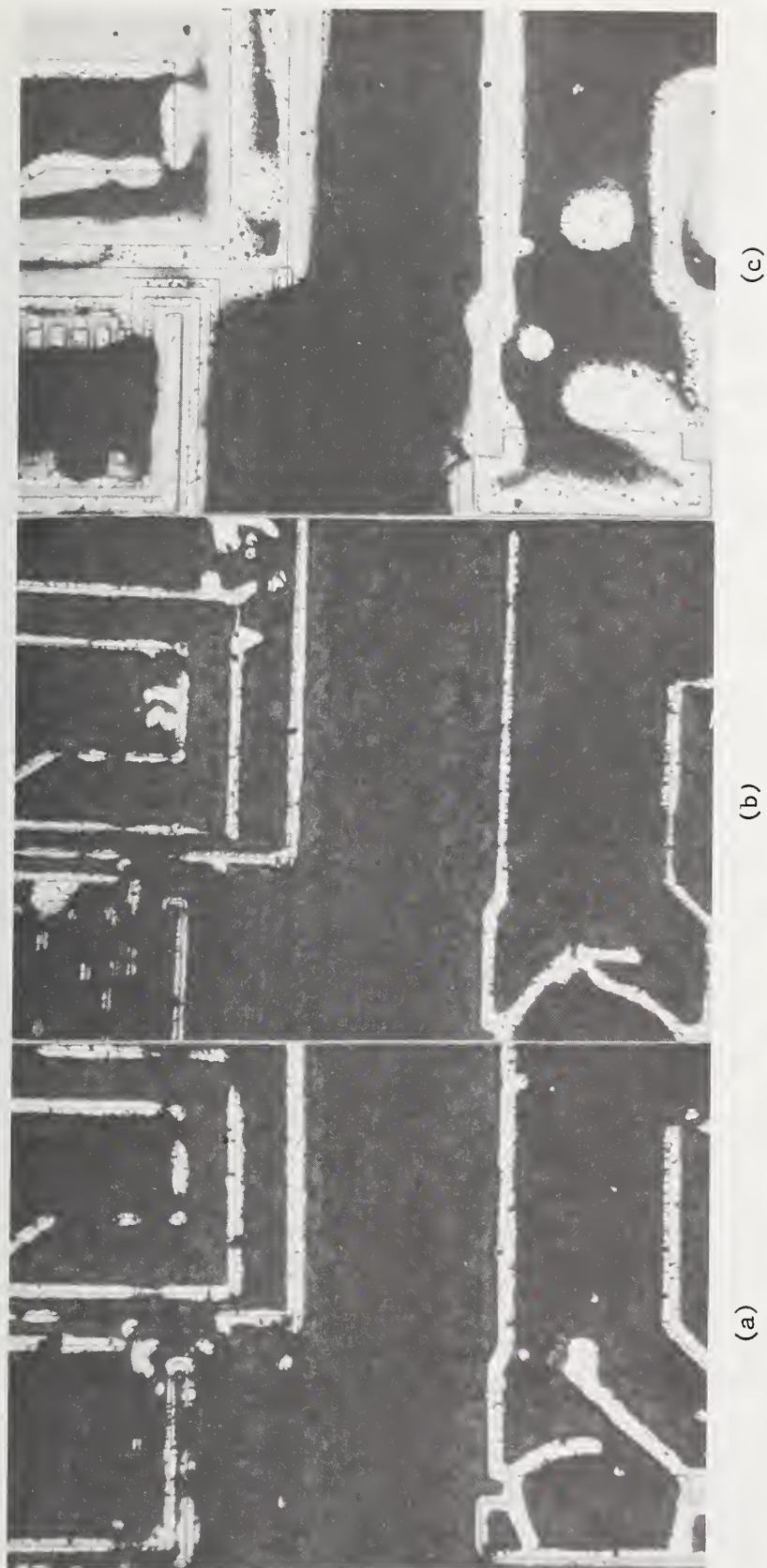


Figure 43. Carbon black reverse-decoration as function of time delay between charging and deposition. The time delays are (a) 4 s, (b) 10 s, (c) 120 s. Corona potential was +7000 V dc (78.5X, brightfield).

4.4.5 Nondestructiveness of Methods

Since the corona-charging method, in particular the reverse carbon black decoration technique, was found to be the most attractive method, only this process was tested for nondestructiveness. The conventional cell electrophoretic method was not evaluated in this respect. Several types of extensive tests were done. In one test, device wafers were aluminum-etched to reveal pinholes. Then the wafers were exposed to the corona discharge at 10,000 V dc for various times ranging up to 100 s. After the corona discharge, aluminum etching revealed no new pinholes.

In a second test, one set of five device wafers was reverse-decorated with carbon black and a second set of five was direct-decorated with phosphor. After cleaning, the decoration was repeated. This process was repeated five times. Only one wafer showed new defects (pinholes). These were found after the third carbon black deposition test. During cleaning, this wafer had been placed face down in the bottom of the ultrasonic tank, and it is believed that the mechanical contact caused these defects. Subsequent tests with the ultrasonic tank used in this manner did induce defects.

A third test involved automatic probe testing of CMOS wafers. These were chosen since it is expected that CMOS devices are susceptible to static electrical damage. Two large (75 mm) CMOS device wafers were probed, and a map was made of good and bad devices. Then the wafers were charged, decorated, and cleaned. The wafers were probed again. One wafer showed a net loss of four devices out of about 130 good devices. The other wafer showed a net gain of five devices out of about 100 good devices. These variations are within the normal tolerance of repeated wafer probe testing. It is concluded that the process of corona charging and decoration is nondestructive. No life tests of decorated and cleaned devices were done, however. Thus, it may be possible to use decorated wafers for product, but an assessment of reliability by accelerated life testing is needed.

4.5 Techniques for Quantifying Defect Density

4.5.1 Manual Microscopic Analysis

The density of demarcated or decorated localized structural defects in a dielectric layer can be determined by counting the number of defect sites per unit sample area, using one of several microscopic techniques discussed previously [1]. The choice depends on the uniformity and density level of defects, the type of material used in decorating, the degree of accuracy required, and the specific purpose of analysis.

Incident white light, brightfield illumination or Nomarski differential interference contrast are most suitable for observing demarcation-etched samples. Observation under intense incident uv light from sources positioned directly over the sample stage of the

microscope is used for luminescing decoration material. Brightfield illumination is best for carbon black decoration.

The magnifications used should be sufficient to allow resolution of individual demarcated defect sites, but not higher, to be able to observe the largest possible sample area within the field of view. It is impossible to specify a fixed magnification that would hold for all cases, but we have found a magnification range within 50 to 500 diameters most useful.

The greatest difficulty in determining the density of defects by any method concerns the distribution uniformity. If the uniformity of distribution is "good," counting within a few sample sites may provide an adequate measure of the true statistical distribution. If it is "fair," which is the most common occurrence, examining a substantial number (say 5 to 15) of areas over the sample may be necessary to arrive at a valid average density value. Samples with "poor" uniformity are best treated by identifying the sample areas into "good," "fair," and "poor," and retaining separate density values for each rather than computing a meaningless average value.

The sampling areas for counting should be spread in a reasonably uniform manner over the sample surface. If it is a device wafer or patterned sample, one may choose to examine every nth unit and count the defects within that defined area. If the sample is not patterned, then the microscope stage micrometer can be used to space the observation sites uniformly over the sample. The circular area of the microscope field of view for the magnification may be used as a convenient unit. Photomicrography affords a useful record of the defect density and often facilitates counting of the defect sites, especially if the density is high; it also provides an accurately defined area of the sample surface.

4.5.2 °Feasibility Study of Automated Read-out

A major advantage of the carbon black reverse decoration method is the high optical contrast available in reflected light microscopy. This permits a fairly simple form of automated quality assessment with a microscope-mounted photocell to measure the integrated light reflected from the defect areas. This technique is much simpler than the use of computer-implemented image analysis. The latter would provide a defect count, which the integrated reflected-light method does not furnish. However, based on our feasibility study, it is believed that the simple method explored here could be used in a production facility to rank wafer quality and set a quality acceptance criterion.

Initially, photomicrographs were made of carbon black reverse-decorated devices on IC wafers. Transparencies made from these micrographs were then mounted in an optical system so that a collimated light beam was passed through the transparency and then focused on the faceplate of a vacuum photocell to form an image of the light source. An image of the transparency is not desired since the photocell response may not be uniform across the faceplate. The current output of the

photocell varies linearly with incident light. It was found that the current output varied inversely with subjective judgments of device quality made by counting pinholes and estimating crack lengths.

Based on these encouraging preliminary results, a photocell-microscope system was assembled to take direct readings of reflected light from decorated wafers. The arrangement used is shown schematically in figure 44. By placing a plano-convex lens of 57-mm focal length at the end of the camera tube, an image of the light source field stop was obtained about 6 cm from the end of the camera tube. This image, of uniform luminance, was placed on the photocell faceplate. The photocell employed an S-11 cathode and was operated at 100 V. Light intensity was adjusted to give convenient current levels, and the overall magnification was chosen so that a large portion of the circuit was visible, but bond pads and grid lines were excluded. Shielding prevented introduction of ambient light. Current readings were taken on 20 circuits of each of two wafers. For the "good" wafer, the lowest individual current was 2.9×10^{-9} A, the highest was 5.5×10^{-9} A, and the average was 3.5×10^{-9} A. For the "bad" wafer, the lowest current was 6.7×10^{-9} A, the highest was 1.5×10^{-8} A, and the average was 1.0×10^{-8} A. Pinhole counts on these wafers resulted in a difference of a factor of two in defect density. Thus, the photocell current measurement can easily detect a difference of a factor of two in pinhole density and is probably more sensitive than this.

4.6 Advantages of the Reverse Decoration - Carbon Black Method

In this section the relative advantages of the carbon black reverse decoration technique are summarized. Based on our results, the carbon black method is recommended for defect detection in most cases. In the discussion several unique advantages of the corona-charging technique as used in the reverse decoration will be pointed out. The use of the high-voltage discharge, which initially appears to violate the normal rules for treatment of devices (particularly, MOS type), will be seen to be a definite advantage and to render the process actually nondestructive.

4.6.1 Speed

In the standardized process to be described later, the sample is charged for 18 s, and after a 10-s delay, is immersed in the carbon black suspension for 6 or 12 s. Thus, the total decoration process time is, at most, about 40 s. We do not include in this time the recommended 5 min, 200°C bake since this can be done in batch. This process time of 40 s may be compared with the 5 min needed for metal etching, the several minutes needed for electrolytic techniques [14,15] or for the conventional electrophoretic method previously described here.

4.6.2 Simplicity

The process is very simple and does not require precise positioning or delicate manipulations, as is sometimes the case in, for

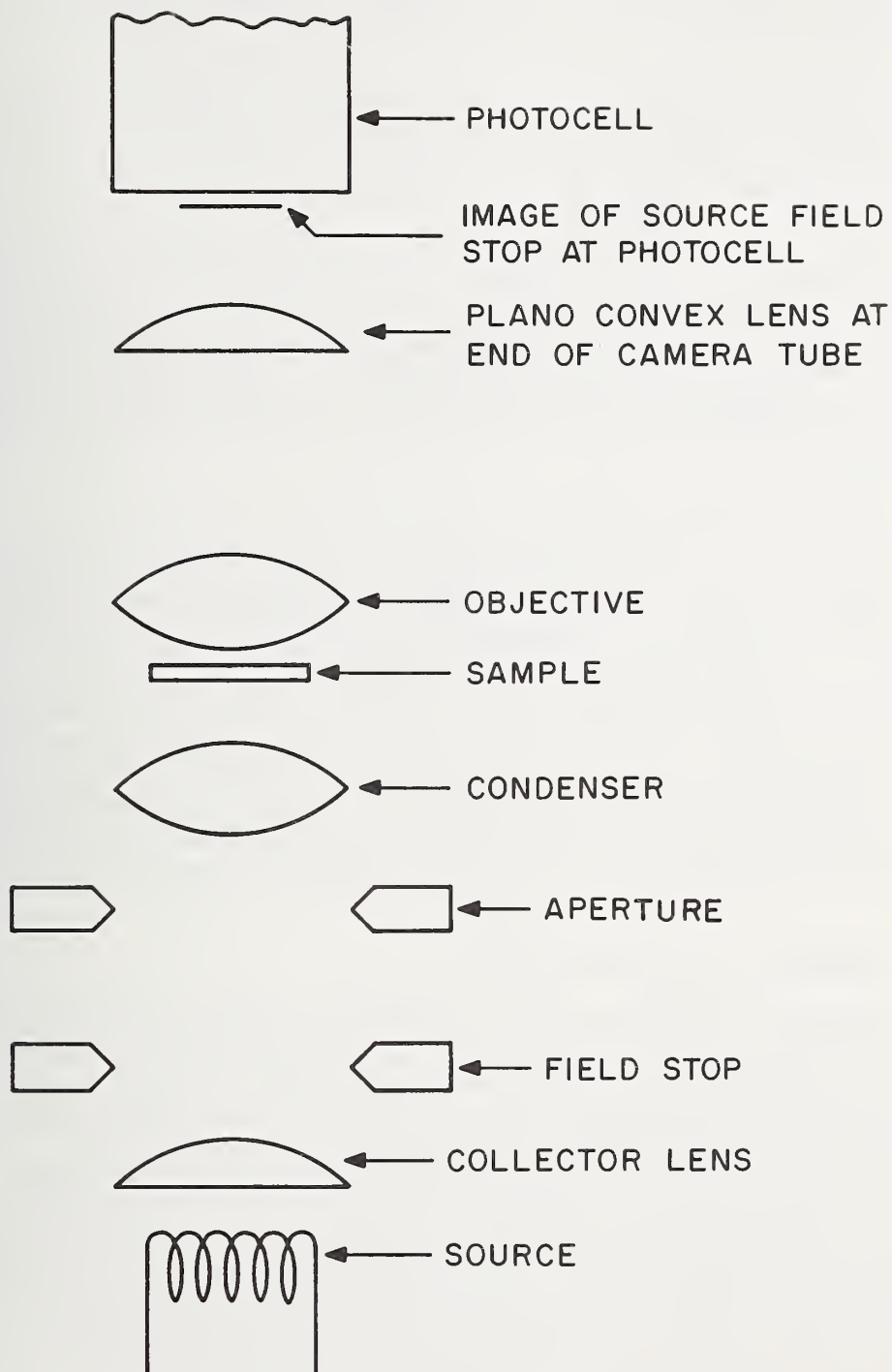


Figure 44. Schematic of microscope use for obtaining image of source field stop at photocell for reflected light measurements. The sample is both illuminated by the light source and observed by the photocell from the same side.

example, the liquid crystal technique [8]. The sample is placed on a platform for charging and then dipped into the carbon black suspension. The process thus shares the simplicity of chemical etching, with the added relaxation that the time of immersion in the liquid is constant for a wide range of samples, and does not depend on sample parameters as in the etching method, where the aluminum thickness must be considered.

4.6.3 Permanence of Decoration

Liquid crystal and bubble formation techniques are real-time methods in that the decoration exists only during the process implementation. A photograph must be made for later examination. The carbon black decorated sample, however, has a permanent decoration and it may be set aside for future examination. This feature of permanence is an important one which the process shares with etching, electrophoretic, and copper decoration methods.

4.6.4 Nondestructive Nature

Unlike the etching or electrolytic copper techniques, the carbon black decoration can be removed. Tests by wafer probing showed no device loss after cleaning, as described previously. In methods which make use of voltages applied between electrodes and the sample in an electrolyte, as used in copper decoration for example, there is the possibility of sample damage by high currents at dielectric weak spots. The corona-charging process in a dry ambient ($RH \lesssim 30\%$) is inherently nondestructive since corona potentials are well below sparking voltage and the corona has a very high impedance. Furthermore, any dielectric weak spot will discharge only the surface charge immediately surrounding it, and the stored energy is not great enough to cause any dielectric damage.

4.6.5 Avoidance of Junction Effects

Decoration methods using electrolytes or other low-resistivity liquids, such as alcohol or acetone, are limited by device junction effects. For example, a dielectric defect over a reverse-biased junction may not be detected or the deposition rate of decorating material may be slow. This effect can be overcome or moderated by illuminating the sample to induce photocurrents in reverse-biased junctions, but this may be difficult in some cases. For example, in the case of a large sample, as a wafer immersed in a decorating suspension of light-scattering particles, insufficient light may reach certain portions of the sample. On the other hand, the corona current impedance is so great that even reverse-biased junctions are sufficiently conducting that they do not interfere with charging effects.

4.6.6 High Contrast

The reverse decoration with carbon black provides a very high contrast when imaged in a microscope in reflection. This high contrast contributes to rapid evaluation of the relative quality of samples by

the observer and, in addition, permits automated assessment by use of a photocell attachment to the microscope.

4.6.7 Ease of Observation

The reverse decoration process leaves the defect uncovered for easy examination by optical or electron microscopy. All other known processes result in direct decoration and the defect is covered or altered in some way.

4.6.8 Limitation

The only fundamental limitation encountered thus far has been devices with regions of metal not connected to the semiconductor. This floating metal is brought to a high potential by the corona so that the metal is outlined with carbon black, but no defects can be detected over it. Thus, floating gates on some memory devices would not decorate properly if the device were examined at a stage of processing before the overlying metal is deposited. The other regions of the sample could be successfully decorated, however. After the device is completed and the second metal covers the floating gate, then it is possible, of course, to decorate the device in the standard manner.

5. ADVANTAGES AND DISADVANTAGES OF THE METHODS INVESTIGATED

In this section a comparison of the five processes investigated under this contract is presented in tabular form. The comparison is made on the basis of simplicity of procedure, process time, permanence of the decoration (adhesion), destructiveness or nondestructiveness, susceptibility to reverse-biased junction effects, contrast in microscopic observation, sensitivity of detection, ability to detect partial or latent defects and to obtain a depth profile of partial defects, and ease of microscopic observation and limitations. For each of these characteristics, the five processes are compared in table 6. The comparison assumes that typical, aluminum-metallized IC wafers with PSG passivation overcoats are being tested.

TABLE 6. ADVANTAGES AND DISADVANTAGES OF METHODS INVESTIGATED

Characteristic Method	Simplicity	Analytical Process Time	Decoration Permanence	Destructive	P-n Junction Effects	Optical Contrast	Analytical Sensitivity	Partial Defect Detection	Partial Defect Depth Profile	Ease of Observation	Limitation
Metal demarcation etching	Very Simple	5 min	Absolute	Yes (at defect sites)	No	Low	High	No	No	Less easy	Defects over metal only
Metal-insulator sequential etching	Simple	30 min	Absolute	Yes	No	Low	Very high	Yes	Yes	Less easy	Defects over metal primarily
Electrophoretic decoration	Very Simple	5 min	Good	Possible insulator breakdown	Reverse bias junctions may be problem	Medium	Medium, suitable for large defects	Yes	No	Easy	Floating metal a problem; defect size
Direct decoration by corona charging	Simple	40 s	Excellent	No	No	Medium	High	Yes	No	Easy	Floating metal a problem
Reverse decoration by corona charging	Simple	40 s	Excellent	No	No	Very high with carbon black	Very high; carbon black shows defects not found by SEM	Yes	No	Very easy	Floating metal a problem

6. ADDITIONAL EXAMPLES OF APPLICATIONS

6.1 Metal Demarcation Etching

We have applied this simple, fast, and absolute test method widely in the analysis, control, and evaluation of oxide-, glass- and nitride-passivated IC test wafers and single pellets, including plastic encapsulated and hermetically sealed devices [5]. A few representative examples are presented here to illustrate further the capability of the technique.

The appearance of demarcation-etched area pinholes is shown in figure 45, while edge pinholes along the delineated edges of metallization interconnect lines are seen in figure 46. These samples were individual IC pellets in plastic packages that were prepared for analysis by techniques reported elsewhere [5].

Experimental examples of typical pinholes in silicon nitride overcoats deposited by rf glow discharge reactions at 300°C are shown in figure 47 for an aluminum-metallized IC, and in figure 48 for a gold-metallized IC.

6.2 Metal/Insulator Sequential Etching

A typical example of a sequentially metal/glass-etched, aluminum-metallized IC is shown in figure 49. Most of the pinholes seen were opened after repeated glass etching, and thus represent buried, partial, or latent pinholes that had resided in part of the passivation layer.

Extensive use has been made of the sequential metal-insulator etching method for the quantitative and comparative analysis of CVD passivation layers of various compositions, structures, layer combination, and post-deposition heat treatments. The results of one typical application for pinhole testing are presented graphically in figure 50. Similar results have been obtained for edge coverage thickness analysis or the determination of latent or ultrafine microcracks not detectable by direct metal demarcation etching.

Latent microcracks in glass layers that are invisible even by high-magnification SEM and that cannot be detected by direct metal demarcation etching can be successfully developed by a brief period of glass etching, as discussed further in section 6.5.

6.3 Electrophoretic Decoration

The process of electrophoretic decoration with phosphor particles or lead aluminosilicate glass particles has been used to decorate defects in thermal oxides on mesa-type power devices and in passivating layers on ICs. Several examples are given in section 4.3. This technique has proved useful for large defects.

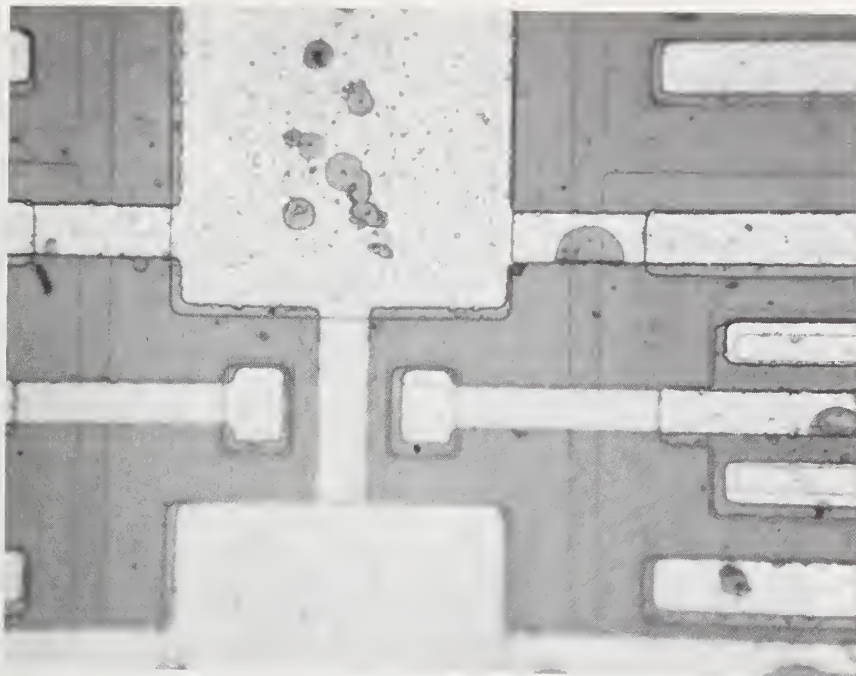


Figure 45. Selectively demarcation-etched area pinholes in a defective passivation test layer over an aluminum-metallized IC (760X).

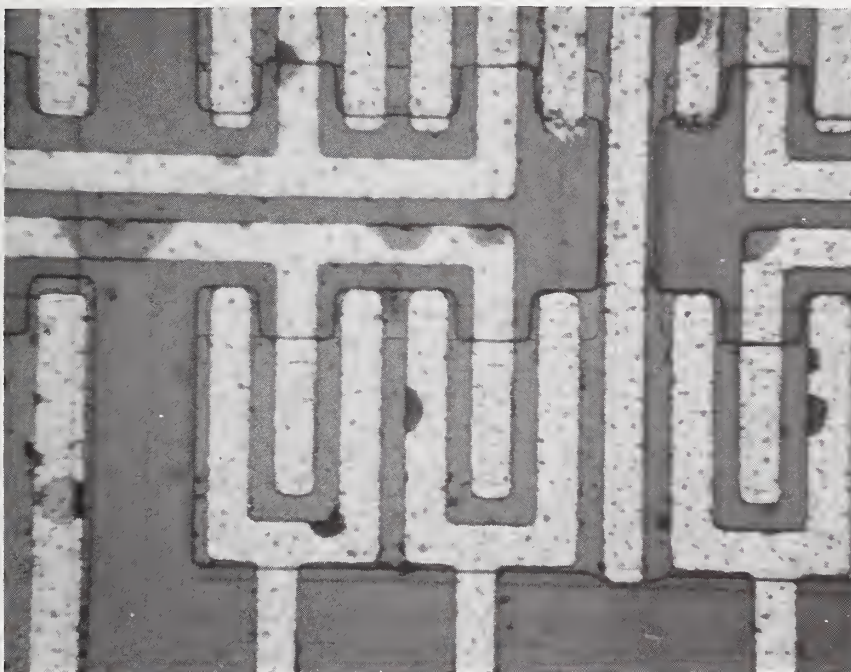


Figure 46. Selectively demarcation-etched edge pinholes in a defective passivation test layer over an aluminum-metallized IC. Particulates are surface impurities left from plastic de-capsulation processing (385X).

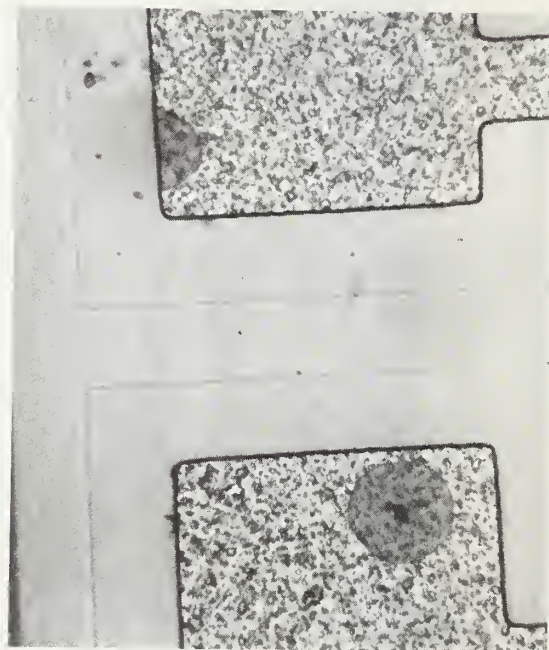
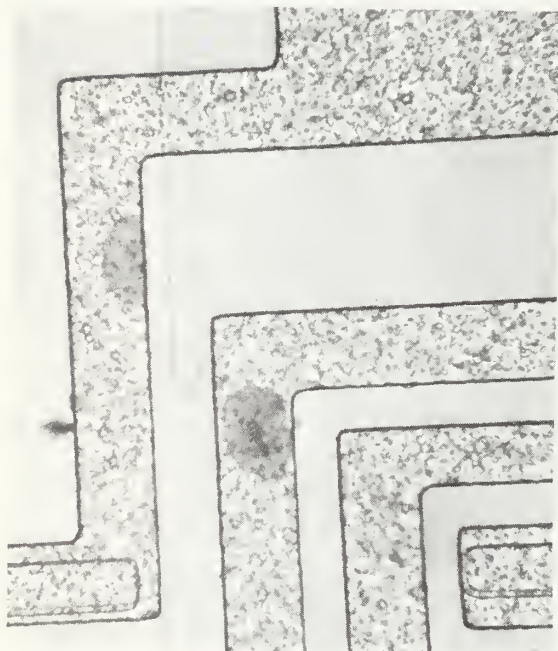
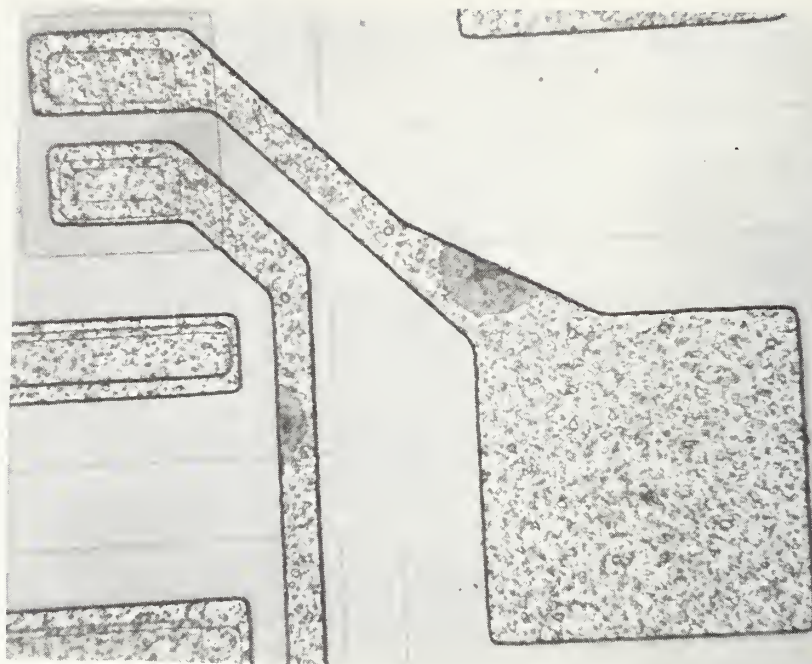


Figure 47. Variety of selectively demarcation-etched area and edge pinholes in a rf plasma-deposited silicon nitride passivation layer over an aluminum-metallized IC (385X).

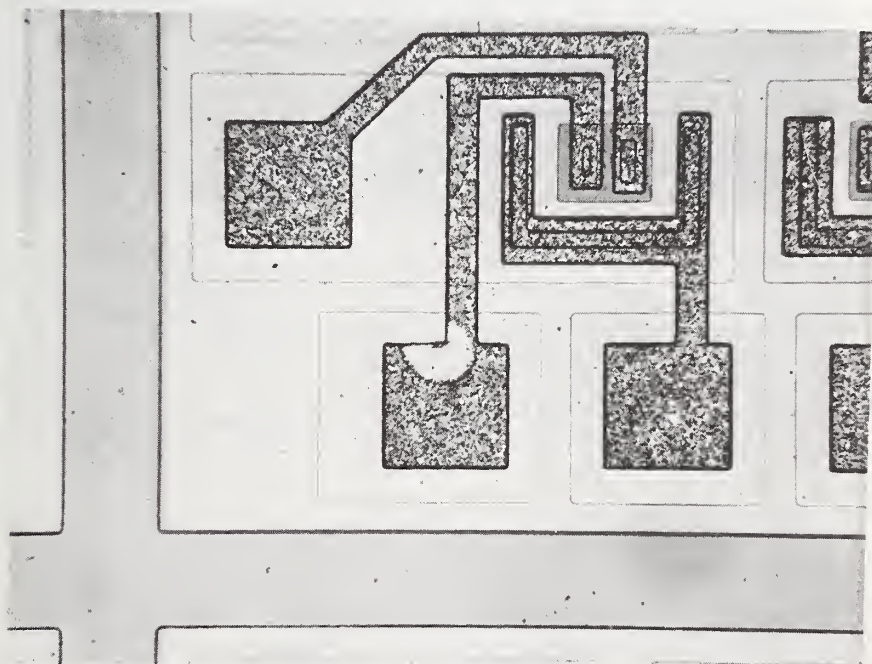
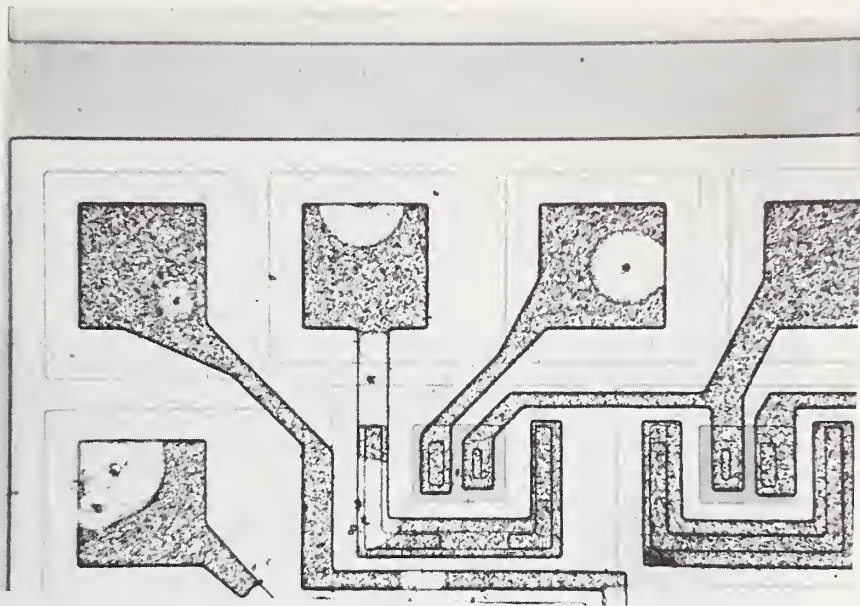


Figure 48. Variety of selectively demarcation-etched area and edge pinholes in a rf plasma-deposited silicon nitride passivation layer over a gold-metallized IC (150X).

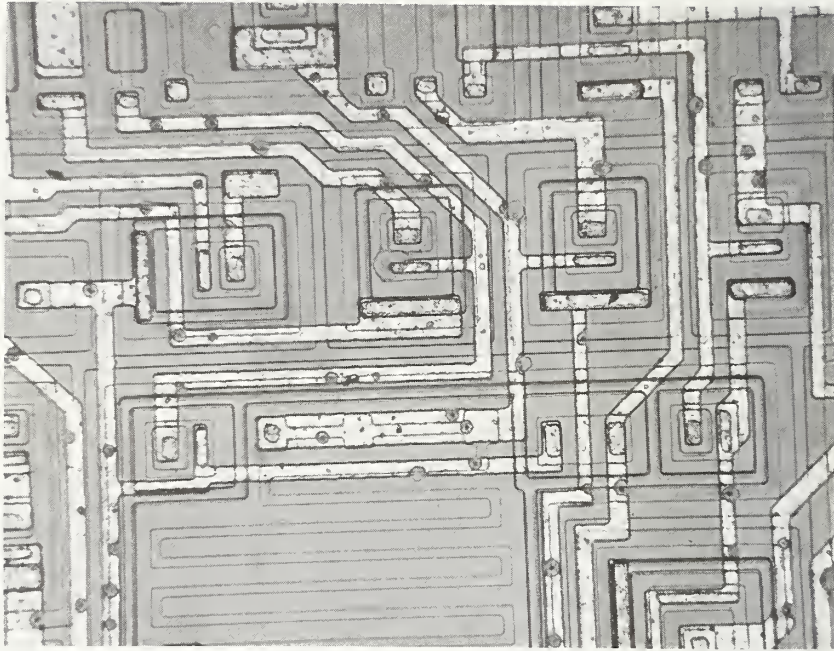


Figure 49. Sequentially metal/glass-etched aluminum-metallized and glass-passivated IC showing numerous pinholes that were opened on glass etching (150X).

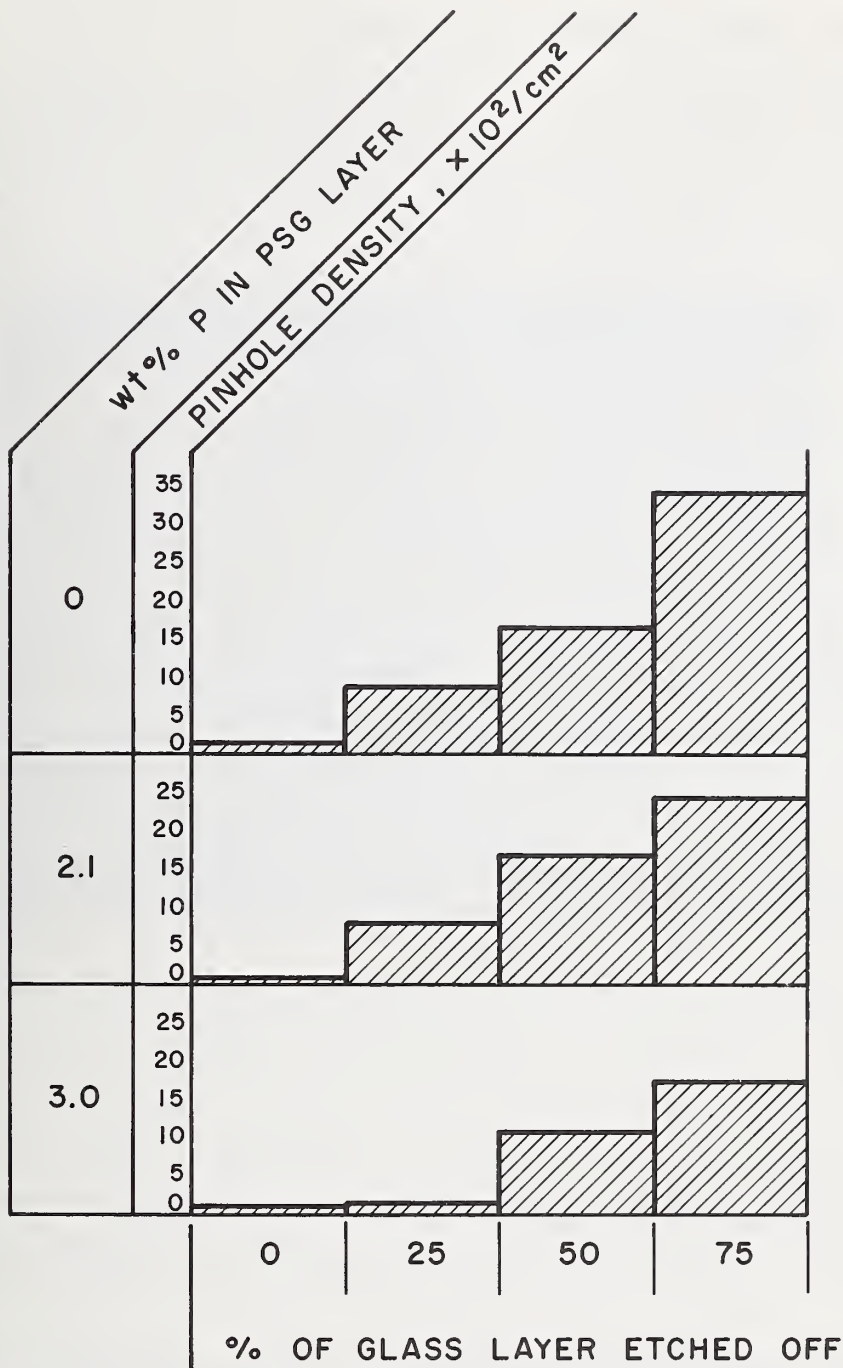


Figure 50. Density of open and partial pinholes as a function of glass composition and layer depth. Samples used were experimental aluminum-metallized ICs overcoated with 1.15- μm CVD SiO_2 or PSG. The residual layer thickness are 1.15, 0.86, 0.58, and 0.29 μm .

6.4 Direct Decoration by Corona Charging

Direct decoration by corona charging has been applied to bipolar and MOS type IC wafers, principally using uv phosphors; examples have been given in section 4.4.2. Defect detection by this method has also been accomplished on circuit boards. In this application, it was desired to find pinhole defects in a black resist material applied over electroless copper. A white powder (lead aluminosilicate glass) was used for direct decoration, and the white deposit on black field made the pinhole detection very easy. Glass powders have also been used to find defects in photoresist layers on power transistor wafers.

6.5 Reverse Decoration by Corona Charging

For reverse decoration, we have principally used carbon black since it results in very high contrast. Examples of this decoration on IC wafers have been shown in section 4.4.3. In addition, the process can find defects in passivation layers over devices on thick insulator substrates such as silicon on sapphire (SOS) IC wafers. An example is shown in figure 51. Thin layers (hundreds of angstroms) of glow discharge polymerized plastic coatings have various useful applications. Pinhole defects were found in layers of polystyrene formed in this manner. The deposited carbon layer was very thin, possibly because of the extremely thin polystyrene layer, and contrast was low. However, some defects could be observed.

The reverse carbon black method has been very useful in process studies (not a part of this contract). For example, stress in passivation layers was studied by observing the cracking induced by extreme heat treatments. This cracking, in some cases, occurred at the edges of large aluminum areas, as shown by carbon black decoration in figure 52(a). These edge cracks could not be found by aluminum etching for etch times up to 20 min. In addition, no evidence of the cracks could be found by SEM, as shown in figure 52(b). Thus, carbon black reverse decoration can find defects not detectable by etching nor by SEM. When these samples were given a buffered hydrofluoric acid etch for 10 s, which widened the cracks to about 2000 Å, it was possible to detect the cracks by aluminum etching and by SEM. The crack detected by SEM in figure 52(c) is at the lower edge of the passivation glass over the aluminum metal step.

Thermally grown MOS gate oxides have been reverse-decorated with carbon black. Defects were found and related to process variations.

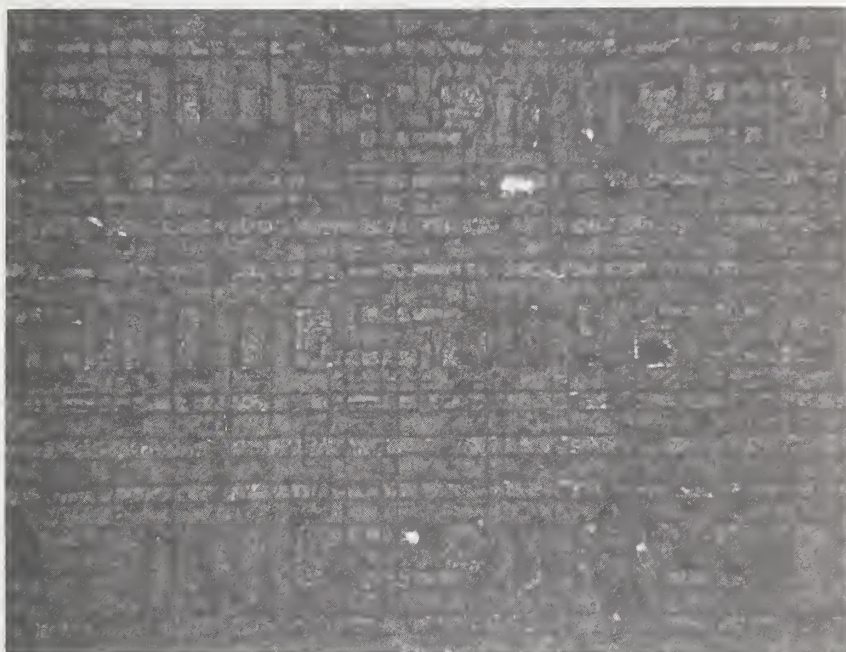
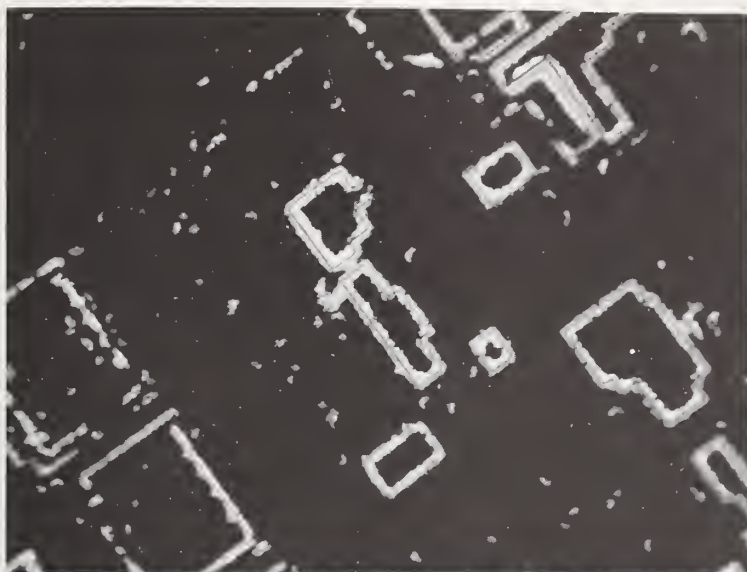


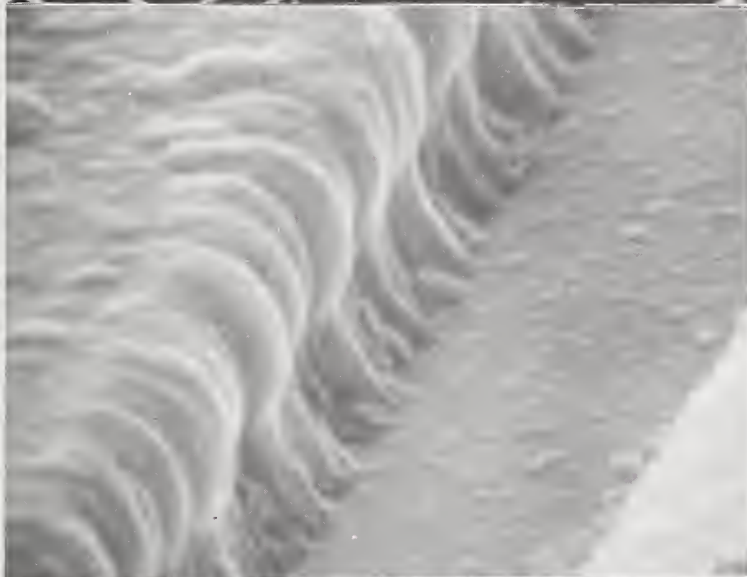
Figure 51. Carbon black deposited on CMOS SOS device wafer showing defects in passivation layer (385X, brightfield).

Figure 52. Example of cracking at edges of large aluminum areas due to extreme heat treatment.

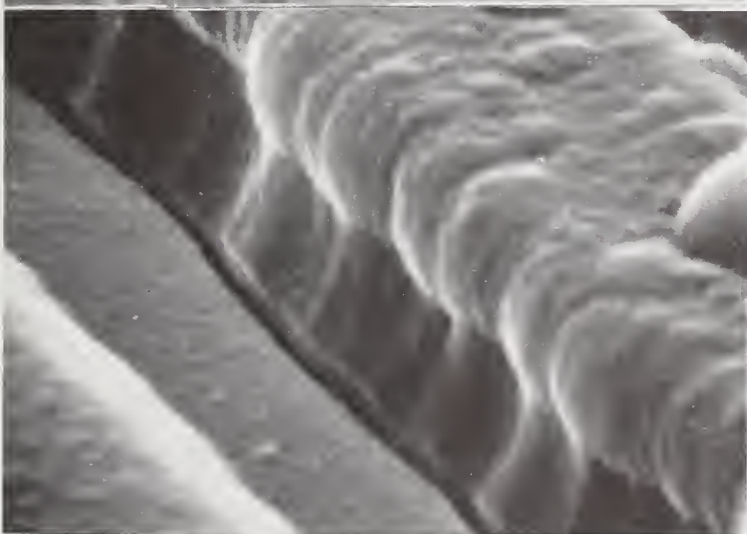
- (a)-Cracks outlined by carbon black (150X, brightfield),
- (b)-SEM cannot detect cracks (20,000X),
- (c)-After 10-s buffered hydrofluoric acid etching, the SEM does resolve the cracks (20,000X).



(a)



(b)



(c)

7. STANDARD PROCEDURES

Most of the procedural details have been noted and discussed in the body of this report. To facilitate use of the techniques, the various procedural steps and reagents are listed and referenced with the respective sections of the report.

7.1 Metal Demarcation Etching for Glassed Aluminum-Metallized ICs

7.1.1 Determination of the Aluminum Etching Time

Immerse the mounted IC device pellet or the IC wafer test piece in agitated aluminum standard etchant at $50 \pm 0.5^\circ\text{C}$ as noted in section 4.1.3. The etchant composition is given in table 1. Allow to etch until the exposed aluminum in the bonding pads of the device is just disappearing, as seen under the microscope. Depending on the thickness, this may take 1 to 3 min, since the etch rate is 150 Å/s. High accuracy is not required in estimating this time.

7.1.2 Demarcation Etching Time

An etch time factor (defined in section 4.1.5.3) of 1.25 is recommended for high defect densities, and a factor of 2.5 for low densities. Accordingly, continue etching to a total time of either 1.25 or 2.5X the aluminum etch time estimated in section 7.1.1.

7.1.3 Examination of Etched Sample

Rinse the sample in deionized water, blot dry, and examine under a microscope as described in section 4.5.1.

7.1.4 Determination of Defect Density

This procedure has been described in detail in section 4.5.1 for manual read-out, and in section 4.5.2 for instrumental measurement techniques.

7.2 Sequential Metal/Insulator Etching

7.2.1 Determination of the Aluminum Etching and Demarcation Etching Time

Proceed as outlined in sections 7.1.1 and 7.1.2. Then mask about 70 to 80% of the sample with an acid-resistant coating (such as a melted or dissolved wax or resin) in preparation for glass etch testing.

7.2.2 Determination of the Glass Overcoat Etching Time

Immerse the sample in ammonium fluoride-buffered hydrofluoric acid* at 25°C until the overcoat is etched off. The etch rate for CVD silicon

*392 cm³ 49% HF plus 2370 cm³ 40% NH₄F solution.

dioxide is usually about 90 Å/s. The etch rate for PSG varies, depending on the phosphorus content, but is usually in the range of 110 to 130 Å/s. Etching is continued until the interference color in incident white light under the microscope of the non-metallized device areas is the same as that of the bonding pads after the aluminum was etched off. This represents the dense silicon dioxide layer underneath the metallization. Further etching for short times will not materially change the interference color since the etch rate of thermal oxide is very much lower than those of CVD PSG or oxide.

7.2.3 Determination of Film Thicknesses

It is usually desirable, but not mandatory, to determine the aluminum and overcoat film thicknesses at this point. Stylus-type measurement techniques using etched steps produced by masking during the etching treatments described above are most convenient for this purpose. From the etching time and the film thicknesses, the etch rate can then be determined for PSG, from which the composition can be calculated as described elsewhere [5].

7.2.4 Sequential Etching Procedure

Depending on the objective, the overcoat etching can be performed in any number of steps. Usually, four or five steps are adequate to supply information on the distribution of defects as a function of layer thickness. Metal demarcation etching is carried out as described in section 7.1.2 as the first step to obtain the density of open defects. Overcoat etching is then carried out for a time period corresponding to either 1/4 or 1/5 of the total etch time, followed by another treatment of metal etching. Defect densities are determined after each pair of treatments, as described in section 4.5.1. Additional details of the procedure have been presented with the examples in section 4.2.

7.3 Electrophoretic and Corona Decoration Methods

Since the suspensions described here can be used for conventional electrophoretic decoration as well as for direct and reverse corona decoration, their preparation is described in this one section.

7.3.1 Phosphor and Glass Suspensions

First, a stock solution of OLOA 1200 (the preparation is described in section 4.3.4) is used to prepare the suspensions as follows. Add 1 ml of OLOA 1200 stock solution to 400 ml of $C_2Cl_3F_3$ and stir. Add 1-g zinc silicate (manganese) small-particle phosphor B and shake for 2 min in a jar.

For the lead aluminosilicate glass powder, best results are obtained by adding 10 ml of OLOA 1200 stock solution to 400-ml $C_2Cl_3F_3$; stir and add 8 g of the glass powder, and shake 2 min in a jar. In use, these (and any other) suspensions are slowly stirred by a magnetic bar.

7.3.2 Carbon Black Suspension

For this suspension, a concentrate is made (described in section 4.4.3.1), and added to $C_2Cl_3F_3$ at the ratio of 1 ml/400 ml, and stirred. In use, this suspension is also slowly stirred by a magnetic bar.

7.3.3 Equipment

The equipment for electrophoretic decoration was described in section 4.3.2. Corona-charging apparatus is described in section 4.4.1. The corona process is carried out in a glove box in flowing nitrogen with RH of about 25%.

7.3.4 Sample Preparation

Dust and other particles should be removed from samples by blowing with clean air or by distilled-water rinsing, followed by careful drying on a spinner or by rinsing in acetone followed by $C_2Cl_3F_3$.

It is required that the sample be grounded; thus, for wafers, it is sufficient to place the wafer on a grounded plate after ensuring that the reverse side is bare silicon. The normal native oxide is tolerable.

Chips are conveniently handled by fastening them to metal strips with conducting silver paste. Several can be processed at one time. For opened packaged devices, the lead frame and wire bonds will normally act to connect the silicon to ground. If necessary, the ground connection can be made by painting conducting silver paste from the chip edge to some region of the package which can be grounded.

Samples should be baked at 200°C for 5 min prior to placing them in the glove box for corona charging or prior to electrophoretic decoration. This is conveniently done on a hot plate (for wafers and chips) or in an oven for opened packaged devices.

7.3.5 Electrophoretic Process

For the glass suspensions, a deposition at 50 V for 8 min with 17-mm electrode spacing to sample gives good decoration with low background deposition. For the phosphor suspensions, good decoration with low background deposition is obtained at 25 to 50 V for 5 min with 17-mm electrode spacing to sample.

7.3.6 Corona Decoration Process

For direct defect decoration with phosphor or glass, charge sample negatively for 18 s with corona wires 20 cm from sample at -7000 V. After a 10-s delay, immerse sample in suspension for 10 s.

For reverse-defect decoration with carbon black, charge sample positively for 18 s with corona wires 2 cm from sample at +7000 V. After a 10-s delay, immerse wafers, and chips for 12 s, and opened packaged devices for 6 s.

For wafers or wafer sections which do not have bond pads etched open, a grid must be placed over the sample during charging. This grid was described in section 4.4.1.3.

7.3.7 Cleaning Procedure

The cleaning procedure has been described in section 4.4.4.

8. CONCLUSIONS

Major conclusions reached are briefly summarized below.

1. The method of selective metal etching to demarcate localized structural defects in dielectric overcoats has been demonstrated to be simple, effective, and sensitive. It is an absolute method but has the disadvantage of being destructive. It is used primarily in test applications where the sample can be sacrificed or where an absolute standard for comparison with other techniques is desired.
2. The sensitivity of the demarcation etching is influenced by the size of the defect opening. Microcracks in 1- μ m-thick PSG layers over aluminum can be detected down to widths of less than 500 Å. Extending the etch time further can additionally increase the sensitivity.
3. Sequential etching of metal/insulator structures is capable of detecting buried, latent, or partial defects within the dielectric overcoat. Determination of the defect density after each pair of etching treatments then provides the defect density as a function of dielectric or insulator layer depth. The method is reliable but time-consuming and destructive. It is recommended for testing applications in process research.
4. Numerous examples have been presented illustrating specific and general applications of the two selective etching methods.
5. Electrophoretic decoration technique can be used for defect detection and is particularly attractive when white powders or uv phosphors are used for examining relatively large defects. However, it is inferior to the corona methods.
6. Corona-charging methods are widely applicable and most attractive for general use. In particular, the carbon black reverse decoration method has been most useful in a variety of applications.
7. In general, the corona techniques are not destructive, are rapid, sensitive, and simple, and are capable of detecting certain partial or latent defects. The carbon black reverse decoration method can detect defects not found by aluminum etching nor by SEM, unless glass etching is first used to enlarge the defect. By comparison with etching, this technique has been shown to be very selective. Because of its high contrast, it is suitable for a simple form of wafer inspection automation.
8. Post-decoration device recovery procedures have been developed and proven to be effective. It has been shown that device yield is not decreased by carbon black decoration.

9. A good correlation has been shown to exist among the various methods developed under this contract. Advantages, disadvantages, limitations, sensitivity limits, and applicability of each have been pointed out and demonstrated experimentally in many instances.
10. The population density of demarcation-etched defects is readily determinable by microscopic read-out techniques with or without photomicrographic recording.
11. The population density of decorated defects can be quantified by microscopic techniques combined with reflected light measurements. It is possible to automate this type of read-out technique on a step-and-repeat basis, using automatic and computerized instrumental recording of the data.
12. The methods that have been described were developed and refined specifically for the evaluation of dielectric overcoats on aluminum-metallized ICs. We have shown, however, that these methods are also applicable for analyzing other metal/dielectric structures and devices and, in fact, for the evaluation of insulator coatings in general.
13. The availability of a well-defined, practical test method for evaluating the integrity of IC passivating overcoats now offers device manufacturers a much needed tool for controlling their products during fabrication. Since the recommended techniques are nondestructive, a 100 percent quality control is feasible on the device wafer level. It will make it possible to reprocess defective wafers at this point rather than continue their processing, thus eliminating very large potential losses that would be caused by completing defective material into finished IC devices.
14. More importantly, these expedient, sensitive, and nondestructive test methods make it possible to establish a rapid information feedback of the test results to the production line and allow immediate correction of faulty processing conditions. In addition to being an early, rapid detection system for defects occurring on the production line, the new test methods are a valuable tool for assessing developmental studies for improving materials and processes.
15. The methods developed and perfected during this program also make it possible to test finished IC devices by the manufacturer, or by the procurement agency or individual customer company, and allow a reasonable degree of presently nonexistent standardization of the integrity of overcoat passivation layers on finished IC products.
16. In summary, the practical benefits of the new test methods are very considerable when applied to production and product control, both in terms of cost savings due to early detection of production line defects and rapid information feedback for corrective action.

Batch removal and batch processing of defective material in wafer form will be an additional cost-saving factor.

17. Major parts of the information presented in this report have been presented elsewhere [37,38].

9. RECOMMENDATIONS FOR FUTURE WORK

Following the successful completion of the 12-month program discussed in this final report, we recommend that some additional research work be considered in certain areas that merit additional effort. The main objectives of this effort would be: (1) to extend the new methods for defect detection to important additional applications, (2) to conduct further studies of the mechanism governing the new method of reverse decoration, (3) to apply the refined methods to a critical examination and analysis of currently manufactured commercial integrated circuits, and (4) to explore the general applicability of the new measuring methods for evaluating the structural integrity of both inorganic and organic dielectric films of all types. Some proposed experimental details for each of these objectives are presented below.

9.1 Extending the Applicability of the New Measuring Methods

The methods developed during the present contract period have been concerned almost exclusively with aluminum-metallized ICs overcoated with CVD silicon dioxide or phosphosilicate glass. Low-temperature deposited silicon nitride layers appear to be feasible for passivation of aluminum- and gold-metallized IC wafers. When these films are deposited under suitable conditions, they can effectively serve as a moisture barrier and as an alkali ion barrier. Low-temperature silicon nitride films have been deposited by plasma deposition techniques, by reactive sputtering, and by photochemical deposition techniques. At least one IC manufacturer is, at present, producing and marketing silicon devices passivated by these systems, and more semiconductor products of this type will most certainly become available in the near future. We therefore propose that the applicability of our test methods to devices metallized with gold and/or passivated with silicon nitride overcoat layers be examined in detail and optimized for maximum performance and sensitivity.

Devices passivated with low-temperature aluminum oxide should also be studied since aluminum oxide films, like silicon nitride films, can be effective alkali barriers and can also serve as a moisture barrier when deposited under suitable conditions, with potential cost and adhesion advantages compared with low-temperature-deposited silicon nitride films.

Certain ICs (such as PMOS types) employ polycrystalline silicon as first-level metallization material, and fused CVD phosphosilicate glass as a tapered dielectric. Application of our test methods to such devices would be of interest and could be examined for determining edge coverage quality and certain structural defects associated with multi-level LSI circuits.

9.2 Mechanism of Reverse Decoration

The new method of reverse decoration based on corona charging and electrophoretic deposition of carbon black is an extremely powerful tool

for dielectric defect detection, as we have just demonstrated. Further studies of the mechanism of this process would be desirable in order to make additional methodological improvement feasible. For example, the relationship of the diameter of the bare regions surrounding a decorated point defect and the test conditions should be ascertained. Specifically, the effects of humidity, temperature, corona-charging voltage, surface impurities, and dielectric composition on the bare area must be assessed. Optimization of these parameters can be expected to enhance the resolution and detection sensitivity of the method considerably.

9.3 Critical Examination of Commercial ICs

A survey should be conducted of the structural quality of presently available commercial ICs with respect to passivation overcoats. The methods for analysis of single IC pellets will be utilized in this work, both as a demonstration of its applicability and to gain useful data on the degree of perfection of passivation overcoats now being produced by various device manufacturers.

9.4 Applicability to Inorganic and Organic Dielectric Film Evaluation in Various Technological Fields

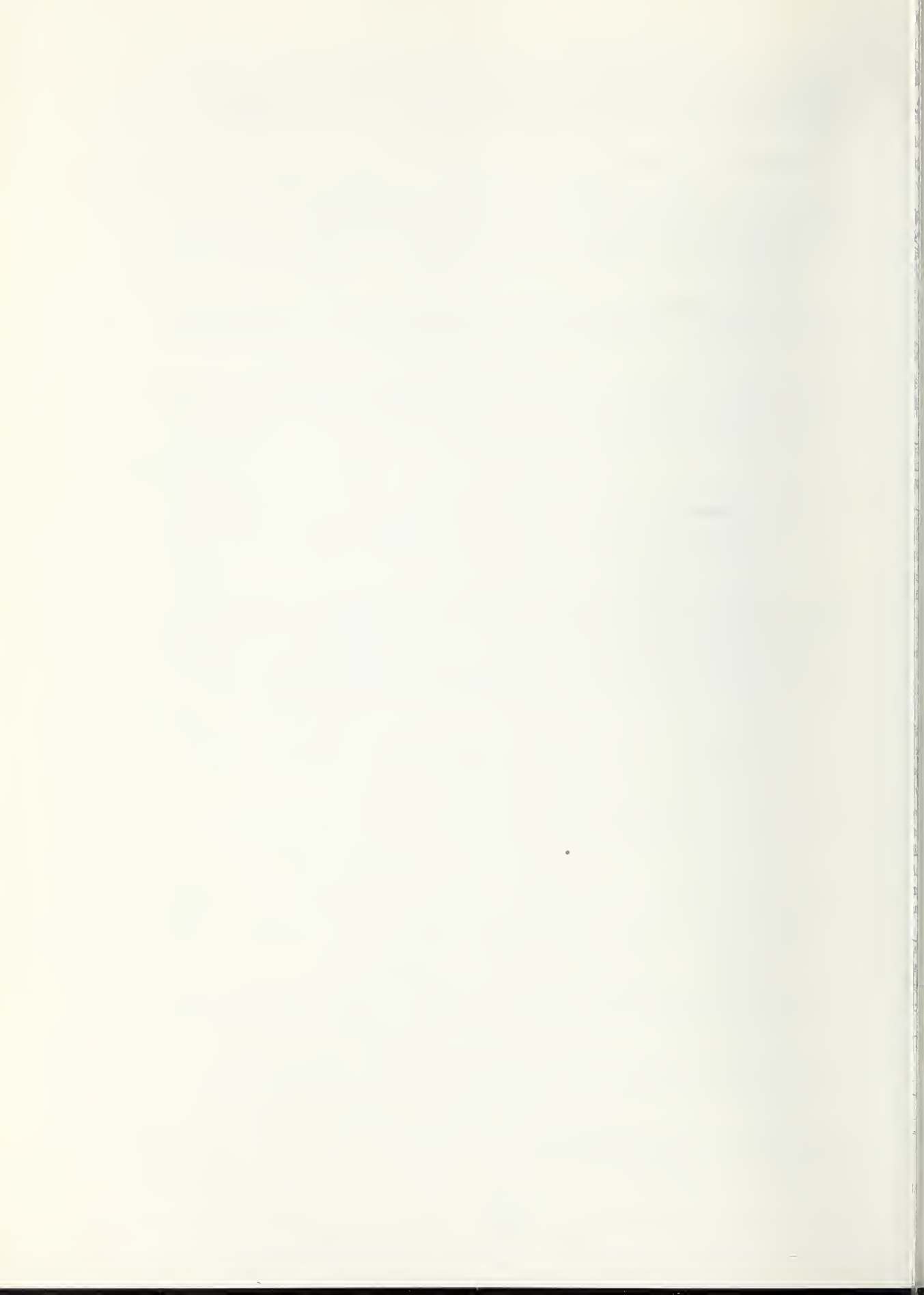
A survey and feasibility study aimed at a broad application of the methods for evaluating both inorganic and organic dielectric coatings would be of great value. For example, testing of the integrity of photopolymer films used in precision photolithography is one good example. Anticorrosion protective coatings on metals is another example. The examination of primary passivation layers on silicon offers a natural extension for applying the methods. Testing of the integrity and edge coverage of fused CVD PSG overcoat layers on multilevel LSI is another important application where the principles discussed may be usefully employed. In this particular example a selective etchant for polycrystalline silicon may have to be devised that does not attack the glass passivation.

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