NBS SPECIAL PUBLICATION 400-3

Semiconductor Measurement Technology:

ARPA/NBS Workshop I. Measurement Problems in Integrated Circuit Processing and Assembly

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[1] Headquarters and Laboratories at Gaithersburg, Maryland, unless otherwise noted; mailing address Washington, D.C. 20234.
[2] Part of the Center for Radiation Research.
[3] Located at Boulder, Colorado 80302.
[4] Part of the Center for Building Technology.

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PREFACE

The Semiconductor Technology Program serves to focus NBS efforts to enhance the performance, interchangeability, and reliability of discrete semiconductor devices and integrated circuits through improvements in measurement technology for use in controlling device fabrication processes and in specifying materials and devices in national and international commerce. Its major thrusts are the development of carefully-evaluated and well-documented test procedures and associated technology for use on production lines, and the dissemination of such information to the electronics community. Application of the output by industry is expected to contribute to higher yields, lower cost, and higher reliability of semiconductor devices. In addition, the improvements in measurement technology will lead to greater economy in government procurement and will provide a basis for controlled improvements in fabrication processes and in essential device characteristics.

The Program receives direct financial support principally from three major sponsors: the Defense Advanced Research Projects Agency (ARPA),* the Defense Nuclear Agency (DNA),† and the National Bureau of Standards (NBS).× The ARPA-supported portion of the Program, Advancement of Reliability, Processing, and Automation for Integrated Circuits with the National Bureau of Standards (ARPA/IC/NBS), addresses critical Defense Department problems in the yield, reliability, and availability of integrated circuits. The DNA-supported portion of the Program emphasizes aspects of the work which relate to radiation response of electron devices for use in military systems. There is considerable overlap between the interests of DNA and ARPA and both interests parallel the measurement-oriented mission of the NBS.

Cooperation with industrial users and suppliers of semiconductor devices is achieved through NBS participation in standardizing organizations; through direct consultations with device and material suppliers, government agencies, and other users; and through periodically scheduled symposia and workshops. This report describes the results of the first workshop in this series which was an activity of the ARPA/IC/NBS program.

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Measurement Problems in Integrated Circuit Processing and Assembly

by

Harry A. Schafft

The dual purpose of the workshop was (1) to announce and describe the new effort, "Advancement of Reliability, Processing, and Automation for Integrated Circuits with the National Bureau of Standards," sponsored by the Defense Advanced Research Projects Agency (ARPA), and (2) to obtain additional input on critical measurement problems in integrated circuit processing and assembly to assist in planning future work in the effort. More than 130 engineers representing 61 organizations from the electronics industry and government participated in the workshop. The measurement problems in silicon, oxides, photolithography, and assembly and the problems in information dissemination that were identified by the participants are summarized. Included as appendices are summaries of two talks given: one which described the results of earlier direct contacts with a cross section of industrial representatives on major measurement problems in integrated circuit processing and assembly and the other which described the initial plans for work in the new effort.

Key Words: Die bonding; hermeticity; integrated circuits; measurement methods; microelectronics; oxides; photolithography; process control; reliability; semiconductor devices; silicon; wire bonding.

Introduction

The first workshop under the new effort, Advancement of Reliability, Processing, and Automation for Integrated Circuits with the National Bureau of Standards, sponsored by the Defense Advanced Research Projects Agency (ARPA), was held on September 7, 1973, in Palo Alto, California. The dual purpose of this ARPA/NBS workshop was to announce the start of the new effort and to supplement input obtained from earlier direct contacts with a cross section of industrial representatives on the major measurement needs for improved control of process and assembly procedures for integrated circuits. A total of 137 scientists and engineers representing 61 organizations attended.

first workshop

purpose of workshop

The new effort is being developed in concert with the reliability laboratories of the three military services. The major thrusts of the effort are the development of well-documented test procedures and measurement technology for use on semiconductor devices production lines and the dissemination of such information to the electronics community. A feature of the effort will be the contracting of selected work to industrial, university, government, and independent research laboratories. Application of the output of the program by industry is expected to contribute to higher yields, lower cost, higher reliability, and greater availability of special

major thrusts of effort

contract work

goals

Semiconductor Technology Program

devices such as those needed by the Department of Defense. This effort is part of the NBS Semiconductor Technology Program which is described briefly in Appendix 1.

Morning Session

rationale for effort

During the morning session, Dr. C. M. Stickley, Director of ARPA's Materials Sciences Office, outlined the rationale for a new program which is intended to make it possible for the Defense Department to obtain in the future the large-scale integrated circuits that it needs to meet its specialized applications with low-volume purchases at acceptable costs and reliability. He pointed out that the cost to the Department of Defense for electronics equipment maintenance alone is reported to be five billion dollars yearly. The long term goal is to reduce these costs through enhanced integrated circuit reliability. As a new thrust of the Department of Defense to this goal, the ARPA/NBS effort will be concentrated in process understanding and control. Dr. Stickley described the role of NBS as primary agent for the five-year effort.

aims of effort

NBS approach

Representing the NBS Electronic Technology Division, where the effort is to be conducted, J. C. French described the Division's involvement in and approach to measurement methods in the area of semiconductor technology, H. A. Schafft discussed the results of field visits made to identify major measurement problems in process and assembly control that interfere with achieving greater yield and reliability, and W. M. Bullis outlined plans for the various technical areas to be covered in the development of improved measurement methods and associated technology for controlling and automating key processing and assembly procedures. Summaries of the talks given by H. A. Schafft and W. M. Bullis are included in Appendices 2 and 3, respectively.

field visits

plans

Appendices

Afternoon Session

problem areas

In the afternoon, discussion groups met to identify non-proprietary measurement problems related to silicon, oxides, photolithography, and assembly and problems of information dissemination for consideration in planning work in the ARPA/NBS effort. In general, the input from these groups and the workshop as a whole corroborated the findings obtained from earlier direct contacts and reviewed by H. A. Schafft in the morning session. Two variances were noted, however. There appears to be greater interest in the use of test patterns for silicon process control and in tests for metallization step coverage than was indicated in consultations made earlier in the year with representatives of the electronics community.

corroboration

variances

The measurement needs expressed by the discussion groups are summarized in the following paragraphs:

Silicon

Measurements of thickness and resistivity of thin (<2 μm) epitaxial layers were singled out as the greatest need; adequate techniques for these measurements do not now exist. Other high priority areas mentioned were methods for determining impurity profiles, particularly in the base region of bipolar transistors, and rapid methods for inspecting wafers and other materials for particulate contamination which could cause defects to be introduced during growth of epitaxial films.

thickness measurement

profiles

particular contamination

The usefulness of test patterns for determining impurity profiles in the base region was widely recognized. However, it was emphasized particularly in the case of small-geometry devices that test patterns may not adequately reflect the true characteristics; in fact, it was noted that the device itself makes the best test vehicle, if it is accessible.

test patterns

A problem noted in connection with the use of test patterns was associated with the large volume of data which must be acquired and analyzed. Automated procedures and standardized reporting formats would be welcomed.

automated procedures

Other problem areas identified where measurement procedures need improvement were characterization of swirl defects, determination of surface flatness before and during processing, and evaluation of resistivity homogeneity on both microscopic and macroscopic scales.

defects, flatness, inhomogeneities

There was much discussion of the relationship between the properties of silicon and device reliability. There was general agreement that it was nearly impossible to ascribe the causes of failed devices to silicon defects. However, because the characteristics of a device can be more accurately predicted if the parameter distributions are narrow, the ability to control all processes, including wafer fabrication does impact device reliability. To this end, rapid and simple measurements of appropriate accuracy and precision are required at many points.

process control and reliability

Oxides

Although a number of problem areas were discussed by the oxide group, it had difficulty in defining specific measurement needs. Oxide stability is of considerable concern. The bias-time-temperature stress tests are commonly used to test stability of oxides but there is great variability in the stress conditions used, even within a given company. While the needs for standardizing the stress conditions and for more quantitative tests of stability were implicit, no specific mention of such needs was expressed. Another area of considerable concern is in regard to assuring that contact windows are free of oxides and photoresist; oxides are the primary concern. While it is common to over-etch somewhat in an attempt to remove all residues, this procedure is

tests for oxide stability

tests for oxide removal

not always successful. Therefore there is a need for an inspection method that can be used immediately after the etching procedure to detect the presence of any oxide or other residues in contact windows.

thickness standards?

The control and rapid measurement of oxide thickness is of moderate concern. A number of methods are used to measure oxide thickness; a common method is to use interference colors. The use of standard oxide films of specific thickness was felt by the group to be impractical because of problems experienced with oxide film instabilities.

test patterns

The use of test patterns was discussed and the group concluded that the device itself is ultimately the best test pattern. The problems with handling and interpreting the data from test patterns mentioned in the silicon group were repeated in this group.

Photolithography

mask inspection vs. photoresists

Problems with mask inspection were considered to be more critical than those with photoresists. This is because more time and material are apt to have been invested before a defective mask is detected and replaced than if a problem with photoresist is discovered.

mask inspection

Therefore, of primary concern was the need to improve the methods for inspecting glass masks for defects and dimensional correctness. Specifically there is a need for a method to detect automatically the location and number of mask imperfections, such as pin holes, and to provide a quantitative measure of mask quality. Methods are needed to measure both linear and angular dimensions. Methods for linear dimensions should be capable of measuring lengths of up to 3 inches (7.6 cm) with an accuracy of ±20 μin. (0.5 μm). Referee methods are needed to establish the degree of registration between levels of a mask set and to measure both die and array dimensional errors ["runout"].

photoresist bibliography

It was felt that because the photoresist literature is so extensive and scattered in many journals, it would be extremely useful if NBS could compile a bibliography of work done in the field. This would then facilitate an awareness of at least what work has been done.

photoresist characterization and use

Many information deficiencies in the characterization and use of photoresist are felt to exist. Paramount is the need to determine the interrelation of the physical properties of the photoresist material, such as specific gravity, viscosity, and solids content, with the properties of the photoresist film, such as resolution, etch resistance, and adhesion. Also, concern was expressed about how developers, thinners, and impurities can affect the properties of the photoresist film and its removal. Specific problems were mentioned with regard to defining and measuring the photosensitivity and cleanliness of photoresists. While processes can be altered to compensate for different levels of cleanliness no quantitative procedures appear to be available.

There is also a critical need for light standards for use in controlling and in assuring constancy of the exposure of photoresist films. Problems exist with aging of the lamps used to illuminate photoresists.

light standards

Finally, interest was expressed in the need for research in electron beam lithography, in general, and in particular for range-straggle information for ions and electrons in metals, polymers, and semiconductors because of the growing use of ion implantation and electron beam lithography.

electron beam lithography

Assembly

Concerns were expressed in three areas: bonding, packaging, and hermeticity.

In wire bonding there is a need for 100% testing for bond integrity to eliminate random, weak wire bonds. Tests for the bondability of wires and metallizations are also needed to avoid the more systematic bonding problems that are encountered. Tests for surface cleanliness were of particular interest because dirty metal was felt to be responsible for many bonding problems. To isolate problems associated with the bonding machine itself, a need was expressed for a test surface to which wires could be bonded.

wire bonding

A strong desire was expressed to have NBS disseminate information and make available surveys on bonding. In particular, a manual on procedures for bonding and the characteristics of materials used in bonding was desired.

bonding surveys and manuals

Discussions devoted to die bond problems were directed primarily to the importance of having methods for determining the purity and bondability of materials used in the die bond.

die bonding

In packaging there is a need to develop methods to characterize package materials, particularly of glass-frit ceramic packages, to assure package consistency. Problems were mentioned in methods for determining the quality of glasses, the retention of the binders, and the detection of voids. Furthermore, while there is a desire for a "high-reliability" package, there is no clear concept of how to define such a package nor how to test and evaluate it. Additionally, there is generally poor communication between the suppliers and users of packages in regard to their respective needs.

packages

In hermeticity there is a need to evaluate the capabilities of the methods used in order to obtain assurance in the measurements made and to be able to intercompare methods. Also there is a need to correlate the

hermeticity

penetration of moisture and other undesirable vapors into the package with the measured leak rates for tracer gases used and therefrom determine needs for leak rate rejection levels.

Information Dissemination

information proliferation

It was unanimously agreed that the proliferation of information in the semiconductor electronics field is a very serious problem. There is a desperate need to order, evaluate, and disseminate information that already exists. This need was corroborated in the other discussion groups. Filling in the gaps of information, although very significant appeared to be of secondary importance.

NBS role

It was proposed that NBS could play a valuable role in addressing this need by serving as a center for collecting information and distributing it in usable form. Publications which the group thought to be most widely read by the engineering community were discussed.

vehicles for dissemination

Vehicles for disseminating information were discussed. Bibliographies, reviews, and state-of-the-art surveys which are periodically updated are needed. Workshops and other meetings were felt also to be useful.

meetings

Meetings involving primarily information input and exchange on a particular topic should include experts by invitation; the location of these meetings was not considered to be overly important. However, meetings involving primarily information output require care in the selection of the meeting location to maximize the number of people reached. With regard to the latter meeting type it was suggested that NBS explore the use of video tape presentations with an expert in attendance to answer questions.

Acknowledgement

The efforts of the many people involved in this workshop are acknowledged here with pleasure. The following acted as discussion group leaders during the afternoon session and provided me with summary statements on the results of their respective groups which were used in the preparation of this report: James R. Ehrstein and W. Murray Bullis for the silicon group, Martin G. Buehler and Willie E. Phillips for the oxide group, Thomas F. Leedy and Donald B. Novotny for the photolithography group, George G. Harman and Stanley Ruthberg for the assembly group, and David L. Blackburn for the information dissemination group. Behind the scenes but vitally important to the success of the workshop were the efforts of Kathryn O. Leedy who played a major role in the publicity and preparations for the workshop and in the operation of the workshop itself. Also involved in this work were Charles P. Marsden, Bonnie S. Hope, and David C. Lewis. Thanks go to C. Martin Stickley, Judson C. French, and W. Murray Bullis for their talks in the morning session which helped set the stage for the afternoon group discussions. Finally, thanks go out to the attendees who with their active participation made it the useful and interesting workshop that it was.

My special thanks go to Marilyn L. Stream who typed the camera-copy draft.

Appendix 1

THE SEMICONDUCTOR TECHNOLOGY PROGRAM

in the

Electronic Technology Division
Institute for Applied Technology
National Bureau of Standards
Washington, D. C. 20234

PROGRAM OBJECTIVES

The Semiconductor Technology Program serves to focus NBS efforts to enhance the performance, interchangeability, and reliability of discrete semiconductor devices and integrated circuits through improvements in measurement technology for use in controlling device fabrication processes and in specifying materials and devices in national and international commerce. Its major thrusts are the development of carefully-evaluated and well-documented test procedures and associated technology for use on production lines, and the dissemination of such information to the electronics community. Application of the output by industry is expected to contribute to higher yields, lower cost, and higher reliability of semiconductor devices. In addition, measurement technology will provide a basis for controlled improvements in fabrication processes and in essential device characteristics, such as uniformity of response to radiation effects.

SPONSORS

The Program receives direct financial support principally from three major sponsors: the Defense Advanced Research Projects Agency (ARPA), the Defense Nuclear Agency (DNA), and the National Bureau of Standards (NBS). The ARPA-supported portion of the Program addresses critical Defense Department problems in the yield, reliability, and availability of integrated circuits. The DNA-supported portion of the Program emphasizes aspects of the work which relate to assurance of radiation hardness of electron devices for use in military systems. There is considerable overlap between the interests of DNA and ARPA, and both interests parallel the measurement-oriented mission of NBS.

INDUSTRY TIES

Cooperation with industrial users and suppliers of semiconductor devices is achieved through NBS participation in standardizing organizations; through direct consultations with device and material suppliers, government agencies, and other users; and through periodically scheduled symposia and workshops. New ties to the industry will develop through the contracting out of selected parts of the program activity. Direct input from these contracts is expected to augment the valuable assistance that has traditionally been received from the industry through cooperative experiments and technical exchanges.

REPORTS

Progress reports are regularly prepared by the Electronic Technology Division for issuance as NBS Special Publications under the new title Semiconductor Measurement Technology, continuing the series of reports issued as NBS Technical Notes during the past five years. More detailed reports such as state-of-the-art reviews, literature compilations, and summaries of technical efforts conducted within the Program are issued as these activities are completed.

Selected Activities in the Semiconductor Technology Program

MATERIALS

- STANDARD WAFERS FOR FOUR-PROBE RESISTIVITY
- SPREADING RESISTANCE MEASUREMENTS
- CAPACITANCE-VOLTAGE MEASUREMENTS
- THERMALLY STIMULATED CURRENT AND CAPACITANCE
- INFRARED RESPONSE MEASUREMENTS
- CHARACTERIZATION OF GOLD-DOPED SILICON
- CARRIER LIFETIME
- OXIDE AND INTERFACE STATE CHARACTERIZATION

PROCESS CONTROL

- TEST PATTERNS FOR PROCESS CONTROL
- PHOTORESIST MEASUREMENTS
- MASK INSPECTION
- BEAM LEAD AND WIRE BOND EVALUATION
- DIE ATTACHMENT EVALUATION
- HERMETICITY

DEVICES

- SCANNING ELECTRON MICROSCOPY
- THERMAL RESISTANCE AND THERMAL RESPONSE
- HOT SPOT DETECTION
- MICROWAVE MIXER DIODE EVALUATION
- NUCLEAR RADIATION DETECTORS
- CONTROLS AND SCREENS FOR HARDNESS ASSURANCE

- STANDARDIZATION ACTIVITIES
- SEMINARS AND WORKSHOPS
- TECHNICAL CONSULTATION

Appendix 2

Process- and Assembly-Control Problems and Measurement Needs

by

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To assist in the selection of activities to be undertaken in the ARPA/NBS effort, initial consultations were completed with representatives of the electronics community to identify the more important measurement problems in process control for silicon wafer fabrication and device assembly primarily of bipolar and MOS digital integrated circuits. These consultations were made during visits to ten device manufacturing companies and one private research organization where discussions were conducted with a total of almost 100 technical people. source of review

The generalized need expressed by many of the respondents was for more nondestructive, direct, and rapid production-type methods for measurement in order to reduce the appreciable number of silicon slices that would have to be sacrificed if all the necessary measurements were to be made, to avoid the need to infer product characteristics from tests on sample silicon slices, and to provide the faster feedback necessary to allow the desired degree of control on the production line. general needs

The most critical measurement needs identified during the visits are ranked and reviewed briefly in the following paragraphs. The relative importance of the problem areas identified was gauged according to the number of organizations that mentioned the area as being important and the degree of interest or ranking that was indicated by the respondents. ranking criteria

Process control measurement problems of primary concern are with: (1) the starting silicon material in regard to defects and resistivity; (2) silicon diffused and epitaxial layers in regard to thickness, doping profiles, and sheet resistivity; (3) oxide films in regard to stability and impurities; (4) photolithographic and associated procedures in regard to mask inspection, photoresist materials and their use, and pin holes; and (5) hermeticity. five areas of primary concern silicon — defects

With regard to the starting silicon material and silicon layers there are a number of problem areas that were mentioned. There is a general need for improved methods for detecting and characterizing defects and contaminants, and for determining the effect they have on device yield and reliability. Among the defects mentioned were swirling patterns of vacancies, crystallographic defects, ion-implantation-induced defects, defects in epitaxial material, and back-lap defects.

silicon — resistivity profiles

Improvements in the measurement of resistivity of bulk silicon and of diffused and epitaxial silicon layers and in the measurement of resistivity profiles of these layers were of broad interest. A number of organizations expressed concern about resistivity inhomogeneities in silicon slices and the need for adequate methods for measuring them. Concerns were also expressed about the correction factors used with the spreading resistance method, about insufficient reproducibility of the four-probe method on a routine basis, and about the problems associated with the use of the four-probe method for measuring thin epitaxial layers. Those using the capacitance-voltage method for measuring profiles were generally not satisfied with the method.

epi thickness, junction depth

Much concern was expressed in most of the organizations about the inadequacy of the methods for measuring junction depth and epitaxial film thickness. The concern is most acute for layers less than about 1 μm thick, which are now being more widely used. While many use the lap-and-stain method, no one expressed satisfaction with this method. Complaints about the need to interpolate between fringes and the difficulty of staining, especially for thin layers, were common. Problems mentioned with nondestructive methods employing infrared interferometry involved insufficient sensitivity and precision, inability to make quantitative measurements on epitaxial layers over buried layers because of out-diffusion, and inability to measure epitaxial layer thicknesses less than about 1 μm.

oxide characterization

A strong need was expressed for improved means for characterizing oxides in MOS devices. Dissatisfaction with the capacitance-voltage method used to test for oxide stability was widespread. A typical comment was that the method could not be used to identify the reason for oxide instability. Some felt the method to be too slow and others felt it to be insufficiently sensitive to the level of impurities encountered that would have an effect on stability. Many felt that there should be a standard method for judging oxide stability by specifying temperature-bias-time stress conditions and the allowed shift in threshold voltage as a result of these stresses. Fewer expressed a need to have adequate means of determining the kinds and levels of impurities that can lead to instability.

photolithography

Great interest was expressed in the need for improved control of the photolithographic and associated procedures. There was a general and strong need to have a better means of inspecting photomasks. Present visual inspection methods are inadequate because of the time needed to make the inspection, the operator subjectivity, and the inability to detect all defects. The inability to detect random defects is of particular concern. It is felt that better inspection methods would significantly improve yield.

mask inspection

Great concern was expressed over the need to improve the methods for characterizing photoresist materials and photoresist films in use-type tests. Needs varied from knowing what characteristics to measure to how to measure these characteristics. Also, many were frustrated about the inadequacy of their methods for calibrating and determining the uniformity of the light used in photoresist exposure.

photoresists

On the slice itself there is a desire to detect smaller pin holes (or defects) and potential pin holes, and to do this by nondestructive means if possible. Also, an often expressed need was one of being able to even define what a pin hole is.

pin holes

Still another problem is the disagreement of the filar eyepiece and the double image shear methods for measuring oxide window dimensions, line width and line separation on the mask and slice. Some suggested the need for length standards that could be used for calibration purposes to resolve the differences.

length measurements

While control of the various assembly procedures is important to yield and reliability, and processes such as die attachment and wire bonding continue to be of major importance, the problems with hermeticity testing appear to be particularly frustrating to many in the industry. Common complaints are: the lack of agreement between the helium leak detector and the radioisotope methods and the problems that ensue at the vendor-user interface; the lack of adequate leak-rate standards; and the subjectivity of the bubble test for detecting large leaks.

assembly

hermeticity

There are a number of other problem areas of somewhat less relative importance by virtue of the smaller number of times they were mentioned. These process control measurement problems are in the control of incoming materials, ion implantation processes, and surface cleanliness.

three areas of moderate concern

With regard to incoming materials there is a need for fast, production-line methods to test for impurities in acids, solvents, dopants, etc. In general, there is the additional problem of not knowing which impurities may have a potentially harmful effect on device yield and reliability and at what concentrations. Maintenance of piece-part quality is also a common problem.

incoming materials

ion implantation

Of the organizations involved in the use of ion implantation, there is the commonly expressed need to improve methods for monitoring and controlling the number and uniformity of the ions implanted.

surface cleanliness

Finally, there is no satisfactory method for the production line that can determine if selected localized areas on the device slice are sufficiently clean and free of residues for metallization deposition or for wire bonding.

other areas mentioned

The following measurement areas were also mentioned: temperature in epitaxial reactors and diffusion furnaces; gas flow rates; metallization and oxide thickness; phosphorus concentration in glass overcoats; dielectric breakdown characteristics of oxides; characteristics of silicon nitride layers; wafer warpage; metallization step coverage; and test pattern usage.

Initial Plans for the ARPA/NBS Program

by

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preliminary and planning phase

A preliminary and planning phase of the new program was undertaken early this year. Principal emphasis during this period was placed on selection of task areas to be undertaken at the beginning of the program and on formulation of specific objectives for these areas. This was accomplished through field visits to over 25 groups in industry, government, universities, and research institutes; contacts with or visits from more than 10 other such groups; intensive review of ongoing project activities; work with the Quality and Hardness Assurance Subcommittee of ASTM Committee F-1 on Electronics; and review of recommendations developed in related studies by other organizations, such as the Navy program on Integrated Circuit Reliability and Manufacturing Science.

formulation of task areas

The information developed in these various activities was combined with past experience to formulate the initial program task areas. These areas fall generally into two classes: One class consists of ongoing or new areas in which the needs are well defined and the resouces are on hand or soon to become available so that significant output can be anticipated during the first year, whether through in-house or contracted efforts. The second class consists of areas where the broad need is apparent but the details are not. In these areas, further definition of the specific work to be undertaken remains to be completed. This definition may be done in-house, by contract, or both ways.

specific task areas

Specific task areas are listed below together with a brief discussion of the approach and an indication of the progress expected to be made during fiscal year 1974. The ordering of the tasks in the list follows the progression from raw materials to final assembly; it should not be taken as an indication of priority.

resistivity

Resistivity; Dopant Characterization — Dopant atoms are intentionally added to semiconductor materials to control the electrical properties and to form device structures. The resistivity, usually measured by the four-probe method, which is the basic electrical parameter by which semiconductor materials are specified, is governed directly by the density of dopant atoms. To assist the industry in further improving the measurement of resistivity, standard reference wafers with provisionally certified resistivity values were developed, with partial support from the NBS Standard Reference Materials Program, for sale to the industry. Experimental efforts will be undertaken to determine the stability of these standards and to establish a basis for the full certification of each standard wafer. This will be a voluntary, cooperative effort with selected owners of standard wafers; the industrial portion will be undertaken at no cost to the government. Recently considerable interest has developed in the industry with regard to updating and improving the relationships between resistivity and dopant density particularly in specific ranges where existing information appears to be suspect. To this end, a review of the available data will be undertaken; this may lead to initiation of a redetermination of resistivity and carrier mobility in silicon as a function of dopant density later in the year. Knowledge of doping densities in thin epitaxial, diffused, or implanted semiconductor layers is critical to the control and understanding of device performance. Frequently it is necessary to know the density profile as a function of position within the layer. Work on several methods appropriate to these measurements has been underway; efforts will be concentrated on evaluating and comparing the spreading resistance and junction capacitance-voltage methods. To support the above activities an expanded mathematical study of the dopant profiles resulting from diffusion will be continued with emphasis on the redistribution of boron during heat treatments.

resistivity standard reference wafers

stability of standards

relationship between resistivity and dopant density

impurity profiles

impurities and defects

Crystal Defects and Contaminants — Other chemical impurities and crystallographic defects can also affect device characteristics. Although these impurities and defects are usually unintentionally introduced during crystal growth or subsequent wafer processing, they may also be added intentionally to control material parameters such as minority carrier lifetime and related device characteristics. Since these impurities and defects do not usually affect the resistivity, their presence must be detected by other means. Study of new, powerful methods for identifying and counting defects and impurities in junction structures, based on measurement of thermally or optically stimulated current and capacitance will continue; in addition to research on the methodology and interpretation, a defect catalog will be generated and simplified instrumentation, suitable for use in a production environment, designed and constructed. These tools will permit the rapid identification of defects and contaminants in junction structures on the fabrication line. In addition,

new, powerful methods

defect catalog

several of the more traditional carrier lifetime measurements will be compared with each other and with the results of the thermally stimulated current and capacitance measurements, and work will be completed on the energy level model for gold, an impurity widely used to control minority carrier lifetime, in silicon. Some of the mathematical modeling effort discussed above will also relate to the interpretation of experiments in this area.

carrier lifetime

gold in silicon

Oxide or Other Insulator Films — Stable insulator characteristics are essential to the reliable operation of metal-insulator-semiconductor (MIS) integrated circuits. A new effort on insulator characterization will begin with a detailed review of the existing state of the art in control procedures used during fabrication of MIS devices. At the same time, experimental investigations of methods for determining stability and other characteristics of insulator films will be initiated and several surface analysis methods including ion microprobe analysis, Auger spectroscopy, and ESCA will be studied in cooperation with both the NBS Institute for Materials Research and the NRL group on radiation-hardened MIS devices; the latter is funded through DNA as a consequence of the realization that problems in assuring stable insulator films are particularly acute in the more exotic combinations used in radiation-hardened MIS devices.

oxides

characterization

MIS devices

surface analysis

radiation-hardened MIS devices

Test Patterns — Special device configurations are widely used to monitor process procedures. These configurations are designed so that the measured electrical characteristics can be interpreted in terms of the desired process parameters. These patterns may be included on each circuit chip or spotted at various selected points on the wafer. Earlier this year, a test pattern was designed and fabricated primarily for use in evaluating in-house processing procedures. This pattern contains 20 individual structures; both *p-n* junction and MOS capacitor structures are represented. Although it is substantially larger than would be appropriate for use in connection with device production, it will furnish a reference for analysis of test patterns used in the industry. The first phase of an effort to collect, review, and analyze test patterns used in the industry, will be completed. In addition, work on a CCD test vehicle for evaluating certain characteristics of MOS devices is expected to be funded at the Naval Electronics Laboratory Center under this program and efforts on test patterns for use in electrical tests of metallization step coverage will be initiated.

test patterns

CCD test vehicle

Photolithography — There are a number of problems associated with the use of ultraviolet-sensitive emulsions in the photolithographic steps of device fabrication. Generally these relate to contamination, application, exposure, and removal. This problem area will be reviewed in detail and if appropriate experimental work will be initiated either in-house or by contract.

photolithography

photoresists

mask inspection

Length calibrations and automated procedures for locating and identifying flaws in masks used in the photolithographic processes would be a boon to the industry. Much effort has been expended by the military and NASA on systems for accomplishing automated pattern inspection on wafers. It may be that these systems are too ambitious for the present state of the art; it is hoped to undertake a contract effort to determine whether, within the present state of the art, an automated mask inspection system is feasible.

film and layer thickness

Film and Layer Thickness — Another quantity of critical importance to device performance is the thickness of the various layers and films which comprise devices. In particular, rapid, noncontacting procedures are needed for determining thickness of epitaxial layers, oxide films, diffused layers, implanted layers, and the like. This area will be reviewed with the aim of intiating appropriate experimental work later in the program.

wafer inspection and test

SEM

flying spot scanner

other methods

Wafer Inspection and Test — Visual inspection procedures have long been used to screen wafers and individual dice. More recently, inspection by scanning electron microscopy has been found to reveal in circuits flaws which cannot be detected by visual inspection. In addition, both the scanning electron microscope (SEM) and a flying spot scanner with a laser source have been shown to be feasible instruments for use in exercising relatively complex integrated circuits to permit essentially noncontacting testing of circuits or circuit elements. A flying spot scanner will be constructed, tested, and used in conjunction with an existing SEM to study effects of electron beam induced damage to circuits inspected or tested with the SEM. Plans for further study of inspection methods and noncontacting test procedures will be developed in parallel with this work, probably with out-of-house assistance.

die and wire bonding

beam-lead

Bonding — Bonding of the die to the header and bonding of the electrical interconnection leads are critical steps in the assembly of devices. Dissemination of the results of past efforts on ultrasonic aluminum wire bonding, pull-test procedures, and die attachment evaluation by the thermal response technique will continue. Development of an in-process monitoring system for ultrasonic wire bonding will also continue. Facilities for beam-lead bonding will be established, procedures for testing beam-lead bonds will be reviewed, and detailed study of evaluation of beam-lead bonds will be initiated if appropriate.

hermeticity

Hermeticity and Residual Gas Analysis — Tests for detection of both fine and gross leaks in hermetic packages have been of concern to the military for some time. The theoretical bases for the analysis of two of the most widely used methods, helium mass spectrometry and radioisotope, are not in accord. Further, it would be desirable to have a single, noncontaminating test sensitive to all sizes of leaks. Accordingly a new effort is being established to develop procedures for intercomparison of leak rates; transfer standards, and, eventually, improved test procedures. A further extension of this type of activity is analysis of the residual gas content in production equipment such as vacuum evaporation and sealing stations.

residual gas analysis

Thermal Properties — Thermal characterization of certain types of integrated circuits is essential to assure that they have appropriate power handling capabilities. Electrical tests involving the use of the substrate isolation diode will be investigated to determine their applicability in this area. Also in a related effort, work on high current devices, and r-f power devices will be undertaken, and study of current crowding effects in power devices will continue.

thermal characterization

integrated circuits

power devices

Processing Facility — Some improvements in the in-house processing facility are essential to permit it to be utilized efficiently in providing devices and test patterns for evaluation of various measurement procedures and in preliminary establishment of the feasibility of selected process control procedures. Steps are now being taken to upgrade these facilities in order to reduce background contamination levels to an extent which will permit fabrication of low-leakage *p-n* junctions and satisfactory MOS capacitors and transistors.

processing facility

Planning — The general review of process control procedures and collection of information regarding relationships between processes and reliability will continue for the next few years to assure timeliness and completeness of the program. This activity will include field visits, literature reviews and interaction with coordination groups and standards groups. Workshops and symposia in the early stages of the program will also be used for gaining additional insight into industry problems. Both in-house and contract efforts will be employed.

planning

information input

methods

Contract Efforts — In addition to state-of-the-art reviews to assist in program definition and planning, contract research may be undertaken for the purposes of development or evaluation of test methods, development or fabrication of test specimens, and development of test instruments. Supporting research activity in selected areas may also be undertaken by contract. As part of the overall effort it is also expected that funds will be made available for direct ARPA support of related activities in the various military services; these projects will not come under the direct purview of NBS.

contract research

Dissemination — Initially, the workshops and symposia will be organized to emphasize the input of information to the program; later, the emphasis will shift to dissemination. Other means of dissemination are expected to include technical publications, direct interactions with industry and

information dissemination

government organizations, and interactions with standards committees. As appropriate, artifacts, such as standard reference materials, will be developed to assist in utilization of the measurement technology. Eventually, measurement assurance programs may be developed to enhance further the utilization of the technology developed.

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UPPLEMENTARY NOTES

BSTRACT *(A 200-word or less factual summary of most significant information. If document includes a significant ibliography or literature survey, mention it here.)*

The dual purpose of the workshop was (1) to announce and describe the new ffort, "Advancement of Reliability, Processing, and Automation for Integrated ircuits with the National Bureau of Standards," sponsored by the Defense Adanced Research Projects Agency (ARPA), and (2) to obtain additional input on ritical measurement problems in integrated circuit processing and assembly to ssist in planning future work in the effort. More than 130 engineers repreenting 61 organizations from the electronics industry and government particiated in the workshop. The measurement problems in silicon, oxides, photolithoraphy, and assembly and the problems in information dissemination that were dentified by the participants are summarized. Included as appendices are ummaries of two talks given: one which described the results of earlier direct ontacts with a cross section of industrial representatives on major measurement roblems in integrated circuit processing and assembly and the other which desribed the initial plans for work in the new effort.

EY WORDS *(six to twelve entries; alphabetical order; capitalize only the first letter of the first key word unless a proper ame; separated by semicolons)*

ie bonding; hermeticity; integrated circuits; measurement methods; microelectronics; xides; photolithography; process control; reliability; semiconductor devices; ilicon; wire bonding.

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