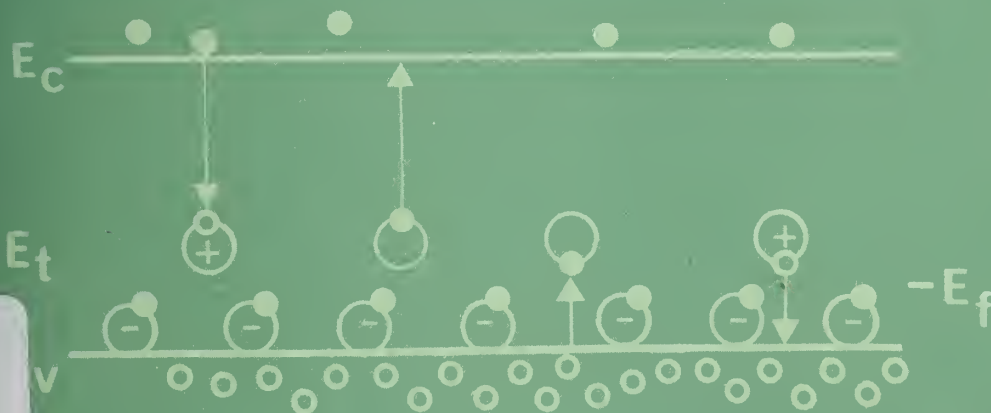# NBS SPECIAL PUBLICATION 400-26

U.S. DEPARTMENT OF COMMERCE / National Bureau of Standards

Semiconductor Measurement Technology:

Defects in PN Junctions and MOS Capacitors Observed Using Thermally Stimulated Current and Capacitance Measurements

Videotape Script

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Office of Standard Reference Data — Office of Information Activities — Office of Technical Publications — Library — Office of International Relations — Office of International Standards.

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[1] Headquarters and Laboratories at Gaithersburg, Maryland, unless otherwise noted; mailing address Washington, D.C. 20234.
[2] Located at Boulder, Colorado 80302.

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Special publication, no. 400-26,

Martin G. Buehler

Electronic Technology Division
Institute for Applied Technology
National Bureau of Standards
Washington, D.C. 20234

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PREFACE

    This is the script for the first in a series of videotape presentations being dis-
tributed on loan without charge in order to disseminate more effectively to the semi-
conductor community the measurement technology improvements developed under the Semi-
conductor Technology Program in the Electronic Technology Division of the National Bureau
of Standards (NBS).

    The Semiconductor Technology Program serves to focus NBS efforts to enhance the per-
formance, interchangeability, and reliability of discrete semiconductor devices and in-
tegrated circuits through improvements in measurement technology for use in specifying
materials and devices in national and international commerce and for use by industry
in controlling device fabrication processes. Its major thrusts are the development of
carefully evaluated and well documented test procedures and associated technology and
the dissemination of such information to the electronics community. Application of the
output by industry will contribute to higher yields, lower cost, and higher reliability
of semiconductor devices. The output provides a common basis for the purchase specifi-
cations of government agencies which will lead to greater economy in government procure-
ment. In addition, improved measurement technology will provide a basis for controlled
improvements in fabrication processes and in essential device characteristics.

    The Program receives direct financial support principally from three major sponsors:
The Defense Advanced Research Projects Agency (ARPA),[*] The Defense Nuclear Agency (DNA),[†]
and the National Bureau of Standards.[x] The ARPA-supported portion of the Program, Advance-
ment of Reliability, Processing, and Automation for Integrated Circuits with the National
Bureau of Standards (ARPA/IC/NBS), addresses critical Defense Department problems in the
yield, reliability, and availability of integrated circuits. The DNA-supported portion
of the Program emphasizes aspects of the work which relate to radiation response of
electron devices for use in military systems. There is considerable overlap between the
interests of DNA and ARPA. Measurement oriented activity appropriate to the mission of
NBS is a critical element in the achievement of the objectives of both other agencies.

    Essential assistance to the Program is also received from the semiconductor indus-
try through cooperative experiments and technical exchanges. NBS interacts with indus-
trial users and suppliers of semiconductor devices through participation in standardizing
organizations; through direct consultations with device and material suppliers, govern-
ment agencies, and other users; and through periodically scheduled symposia and workshops.
In addition, progress reports are regularly prepared for issuance in the NBS Special
Publication 400 sub-series. More detailed reports such as state-of-the-art reviews,
literature compilations, and summaries of technical efforts conducted within the Program
are issued as these activities are completed. Reports of this type which are published
by NBS also appear in the Special Publication 400 sub-series. Announcements of avail-
ability of all publications in this sub-series are sent by the Government Printing Office
to those who have requested this service. A request form for this purpose may be found
at the end of this report.

Defects in PN Junctions and MOS Capacitors

Observed Using Thermally Stimulated Current and Capacitance Measurements

Videotape Script

by

Martin G. Buehler

Two measurement methods are described which detect and characterize defects which can control such device characteristics as lifetime and junction leakage. The methods can be used as diagnostic tools in the fabrication of bipolar and MOS devices. The number of different kinds of defects and their densities may be obtained with little effort and simple apparatus. Positive identification of these defects may be obtained with more effort and more sophisticated apparatus. Of more importance, the measurements characterize defects in an environment which is identical to that of the finished product. Thus, the answers derived are directly applicable to process control and device design.

These methods involve thermally stimulated capacitance and current measurements which utilize the ability of defects in the vicinity of a p-n junction or in an MOS capacitor to trap holes or electrons and emit them after receiving sufficient thermal energy. Values for defect densities, energy levels, and emission rates can be derived from these measurements. The limit of detectability can be as low as 10^{10} defects/cm^3. These values provide sufficient information to positively identify the defects.

Three vehicles are used to illustrate the methods: a gold doped n^+-p diode, a p^+-n diode with a process-induced defect center, and a gold doped n-type MOS capacitor. Two cryostats are described which have a maximum heating rate of 10 K/s.

Key Words: Cryostat; defects; gold-doped silicon; measurement methods; microelectronics; MOS capacitor; p-n junctions; semiconductors; silicon; thermally stimulated capacitance; thermally stimulated current.

The class of measurements that will be presented are known as thermally stimulated (000)* current and capacitance measurements. These measurements detect defects in the space charge region of p-n junctions and MOS capacitors. The defects may be intentionally introduced, such as gold, or they may be processed induced defects or radiation induced defects. The introduction of these defects has the effect of either changing the resistivity of silicon or of lowering its lifetime and thereby increasing the leakage currents in junctions. The thermally stimulated current and capacitance measurements are very sensitive to the presence of defect centers, for they are able to detect as little as one defect center in a trillion silicon atoms.

The measurements presented here are for defect centers observed in silicon; however, defects have been observed by these measurements in other semiconductors. Compared to other methods, these measurements are the most sensitive and the analysis is rapid.

In this presentation the physics of the measurement is discussed first, followed by

*Tape counter setting

various practical examples, and finally the measurement apparatus is described.

The key features of the thermally stimulated current and capacitance measurements are shown in this energy band diagram. [Figure 1] In this p-type semiconductor, acceptors have an electron and are negatively charged. For conceptional purposes these donor defects may be thought of as the gold donor defect in p-type silicon. These defects have an energy level, E_t, close to the valence band. Defects communicate with the valence band and conduction band through either electron capture, electron emission, hole capture, or hole emission [indicated by arrows, in Figure 1, from left to right]. Donor defects are either positive, when a hole resides at the center, or neutral, when an electron resides at the center.

In the space-charge region the emission rates govern the charge state of the defect center. From energy considerations the hole emission rate is much faster than the electron emission rate. Thus, the defect has no charge in the space-charge region under steady state conditions. In the neutral region the charge state is governed by the Fermi energy level, E_f, which dictates that the defect be positively charged.

In order to detect defect centers, there must be a change in charge states between centers in the space-charge region and those in the neutral region. This point will be amplified later.
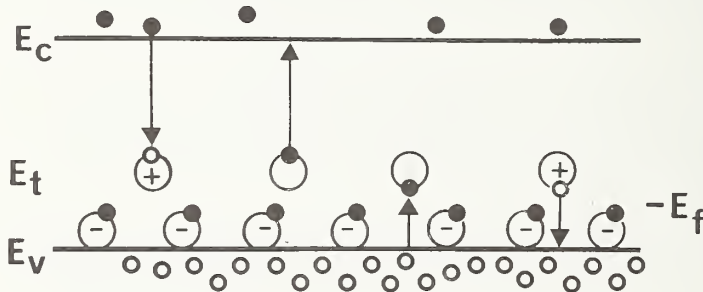

Figure 1. Emission and capture processes at a defect center in the energy gap of a semiconductor.

The emission rate for the holes and electrons depends on the defect energy level. The mathematical relationship is shown next. [Figure 2] This expression pertains to holes or electrons depending on whether the subscript x is p or n. The expression indicates that the emission rate depends on a pre-exponential B-coefficient, times the temperature T squared, times the negative exponential of the energy needed by a hole or electron to escape to its respective band edge normalized

EMISSION RATE

$$e_x = B_x T^2 \exp(-\Delta E_x/kT)$$

HOLE EMISSION (x = p)

ELECTRON EMISSION (x = n)

Figure 2. Emission rate expressions

by kT, where k is the Boltzmann constant.

The nature of the measurement is illustrated next [Figure 3] by this schematic representation of an n^+-p junction with two donor defects on the lightly doped p-type side of the junction [defect indicated by a star]. With zero bias applied to the junction, the space-charge region is very small, extending from the junction to the dashed line [Figure 3A]. The n^+ region is assumed to be so heavily doped that the space-charge penetration into this region may be neglected. In the neutral region, the negative charge on the acceptor atoms is neutralized by valence-band holes, and the positive charge on the donor defects is neutralized by conduction-band electrons.

Under zero bias the junction is now lowered to liquid nitrogen temperature. Now, at this temperature, a reverse bias is applied to the junction which widens the space-charge region as illustrated here [Figure 3B]. Valence-band holes and conduction-band electrons are removed from the space-charge region. At this temperature the hole remains on both defect centers: the one in the space-charge region and the one in the neutral region.

(95)

Figure 3. Charge state of defect centers in n^+-p junction.

As the temperature of the junction is increased, a critical temperature is reached, called the emission temperature, at which the hole on the defect in the space-charge region receives sufficient thermal energy to be released to the valence band. Through this process the defect center has changed charge state from positive to neutral and the release of the hole constitutes a current which can be measured in an external circuit. The change in charge state means that the space-charge region must shrink so as to maintain charge balance [indicated in Figure 3C]. This motion of the space-charge region constitutes a change in the junction capacitance which can also be measured in an external circuit. This example illustrates the case of the gold donor in a silicon n^+-p junction.

Experimental results for such a junction will be shown next [with use of Figure 4]. The junction was first cooled to liquid nitrogen temperature. The donors were charged with holes by zero biasing the junction. After a reverse bias of 22.5 volts was applied, the junction was heated slowly at 0.61 kelvin per second and the current measured [Figure 4A]. The junction was again cooled to liquid nitrogen temperature and defects charged, but this time the junction was heated at 5 kelvin per second.
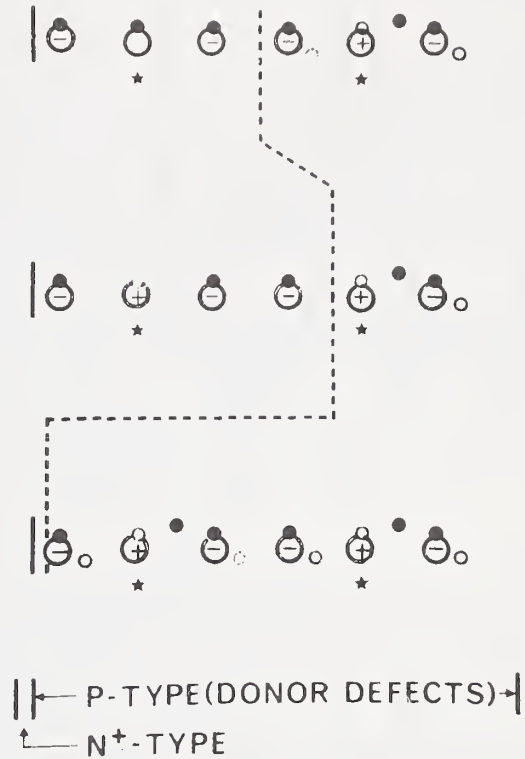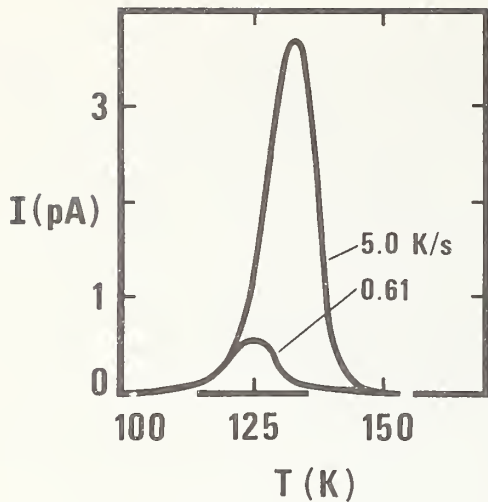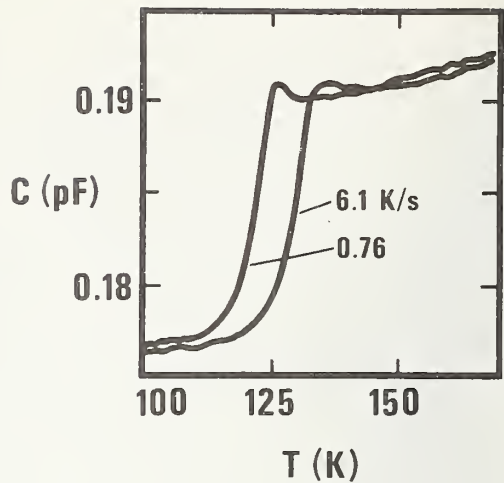
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Figure 4. Response of a gold doped n^+-p junction.

These dynathermal or dynamic-temperature measurements indicate that hole emission (165) from the gold donor is heating-rate dependent, for at the slower heating rate the peak occurs at 125 kelvin and at the higher heating rate it occurs at 134 kelvin. Because the current response is governed by the rate at which holes are emitted per unit time, the sensitivity of this measurement depends on the heating rate. For a high heating rate of 10 kelvin per second it is possible with our equipment to detect 10^{10} defects/cm^3 or one defect center in a trillion silicon atoms.

Next [Figure 4B] is shown the dynathermal capacitance response of the gold donor. This step in the capacitance response is directly related to the number of gold atoms which in this case is about 10^{15}/cm^3. Because the capacitance response is governed by the number of the holes emitted, the magnitude of the capacitance step is not heating rate dependent. For our equipment, defect centers are detectable if their density is greater than one defect in five hundred background dopant atoms.

For the non mid-gap defect shown here, the capacitance measurement is by far the easier in terms of the experimental apparatus and theoretical interpretation. For example, simple cryostats may be used, for icing is not a problem and low heating rates may be used. However, as will be shown, the dynathermal current measurements are superior when evaluating mid-gap defect centers which are the source of junction leakage.

The next example is a process-induced defect center in a silicon p^+-n junction. This defect was unintentionally introduced into the junction. It resulted from the fabrication process. The dynathermal current and capacitance response for this defect [Figure 5] indicates that this center has two energy levels, as indicated by the emission processes at 150 and 225 kelvin. This example allows a comparison between the dynathermal response of a non-mid-gap energy level and a mid-gap energy level. The non-mid-gap energy level is initially completely full of electrons and finally completely emptied of electrons. The mid-gap energy level is initially completely full of electrons but after the electrons have begun to be emitted, this level begins to generate both electrons

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and holes. It is the leakage source for the junction as indicated by the rapid rise in the current with temperature. This shoulder response of the dynathermal current is a key to its rapid identification. As will be shown this response is quite different from the gold acceptor response.

Figure 5. Response of a p^+-n junction with process-induced defect centers.

Before this center is discussed further, a limitation of the measurements is discussed [with the use of Figure 6]. The ability of these measurements to detect defects depends on whether the defects change charge state. This in turn depends on the position of the defect energy level in the energy gap. As an example, consider an n-type semiconductor [Figure 6A] with an acceptor defect center whose energy level is located well below mid-gap. In the neutral region, denoted by electrons in the conduction band, the center is negatively charged. In the space-charge region, denoted by the absence of electrons in the conduction band, the electron sticks on the center for at reasonable temperatures the electron cannot receive enough thermal energy to be excited to the conduction band. This defect center does not change charge state and is therefore not detectable by these measurements.

For an energy level at mid-gap, the center is initially charged with an electron but in its final state it acts as a generation site emitting holes and electrons [Figure 6B]. Its final charge state is governed by these emission rates which dictate its detectability.

For an energy level above mid-gap, centers are initially fully charged with electrons and finally fully discharged [Figure 6C]. These centers have optimum detection conditions.

In summary [Figure 6D], the ability to detect defects in n-type silicon depends on the position of the energy level of the defect center. If the energy level lies in the lower half of the gap, then no measurement is possible (M=0). If the level is in the upper half of the energy gap then the measurement has the best chance of succeeding (M=1).

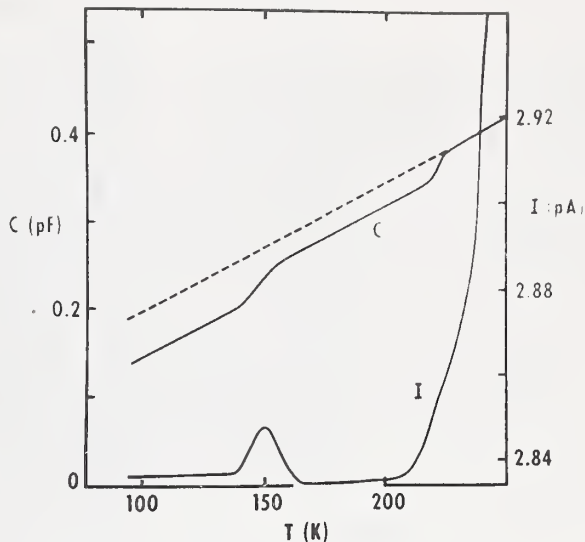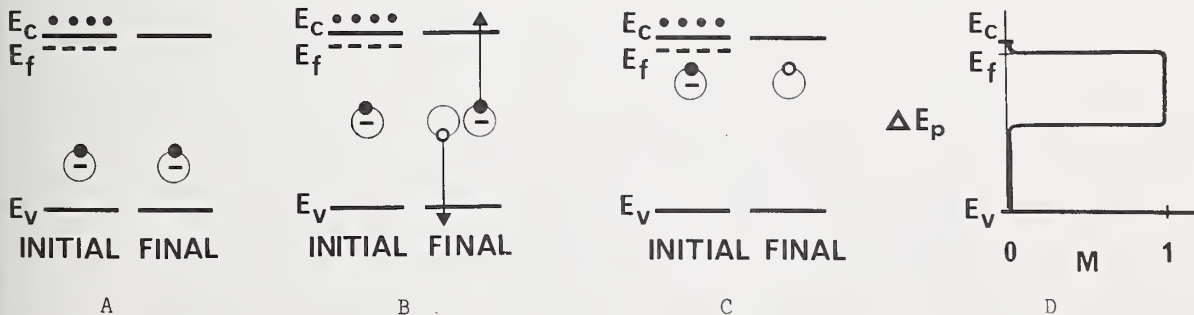Figure 6. Measurement detectability of acceptor defect centers located at different energy levels.

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If the level lies above the Fermi level, E_f, detectability is poor because the center is initially not charged with electrons.

The three kinds of measurement methods used to characterize defects are discussed now with respect to the process-induced defect in a silicon p^+-n junction [Figure 5]. The measurements shown here are dynathermal measurements. The emission temperature and the heating rate are initial clues to the atomic identity of the defect center. The emission temperature is defined by the current peak or the maximum capacitance slope. A more definitive analysis of the emission rate, which involves the energy level determination, follows from isothermal capacitance measurements. In this measurement, made at a fixed temperature, the capacitance time constant is determined as the capacitance goes from its initial state to its final state. Measurements are taken at various temperatures and from the analysis comes both the energy level and the pre-exponential B-coefficient. Such measurements were used to evaluate the electron emission rate for the 150 kelvin emission process.

The emission process at 225 kelvin is a mixture of both electron and hole emission. To evaluate these emission rates both isothermal capacitance and steady state leakage measurements are needed. The results of such evaluations are shown next [Figure 7] for the two emission processes. The non-mid-gap electron emission observed at 150 K is characterized by this emission rate, $[e_n = 4.1 \times 10^3 \, T^2 \exp(-0.23/kT)]$, and its energy level is in the middle of the upper half of the energy gap. The emission process observed at 225 K is given by these electron and hole emission rates, $[e_n = 3.5 \times 10^8 \, T^2 \exp(-0.61/kT)$ and $e_p = 3.4 \times 10^6 \, T^2 \exp(-0.55/kT)]$, and their energy level is near mid-gap. The defect density, N_t, for the two levels is the same within experimental error since both emission processes are coupled to the same defect center.

$$T_e = 150 \text{ K for } \beta_e = 7.5 \text{ K/s}$$

$$e_n = 4.1 \times 10^3 \, T^2 \exp(-0.23/kT)$$

$$N_t = 3.0 \times 10^{12} \text{ cm}^{-3}$$

$$T_e = 225 \text{ K for } \beta_e = 4.2 \text{ K/s}$$

$$e_n = 3.5 \times 10^8 \, T^2 \exp(-0.61/kT)$$

$$e_p = 3.4 \times 10^6 \, T^2 \exp(-0.55/kT)$$

$$N_t = 2.9 \times 10^{12} \text{ cm}^{-3}$$

Figure 7. Emission rate expressions and defect density for the process-induced center shown in Figure 5.
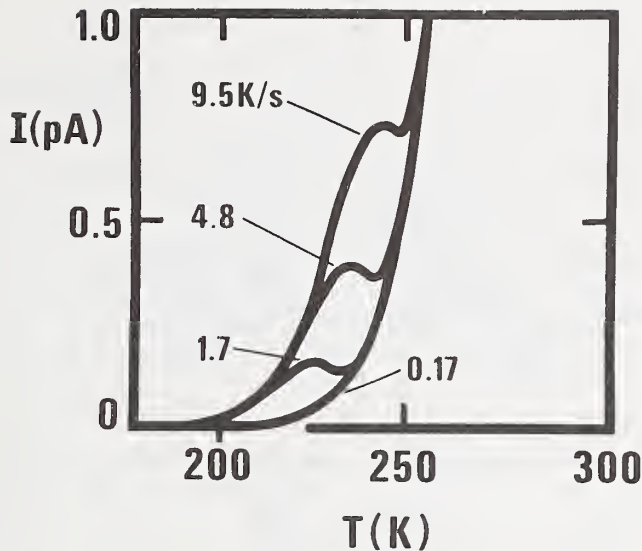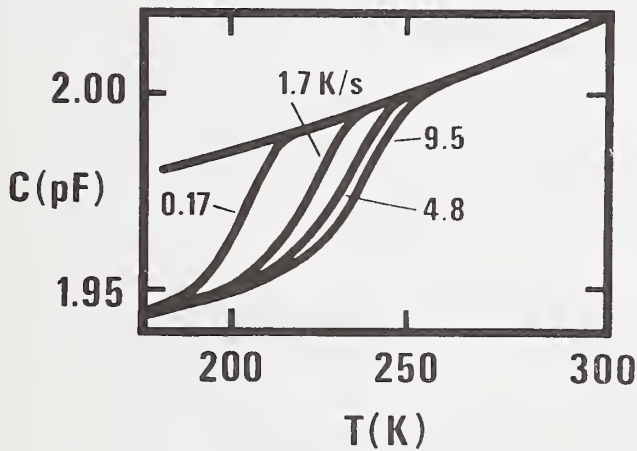
Figure 8. Response of a gold doped p^+-n junction.

The shoulder shape of the dynathermal current response is a unique signature for (311) the process-induced defect center [Figure 5]. This shape is distinctly different from the dynathermal current response for the gold acceptor defect in a silicon p^+-n junction shown next [Figure 8A]. This response shows a peak and valley before it goes into steady state leakage. This dramatically demonstrates how dynathermal current measurements can be used to identify mid-gap defect centers. The currents shown here were measured at various heating rates. If the heating rate is slow enough, [0.17 K/s], electron emission is difficult to detect and the current response is essentially the steady state leakage response. The capacitance response is shown next [Figure 8B] for various heating rates. From this shift in characteristics the gold density was found to be about 3 percent of the background donor density.
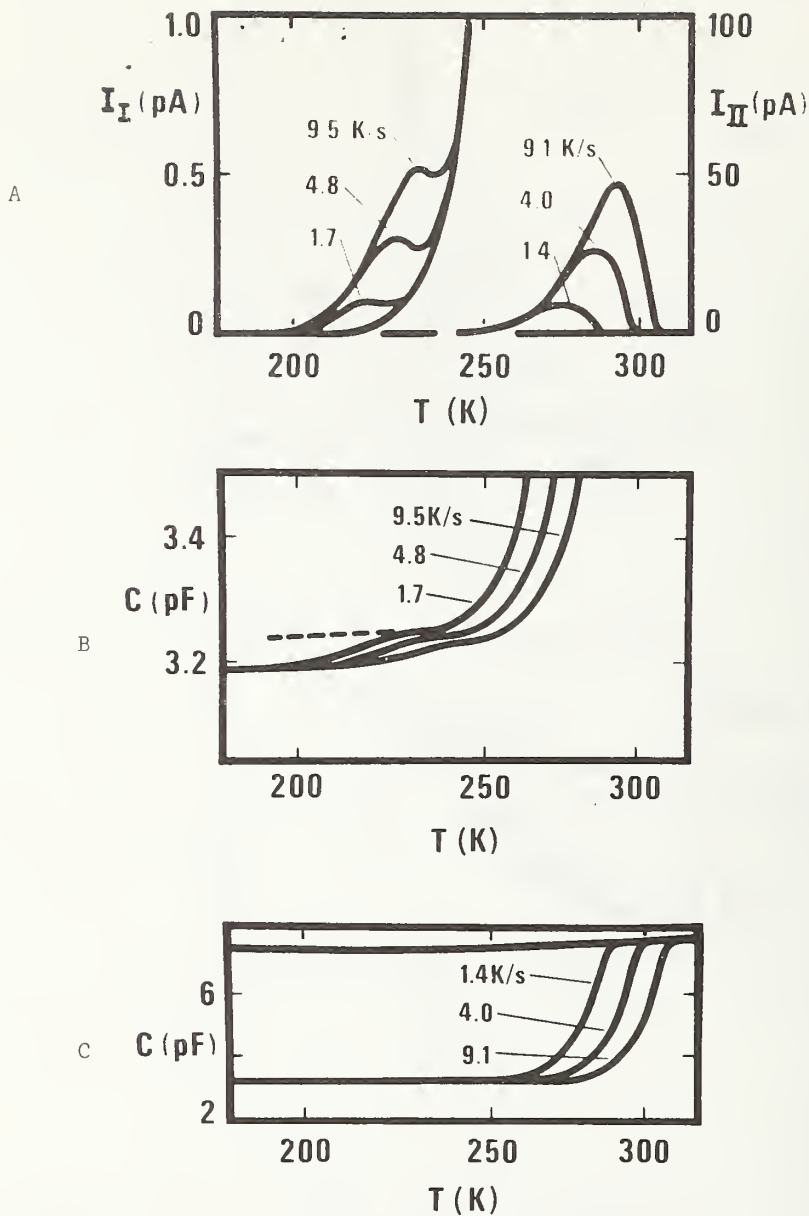
Figure 9. Response of a gold doped n-type MOS capacitor.

The current and capacitance response for a gold doped silicon p^+-n junction is (330) identical to the initial response of a gold doped n-type MOS capacitor. The dynathermal current response of such an MOS capacitor is shown next [Figure 9A] for various heating rates. The phase I response has a peak and valley characteristic indicative of the gold acceptor. This response, which is dominated by electron emission, is scaled according to the left hand axis. In addition to phase I there is a second phase. The phase II response, which is dominated by hole emission, is scaled according to the right hand axis. Notice that once equilibrium has been reached [at high temperatures], no current flows through the MOS capacitor.

The phase I capacitance response is shown next [Figure 9B] and from this step in the

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response the gold density was found to be about 4 percent of the background donor density. (345)
Once the gold center begins to act as a generation site, the capacitance begins to change
rapidly. By rescaling the capacitance response, the overall response is shown next [Figure 9C] where phase I response is no longer visible. The phase II response is clearly
evident. Once the capacitance reaches equilibrium inversion, no further change is
noted. This point corresponds to cessation of current flow through the capacitor.

The physics of this measurement is explained in the following schematic diagram of an MOS capacitor [Figure 10]. A bias has been applied to the metal gate so as to invert the oxide-silicon interface represented by the hole [at the oxide-silicon interface, Figure 10A]. A space-charge region exists free of conduction-band electrons and valence-band holes [from the interface to the dashed line]. This region is followed by a neutral region. Acceptor defects are located at three positions [indicated by stars]. This condition is established at room temperature and then the MOS capacitor is cooled to liquid nitrogen temperature. At this low temperature the applied bias is changed so that the space-charge region is increased [Figure 10B]. This gold center [middle one] has been effectively charged with an electron which sticks since at this low temperature it does not receive enough thermal energy to be released.

As the temperature is increased, the electron is emitted and the space-charge region shrinks ever so slightly in order to maintain charge balance [Figure 10C].

Figure 10. The charge state of defect centers in an n-type MOS capacitor.

This is the phase I response, which is dominated by electron emission.

As the temperature continues to rise, these gold defects act as generation sites
emitting electrons and holes. Emitted electrons are swept by the electric field to the
neutral region; whereas, emitted holes are swept to the oxide-silicon interface where
they increase the hole density. This is the phase II response which is dominated by hole
emission. As holes appear at the oxide-silicon interface, the space-charge region shrinks
so as to maintain charge balance. The space-charge region continues to shrink until equilibrium inversion conditions are established [Figure 10D].
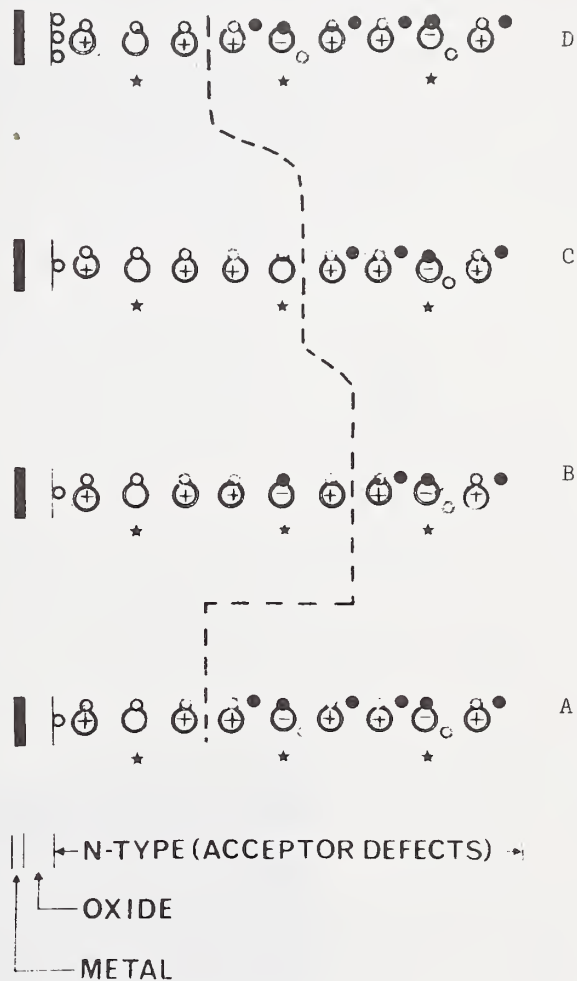
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A brief review of the MOS capacitor dynathermal response is presented next [Figure 11].(396) This current response [Figure 11A] illustrates the turn-on of phase I, the phase I emission temperature [T_{eI}], the phase II emission temperature [T_{eII}], and final equilibrium [zero current]. These four critical temperatures [indicated by the dashed lines] are related to the capacitance response as shown here [Figure 11B]. The phase I turn-on, the transition between phases, and final equilibrium are related to the MOS capacitance gate voltage characteristics [Figure 11C]. The room temperature, high frequency characteristics are shown by the heavy line. Recalling the measurement sequence, gate bias V_{g1} is first applied at room temperature and then the capacitor is lowered to liquid nitrogen temperature. Gate bias V_{g2} then biases the MOS capacitor into deep depletion. With V_{g2} applied, the temperature is increased and during phase I, electrons are emitted. As the temperature continues to rise, holes are pumped into the oxide-silicon interface until the equilibrium inversion condition is achieved.

The dynathermal measurements show great promise in being able to identify the atomic nature of defects found in the space-charge region of p-n junctions and MOS capacitors. A catalog of defects might take the following form [Figure 12]. Here the defect energy level relative to the appropriate band edge has been plotted with respect to its phase I emission temperature for a heating rate of 1 kelvin per second.
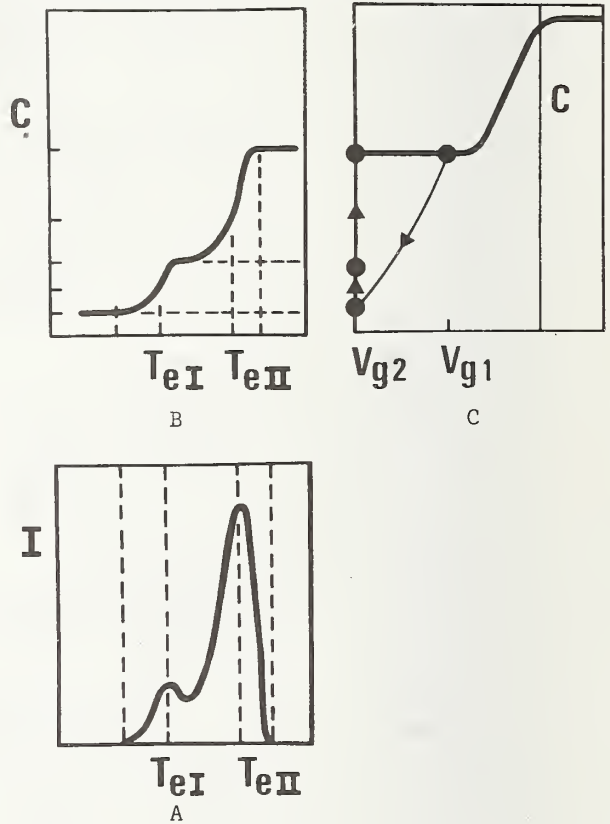

Figure 11. A schematic representation of the MOS capacitor response shown in Figure 9.

The dashed lines are related to the emission rate B-coefficient and the heating rate. For example, the gold donor [hole emission] has an emission temperature of 128 kelvin for a heating rate of 1 K/s; whereas, for a heating rate of 10 K/s it has a 136 kelvin emission temperature. In addition to the process-induced defect centers and the gold centers, radiation-induced defect centers are also shown. These centers were generated by electron irradiation or by neutron irradiation. Some centers have the same energy level but different B-coefficients and thus have different emission temperatures. Other centers have the same emission temperatures but different energy levels. If they are non-mid-gap centers, they can be identified by determining their energy levels from isothermal capacitance measurements. If they are mid-gap centers, then the shape of the dynathermal current response can be used to establish their identity. For example
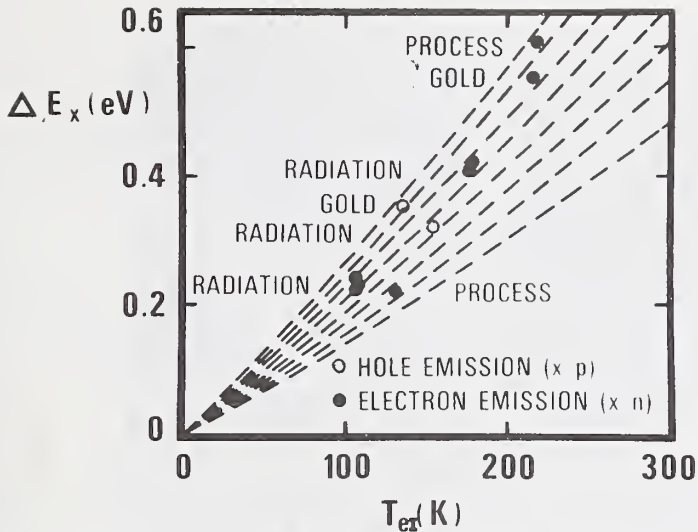
Figure 12. Emission temperatures of various defect centers in silicon for a heating rate of 1 K/s.

recall that the process-induced defect had a shoulder response [Figure 5] whereas the   (436)
gold acceptor defect had a peak and valley response [Figure 8A].

The experimental apparatus used in these experiments is capable of measuring currents one hundred times less than a picoampere and of measuring capacitance changes one hundred times smaller than a picofarad at heating rates as high as 10 kelvin per second. This is achieved in part by mounting p-n junctions or MOS capacitors on a TO-5 header. The unit under test is mounted on a ceramic slab as shown here [Figure 13]. The ceramic slab is gold coated on both sides which allows easy alloying. On its top side the gold coating is broken so that a temperature sensing diode mounted here is electrically isolated from the unit under test. The temperature sensing diode is forward biased at 10 microamperes, and its forward voltage is proportional to the temperature.
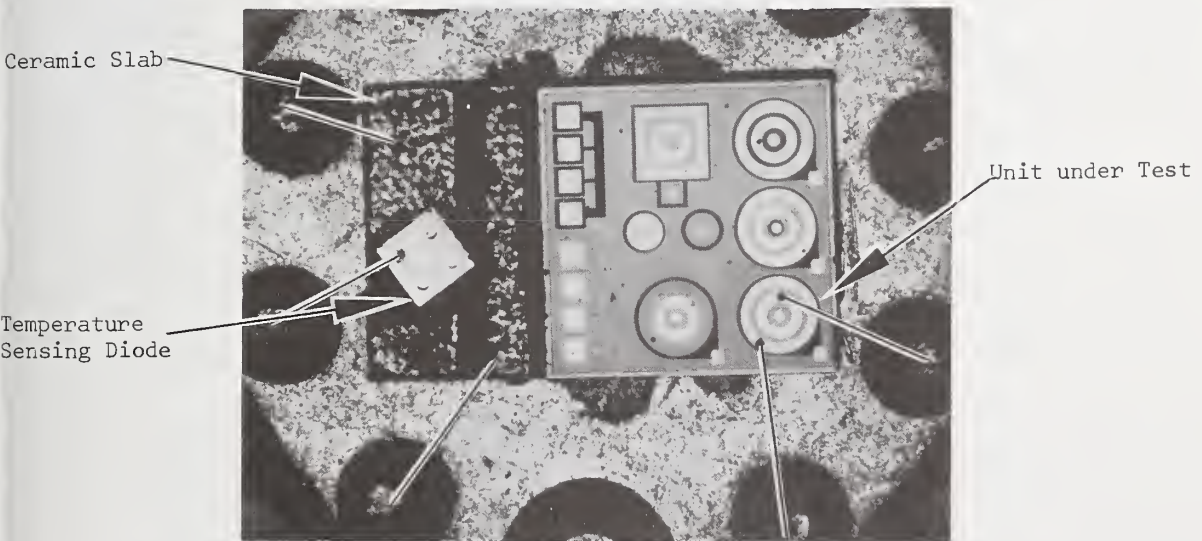

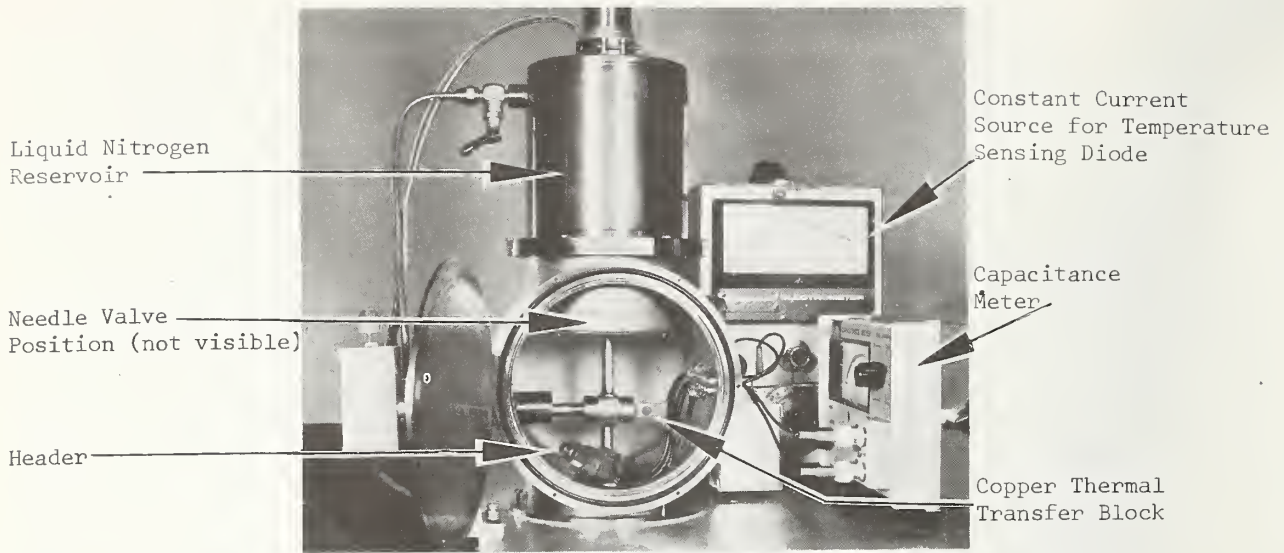Figure 13. Sample mounting scheme in a 10-pin TO-5 header.

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Figure 14. Cryostat number 1.

Two experimental systems are in current use in our laboratory. The first system (453)
[Figure 14] is capable of both dynathermal and isothermal measurements. It consists of
a liquid nitrogen reservoir with a needle valve at the bottom of the reservoir which al-
lows the liquid nitrogen to flow around a copper thermal transfer block and out of the
cryostat. Within the copper block is a 150 watt heater. Under test conditions the TO-5
header is mounted in the hole in the copper block. The chamber is evacuated using a
roughing pump. This procedure prevents icing problems. Dynathermal measurements consist
of cooling the unit under test to liquid nitrogen temperature, charging the defects
using a proper bias sequence, shutting off the liquid nitrogen, heating the copper block,
and recording the current or capacitance response.

The second and simpler system that has only dynathermal capabilities is shown here
[Figure 15]. It consists of a funnel which directs liquid nitrogen into the bellows area
where the TO-5 header is mounted. The cap is raised into position and the chamber is
evacuated. The capacitance meter is located close to the apparatus to minimize lead
length. A closer view [Figure 16] reveals the TO-5 header positioned into the base of
a copper thermal transfer block. The header looks directly into the end of a 150 watt
heater which is silver soldered into the copper block. The heater leads are taken out of
the funnel and thereby shielded from the TO-5 header. This cryostat features quick load-
ing and unloading capabilities. A dynathermal measurement can be performed in well under
10 minutes.

In conclusion, this class of measurements reveals defects in the space-charge
region of p-n junctions and MOS capacitors if the defects can be charged and discharged.
This means that defects must lie in the mid to upper half of the energy gap in n-type
silicon, and must lie in the mid to lower half of the gap in p-type silicon. However,
this is not a handicap in that these measurements can detect mid-gap leakage centers

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Constant Current
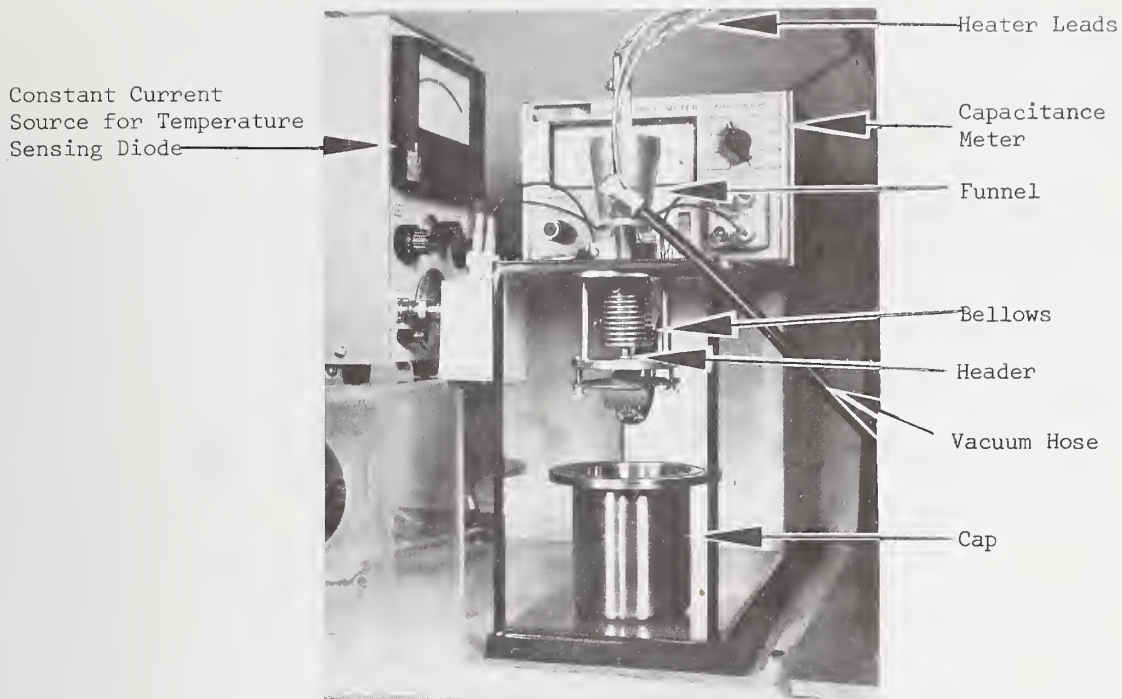Source for Temperature
Sensing Diode

Heater Leads

Capacitance
Meter

Funnel

Bellows

Header

Vacuum Hose

Cap

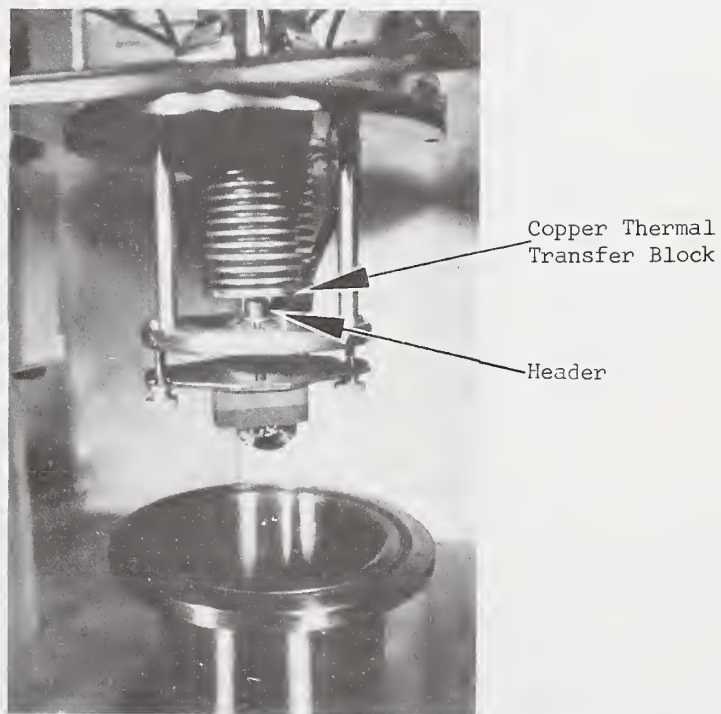Figure 15.   Cryostat number 2.

Copper Thermal
Transfer Block

Header

Figure 16.   Close up view of cryostat number 2.

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in both n- and p-type silicon. The detectability of the defects is one defect in a $\quad$ (490)
trillion silicon atoms when measuring current, and when measuring capacitance it is
one defect in five hundred dopant atoms. These estimates are conservative for ulti-
mate detectable limits may be lower. Dynathermal measurements are useful in provid-
ing a quick thermal scan which reveal the variety of emission processes present and
the density of each. From a defect catalog the atomic nature can be tentatively iden-
tified. Mid-gap leakage centers that have a unique dynathermal current signature can
be readily identified. For non mid-gap centers, isothermal capacitance measurements
can be used to determine its energy level. Using a defect catalog leads to positive
identification.

In our laboratory, work is currently under way to catalog more defect centers by
intentionally doping silicon with various defect centers. In addition, work is directed
toward enhancing the usefulness of these measurements. For example, the measurements
as described here are limited in that chips must be mounted on TO-5 headers. A hot and
cold stage is under development that will allow these measurements to be made in wafer
form providing rapid feedback for process control.

The material presented here is available in various written forms. Two journal
articles [1], [2], have been published and a third is in preparation [3]. Many of the
details have been published in the NBS quarterly reports issued by the Electronic Tech-
nology Division. For these or other technical information, please contact me, Martin
Buehler, National Bureau of Standards, Building 225, Room B-346, Washington, D. C. 20234.

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[1] Buehler, M. G., Impurity Centers in PN Junctions Determined from Shifts in the
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$\quad$ in Silicon p-n Junctions, *Semiconductor Silicon/1973*, H. R. Huff and R. R. Burgess,
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[3] Buehler, M. G., and Phillips, W. E., Gold Acceptor Observed in a Silicon p^+-n Junc-
$\quad$ tion and a n-type MOS Capacitor by Dynathermal Capacitance and Current Measurements,
$\quad$ accepted for publication in *Solid-State Electronics*.

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16. ABSTRACT (*A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.*)

Two measurement methods are described which detect and characterize defects which can control such device characteristics as lifetime and junction leakage. The methods can be used as diagnostic tools in the fabrication of bipolar and MOS devices. The number of different kinds of defects and their densities may be obtained with little effort and simple apparatus. Positive identification of these defects may be obtained with more effort and more sophisticated apparatus. Of more importance, the measurements characterize defects in an environment which is identical to that of the finished product. Thus, the answers derived are directly applicable to process control and device design.

These methods involve thermally stimulated capacitance and current measurements which utilize the ability of defects in the vicinity of a p-n junction or in an MOS capacitor to trap holes or electrons and emit them after receiving sufficient thermal energy. Values for defect densities, energy levels, and emission rates can be derived from these measurements. The limit of detectability can be as low as 10^{10} defects/cm^3. These values provide sufficient information to positively identify the defects.

Three vehicles are used to illustrate the methods: a gold doped $n+$-p diode, a $p+$-n diode with a process-induced defect center, and a gold doped n-type MOS capacitor. Two cryostats are described which have a maximum heating rate of 10 K/s.

17. KEY WORDS (*six to twelve entries; alphabetical order; capitalize only the first letter of the first key word unless a proper name; separated by semicolons*) Cryostat; defects; gold-doped silicon; measurement methods; microelectronics; MOS capacitor; p-n junctions; semiconductors; silicon; thermally stimulated capacitance; thermally stimulated current.

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