Semiconductor Measurement Technology

Progress Report
July 1 to December 31, 1975

NATIONAL BUREAU OF STANDARDS

The National Bureau of Standards [1] was established by an act of Congress March 3, 1901. The Bureau's overall goal is to strengthen and advance the Nation's science and technology and facilitate their effective application for public benefit. To this end, the Bureau conducts research and provides: (1) a basis for the Nation's physical measurement system, (2) scientific and technological services for industry and government, (3) a technical basis for equity in trade, and (4) technical services to promote public safety. The Bureau consists of the Institute for Basic Standards, the Institute for Materials Research, the Institute for Applied Technology, the Institute for Computer Sciences and Technology, and the Office for Information Programs.

THE INSTITUTE FOR BASIC STANDARDS provides the central basis within the United States of a complete and consistent system of physical measurement; coordinates that system with measurement systems of other nations; and furnishes essential services leading to accurate and uniform physical measurements throughout the Nation's scientific community, industry, and commerce. The Institute consists of the Office of Measurement Services, the Office of Radiation Measurement and the following Center and divisions:

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Standards Application and Analysis — Electronic Technology — Center for Consumer Product Technology: Product Systems Analysis; Product Engineering — Center for Building Technology: Structures, Materials, and Life Safety; Building Environment; Technical Evaluation and Application — Center for Fire Research: Fire Science; Fire Safety Engineering.

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Computer Services — Systems and Software — Computer Systems Engineering — Information Technology.

THE OFFICE FOR INFORMATION PROGRAMS promotes optimum dissemination and accessibility of scientific information generated within NBS and other agencies of the Federal Government; promotes the development of the National Standard Reference Data System and a system of information analysis centers dealing with the broader aspects of the National Measurement System; provides appropriate services to ensure that the NBS staff has optimum accessibility to the scientific information of the world. The Office consists of the following organizational units:

Office of Standard Reference Data — Office of Information Activities — Office of Technical Publications — Library — Office of International Relations — Office of International Standards.

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PREFACE

The Semiconductor Technology Program serves to focus NBS efforts to enhance the performance, interchangeability, and reliability of discrete semiconductor devices and integrated circuits through improvements in measurement technology for use in specifying materials and devices in national and international commerce and for use by industry in controlling device fabrication processes. Its major thrusts are the development of carefully evaluated and well documented test procedures and associated technology and the dissemination of such information to the electronics community. Application of the output by industry will contribute to higher yields, lower cost, and higher reliability of semiconductor devices. The output provides a common basis for the purchase specifications of government agencies which will lead to greater economy in government procurement. In addition, improved measurement technology will provide a basis for controlled improvements in fabrication processes and in essential device characteristics.

The Program receives direct financial support principally from two major sponsors: the Defense Advanced Research Projects Agency (ARPA)[*] and the National Bureau of Standards (NBS).[†] In addition, the Program receives support from the Defense Nuclear Agency (DNA),[§] Air Force Space and Missiles Systems Organization,[¶] and the Navy Strategic Systems Project Office.[#] The ARPA-supported portion of the Program, Advancement of Reliability, Processing, and Automation for Integrated Circuits with the National Bureau of Standards (ARPA/IC/NBS), addresses critical Defense Department problems in the yield, reliability, and availability of digital monolithic integrated circuits. Other portions of the Program emphasize aspects of the work which relate to the specific needs of the supporting agency. Measurement oriented activity appropriate to the mission of NBS is an essential aspect in all parts of the Program.

Essential assistance to the Program is also received from the semiconductor industry through cooperative experiments and technical exchanges. NBS interacts with industrial users and suppliers of semiconductor devices through participation in standardizing organizations; through direct consultations with device and material suppliers, government agencies, and other users; and through periodically scheduled symposia and workshops. In addition, progress reports, such as this one, are regularly prepared for issuance in the NBS Special Publication 400-sub-series. More detailed reports such as state-of-the-art reviews, literature compilations, and summaries of technical efforts conducted within the Program are issued as these activities are completed. Reports of this type which are published by NBS also appear in the Special Publication 400- sub-series. Announcements of availability of all publications in this sub-series are sent by the Government Printing Office to those who have requested this service. A request form for this purpose may be found at the end of this report.

Another means of interaction with the electronics community is by direct contact. In particular, comments from readers regarding the usefulness of the results reported herein and relating to directions of future activity in the Program are always welcome.

Disclaimer

Certain commercially available materials or instruments are identified in this publication for the purpose of providing a complete description of the work performed. The experiments reported do not constitute a complete evaluation of the performance characteristics of the products so identified. In no case does such identification imply recommendation or endorsement by the National Bureau of Standards nor does it imply that the items identified are necessarily the best available for the purpose.

SEMICONDUCTOR MEASUREMENT TECHNOLOGY

PROGRESS REPORT
July 1 to December 31, 1975

Abstract: This progress report describes NBS activities directed toward the development of methods of measurement for semiconductor materials, process control, and devices. Both in-house and contract efforts are included. The emphasis is on silicon device technologies. Principal accomplishments during this reporting period included (1) preliminary results of a systematic study of the effects of surface preparation on spreading resistance measurements; (2) development of an optical test for surface quality of sapphire; (3) development of a basis for an exposure sensitivity specification for photoresists; and (4) development of a modular cell concept for test structure design and layout. Also reported are the results of work on four-probe resistivity measurements, comparison of techniques for surface analysis, ion microprobe mass analysis, analysis of process chemicals with flame emission spectrometry, redistribution profiles, thermally stimulated current response of interface states, bias-temperature stress test measurements on MOS capacitors, a high voltage capacitance-voltage method for measuring characteristics of thick insulator films, hydrogen chloride oxidation, ion implantation parameters, methods for determining integrity of passivation overcoats, measurement of free sodium in an oxidation furnace by resonance fluorescence, a square array collector resistor test structure, an electrical alignment test structure, two dimensional wafer maps, test pattern design and analysis for silicon-on-sapphire MOS device technologies, a nondestructive acoustic emission test for beam-lead bonds, wire bond pull test, bondability of doped aluminum metallizations, leakage into double hermetic enclosures, a static expansion dry gas gross leak test, correlation of moisture infusion in semiconductor packages with leak size and device reliability, an automated scanning low-energy electron probe, an optical flying-spot scanner, scanning electron microscopy, scanning acoustic microscopy, and thermal resistance measurements on power transistors and simple integrated circuits. Supplementary data concerning staff, publications, workshops and symposia, standards committee activities, and technical services are also included as appendices.

Key Words: Acoustic emission; Auger electron spectroscopy; beam-lead bonds; bias-temperature stress test; boron redistribution; capacitance-voltage methods; dopant profiles; electrical properties; electronics; four-probe method; hermeticity; interface states; ion implantation; ion microprobe mass analysis; leak tests; measurement methods; microelectronics; moisture infusion; optical flying-spot scanner; passivation overcoats; photoresist; pull test; resistivity; scanning acoustic microscope; scanning electron microscope; scanning low energy electron probe; semiconductor devices; semiconductor materials; semiconductor process control; silicon; silicon dioxide; silicon on sapphire; spreading resistance; test patterns; thermal resistance; thermally stimulated current; ultrasonic wire bonding; voltage contrast mode; X-ray photoelectron spectroscopy.

1. INTRODUCTION

This is a report to the sponsors of the Semiconductor Technology Program on work during the twenty-ninth and thirtieth quarters of the Program. It summarizes work on a wide variety of measurement methods for semiconductor materials, process control, and devices that are being studied at the National Bureau of Standards. The Program, which emphasizes silicon-based device technologies, is a continuing one, and the results and conclusions reported here are subject to modification and refinement.

The work of the Program is divided into a number of tasks, each directed toward the study of a particular material or device property or measurement technique. This report is subdivided according to these tasks. Highlights of activity during the quarters are given in section 2. Subsequent sections deal with each specific task area. References cited are listed in the final section of the report.

The report of each task includes a narrative description of progress made during this reporting period. Additional information concerning the material reported may be obtained directly from individual staff members identified with the task in the report.

Background material on the Program and individual tasks may be found in earlier progress reports as listed in Appendix B. From time to time, publications are prepared that describe some aspect of the program in greater detail. Current publications of this type are also listed in Appendix B. Reprints or copies of such publications are usually available on request to the author.

In addition tutorial videotapes are being prepared on selected measurement topics for dissemination to the electronics community. Currently available videotapes and procedures for obtaining them on loan are also listed in Appendix B.

Communication with the electronics community is a critical aspect both as input for guidance in planning future program activities and in disseminating the results of the work to potential users. Formal channels for such communication occur in the form of workshops and symposia sponsored or co-sponsored by NBS. Currently scheduled seminars and workshops are listed in Appendix C. In addition, the availability of proceedings from past workshops and seminars is indicated in the appendix.

An important part of the work that frequently goes beyond the task structure is participation in the activities of various technical standardizing committees. The list of personnel involved with this work given in Appendix D suggests the extent of this participation. In most cases, details of standardization efforts are reported in connection with the work of a particular task.

Technical services in areas of competence are provided to other NBS activities and other government agencies as they are requested. Usually these are short-term, specialized services that cannot be obtained through normal commercial channels. To indicate the kinds of technology available to the Program, such services provided during the current calendar year are listed in Appendix E.

2. HIGHLIGHTS

Highlights of progress in the various technical task areas of the program are listed in this section. Unless otherwise identified the work was performed at the National Bureau of Standards.

Particularly significant accomplishments during this reporting period included (1) preliminary results of a systematic study of the effects of surface preparation on spreading resistance measurements; (2) development of an optical test for surface quality of sapphire; (3) development of a basis for an exposure sensitivity specification for photoresists; and (4) development of a modular cell concept for test structure design and layout.

Resistivity — The range of validity of existing correction factors for measurement of the resistivity of wafers with finite diameter by the four-probe method was studied experimentally for specimens of intermediate thickness. The results of this study enable measurements of resistivity on specimens in a range of diameter and thickness not previously covered by ASTM standards.

A systematic study of the effect of surface preparation, surface orientation, probe material, and probe condition on measured spreading resistance was nearly completed. The initial results suggest that there is no significant dependence of the form of the relationship between spreading resistance and resistivity on probe material or condition; however, statistically significant differences were observed between wafers of various surface orientation and conductivity type for all probe materials. In addition, differences were observed between various surface preparation techniques.

Further work on the development of the high-speed spreading resistance probe at RCA Laboratories was concerned principally with the problem of excessive probe wear.

Physical Analysis Methods — Comparison of impurity profiles measured by ion microprobe mass analysis, Auger electron spectroscopy, and x-ray photoelectron spectroscopy showed that in the absence of calibration standards, only relative results could be obtained. Further, in the case of the latter two spectroscopies, difficulties were encountered in calibrating the penetration depth so that both the density and depth scales could only be determined on a relative basis.

Development of calibration standards for ion microprobe mass analysis at Texas Instruments continued with characterization of machine parameters, characterization of silicon wafers to be used for specimen preparation, and implantation of specimens with phosphorus dots.

Initial results of the study of Auger electron spectroscopy, being conducted jointly by Stanford University and Varian Associates, included observation of the desorption of oxygen by an electron beam on both silicon dioxide and unsaturated silicon oxides and the use of the chemical shift of the Auger Si_{KLL} transition to develop a model for the silicon-silicon dioxide interface. The latter data suggest that the microscopic mixture model is preferred to the random bonding model for unsaturated silicon oxides. In addition, results were obtained relating to ion penetration depth, ion stimulated Auger transitions, and carbon contamination.

Sodium contamination in a variety of materials used for fabrication of semiconductor devices was determined by means of flame emission spectrometry. This technique provides a sensitive method for monitoring trace sodium content in both solid and liquid materials. No significant trends in sodium contamination level were observed when the results obtained were compared with the results published 2 to 7 years ago.

Additional work on the rapid, nondestructive infrared reflectance technique being developed at RCA Laboratories to determine the surface quality of sapphire substrates has demonstrated that there is correlation between the infrared reflectance signal and the surface roughness of a substrate.

Test Structure Applications — The boron redistribution profile of an oxidized silicon wafer was measured by means of the dynamic MOS C-V deep depletion method; the experimentally measured profile could be fitted by that derived theoretically if appropriate values of the boron diffusion and distribution coefficients were chosen.

The thermally stimulated current response of the energy states found at the oxide-silicon interface of an *n*-type MOS capacitor were observed. The response can be modeled by a continuum of energy levels in the forbidden gap of silicon, but no detailed analysis was undertaken.

Comparison of flat band voltage shifts obtained by means of the bias-temperature stress test before and after electron beam irradiation without bias suggests that there is a correlation between the shift due to radiation and the mobile charge density in the oxide and that irradiation does not appear to affect the density of mobile charge. No further work on the bias-temperature stress test is planned.

Further instrumental improvements were made in the extended-range high voltage capacitance apparatus being developed at RCA Laboratories to measure capacitance-voltage characteristics of thick insulators. The previously incorporated bias protection circuitry was shown to be effective in preventing damage to the capacitance meter following breakdown of the specimen.

Materials and Procedures for Wafer Processing — In connection with the development of qualification procedures for oxidation furnaces, a tunable dye laser has been used to detect, by means of resonance fluorescence, sodium in an open quartz tube oxidation furnace operated at 1000°C. The detection limit for free sodium was estimated to be approximately 5×10^5 cm^{-3}. A sodium density of about 2×10^7 cm^{-3} was observed in an intentionally contaminated furnace; preliminary analysis suggests that much more sodium is present in other forms than is present as free sodium and that, even with its great sensitivity, the resonance fluorescence technique may be inadequate for monitoring sodium contamination during oxidation.

Data collection continued in connection with the study of ion implantation parameters at Hughes Research Laboratories. The characteristics and limitations of the Schottky barrier capacitance-voltage technique for measuring implanted profiles were investigated for various experimental conditions. Additional data were collected on profiles for a number of impurities; preliminary data were obtained on the sensitivity of the profile to the angle of incidence and crystallographic direction. In addition, initial experiments related to measurement of total dose were carried out with emphasis on the study of suppression of secondary electron emission; these results will be reported in detail at a later date.

In the study of methods for measuring the integrity of passivation overcoats at RCA Laboratories, optimum etch conditions were established for use with the selective chemical etch method, nonluminescing materials were found to be less suitable than luminescing materials for defect decoration, and the corona decoration method was shown to be superior to the more commonly employed electrophoretic cell method.

In the study of methods for characterizing process chemicals, being conducted at Pennsylvania State University, calculations of the equilibrium partial pressures of the various species in the chlorine-hydrogen-oxygen system was carried out. The effect of the presence of excess water vapor was also investigated. Comparison with published experimental data suggests that the chlorine pressure is the critical parameter and that it can be controlled by a combination of the amount of added hydrogen chloride gas and the water vapor concentration.

Photolithography — An analysis of the photoresistance exposure process was undertaken to establish a basis for specification of exposure sensitivity. The results suggest that a set of material-related parameters can be used to determine the speed of photoresist materials appropriate to a particular exposure apparatus.

Analysis of automated methods for inspecting photomasks was completed at Lawrence Livermore Laboratories; a report on this work is being prepared. Preliminary evaluation of a diffraction-based optoelectronic method for measuring small dimensions was completed at Recognition Systems, Inc. In this work, which will be reported in detail at a later date, it was shown that resolution comparable with that obtained in the scanning electron microscope could be achieved without the necessity of a vacuum chamber.

Theoretical studies have been initiated on the effect on the adjacent line on line-width measurements with an optical microscope used in the conventional fashion. In addition, work has been initiated on application of the spatial filtering technique to line-width measurement with an optical microscope. Preliminary results have been obtained in both studies and detailed reports are being prepared.

Test Patterns — The square array collector resistor test structure was analyzed to determine correction factors for use when the backside of the structure is conducting. It was found that the correction can be ignored for most cases of practical interest.

An electrical test structure was designed for the purpose of evaluating the amount of misalignment between emitter and base regions in a bipolar process.

Investigation of modular concepts for test structure design and test pattern layout led to the selection of a rectangular cell with a 2 by 10 probe pad array as the basis for standardization. Modularization of the pattern in the cells is crucial to the testing strategy and permits standardization of the entire test structure design including probe pads and metallization runs. In order to implement these concepts in connection with a specific integrated circuit technology, a T^2L test pattern which includes a simple NAND gate is being designed and fabricated.

Computer programs were developed to permit the display of the geometrical variation of parameters obtained from measurements on test structures as whole wafer density maps. The program permits interpolation of data between actually measured points which facilitates the interpretation of the wafer map.

The design of the test structures for use in the test pattern being developed at RCA Laboratories for SOS/LSI technology was completed and fabrication of the mask set was initiated.

Interconnection Bonding — Procedures were refined for fabricating beam-lead devices with a few weak bonds for use in studying the nondestructive acoustic emission test for evaluating the quality of beam-lead bonds. In addition, several instrumental changes were made to improve detection sensitivity. In the course of this study, a novel method was developed to determine the downward force necessary to produce threshold deflections of a bonded beam-lead die.

A study showed that there is no dependence of the measured pull strength on the rate of pull of ultrasonic gold wire bonds. A similar result had been obtained previously for ultrasonic aluminum wire bonds, but verification for gold wire was desired to increase the scope of a pull test method being developed by ASTM Committee F-1 on Electronics. During this study it was found that a double deep-grooved bonding tool was most suitable for making ultrasonic bonds with fine gold wire.

The suitability of silicon- and copper-doped aluminum metallizations for ultrasonic bonding of aluminum ribbon and round wire was determined. A satisfactory bonding schedule could be developed for all metallizations studied; as with pure aluminum metallization, it was found that ribbon wire exhibited a higher pull strength for a broader range of bonding conditions than round wire.

Hermeticity — An analysis was made of the infusion of dry gas into a hermetic double enclosure with specified leak sizes in each container. It was found that simply surrounding one hermetic enclosure by another does not assure hermetic improvement, although it is obviously a protection against a badly leaking inner enclosure. Significant enhancement was obtained only if the leak size in the outer enclosure was less than 10 times that of the inner enclosure or if the free volume of the outer enclosure was at least 10 times that of the inner one.

The dry gas, static-expansion, differential-pressure gross leak test was analyzed to determine the relationship between the meter indication and leak size in the device under test. It was found that the leak size is related to the rate of rise of the meter indication at very early times and that the internal free volume of the device under test is related to the equilibrium indication.

The initial effort on moisture measurements in integrated circuit packages was completed at Martin Marietta-Orlando. Preliminary calibrations were run on the dew point sensors and an instability of the microvent leaks which was observed under pressure was corrected by modifying the design.

Device Inspection and Test — The automated scanning low energy electron probe, being developed at the Naval Research Laboratory, was applied to the study of wafer defects. Evidence of both surface contamination and crystal defects was observed, but additional work will be necessary to permit detailed correlation of the observations with appropriate causes.

The photoresponse of the substrate diode of an integrated circuit to low-power 1.15-μm laser irradiation was calibrated in terms of device temperature as an additional example of the usefulness of the optical flying-spot scanner for thermal mapping. Significant deviations from the curve predicted by simple theory were observed at temperatures above about 75°C.

Tests of the cylindrical secondary electron detector intended to improve the sensitivity

of the scanning electron microscope in the voltage contrast mode showed that the voltage sensitivity was substantially improved. However, as it is presently constructed, the spatial resolution of this detector is inadequate for use in examining integrated circuits; additional modifications are not planned at the present time.

Studies of scanning acoustic microscopy as a technique for the inspection of semiconductor devices and integrated circuits were initiated at Hughes Research Laboratories and Stanford University. This technique has been shown to have 2-μm resolution and it is thought to be capable of observing subsurface defects.

Thermal Properties of Devices — It was found that the electrical switching transients which occur on switching a transistor out of the quasi-saturation mode do not permit ac-

curate measurements of thermal resistance to be made using the standard emitter-only switching technique. This mode of operation occurs in some devices under the high current, low voltage conditions often used for making thermal resistance measurements.

A study of several techniques for measuring thermal resistance of integrated circuits was completed. It was found that the forward voltage of the collector-substrate isolation junction is not a satisfactory temperature sensitive parameter for determining the peak temperature of an integrated circuit. Peak temperature determination by electrical means appears to be possible only if the heat generating element is accessible at the pins of the circuit. The sensitivity of the forward voltage of the isolation junction as the temperature sensitive parameter for determining the quality of the die attach of integrated circuits remains to be evaluated.

3. RESISTIVITY

3.1. Four-Probe Method

Resistivity measurements by the four-probe method are covered by ASTM standard test methods only if the slice thickness is less than the probe spacing [1] or if it is greater than four times the probe spacing [2]. Slices with thickness between one and four times the probe spacing are frequently used for production control of silicon crystal growth and for spreading resistance calibration sets. This task was undertaken to identify appropriate geometrical correction factors for use in this range.

Geometrical correction factors in these standards are derived from the basic equation for resistivity, ρ, measured with a collinear, equally-spaced, four-probe array [3]:

$$\rho = 2\pi s \frac{V}{I} , \tag{1}$$

where V is the potential difference between the inner pair of probes, I is the current between the outer pairs of probes and s is the spacing between adjacent probes. The ASTM method for four-probe measurements on semi-infinite solids [2] requires the use of no correction factors for geometry; eq (1) is corrected only for non-uniform probe spacing and for temperature variation of resistivity:

$$\rho = 2\pi s F_{sp} F_T \frac{V}{I} , \tag{1a}$$

where $F_{sp}' = 1 + 1.25[1-(s_2/s)]$. s_2 is the spacing between the inner two probes, s is the average probe spacing, $F_T = 1 - C_T(T-23)$, C_T is the temperature coefficient of resis-

Table 1 — Values of the Correction Factor $G_7(w/s)$ for Finite Specimen Thickness

w/s	$G_7(w/s)$
1.000	1.5045
2.000	1.0939
3.000	1.0306
4.000	1.0134
5.000	1.0070
6.000	1.0041
7.000	1.0026
8.000	1.0017
9.000	1.0012
10.000	1.0007

tivity [1], and T is the temperature, in degrees Celsius, of the specimen at the time of measurement. In this method it is stated that the maximum error introduced by geometrical effects is less than 2 percent if the thickness of the specimen and the distance from any probe to the nearest point on the edge are at least four times the probe spacing.

Valdes [3] derived, from the method of images, a factor, $G_7(w/s)$ to correct eq (1) for finite thickness, w:

$$\rho = \frac{2\pi s}{G_7(w/s)} \frac{V}{I} , \tag{1b}$$

where $G_7(w/s)$ is tabulated in table 1. In the limit of a very thin sheet, $G_7(w/s)$ approaches the value of $(2s/w) \ln 2$ and the resistivity becomes

$$\rho = \frac{\pi}{\ln 2} w \frac{V}{I} . \tag{2}$$

Smits [4] has reported an equivalent factor, $F(w/s)$, calculated from formulae given by Uhlir [5], to correct eq (2) for finite values of w:

$$\rho = \frac{\pi}{\ln 2} w F(w/s) \frac{V}{I}, \tag{2a}$$

where $F(w/s) = 2 \ln 2 \, s/[w \, G_7(w/s)]$. For $0 \leq w \leq (s/2)$, $F(w/s)$ lies between 1.0000 and 0.9974.

Smits [4] also calculated a factor, C, to correct eq (2) for measurements at the center of a circular specimen of finite diameter:

$$\rho = wC \frac{V}{I} , \tag{2b}$$

where C has the value $\pi/\ln 2 = 4.532$ in the limit of infinite diameter.

The ASTM method for four-probe resistivity measurements on circular slices [1] assumes that correction factors $F(w/s)$ and C^* can be combined multiplicatively provided that $w \leq s$ and the diameter, $d \geq 10s$:

$$\rho = wC \, F(w/s) \frac{V}{I} . \tag{2c}$$

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* The factor C is designated F_2 in ASTM Method F 84.

The method also provides other multiplicative correction factors to account for non-uniform probe spacing and for temperature variation of resistivity:

$$\rho = wC \ F(w/s) \ F_{sp} F_T \frac{V}{I} \ , \qquad (2d)$$

where in this case $F_{sp} = 1 + 1.082[1-(s_2/s)]$. Thus the regime $s \leq w \leq 4s$ is not covered by either standard method. Since analytical determination of appropriate correction factors for thick specimens with small diameter appears to be intractable, an empirical study was carried out.

A 21-mm thick slice was cut from a 3-in. (76-mm) diameter p-type silicon crystal with a nominal room temperature resistivity of 10 $\Omega \cdot$cm. Only the central 1.0-in. (25 mm) diameter region was used since the radial resistivity variation in the remainder of the slice was judged to be too great for use. The resistivity was measured at the center of the slice with a four-probe array with the standard [1] 1.59 mm probe spacing. The slice was fractioned and the resulting slices were repetitively thinned and remeasured at the center until the thickness was about 1 mm. Slices with thickness between about 5 mm and 1 mm were also measured with a probe with nominal 1.0 mm spacing. The results, expressed as the percent difference between resistivity calculated from measurements in the thinnest slices using eq (2d) and the resistivity calculated using either eq (2d) or (1a) as a function of slice thickness normalized by probe spacing, are plotted in figure 1.

Although some scatter would be expected since each of the measured V/I ratios has an uncertainty typified by a relative sample standard deviation of 0.3 to 0.5 percent, data from a given slice tended to be grouped along a well defined curve. It can be seen that if eq (2d) is used when $w/s \leq 2.5$ and if eq (1a) is used when $w/s \geq 2.5$, errors introduced by geometrical considerations are less than 2 percent provided the measurement is made at the center of the slice and provided that the diameter is at least 16 times the probe spacing. For larger diameter slices, smaller errors are expected.

<div align="right">(J. R. Ehrstein and D. R. Ricks)</div>

3.2. Spreading Resistance Methods

An extensive series of experiments was undertaken to determine the effect of specimen
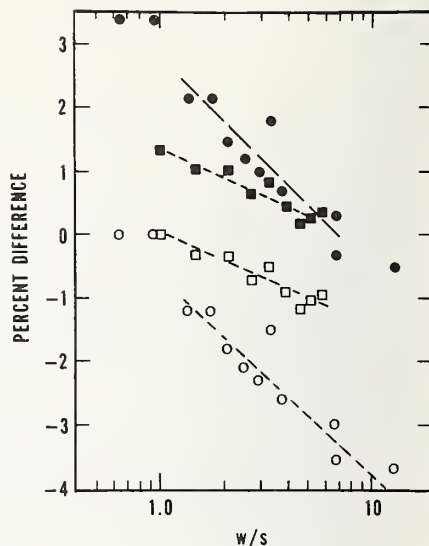
Figure 1. Percent difference between calculated and actual resistivity as a function of the ratio of the thickness, w, of a 25-mm diameter slice to the probe spacing, s. (circles: s = 1.59 mm; squares: s = 1.02 mm; solid points: calculated from eq (1a); open points: calculated from eq (2d).)

surface preparation and probe material on the empirical calibration between specimen resistivity and spreading resistance. These results are prerequisite to the investigation of the validity of using bulk silicon specimens to calibrate spreading resistance measurements on epitaxial silicon wafers.

In the present study specimens were cut from 1.5- to 2.0-in. (38- to 51-mm) diameter Czochralski-grown silicon crystals. Fifteen crystals each of n- and p-type silicon were grown in the [111] direction and twelve crystals of n-type silicon were grown in the [100] direction. Crystal orientation was specified to ±3 deg and was not rechecked at NBS.

Slices 0.25-in. (6.3 mm) thick were cut perpendicular to the growth axis of each crystal to provide specimens with exposed (111) or (100) faces. Extra slices 0.12-in. (3.0-mm) thick were cut from seven [111] crystals of each type; these were used to provide specimens with exposed (110) faces by cutting along the diameter parallel to the orientation flat. The slices, except for those cut from three high resistivity [111] n-type crystals had a resistivity range not exceeding 5 percent between half radius points along a diameter. The resistivity was measured at

the center of each slice by the four-probe method (see sec. 3.1.); it was judged to be known to ±2 percent except for the slices with excessive resistivity variation for which it was judged to be known to ±3 percent. For each set of like orientation and conductivity type the resistivities were distributed relatively uniformly over the range 10^{-3} to 10^2 $\Omega \cdot$cm.

Rectangular parallelipipeds, 0.50-in. (12.7-mm) long and 0.25-in. (6.3 mm) thick, were cut from the central region of each slice along a diameter. The width of the oriented face varied from 1.3 to 3.0 mm depending on the number of slices in the set; the total width of all specimens in a set was about 20 mm. Sets of like orientation and conductivity type were mounted on a common block as shown in figure 2, with the oriented face upward and arranged so that the resistivity was a somewhat random function of position. The common mounting and partial randomization were to ensure that surface preparation would be as nearly identical for all specimens in a group and that there would be no systematic relationship between surface preparation and resistivity.

Six different surface preparations are being studied: lap with 5-μm alumina, chemical polish with CP₄ etch [6], chem-mechanical polish with slica sol [7], chem-mechanical polish with zirconium silicate [8], mechanical polish with 0.3-μm alumina polish in aqueous slurry, and mechanical polish with 0.3-μm alumina in a non-aqueous commercial thinner designed for diamond polishing. Measurements are being made with four probe ma-

terials: tungsten-ruthenium alloy of nominal radius 0.75 mil (19 μm) [9], tungsten carbide of nominal radius 1.0 mil (25 μm) [10], osmium of nominal radius 1.0 mil (25 μm) [11], and osmium-tungsten alloy of nominal radius 1.0 mil (25 μm) [12]. Two sets of the last type of probes were used; one set was relatively blunt from extensive use while the other was new and freshly conditioned [13].

A commercial two-probe instrument which determines the logarithm of the ratio of the current through the probes to a current through a standard resistor, each driven by a constant, 10-mV source is being used to make the spreading resistance measurements. The probes, which are loaded with 45 g, are stepped across the composite blocks in a direction perpendicular to the long axis of the parallelepipeds at intervals of 250 μm. Measurements are being made on each block for each surface preparation with each of the five sets of probes. In addition, measurements are being repeated on all surfaces prepared with aqueous media (except CP₄ etch) following a bakeout at about 160°C for 20 min in room air; this bakeout has been observed to greatly improve the spreading resistance measurements on p-type specimens with resistivity of 1 $\Omega \cdot$cm or more [14].

The results obtained so far show no significant dependence of the form of the spreading resistance-resistivity (R_{sp}-ρ) relation on probe material. This is illustrated in figure 3 which shows the results of measurements with the various probe tips on the (111) n-
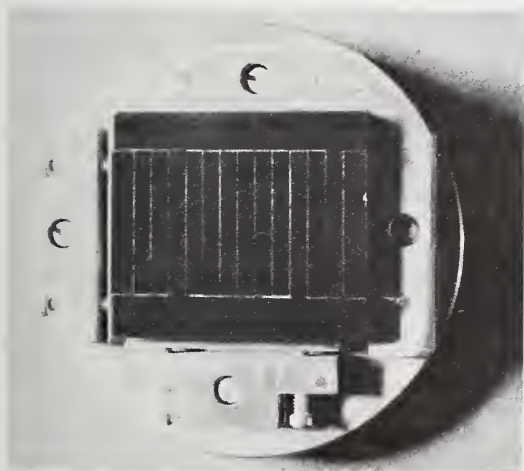
Figure 2. Photograph of typical specimen block.

Figure 3. Ratio of spreading resistance, R_{sp}, to resistivity, ρ, as a function of resistivity as measured with a variety of probe tips on a (111) n-type silicon surface chem-mechanically polished with silica sol and baked out. (●: blunt osmium-tungsten alloy; O: freshly conditioned osmium-tungsten alloy; ■: tungsten carbide; □: tungsten-ruthenium alloy; ▲: osmium.)

Figure 4. Ratio of spreading resistance, R_{sp}, to resistivity, ρ, (logarithmic scale) as a function of resistivity as measured with freshly conditioned osmium-tungsten alloy probe tips on a variety of silicon surfaces chem-mechanically polished with silica sol and baked out. ($\bullet$: (111) n-type; $\blacktriangledown$: (110) n-type; $\bigcirc$: (100) n-type; $\blacksquare$: (111) p-type; $\blacktriangle$: (110) p-type; solid lines are least squares fits to the data with parameters as listed in table 2.)

type silicon surfaces chem-mechanically polished with silica sol and baked out. Differences in absolute value of the spreading resistance response can be seen; these appear to be primarily related to differences in effective contact radius of the various probe tips.

However, statistically significant differences were observed between wafers of various surface orientation and conductivity type for all probe materials. Figure 4 and table 2 illustrate these differences for the case of measurements with the freshly conditioned osmium-tungsten alloy tip on surfaces chem-

Table 2 — Linear Regression Coefficients for Spreading
Resistance Calibration Plots

Surface Orientation	Conductivity Type	b[a]	s_b[a]	m[a]	s_m[a]	Total Data Points	Excluded Data Points[b]
(111)	p	2.926	0.005	-0.020	0.004	15	1-3,15
(111)	n	3.290	0.012	-0.011	0.009	15	1,2
(100)	n	3.169	0.009	-0.032	0.008	12	none
(110)	p	2.872	0.013	-0.036	0.015	7	1,2
(110)	n	3.316	0.023	-0.037	0.019	7	none

[a] $\log(R_{sp}/\rho) = (b \pm s_b) + (m \pm s_m) \log \rho$

[b] Data points (counting from leftmost point) excluded when $R_{sp} < 10\ \Omega$ (see text) except for point 15 for case of (111) p-type case which was apparently high because of incomplete post polish bakeout.

mechanically polished with silica sol and baked out. The calibration plots in the figure are presented as log R_{sp}/ρ against log ρ. As compared with the more usual log R_{sp} against log ρ plots, the present format emphasizes both deviations from linearity in a given plot and differences between plots made for different conditions.

Discrepancies in linearity of the $R_{sp}-\rho$ relationship for resistivities below 0.01 $\Omega\cdot$cm are believed to be instrumental in nature. Shifts in the direction of high spreading resistance were observed for all probe-specimen combinations for which the measured spreading resistance was less than about 10 Ω. One cause may be an increase in series resistance due to spreading resistance into the probe material. Spreading resistances of 1.5 to 2.5 Ω have been measured for the probe materials under several conditions. If this is subtracted from the spreading resistance measured on silicon specimens, an otherwise linear relation is generally continued down to 0.001 $\Omega\cdot$cm. A second possible cause concerns the inability of the current source to operate in the constant voltage mode under the high current conditions associated with small resistive loads.[†]

The response on variously prepared (111) surfaces, both p- and n-type, is illustrated in figure 5 for the case of the freshly conditioned osmium-tungsten alloy tip. For p-type material, the response on the various surface preparations does not appear to be significantly different except that chem-mechanically polished specimens with resistivity 0.5 $\Omega\cdot$cm or more show large fluctuations unless baked out [14]. (The 60 $\Omega\cdot$cm point on the baked out chem-mechanically polished surface is high because of an incomplete bake cycle and should be disregarded.)

[†] The exact cause of the deviation from linearity at low specimen resistivity should have virtually no effect on the interpretation of measurements on bulk specimens having the same surface condition as the calibration specimens. However, interpretation of data on graded or multilayered structures may well be affected depending on the algorithm used, and certainly any detailed modeling of the spreading resistance phenomenon, such as inclusion of pressure dependent effects, will be influenced by an understanding of the dependence of measured spreading resistance upon resistivity.

For n-type material, the response on lapped surfaces is distinctly different from that on polished surfaces. On lapped surfaces, with or without bakeout, a strong peak in the ratio of R_{sp} to ρ is observed for resistivities in the vicinity of 0.1 $\Omega\cdot$cm; the effect is more pronounced after bakeout. Polished surfaces
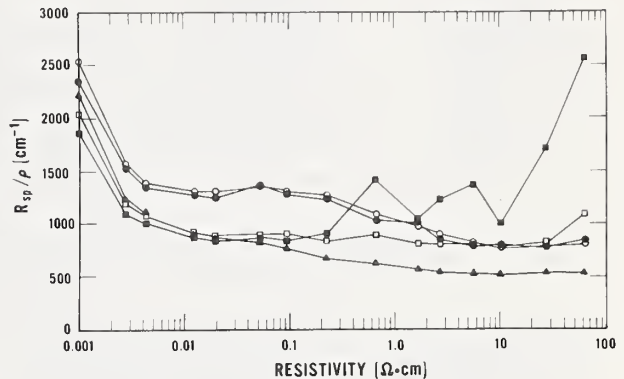
a. p-type.
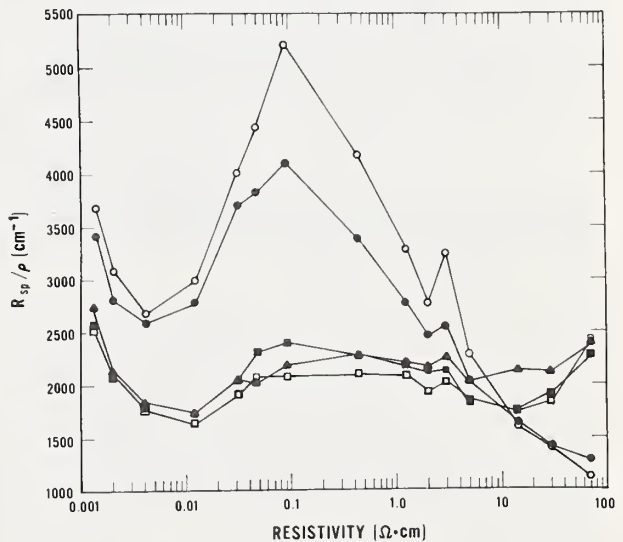
b. n-type.

Figure 5. Ratio of spreading resistance, R_{sp}, to resistivity, ρ, as a function of resistivity as measured with freshly conditioned osmium-tungsten alloy probe tips on (111) p- and n-type silicon surfaces prepared in various ways. (circles: lapped with 5-μm alumina; squares: chem-mechanically polished with silica sol; triangles: mechanically polished with 0.3 μm alumina in non-aqueous thinner; solid points: not baked out; open points: baked out.)
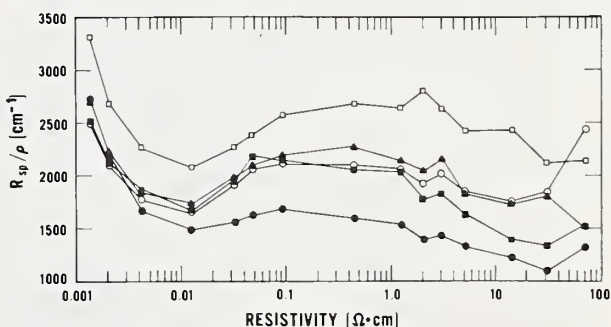
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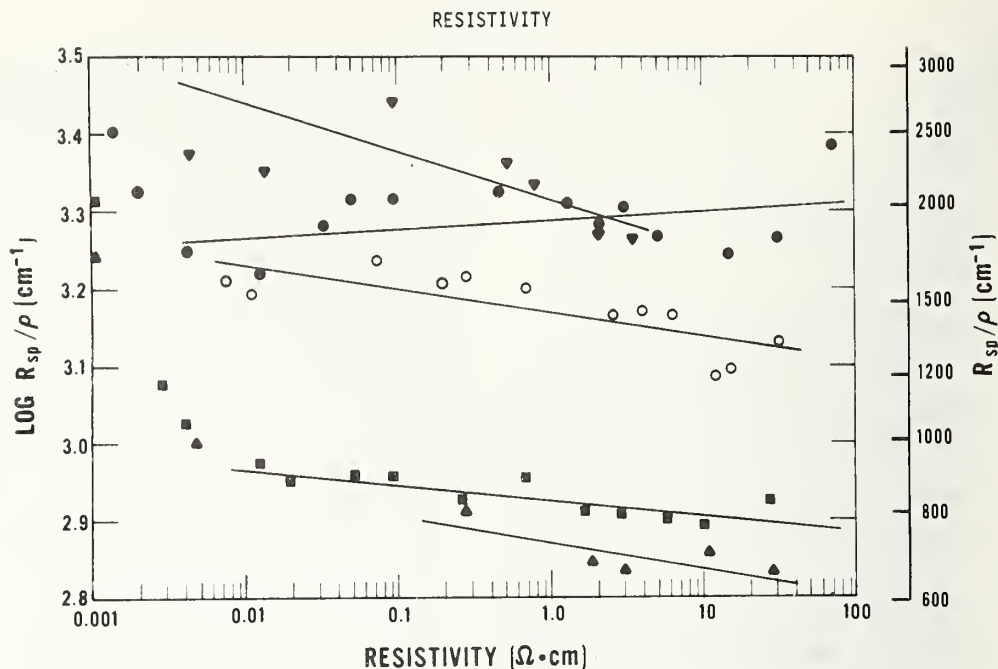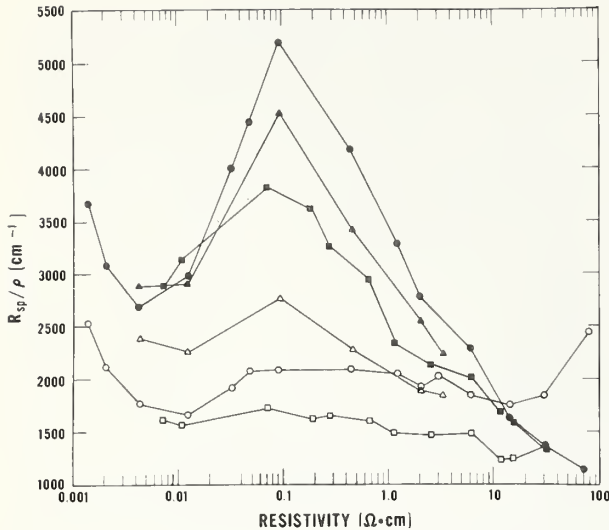
Figure 6. Ratio of spreading resistance, R_{sp}, to resistivity, ρ, as a function of resistivity as measured with freshly conditioned osmium-tungsten alloy probe tips on n-type silicon surfaces showing extremes of behavior. (circles: (111) surface; triangles: (110) surface; squares: (100) surface; solid points: lapped with 5-μm alumina and baked; open points: chem-mechanically polished with silica sol and baked.)

show a more nearly linear response than do the lapped surfaces; the response of surfaces chem-mechanically polished in aqueous media is not improved by bakeout.

Extremes of behavior for three orientations of n-type surfaces are illustrated in figure 6; the measurements reported were made with the freshly conditioned osmium-tungsten alloy tip. The most nearly linear response occurs on the chem-mechanically polished (100) surface; data shown were taken following bakeout but are essentially the same as data taken prior to bakeout.

Additional measurements to complete the matrix are underway; preferred surface preparation procedures can better be established following the conclusion of the experiment.
(J. R. Ehrstein and D. R. Ricks)

3.3. High-Speed Spreading Resistance Probe

Additional tests were conducted with the prototype high-speed spreading resistance probe (NBS Spec. Publ. 400-19, pp. 10-13). The response of the instrument was found to be excessively noisy under light load conditions which are best from the standpoint of probe wear. To correct this problem, hinged probe arm supports, pictured in figure 7, were designed and built. Results of measurements made with the previous holder suggest that the use of probe points with relatively large tip radius minimizes both noise and probe wear. The most suitable tips appear to be those with a large number of small, uniform micropoints; one way to achieve this condition is to dress the points with a stone of 6-μm diamond in an epoxy matrix. Experience with osmium alloy and tungsten carbide probe points with tip radius from 1/4 to 6 mil (6 to 150 μm) showed that wear occurred principally as a result of breakage of micropoints (so that increasingly larger loading was necessary to maintain good electrical contact) or, under heavier loads, shear-type fracture of larger pieces (resulting in the formation of deeply gouged tracks). Small changes in the tip micropoint configuration do not appear to have more than a secondary effect on the relationship between spreading resistance and resistivity.

A compilation of the hardness of silicon and a variety of commercially available point materials is presented in table 3. It was found that the materials which are softer than silicon, hardened Inconel, steel, and tungsten, did not make good contact. The tracks were only faintly visible and the readings were very noisy. Points of all materials harder than silicon, tested to date, produced good track marks when the point tips were in good condition.
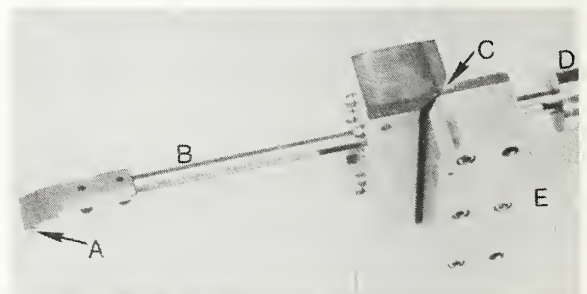
A Probe tip
B Arm
C Hinge
D Counterweight
E Base

Figure 7. Hinged probe-arm assembly.

Table 3 — Hardness of Probe Tip Materials

Material Identification	Constituents	Vickers Hardness[a]	Knopp Hardness[a]
Inconel 718, hardened [15]	nickel-chromium-molybdenum-iron	530	480
Tungsten [11]		535	490
Carbon steel [11]		790-870	730-750
Silicon [11]		1150-1400	900-1110
Carballoy 55A [16]	87% tungsten carbide, 13% cobalt	1180-1380	1000-1200
Carballoy 779 [16]	91% tungsten carbide, 9% cobalt	1300-1400	1150-1250
Osmium Alloy [11]	osmium, tungsten, cobalt	>1150	>1000
Fidelitone K75 [9]	tungsten-ruthenium	1650	1500
Carballoy 883 [16]	94% tungsten carbide, 6% cobalt	1650-1750	1500-1600
Carballoy 895 [16]	94% tungsten carbide, 6% cobalt		2000

[a]Hardness figures quoted are derived from a variety of sources and were obtained by using different methods. Therefore comparisons between various materials are not precise and the data given should be used only as a rough guide.

The instrument was shown to respond to various surface preparations in a manner similar to that previously found using a commercially available stepping-type instrument although the traces on the high-speed instrument were frequently somewhat noisier. For example, the effects of the strong inversion layer on air-dried chem-mechanically polished p-type (111) surfaces were removed by baking in air at 160° to 170°C for 15 min while no such effect was observed on chem-mechanically polished n-type (100) surfaces. Beveled speci-mens, prepared by high-speed diamond grinding [15] showed no distinct step in resistance when traversing from the original surface of the wafer onto the beveled surface. Repeated traces (slightly displaced) along the diameter of a heavily striated wafer, taken with an osmium alloy tip of 0.4-mil (10-μm) radius loaded with 60 g, were able to resolve features 50 to 100 μm in extent. It was possible to traverse a 3.0-in. (76-mm) diameter, taking a measurement every 250 μm, in 5 min with a reset time of 3-1/3 min.

(A. Mayer[§] and N. Goldsmith[§])

[§]Work performed at RCA Laboratories under NBS Contract No. 5-35914. NBS contact for additional information: J. R. Ehrstein.

4.1. Comparative Study of Surface Analysis Techniques

Several other aspects of the comparative study of surface analysis techniques (NBS Spec. Publ. 400-12, pp. 17-18) have been completed. The boron-implanted silicon specimen was profiled by secondary ion mass spectrometry (SIMS) using two different instruments, a direct imaging ion microscope and an ion microprobe. The specimen was a phosphorus-doped silicon wafer with room temperature resistivity in the range 5 to 10 $\Omega\cdot$cm and (100) surfaces. The 150-keV ^{11}B implant was misaligned by 7 deg with respect to the [100] direction to minimize channelling effects and then annealed at 1000°C in a non-oxidizing atmosphere for 1 h to electrically activate the boron.

Both SIMS studies employed an O_2^+ primary ion beam for sputtering while positive secondary ions ($^{11}B^+$, $^{30}Si^+$) were collected for analysis. A 5.5-kV gun-to-specimen primary ion accelerating voltage was used for the ion microscope analysis. The primary ion beam, carrying a current of 200 nA, was focussed to a 100-μm beam diameter and rastered over a square area, 350 μm on a side; this technique produces a crater with a flat bottom even if the current density is not uniform across the beam diameter. A mechanical aperture inserted at the focal plane of the ion microscope was used to stop-down the secondary ion collection area to the central 200-μm region of the crater to eliminate crater wall effects that could otherwise obscure the depth profile. The analyzer slits were set to give a mass resolution $m/\Delta m = 50$ at 10-percent valley. The ion microprobe was operated at a 20-kV accelerating voltage with a 35-nA beam focussed to a 10-μm spot and rastered over a 100-μm by 80-μm area. Electronic gating was used to restrict the region from which secondary ions were collected to the central 50-μm by 40-μm part of the analysis crater. The resolution of the mass analyzer was set so that $m/\Delta m = 190$ at 10-percent valley.

The boron counting rate measured as a function of time was normalized at every instant to the silicon counting rate to minimize the dependence of the boron signal on variations in the operating conditions of the instrument and on minor inhomogeneities in the matrix. The sputtering time was converted to a depth scale through the sputtering rate which was assumed constant and was determined by dividing the final crater depth, measured by stylus profilometry, by the total analysis time.

Both measurements indicated that the peak of the distribution occurred at 390 nm and, except in the tail of the distribution at large depths (where, because of the low boron densities involved, instrumental artifacts are expected to play an increasingly important role), the relative magnitudes agreed well with each other. The peak location, which was expected to remain essentially fixed during the anneal, is much shallower than the value of 570 nm predicted by the calculations of Johnson and Gibbons [18]. However, other workers [19,20] have also reported values around 400 nm and recent calculations [21] give a value of 420 nm. It should be noted that, because of the absence of calibration standards, only relative density scales were reported for both measurements.

The profile of the zinc-implanted specimen, which was much more heavily doped, was measured by Auger electron spectroscopy (AES) and x-ray photoelectron spectroscopy (XPS) as well as by SIMS. The profiles obtained are plotted in figure 8. Note that both scales are normalized. The SIMS profile
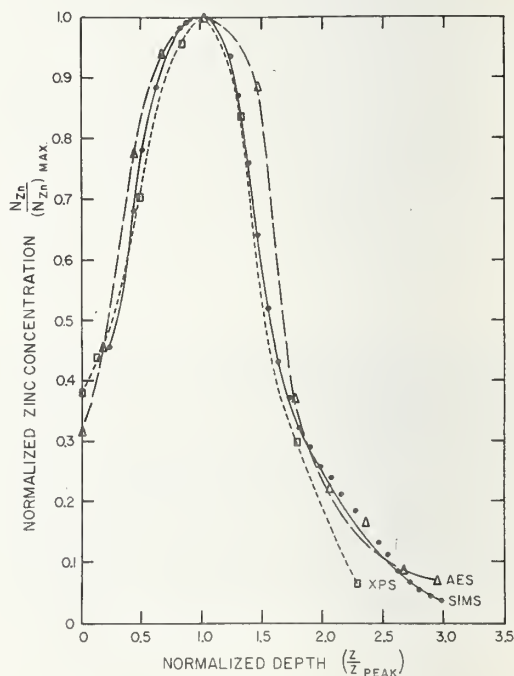
Figure 8. Normalized zinc concentration depth profiles as measured by secondary ion mass spectrometry, Auger electron spectroscopy, and x-ray photoelectron spectroscopy.

was obtained with the ion microscope as described above except that $^{65}Zn^+$ ions were collected for analysis rather than $^{11}B^+$. The intensities of the zinc 994-eV Auger electron peak and the zinc $3p_{3/2}$ photoelectron peak were used to infer the profiles in the AES and XPS measurements, respectively. While these profiles appear to agree on the normalized basis shown, the position of the peak of the distribution, the range straggling, and the density levels do not agree on an absolute basis. Much of the difference is attributed to differences in the sputter etch characteristics of the crater [22].

Because SIMS is plagued by severe matrix dependent variations of the ionization yields and ill-defined sputtering rates, the true compositional profile and the measured data curve may not bear an exact likeness. Nevertheless, SIMS remains the most sensitive of all the profiling methods considered here with the detection limits for some elements reaching into the parts per billion range. In addition, SIMS can have excellent lateral resolution ($\sim$1 μm) making it suitable for microelectronic device analysis.

By comparison to SIMS, matrix effects in AES and XPS are relatively minor, although in XPS, matrix effects are advantageously used to determine the chemical state of the detected species. The shallow escape depths ($\sim$1 nm) of the detected electrons make these spectroscopies ideal for studying impurities on surfaces and at interfaces. (A. G. Lieberman)

4.2. Calibration Standards for Ion Microprobe Mass Analyses

Ion microprobe mass analyses (IMMA) and neutron activition analyses (NAA) were completed on the 12 wafers being used for evaluation of substrate impurity content (NBS Spec. Publ. 400-19, pp. 20-22). The results of the analyses are summarized in table 4. The neutron activation analyses clearly showed that the impurities in the substrate material are well below the detection limits of the IMMA technique. The ion microprobe mass analyses found only a normal background of 2 to 5 counts per second except for ^{31}P and ^{75}As, where the SiH^+ and Si_2O^+ molecular ions contribute to the signal.

The ion microprobe measurements were made using the parameters most frequently used for depth distributions. The primary sputter source was 20-kV O_2^+ with 30-nA current

Table 4 — Substrate Purity Evaluation

Ion Microprobe Mass Analysis (counts per second)					
Specimen	^{23}Na	^{31}P	^{52}Cr	^{75}As	^{197}Au
Silicon-1	3	47	4	3	6
Silicon-3	2	29	3	11	6
Silicon-5	1	18	1	2	2
Silicon dioxide-7	2	32	3	9	3
Silicon dioxide-9	3	27	3	17	4
Silicon dioxide-11	4	32	2	14	4

Neutron Activation Analysis (parts per million, atomic)					
Specimen	^{23}Na	^{31}P	^{52}Cr	^{75}As	^{197}Au
Silicon-2	0.001	<1	<5	<0.01	5×10^{-6}
Silicon-4	0.001	<1	<5	<0.01	5×10^{-6}
Silicon-6	0.001	<1	<5	<0.01	$<1.5 \times 10^{-5}$
Silicon dioxide-8	<2	<1	<50	<0.5	<0.01
Silicon dioxide-10	2	<1	<50	<0.5	<0.01
Silicon dioxide-12	<2	<1	<50	<0.5	<0.01

focussed to a 20-μm spot and swept in a 100-
μm by 80-μm raster. The secondary ions were
detected from the central one-fourth of the
sputtered area using a mass resolution (m/Δm
at 10-percent valley) of 190. The secondary
ion counts were collected in groups of 100
ten-second counting periods. The results re-
ported are the mean of each group of 100 di-
vided by 10.

Preliminary measurements on an initial group
of phosphorus-implanted microvolumes show
that the SiH$^+$ molecular interference plays
a major role particularly when the phos-
phorus-implanted region is small compared
with the total acceptance area.
                    (R. Dobrott[*] and G. B. Larrabee[*])

4.3. Electron Spectroscopy Techniques

This task was undertaken to investigate
various aspects of Auger electron spectros-
copy (AES) and photoelectron spectroscopy
(PES) in conjunction with ion sputter or
other methods of etching as applied to the
examination and analysis of MOS device struc-
tures. Application areas of particular sig-
nificance are the characterization of oxide-
semiconductor interfaces and of the associ-
ated oxide films and the characterization of
metal-metal, metal-oxide, and metal-semicon-
ductor bonds.

Initial efforts in this task are concerned
primarily with investigation of ion profil-
ing phenomena and Auger electron spectros-
copy. In the former area, surface rough-
ness effects, preferential etching effects,
ion beam effects, and effects of contami-
nation in the ion source gas are being
studied. In the latter, emphasis is being
placed on determination of electron beam
induced surface damage and extraction of
chemical bonding as well as chemical com-
position information from the spectra.

Surface Roughness — Study of the roughness of
the crater formed by argon ion sputtering
leads to the conclusion that surface rough-
ness is not the cause of the observed width
of the silicon-silicon dioxide interface [23].
No roughness was observed at the bottom of
craters formed by a low energy, rastered ion

beam in silicon dioxide-silicon structures
when they were examined by both scanning elec-
tron microscopy and transmission electron
microscopy (replica technique).

Preferential Etching — It would be expected
and has been observed that preferential
etching is most evident in polycrystalline
materials where different crystal faces
etch at different rates. The silicon
oxides, on the other hand, are noncrystal-
line. There have been reports of preferen-
tial etching during bombardment by high-
energy helium ions during backscattering ex-
periments [24]. However, with argon as the
sputtering ion at energies from 1 to 3 keV
no significant preferential etching effects
have been observed. Possible differences in
sputtering rates on different faces of sili-
con, which would be important in interpret-
ing profiles on the silicon side of a sili-
con dioxide-silicon interface, are being in-
vestigated.

Ion Penetration Depth — An important factor
that enters into the depth resolution of
Auger-ion profiling is the penetration
depth of the primary ions. The penetration
depth, or ion range, in the solid is a mea-
sure of the extent of the stirred or altered
surface layer. Although considerable data,
both theoretical [21] and experimental [25],
have been published concerning the range of
ions at energies used for ion implantation,
at energies below 10 keV there is, practi-
cally speaking, no experimental information
and the theory is not well established.

Argon ion penetration was measured for the
(100) orientation of silicon in the energy
range 1 to 3 keV typically used for sput-
tering. A specimen was sputtered for 2 min
by means of a 75 μA/cm^2 argon ion beam, of
a particular energy. The beam strikes the
specimen at an angle of 53 deg with respect
to the surface normal and was rastered to
give uniform current density. In this pro-
cess at least 15 nm is removed. Immediately
after sputtering the argon is pumped out and
replaced with xenon to the same pressure,
5×10^{-5} Torr (6.7 mPa). The Ar$_{KLL}$ signal
from the specimen is monitored as a function
of the Xe$^+$ sputtering time. The sputtering
rate was taken as 0.5 nm/min at the energy
of 1 keV and the beam current density of
2.5 μA/cm^2 employed. The time to remove the
implanted argon completely is used as a mea-
sure of the ion range. The results are pre-
sented in figure 9. Both the absolute magni-
tude and the rate of increase are smaller

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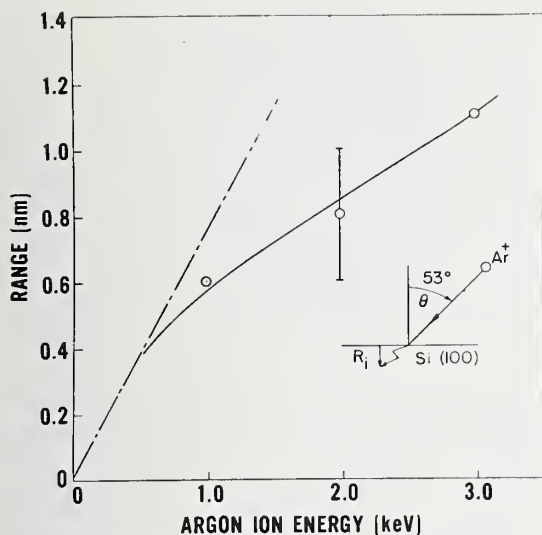
Figure 9. Energy dependence of argon ion range (penetration depth) in [100] direction of silicon. (Broken line is extrapolated from ion implantation data on silicon [21].)

Figure 10. Auger spectra from a (100) silicon surface. (Solid curve: 3.0-keV Ar^+ ion bombardment only, current = 16 μA; dashed line: 4.5-keV electron bombardment only, current = 5 μA; same detection sensitivity for both spectra.)

than expected from extrapolation of data in the 100 to 1000 keV energy range [21]. This is attributed to the influence of large angle scattering at low energies, an effect not presently included in the theoretical calculations.

In routine depth profiling experiments, 1-keV argon ions are employed for sputter etching. The depth of the perturbed layer in silicon is about 0.6 nm, which is one of the microscopic limitations on the ion sputtering technique. Although the damage depth may be reduced by using lower ion energy, the decrease in sputtering yield results in an intolerable increase in total sputtering time. Ion penetration depths in silicon dioxide and silicon nitride are expected to be smaller than in silicon [21]. In these materials it is hardly possible to observe the Ar_{KLL} signal under the conditions of the experiment described above.

Ion Stimulated Auger Transitions — For certain materials, silicon and aluminum for example, intense, well defined Auger emission stimulated solely by the ion beam have been observed under specific operating parameters. For other materials, silicon dioxide for example, this ion stimulated Auger (ISA) emission is found to be extremely weak for the same ion beam parameters. In figure 10 an Auger spectrum stimulated solely by electron

bombardment is compared with an ISA spectrum taken with ion beam parameters favorable for a large signal. This comparison displays the distinct differences in the two types of spectra and demonstrates the need for careful selection and matching of electron and ion beam parameters to avoid erroneous results during electron stimulated Auger (ESA) sputter profiling of devices containing elemental silicon. Investigation of the ISA yield in silicon as a function of the Ar^+ ion beam energy showed that the yield at 1 keV is negligible. For an ion beam energy of 3 keV, however, it was found that the ion beam current must be kept quite small if the ISA contribution from silicon to the Auger spectrum is to remain less than 5 percent during sputter profiling with the usual ESA operating parameters. This strong dependence of the ISA yield on ion beam energy provides one with the ability to eliminate its effects during ESA sputter profiling as well as the possibility of using ISA itself as a new tool for profiling specific interfaces.

Quadrupole Mass Analysis of Impurities in the Ion Source Gas — A common mode of vacuum system operation during sputter profiling involves activating the titanium sublimation pump and subsequently turning off the ion pump. This procedure, which results from

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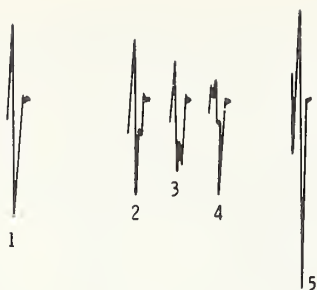
a. Si_{KLL} Auger lines obtained at the corresponding depths as marked below.
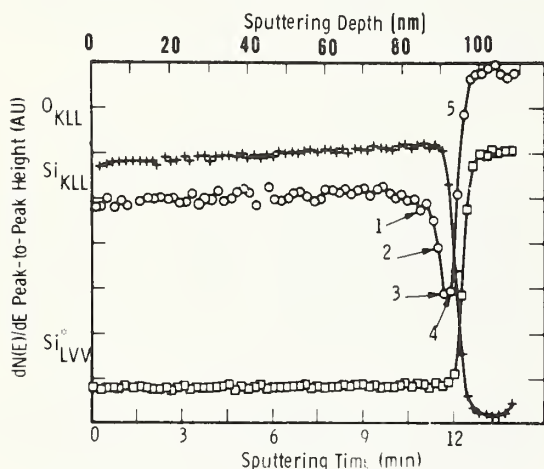
b. O_{KLL}, Si_{KLL}, and Si_{LVV} profiles. Sputtering rate: ~7.7 nm/min.

Figure 11. Chemical depth profiles through about 100 nm of silicon dioxide thermally grown on a (100) silicon surface.

the physical configuration of many common ultra high vacuum (UHV) systems, allows one to fill the chamber with inert gas, in this case argon, to the sputter operating pressure (~5 × 10⁻⁵ Torr) while the fresh titanium film getters the reactive impurity gases. Titanium at room temperature does not, however, pump the methane which is produced upon extinguishing the ion pump. Methane pressure in the baked UHV chamber varied from 3 to 15 percent of the total pressure in the chamber; the remainder was almost entirely argon except for a small quantity of helium. Although carbon contamination can be a severe problem in surface analysis, no effect of methane on the Auger spectra or on the depth profiles was found for the customarily employed electron and ion beam operating parameters.

Electron Beam Induced Surface Damage — The electron stimulated desorption of oxygen in silicon oxides was studied under a variety of conditions [26,27]. In general it was found that primary beam interactions in AES analysis depend on the chemical composition of the specimen under investigation and its pre-history. It was also found that beam interactions may be minimized by a suitable choice of primary beam parameters such as energy and flux. A total exposure of up to 10^{19} 2-keV electrons per square centimeter appeared to leave the surface, practically speaking, virgin although not untouched.

Chemical Shift Studies — Chemical shifts were observed in the silicon $KL_{2,3}L_{2,3}$ Auger transition in unsaturated silicon oxide films vapor deposited on silicon [28]. These results are interpreted [29] as supporting the microscopic mixture model [30] in preference to the random bonding model [31] for the chemical structure of unsaturated silicon oxides. Chemical shifts of Auger lines have proven very useful in analysis of interfaces as they appear in chemical depth profiles of layered structures [23]. A typical depth profile is shown in figure 11. Here a 100-nm thick oxide thermally grown on a (100) face of silicon has been sputtered through, and peak-to-peak heights of the Si_{KLL}, O_{KLL}, and Si_{LVV} lines are plotted as a function of sputtering time. Knowing the rate of sputtering, 7.7 nm/min in this case, the time scale can be converted to distance or depth into the specimen. The bulk of the oxide layer shown in the figure is homogeneous silicon dioxide, SiO_2. However, at the interface, the stoichiometry appears to be SiO_x, where x < 2. This is demonstrated by the dip in the Si_{KLL} profile, caused by the presence of silicon atoms in two chemical states. The Si_{KLL} lines plotted above the depth profiles in the figure show how the 1611 eV line decays and the 1618 eV line grows as the interface is sputtered through.

A closer examination of the interface region, figure 12, shows that the silicon atoms change their chemical state in an orderly fashion over a spatial extent of about 8 nm. The interface in the figure appears to be wider than the "real" interface due to escape depth and ion beam effects. When these effects are taken into account, one arrives at a "real" interface width on the order of 3 nm. Based on this experimental data and
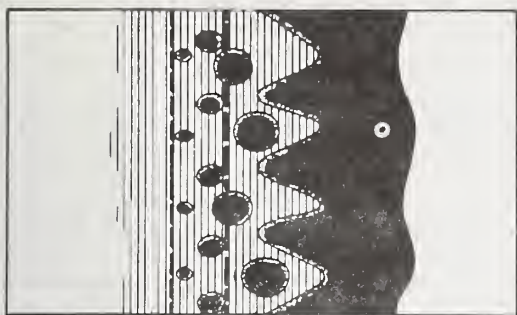
a. Model of morphology of interface. Dotted areas are connective regions between silicon, shown as black areas, and silicon dioxide, shown as areas with vertical lines. The broken vertical lines indicate the electron escape depth at 1600 eV.
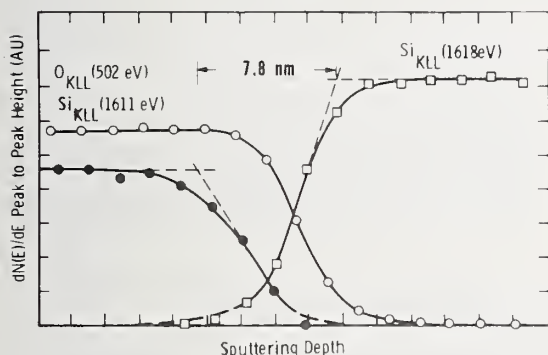
b. Depth profiles showing the falloff of the O_{KLL} line and the change from the 1611 eV to the 1618 eV Si_{KLL} line through the interface region. One division on the horizontal scale is equivalent to 1.9 nm.

Figure 12. Details of interface region.

on the transport properties of MOS-channel devices, a model of the chemical structure and the morphology of the oxide-silicon interface was formulated [32]. A sketch of this model is shown at the top of figure 12. The black areas represent silicon, the areas with thin vertical lines represent silicon dioxide, and the dotted areas represent connective regions between the silicon and the silicon dioxide. The vertical broken lines indicate the escape depth of 1600 eV electrons.

(J. S. Johannessen[†§], W. E. Spicer[†], P. E. Lusher[¶], and Y. E. Strausser[¶])

4.4. Sodium Contamination Studies

Sodium and other alkali contaminants are known to have a deleterious effect on the electrical behavior of microelectronic devices. Thus, the impurity content of processing materials used for semiconductor device fabrication must be carefully controlled. Flame emission spectrometry has been used as a measurement technique for determining levels of contamination in processing materials [33-36]. New results have recently been obtained using this technique to measure the sodium trace contamination in a variety of typical commercial electronic grade materials.

The instrumentation used for the measurements has been described in detail elsewhere [37]. Briefly, it consists of a flame emission spectrometer which scans repetitively a narrow region of the optical spectrum while the second derivative of the output light intensity signal is measured. Using this technique, matrix spectral interferences are minimized and very small samples can be used.

The minimum detectable quantity of sodium was estimated to be in the range of 100 pg/ml with a precision of ±25 percent or better at this level. The minimum specimen volume used for analysis was approximately 100 µl. Purified spectroscopic grade reagents and TFE fluorocarbon containers were used for preparing the specimens analyzed. Blank solutions were carefully checked and all intermediate operations for the analysis were controlled to prevent transport of sodium from the ambient into the analyzed specimen. Fresh sodium standard solutions were used for calibrations both before and after each specimen analysis.

Table 5 — Sodium Trace Contamination Measurements
by Flame Emission Spectrometry

Sample (Electronic Grade Purity)	Present Results [μg/ml]	[μg/g]	Yurash-Deal [33] [μg/ml]	Knolle [35,36] [μg/ml]
Acetone	0.0008		0.010-0.050	0.001
Ammonia (NH_3 28-30%)	0.008			0.007
Buffered Etch for Silicon Dioxide	0.1			
Hydrochloric Acid (37-38%)	0.5			0.015
Hydrofluoric Acid (49%)	0.6 0.08		0.150	0.019
Hydrogen Peroxide (30-32%)	0.25			0.995
Methanol	0.38			0.174
Nitric Acid (70-71%)	0.72			0.087
Water (deionized, 18 MΩ·cm)	<0.0001		0.0004	<0.002
Arsenic Spin-on Solution	0.24			
Phosphorous Spin-on Solution	0.34			
Positive Photoresist	0.05			
Aluminum Pellet		0.7		
Aluminum Film (0.5 μm thick)		∿7		
Tungsten (Resistance Heater Wire)		1.5		

A pressure stabilized air-acetylene or oxygen-hydrogen flame was used.

Table 5 presents some typical results of the present measurements along with some previously reported data also obtained using flame emission spectrometric techniques. There are no obvious trends detected when the current experimental results are compared with those reported earlier. In general, solvents exhibited lower sodium levels than acids. The sodium content of deionized water (18 MΩ·cm at 25°C) was lower than the detection limit of this experiment. Aluminum used for metallization exhibited sodium bulk contamination in the 0.5 μg/g range as received from the vendor. The sodium concentration measured in a 0.5-μm thick film of aluminum, e-gun evaporated on a silicon dioxide layer thermally grown on a silicon wafer, was ∿7 μg/g, which suggests that the contamination level is increased by the metallization process.

No attempt was made to investigate the relationship between sodium content in processing materials and the sodium content in a finished device. Obviously, various materials contribute different amounts of sodium, but an appropriately controlled experiment to examine this effect would be difficult because sodium is present to some extent in nearly every processing material. However, flame emission spectrometry provides a sensitive technique for monitoring sodium content in processing materials and can be applied in process control efforts.

(S. Mayo and T. C. Rains[#])

4.5. Optical Test for the Surface Quality of Sapphire Substrates

As a basis for all optical measurements, it is important to know how the optical constants n (the refractive index) and k (the absorption index) vary in the optical region of interest, which is generally a region of high absorption. These constants express dispersion and absorption processes in quantitative terms. As these processes are distorted, shifted, or otherwise changed by introduction of lattice damage, the values of n and k can be used to measure quantitatively the degree of change in the lattice modes.

The optical constants can be derived by means of the Kramers-Kronig relations from measured values of reflectivity as a function of frequency following the general treatment of Roessler [38] and the related computer program of Klucker and Nielsen [39,40]. Absolute reflection spectra were obtained for variously polished surfaces using either P or S polarization with respect to the (1102) surface. For both polarizations, the spec-

tra show that there is significant change in the reflectivity near 600 cm^{-1} with increasing grit size, or hardness, of the polishing medium. Below about 500 cm^{-1}, the effect of polishing damage on the sapphire reflectivity is less evident although clearly present [40].

The optical constants were calculated for both polarizations from each of the spectra at 300 to 400 points. Calculated values of n and k at the maxima of the dispersion curves, S polarization, are given in table 6 for surfaces polished with silica sol [8], 0.3-μm alumina, and 1-μm diamond. In this case, as with P polarization [40], polishing damage greatly diminishes the magnitude of the calculated optical constants and shifts the position of maxima in the dispersion curves to shorter wavelengths.

The influence of polishing damage on the magnitude of the calculated optical constants can be understood from the data given in table 7. Changes, ΔR, of 0.005, 0.01, and 0.02, were deliberately introduced into the value of the reflectivity, R, in the computer program on the reference specimen polished with silica sol. The effect of these small changes on the values of n and k is considerable, as shown in the table.

Thus, the surface quality of polished sapphire can easily affect the magnitude of the measured reflectivity and in turn grossly affect the magnitude of the calculated optical constants. Note, however, that this characteristic of the Kramers-Kronig relations imposes strict conditions on the procedures and equipment used to obtain reflection spectra. The reflection data must be accurate to much better than 1 percent before attempting to determine absolute values of the optical constants. This condition is difficult to achieve with commercial spectrometers. Similar errors could be introduced in base-line setting. Thus, only the wavelengths for the lattice modes can be considered to be accurate, and the calculated optical constants must be considered as estimates until the accuracy of these measurements can be more fully studied. For purposes of this work, the wavelengths of the lattice modes and relative values of the optical constants are of primary importance. Generally, the ΔR changes observed in commercial specimens [40] are much greater than the values introduced above. In addition, various experimental errors [40] and the effect of specimen curvature must also be considered in interpreting reflectance data.

Table 6 — Calculated Optical Constants for (1$\bar{1}$02) Sapphire with Various Surface Polishes, S Polarization

Surface Finish	energy eV	wavelength, μm	wave number, cm^{-1}	n	k
Standard (silica sol)	0.05158	24.0	416	44.4	
	0.05183	23.9	417.9		28.9
	0.06026	20.6	486	4.5	
	0.06051	20.5	488		5.2
	0.07192	17.2	580	29.3	
	0.07217	17.18	582		21.8
0.3-μm alumina	0.05307	23.4	428	13.5	
	0.05332	23.3	430		8.2
	0.06026	20.6	486	1.98	
	0.06101	20.3	492		3.4
	0.07490	16.6	604	12.9	
	0.07614	16.3	614		10.4
1-μm diamond	0.05258	23.6	424	6.4	
	0.05282	23.5	426		4.7
	0.06002	20.7	484	1.24	
	0.06076	20.4	490		2.3
	0.06721	18.5	542	2.25	
	0.06894	17.9	556		1.74
	0.07886	15.7	636	15.3	
	0.08010	15.5	646		9.1

Table 7 — Effect of Constant Reflectance Error, ΔR, Introduced in Calculation
of Optical Constants for (1$\bar{1}$02) Sapphire, S Polarization

ΔR	energy, eV	wavelength, μm	wave number, cm^{-1}	n	k
zero, standard	0.05158	24.0	416	44.4	
(silica sol)	0.05183	23.9	418		28.9
surface finish	0.06026	20.6	486	4.5	
	0.06051	20.5	488		5.2
	0.07192	17.2	580	29.3	
	0.07217	17.18	582		21.8
0.005	0.05158	24.0	416	34.0	
	0.05183	23.9	418		25.2
	0.06026	20.6	486	4.2	
	0.06051	20.5	488		5.0
	0.07192	17.2	580	26.3	
	0.07217	17.18	582		19.6
0.01	0.05134	24.1	414	29.9	
	0.05158	24.0	416	25.6	23.6
	0.06026	20.6	486	3.9	
	0.06051	20.5	488		4.8
	0.07192	17.2	580	22.3	
	0.07217	17.18	582		17.5
0.02	0.05134	24.1	414	24.1	
	0.05158	24.0	416		19.7
	0.06026	20.6	486	3.3	
	0.06051	20.5	488		4.3
	0.07167	17.3	578	14.7	
	0.07192	17.2	580	13.9	
	0.07217	17.18	582		13.5

Although it is apparent that surface damage significantly affects the optical constants of (1$\bar{1}$02) sapphire, it is clear that a formal dispersion analysis is not practical for testing the surface quality of sapphire, or any dielectric or semiconductor material, where frequent testing of many samples is required as in production facilities. The experimental procedures and the mathematical calculations are time consuming. More significantly, the magnitude of the difference between undamaged and slightly damaged surfaces, while not small, is still not sufficient for detecting lightly damaged surfaces. The multiple reflection technique has an order of magnitude more sensitivity to surface damage.

Multiple reflection techniques are often used to amplify small changes in absorption processes for measurement purposes. Two types of conditions exist for multiple reflections: (a) external reflections occur in a low refractive index medium, such as air, from a high refractive index medium, such as a mirror surface, and (b) internal multiple reflections occur in a medium of high refrac-

tive index surrounded by a medium of low refractive index, as in optical waveguides [41, 42]. With either external or internal reflections it is well established that surface defects diminish the magnitude of the reflected light beam. The loss may be very small for a single reflection, but becomes amplified with multiple reflection.

The qualitative features of the resulting spectra, single and multiple reflection, are shown in figure 13.$^{\times}$ Note the loss of weak band structures in the multiple reflection spectra. More significantly, note the magnitude and frequency shift of the band near 600 cm^{-1} for the damaged specimen in comparison with the undamaged specimen. These effects allow for a relative, quantitative

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$^{\times}$The sharp discontinuity at 600 cm^{-1} is due to instrumental effects. A grating change occurs here which causes a shift in the curves. All curves show this discontinuity which does not, however, significantly affect the interpretation of data.
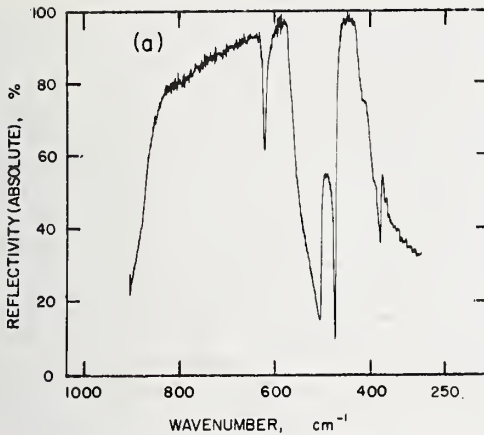
a. Undamaged surface, single reflection spectrum.
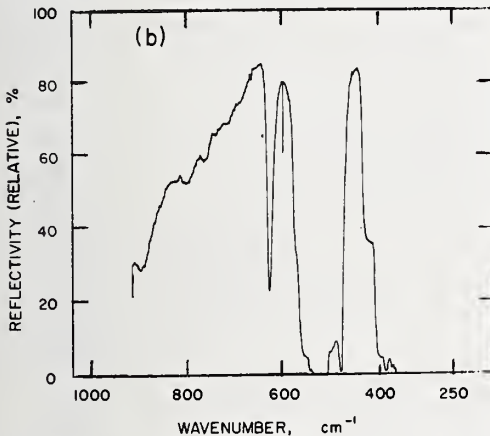
b. Undamaged surface, multiple reflection spectrum.
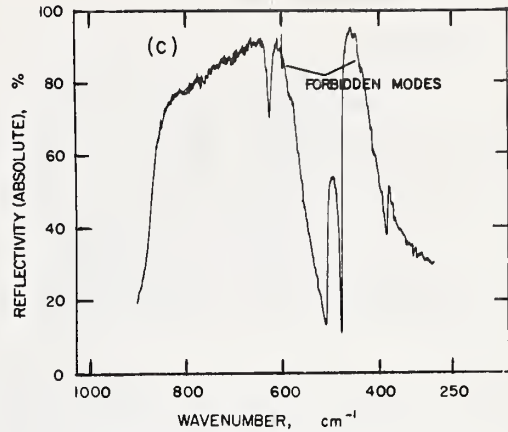
c. Damaged (as received) surface, single reflection spectrum.
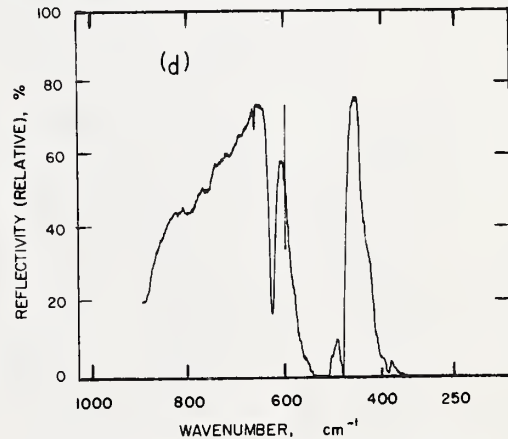
d. Damaged (as received) surface, multiple reflection spectrum.

Figure 13. Reflection spectra of undamaged and damaged sapphire. (The former, obtained by silica sol polishing, was satisfactory for device fabrication; the latter was not. Vertical spike at 600 cm^{-1} is an instrumental artifact.)

evaluation of surface damage of the type reported by Barker [43].

Relative multiple reflection measurements have been made on about 30 as-received (1102)-oriented sapphire specimens [40]. In general, it appears that the properties of sapphire, prior to cutting and polishing, are not directly associated with the damage introduced in the finishing processes. Thus, the variation in the quality of the sapphire is probably due solely to polishing. It is a great deal of variation in the type of finish provided, often varying from lot to lot, by the same supplier.

As a characteristic of the multiple reflection technique, it should be noted that occasionally a specimen exhibited a multiple reflection spectrum suggesting the presence of surface contamination or wafer misalignment; i.e., band amplitude is strongly diminished over the entire spectrum but damage effects are not present. This effect has not been studied in detail. (M. T. Duffy[+], P. J. Zanzucchi[+], and G. W. Cullen[+])

5. TEST STRUCTURE APPLICATIONS

5.1. Redistribution of Boron in Oxidized Silicon

It is known that thermal oxidation brings about a redistribution of the dopant impurity near the silicon surface. Boron, with a segregation coefficient less than one, preferentially segregates into the oxide with the result that the silicon region close to the oxide is depleted of boron. The profile of the boron in the redistributed region depends on parameters such as the oxidation time and the diffusion and segregation coefficients.

The redistribution profile was obtained for a boron-doped silicon wafer with (111) surfaces and a nominal resistivity of 1 Ω·cm which had been oxidized in steam at 1100°C for 18 min. The wafer was then patterned using the metallization mask of Test Pattern NBS-3 (NBS Spec. Publ. 400-12, pp. 19-22) [44]. The impurity density was determined from capacitance-voltage measurements made on the MOS capacitor over collector (test structure 3.8) by the dynamic MOS C-V (deep depletion) method (NBS Spec. Publ. 400-17, pp. 8-11). The experimentally determined profile was compared with profiles calculated from the previously described redistribution model (NBS Spec. Publ. 400-19, pp. 25-26) as shown in figure 14. In the figure, the dopant density, C, is normalized with respect to the bulk value, C_B, which is determined from data in the unredistributed region. On the horizontal axis the distance from the oxide-silicon interface, $y-y_0$, is normalized by the quantity $2\sqrt{Dt}$, where D is the diffusion coefficient of boron in silicon and t is the oxidation time. As seen in the figures the dopant density is essentially flat at depths greater than $2\sqrt{Dt}$, but decreases as the oxide-silicon interface is approached. However, near the interface a sharp upturn occurs due to failure of the space charge approximation at a distance of several Debye lengths from the oxide (NBS Spec. Publ. 400-19, pp. 26-27). The three experimental plots were obtained on the same capacitor at different times; the small variations in the various constants determined from analysis of the experimental data, as listed in table 8, are indicative of random experimental fluctuations.

The values of the parameters used in the model were taken from various sources. The constants in the growth equation for a wet (steam) oxidation at 1100°C were taken from Deal and Grove [45]. The ratio of the diffusion coefficient in silicon dioxide to that in silicon was taken as 2.9×10^{-4} [46]. The boron at the gas-oxide interface was assumed not to escape. The ratio of silicon consumed to oxide thickness was taken as 0.44. The oxide thickness calculated by the program was 340 nm compared to an ellipsometer measurement of 299 nm. This discrepancy is thought to be due at least in part to an uncertainty in the oxidation time. The wafer was not preheated before oxidation started; although 2 min was subtracted from the nominal time to allow for this fact, more may be appropriate. Initially, the boron diffusion coefficient, D, at 1100°C was taken as 2.65×10^{-13} cm^2/s, after the work of Prince and Schwettman [47]. This case is plotted in figure 14a; theoretical curves were computed for several values of segregation coefficient, m, defined as the ratio of the boron density with silicon to that in the oxide at the oxide-silicon interface. As seen in figure 14a, the experimental profile does not agree with the theoretical calculation for any value of segregation coefficient. Since many different values have been reported for the diffusion and segregation coefficients, it seemed appropriate to generate plots with different values of diffusion coefficient and vary the segregation coefficient to arrive at a reasonable fit. It was found that the best fit could be achieved if the diffusion coefficient had the value, 3.69×10^{-13} cm^2/s and m = 0.2 as shown in figure 14b. Although the curve for D = 5.78×10^{-13} cm^2/s and m = 0.45, shown in figure 14c, is close to the experimental one, the slopes are significantly different in the region to the right of the Debye limit. These results are considered preliminary and there is no assurance that suitable fits to the redistribution curve for other oxidations at the same temperature could be obtained with these values of D and m.

(W. R. Thurber,
M. G. Buehler, and S. R. Kraft[*])

The computer program for solving the redistribution problem was extended to permit successive oxidations in sequential steps with different material constants and oxidation conditions permitted at each step. Debugging of the program with this extension was carried out; also the modifications in the computer output that are required by this extension were incorporated into the program. The program is also being extended to permit sequential oxidation steps in which the oxide grown at earlier time steps is removed before the next step is commenced. (S. R. Kraft[*])

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[*] NBS Mathematical Analysis Section, Applied Mathematics Division.

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a. $D = 2.65 \times 10^{-13}$ cm^2/s $\quad$ b. $D = 3.69 \times 10^{-13}$ cm^2/s $\quad$ c. $D = 5.78 \times 10^{-13}$ cm^2/s
$\quad\quad = 1.59 \times 10^{-3}$ µm^2/min. $\quad\quad = 2.21 \times 10^{-3}$ µm^2/min. $\quad\quad = 3.47 \times 10^{-3}$ µm^2/min.
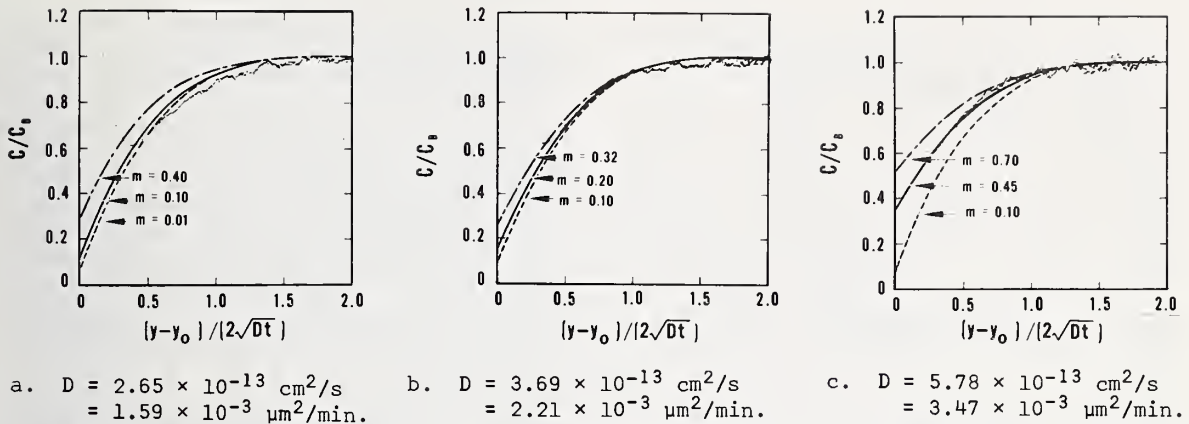
Figure 14. Redistribution profile of boron in silicon following an 18-min steam oxidation at 1100°C. (Experimental curves (dotted) obtained by the dynamic MOS C-V (deep depletion) method; the rising portion at small distances is an artifact of the measurement. See table 8 for the capacitor and redistribution parameters used to calculate the theoretical curves. The value of segregation coefficient, m, used is shown on each curve and the value assumed for the boron diffusion coefficient, D, in silicon is indicated under each plot; see text for discussion of assumptions for m and D.)

Table 8 — Capacitor and Redistribution Parameters

Case	a	b	c
Oxide thickness, nm	326	320	323
Oxide capacitance, pF	12.08	12.31	12.19
Flat-band capacitance, pF	11.68	11.91	11.79
Flat-band voltage, V	-5.7	-5.9	-5.6
Background dopant density, cm^{-3}	1.46×10^{16}	1.55×10^{16}	1.54×10^{16}
Debye length, µm	0.0475	0.0462	0.0463
$2\sqrt{Dt}$, µm	0.338	0.400	0.500
Debye length (units of $2\sqrt{Dt}$)	0.140	0.116	0.093

5.2. Thermally Stimulated Current and Capacitance Measurements

A study was made of the thermally stimulated current response of the energy states found at the oxide-silicon interface of an n-type MOS capacitor. The capacitor used in this measurement consisted of an aluminum metallization 15.0 mil (381 µm) in diameter evaporated on a silicon dioxide layer, oxide 390 nm thick, thermally grown on an n-type silicon substrate with (111) surfaces and a nominal room temperature resistivity of 7 Ω·cm. The main capacitor was surrounded by a peripheral field plate which was biased into accumulation during the measurements. The device (17.22) was alloyed to a ceramic slab mounted in a TO-5 header. The temperature was measured with a temperature-sensing diode alloyed to the ceramic slab but electrically isolated from the MOS capacitor.

The presence of interface states can be seen as a distortion in the experimental room temperature 1-MHz capacitance-voltage (C-V) characteristic from the theoretical C-V curve without interface states as shown in figure 15. From the analysis of Deal *et al.* [48] the interface state density can be estimated from the shift, ΔV, of the C-V curve along the voltage axis:

$$N_{FS} = \Delta V \cdot C_o / qA,$$

where C_o is the oxide capacitance, q is the electronic charge, and A is the area of the capacitor. For ΔV = 1.9 V, as in this example, the total interface state density is about 1×10^{11} cm^{-2}. A C-V curve measured from accumulation into deep depletion at 95
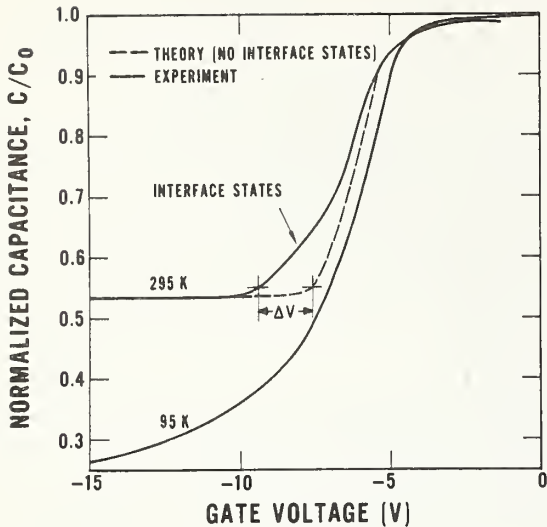
Figure 15. Distortion of the room temperature high frequency C-V characteristic of an *n*-type silicon MOS capacitor which results from the presence of interface states. (The oxide capacitance, C_o, is 10.0 pF and the normalized flat-band capacitance is 0.88. Device 17.22)

K is also shown in the figure. At low temperature the interface states are not active and do not distort the C-V curve.

The thermally stimulated current response experiments were conducted as follows. First, zero bias was applied to the gate of the MOS capacitor while it was at room temperature and then its temperature was lowered to 95 K. This effectively charges the interface states with electrons. Second, a bias, V_g, was applied, the temperature was increased, and the thermally stimulated current response was recorded.

Several features are evident in the response curves which are shown in figure 16 for various values of V_g along with the heating rate as a function of temperature. At 95 K electrons are emitted from interface states close to the conduction band edge. As the heating rate increases from zero to its maximum value, electrons are emitted at a rate which generally follows the heating rate. When the heating rate reaches its maximum value, the current reaches a constant value for $V_g \leq -7$ V as electrons are released from states farther and farther from the conduction band edge. When the supply of electrons is exhausted, the current decreases, but if holes are required to satisfy the surface potential a peak occurs in the current for
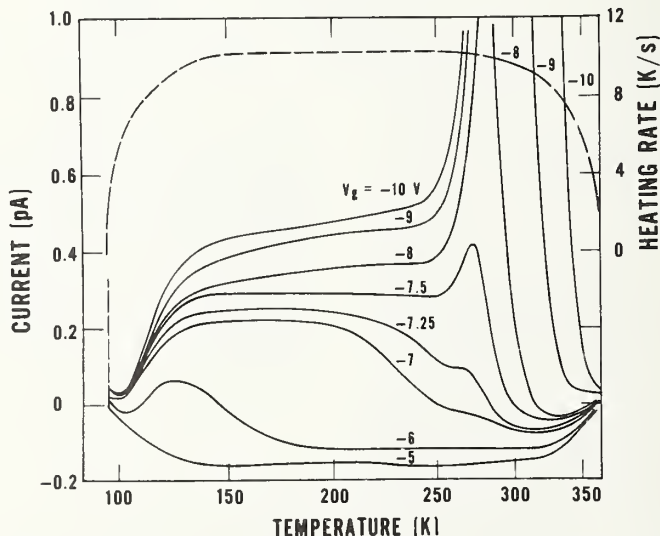
Figure 16. Thermally stimulated current response of interface states in an *n*-type silicon MOS capacitor for various values of gate voltage, V_g. (The heating rate as a function of temperature is shown as the dashed curve. Device 17.22.)

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temperatures above 250 K. The size of the current peak depends on the number of holes needed to satisfy the inversion condition. Once the inversion condition is met the current decreases to zero.

The thermally stimulated current response from interface states can be modeled by a continuum of energy levels in the forbidden gap of silicon at the oxide-silicon interface. The thermally stimulated current response to this continuum of energy levels is substantially different from the response of a point defect center such as the gold donor in silicon which produces a distinct current peak with a half width of about 8 K for a heating rate of 10 K/s [49].

(M. G. Buehler and W. E. Phillips)

5.3. Oxide Film Characterization

Additional irradiation experiments were carried out with the scanning electron microscope (SEM) on MOS capacitors to study the effect of SEM irradiation on mobile ion density. It is well known that SEM irradiation of MOS capacitors causes both a large shift in the flat-band voltage (NBS Spec. Publ. 400-19, pp. 29-31) and a high density of interface states. This is illustrated in figure 17; the high frequency (1-MHz) C-V characteristic after irradiation (curve b) is displaced from and shows greater dispersion than the characteristic before irradiation (curve a). Some hysteresis is also introduced into the characteristic; the direction of the hysteresis in this case suggests that it is probably due to trapping effects at the silicon dioxide-silicon interface. A thermal anneal of the irradiated sample readily removes the interface state dispersion and the hysteresis as well as most of the flat-band voltage shift; this is shown as curve c in the figure. Since the minimum capacitance for the initial curve is higher than the annealed curve, it appears that the dopant density in the semiconductor near the interface has decreased.

To assess the effect of radiation on the mobile ion density, it is necessary to make bias-temperature stress measurements. Measurements were performed on MOS capacitors formed on n-type silicon wafers with a nominal dopant density of 8×10^{14} cm^{-3}. The oxide films were thermally grown in dry oxygen at 1000°C to a thickness of about 110 nm. Following the oxidation, the wafers were annealed in dry nitrogen at 1000°C for 20 min. Aluminum was e-beam evaporated over the oxide
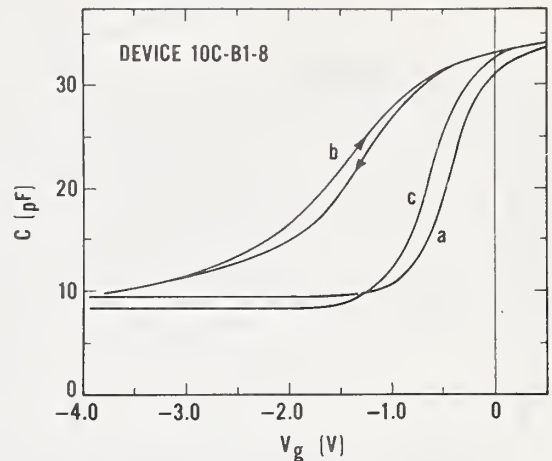
Figure 17. Effect of electron-beam irradiation on the capacitance-voltage characteristics of an n-type silicon MOS capacitor. (Curve a: after processing; curve b: after irradiation; curve c: after thermal anneal.)

to a thickness of about 500 nm, patterned with the Metal mask of Test Pattern NBS-3 (NBS Spec. Publ. 400-12, pp. 19-22) [44], and further annealed in dry nitrogen at 500°C for 15 min. The entire backside of the wafer was metallized with antimony-doped gold. The devices were not intentionally contaminated, so that the reported ion densities represent the level of contamination for this particular lot.

After processing the wafer, the flat-band voltages were determined by measuring the capacitance-voltage characteristics at 1 MHz. The mobile ion density was then determined from the net flat-band voltage shift under negative bias-temperature stress (-10 V, 300°C, 5 min) followed by positive bias-temperature stress (+10 V, 300°C, 5 min). Following exposure to a total dose of 10^4 Gy (10^6 rads(Si)) without bias in the scanning electron microscope and anneal at 300°C for 20 min in dry nitrogen, the flat-band voltage and mobile ion density were again determined.

Mobile ion densities before and after the irradiation are compared in figure 18. With the exception of two data points, most of the data cluster near the 45 deg line which represents equality of mobile ion density before and after irradiation. This fact suggests that the density of mobile ions is not affected by the SEM irradiation.
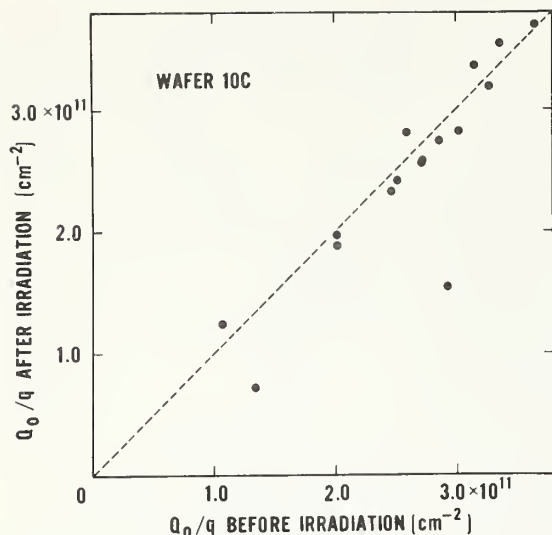
Figure 18. Comparison of mobile ion density, Q_O/q, before and after electron beam irradiation and thermal anneal.

The position of the flat-band voltage, V_{fb}, before and after irradiation is plotted in figure 19 against the mobile ion density, Q_O/q, as determined before irradiation. In the "as processed" condition, the flat-band voltages are grouped between -0.33 and -0.42 V. These data do not offer any clue to the fact that mobile ions are present. Following irradiation and anneal, the flat-band voltages appear to be directly correlated to the presence of mobile ions. The dashed line is a linear fit to the data points; when ex-

trapolated back to zero mobile ion density, it predicts a flat-band voltage of -0.3 V which is appropriate for aluminum metallization on n-type silicon with dopant density of 8×10^{14} cm^{-3}. This coincidence also implies that the surface state charge is less than 2×10^9 cm^{-2}. Without many more extensive measurements, however, it is not clear that this correlation can be generalized. It is not planned to carry out such measurements at the present time.   (R. Y. Koyama)

5.4. Extended Range MIS C-V Method

Further improvements have been made in the modified instrument for measuring capacitance at applied voltages of up to 10 kV (NBS Spec. Publ. 400-19, pp. 31-32). These improvements include bias protection circuitry which protects the capacitance meter by limiting the input voltage (terminal-to-ground) to ±200 V while allowing up to ±10 kV on the capacitor; a linear sweep, high voltage power supply which provides a programmed ramp voltage (in several output waveform configurations) in the range of ±10 kV; a specimen holder which prevents premature breakdown around the capacitor; and a safety interlock system for protection of personnel using the apparatus.

An evaluation of this instrument has begun by investigating its use with several different commercially available capacitance meters. Initial results suggest that the instrument can be expected to perform satisfactorily with the following 1-MHz meters: 71A[†], 72A[†], and 410.[§] Minor circuit modifications are required for use with the last two.

This instrument has been utilized to characterize the silicon-sapphire interface region using back-gate MIS capacitors [50]. In four out of 50 cases the specimen broke down at applied voltages between 7 and 10 kV, but in each case the capacitance meter was undamaged. This demonstrated the efficacy of the bias protection circuitry under actual measurement conditions.   (A. M. Goodman[¶])

Figure 19. Flat-band voltage, V_{fb}, as a function of mobile ion density, Q_O/q, before and after electron beam irradiation and thermal anneal.

6. MATERIALS AND PROCEDURES
FOR WAFER PROCESSING

6.1. Oxidation Furnace Contamination

Sodium contamination in microelectronic devices has been correlated with erratic electrical behavior of these devices [51]. The electrical properties of silicon dioxide films in MOS devices have been the subject of many investigations in which sodium was shown to be one of the principal causes of instabilities [52]. Among other sources of sodium contamination such as those due to materials associated with processing of semiconductor devices (sec. 4.4.), the oxidation furnace atmosphere itself was suggested as a prominent one because of the high diffusion coefficient of sodium in silicon and silicon dioxide at temperatures used for oxidation [53,54]. It has been postulated that sodium is transferred from the furnace material to the silicon wafer through the furnace atmosphere as free sodium atoms. Contamination control during device processing has been highly recommended to produce radiation hardened, stable MOS devices. The mechanisms by which alkali contamination affects hardness are not well established [55] although ion microprobe studies of MOS devices show a correlation of sodium content in the oxide w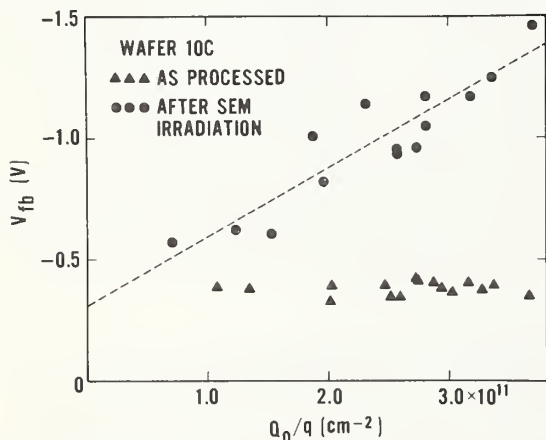ith radiation sensitivity [56]. This task was undertaken to develop a technique for measuring sodium impurities in atmospheres of furnace used in the growth of MOS oxides and in their subsequent annealing.

Because sodium is highly reactive, it was expected that the density of free sodium would be very low. Detection of free sodium at the anticipated levels is very difficult. Atomic absorption techniques are limited to density ranges above 10^8 cm^{-3} by the difficulty of measuring small changes in transmitted light [57]. Sodium densities as small as 100 cm^{-3} were recently detected in an evacuated tube at $-28°C$ by a resonance fluorescence technique [58]. This method [59] has been extended to determination of sodium density levels in an open quartz tube at $1000°C$.

A diagram of the apparatus used for the detection of resonance fluorescence from sodium vapor is shown in figure 20. Amplitude modulated radiation from a tunable cw dye laser passes down the furnace 2 deg off axis and out through a hole in the laboratory wall to minimize return reflections. The fluorescence emission traveling out of the tube in the direction opposite to the laser beam is collected by a telescopic system, passed through an interference filter centered on the sodium D_2 line and focussed onto a photomultiplier tube. The ac signal corresponding to the fluorescence is synchronously detected, digitized, and recorded on a multichannel analyzer as a function of the wavelength of the dye laser.

The dye laser was longitudinally pumped by an all-line argon ion, cw laser with power up to 5 W. An intra-cavity birefringent filter was used to coarse-tune the dye laser with a resultant bandwidth of 0.03 nm. Insertion of a 0.5 mm etalon into the cavity further nar-

A   Power amplifier
C   2-kHz chopper
D   Diaphragm
E   0.5-mm etalon mounted on torsion motor
F   Interference filter, 588.5 nm, FWHM: 1.25 nm
ℓ Length of observed region
L   Lens
M   Mirror
MS   Multi-channel scaler
P   Power meter
PM   Photomultiplier tube
PSD   Phase-sensitive detector
S   Sweep counter
T   Telescope
V/F   Voltage-to-frequency converter
W   0.5-Hz sinusoidal wave generator
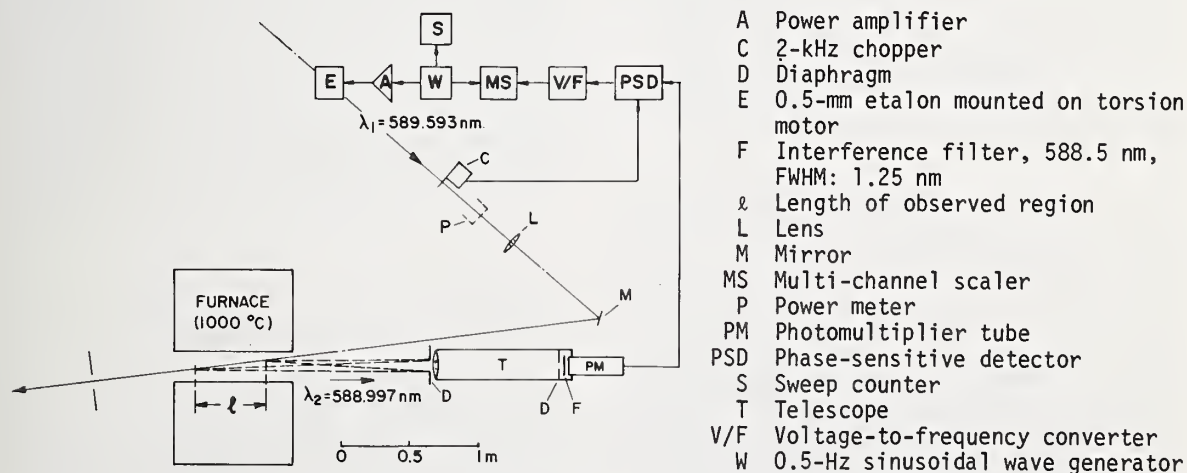
Figure 20. Experimental arrangement for sodium detection in a semiconductor processing furnace by resonance fluorescence.

rowed the output to 0.003 nm. The laser emission wavelength could be repetitively and reproducibly scanned over the absorption line by rotating the etalon through an angle of about 1 deg with an oscillatory torsion motor driven by a low frequency (0.5 Hz), low amplitude, sinusoidal wave. The laser was tuned to center the sodium D_1 line (589.6 nm) on the approximately linear portion of the sinusoidal wavelength scan. The signal-to-noise ratio was increased by repetitive scanning of the laser wavelength and summing the data from approximately 100, 2-s sweeps in the multichannel analyzer. The wavelength scale was calibrated by passing a portion of the output of the laser through the spectrum analyzer.

Problems associated with Doppler and collisional cross-section reduction, reaction of the sodium with oxygen and water, quenching of the emission by molecular collisions, and scattering from furnace gases, thermal gradients, and suspended dust particles result in a poorer detection limit than is obtained under ideal conditions at lower temperatures. Geometrical restrictions related to the structure of the furnace also contribute to the poorer detection limit. A major limitation to the minimum observable sodium signal is scattered laser light. Extreme care was necessary in the placement of optical components, apertures, and the dumping of the laser beam to minimize back reflection. Background black-body emission from the furnace was discriminated against by the sodium interference filter and synchronous detection. The scattered light signal is reduced approximately an order of magnitude when the D_1 transition is excited and the D_2 emission observed, in agreement with the transmission characteristics of the interference filter. At atmospheric pressure, collisions with molecular nitrogen and oxygen in the furnace completely equilibrate the population of these two levels according to their statistical weights [60].

Sodium fluorescence signals were not observable in clean quartz tubes. Non-quantitative sodium contamination was intentionally introduced by aspirating dilute sodium chloride solutions into the hot tube for short periods of time and then waiting for several hours until a relatively constant level of contamination was observed. A typical fluorescence signal from sodium vapor inside of the quartz tube is shown in figure 21. The average excitation power was 70 mW. The observed linewidth of the excitation spectrum (7.5 GHz or ∿0.01 nm) agrees reasonably well with the cal-
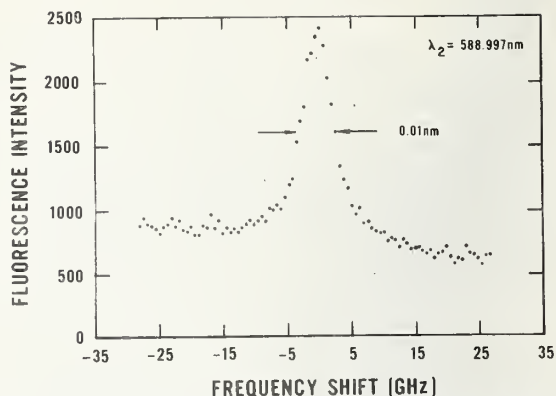
Figure 21. Typical sodium fluorescence signal detected in an intentionally contaminated quartz furnace tube at atmospheric pressure and 1000°C.

culated linewidth taking into account Doppler (2.7 GHz) and pressure (6.2 GHz) broadenings under the conditions of the experiment. This good agreement is indicative of the frequency stability of the laser system. A statistical analysis of the data in figure 21 shows that the ratio of the fluorescence signal at the peak to the noise in the scattered light is greater than 50. From preliminary calibration runs it is estimated that this signal corresponds to a sodium density of about 2×10^7 cm^{-3}. This would correspond with a minimum detectable sodium contamination level of about 5×10^5 cm^{-3}.

More detailed calibrations and comparisons of sodium contamination in oxide films grown with varying amounts of sodium in the furnace atmosphere are being carried out. However, it appears likely that much more sodium is present in forms other than free sodium and therefore that even with its extremely good sensitivity to free sodium, the resonance fluorescence technique may not be adequate for monitoring sodium contamination during oxidation. (S. Mayo, R. A. Keller[*†], J. C. Travis[*§], and R. B. Green[*§])

6.2. Ion Implantation Parameters

In the study of methods for measuring the critical parameters associated with ion implantation, characteristics and limitations of the Schottky-barrier capacitance-voltage (C-V) technique for measuring implanted profiles were investigated for various experimental conditions. Additional data were collected on profiles for a number of impurities; preliminary data were obtained on the sensitivity of the profile to the angle of incidence and the crystallographic direction.

Schottky-Barrier Capacitance-Voltage Technique — Four metallization systems, aluminum, gold, titanium-gold, and molybdenum-gold, were studied on boron-implanted, (111) silicon surfaces. Eight, 100-$\Omega \cdot$ cm p-type wafers were implanted (7 deg off the normal to the (111) plane) with boron at 300 keV to a dose of 1.5×10^{12} cm^{-2} and annealed at 750°C in dry nitrogen for 30 min. Four of the wafers were cleaned by ultrasonic degreasing followed by acetone, alcohol, and deionized water rinses, and four were dipped in hydrofluoric acid for 15 s and rinsed in deionized water. Schottky barriers, about 100 nm thick, were evaporated in an ultra-high vacuum electron beam evaporator through a metal mask which defined a pattern of circular dots nominally 0.12, 0.25, 0.50 and 1.0 mm in diameter. Each metal system was evaporated onto both a cleaned (but unetched) and an etched wafer; the evaporation onto the etched wafer was carried out with the least possible delay after etching. The barrier capacitance was measured as a function of voltage [61] immediately after the formation of the Schottky barriers and at subsequent times to establish the stability of the dopant profile as deter-

mined by this technique. All four metal systems on the etched wafers produced shorted barriers and no profiles could be determined. After about six weeks, some increase in the shorting resistance was observed and, based on published reports [62], it is expected that at least some of the barriers will improve after several months and ultimately yield both rectifying current-voltage (I-V) characteristics and satisfactory C-V profiles.

On the other hand, good Schottky I-V characteristics and fair C-V profiles were obtained within one day for the four metal systems placed on natural (unetched) silicon surfaces which are assumed to have a 3- to 5-nm thick native oxide present at the time of deposition. The C-V profiles changed during the first few days and then stabilized. Schematic representations of the C-V profiles showing the characteristics of the initial and stabilized C-V profiles for each of the four metallization systems are shown in figure 22. Since aluminum yielded the most stable profile, changing only slightly in background level, it is felt to be the best choice for routine work on p-type silicon. Profiles on some aluminum Schottkys have been found to be unchanged over a 13-month period.

Size effects were investigated by comparing the characteristics of the different diameter dots. It was found that the smallest diameter dots gave the best characteristics despite the fact that they suffer from a larger ratio of peripheral to barrier capacitance. Many of the larger dots tend to have degraded characteristics because of barrier defects although good I-V and C-V data could be obtained from selected 0.25- and 0.50-mm diameter dots.

a. Aluminum.   b. Gold.   c. Titanium-gold.   d. Molybdenum-gold.

Figure 22. Representation of capacitance-voltage profiles for four Schottky barrier metallizations on natural (unetched) silicon surfaces. (Solid curves: immediately after metal deposition; dashed curves: after stabilization. Both scales are logarithmic. Vertical scale is density ranging from 10^{14} to 10^{17} cm^{-3}; horizontal scale is depth ranging from 0.1 to 10 μm.)
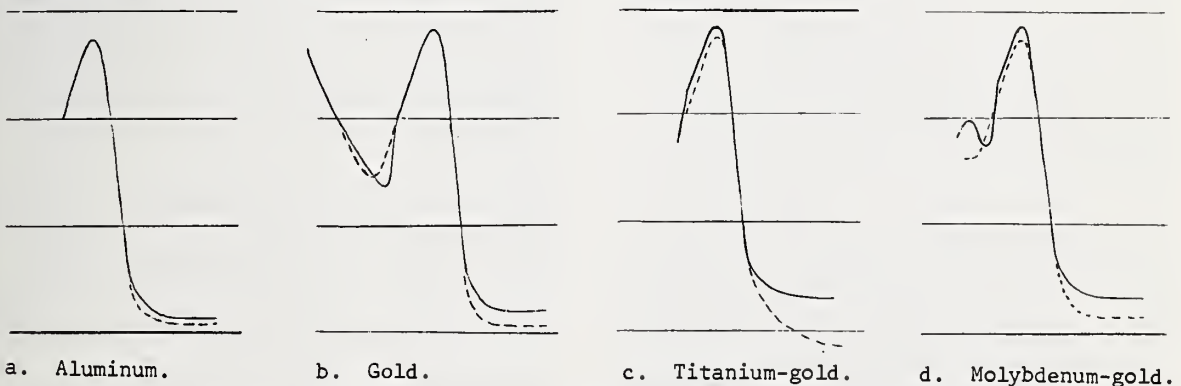
One of the largest sources of error in the measurement of dopant profiles by any C-V technique is associated with the determination of the area of the capacitor. In the present work, the areas were calculated from the average of two measurements of the metallization diameter taken 90 deg apart. The measurements are made with a high quality optical microscope using reflected light at 200X. Calibration is done using an eyepiece reticle and a stage micrometer each time the microscope is used. Individual diameter measurements are reproducible to better than 2 percent. The dots are often slightly out-of-round; although the diameter averaging corrects for this to some extent, the area determinations are less precise, but to an indeterminant degree. Dots with edge notches are not used for C-V measurements, nor are significantly elongated dots or dots with damage or imbedded dirt. Unobservable flaws may result from possible spots or poor adhesion or defects in the silicon beneath the surface. Errors due to such sources can be eliminated by measuring C-V curves for six to eight diodes and discarding any curves that deviate significantly from the norm established by the remainder that agree closely. Usually one out of six 0.12-mm diameter dots is found not to be in agreement with the rest.

In measuring dopant profiles by automatic C-V profiling techniques [61], the probing voltage is swept for the calculation of dopant density as a function of depth. The influence of the rate at which the voltage is swept was determined in an experiment in which a typical profile was measured for five values of the voltage sweep rate with the use of a commercially available automatic C-V profiler. The voltage was always started at 20 V and decreased to 0 V; the initial sweep rate ranged from about 8 V/s to about 0.7 V/s, but the sweep rate in each case decreased significantly as the voltage approached 0 V. Significant distortions of the measured profile were observed for sweep rates of about 1 V/s or greater.

It was found that the presence of normal overhead room illumination does not affect the measured dopant profiles for any of the metal systems. However, if the barrier is illuminated by a microscope lamp (such as is used while contacting the dot with the probe to complete the electrical circuit) the profiles are significantly distorted. For the aluminum barrier, the effect of this intense illumination is to depress the peak, fatten the width at high densities (near the peak) and raise the apparent background density.

The C-V technique was found to yield profiles only for implantation doses less than about 3×10^{12} cm^{-2}. Below this dose it was demonstrated that both the peak density and the density in the tail of the distribution vary in direct proportion to the dose. The peak density is assumed to be proportional to the dose at levels up to about 10^{17} cm^{-2}, above which the implanted concentration becomes so great that stoichiometric or chemical changes, film growth, sputtering, etc., may cause other effects in implanted profiles. Recently techniques other than C-V profiling have been used to demonstrate that the tail of the distribution originates from channeling effects [63,64]. One can assume on this basis that the channeling tail on random implanted distributions increases proportionally with the peak density and with the implanted dose up to the point where the silicon is made totally amorphous (at a dose of about 5×10^{14} cm^{-2}), and then that it remains constant. With this simple model one can develop a representation for profiles from misaligned (or off-axis) implantations at doses above the upper limit amenable to direct study by C-V profiling.

Profile Measurements — Initial determinations of range, R_p, and range straggle, ΔR_p, have been made as a function of ion energy for implantations of aluminum, gallium, indium, arsenic, antimony, and bismuth 7 deg off the (111) plane of silicon. Except for aluminum, the experimentally determined values of R_p agreed well with the calculations of both Gibbons *et al.* [21] and Brice [65] as did the previously determined measurements on boron- and phosphorus-implanted silicon (NBS Spec. Publ. 400-19, p. 33).[¶] For aluminum the measured ranges were in good agreement with the calculations of Brice [65] and earlier calculations of Johnson and Gibbons [18], but were significantly smaller than the more recent calculations of Gibbons *et al.* [21].

Preliminary measurements indicate that implanted profiles are quite sensitive to angle of incidence and crystal direction even in off-axis implantations. The effect appears to be greatest in the case of (110) surfaces and less in the cases of (111) and (100) surfaces. Since the deviations occur principal-

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[¶]Note that in all cases the implantations were made into 100-Ω·cm substrates of the *same* conductivity type rather than opposite, as reported previously. - *Ed.*

ly in the tail of the distribution, they may be more significant for low-dose implantations (below 5×10^{14} cm^{-2}).

(R. G. Wilson[#] and D. M. Jamba[#])

6.3. Passivation Integrity

Three methods are being investigated for application to the decoration of localized structural defects, such as pinholes and microcracks, in oxide, glass, or nitride passivation overcoats on metallized integrated circuits. These include selective chemical etching, electrophoretic cell, and corona discharge techniques. A preferred method is being sought which does not damage defect-free areas, can decorate latent or partial defects such as thin spots, and can be adapted for automated counting. Both silicon dioxide and phospho-silicate glass (PSG) chemically vapor deposited (CVD) on aluminum metallization were studied [66].

Selective Chemical Etching — In this method, the specimen is immersed in an acid solution which attacks the aluminum through cracks or holes in the overcoat. Various etchant compositions, temperatures, and times were studied to determine an optimum procedure. The results were compared against those obtained with a "standard" etchant composed of 74.1 volume percent phosphoric acid (85%), 7.4 volume percent nitric acid (70%) and 18.5 volume percent distilled water in which the specimen is etched at 50°C for a time 25 percent longer than is necessary to just etch through the aluminum (etch time factor of 1.25).

Nine different compositions, based on various ratios of the above acids and also including acetic acid or a surfactant, were formulated and compared using integrated circuits with a high density of uniformly distributed microcracks as the test specimens. The time required to etch through the aluminum film at 50°C was experimentally determined for each etchant composition; this time was multiplied by 1.25 to establish the appropriate etch time. No difference in defect detection was observed.

The standard composition was tested at 40°C and 60°C for times adjusted to maintain the

etch time factor at 1.25; again no differences were observed. The lateral etch rate for the standard composition at 50°C was tested by progressively etching a specimen and measuring the half-width of the aluminum removed under the glass. For etch time factors greater than one the etch rate was constant (0.4 µm/min contrasted with a vertical etch rate of 0.9 µm/min). It was concluded that, although an etch time factor of 2.50 makes some defects (not noticeable when etched half as long) visible, an etch time factor of 1.25 is best for maximum planar resolution in specimens with a high density of defects.

The effect of ultrasonic agitation on the etching at 50°C of aluminum under cracked glass was investigated by using specimens that had been etched under normal conditions with an etch time factor of 1.25. No new defects became visible as a result of continued etching with ultrasonic agitation. However, the protruding glass film overhang above the etched out aluminum was removed by this treatment, leading to irregularly tapered aluminum edges. The aluminum etch rate increased by a factor of approximately three. No advantage was found by this technique.

Impregnation with etchant under reduced pressure (0.3 torr) was tested to see whether removal of air from the defects prior to etching could increase the defect detection sensitivity. A pre-etched specimen was used, as above. No new defects could be discovered by this technique, but the aluminum etch rate again increased three-fold, probably due to increased speed of penetration of the etchant.

Electrophoretic Cell Method — In the electrophoretic cell method, the wafer or device is held in a liquid suspension of decorating particles. A voltage is applied between the wafer and an opposite electrode, causing the particle to move toward and deposit on the wafer in regions not protected by the nonconducting overcoat. Several different powders were tested as decorating particles in two liquid vehicles. Decoration of pinholes was achieved by this technique. However, even under the best conditions there are several drawbacks to this method. With conducting liquids there is no possibility of detection of partial pinholes or of very fine cracks. Partial pinholes can be detected with insulating liquids, but their unwanted deposition on good oxide occurs. This latter effect is caused by capacitive charging of the oxide by the charged particles. Other difficulties encountered included adhesion

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[#]Work performed at Hughes Research Laboratories under NBS Contract No. 5-35891. NBS contact for additional information: K. F. Galloway.

problems and random background deposition not related to defects.

Corona Decoration Methods — In this technique the wafer is subjected to a low current corona discharge in dry nitrogen at room temperature for several seconds to deposit a surface charge on the insulator regions. The wafer is then immersed in an insulating liquid containing charged decorating particles. For the case of charges of like sign on both the insulator and the particles, the particle is deposited on the conducting regions of the wafer (such as pinholes) and on regions of low potential or disturbed field pattern (such as partial pinholes). For opposite sign of charge, the particles are deposited on the insulator region only, permitting reverse decoration of defects. A very fine manganese-doped zirconium silicate phosphor powder was selected for the initial tests. Its small particle size makes it particularly advantageous. Observation of the fluorescing particles in the microscope is striking and allows easy detection of defects.

Evaluation of the direct decoration corona technique showed it to have important advantages over the electrophoretic cell method. It resulted in a cleaner background since the charge on the insulator acts to repel the decorating powder. It was found to be reproducible in repeated testing of the same wafer, and with certain simple modifications in the technique, fine cracks and relatively large partial pinholes could be detected.

With special test patterns for phosphor deposition, the effect of corona source voltage, wafer-to-source spacing, and immersion time of the wafer in the phosphor suspension were determined. Increasing the immersion time up to 12 s resulted in greater phosphor deposit and improved the detectability of small pinholes. For times greater than 12 s, portions of the deposit were sometimes removed. For a 2.5-cm wafer-to-corona-source spacing, increasing the corona voltage from 6 to 10 kV was found to result in increased deposition and improved detectability. Some scatter of phosphor not related to pinhole defects (as decorated by etching techniques) was observed. Larger pinholes were decorated but some smaller ones, subsequently decorated by etching techniques, were missed. Decreasing the wafer-to-source spacing lowered the amount of deposited phosphor, and slightly decreased the detectability. Closer spacing and higher voltages may result in damage to the wafer. The most suitable conditions (10 kV in the corona wires with a 2.5 cm spacing)

resulted in decoration of pinholes with a diameter of 1.5 µm or more.

By using a special test pattern to etch a 500-nm thick silicon dioxide film thermally grown on a silicon wafer and then regrowing 200 nm more oxide on the patterned wafer, partial pinholes 500 nm deep with 200 nm of oxide remaining at the bottom of the hole were simulated. The wafer was heated to 100°C for 10 s between charging and immersion in the phosphor suspension; the partial pinholes with diameter of about 2 µm or more were decorated but 1 µm diameter partial pinholes were not. Without the heat treatment, partial pinholes with diameter less than about 5 µm could not be detected. It is believed that the elevated temperature causes charge on the oxide in the bottom of the partial pinhole to leak away at a faster rate than on the thicker oxide, thus enhancing the phosphor decoration. Thinner bottom layers were also prepared and tested with similar results. In the decoration of actual device wafers and comparison with etch detection methods, no partial pinholes could be found. Thus, it was concluded that if partial pinholes exist in the passivating layers of these device wafers they are smaller than about 2 µm in diameter. This is certainly not surprising since one might expect a defect as large as 2 µm in diameter to penetrate the passivation layer completely.

It was also found that very fine cracks could be more readily observed by exposing the wafer to humid ambient for several seconds between charging and phosphor deposition. This allows surface conduction to leak away charge from the boundary of the crack, producing a low voltage pattern along the crack which could be readily decorated with phosphor.

The corona decoration procedure was carried out on production wafers to establish the nondestructive nature of the test. The wafers were tested on automatic test equipment before and after decoration and removal of the phosphor. The yield maps were essentially identical; thus it can be concluded that the devices were not damaged by the decoration and removal procedures.   (W. Kern[x], R. B. Comizzoli[x], and C. E. Tracy[x])

6.4. Process Chemicals Characterization

Improved stability of MOS devices under bias-temperature stress has been reported to result from the addition of small amounts of hydrogen chloride (HCl) or chlorine (Cl_2) to the oxidation furnace ambient [67-69]. This improvement is attributed to an interaction between chlorine and sodium which effectively immobilizes the latter. Kriegler [70] has shown that small amounts of water vapor in the furnace ambient can destroy the stabilizing effects of the chlorine. The degradation of the oxide is attributed to the inability of the chlorine species present to interact with the sodium.

To study the effects of excess water vapor on the chlorine species, equilibrium partial pressures of the various species in the chlorine-hydrogen-oxygen (Cl-H-O) system were calculated using a modified SOLGAS program [71]. The calculations were performed for temperatures from 700° to 1300°C for given ratios of the input gases holding the total pressure at 1 atm. The results for the $HCl-O_2$ system are given in figure 23 for 2 and 20 volume percent HCl. The predominant species are O_2 and HCl. In addition Cl_2 and H_2O are present in equal amounts from the reaction

$$2HCl + \frac{1}{2} O_2 \rightarrow Cl_2 + H_2O.$$
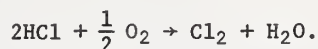
If excess water vapor is added to the ambient, the H_2O concentration is enhanced and the Cl_2 concentration is depressed as illustrated in figure 24 for an oxygen atmosphere with 1 volume percent HCl and 0, 0.26 or 0.66 percent H_2O.
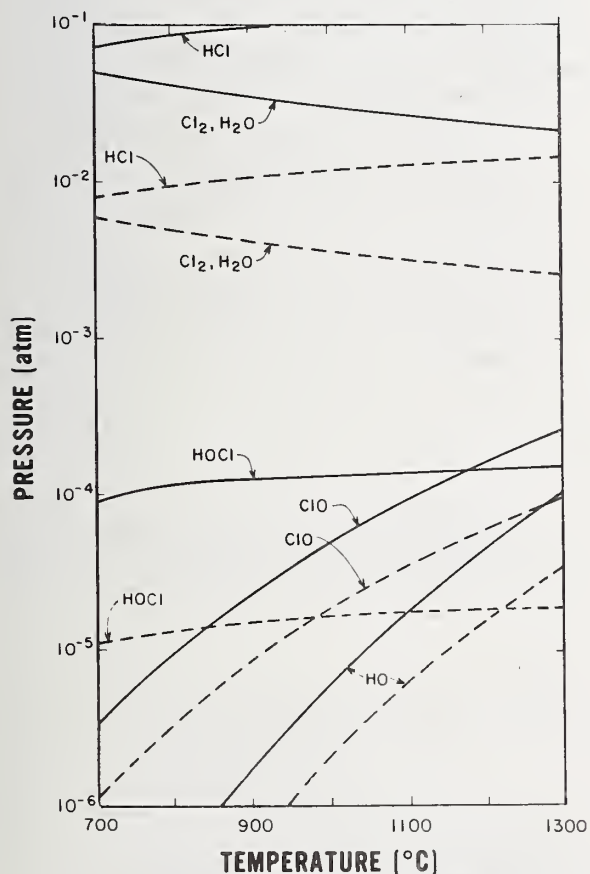
Figure 23. Equilibrium partial pressures in 2% HCl-98% O_2 and 20% HCl-80% O_2 mixtures. (Total pressure = 1 atm; solid curves: 20% HCl; dashed curves: 2% HCl.)
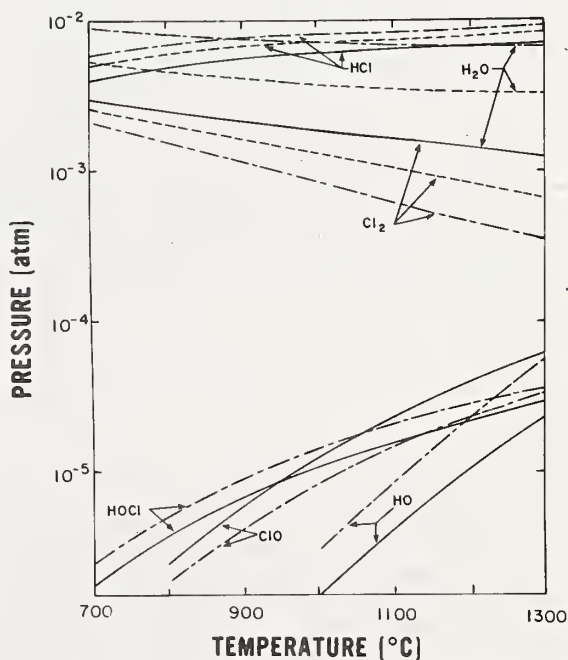
Figure 24. Equilibrium partial pressures in 1% HCl-99% O_2 mixtures with 0, 0.26%, and 0.66% added water vapor. (Total pressure = 1 atm; solid curves: 0 added H_2O; dashed curves: 0.26% added H_2O (2 Torr); broken curves: 0.66% added H_2O (5 Torr).)
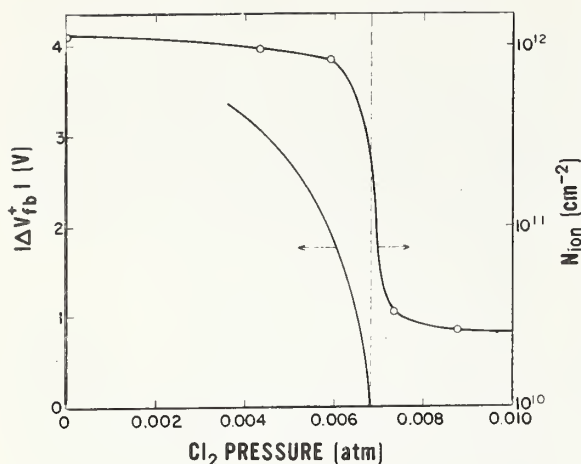
Figure 25. Mobile ion density, N_{ion}, and magnitude of the flat-band voltage shift, ΔV_{fb}^{+}, as a function of equilibrium chlorine pressure in HCl oxidations on (100) silicon at 1150°C. (After data of Kriegler [70]; variations in mobile ion density are result of variations in the initial HCl-O_2 ratio; variations in flat-band voltage shift are result of variations in amount of water vapor added to a 6% HCl-94% O_2 mixture.)

The effect of the reduced chlorine pressure can be seen from Kriegler's data [70] which are replotted in figure 25. The upper curve relates the mobile ion density, N_{ion}, in the oxide to the chlorine pressure in the furnace which was varied by altering the initial HCl/O_2 ratio. The lower curve relates flat-band voltage shifts, under bias-temperature stress, to the chlorine pressure in the furnace; in this case the chlorine pressure was varied by adding excess water vapor to a 6 volume percent HCl-O_2 mixture. Below a critical chlorine pressure, whose exact value probably is dependent on the amount of sodium present, the mobile ion density and flat-band voltage shift both increase significantly indicating a lack of stabilizing influence by the chlorine.

These results suggest that both the HCl fraction and the water vapor concentration must be controlled if the chlorine is to stabilize the oxide. Since the level of water vapor easily detectable in HCl is less than 10 parts per million [68], the degree of control needed appears to be well within the capability of available measurement technology.
(R. Tressler[+], J. Stach[+], and D. Metz[+])

7. PHOTOLITHOGRAPHY

7.1. Photoresist Exposure*

Photoresist films are commonly exposed by ultraviolet light in the fabrication of semiconductor devices. The ultraviolet light source is commonly a short-arc, mercury lamp which provides radiation with a spectrum that consists principally of six high intensity, approximately monochromatic bands at wavelengths of 312, 335, 365, 405, 435, and 540 nm. Exposure times are usually determined from single parameter irradiance measurements. These measurements are usually made with detectors sensitive to 300- to 500-nm wavelength radiation, for example, and produce a photocurrent that is weighted by all of the radiation bands. However, this photocurrent does not have a known relationship to the active light energy which causes photolysis in the resist because the detector is the light integrating medium when the total source irradiance is measured and the resist is the light integrating medium when it is exposed. These two media do not integrate the radiation equally since their respective sensitivities are not the same.

From an analysis of the exposure process, a basis for establishing exposure indices of resists has been developed [72]. If monochromatic radiation of wavelength λ_μ and irradiance E_μ is incident on the photoresist for a time t_μ long enough to expose the resist completely, the energy density, $H_{c\mu}$, is given by

$$H_{c\mu} = E_\mu t_\mu. \tag{3}$$

The sensitivity, S_μ, of the photoresist to energy of wavelength λ_μ can be defined as

$$S_\mu = 1/H_{c\mu}. \tag{4}$$

If the photoresist is exposed simultaneously to all six discrete bands, designated μ-

bands, for a time t to completely expose the resist, Van Kreveld's additivity law [73] requires that the fractional exposure energy density contributed by each band be $S_\mu E_\mu t$ so that the sum of all contributions is:

$$\left(\sum_{\mu=1}^{6} S_\mu E_\mu\right) t = 1. \tag{5}$$

Hornberger et al. [74] have calculated the variation of the concentration of bleachable chromophore (the initiator in negative resists or the inhibitor in positive resists) as a function of the exposure times and film thickness. If the exposure criterion is adopted that optimum exposure is reached when a critical chromophore concentration exists in a film layer dx thick located at the extreme film thickness d, exposure times may be read directly from Hornberger's plots of chromophore concentration *versus* film thickness for various exposure times. The values of the exposure times obtained in this manner are plotted as a function of film thickness in figure 26 which shows that the exposure times are exponential functions of the film thickness throughout a range of chromophore concentration from 0.80 to 0.07. This range includes the critical chromophore concentrations for exposure discussed by Hornberger et al. [74] for positive resists and Blais [75] for negative resists. Therefore, since the exposure times obtained in this way are proportional to the incident exposure energies, it can be assumed that, for each band μ,

$$H_{c\mu} = H_{o\mu} 10^{\alpha_\mu d}, \tag{6}$$

where $H_{o\mu}$ is a threshold energy density which may be interpreted as the exposure energy density necessary to expose a hypothetical resist film of zero thickness, and α_μ is the slope of the appropriate curve in figure 26. If eqs (4), (6), and (5) are combined, one obtains

$$\sum_{\mu=1}^{6} \frac{E_\mu}{H_{o\mu}} 10^{-\alpha_\mu d} = \frac{1}{t}. \tag{7}$$

This relationship provides the basis for an exposure sensitivity specification. The values of the parameters $H_{o\mu}$ and α_μ can be
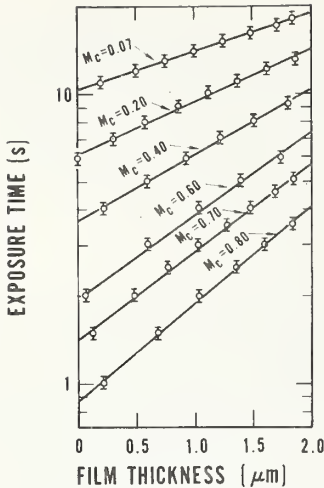
Figure 26. Exposure time required to obtain a critical chromophore concentration, M_c, in an infinitesimal layer located at the extreme thickness of the film. (After data of Hornberger *et al.* [74]. Error bars represent ±5 percent uncertainty in exposure time.)

used both to specify the photoresist exposure sensitivity and for control of exposure. These values are independent of film thickness and can be determined for each wavelength band by measuring the time for complete exposure as a function of resist thickness. To assure that these exposure times relate to those in actual use, it is suggested that complete exposure be defined as the exposure that produces lines in the developed resist image that have the same width as the lines on the printing mask. The values E_μ can be determined experimentally by using appropriate narrow bandpass filters and a photodetector with known response:

$$E_\mu = I_{D\mu}/S_{D\mu}, \tag{8}$$

where $I_{D\mu}$ is the detector photocurrent and $S_{D\mu}$ is the detector sensitivity at the wavelength λ_μ.

Comparative photoresist "speeds" may be obtained from the specified values of α_μ and $H_{o\mu}$ for any photoresist by combining them with the values of E_μ that are typical for the exposure equipment being used to calculate the value of $1/t$ from eq (7); the larger the $1/t$ value, the "faster" the resist.

To control exposure, the band intensities are simultaneously and continuously monitored by a series of detectors, each combined with a different thin film, narrow bandpass filter corresponding to a particular mercury spectral line. These continuously monitored band intensities are transmitted to a microprocessor which has the appropriate values of α_μ, $H_{o\mu}$, and d stored in its memory. The microprocessor is used to analyze this information on a real-time basis to give continuous values of the required exposure times and control the exposure accordingly. This means of control automatically and continuously adjusts the exposure time for any changes that may occur in the intensities of the spectral bands. Furthermore, such a monitoring system could also calculate and automatically correct for changes in exposure times that are caused by changes in the optical densities of photomasks providing the optical density values were read into the microprocessor.

Many of the relations proposed in this work need to be verified experimentally before they can be used either as a basis for standard specifications of photoresists or for calculating and monitoring exposure times. The proposed equal line width criterion for optimum exposure must be experimentally examined to assure its equivalence to the concept of a critical inhibitor or initiator concentration existing in the layer dx at the film thickness d. It should be kept in mind that the values of α_μ and $H_{o\mu}$ may be functions of the development. If this turns out to be the case, the complete development specification must become part of the total resist exposure specification. The substrate for the photoresist film must also be carefully chosen since the presence of standing light waves and interference effects from reflections at the photoresist-substrate interface are important in determining exposure.

(D. B. Novotny)

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8.1. Square Array Collector Resistor

The square array collector resistor struc-
ture (NBS Spec. Publ. 400-17, pp. 25-26) [76]
was analyzed for the case when the backside
was conducting. The correction divisor to
obtain the actual resistivity from the mea-
sured voltage-current ratio was derived by
use of the method of images [3] for the case
of a wafer of infinite lateral extent but fi-
nite thickness. This correction divisor is
also applicable to the case of measurements
made with a mechanical square four-probe ar-
ray when the backside of the wafer is metal-
lized.

Resistivity is determined with a square ar-
ray by forcing current between two adjacent
probes, I_1 and I_2, and measuring the voltage
between the other two probes; see insets C
and D of figure 27. If the substrate is as-
sumed to be semi-infinite in extent, the re-
sistivity, ρ_∞, can be calculated from [5]

$$\rho_\infty = \frac{2\pi s V}{(2 - \sqrt{2})I} = 10.726s \frac{V}{I}, \tag{8}$$

where V is the voltage, I is the current and
s is the probe spacing. If the wafer has a

finite thickness, w, eq (8) must be modified
to obtain the true resistivity:

$$\rho_w = \rho_\infty / C_4(w/s) \tag{9}$$

where

$$C_4(w/s) = 1 + \frac{4}{2-\sqrt{2}} \sum_{n=1}^{\infty} (-1)^n \left(1 + \frac{4n^2 w^2}{s^2}\right)^{-\frac{1}{2}}$$

$$- \frac{2\sqrt{2}}{2-\sqrt{2}} \sum_{n=1}^{\infty} (-1)^n \left(1 + \frac{2n^2 w^2}{s^2}\right)^{-\frac{1}{2}}$$

is the correction divisor for the case con-
sidered. This function is tabulated in table
9 for w/s ratios from 1 to 10. Also given in
the table are values of the correction divi-
sor $C_3(w/s)$ derived by Uhlir [5] for the case
of a square array on a wafer with a noncon-
ducting backside.

It is more convenient to use eq (8) rather
than the more complex corrected relationship,
eq (9), in calculating resistivity from

Figure 27. Magnitude of resistivity measure-
ment errors for four-probe arrays.

Table 9

Resistivity Correction Factors for Square
Four-Probe Arrays

w/s	C_3	C_4
1.0	1.3443	0.7700
1.5	1.1249	0.9111
2.0	1.0572	0.9584
2.5	1.0305	0.9776
3.0	1.0180	0.9867
3.5	1.0115	0.9915
4.0	1.0078	0.9942
4.5	1.0055	0.9959
5.0	1.0040	0.9970
5.5	1.0030	0.9977
6.0	1.0023	0.9982
6.5	1.0018	0.9986
7.0	1.0015	0.9989
7.5	1.0012	0.9991
8.0	1.0010	0.9993
8.5	1.0008	0.9994
9.0	1.0007	0.9995
9.5	1.0006	0.9996
10.0	1.0005	0.9996

square array measurements. The relative error introduced by this is given by

$$\frac{\rho_\infty - \rho_w}{\rho_w} = C_i - 1, \qquad (10)$$

where C_i is the correction divisor appropriate to the geometrical conditions. The magnitude of this error is plotted in figure 27 as a function of w/s for the cases of measurements on wafers with conducting and nonconducting backsides. For comparison, the magnitudes of the errors introduced by using the uncorrected relationship for the collinear four-probe array (see eq (1), sec. 3.1.), based on calculations of Valdes [3], are shown in the figure as dashed curves. Note that for both arrays, the error is negative (the uncorrected resistivity is less than the true resistivity) for the case of measurements on wafers with conducting backsides while the opposite is true for the case of measurements on wafers with nonconducting backsides.

For the square array collector resistor structure on test pattern NBS-3 (NBS Spec. Publ. 400-12, pp. 19-22) [44], the probe spacing is 2.25 mil (57.2 μm). The error introduced by using eq (8) when the backside is metallized is 0.6 percent or less for wafers with thickness of 9.0 mil (230 μm) or more. A preliminary experiment was conducted using a square array collector resistor structure fabricated with the large-pipe base mask [76] of test pattern NBS-3 on wafer A1.8B-1, a 1.8-$\Omega\cdot$cm boron-doped silicon wafer, 285 μm thick with a nonconducting backside. Resistivity, ρ_∞ corrected to 23°C (see sec. 3.1.), was measured on 17 structures. The wafer was split. The larger portion, which contained 12 structures, was thinned to 185 μm by lapping the backside, and the resistivities were redetermined. The average change in ρ_∞ for these 12 structures was +1.16 percent with a sample standard deviation of 0.13 percent, in reasonable agreement with the +1.08 percent calculated change in ρ_∞. The other five structures showed an average change of -0.03 percent with a sample standard deviation of 0.05 percent. The thinned portion of the wafer was metallized by evaporating aluminum on the backside and heating it to 500°C for 20 min in nitrogen, and the resistivities were redetermined again. The average change in ρ_∞ for the 12 structures in this case was -2.88 percent with a sample standard deviation of 0.24 percent, slightly larger than the calculated change of -2.62 percent. The other five

structures, which were not subjected to the heating cycle showed an average change of -0.03 percent with a sample standard deviation of 0.03 percent. These results appear to agree with the calculations within the systematic experimental errors which are expected to be present.

(M. G. Buehler and W. R. Thurber)

8.2. Emitter-Base Electrical Alignment Test Structure

In the fabrication of integrated circuits the alignment of one mask with another is a critical aspect. An electrical alignment structure for use in monitoring alignment of a contact mask with a diffusion mask has been reported [77]. To use this structure, 13 probe contacts are required.

A new electrical alignment resistor was developed for determining the alignment of the emitter diffusion mask with the base diffusion mask. With this test structure the alignment can be determined quantitatively in two orthogonal directions with the use of eight probe contacts. The test structure consists of a base diffusion which forms a square path that is contacted at eight places as shown in figure 28. Rectangular emitter diffusions overlap the base diffusion at four locations and pinch the base at these locations. Opposite emitter diffusions are offset from each other by a known amount, ΔL, typically about 5 μm (0.2 mil).*

To determine the left-to-right misalignment, current is passed into I_1 and taken from I_2 as shown in the figure. The potential differences between V_1 and V_2, V_2 and V_3, V_1 and V_3, V_4 and V_5, V_5 and V_6, and V_4 and V_6 are measured. If these are designated as V_{21}, V_{32}, V_{31}, V_{54}, V_{65}, and V_{64}, respectively, the misalignment distance, ΔL_2, is given by

$$\Delta L_2 = \Delta L \frac{V_{64}(V_{21}-V_{32})}{V_{31}(V_{54}-V_{65}) - V_{64}(V_{21}-V_{32})} \qquad (11)$$

provided that the misalignment, the lengths of the base channels, the widths of the emitter diffusions, and the emitter and base

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* This displacement was suggested by D. Ritchie, Tektronix, Inc., Beaverton, Oregon, as a means for calibrating the structure.
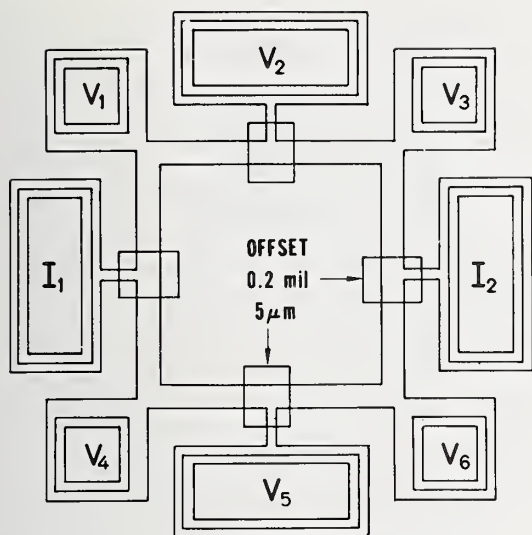
Figure 28. Emitter-base alignment resistor.

junction depths are assumed to be the same in the top and bottom current paths. It is not necessary to assume equal currents in both paths. To obtain the top-to-bottom misalignment the probe locations are shifted 90 deg counterclockwise, and the above procedure is repeated.

Use of the structure requires that only dc electrical measurements be made so that the method is both rapid and economical when performed on an automatic wafer probing apparatus. It can be used to determine lateral misalignment which results from operator error or from mask errors such as run out or variation in magnification from mask to mask. If significant rotational misalignment is present, eq (11) does not give an accurate value for the misalignment distance in either current path. However, rotational misalignment, which is usually small, can be evaluated from measurements on structures at various locations on the wafer. (M. G. Buehler)

8.3. Test Patterns with Modular Cells

A common practice within the semiconductor industry is to arrange probe pads around the periphery of the test pattern and to connect the test structures to the probe pads with metal lines [78]. This is done primarily for convenience in testing; frequently when the test pattern is spotted at selected locations on a wafer of integrated circuits, the probe pad layout is identical to that of the

circuit itself [79]. However, the metal interconnections between test structure and probe pads can be quite long; in some cases the resistance introduced may affect the measured properties of the test structure. Even if the probe pads are placed very close to the test structure, their size, contact opening, and location may also affect the characteristics of the test structure.

Such variability does not lend itself to standardization of the test structures because each test pattern becomes a new adventure in design. This leads to the design of unproven test structures and to uncertainty when comparing results from different test patterns. To avoid such problems it is necessary to consider the probe pads as an integral part of the test structure layout. This means that the pad location and metal interconnections to the test structure cannot be left to the discretion of the test pattern designer. In several cases, test structures, previously tested at NBS and found to be satisfactory, have been found not to work satisfactorily at other laboratories because of differences in contact and probe pad layout which led to such problems as shorts between probe pads and active regions of the structure, excessive contact resistance, or distortion of current paths.

A key to the full utilization of test patterns is a modular arrangement of probe pads which allows the use of standardized test structures. The test pattern is organized in a hierarchy whose smallest part is the test structure. The structures form the test cells which comprise the test pattern. A study was undertaken to determine the most suitable modular test cell layout by considering the probe pad size and arrangement along with the test structure design.

Probe pads used with the test structures in a test pattern have different size requirements than bonding pads associated with an integrated circuit. A test pattern generally has many more pads than an integrated circuit, and the pads usually take up a large fraction of the area of the test pattern. In addition, test patterns are usually tested while in wafer form, rather than after they are bonded. These constraints restrict the size of the test structure probe pad to the smallest practical area. Currently, the size of probe pads varies from a square 50 μm (2 mil) on a side to a square 150 μm (6 mil) on a side. Smaller pads can be probed with manual equipment, but 50 μm (2 mil) appears to be the practical lower limit for probing a 100-mm
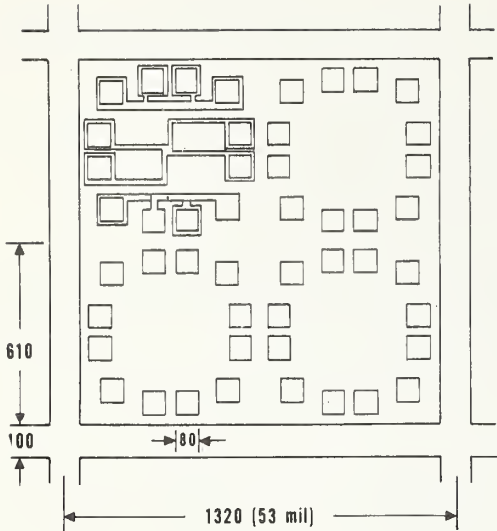
Figure 29. Test pattern with four 4 by 4 square test cells. (Dimensions in micrometers unless otherwise noted.)
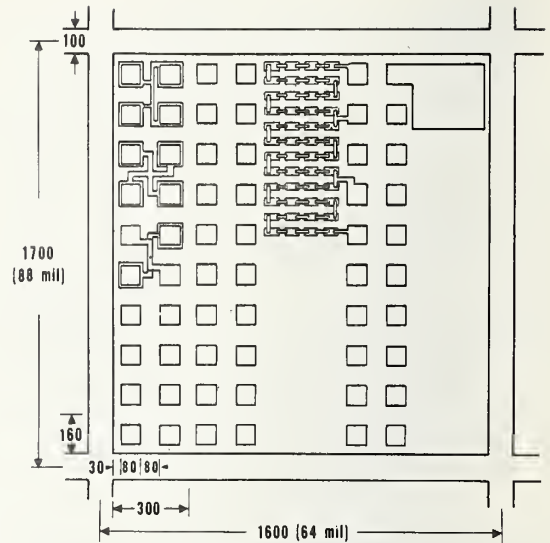
Figure 30. Test pattern with 2 by 10 rectangular test cells. (Two of the five cells were omitted to leave room for large area and chain structures. Dimensions in micrometers unless otherwise noted.)
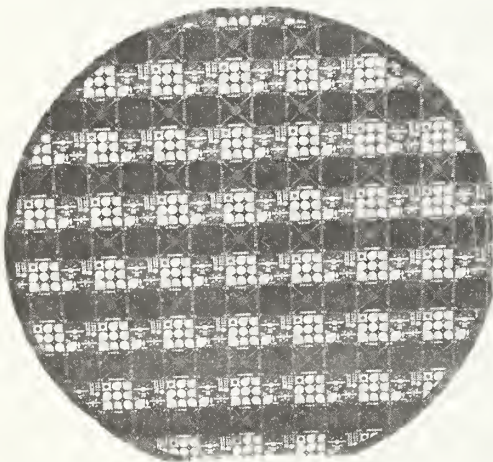
Figure 31. Photomicrograph of test pattern NBS-3 fabricated on 2-in. (50 mm) diameter wafer. (Magnification: ~1.5X.)
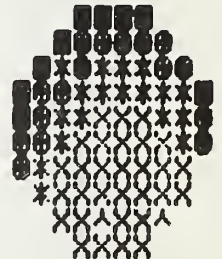
Figure 32. Base sheet resistance wafer map with data points only.

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diameter silicon wafer with automated wafer probing equipment. For initial tests, a square probe pad 80 μm on a side has been chosen as the standard size.

The probe pad arrangement within a test cell was examined with several requirements in mind. A single probe card must be able to address all the test structures within the test cell. All types of test structures must be accommodated within the test cell configuration. The types include discrete resistors and transistors, resistor chains, and large area structures for layer integrity tests. The number of pads per cell is influenced by the time required to electrically scan from structure to structure as compared to the time required to mechanically scan from structure to structure. Electrical scanning between structures is generally much faster than mechanical scanning which indicates that the number of pads per cell should be large so as to minimize the mechanical scan time. However, there is a practical limit to the number of pads that can be probed at the same time.

Brooksby [80] has described a modular test pattern biased on a square 4 by 4 array with 12 pads per cell as illustrated schematically in figure 29. The rectangular array illustrated schematically in figure 30 offers certain advantages over the square array in terms of conservation of area and flexibility. It is not restricted to the 2 by 10 array shown in the figure. In its most general form the rectangular array is a 2 by N array where N is an arbitrary number of probe pads. Three four-terminal test structures fit into the square 4 by 4 array cell, but four such structures can be accommodated by the rectangular array in the same area. The square array is not as flexible as the rectangular array with regard to the addition or deletion of test structures. In the rectangular array, omission of a cell or two can accommodate large area and resistor chain structures as illustrated in the figure. In the square array the metallization pattern associated with a particular structure depends on its location within the array; in the rectangular array the pad configuration, and hence the metallization pattern, is invariant. Once the number of pads for the square array has been established then the electrical to mechanical scan time ratio is fixed for a particular test routine. But for the rectangular array, the electrical to mechanical scan time ratio is adjustable by lengthening or shortening the array.

During this study many representatives of the semiconductor industry were consulted. The consensus reached, together with the considerations outlined above, led to the choice of the rectangular cell in a 2 by 10 configuration as the vehicle for the next test patterns to be designed in the program. With the development of a computerized library of test structures, selected structures can be assembled rapidly into a test pattern to meet the needs of a particular fabrication technology. The first of these is scheduled to be based on bipolar TTL technology.

(M. G. Buehler)

8.4. Mapping of Geometrically Dependent Data in Two Dimensions

It is frequently of considerable importance in connection with device processing to obtain information regarding the variability of characteristics across a semiconductor wafer. Such variations can be determined from measurements on devices or test patterns, such as NBS-3 (NBS Spec. Publ. 400-12, pp. 19-22) [44], repeated across the wafer as shown in figure 31. This type of data is frequently displayed as histograms or contour maps. However, in many cases the trends are more easily visualized if the data are presented as density maps. Data presentation by this format offers several advantages; it provides a pictorial representation of a large amount of data and permits easy identification of positional dependencies and anomalies.

A computer program in modified BASIC language [81] was developed to tabulate the data into seven magnitude cells and to map them in two dimensions. The program has been run and verified on a small minicomputer with 24 K words of core memory where each word consists of two 8-bit bytes. At present, the display method is restricted to cathode-ray tubes; however, with minor modifications it could be extended to line printers.

Several presentations are available. The simplest includes a tabulation of the input data into magnitude cells and assignment of keys to these cells. Using these keys, the data are positionally mapped. As an example, base sheet resistance data obtained[†] on 75 van der Pauw sheet resistors (test structure 3.22) fabricated on a 2-in. (50-mm) diameter wafer, are shown in figure 32. The table on

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[†] These data were obtained by means of an automatic wafer prober connected to a computer controlled data acquisition and analysis system (NBS Spec. Publ. 400-12, p. 4).

the left side of the figure presents the magnitude cells, the number of measurements that fall within each cell and the key for each cell. This key is used in the wafer map of the sheet resistance shown on the right. This presentation can be generated in 2 min.

A more complex presentation retains the table of magnitude cells and keys, but also provides for bilinear interpolation [82] between input data points. A second wafer map of the same input data, as above, but with inclusion of three interpolated points between each pair of input data points, is shown in figure 33. Provision has also been made for interpolating in place of data points which have been determined not to be valid. This more complex presentation requires 12 to 15 min but is much more readily visualized than the more compressed simple display.   (J. P. Chandler and J. M. David)

8.5. Test Pattern Design and Analysis for SOS/LSI

This task was undertaken to produce a set of overlay masks containing test devices and structures suitable for characterizing a large scale integration (LSI), silicon-on-sapphire (SOS) process (or other mask compatible processes), and to develop testing procedures for these structures.

The mask set, which is now being made, was designed principally for use with silicon-gate technology. A frequently used SOS process involves the use of only one type of silicon. This process makes use of a device that is unique to SOS-type technologies for providing either the n- or p-channel transistor for CMOS circuits. The device is a junctionless transistor formed from silicon of the same type as the source and drain and is sometimes called a deep-depletion transistor. The key to the successful operation of this device is that the silicon can be completely depleted throughout, and low minimum currents are thereby obtained. The operation of this device is otherwise very similar to that of MOS transistors with junctions. With the deep-depletion device a CMOS technology can be implemented with only a single epitaxial layer. Processing proceeds according to the following sequence:

(1)   Define epi islands (Mask Level 1)
(2)   Grow channel oxide (approximately 110 nm thick)
(3)   Deposit polysilicon (500 nm thick)
(4)   Diffuse polysilicon (p^+)
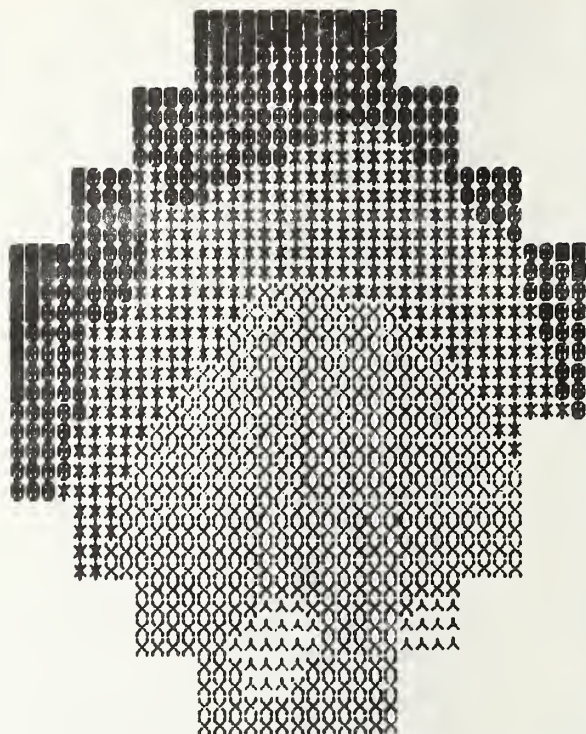
Figure 33. Base sheet resistance wafer map with interpolated points. (Same key as for figure 32.)

(5)   Define polysilicon (Mask Level 3)
(6)   Etch channel oxide (self-aligned)
(7)   Deposit n^+ doped oxide as diffusion source or p^+ diffusion mask
(8)   Define n^+ doped oxide (Mask Level 4)
(9)   Deposit p^+ doped oxide diffusion source
(10)   Diffuse n^+ and p^+ regions
(11)   Open contact holes (Mask Level 5)
(12)   Deposit aluminum
(13)   Define aluminum (Mask Level 6)
(14)   Deposit silicon dioxide overcoat (optional)
(15)   Open overcoat (Mask Level 7)

Note that in the single epitaxial process, Mask Level 2 is not mentioned. This level allows formation of devices from the opposite type of starting material. The precise use of this mask depends on the method used to create the two types of material. In one method this second level mask is used for definition of a second epitaxial layer of type opposite from the first. This method requires a compatible first level mask. In another method the second level mask is used as an ion-implantation mask; in this case the first level mask is the same as that used for the single epi process.

Precisely the same layout can be used for nonrefractory metal gate processes. In these processes the channel regions are not defined by the gate metallization. Slight modifications in all mask levels after the second are required to use these masks for metal gate processes. Space is allowed for certain metal gate structures which are not possible with self-aligned gates. Considerable duality exists between SOS and bulk CMOS processes. Since the bulk test structures need not be self-isolated (because of the testing procedure used), largely the same layout can be used for both SOS and bulk.

As noted previously (NBS Spec. Publ. 400-19, p. 47) the pattern has been partitioned into five classes, each intended to test a different aspect of the processing. The type I pattern provides a comprehensive collection of individual structures of nominal or typical dimensions. It includes a variety of crossovers, sheet resistors, contact resistors, MOS capacitors, diodes, and MOS transistors. These structures are useful as electrically accessible devices to test design and process parameters.

The type II pattern, intended to provide information regarding spatial variation of certain electrical parameters, was described in detail previously (NBS Spec. Publ. 400-19, p. 47). The type III pattern contains contact resistors, MOS capacitors, and MOS transistors of various sizes for the purpose of providing information regarding the effects of different geometrical features on key device structures.

The devices in the type IV pattern consist of MOS transistors, crossovers, and contact resistance structures. These devices are connected in series or in parallel with varying numbers of devices available in order to provide information concerning the reproducibility of a large number of identical devices.

The type V pattern is intended to provide information concerning the lithographic properties, the operation of certain basic CMOS building blocks, and their dynamic performance. The devices available include optically and electrically accessible lithographic structures, and certain CMOS building block structures such as ring counters, inverters, and gates.

A relatively complete analysis of a process used to fabricate a CMOS LSI circuit can be obtained from this collection of test structures. These structures depend only on the process and the device design; they are intended to be completely circuit-independent. The general partitioning chosen should be useful for any MOS technology. The specific layout may also be used in many cases. Many structures were designed such that the electrical access need not be changed for different technologies. This allows libraries of general test and analysis programs to evolve.

One of the most important features of the test structure design is that any device can be operated independently of any other device, even if common connections exist. This is allowed because the pads contacted by probes not being used for the test are assumed to be completely open and unable to provide a current path. For bulk silicon processes the substrate in addition to the unused probes may be completely isolated from ground during testing to eliminate the need for specific device isolation. This allows a much greater packing density for test devices.

(W. E. Ham[§] and J. M. David)

9. INTERCONNECTION BONDING

9.1. Non-Destructive Test for Beam-Lead Bonds

Test Device Fabrication — Procedures were refined for fabricating beam-lead devices with a few weak bonds for use in studying the acoustic emission test (NBS Spec. Publs. 400-12, pp. 31-32, and 400-19, pp. 48-50). A photomask set was obtained to pattern beam-lead bonding pads on thin-film chrome-gold substrates and permit removal of diffused chromium oxide [83] from the surface in preselected areas, while leaving it in others to impair the beam-lead bondability. Figure 34 shows a photomicrograph of an etched substrate in which the chromium oxide areas have been stained for better visibility. The four different patterns include a control with all well bonded beams, a single weak beam in the center, two weak beams in the center, and a single poorly bonded beam on a corner location.

To assure the fabrication of reproducible chrome-inhibited bonding pads, the following standard procedure was developed for processing the tantalum nitride, chrome, gold metallization:

(1) Initial wafer clean up. Place in boiling trichloroethylene for 15 min, rinse in semiconductor grade methanol, then bake at 200°C for 30 min.

(2) Photoresist application for the first masking operation, gold pattern etch. (a) Spin photoresist for 15 s at 3000 rpm. Bake at 75°C for 25 min. (b) Repeat step (2a) to obtain a double photoresist layer. (c) Expose through first mask for 15 s. (d) Develop for 30 s. (e) Wash in deionized water and blow dry. (f) Post bake at 120°C for 25 min. (g) Immerse in aqua regia for 4 min. (h) Strip photoresist in boiling acetone for 15 min, rinse in fresh acetone, wash in deionized water for 5 min and dry in air.

(3) Chromium up-diffusion and oxidation step. Bake substrates in air for 2 h at 310°C.

(4) Photoresist and exposure process for the second masking operation, preferential chromium oxide removal. Repeat steps (1) and (2) except in place of step (2g), etch with ceric ammonium nitrate [83] for 7 min. It is very important to etch in ceric ammonium nitrate within 1 h after the 120°C photoresist post bake. If the process of etching many substrates takes longer, then leave some of the substrates in the oven until ready for etching.

It should be pointed out that when using the chrome-diffused gold bonding pads, some degree of control over the beam-lead bond peel strength can still be exercised by varying the bonding parameters (force and temperature). In this manner the peel force for an individual beam can be varied from approximately 0.5 to 3 gf (5 to 29 mN).
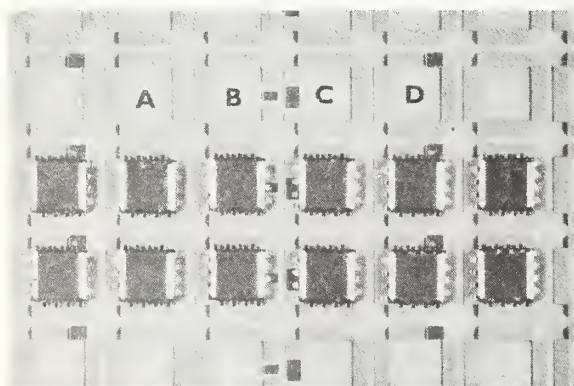
Figure 34. Photomicrograph of a patterned substrate showing chromium oxide areas (stained black) and bonded beam-lead devices. (Column A: all good bond areas; column B: one weak bond area, right center; column C: two weak bond areas, left center; column D: one weak bond area, top right corner. Magnification: ∿7X.)
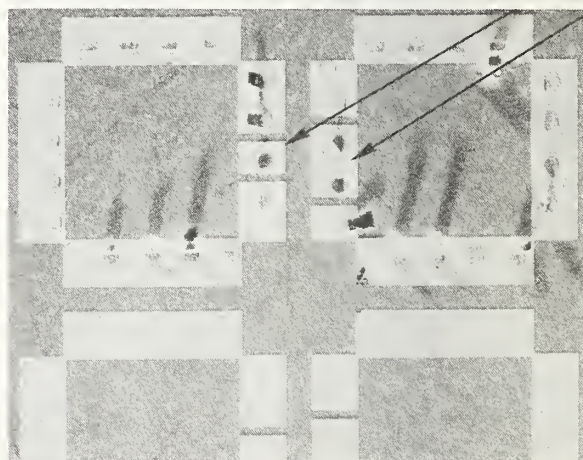
Figure 35. Photomicrograph of a portion of a patterned substrate from which bonded beam-lead devices have been pulled off. (Chromium oxide covered areas indicated by arrows. Magnification: ∿24X.)

A portion of a patterned substrate from which two bonded beam-lead devices were pulled off is shown in figure 35. All beams not bonded onto chromium oxide-masked gold areas either broke at the bond heel, the chip anchor, or in the beam span. However, two of the chromium oxide masked bonds lifted off and the third partially peeled before breaking. This latter beam demonstrates that while the chrome oxide on the surface weakens the bond it nevertheless still permits bonds having intermediate strength. (Y. M. Liu and G. G. Harman)

Instrumental Improvements — Two different types of force probes have been described previously (NBS Spec. Publ. 400-19, pp. 48-50). One was a force probe consisting of an acoustic emission detector attached to the end of an acoustic waveguide. Downward force is applied by the waveguide to the top of the die; any acoustic emission is transmitted upward to the detector. The other was a simple vacuum chuck with silicone rubber cup molded on its tip to fit the beam-lead die. This chuck can apply an upward lifting force of about one-half gram force per beam to the die; any acoustic emission signal is detected with a pickup attached to the substrate. Probes which can apply both downward and upward forces were prepared by drilling holes in the ceramic acoustic waveguide and molding the vacuum cup on the bottom. Two versions of these probes are shown in figure 36.

The modified probes are used in conjunction with substrate detectors. Two such detectors and mounts are shown in figure 37. The dark circle in the center of each mount is the acoustic emission detector. In the case of the mount in figure 37a, the substrate is held down by vacuum, while in the case of the mount in figure 37b, the detector was too large to permit adequate area for vacuum hold-down grooves, so the substrate is held down with a circular weight. In both cases the detector is forced upward against the substrate by a spring, which can be seen in only one of the photographs, and the detector surface has been coated with a thin layer of silicone rubber to facilitate acoustical mating of the detector with the substrate. Use of the coating avoids the necessity of using "sticky goop" or other viscous acoustic mating materials that must be removed from the substrate with solvents.

The primary method of using the new probe-detector system is by using a substrate detector tuned to the optimum substrate frequency, about 375 kHz, and a probe detector tuned to the optimum die frequency, about 1.1 MHz. The two acoustic emission signals can be recorded separately with the circuit shown in figure 38 or combined through a differential input preamplifier to give a complex waveform signal unmistakable for noise. A typical combined substrate-die acoustic emission waveform from a weak corner beam lead is shown in figure 39. (G. G. Harman)

Test for Threshold of Motion — In the course of investigating the acoustic emission test a novel method was developed to determine the downward force necessary to produce threshold deflection of a bonded beam-lead die. The force was applied by a simple probe, and a 1-mW helium-neon laser with a focussed spot size of about 25 μm diameter was directed under the die at a low angle between two beam leads as shown in the diagram of figure 40. The laser beam is reflected back and forth between the substrate and the die and establishes a static interference pattern that can be seen extending outward from the edges of the die for an eighth to a quarter of a millimeter. Deflection of the die by only a fraction of a wavelength produces changes in the interference patterns that can be seen easily through a 30X binocular microscope, even though no motion of the die is discernible. The threshold motion of an individual unbonded beam can also be seen by this method. Although necessarily qualitative in nature, this technique may be useful in other types of visual inspection and should be a valuable aid in the observation of relative thermal expansion of components in hybrids as well as for studying creep phenomena. (G. G. Harman)

9.2. Wire Bond Pull Test

At the request of the Interconnection Bonding Section of ASTM Committee F-1 on Electronics, an experiment was conducted to investigate the effect of pull rate on the measured pull strength of single-level ultrasonic gold wire bonds. Gold wire of 99.99 percent purity, with a diameter of 0.001 in. (25 μm), elongation of 1 to 2 percent, and a breaking load of 12 gf (0.12 N), was ultrasonically bonded to an 800-nm thick aluminum film evaporated over a 700-nm thick silicon dioxide film thermally grown on a silicon slice. The aluminum film was photolithographically patterned into squares 0.005 in. (0.13 mm) on a side on 0.010 in. (0.25 mm) centers [84]. In an initial power series experiment [85] undertaken to establish a preferred bonding schedule, a standard flat bonding tool was used. A large variation was observed in both mean bond strength and standard deviation; this sug-
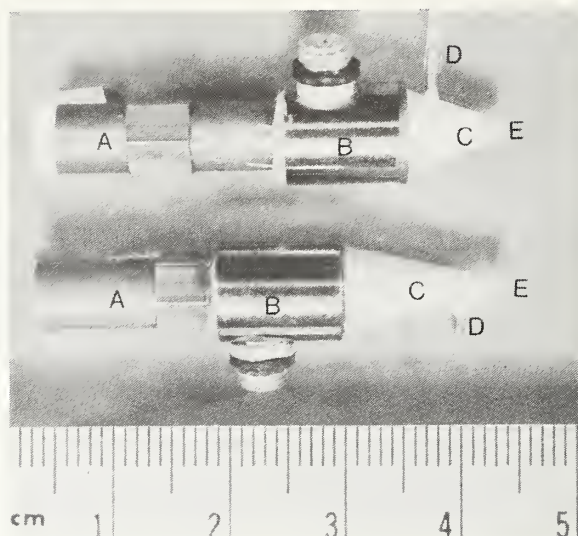
A Force gauge adapter
B Detector
C Acoustic waveguide
D Vacuum port
E Molded vacuum cup

Figure 36. Two acoustic emission detectors
with waveguide probes and die-vacuum cups.

a. Vacuum hold down.
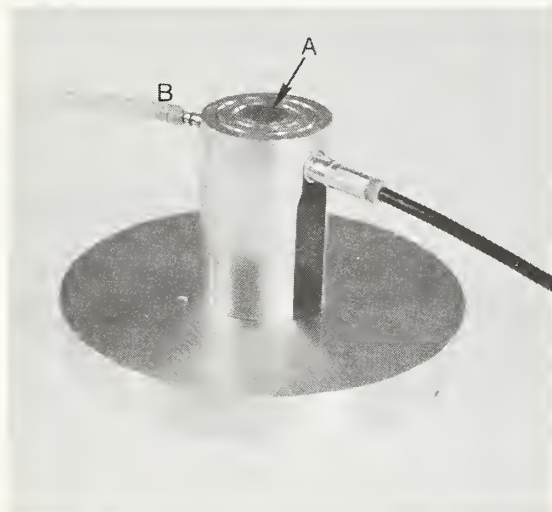
A Detector
B Vacuum line
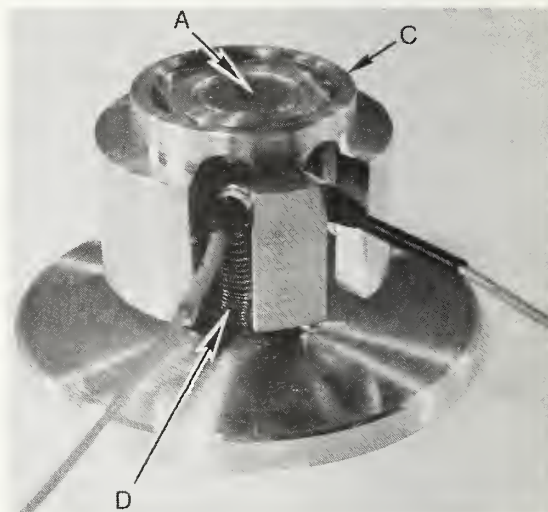
b. Mechanical hold down.

C Weight
D Spring

Figure 37. Substrate detector mounts

48
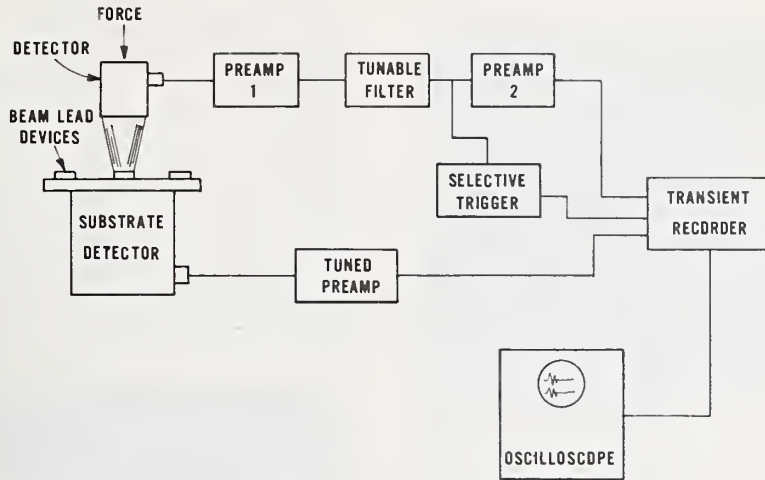
Figure 38. Schematic diagram of acoustic emission detection apparatus.
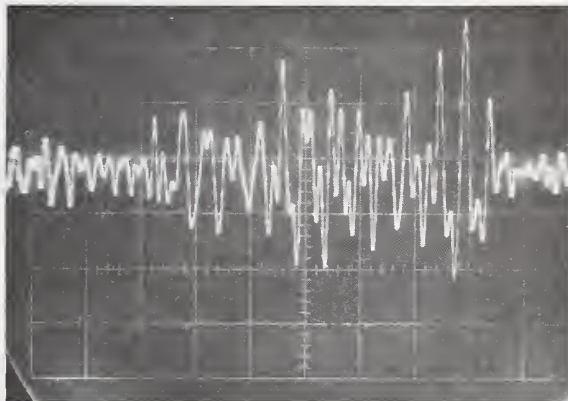
Figure 39. Combined substrate-die acoustic emission waveform from a device with a poorly bonded corner beam lead stressed to 6 gf (59 mN). (Probe tuned to 1 MHz; substrate detector tuned to 500 kHz. Horizontal scale: 0.1 μs/div; vertical scale: 2 V/div.)
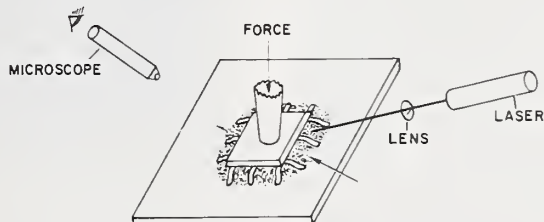
Figure 40. Illustration of use of static interference pattern to observe the threshold of mechanical movement. (The pattern is denoted by the arrow.)
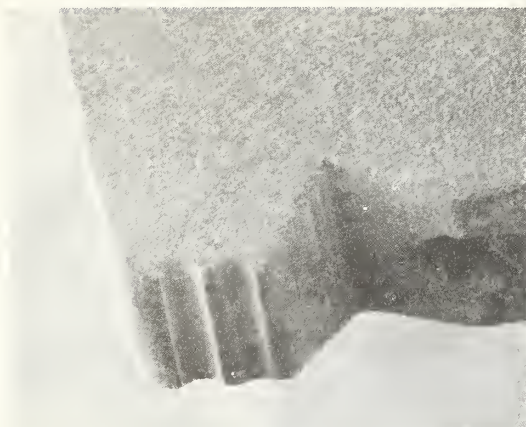
Figure 41. Scanning electron micrograph of a double-grooved, tungsten carbide tool for ultrasonic bonding. (Magnification: ∿150X.)

gested that the bonding tool was not transmitting the ultrasonic energy adequately to the wire-metallization interface.

To correct the situation a new polished tungsten carbide bonding tool with a foot length of 4.5 mil (114 μm) was modified by cutting two deep grooves to a depth of 20 to 25 μm as shown in the scanning electron micrograph in figure 41. A new power series experiment was carried out to establish a suitable bonding schedule for use with the modified grooved tool. A typical curve is shown in figure 42. Ten to fifteen single-level bond pairs were made at each power setting. In this case the bonding force was 30 gf (0.29 N) and the bonding time was 50 ms for both bonds. The tool tilt was 2 deg forward for the first bond and 2 deg backward for the second bond. The power setting was varied from 2 to 10 for the first bond and held at 5.5 for the second bond. The bond-to-bond spacing was 0.060 in. (1.52 mm) and the loop height was 0.015 in. (0.38 mm). All bond pairs broke or lifted off at the first bond. The mean bond pull strengths and standard deviations for integral first-bond power settings are shown in figure 42. The preferred first-bond power setting was 5; scanning electron micrographs of a typical bond pair made with these conditions are shown in figure 43.

These conditions, which yielded a mean pull strength of 10.5 gf (0.103 N) and a sample standard deviation of about 0.4 gf (0.004 N), were also used to fabricate the 800 bond pairs needed for the determination of measured pull strength as a function of pull rate. The pull rate was varied between about
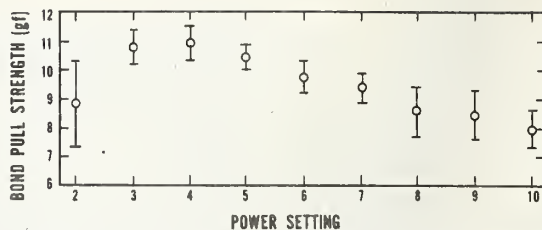
Figure 42. Bond pull strength as a function of first-bond power setting for ultrasonic bonds made with 25-μm diameter gold wire.
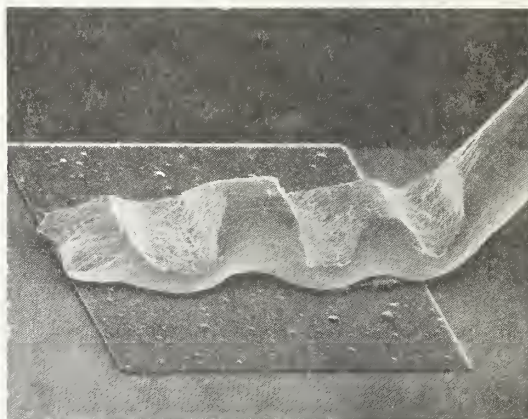
a. First bond. Magnification: ∿400X.
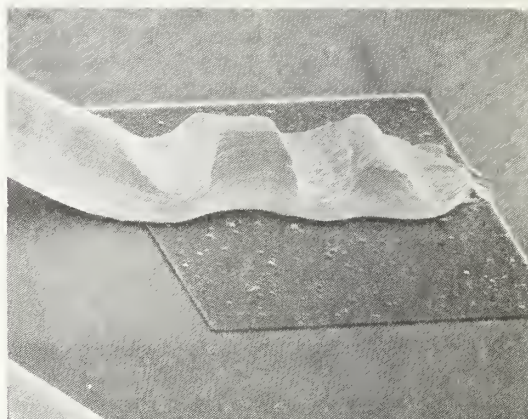
b. Second bond. Magnification: ∿400X.

Figure 43. Scanning electron micrographs of typical gold ultrasonic wire bonds made under preferred conditions with a double-grooved tool.
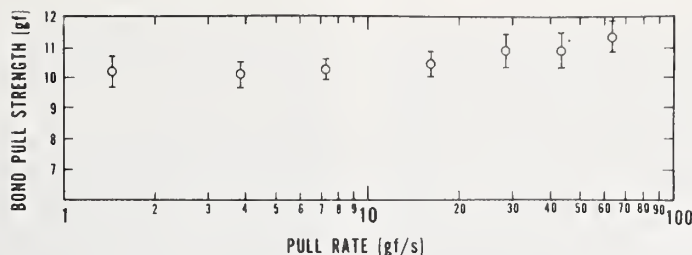
Figure 44. Bond pull strength as a function of pull rate for ultrasonic bonds made with 25-μm diameter gold wire under preferred conditions.

1.4 and 64 gf/s (0.014 to 0.63 N/s) and was controlled by a variable speed motor. At each of seven pull rates, 20 to 25 bonds were pulled to destruction. For pull rates lower than about 10 gf/s (0.098 N/s) the breaking force was recorded on an X-Y recorder (NBS Tech. Note 560, p. 37) but, because the recorder has a low (nominally 76 cm/s) slewing speed, the breaking force at more rapid pull rates was read directly from the gram gauge. The results, plotted in figure 44, show that the pull rate can vary over this range without a significant variation in measured pull force. The slight increase at higher pull rates is probably an artifact due to the inertia of the gram gauge.

Further investigation of the characteristics of the double deep-grooved bonding tool showed that a broad range of ultrasonic power can be used without appreciably increasing the bond deformation, which suggests that the bonding tool may stall after the bond is formed and the ultrasonic energy is no longer transmitted to the bonding interface.

(H. K. Kessler)

9.3. Bondability of Doped Aluminum Metallizations

A study was undertaken to evaluate the bondability of aluminum ribbon and round wire ultrasonically bonded to copper- and silicon-doped aluminum metallizations. Recently improvements have been reported relating to the addition of silicon to aluminum metallization to prevent interdiffusion [86] and the addition of copper to aluminum metallization to prevent electromigration [86,87].

A 900-nm thick film of aluminum-3.5% copper metallization was deposited on an oxidized silicon wafer by using an aluminum-12% copper mixture as the charge in a one-pot electron beam evaporation system. Films of aluminum-1% silicon and aluminum-1.5% silicon were obtained from commercial sources. The films were etched into square pads, 0.005 in (0.13 mm) on a side on 0.010 in. (0.25 mm) centers by conventional photolithographic techniques to form single-level substrates [84] for the bonding study.

Two types of wire were employed. Both were aluminum-1% silicon with 1 to 2 percent elongation and a breaking load of 12 to 14 gf (0.118 to 0.137 N). The ribbon wire had dimensions of 1.5 by 0.5 mil (35 by 13 μm) and the round wire had a diameter of 1.0 mil (25 μm) so that the cross sectional areas were essentially the same.

Power series [85] were carried out by varying the power dial setting for the first bond. All bonds were made with a bonding force of 25 gf (0.24 N) using a tungsten carbide tool with a foot length of 4.5 mil (114 μm). The power dial setting for the second bond was kept constant at 4.5. Bonding time for both the first and second bond was 50 ms. All bonds were pulled to destruction with a pull rate of 3.8 gf/s (0.037 N/s).

The results are presented in figure 45. For the case of aluminum metallization doped with 1 or 1.5% silicon the pull strength-power curves generally follow the shape obtained for pure aluminum metallization which suggests that both the ribbon and round wire can be bonded satisfactorily to these alloys. Although satisfactory bonds could be made to the copper-doped aluminum metallization, it was found that at high power (settings from 7 to 10) the variability was significantly larger than is usually obtained for bonding to pure aluminum. Also, for the round wire there was a sharp drop in pull strength at low power. For both copper- and silicon-doped aluminum metallization, the ribbon wire exhibited a higher pull strength than the round wire; this is consistent with previous results obtained on pure aluminum metallization [88].

(H. K. Kessler)
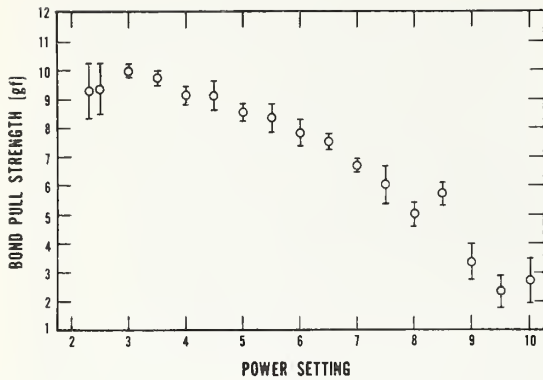
a. 1% silicon-doped aluminum metallization.
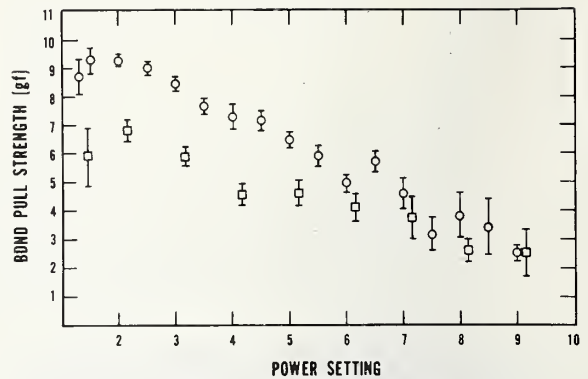
b. 1.5% silicon-doped aluminum metallization.
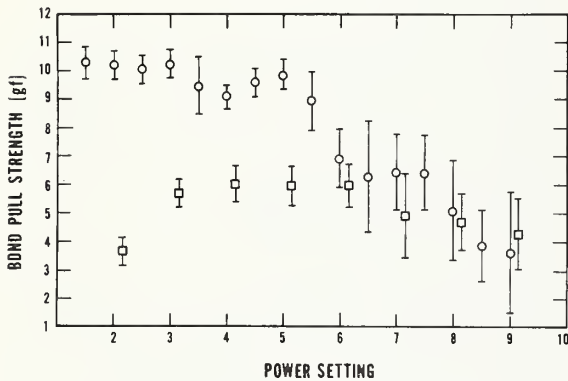
c. 3.5% copper-doped aluminum metallization.

Figure 45. Bond pull strength as a function of first-bond power setting for ultrasonic wire bonds made with aluminum-1% silicon wire. (O: 38- by 13-μm ribbon wire; □: 25-μm diameter round wire. The error bars represent one sample standard deviation of a group of 20 to 25 bonds.)

10. HERMETICITY

10.1. Gas Infusion into Double Hermetic Enclosures

In some applications, it is customary to incorporate hermetically sealed semiconductor devices and other components within an outer hermetic case. Intuitively, this would be expected to increase seal assurance. However, a detailed analysis of the gas flow equations suggests that a significant reduction of gas infusion occurs only under certain conditions.

Consider first the infusion of dry gas into the double enclosure depicted in figure 46. The outer case, which has an internal free volume of V_1, has been leak tested to a value of L_1 so that the leak size is L_1 or lower. Inside, there is a smaller package of internal free volume V_2 which had been leak tested to a value of L_2 before being placed in the outer case. Since the infusion of a noncondensable gas into semiconductor devices from a dry atmosphere appears to be primarily by free molecular flow for the leak range $< 1 \times 10^{-5}$ atm·cm^3/s, which is the range of interest in determining the fine leak reject limit, it is assumed that infusion through the leaks L_1 and L_2 is by free molecular flow.

Exact solutions of the flow equations have been obtained [89]. Pressure-time curves for a typical example are shown in figure 47 in terms of normalized variables. On the vertical axis the chamber pressure is normalized to the external driving pressure, P_b, and on the horizontal axis the time is normalized to the time constant of the inner volume which is given by $\tau_2 = P_0 V_2 / L_2$ where P_0 is atmospheric pressure. Curve 1 represents the case where the inner package has been exposed directly to the external gas; the pressure rises exponentially and reaches a value 63 percent of the external driving pressure at $t = \tau_2$. Curves 2 and 3 depict the pressure in the outer and inner packages, respectively, if the smaller package is surrounded with an outer case whose volume is 10 times that of the inner package but whose leak rate is identical. Note that for very small times the pressure rise is linear in time in the outer chamber but quadratic in time in the inner package. Thus, although pressure is much lower in the inner chamber at early time, it rises rapidly and reaches that of the outer chamber within a time less than $10\tau_2$. By comparing curves 3 and 1, one can determine the reduction in pressure obtained with a double enclosure as compared to the single package by itself.

A complete description of pressure reduction can be obtained from the exact solution by computing the pressure time characteristics for any desired situation. The long term behavior of the system can be quantified by considering as a merit factor the ratio of the pressure of the inner enclosure when isolated to that when enclosed at the time $t = \tau_2$. This allows one to represent the behavior of any combination of volumes and leak sizes by a single number. Further, examination of many characteristics shows that this merit factor also provides a rough approximation to the increase in time necessary for the gas concentration in the inner enclosure to rise to the same value as would exist in the single enclosure at $t = \tau_2$.

The merit factor is shown in figure 48 for a broad range of leak size ($\gamma = L_1/L_2$) and volume ($\delta = V_1/V_2$) ratios. It is seen that simply surrounding one hermetic enclosure by another is not assurance of hermetic improvement, although it is obviously a protection against a badly leaking inner enclosure. It is further seen that significant enhancement is only obtained if outer enclosure leakage is not greater than ten times inner leakage or the outer free volume is at least ten times that of the inner free volume. For vanishingly small outer free volumes, the effective leak rate approaches that of a single enclosure with leak conductances in shunt. The curves in this figure can also be used to establish the conditions where the use of a double enclosure can be expected to significantly reduce gas infusion and to determine the effects of leak testing sensitivity and precision on the assurance of seal quality [90].

The above analysis was made for a dry, noncondensable gas. While a package with the reasonably acceptable leak rate of 10^7 atm·cm^3/s has a time constant of the order of 1 day to 4 months, depending on its volume, the effective service life of typical devices is many times longer. This is probably because the infusion rate of water vapor, which has been identified as a principal source of device degradation, into microchannels is complicated by condensation, absorption, etc. Unfortunately, there is no good model to relate the time constant of a package for a well behaved gas to the service life. However, since moisture infusion is much slower than the infusion of a dry, noncondensable gas, one may infer that the ratios presented in figure 48 would also apply to the longer
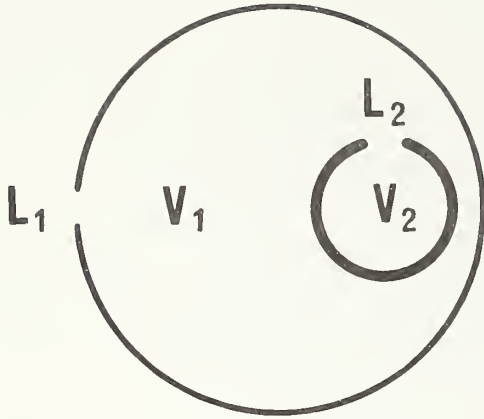
Figure 46. Schematic diagram of double hermetic enclosure.

Figure 47. Pressure-time curves for enclosures immersed in a gas of pressure P_b at time $t = 0$. (Curve 1: single enclosure of volume V_2 and leak size L_2; curve 2: outer enclosure of volume $V_1 = 10 V_2$ and leak size $L_1 = L_2$; curve 3: inner enclosure of volume V_2 and leak size L_2; $\tau_2 = P_0 V_2/L_2$.)
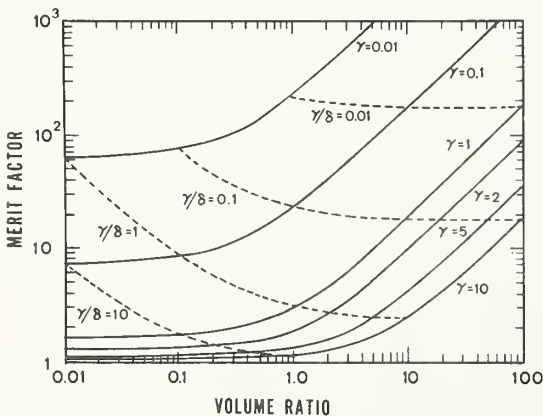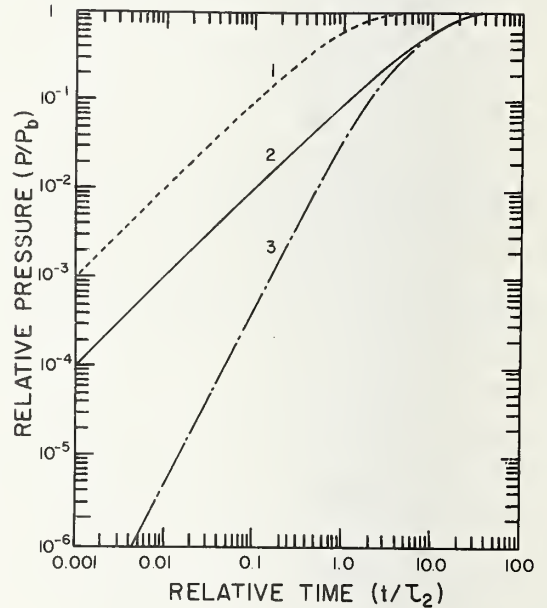
Figure 48. Merit factor for double hermetic enclosures for various values of leak size ratio ($\gamma = L_1/L_2$) and volume ratio ($\delta = V_1/V_2$).

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times associated with device life and provide a quick measure of the effectiveness of a double hermetic enclosure for different volume and leak size ratios.

(S. Ruthberg)

10.2. Static-Expansion, Differential-Pressure Gross Leak Test

The limiting factor in dry gas, gross leak test procedures is the rapid depletion of gas from the package interior which results in the nondetection of large leaks. The static-expansion, differential-pressure test has been suggested (NBS Spec. Publ. 400-4, p. 70, and 400-8, p. 42) as one method to circumvent the problem associated with long dwell time between pressurization and testing. The procedure employs gas expansions in two similar and parallel systems. A differential pressure measurement made after expansion provides a quantitative measure of the leak size.

The apparatus is shown schematically in figure 49; standard symbols [91] are used to indicate the components. The package to be tested is placed in the test chamber of volume v_1 which has internal dimensions just sufficient to contain the package.* A similar but solid artifact of the same external volume is placed in the parallel reference chamber of volume $V_1 = v_1$. Both chambers are pressurized to the desired value P_t, for the same time. After pressurization, the quantity of gas in the test and reference chambers is the same provided that there is no leak in the device under test. However, if the device leaks, the quantity of gas introduced into the test chamber is greater by the amount driven into the test device interior. The gas in the small volumes is then allowed to expand into the associated larger and previously evacuated identical chambers of volume v_2 and V_2. A difference in quantity of gas in the two volumes causes a meter indication. The use of a parallel reference chain eliminates the need for absolute measurement, minimizes the effects of adsorption and variation in valve closure, and allows a wide range of test object volumes and materials by adjustment of the tare, and the carrier where needed. Any test gas may be used.

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*Alternatively, the test specimen may be placed in a carrier with internal dimensions to fit the package and external dimensions to fill v_1.
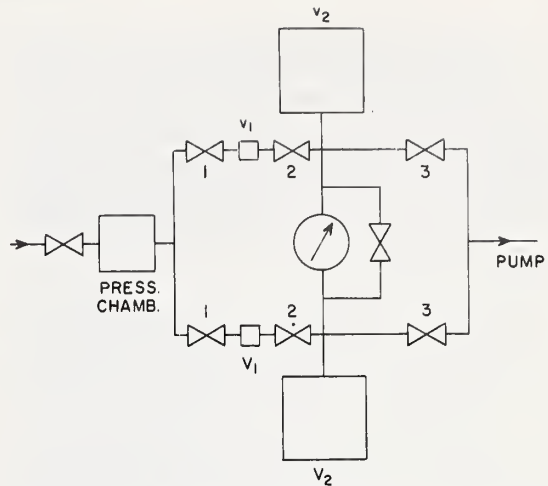
Figure 49. Schematic diagram of apparatus for static-expansion, differential-pressure gross leak test.

Exact solutions of the gas flow equations have been derived, based upon laminar viscous flow theory, which is appropriate for the gross leak range. If it is assumed that the temperature of the apparatus is uniform, that the time interval between pump isolation and expansion is small, and that the pressurization time is long enough that the pressure inside the device under test is equal to P_t, one finds that the initial rate of rise is given by

$$\frac{dp_2'}{dt} = \frac{P_t^2 L}{(v_0 + v_2) P_0^2} \frac{1}{(1 + \frac{P_t L}{v_i P_0^2} t)^2} , \qquad (12)$$

and that the steady state differential pressure is given by

$$\Delta p = P_t v_i / v_2 \qquad (13)$$

where L is the leak rate, v_0 is the difference between v_1 and the external volume of the package, v_i is the internal volume of the package, P_0 is atmospheric pressure, and the other symbols have been defined previously. Thus it can be seen that the rate of change of indication is a measure of the leak rate and the amplitude is a measure of the internal free volume of the package.

(S. Ruthberg)

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10.3. Correlation of Moisture Infusion, Leak Size, and Device Reliability

The first phase of the study to derive a quantitative relationship between leak size in hermetic packages and moisture infusion (NBS Spec. Publ. 400-19, pp. 52,54) was completed with analysis of the moisture sensor evaluation and refinement of procedures for microvent fabrication.

Two moisture sensors, one an interdigitated thick film finger structure and the other an electrode system between the die attach area and the package leads, were fabricated on each of 25 open ceramic, 14 pin, dual-in-line packages. To reduce extraneous leakage, all exposed surfaces except those associated with the sensors themselves were coated with epoxy.

To test the sensors, the package was mounted on a temperature controlled probe in an environmental chamber which was first stabilized in a dry mode and then set to give the desired relative humidity in the range from 5 to 50 percent; it was necessary to use high purity deionized water (7 to 10 $M\Omega \cdot cm$) to control the humidity in the chamber. The thermoprobe was stabilized at an initial reference temperature and then its temperature was reduced in small increments while the leakage current which resulted from an applied potential of 50 V was monitored. The dew point was detected by observation of the abrupt change in current as shown in the current-temperature characteristics of figure 50a [92]. The change in current is caused by conduction through the water condensed on the sensor surface. In an integrated circuit package the normal contamination is a complex electrolyte mixture of reasonably high conductivity. However, the moisture in the environmental chamber was much less conductive, and the observed currents were orders of magnitude lower than found typically in sealed packages which contain moisture. To establish the position of the dew point under these conditions it was required that three consecutive data points in the flat region have currents within 10 percent of each other and that the peak current be more than twice the average current in the flat region; the dew point was taken as the temperature at which the current was 120 percent of the average current in the flat region. Of the total of 80 test runs, dew points could be determined for 63.

Besides the problems of low currents, anomalies occurred in some cases because of moisture absorption by the epoxy which was used to coat the specimen and printed wiring board. The curve in figure 50b shows the appearance of the current temperature characteristic obtained in test runs that were affected by this phenomenon. These characteristics showed only a monotonic rise without a flat band. A few runs, in which the temperature range did not include the dew point resulted in a flat current-temperature characteristic as shown in figure 50c.

Analysis of the data indicated that there was no systematic error in the use of either dew point sensor but there was a random variation of about 5°C. Most of this variation appears to be related to the techniques required to combine a macro-environment and a micro-sensor: psychrometric error and gradients in the environmental chamber, the hydroscopic nature of the epoxy used to seal the printed wiring board, temperature differential between the thermoprobe and sensor, and perturbation of the air in the chamber by the radiating surfaces of the thermoprobe. Evaluation of procedures for calibrating and using the sensors are continuing.

A combination of laser drilling and various multiple electrochemical processes were used to fabricate 100 sample microvents. Both scanning electron microscope analysis and helium leak detector measurements were used to evaluate the fabrication procedures. Leak rates ranged from about 5×10^{-8} to over

a. Desired characteristic   b. Epoxy leakage.   c. No dew point in range.
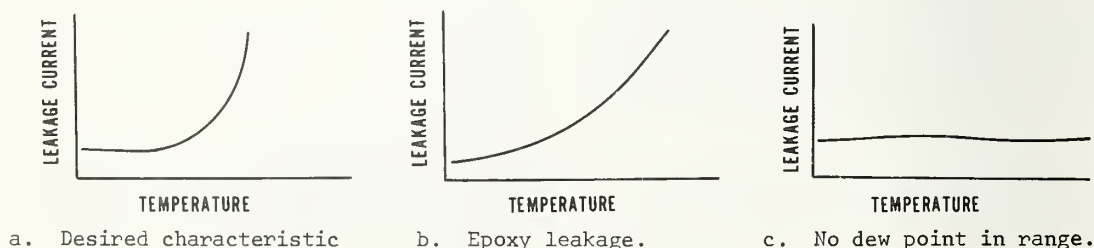
Figure 50. Leakage current-temperature characteristics for dew point sensors.

1×10^{-5} atm·cm^3/s. The lids were sealed to headers with a yield of 98 percent. The units with gross leaks were subjected to the weight gain test [93] while the remainder were measured by the radioisotope leak test [94]. A number of units were stored in 85 percent relative humidity at 85°C for 168 h and leak tested again. The test data indicated that the microvents were highly unstable under conditions of repeated leak test, because of distortion of the lids by the test pressurization. When stiffeners were added to the lids, satisfactory agreement was obtained between leak test results before and after exposure to 96 h storage in 85 percent relative humidity at 85°C. The microvent design has been modified to include integral stiffeners.

(S. Zatz[†] and S. Ruthberg)

11. DEVICE INSPECTION AND TEST

11.1. Dual-Laser, Flying-Spot Scanner

The photoresponse of the substrate diode of an integrated circuit was calibrated in terms of device temperature as an additional example of the usefulness of the electronic thermal mapping technique described previously (NBS Spec. Publ. 400-19, pp. 60-61) in connection with mapping the temperature distribution of a discrete UHF transistor. The integrated circuit studied was an array of five 750 mW silicon *npn* transistors on a common substrate with the substrate *p-n* junction located about 10 μm below the top surface. The relative photoresponse to low-power 1.15 μm laser irradiation of this junction was calibrated against temperature by mounting the device in a controlled-temperature heat sink and measuring the photocurrent at a constant reverse bias of 30 V over the temperature range from 35° to 150°C.

The results are compared in figure 51 with the results of a calculation based on published values [95] of the variation of the optical absorption with temperature. For the calculation it was assumed that all absorbed radiation produced hole-electron pairs that were collected at the junction; with this assumption the photoresponse exponentially increases with temperature at a rate of about 2.6%/°C. The departure of the datum points from the line at the higher temperatures can probably be attributed to the fact that other mechanisms must be taken into account. Even
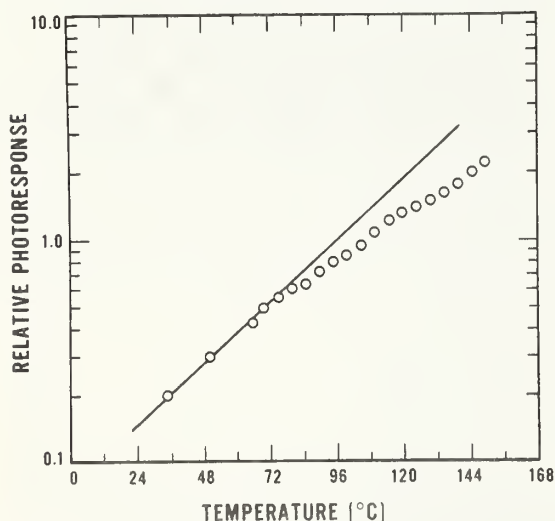
Figure 51. Photoresponse of substrate *p-n* junction as a function of temperature. (Solid line: calculated; circles: experimental.)

around 150°C the rate of increase is about 1.6%/°C which is large enough for the phenomenon to be a practical temperature indicator.
(D. E. Sawyer, D. W. Berning, H. P. Lanyon[*], J. D. Farina, and D. L. Blackburn)

11.2. Automated Scanning Low Energy Electron Probe

Initial investigations of wafer defects were begun by means of the automated scanning low energy electron probe (ASLEEP) (NBS Spec. Publ. 400-19, pp. 55-56) on a 2-1/2 in. (63 mm) diameter silicon wafer which contained process induced defects as indicated in the x-ray topograph[†] of figure 52. For ease of mounting in the ASLEEP system and to provide samples which could be subjected to different processing steps the wafer was divided into quarters.

The first quarter was given an HF dip to remove the oxide and placed in the ASLEEP system. Curved lines concentric with the circular edge of the slice were observed. These are suspected as being due to the polishing operation when the wafer was manufactured. Figure 53 is an ASLEEP photograph showing these features. The scale of the x-ray topograph is not large enough to determine unambiguously whether these lines appear or not. However, examination in other regions of the quarter showed faint lines which intersect at a 60 deg angle as expected for dislocations. The specimen charges readily and hence the faintness of the lines may be due to an oxide layer covering the specimen.

The second quarter was examined in an electron diffraction camera and was found to have a thick oxide coating. The oxide was stripped from the specimen and then it was cleaned using a spin cleaning process where deionized water and solvents are applied to the center of the spinning specimen and centrifugal force slings the contaminated material off the edge of the wafer. The specimen was returned to the electron diffraction camera and the surface was observed to be single crystal silicon. The specimen was then installed in the ASLEEP system. One of the first things observed was a series of concentric rings centered on the center of the quarter rather than the center of the slice.

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[*] Worcester Polytechnic Institute, Worcester, MA 01609.

[†] The wafer and topograph were kindly provided by Dr. G. H. Schwuttke of IBM.

Figure 52. X-ray topograph of a 63-mm diame-
ter silicon wafer containing process-induced
defects.

Figure 53. ASLEEP image of 2.5 by 2.5 mm ar-
ea of portion of silicon wafer showing polish-
ing damage.
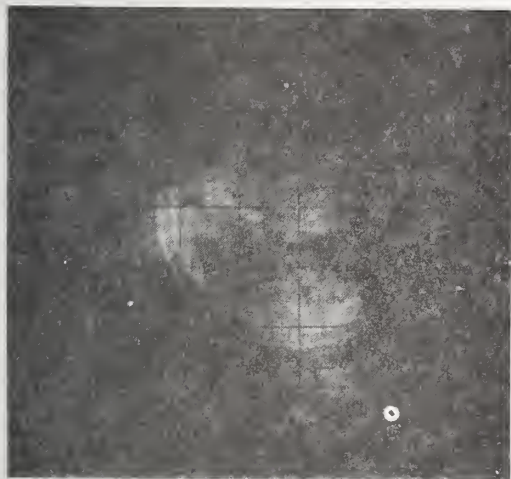
Figure 54. ASLEEP image of 6.3 by 6.3 mm ar-
ea of portion of silicon wafer showing damage
due to spin cleaning.
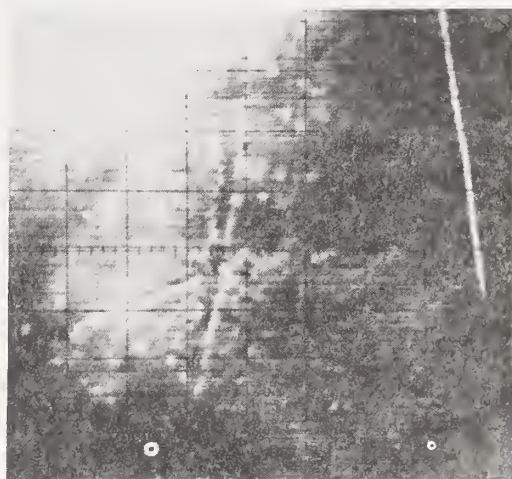
Figure 55. ASLEEP image of 2.5 by 2.5 mm ar-
ea of portion of silicon wafer showing appar-
ent dislocation lines.

Figure 54 shows this feature. It is felt
that these rings are due to surface damage
caused by the spin cleaning operation.

Further careful examination of this specimen
revealed extensive lines which intersect at
a 60 deg angle as expected for dislocations.
Figure 55 shows a group of these lines. A
mosaic of pictures has been assembled to map
these lines. Since ASLEEP examines a speci-
men at a much larger magnification than x-ray
topography correlation of specific defects
seen in ASLEEP with specific defects in the

x-ray topograph is difficult. However,
study in the scanning electron microscope
has indicated that the features seen in the
ASLEEP image may be dislocations of the same
type as are seen in the topograph.

(W. C. Jenkins[§])

11.3. Scanning Electron Microscopy - Voltage Contrast Mode

The cylindrical secondary electron detector (NBS Spec. Publs. 400-4, pp. 54, 56, and 400-8, p. 36) was installed in the specimen chamber of the scanning electron microscope and its response tested. To install the new detector it was necessary to move the standard Everhart-Thornley type detector to provide added space within the specimen chamber and to eliminate the possibility that the two detectors would come into contact. It was also necessary to replace the original single conductor leads to the detector with coaxial leads. An adapter providing nine coaxial feed-throughs was made to fit the specimen chamber airlock. The use of coaxial leads removed 60 Hz pickup almost entirely and reduced to some extent other components of noise.

For testing the response of the detector, a machined copper stub was used as the speci-

men. Various combinations of bias conditions were established on the detector and, for each, the collected current was measured as a function of specimen voltage. Figure 56 is a plot of the curves obtained for the four conditions listed in table 10. The shapes of curves such as B and C in the figure have been attributed [96] to the presence within the detector of tertiary electrons when secondary electrons strike the interior surfaces of the detector. These curves have the steepest slopes in the region about zero bias, $\sim$70 pA/V, so that a 1 mV change in specimen potential would result in a 0.07 pA (or 0.1 percent) shift in collector current.

When the copper stub was replaced by a silicon chip, 0.8 mm square, containing seven diffused resistors and associated bonding pads mounted on a TO-5 header, the results were disappointing. The collected current was very low and did not evidence significant change as the voltage was varied on the resistive patterns. These effects were due, at least in part, to the reduced size of the specimen and lower secondary emission of silicon as compared with copper. Several techniques were tried to improve the response including increased bias voltage on portions of the detector, a positive bias on the collector electrode, changes in accelerating voltage, and increased beam current. None gave the desired improvement; in fact, in many cases the noise level increased so as to completely mask any signal.

On the basis of this evaluation, it has been concluded that the spatial resolution of this detector, as it is presently constructed, is inadequate for examining integrated circuits. Further studies of this type of detector are not planned at the present time.

(W. J. Keery)
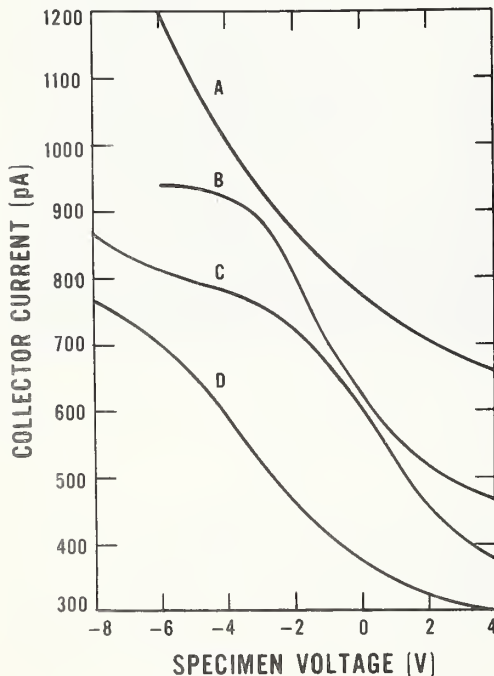
Figure 56. Output of cylindrical detector for various operating conditions as given in table 10.

Table 10. Detector Bias Conditions

Case	Bias Voltages, V		
	Top	Bottom	Insert
A	-10	-7.5	+150
B	-30	-6	+300
C	-5	-3	+200
D	-15	-15	+400

11.4. Scanning Acoustic Microscopy

New tasks have been initiated at Hughes Research Laboratories[¶] and Stanford University[#] to evaluate scanning acoustic microscopy as a technique for the inspection of semiconductor devices and integrated circuits. These tasks are building on prior work at Stanford University in which 2 μm resolution was demonstrated and various anticipated instrumental capabilities, including observation of subsurface defects, were discussed [97].

This early work was carried out with a microscope operating in the reflection mode, adapted from one designed for transmission microscopy. One of the purposes of the present tasks is to optimize the microscope in the reflection mode. In addition various other instrumental improvements are being developed.

The Stanford group is emphasizing the exploration of various techniques adapted from optical microscopy, such as dark field illumination and phase contrast methods. They are also seeking immersion media with less attenuation than water, which has more than 100 dB/mm transmission loss at 1 GHz.

The Hughes group is emphasizing the design and construction of an acoustic microscope instrument suited particularly for examination of solid-state device specimens. In addition, Hughes is studying the possibility of using anti-reflection lens coatings to reduce losses and spurious reflections, and the application of pulse techniques to simplify the microwave circuitry. Arrangements have been made to keep the two groups in communication with each other to permit early application of Stanford's findings in the Hughes prototype instrument.

(R. I. Scace)

12. THERMAL PROPERTIES OF DEVICES

12.1. Thermal Resistance — Power Transistors

It frequently seems to be convenient to make thermal resistance measurements under high-current, low-voltage conditions. There are several reasons such measurements may be misleading. First, these conditions result in the most uniform distribution of junction current and temperature, and therefore the thermal resistance would be expected to be lower than that encountered under other operating conditions such as those in which current crowding occurs. Second, for these conditions only a small percentage of the total allowed power is applied to the device and the subsequent rise in temperature may be quite small. This means that the accuracy of the measured thermal resistance is considerably less than one would expect for the case of a large rise in temperature.

In addition, some devices operate in a quasi-saturation mode [98] under these conditions. A study of a group of devices for which this is the case has shown that the electrical

switching transients which occur in quasi saturation do not permit accurate measurements of thermal resistance to be made using the EIA recommended standard [99]. The problems encountered are illustrated in figure 57, which shows the measured junction temperature, divided by the power dissipated in the device, plotted against the square root of the time after cessation of power for a transistor with collector current of 4 A and a range of values of collector-emitter voltage, V_{CE}. The device is operating in the quasi-saturation mode at 5 and 7.5 V and is just beginning to come out at 10 V. Note that for 5, 7.5, and 10 V there is almost no linear portion of the curve as would be predicted by one-dimensional cooling [100]; this lack indicates that non-thermal switching transients are present.

The reduced peak junction temperature at 5, 10, and 20 V as measured with an infrared microradiometer is also indicated in the figure at zero time. Because the electrical method is known to average the junction temperature, it should always indicate a temperature less than the peak temperature. Only at 20 V is this the case; at 5 V, the electrically measured apparent temperature is greater than the peak temperature even after the device has cooled for 250 μs. This arises because the non-thermal switching transients completely obscure the temperature dependence of the junction voltage. Thus, the possibility that a device may be operating in the quasi-saturation mode under high-current, low-voltage conditions further renders measurement of thermal resistance under these conditions undesirable.

(S. Rubin and D. L. Blackburn)

12.2. Thermal Resistance — Integrated Circuits

This task was undertaken to evaluate and compare the various measurement techniques commonly used for measuring thermal resistance of junction-isolated integrated circuits. In particular, the temperature indicated by the collector-substrate isolation junction [101] was compared with those indicated by the emitter-base junction of the power dissipating transistor [99] and by the infrared microradiometer. In addition, a very simple computer simulation was used to show that one dimensional transient heat flow theory accurately describes the cooling response
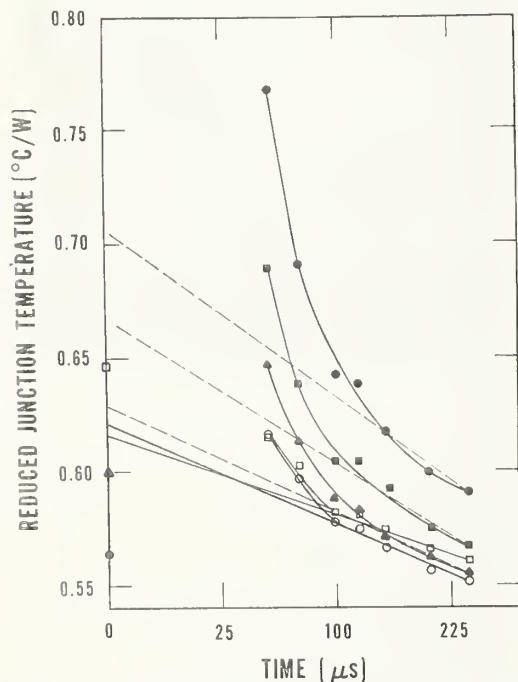

Figure 57. Cooling curves for a transistor operated with a collector current of 4 A and various emitter-collector voltages. (●: V_{CE} = 5 V; ■: V_{CE} = 7.5 V; ▲: V_{CE} = 10 V; ○: V_{CE} = 15 V; □: V_{CE} = 15 V; reduced temperatures as measured with infrared microradiometer are indicated at zero time.)

for short times for small heat sources located on the integrated circuit.

A computer program, based on the work of Joy and Schlig [102], was used to compute the peak temperature associated with square heat sources located on the surface of a semi-infinite plane. For short periods of time, this should accurately represent the heating or cooling of a single, small heat source (transistor) located on an integrated circuit chip. The cooling response was calculated for square heat sources, 0.05, 0.13, and 0.25 mm on a side. The results are given in figure 58 together with the cooling response associated with one-dimensional heat flow (which results in a square root of time dependence of the junction temperature). It can be seen that for heat sources 0.13 mm and larger on a side, the cooling response follows that of one-dimensional heat flow for at least short times longer than 3 μs, the earliest time after cessation of power that it is practical to make electrical measurements. Therefore it is possible to extrapolate the measured cooling response back to the time power is removed (t = 0) to find the steady-state temperature. This temperature cannot be measured electrically because of the presence of non-thermal switching transients. In addition it is possible to determine the area of the heat source from the slope of the cooling curve [100].

Measurements of thermal resistance were made on several bipolar integrated circuits. Most of the measurements were made on a simple array containing seven transistors, each in an isolation tub. Although arrays with other metallization patterns were also studied, the most versatile array was the one pictured in figure 59 in which five of the seven transistors are pinned out independently and could be connected together externally as desired; the sixteenth pin is connected to the substrate.

The cooling response for one of the transistors on this device, measured with a case temperature of 50°C and using the forward voltage of the emitter-base junction of the transistor as the temperature sensitive parameter (TSP) [99], is shown in figure 60. From the slope of the straight line, the area was estimated to be about 0.022 mm² which compares satisfactorily with the junction area of 0.018 mm² measured on the photomicrograph in figure 59. The extrapolated junction temperature was 142°C in close agreement with the value of 145°C measured with the infrared microradiometer. Thus, the one dimensional transient heat flow theory appears to explain
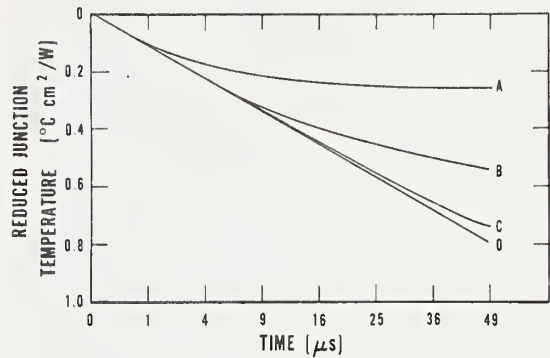
Figure 58. Computed cooling curves for square heat sources of various sizes located at the top surface of a semi-infinite plane. (A: side of square, 0.05 mm; B: side of square, 0.13 mm; C: side of square, 0.25 mm; D: one-dimensional heat flow.)
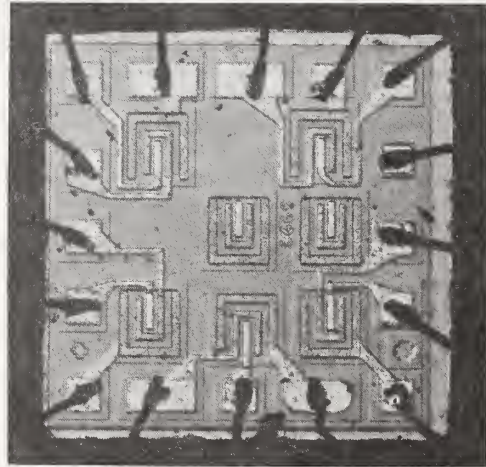
Figure 59. Photomicrograph of integrated transistor array with each transistor individually pinned out. (Magnification: ∿42X.)
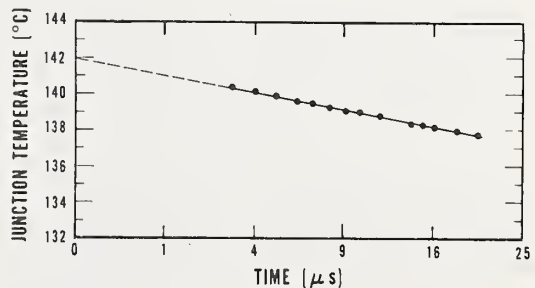
Figure 60. Cooling curve for typical individually pinned-out integrated circuit transistor for a case temperature of 50°C.

quite adequately the experimentally measured cooling response. The temperature determined by using the forward voltage of the collector-substrate isolation junction under the active transistor as the TSP was significantly lower, 126°C, and if the forward voltage of all the collector-substrate junctions connected together was used as the TSP [101], the measured temperature was still lower, 120°C.

In all cases when the measurement of temperature was made using the transistor that was also dissipating the power, the emitter-base junction indicated a significantly higher temperature than did the collector-substrate junction. When the temperature was sensed at a device remote from the heat source, both the emitter-base and the collector-substrate junctions indicated approximately the same temperature, but the value was very much lower than the peak temperature at the heat source. If some or all of the collector-substrate junctions were sensed in parallel, the indicated temperature was intermediate between the temperature indicated by the isolation junction in the vicinity of the heat source and the one measured by an isolation junction remote from the source.

One can conclude from these results that the forward voltage of the collector-substrate junction is not a satisfactory TSP for determining peak temperature of an integrated circuit. If the emitter-base junction of the heat generating element is accessible at the pins of the circuit, the peak temperature can be determined in the usual way [100]. In a complex circuit it may not be possible to access the appropriate junction directly. As an example, measurements were made on an integrated voltage regulator circuit in which the main power dissipating element was an output Darlington transistor pair, of which the base and emitter terminals were available for sensing. Since the recommended procedure [103] for measuring the thermal resistance of Darlingtons could not be used conveniently because the appropriate junctions were not accessible, an average of the temperatures of the input and output transistors was measured using the available terminals. Although this temperature is significantly lower than the peak temperature, it was 9°C higher than the temperature measured using the forward voltage of the collector-substrate isolation junction as the TSP.

The sensitivity of the forward voltage of the collector-substrate isolation junction as the TSP for the determination of the quality of the die attach of integrated circuits remains to be evaluated.

(J. D. Farina and D. L. Blackburn)

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SEMICONDUCTOR TECHNOLOGY PROGRAM STAFF

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SEMICONDUCTOR TECHNOLOGY PROGRAM PUBLICATIONS

B.1. Prior Reports

A review of the early work leading to this Program is given in Bullis, W. M., Measurement Methods for the Semiconductor Device Industry — A Review of NBS Activity, NBS Tech. Note 511 (December 1969).

Progress reports covering the period July 1, 1968, through June 30, 1973, were published as NBS Technical Notes with the title, Methods of Measurement for Semiconductor Materials, Process Control, and Devices:

Quarter Ending	NBS Tech. Note	Date Issued	NTIS Accession No.
September 30, 1968	472	December 1968	AD 681330
December 31, 1968	475	February 1969	AD 683808
March 31, 1969	488	July 1969	AD 692232
June 30, 1969	495	September 1969	AD 695820
September 30, 1969	520	March 1970	AD 702833
December 31, 1969	527	May 1970	AD 710906
March 31, 1970	555	September 1970	AD 718534
June 30, 1970	560	November 1970	AD 719976
September 30, 1970	571	April 1971	AD 723671
December 31, 1970	592	August 1971	AD 728611
March 31, 1971	598	October 1971	AD 732553
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September 30, 1971	717	April 1972	AD 740674
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March 31, 1972	733	September 1972	AD 748640
June 30, 1972	743	December 1972	AD 753642
September 30, 1972	754	March 1973	AD 757244
December 31, 1972	773	May 1973	AD 762840
March 31, 1973	788	August 1973	AD 766918
June 30, 1973	806	November 1973	AD 771018

After July 1, 1973, progress reports were issued in the NBS Special Publication 400 subseries with the title, Semiconductor Measurement Technology:

Quarter Ending	NBS Spec. Publ.	Date Issued	NTIS Accession No.
September 30, 1973	400-1	March 1974	AD 775919
December 31, 1973 March 31, 1974	400-4	November 1974	COM 74-51222
June 30, 1974	400-8	February 1975	AD/A 005669
September 30, 1974	400-12	May 1975	AD/A 011121
December 31, 1974	400-17	November 1975	AD/A 017523
March 31, 1975 June 30. 1975	400-19	April 1976	PB 251844

B.2. Current Publications

As various phases of the work are completed, publications are prepared to summarize the results or to describe the work in greater detail. Publications of this kind which have been issued recently are listed below:

Jerke, J. M., *Semiconductor Measurement Technology:* Optical and Dimensional-Measurement Problems with Photomasking in Microelectronics, NBS Spec. Publ. 400-20 (October 1975).

Lieberman, A. G., Problems in Using Surface Analysis Techniques for the Depth Profiling of Microelectronic Materials, *Technical Digest, 1975 International Electron Devices Meeting*, Washington, D.C., December 1-3, 1975, pp. 126-129 (IEEE Cat. No. 75-CH 1023 1ED).

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Pease, R. L., Galloway, K. F., and Stehlin, R. A., Radiation Damage to Integrated Injection Logic Cells, *IEEE Trans. Nucl. Sci.* NS-22, 2600-2604 (1975).

Schafft, H. A., Ed., *Semiconductor Measurement Technology*: ARPA/NBS Workshop III. Test Patterns for Integrated Circuits, NBS Spec. Publ. 400-15 (January 1976).

Albers, J. H., Ed., *Semiconductor Measurement Technology*: The Destructive Bond Pull Test, NBS Spec. Publ. 400-18 (February 1976).

Sawyer, D. E., and Berning, D. W., *Semiconductor Measurement Technology*: Laser Scanning of Active Semiconductor Devices - Videotape Script, NBS Spec. Publ. 400-27 (February 1976).

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Kenney, J. M., *Semiconductor Measurement Technology*: Permanent Damage Effects of Nuclear Radiation on the X-Band Performance of Silicon Schottky-Barrier Microwave Mixer Diodes, NBS Spec. Publ. 400-7 (April 1976).

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Buehler, M. G., *Semiconductor Measurement Technology*: Microelectronic Test Pattern NBS-3 for Evaluating the Resistivity-Dopant Density Relationship of Silicon, NBS Spec. Publ. 400-22 (May 1976).

B.3. Availability of Publications

In most cases reprints of articles in technical journals may be obtained on request to the author. NBS Technical Notes and Special Publications are available from the Superintendent of Documents, U.S. Government Printing Office, Washington, D. C. 20402, or the National Technical Information Service, Springfield, Virginia 22161, or both.

Current information regarding availability of all publications issued by the Program is provided in the latest edition of NBS List of Publications No. 72 which can be obtained on request to Mrs. E. C. Cohen, Room A327, Technology Building, National Bureau of Standards, Washington, D. C. 20234.

B.4. Videotapes

Color videotape cassette presentations on improvements in semiconductor measurement technology are being prepared for the purpose of more effectively disseminating the results of the work to the semiconductor industry. These videotapes are available for distribution on loan without charge on request to Mrs. E. C. Cohen, Room A327, Technology Building, National Bureau of Standards, Washington, D. C. 20234. Copies of these videotapes· may be made and retained by requestors. Two videotapes, Defects in PN Junctions and MOS Capacitors Observed Using Thermally Stimulated Current and Capacitance Measurements, by M. G. Buehler and Laser Scanning of Active Semiconductor Devices, by D. E. Sawyer and D. W. Berning have been completed and released for distribution. As an added feature, arrangements can be made for the authors to be available for a telephone conference call to answer questions and provide more de-tailed information, following a prearranged showing of either of the videotapes.

APPENDIX C

WORKSHOP AND SYMPOSIUM SCHEDULE

C.1. Proceedings or Reports of Past Events:

Symposium on Silicon Device Processing, Gaithersburg, Maryland, June 2-3, 1970. (Cosponsored by ASTM Committee F-1 and NBS). Proceedings: NBS Spec. Publ. 337 (November 1970).

ARPA/NBS Workshop I. Measurement Problems in Integrated Circuit Processing and Assembly, Palo Alto, California, September 7, 1973. Report: NBS Spec. Publ. 400-3 (January 1974).

ARPA/NBS Workshop II. Hermeticity Testing for Integrated Circuits, Gaithersburg, Maryland, March 29, 1974. Report: NBS Spec. Publ. 400-9 (December 1974).

Spreading Resistance Symposium, Gaithersburg, Maryland, June 13-14, 1974. (Co-sponsored by ASTM Committee F-1 and NBS). Proceedings: NBS Spec. Publ. 400-10 (December 1974).

ARPA/NBS Workshop III. Test Patterns, Scottsdale, Arizona, September 6, 1974. Report: NBS Spec. Publ. 400-15 (January 1976).

ARPA/NBS Workshop IV. Surface Analysis for Silicon Devices, Gaithersburg, Maryland, April 23-24, 1975. Proceedings: NBS Spec. Publ. 400-23 (March 1976).

NBS/FDA Workshop. Reliability Technology for Cardiac Pacemakers, Gaithersburg, Maryland, July 28-29, 1975. Report: NBS Spec. Publ. 400-28 (June 1976).

Reliability Technology for Cardiac Pacemakers, II, Gaithersburg, Maryland, July 19-20, 1976. Report: in preparation.

STANDARDS COMMITTEE ACTIVITIES

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M. G. Buehler, Chairman, Task Force on Test Patterns, Process Controls Section; Semiconductor Crystals, Semiconductor Processing Materials, Semiconductor Measurements, and Quality and Hardness Assurance Subcommittees

*W. M. Bullis, Secretary; Editor, Semiconductor Crystals Subcommittee

J. R. Ehrstein, Chairman, Resistivity Section; Semiconductor Crystals, Semiconductor Processing Materials, Semiconductor Measurements, and Quality and Hardness Assurance Subcommittees

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G. G. Harman, Secretary, Interconnection Bonding Section; Hybrid Microelectronics, and Packaging Subcommittees

K. O. Leedy, Chairman, Packaging Subcommittee; Chairman, Interconnection Bonding Section; Semiconductor Crystals, Semiconductor Processing Materials, Semiconductor Measurements, Hybrid Microelectronics, and Quality and Hardness Assurance Subcommittees

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ASTM Committee E-10 on Radioisotopes and Radiation Effects

W. M. Bullis, Subcommittee 7, Radiation Effects on Electronic Materials

J. C. French, Subcommittee 7, Radiation Effects on Electronic Materials

R. I. Scace, Subcommittee 7, Radiation Effects on Electronic Materials

---

*All subcommittees.

Electronic Industries Association: Solid State Products Division, Joint Electron Device
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    D. L. Blackburn, Task Group JC-25-5 on Thermal Characterization on Power Transistors,
        and Committee JC-25 on Power Transistors

    F. F. Oettinger, Chairman, Task Group JC-25-5 on Thermal Characterization on Power
        Transistors, Committee JC-25 on Power Transistors; Technical Advisor, Thermal
        Properties of Devices, Committees JC-13.1 on Government Liaison for Discrete
        Semiconductor Devices, and JC-22 on Rectifier Diodes and Thyristors

    S. Rubin, Chairman, Council Task Group on Galvanomagnetic Devices

    D. E. Sawyer, Task Group JC-24-5 on Transistor Scattering Parameter Measurement
        Standard, Committee JC-24 on Low Power Transistors

    H. A. Schafft, Technical Advisor, Second Breakdown and Related Specifications
        Committee JC-25 on Power Transistors

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    F. F. Oettinger, Standards Committee Task Force on Second Breakdown Measurement
        Standards

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Technical services in areas of competence are provided to other NBS activities and other government agencies as they are requested. Usually these are short-term, specialized services that cannot be obtained through normal commercial channels. Such services provided during this and the previous reporting period, which are listed below, indicate the kinds of technology available to the program.

E.1. Semiconductor Device Fabrication (J. Krawczyk)

MOS capacitors with gates transparent to ultraviolet radiation were fabricated for the Harry Diamond Laboratories.

E.2. Oxidation (Y. M. Liu and J. Krawczyk)

Silicon wafers were oxidized for the NBS Polymers Division for ellipsometer studies.

E.3. Metal Evaporation (J. Krawczyk)

Aluminum films of various thickness were vacuum evaporated in two stages on several quartz substrates. These were for use in metal-vacuum-metal tunneling experiments for the NBS Mechanics Division.

E.4. Scanning Electron Microscopy (W. J. Keery)

Samples of gypsum wall board which had been exposed to fire damage were examined for the Fire Safety Engineering Division.

A portion of a lunar sample was examined with Dr. P. Bell of Carnegie Institute.

Several samples of glass plates coated with an optically transparent tin oxide film were examined for the NBS Optics and Micrometrology Section. These samples were to be substrates for photomask line width standards. The coatings were poor and the SEM was crucial in diagnosing the causes and developing modifications to the procedures to be used by the coating supplier.

E.5. Semiconductor Evaluation (W. R. Thurber)

Several crystals of high-resistivity silicon were evaluated for Eglin Air Force Base.

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	14. Sponsoring Agency Code

15. SUPPLEMENTARY NOTES

16. ABSTRACT *(A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.)*

This progress report describes NBS activities directed toward the development of methods of measurement for semiconductor materials, process control, and devices. Both in-house and contract efforts are included. The emphasis is on silicon device technologies. Principal accomplishments during this reporting period included (1) preliminary results of a systematic study of the effects of surface preparation on spreading resistance measurements; (2) development of an optical test for surface quality of sapphire; (3) development of a basis for an exposure sensitivity specification for photoresists; and (4) development of a modular cell concept for test structure design and layout. Also reported are the results of work on four-probe resistivity measurements, comparison of techniques for surface analysis, ion microprobe mass analysis, analysis of process chemicals with flame emission spectrometry, redistribution profiles, thermally stimulated current response of interface states, bias-temperature stress test measurements on MOS capacitors, a high voltage capacitance-voltage method for measuring characteristics of thick insulator films, hydrogen chloride oxidation, ion implantation parameters, methods for determining integrity of passivation overcoats, measurement of free sodium in an oxidation furnace by resonance fluorescence, a square array collector resistor test structure, an electrical alignment test structure, two dimensional wafer maps, test pattern design and analysis for silicon-on-sapphire MOS device technologies, a nondestructive acoustic emission test for beam-lead bonds, wire bond pull test, bondability of doped aluminum metallizations, leakage into double hermetic enclosures, a static expansion dry gas gross leak test, correlation of moisture infusion in semiconductor packages with leak size and device reliability, an automated scanning low-energy electron probe, an optical flying-spot scanner, scanning electron microscopy, scanning acoustic microscopy, and thermal resistance measurements on power transistors and simple integrated circuits. Supplementary data concerning staff, publications, workshops and symposia, standards committee activities, and technical services are also included as appendices.

17. KEY WORDS *(six to twelve entries; alphabetical order; capitalize only the first letter of the first key word unless a proper name; separated by semicolons)*
Acoustic emission; Auger electron spectroscopy; beam-lead bonds; bias-temperature stress test; boron redistribution; capacitance-voltage methods; dopant profiles; electrical properties; electronics; four-probe method; hermeticity; interface states; ion implantation; ion microprobe mass analysis; leak tests; measurement methods; microelectronics; moisture infusion; optical flying-spot scanner; passivation overcoats; photoresist; pull test; resistivity; scanning acoustic microscope; scanning electron microscope; scanning low energy electron probe; semiconductor devices; semiconductor materials; semiconductor process control; silicon; silicon dioxide; silicon on sapphire; spreading resistance; test patterns; thermal resistance; thermally stimulated current; ultrasonic wire bonding; voltage contrast mode; X-ray photoelectron spectroscopy.

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