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U.S. DEPARTMENT OF COMMERCE / National Bureau of Standards

Semiconductor Measurement Technology:

Planar Test Structures for Characterizing Impurities in Silicon

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PREFACE

This was presented as an invited paper by M. G. Buehler at the Large-Scale Integration (LSI) Process Technology/Semiconductor Preparation and Characterization Session of the Electrochemical Society Meeting in Toronto, Canada on May 14, 1975. An abstract was published in Extended Abstracts, The Electrochemical Society, Vol. 75-1, 403-404 (1975).

The work was conducted as part of the Semiconductor Technology Program at the National Bureau of Standards. Portions of this work were supported by the Defense Nuclear Agency (IACRO 75-816), Advanced Research Projects Agency (Order No. 2397), U.S. Navy Strategic Systems Project Office (IPR SP-75-4), and the NBS.

In the semiconductor industry it is common practice to design photomasks in English units. The photomasks used in this study were laid out in English units. The equivalent metric unit is given in parentheses and in some cases rounded off to an appropriate number of significant figures.

PLANAR TEST STRUCTURES FOR CHARACTERIZING IMPURITIES IN SILICON

by

M. G. Buehler, J. M. David, R. L. Mattis, W. E. Phillips, and W. R. Thurber

Abstract: Various test structures such as sheet resistors, *p-n* junctions, and MOS capacitors and their associated physical models have been developed to characterize dopants and defects in silicon. These structures address various needs within the semiconductor industry for (a) well-designed and miniaturized test structures such as an orthogonal van der Pauw sheet resistor, (b) simple and economical measurements such as the oxide window width of a diffused layer, (c) updated values for the resistivity versus dopant density relation, and (d) improved detection methods for identifying defect centers which control the lifetime and leakage currents of devices.

Key Words: MOS capacitors; *p-n* junctions; resistivity of silicon; semiconductor devices; semiconductor process control; sheet resistors; test patterns; thermally stimulated currents.

1. INTRODUCTION

The kinds of planar test structures discussed here consist of sheet resistors, *p-n* junctions, and MOS capacitors. These structures were used to determine the sheet resistance of diffused layers, the dopant density and resistivity of bulk collector regions, and the identity of defect centers such as gold.

The discussion of diffused layers involves the intercomparison, design, and over-etch of sheet resistors. Simple and economical sheet resistance measurements are shown to lead to values for the width of diffused layers.

For device design, it is essential to have a correct resistivity versus dopant density relation, and various structures were designed to update this relation in both *n*- and *p*-type silicon. Dopant density values were obtained from gated diodes and MOS capacitors, and resistivity values were obtained from collector four-probe resistors fabricated on wafers with a variety of resistivities. The measured values were combined into a resistivity versus dopant density plot and compared with existing relations. For *p*-type silicon the traditionally used Irvin curve [1] differs significantly from the more recent Wagner curve [2] which also differs from our experimental data.

The important device characteristics, lifetime and leakage current, are degraded by defect centers such as gold. This defect center was studied in *n*-type MOS capacitors and in both p^+n and n^+p junctions. From thermally stimulated current measurements, the current response is very different for gold doped p^+n as compared with n^+p junctions. But the responses of gold doped *n*-type MOS capacitors and gold doped p^+n junctions are essentially the same. These thermally stimulated current responses can lead to rapid identification of gold contamination in silicon devices.

The thrust of this work emphasizes well-designed and miniaturized test structures and the development of the associated mathematical models. Once developed, these test structures could become part of a process control test pattern. The test structures used in this study are included in test pattern NBS-3 [3]. This pattern, which is shown in figure 1, was designed primarily for use in the

evaluation of the resistivity versus dopant density relation. The overall size of the pattern is 200 mil (5.08 mm) on a side, and it is repeated every 200 mil (5.08 mm) over a wafer. The pattern contains diodes, transistors, MOS capacitors sheet resistors, contact resistors, etch-control structures, and a surface profilometer structure. The large blank area is intended for Hall effect measurements once the wafer is scribed and broken into chips. The structures discussed in the following sections are the large base-collector gated diode (3.10),* the small base-collector gated diode (3.14), the collector MOS capacitor (3.8), the collector four-probe resistor (3.17), and a variety of sheet resistors (3.11, 3.22, 3.28, and 3.30).

2. DIFFUSED LAYER SHEET RESISTANCE

Four sheet resistors in each of the patterns across a wafer were measured and the results displayed in figure 2. Sheet resistance values obtained from the van der Pauw [4] structures (3.11, 3.22, and 3.30) are comparable, which is expected since sheet resistances determined from symmetrical van der Pauw structures are independent of geometry. Values obtained from the bridge structure are low because, in the computation of the sheet resistance, the width was assumed to be the same as the photomask dimension, W(mask) = 1.50 mil (38.1 μm).

This point was explored further by combining sheet resistance measurements from the bridge (3.28) and van der Pauw (3.22) structures which are depicted in figure 3. The effective width of the bridge structure is given by

$$W_e = W(\text{mask}) + \alpha X_j + W_{oe}$$

where αX_j accounts for lateral diffusion and W_{oe} accounts for lateral over-etch. The van der Pauw measurement yields the sheet resistance directly. This was combined with the nearest-neighbor bridge measurement to obtain W_e. The base-diffusion-window width, W, was calculated from $W = W_e - \alpha X_j$. Values for W are shown in figure 4 as a function of position across a wafer for three different etch times. For these measurements αX_j = 0.02 mil (0.5 μm) where α = 0.3 [5]. The width of the bridge structure was also determined from photomicrographs, and the results, shown as solid data points, are in good agreement with the values derived from electrical measurements. The effective width, W_e, of the bridge structure for the 3 min etch equals the window width, W = 1.57 mil (39.9 μm), plus αX_j or 1.59 mil (40.4 μm). This value is 6 percent larger than the photomask dimension, W mask). The difference between W_e and W(mask) is important in the design of diffused integrated circuit resistors. Also apparent in figure 4 is the fact that electrical measurements can resolve dimensions smaller than 10 μin (0.25 μm). In addition these electrical dimensional measurements are inexpensive, especially when acquired by automatic probing machines. These measurements are discussed more fully elsewhere [6].

The orthogonal van der Pauw structure (3.22) shown in figure 3 is depicted in greater detail in figure 5. A mathematical model was developed for this structure to determine if a geometrical correction factor is needed in calculating the sheet resistance from the van der Pauw formula. The Laplace equation was solved with the use of finite-difference methods for the geometry shown in the lower part of figure 5 where the bonding pad areas were replaced by shorts on the ends of the arms. For this structure the measured sheet resistance differs from the van der Pauw value by less than 0.1 percent as indicated in figure 6. Here R_s(TRUE) is the true sheet resistance and R_s(VDP) is the sheet resistance determined from measurements with the use of the van der Pauw formula, which appears at the top of figure 6. The curves shown in figure 6 reveal that the side arms may be surprisingly short and wide compared to the active region without requiring as much as one percent correction to the van der Pauw formula. The active region is considered to be a square whose side is S. This study also allows the design of new structures whose active

*The number following the decimal point refers to a structure shown in figure 3; the number 3 is the test pattern designation.

regions are typical of device geometries. For example, the cross structure (D/S = A/S = 1) has a small error and can be fabricated with the use of minimum line width.

3. BULK DOPANT DENSITY

Dopant densities were determined in the collector (or bulk) region of a base-collector diode with the use of the junction C-V method [7]. As shown in figure 7, the diode (3.10) is gated and contains an inversion stop (labeled emitter). The dopant profiles for the gated diode are shown in figure 8 where incorrect profiles appear if the gate bias is improper. The proper gate bias is -5.5 V which corresponds to the flat-band condition for an equivalent MOS capacitor structure. This allows the peripheral junction capacitance to be approximated by a quarter toroid. The diode used in this study was 17 mil (430 μm) in diameter. Profiles can also be obtained with the use of a smaller diode (3.14) such as shown in figure 9 where again the base contact is confined within the base diffusion. This allows the measurement of correct capacitance values. An intercomparison of profiles for large and small diodes is shown in figure 10 where the peripheral correction brings the profiles of both diodes into agreement.

Dopant densities were also determined in the collector region of a collector MOS capacitor (3.8) as depicted in figure 11 with the use of the MOS capacitor C-V deep depletion method [8]. A dopant profile shown in figure 12 indicates the presence of phosphorus pile-up at the surface. The dopant density derived with the use of the MOS capacitor C_{max}-C_{min} method [9] is indicated as 1.04×10^{16} cm^{-3}. This value is considerably different from the bulk value of 6.28×10^{15} cm^{-3}.

The resistivity of bulk collector regions was determined [10] with the use of the collector four-probe resistor (3.17) shown in figure 13 where current points are denoted I_1 and I_2 and voltage points are denoted V_1 and V_2. The structure is essentially a piped-transistor where the emitter is connected to the collector through a hole in the base. The base, which surrounds the structure, effectively shuts off surface currents forcing currents to flow in the collector region. The probe spacing is 2.25 mil (57 μm) which is small compared to the wafer thickness [$\sim$ 10 mil (25 μm)] so that back-side shorting effects are negligible.

The resistivity versus dopant density relation is depicted in figure 14 for *n*-type silicon in terms of the normalized difference between the Irvin curve and the Caughey-Thomas [11] closed-form formula. It is seen that the Caughey-Thomas formula fits the Irvin curve to within $\pm$6 percent over the dopant density range from 10^{14} to 10^{20} cm^{-3}. Experimental data, which were determined by the above described methods, were compared to the Caughey-Thomas relation as shown in figure 15. If one ignores the high MOS capacitor values, where experimental difficulties were experienced, the data are within $\pm$6 percent of the Caughey-Thomas relation.

For *p*-type silicon the situation is much less satisfactory. The nature of the resistivity versus dopant density problem is shown in figure 16 for the case of *p*-type silicon. The traditionally used curve is that developed by Irvin [1]. More recently Wagner [2] developed another curve to fit ion implantation data. In the range of dopant densities between 10^{17} and 10^{18} cm^{-3}, these curves differ in resistivity by more than 50 percent. The data points represent experimental results based on junction C-V, Hall effect, and four-probe measurements taken in conjunction with the American Society for Testing and Materials (ASTM), Committee F-1 on Electronics. These data tend to follow the Wagner curve. The impact of the different curves shown in figure 16 on device design is shown in figure 17 where the surface density for a Gaussian diffusion is calculated from a knowledge of the background density, the sheet resistance, and the junction depth. It is seen that the surface density near 10^{18} cm^{-3} differs by a factor of two depending on the choice of the resistivity versus dopant den-

sity relation. The data of figure 16 are replotted in figure 18 to point up the need for additional work in p-type silicon. Even though the data agree better with the Wagner curve than with the Caughey-Thomas closed-form formula of the Irvin curve, significant discrepancies are observed.

4. DEFECT CENTERS

Defect centers, which cause lifetime and leakage current degradation in devices, were measured by the same kind of structures used to determine dopant density profiles. These structures (3.8 and 3.10) are shown in figures 7 and 11, and the class of measurements used to detect the defects is the thermally stimulated current measurements. This measurement method [12] is outlined in figure 19 where the upper curve indicates that a diode is cooled to near liquid nitrogen (LN_2) temperature and then warmed back to room temperature (RT). While the diode is at liquid nitrogen temperature the middle curve indicates that the diode is zero biased which charges defects with majority carriers (electrons for n-type or holes for p-type). Reverse bias is applied before the diode is warmed up. The lower curve indicates that during the warm-up cycle, certain defects emit majority carriers which are detected as a current pulse before the diode goes into steady-state leakage.

The thermally stimulated current response of various defect centers is shown in the following figures. In figure 20 the gold donor current peak [13] occurs near 130 K. The exact peak temperature depends on the heating rate. The gold acceptor current peak [14] occurs near 220 K as shown in figure 21. This response is quite different from the gold donor response. As indicated by the rapid rise in the current at higher temperatures, the gold acceptor center is the source of junction leakage. The response of the gold acceptor shown in figure 21 was observed in a p^+n junction. A similar response [14] was observed in an n-type MOS capacitor as shown in figure 22. In addition to the peak at 220 K a second peak occurs near 290 K. This higher temperature peak occurs as the MOS capacitor depletion region changes from its deep depletion width to its steady-state inversion width. From a theoretical model of the thermally stimulated current, the shape of the gold acceptor response depends on the fraction, G, of the depletion region over which defects are charged. This is illustrated in figure 23 where for G = 1 all defects in the depletion region are initially charged and for G = 0 none of the defects are charged.

5. CONCLUSIONS

As part of a project to provide the semiconductor industry with well-designed and miniaturized structures for use in process control, various test structures and associated measurement methods were studied. Measurements of large and small van der Pauw structures and gated diode structures were shown to yield the same result. The geometrical design criterion for the orthogonal van der Pauw structure was established. Combination of electrical measurements from bridge and van der Pauw structures yields values for the base-diffusion-window width with high spatial resolution.

The resistivity-dopant density relation for silicon is being up-dated for use in device design. Initial preliminary results suggest that for n-type the Caughey-Thomas formula and for p-type the Wagner formula appear to be the best available in the current literature.

Simple test structures can be used to detect and identify lifetime and leakage centers. The thermally stimulated current response of gold in silicon leads to its rapid identification as a contaminant in p-n junctions and MOS capacitors.

6. ACKNOWLEDGEMENTS

The authors are indebted to R. Y. Koyama for establishing the MOS capacitor C-V deep depletion method and for the data appearing in figure 12, and to W. M. Bullis for a critical reading of the manuscript.

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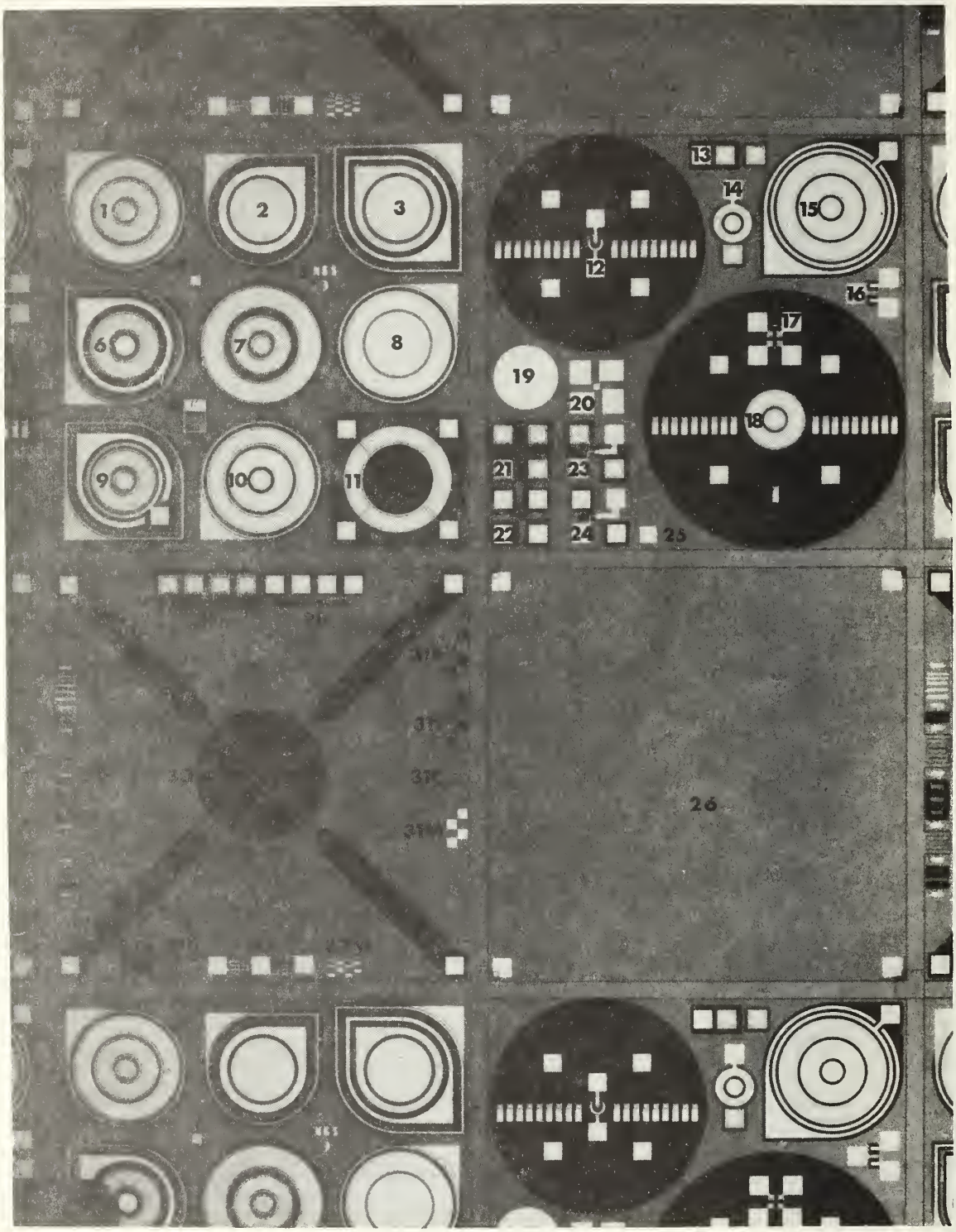
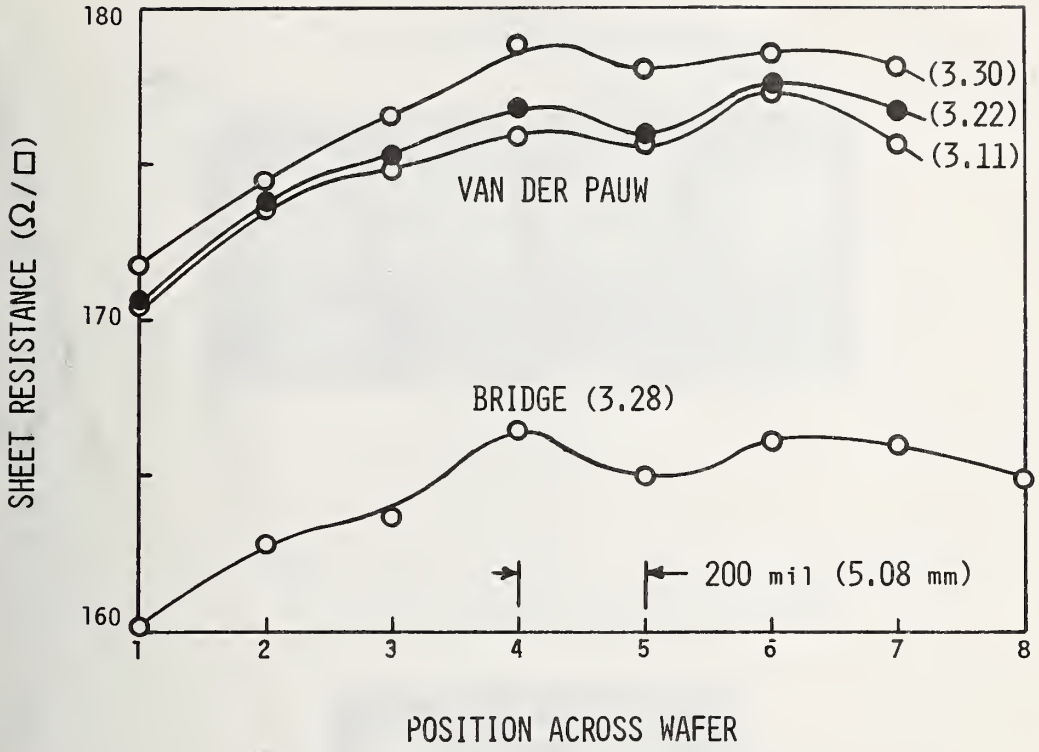


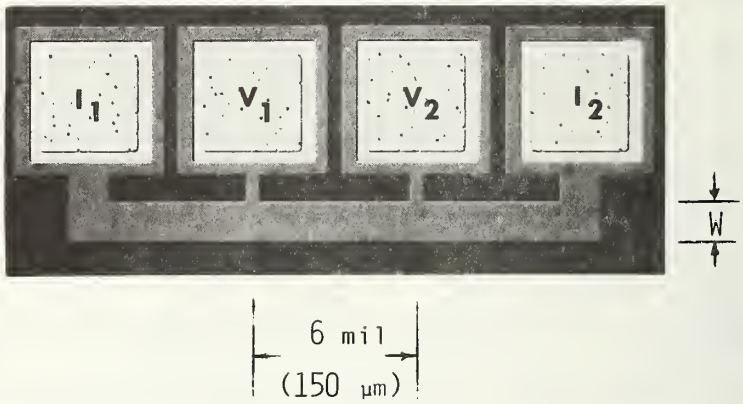
Figure 1. Test pattern NBS-3 [3] fabricated with base (B), emitter (E), contact (C), and metal (M) masks. The length of the pattern along one side is 200 mil (5.08 mm).



NUMBER	STRUCTURE	DIMENSION
3.11	VAN DER PAUW (GATED)	12 mil (300 μm)
3.22	VAN DER PAUW	1.5 mil (38 μm)
3.30	VAN DER PAUW	30 mil (760 μm)
3.28	BRIDGE	1.5 mil (38 μm)

Figure 2. Base sheet resistance values across a silicon wafer for both the bridge and van der Pauw structures. The dimension refers to the active portion of the structures; diameters are indicated for 3.11 and 3.30, the length of the side of a square is indicated for 3.22, and the width of the bridge structure is given for 3.28.

BRIDGE SHEET RESISTOR (3.28)



VAN DER PAUW SHEET RESISTOR (3.22)

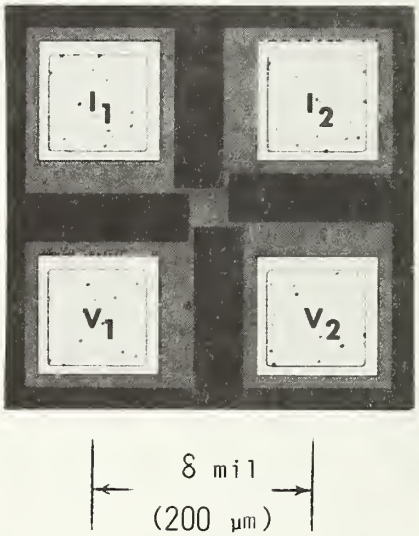


Figure 3. Base bridge and van der Pauw sheet resistor structures. The center-to-center metal pad spacings are indicated. The voltage points are denoted V_1 and V_2, and the current points are denoted I_1 and I_2. The van der Pauw structure was laid out with orthogonal boundaries to aid automatic pattern generation.

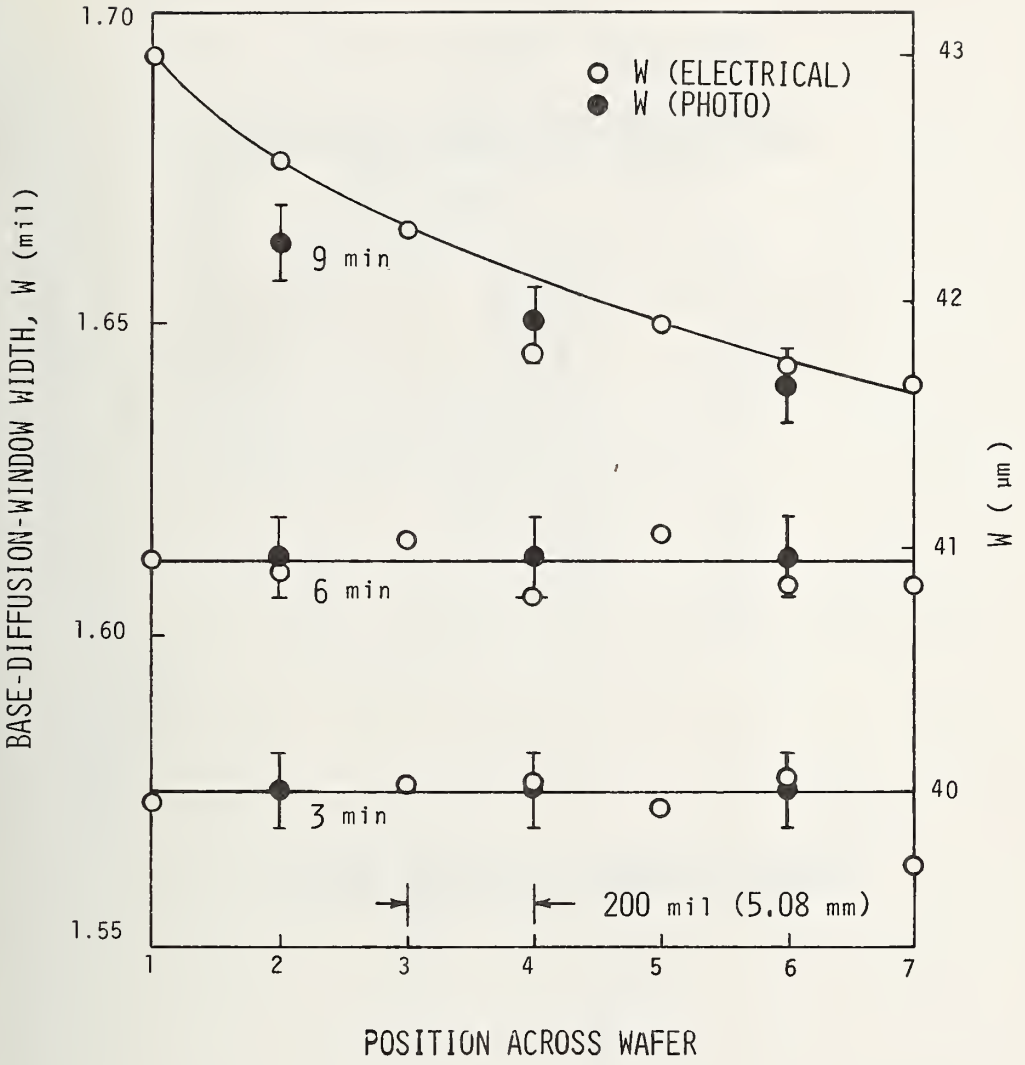
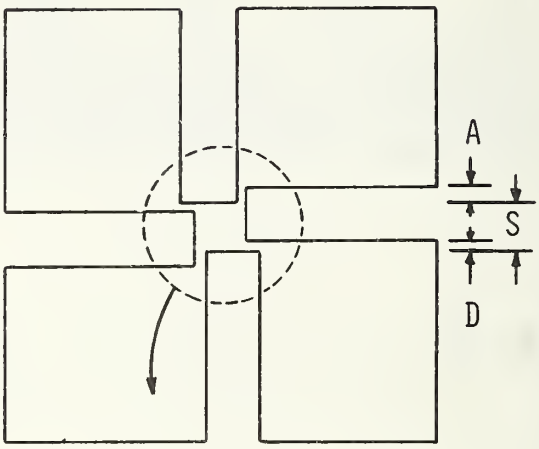


Figure 4. Base-diffusion-window width across three silicon wafers etched for three, six, and nine minutes and measured by electrical and photographic methods.

VAN DER PAUW SHEET RESISTOR (3.22)



MATHEMATICAL MODEL EQUIVALENT GEOMETRY

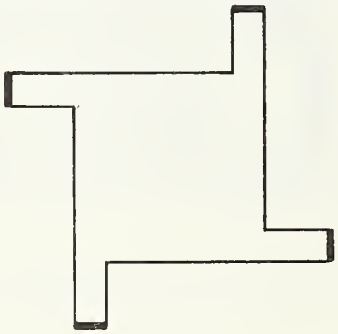


Figure 5. The orthogonal van der Pauw sheet resistor structure and its mathematical equivalent geometry. The dimension S = 1.5 mil (38 μm), A/S = 1/3, and D/S = 1/6.

Figure 6. Influence of geometrical factors on the orthogonal van der Pauw sheet resistance measurement as determined by a theoretical calculation. In the van der Pauw formula, $R_s(VDP)$, ΔV is $V_1 - V_2$ for a current I passed into I_1 and out of I_2 as shown in the van der Pauw structure of figure 3.

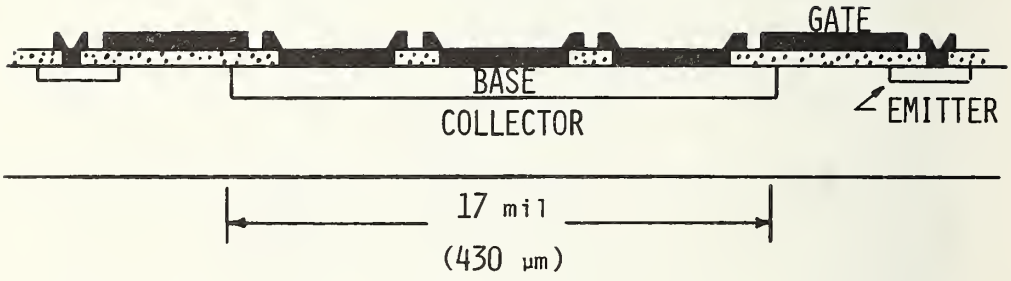


Figure 7. Cross sectional view of the large base-collector diode (3.10).

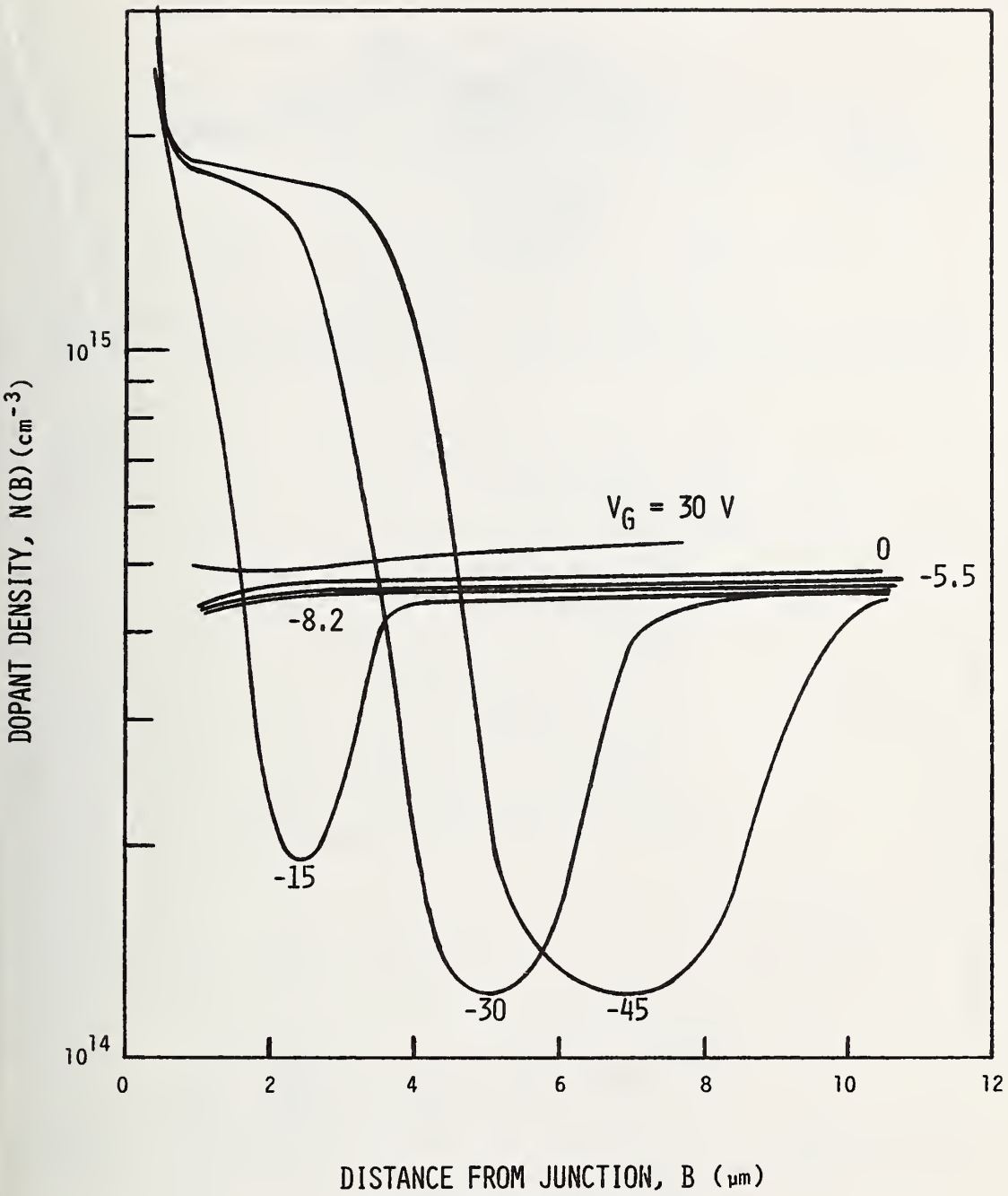


Figure 8. Junction C-V apparent dopant profiles taken with the use of the gated diode (3.10) shown in figure 7 biased with various gate voltages, V_G.

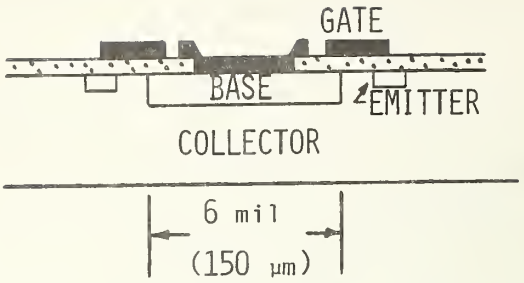


Figure 9. Cross sectional view of the small base-collector gated diode (3.14).

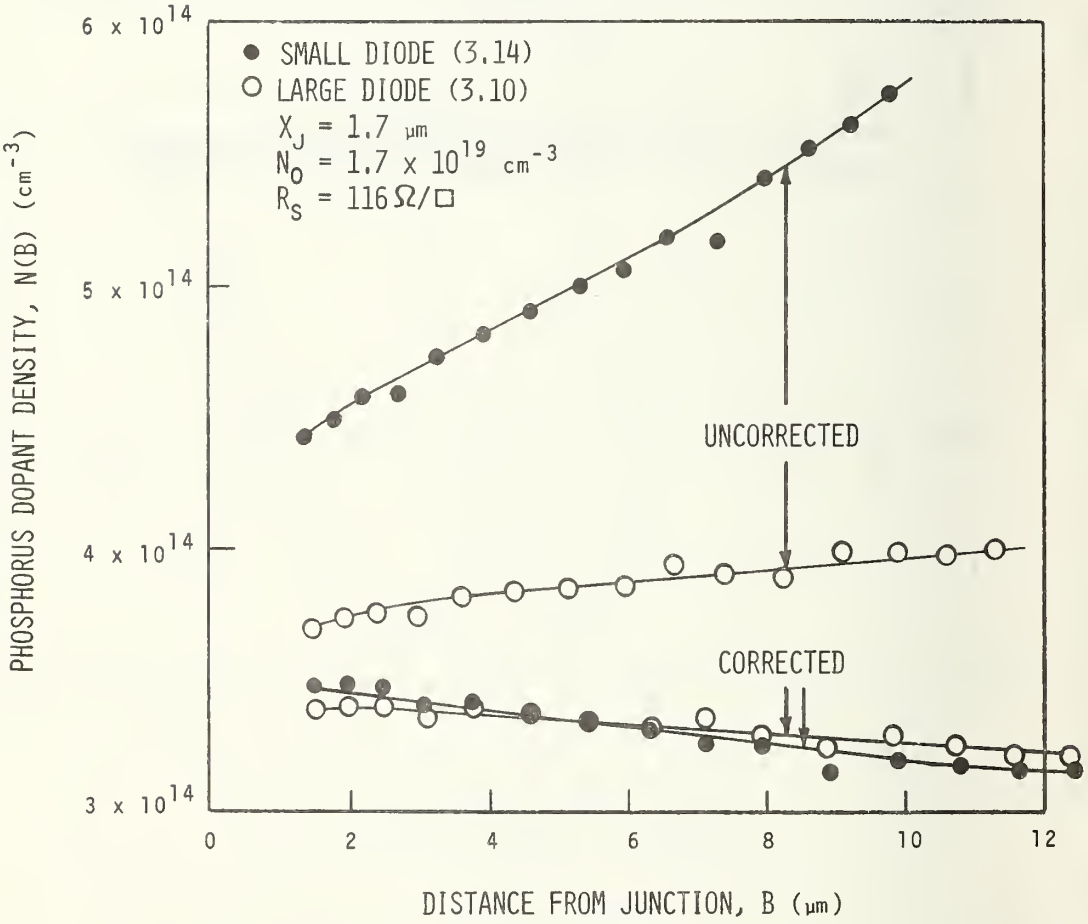


Figure 10. Junction C-V dopant profiles taken with the large and small base-collector gated diodes shown in figures 7 and 9. The corrected profiles illustrate the importance of the peripheral capacitance correction (wafer B12Ph-1).

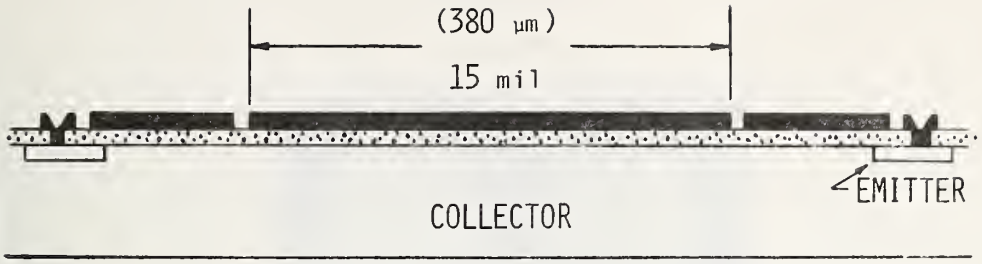


Figure 11. Cross sectional view of the collector MOS capacitor (3.8).

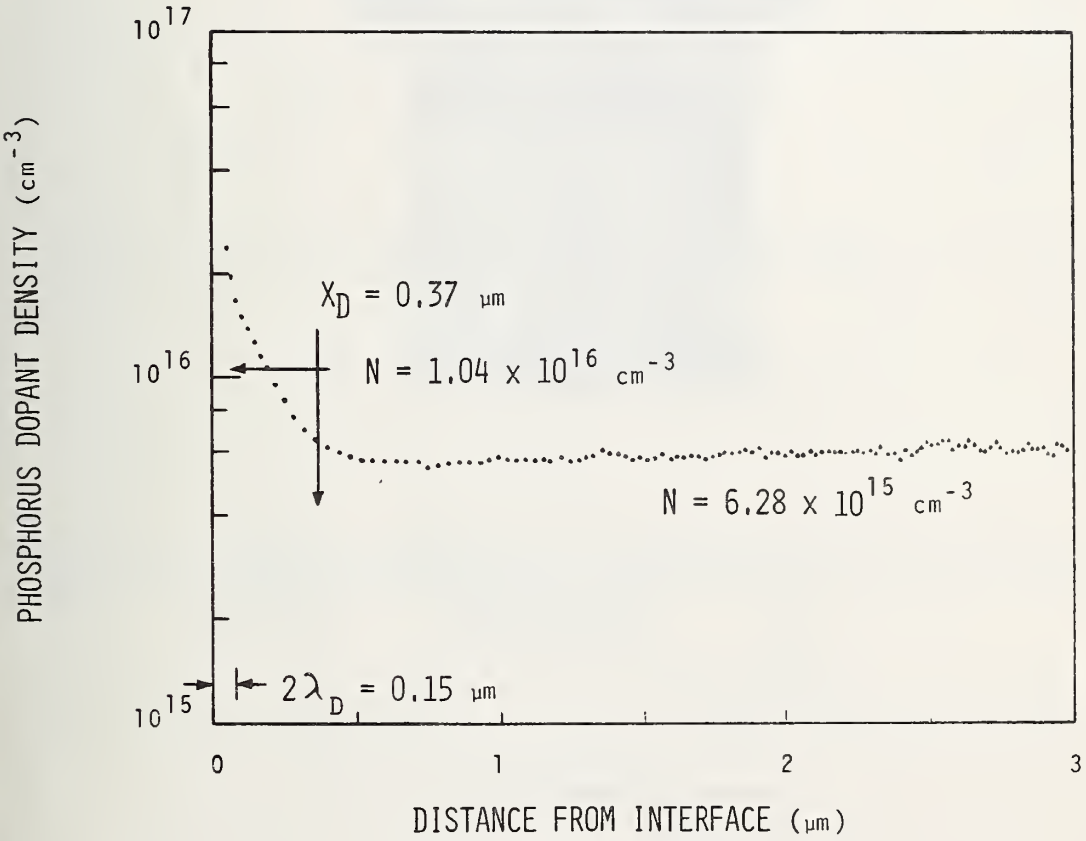


Figure 12. MOS capacitor C-V dopant profile taken with the use of the collector MOS capacitor (3.8) shown in figure 11 (wafer 702). The depletion depth in the silicon for the inversion condition is X_D, and the Debye length is λ_D.

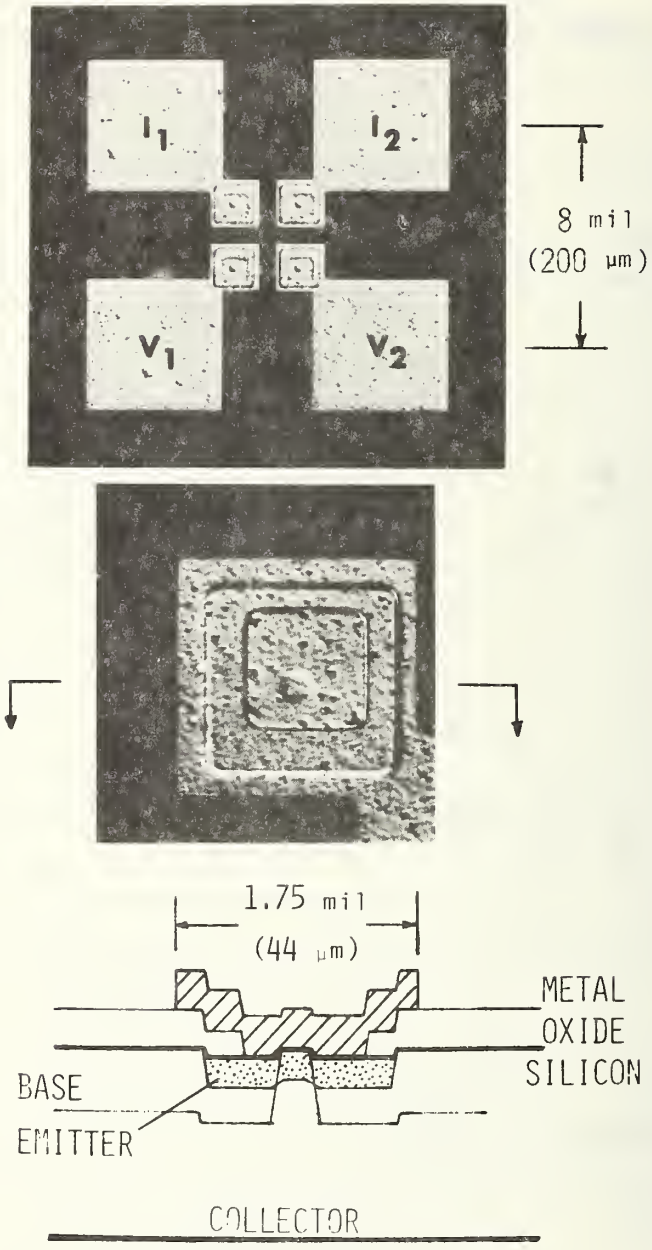


Figure 13. Top view and cross sectional views of the collector four-probe resistor (3.17). The center-to-center metal pad spacing is indicated on the upper photomicrograph.

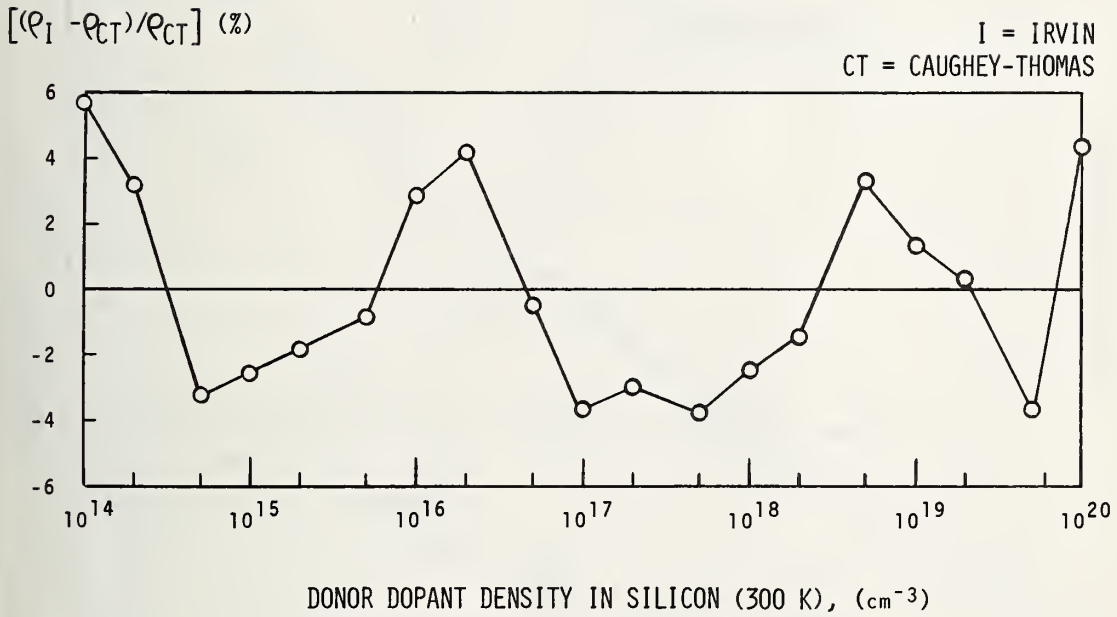


Figure 14. Normalized resistivity difference versus dopant density for *n*-type silicon (300 K) which compares the work of Irvin [1] and Caughey-Thomas [11].

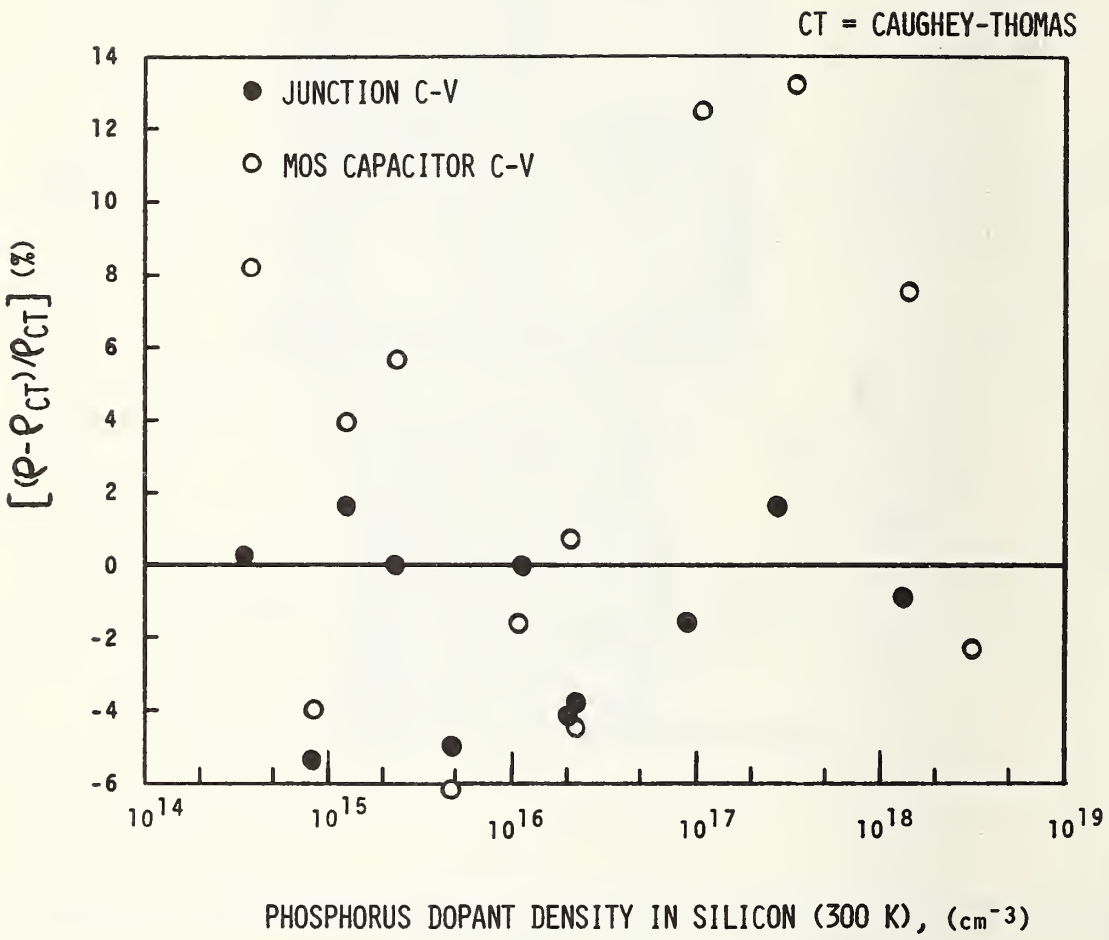


Figure 15. Normalized resistivity difference versus dopant density for *n*-type silicon (300 K) which compares experimental data determined by NBS to the Caughey-Thomas [11] formula.

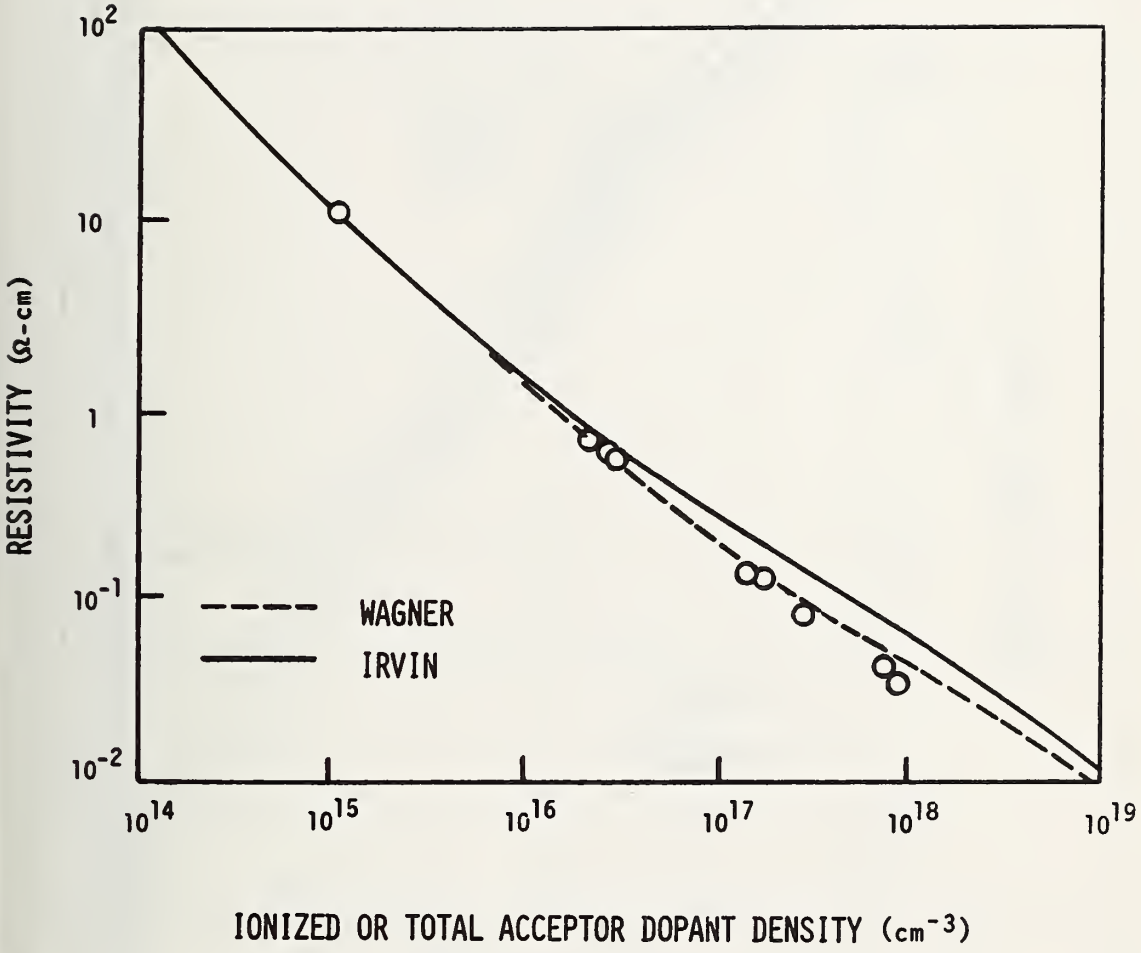


Figure 16. Resistivity versus dopant density relation for p-type silicon (300 K). The curves are taken from the work of Irvin [1] and Wagner [2]. The data points are explained in the text.

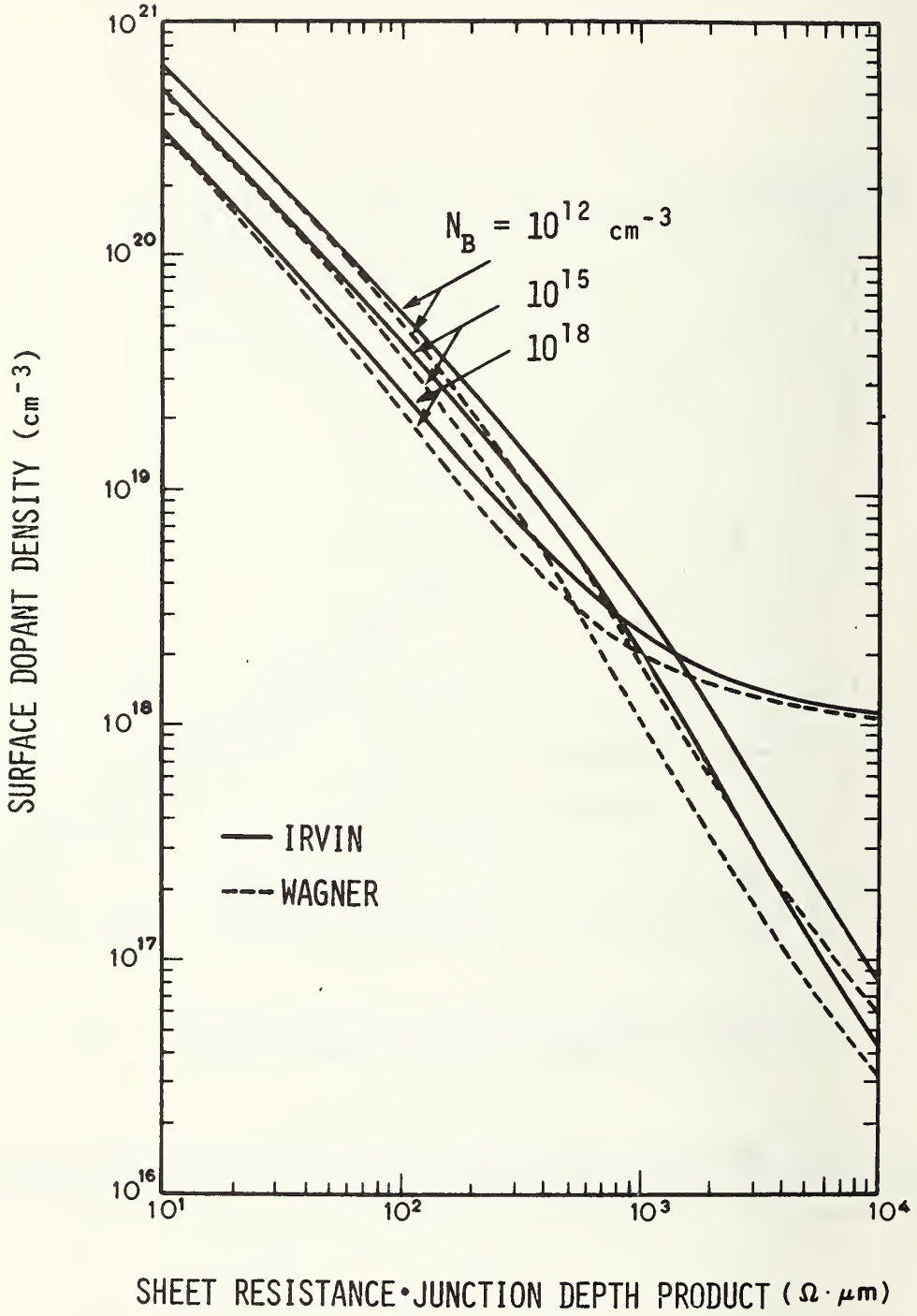


Figure 17. Surface dopant density of a *p*-type Gaussian diffused layer in uniformly doped *n*-type silicon as a function of the product of the sheet resistance (300 K) and junction depth for various background dopant densities, N_B.

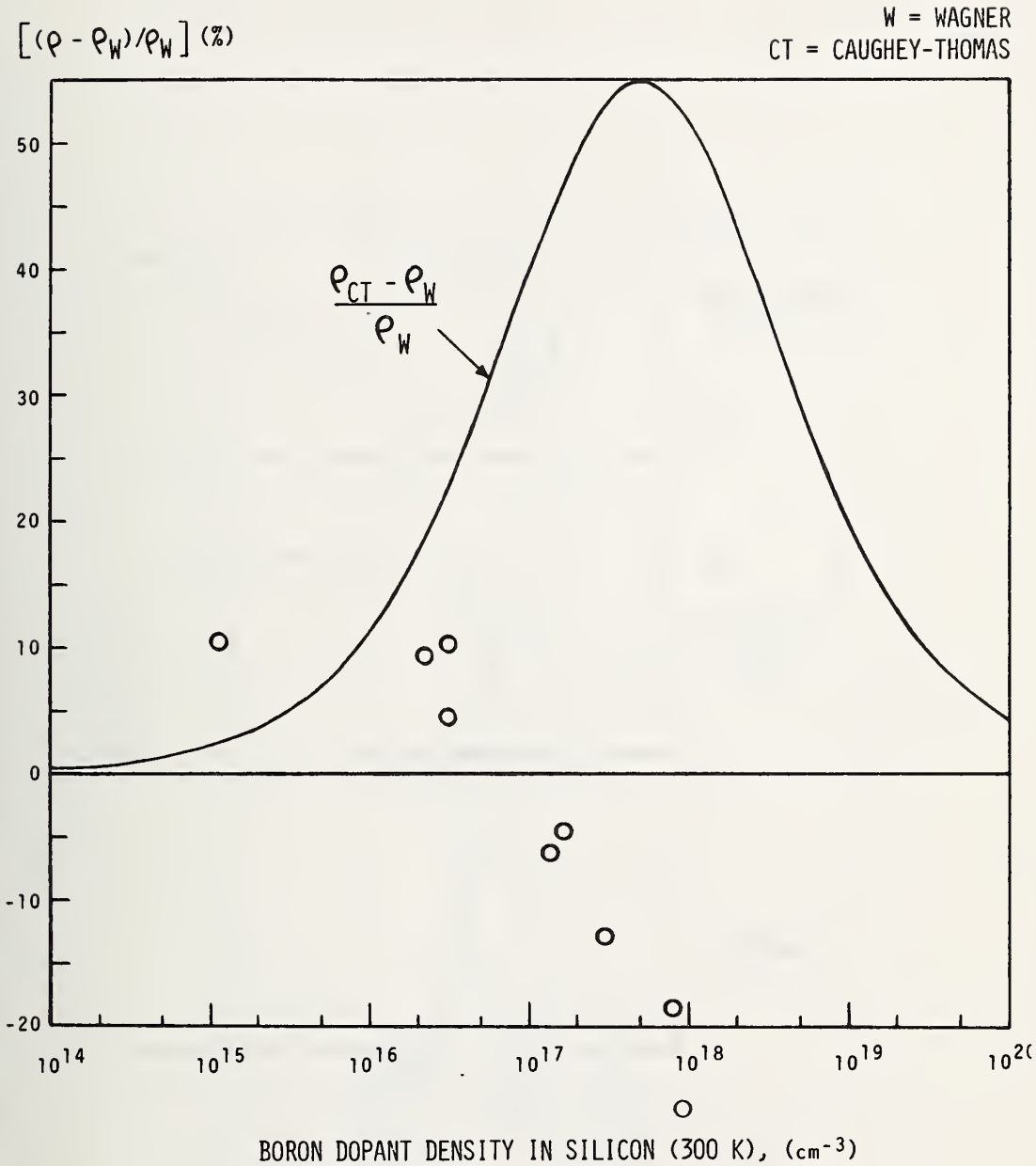


Figure 18. Normalized resistivity difference versus dopant density for *p*-type silicon (300 K) which compares experimental data to the Wagner formula [2]. Also shown is a comparison between the Caughey-Thomas [11] and Wagner [2] formulas.

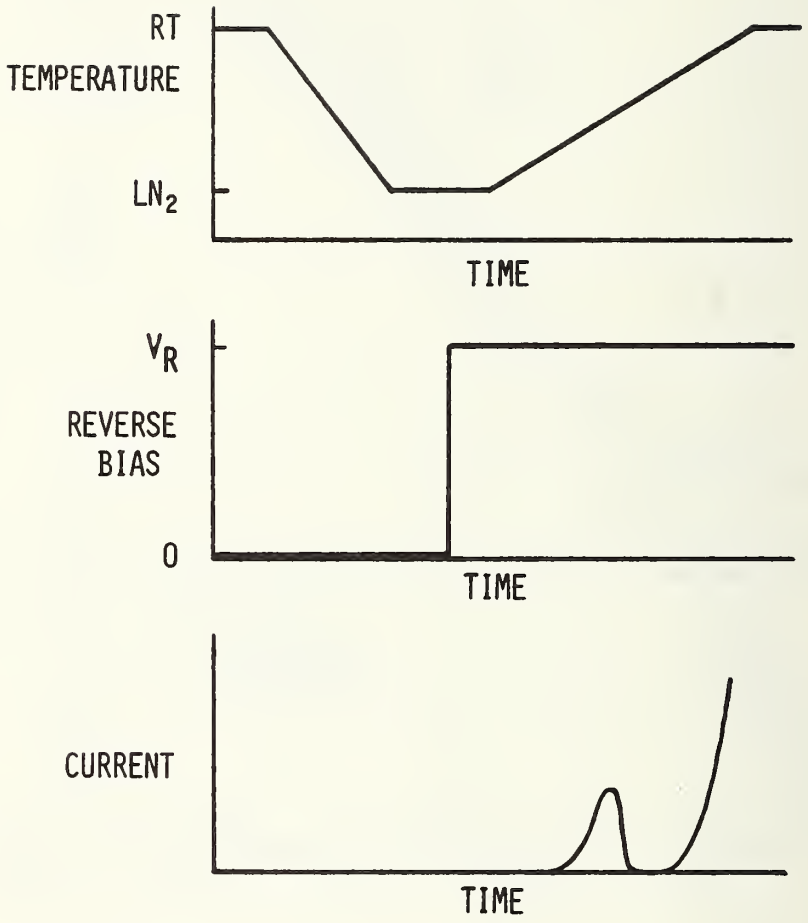


Figure 19. An outline of the thermally stimulated current measurement obtained with the use of a *p-n* junction.

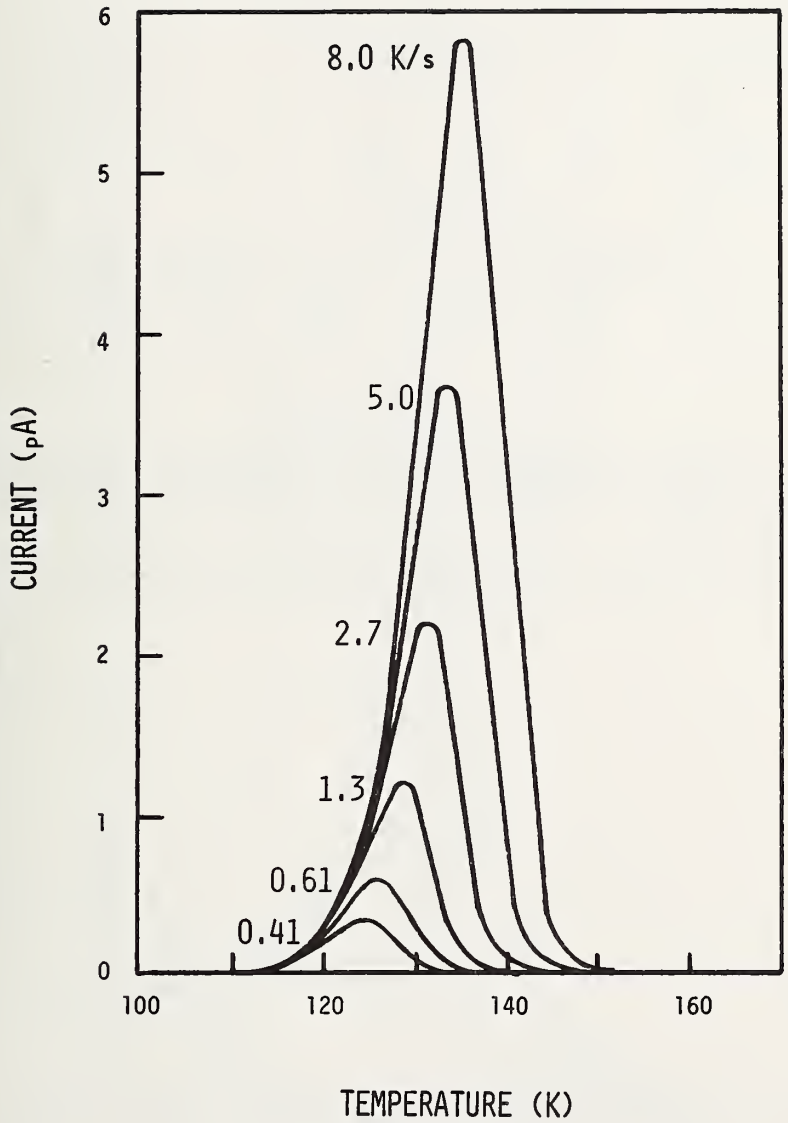


Figure 20. Thermally stimulated current response of the gold donor located on the n-side of an n^+p silicon junction for various heating rates [13].

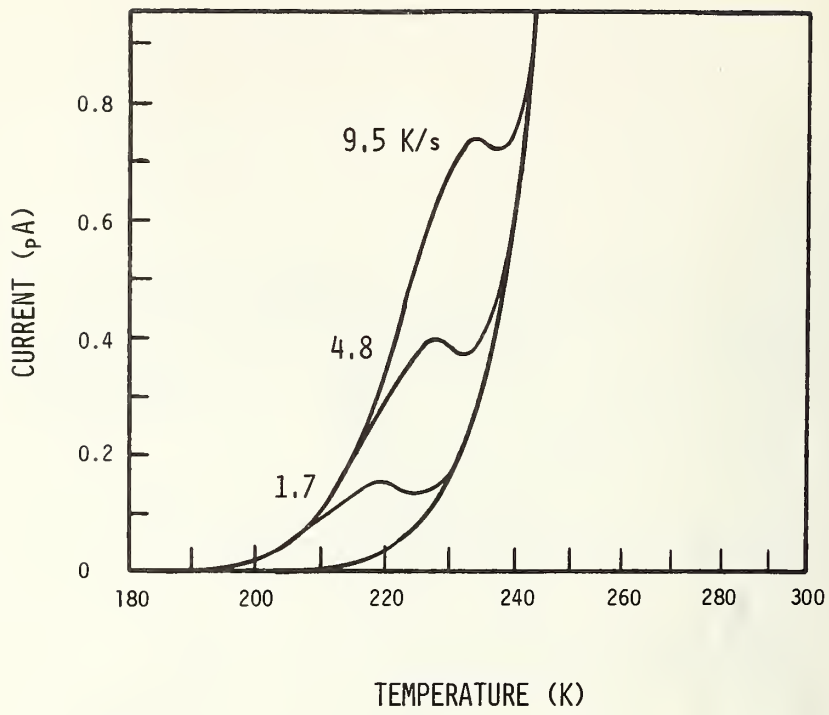


Figure 21. Thermally stimulated current response of the gold acceptor located on the n-side of a $p^{+}n$ silicon junction for various heating rates [14].

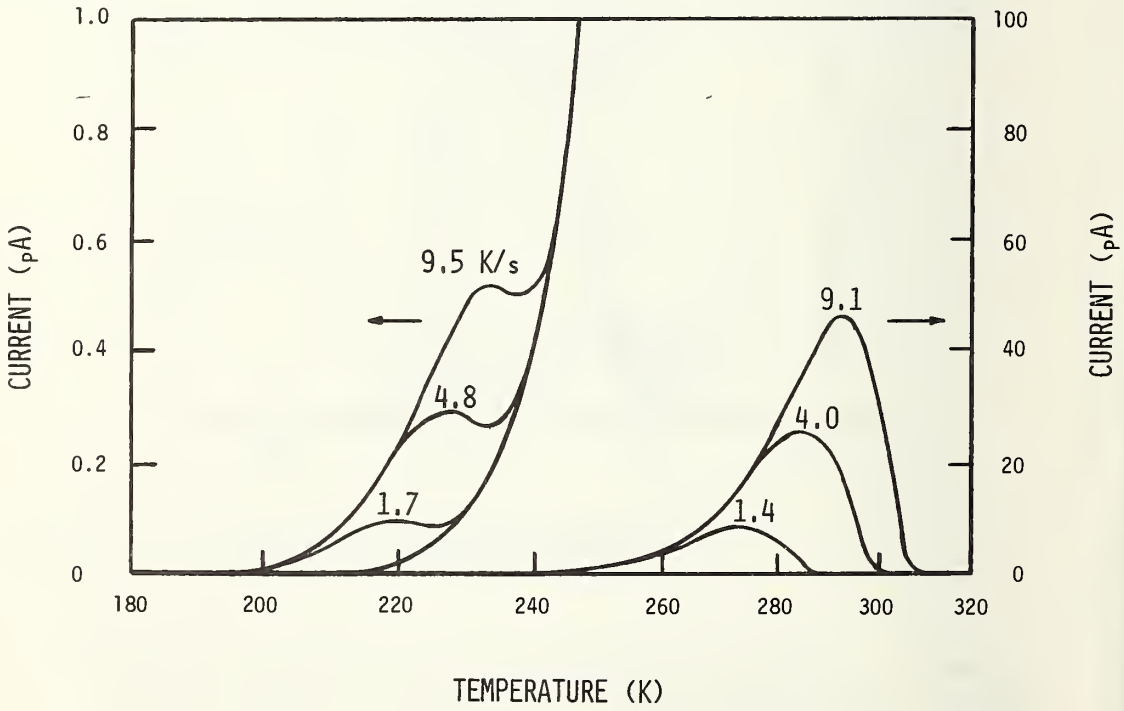


Figure 22. Thermally stimulated current response of the gold acceptor in an n-type silicon MOS capacitor for various heating rates [14].

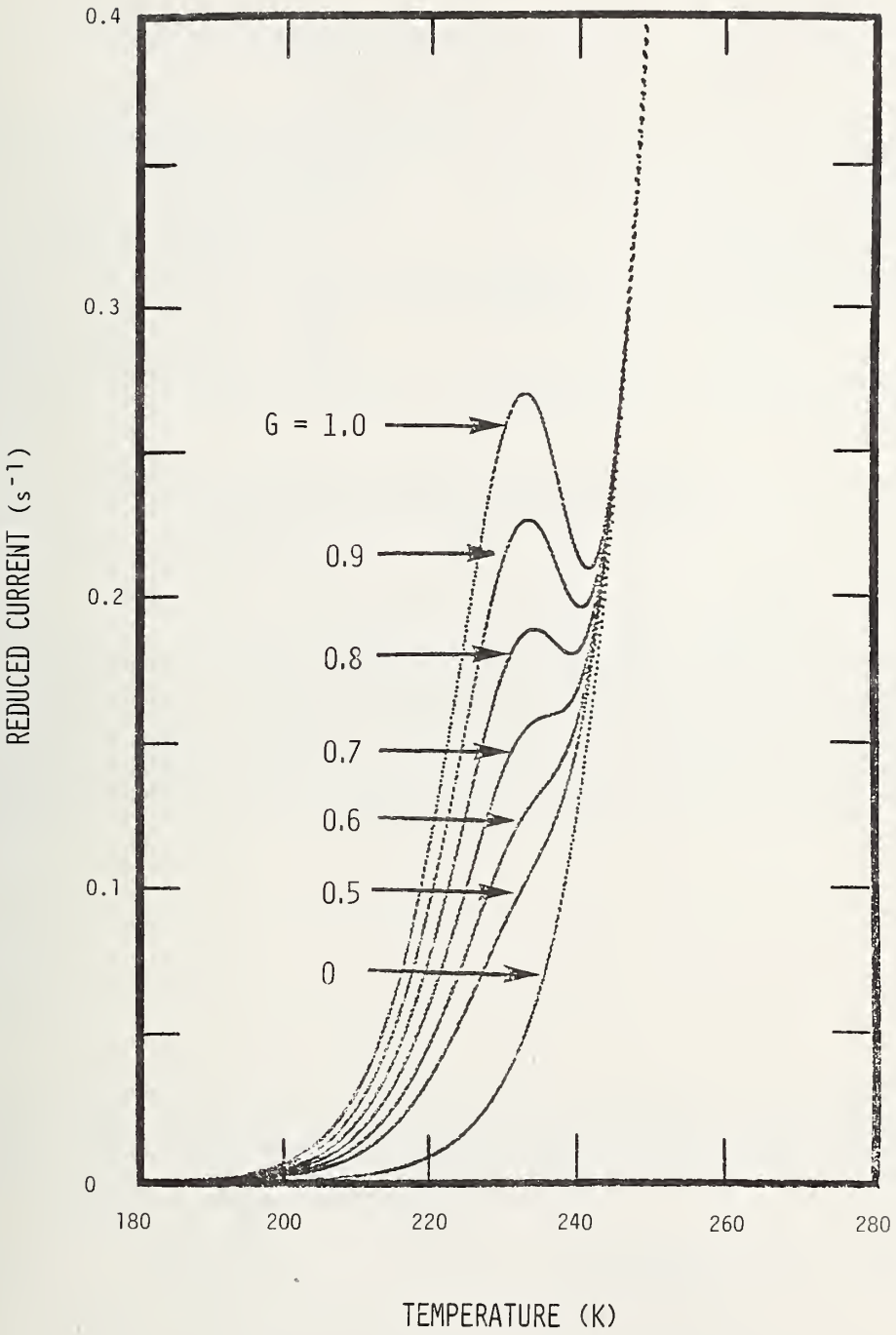


Figure 23. Thermally stimulated current response of the gold acceptor in *n*-type silicon for a heating rate of 10 K/s and for various G-factor values (explained in the text) [14]. The current is divided by a factor which includes the electronic charge, the area of the junction, the depletion width and the gold density.

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16. ABSTRACT *(A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.)*

Various test structures such as sheet resistors, p-n junctions, and MOS capacitors and their associated physical models have been developed to characterize dopants and defects in silicon. These structures address various needs within the semiconductor industry for (a) well-designed and miniaturized test structures such as an orthogonal van der Pauw sheet resistor, (b) simple and economical measurements such as the oxide window width of a diffused layer, (c) updated values for the resistivity versus dopant density relation, and (d) improved detection methods for identifying defect centers which control the lifetime and leakage currents of devices.

17. KEY WORDS *(six to twelve entries; alphabetical order; capitalize only the first letter of the first key word unless a proper name; separated by semicolons)* MOS capacitors; p-n junctions; resistivity of silicon; semiconductor devices; semiconductor process control; sheet resistors; test patterns; thermally stimulated currents.

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