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Semiconductor Measurement Technology

Progress Report

January 1 to June 30, 1975

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[1] Headquarters and Laboratories at Gaithersburg, Maryland, unless otherwise noted; mailing address Washington, D.C. 20234.

[2] Located at Boulder, Colorado 80302.

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Institute for Applied Technology
National Bureau of Standards
Washington, D.C. 20234

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PREFACE

The Semiconductor Technology Program serves to focus NBS efforts to enhance the performance, interchangeability, and reliability of discrete semiconductor devices and integrated circuits through improvements in measurement technology for use in specifying materials and devices in national and international commerce and for use by industry in controlling device fabrication processes. Its major thrusts are the development of carefully evaluated and well documented test procedures and associated technology and the dissemination of such information to the electronics community. Application of the output by industry will contribute to higher yields, lower cost, and higher reliability of semiconductor devices. The output provides a common basis for the purchase specifications of government agencies which will lead to greater economy in government procurement. In addition, improved measurement technology will provide a basis for controlled improvements in fabrication processes and in essential device characteristics.

The Program receives direct financial support principally from three major sponsors: the Defense Advanced Research Projects Agency (ARPA),* the Defense Nuclear Agency (DNA),† and the National Bureau of Standards (NBS).× In addition, the Program receives support from the U. S. Navy Strategic Systems Project Office.§ The ARPA-supported portion of the Program, Advancement of Reliability, Processing, and Automation for Integrated Circuits with the National Bureau of Standards (ARPA/IC/NBS), addresses critical Defense Department problems in the yield, reliability, and availability of integrated circuits. The DNA-supported portion of the Program emphasizes aspects of the work which relate to radiation response of electron devices for use in military systems. There is considerable overlap between the interests of DNA and ARPA. Measurement oriented activity appropriate to the mission of NBS is a critical element in the achievement of the objectives of both other agencies.

Essential assistance to the Program is also received from the semiconductor industry through cooperative experiments and technical exchanges. NBS interacts with industrial users and suppliers of semiconductor devices through participation in standardizing organizations; through direct consultations with device and material suppliers, government agencies, and other users; and through periodically scheduled symposia and workshops. In addition, progress reports, such as this one, are regularly prepared for issuance in the NBS Special Publication 400 sub-series. More detailed reports such as state-of-the-art reviews, literature compilations, and summaries of technical efforts conducted within the Program are issued as these activities are completed. Reports of this type which are published by NBS also appear in the Special Publication 400 subseries. Announcements of availability of all publications in this sub-series are sent by the Government Printing Office to those who have requested this service. A request form for this purpose may be found at the end of this report.

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*Through ARPA Order 2397, Program Code 5D10 (NBS Cost Center 4259555). All contract work was funded from this source.

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§Code SP-23, through project order N0016475P070030 administered by Naval Ammunition Depot, Crane, Indiana (NBS Cost Center 4251533) and Code SP-27, through IPR SP6-75-4 (NBS Cost Center 4251547).

SEMICONDUCTOR MEASUREMENT TECHNOLOGY

PROGRESS REPORT
January 1 to June 30, 1975

Abstract: This progress report describes NBS activities directed toward the development of methods of measurement for semiconductor materials, process control, and devices. Both in-house and contract efforts are included. The emphasis is on silicon device technologies. Principal accomplishments during this reporting period included (1) completion and analysis of an interlaboratory evaluation of standard reference wafers for resistivity measurement by the four-probe method, (2) analysis of the effect of finite contact size on sheet resistance as measured with a van der Pauw structure, (3) calculation of errors introduced in measuring line width with typical microscope systems, (4) development of procedures for predicting the magnitude of electron beam induced current in silicon device structures, (5) application of the optical flying-spot scanner to observation of hot spots and nonlinearities in UHF power transistors and of logic patterns in an MOS shift register, and (6) determination of a more accurate electrical method, based on peak junction temperature measurement, to establish safe operating area curves for medium power transistors. Also reported are the results of work on spreading resistance measurements, ionization of dopant impurities in silicon, Rutherford backscattering measurements, X-ray photoelectron spectroscopy, ion microprobe mass analysis, tests for determining the surface quality of sapphire substrates, reevaluation of Irvin's curves, mathematical models of dopant profiles, deep depletion measurements of dopant profiles and epitaxial layer thickness, bias-temperature stress tests on MOS capacitors, a high voltage capacitance-voltage method for measuring characteristics of thick insulator films, ion implantation parameters, methods for determining integrity of passivation overcoats, optical imaging and calibration standards for photomask metrology, line-width measurements, charge-coupled device test structures, a test pattern for silicon-on-sapphire MOS device technologies, a nondestructive acoustic emission test for beam-lead bonds, pull and shear tests for wire bonds, leak detection by helium mass spectrometry, correlation of moisture infusion in semiconductor packages with leak size and device reliability, an automated scanning low-energy electron probe, electron beam induced damage in silicon device structures, and thermal resistance measurements on Darlington transistors. Supplementary data concerning staff, publications, workshops and symposia, standards committee activities, and technical services are also included as appendices. A sixth appendix summarizes the results of an assessment of the impact of automation of integrated circuit processing and assembly on future measurement requirements in the industry.

Key Words: Acoustic emission; beam-lead bonds; bias-temperature stress test; boron redistribution; capacitance-voltage methods; charge-coupled devices; Darlington pairs; deep depletion; dopant profiles; electrical properties; electron beam induced current; electron beam induced damage; electronics; epitaxial layer thickness; hermeticity; leak tests; measurement methods; microelectronics; optical flying-spot scanner; passivation overcoats; photomask metrology; pull test; resistivity; Rutherford backscattering; scanning electron microscope; scanning low energy electron probe; semiconductor devices; semiconductor materials; semiconductor process control; shear test; sheet resistors; silicon; silicon-on-sapphire; spreading resistance; test patterns; thermal resistance; thermal response; transistors; wire bonds; X-ray photoelectron spectroscopy.

1. INTRODUCTION

This is a report to the sponsors of the Semiconductor Technology Program on work during the twenty-seventh and twenty-eighth quarters of the Program. It summarizes work on a wide variety of measurement methods for semiconductor materials, process control, and devices that are being studied at the National Bureau of Standards. The Program, which emphasizes silicon-based device technologies, is a continuing one, and the results and conclusions reported here are subject to modification and refinement.

The work of the Program is divided into a number of tasks, each directed toward the study of a particular material or device property or measurement technique. This report is subdivided according to these tasks. Highlights of activity during the quarters are given in section 2. Subsequent sections deal with each specific task area. References cited are listed in the final section of the report.

The report of each task includes a narrative description of progress made during this reporting period. Additional information concerning the material reported may be obtained directly from individual staff members identified with the task in the report. Considerable reorganization of the Program occurred at the end of this reporting period. This report is organized along the new organizational structure which is listed together with staff telephone numbers in Appendix A.

Background material on the Program and individual tasks may be found in earlier progress reports as listed in Appendix B. From time to time, publications are prepared that describe some aspect of the program in greater detail. Current publications of this type are also listed in Appendix B. Reprints or copies of such publications are usually available on request to the author. In addition tutorial videotapes are being prepared on selected measurement topics for dissemination to the electronics community. Currently available videotapes and procedures for obtaining them on loan are also listed in Appendix B.

Communication with the electronics community is a critical aspect both as input for guidance in planning future program activities and in disseminating the results of the work to potential users. Formal channels for such communication occur in the form of workshops and symposia sponsored or cosponsored by NBS. Currently scheduled seminars and workshops are listed in Appendix C. In addition, the availability of proceedings from past workshops and seminars is indicated in the appendix.

An important part of the work that frequently goes beyond the task structure is participation in the activities of various technical standardizing committees. The list of personnel involved with this work given in Appendix D suggests the extent of this participation. In most cases, details of standardization efforts are reported in connection with the work of a particular task.

Technical services in areas of competence are provided to other NBS activities and other government agencies as they are requested. Usually these are short-term, specialized services that cannot be obtained through normal commercial channels. To indicate the kinds of technology available to the Program, such services provided during the period covered by this report are listed in Appendix E.

During this period, a study of the impact of automation in the semiconductor industry on measurement technology requirements during the next five to ten years was conducted. The findings and conclusions from this study are summarized in Appendix F.

2. HIGHLIGHTS

Highlights of progress in the various technical task areas of the program are listed in this section. Unless otherwise identified the work was performed at the National Bureau of Standards.

Particularly significant accomplishments during this reporting period included (1) completion and analysis of an interlaboratory evaluation of standard reference wafers for resistivity measurement by the four-probe method, (2) analysis of the effect of finite contact size on sheet resistance as measured with a van der Pauw structure, (3) calculation of errors introduced in measuring line width with typical microscope systems, (4) development of procedures for predicting the magnitude of the electron beam induced current in silicon device structures, (5) application of the optical flying-spot scanner to observation of hot spots and nonlinearities in UHF power transistors and of logic patterns in an MOS shift register, and (6) determination of a more accurate electrical method, based on peak junction temperature measurement, to establish safe operating area curves for medium power transistors.

Resistivity — Analysis of the results of the interlaboratory evaluation of standard reference material SRM 1520, boron-doped silicon for four-probe resistivity measurements, was completed; the standard wafers were shown to be stable and the 95 percent confidence estimate of reproducibility for two-laboratory referee measurements was found to be less than 2 percent.

A study of the effect of surface preparation and other measurement parameters on the resistivity of silicon wafers as determined by the spreading resistance technique is nearing completion. Theoretical and experimental development of a simplified algorithm for analysis of spreading resistance measurements on graded structures was begun at Solecon Laboratories. The algorithm is based on a relationship similar to that employed in analyzing differential sheet resistance measurements. Preliminary measurements at RCA Laboratories suggest the feasibility of a high-speed spreading resistance probe which operates without lifting the probe tips from the wafer surface while they are moved across the surface. At present, readings may be taken 4.5 to 7 times faster than with conventional equipment.

As one phase of the work to reevaluate the relationship between resistivity and impurity density in n- and p-type silicon, several models were used to analyze the ionization state of dopant impurities as a function of dopant density. None of the models studied gave satisfactory results in the intermediate density range around 10^{18} cm^{-3}.

Surface Analysis Methods — Analysis of Rutherford backscattering measurements on a heavily zinc implanted silicon specimen, made as part of a comparative study of electron, ion, and photon beam surface analysis measurement technologies, illustrated some of the advantages and limitations of this technique for profiling impurity densities.

Additional study of the angular dependence of x-ray photoelectron spectra from silicon revealed crystal orientation effects and suggest that the bulk plasmon peak results from an extrinsic process which occurs during the path of the electron out of the solid.

Work was undertaken at Texas Instruments to develop methods for preparation of standard specimens for empirically calibrating an ion microprobe mass analyzer so that quantitative measurements can be made of selected impurities in silicon and silicon dioxide regions of semiconductor devices. A mask was designed and fabricated for use in defining a pattern of small areas in which the impurity of interest can be ion implanted.

A rapid nondestructive infrared reflectance technique to determine the surface quality of sapphire substrates is being investigated at RCA Laboratories. Correlation has been observed between the results of reflectance measurements and other analytical methods such as x-ray diffractometry, x-ray surface and transmission topography, and chemical etch tests.

A study of techniques for determining and controlling the quality of furnace environments used in growing and subsequent annealing of gate oxides for MOS devices was undertaken. Attempts to measure trace amounts of sodium in the furnace gas by means of a flame emission spectroscopy system attached to the exit port of the furnace tube were unsuccessful. Preliminary measurements suggest that resonance fluorescence spectroscopy can be used to detect extremely low levels of free sodium in the furnace tube, and further investigation of this technique is in progress.

Surface analysis for silicon devices was the topic of the fourth ARPA/NBS Workshop

held at NBS Gaithersburg in April. The workshop was attended by 146 representatives from industry, government, and universities. Highlighting the workshop were three approaches to overcoming the problem of sodium migration during distribution profiling measurements and debates about the existence and extent of the non-stoichiometric transition region at the silicon dioxide-silicon interface. Another area of active discussion by speakers and participants involved consideration of the detection limits and capability for making quantitative determinations by beam probe techniques. It was pointed out that no single beam spectroscopy can provide all the answers and that before beam techniques can be used to provide reliable and quantitative determinations, both standard reference materials and standard measurement procedures must be developed.

Test Structure Applications — Additional data on *n*-type silicon have been collected in the study of the resistivity-dopant density relationship with the use of the collector four-probe resistor and the base-collector diode on Test Pattern NBS-3. Electron mobilities found from these measurements were in good agreement with mobility values calculated from an empirical fit to Irvin's curve for *n*-type silicon.

The computer program developed to solve the boron redistribution problem by means of a finite difference algorithm was extended to include a radiative-type boundary condition at the oxygen-oxide interface.

Theoretical analysis of the MOS deep depletion method for profiling dopant density distributions showed that dopant densities can be calculated to within about 5 percent at depths as small as two Debye lengths from the surface when the depletion model is used. This measurement technique was also applied to the determination of epitaxial layer thickness.

Preliminary bias-temperature stress measurements made on a group of MOS capacitors fabricated on *n*-type silicon wafers showed flat band voltage shifts of 1 V or less. These capacitors also showed similarly small voltage shifts under irradiation (unbiased) to 10^4 Gy (10^6 rad(Si)) in the scanning electron microscope.

Several instrumental improvements were made in the extended range capacitance-voltage technique being developed at RCA Laboratories for application to measurements on metal-insulator-semiconductor structures with thick insulator layers.

Materials and Procedures for Wafer Processing — As part of a study being conducted at Hughes Research Laboratories on critical parameters associated with ion implantation, preliminary range and range straggle measurements of boron and phosphorus implants into opposite-type silicon wafers were made by means of an automatic capacitance-voltage method.

In work undertaken at RCA Laboratories to develop techniques for evaluating the integrity of passivation overcoats on metallized integrated circuits, three different techniques are being investigated and compared.

Photolithography — A theoretical investigation was begun to determine quantitatively the effects of coherence of the illumination on the image of two parallel opaque lines on a transparent background and on the image of two parallel transparent lines on an opaque background. The results of these calculations yield a quantitative measure of the image quality based on root-mean-square differences between the spectra of the image intensity profile and the ideal intensity profile.

Calculations were also made of the effect of the degree of coherence of the illumination at the object plane of a microscope with diffraction limited lenses and its effect on the intensity profile of a single edge. Effects of spherical aberration and defocussing were considered, and the measurement errors which might be encountered in using filar and image shearing eyepieces were estimated.

Because of difficulties in fabricating the originally designed measurement artifact intended for use in establishing standards for line-width measurements in the 1 to 10 μm range, a substitute interim artifact was obtained. Comparative measurements were made on this artifact with filar and image shearing eyepieces. The results of these measurements agreed well with the predictions of the above theoretical calculations.

Test Patterns — Finite difference methods were used to solve Laplace's equation in two dimensions in order to calculate correction factors to account for the finite length and width of contact arms on sheet

resistor test structures of the van der Pauw type. Cross structures with minimum process stripe widths were found to be feasible.

The investigation at the Naval Electronics Laboratory Center of the applicability of the charge-coupled device as a test structure for use in semiconductor process control was concluded with additional correlation of parameters measured on various charge-coupled device structures and those measured on more conventional structures such as MOS capacitors, MOS transistors, and gated diodes.

A task to develop a test pattern array for complementary MOS on sapphire integrated circuits was initiated at RCA Laboratories with the selection of design rules and five classes of test structures to be included in the pattern.

Interconnection Bonding — Procedures have been developed to bond beam-lead devices with one or two controlled weak bonds for use as test vehicles in the study of acoustic emission as a nondestructive test for weak beam-lead bonds. Instrumental changes were made to improve the reproducibility and sensitivity of the apparatus to the very weak acoustic emission of poorly bonded beam leads.

An interlaboratory evaluation of the destructive, double-bond pull test is being conducted in cooperation with ASTM Committee F-1 on Electronics. In addition, a two-laboratory comparison of the bond pull test with the bond shear test was conducted to determine their significance for evaluating aluminum-aluminum ultrasonic bonds. The shear test was found not to be sensitive to the weakest part of the connection, the heel of the first bond. The pull test, on the other hand, is particularly sensitive to the weakening of the bond heel.

Hermeticity — Several schemes are being investigated for quantitative measurement of gross leaks in hermetic packages. The rapid cycle dry gas gross leak test was analyzed further to include the case of repeated testing without repressurization in helium in order to pick out quickly leakers from a batch of parts.

The effect of helium absorption on the test specimens being used in an interlaboratory evaluation of the back-pressurization technique for leak detection with a helium mass spectrometer, being conducted in cooperation with ASTM Committee F-1 on Electronics, was further studied. It was decided that the interlaboratory test should be deferred until test specimens which are less susceptible to helium absorption can be obtained.

A study has been initiated at Martin-Marietta Aerospace to derive a quantitative relationship between leak size in hermetic packages and moisture infusion. The initial phase of the work involved the calibration of an *in-situ* moisture sensor, development of microventing procedures, and selection of a moisture sensitive integrated circuit.

Device Inspection and Test — Work on the automated scanning low energy electron probe at the Naval Research Laboratory continued with assembly of the system and demonstration of its ability to observe variations in dielectric uniformity on an oxidized silicon wafer.

To facilitate application of the scanning electron microscope operating in the electron beam induced current (EBIC) mode for the diagnostic examination of silicon devices, a procedure was developed for predicting the magnitude of the EBIC signal. The procedure is based on published depth-dose curves and an analysis of the value for the fraction of energy backscattered which was shown to be essentially constant over the energy range of interest. Despite the fact that several simplifying assumptions were made, reasonable agreement was achieved with an experimental result.

The dual-laser flying-spot scanner was used to examine several device types. Hot-spot formation was observed in UHF power transistors of a type used extensively in phased array radar transmitters. The devices were operating well within rated conditions when the hot spots formed. The internal logic states in a *p*-MOS shift register were also observed with the scanner. The logic pattern was displayed nondestructively, and it was possible to change states within the device selectively and reversibly by increasing the incident light intensity.

Thermal Properties of Devices — Additional measurements were made on a specially fabricated four-terminal Darlington transistor to confirm the previously reported procedure for obtaining the thermal resistance of the output transistor from indirect electrical measurements.

Electrical techniques for estimating the peak junction temperature of power transistors were further developed. By comparing electrically determined peak junction temperatures with those determined by infrared microradiometry, it was demonstrated that these techniques could be used to determine more accurately the safe operating area limits of such transistors.

3. RESISTIVITY

3.1. Standard Reference Materials

The multipass interlaboratory test (NBS Spec. Publ. 400-17, pp. 8-9) of SRM 1520 [1] was completed. The purpose of the test was to establish both the stability of this SRM over a reasonable period of time and the level of agreement to be expected by any two laboratories using the SRM for referee purposes.

Each of the six participating laboratories, including NBS, was required to measure the room temperature resistivity of both wafers of its resident SRM set once a month for a twelve-month period. The measurements were made according to the standard four-probe method [2], except that only two repetitive measurements on each wafer were required instead of the normal ten. Raw data were submitted directly to NBS for calculation and reduction. This part of the experiment served both as a data base from which to estimate the time stability of the SRM sets, and also as a screen against sudden changes in any laboratory's measurement response which would influence the second part of the study.

In the second part of the test, two complete SRM sets, two silicon wafers at each of the two resistivity levels, were circulated to each of the participating laboratories with a frequency of one laboratory per month. Two complete cycles of the laboratories were made during the study. The estimate of precision to be expected in referee use of the SRM's was generated from these data. The resistivity was again measured according to the standard four-probe method [2] but only five repetitions were required per wafer. The use of two complete sets in this part served both to enlarge the data base and to provide allowance for possible specimen breakage during the study.

The data reported by one participant showed a statistically significant high-side bias for all measurements. Since it was determined that this participant failed to follow the measurement procedure with respect to probe specifications and correction for temperature, these data were excluded from the final analysis of the results of the experiment.

The stability was evaluated by analyzing the drift of the resistivity values obtained on the ten resident specimens during the course of the experiment. The results are summarized in table 1. The data from each resident specimen were fitted to individual linear regressions [3] as a function of month number. The slopes of the individual regressions, if statistically significant above measurement scatter, indicate the extent of drift for that specimen-laboratory combination over the course of twelve months.

Individual estimates of slope and intercept with their estimated standard deviation are shown in the table. While seven of the ten estimated slopes were negative, indicating slight decrease of resistivity with time on balance, only one of the calculated slopes was larger than its estimated standard error. In addition, the small values of correlation coefficient suggest that the resistivity changes are not linear with time.

With separate analyses for high and low resistivity levels, pooled estimates indicate that only slopes greater than 0.018 and 0.00018 ohm centimeters per month, respectively, would have been statistically significant at the 95 percent confidence level. The point of interest is the typical drift, if any, of all the specimens at either the low resistivity or the high resistivity level, taken as a whole for each level. Since there was only one slope in either category which exceeded its respective significance limit, this is well short of the 95 percent yield expected from the analyses performed if the hypothesis of detectable drift for material of either resistivity level were true. Hence, as a whole, this hypothesis must be rejected.

A statement of the precision to be expected in various referee measurement uses was derived from analysis of the measurements on the circulating sets of wafers using the calculated values of within laboratory and between laboratory variation for each specimen used [4]. Table 2 summarizes the results of the measurements and gives estimates from these results of the repeatability for replicate measurements within a lab and the reproducibility of measurements between two labs which could be expected with 95 percent confidence if the same specimens were used for referee measurement. The estimates of repeatability and reproducibility [4] are broken into three situations, namely those where the two laboratories involved would measure the specimen one, five, or ten

times each before comparing results.

Although these estimates show noticeable variation from specimen to specimen, it is judged that the data base is sufficiently large to pool the present results and apply the projected values to any SRM slices generated from the same starting material. The resulting 95 percent confidence estimates of reproducibility for two laboratory referee measurements are 1.9 percent, 1.7 percent, and 1.67 percent for the cases of one, five, and ten measurements per laboratory, respectively. (J. Mandel,* J. R. Ehrstein, and F. H. Brewer)

*NBS Institute for Materials Research.

Table 1 — Summary and Analysis of Four-Probe Resistivity Measurements on Resident Wafers

Month	Laboratory 1		Laboratory 2		Laboratory 3		Laboratory 5		Laboratory 6	
	A	B	A	B	A	B	A	B	A	B
1	0.11962	11.275	0.11732	11.180	0.11954	11.358	0.11775	11.090	0.12035	11.095
2	0.12020	11.294	0.11814	11.421	0.11987	11.313	0.11800	11.075	-	-
3	0.12010	11.329	0.12173	11.675	0.11972	11.238	0.11780	11.050	0.12006	11.088
4	0.12002	11.288	0.11904	11.298	0.11908	11.242	0.11970	11.135	0.11922	11.160
5	0.12008	11.328	0.11824	11.158	0.11912	11.208	0.11973	11.204	-	-
6	0.12000	11.286	0.11850	11.368	0.11917	11.268	0.11975	11.260	0.12084	11.012
7	0.12032	11.324	0.11979	11.599	0.11958	11.333	0.11885	11.015	0.11928	11.042
8	0.12006	11.304	0.11790	11.246	0.11898	11.257	0.11659	10.815	0.11987	11.096
9	0.11998	11.312	0.11830	11.306	0.11898	11.290	0.11675	10.885	0.12048	11.120
10	0.12005	11.305	0.12031	11.489	0.11966	11.296	0.11896	11.046	0.11988	11.102
11	0.11982	11.274	0.11955	11.509	0.11967	11.250	0.11778	10.998	0.12004	11.163
12	0.11984	11.288	0.11934	11.441	0.11892	11.291	0.11738	10.912	0.11960	11.113
b_0	0.120035	11.3032	0.118522	11.3250	0.119574	11.2888	0.118774	11.1617	0.120094	11.0778
S_{b_0}	0.000117	0.0125	0.000767	0.1016	0.000209	0.0276	0.000701	0.0706	0.000393	0.0350
b_1	-0.000004	-0.0004	0.000075	0.0101	-0.000033	-0.0016	-0.000080	-0.0187	-0.000018	0.0030
S_{b_1}	0.000016	0.0017	0.000104	0.0138	0.000028	0.0037	0.000095	0.0096	0.000050	0.0044
r	0.089	0.077	0.223	0.226	0.348	0.131	0.256	0.524	0.130	0.232

Notes: b_0 = Estimated intercept

S_{b_0} = Estimated standard deviation of intercept

b_1 = Estimated slope

S_{b_1} = Estimated standard deviation of slope

r = Correlation coefficient

All values (except r) in ohm centimeters

Table 2 — Four-Probe Resistivity Measurements on Circulating Wafers

A. EXPERIMENT

Laboratory	A-13		A-17		B-84		B-85	
	ρ, Ω·cm	s, %	ρ, Ω·cm	s, %	ρ, Ω·cm	s, %	ρ, Ω·cm	s, %
Round 1								
1	0.11925	0.40	0.11977	0.13	11.108	0.13	11.175	0.10
2	0.11941	0.20	0.11967	0.07	11.054	0.60	11.067	1.06
3	0.11900	0.15	0.11970	0.39	11.140	0.54	11.418	0.83
5	0.11962	0.21	0.12010	0.21	11.168	0.10	11.252	0.12
6	0.11826	0.21	0.11913	0.30	11.049	0.16	11.103	0.31
Round 2								
1	0.11940	0.40	0.11984	0.22	11.112	0.07	11.228	0.32
2	0.11897	0.13	0.11954	0.25	11.103	0.53	11.302	0.52
3	0.11984	0.39	0.12076	0.54	11.163	0.16	11.346	0.56
5	0.11805	0.47	0.11909	0.24	11.034	0.29	11.113	0.36
6	0.11743	0.20	0.11813	0.10	11.051	0.31	11.192	0.17

B. ANALYSIS

	A-13	A-17	B-84	B-85
$\bar{\rho}$, Ω·cm	0.11892	1.11957	11.1003	11.1980
$\hat{\delta}$, %	0.297	0.280	0.308	0.426
$\hat{\delta}_L$, %	0.633	0.564	0.406	0.782
R_{w_1}, %	0.824	0.776	0.854	1.180
R_{w_5}, %	0.369	0.347	0.382	0.528
$R_{w_{10}}$, %	0.261	0.246	0.270	0.373
R_{b_1}, %	1.94	1.75	1.41	2.47
R_{b_5}, %	1.79	1.60	1.19	2.23
$R_{b_{10}}$, %	1.77	1.58	1.15	2.20

Notes: ρ = average of five measurements

s = relative sample standard deviation (coefficient of variation) of five measurements

$\bar{\rho}$ = grand average of reported averages

$\hat{\delta}$ = calculated coefficient of variation from within lab error

$\hat{\delta}_L$ = calculated coefficient of variation from between lab error

R_{wi} = predicted repeatability within lab - i measurements

R_{bi} = predicted repeatability between labs - i measurements

3.2. Spreading Resistance Measurements on Graded Structures

This task was undertaken to develop a simplified calculational procedure for the analysis of spreading resistance measurements on nonuniform structures such as diffused layers, for the purpose of computing profiles of resistivity with position in the layer. Thickness correction factors have been developed for layers of uniform resistivity [5-8], but their extension to nonuniform layers requires excessive computer time [5-7] or is of questionable validity [8].

In the present work it is intended to demonstrate that a differential relationship suggested earlier [8] can, with the use of a relatively simple correction factor, be used to generate resistivity profiles, utilizing only the difference between successive spreading resistance measurements and the thickness dependence of the correction factor.

Formally, for a pair of circular contacts on one surface of an infinite slab of material with uniform conductivity, σ, the conductance, G, between the contacts is

$$G = 2a\sigma H(t), \qquad (1)$$

where a is the contact radius and H(t) is a dimensionless factor which contains a correction for slab thickness, t. By applying the principle of superposition, eq (1) can be generalized to an n-layer structure with the result that

$$G = 2a \sum_{i=1}^{n} (\sigma_{i-1} - \sigma_i) H(t_{i-1}), \qquad (2)$$

where $\sigma_n = 0$.

After changing eq (2) to an integral form, and performing considerable mathematical manipulation, one finds that, in the limit for thin layers,

$$\sigma(x) = C_1 \frac{dG}{dx} \qquad (3)$$

provided that the limiting form of H(t) is linear in thickness for small t. Use of eq (3) permits one to calculate conductivity (or resistivity) profiles from measurements of conductance as a function of distance into the film, starting from the deepest part of the layer. Under some circumstances, however, it may be necessary to know the second derivative of H(t) with respect to x which appears in the more general equation for $\sigma(x)$.

In order to evaluate H(t), the potential distribution problem defined by two circular equipotential contacts on the surface of the two layer structure must be solved. Because it has mixed boundary conditions, the problem has no known analytic solution for a layer of finite thickness. It is expected however that the method used by Schumann and Gardner [5], based on the solution for a semi-infinite layer, can be applied. In using this formulation, a current distribution is assumed under the contact, and the resulting potential averaged over the contact interface in order to evaluate the factor H. The effects on the factor H of several assumed current distributions and weighted admixtures of such current distributions are being considered in order to more realistically approximate geometries which are not semi-infinite. (D. H. Dickey*)

Four sets of boron diffused wafers were prepared for use in studying the validity of the simplified calculational procedure described above. Boron was diffused into 10 Ω·cm phosphorus-doped wafers under contions designed to yield a surface density of 10^{19} cm^{-3} or lower and a junction depth of 1, 2, 5, or 10 μm. Each set consisted of four wafers with the same junction depth diffused at the same time. Sheet resistance of each layer has been determined by the four-probe method [9] and two wafers of each set were prepared for profile determinations by spreading resistance both at NBS and at Solecon Laboratories. An additional wafer from each set has been reserved for profiling by the incremental sheet resistance method [10] at NBS.
(Y. M. Liu)

3.3. High-Speed Spreading Resistance Probe

One of the limitations of the spreading resistance technique is the time required to collect data. This task was undertaken to define the mechanical and electrical conditions required to record the spreading resistance of two-point probe-to-silicon contact at substantially faster rates than the usual maximum rate of 10 to 15 data points per minute and to provide means for digital re-

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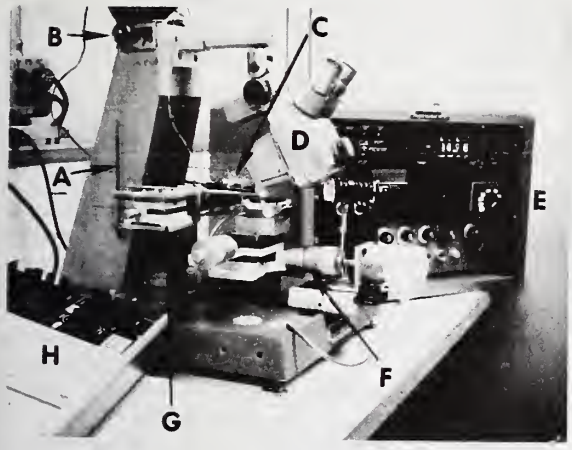
*Work performed at Solecon Laboratories under NBS Contract No. 5-35881. NBS contact for additional information: J. R. Ehrstein.



A Weights
B Pulley
C Prism
D Microscope
E Stepping motor drive
F Motor driven table
G Arm micrometer stage
H Point plotter

Figure 1. Two-point spreading resistance probe as modified for high-speed operation.

cording of the spreading resistance in a form suitable for subsequent computer analysis.

The approach selected was to modify a previously built two-point probe to permit readings to be taken while the probe points are dragged over the wafer surface. A view of the apparatus is shown in figure 1. The probe points are mounted on separate arms, each of which is pivoted on ball bearings. The force at the tip is varied by loading the other end of the arm with weights (A) via a pulley system (B). Brass weights permit the load to be varied from about 5 g to about 250 g in 4.5 g increments. The pivot for each arm is attached to an x-y micrometer stage (G) so that the separation and alignment of the probe points can be adjusted by viewing the points from the rear with the use of the microscope (D) and prism (C). The minimum spacing that can be obtained between the points is 200 μm. With some modifications of the holders, spacing down to about 100 μm should be achievable.

The probes are fixed; the wafer is placed on a table (F) driven by a stepping motor, capable of 200 steps per second, driven by a preset indexer (E). The indexer can be set so that the wafer moves under the probes at speeds between 9.4 and 850 μm/s. The resistance is determined by measuring the current which results when a potential of 10.0 ± 0.1 mV is applied between the two probe points. A voltage proportional to the logarithm of the current drives the y-axis of an x-y recorder operated as a point plotter (H) while a signal obtained from a ramp generator drives the x-axis. An internal timing circuit is used to trigger the recording of the two signals; at present readings may be taken as rapidly as 69 times per minute, 4.5 to 7 times faster than with conventional equipment.

The objectives of the initial experiments were to establish operating regions and to delineate the limits of usefulness. Major emphasis was placed on the choice of point geometry and loading; the criteria of selection were mainly the signal-to-noise ratio of the recorded trace, the reproducibility of the calibration graph, and the sensitivity to resistance change with load and speed. These experiments were conducted with tungsten carbide probe tips with 25-mil (0.64-mm) diameter shafts.

In a typical set of experiments a new pair of points is inserted into the holders, adjusted for equal length, and locked with a set-screw. Fine adjustment is made for spacing and alignment so that the line joining the probe tips is perpendicular to the direction of travel. Most runs were made with a spacing of 200 to 400 μm between points. The wafer is placed on the table and held down by vacuum supplied by a small pump. The arm assembly is lowered manually until the points touch the wafer and the arms are gently lifted off their rest stops. It is this action that applies the preselected load. Unlike the conventional spreading resistance probe, the lowering of the points onto the wafer is not a critical step. Sets of runs are then made using the same weight and a series of resistivity standards, followed by the next run at a greater loading, all under the same speed conditions and in ambient light. The temperature in the measurement room can fluctuate by about 8°C and is recorded. All scans are made in the same direction, such that the angle between the

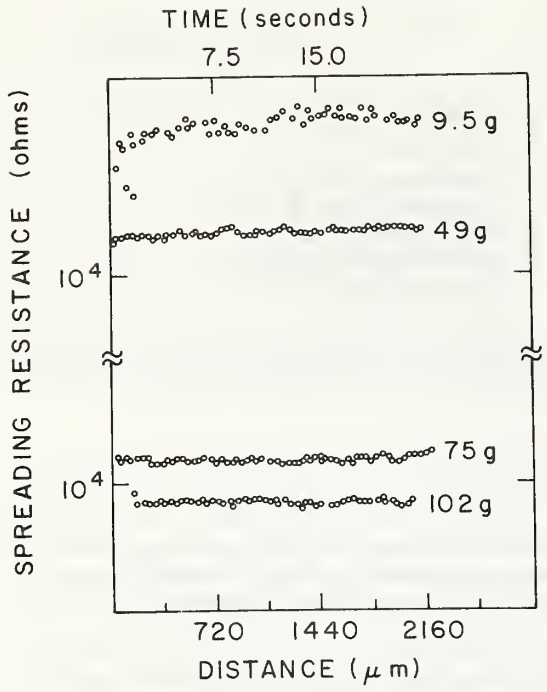


Figure 2. Spreading resistance as measured with four different loads on a tungsten carbide tip of radius 6.4 μm.

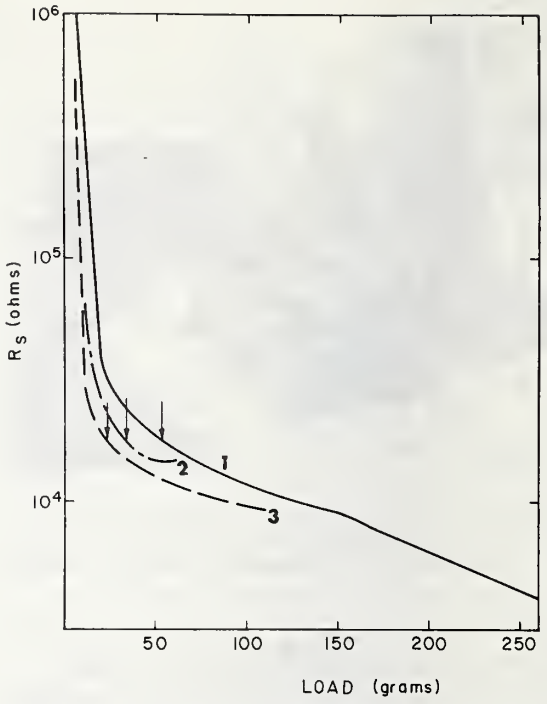
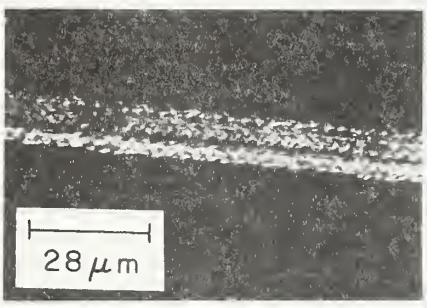
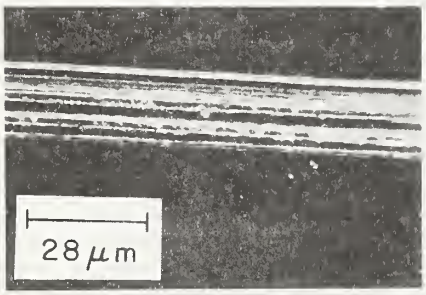


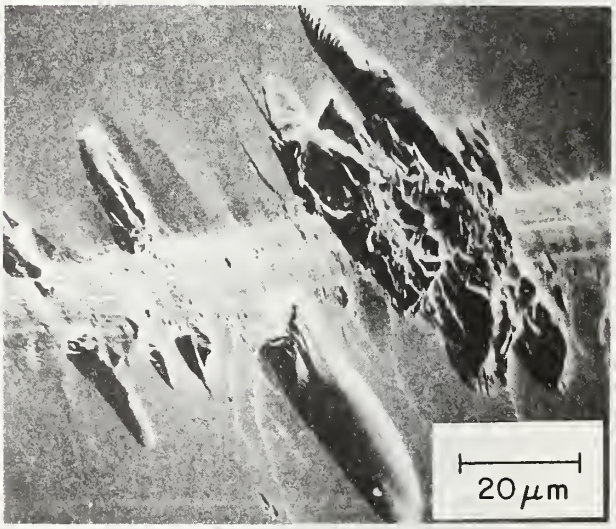
Figure 3. Spreading resistance as a function of load for three tungsten carbide tips of different radius. (Curve 1, 25 μm; curve 2, 10 μm; curve 3, 6.4 μm; the vertical arrows indicate the load below which the signal-to-noise ratio is unacceptably low.)



a. Load: 9 g.



b. Load: 49 g.



c. Load: 129 g.

Figure 4. Scanning electron micrographs of tracks left by a tungsten carbide probe tip of radius 6.4 μm.

shaft and the wafer surface is about 85 deg; the wafer is moved in the direction of the acute angle.

With tungsten carbide points the trace is noisy when the load is light and becomes reasonable after a sufficient force has been applied. Figure 2 shows a set of typical results on the same wafer with progressively greater probe loadings. The probe loading also affects the measured resistance. Figure 3 is a plot of measured resistance as a function of loading for probes of three different tip radii. All three curves in the figure show an inflection point. Experimentally, it is found that the signal-to-noise ratio increases as the loading is increased and is generally not acceptable at loadings less than the value indicated by the vertical arrows. From scanning electron micrographs of probe tracks, such as those illustrated in figure 4, it is clear that the contact area is smaller with the light load and that the point does not maintain uniform contact with the surface. At very heavy loads, the surface tends to chip and fissures appear; the resistance decreases as load is increased but the noise level does not change.

These observations lead to the tentative conclusion that the points make contact over the entire width of the track mark. This agrees with the experimental results that greater loading and larger radius give lower spreading resistance values roughly in proportion to the width of the track mark. It is clear that the silicon in contact with the point is highly disturbed. However, the disturbed layer is probably only a small fraction of the volume of silicon sampled by the probe point. The disturbed layer may, in fact, help to minimize surface effects by increasing the surface recombination velocity.

Tests were conducted over the entire speed range using tungsten carbide points on n-type silicon wafers with room temperature resistivity ranging from 0.01 to 70 Ω·cm. The probe tips used had radii of 0.25, 0.4, and 1.0 mil (6.4, 10, and 25 μm) and were loaded with about 40, 60, and 150 g, respectively. No substantial difference in measured resistance or noise was observed as a function of the speed with which the probe point traversed the wafer.

Initial calibration studies were carried out using n-type silicon wafers in the above resistivity range. The wafers were chemmechanically polished and the resistivity measured by the four-probe method [2]. The spreading resistance was measured using tungsten carbide points with a radius of 0.25 mil (6.4 μm), a load of 49 g. and a traverse speed of 63.5 mm/s. The initial calibration plot of log spreading resistance against log resistivity exhibited considerable scatter suggesting that many of the wafers may have substantial non-uniformities. Data obtained after the wafer surfaces had been cleaned in a mixture of 5 parts sodium hydroxide, 1 part water and 1 part hydrogen peroxide followed by a mixture of 5 parts hydrochloric acid, 1 part water, and 1 part hydrogen peroxide, and dried in air at 150°C for over 15 min did not show significant differences.

A few tests were run with a drop of high pressure cutting oil on the surface. The effect of this film was to raise the measured resistance by about 30 percent without decreasing the amount of noise. Examination of the track marks using phase contrast microscopy at 720X indicated that the amount of debris close to the track was reduced.

(A. Mayer* and N. Goldsmith*)

3.4. Ionization of Dopant Density in Silicon

In semiconductor studies it is often of importance to know the relationship between the density of majority carriers and density of dopant impurities in uncompensated material. In particular, in theoretical calculation of carrier mobility it is necessary to know the relative amounts of ionized and neutral atoms to compute their scattering contributions. For lightly doped, but extrinsic, uncompensated silicon at room temperature the Fermi energy lies between the impurity energy and the center of the band gap; hence, essentially all the substitutional dopant atoms are ionized and the majority carrier and dopant densities are equal. As the density of dopant atoms is increased, the Fermi energy approaches and passes through the impurity energy and the fraction of ionized dopant atoms is decreased; hence, the majority carrier density may be less than the dopant density. At still higher dopant densities the system becomes metallic and the dopant atoms are again fully ionized. The unresolved question is whether there is a significant region of dopant density which lies

*Work performed at RCA Laboratories under NBS Contract No. 5-35914. NBS contact for additional information: J. R. Ehrstein.

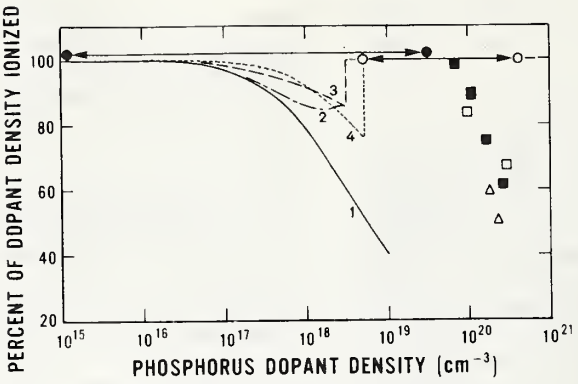


Figure 5. Ionization of phosphorus in silicon at 300 K. (Theoretical: 1, constant ionization energy; 2, eq (5); 3, eq (6); 4, Berg [18]. Experimental: □, Gardner *et al.* [19]; ○, Crowder and Fairfield [20]; ●, Nakanuma [21]; ■, Esaki and Miyahara [22]; △, Irvin [24] (arsenic).)

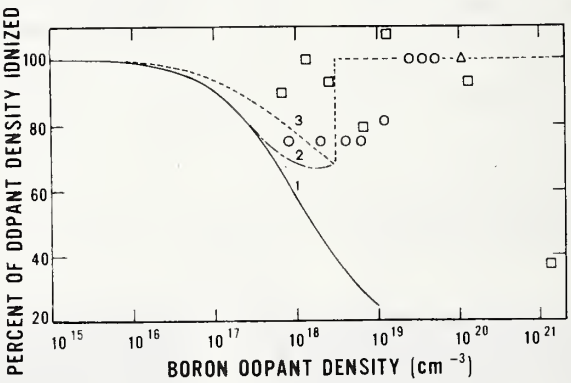


Figure 6. Ionization of boron in silicon at 300 K. (Theoretical: 1, constant ionization energy; 2, eq (5); 3, eq (6). Experimental: □, Pearson and Bardeen [12]; △, Irvin [24]; ○, Hofker *et al*, [25].)

between the two regions of essentially full ionization. To begin to answer this question calculations were made of the fraction of ionized dopant atoms according to various models and the results compared with available experimental data.

The calculation of the ionized dopant density was made using a digital computer to solve, by iteration, for the Fermi energy in the charge balance equation. Since the minority carrier density can be neglected in extrinsic silicon, the majority carrier density equals the density of ionized dopant atoms. Therefore, the charge balance equation becomes for n-type material

$$N_c\{\exp[(E_c-F)/kT] + 0.27\}^{-1} = N_d\{1 + g_d^{-1}\exp[(F-E_c+\varepsilon_d)/kT]\}^{-1}, \quad (4a)$$

and for p-type material

$$N_v\{\exp[(F-E_v)/kT] + 0.27\}^{-1} = N_a\{1 + g_a\exp[(\varepsilon_a+E_v-F)/kT]\}^{-1}, \quad (4b)$$

where N_c or N_v is the effective density of states in the conduction or valence band, E_c or E_v is the energy of the conduction or valence band edge, F is the Fermi energy; k is Boltzmann's constant; T is absolute temperature; N_d or N_a is the donor or acceptor dopant density, g_d or g_a is the degeneracy factor of the donor or acceptor impurity, and ε_d or ε_a is the ionization energy of the donor or acceptor impurity. A value of 0.5 was used for g_d while g_a was taken as 0.25. The carrier density on the left hand side of these equations includes an approximation given by Blakemore [11] for the Fermi integral which gives results within ±3 percent of those given by the Fermi integral whenever $F/kT < 1.3$. This limit was not exceeded in the present calculations so that the results are statistically correct for degenerate as well as non-degenerate conditions. For electrons, a density-of-states effective mass of 1.18 m_o [12] was used giving $N_c = 3.22 \times 10^{19}$ cm^{-3} at 300 K. For holes, a mass of 0.81 m_o [12] was used resulting in $N_v = 1.82 \times 10^{19}$ cm^{-3} at 300 K.

Figures 5 and 6 show percentage of dopant density ionized as a function of total density for phosphorus-doped and boron-doped silicon, respectively, at 300 K for several models. The curve for a constant ionization energy of 0.045 eV (appropriate to both impurities) shows a rapid decrease in percent ionization for dopant densities greater than 10^{17} cm^{-3}. Because of both effective mass and degeneracy factor differences, the fraction of ionized atoms is less for boron-doped silicon than for phosphorus-doped with the same dopant density.

Experimental evidence exists which shows that the ionization energy is not constant, but decreases with increasing dopant density [13, 14]. Penin [14] found that the equation

$$\varepsilon_d = \varepsilon_{d0} - 8\varepsilon_{d0}\left(\frac{1}{2} + \frac{a^*}{r_d}\right)\exp\left(-\frac{r_d}{a^*}\right) \qquad (5)$$

with an ionization energy $\varepsilon_{d0} = 0.045$ eV for lightly-doped material, an average distance $r_d = [3/(4\pi N_d)]^{1/3}$ between impurity atoms, and an effective Bohr radius $a^* = 21 \times 10^{-8}$ cm gave a calculated ionization energy in good agreement with his experimental results for phosphorus-doped silicon. For boron-doped silicon the same equation with identical parameters was used as ε_{d0} and a* are essentially the same as in phosphorus-doped material. As seen in the figures, the use of this equation results in a higher fraction of ionized atoms at large dopant densities. At 3×10^{18} cm^{-3} the ionization energy has decreased to zero. This is also the dopant density for which the theoretical calculations of Kleppinger and Lindholm [15] predict a disappearance of the ionization energy due to significant overlapping of the impurity and conduction bands. The assumption is made that all impurity atoms are ionized at higher dopant densities. This transition is indicated by a dashed vertical line. Complete ionization at high dopant densities is in agreement with Hall coefficient measurements in heavily doped *n*- and *p*-type silicon from 4 to 300 K which show no evidence of an ionization energy at impurity densities greater than 3×10^{18} cm^{-3} [16]. Furthermore Fistul' [17] argues that heavily doped semiconductors do not have shallow impurity levels and consequently the dopant is completely ionized as in the case of metallic conduction.

The second model for the ionization energy follows Pearson and Bardeen [13] in that the energy is taken inversely proportional to the average distance of separation between the dopant atoms:

$$\varepsilon_d = \varepsilon_{d0} - aN_d^{1/3}, \qquad (6)$$

where the constant a was assigned the value 3.1×10^{-8} cm·eV for both phosphorus- and boron-doped silicon to give zero ionization energy at a dopant density of 3×10^{18} cm^{-3} for comparison with eq (5). With eq (6) the ionization energy begins to decrease at lower doping densities than for eq (5) and because of the more gradual decrease in ε_d the ionized density decreases monotonically in contrast to the scallop in the curve between 1 and 3×10^{18} cm^{-3} associated with Penin's model.

The above calculations were made assuming a single energy level for the impurity states and a conduction or valence band density of states appropriate for lightly doped material. It is known [14] that as the doping density increases the impurity level broadens into a band and there is tailing in the density of states of the nearby intrinsic band edge. To some extent the use of an ionization energy which depends on doping density

incorporates these changes. However for densities greater than 10^{17} cm^{-3} the above equations begin to lose their validity. Consequently calculations were also made using a model developed for gallium arsenide by Berg [18]. This model takes into account the broadening of the impurity level and the tailing of the conduction band. The density of states in the broadened impurity level was assumed to be Gaussian in nature as formulated by Dyakonov *et al.* [19]. Berg found that the model gave good computer fits to his data provided that the tailing of the conduction band edge was increased by the factor 1.6 over the theoretical value. This same factor was also used in the present calculations for *n*-type silicon. As seen in figure 5 the percent ionization is similar to that obtained from the Pearson and Bardeen model. Ionization is considered to be complete when the tail of the conduction band crosses the middle of the impurity band, which remains centered at 0.045 eV. This transition to complete ionization is indicated by the vertical line at a density of about 5×10^{18} cm^{-3}. The model was not estended to calculations on *p*-type silicon but the results are expected to show similar trends.

Experimental data on percentage ionization are also shown in figures 5 and 6. For phosphorus-doped silicon, Gardner *et al.* [20] compared carrier density derived from plasma resonance with total density obtained from neutron activation analysis. On a phosphorus-implanted specimen Crowder and Fairfield [21] measured essentially the same impurity profile by neutron activation analysis as they obtained by differential Hall effect measurements. Nakanuma [22] studied the incorporation of phosphorus in epitaxial silicon by radiotracer studies and compared the phosphorus content with that obtained by Hall effect and conductivity measurements. He found no existence of electrically inactive phosphorus in the layers up to densities of 3×10^{19} cm^{-3}. Using colorimetric analysis and Hall effect measurements, Esaki and Miyahara [23] determined that the percentage of ionized phosphorus in silicon at room temperature decreases gradually from nearly 100 to 60 percent with increasing phosphorus density in the range from 0.68 to 2.6×10^{20} cm^{-3}. Mousty *et al.* [24] compared neutron activation analysis and Hall effect measurements on silicon doped with phosphorus in the range 10^{17} to 10^{19} cm^{-3}. With the assumption of complete ionization, they calculated the Hall scattering factor and found that it increased from 1.0 at 10^{17} cm^{-3} to 1.3 at 10^{18} cm^{-3} and then decreased to 1.0 at 10^{19} cm^{-3}. There is the possibility that the peak in the scattering factor is due in part to incomplete ionization. Irvin [25] gives results on two specimens of arsenic-doped silicon* on which both neutron activation analysis and Hall effect measurements were made and on one boron-doped specimen for which the total boron content was determined by a photometric technique for comparison with the Hall effect result. Based on the amount of boron impurity added to the melt and subsequent Hall effect measurements on the grown crystals, Pearson and Bardeen [13] concluded that each boron atom gave one charge carrier (within ±20 percent) except for one very heavily doped crystal in which only part of the boron went into solid solution. Hofker *et al.* [26] profiled a boron-implanted wafer by secondary ion mass spectrometry and compared it with Hall effect measurements on the same wafer.

The sharp decrease in electrical activity of dopant atoms at densities greater than about 10^{20} cm^{-3} appears to occur because many of the dopant atoms do not occupy substitutional sites at these high densities rather than because of incomplete ionization. Unfortunately, the available experimental data are insufficient to resolve the question of whether there is an intermediate range of dopant densities, near 10^{18} cm^{-3}, for which ionization may not be complete. Therefore it is not possible at this time to establish the validity of any of the models used in the calculations. (W. R. Thurber)

*The parameters for arsenic-doped silicon are very similar to those of phosphorus-doped silicon.

4. SURFACE ANALYSIS METHODS

4.1. Comparative Study of Surface Analysis Techniques

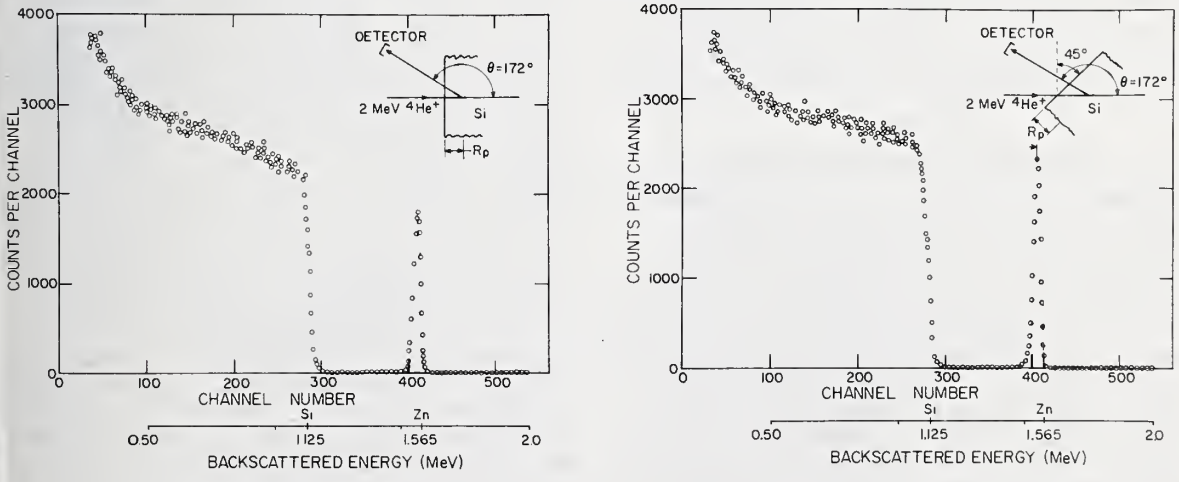
As part of the comparative study of surface analysis techniques (NBS Spec. Publ. 400-12, pp. 17-18) a Rutherford backscattering experiment [27, 28] was performed.* Only one of the four specimens included in the study was suitable for analysis by this technique. The atomic number of the impurity in each of the other three specimens was below the atomic number of the host matrix, and there was an insufficient amount of the impurity present for it to be observed over the background signal due to the host. The specimen which was measured, a silicon wafer implanted with 30 keV zinc ions to a dose of 5×10^{16} cm^{-2}, was exposed to a 40 nA current of 2.0 MeV $^4He^+$ ions over a 1 mm^2 area, to a total dose of 10 μC.

The experiment is conducted by recording the number of particles backscattered from the specimen at a fixed angle as a function of the energy of the backscattered particles using a silicon surface barrier detector and multi-channel pulse--height analyzer [27]. Two measurements were made, one with normal incidence and one with the beam incident at 45 deg. The results are presented in figure 7. The energy scale was established by measuring the $^4He^+$ backscattered energies from aluminum (1.102 MeV) and gold (1.845 MeV) surfaces; the channel width was determined to be 3.46 keV.

The projected range of the implanted particles may be estimated from the energy difference between the energy of the peak response obtained with normal incidence and the energy of a backscattered helium atom just after collision with a zinc atom. This energy loss corresponds to a range of about 37.5 nm which is somewhat larger than the value, 22.4 nm, predicted by LSS theory [29].

If the detector had sufficient resolution, the distribution profile of the implanted ions could be inferred from the shape of the response. However, the resolution of the detector used was only ∿15 keV. Since the expected range straggling, defined as the half width of the distribution profile at $1/\sqrt{e}$ of the maximum density, corresponds to an energy difference of only about 4 keV, it is clear that the width of the response peak is due primarily to the detector resolution, and no information regarding the shape of the implanted distribution can be inferred. Although detecting systems with significantly better resolution are available, they are much less sensitive than silicon detectors and their use requires much greater time to complete the measurement.

*The measurements were made by Prof. M. A. Nicolet at the van de Graaf accelerator facility of the California Institute of Technology, Pasadena, California.



a. Normal incidence.

b. Angle of incidence, 45 deg.

Figure 7. Yield as a function of energy of backscattered 2.0 MeV $^4He^+$ ions from zinc-implanted silicon wafer.

It is also possible to determine the total zinc implantation dose, D_{Zn}, from the ratio of the area of the response peak to the area under a portion of the silicon plateau [28]. If this is done for the two measurements in figure 7, one obtains $D_{Zn} = 4.99 \times 10^{16}$ cm^{-2} and 5.52×10^{16} cm^{-2}. These values are in reasonable agreement with the value of D_{Zn} (5×10^{16} cm^{-2}) determined at the time of implantation.

Although this technique is a rapid, nondestructive method for establishing identity, location, and density of impurity atoms, it has several important limitations. First, it is most sensitive to impurities of high atomic number; the bulk detection limit is proportional to the square of the atomic number. Furthermore, for elements of lower atomic number than the host matrix, the peak appears superimposed on the host plateau, which further degrades the detection limit. Second, the method lacks lateral resolution. If the beam diameter were reduced to increase lateral resolution, the duration of the measurement would have to be substantially increased or else the detection limits would suffer significantly. Third, the position of the peak depends on both the location and identity of the impurity atoms and also on the orientation of the crystal. This can complicate the analysis and may require that one have considerable knowledge of the specimen to sort out the various parameters of interest. Finally, the technique requires rather large amounts of the impurity to be present if it is to be seen; hence it is more frequently used for analysis of thin surface layers than for profiling trace impurity distributions. (A. G. Lieberman)

4.2. X-Ray Photoelectron Spectroscopy

Previous studies of the angular dependence of x-ray photoelectron spectra from dirty surfaces, which revealed depth profile information about carbon and oxygen overlayers on silicon (NBS Spec. Publ. 400-12, pp. 15-17), were extended to clean silicon surfaces. The angular dependence of the Si(2p) photoline at about 1160 eV, its associated first surface (Sp) and bulk (Bp) plasmon peaks at about 1150 and 1145 eV, respectively, the Si(2s) photoline at about 1110 eV, the background signal at about 1000 eV, and the KLL Auger complex near 1600 eV were measured. The results are shown in figure 8.

The background region shows only a smooth variation with angle. At small and negative angles, the intensity falls off due to shadowing of the x-ray beam by the specimen surface. At angles near 90 deg, the specimen subtends a small solid angle at the analyzer slits. Also, microscopic surface irregularities tend to reduce the electron intensity.

The behavior of the other spectral regions is much more interesting, showing a number of sharp peaks with angular widths as small as 2 or 3 deg. Similar effects have been reported previously on single crystals of sodium chloride and gold, although not with such sharp angular resolution. The explanation for these regions of enhanced emission has been attributed to internal electron diffraction or channeling effects. While a channeling description is apparently valid for heavy particles and high ($\sim$ 100 keV) energy electrons, there is some doubt that this description is valid for electrons in the 1 keV energy range. However, data reported for emission of β- particles (with energy up to 450 eV) from radioactive ^{175}Yb implanted in a silicon single crystal [30] appear to substantiate the validity of the channeling concept at low energies.

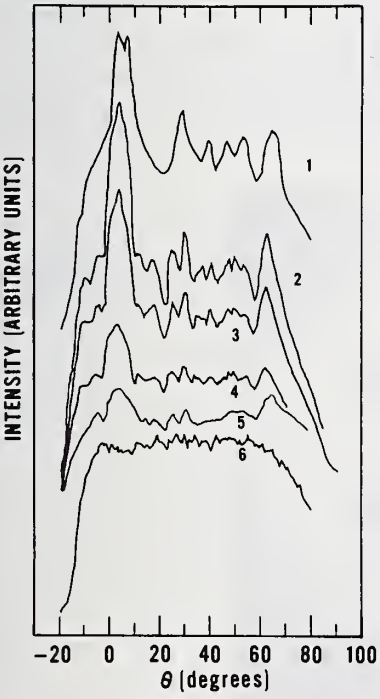
Ratios of certain pairs of intensities are also shown in figure 8. The Si(2s) to Si(2p) ratio (not plotted) is essentially constant. The bulk plasmon (Bp) to Si(2p) ratio, however, shows a number of peaks and valleys. In particular, at angles where the Si(2p) intensity goes through a maximum, the Bp intensity does not increase proportionately as much. This has some profoundly interesting implications. One of the most important, but also most difficult, questions faced by the ESCA Task Force of the Surface Analysis Subcommittee of ASTM Committee E-2 on Emission Spectroscopy is the question of how should one measure XPS peak intensities to derive quantitative elemental ratios. The difficulty arises in part because one has not known to what extent plasmon and other energy loss peaks should be included with the main photopeak intensity. Previously, there has been no good way of distinguishing whether the plasmon peaks seen are an intrinsic process associated with the primary photo-ionization event or an extrinsic process produced during the path of the electron out of the solid. The existing data are contradictory and inconclusive. For magnesium, aluminum, and sodium, one group maintains that plasmon creation is entirely an extrinsic process [31], while for graphite, another group maintains that the process is entirely intrinsic [32].

If, in silicon, the bulk plasmon creation were entirely an intrinsic process, one might assume that the effective origin of the emitted electron would be associated with its original silicon lattice site, in which case the Bp intensity should scale with the Si(2p) line intensity. If the plasmon were created during the passage of this electron from the solid, its effective origin would be expected to correspond to a non-substitutional location and the Bp/Si(2p) intensity ratio should then decrease along channeling directions. This is precisely what is observed to happen in the vicinity of the <111> channeling direction at $\theta = 0$ deg. This may be the first solid experimental evidence and method for deciding between the intrinsic versus extrinsic character of a plasmon excitation.

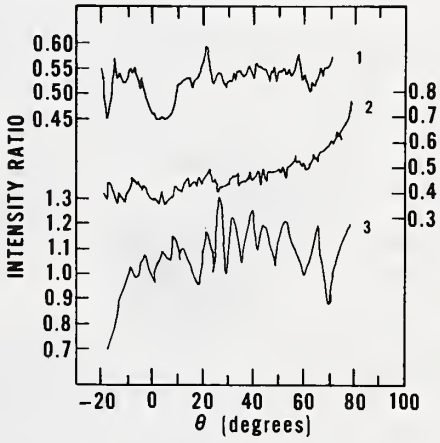
The surface plasmon (Sp) to Si(2p) ratio is quite scattered due to poor statistics on the Sp count rate, but it also appears to show a dip near the <111> direction at $\theta \simeq 0$ deg.

The more interesting behavior is the increase in the ratio at large angles where the electrons are leaving nearly parallel to the specimen surface. It is under these angular conditions that the surface tends to be emphasized in the spectra so the Sp count rate tends to become proportionally larger.

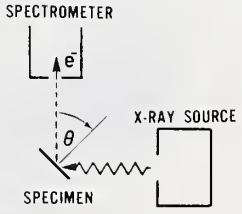
The KLL/Si(2p) ratio shows still another interesting behavior. At small angles, the x-ray beam strikes the specimen at near grazing incidence and eventually approaches the critical angle for total reflection. Under these conditions, the x-ray penetration depth is limited to approximately the wavelength of the radiation which is in the order of 1 nm. Since the escape depth of the Auger electrons at about 1600 eV is greater than that of the Si(2p) photoelectrons at about 1160 eV, the limited penetration depth of the x-rays selectively decreases the effective depth from which the Auger electrons originate and hence causes the KLL/Si(2p) ratio to decrease near grazing incidence.



a. Relative intensities for the KLL Auger complex, curve 1; the Si(2p) and Si(2s) photolines, curves 2 and 3, respectively; the bulk (Bp) and surface (Sp) plasmons, curves 4 and 5, respectively; and the background spectrum, curve 6.



b. Intensity ratios: Bp/Si(2p), curve 1; Sp/Si(2p), curve 2; and KLL/Si(2p), curve 3.



c. Geometric arrangement

Figure 8. Angular dependence of x-ray photoelectron spectra from clean silicon surfaces.

Due to randomizing collisions of the emitted photoelectrons, anisotropies of the valence band structure were thought to be removed from the XPS spectra. However, a possible consequence of the dependence of the escape probability of an electron upon electron site origin is that the apparent valence band density of states might indeed depend on the angle of observation. From observations of the valence band spectrum of silicon at several different angles, it was deduced that the apparent density of states does indeed change.

It has been tacitly assumed by most XPS experimentalists that crystal orientation would have little or no effect on valence band spectra provided one stayed away from grazing electron take-off angles where the surface is strongly emphasized. These results show this assumption is not valid.

(N. E. Erickson*, A. G. Lieberman, T. E. Madey* and J. T. Yates, Jr.*)

4.3. Calibration Standards for Ion Microprobe Mass Analysis

This task was undertaken to develop methods for preparation of standard specimens for empirically calibrating an ion microprobe mass analyzer (IMMA) so that quantitative measurements can be made of selected impurities in silicon and silicon dioxide regions of semiconductor devices. Implicit in this objective is the evaluation of the applicability of the IMMA for this type of analysis and the determination of the instrumental parameters best suited for these analyses.

The plan for preparation of the standards is to ion implant the impurity of interest into silicon or silicon dioxide matrices in small, well-defined surface areas. Since the depths of the implants are controlled by the implant energy, the standard sample will be essentially a microvolume containing a known total amount of impurity but with a concentration that ranges from several thousand parts per million atomic to less than 1 part per billion atomic. The microvolumes range in size from small enough to be entirely consumed during analysis to large enough to be considered an infinite surface plane. Aluminum metallization is used to locate the implanted region and, in the case of silicon dioxide, to act as the necessary surface conductive layer.

The microvolume photomasks have been designed and fabricated. The repeat pattern is 100 by 100 mils (2.54 by 2.54 mm) and contains regions ranging in size from 1/2 by 1/2 mil (13 by 13 μm) to 30 by 30 mils (0.76 by 0.76 mm). Figure 9 shows a photomicrograph of the photomask repeat pattern. The numbers and sizes of the implanted regions are listed in table 3. The metal locator photomask has an identical pattern with each opening slightly larger than the implant opening. The regions outside the implant openings are protected from implantation by the photoresist film. Both are correct positive photomasks to facilitate alignment without special alignment marks that could necessitate extra processing steps. Figure 10 is a photomicrograph of an oxide layer implanted with phosphorus using this set of masks.

Initial material selected for the study is a group of 190 2-in. (50-mm) diameter wafers cut from the same dislocation-free, float-zone *p*-type silicon crystal with room temperature resistivity in the range 3 to 25 Ω·cm. Twelve wafers were chosen randomly for evaluation of substrate impurity content. All 12 wafers were cleaned according to a standard procedure; six were oxidized in dry oxygen at 1100°C to obtain a 0.12 μm thick

Table 3 — Number and Sizes of Microvolumes in Repeat Patterns of Implantation Photomask

Size, mils (μm)	Number
½ × ½ (13 × 13)	5
1 × 1 (25 × 25)	5
2 × 2 (51 × 51)	9
2 × 3 (51 × 76)	9
3 × 4 (76 × 100)	9
4 × 5 (100 × 130)	5
5 × 6 (130 × 150)	4
6 × 7 (150 × 180)	4
7 × 8 (180 × 200)	1
8 × 9 (200 × 230)	1
9 × 10 (230 × 250)	1
30 × 30 (760 × 760)	1

*NBS Surface Processes and Catalysis Section, Physical Chemistry Division.

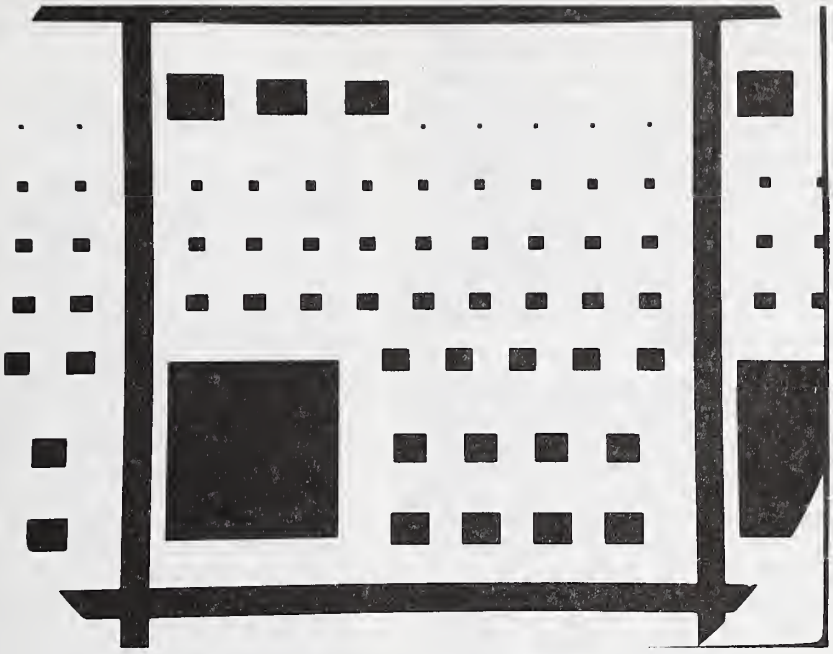


Figure 9. Photomicrograph of photomask repeat pattern. (Magnification: ∿27X.)

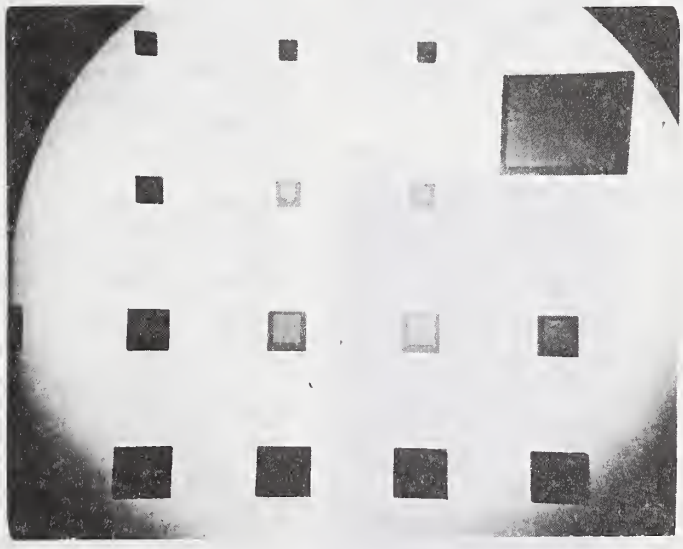


Figure 10. Photomicrograph of oxidized silicon wafer showing implantation micro-volumes in a portion of the repeat pattern. (Magnification: ∿76X.)

oxide. To minimize the introduction of contamination during oxidation the furnace had double quartz tubes with dry nitrogen flowing between the walls of the inner and outer tubes. All 12 wafers are being analyzed by neutron activation analysis and ion microprobe mass analysis (IMMA). Long-term point counts are being taken on the IMMA at masses 23, 30, 31, 52, 75, and 197, corresponding to sodium, silicon, phosphorus, chromium, arsenic, and gold, to determine a statistical background level relative to the silicon matrix to be expected in the analysis of the implanted standards.

The linearity of the IMMA secondary ion pickup and detection system is being determined as a function of raster size by monitoring the silicon ion count at 10-second intervals over a one- to two-hour period. The initial parameters chosen for the study were a silicon matrix; a $^{32}O_2^+$, 20 keV, 10 nA primary sputter beam with a 15 μm spot; and a 20-mil (0.5-mm) resolution slit. The raster size is being varied from 25 by 20 μm to 300 by 240 μm in 25 by 20 μm steps. This study has already shown that the pickup can vary as much as 50 percent from raster site to raster site. However, the variation does not appear to be a predictable function of raster size. The variation is minimized by tuning the primary magnet and primary column for symmetrical ion current at the opposite extremes of both the x-axis and y-axis sweeps. Also, the secondary magnet must be tuned for the best symmetrical signal at the opposite ends of the x-axis sweep.

Characterization of the secondary ion signal as a function of raster size and electronic aperture size has been initiated. The Si signal is being collected in 10-s increments using 200 by 160 μm, 150 by 120 μm, 100 by 80 μm, and 50 by 40 μm rasters with electronic aperture ratios of 1 by 1, 3/4 by 3/4, 1/2 by 1/2, and 1/4 by 1/4 on each raster size. The first results suggest that the signal is a function only of the electronic aperture acceptance ratio and is independent of the raster size. This shows that constant sputtered volumes do produce a constant secondary ion signal.

The sputter rate for 20-keV $^{32}O_2^+$ on silicon as a function of raster size has been determined by measuring the depth of the craters sputtered during the raster size linearity study. The depths were measured by both optical interferometry and surface profilometry. The sputter rates obtained from the 10 nA beam ranged from 0.017 to 4.16 nm/s and varied linearly with surface area sputtered. (R. Dobrott* and G. B. Larrabee*)

4.4. Optical Test for Surface Quality of Sapphire Substrates

This task was undertaken to develop a fast nondestructive optical test for the surface quality of sapphire substrates and to correlate optical data with data from conventional analytical techniques and with measurements of the electrical properties of heteroepitaxial silicon films in silicon-on-sapphire (SOS) structures. Barker [33] has demonstrated that forbidden vibrational modes may be introduced into the infrared reflection spectrum of sapphire as a result of crystallographic strain and work damage. This observation is being utilized in the development of a process to examine nondestructively the surface perfection of sapphire substrates on which the silicon is to be heteroepitaxially grown. The reflection technique is ideally suited for surface analysis, particularly in the case of sapphire, since the surface penetration depth in the spectral region of interest is estimated not to exceed a few hundred angstroms. This is a region of vital importance to the nucleation and growth of silicon films, and thus significantly affects the properties of semiconductor devices. The techniques under investigation can be used to study the surface perfection of sapphire substrates both before and after silicon epitaxy, since silicon is transparent in the spectral region of the measurement.

Sapphire substrates from several different crystal growth and polishing vendors have been examined by the infrared reflectance technique, and the results compared with control specimens. Examples of the reflectance spectra of both "good" and "poor" surfaces are given in figure 11. The specimens were supplied by different vendors for use in silicon epitaxy; the spectra were obtained on the surfaces as received. Curve a displays a high degree of surface perfection similar to the spectrum that would be obtained on a sapphire surface after annealing or chemical etching to remove

*Work performed at the Central Research Laboratories of Texas Instruments Incorporated under NBS Contract No. 5-35917. NBS contact for additional information: A. G. Lieberman.

polishing work damage. Curve b displays surface damage similar to that left by diamond polishing grit of particle size from 3 to 6 μm. In addition, Barker's surface analysis technique has been extended to multiple reflection methods to greatly accentuate small differences in the surface quality of the substrates. This is essential in order to understand uncontrolled variations in crystallinity and electrical properties of epitaxial silicon films.

Other analytical methods such as x-ray diffractometry (line broadening), x-ray surface and transmission topography, and chemical etch tests have also been used to characterize sapphire surfaces. It was found that there is a correlation between the results of reflectance measurements and the other analytical tests performed. For example, the x-ray surface topograph in figure 12 shows two distinct regions. The dark region which was polished with 6 μm diamond shows considerable lattice damage as indicated by the features in that portion of the topograph. The light region which was polished with a suspension of colloidal silica to achieve a high degree of surface perfection shows a featureless topograph consistent with the characteristics of a defect-free surface. The infrared reflectance spectra of these regions were similar to the traces shown in figure 11 and thus consistent with x-ray data.

Diffractometry traces (θ:2θ mode) from the same two regions are shown in figure 13. The half width for the "good" surface was 0.035 deg and for the damaged surface 0.045 deg. These values are typical for several specimens prepared in the above manner. The line broadening is 0.01 deg due to polishing damage if it is assumed that the surface polished with colloidal silica is a perfect surface. Photomicrographs of surfaces preferentially etched in potassium hydroxide show characteristics similar in appearance to the x-ray topographs, revealing decoration of damage lines on the crystal surface. Characterization of very small differences in surface perfection is being explored. As a result of present work, infrared surface analysis based on multiple reflectance appears to be potentially more sensitive to surface perfection than any of the other nondestructive tests currently in use.

Either absolute or relative values of the optical constants [refractive index (η) and the absorption index (k)] are the parameters for quantifying the magnitude of the observed forbidden modes. Absolute values of the constants are obtained from numerical analysis of reflectance data using Kramers-Kronig relations following the general treatment of Roessler [34] and the related computer program of Klucker and Nielsen [35]. Initial

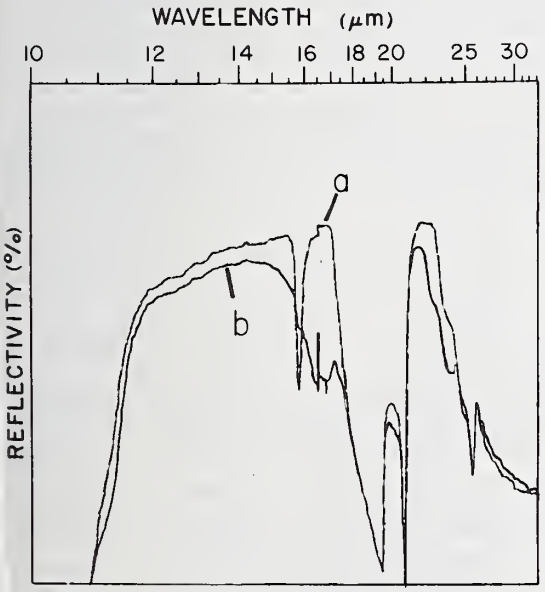


Figure 11. Infrared reflectance spectra of sapphire surfaces. (Curve a, surface polished with a suspension of colloidal silica; curve b, surface polished with 6 μm to 3 μm diamond.)

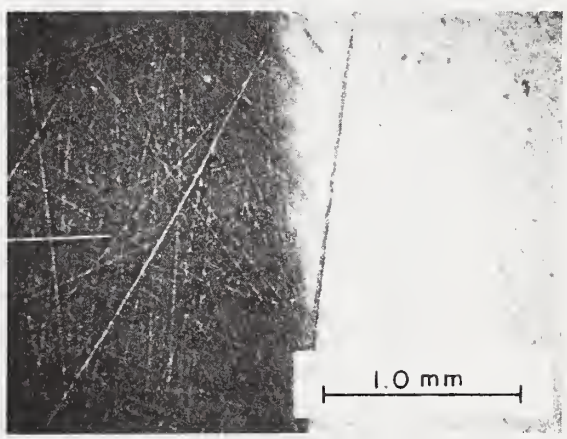


Figure 12. Reflection x-ray topograph of specially prepared ($\bar{1}012$) sapphire surface obtained with copper radiation using the ($\bar{3}030$) reflection plane.

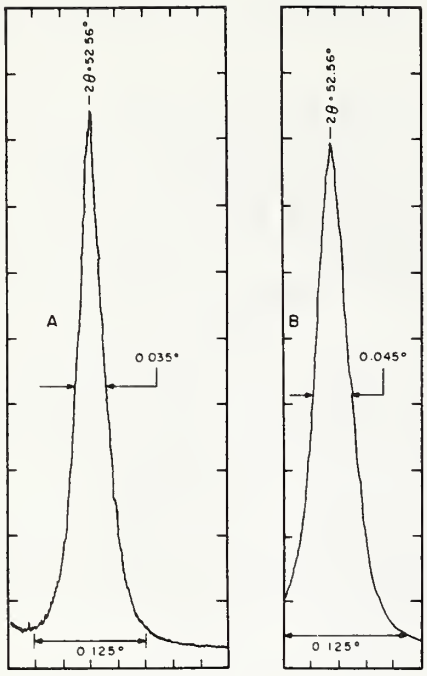


Figure 13. Diffractiometer traces of specially prepared ($\bar{1}012$) sapphire surfaces obtained in the θ:2θ mode with copper radiation using the ($02\bar{2}4$) reflection plane. (Surface polished with a suspension of colloidal silica, curve A; surface polished with 6 μm to 3 μm diamond, curve B.)

activity has centered on obtaining and testing the program with standard test data supplied with the program. This phase of testing is now complete.

The general applicability of multiple reflectance measurements to dielectrics and semiconductors is being examined. The wavelength region of interest depends on the absorption characteristics of the material in question. Preliminary measurements indicate that the deformation of symmetry states (as in sapphire) is not essential to these measurements. Epitaxial silicon films grown on work-damaged surfaces (as revealed by infrared reflectance) are degraded electrically relative to films grown simultaneously on control substrates. Optical reflectance measurements made on the silicon films in the ultraviolet region near the absorption edge of silicon have shown higher absorption coefficient values at a given wavelength for the silicon on the degraded sapphire than for the films grown simultaneously on the control substrates. Thus, it may also be possible to monitor the quality of the epitaxial film optically. (M. T. Duffy*, P. J. Zanzucchi*, and G. W. Cullen*)

*Work performed at RCA Laboratories under NBS Contract No. 5-35915. NBS contact for additional technical information: K. F. Galloway.

5. TEST STRUCTURE APPLICATIONS

5.1. Reevaluation of Irvin's Curves

Resistivity and carrier density measurements were made on additional phosphorus-doped silicon wafers as part of the continuing work on the experimental redetermination of the resistivity-dopant density relation using previously reported procedures (NBS Spec. Publ. 400-17, pp. 13-14). Bulk resistivity was determined from measurements on test structure 3.17, collector four-probe resistor. Electron density was obtained from measurements on test structure 3.8, the MOS capacitor over collector, by the deep depletion method (NBS Spec. Publ. 400-17, pp. 8, 10-11) and from measurements on test structure 3.10, base-collector diode, by the junction capacitance-voltage (C-V) method (NBS Tech. Note 788, pp. 9-11). Electron density data from the junction C-V method were used for calculating the mobility as this method appears to be more reproducible at the present time than the MOS procedure.

The four-probe resistor and the base-collector diode are about 3 mm apart on the test pattern; this can be a source of error in wafers with large resistivity variations. In order to minimize the effects of these variations, mobility is computed from the electron density measured on a diode and the average of the resistivities measured on the two collector resistors on either side of the diode. The procedure is repeated for typically four good diodes in the same general area of the wafer, usually near the center, to arrive at an average mobility as given in table 4. Wafers were screened for radial resistivity gradients by four-probe measurements prior to processing. The maximum variation found for the wafers in the table was 6 percent between center and half-radius positions. With the averaging technique employed, the error in the mobility due to gross resistivity gradients is estimated to be no greater than about 1 percent.

The experimental mobility values were compared with those calculated from the measured electron-density by the equation of Caughey and Thomas [36] which closely fits the Irvin curve [24] for n-type silicon. These results further suggest that the Caughey-Thomas equation for mobility gives values in agreement with experiment to within ±5 percent in the resistivity range studied. (W. R. Thurber, R. L. Mattis, Y. M. Liu, and M. G. Buehler)

5.2. Mathematical Models of Dopant Profiles

The computer program developed to solve the boron redistribution problem using a finite difference algorithm (NBS Spec. Publ. 400-17, pp. 11-12) was extended to include a radiative-type boundary condition at the oxygen-oxide interface ($z = 0$):

$$-D_1 \left.\frac{\partial C_1}{\partial z}\right|_{z=z_o} = - C_p[C_1(0,t) - C_u], \qquad (7)$$

where D_1 and C_1 are the diffusion coefficient and concentration of the impurity in the oxide, C_p and C_u are specified positive constants, z_o is the coordinate of the oxide-silicon interface in the moving coordinate system (NBS Spec. Publ. 400-1, pp. 9-11) associated with the oxide. Equation (7) is believed to be more appropriate in certain

Table 4 — Preliminary Resistivity-Carrier Density Data for Phosphorus-Doped Silicon at 300 K

Slice No.	ρ, Ω·cm	n(MOS), cm^{-3}	n(jcn), cm^{-3}	μ(exp), $cm^2/V{\cdot}s$	μ(calc), $cm^2/V{\cdot}s$	percent diff[a]
A0.27Ph-2	0.276±0.005	$(2.20\pm0.05)\times10^{16}$	$(2.21\pm0.05)\times10^{16}$	1023±26	983	4.1
B0.47Ph-1	0.499±0.011	$(1.134\pm0.026)\times10^{16}$	$(1.147\pm0.045)\times10^{16}$	1093±49	1088	0.5
A2.0Ph-2	2.24±0.07	$(2.37\pm0.05)\times10^{15}$	$(2.24\pm0.03)\times10^{15}$	1244±13	1244	0.0
B3.9Ph-1	4.02±0.03	$(1.270\pm0.048)\times10^{15}$	$(1.237\pm0.007)\times10^{15}$	1255±12	1272	-1.3
B12Ph-1	13.35±0.45	$(3.87\pm0.16)\times10^{14}$	$(3.60\pm0.14)\times10^{14}$	1301±36	1306	-0.4

[a] $100\times[\bar{\mu}(\text{exp})-\mu(\text{calc})]/\mu(\text{calc})$

cases of redistribution than the boundary conditions employed previously (NBS Spec. Publ. 400-1, p. 11, eq (8)).

Ku [37] has found a closed-form solution to the uniform redistribution problem with the assumption that eq (7), with $C_p = 0$, holds at the oxygen-oxide interface. His work suggests that the solution to the uniform redistribution problem in the case of zero flux between the oxide and air should possess two qualitative features: (i) that the value of the concentration in the silicon at the moving front be independent of time and (ii) that the concentration in the oxide be spatially uniform and independent of time. The computer program reproduced both these features to several significant figures, except for a very brief period of time near t = 0. The total time taken until these qualitative features set in can be shortened by using smaller time increments, Δt. (S. R. Kraft*)

5.3. Dynamic MOS C-V Method

In a previous discussion of the MOS deep depletion method for profiling dopant density (NBS Spec. Publ. 400-17, pp. 8, 10-11), it was observed that the model for extracting the profile breaks down in the region near the surface due to the departure of the experimental capacitance-voltage curve from the ideal depletion curve. An analysis was carried out to determine how close to the surface one can make a profile measurement before the depletion model breaks down.

An experimental high frequency deep depletion curve, an ideal high frequency deep depletion curve, and a theoretical low frequency curve are illustrated in figure 14 for the case in which the flat band voltage occurs at zero applied gate voltage (i. e., work function differences, oxide charge, and interface state charge are neglected). Although a uniformly doped *p*-type substrate is assumed for purposes of illustration, the results are applicable to *n*-type substrates and can be extended to the case of nonuniform (with depth) dopant distributions.

The experimental deep depletion curve deviates from the ideal in the accumulation region, at the flat-band condition, and partly into the depletion region. However, in these regions, the experimental curve coincides with the low frequency curve. The analysis involves use of the theoretical expression [38] for the low frequency depletion capacitance based on the assumption of uniform doping in the semiconductor and calculation of the total MOS capacitance, assuming an oxide thickness, X_o. The apparent dopant density profile is then calculated using the depletion model.

The apparent profile is described by two parametric equations

$$\frac{N(X)}{N_A} = \frac{a^3}{\sinh U_f \, [2b^2 \cosh (U_f - U_s) - a^2]}, \quad (8)$$

and

$$X = - \sqrt{2} \, L_D \, \frac{b}{a} , \quad (9)$$

where N_A is the assumed constant dopant density = $2 n_i \sinh U_f$, U_f is the Fermi potential, U_s is the surface potential, $a = \sinh (U_f - U_s) - \sinh U_f$, $b = [\cosh (U_f - U_s) - \cosh U_f + U_s \sinh U_f]^{1/2}$, n_i is the intrinsic carrier density, and L_D is the intrinsic Debye length. The dimensionless potentials U_f and U_s are normalized to kT/q, where k is Boltzmann's constant, T is absolute temperature, and q is the electronic charge, and are referenced to the intrinsic Fermi potential.

In carrying out the analysis, eq (8) is solved iteratively to determine the surface potential which corresponds to the maximum permissible error in N(X). The value of X for this value of surface potential, calculated from eq (9), gives the minimum depth (X_{min}) which corresponds to the given error; the profile is more accurate at larger values of X. It turns out that, for sufficiently extrinsic material ($N_A \geq 10^{14}$ cm^{-3}), the ratio $N(X)/N_A$ is essentially independent of N_A, and that X_{min} is inversely proportional to the square root of N_A.

The results of this analysis are plotted in figure 15 which presents error curves for the minimum profiling depth as a function of the background dopant level. For example, with a background dopant density of 10^{16} cm^{-3}, one can determine the profile with error approaching 1 percent for depths near 0.14 μm; the

*NBS Mathematical Analysis Section, Applied Mathematics Division

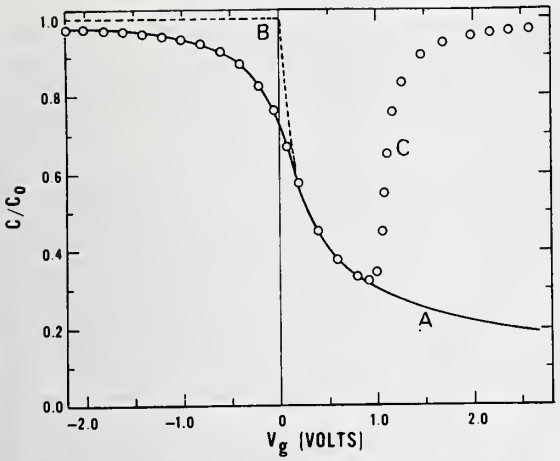


Figure 14. Capacitance-voltage characteristics of a *p*-type MOS capacitor with N_A = 10^{15} cm^{-3}, X_o = 120 nm, and C_o = 2.88 × 10^{-8} F/cm^2. °(Curve A, high frequency, deep depletion, experimental; Curve B, high frequency, deep depletion, ideal; Curve C, low frequency, theoretical.)

error approaches 10 percent for depths near 0.104 μm.

A commonly used limit for the depletion model is defined as 2λ, where λ is the extrinsic Debye length [39]. The dashed line on figure 15 indicated the error line for the 2λ limit. For any dopant density, the 2λ line corresponds to a 5.34 percent error at the indicated X_{min}. (R. Y. Koyama)

5.4. Epitaxial Layer Thickness

The MOS capacitance method for epitaxial layer thickness measurement was raised to a higher level of sophistication by employing the deep depletion MOS capacitance-voltage (C-V) method (NBS Spec. Publ. 400-17, pp. 8, 10-11). The method is basically the ramp-voltage method as it has been described (NBS Spec. Publ. 400-4, p. 51) except that instead of merely locating the capacitance, C_t, at which a break in the C-V curve occurs, the entire dopant density profile is calculated from the C-V curve. Consequently, the deep depletion method is applicable over the wider range associated with the ramp-voltage method (NBS Spec. Publ. 400-17, pp. 39-41).

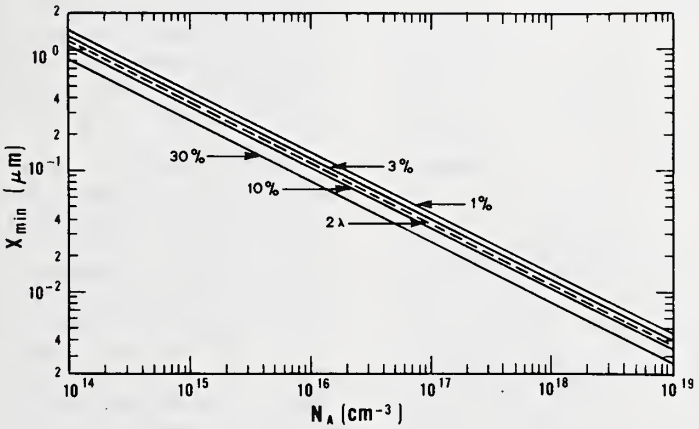


Figure 15. Error curves for minimum profiling depth as a function of background dopant density. (See text for discussion.)

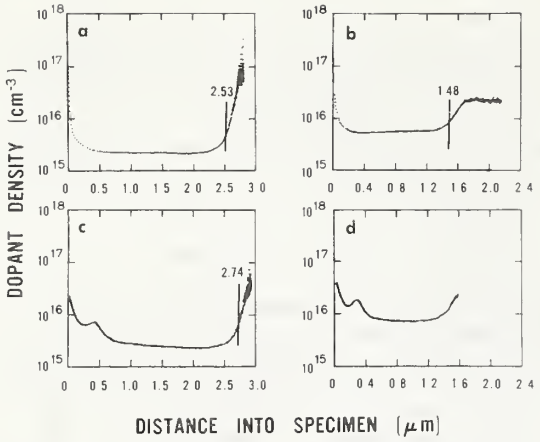


Figure 16. Dopant density profiles calculated from the deep depletion C-V characteristics of an MOS capacitor on four epitaxial layers. (a, Wafer 2303, thermal oxide dielectric; b, Wafer 2353, thermal oxide dielectric; c, Wafer 2302, negative photoresist dielectric; d, Wafer 2351, negative photoresist dielectric. The vertical bar marks the layer thickness as measured by the step-relaxation method.)

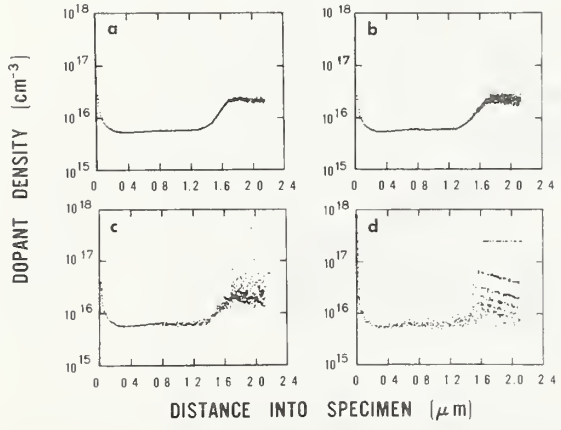


Figure 17. Dopant density profiles calculated from Wafer 2353 by signal averaging R repetitive deep depletion C-V characteristics. (a, R = 1000; b, R = 100; c, R = 10; d, R = 1.)

Typical dopant density profiles are shown for devices on four wafers in figure 16. For three of the specimens, the epitaxial thickness was measured by the step-relaxation method (NBS Spec. Publ. 400-4, p. 51) and is indicated by a vertical line which, in each case, lies within the transition region which constitutes the layer-substrate interface. The fourth specimen was not measurable by the step-relaxation method for a voltage step from +100 V to -100 V. The high dopant density calculated for shallow depths is an artifact of the measurement (sec. 5.3) and does not represent a real dopant density variation.

In two of the wafers studied, the dielectric was thermally grown silicon dioxide; in the other two, the dielectric was negative photoresist (NBS Spec. Publ. 400-12, p. 26). In obtaining these profiles, a triangular voltage waveform was applied to the devices. The capacitance of the device for the positive-going voltage could therefore be observed in addition to the capacitance for negative-going voltage. For the wafers having thermal oxide dielectric the capacitance was nearly a single-valued function of voltage regardless of the voltage slope. For the wafers having negative photoresist dielectric, however, there was a significant dependence on the slope. With the negative photoresist dielectric there was also an additional anomaly in the C-V curve at shallow depths. Because of these effects, the profiles measured with oxide dielectric are believed to be more accurate than those measured with photoresist dielectric, but the problems do not appear to affect the determination of the epitaxial layer thickness.

Because the equation for calculating the dopant density includes a derivative, precautions must be taken to eliminate excessive scatter from the profiles. To obtain the profiles shown in figure 16, the derivative was calculated from a formula which effectively averages over a range of 16 data points. In addition, signal averaging was carried out such that the C-V curve which was analyzed represented the average of 1000 repetitive responses. The need for signal averaging was noted by calculating profiles in which 1000, 100, 10, and 1 responses were used to construct the average C-V curve. Such profiles are shown in figure 17 for the specimen with the profile shown in figure 16b. Note that the portions of the profile in the transition region and substrate suffer the greatest degradation as averages of fewer responses are taken. The non-random nature of

the scatter for the case of no signal averaging (single response) is a result of the 10-bit resolution of the capacitance measurement and the manner in which the computer operates on arrays.

Examination of these profiles graphically illustrates the problem which has been encountered in attempting to correlate measurements of epitaxial layer thickness by different methods. The transition region has a finite width and different methods identify different points in the transition region as the location of the boundary between layer and substrate. Hence, the agreement between methods depends on the nature of the transition region, especially for the case of very thin layers where the width of the transition region may be comparable with the layer thickness. The present procedure may be of use in developing suitable criteria for definition of the location of the boundary or in controlling the profile shape in the transition region. (R. L. Mattis)

5.5. Bias-Temperature Stress Test

A preliminary set of measurements was carried out as the initial phase of an effort to develop improved understanding of the application of the bias-temperature stress test to the characterization of oxide films. The oxides used in this phase of the study were thermally grown on 2.0-in. (51-mm) diameter *n*-type silicon wafers with room temperature resistivity in the range 5 to 10 Ω·cm and <100> surfaces. Oxidation at 1000°C for 100 min in dry oxygen resulted in an oxide film approximately 80 nm thick. Following the oxidation the wafers were annealed in dry nitrogen at 1000°C for 20 min. Aluminum was e-beam evaporated over the oxide to a thickness of about 500 nm, further annealed in dry nitrogen at 500°C for 15 min, and patterned with the Metal mask of Test Pattern NBS-3 (NBS Spec. Publ. 400-12, pp. 19-22). The entire backside of the wafer was metallized with antimony-doped gold.

The test pattern mask contains four 15-mil (0.38-mm) diameter capacitor gate electrodes (test structures 3.2, 3.3, 3.8, and 3.19); the test pattern is repeated every 200 mils (5.1 mm) in both directions across the wafer. The primary measured quantity for the investigation is the flat-band voltage, V_{FB}, of MOS capacitors determined by the high frequency capacitance-voltage (C-V) technique (NBS Spec. Publ. 400-4, pp. 34-37). The general procedure for the study of a given wafer was to measure the capacitance as a function of voltage for a number of 3.8 test structures in the "as-processed" condition; at the least, the 16 structures in the central 4 by 4 array of patterns were measured. Following this, the wafer was subjected to one or more of the following treatments:

positive bias-temperature (BT) stress — heat wafer to 300°C on hot-cold stage (NBS Spec. Publ. 400-4, pp. 39-40); contact the grounded probe to the gate electrode; apply +10 V to probe for 10 min; cool wafer to room temperature with the grounded probe still contacting the gate electrode.

negative bias-temperature (BT) stress — heat wafer to 300°C on hot-cold stage; contact the grounded probe to the gate electrode; apply -10 V to probe for 10 min; cool wafer to room temperature with the grounded probe still contacting the gate electrode.

heat treatment — heat wafer to 300°C on hot-cold stage for 20 min in dry nitrogen ambient with no probe contact.

electron irradiation — expose, without applying bias, a portion of the wafer to a dose of 10^4 Gy (10^6 rads(Si)) in the scanning electron microscope using a beam energy of 20 keV, a beam current of 0.25 nA, and an exposure time of 10^3 s.

Six lots of several slices each have been fabricated by the processing facility with no special treatment of the furnace. As an example of preliminary results, figure 18 summarizes the flat-band voltage measurements on the four wafers of the fifth lot. Each bar represents the span of the flat-band voltages for the measured number of devices shown in parentheses and is labeled with the condition of the device. To begin with, the flat-band voltages of the as-processed wafers fell in the region from -0.21 to -0.27 V. Three of the four wafers had flat-band voltages for the 16 measured devices tightly grouped within ±10 mV; these were subjected to additional study. It should be noted here that since the gate metal is aluminum, the intrinsic shift of the flat-band voltage due to the metal-semiconductor contact potential difference is about -0.3 V [40] for the specimens studied. Therefore, in the as-processed condition, these devices appear to have a net negative charge in the interface or oxide region of the capacitors.

Wafer 5A was subjected to negative BT stress, positive BT stress, and heat treatment. The

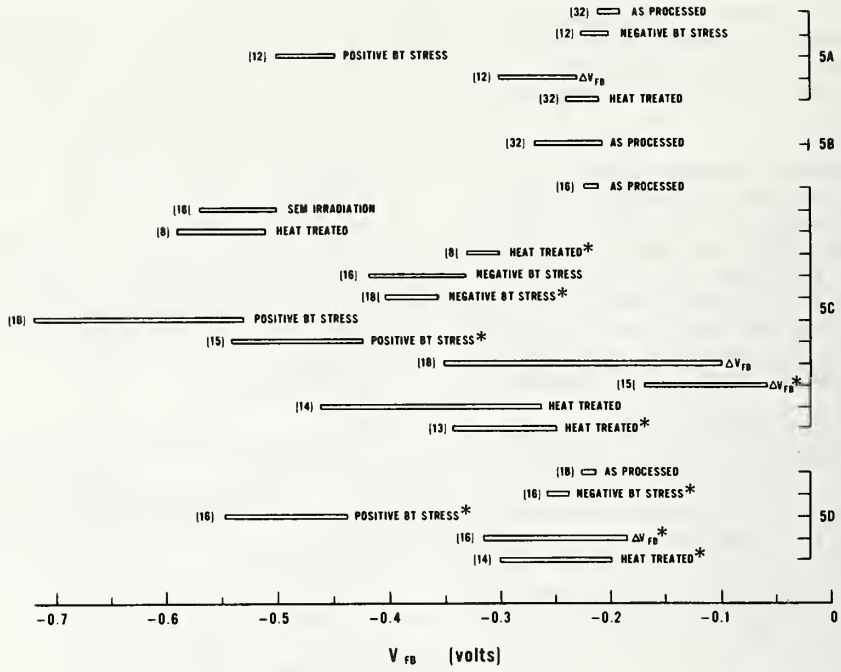


Figure 18. A summary of flat-band voltage measurements on MOS capacitors at room temperature following various treatments. (See text for explanation.)

presence of positive mobile ion species is readily revealed by the negative shift of the flat-band voltage under positive BT stress. In this case there was a slight negative shift with the negative BT stress as well. The net flat-band voltage shift (ΔV_{FB}) indicates mobile ion contamination for these devices ranging between 6.7 and 8.7 $\times$ 10^{10} cm^{-2}. Subsequent heat treatment of the wafer caused V_{FB} to drift back toward the as-processed condition but without full recovery.

Wafer 5C was subjected to electron irradiation, heat treatment, negative and positive BT stress, and a second heat treatment. There are two separate subsets of devices. One subset contained 16 devices which were measured in the as-processed condition in the usual way. The second subset contained 16 devices which were not measured in the as-processed condition; the devices in this subset, consequently, had not been probed prior to the electron irradiation. The data from the second subset are marked with an asterisk in the figure. Electron irradiation caused a large negative shift of the flat-band voltage and simultaneously introduced a high density of interface states in the subset measured after irradiation. Heat treatment after irradiation appeared to remove the interface states; the flat-band voltage for previously measured devices shifted to slightly more negative values whereas those measured for the first time after processing, irradiation, and heat treatment formed a tighter group at smaller flat-band voltages. With negative and positive BT stress, both sets of devices behaved similarly although the second subset of devices was affected less and always formed a tighter grouping. The net flat-band voltage shift resulting from negative and positive BT stress indicate ionic contamination ranging from 2.9 to 10.2 $\times$ 10^{10} cm^{-2} and from 1.7 to 5.0 $\times$ 10^{10} cm^{-2} for the first and second subsets, respectively. After subsequent heat treatment of the wafer the flat-band voltage relaxed toward the as-processed value.

Wafer 5D was treated similarly to wafer 5A, but the devices measured after BT stressing were different from those measured in the as-processed condition. Although the flat-band voltage showed larger spreads, the behavior was essentially the same as that of wafer 5A.

These results are presented only to be indicative of the kind of information which might be expected from study of the BT stress test; they are too preliminary to warrant detailed

analysis and definitive conclusions. It should be noted that the use of the BT stress test as an indicator of mobile ion contamination assumes that the mobile ions merely shift the C-V curve in an amount proportional to the net charge moved to the interface. In general, however, this assumption is an oversimplification. Interface states can distort the C-V characteristic which can cause error in the determination of the flat-band voltage. This is particularly true of devices which have been electron irradiated and those which have high mobile ion contamination.

(R. Y. Koyama and D. A. Maxwell)

5.6. Extended Range MIS C-V Method

The metal-insulator-semiconductor (MIS) capacitance-voltage (C-V) technique is widely used to determine such parameters as semiconductor dopant density, flat-band voltage, and interface state density. A basic limitation of the technique has been the accuracy with which the semiconductor depletion capacitance, C_s, could be determined. Generally for reasonable accuracy, it was necessary that the ratio of C_s to C_I, the insulator capacitance, be ten or less. Recently, modified instrumentation has been developed [41] so that accurate measurements can be made when the ratio C_s/C_I is 100 or more. The inherent limit no longer depends on this ratio but on the noise level of the capacitance measurement. This modified measuring instrument then allows the use of the C-V technique on MIS structures with thick insulator layers.

Among the potential applications of the modified instrument are the characterization of the silicon-glass interface under a thick (50 μm) layer of glass, the determination of the flat-band voltage under a thick field oxide on an LSI chip, and the characterization of silicon on sapphire and the silicon-sapphire interface by using the sapphire substrate as the insulator in an MIS capacitor. The original modified instrument [41], although suitable for demonstration purposes and laboratory application, requires improvement and additional modification before it will be suitable for general use. This task was undertaken to develop improved bias protection circuitry to prevent damage to the measurement equipment in case of catastrophic dielectric failure of the specimen under high bias, to develop a high-voltage power supply with a linear sweep capability to facilitate use of the instrument in applications where the capacitance is a function not only of the applied voltage but of the sweep rate as well, to develop an improved specimen holder with an integral safety interlock system, and to further demonstrate the applicability of the method.

The original modified instrument [41] had a potential problem when very high bias voltages were applied to the specimen under test. If the specimen capacitor developed a short circuit, a large part of the applied bias voltage was transferred to the capacitance meter, thus damaging it. To prevent this damage, a bias protection circuit was developed that prevents voltage excursions beyond the ±200 V limit of the capacitance meter. However, the use of the circuit limits the range of capacitance that may be measured without introducing excessive added error. The first version of the circuit limited the measured capacitance to the range 0 to 40 pF if the added error introduced by the circuit was to be kept below 1 percent. To overcome this limitation, the values of the components in the previous version of the circuit were optimized. The resulting improved bias protection circuit has been tested to ±9600 V under repeated breakdown conditions. The added error in the range of measured capacitance 0 to 140 pF is less than 1 percent.

The modified technique [41] often requires the application of high bias voltage to the capacitor sample to be measured. When this bias voltage exceeds some threshold value (typically 3 to 5 kV), there exists the danger of breakdown along the insulator surface or at an electrode edge. One method for prevention of this breakdown [42] is to coat the surface and electrode edge with a grease-like silicone material; this is very effective but is messy, time-consuming, and inconvenient. It has been found that if an insulating silicone rubber toroid, having appropriate properties, is pressed over the specimen surface including the electrode edge, breakdown can be effectively prevented at applied bias voltages up to ±10 kV. The surface of the rubber in contact with the specimen must be very smooth, and the rubber itself must be very resilient. It is also important that the rubber contain no voids in the vicinity of the surface (in contact with the insulator) and that it have both a very high resistivity and a low dissipation factor.

Other instrumental improvements, including the power supply with linear sweep capability interlock, are being constructed. Initial evaluations have been made of the measurement

technique as a diagnostic tool for characterizing the silicon-sapphire interface and for monitoring changes at or near the interface resulting from high-temperature processing steps and high-energy irradiation in connection with other projects. In these studies changes in the charge density at the silicon-sapphire interface due to oxidation and annealing steps and to electron irradiation were observed directly. (A. M. Goodman*)

*Work performed at RCA Laboratories under NBS Contract No. 5-35912. NBS contact for additional information: R. Y. Koyama.

6. MATERIALS AND PROCEDURES FOR WAFER PROCESSING

6.1. Ion Implantation Parameters

This task was undertaken to develop and disseminate to the semiconductor device and integrated circuit industry practical information and experimental data to assist in improving the design and fabrication of ion-implanted doping profiles. Some of the important aspects of profile control still needed are accurate knowledge and control of dose and of ion range and straggle (or standard deviation). This control of implanted doping profiles in production is important because implantation is known to be capable of much greater control of doping profiles than diffusion, and it is possible to construct implanted profiles which cannot be obtained by diffusion. However, this potential superiority of implantation can be lost to the practical world of device and circuit fabrication unless adequate knowledge and control of dose and range and straggle are provided. Initial measurements have been made of range and range straggle of boron and phosphorus implanted into 100 Ω·cm silicon of the opposite conducting type in a production-type implantation system. Doses were approximately 1.5×10^{12} cm^{-2} and implantation energies were varied from a lower limit that gives a range of about 150 nm to an upper limit of 600 keV. After implantation, the wafers were annealed at 900°C for 30 min in argon. The results for profiles implanted with the beam tilted 7 deg from the <100> direction generally agreed with the results of calculations [29,43] based on LSS theory.

The range, R_p, and range straggle, ΔR_p, were determined from measurements of the dopant profile made on reverse-biased Schottky barrier diodes by means of an automatic capacitance-voltage technique described by Gordon *et al.* [44]. Schottky barriers were employed because with them contact can be made to a wafer without disturbing the implanted profile. The barrier is formed by evaporating a metal film (aluminum for *p*-type implanted surfaces and gold for *n*-type) about 100 nm thick through a metal mask which defines dots varying in size from 0.1 to 0.15 mm in diameter on the front (implanted) surface of the wafer. A low resistance contact is made on the backside of the wafer by low energy implantation of a suitable dopant.

(R. G. Wilson*)

6.2. Passivation Integrity

This task was undertaken to develop techniques for evaluating the integrity of passivation overcoats on metallized integrated circuits, specifically practical techniques to detect localized structural defects and to measure their population density. The techniques are intended to be suitable for routine quality control by manufacturers, to be applicable both to IC devices in wafer form and to individual pellets, and to allow estimation or quantization of the number of localized structural defects (such as pinholes and microcracks) per unit area in the oxide, glass, or nitride overcoat. Essentially nondestructive methods, which do not damage areas that are defect-free, are preferred.

Three types of promising methods are being explored, developed, and assessed to allow comparison: (1) selective chemical etching to visualize defects, (2) electrophoretic defect decoration, and (3) electrostatic corona charge decoration of defects. In the initial phase of the work test structures have been designed and fabricated, specialized instrumental equipment has been set up, and investigation of the three methods has been started.

(W. Kern† and R. B. Comizzoli†)

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*Work performed at Hughes Research Laboratories under NBS Contract No. 5-35891. NBS contact for additional information: D. C. Lewis.

†Work performed at RCA Laboratories under NBS Contract No. 5-35913. NBS contact for additional information: T. F. Leedy.

7. PHOTOLITHOGRAPHY

7.1. Optical Imaging for Photomask Metrology

Line widths in the micrometer range are commonly measured with a microscope equipped with a micrometer eyepiece. In this measurement it is not the physical object or geometrical line width which is measured, but instead it is the magnified image of the line. Therefore, the accuracy of these measurements is strongly dependent on the quality of the line image. This quality depends on the aberrations of the imaging lens, the focus or amount of defocus present, and the spatial coherence of the light [45]. The spatial coherence is a measure of the phase correlation of the light in a plane perpendicular to the direction of propagation. The degree of correlation is a measure of the ability of the light to manifest interference effects. It ranges from a value of 1 for coherent light where the phase at each point in the perpendicular plane is correlated with the phase at any other point and interference occurs, to a value of 0 for incoherent light where the phase at any point is completely independent and interference is absent. The degree of correlation is a function of the type of illumination, the path length, and the numerical aperture of the focusing lens element in the optical system.

A theoretical investigation was begun to determine quantitatively the effects of coherence on the image of two parallel opaque lines on a transparent background and its inverse. This is the simplest statement of the problem that must be solved to determine the effects of coherence on line width measurements. The first part of this investigation considers a single line and a diffraction limited lens system. It addresses two questions:

> What is the minimum size of a single opaque line on a transparent background that can be recognizably imaged as a line at any given quality level? and
>
> How can this quality level be specified?

The first of these questions was approached by calculating the intensity profile of the image of an ideal line for both the case of spatially incoherent light and the case of spatially coherent light. Here an ideal opaque line is defined as having zero percent transmittance across its width and a 100 percent transmittance elsewhere. The intensity profiles of the image of an object are formally written [46] for the incoherent case as:

$$I = \iint \tilde{h}(x,y)\ \tilde{h}^{*}(x,y)\ U_g(x,y)\ U_g^{*}(x,y)\ dxdy,$$

and for the coherent case as:

$$I = \left| \iint \tilde{h}(x,y)\ U_g(x,y)\ dxdy \right|^2,$$

where $U_g(x,y)$ is the complex amplitude of radiation from the object, and $\tilde{h}(x,y)$ is the complex response of the optical system.

Expressions for these functions were derived with the assumption that the lens was diffraction-limited with an impulse response of sin x/x for the one dimensional case. The characteristic width of this function, taken to be the distance between the first node points on each side of the line x = 0, is a measure of the smallest dimension that can be resolved by the lens. The expressions for the intensity profiles for both illumination cases were derived in terms of the ratio, A, of object line width, 2b, to the width of the impulse response; the numerical aperature, NA; the wavelength of the light, λ; the magnification of the lens, m; and the image coordinate, β.

The expression for the image intensity profile for the coherent case is:

$$I(\xi) = \left| 1 - \frac{2}{\pi}\left\{ \mathrm{Si}\left[2\pi\left(\xi + \frac{A}{2}\right)\right] - \mathrm{Si}\left[2\pi\left(\xi - \frac{A}{2}\right)\right] \right\} \right|^2,$$

and for the incoherent case is:

$$I(\xi) = 1 - \frac{1}{\pi}\left\{ \mathrm{Si}\left[4\pi\left(\xi + \frac{A}{2}\right)\right] - \mathrm{Si}\left[4\pi\left(\xi - \frac{A}{2}\right)\right] - \frac{1-\cos\left[4\pi\left(\xi + \frac{A}{2}\right)\right]}{4\pi\left(\xi + \frac{A}{2}\right)} + \frac{1-\cos\left[4\pi\left(\xi - \frac{A}{2}\right)\right]}{4\pi\left(\xi - \frac{A}{2}\right)} \right\},$$

where $\xi = \beta\ \mathrm{NA}/\lambda m$ and $\mathrm{Si}[x] = \int_0^x (\sin \nu/\nu)\, d\nu$.

These functions are plotted in figure 19 as a function of the parameter ξ for the indicated values of A. In all calculations the wavelength was taken as 500 nm. For illustrative purposes this figure is divided vertically through the center, with the edges of the ideal image intensity profile (the

image profile that is an exact magnification of the object profile) located at $\xi = \pm 1.0$. The intensity profiles for incoherent light are plotted on the left side of the figure and the profiles for coherent light on the right side. Since the profiles are symmetrical about the center of the figure, the complete line profile may be visualized by mirroring any particular profile through the figure center. The profiles I-1 and C-1 in the figure show a badly degraded image and are indicative of the images that result when a line whose width is somewhat smaller than the resolution limit of the lens is imaged. The other curves of this figure represent image intensity profiles for wider lines and illustrate the image edge profiles becoming sharper as the line widths become appreciably larger than the impulse response of the lens.

With the exception of the curves I-1 and C-1 in figure 19, all of the image intensity profiles cross the ideal image edge at nearly the same point for each illumination case. For the incoherent case this point is at approximately 50 percent transmittance. This is a relatively easy intensity level to distinguish visually. However, the image intensity profiles for the coherent case cross the ideal image edge at 25 percent transmittance, and this cannot be consistently detected visually.

Which profiles are actually present when measuring a line width with a microscope? It is not uncommon to observe "ringing" near the line image edge in a microscope (bright and dark bands near the image edge). Such "ringing" is shown for the case of coherent illumination by the oscillations of the image intensity profiles about 100 percent transmittance, while this phenomenon is absent for the incoherent case. Thus, it may be concluded that an appreciable amount of illumination coherence is present under normal microscope operating conditions.

To establish a quantitative measure of the image quality, the RMS differences between the spectra of the image intensity profiles and the ideal intensity profiles were evaluated. This difference is arbitrarily defined as

$$D = \left[\frac{1}{P}\int_0^P \left\{F[I_i(\xi)] - F[I_a(\xi)]\right\}^2 d\xi\right]^{\frac{1}{2}}$$

where $F[I_i(\xi)]$ is the spectrum of the ideal

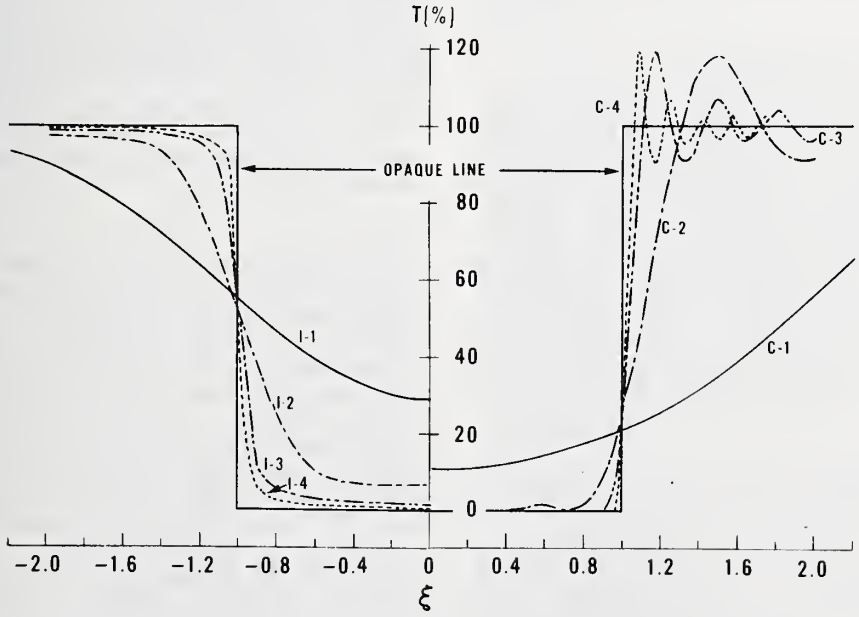


Figure 19. Image intensity profiles of an opaque line on a transparent background for incoherent and coherent illumination. (See test for discussion of curves.)

Table 5 — Object Line Widths and Corresponding RMS Differences Determined from the Curves of Figure 19.

Curve	A	% RMS	Object Line Width for NA of 0.25	0.5	0.65	0.85
Coherent Illumination:						
C-1	0.4	10	0.7 μm	0.4 μm	0.3 μm	0.2 μm
C-2	2.2	5	4.4	2.2	1.7	1.3
C-3	6.3	2	12.5	6.3	4.8	3.7
C-4	12.3	1	24.7	12.3	9.5	7.2
Incoherent Illumination:						
I-1	0.4	10	0.9 μm	0.4 μm	0.3 μm	0.2 μm
I-2	1.5	5	2.9	1.5	1.1	0.9
I-3	4.9	2	9.7	4.9	3.7	2.9
I-4	9.8	1	19.5	9.8	6.3	5.7
Impulse Response Width:			2.0 μm	1.0 μm	0.76 μm	0.59 μm

image intensity profile, $F[I_a(\xi)]$, is the spectrum of the calculated or actual image profile, and P is the interval of integration.

The spectrum of the image, $F[I(\xi)]$, is a function in the spatial frequency domain (line cycles per unit length). Since a lens forms an image by transmitting information of different spatial frequencies, a comparison of the spectrum of the image with that of the object should provide a quantitative measure of the image quality. Values of the percent RMS differences are listed in table 5 as functions of values of the parameter A. For each of several numerical apertures commonly found in microscope objectives, table 5 also lists the approximate width of the impulse response and the corresponding object line widths. (R. E. Swing*)

An investigation of the degree of coherence of the illumination at the object plane of a microscope with diffraction limited lenses and its effect on the intensity profile of a single edge was begun. The degree of coherence is a function of the illumination source and of both the condenser and objective numerical apertures. Light produced by a large incandescent source and focused by a lens is completely incoherent only when the source-to-lens distance is very small and the angle from the source subtended by the lens diameter is very large. As the source-to-lens distance increases, the coherence of the light increases. The degree of coherence of the illumination affects the shape of the image intensity profile and its displacement from the step function edge position that would be predicted by geometric optical considerations only.

Figure 20 (after Welford [47]) compares several theoretically calculated edge image intensity profiles. Curve A represents the edge image intensity profile for a large incandescent source and uniformly filled, matched condenser and objective lenses with numerical apertures of 0.65. Curve B represents the profile for incoherent illumination corresponding to an infinitely large condenser aperture. Curve C represents the profile for coherent illumination corresponding to an infinitely small condenser aperture. The ideal edge is shown by Curve D. These curves are all normalized to converge to the 100 percent intensity level at large distances from the edge.

Several phenomena are illustrated in this figure. The edge image intensity profile for incoherent illumination (Curve B) has zero displacement from the ideal edge position at the 50 percent intensity level. This is the

*NBS Optics and Micrometrology Section, Mechanics Division.

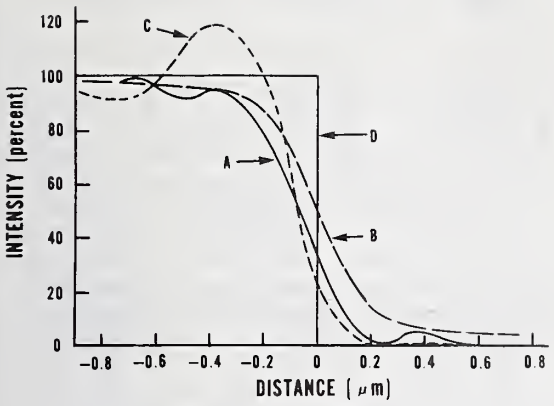


Figure 20. Image intensity profiles of a single edge viewed by light of wavelength λ = 500 nm. (A, matched numerical apertures of 0.65; B, incoherent illumination; C, coherent illumination; D, ideal edge.)

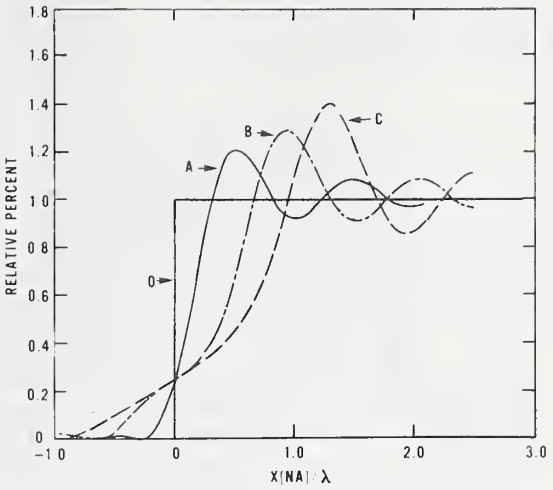


Figure 21. Image intensity profiles of a single edge viewed by coherent illumination with varying defocus. (A, no defocus; B, $\frac{1}{2}\lambda$ defocus; c, 1λ defocus; D, ideal edge.)

intensity level at which the edge is usually located by visual observations. On the other hand a displacement of 0.08 μm is observed at the 50 percent intensity level for the edge profile obtained for matched numerical apertures (curve A). The displacement distance, x, from the ideal edge may be found for pairs of matched apertures from the relation

$$x = \frac{0.65}{NA} \quad x_f \quad ,$$

where x_f is the x-coordinate appropriate to curve A in figure 20.

Ringing is shown in curve A by the oscillations between the 90 and 100 percent intensity levels. These appear in the microscope image as alternate light and dark bands parallel to the edge image. This observed ringing indicates that the illumination has a high degree of coherence. Also, the edge intensity profile produced with matched numerical apertures is closer to the intensity profile for coherent illumination than it is to the intensity profile for incoherent illumination.

Focus affects the shape of the edge intensity profile and is subjectively determined by selecting the object-to-lens distance which produces the sharpest image. Theoretical calculations of the effect of defocusing on intensity profiles were made for coherent illumination. The amount of defocus, Δ, is the longitudinal displacement of the actual object plane from the object plane predicted by geometric optics (the geometric focus). In making the calculations it is more convenient to consider the quantity $n\lambda$, the maximum deviation, in multiples of wavelength, of the actual wave front from the ideal spherical wave front, which is related to Δ by

$$n\lambda = \Delta \ (NA)^2/2.$$

Figure 21 shows image intensity profiles for various amounts of defocus. It may be seen from this figure that, due to the ringing, the contrast between the edge and the first dark band is greater for small amounts of defocus than for the proper focus. Consequently, an observer may easily choose a defocused microscope setting as the correct or best focus because of the increased sharpness produced by a small amount of defocusing. If this should occur, the location of the edge would be chosen from an image intensity profile that is appreciably degraded and would be displaced significantly from the geometric image. The tendency for an observer to choose an incorrect focus and degraded edge profile can be further appreciated by noting that a 1λ defocus for λ = 0.5 μm and an objective lens with NA = 0.65 corresponds to a defocus displacement Δ of only about 2.4 μm (or about 0.1 mil).

The image quality is also degraded by spherical aberration of the objective lens. This aberration causes light rays passing through the outer portions of the lens to be focused at a different distance from the lens than

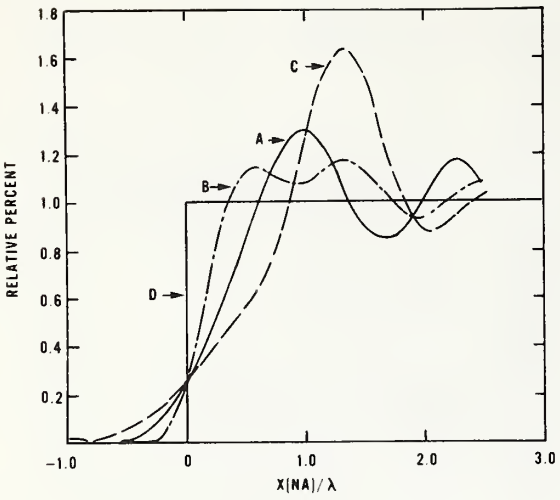
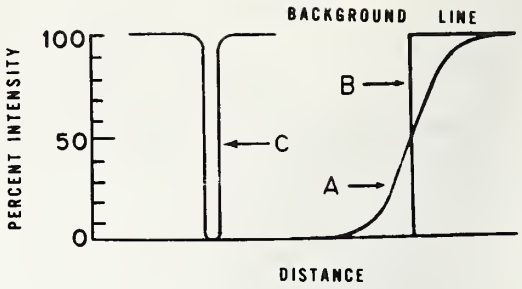
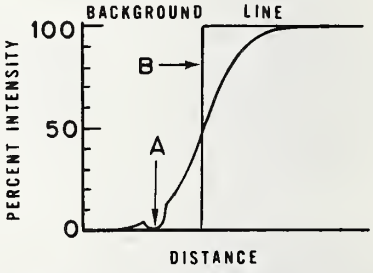


Figure 22. Image intensity profiles of a single edge viewed by coherent illumination with 1λ spherical aberration and varying defocus. (A, no defocus; B, -1λ defocus; C, -2λ defocus; D, ideal edge.)

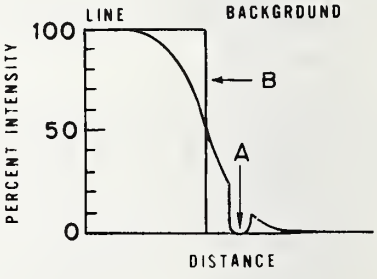
rays passing through the center portions of the lens and is present to some degree in all optical systems. Spherical aberration is greater when microscope objectives are used at the wrong tube length or when objectives and eyepieces of different types or manufacture are used together. The effects of this aberration may be partially compensated by introducing an equivalent amount of defocus; when this is done a sharper image is produced. Spherical aberration is also described in terms of nλ, where nλ now refers to the maximum difference, in multiples of wavelength, between the aberrated wavefront and the ideal spherical wavefront produced by a diffraction limited lens. Figure 22 shows calculated edge image intensity profiles for coherent illumination and an objective lens with a spherical aberration of 1λ and different focus settings. This figure shows that a sharp image intensity profile is produced when the amount of defocus suitably compensates the spherical aberration; this focus is usually called the best focus. This figure also shows that the contrast between the edge image and the bands produced by ringing increases as the defocus is increased further. This illustrates the difficulty of visually choosing the correct



a. Image intensity profiles: A, single edge as viewed by incoherent illumination; B, ideal edge; C, filar eyepiece crosshair.



b. Superposition of the edge and filar eyepiece crosshair image intensity profiles showing the apparent location of the edge (A) and the ideal edge (B) as the crosshair is traversed from a dark region to a bright region.



c. Superposition of the edge and filar eyepiece crosshair image intensity profiles showing the apparent location of the edge (A) and the ideal edge (B) as the crosshair is traversed from a bright region to a dark region.

Figure 23. Line edge location with a filar eyepiece.

focus because of the temptation to adjust the microscope for the highest contrast.

These edge image intensity profiles were used in a preliminary analysis of line width measurement errors that one might expect when using microscopes equipped with a filar or image shearing eyepiece or using equipment that locates the edge by electronically processing the edge image intensity profile. Calculations were made for a transparent line on an opaque background, viewed by 0.55-μm transmitted light. Image intensity profiles for incoherent illumination, coherent illumination, matched numerical apertures, defocus with coherent illumination, and spherical aberration with defocus and coherent illumination were considered. The optical system consisted of a 12.5X eyepiece and a 40X, 0.65 numerical aperture objective. Since the model is based on the image intensity profile of a single edge, the results are applicable only for lines 20 μm or more wide. For narrower lines viewed with this system, it may not be assumed with confidence that the diffraction effects occurring at one edge do not interfere with those at the other edge.

Consider first measurements with a filar eyepiece. The intensity profile of an ideal edge for incoherent illumination and the image intensity profile that results in a filar eyepiece with the cross hair located in the image plane are illustrated in figure 23a. When the cross hair is traversed from the dark region to the bright region, the edge position is taken as the center of the cross hair image when the edge of the cross hair nearer to the bright region just begins to cover the bright region as illustrated in figure 23b. For illustrative purposes, the threshold visibility point is arbitrarily taken at the 10-percent intensity level. Thus, the edge is located by the filar eyepiece at the value of the coordinate corresponding to the 10-percent intensity level minus one-half the cross hair width. When the cross hair is traversed from the bright region to the dark region, a bright line begins to appear on the dark side of the cross hair image as shown in figure 23c. The edge position is taken as the position of the center of the cross hair image when this bright line is just no longer visible. In this case the edge is also located by the filar eyepiece at the value of the coordinate at the 10-percent intensity level minus one-half the cross hair width. If, when the measurement is made, the image of the cross hair is traversed across the line in one direction (as is usually the case), the measured line width is equal to the difference of the coordinates of the two 10-percent intensity level positions.

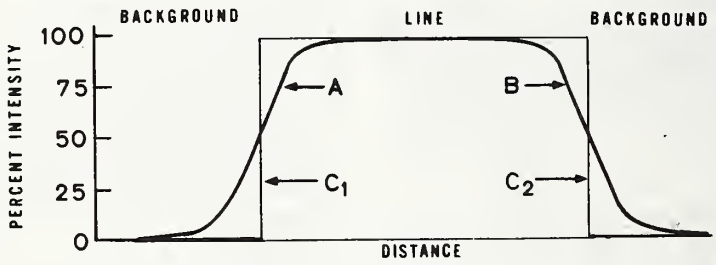
An image shearing micrometer eyepiece positions the images of the two edges of a line side by side so that one of the edge images can be traversed across the other. The image intensity profiles of a left and right edge with the ideal edge located at the 50 percent intensity level are shown in figure 24a for the case of ideal symmetric edges. As these two images are superimposed by the image shearing eyepiece, the intensity profiles add. As the images cross, the bright region between them (1) narrows to a bright line, as shown in figure 24b, which corresponds to the two edge profiles crossing at the 75-percent intensity levels, (2) disappears when the two edge profiles cross at the 50-percent intensity levels, and (3) finally changes to a narrow dark line, as shown in figure 25c, which corresponds to the two edge profiles crossing at the 25-percent intensity levels. The line edge location is generally picked when the two edge images touch with neither a bright line nor a dark line existing between the two images. For symmetric edges this criterion results in locating the edge at the 50-percent intensity level and no measurement error results if the illumination is incoherent. If the ideal edge location corresponds to some other intensity level, as would be the case for coherent or partially coherent illumination, there will be some error in locating the edge.

Very explicit criteria may be applied consistently to determine the edge location with electronic processing and analysis of the image intensity profile. One of these criteria is to locate the edge at the 50-percent image intensity level which results in locating the edge at the same position as the image shearing micrometer eyepiece. Another of these criteria is to locate the edge at the position of maximum image intensity profile slope. This criterion results in locating the edge position at the 50-percent intensity level only for the case of incoherent illumination.

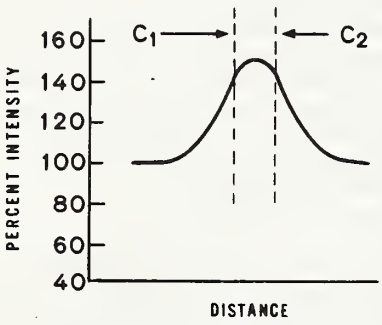
Results of calculations of measurement error, based on the above criteria, are listed in table 6. The apparent width is greater than the actual width when the error is positive and smaller when the error is negative. If the illumination is reflected rather than

Table 6 — Line Width Measurement Errors for a Transparent Line (20 μm or Wider) on an Opaque Background Viewed with 550 nm Illumination

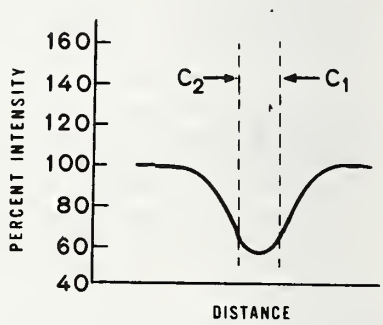
Illumination Condition	Filar Eyepiece	Image Shearing Eyepiece or 50 percent Intensity Level	Maximum Slope
Incoherent Illumination — Geometric Focus	+0.56 μm	0.0 μm	0.0 μm
Matched Numerical Apertures — Geometric Focus	+0.27	-0.17	-0.23
Coherent Illumination — Geometric Focus	+0.16	-0.19	-0.25
— ±0.65 μm from Geometric Focus (±λ/4 Defocus)	+0.25	-0.34	-0.46
— ±1.3 μm from Geometric Focus (±λ/2 Defocus)	+0.59	-0.66	-1.00
— +λ/4 Spherical Aberration	+0.17	-0.14	-0.28
— +λ/4 Spherical Aberration, -λ/4 Defocus	+0.14	-0.17	-0.30
— +λ/4 Spherical Aberration, -λ/2 Defocus	+0.20	-0.09	-0.30
— +λ/2 Spherical Aberration	+0.16	-0.19	-0.25
— +λ/2 Spherical Aberration, -λ/2 Defocus	+0.30	+0.02	-0.68
— +λ/2 Spherical Aberration, -λ Defocus	+0.41	+0.14	-0.97



a. Image intensity profiles of opposite line edges viewed with incoherent illumination illustrating the images prior to superpositioning them over each other with the image shearing eyepiece: A, left edge; B, right edge; C_1, left ideal edge; C_2, right ideal edge.



b. Overlap of image intensity profiles A and B with a bright band between the two light images corresponding to locating the line edge at the 75-percent intensity level.



c. Overlap of image intensity profiles A and B with a dark band between the two light images corresponding to locating the line edge at the 25-percent intensity level.

Figure 24. Line edge location with an image shearing micrometer eyepiece.

transmitted or if the line is opaque on a transparent background, the sign of the error is reversed.

It should be stressed that these results are for the case of wide lines where the two edges may be treated independently. It should also be noted that in practice higher numerical aperture objectives are frequently used in line-width measurements although they are not used to full capacity due to a lower numerical aperture of the condenser. At best they are illuminated non-uniformly which reduces their resolving power. This may also be true of the 0.65 numerical aperture considered here. Many other factors which affect line-width measurement by narrowing or broadening the line image were not considered. These factors include the properties of the photomask materials, electronic clipping and edge enhancement, and the variability of the human eye. The method of calibration of the measuring instrument also was not considered.

(D. Nyyssonen†)

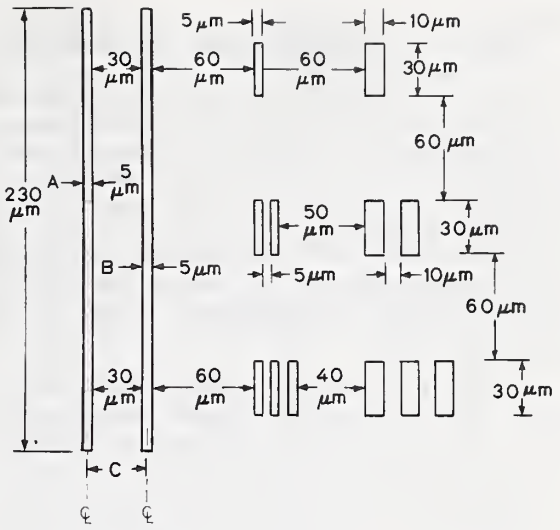


Figure 25. Interim chromium-on-glass line-width measurement artifact with transparent lines on an opaque background. (All dimensions are nominal, ±0.25 μm.)

7.2. Calibration Standards for Photomask Metrology

Attempts to fabricate the previously described artifact (NBS Spec. Publ. 400-17, pp. 37-38), intended for use in establishing standards for line width measurements in the 1- to 10-μm range, have been thus far unsuccessful. This measurement artifact was to resemble a hard surface photomask. The pattern was to be etched in a chromium film deposited on a glass substrate coated with a tin oxide film. The tin oxide film is optically transparent and was to provide a conductive substrate in order to enable the artifact to be used in a scanning electron microscope (SEM). On every attempt to fabricate this artifact, a reaction occurred between the chromium and tin oxide resulting in an unacceptable loss of opacity in the chromium. The reaction has not been identified.

An alternative approach to producing a measurement artifact was evaluated. A mask of the design shown in figure 25 consisting of transparent lines on an opaque background was obtained. These lines were scribed on a glass plate coated with chromium to a thickness of 50 to 100 nm. The patterned artifact was then overcoated with approximately 50 nm of carbon to enable its use in the SEM. This carbon layer does not affect the transparency of the artifact and provides the necessary conductive coating.

(J. M. Jerke* and D. B. Novotny)

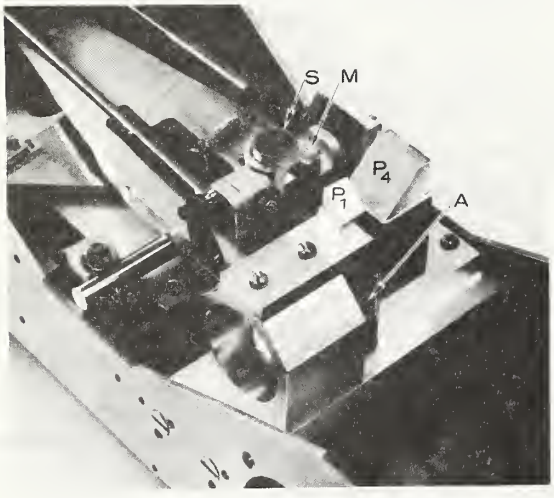
7.3. Line-Width Measurements

A series of measurements was made on the dimensions A, B, and C on the artifact illustrated in figure 25. These measurements were made to obtain additional data to assist in developing a basis for comparison of measurements made with microscopes equipped with different eyepieces. All of these measurements were made using a narrow-pass filter with the band center at 486 nm. The center-to-center spacing between two lines (dimension C) was measured on the NBS line-standard interferometer [48] as 34.924 ± 0.0025 μm. The uncertainty in this measurement is the 3-sigma value and represents the range in which 99 percent of the mean values of any set of measurements of this dimension will fall when made with the NBS line-standard interferometer. The results of the measurements made with various microscope eyepiece combinations are listed in table 7; the uncertainties represent the sample standard deviation obtained for each set of measurements. The measurements were normalized to the mean value of dimension C. The standard deviation associated with dimension C represents calibration uncertainty.

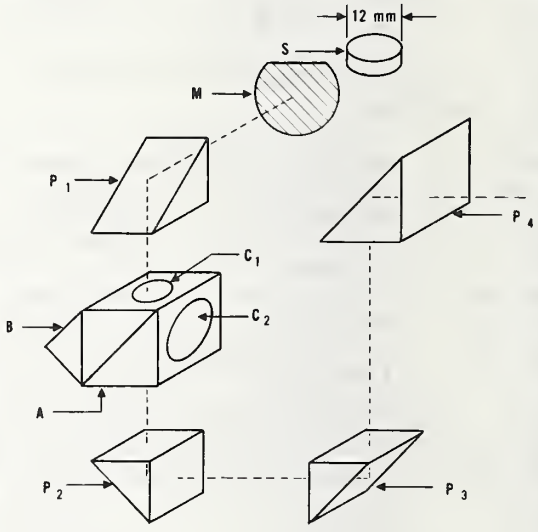
†NBS Optical Physics Division

Table 7 — Measured Values for Dimensions A, B, and C of Interim Measurement Artifact

Illumination Condition	Filar Eyepiece			Image Shearing Eyepiece		
	A, μm	B, μm	C, μm	A, μm	B, μm	C, μm
Transmitted Light, Bright Field	5.25±0.09	5.22±0.04	34.92±0.11	4.87±0.06	4.88±0.02	34.92±0.03
Reflected Light, Bright Field	4.94±0.92	4.92±0.01	34.92±0.02	5.11±0.03	5.09±0.04	34.92±0.09
Reflected Light, Dark Field	5.09±0.09	5.16±0.06	34.92±0.07	5.27±0.10	5.24±0.10	34.92±0.19



a. Photograph of the interferometer mounted on a scanning electron microscope stage.



b. Schematic drawing of the configuration of the interferometer and associated optical components.

A Beam-splitting polarizing cube
B Corner cube
C_i Quarter-wave retardation plates
M Stage mirror
P_i Prisms
S Test specimen

Figure 26. Polarizing interferometer.

Differences between values measured with filar and image shearing eyepieces for the bright-field, transmitted-light case agree in sign with the predictions of the calculations summarized in table 6 for matched numerical apertures. The differences for the bright-field, reflected-light case are opposite in sign as predicted from the discussion of section 7.1. Caution, however, should be used in comparing the differences in table 7 with the errors predicted in table 6. The model used to predict the errors assumed no interaction between the two edge profiles, an assumption probably not valid for 5-μm wide lines.

(F. W. Rosberry* and D. B. Novotny)

A polarizing interferometer with a 1 nm displacement resolution was constructed to make *in-situ* measurements of the movement of a scanning electron microscope (SEM) stage without interference from subtle changes in the optical path length caused by flexing of the vacuum system walls. A photograph of this interferometer mounted on an SEM stage is shown in figure 26; the configuration of its components is also shown schematically in the figure. The principles of operation of this interferometer are similar to those previously described (NBS Spec. Publ. 400-17, p. 36). The relative sizes of the interferometer and other components shown in the photograph may be estimated by comparing them with the diameter of the specimen, S, which is 12 mm. The interferometer consists of one beam-splitting polarizing cube, A; one corner cube, B; three quarter-wave retardation plates, C_1 (the one at the bottom of the interferometer is not shown); and a reference mirror cemented to one of the retardation plates, C_2. The path of the laser beam is shown by a dashed line. The beam enters the SEM chamber through a side port and is directed to the interferometer and to the stage mirror, M, by the system of prisms, P_1.

This circuitous beam path was necessary to minimize the blockage of secondary electrons by the interferometer and optical components. Failure to minimize this blockage was shown to result in an unacceptably low signal-to-noise ratio. The positions of the interferometer and its components were determined by placing objects simulating their sizes into the SEM chamber in various possible alignment configurations. All of the configurations which lent themselves to easy optical alignments blocked 80 to 90 percent of the emitted secondary electrons which would normally be detected. The illustrated configuration results in a decrease of only 20 percent in the normal signal-to-noise ratio.

(A. W. Hartman*)

*NBS Optics and Micrometrology Section, Mechanics Division.

8. TEST PATTERNS

8.1. Sheet Resistor Test Structures

The equation for the sheet resistance of a symmetrical van der Pauw structure [49]

$$R_s(\text{vdP}) = \frac{\pi}{\ell n 2}\frac{\Delta V}{I}, \qquad (10)$$

where I is the current and ΔV is the measured potential difference, assumes infinitely narrow contacts along the perimeter of the device. In the past this assumption was usually appropriate since most van der Pauw test structures could be designed with large body areas and small contact arms. However, the need to measure the sheet resistance of very small devices produces an uncertainty in the validity of this assumption since the width of the contact arms must be a significant fraction of the perimeter of the device.

A computer program was developed to solve for the error in measuring the sheet resistance of a van der Pauw structure designed with orthogonal boundaries and finite size contacts. This program uses a nine-point finite difference approximation to Laplace's equation and a successive over-relaxation solution [50]. This solution is used to set up the indefinite admittance matrix for a four terminal network which is solved for the van der Pauw voltage [51]. Checks for residue oscillation are made and the over-relaxation factor adjusted accordingly. The program starts with a coarse grid which is refined in steps until the desired accuracy is obtained. At present this program can operate on several geometries ranging from a square to a cross, including all orthogonal "pinwheels" having rotational symmetry.

A typical van der Pauw sheet resistor of this type is shown in figure 27. This structure is included in test pattern NBS-3 (NBS Spec. Publ. 400-12, pp. 19-22). This geometry was modeled for the computer program by replacing the extended pad area and metallized contacts by shorts at the ends of the contact arms as shown in figure 28. This represents the worst case condition.

The normalized error

$$E = [R_s(\text{true}) - R_s(\text{vdP})]/R_s(\text{true}),$$

where $R_s(\text{true})$ is the true sheet resistance and $R_s(\text{vdP})$ is the sheet resistance obtained from eq (10), is plotted for symmetric, orthogonal pinwheels in figure 29 and for symmetric, orthogonal quadrate crosses in figure 30. These figures can also be used to obtain the true sheet resistance from

$$R_s(\text{true}) = \frac{R_s(\text{vdP})}{1 - E}.$$

This analysis demonstrates that many novel van der Pauw designs are possible. For example, a cross constructed with minimum process stripe widths (D/S = A/S = 1.0) is found to have negligible error. (J. M. David)

8.2. Charge-Coupled Device Test Pattern

This study was undertaken to investigate the applicability of the charge-coupled device (CCD) as a test structure for use in semiconductor process control. The study was concluded with additional correlation of parameters as measured from various CCD structures and those measured using more conventional structures such as MOS capacitors, MOS transistors, and gated diodes.

Additional measurements were made of oxide thickness, dopant density, flat band voltage, and mobile charge density on two wafers using both the 32-bit and 128-bit circular CCDs (operated as capacitors) and various MOS capacitors (NBS Spec. Publ. 400-17, pp. 28-31). The results are summarized in table 8.

Additional measurements of transistor parameters were also made on a wafer using several MOS field effect transistors and the 32-bit and 128-bit circular CCDs operated as transistors (NBS Spec. Publs. 400-12, pp. 23, 25, and 400-17, pp. 30-31). The results of these measurements are summarized in table 9.

Surface state densities were determined on gated diodes by measuring the leakage current as a function of gate voltage. When this is done the fraction of the leakage current due to the surface states can be extracted. This fraction, $I_{gen,s}$, is given by

$$I_{gen,s} = qA_s n_i s_o/2,$$

where q is the electronic charge, A_s is the area of the gate, n_i is the intrinsic carrier density, and s_o is the surface recombination velocity which is given by

$$s_o = \sigma v_{th} \pi (kT/q) N_{ss},$$

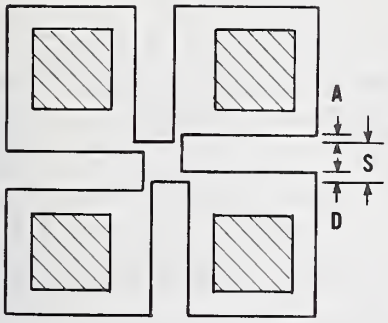


Figure 27. Schematic diagram of orthogonal pinwheel van der Pauw sheet resistor structure.

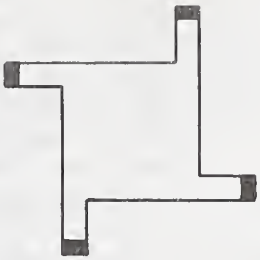


Figure 28. Equivalent geometrical model of orthogonal pinwheel.

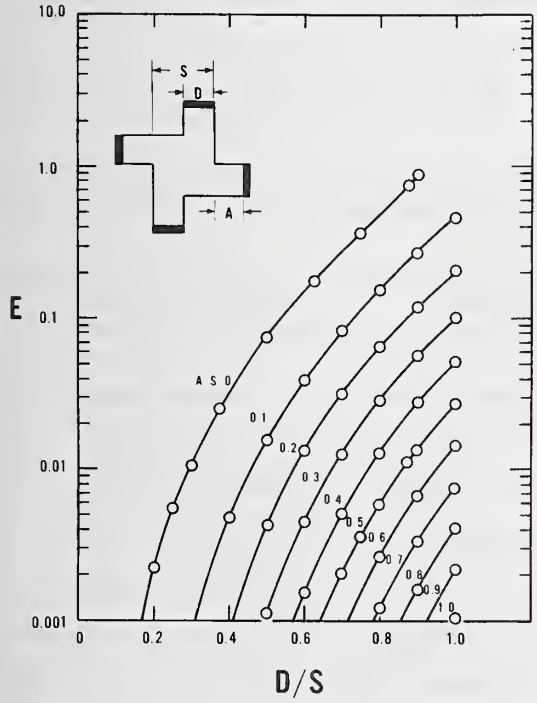


Figure 29. Calculated measurement error due to finite contact width for orthogonal pinwheels with four-fold rotational symmetry.

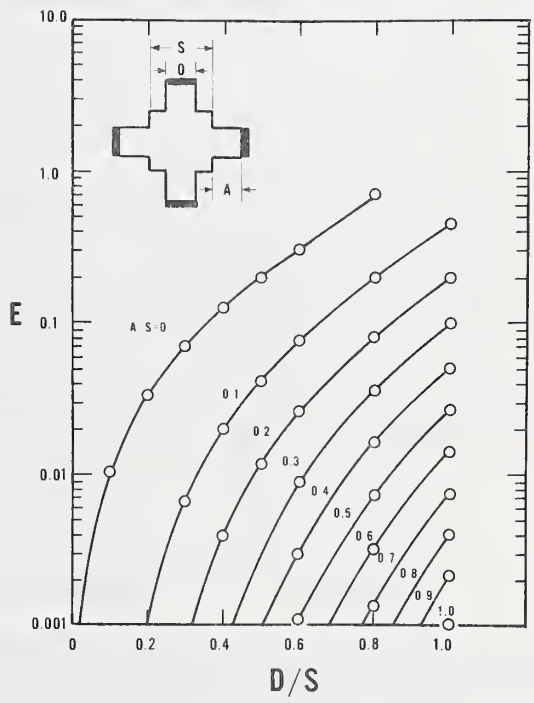


Figure 30. Calculated measurement error due to finite contact width for orthogonal quadrate crosses.

Table 8 — MOS Capacitor Parameters

Wafer	Device	Cell No.	Thin Oxide Thickness, nm	Thick Oxide Thickness, nm	Substrate Dopant Density, cm^{-3}	Flat-Band Voltage, V	Mobile Charge Density, cm^{-2}
CCD 242	MOSCAP	13	110.8±15.1		(1.74±)×10^{15}	-1.00±0.12	(3.1±2.4)×10^{10}
	MOSCAP	20	112.5±14.0	1067±126	(1.45±)×10^{15}	-0.99±0.10	(2.9±0.9)×10^{10}
	MOSCAP	21		1078±141	(1.52±0.45)×10^{15}	-2.16±0.33	
	32-bit CCD	2	109.7±20.2	1026±226	(3.8±3.7)×10^{15}	-1.54±0.26	(5.6±3.4)×10^{10}
	128-bit CCD	1	109.2±20.0	1131±183	(4.9±3.0)×10^{15}	-1.30±0.07	(7.2±3.2)×10^{10}
CCD 245	MOSCAP	13	115.2±9.5		(1.43±0.01)×10^{15}	-1.00±0.06	(1.9±1.1)×10^{10}
	32-bit CCD	2	105.2±5.2	910±47	(5.0±0.9)×10^{15}	-1.12±0.15	(4.5±3.2)×10^{10}
	128-bit CCD	1	111.8±19.1		(4.2±2.0)×10^{15}	-1.44±0.20	(1.1±0.5)×10^{10}

Table 9 — MOS Transistor Parameters

Wafer	Device	Cell No.	W/L	Linear Region		Saturation Region	
				V_T, V	μ_L, $cm^2/V \cdot s$	V_T, V	μ_S, $cm^2/V \cdot s$
CCD 242	MOSFET	26	31.1	-0.088±0.001	1080±62	-0.203±0.001	856±77
	MOSFET	23	3.39	-0.143±0.002	1072±59	-0.208±0.001	792±65
	MOSFET	28	1.55	-0.100±0.001	1054±24	-0.159±0.001	672±94
	23-bit CCD	2	0.0080	-0.35±0.26	1673±181	-0.69±0.19	676±257
	128-bit CCD	1	0.0029	-0.25±0.03	1768±286	-0.50±0.20	544±100

where σ is the capture cross section for minority carriers (taken as 10^{15} cm^{-2} [52]), v_{th} is the thermal velocity of minority carriers (taken as 10^7 cm/s at room temperature), k is Boltzmann's constant, T is the absolute temperature, and N_{ss} is the number of generation-recombination centers per unit area per electron volt near the surface of the silicon (surface state density). Values for N_{ss} measured on four gated diodes on wafer 242 ranged from 1.4×10^{10} to 2.1×10^{10} $cm^{-2} \cdot eV^{-1}$. These results were compared with measurements of surface state density by the double-pulse, charge transfer loss method (NBS Spec. Publ. 400-12, p. 25) [53] on a sampling of 128-bit circular CCD's on the same wafer which yielded value between 1.4×10^{10} and 8.8×10^{10} $cm^{-2} \cdot eV^{-1}$ for N_{ss}.

(I. Lagnado*)

8.3. Test Pattern Design and Analysis for SOS/LSI

This task was undertaken to produce a set of overlay masks containing test devices and structures suitable for characterizing a large scale integration (LSI), silicon-on-sapphire (SOS) process (or other mask compatible processes) and to develop testing procedures for these structures.

The pattern is comprised of five classes of test structures, each intended to test a different aspect:

1. structures to test design and process parameters,
2. structures to test spatial variations,
3. structures to test geometrical variations,
4. redundant arrays to test series strings of transistors, crossovers, and contact openings, and
5. circuit elements, and dimensional and alignment structures.

Classes 1, 3, 4, and 5 occupy quadrants of the pattern while class 2 structures are arranged in a cross between the quadrants. The design of the type 2 pattern was completed. It was done first since it largely determines the area remaining in the quadrants. The design rule for this and all other patterns to be tested with probe cards (or equivalent) was chosen to be pads 4 mils (0.1 mm) on a side, minimum, on 6-mil (0.15-mm) centers, minimum. These dimensions have been used previously and cause little problem during automatic probing. This choice of pad center and size has a first order effect on the overall pattern size. The type 2 pattern consists of four devices:

1. Probe resistance test and coding function,
2. *n*-channel MOS transistor, 0.3 mil by 0.6 mil (8 μm by 15 μm),
3. *p*-channel MOS transistor, 0.3 mil by 0.6 mil (8 μm by 15 μm), and
4. MOS capacitor with both types of diffusion.

The first device consists of two pads short-circuited together. It serves to test both the presence of a suitable pattern and the resistance of the contacting probes. Information regarding the wear of probe tips and variation in probe resistance across a wafer can be obtained from this structure The next two devices provide high information density and were chosen with nominal dimensions. These dimensions are flexible and may be adjusted to suit particular conditions of greatest interest. The fourth device is an MOS capacitor. Since it has both types of peripheral diffusion, the type of starting material is irrelevant, and both sides of the C-V curve are available. It would be desirable to use more devices but the pattern size with only these devices is approximately 40 mils (1 mm) long and 6 mils (0.15 mm) wide. This allows a maximum of 40 devices of each type across the pellet in either direction. Consideration is being given to adding another capacitor to allow for the possibility of two types of starting material or to examine the so-called "well" in bulk CMOS processes. This would add approximately 7 mils (0.18 mm) to the length.

(W. E. Ham† and J. M. David)

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*Work conducted at Naval Electronics Laboratory Center under NBS Order No. 502498. NBS contact for additional information: M. G. Buehler.

†Work conducted at RCA Laboratories under NBS Contract 5-35916.

9. INTERCONNECTION BONDING

9.1. Non-Destructive Test for Beam-Lead Bonds

In earlier work on the acoustic emission test on bonded beam-lead devices (NBS Spec. Publ. 400-12, pp. 31-32), the devices were stressed by applying a downward force on the die. Although some tests were very successful in detecting weakly bonded beam leads, the results of other tests were more ambiguous. Therefore, to establish a base line for measurement techniques and equipment sensitivity, bonds made by bonding 0.001-in. (25-μm) diameter aluminum wire bonds to gold metallization on both ceramic and silicon substrates were monitored for acoustic emission during pull testing. Emission from partial lift-ups and pre-break cracks, comparable with the expected emission from weak beams, was easily detected. The actual wire-bond breaks registered much higher counts. To avoid any ringing of the broken wire, the entire bond system, including the pulling hook, was covered with a thick acoustic coupling compound known as "sticky goop." This damped all but the acoustic emission from the direct break. Since this emission was a single high-amplitude peak, it was more easily observed on an oscilloscope than on the normal acoustic emission averaging counter.

In an effort to improve reproducibility and sensitivity to the very weak acoustic emission from poorly bonded beam leads, different types of detector configurations and extended frequency ranges were investigated. A special detector probe was prepared* to convert the force probe into a combined force probe and detector as shown in figure 31. Preliminary measurements indicate that this method of mounting the detector is more effective than the conventional method of mounting the detector under the substrate. However, coincidence systems involving both types of mounted detectors may be even more sensitive than either one alone. The emission picked up from the die has higher frequency components than that through the substrate so that the detector electronics must have higher frequency response. The best measurements thus far have resulted from stressing the device near the sides rather than in the middle as previously described. This suggested that a rocking or wobbling force might be better than a constant one.

*This probe was prepared by Seymour Edelman, NBS Bulk Properties Section, Polymers Division.

A combination wobble-detector-probe is pictured in figure 32.

In the above work it was found that the acoustic emission from poorly bonded beams often consisted of a few short peaks above the noise. These may not be observed in typical acoustic-emission count totalizing equipment, where the discriminator is typically adjusted for a background noise level of 5 to 10 counts per interval. Therefore, digital pulse capturing equipment has been used to record the bursts which could then be observed on an oscilloscope. Tunable frequency filters also can be used to separate the signal from the noise, since the signal tends to have a frequency appropriate to the geometrical resonance of the chip or substrate, depending on the position of the detector.

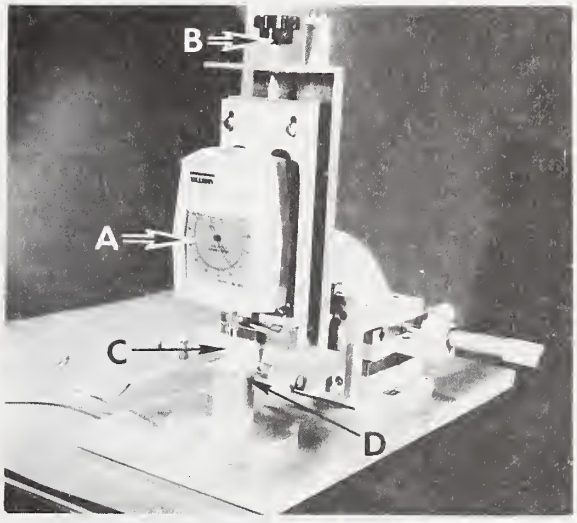
The primary method of stressing beam-lead devices has been to apply a force downward onto the die. However, since it would be desirable to find a practical method of lifting the die upward, thus applying a direct peel force on the beam-lead bonds as well as on the beam anchors, a vacuum chuck was made to pull a bonded beam-lead device upward. A silicon rubber chuck, molded with the imprint of a 14-beam die, was bonded to the end of a hypodermic needle, and the needle hole was cut through the rubber as shown in figure 33. This unit can replace the force probe detector on the force gauge in the test apparatus (fig. 32). Tests with this apparatus yielded a maximum pull force of about 50 mN (5 gf) using house vacuum and about 60 mN (6 gf) using a mechanical pump vacuum. This may be sufficient to stress beams for acoustic emission tests. However, because air leaks generate noise at frequencies up to several hundred kilohertz, use of the chuck must be reevaluated in the 1 to 3 MHz range.

(G. G. Harman and W. A. Cullins)

Initial procedures for contaminating bonding substrates to produce test specimens with one or two weak beams sometimes resulted in good bonds. A new method was found to impair beam lead bondability in a reliable manner. In this method, chrome-gold coated ceramic substrates are heated to 300°C for 2 h to diffuse the chrome to the surface where it oxidizes [54, 55]. The chrome oxide is removed by etching with ceric ammonium nitrate in regions where good bonds are desired. Bonds made to regions where the chrome oxide remains are weak and unreliable. Photomasks

A Acoustic waveguide and force probe
B Sensitive piezoelectric detector
C Adaptor coupling to force gauge

Figure 31. Acoustic emission detector and force probe.



A Force gauge
B Wobble control
C Acoustic waveguide and emission detector
D Substrate with beam-lead devices

Figure 32. Combination wobble-force probe and acoustic emission detector.

A Molded silicone rubber chuck for gripping die
B Vacuum port
C Adaptor coupling to force gauge

Figure 33. Vacuum chuck for pulling beam-lead devices.

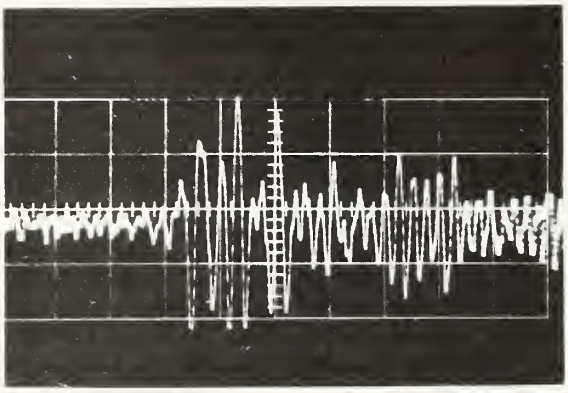
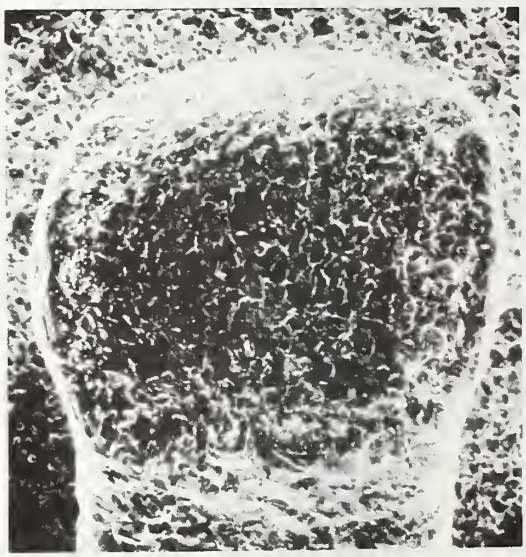


Figure 34. Typical acoustic emission wave form. (Vertical scale, 0.25 V/div; horizontal scale, 6 μs/div.)

were designed to facilitate etch removal of the chrome oxide in designated patterns.

An investigation was carried out to establish that the chrome-oxide method of producing unreliable bonds still left a few areas that were welded and therefore could produce valid acoustic emission signals when the device was stressed. Devices were bonded with various bonding schedules to substrates that had chrome oxide on the surface. The devices were stressed with the wobble-force-detector apparatus (fig. 32) and acoustic emission signals were recorded on digital pulse capturing equipment. The oscilloscope trace of a typical signal is shown in figure 34. The poorly bonded beams were then peeled back and examined for evidence of bonded areas and acoustic emission point sources. Examination of the beam-lead depression in the substrate with a scanning electron microscope, revealed tiny broken welded areas around the perimeter as shown in the scanning electron micrograph in figure 35a. The largest of these is indicated by the arrow. These broken welded areas are also shown as tiny white dots in a circle near the perimeter in the scanning electron micrograph of the beam itself in figure 35b. The fact that the welded areas lie around the perimeter is in agreement with deformation theory of thermal compression bonding first put forth by Tylecote [56]. (G. G. Harman)

a. Depression in the substrate remaining after beam was peeled back. The arrow denotes the largest broken welded area. Magnification: ∿580X.)



b. Peeled beam lead. (Magnification: ∿580X.)

Figure 35. Scanning electron micrographs of a poorly bonded beam lead.

9.2. Wire Bond Pull and Shear Tests

The bond pull test and the bond shear test were compared in an experiment conducted jointly with Sandia Laboratories to determine their significance for aluminum-aluminum ultrasonic bonds. Three groups of wire bonds were made on an 800 nm thick aluminum film electron-beam evaporated on an oxidized silicon wafer. The aluminum film was patterned into squares 5.0 mil (0.127 mm) on a side on 10.0 mil (0.254 mm) centers. Each group consisted of approximately 40 loops of 1.0 mil (25 μm) diameter aluminum wire ultrasonically bonded at each end. Different conditions were used in bonding each of the groups so that the bonds in each group had a significantly different deformation. All of the bond pairs were designed to break at the heel of the first bond. Thus, the entire welded portion of the bond remained on the bonding pad after pull testing and the bond could be subsequently shear tested. The ratio of the loop height to the bond-to-bond spacing was set to be 0.3 so that when the bond pairs were pulled midway between the two bonds, the force in the direction of pull was equal to the force in the wire. Therefore, the pull strength and shear force data could be compared directly.

First, half the bond pairs in each group were tested by pulling in a direction normal to the substrate midway between the bonds. Then, a newly developed precision shear tester [57] was used to obtain bond shear forces on both the pulled and unpulled bonds.* The results of these measurements are summarized in figure 36.

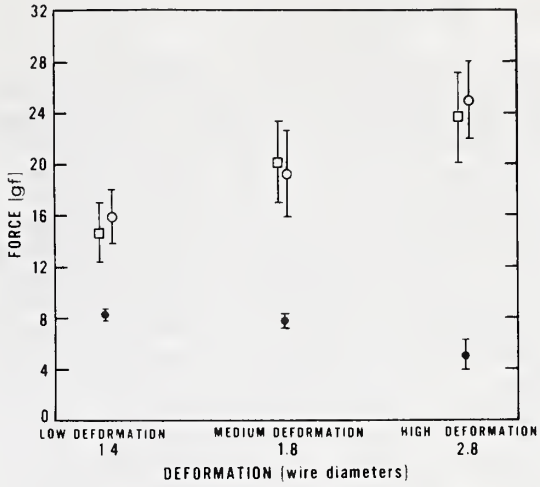


Figure 36. Data from bond pull test and bond shear test. (Pull test, ●; shear test before pulling, □; shear test after pulling, ○; error bars represent one sample standard deviation above and below the mean strength of approximately 20 bonds.)

These results may be understood if the metallurgical nature of the bond is considered. For aluminum ultrasonic bonds the bond heel becomes metallurgically overworked and weak as the bond deformation increases, but the amount of the welded area increases. The pull test is particularly sensitive to the weakening of the bond heel but not to the total weld area unless the latter is so small that the bond lifts off during the test. Therefore, the pull force decreases as the deformation increases.

The shear test, on the other hand, is completely independent of the condition of the heel; it is sensitive only to the actual amount of welding. As such, it has been used to evaluate the quality of welding in thermal compression bonds [57] and is a very valuable research tool. In figure 36 it is apparent that the shear force increases as the deformation increases, indicating that the amount of welded area increases with deformation. However, from the relatively larger error bars in the shear test data it can be concluded that, even though the bond heel strength in the pull test is uniform, the actual welded area under each bond displays a random variation. This is consistent with previous work on the formation of ultrasonic bonds [58].

No comparison was made between the pull test and the shear test on gold wire. However, past work with ultrasonically bonded gold wire [59] has shown that the bond pull test is relatively less sensitive to bond and heel deformation of gold wire bonds than to that of aluminum wire bonds for deformations up to about three wire diameters. The shear strength of gold wire bonds, however, would be expected to increase with bond deformation in the same way as for aluminum wire bonds.

(G. G. Harman and C. A. Cannon)

*This portion of the experiment was conducted at Sandia Laboratories by Wayne Vyne.

10. HERMETICITY

10.1. Helium Mass Spectrometer Method

Anomalously high values of indicated leak rate were obtained from the second stage of the interlaboratory evaluation of the helium mass spectrometer leak detector method [60] for testing fine capillary leaks in large volume (~1.5 to 2 cm^3) containers which is being conducted in cooperation with ASTM Committee F-1 on Electronics (NBS Spec. Publ. 400-4, p. 67). Experimental data obtained with sealed-off capsules of approximately the same dimensions as the test leak specimens indicated that the high, uniform values of measured leak rate were due to initial permeation of helium into the borosilicate glass matrix followed by diffusive outgassing after removal of pressurization (NBS Spec. Publ. 400-12, pp. 33-34). A fixture was devised to allow exposure only of the tip area of the leak to the leak detector which reduced background outgassing by about a factor of ten; however, such manipulation increased the possibility of damaging the fine capillary tip.

At the January meeting of the Hermeticity Section of Committee F-1, it was decided to defer continuation of the interlaboratory test until it could be determined whether a modified pressurization schedule could be used to attenuate outgassing without causing severe degradation of leak testing sensitivity. The possibility of conducting the pressurization step at reduced temperature, to decrease diffusion of helium into the glass, was also discussed but rejected as being too awkward to be practical.

To evaluate the effects of modification of the pressurization schedule, the indicated leak rates were determined for the sealed-off capsules with an exposed surface area of about 16 cm^2 following pressurization in helium at 5 atm (absolute) (5×10^5 Pa) for 0.2, 0.5, 1, and 20 h. Equivalent leak, or outgassing, rate, R, was measured as a function of time from a few minutes after pressurization until the rate fell off to about 10^{-8} atm·cm^3/s (10^{-9} Pa·m^3/s) or less. The results are shown in figure 37. As expected, initial outgassing rates were found to be essentially independent of pressurization time, being a function of helium concentration in the glass surface.

The minimum detectable leak rate is limited by the outgassing rate. The dwell time necessary for the outgassing rate to fall to a particular value can be derived from the data of figure 37 as a function of pressurization time with maximum allowable outgassing rate, R_{max}, as a parameter. Some extrapolation was employed as indicated in the figure by the broken portion of the curves. Typical dwell time characteristics, which are of the form

$$t_d = bt_p^a ,$$

where t_d is the dwell time in hours and t_p is the pressurization time in hours, are shown in figure 38. For all three characteristics the exponent a is about 0.65.

If the leak detector sensitivity, Q_{min}, is taken as R_{max}, the smallest and largest detectable leak sizes, L_{min} and L_{max}, for given values of t_d and t_p can be determined according to the procedures of ASTM Method F134 [60]. Examples are listed in table 10. It should be noted that about one fifth of the test leaks have leak sizes smaller than 8×10^{-8} atm·cm^3/s (8×10^{-9} Pa·m^3/s) and about two fifths have leak sizes smaller than 2×10^{-7} atm·cm^3/s (2×10^{-8} Pa·m^3/s). Only one of the 50 test leaks has a leak size larger than 3×10^{-5} atm·cm^3/s (3×10^{-6} Pa·m^3/s).

From these results it was concluded that the interlaboratory evaluation should be deferred until additional test specimens, less susceptible to helium absorption, can be obtained. (S. Ruthberg)

10.2. Correlation of Moisture Infusion, Leak Size, and Device Reliability

A study has been initiated to derive a quantitative relationship between leak size in hermetic packages and moisture infusion along with the consequent effect on device reliability. The approach is to incorporate a dew point moisture sensor and a moisture-susceptible integrated circuit into packages, each with a prefabricated microchannel leak of known size, which would then undergo leak testing and accelerated life test.

The first phase of this effort was undertaken to evaluate the accuracy of the dew point measurement procedure, fabrication procedures for and stability of the microvents, and the moisture sensitivity of a suitable integrated circuit.

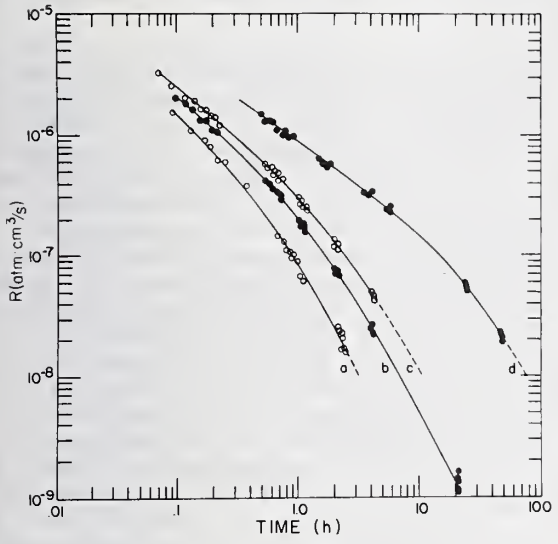


Figure 37. Helium outgassing rate, R, of sealed borosilicate glass capsules as a function of dwell time between pressurization and measurement. (Pressurization times: Curve a, 12 min; Curve b, 30 min; Curve c, 1 h; Curve d, 20 h.)

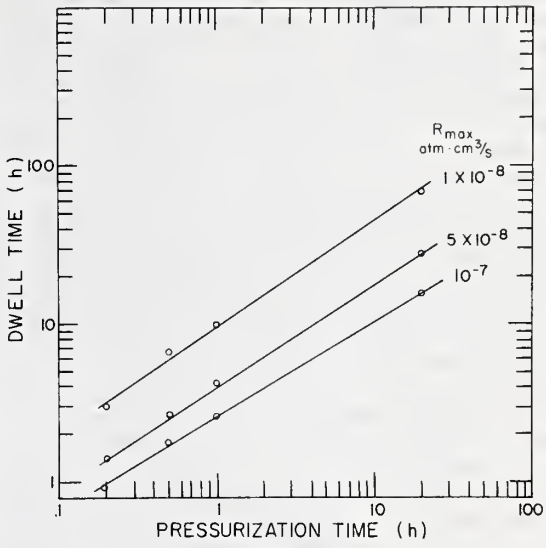


Figure 38. Dwell time necessary for helium outgassing rate of sealed borosilicate glass capsules to fall to specified maximum allowable rates, R_{max}, as a function of pressurization time.

Table 10 — Smallest and Largest Detectable Leak Sizes for Borosilicate Glass Capillary Test Leaks[a]

t_p, h	t_d, h	$Q_{min} = R$, atm·cm³/s	L_{min}, atm·cm³/s	L_{max}, atm·cm³/s
1	4	5×10^{-8}	9×10^{-7}	6×10^{-4}
1	10	1×10^{-8}	4×10^{-7}	3×10^{-4}
20	30	5×10^{-8}	2×10^{-7}	7×10^{-4}
20	75	1×10^{-8}	9×10^{-8}	3×10^{-5}

[a] pressurized at 5 atm for t_p hours; package volume = 2 cm³

Two types of moisture sensor are being utilized. One is an interdigitated set of thick film electrodes on an alumina substrate. The second is an electrode system formed between the die attach area and the leads of a dual-in-line package. In use, the leakage current between the electrodes is measured while the temperature of the package is reduced, by means of a thermoprobe, until the dew point is reached as indicated by an abrupt current increase [61]. A set of 25 specimens was fabricated; each specimen is an open microcircuit package with the two sensors attached. To reduce electrical leakage each specimen was coated with epoxy on all surfaces but the sensor and the area which would be contained within the internal volume of the package if it were sealed. To test the sensors, each package was mounted on a temperature controlled probe and was placed in an environmental chamber which was first stabilized in a dry mode and then set to give the desired relative humidity in the range between 5 and 50 percent. The thermoprobe was stabilized at an initial reference temperature and then brought down in small temperature increments while leakage current was monitored. The relative humidity appropriate to the measured dew points was compared with the relative humidity of the chamber. Initial data indicate close agreement between the two sensors and the psychrometric parameters.

The microvents are produced by laser drilling the case and back plating until a suitable leak size has been obtained. A matrix experiment has been performed to determine the suitability of procedures. A reasonable yield with a range of leaks from 10^{-5} to 10^{-8} atm·cm^3/s (10^{-6} to 10^{-9} Pa·m^3/s) has been obtained.

The 741 operational amplifier was selected for trial as a suitable integrated circuit test vehicle. This is a monolithic bipolar device with an MOS capacitor. Two groups of 25 devices each were obtained. One group was unpassivated; the second was passivated with silane glass. All devices were pretested thermally and electrically, mounted for direct exposure, and then submitted to a humidity step-stress test under dc bias at 85°C. The devices were operated for 168-h incremental periods at 20, 50, 70, 85, and 95 percent relative humidity until failure, which was defined as drift of one or more electrical parameters outside specified limits. Two of the unpassivated devices failed in the first step, 15 more in the second step, 7 in the third step, and the last in the fourth step. Of the glassivated devices, one failed in the second step, one in the third step, one in the fourth step, and 4 in the fifth step. Each of the failed circuits was examined microscopically to establish the cause of failure. All failures were determined to be moisture related as evidenced by the presence of corrosion on the aluminum metallization runs. Based on these results the unpassivated 741 operational amplifier was selected for use in the moisture sensitivity life test.

(S. Zatz* and S Ruthberg)

*Work performed at Martin-Marietta Aerospace, Orlando Division under NBS Contract No. 535880.

11. DEVICE INSPECTION AND TEST

11.1 Automated Scanning Low-Energy Electron Probe

The initial electron gun structure (NBS Spec. Publ. 400-12, p. 28) for the ASLEEP system was completed and mounted in the vacuum system for testing and alignment. The gun was placed in the circuit shown in figure 39 for beam current tests. The target was an aluminum grid comprising 60 μm wide lines on 600 μm centers over silicon dioxide (NBS Spec. Publ. 400-17, p. 46) mounted on the specimen manipulator. The 6-V battery was inserted into the circuit during initial testing to overcome patch effects at the target. The focus coil was adjusted to a magnetic induction of 70 gauss (7 mT) and the target current maximized by adjusting the various potentials. The maximum current collected by the target was 1.7 nA, obtained with the heater current at 9.3 A, grid 1 at 30 V and grid 3 at 500 V.

The first electron gun developed a short between the high voltage and the cathode necessitating a modification of the design. The glass insulators used to shield the high voltage leads were fractured where they crossed the low voltage elements of the gun. Notching the grid and cathode holders to allow clearance for stronger tubular ceramic insulators corrected this problem. The original gun used three sapphire rods to hold the gun elements in place. The rods were notched and metal tabs were inserted in the notches and spotwelded to the gun elements. This scheme made alteration and repair of the gun difficult. The elements of the gun are now held in their proper relationship by hollow ceramic spacers through which a bolt can be run to hold the assembly under compression. The modified gun has been tried and found to be more successful.

The computer control system rasters the electron beam over the test grid. If the electrometer in the beam current test circuit (fig. 39) is replaced by a low noise amplifier, an image may be formed on a cathode ray tube (CRT) by using the amplified target current signal to control the CRT beam intensity. Figure 40 is a picture of one such image taken of the aluminum grid during preliminary system checkout. The narrow line at about one half the grid spacing near the edge of the picture is a scratch in the silicon dioxide surface. Figure 41 is an image of an array of MOS capacitors made of 30-mil (0.75-mm) diameter dots of aluminum on silicon dioxide 100 nm thick. The capacitors were scanned with a beam of fixed energy (approximately 3.5 eV). The four white capacitor dots in the center of the picture are shorted to the substrate due to defects in the oxide. Similarly, two rows of shorted capacitors are located where the wafer was scribed and broken.

Additional software has been generated for presenting surface potential mapping information. The electron beam is scanned in the x-y plane, the retarding voltage is ramped to a preselected threshold current level, the surface potential is scanned over any selected area of the target, and the results are presented in a three dimensional display all under computer program control. In the presentation, the y-axis is somewhat elongated and the z-axis deflection of the scan line is proportional to the relative surface potential. Figure 42 shows a surface potential scan of an array of capacitors on silicon dioxide. Variations in height of the profiles are a direct measure of the dielectric uniformity assuming the metal work function to be constant. A high dot indicates a high capacitance. This result qualitatively demonstrates the ASLEEP as a non-destructive computerized surface diagnostic technique.

(W. C. Jenkins* and G. P. Nelson*)

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*Work conducted at the Naval Research Laboratory under NBS Order No. 501718. NBS contact for additional technical information: K. F. Galloway.

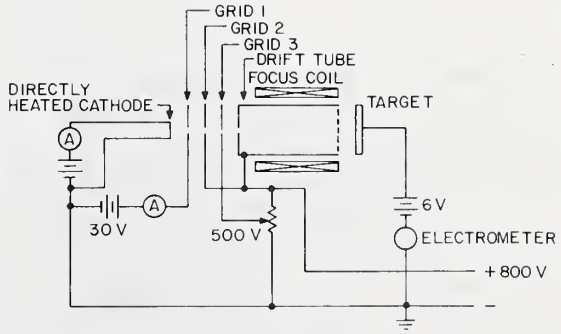


Figure 39. Circuit for testing electron gun beam current.

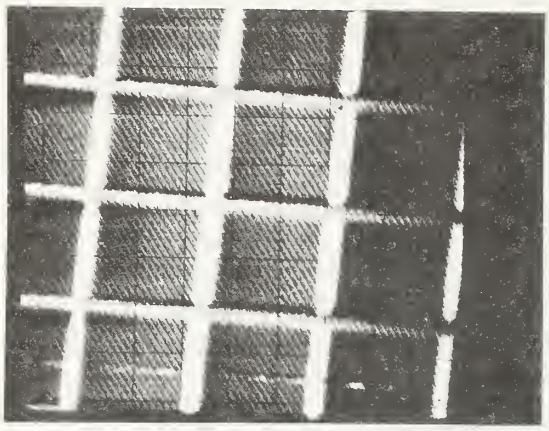


Figure 40. ASLEEP image of aluminum grid.

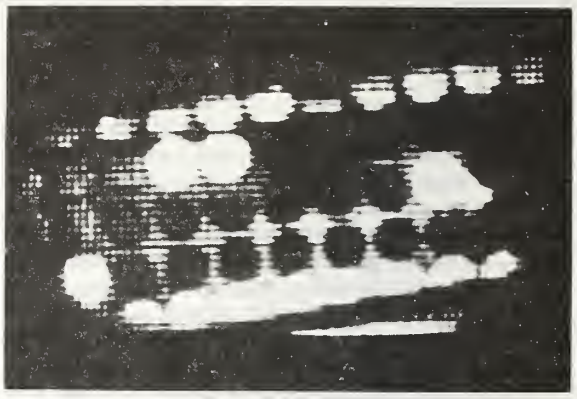


Figure 41. ASLEEP image of MOS capacitor array.

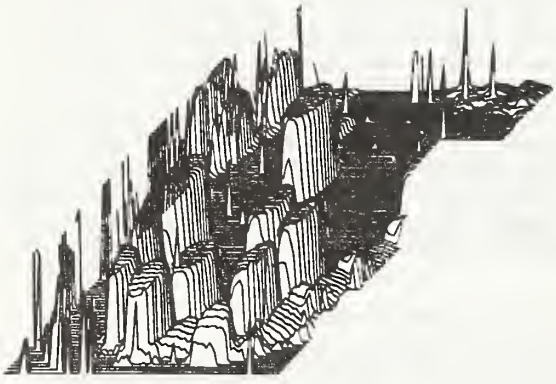


Figure 42. ASLEEP scan of 30-mil (0.76-mm) diameter MOS capacitors on 35-mil (0.89-mm) centers.

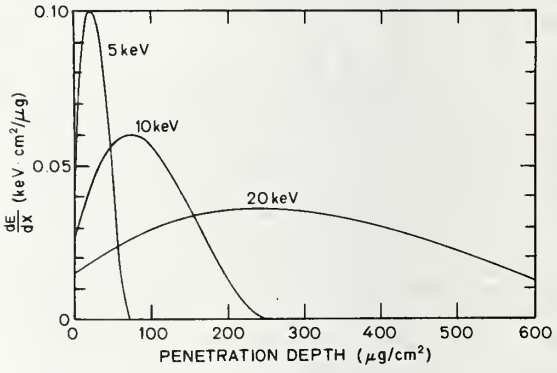


Figure 43. Energy dissipation as a function of penetration depth for several electron energies in material with atomic number between 10 and 15 calculated according to Everhart and Hoff [68].

11.2. Scanning Electron Microscopy — Electron Beam Induced Current Mode

A first-order prediction of the magnitude of electron beam induced current (EBIC) signals in device structures resulting from exposure to the electron beam in a scanning electron microscope (SEM) can be obtained from elementary considerations. This problem has been approached with varying degrees of sophistication by several authors [62-66]. The EBIC signal can be predicted if the magnitude and spatial variation of the electron-hole generation within the structure is known. Specific construction details of the device, device biasing, and SEM operating parameters, such as beam accelerating voltage and beam current, must be considered. In many cases the required specimen details are known or can be estimated to an acceptable accuracy.

Early work on the distribution of energy loss as a function of penetration depth for kilovolt electrons, the information necessary for calculating electron-hole generation, was done by Grün [67]. He experimentally determined the electron energy absorption as a function of penetration depth in air and demonstrated two important points. First, he obtained a relationship between electron

projected range, R_G, and electron beam energy, E_B:

$$R_G = 4.57\ E_B^{1.75},$$

where R_G is expressed in micrograms per square centimeter* and E_B is expressed in kiloelectron volts, which was valid over the range 5 keV $\leq E_B \leq$ 25 keV. Second, he showed that the shape of the depth-dose curve is practically invariant if the penetration distance is normalized to R_G and the energy is normalized to E_B. Everhart and Hoff [68] extended these general conclusions to solids and obtained a generalized depth-dose curve for solid materials by taking the steady-state electron beam induced current through the insulating layer of a metal-oxide-semiconductor structure as a measure of the energy dissipation in that layer. They found for structures of aluminum, silicon dioxide, and silicon the projected range,

$$R_G = 4.0\ E_B^{1.75},$$

to be accurate for 5 keV $\leq E_B \leq$ 25 keV. They also found that for elements with atomic number in the range $10 < Z < 15$, the energy dissipation is given by

$$\frac{dE}{dx} = \frac{(1-f_B)\ E_B\ \lambda(y)}{R_G}, \qquad (11)$$

where $y = x/R_G$, f_B is the fraction of incident energy backscattered, and $\lambda(y) = 0.60 + 6.21y - 12.40y^2 + 5.69y^3$. Equation 11 is plotted in figure 43 for several beam energies with the assumption that $f_B = 0.1$ (sec. 11.3.). From these curves one can estimate the EBIC signal in a silicon device.

Consider a silicon p-n junction covered by aluminum or silicon dioxide or both to a thickness t as illustrated in figure 44a. If one assumes that all the energy deposited in the silicon goes into the creation of electron-hole pairs, the number of pairs generated by each incident electron is

$$N = E_D/E_p,$$

where

$$E_D = \int_t^{R_G} \frac{dE}{dx}\, dx$$

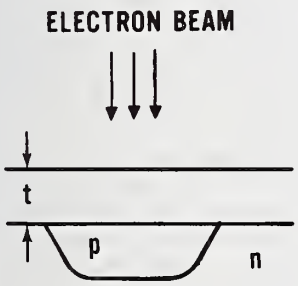
and E_p, the energy required to create one pair, is 3.64 eV [69].

If one assumes 100 percent collection efficiency, the electron beam induced current,

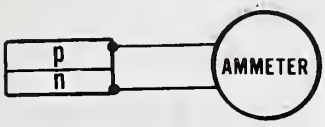
$$I_E = I_B N,$$

where I_B is the SEM beam current, is registered by the ammeter in figure 44b. The quantity N is therefore the current gain; N is plotted as a function of electron beam energy for several thicknesses of absorber above the silicon in figure 45 and as a function of absorber thickness for several beam energies in figure 46. The nomograph in figure 47 can be used to convert aluminum, silicon dioxide, or aluminum plus silicon dioxide thickness in micrometers to absorber thickness in micrograms per square centimeter.

As an example of the use of these graphs to make a quick estimate of the current gain to



a. Schematic illustration of junction showing absorber thickness, t, above silicon and incident electron beam.



b. Schematic illustration of experimental arrangement for current measurement.

Figure 44. Examination of silicon p-n junction in the electron beam induced current mode.

*The measure of length used here is the product of material density and thickness.

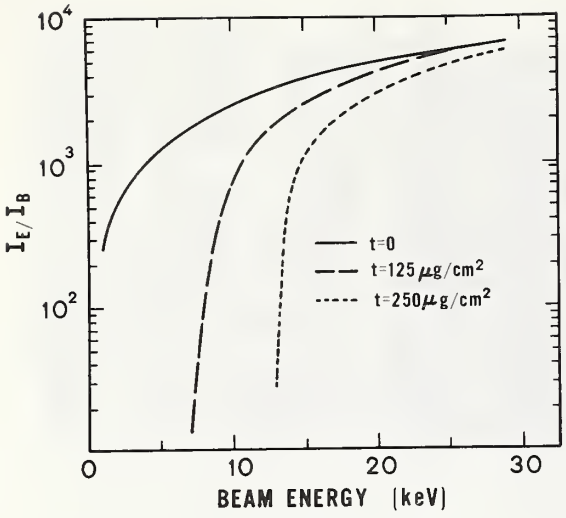


Figure 45. Current gain, I_E/I_B, for several absorber thicknesses as a function of electron beam energy.

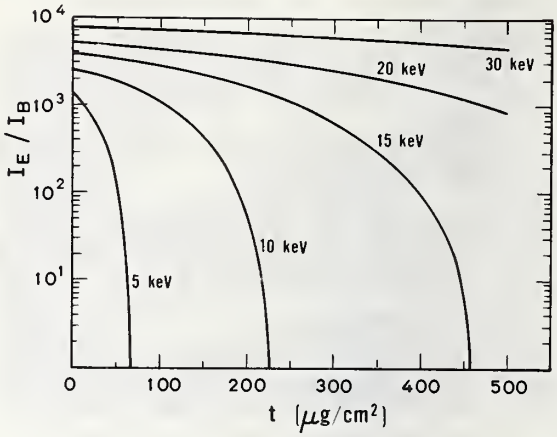


Figure 46. Current gain, I_E/I_B, for several beam energies as a function of absorber thickness, t.

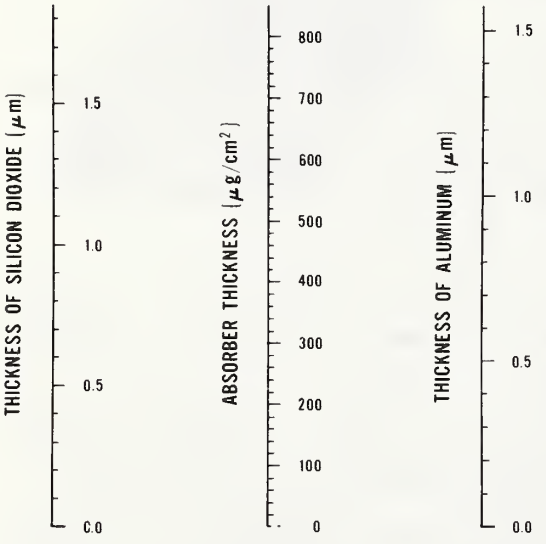


Figure 47. Nomograph to convert aluminum, silicon dioxide, or aluminum plus silicon dioxide thickness in micrometers to absorber thickness in micrograms per square centimeter. (To use, draw a line from the silicon dioxide thickness to the aluminum thickness and read the absorber thickness directly.)

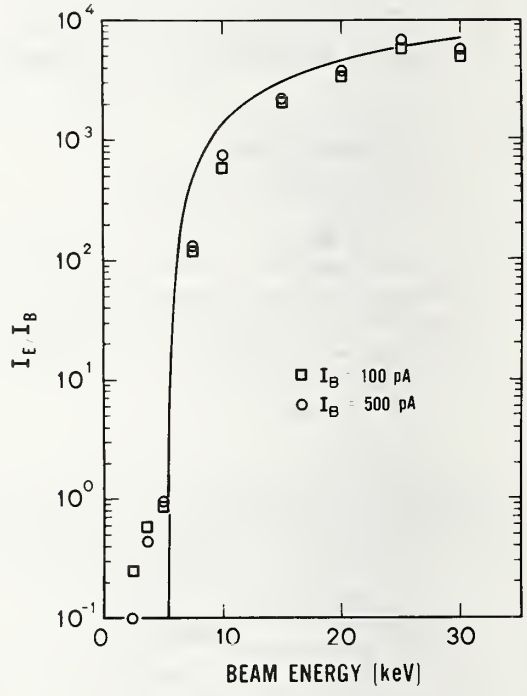


Figure 48. Comparison of measured electron beam induced currents with the results of the elementary calculation.

be expected when performing an EBIC examination, consider a 10-keV electron beam incident on a silicon structure with a 500-nm thick surface film of silicon dioxide. From figure 47, the total absorber thickness is 115 μg/cm^2 and from figure 46 the current gain is 800.

An experimental measurement was made for comparison with the results of this calculation. The device chosen for study was a *p-n* diode similar to the one shown in figure 44. The diode was fabricated in a wafer of phosphorus-doped silicon with room temperature resistivity in the range 5 to 10 Ω·cm and a <111> surface orientation. The *p*-region was formed by diffusing boron to a depth of approximately 1.4 μm; the diffusion profile was gaussian and the sheet resistance was about 180 Ω/□. The thickness of the oxide layer above the junction was approximately 330 nm. The I-V characteristics of the diode were unchanged when measured after performing the EBIC measurements.

The diode was exposed to both 100 and 500 pA SEM electron beams at energies from 2.5 to 30 keV. Although the active region of the diode was 1.5 mm (0.06 in.) in diameter only a small portion of the central part (approximately 10^{-3} cm^2) was scanned in order to eliminate edge effects. The electron beam induced current was measured with an ammeter capable of measuring currents from 1 nA to 100 μA connected across the *p-n* junction. The results are shown in figure 48 in which I_E/I_B (or N) is plotted as a function of beam energy. The solid line represents the calculation for an absorber thickness of 330 nm. It is apparent that there is reasonable agreement between the experimental and theoretical results. Discrepancies at higher beam energies may arise from failure to collect all the carriers produced while the disagreement below 5 keV may be attributed to the injection of energy (low energy x-rays, electron straggling, etc.) or charge from the absorber. Plotting the induced current normalized by the beam current produces a curve that is essentially independent of beam current, as expected. Similar results were obtained for other similar diodes.

The simple calculation presented here seems to give an adequate first order prediction of the electron beam induced currents for simple device structures. However, the validity of the assumptions used should be assessed for each specific application.

(K. F. Galloway, K. O. Leedy, D. E. Sawyer, and W. J. Keery)

11.3 Scanning Electron Microscopy — Electron Beam Induced Damage

In order to utilize the energy deposited versus penetration results of Everhart and Hoff [68] to calculate the energy deposited in aluminum, silicon dioxide, and silicon structures by a low energy electron beam (NBS Spec. Publ. 400-17, pp. 43-46), knowledge of the fraction of incident energy backscattered from the specimen (f_B) is necessary. This fraction is usually taken to be 0.1 from the work of Bishop [70] at 30 keV. A study was undertaken to examine the validity of using this value at lower electron beam energies.

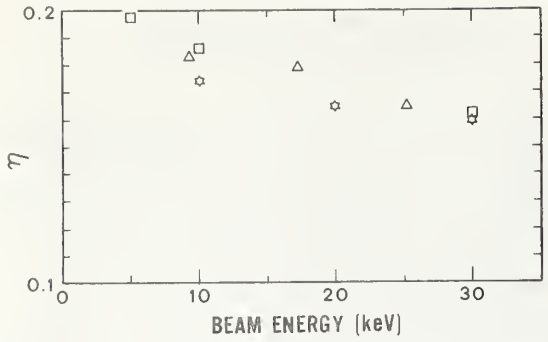
The fraction f_B depends on η, the fraction of incident electrons backscattered, and the fractional mean energy of the backscattered electrons:

$$f_B = \eta \, \bar{E}_{Bck}/E_B \, ,$$

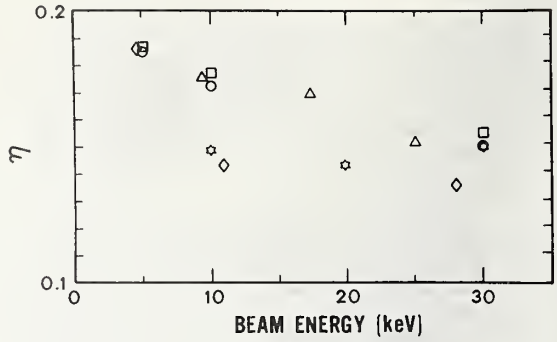
where $\bar{E}_{Bck}$ is the mean energy backscattered and E_B is the beam energy. Both $\bar{E}_{Bck}/E_B$ and η depend on the incident energy, specimen composition, the incident beam angle, and the scattering angle at which they are measured. The data reviewed here are for normal incidence and are integrated over all possible scattering angles.

There have been several experimental determinations of η using a variety of experimental techniques [71-75]. In the energy range of interest here (usually $E_B \leq 30$ keV), the fraction of electrons backscattered from aluminum or silicon is almost independent of the beam energy, E_B, as shown in figure 49.

Data on the fractional mean energy backscattered are scarce [70,76,77]. Figure 50 illustrates the variation of $\bar{E}_{Bck}/E_B$ with beam energy for electrons backscattered from aluminum. The values given by Thomas [76] were measured at 138 deg with respect to the beam direction; the average value over all backscattering angles would be greater. values of f_B for an aluminum specimen can be calculated using these values of $\bar{E}_{Bck}/E_B$ and values of η from figure 49b interpolated where necessary to obtain values at the same energies. The results, with error bars estimated on the basis of scatter in the reported data, are shown in figure 51. It is



a. Silicon. ✡, Heinrich [71]; □, Bishop [73]; △, Drescher *et al.* [75].



b. Aluminum. ✡, Heinrich [71]; O, Colby *et al.* [72]; □, Bishop [73]; ◊, Weinryb and Philibert [74]; △, Drescher *et al.* [75].

Figure 49. Ratio of backscattered to incident electrons, η, as a function of beam energy.

apparent that taking the value of f_B to be 0.1 in the range 5 to 30 keV makes no more than a 2 percent contribution to the error in calculating the energy deposited. This contribution is small in comparison to the other possible sources of error. To a first approximation for silicon specimens, values of f_B can be taken to be the same as aluminum. The results are also expected to be applicable in general to devices consisting of silicon, silicon dioxide, and aluminum. (K. F. Galloway, W. J. Keery, and K. O. Leedy)

11.4. Flying-Spot Scanner

The dual-laser flying-spot scanner (NBS Spec. Publ. 400-17, pp. 42-43) was applied to characterization of UHF power transistors and an MOS shift register. In the former it was revealed that the scanner could be used to map temperature variations over the active regions and to detect portions of the device which operate in a nonlinear manner. In the latter, the logic pattern was displayed nondestructively and it was possible to change states within the device selectively and reversibly.

The UHF transistors studied were bipolar silicon devices designed to furnish 5 W at frequencies up to 1 GHz. The surface topology is shown in the photomicrograph in figure 52. There are four in-line cells connected in parallel with a total active area 1.2 mm long and 0.15 mm wide which appears as a broad vertical stripe in the center of the figure. The emitter and base contacts are interdigitated; the emitter fingers come in from the right and the base fingers from the left. The finger metallization is 2 μm wide, and the metallization stripes are separated by 8 μm. The separation allows access of the laser to the active regions of the device.

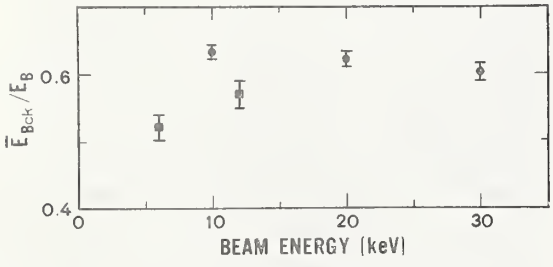


Figure 50. Fractional mean energy backscattered, $\bar{E}_{Bck}/E_B$, from aluminum as a function of beam energy, E_B. (●, Thomas [76]; ■, Darlington [77].)

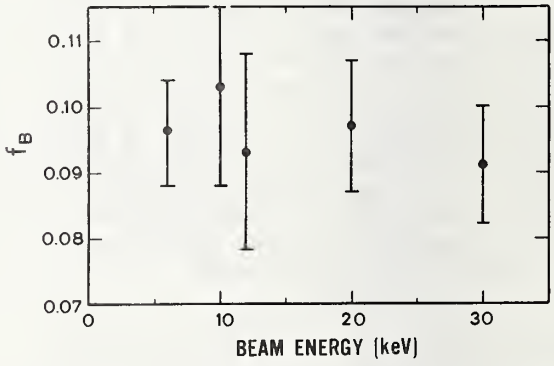


Figure 51. Fraction of incident energy backscattered, f_B, from aluminum as a function of beam energy.

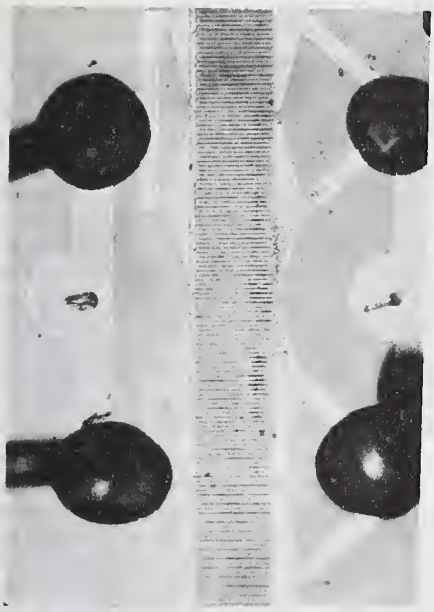


Figure 52. Photomicrograph of silicon interdigitated UHF transistor showing surface topology. (Magnification: ∿116X.)

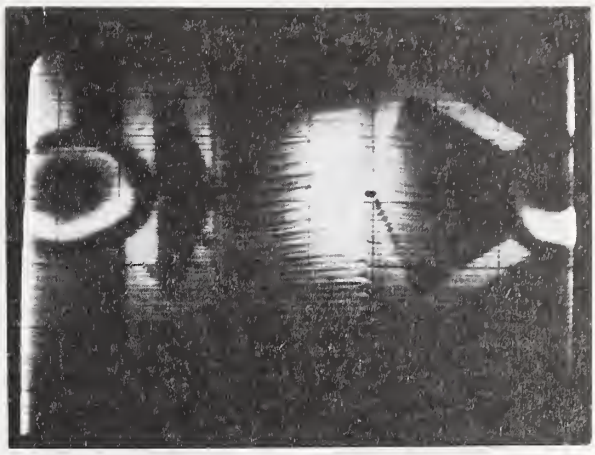


Figure 53. Photograph of the scanner display screen showing enhancement of 1.15-μm photoresponse due to hot-spot operation. (The hot-spot region is the bright region approximately in the center.)

The transistors were scanned while they were operated in a dc-biased common-emitter configuration. The collector load was 60 Ω and the voltage drop across the resistor was used to modulate the display screen. It was found that localized regions of high temperature, or hot spots, formed in several of the transistors within the operating range listed in the manufacturer's data sheet. Figure 53 is a photograph of the display screen for one of the UHF transistors scanned with the 1.15 μm laser while being operated with a collector-emitter voltage, V_{CE}, of 26 V and a collector current, I_C, of 250 mA. The display was formed by using intensity modulation to present a reflected-light image and by using intensity modulation and vertical deflection of the horizontal scan lines together to present the 1.15 μm transistor photoresponse. The hot-spot region is the bright area in the center of the photograph. The hot-spot location was confirmed using a conventional passive infrared microscope.

The enhanced photoresponse is due to the increase in absorption coefficient, α, with temperature. The absorption of monochromatic radiation varies with the distance x into silicon as exp(-αx). For single-crystal silicon at room temperature, $\alpha \simeq 0.3\ cm^{-1}$ for 1.15 μm radiation [78]. However, as the temperature is increased, the forbidden energy gap becomes smaller [79] and α increases, resulting in an increase in the number of electron-hole pairs photogenerated in the active volume of the device. Calculations relating the enhanced photoresponse to temperature-induced bandgap variations are in order of magnitude agreement with the preliminary experimental observations.

Although the results presented were obtained with static operating conditions, similar results with the transistor operating with rf drive and in its own circuit should be feasible. While these initial observations have focussed on hot-spot observations, the usefulness of the measurement technique is not restricted to hot-spots. For example, as the power dissipation was increased in the range prior to the onset of hot-spots, the normal temperature rise of the transistor was readily detected by a uniform enhancement of its photoresponse.

A transistor of the same type was used for the characterization of regions of nonlinear operation. During normal operation, lasers produce optical radiation, not at just one discrete wavelength, but with a series of discrete lines centered about the nominal wavelength. Mixing of these lines produces a partial modulation of the laser radiation in multiples of a fundamental modulating frequency. For the 0.633 μm laser used for this part of the investigation, the fundamental frequency is 500 MHz, and this 500 MHz mod-

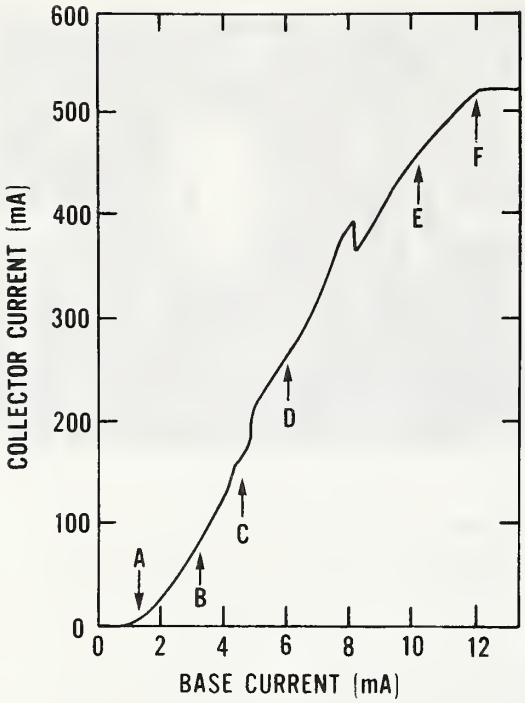


Figure 54. Collector-base characteristic of UHF transistor connected in a common-emitter circuit. (The nonlinear region in the center (D) is associated with hot-spot operation.)

ulation was used for the detection of nonlinearities. The transistor was connected in the common-emitter mode with a supply voltage of 35 V. The base current, I_B, was adjusted to allow the transistor to be biased anywhere between cutoff and a saturation current (I_C) of 520 mA. The I_C-I_B characteristic for a typical device is shown in figure 54. The deviation from linearity near the center was found to be associated with the formation of a hot spot.

The mapping of operating nonlinearities was performed by scanning the transistor with the modulated laser. A 470 MHz signal generator was coupled to the base lead and a 30 MHz intermediate frequency amplifier and detector were connected across the 60 Ω collector load resistor. The detector output was used to modulate the display screen.

If square-law nonlinearities are present within the transistor, frequency mixing of the 470 MHz signal and the 500 MHz laser modulation occurs and a 30 MHz difference frequency output is produced. The internal operating mechanism is believed to be the following: The relationship between base minority carrier density in excess of equilibrium, and the internal base current, whether this current be due to an electrical input or to photogeneration, can quite generally be represented by a power series. For devices, or device portions, which are operating linearly, the power series (exclusive of a possible constant) is a single term linear in the current and the characteristics are described by a straight line. For this case, there is no variation in the minority carrier distribution within the device at frequencies other than the two input ones, and so only these two frequencies appear in the electrical output. However, if the characteristics are not linear, frequency mixing may be detected at the output. Specifically, if the square term is present, and this is the next possible term in the power series after the linear one, frequencies which are the sum and the difference of the two inputs are produced.

If the UHF characteristics are similar to the static one shown in figure 54, then it might be anticipated that mixing would occur with the transistor biased near saturation, near cutoff (the characteristics near cutoff resemble those of a mixer diode), and perhaps in the hot-spot regime. Mixing in these regions was found to occur as indicated by the photographs of the display screen shown in figure 55. These photographs show the display at the corresponding operating points indicated by arrows in figure 54. In A, the transistor is in partial cutoff, and a strong i-f output is obtained uniformly. In B, the first linear region has been entered, and the signal has decreased. The hot-spot region has been entered in C. There actually are two hot spots, one on each side of a cell boundary, and their locations as determined with a passive infrared scanner are indicated by arrows in D. It is interesting to see that operation in the hot-spot regime can influence linearity in cells other than just the one, or ones, operating in this regime. Perhaps this is due to coupling through the collector region common to all cells. In E, the operating point is outside of the hot-spot region, and the characteristics again are fairly linear and so little mixing occurs. For the last case, F, the device is near saturation, and again strong non-linearity is observed on the display screen. Inspection of the display screen shows that the nonlinearity is more pronounced along the right-hand emitter side. Perhaps this is so because the base contact is on the left, and

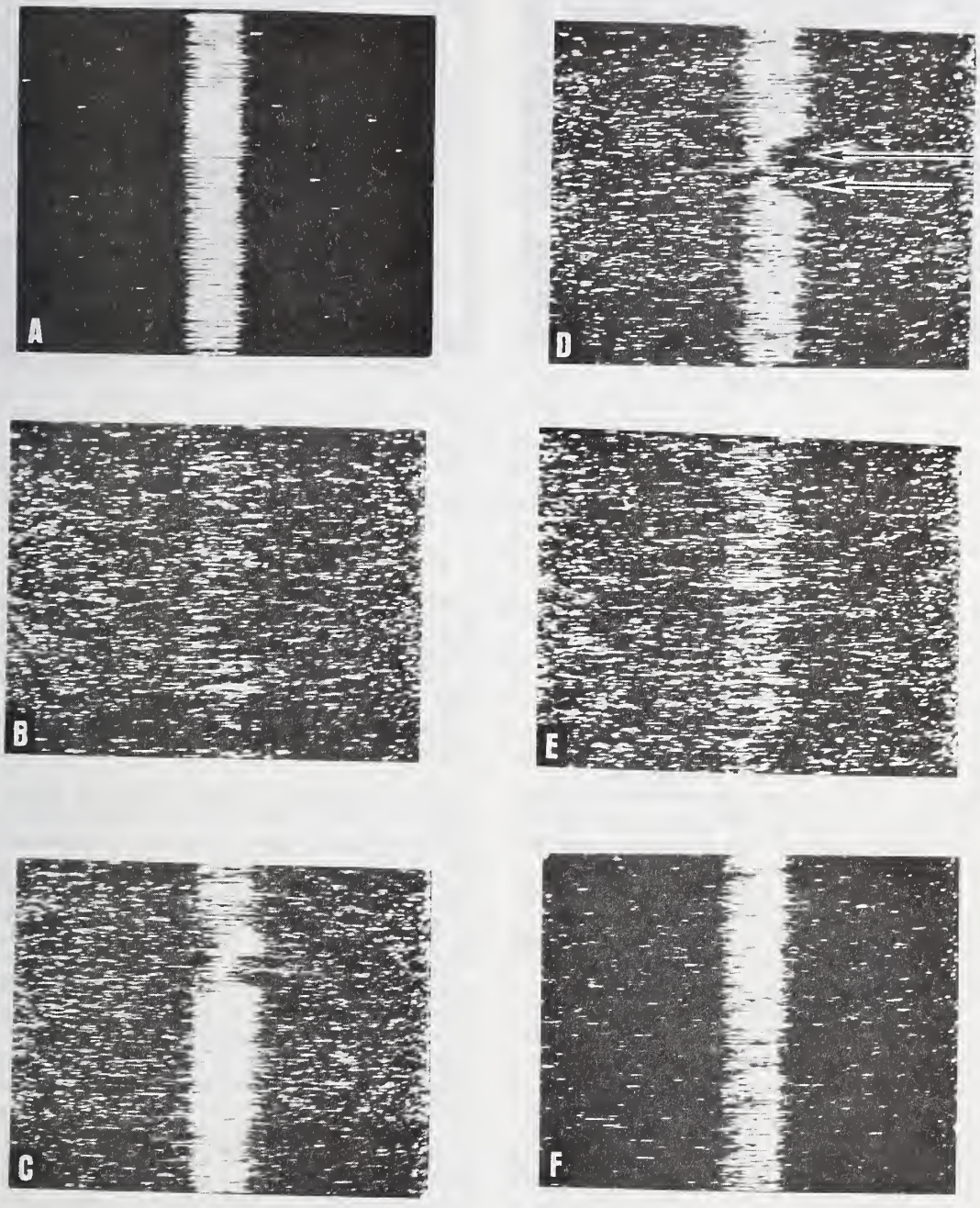
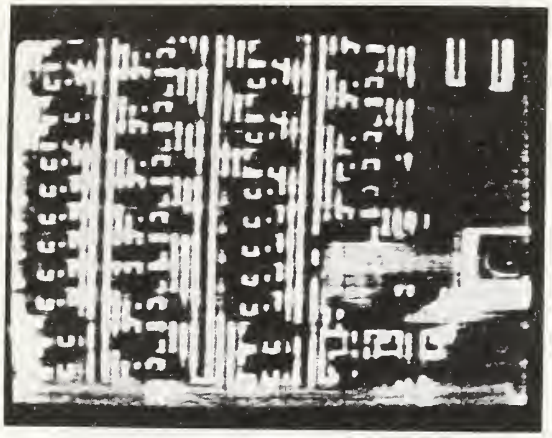
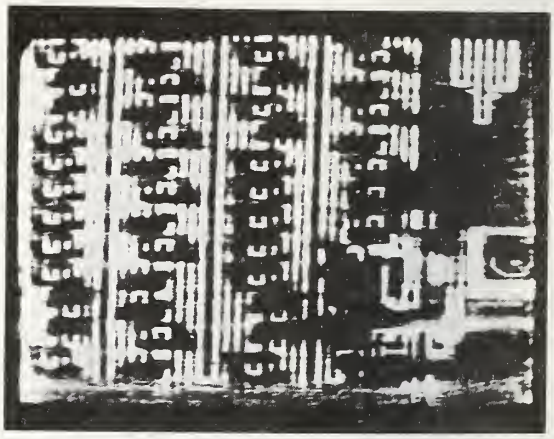


Figure 55. Photographs of the scanner display screen showing electrical nonlinearity in the UHF transistor at certain of the operating points indicated by arrows on the collector-base characteristic. (See text for discussion.)



a. Initial static condition.



b. Static condition after a single clock pulse was injected through the clock input and a logical one injected via the data input at the lower left of the figure.

Figure 56. Photographs of the scanner display screen showing a portion of a *p*-MOS shift register.

a small amount of debiasing of the right-hand emitter side is occuring due to the dc voltage drop along the base fingers.

It was also shown that the scanner can be used to observe logic information passing through an MOS shift register without altering the characteristics of the device. Previously, the scanning electron microscope has been used to examine MOS logic circuits [80], but this requires the inconvenience of inserting the circuit into and removing it from a vacuum system. Furthermore, the electron beam can cause catastrophic damage to MOS circuits especially when they are exposed under bias (NBS Spec. Publ. 400-17, pp. 43-46) unless special precautions are taken [81]. The shift register was a static dual 128-bit *p*-MOS ion-implanted device. In order to be able to observe the logic flow in the device with the laser scanner, the package leads were connected as appropriate for normal circuit operation and information which describes the circuit operation was extracted by monitoring variations in power supply current to the device.

Figure 56 shows the pictures of the displays obtained by scanning the *p*-MOS shift register with the 0.633 μm laser at low intensity. Figure 56a shows about one third of one of the 128-bit registers and some associated input/output circuitry. In the main part of the register a random pattern of logical ones and zeros which appear as displaced dark and light areas can be seen. The logic flows, in this register, along a snake-like path which begins in the left-hand column at the bottom and flows up the column, then down the second column, up the third and down the fourth, where it switches the output circuitry at the bottom of the fourth column.

Figure 56b shows the same register after a single clock pulse has been injected through the clock input and a logical 1 injected via the data input. It can be easily seen upon comparison of the two photographs how the logical ones and zeros have shifted in accordance with the clock pulse. The output has also switched states. Demonstrated here is the operation of a good device, although improper internal operation on a defective device has also been observed. When the circuit was operated with reduced power supply voltage, it was observed that some logic cells did not always function properly.

It was also found while scanning this MOS device that internal logic states can be changed nondestructively by increasing the laser intensity with the polarizer-analyzer combination in the optical system. Logical ones can be selectively changed to zeros and vice versa by decreasing the laser scan raster to a region on the logic cell where a change is desired. The laser is aimed to one side of the logic cell to change a zero to a one, and to the other side to change a one to a zero; aiming the laser is accomplished by

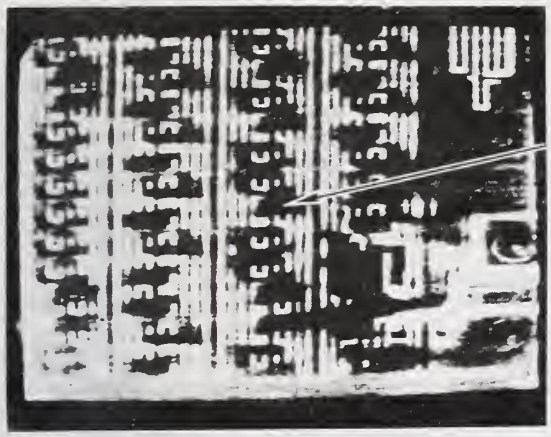


Figure 57. Photograph of the scanner display screen showing a portion of a *p*-MOS shift register in the same static condition as in figure 56b except that a logical one was changed to a logical zero (shown by the arrow) by the laser beam.

moving the device. The laser intensity is then increased to change the state of the cell, and then returned to its previous intensity. The laser raster scan then can be restored to its original size. The scan raster is decreased by electronically decreasing the excursion of the laser deflection mirrors. This operation changes only the desired cell and does not affect the state of any other cells in the register.

Figure 57 shows the register as it appeared in figure 56b except that the laser was used to change the state of the logic cell identified by the arrow. Note that no other logic cell has been changed and no input pulses were injected into the device. This ability to change internal logic states nondestructively could have far-reaching benefits in testing of LSI devices which have internal processing blocks which are not externally accessible.

(D. E. Sawyer* and D. W. Berning)

* Prof. H. P. D. Lanyon, Electrical Engineering Department, Worcester Polytechnic Institute, Worcester, Massachusetts, provided theoretical insight into effects that govern the temperature dependence of the photoresponse.

12. THERMAL PROPERTIES OF DEVICES

12.1. Thermal Resistance — Darlington Pairs

Previous work on the measurement of thermal resistance of Darlington transistors showed that the thermal resistance of the output transistor, $R_{\theta JC2}$, is given to a good approximation by

$$R_{\theta JC2} = 2R_{\theta JC(1+2)} - R_{\theta JC1} \qquad (12)$$

where $R_{\theta JC(1+2)}$ is the thermal resistance determined by measuring the series combination of both emitter-base junction voltages and $R_{\theta JC1}$ is the thermal resistance of the input transistor* (NBS Spec. Publs. 400-12, pp. 35-37, and 400-17, pp. 52-55). The experimental results reported previously were made on devices using external emitter-base shunt resistors which had magnitudes which were nearly optimum for directly measuring $R_{\theta JC1}$ and $R_{\theta JC(1+2)}$ by the emitter-only switching technique [82]. To test this relationship further, measurements were made on a specially fabricated four-terminal Darlington device† with an input diode and integrated emitter-base shunt resistors whose magnitudes and ratio were considerably less than optimum [83].

It was found that eq (12) is still valid in this instance, but that it was not possible to measure $R_{\theta JC1}$ by the emitter-only switching method using the emitter-base voltage as the temperature sensitive parameter (TSP) because the ratio of the input shunt resistance to the output shunt resistance was too small (2:1) to allow the input transistor to be turned on while the output transistor was turned off. Therefore, the collector-base voltage of the input transistor was used as the TSP to determine $R_{\theta JC1}$ with the use of the measuring circuit (NBS Spec. Publ. 400-12, pp. 35-37 connected in the grounded-base, emitter-and-collector switching mode with switches S_1 and S_4 open, switch S_2 closed, and switch S_3 set to C as shown in figure 58. During measurement, the series transistor switch Q_s is turned off and the parallel transistor switch Q_p is turned on by a clock pulse which also activates a sample-and-hold circuit (not shown) which senses the voltage between terminal C and terminal B_1. In this measuring configuration, the measuring current, I_M, has two possible parallel paths: via the collector-base junction of the transistor Q_1 or via the resistor R_1 in series with the collector-base junction of the transistor Q_2. The desired path is via Q_1, as indicated in the partial circuit diagram in figure 59. However, if R_1 is small and Q_2 is, as is usual, hotter than Q_1, a considerable amount of current may also pass through Q_2. One way to reduce the effects of the unwanted parallel paths is to make I_M larger so that the voltage drop in R_1 restricts the percentage of I_M that is diverted from Q_1. For the device studied, $R_{\theta JC1}$ as measured by this method reached a constant value for $I_M \geq 3$ mA.

The thermal resistance of the input transistor was also measured by the emitter-only switching method (with switch S_1 open, switches S_2 and S_4 closed, and switch S_3 set to E in the circuit of figure 58 by changing the lead from terminal E_2 to terminal B_2E_1 which provides direct access to the emitter-base junction of Q_1. As with discrete devices, this value of $R_{\theta JC1}$ was found to be larger than that determined using the collector-base voltage as the TSP. Although the emitter-only switching value is probably the more accurate, it would not be measurable for a three-terminal Darlington of the same internal configuration.

To study the validity of directly measuring the thermal resistance of the output transis-

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*Note that for a Darlington transistor, $R_{\theta JC1}$ is defined as the rise in temperature of the hottest spot on the input transistor divided by the total power dissipation with both transistors operating normally and $R_{\theta JC2}$ is defined as the rise in temperature of the hottest spot of the output transistor divided by the total power dissipation with both transistors operating normally. The thermal resistance of the device as a whole is taken as the larger of $R_{\theta JC1}$ or $R_{\theta JC2}$. The quantity $R_{\theta JC(1+2)}$ is an average of the thermal resistances of the input and output transistors given by the ratio of the apparent temperature rise indicated by the sum of the junction voltages to the total power dissipation.

†Type c device as defined in figure 26, NBS Spec. Publ. 400-12, p. 35.

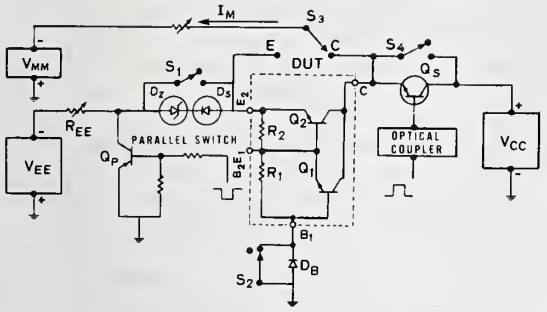


Figure 58. Modified circuit for measuring thermal resistance set up as a grounded base, emitter-and-collector switching circuit using the collector-base junction voltage of the input transistor as the temperature sensitive parameter.

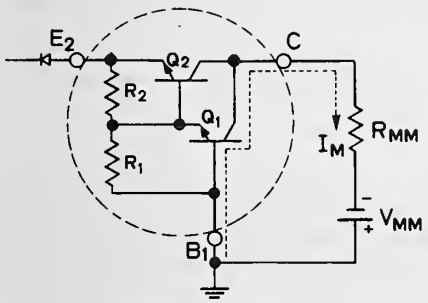


Figure 59. Desired current path when measuring the thermal resistance of the input Darlington transistor using the grounded-base, emitter-and-collector switching method with the collector-base junction voltage as the temperature sensitive parameter.

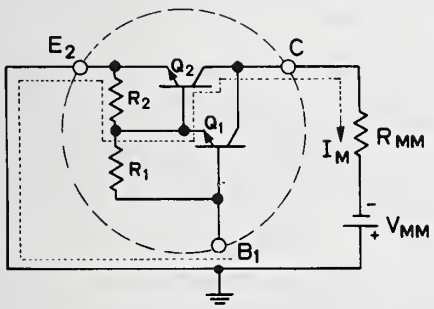


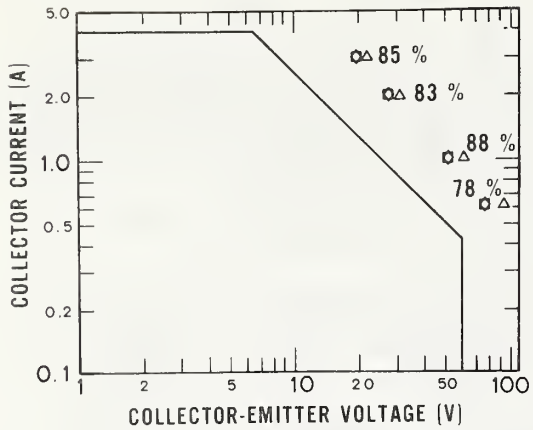
Figure 60. Desired current path when measuring the thermal resistance of the output Darlington transistor using the grounded-emitter, emitter-and-collector switching method with the collector-base junction voltage as the temperature sensitive parameter.

tor, $R_{\theta JC2}$, by using the collector-base voltage of Q_2 as the TSP this measurement was made [83] on the same four-terminal Darlington device with a range of measuring currents in the circuit of figure 58 connected in the quasi-grounded-emitter, emitter-and-collector switching mode with switches S_2 and S_4 open, switch S_1 closed, and switch S_3 set to C. The measured value ranged from 2.39°C/W for I_M = 0.5 mA to 4.16°C/W for I_M = 24 mA. The reason for this strong current dependence is the multiplicity of current paths available for the measuring current, I_M. Among the possibilities are: the series combination of the resistor R_2 and the base-collector junction of the transistor Q_2 (the desired path shown in figure 60; the series combination of the emitter-base and the base-collector junctions of Q_2; the series combination of the resistors R_2 and R_1 and the base-collector junction of the transistor Q_1; the series combination of R_2 and the emitter-base and base-collector junctions of Q_1. Conduction across the emitter-base junctions is made possible when the junctions are reverse biased by current passing through the appropriate shunt resistor. The relative fractions of current in the various paths depends on the magnitude of I_M. If a commutating diode were across the output, (as is often the case), the possibilities are even more numerous. (S. Rubin)

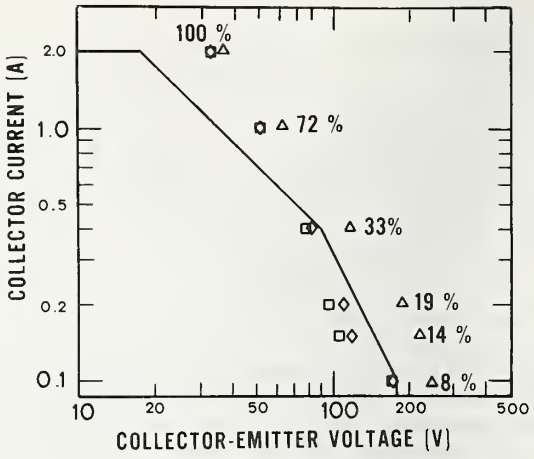
12.2. Transient Thermal Response

An electrical technique for measuring the peak junction temperature of power transistors has been developed (NBS Spec. Publs. 400-12, pp. 37-40; 400-17, pp. 55-56). The importance and utility of such a technique for determining the peak junction temperature can be seen by comparing the measured safe operating area (SOA) limits of a device with the manufacturer's published SOA.

The values of collector current, I_C, and collector-emitter voltage, V_{CE}, for which the measured junction temperature equalled the specified maximum safe junction temperature were determined by three techniques, standard electrical [82], electrical peak temperature [84], and infrared microradiometry, for a number of devices. These values of I_C and V_{CE} are compared with the manufacturer's specified SOA limits for two different devices in figure 61. The percentage of the



a. 25-W single diffused transistor



b. 35-W triple diffused transistor

Figure 61. Safe operating area plots. (Solid curves, manufacturer's specified safe operating area limits; data points, current-voltage values at which the junction temperature as measured by the infrared (□), standard electrical (△), or electrical peak (◇) technique equalled the specified maximum safe junction temperature. The percentage of available active area being used at steady state is shown for each standard electrical measurement.)

total active area of the device actually dissipating power at steady-state is noted for each point that was determined by the standard electrical technique.

The steady-state current distribution, and therefore the temperature distribution, is essentially uniform over the entire thermally limited operating range for the 25-W device. This is why the agreement between the three techniques is so good. Note that the electrical peak temperature values agree almost exactly with values determined by infrared microradiometry. The manufacturer has been rather conservative in the thermal rating of this device; the specified SOA thermal limits restrict the power that can be applied to the device to considerably less than that for which the peak junction temperature equals the maximum safe temperature (200°C).

The 35-W device exhibits severe current nonuniformities, and therefore temperature nonuniformities, over a significant portion of the specified SOA. Note that both the infrared microradiometry and electrical peak temperature techniques show that the maximum safe temperature (200°C) can be exceeded within the published SOA limits. This is shown by the points which lie to the left of the specified SOA for $I_C \leq 0.4$ A. However, the standard electrical technique would lead one to believe that the specified SOA safely limits the power over the entire range.

For both devices studied, use of the standard electrical technique would appear to permit operation at higher power than either of the other two methods. However, it is well known that the peak junction temperature cannot be measured accurately by standard electrical techniques. Consequently, when this method is used to develop the SOA, the limits are normally shifted toward lower voltages. In spite of this, the resulting limits do not guarantee that the maximum safe temperature will not be exceeded for low current-high voltage operation when current constrictions occur. On the other hand, for high current-low voltage operation, both devices studied tended to be underutilized in that more power could safely be dissipated than the specified SOA limits permit. The ability to measure the peak junction temperature by a relatively simple electrical method should enable manufacturers to generate more realistic SOA limits and also permit device users to verify more readily the specified SOA limits for particular devices and applications.

Although the sets of measurements reported were made on only one device of each type, they are in each case representative of numerous measurements made on many similar devices. (D. L. Blackburn)

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APPENDIX A

SEMICONDUCTOR TECHNOLOGY PROGRAM STAFF

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APPENDIX B

SEMICONDUCTOR TECHNOLOGY PROGRAM PUBLICATIONS

B.1. Prior Reports

A review of the early work leading to this Program is given in Bullis, W. M., Measurement Methods for the Semiconductor Device Industry — A Review of NBS Activity, NBS Tech. Note 511 (December 1969).

Progress reports covering the period July 1, 1968, through June 30, 1973, were published as NBS Technical Notes with the title, Methods of Measurement for Semiconductor Materials, Process Control, and Devices:

Quarter Ending	NBS Tech. Note	Date Issued	NTIS Accession No.
September 30, 1968	472	December 1968	AD 681330
December 31, 1968	475	February 1969	AD 683808
March 31, 1969	488	July 1969	AD 692232
June 30, 1969	495	September 1969	AD 695820
September 30, 1969	520	March 1970	AD 702833
December 31, 1969	527	May 1970	AD 710906
March 31, 1970	555	September 1970	AD 718534
June 30, 1970	560	November 1970	AD 719976
September 30, 1970	571	April 1971	AD 723671
December 31, 1970	592	August 1971	AD 728611
March 31, 1971	598	October 1971	AD 732553
June 30, 1971	702	November 1971	AD 734427
September 30, 1971	717	April 1972	AD 740674
December 31, 1971	727	June 1972	AD 744946
March 31, 1972	733	September 1972	AD 748640
June 30, 1972	743	December 1972	AD 753642
September 30, 1972	754	March 1973	AD 757244
December 31, 1972	773	May 1973	AD 762840
March 31, 1973	788	August 1973	AD 766918
June 30, 1973	806	November 1973	AD 771018

After July 1, 1973, progress reports were issued in the NBS Special Publication 400 subseries with the title, Semiconductor Measurement Technology:

Quarter Ending	NBS Spec. Publ.	Date Issued	NTIS Accession No.
September 30, 1973	400-1	March 1974	AD 775919
December 31, 1973 March 31, 1974	400-4	November 1974	COM 74-51222
June 30, 1974	400-8	February 1975	AD/A 005669
September 30, 1974	400-12	May 1975	AD/A 011121
December 31, 1974	400-17	November 1975	

B.2. Current Publications

As various phases of the work are completed, publications are prepared to summarize the results or to describe the work in greater detail. Publications of this kind which have been issued recently are listed below:

Rogers, G. J., Sawyer, D. E., and Jesch, R. L., *Semiconductor Measurement Technology:* Measurement of Transistor Scattering Parameters, NBS Spec. Publ. 400-5 (January 1975).

Lewis, D. C., On the Determination of the Minority Carrier Lifetime from the Reverse Recovery Transient of *pn*R Diodes, *Solid-State Electronics* 18, 87-91 (January 1975).

Sher, A. H., *Semiconductor Measurement Technology:* Improved Infrared Response Technique for Detecting Defects and Impurities in Germanium and Silicon *p-i-n* Diodes, NBS Spec. Publ. 400-13 (February 1975).

Jerke, J. M., Development of Dimensional Measurement Techniques from 1 to 10 Micrometers and Application to Optical Microscope Measurements, Winter Symposium '75 on Micro-Photofabrication, Society of Photographic Scientists and Engineers, Palo Alto, California, February 6-7, 1975, Paper C2.

Ciarlo, D. R., and Schultz, P. A., Automated/C Photomesh Inspection Technologies, Winter Symposium '75 on Micro-Photofabrication, Society of Photographic Scientists and Engineers, Palo Alto, California, February 6-7, 1975, Paper C4.

Blackburn, D. L., An Electrical Technique for the Measurement of the Peak Junction Temperature of Power Transistors, *13th Annual Proceedings, Reliability Physics 1975*, Las Vegas, Nevada, April 1-3, 1975, pp. 142-150 (IEEE Cat. No. 75-CHO 931-6 PHY).

Blackburn, D. L., and Oettinger, F. F., Transient Thermal Response of Measurements of Power Transistors, *IEEE Trans. Industrial Electronics and Control Instrumentation* IECI-22, 134-141 (May 1975).

Galloway, K. F., Keery, W. J., and Leedy, K. O., Integrated Circuit Damage Resulting from SEM Examination, *Proc. 25th Annual Electronic Components Conference*, Washington, D. C., May 12-14, 1975, pp. 263-266.

Buehler, M. C., David, J. M., Mattis, R. L., Phillips, W. E., and Thurber, W. R., Planar Test Structures for Characterizing Impurities in Silicon, *Extended Abstracts* of the Meeting of the Electrochemical Society, Toronto, Ontario, May 11-16, 1975, pp. 403-404.

Rubin, S., Thermal Resistance Measurements on Monolithic and Hybrid Darlington Power Transistors, *PESC '75 Record, IEEE Power Electronics Specialists Conference 1975*, Culver City, California, June 9-11, 1975, pp. 252-261 (IEEE Cat. No. 75-CHO 965-4 (AES).

Kraft, R., Finite Difference Techniques for Diffusion and Redistribution Problems with Segregation-type Boundary Conditions, *Proceedings of the AICA International Symposium on Computer Methods for Partial Differential Equations*, Lehigh University, Bethlehem, Pa., June 17-19, 1975, pp. 328-334.

Jerke, J. M., *Semiconductor Measurement Technology:* Optical and Dimensional-Measurement Problems with Photomasking in Microelectronics, NBS Spec. Publ. 400-20 (October 1975).

Lieberman, A. G., Problems in Using Surface Analysis Techniques for the Depth Profiling of Microelectronic Materials, *Technical Digest, 1975 International Electron Devices Meeting*, Washington, D.C., December 1-3, 1975, pp. 126-129 (IEEE Cat. No. 75-CH 1023 1ED).

Sawyer, D. E., and Berning, D. W., Laser Scanning of Active Semiconductor Devices, *Technical Digest, 1975 International Electron Devices Meeting*, Washington, D. C., December 1-3, 1975, pp. 111-114 (IEEE Cat. No. 75-CH 1023 1ED).

Buehler, M. G., David, J. M., Mattis, R. L., Phillips, W, E., and Thurber, W. R., *Semiconductor Measurement Technology:* Planar Test Structures for Characterizing Impurities in Silicon, NBS Spec. Publ. 400-21 (December 1975).

Pease, R. L., Galloway, K. F., and Stehlin, R. A., Radiation Damage to Integrated Injection Logic Cells, *IEEE Trans. Nucl. Phys.* NS-22, 2600-2604 (December 1975).

B.3. Availability of Publications

In most cases reprints of articles in technical journals may be obtained on request to the author. NBS Technical Notes and Special Publications are available from the Superintendent of Documents, U.S. Government Printing Office, Washington, D. C. 20402, or the National Technical Information Service, Springfield, Virginia 22161, or both. Current information regarding availability of all publications issued by the Program is provided in the latest edition of NBS List of Publications No. 72 which can be obtained on request to Mrs. E. C. Cohen, Room B346, Technology Building, National Bureau of Standards, Washington, D. C. 20234.

B.4. Videotapes

Color videotape cassette presentation on improvements in semiconductor measurement technology are being prepared for the purpose of more effectively disseminating the results of the work to the semiconductor industry. These videotapes are available for distribution on loan without charge on request to Mrs. E. C. Cohen, Room B346, Technology Building, National Bureau of Standards, Washington, D. C. 20234. Copies of these videotapes may be made and retained by requestors. Two videotapes, Defects in PN Junctions and MOS Capacitors Observed Using Thermally Stimulated Current and Capacitance Measurements, by M. G. Buehler, and Laser Scanning of Active Semiconductor Devices, by D. E. Sawyer and D. W. Berning, have been completed and released for distribution. As an added feature, arrangements can be made for the authors to be available for a telephone conference call to answer questions and provide more detailed information, following a prearranged showing of either of the videotapes.

APPENDIX C

WORKSHOP AND SYMPOSIUM SCHEDULE

C.1. Proceedings or Reports of Past Events:

Symposium on Silicon Device Processing, Gaithersburg, Maryland, June 2-3, 1970. (Cosponsored by ASTM Committee F-1 and NBS). Proceedings: NBS Spec. Publ. 337 (November 1970).

ARPA/NBS Workshop I. Measurement Problems in Integrated Circuit Processing and Assembly, Palo Alto, California, September 7, 1973. Report: NBS Spec. Publ. 400-3 (January 1974).

ARPA/NBS Workshop II. Hermeticity Testing for Integrated Circuits, Gaithersburg, Maryland, March 29, 1974. Report: NBS Spec. Publ. 400-9 (December 1974).

Spreading Resistance Symposium, Gaithersburg, Maryland, June 13-14, 1974. (Cosponsored by ASTM Committee F-1 and NBS). Proceedings: NBS Spec. Publ. 400-10 (December 1974).

ARPA/NBS Workshop III. Test Patterns, Scottsdale, Arizona, September 6, 1974. Report: NBS Spec. Publ. 400-15 (February 1976).

ARPA/NBS Workshop IV. Surface Analysis for Silicon Devices, Gaithersburg, Maryland, April 23-24, 1975. Proceedings: NBS Spec. Publ. 400-23 (March 1976).

Reliability Technology for Cardiac Pacemakers, Gaithersburg, Maryland, July 28-29, 1975. (Cosponsored by Food and Drug Administration and NBS). Report: NBS Spec. Publ. 400-28 (to appear).

APPENDIX D

STANDARDS COMMITTEE ACTIVITIES

ASTM Committee F-1 on Electronics

J. H. Albers, Secretary, Packaging Subcommittee; Hybrid Microelectronics Subcommittee

M. G. Buehler, Chairman, Task Force on Test Patterns, Process Controls Section; Semiconductor Crystals, Semiconductor Processing Materials, Semiconductor Measurements, and Quality and Hardness Assurance Subcommittees

*W. M. Bullis, Secretary; Editor, Semiconductor Crystals Subcommittee

J. R. Ehrstein, Chairman, Resistivity Section; Semiconductor Crystals, Semiconductor Processing Materials, Semiconductor Measurements, and Quality and Hardness Assurance Subcommittees

*J. C. French, Chairman, Editorial Subcommittee

G. G. Harman, Secretary, Interconnection Bonding Section; Hybrid Microelectronics, and Packaging Subcommittees

K. O. Leedy, Chairman, Packaging Subcommittee; Chairman, Interconnection Bonding Section; Semiconductor Crystals, Semiconductor Processing Materials, Semiconductor Measurements, Hybrid Microelectronics, and Quality and Hardness Assurance Subcommittees

T. F. Leedy, Semiconductor Crystals, Semiconductor Processing Materials, Semiconductor Measurements, and Quality and Hardness Assurance Subcommittees

D. C. Lewis, Laser, Semiconductor Crystals, Semiconductor Processing Materials, Semiconductor Measurements, Hybrid Microelectronics, Packaging, and Quality and Hardness Assurance Subcommittees

*C. P. Marsden, Honorary Chairman

R. L. Mattis, Editor, Semiconductor Measurements Subcommittee; Semiconductor Crystals, and Semiconductor Processing Materials Subcommittees

*J. F. Mayo-Wells, Secretary, Editorial Subcommittee

D. B. Novotny, Editor, Semiconductor Processing Materials Subcommittee; Semiconductor Crystals and Packaging Subcommittees

W. E. Phillips, Chairman, Lifetime Section; Secretary, Semiconductor Crystals Subcommittee; Semiconductor Processing Materials, Semiconductor Measurements, and Hybrid Microelectronics Subcommittees

G. J. Rogers, Lasers and Quality and Hardness Assurance Subcommittees

S. Ruthberg, Chairman, Hermeticity Section; Hybrid Microelectronics, and Packaging Subcommittees

*R. I. Scace, First Vice-Chairman

*H. A. Schafft, Publicity Officer

A. H. Sher, Semiconductor Crystals, Semiconductor Processing Materials, Semiconductor Measurements, Hybrid Microelectronics, Packaging, and Quality and Hardness Assurance Subcommittees

W. R. Thurber, Semiconductor Crystals and Semiconductor Measurements Subcommittees

ASTM Committee E-10 on Radioisotopes and Radiation Effects

W. M. Bullis, Subcommittee 7, Radiation Effects on Electronic Materials

J. C. French, Subcommittee 7, Radiation Effects on Electronic Materials

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*All subcommittees.

D. C. Lewis, Subcommittee 7, Radiation Effects on Electronic Materials

R. I. Scace, Subcommittee 7, Radiation Effects on Electronic Materials

Electronic Industries Association: Solid State Products Division, Joint Electron Device Engineering Council (JEDEC)

D. L. Blackburn, Task Group JC-25-5 on Thermal Characterization on Power Transistors, and Committee JC-25 on Power Transistors

F. F. Oettinger, Chairman, Task Group JC-25-5 on Thermal Characterization on Power Transistors, Committee JC-25 on Power Transistors; Technical Advisor, Thermal Properties of Devices, Committees JC-13.1 on Government Liaison for Discrete Semiconductor Devices, and JC-22 on Rectifier Diodes and Thyristors

S. Rubin, Chairman, Council Task Group on Galvanomagnetic Devices

D. E. Sawyer, Task Group JC-24-5 on Transistor Scattering Parameter Measurement Standard, Committee JC-24 on Low Power Transistors

H. A. Schafft, Technical Advisor, Second Breakdown and Related Specifications Committee JC-25 on Power Transistors

IEC TC47, Semiconductor Devices and Integrated Circuits

S. Rubin, Technical Expert, Galvanomagnetic Devices; U.S. Specialist for Working Group 5 on Hall Devices and Magnetoresistive Devices

IEEE Electron Devices Group

J. C. French, Standards Committee

F. F. Oettinger, Standards Committee Task Force on Second Breakdown Measurement Standards

H. A. Schafft, Standards Committee Task Force on Second Breakdown Measurement Standards

IEEE Magnetics Group

S. Rubin, Chairman, Galvanomagnetic Standards Subcommittee

Semiconductor Equipment and Materials Institute

R. I. Scace, Standards Committee

Society of Automotive Engineers

W. M. Bullis, Planning Subcommittee of Committee H on Electronic Materials and Processes

J. C. French, Subcommittee A-2N on Radiation Hardness and Nuclear Survivability

F. F. Oettinger, Steering Committee, Electronic Systems Committee

APPENDIX F

AUTOMATED INTEGRATED CIRCUIT PROCESSING AND ASSEMBLY*

A study was conducted to review automated procedures for integrated circuit (IC) processing and assembly, forecast future trends or directions expected in this technology, and identify economic and technological factors which at this time appear to inhibit or delay the development of such automated procedures. In this context the following were examined:

1. the susceptibility of existing process technologies to automation;

2. the present status of automation at various stages of production within the IC industry, here including both device manufacturers and manufacturers of processing equipment;

3. the impact which emerging process technologies are likely to have on automation in the future;

4. the status of development of the measurement technology needed for control of automated processes, and the availability of equipment to perform such measurements;

5. the business, economic, and technological factors which may inhibit or delay the advent of automated processes; and

6. the priorities for automating various key process and assembly functions and the criteria appropriate for developing these priorities.

The study identified certain areas of importance for further automation of IC production. The primary emphasis of this study of automation was its application to the processing of wafers for integrated circuits and the assembly of chips from these wafers into devices. Thus, other areas of automation also applicable to semiconductors or the circuit design of ICs were only given minor attention or excluded.

Information for the study was obtained from field visits, interviews, and analysis of in-house data on the basis of which subjects especially relevant to automated IC processing and assembly were identified. Discussions were restricted to information which respondents felt was not proprietary and not confidential. In this connection over 20 commercial IC manufacturers were visited regarding the automation and measurements used in IC production and how they intend to apply automation in the areas under study in the future; 15 other laboratory or pilot IC fabrication facilities were visited to discuss their special needs for automation and measurements in IC manufacture; and relevant equipment, such as processing equipment, production automation systems and services, measuring equipment, and test systems were reviewed.

Many IC manufacturers considered the automation of their production an important subject with certain details held proprietary. Nevertheless, in general respondents were quite willing to discuss information on measurements and automation which are normally shown to interested customer-visitors and where a description of capabilities on ongoing research might enhance their own marketing efforts, such as new research already published, processing equipment or systems for sale, controls included in detailed purchase specifications, and trends in automation on a broad and general basis. The helpful cooperation of many individuals in the industry was essential to the conduct of the study and is gratefully acknowledged.

Today, some 80 to 130 steps are used in manufacturing ICs. Many of these are repeated, so that about 20 to 30 basic unit processes or operations are used. The differing susceptibility of various unit operations has led to differing status in regard to the degree of

*This study was conducted by Arthur D. Little, Inc., Cambridge, Mass., under NBS Contract No. 4-35807. The views and conclusions expressed herein are those of the author and should not be interpreted as necessarily representing the official position, either expressed or implied, of the Defense Advanced Research Projects Agency or the National Bureau of Standards. This summary is presented in preliminary form both to provide feedback to the industry and to elicit comments, pro or con, from the industry. Comments should be addressed to W. M. Bullis, National Bureau of Standards, Washington, D. C. 20234.

automation. It was found that automation has only been applied to those unit operations where positive results of control were demonstrable, technologies were feasible and available, automation appeared necessary or desirable, economics were favorable, and management interest and business climate were positive.

Although many process steps now are extensively mechanized, only a few steps are automated to a high degree of control. The increasing mechanization of handling has improved process consistency. This provides an approach toward a smooth flow of product wafers, chips, and devices and has aided efficient and rapid processing and facilitated measurement and data collection on a similar mechanized basis. The higher throughput per equipment also has improved the economics of measurement and processing.

There is a general trend towards automation of individual unit processes. The least automated process steps are etching and cleaning steps which are still difficult to control at all. In other processes the processing conditions are kept constant with sensitive analog measurements and feedback control, such as for temperature, gas flow, or bonding pressures. Here open-loop control is the best solution at this time. This allows one to freeze the process or assembly conditions with individual regulators or feedback controls. The final device characteristics cannot yet be measured accurately enough or results are still too inconsistent for use of parameter measurements in closed-loop control. Only in a few instances has closed-loop automation been applied to control some parameter of the IC crystal, wafer, device, or contacts.

Automation is being applied to the sequencing and control of the process variables, or to the data collection and analysis of status. Automation of time and program sequence control is becoming prevalent, and a few automated data collection systems are now being introduced. At present, these two automation approaches have been coupled only in the case of crystal growing. Although there are only a few computer-controlled systems in use, there is large and widespread interest in computer control and many in the industry specify computer compatability for all new equipment.

It was found that highly automated electronic test equipment is available for the measurement of IC and test pattern characteristics. Several IC manufacturers are now extensively automating the collection and analysis of electrical measurements from test pattern chips measured at the completion of wafer processing with the hope that results from these measurements will provide improved understanding and control of the processes as well as means for further automation.

Other in-process parameters which are now routinely measured on wafers include the sheet resistance or resistivity and thickness of silicon layers, the thickness of dielectric layers, and the electrical characteristics of simple transistors and MOS capacitors. The impossibility of measuring the wafer, chip, or device during many processes generally rules out closed-loop control except via post-process parameter measurements. The latter are limited by problems of electrical contacting, optical instrument complexity, the minute dimensions involved, and inability to profile a wafer surface in depth nondestructively.

A number of in-process parameter measurements could become suitable for closed-loop automatic control with greater measurement accuracy or improved methods of instrumentation. Among the parameters of interest are epitaxial layer thickness and composition, oxide layer thickness and composition, transistor base width, MOS transistor load resistors and threshold voltage, photoresist exposure, completion of etching of layers, and contact and bond characteristics.

Inspection and defect analysis after many photolithographic steps is presently carried out visually by operators. This is highly subjective, not consistent, and very costly. Visual inspection at many IC manufacturers requires as many as 20 percent of all direct production workers.

Based on the above findings several conclusions were reached:

1. *There are significant needs and opportunities for further extending and enhancing the automation of IC production that go beyond the present status.* There is no overall automated production system yet in sight to cover most processing or assembly steps. Mutual compatability of unit equipment and overall system integration will require considerable further development and standardization. Among the technological factors likely to retard the adoption of

automation are the lack of correlation between some process variable measurements and product parameters and characteristics, present difficulties in measuring the thickness of dielectric or oxide layers especially in windows to be etched, limited accuracy and range of the measurement of desired process variables, long throughput time of wafer and device production, which delays the feedback of measurement results for corrective action or closed-loop control, lack of measurement equipment providing suitable accuracy and reliability for use in a production environment, lack of standardization for sequence control and data acquisition, too long a delay between a process step and the measurements such as on test patterns, and the potential displacement by alternative emerging processes.

Economic factors likely to inhibit automation in the future are the high cost of most automation equipment, computers, and their software. Other factors are the cost and time required for the development of automation, difficulties in evaluating possible cost savings, and accounting and organizational conditions. On the other hand, business pressures continue on the IC industry for increased and more flexible production at lower cost and scrap. Thus investments in additional automation are being considered and approved.

2. *Measurements are important for automation.* Each present improvement in automation has resulted from significant progress in measurement and control techniques. Present industry emphasis on freezing process variables focuses immediate attention on measuring process variables with requirements for greater accuracy of presently measured variables and new techniques for those now not routinely measured.

   For a number of state-of-the-art devices industry is using closed-loop control of the most critical product parameter, requiring in-process measurement of such parameters as of MOS threshold voltages, high resistivity for transistor loads, narrow base widths, or line widths of critical patterns. These uses are generally rather limited; more widespread policies of measuring product parameters in-process primarily for monitor purposes and indications of error or alarm have caused an unwarranted stagnation in the interest for improved measuring equipment for production use. However, it is important to note that improved methods of measurements and rapid evaluation of measurement data are needed for process control in future automated production and that several emerging processes use different technologies and require other physical principles of measurement than were used in production heretofore. Among the quantities involved are ion beam currents, dopant vapor pressures, etching rates of new etching media, alignment errors, photoresist sensitivity, laser position, and bonding pressure.

   Many new measurement techniques now being developed by industry or at NBS are applicable to research and development as contrasted with production of ICs. To be also applicable to the automation of production processes, new measurement techniques must provide non-destructive readings, high accuracy and consistency, and rapid availability of data, measured on reliable equipment.

3. *Industry's movements in two opposite directions regarding measurements on test patterns and monitor wafers are not incompatible.* On the one hand, appreciable effort is placed in the development and use of test patterns preceding wafer probe tests, to overcome deficiencies perceived with present monitor wafer measurements. On the other hand, respondents show strong interest in improving methods and techniques of measuring in-process wafer parameters on product or monitor wafers, to provide more accuracy and versatility even in the production environment.

   In favor of test patterns are the following:

   (1) contacting problems are avoided, with better accuracy;

(2) automated equipment can measure many different parameters on appropriately designed test patterns;

(3) extensive data analysis facilities are available in the equipment;

(4) the computer system easily makes corrections for calibration curves, temperature, or other influences; and

(5) there is considerable silicon and labor saving if monitor wafers are eliminated.

In favor of monitor wafer measurements are:

(1) smaller companies can afford the less expensive equipment;

(2) with new processes, measurements can be made during a run instead of waiting;

(3) short enough turn around time might never be attained to permit utilization of test pattern measurements for process control and automation;

(4) monitor wafers will still be needed to control errors immediately; and

(5) continuity with prior experience and intuition is preserved.

Both approaches are necessary and useful.

4. *Measurements of geometrical variations of parameters are important.* For IC and LSI processing, a number of areas have become important which relate to the distribution of defects on chips and wafers, and to the profiles of composition in depth of the several layers. Thus there is interest in industry in such topics as:

(1) measurement of defects now recorded by microscopic visual inspection, ranging from bare wafers to those in process, to bonded and metallized chips;

(2) recording and evaluating the variations of the many types of measurements over the geometry of chips, wafers, and lots;

(3) utilizing data analysis, correlation techniques, and display methods to treat the accumulation of measurements and statistical data, especially to evaluate geometrical variations;

(4) developing non-contacting scanning methods for wafer and chip evaluation;

(5) improving techniques of avoiding contact errors in conventional probe measurements, such as of resistance and capacitance; and

(6) depth-profiling of parameters by electrical and optical or other means, including capacitance-voltage profiling.

5. *The requirements on control of automation for production of ICs for commercial and DOD use are sometimes divergent.* Commercial priority is placed on high volume production for lowest component cost. This approach involves use of automated production to maximize yields and minimize labor, material, and production costs. Priority for DOD end use is the quick certain delivery of small quantities of very reliable devices to minimize system, maintenance and repair costs, with considerable documentation of test results, lot production information, and inspections. These needs are served by automated production to minimize elapsed time and engineering effort at both component and system levels, retain all data to provide traceability of information, and facilitate prompt re-manufacture at an undetermined later time.

(H. G. Rudenberg*)

*Arthur D. Little, Inc.

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15. SUPPLEMENTARY NOTES

16. ABSTRACT *(A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.)*

This progress report describes NBS activities directed toward the development of methods of measurement for semiconductor materials, process control, and devices. Both in-house and contract efforts are included. The emphasis is on silicon device technologies. Principal accomplishments during this reporting period included (1) completion and analysis of an interlaboratory evaluation of standard reference wafers for resistivity measurement by the four-probe method, (2) analysis of the effect of finite contact size on sheet resistance as measured with a van der Pauw structure, (3) calculation of errors introduced in measuring line width with typical microscope systems, (4) development of procedures for predicting the magnitude of electron beam induced current in silicon device structures, (5) application of the optical flying-spot scanner to observation of hot spots and non-linearities in rf power transistors and of logic patterns in an MOS shift register, and (6) determination of a more accurate electrical method, based on peak junction temperature measurement, for establishing safe operating area curves for medium power transistors. Also reported are the results of work on spreading resistance measurements, ionization of dopant impurities in silicon, Rutherford backscattering measurements, X-ray photoelectron spectroscopy, ion microprobe mass analysis, tests for determining the surface quality of sapphire substrates, reevaluation of Irvin's curves, mathematical models of dopant profiles, deep depletion measurements of resistivity profiles, measurement of epitaxial layer thickness by the deep depletion method, bias-temperature stress test measurements on MOS capacitors, a high voltage capacitance-voltage method for measuring characteristics of thick insulator films, ion implantation parameters, methods for determining integrity of passivation overcoats, optical imaging and calibration standards for photomask metrology, line-width measurements, charge-coupled device test structures, test pattern design and analysis for silicon on sapphire MOS device technologies, nondestructive acoustic emission test for beam-lead bonds, pull and shear tests for wire bonds, a rapid cycle dry gas gross leak test, leak detection by helium mass spectrometry, correlation of moisture infusion in semiconductor packages with leak size and device reliability, an automated scanning low-energy electron probe, electron beam induced damage in silicon device structures, and thermal resistance measurements on Darlington transistors. Supplementary data concerning staff, publications, workshops and symposia, standards committee activities, and technical services are also included as appendices. A sixth appendix is included to summarize the results of a study which was carried out to assess the impact of automation of integrated circuit processing and assembly on future measurement requirements in the industry.

17. KEY WORDS *(six to twelve entries; alphabetical order; capitalize only the first letter of the first key word unless a proper name; separated by semicolons)*

Acoustic emission; beam-lead bonds; bias-temperature stress test; boron redistribution; capacitance-voltage methods; charge-coupled device structures; Darlington pairs; deep depletion; dopant profiles; electrical properties; electron beam induced current; electron beam induced damage; electronics; epitaxial layer thickness; four-probe method; hermeticity; leak tests; measurement methods; microelectronics; moisture infusion; optical flying-spot scanner; oxide films; passivation overcoats; photomask metrology; pull test; resistivity; Rutherford backscattering; scanning electron microscope; scanning low energy electron probe; semiconductor devices; semiconductor materials; semiconductor process control; shear test; sheet resistors; silicon; silicon on sapphire; spreading resistance; test patterns; thermal resistance; thermal response; transistors; ultrasonic bonding; wire bonds; X-ray photoelectron spectroscopy.

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