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U.S. DEPARTMENT OF COMMERCE / National Bureau of Standards

Semiconductor Measurement Technology:

ARPA/NBS Workshop III. Test Patterns for Integrated Circuits

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Test Patterns for Integrated Circuits

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PREFACE

The workshop on test patterns for integrated circuits was conducted as part of the Semiconductor Technology Program in the Electronic Technology Division of the National Bureau of Standards (NBS). This Program serves to focus NBS efforts to enhance the performance, interchangeability, and reliability of discrete semiconductor devices and integrated circuits through improvements in measurement technology for use in specifying materials and devices in national and international commerce and for use by industry in controlling device fabrication processes. Its major thrusts are the development of carefully evaluated and well documented test procedures and associated technology and the dissemination of such information to the electronics community. Application of the output by industry will contribute to higher yields, lower cost, and higher reliability of semiconductor devices. The output provides a common basis for the purchase specifications of government agencies which will lead to greater economy in government procurement. In addition, improved measurement technology will provide a basis for controlled improvements in fabrication processes and in essential device characteristics.

The Program receives direct financial support principally from three major sponsors: the Defense Advanced Research Projects Agency (ARPA), the Defense Nuclear Agency (DNA), and the National Bureau of Standards. The ARPA-supported portion of the Program, Advancement of Reliability, Processing, and Automation for Integrated Circuits with the National Bureau of Standards (ARPA/IC/NBS), addresses critical Defense Department problems in the yield, reliability, and availability of integrated circuits. The DNA-supported portion of the Program emphasizes aspects of the work which relate to radiation response of electron devices for use in military systems. There is considerable overlap between the interests of DNA and ARPA. Measurement oriented activity appropriate to the mission of NBS is a critical element in the achievement of the objectives of both other agencies.

Essential assistance to the Program is also received from the semiconductor industry through cooperative experiments and technical exchanges. NBS interacts with industrial users and suppliers of semiconductor devices through participation in standardizing organizations; through direct consultations with device and material suppliers, government agencies, and other users; and through periodically scheduled symposia and workshops. This report describes the results of the third workshop in the ARPA/NBS workshop series. In addition, progress reports are regularly prepared for issuance in the NBS Special Publication 400 sub-series. More detailed reports such as state-of-the-art reviews, literature compilations, and summaries of technical efforts conducted within the Program are issued as these activities are completed. Reports of this type which are published by NBS also appear in the Special Publication 400 sub-series. Announcements of availability of all publications in this sub-series are sent by the Government Printing Office to those who have requested this service. A request form for this purpose may be found at the end of this report.

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Test Patterns for Integrated Circuits

Harry A. Schafft, Editor

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Test Patterns for Integrated Circuits

by

Harry A. Schafft, Editor

Synopses are presented of talks and discussion periods at a meeting on the use and development of MOS and bipolar test patterns and associated data acquisition systems. The discussions revealed that device manufacturers and users are making increased use of test patterns as powerful new measurement tools that can electrically monitor various process parameters to aid in the control of materials, wafer processes, circuit performance, and reliability. However, the large volume of data generated from these test patterns and the requirement for rapid diagnostic feedback present severe challenges in data management and display. In this report several data acquisition systems are described, as are approaches for presenting data in more easily interpretable graphic displays. The need for improvements in the design of test patterns is emphasized. In particular, problems with measuring contact resistance and the properties of oxides, surfaces, and defects are identified. Numerous test structures are described including charge coupled device structures which can measure some characteristics not easily measured by other means. Also described are NBS's efforts and plans to identify, analyze, and intercompare selected test structures of value to the industry and its customers, and to develop measurement methods for use with these structures.

Key Words: Data acquisition; data display; integrated circuits; measurement technology; microelectronics; process control; reliability; semiconductors; silicon; test patterns.

1. Introduction

The purpose of the workshop held on September 6, 1974 in Scottsdale, Arizona, was to promote an interchange among various industrial and government organizations leading to a better understanding of the present and future usage of test patterns. Test patterns are special structures included on silicon wafers used in integrated circuit production. These structures permit electrical measurements to be made from which information may be gleaned about wafer processing steps, circuit performance, and circuit reliability.

Test patterns may consist of specially designed structures to test such process steps as diffusion, etching, and alignment; or they may consist of selected device elements in the circuit itself that are accessed by altering the circuit metallization. Many names have been given to test patterns in the two categories. A partial listing of names compiled by M. G. Buehler of NBS is as follows: In the first category there are test patterns, test coupons, test chips, test pattern pellets, reliability test sites, reliability evaluation devices, process control bars, process control test chips, and material evaluation test chips. In the

second category there are kit parts, metal breakouts, and expanded metallization test chips.

Despite the wide use of test patterns, there has been little interchange among various industrial and government organizations which would lead to improved effectiveness of test patterns as measurement tools and to their broad application. Both government and industry would benefit from a better knowledge of the capabilities and limitations of these measurement tools. Furthermore, they may acquire increased importance in their possible wide use as vehicles for qualifying wafer lots, making all the more important well-evaluated, optimally-designed, standard test patterns.

Dr. Martin G. Buehler, who heads the NBS effort on test patterns, organized the technical program of the workshop and served as workshop chairman. The workshop featured invited talks and open discussion and question periods on the use and development of MOS and bipolar test patterns, and on data acquisition systems for both production and laboratory environments. The workshop served to expand on the material in a Mini-Symposium on Semiconductor Test Patterns[1] which was conducted in January 1974 by the ASTM Committee F-1 on Electronics. ASTM efforts in test patterns have continued with the creation of a task force, headed by Buehler, to evaluate various test pattern structures useful for radiation hardness and quality assurance, and to recommend standard test structures for manufacturers and their customers.

In this report, the eight invited talks and four extended discussion periods from the workshop are grouped into four sections similar to the way they were arranged at the workshop and are presented in synopsis form. The discussion period subsections also include synopses of the material covered in the brief question periods that were held after each of the talks of the section.

The synopses of the talks and discussion periods were largely prepared from tape transcripts. In some cases, written materials supplied by the author was used either in place of or in addition to the transcripts. The synopses of the individual presentations represent the work and opinions of the speakers who have examined and approved them. In most cases the figures shown are those provided by the speakers; otherwise they have been developed from materials supplied by the speakers.

The workshop was the third of a series of meetings intended to address various semiconductor measurement technology problems. It was attended by 76 engineers and scientists representing 24 organizations from the semiconductor industry and the federal government. These workshops are a part of an effort, Advancement of Reliability, Processing, and Automation for Integrated Circuits with the National Bureau

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[1]The Mini-Symposium was organized and chaired by Earl W. Riggs, U.S. NAD Crane, Dept. FLSD, Code 7024, Bldg. 2906, Crane, Indiana 47522. A paper presented by Dr. Buehler has been published [1]. Requests for other papers presented may be directed to Mr. Riggs.

of Standards, sponsored by the Defense Advanced Research Projects Agency (ARPA). This effort is a major element of an NBS program which seeks to develop, and to disseminate to the electronics community, carefully evaluated and well documented test procedures and associated technology to solve measurement and standardization problems in connection with the manufacture, procurement, and application of semiconductor devices.

2. Highlights

It is clear from the workshop that device manufacturers consider test patterns to be vital measurement tools for obtaining information about the results and control of their processing steps. This information is used by them for establishing process lines quickly and for improving and maintaining yield and product reliability. It is also clear that customers concerned with purchasing reliable semiconductor devices with reproducible performance are becoming increasingly aware of the utility of test patterns in qualifying wafers used in the devices they buy.

The workshop showed that the semiconductor industry routinely uses test patterns for a variety of purposes to an extent not indicated before in public. Speakers discussed their philosophy about the use of test patterns and how they have found test patterns to be useful for process control, monitoring, and design; for circuit element testing; for product assurance; for line-to-line comparisons; for device vendor as well as materials supplier comparisons; and for increasing the rate of yield improvement of new products.

Data management is a key element in the use of test patterns. The large volume of data generated from the use of test patterns and the requirement for rapid diagnostic feedback presents a severe data management challenge which make automatic data acquisition and display systems indispensible. It was pointed out that even the more sophisticated automatic data acquisition systems can be deficient in presenting the huge volume of data in a way that allows it to be digested quickly by the user. Data acquisition systems were described, as were attempts to present data in easily interpreted graphic displays, such as three-dimensional displays of parameter values over the wafer.

Among the guidelines given by the speakers for designing and using test patterns were the following:

> With regard to design, structures should be constructed so as to minimize their sensitivity to processes other than the one they are intended to check. If a given test structure is very sensitive to alignment, it should be incorporated on the circuit chip. Test patterns that are to register with the circuit pattern should have a contact pad arrangement that corresponds to that of the circuit. And the test pattern should consist of a sufficiently flexible set of test structures to allow its use on a variety

of product lines. Some suggested that these test structures be arranged in conveniently probeable modular test cells.

With regard to use, as many test structures and measurements as is feasible should be incorporated at the earliest stage of product development. Reductions in the number of test patterns and measurements can be made as improved process control is achieved. Reductions in the number of test patterns can be made conveniently when mask changes are made during the development of the product. However, the less static the technology, the more the use of test patterns is required.

With regard to the data taken from test patterns, it is a mistake to condense data to long listings and to rely on average values of parameters. To have standard deviation values is a minimum requirement; it is better to have density distributions of parameter values. For the latter, it is necessary to identify the location on the wafer of the test pattern originating the data.

In a production line environment, test pattern usage is best accomplished by means of a unified system for data acquisition, analysis, and storage.

A significant educational problem remains for both test pattern proponents as well as potential users. However essential test patterns may be, test patterns will not be used unless they are easy to use, readily available, well-understood, and well-documented, so they can be used with confidence by everyone involved.

The need to improve the design of test structures to make them more effective measurement tools of broader applicability was generally recognized by the workshop participants. In particular, problems with measuring contact resistance and the properties of oxides, surfaces, and defects were identified. The difficulty of separating different interacting process variables was also mentioned. Among the test patterns discussed were structures to monitor alignment, diffusion depth, line widths and lengths, contact resistance, and sheet resistance. Also discussed were charge-coupled device test structures to measure material characteristics, process control parameters, and surface-dependent device performance not easily measured by other ways. In particular, a capability to measure a density of fast interface states as low as 10^{10} cm^{-2}, and to measure the lifetime and storage time of MOS devices was described.

Efforts and plans by NBS to assist the industry and government in the more effective application of test patterns were reviewed. The approach is to identify, analyze, and intercompare selected test structures of value to the industry and its customers, and to develop measurement methods for use with these structures. In particular, test patterns were described for measuring factors needed in process control and procurement, and for the redetermination of the resistivity-dopant density

relation (the Irvin curve). Data acquisition systems in use and under development were also described.

3. Overview and MOS Test Patterns

3.1 *Test Pattern Philosophy*

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Test patterns have been routinely used in the laboratory environment for technology design and development, and for doing trouble shooting or diagnostics work. But, one of the major problems for the industry is the routine use of test patterns in a manufacturing environment where thousands of wafers are being processed on a production line.

The primary use of test patterns in a manufacturing environment is to increase the rate of yield improvement in the early stages of manufacturing. The manufacturing costs during these stages, particularly for large scale integration (LSI), are dominated by the chip costs. Hence, the interest is in addressing chip processing costs and their reduction.

Diagnostic feedback is a key factor in improving and maintaining processing yield, assuming that the cycle time is reasonably short. The data base for such feedback is obtained from circuit testing, process control test patterns, in-process testing, and input materials testing. The data needed for circuit testing may be vastly different from that required for device characterization or device screening. The kind of circuit test data needed is the kind which may be used to indicate what changes in processing are required. Such interpretation is generally difficult, especially for complex circuits. Process control test patterns can assist in this interpretation and essentially serve as a bridge between the circuit and processing areas when test pattern data are correlated with in-process data. Many problems that develop on the processing line originate from input materials, so data about these materials are also needed.

The management of this data base is a key element in the diagnostic feedback process, and the problems associated with such management are one of the primary reasons why test patterns have not been more effectively used in manufacturing. The data obtained from test patterns have generally been presented in the form of averages. But, from the diagnostic point of view, averages do not provide enough detailed information; it is important to know the location on the wafer of the test pattern from which the data were obtained.

Process control test patterns presently are designed to monitor individual process parameters, process interactions, and defect density distributions. Test patterns to monitor individual process parameters are widely used to correlate with

in-process measurements and to generate control charts. These test patterns are probably the easiest to use. Because process control test patterns can be effectively used for parametric diagnostics and process characterization, they can be used effectively for improving processes; for comparing different process lines, such as comparing a new line with an established line; and for comparing different vendors. However, these structures must be designed to minimize the interactive effect of other parameters. For example, the test pattern to measure sheet resistance should not be sensitive to etching processes. Their use in control charts provides a means of alerting the process line to parameter trends that if allowed to continue would result in reduced yield. One potential danger in the use of these patterns is the risk of generating too much data and apparent parameter correlations, if insufficient care is exercised in managing the data base.

Test patterns designed to monitor process interactions (interactive parameter test patterns) are generally transistors or other devices. By inference, such a test structure can be used to characterize a process or process parameter instead of using several test structures to obtain the required information more directly. Generally the structure is also a device about which one wants to keep a history. More work needs to be done in designing such structures and in developing data reduction programs so that the process variables can be separated more effectively.

Test patterns designed to look at a defect density distribution (statistically oriented test patterns) are important in producing LSI structures because defect density plays an important role in any discussion of yield for such devices. A limitation of such test patterns is that the "capture cross section" for random defects is much less than the LSI devices themselves unless many such structures are put on the wafer. To date, this limitation has frustrated attempts to obtain useful data that can be correlated with yield. If wafers with only test patterns on them are used, information about the defect density distribution may be obtained. With such defect maps, changes in the process may be made to minimize the effect of such defects on the circuits to be made. Also, such defect maps may be useful in process improvement studies. In particular, they may be able to reveal the location of problem areas on the wafer.

Another use to which such structures can be put is to correlate measurements on test structures designed to detect a defect with wafer yield and determine, for example, if statistical differences in wafer yield can be related to a particular defect. Such experiments consume considerable time and require wafer identification. It is very important to develop some kind of method that will allow, at least in some limited fashion, the identification of wafers in other uses of test patterns as well. Not to be able to do this leads to the use of "averages" which makes for less efficient use of test patterns for process improvement.

Test patterns can also be used to decide if a wafer should be scrapped, but it is generally worthwhile to do this only when fabricating devices with multilayer

metallization. In order to make good measurements, metallized contacts to the test patterns are needed. Thus, test patterns are not generally tested until after the first metallization step. For circuits with a multilayer metallization it is worthwhile to examine the test patterns carefully after the first metallization step and decide whether to scrap the wafer because of the expense of continuing until the circuits themselves are probed. For circuits with single-layer metallization, however, the cost of continuing fabrication to the circuit probe step is usually not great enough to warrant scrapping the wafer on the basis of the test pattern data.

There are other considerations in test pattern engineering. Two are the placement and the quantity of test patterns on a wafer. The most common procedure is to distribute a few test structures in each quadrant of the wafer. Other placement patterns are spirals and rows or columns, using enough structures to get topological information. And even though there is severe pressure to process as many circuits as possible on a new product line when the yield is low, it is at this stage when the largest number of test patterns are needed. As the process line matures and the yield increases, the number of test patterns can be reduced. These reductions can be made conveniently when mask changes are made as the product matures.

Another consideration in test pattern engineering is modularization where a set of test patterns is used for many different products. Not all the test patterns would be used for each particular product, but enough would be used in common to allow the same process on different product lines to be monitored with the same test structures. The data accumulated can be very useful in comparing and evaluating different product lines.

Finally, to obtain information about the performance of a particular circuit, the best approach is to use a special metallization pattern over the circuit to gain access to specific devices in that circuit. This approach can also be used to obtain information about the distribution of values of a parameter over the wafer. However, for generating data to control the process line and make process improvements, it is important that the same test structures are used for all products of a family-type so that a data base can be rapidly accumulated against which each line and process can be referenced.

3.2 *MOS Test Structures for Production Use*

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The commitment by American Micro-Systems, Inc. (AMI) to silicon gate technology rather than to standard metal gate technology presents the possibility for many more process problems because of the longer and more complex processes required in the former technology. Also, because the silicon gate processes are continually undergoing improvements, means are needed for effectively evaluating whether a process

change is beneficial or not. Furthermore, because of the large-volume production environment, individualized time-consuming techniques such as grooving and staining or angle lapping wafers cannot be used effectively. Problems must be detected by electrical means using statistical sampling methods. Finally, there is the need to be able to correlate circuit yield with process parameters to improve circuit yield. Test patterns and an automated data management system have been developed to answer these needs, in short, to provide an automated and objective means of diagnosing and controlling the fabrication process for producing complex MOS LSI circuits.

Criteria for implementing test patterns in a production environment are as follows. Test patterns must be designed to provide specific information about a process problem. For example, it is not enough that test patterns indicate that a metallization step coverage problem exists; they must reveal what kind of steps are creating the problem. Test patterns must be included in every production wafer. High volume production requires that test patterns be compatible with a data acquisition system. Finally, the results of test pattern measurements must be presented in a meaningful manner so that engineers in the process, product, and circuit areas can digest and use the results.

Seven basic types of test patterns used in the development and production of silicon gate MOS devices are listed in table 1. The last test pattern listed is specially designed for use in a high-volume production environment. It uses a structure, shown in figure 1, which is located at 8 sites on the wafer as shown in figure 2.

Table 1. BASIC TYPES OF TEST PATTERNS

1. Process Reliability and Characterization Test Patterns
   - to aid in new process development
   - for process reliability testing (e.g. reliability of gate oxide, junction integrity, metal step coverage)
   - for characterizing basic parameters (e.g. sheet resistance, mobility, oxide thickness)
2. Process Design Rule Evaluation Test Patterns
   - to determine dimensional limitations of a process (regarding proximity of diffusion regions, metal lines, etc.)
3. Circuit Oriented Test Patterns
   - primarily to verify innovative circuit techniques
4. Wafer Map Test Pattern
   - six-paded structure incorporated into every MOS circuit
   - to obtain values of intrinsic parameters such as sheet resistivities over the wafer
5. In-Line Process Control Monitor Test Pattern
   - to monitor particular processes (e.g. ion implantation)
6. Pilot Line Wafer Configuration Test Pattern
   - a basic test structure (shown in figure 1) which is stepped into 5 columns on a wafer (as shown in figure 3)
   - for pre-production evaluation work
7. High Volume Production Wafer Configuration Test Patterns
   - the same basic test structure as in no. 6 which is stepped into only 8 locations on the wafer (as shown in figure 2)
   - for evaluation work on production line

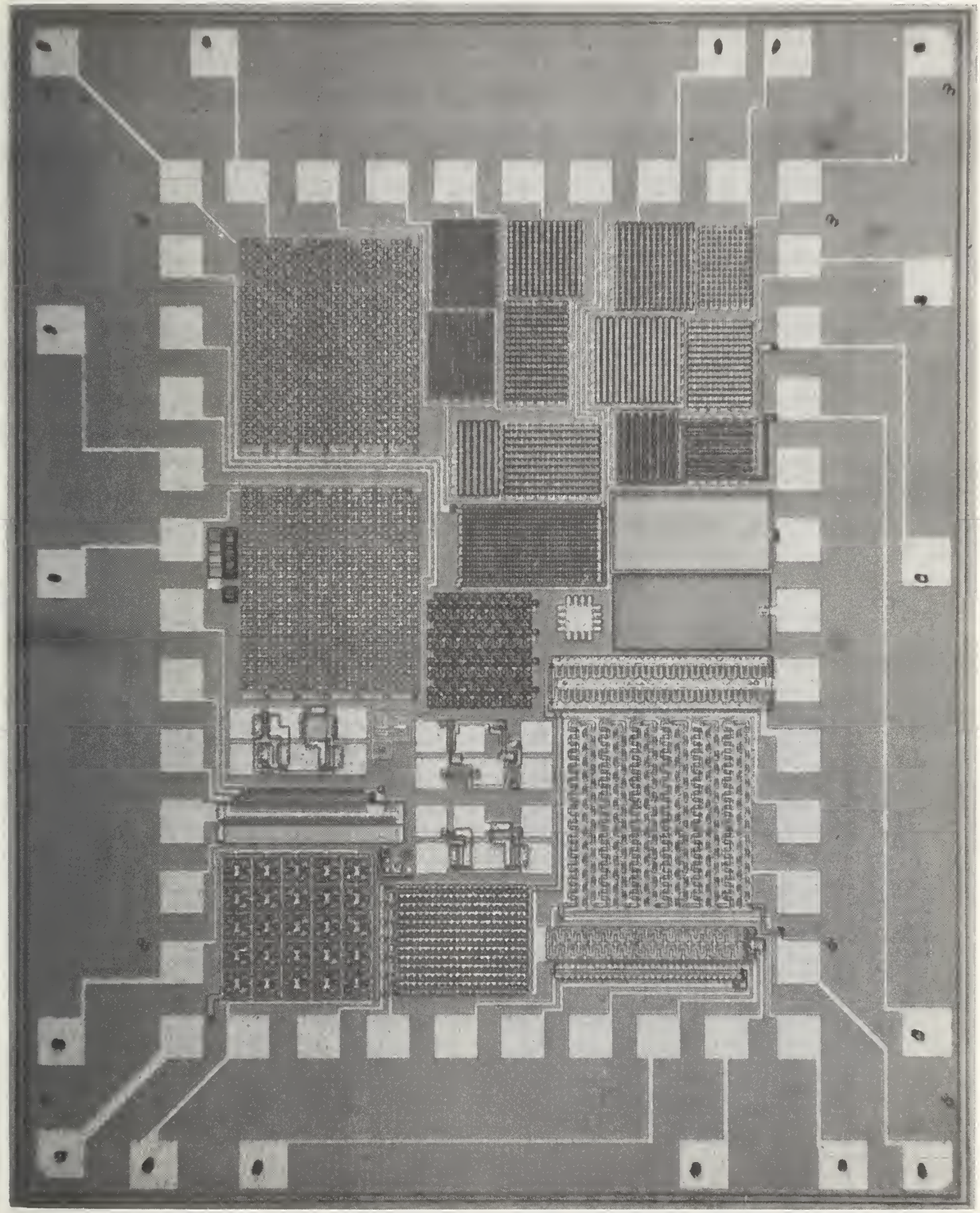

Figure 1. Test pattern test structure used in both pilot lines and high-volume production lines.

The cell in the center of the wafer is blank and is used for alignment purposes. This same test structure is used on pilot lines where many more are used; in particular, 5 columns of such structures may be included on a wafer in the way shown in figure 3.

The test structure in figure 1 has two sets of contact pads. The pads in the outer set are located in the same locations as those pads for the circuit being produced. In this way an automatic probing procedure can be used to detect that the cell being probed is a test pattern and then institute a special testing sequence which by probing the 42 pads on the inner set can make a total of 75 dc tests on the internal test structures accessed. The effectiveness of such a test pattern depends on the assumption that at the production stage no major process changes are made and that the product is of such maturity that the basic processes, such as for obtaining specific sheet resistance and threshold voltage, are under control and concern has shifted to such problems as reducing the defect density on the wafer.

To use test patterns effectively on a production line, it is critical that the test patterns be incorporated into a unified system for data acquisition, analysis, and storage. For example, it would be impossible to cope with the volume of test pattern data obtained on a production line involving the introduction of about 1000 wafers per day without an appropriate data management system.

The data handling system used at AMI is shown as an operational flow chart in figure 4. Wafers leaving the fabrication area can be tested in one of three ways. One is with a semiautomatic tester which requires manually operated movement to test different cells on a wafer. At each cell the tester can automatically sequence through

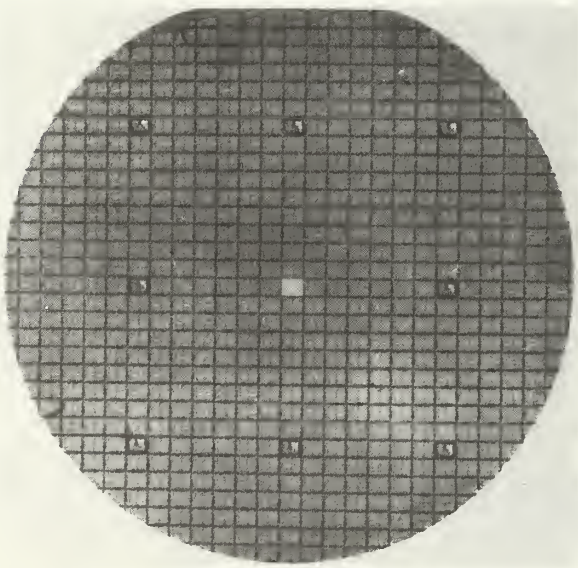

Figure 2. Eight, non-central locations where the test pattern structure, shown in figure 1, is positioned on a wafer processed in a high-volume production line. The center cell, which is blank, is used for alignment.

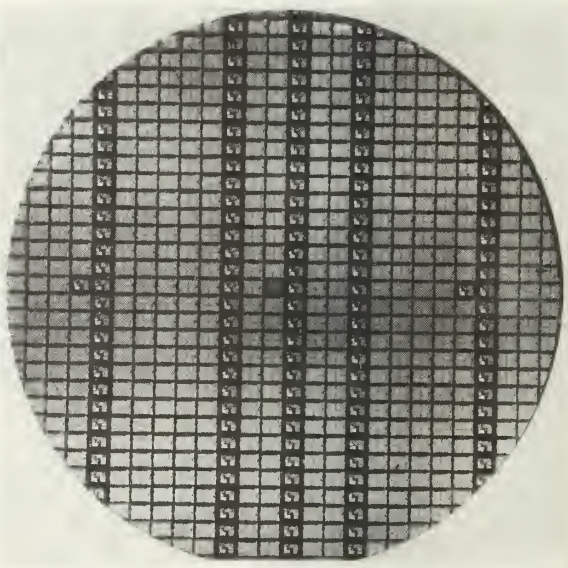

Figure 3. Five columns of test pattern structures, shown in figure 1, positioned on a wafer processed on a pilot line.

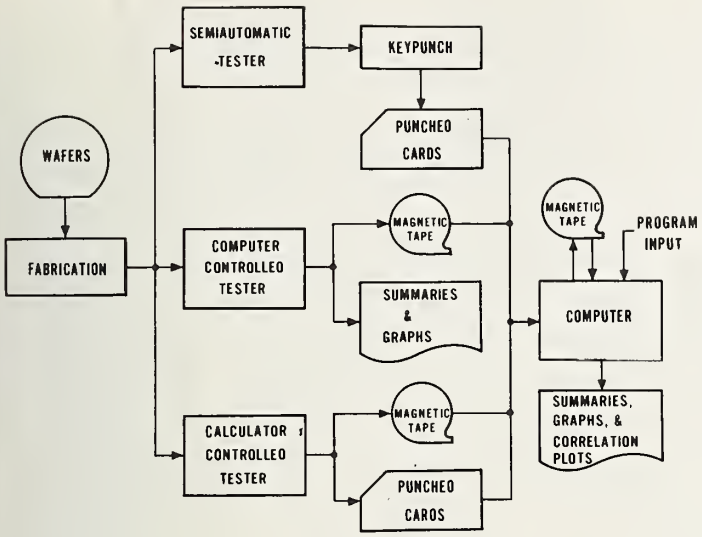

Figure 4. Operational flow of the AMI data collection, analysis, and storage system.

as many as 25 dc tests and digitally display the results. The results can also be transcribed onto coding sheets and punched onto computer cards. Another way of testing wafers is by way of a programable calculator-controlled tester (HP 9820)* which can automatically sequence through as many tests as are required and display the results, record the results on a thermal printer, or store the data on magnetic tapes. The third and most powerful way of testing the wafers uses a computerized tester (Fairchild Sentry 600)* which is capable of performing numerous ac tests and as many dc tests as are required, all in a time of the order of seconds. The output can be stored on magnetic tape or displayed in a wide variety of ways. The final link in the data management system is a special computer program (ALGOL) written for an in-house computer (Burroughs 6700)* which is capable of accepting data obtained from any one of three sources mentioned. The data can be manipulated, analyzed, and stored by the computer, as desired.

A variety of outputs and displays can be used. Test patterns and the program are so designed that failures can be categorized not only according to location on the wafer but also according to the part of the process involved. One of the most powerful features of the program is the capability to create a correlation plot between any two measured parameters which are described by a lot number, date code, yield number, or other type of identifying label.

To indicate how test patterns can be used as diagnostic tools, an example of a low breakdown voltage problem in a silicon-gate MOS transistor lot will be discussed. A number of potential causes for a low breakdown can be tested for with the use of

*Commercial equipment is identified to adequately specify the system used. In no case does identification imply recommendation or endorsement by the National Bureau of Standards nor does it imply that the equipment identified is necessarily the best available for the purpose.

appropriate test patterns to determine which part of the process is at fault. Possible causes for low breakdown are a low junction voltage, a short-circuit in the glass protective coating or between the gate and drain, and a narrow channel length.

There are a number of reasons for a narrow channel length. It can be caused by having a poly-silicon gate that is too narrow because the gate acts as a mask to separate the drain and source during the diffusion process and so determines the channel length. Over etching the gate oxide beneath the poly-silicon gate enlarges the area available for diffusion and so also reduces the channel length, as does too deep a diffusion of the drain and source because of the lateral spread under the gate. Finally, misalignment of the gate with respect to the source and drain regions can also result in a channel length that is too narrow.

A test structure that can be used to detect poly-silicon gate structures that are too narrow consists of two adjacent poly-silicon resistors, one 20 mils (0.51 mm) long and 2 mils (0.05 mm) wide and the other 15 mils (0.38 mm) long and 0.25 mil (0.006 mm) wide. The resistance of both resistors is measured and the ratio of resistivities of the two resistors is calculated using the design valves for the widths and lengths of the resistors. Changes in the process which would affect the poly-silicon gate width will significantly affect the actual width of only the 0.25 mil (0.006 mm) wide test resistor. This in turn will result in the calculated ratio of resistivities being significantly different from unity. The operation of this test pattern is predicated on the assumption that the thickness and doping of the poly-silicon will be the same for the two test resistors.

A test pattern to determine if the source and drain diffusions are too deep consists of two adjacent p^+ islands that are designed to be so close that the depth of the diffusion can be conveniently evaluated by a measured punch-through voltage for the structure. A low punch-through voltage will indicate an undesirably deep diffusion.

To detect a misalignment of the poly-silicon gate with respect to the source and drain diffusion regions, a structure is used which consists of four minimum-gate-width

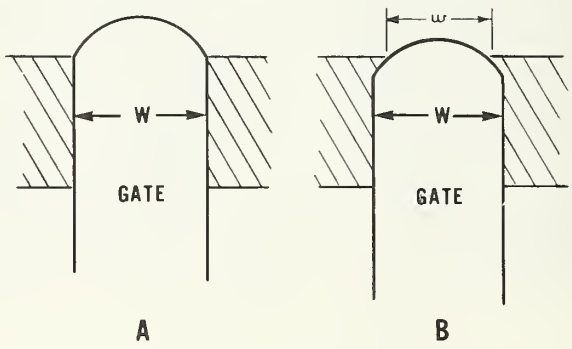

Figure 5. Topview of a structure to test alignment of the poly-silicon gate, of width W, with respect to the source-and-drain diffusion region (shaded). Satisfactory alignment is shown in A. Misalignment is illustrated in B where the minimum channel length is w, which is significantly less than the designed width, W, of the gate.

elements arranged sequentially at right angles to each other. A sketch of one element with proper alignment is shown in figure 5A. The width of the gate is designed to be about 0.25 mil (0.006 mm) to accentuate the rounding effect at the end of the gate. The channel length is determined by width W. A misalignment is illustrated in figure 5B. Here the minimum channel length is determined by w and is detected by a low punch-through voltage.

This is only one example of the use of test structures by a semiconductor device manufacturer. In summary, AMI has found test patterns to be invaluable tools for process monitoring, process control, and diagnostics. By implementing test patterns on all major process lines, test patterns can also be used to compare objectively different processes and fabrication lines.

3.3 *MOS Test Structures for Laboratory Use*

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An important aspect of the thrust in microelectronics at the Naval Electronics Laboratory Center (NELC) is the improvement of the reliability of military electronic systems through improved process control. Earlier diagnostic examinations of LSI devices showed that the reliability of such systems based on complex LSI devices is affected and in fact often limited by contamination or localized defects in or near the oxide-silicon interface in MOS structures.

In order for the Navy and the other Services to be able to procure LSI devices of sufficient reliability at acceptable cost in low-volume purchases, it must be able to find a way to detect, reduce, and control these contaminations and localized defects in a routine way.

An approach taken by the NELC Microelectronics Division has been to exploit the sensitivity of the charge coupled device (CCD) to fixed oxide charge and fast interface states in an appropriately designed test structure to measure material characteristics, process control parameters, and surface-dependent device performance not easily measured with other test structures.[1]

To evaluate the use of the CCD as a process control tool requires an intercomparison of the results of CCD's and those from conventional test structures. Two test patterns have been developed for this purpose. One contains four CCD structures, two linear and two circular, which are shown in figure 6. The other test pattern, shown in figure 7 contains a number of conventional structures such as MOS transistors and capacitors, gated diodes, and contact and van der Pauw resistors.

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[1]This work is being supported by the Semiconductor Technology Program at NBS under ARPA Order No. 2397, Program Code 5D10. More details of work on this project may be obtained from quarterly progress reports of the Program which are published in the NBS Special Publication 400 series.

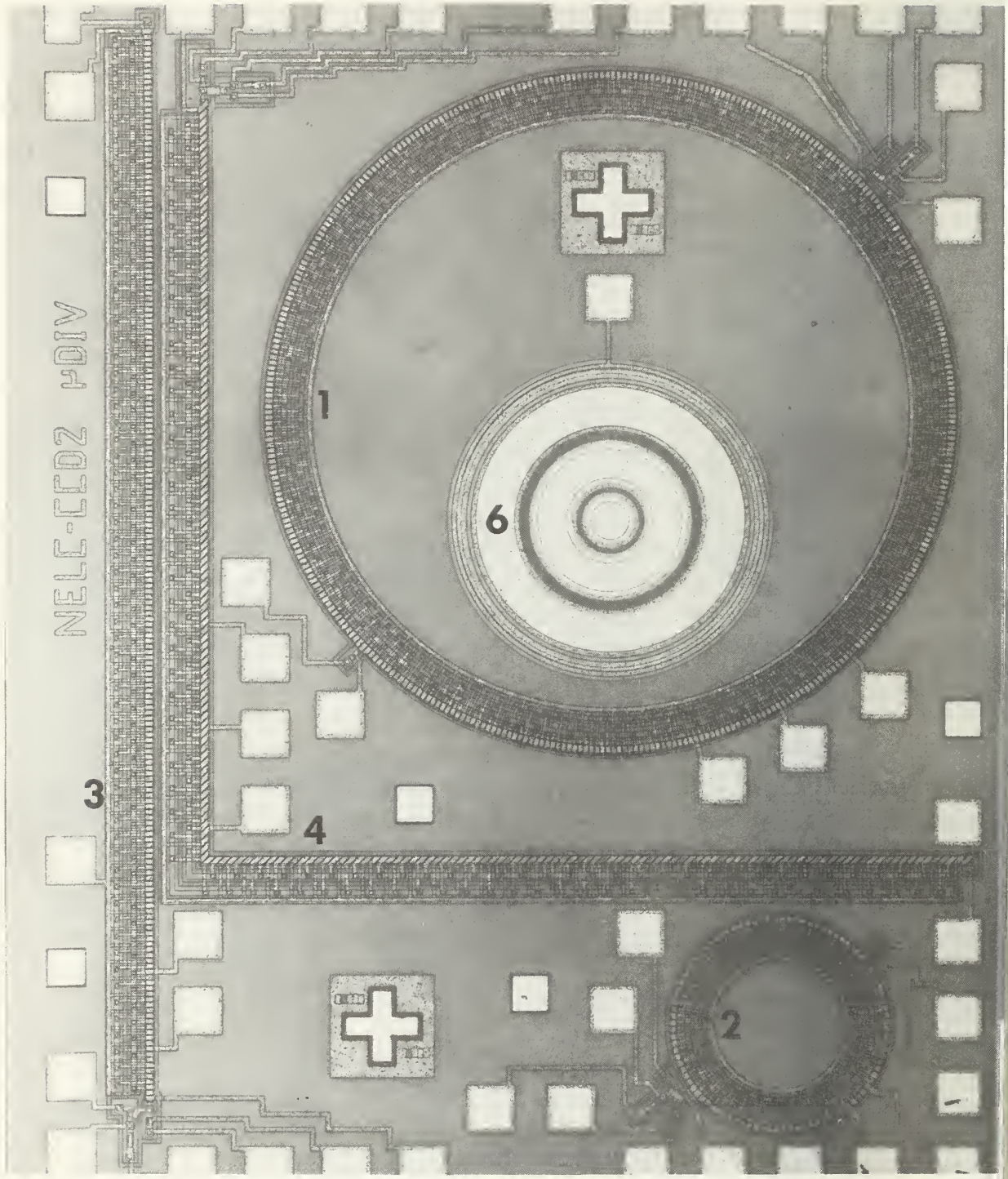

Figure 6. Photomicrograph of CCD test structures where the overall horizontal dimension is about 103 mil (2.6 mm).

Structure	Description
1	128-bit circular CCD
2	32-bit circular CCD
3	64-bit linear CCD
4	64-bit parallelogram CCD
6	Gated n^+p junction (diameter = 20 mil, 0.51 mm)

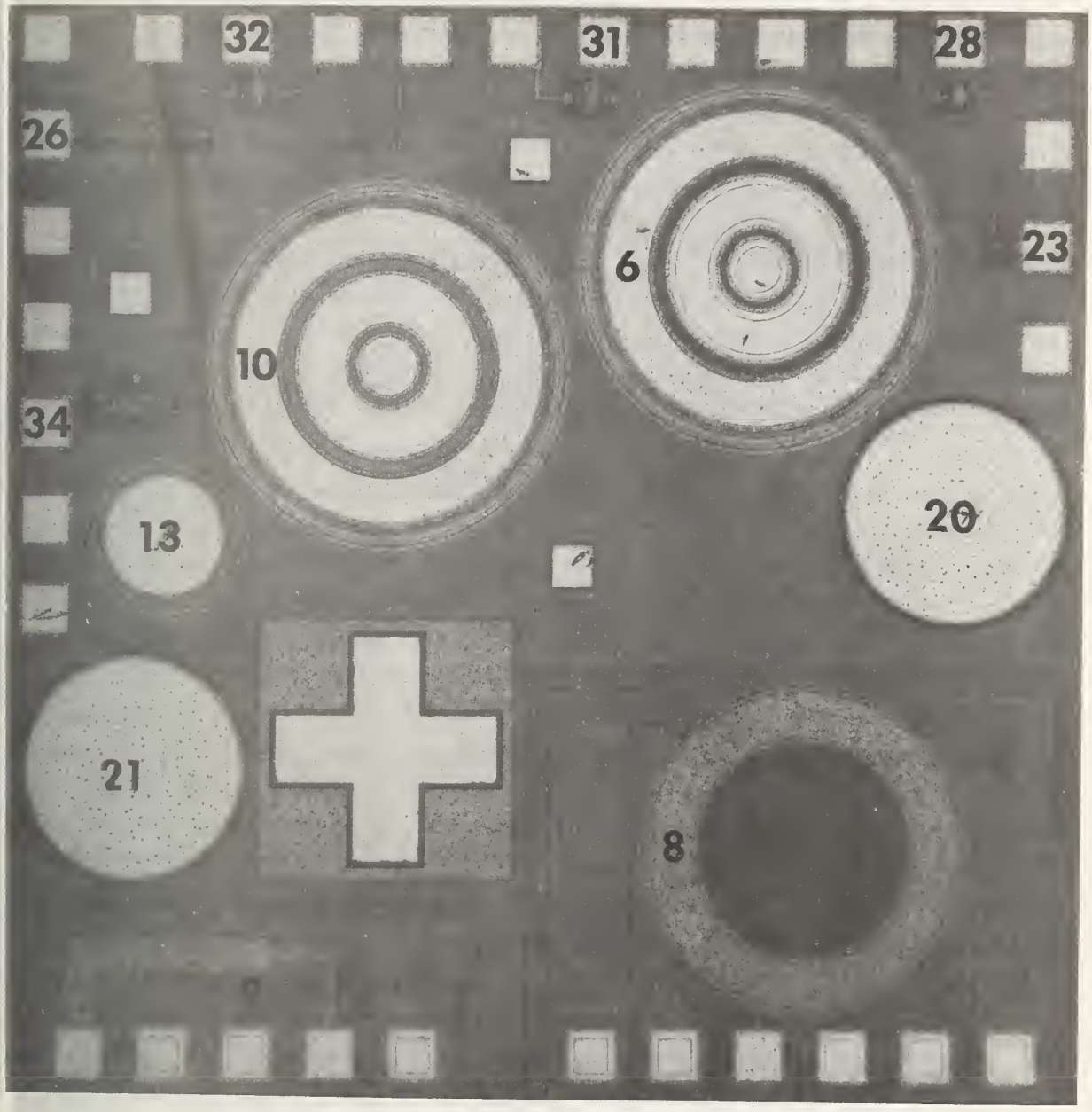

Figure 7. Photomicrograph of conventional test structures where the overall horizontal dimension is about 103 mil (2.6 mm).

Structure	Description
8	Gated van der Pauw resistor in n^+-layer
9	Metal to n^+-layer contact resistor
10	Substrate (p-type) resistor
13	p-MOS capacitor with field plate (diameter = 11.4 mil, 0.29 mm)
20	p-MOS capacitor (gate oxide) (diameter = 20 mil, 0.51 mm)
21	p-MOS capacitor (field oxide) (diameter = 20 mil, 0.51 mm)
23	n-channel MOSFET (W/L = 2, L = 0.4 mil, 0.010 mm)
26	n-channel MOSFET (W/L = 12.5, L = 0.4 mil, 0.010 mm)
28	n-channel MOSFET (W/L = 1, L = 1.0 mil, 0.025 mm)
31	n-channel field oxide MOSFET (Isolation check)
32	n-channel field oxide MOSFET (W/L = 1, L = 1.2 mil, 0.030 mm)
34	n-channel MOSFET (W/L = 25, L = 0.4 mil, 0.010 mm)

Plans for correlating the results from the two test patterns are as follows. The interface state density determined from the CCD's [2] can be compared to values obtained from the MOS transistors [3], the MOS capacitors [4], and the gated diodes [5]. The fixed oxide charge from the CCD's [6] can be compared to values obtained from the MOS transistors [7] and MOS capacitors [8]. Finally, the CCD's can be operated as long channel MOS transistors, gated diodes, and MOS capacitors. The results of measurements on the CCD's operated in this way can be compared with those on conventional test structures of the same family.

Initial work with the CCD's, in preparation for intercomparison with the other test structures, has demonstrated that a CCD can function not only as charge transfer device but also as an MOS field effect transistor, a gated diode, and an MOS capacitor. This is accomplished by application of appropriate sets of externally adjusted voltage levels to the CCD.

The primary CCD test structure (number 2 in figure 6) consists of aluminum electrodes deposited on a high purity thermal oxide over 1.5 to 3 Ω·cm, *p*-type (100) silicon to form a closed-loop, 32-bit electrode array, 18 mils (460 μm) in diameter. The circular configuration has the advantage over a linear array of being more compact and of being able to allow multiple charge transfers around the loop. The sequential application of properly phased voltage pulses to repeated sets of three electrodes have been used to make as many as 5000 charge transfers.

Circular CCD's in the charge transfer mode can be used to measure the fast interface state density per unit energy, N_{FS}. Interface states represent a source for fixed loss in this operating mode. As charge carrier packets are transferred, a certain number will be captured by these states and re-emitted after some time. If they are emitted at the next or following clock phases they will follow the first pulse and be revealed as a trailing edge which will give an indication of the transfer loss and hence the interface state density.

A double pulse method [2] has been used to obtain a quantitative measure of N_{FS} in a 32-bit circular CCD. The method involves the injection of a pair of charge-carrier packets followed, after N_{zero} empty packets, by a second pair of charge-carrier packets. As the packets are circulated, the pulse height P of the lead packet in the second charge carrier pair is attenuated from its original height P_o after N_{tran} charge transfers. The fractional charge loss per transfer, α [given by $\alpha = (P_o - P)/(P_o \cdot N_{tran})$], is related to N_{FS} by

$$\ell n\, N_{zero} = (N_{sig}/N_{FS}kT)\alpha + \ell n\, F$$

where k is Boltzmann's constant, T the temperature, N_{sig} the unattenuated signal charge density, and F the fraction of time available from each period during which the charge

can be transferred. N_{FS} is determined from the slope of the straight line in a plot of $\ell n\ N_{zero}$ versus α; F is determined from the N_{zero} intercept. The value $N_{FS} = 1.2 \times 10^{10}\ (cm^2 \cdot eV)^{-1}$ at room temperature was obtained using $N_{sig} = 5 \times 10^{11}\ cm^{-2}$, a value derived from the electrical characteristics of the output inverter stage of the CCD.

3.4 *Discussion Period*

Murakami was asked if there are any products where the number of mask levels would preclude the use of test patterns. He answered no and went on to point out that their use of test patterns is not oriented to a given product line or technology. It is directed to examining individual process steps and to revealing problems that may be present. Any one of these process steps may be associated with many different products.

In response to other questions, he said that test pattern data are not supplied to their customers because they consider this data to be proprietary information which can be used for yield analysis. They keep their test pattern data for as long as six months by which time the data have generally become obsolete because of the many process changes that have occurred in that period.

Callahan was asked if test patterns have been used to compare and evaluate those incoming materials for which there are no satisfactory measurement methods available to characterize them. The detection of impurities in processing gases and photoresists was cited as an example. He replied that test patterns have been used to evaluate and compare silicon purchased from vendors and from in-house suppliers. He added that it is very important to be able to separate effects due to incoming materials from those due to processing. However, he knows of no one who has used test patterns to evaluate incoming material other than silicon.

Most of the other questions and discussion dealt with the topic of reliability and the possible use of test patterns to predict product reliability.

Callahan responded to the first series of questions on the use of test patterns for reliability assurance. He said that Motorola has used test patterns generated in-house to estimate the reliability or expected life of products in the development stage. They look for specific reliability problems. He referred to one occasion where the use of test patterns revealed a reliability problem that would not have otherwise been detected until well into the production stages of the product. They have worked with the customer in such efforts and while they have never used a test pattern suggested or supplied by a customer, he sees no obstacles to using appropriate customer generated test patterns.

Callahan indicated that he is not aware of test patterns being used for reliability assurance on the production line. He mentioned that it is difficult to utilize test patterns efficiently to detect problems that affect only a small percentage of circuits

on a wafer, a percentage that would nevertheless be very serious if translated to failures in the field.

A participant added that he is aware that it is relatively common practice for some commercial customers to require temperature bias tests on oxides and a quality assurance certification.

Another participant asked if anyone could indicate the percentage of field failures due to problems that can be detected by the use of test patterns. Callahan volunteered that he could not give a percentage. The percentage can depend very much on the way and the environment in which the device was assembled. While some problems such as drift in the threshold voltage can be caught with test patterns, his experience is that most field failures are due to assembly, after the wafer has been processed.

There seemed to be general agreement that many field failures are due to mechanical failures of some kind that cannot be addressed by test patterns.

One participant philosophised that if one examines the test records of devices with non-mechanical failures, they show that many devices only marginally passed some of the electrical tests. Also, failures are caused by defects that become large enough to cause failure only after some period of operational life of the device. The example cited is the circuit that has a shallow pin hole which during the course of operational life enlarges to cause a short circuit. Therefore, when attempting to predict reliability and life, it is not the test pattern data that is necessarily of significance but rather it is the overall yield from a wafer or a lot that is of significance. If one wants to predict reliability in the field, he reiterated, the measure to look at is the yield.

Murakami indicated later that the yield of a wafer or lot is not necessarily the answer to predicting reliability. He cited experience with shift registers where two of the reliability problems are poor or open-circuit contacts and metallization continuity over oxide steps. They have not found good correlation between the yield of their test patterns designed to test for these problems and overall product yield. He feels that the data from his test patterns, at least in this case, are more sensitive indicators for product reliability.

A participant argued that many mechanisms that lead to reliability problems are not well understood. These mechanisms relate to material and process-induced defects. He added that if test patterns are to be used in this area they need to be far more sophisticated then they are now. Furthermore, the approach of using test patterns has to be entirely different. Analysis cannot be based solely on electrical measurements but will need to involve structural measurements and diagnostic procedures as well.

Another participant cited the responsibility of the user in the reliability area. The user must communicate to the device vendor what his worst-cast conditions will be. He added that test patterns can do a good job in the reliability as well as in the

process control area if the device manufacturer can anticipate how the devices will be used.

4. Bipolar Test Patterns

4.1 *Bipolar Test Structures for Production Use*

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Large-volume production of standard commercial bipolar integrated circuit devices, as distinct from custom military and commercial products, dictates that the fabrication of test patterns involve a minimum number of changes in the fabrication process because additional processing tends to adversely affect production yield and cost. This constraint has led to the following guidelines in the use of test patterns. Only a metal mask change is made with no additional processing steps and at most five test sites per wafer are used. Hence, the test pattern employed consists of the circuit itself with a modified metallization pattern which allows electrical access to selected circuit elements (test elements).

These test patterns are used primarily in the following three ways:

1. To determine if the important parameters of the active and passive elements of the circuit are within their respective specified ranges. This allows an estimate to be made of the yield of the wafer and provides a basis for deciding if all the circuits on the wafer should be checked electrically.

2. To determine possible causes for abnormally low yield from a wafer of a production run.

3. To provide an after-the-fact measure of the control over the wafer fabrication processes.

The use of test patterns as in-process control tools in this environment is limited. Control over processes up to and including metallization is accomplished by the use of pilot wafers and by testing individual devices on a wafer.

Test patterns are usually placed in five locations, one at the center and the remaining four in separate quadrants at a distance from the center of from 1/2 to 3/4 the wafer radius. For large scale integrated circuits, usually only two or three locations are used.

Experience has indicated that a maximum of five test sites on a wafer provides sufficient information to make adequately accurate estimates of the potential yield from the wafer. To increase significantly the accuracy of such estimates would require many more test sites which would contribute to a significant decrease in yield and therefore be unacceptable for a well-established, high-volume production facility.

The most commonly used test elements for linear or digital circuits are as follows: transistors, one of each geometry and type (*npn, pnp*), if possible; diodes; diffused, thin film, and pinched resistors; and capacitors. In the case of multi-level, large scale integrated devices, a via test element and a crossover test element are used in addition to the test elements listed above.

A number of parameters are measured on these test elements. For transistors, h_{FE}, $V_{(BR)CEO}$, $V_{(BR)CBO}$, V_{BE}, and V_{BE}, and $V_{CE(sat)}$ are measured. The forward voltage drops, V_{bc} and V_{be}, are measured to check contact resistance, and the saturation voltage is usually measured only on digital circuits. For diodes, BV_R and V_F are measured. The forward voltage drop, V_F, is measured to check the contact resistance or in the case of a Schottky barrier diode to see if it was properly formed. For resistors and capacitors, the resistance and capacitance are measured. The bias conditions for all the above measurements vary with the circuit.

Economics determine the frequency with which these measurements are made. Initially, these parameters are measured on every test structure and every slice. As the process matures the amount of testing decreases.

4.2 *Bipolar Test Structures for Custom Use*

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To use test patterns effectively in a system for process characterization and control, test patterns must be well understood by the engineer and be of sufficient diversity and flexibility that he can use them for evaluating any process step of a variety of device products in a way in which all pertinent variables can be separated. Test patterns must also be easy to probe. Therefore the contact pad arrangement must be modular and always the same. Test patterns must be simple, well-understood, and well-documented so that they can be used with confidence by everyone involved.

Large quantities of data must be taken from test patterns. In addition to the value of the parameter being measured, other information associated with that value must be recorded such as test conditions, time of measurement, wafer, and lot. The position of the test pattern on the wafer is particularly important to record. Position data allows different variables measured in the same test pattern cell to be examined as a function of position on the wafer and allows the search for correlations of variables to be made.

If test patterns are to be used in a production environment, even for custom products where the number of devices produced is not great, it is necessary to gather and process quickly the data from test structures on a wafer — experience has shown

that any wafer not completely characterized within two or three days after fabrication probably never will be. Therefore integral to any control system is a data management system for automatically taking, analyzing, and plotting the data from test patterns. In addition, if the vast amount of data is to be comprehended at all it must be presented in some graphical form.

Graphical presentations are of critical importance when using the mass of data generated from test patterns. To present rows and columns of numbers means that such data will never be used because the data cannot be comprehended in a reasonable time. Such information must be presented in a simple, easily comprehendable form. However, to condense the data to a listing of mean values is a mistake. Even a condensation to standard deviation and mean values can be misleading. A plot of the density distribution of variables is often the most useful way of displaying data. However, if only one measure can be obtained the standard deviation should be chosen.

Twelve contact pads for a test pattern appear to be near optimum for activities at Hewlett Packard. An earlier eight-padded test pattern proved to be too restrictive in the selection of tests that could be conducted, while a twenty-padded test pattern proved to be too complex to be workable.

As test patterns are stepped in with the circuits on a wafer, problems may occur if alignment is critical. In this case, test structures sensitive to alignment should be incorporated with each circuit.

With regard to the number of test patterns to use, experience has shown that the largest number of test patterns should be used at the earliest stages in the development of a product line. This runs counter to traditional thought about the need to maximize product yield at this stage. Test patterns should continue to be used as long as they can improve product yield. As the process is stabilized and more under control, the number of test patterns may be reduced.

Two examples of test structures used are briefly described below. One structure is used for measuring mask alignment. It includes a thin metal stripe which crosses over a diffused channel, midway between two channel taps. Alignment of the metal stripe with respect to the diffused channel and taps is determined by conducting a current along the channel and comparing the voltage difference between the metal stripe and each of the two diffused taps. Perfect alignment is indicated by equal voltage differences.

A problem was experienced with a photomask resolution pattern for producing alternate metalized and unmetalized stripes of equal width such as shown in figure 8A. A test of the exposure and etch processes is to determine how well the adjacent stripes agree in width. This proved difficult to do. A second pattern,

shown in figure 8B was incorporated which reduced the difficulty of this determination by now requiring only a judgment of the degree of displacement of the lines of adjacent left and right patterns.

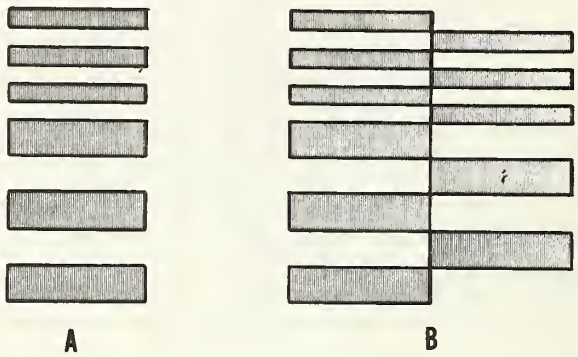

Figure 8 - Mask patterns designed for evaluating under or over exposures and etches. The most commonly used pattern is shown in A, while the recommended pattern is shown in B.

Much needs to be done in improving the design of test patterns. The measurement of contact resistance, even with a Kelvin contact design, is unsatisfactory and it is hoped that work at NBS will provide the industry with an improved test pattern to make this measurement. Much work still needs to be done in designing test patterns that are better able to separate the many variables in a process that affect the product. The characterization of oxides and surface properties as well as the detection of defects are all areas where much improvement is needed in the test patterns available to make the required measurements. Work on charge-coupled devices for characterizing oxides and surfaces is promising and work in this area will be followed with great interest.

4.3 *Discussion Period*

One could hardly have a clearer disagreement between the approach to the use of test patterns than was presented by Symeon and Brooksby, observed one participant.

Brooksby responded first to this by pointing out that there are major differences between Symeon's and his own objectives. Symeon has a few circuits which are produced in great quantities. The circuits have been carefully designed by people in his group that understand the effects of the process on their circuits. The processes are stable and fixed. This is not the case with his situation where a great many different circuits are produced with state-of-the-art processes, processes that are continually changing. Furthermore, he has to provide test pattern service to many engineers of diverse backgrounds and disciplines on many different projects.

Symeon agreed and added that they use an approach similar to Brooksby's during the development of a new circuit but this approach is dropped when the production phase begins.

Symeon was asked how the data from measurements made on his selected circuit elements (test elements) could be related to basic processes. For example, if the $V_{(BR)CEO}$ or $V_{(BR)CBO}$ of a transistor was found to be out of specification how would one determine which process was responsible. Symeon pointed out that they do not wait for these data to tell them that there is a breakdown voltage problem. It is too late by that time, considering the number of defective devices that would have been produced. An attempt is made to detect such problems and take corrective action much sooner by making appropriate tests after each process step.

Symeon was asked how he was able to cope with the time involved in taking data manually from their test elements. He implied that the time required to perform the number of measurements that they make is manageable. The number of measurements they make is much less when there are no problems than when there are, he added.

In reply to another question, Symeon said that they make no ac measurements but try hard to design their dc tests so that they may indicate expected ac performance of their circuits.

Brooksby was asked how one can decide beforehand how many test structures to include so that one can measure all parameters that may be needed and how he can see that it is done. He replied that it is a difficult task. First of all, the circuit designer must be able to identify the parameters that are important for his circuit otherwise little guidance can be given in selecting which test structures to use. In addition to the guidance that can be provided, the best that can be done is to encourage the engineer to include more test structures and to perform many more measurements than he may believe necessary. The engineer must be made to understand that to do so is worth the investment. However, this guidance must be based on persuasion rather than on authority to be effective.

Brooksby was questioned about values for the standard deviation of various processes that would be indicative of adequate control. He replied that not enough is known to answer that question in any general way. An acceptable standard deviation depends on the product and the technology. One would also need to know more about the effect of a given variable on the final product.

A misalignment of 1 μm would be disastrous, stated Brooksby in response to a question. The alignment test structure they use is capable of detecting such a misalignment, but, he added, the test structure was designed with enough sensitivity from knowledge beforehand about the maximum misalignment that could be tolerated.

Finally, Brooksby was asked if he was not concerned about contamination introduced from the processing chemicals used. He admitted that their test patterns are incomplete and that he did not know how the control of the processing chemicals could be readily checked with test patterns. Buehler added that some capacitance-voltage test structures have been used to a limited extent to check for chemical contaminants.

5. Data Acquisition

5.1 *Data Acquisition for Production Use*

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The extent to which test patterns can be successfully used to increase production yields is dependent on facilitating easy access to the test pattern data, on interpreting this data, and on educating the process engineers about the utility of such data.

All too often the tendency is to operate in a problem-solving mode where attention is directed to the process line only when yield falls. In such a mode, no data are available to compare process conditions and performance before and after the yield loss, and the temptation is to vary intuitively different processes on the line in an attempt to cure the yield problem. Such an approach ("shotgun approach") usually only aggravates the problem, first, because comparison data is not available when yields become unsatisfactory, and second because of the poorly understood interactions between different processes.

What is needed is a problem-prevention approach which makes heavy use of test patterns and a sophisticated data acquisition system. Such a system, if it is to be used in a high-volume production environment, must have the ability to cope with the huge amounts of data that are generated by test patterns. High volume here means several million circuits a month.

There are two vital considerations to a data acquisition system. First, because of the fast moving nature of the production environment, data must be taken and analyzed rapidly. This data must be available within a matter of hours, otherwise it may not be used. Second, because people ultimately will have to use and interpret the data, the acquisition system must be designed with people in mind.

There are several aspects of people involvement. One, the system must be credible—the engineer must have confidence in its trustworthiness. Two, the system must be user-oriented with respect to the data reduction and display systems so that is is easy to use—there is still much to be done in improving display systems which effi-

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ciently and clearly show the mass of data that is generated in a way that facilitates interpretation by the engineer. Third, the system must be reliable in that it must work day after day without a breakdown. And, fourth, the system must be self-maintaining in the sense that test pattern data is taken, processed, and stored routinely on every wafer processed.

The data acquisition system developed for Texas Instruments gathers data from test patterns consisting of special test structures and of the circuit itself with metallization patterns modified to allow access to selected devices. On any one set of test patterns used for a given circuit, over 60 parameters are measured out of a total of about 300 possible parameters of interest. These parameters are processed and stored for future reference by the acquisition system.

Two types of data are used: one is yield data to show yield trends, and the other is device or test structure data that can be used to indicate why the yield of a given product may not be satisfactory.

5.2 *Data Acquisition for Laboratory Use*

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Data acquisition systems and their use for MOS devices in a laboratory environment are described in the context of work to develop a silicon-on-sapphire (SOS) technology. The distinction between such systems and those designed for production use lies in the variety and flexibility of measurements rather than in the type of measurements that are required. The present systems were designed to provide fast, reliable, and accurate results with easily understood, compact outputs.

The measurement capabilities of various types of data acquisition systems are reviewed in table 2. A device in wafer form can be tested with these systems at any temperature, gas ambient, current, and voltage in the ranges indicated. Available analog outputs include time, temperature, reciprocal temperature, voltage, or current data on linear, square root, or logarithmic scales. The Hall measurement system (C in table 2) while not generally important in investigating integrated circuits, can at times be used effectively. For example, it can be used to distinguish between material scattering and trapping effects on the surface mobility. In particular, it was used in one case to determine that the bulk mobility of mobile carriers was as expected and that a high density of surface states was responsible for the observed mobility. The curve tracer, the last item in table 2, is perhaps the most important acquisition system in most laboratories. Some of the uses for the various types of systems are listed in table 3.

Table 2. Measurement Capabilities of Data Acquisition Systems

A. For Measuring Direct or Slowly Alternating Varying Currents and Voltages

- primary sensing instrument: current detector
- current range: 10^{-14} to 10^{-2} A
- voltage range: 10^{-3} to 10^{3} V
- variable gas ambient: A_2, N_2, O_2, H_2O
- variable temperature ambient: 77 to 700 K
- variable plotting: linear, square root, logarithmic, time, temperature, reciprocal temperature, current, voltage

B. For Measuring Steady State Alternating Currents and Voltages

- primary sensing instrument: lock-in amplifier
- frequency: 10 to 10^{7} Hz
- variable gas ambient: A_2, N_2, O_2, H_2O
- variable temperature ambient: 77 to 700 K
- optical excitation

C. For Measurement in DC Magnetic Fields

- primary sensing instrument: digital voltmeter
- current: 10^{-9} to 10^{-1} A
- voltage: 10^{-6} to 10^{3} V
- magnetic flux density: 10^{2} to 2×10^{4} gauss (10^{-2} to 2 tesla)
- variable gas ambient: A_2, N_2, O_2, H_2O
- variable temperature ambient: 77 to 700 K

D. Manual Wafer Mapping with Capabilities of (A) and (B)

- primary sensing instruments: microscope, digital voltmeter, current detectors, and lock-in amplifier
- semiautomatic step and repeat stage to accomodate 2 in (51 mm) wafers
- adjustable probes
- probe cards
- liquid crystal capability
- computer interface

E. Automatic Testing

- primary sensing instruments: digital voltmeter, lock-in amplifier, current detector
- complete computer control
- step and repeat capability
- operator-software interaction
- direct data transmission with preliminary data
- reduction
- automatic data manipulation and presentation

F. Transistor Curve Tracer

Electrical connection to wafers in systems A and B is accomplished by a probe system illustrated in figure 9. A sapphire wafer is placed directly on top of the nickel-plated copper block. If a silicon wafer is to be examined, a sapphire wafer is sandwiched between the silicon wafer and the block. Maintaining good electrical contact to square contact pads, 4 mils (100 μm) on a side, is difficult over the indicated temperature range from 77 to 700 K, but is can be accomplished if the probe motion is constrained to be entirely vertical. This is necessary to compensate for the vertical expansion of the copper block. Horizontal expansions are unimportant

Table 3. Typical Uses for Data Acquisition Systems

A:	Dielectric Leakage	C:	Hall Measurements
	Junction Properties		Magnetoresistance Measurements
	MOS Gate Transfer Characteristics (Sub-Threshold)	D:	Mapping of Parameters Which are Difficult to Measure Automatically
	CMOS Inverter Characteristics		Very Low Currents
	Low Current DC Beta		Curves With Complicated Shapes
	Bias-Time-Temperature Stability		Phenomena Where Significant Hysteresis Is Expected
	Drain Characteristics		Quick Wafer Scans for a Few Parameters
	Temperature Dependence of Many Types of Currents		Observation of Circuits and Test Devices During Operation
	Thermally Stimulated Currents	E:	Detailed Wafer Mapping of Automatically Measurable Parameters
B:	MOS C-V Curves		Interactive Measurements
	Junction C-V Curves	F:	Large-Signal, Single-Device Measurements
	Noise Measurements		Collector or Drain Characteristics
	Frequency Dependence of Photo Conductivity		
	Small Signal g_m		
	Bias-Time-Temperature Stability		

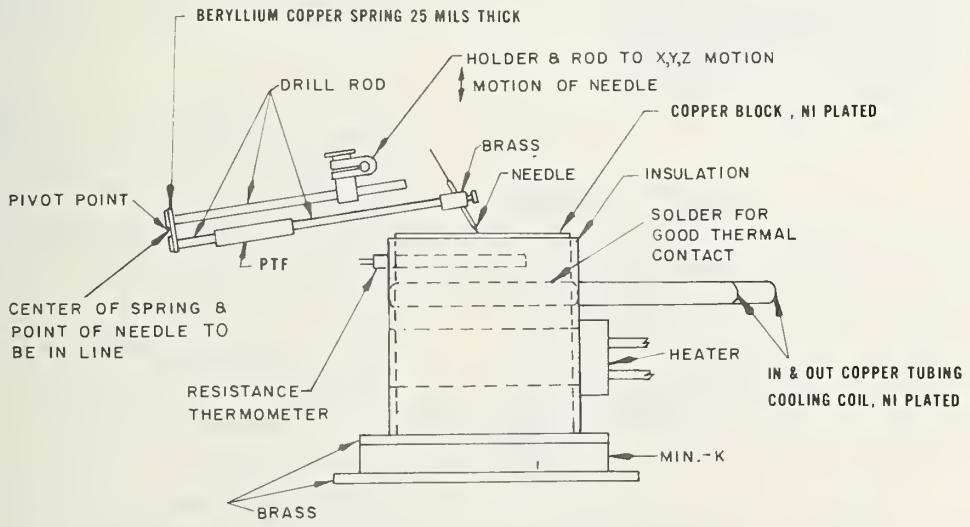


Figure 9. Probe system for making electrical contact to wafers. The wafer holder is designed to allow no more than a 2°C difference between the device and the base, where the temperature is measured. The "MIN-K" specification for the base refers to any low thermal conductivity material that is an electrical insulator. PTF refers to the material polytetrafluoroethylene.

because the wafer is centered on the copper block. The vertical motion is accomplished by placing the pivot point of the probe on the same level as the wafer. Another probe system (not shown) is available for system C for making measurements in magnetic fields and is about 0.5 in. (1.3 cm) high so that it can be placed between the poles of a magnet.

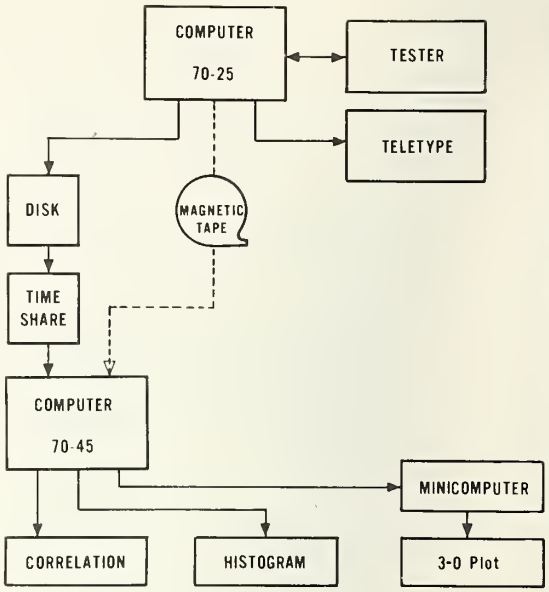


Figure 10. Data flow in computer control system. The dashed line indicates the optimum path.

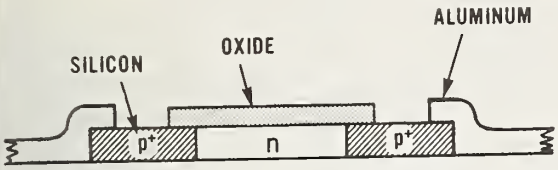
The data acquisition system (system D) has only recently become operational so its full impact has not been felt. However, it has proved to be especially useful for obtaining the kinds of data that are not easily obtained automatically. The operation flow chart for the computer controlled system (system E) is shown in figure 10. The system is controlled by its own computer (RCA 70-25).* The operator at the tester has available powerful software to interact with the computer. After the data has been reduced, it can be sent to the larger computer (RCA 70-45)* to develop correlation, histogram, or 'three-dimensional' plots. A more detailed description of this system is available elsewhere [9].

With the development of the data acquisition came the development of test patterns for SOS technology. The test patterns used to analyze the processes include MOS capacitors and transistors, metallization cross-over test structures, gate-controlled van der Pauw structures, and diffused diodes. To obtain information about parameter variations over the wafer, a square test pattern, approximately 13 mils (330 μm) square, is now used.

Examples of some of the test structures used are briefly described below.

Three test structures have been used to test electrically for mask alignment and thereby obviate the need of a visual inspection for this purpose. The test structure sketched in figure 11 is used to check with a resistance measurement the alignment of a diffusion mask to a silicon island, along one direction. The design of another test structure is shown in figure 12 where the alignment, along one direction, between

*Commercial equipment is identified to adequately specify the system used. In no case does identification imply recommendation or endorsement by the National Bureau of Standards nor does it imply that the equipment identified is necessarily the best available for the purpose.



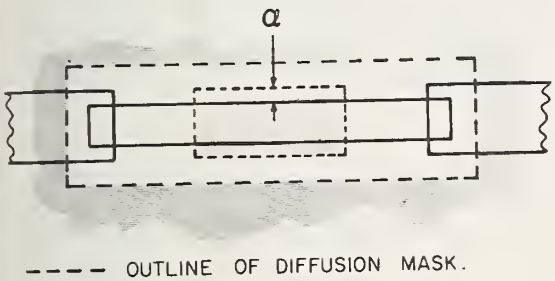


Figure 11. Side (upper) and top (lower) view of test structure for detecting a misalignment of α of the diffusion mask with respect to the lightly-doped n-type silicon island on sapphire. P-type diffusion results in essentially no change in resistance of the island as measured from the aluminum contracts unless the misalignment of the diffusion mask (outlined by dashed lines) is greater than α which results in a marked decrease in resistance.

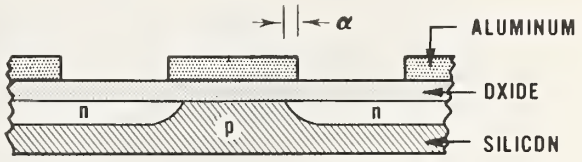


Figure 12. Cross-section of a test structure for detecting a misalignment of α of the diffusion mask with respect to the metallization mask. Misalignment is detected if the capacitances between the center aluminum contact and each of the two outer contacts over the n-type diffused silicon are significantly different.

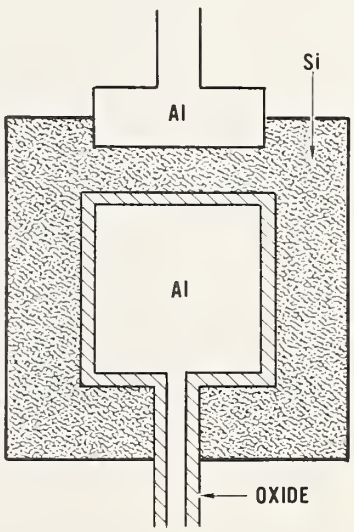


Figure 13. Top view of test structure for testing alignment of metallization to contact openings. Misalignment is detected by a current between upper and lower aluminum (Al) metallizations when the square metallization pad is misaligned with respect to the underlying oxide pad so that it makes electrical contact with the diffused silicon (Si) area.

metallization and diffusion masks may be tested with two capacitance measurements. Finally, a test structure is shown in figure 13 which allows the detection of misalignment of metallization to contact opening along any direction with a current detection measurement. Basically, this structure consists of a metallization pad on a slightly larger oxide pad which in turn lies on a larger area of bare diffused silicon. Misalignment of the two pads is electrically detected when the metallization extends beyond the oxide and contacts the diffused silicon. When several such structures with different sized oxide pads are used, a digital measure of alignment can be obtained.

A method for electrically measuring process-induced changes in dimensions is useable when films of uniform thickness and resistivity can be fabricated over the extent of the test structure. A sketch of such a structure is shown in figure 14. The starting or designed dimensions, W_{1d} and W_{2d}, differ from the actual and final dimensions, W_1 and W_2, by a constant amount, $2W_{oe}$, introduced by fabrication procedures. Knowing W_{1d} and W_{2d} at the enlarged artwork stage, W_{oe} may be obtained by passing a constant current through the structure and measuring the voltage drops, V_1 and V_2, along equal lengths, L, on the wide and narrow stripes, respectively. Evaluating the ratio $\alpha = V_2/V_1$, W_{oe} may be calculated using the following equation,

$$W_{oe} = \frac{W_{1d} - \alpha W_{2d}}{2(1 - \alpha)} .$$

The value of the current should be sufficiently large to allow accurate measurements of V_1 and V_2. For adequate sensitivity, the test structure should be designed so that W_{1d} is 3 to 10 times larger than W_{2d}, and so that W_{2d} is 5 to 10 times larger than the expected value of W_{oe} and larger than any irregularity of the edges. If the magnitude of the irregularity is of the order of W_{oe}, accurate measurement of W_{oe} can still be obtained if L is much greater than W_{oe}. However, if irregularities in the edge are severe, the technique cannot be used. For well-designed structures, a W_{oe} as small as about 1 μin (≈ 0.03 μm) can be measured.

Examples of several types of data outputs are described and illustrated next. The first is an example of plotting one parameter against another; in particular, a capacitance-voltage (C-V) plot of an SOS silicon gate MOS capacitor is shown in

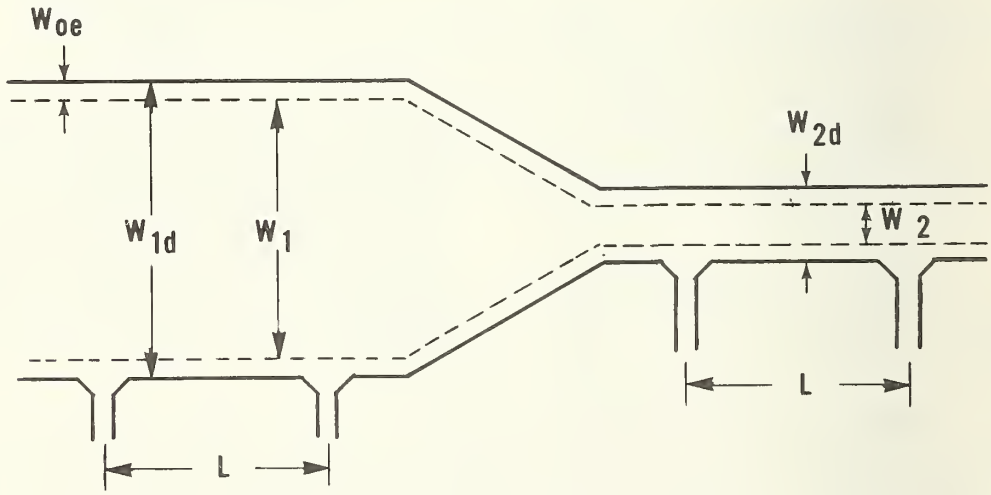


Figure 14. Top view of test structure for measuring the difference, $2W_{oe}$, between the starting dimensions, W_{1d} and W_{2d}, and the final ones, W_1 and W_2, which is introduced by fabrication procedures.

figure 15. The plot displays hysteresis, kinks, and noise. While it is possible to interpret such data on an individual basis, analysis on a fully automated system would be impractical. Such curves have what is called high structure and are suitable only for plotting on a semiautomatic system. Another type of plot on the semiautomatic system is shown in figure 16 where one parameter is plotted against another with a position variable introduced. Here the drain characteristic at a specific gate voltage along a line on the wafer is illustrated. This plot can be generated directly on an x-y recorder in a matter of 10 minutes without need of a computer.

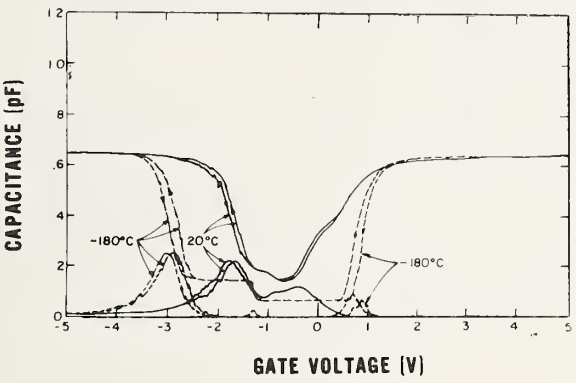


Figure 15. Example of a data output where one parameter is plotted against another.

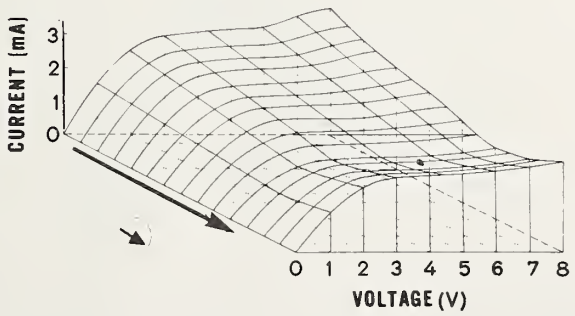


Figure 16. Example of a data output where one parameter is plotted against another with a position variable introduced.

An example of a correlation or scatter plot is shown in figure 17 where the field-effect mobility is plotted against carrier concentration, as measured with a capacitor and analyzed automatically. A definite trend is seen but the scatter of data points indicates that other parameters affect the field-effect mobility.

A presentation that has been useful is the one shown in figure 18 where the magnitude of a parameter (in this case threshold voltage) over a wafer is indicated by the character used. An asterisk is used for the larger, no character for the lower, and a period for the in-between values of the parameter. The numerical values of the threshold voltage over the wafer may also be printed out. A histogram presentation, aside from missing the trend in the value of threshold voltage over the wafer, might show a standard deviation that would be much greater than would be expected over any one die from the wafer.

Another way of displaying data is by way of "three-dimensional" (3D) plots which can reveal correlations more effectively than correlation or scatter plots. The 3D variation of sheet resistance over a wafer is shown in figure 19. In one particular case, a strong correlation between carrier concentration and threshold voltage was apparent with such 3D displays, but the correlation was not as clearly shown in

Figure 17. Example of a correlation, or scatter, plot where the field-effect mobility is plotted against carrier concentration.

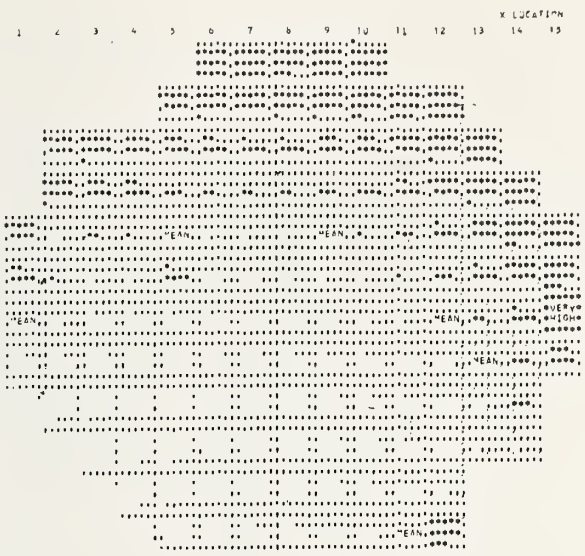


Figure 18. Map of threshold voltage where the magnitude of threshold voltage is indicated by the darkness of the position characters.

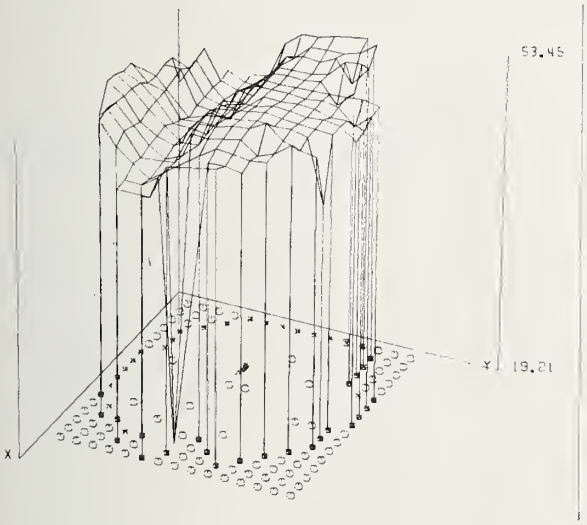


Figure 19. "Three-dimensional" plot of sheet resistance over wafer.

scatter point plots such as that in figure 17. The variation in carrier concentration and threshold voltage were both correlated with the thickness of the epitaxial layer which suggested that greater uniformity in threshold voltage could be attained across the wafer by increasing the uniformity in epitaxial thickness. Variation in the thickness of an epitaxial layer on a sapphire wafer can be revealed with a single photograph of interference fringes generated by a mercury vapor lamp.

Finally, an example is given of a case where the test patterns to measure a parameter were too far apart over the wafer to give any trend data. This example is shown in figure 20 where the distribution of leakage current is given over the wafer. It points to the necessity of not only having an appropriate test structure to measure the desired parameter but also of making sure that the parameter varies smoothly enough to be able to characterize the wafer with confidence using the test structure selected.

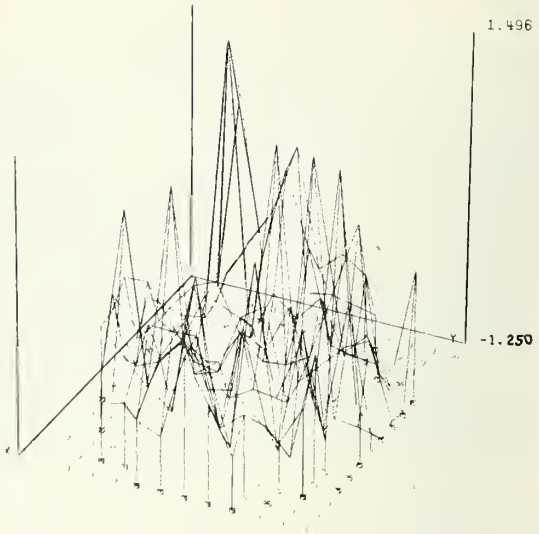


Figure 20. A "three-dimensional" plot where the test patterns used to measure the parameter were too far apart over the wafer to provide trend data.

5.3 *Discussion Period*

Boyd was asked to estimate the effort and cost of developing the data acquisition system he described. He stated that it was difficult for a number of reasons to give precise figures on the time and manpower that was required. Much of the hardware was already available and some considerable effort had already been invested when he took charge. He was involved on the project with the assistance of at least two engineers for the last two years. At the present time the system was still incomplete, needing the incorporation of additional memory, display, and recording capabilities.

He continued by reiterating that it is of absolutely critical importance in the design of such a system that it be easy to use. Otherwise it will not be used. Without a well designed system to present data one is faced with having a mass of data distributed over many sheets of paper that one would literally have to walk along to examine if they were laid out. In such a situation it is impossible for anyone to absorb and analyze the available information.

Ham was asked how the test pattern work he described is transferred to a production environment. He replied that they are at a process understanding stage from which process control can evolve. The thrust of his test pattern work is to determine the capability of the SOS technology so that a circuit designer will know what is possible to produce.

Regarding a question about the capability to perform impurity profiles, Ham replied that they are able to obtain any profiles that C-V measurements can provide in the frequency range from 10 Hz to 1 MHz.

6. NBS Activities

6.1 *NBS Plans for Test Pattern Implementation*

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National Bureau of Standards
Washington, D. C. 20234

The capabilities of a newly acquired computer system and the results of measurements on two test patterns were described. These activities are part of a significant effort at NBS to develop various test structures and encourage their use in the production of integrated circuits. The reason for this effort is that the information obtained from test patterns can be used for process control, for device design, and for the assurance of circuit reliability. At the buyer-seller interface, they can be used to give the buyer confidence in the product he has purchased.

The first test pattern described, NBS-2, is shown in figure 21 with its structures identified in table 4. This test pattern [1] was developed in 1973 to identify problem areas in the NBS fabrication facility and to allow for the development of a variety of measurement methods, such as the junction capacitance-voltage dopant profiling method. Mask sets for test pattern NBS-2 are available on request.* To date, NBS-2 has been made available to thirteen other organizations.

The test pattern is arranged in a square, 200 mil (5 mm) on a side, and uses the concept of modularization. The many structures in NBS-2 were utilized to reveal a number of problem areas in the NBS fabrication facility. For example, measurements of the MOS capacitors indicated processing problems caused by the water which led to the decision to up-grade the in-house water system; measurements of the collector resistor revealed poor backside contact caused by using undoped gold. The capabilities of the NBS processing facility, which was established to satisfy in-house needs, are summarized in part A of table 5. Those capabilities which are being incorporated or soon will be added to the facility are listed in part B of table 5.

The base-to-metal contact resistor (structure 16 of figure 21) is particularly useful in determining if contact windows have been adequately opened. A schematic drawing of this test structure is shown in figure 22. Current is passed between contacts 1 and 4 while the voltage is measured at contacts 2 and 3. In effect, a measure of the resistance at the contact window A is obtained. While this structure needs to be analyzed in greater detail to obtain a quantitative measurement of the specific contact resistance, the qualitative measure of resistance it provides proves very useful for process control.

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*Requests for releasing the four mask sets from a commercial mask-making company should be made directly to M. G. Buehler, National Bureau of Standards, Washington, D. C. 20234. The cost of the set is approximately $100.

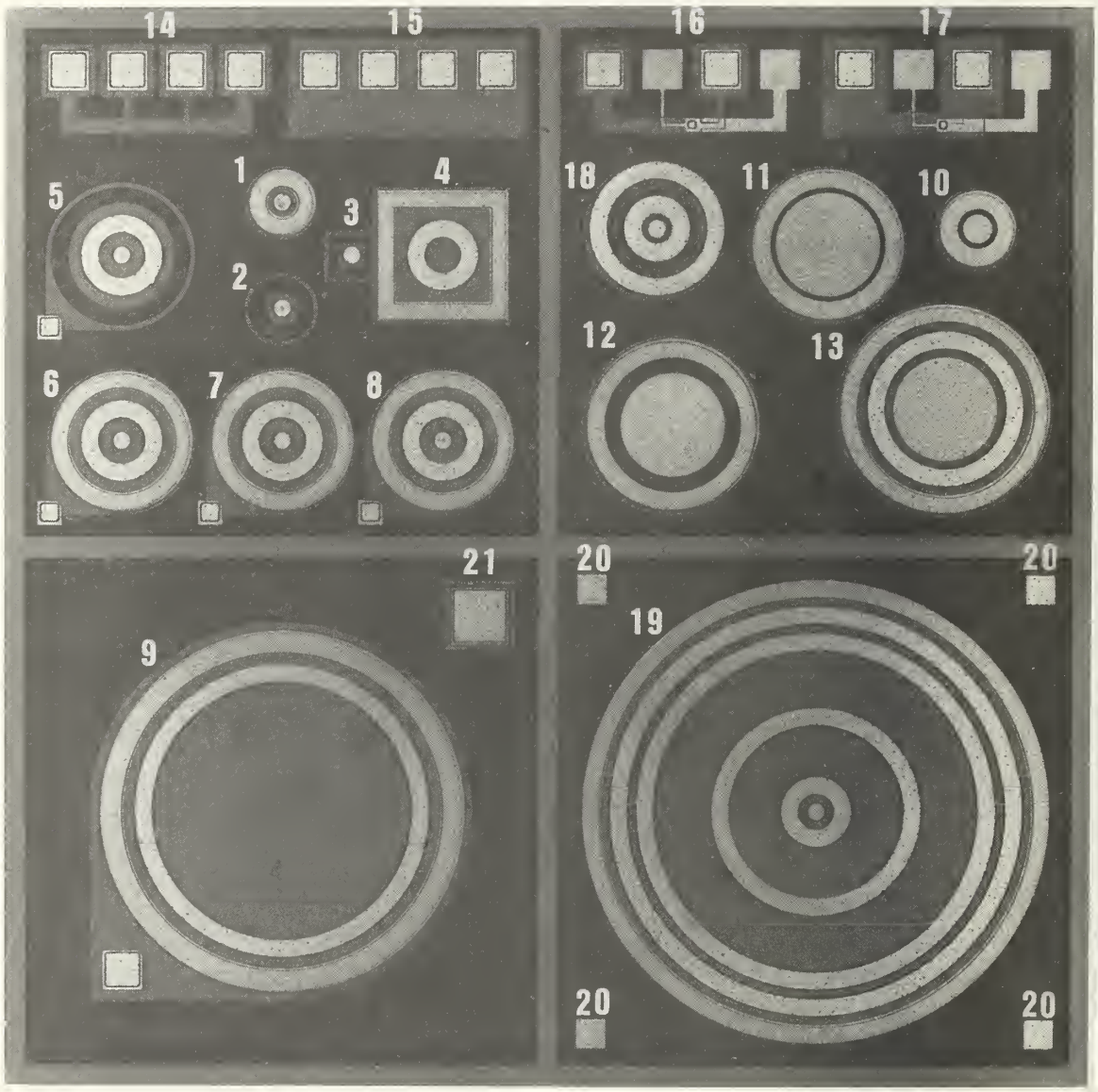


Figure 21. Test pattern, NBS-2, for characterizing the electrical properties of silicon MOS capacitors and *p-n* junctions. The 21 elements are identified in table 4. The overall pattern is 200 mils (5.08 mm) on a side.

Table 4. Planar Test Structures on Test Pattern NBS-2

Number	Test Structure	Number	Test Structure
1	Gated circular base-collector junction with diffused channel stop	10	MOS capacitor over collector with field plate and diffused channel stop
2	Ungated circular base-collector junction with diffused channel stop	11	MOS capacitor over collector with field plate and diffused channel stop
3	Ungated square base-collector junction with diffused channel stop	12	MOS capacitor over collector with distant field plate and diffused channel stop
4	Gated square base-collector junction with diffused channel stop	13	MOS capacitor over base without field plate and diffused channel stop
5	Ungated circular base-collector junction with diffused channel stop	14	Base sheet resistor
		15	Emitter sheet resistor
6	Gated circular base-collector junction with diffused channel stop	16	Metal-to-base contact resistor
		17	Metal-to-emitter contact resistor
7	Gated circular base-collector junction (small emitter) with diffused channel stop	18	Collector resistor
		19	Base-under-the-emitter sheet resistor (tetrode transistor)
8	Gated circular base-collector junction (large emitter) with diffused channel stop	20	Hall effect pattern
9	Gated circular base-collector junction with diffused channel stop	21	Alignment marker

Table 5. Capabilities of NBS Processing Facility

A. Present	B. Future
Oxidization	Epitaxial layer growth
P-type diffusion (BN)	HCL oxides
N-type diffusion (PH_3)	New DI water system
Metallization (Au, Al)	Passivation
Scribe	Hermetic encapsulation
Mount	
Bond	

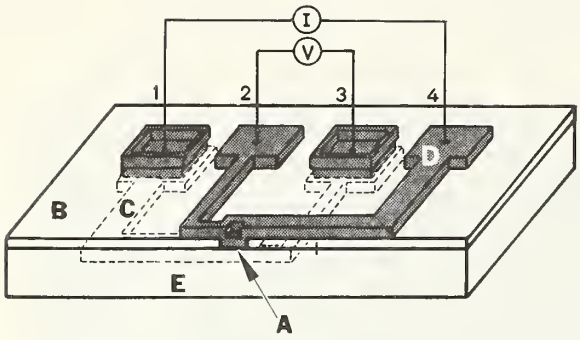


Figure 22. Schematic view of a section through the contact window of the metal-to-base contact resistor test structure 16 from test pattern NBS-2. The current path is through pad 4, the metallization stripe (D), the contact window (A), the p^+ diffused layer (C), and contact pad 1. To measure the potential difference, V, contact is made to the metal side of the contact window through the narrow metallization stripe leading to pad 2 and to the diffused-layer side by the narrow diffused region leading to pad 3. The metallization is isolated from the diffused layer and the n-type silicon substrate (E) everywhere except at pads 1 and 3 and the contact window (A) by an oxide layer (B).

The second test pattern, NBS-3, was designed primarily for use in reconstructing the Irvin curve which relates resistivity to ionized or total dopant density. The original Irvin curve [10] for p-type material is shown in figure 23 by the solid curve. The dashed line is from the more recent data of Wagner [11]. This figure illustrates a discrepancy of nearly 50 percent in the resistivity over the dopant density range from 10^{17} to 10^{18} cm^{-3}. NBS took part in initial measurements conducted under the auspices of the Mobility Section of the ASTM Committee F-1 on Electronics on several boron-doped silicon wafers having different dopant densities. Data points from these measurements are included in figure 23 and indicate an even greater deviation from the Irvin curve at high dopant densities than is indicated by Wagner's curve.

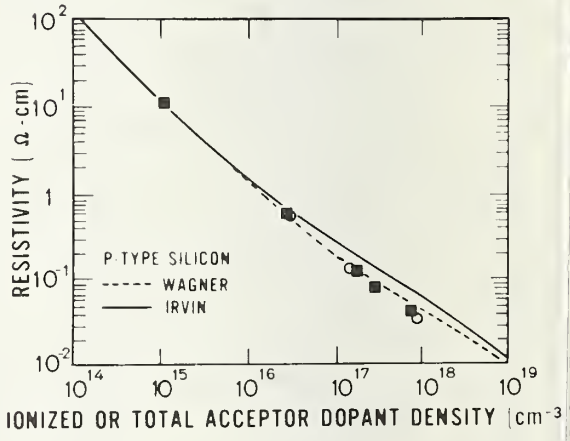


Figure 23. Resistivity as a function of dopant impurity density for p-type silicon. The data points shown as circles were obtained from capacitance-voltage and four-probe resistivity measurements, and the points shown as squares were derived from Hall effect and four-probe resistivity measurements. The curves are taken from the work of Irvin [10] and Wagner [11].

Test pattern NBS-3 is arranged in a square, 200 mil (5 mm) on a side, and is shown in figure 24. The test structures in NBS-3 that are to be used in the reevaluation of the Irvin curve are indicated by asterisks in table 6 where all the test structures of NBS-3 are identified. The test structures in NBS-3 provide for flexibility and cross-correlation of different methods and structures. Some of the test structures are intended to assure that the test

pattern was fabricated properly and to aid in diagnosing problems. Basically, two structures will be used in the Irvin curve evaluation: the base-collector diode (structure 10), from which the collector dopant density will be measured by use of the junction capacitance-voltage method, and the square array collector resistor (structure 17), from which the collector resistivity will be measured.

Test pattern NBS-3 also contains a base sheet resistor (structure 30) used to measure the incremental sheet resistance after successive anodic oxidations in order to determine base dopant profiles. This structure is scribed out of the chip and then bonded to a TO-5 header and electrically connected to the header terminals with wire bonds as illustrated in figure 25. The surface within the circular area is removed by anodic oxidation after the heater is placed in a teflon holder and the electrolyte introduced.

The probe station that has been in use at NBS for over a year is shown in figure 26. A wafer is located on a variable temperature stage which is fixed spatially. Probes must move in an XYZ direction to make contact with the wafer. The stage is housed in a box with a cover so that measurements can be made in the dark. The characteristics of this stage as well as a second newly designed stage are shown in table 7 along with ultimate goals for a future stage.

A computer controlled data acquisition and reduction system, designed for flexibility to accommodate a wide variety of experiments, has recently been put into operation. A functional block diagram of the system with a summary of its characteristics is shown in figure 27. The system incorporates a digital oscilloscope with three preamplifiers and one time-base plug-in for measuring capacitance (C), current (I), and voltage (V), as functions of time. The signals from the plug-ins are digitized into data points with four significant figures. The time to obtain one digitized data point is about 6 μs which allows analyses of a variety of transient phenomena. The digitized data can be manipulated by the computer, programmed in BASIC, for a variety of displays on a cathode-ray tube (CRT) display terminal. A hard copy of the display can also be obtained in a matter of seconds after the display is completed. The system can provide a display of the spatial distribution of the steady-state or time-wise variation of a parameter over a wafer, or a display of the transient variation of a parameter at a given location. The kinds of structures and measurements that the system is intended to address are listed in table 8.

An example of a display that can be obtained is shown in figure 28. The display is of the spatial distribution of the sheet resistance as measured on a bridge-type sheet resistor (structure 28). Using a probing machine that has recently been interfaced with the system, such a display can be generated in about 1.5 min.

In the area of data acquisition, the plans are to develop and promote use of probe stations interfaced with minicomputers that can conveniently and quickly make measurements of a great variety of characteristics over a wide range of conditions,

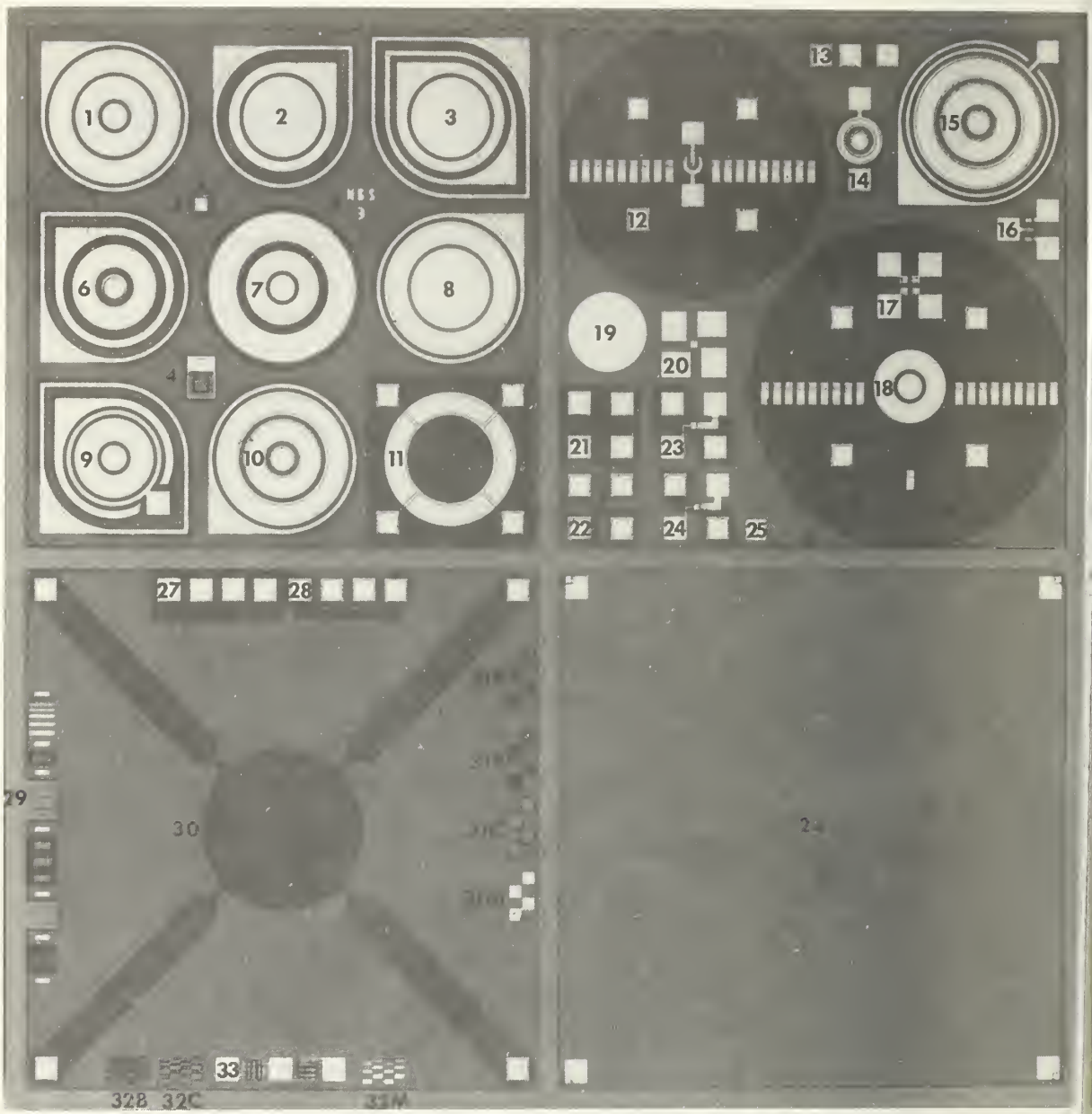


Figure 24. Test pattern, NBS--3, for characterizing the resistivity-dopant density relation in silicon. The 33 test structures are identified in table 6. The overall pattern is 200 mils (5.08 mm) on a side.

Table 6. Planar Test Structure on Test Pattern NBS-3

1.	Gated collector resistor*	18.	Large collector spreading resistor*
2.	MOS capacitor over base	19.	Ungated MOS capacitor over collector
3.	MOS capacitor over emitter	20.	Metal sheet resistor
4.	Alignment markers	21.	Emitter sheet resistor
5.	Logo	22.	Base sheet resistor
6.	Tetrode transistor*	23.	Metal-to-emitter contact resistor
7.	Guarded collector resistor*	24.	Metal-to-base contact resistor
8.	Gated MOS capacitor over collector*	25.	Small MOS capacitor over collector
9.	Gated emitter-base diode*	26.	Hall effect device
10.	Gated base-collector diode*	27.	Emitter sheet resistor
11.	Gated base sheet resistor	28.	Base sheet resistor
12.	Small collector spreading resistor*	29.	Surface profilometer structure
13.	Small bipolar transistor	30.	Incremental base sheet resistor
14.	Small gated base-collector diode	31.	Etch control structures
15.	Large MOSFET	32.	Resolution structure
16.	Small MOSFET	33.	Metal step-coverage resistor
17.	Square array collector resistor*		

*structures designed for resistivity-dopant density evaluation

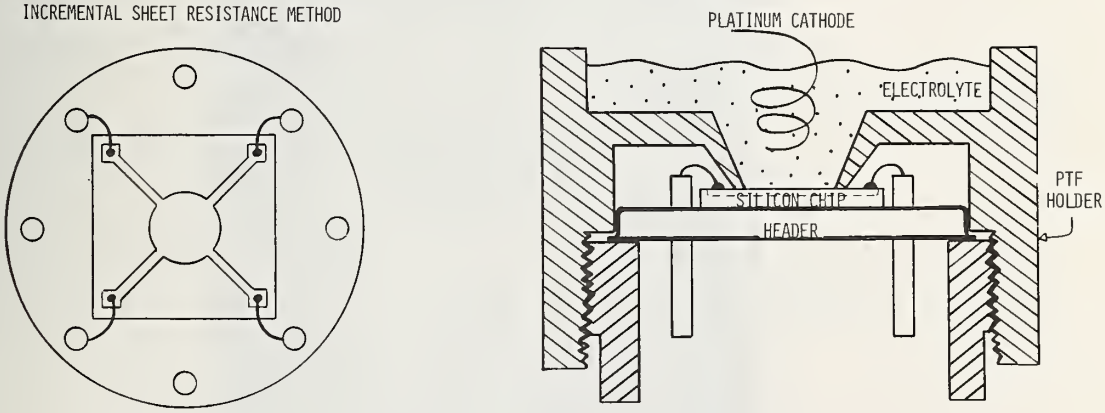
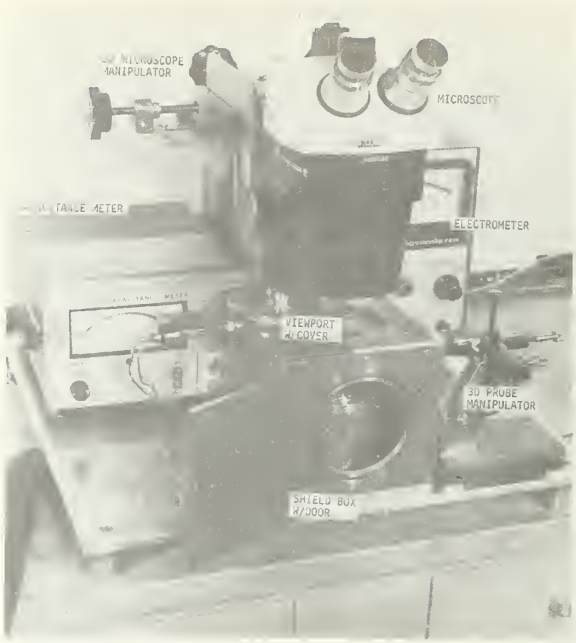
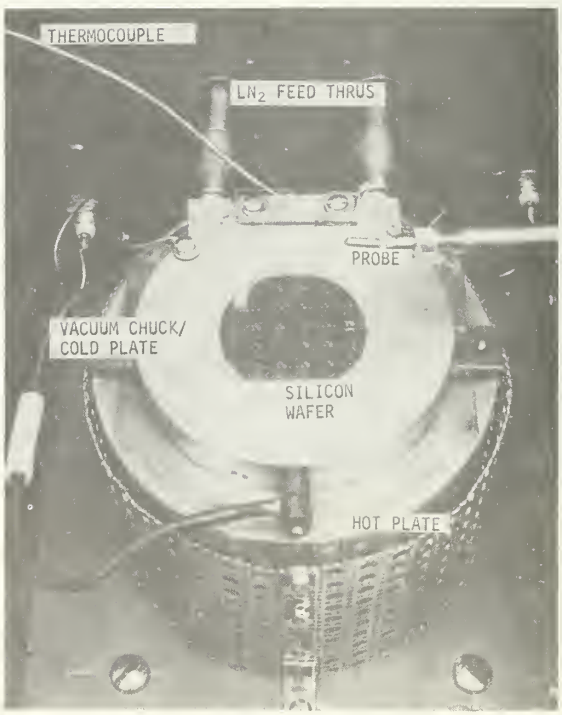


Figure 25. A. Top view of a base sheet resistor structure (number 30 in test pattern NBS-3) bonded to a TO-5 header and electrically connected to the header terminals. B. Sketch of cross sectional view of holder designed for the determination of dopant density profiles by the incremental sheet resistance method with test structure 30 in place. PTF refers to the material polytetrafluoroethylene.



a. Overall view.



b. Close up of stage with shield box partially removed.

Figure 26. Hot-cold stage for wafer characterization.

Table 7. Hot/Cold Wafer Probe Stages

CHARACTERISTICS	STAGE 1	STAGE 2	GOAL
THERMAL			
range	77 to 573 K	77 to 573 K	77 to 573 K
coolant	liquid nitrogen	liquid nitrogen	liquid nitrogen
heater	resistive	resistive	resistive
rate	0.5 K/s	5 K/s	10 K/s
uniformity	--	--	± 1 K
ELECTRICAL			
stage isolation	> 10^{13} Ω	> 10^{13} Ω	> 10^{13} Ω
ENVIRONMENTAL			
light ambient	dark	dark	dark
gas ambient	dry nitrogen	vacuum	vacuum
MECHANICAL			
wafer hold	vacuum	clamp	clamp
probes	one	four	six
stage motion	none	XY	XYZ
probe motion	XYZ	Z	none
microscope motion	XY	none	none

manipulate the data taken, and present it in ways that will allow quick and effective evaluation of the data by process engineers.

To facilitate the implementation of the output of the test pattern work, NBS plans to continue its participation in the work of such sections as 6.4 (Mobility) and 11.5 (Process Controls) of the ASTM Committee F-1 on Electronics; work with other government laboratories; promote interaction within the electronics community, such as by workshops; and publish, particularly in the NBS Special Publication 400 subseries.

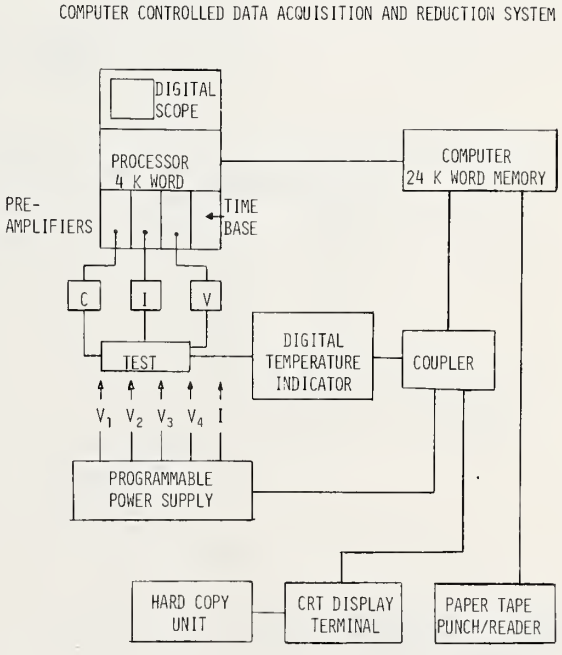


Figure 27. Computer controlled data acquisition and reduction system.

Table 8. Computer Controlled Data Acquisition and Reduction System Test Structure Measurements

STEADY STATE MEASUREMENTS

Test Pattern	Measurements	Parameter
gated *pn* junction	current-voltage	recombination velocity
gated *pn* junction	capacitance-voltage	inversion potential
pn junction	capacitance-voltage	dopant profile
pn junction	capacitance-voltage/current-voltage	lifetime
MOS capacitor	capacitance-voltage	oxide charge
four probe resistor	current-voltage	contact/sheet resistance

TIME-WISE MEASUREMENTS

Test Pattern	Measurements	Parameter
pn junction	capacitance-temperature	defect density
pn junction	current-temperature	leakage defects
MOS capacitor	capacitance-voltage	deep-depletion dopant profile
four probe resistor	current-voltage	mobility

TRANSIENT MEASUREMENTS

Test Pattern	Measurements	Parameter
gated *pn* junction	capacitance-time	defect energy levels
gated *pn* junction	current-time	reverse recovery lifetime
MOS capacitor	capacitance-time	lifetime

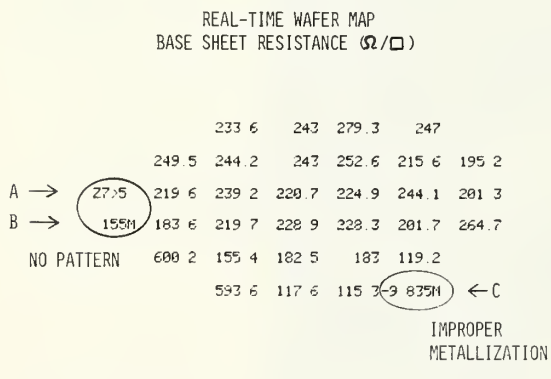


Figure 28. A print-out of the base sheet resistance distribution across a 1.5 in (38 mm) diameter wafer as measured with a bridge-type sheet resistor (structure 28 of test pattern NBS-3). Anomalous readings are indicated at A, B, and C. At A, the probes are beyond the edge of the wafer as indicated by the code 27>5. Improper metallization at B and C are indicated by the low and negative resistance readings (M represents mΩ).

RESISTANCE (OHMS) FOR + AND - I= 1(MA)
RESISTANCE BOUND= 625(OHM)
R VERT= .5(Ω/DIV), A HOR= 1E-3(S/DIV), B HOR= 1E-3(S/DIV)
GEOMETRICAL FACTOR = .25
PROGRAM 74.1.6 (8/29/74)

6.2 *Discussion Period*

Interest in the NBS work on the Irvin curve diverted some of the discussions from test patterns. Concern was expressed by several participants about being able to relate the number of ionized impurities, which would be measured by the NBS test structures, to the total number of impurities which are used in Irvin's original curves. While this could be done satisfactorily by using Fermi-Dirac statistics for the lower impurity concentrations, this may not be possible for impurity concentrations above 10^{18} cm^{-3} because of inadequacies in the available models for impurities at such high concentrations. This was recognized as a problem by Buehler who asked, what is important to the industry, the total number of atoms present or the total number of electrically-active (ionized) impurities? One participant responded by saying that it is the total number of impurities because there is a need to know the number of ionized impurities at high temperatures.

A question was put to the audience about the willingness of device manufacturers to accept test patterns from prospective customers for use on the production line to verify that given processes are under control. There did not appear to be any objection to this from the vendor participants. However, vendor participants appeared to be opposed to letting customers examine wafers with the test patterns in place to evaluate various vendors regarding their capability for producing circuits designed by the customer. The reason for the opposition is that to do so would make available information about yield and design rules that vendors consider highly proprietary. However, it was pointed out that one government organization does just that but that it is done with the agreement that the information obtained is not divulged.

Acknowledgement

I wish to express my gratitude to the speakers for their cooperation in the preparation of this report; they readily provided most of the visual aids they used in their talks, sent useful supplemental visual and written materials, and reviewed their parts of the report. Thanks go to W. Murray Bullis and to Martin G. Buehler for their editorial and technical assistance, to Leo R. Williams for his work with the figures, and to Frances C. Butler for typing the final and camera-copy draft of the report.

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16. ABSTRACT *(A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.)*

Synopses are presented of talks and discussion periods at a meeting on the use and development of MOS and bipolar test patterns and associated data acquisition systems. The discussions revealed that device manufacturers and users are making increased use of test patterns as powerful new measurement tools that can electrically monitor various process parameters to aid in the control of materials, wafer processes, circuit performance, and reliability. However, the large volume of data generated from these test patterns and the requirement for rapid diagnostic feedback present severe challenges in data management and display. In this report several data acquisition systems are described, as are approaches for presenting data in more easily interpretable graphic displays. The need for improvements in the design of test patterns is emphasized. In particular, problems with measuring contact resistance and the properties of oxides, surfaces, and defects, are identified. Numerous test structures are described including charge coupled device structures which can measure some characteristics not easily measured by other means. Also described are NBS's efforts and plans to identify, analyze, and intercompare selected test structures of value to the industry and its customers, and to develop measurement methods for use with these structures.

17. KEY WORDS *(six to twelve entries; alphabetical order; capitalize only the first letter of the first key word unless a proper name; separated by semicolons)*

Data acquisition; data display; integrated circuits; measurement technology; microelectronics; process control; reliability; semiconductors; silicon; test patterns.

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