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Semiconductor Measurement Technology

Quarterly Report

July 1 to September 30, 1973

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[1] Headquarters and Laboratories at Gaithersburg, Maryland, unless otherwise noted; mailing address Washington, D.C. 20234.
[2] Part of the Center for Radiation Research.
[3] Located at Boulder, Colorado 80302.
[4] Part of the Center for Building Technology.

Semiconductor Measurement Technology

Quarterly Report, July 1 to September 30, 1973

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Electronic Technology Division
Institute for Applied Technology
National Bureau of Standards
Washington, D.C. 20234

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PREFACE

The Semiconductor Technology Program serves to focus NBS efforts to enhance the performance, interchangeability, and reliability of discrete semiconductor devices and integrated circuits through improvements in measurement technology for use in controlling device fabrication processes and in specifying materials and devices in national and international commerce. Its major thrusts are the development of carefully evaluated and well documented test procedures and associated technology, for use on production lines and in the exchange of devices and materials, and the dissemination of such information to the electronics community. Application of the output by industry is expected to contribute to higher yields, lower cost, and higher reliability of semiconductor devices. In addition, the improvements in measurement technology will lead to greater economy in government procurement and will provide a basis for controlled improvements in fabrication processes and in essential device characteristics.

The Program receives direct financial support principally from three major sponsors: the Defense Advanced Research Projects Agency (ARPA),* the Defense Nuclear Agency (DNA),† and the National Bureau of Standards (NBS).× The ARPA-supported portion of the Program, Advancement of Reliability, Processing, and Automation for Integrated Circuits with the National Bureau of Standards (ARPA/IC/NBS), addresses critical Defense Department problems in the yield, reliability, and availability of integrated circuits. The DNA-supported portion of the Program emphasizes aspects of the work which relate to radiation response of electron devices for use in military systems. There is considerable overlap between the interests of DNA and ARPA and both interests parallel the measurement-oriented mission of NBS.

Cooperation with industrial users and suppliers of semiconductor devices is achieved through NBS participation in standardizing organizations; through direct consultations with device and material suppliers, government agencies, and other users; and through periodicall scheduled symposia and workshops. In addition, progress reports, such as this one, are regularly prepared for issuance in the NBS Special Publication 400 sub-series. More detaile reports such as state-of-the-art reviews, literature compilations, and summaries of technica efforts conducted within the Program are issued as these activities are completed. Reports of this type which are published by NBS also appear in the Special Publication 400 sub-serie Announcements of availability of all publications in this sub-series are sent by the Government Printing Office to those who have requested this service. A request form for this purpose may be found at the end of this report.

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* Through ARPA Order 2397, Program Code 4D10 (NBS Cost Center 4259555).

† Through Inter-Agency Cost Reimbursement Order 74-811 (NBS Cost Center 4259522).

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SEMICONDUCTOR MEASUREMENT TECHNOLOGY

QUARTERLY REPORT
JULY 1 TO SEPTEMBER 30, 1973

Abstract: This quarterly progress report, twenty-first of a series, describes NBS activities directed toward the development of methods of measurement for semiconductor materials, process control, and devices. Principal accomplishments during this reporting period include (1) extension of the technique for measuring thermally stimulated current and capacitance to include measurements on MOS capacitors, (2) completion of the development of the thermal response method for evaluation of transistor die attachment, (3) analysis of the interlaboratory comparison of transistor scattering parameter measurements, (4) preliminary review of measurement problems in the photolithographic aspects of semiconductor device processing, of problems associated with certain hermeticity testing procedures, and of methods for evaluating metallization step coverage, and (5) initiation of new activity on characterization of oxide films in MOS structures and analysis of diffusion profiles. Results are also reported on spreading resistance, capacitance-voltage, and sheet resistance measurements; the activation energy of the gold acceptor in silicon; evaluation of the base-to-metal contact resistor test structure; metallurgical systems for ultrasonic bonding; burn-out characteristics of fine gold and aluminum bonding wire; transistor thermal resistance measurements; and microwave diode conversion loss measurements. Supplementary data concerning staff, publications, workshops and symposia, standards committee activities, and technical services are also included as appendices.

Key Words: Contact resistance; die attachment; dopant profiles; electrical properties; electronics; gold-doped silicon; hermeticity; metallization; methods of measurement; microelectronics; microwave diodes; mobility; MOS devices; oxide films; photomasks; photoresist; resistivity; resistivity standards; scanning electron microscopy; semiconductor devices; semiconductor materials; semiconductor process control; sheet resistance; silicon; S-parameters; spreading resistance; test patterns; thermal resistance; thermally stimulated capacitance; thermally stimulated current; wire bonds.

1. INTRODUCTION

This is the twenty-first quarterly report to the sponsors of the Semiconductor Technol- Program. It summarizes work on a wide variety of measurement methods for semiconductor erials, process control, and devices that are being studied at the National Bureau of ndards. The Program is a continuing one, and the results and conclusions reported here subject to modification and refinement.

The work of the Program is divided into a number of tasks, each directed toward the dy of a particular material or device property or measurement technique. This report is divided according to these tasks. Highlights of activity during the quarter are given in tion 2. Subsequent sections deal with each specific task area. References cited are ted in the final section of the report.

INTRODUCTION

The report of each task includes a narrative description of progress made during this reporting period. Additional information concerning the material reported may be obtained directly from individual staff members identified with the task in the report. The organization of the Program staff and telephone numbers are listed in Appendix A.

Background material on the Program and individual tasks may be found in earlier quarterly reports as listed in Appendix B. From time to time, publications are prepared which describe some aspect of the program in greater detail. Current publications of this type are also listed in Appendix B. Reprints or copies of such publications are usually available on request to the author.

Communication with the electronics community is a critical aspect both for receiving guidance in planning future program activities and for disseminating results of the work to potential users. Formal channels for such communication occur in the form of workshops and symposia sponsored or co-sponsored by NBS. Currently scheduled seminars and workshops are listed in Appendix C. In addition, the availability of proceedings from past workshops and seminars is indicated in the appendix.

An important part of the work that frequently goes beyond the task structure is participation in the activities of various technical standardizing committees. The list of personnel involved with this work given in Appendix D suggests the extent of this participation In many cases, details of standardization efforts are reported in connection with the work of a particular task. Current standardization activities, including those not associated with a particular task, are summarized at the end of section 2.

Technical services in areas of competence are provided to other NBS activities and other government agencies as they are requested. Usually these are short-term, specialized services that cannot be obtained through normal commercial channels. To indicate the kinds of technology available to the program such services provided during the period covered by this report are listed in Appendix E.

2. HIGHLIGHTS

Considerable expansion in the scope of the program occurred during this reporting period h the inclusion of a new effort on Advancement of Reliability, Processing, and Automation Integrated Circuits with the National Bureau of Standards (ARPA/IC/NBS) funded by the ense Advanced Research Projects Agency. New tasks were established in the areas of insu- or films, photolithography, and hermeticity.

Significant technical accomplishments during this reporting period included:

1. extension of the technique for measuring thermally stimulated current and capacitance to include measurements on metal-oxide-semiconductor (MOS) capacitors,
2. completion of the development of the thermal response method for evaluation of transistor die attachment,
3. analysis of the interlaboratory comparison of transistor scattering parameter measurements, and
4. preliminary review of measurement problems in the photolithographic aspects of semiconductor device processing, of problems associated with certain hermeticity testing procedures, and of methods for evaluating metallization step coverage.

In addition, the first of a series of workshops to aid in communication with the elec- nics community was held. This workshop, on measurement needs for controlling integrated cuit processing and assembly, had the dual objectives of formally announcing the A/IC/NBS program to the semiconductor industry and of giving the industry a forum to pro- le additional input for use in program definition and planning. The results of the work- p are reported in detail elsewhere [1].

Following are highlights of other activities during this quarter.

Resistivity, Dopant Characterization — Development of calibration curves for the NBS eading resistance system continued with generation of the curve for n-type silicon in the ge 0.1 to 100 Ω·cm. Theoretical study of the application of the junction capacitance- tage method for measuring diffusion profiles continued with evaluation of the effect of dom errors in the measured values of capacitance and voltage on the derived net dopant sity on either side of the junction. Mathematical analysis of the boron redistribution blem began with formulation of the problem for both uniform and nonuniform initial dis- butions. The effect of uncertainty in mobility value on diffusion profiles derived from remental sheet resistance measurements was studied by comparing results obtained with the e of two different relationships for hole mobility as a function of impurity density in ype silicon. A multipass round-robin experiment between NBS and six experienced labora- ries was designed to test the stability and multilaboratory precision to be expected from e silicon resistivity standard reference materials now available.

Crystal Defects and Contaminants — The dynathermal current and capacitance responses a gold-doped n-MOS capacitor were found to display two distinct features: one, which is

similar to the feature in the junction response, is characteristic of electron emission from the gold acceptor, and a second at higher temperature, which is not found in the junction response, is characteristic of hole emission from the gold acceptor. Additional Hall effect measurements on a specimen of *n*-type silicon with a phosphorus density about 10^{15} cm^{-3} and a gold density about three times greater yielded an activation energy within less than 1 meV of that obtained earlier on a less heavily doped specimen.

Insulator Films — Studies of silicon oxide films by ion microprobe mass analysis, electron spectroscopy for chemical analysis, and Auger spectroscopy are being initiated. Apparatus is being designed and constructed for use in studying the bias-temperature stress test for characterizing oxide stability. At the request of one of the major sponsors, a program has been initiated to document procedures and tests necessary to achieve radiation-hardened MOS integrated circuits.

Test Patterns — Several modifications were made in the processing procedure as part of a continuing task to demonstrate the application of test patterns in improving and controlling fabrication processes. Although some improvements were made, further iterations are needed to achieve desired values for various characteristics. Study of the metal-to-base contact resistor test structure showed that although the normalization of the measured contact resistance is uncertain, this structure is suitable for identifying deviations from nominal values of contact resistance which might occur in a production run.

Wafer Inspection and Test — Construction was begun of an optical flying-spot scanner for use in evaluating damage to device structures during inspection or test with a scanning electron microscope.

Interconnection Bonding — Characterization of metallurgical systems for ultrasonic bonding continued with confirmation of the previously reported high bond strength for gold wire on aluminum pads, tentative establishment of suitable bonding conditions for gold wire on gold thick-film metallization, and determination of compatible schedules for bonding aluminum wire both to aluminum thin-film bonding pads on silicon dioxide over silicon and to gold thick-film metallization on alumina substrates. A brief study was carried out on the burn out of fine gold and aluminum wire as a result of Joule heating. In addition to the technical effort, dissemination of the methods and technology developed for controlling and testing ultrasonic wire bonding continued at a high level throughout this period.

Thermal Properties of Devices — Repeatability tests of the emitter-base voltage, emitter-only switching technique for measuring thermal resistance of transistors were completed. Additional calculations with a somewhat more complex model were carried out to establish an appropriate extrapolation procedure for use in analyzing thermal resistance measurements; as in the simpler case, a plot of the logarithm of surface temperature as a function of time results in the most nearly straight lines over the appropriate range of delay times.

Microwave Diodes — Additional repeatability studies of the conversion loss measurement stem were made using Schottky-barrier mixer diodes. Groups of diodes were selected for e in a study of the effect of gamma and neutron irradiation on the noise characteristics these diodes.

Standardization Activities — Fifteen staff members participated in the fall meetings ASTM Committee F-1 on Electronics, held in Palo Alto, California, on September 5-7. Most so assisted with the first ARPA/NBS Workshop, held on the final day of the Committee etings.

Editorial work was carried out on five ASTM Committee F-1 draft documents and was itiated on an EIA-JEDEC document. Two documents were reviewed technically for other andards groups. Work continued on two round-robin experiments being conducted by ASTM mmittee F-1.

Dissemination Activities — Organizational activities were undertaken for a workshop on diation Effects in MOS Technology. This workshop, cosponsored by the IEEE Nuclear and asma Sciences Society, the IEEE Electron Devices Group, and NBS, is scheduled for December and 7, 1973, at Washington, D. C. No proceedings of this Workshop are to be printed.

Planning activity also continued for the Spreading Resistance Symposium, scheduled for ne 13-14, 1974, at Gaithersburg, Maryland (NBS Tech. Note 788, p. 64). This symposium is sponsored by ASTM Committee F-1 and NBS. It will immediately follow the June meeting of e committee.

Hermeticity was selected as the subject of the second ARPA/NBS Workshop, which is heduled to be held on March 29, 1974, at Gaithersburg, Maryland. Topic areas to be dis-ssed include failure due to leaks (correlation of leak rate and failure, failure mechanisms, ntamination analysis, and nature of leaks) and evaluation and intercomparison of leak rate asurement procedures (helium mass spectrograph, radioisotope, and new methods).

The third ARPA/NBS Workshop was tentatively scheduled for September 5 and 6 in Scotts-le, Arizona. The subject of this Workshop is design, evaluation, and use of test patterns. is designed to follow and supplement an informal mini-symposium on test patterns planned r the January meeting of ASTM Committee F-1 in New Orleans.

3. RESISTIVITY; DOPANT PROFILES

3.1. Spreading Resistance Methods

In preparation for constructing a calibration curve for phosphorus-doped silicon, a series of wafers was screened for radial uniformity using the spreading resistance instrument. Each wafer was freshly chem-mechanically polished on the surface to be probed by spreading resistance and lapped on the opposite side. Four-probe resistivity measurements were made on the lapped surface of 13 wafers which showed less than 10 percent variation in spreading resistance within the central half-radius region. These had room temperature resistivity in the range from about 0.1 to 100 Ω·cm. There was a linear relationship between spreading resistance and resistivity as measured by the four-probe method, but there were discrepancies of as much as 30 percent from the line of regression. No further work will be undertaken until a more complete set of specimens of *n*-type material is available to fill out the calibration curve.

Discrepancies of 50 to 80 percent in the calibration of spreading resistance for high resistivity boron-doped wafers, previously reported, have not yet been explained. A set of wafers adjacent to those which yielded some of the most discrepant points previously observed in this *p*-type material was prepared by the same chem-mechanical polishing treatment as before but measurement of these wafers has not yet been completed.

(J. R. Ehrstein and D. R. Ricks)

3.2. Junction Capacitance-Voltage Method

Theoretical investigation continued into the feasibility of using capacitance-voltage (C-V) measurements to profile a layer diffused into homogeneous background material. Previously, it was shown that this method requires the background dopant density, N_b, to be known to 1 percent or better in order to obtain a reasonably accurate diffused-layer profile (NBS Tech. Note 806, pp. 10-12). In the present phase, effects of variation in measurement of capacitance and voltage on the profile were studied. As an illustration, idealized C-V data corresponding to junction voltage between 0.3 V forward bias and 100 V reverse bias were generated for the case of a Gaussian diffusion in which the surface dopant density, N_0, was 10^{17} cm^{-3}, the junction depth, X_j, was 1.0 μm, and N_b was 10^{15} cm^{-3}. The relative capacitance interval, $\Delta C/C$, was taken to be 10 percent around zero bias, decreasing to 6 percent at large reverse bias. These ideal data were permuted using random numbers to simulate a measurement error of 0.1 percent (two standard deviations) in both C and V. No systematic error was assumed. These permuted data were then processed to compute dopant profiles on both the lightly-doped (homogeneous) and the heavily-doped (diffused-layer) sides of the *p-n* junction. A composite of these profiles is shown in figure 1. It can be seen that the scatter in the diffused-layer profile significantly exceeds that of the profile on the homogeneous side. Larger and more commonly encountered errors in C would increase the scatter of both profiles but would have a more pronounced effect on the diffused-layer profile. For the conditions considered here the practical range over which one can profile a diffused layer is limited to dopant densities between 6 and 30 times the

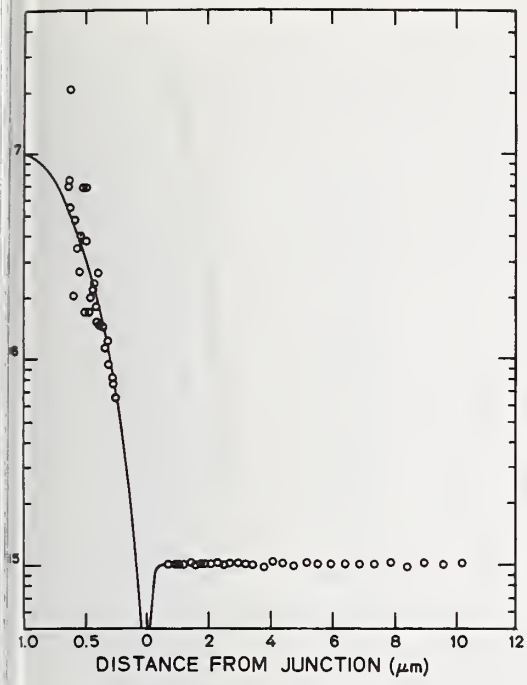

Figure 1. Dopant density profiles on the heavily- and lightly-doped sides of a p-n junction as determined from idealized C-V data modified to simulate a random, normally distributed error with standard deviation of 0.05 percent in the measurement of C and V. (The doping density profile on the heavily-doped side was assumed to be Gaussian with surface doping density of 10^{17} cm^{-3} and junction depth of 1.0 μm as shown by the solid curve to the left of the origin. One point on the heavily-doped side of the junction, 2.28×10^{18} cm^{-3} at 0.6 μm, fell outside the range of the plot. The doping density on the lightly-doped side was taken as 10^{15} cm^{-3}.)

kground dopant density. In this range the measured value of the diffused-layer dopant sity is within a factor of two of the true value.

In addition to errors introduced by measurement error in the capacitance and the rela- e capacitance ratio, which have been considered by Amron [2], the error in the computed fused-layer profile is increased by the interaction of these two effects with the differ- e of large numbers called for in the data reduction algorithm. The net dopant density,), on the heavily-doped side of the junction at the edge of the space-charge region which penetrated a distance A from the junction is [3]

$$N(A)^{-1} = N(W)^{-1} - N(B)^{-1} \qquad (1)$$

re the total space-charge width W = A + B and N(B) is the net dopant density on the htly-doped side of the junction at the edge of the space-charge region which has penetrated istance B from the junction. The quantities derived from capacitance-voltage values are) and W. When N(A) becomes large compared to N(B), as in the case of an abruptly diffused ction, N(B) and B approach N(W) and W, respectively. In the data reduction algorithm,) and B are estimated. As N(B) and B approach N(W) and W, respectively, the calculated ues of N(A) and A become much less reliable.

A theoretical study was also made of the error found in the profile of the lightly- ed side of various diffused junctions when the diffused-layer correction [3] is not ap- ed. Such information is useful in quantifying these errors and in providing guidelines developing diffusion schedules which will minimize the need for these corrections.

The diffused-layer correction accounts for the fact that the space-charge layer pene- tes not only the lightly-doped side of the junction but also the heavily-doped diffused

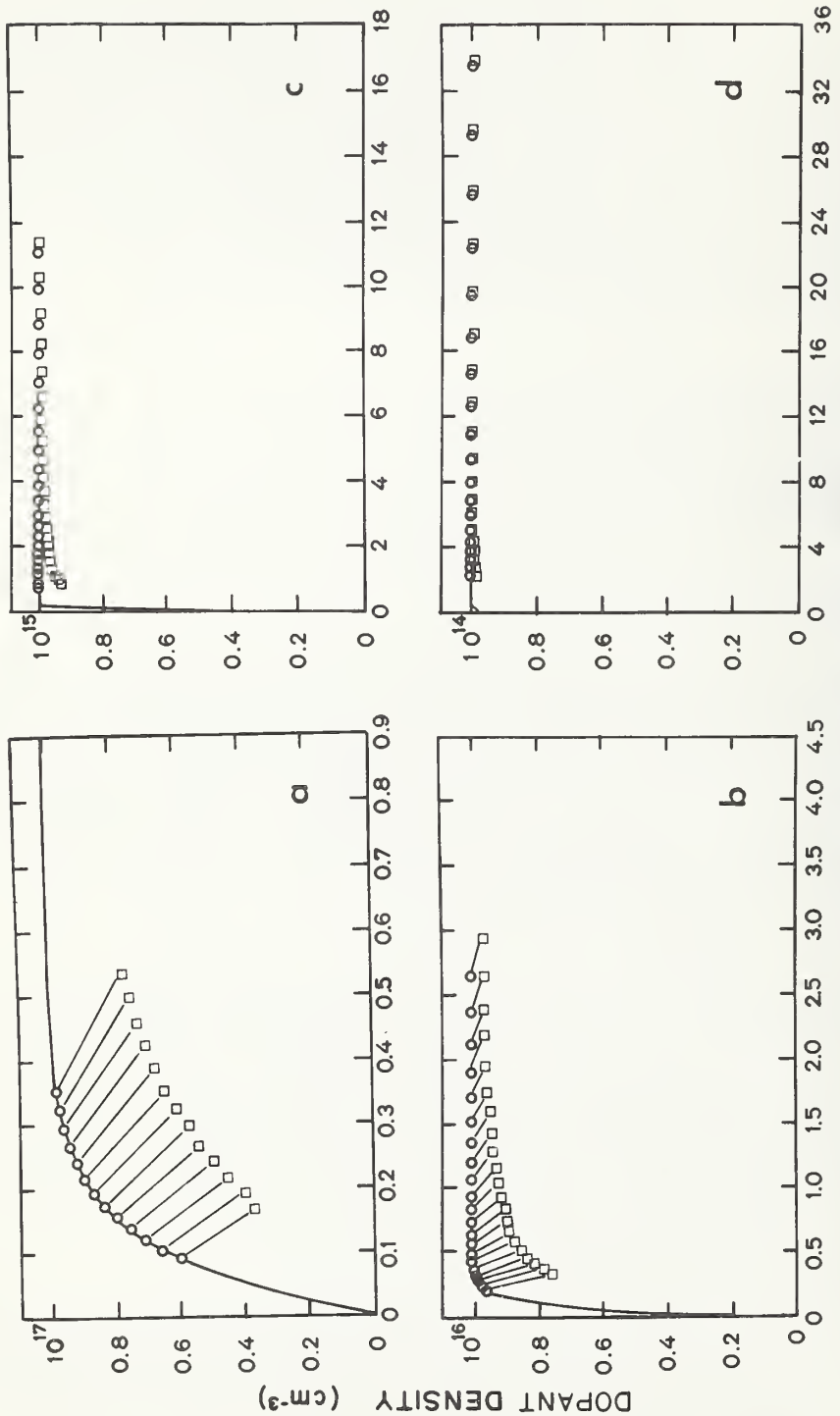

Figure 2. Dopant density profiles on the lightly-doped side of a *p-n* junction as determined from idealized C-V data corrected (O) and not corrected (□) to take account of the penetration of the space charge layer on the heavily-doped side. (The dopant density profile on the heavily-doped side was assumed to be Gaussian with surface dopant density of 10^{19} cm^{-3} and junction depth of 1.0 μm. The dopant density on the lightly doped side was taken as 10^{17} cm^{-3} (a), 10^{16} cm^{-3} (b), 10^{15} cm^{-3} (c), and 10^{14} cm^{-3} (d).)

yer. As above, the junctions were assumed to be formed by a Gaussian diffusion into iformly-doped background material. The junction depth, X_j, was taken as 1.0 μm and the rface dopant density, N_0, was taken as 10^{19} cm^{-3}. Corrected and uncorrected profiles were lculated from idealized C-V data for which the voltage ranged from 0.3 V forward bias to eakdown or 100 V (whichever is smaller) and for which the capacitance was decremented approximately 10 percent for each successive C-V data pair. Profiles calculated for background dopant densities, N_b, of 10^{14}, 10^{15}, 10^{16} and 10^{17} cm^{-3} are shown in figure 2.

The uncorrected profiles, N(W) *vs.* W, are represented by squares, and the corrected ofiles, N(B) *vs.* B, are represented by circles. Connecting lines join data points obined from the same C-V data pair. Note that the uncorrected profiles give erroneously low lues of dopant density which gradually approach the correct N_b value at large distances om the junction. Note also that the uncorrected profiles give erroneously large values r the distance from the junction. This is important when profiling epitaxial layers, for causes the epitaxial-substrate interface to appear farther from the junction than it tually is. Also illustrated is the fact that the errors increase as N_b approaches N_0.

The profiles of figure 2 are valid for both p^+n or n^+p junctions. Peripheral effects ve been neglected and dopant impurities were assumed to be fully ionized. When calculatg the capacitance and voltage, the dielectric constant of silicon was assumed constant th a value 1.036×10^{-12} F/cm and the built-in voltage was taken as 0.7 V. For materials th a different dielectric constant, the respective loci of the N(W) *vs.* W and N(B) *vs.* B rves would be unchanged, but a particular point on a locus would correspond to a different pacitance-voltage pair. (R. L. Mattis and M. G. Buehler)

3. Mathematical Models of Doping Profiles

To couple laboratory efforts on production and measurement of doping profiles in silin, a mathematical study of the diffusion and oxidation processes was begun. The initial ase is directed toward solution of the problem of redistribution of impurities during the idation of silicon considering both uniform and nonuniform initial impurity distributions the silicon.

When a silicon wafer is thermally oxidized, silicon comes from the wafer to form the licon dioxide. This means that during the oxidation, the silicon surface moves with reect to its original position. As oxidation proceeds, dopant atoms in the silicon are in sence either rejected from the oxide or incorporated into the oxide. This effect causes pant atoms to be redistributed within the silicon.

A mathematical description of the physical processes involved in this redistribution oblem has been given elsewhere [4-7]. These authors consider the dopant impurities to be sentially uniformly distributed in the silicon prior to oxidation. It is the purpose of e present study to use numerical methods to solve for the final dopant profiles where itially the dopants are either uniformly or nonuniformly distributed within the silicon.

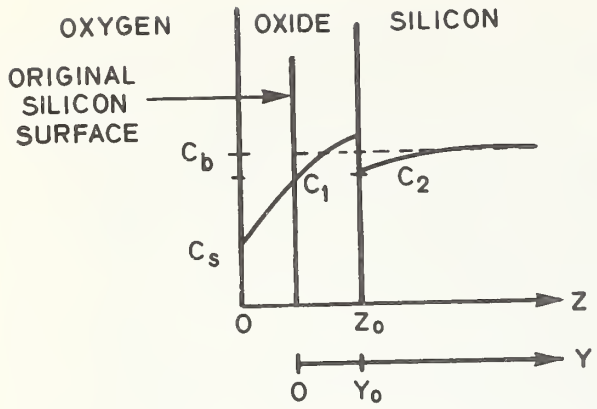

Figure 3. Schematic diagram of dopant distribution in silicon-oxide structure showing both laboratory coordinate, y, and moving coordinate, z.

As in previous work [4-7], the silicon is treated mathematically as a semi-infinite slab with its surface exposed to heated oxygen. As shown in figure 3, the y-axis of the laboratory frame extends into the slab perpendicularly to the surface. In this analysis, the oxide thickness, $z_0(t)$, is assumed to increase parabolically with time according to

$$z_0(t) = At^{1/2} \tag{2}$$

where A is a proportionality constant. The position of the oxide-silicon interface at time t with respect to the initial silicon surface is given by

$$y_0(t) = \alpha z_0(t) \tag{3}$$

where α is some constant fraction.

The kinetics of the oxide-layer growth [6] are such that all the increase in volume undergone by a thin layer of silicon when it is oxidized takes place at the oxide-silicon interface. Away from this growth front the oxide is being uniformly convected to the left with a speed $(1 - \alpha)dz_0(t)/dt$ relative to the laboratory frame. Consequently, there is both diffusive and convective transport of the impurity in the oxide. It is convenient to introduce a moving coordinate system, $z = y + (1 - \alpha)z_0(t)$, in the oxide layer with its origin at the oxide surface. Then the impurity concentration in the oxide, $C_1(z,t)$, obeys, in the moving frame, the simple diffusion equation

$$\partial C_1(z,t)/\partial t = D_1 \partial^2 C_1/\partial z^2 \tag{4}$$

for $0 < z < z_0(t)$. In the silicon there is only diffusion; therefore, in the laboratory frame

$$\partial C_2(y,t)/\partial t = D_2 \partial^2 C_2/\partial y^2 \tag{5}$$

for $y > y_0(t)$ where $C_2(y,t)$ is the impurity concentration in the silicon.

At the oxide-silicon interface, C_1 and C_2 are coupled for $t > 0$ by the equilibrium condition

$$C_2[y_0(t),t] = mC_1[z_0(t),t] \tag{6}$$

ere m is the specified segregation (or distribution) coefficient. Another condition, plicable to the oxide-silicon interface, follows from the conservation of mass:

$$C_2(y_0,t)(\alpha - m^{-1})dz_0/dt = D_1\partial C_1/\partial z\big|_{z=z_0} - D_2\partial C_2/\partial y\big|_{y=y_0}. \quad (7)$$

e boundary condition at the oxide-oxygen interface is assumed to be

$$C_1(0,t) = C_s \quad (8)$$

ere C_s is a specified constant. This assumption is somewhat arbitrary; an alternative ndition which could be assumed at this interface is $\partial C_1/\partial z = 0$ [6].

Equations (4) through (8) and the uniform initial condition, $C_2(y,0) = C_b$, where C_b is constant background concentration, specify the uniform redistribution problem. It has alytic solutions given elsewhere [5,6] for specific cases. This class of problem is ap- icable to MOS devices. Equations (4) through (8) and the nonuniform initial condition for $> y_0$, $C_2(y,0) = C(y)$, where $C(y)$ is a nonuniform dopant concentration, specify the nonuni- rm redistribution problem. This class of problem is applicable to diffused and implanted yers in bipolar silicon devices.

With these formulations of the redistribution problem, it is possible to develop numer- al solutions for a variety of cases including the oxidation of silicon slices both uni- rmly doped and diffused with boron. (S. R. Kraft* and M. G. Buehler)

4. Diffused Layer Sheet Resistance

In the fabrication of semiconductor devices it is common practice to obtain the surface pant density, N_0, of a diffused layer from the measurement of the diffused-layer sheet re- stance, R_s; the junction depth, X_j; the background dopant density, N_b; and an assumed func- onal form for the diffused layer. Irvin [8] has expressed these relations graphically by ing his well-known curves which relate resistivity, and hence carrier mobility, μ, to pant density, N_I, by means of straight-line approximations. Recently, empirical expres- ons [9] have appeared which relate the carrier mobility data of Irvin to dopant density. re recently, Wagner [10] has published a modified hole mobility expression based on his rk on boron-implanted silicon. These expressions have the form

$$\mu = \mu_{min} + (\mu_{max} - \mu_{min})/[1 + N_I/N_{ref})^{\alpha}] \quad (9)$$

ere the constants, μ_{max}, μ_{min}, N_{ref}, and α, are listed in table 1.

The expression for the sheet resistance R_s of a diffused layer with a Gaussian profile

$$R_s^{-1} = q\int_0^{X_j} \mu(N - N_b)dx \quad (10)$$

ere q is the electronic charge, μ is given by eq (9) with $N_I = N + N_b$, $N = N_0 \exp(-x^2/L^2)$,

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* NBS Applied Mathematics Division

Table 1 — Mobility Equation Constants

Type	μ_{max}, $cm^2/V \cdot s$	μ_{min}, $cm^2/V \cdot s$	α	N_{ref}, cm^{-3}	Reference
n	1330	65	0.72	8.5×10^{16}	[9]
p	495	47.7	0.76	6.3×10^{16}	[9]
p	495	47.7	0.76	1.9×10^{17}	[10]

and $L = X_j[\ell n(N_0/N_b)]^{1/2}$. Surface dopant density is plotted as a function of the product of R_s and X_j in figure 4 for a *p*-type layer diffused into uniformly doped *n*-type silicon and in figure 5 for an *n*-type layer diffused into uniformly doped *p*-type silicon. This form of presentation is more convenient for direct use by a process engineer than the form employed by Irvin [8]. Since curves in figure 5 are based on Caughey and Thomas' fit to Irvin's data, the curves are similar to those which appear in Irvin [8], but differences occur for $N_0 > 10^{20}$ cm^{-3} where the expression of Caughey and Thomas fails to fit Irvin's data. The curves in figure 4 are based on Wagner's mobility expression.

The importance of the value of hole mobility assumed in computing the sheet resistance is illustrated in figure 6. For example, there is a difference of a factor of two between values for the surface dopant density for $N_b = 10^{15}$ cm^{-3} and $R_s X_j = 1000$ $\Omega \cdot \mu m$ calculated using the two expressions. As indicated previously (NBS Tech. Note 806, pp. 21-23), the hole mobility at $N_I = 10^{17}$ cm^{-3} is about 240 $cm^2/V \cdot s$ from Caughey and Thomas [9], whereas from Wagner [10] it is about 340 $cm^2/V \cdot s$. Similar differences occur throughout much of the impurity density range of interest. (T. E. Griffin and M. G. Buehler)

3.5. Silicon Resistivity Standards

A simple multipass round-robin experiment has been designed to test both the stability and the multilaboratory precision which can be expected from the silicon resistivity standard reference materials now available from NBS (NBS Tech. Note 806, pp. 8, 66). This experiment is to involve NBS and six other laboratories who have previously collaborated with ASTM Committee F-1 on Electronics in the measurement of bulk silicon resistivity. In the experiment itself each laboratory is expected to measure two sets of standard reference material wafers to be circulated among the laboratories specifically for this test in addition to submitting data taken at specified intervals on the standard silicon wafers which it owns. The experiment is expected to begin soon after the participating laboratories obtain their sets of standards and to run for 12 to 18 months. (J. R. Ehrstein and F. H. Brewer)

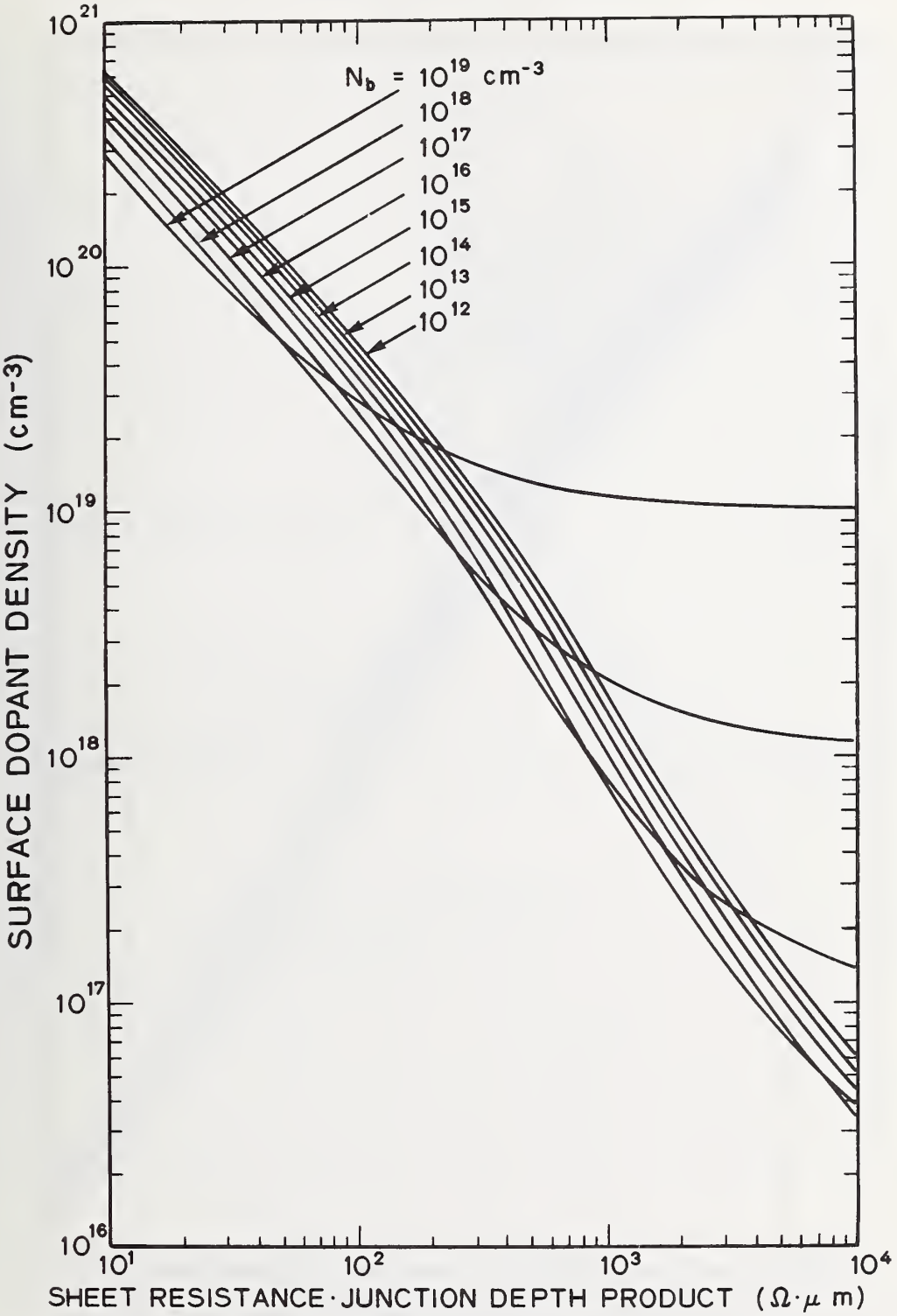


Figure 4. Surface dopant density of a p-type Gaussian diffused layer in uniformly doped n-type silicon as a function of the product of sheet resistance (300 K) and junction depth for various background dopant densities, N_b.

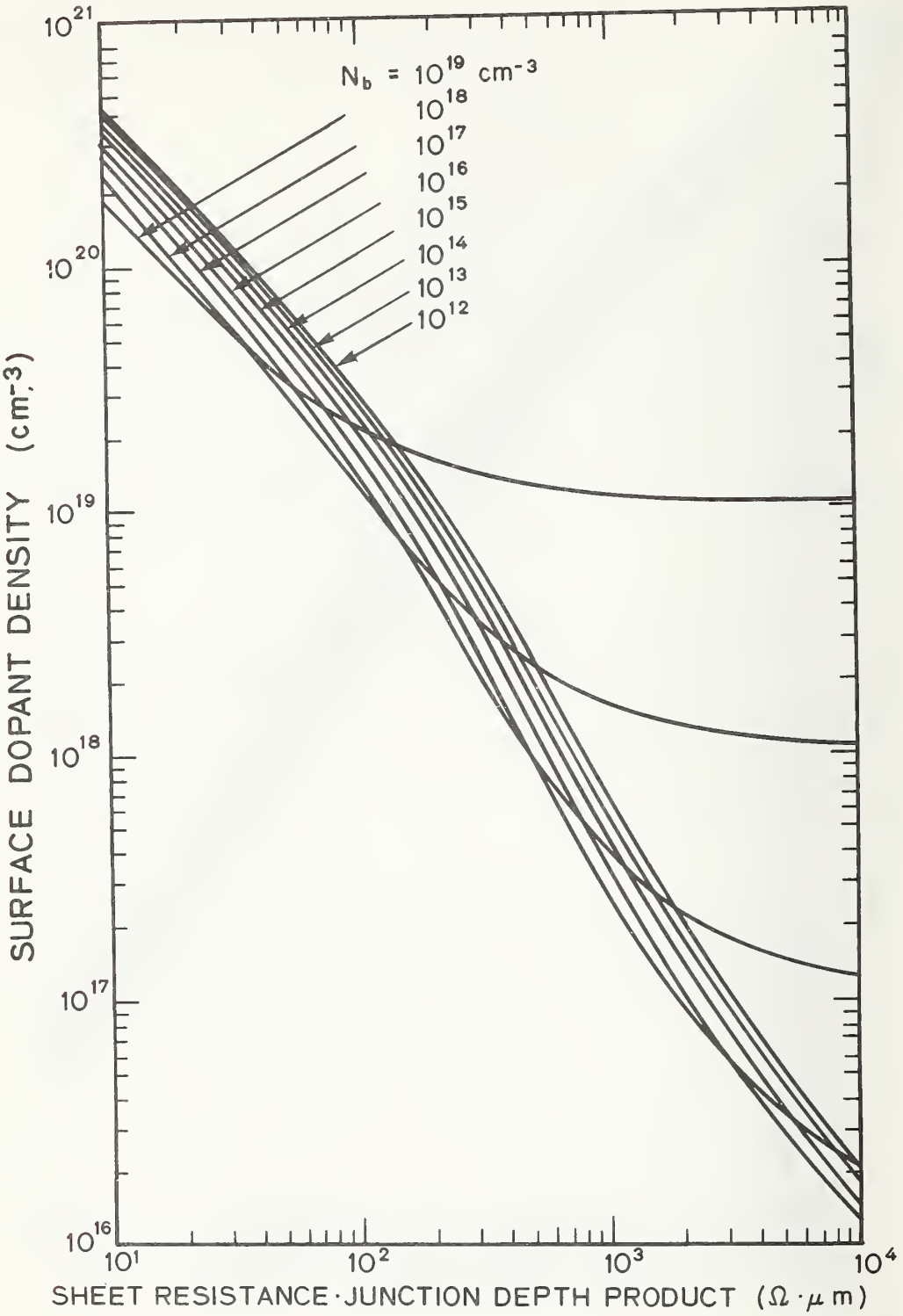


Figure 5. Surface dopant density of an n-type Gaussian diffused layer in uniformly doped p-type silicon as a function of the product of sheet resistance (300 K) and junction depth for various background dopant densities, N_b.

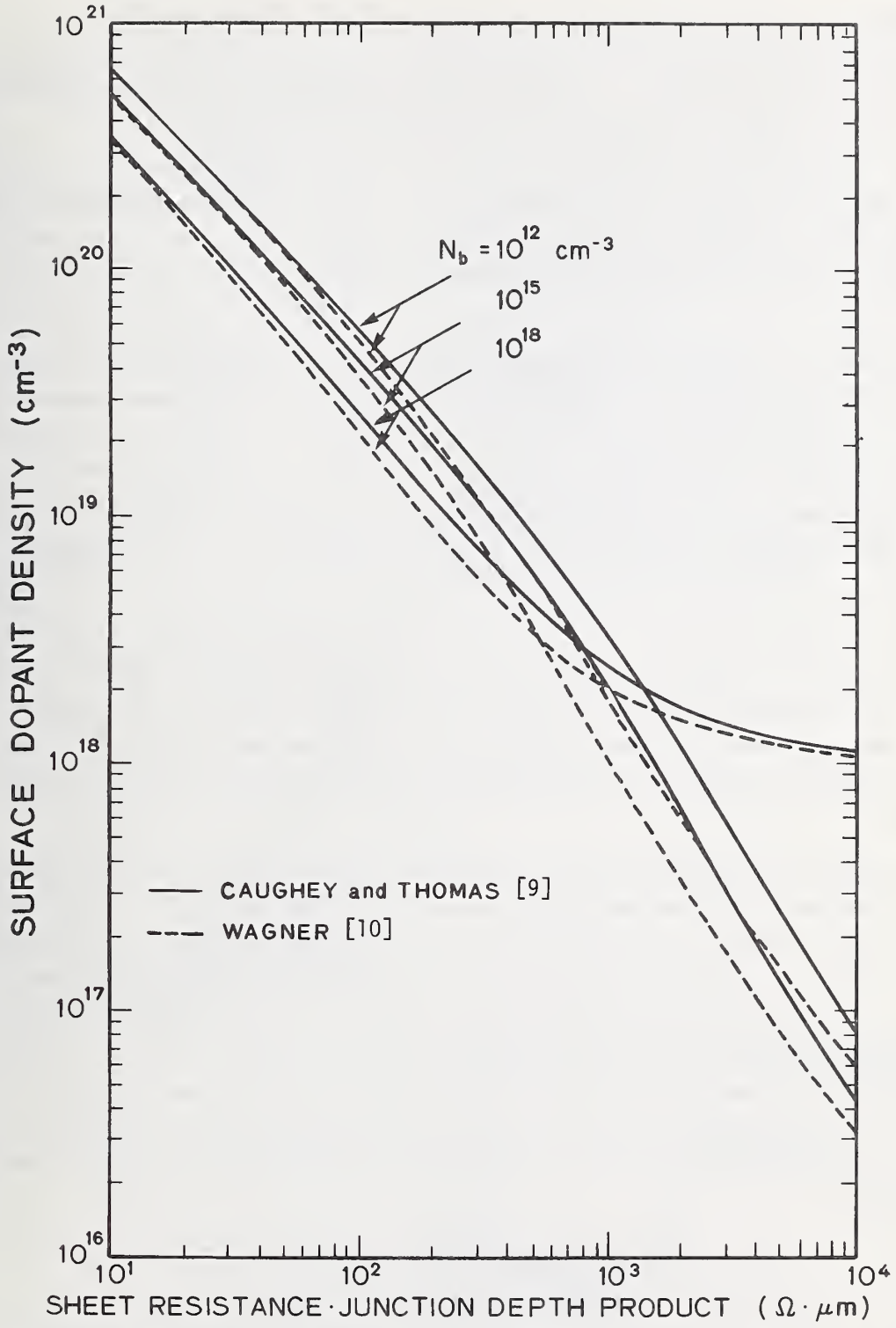


Figure 6. Surface dopant density of a *p*-type Gaussian diffused layer in uniformly doped *n*-type silicon as a function of the product of sheet resistance (300 K) and junction depth for various background dopant densities, N_b, showing the effect of using different relationships between hole mobility and impurity density in the calculation.

4. CRYSTAL DEFECTS AND CONTAMINANTS

4.1. Thermally Stimulated Current and Capacitance Measurements

The dynathermal current and capacitance response of the gold acceptor were measured in a gold-doped n-MOS capacitor. The capacitor was fabricated on the same gold-doped die as the previously studied gold-doped p^+n junction (NBS Tech. Note 806, p. 13). The MOS capacitor had a 20-mil (0.5-mm) diameter gate on a 0.5-μm thick oxide which was thermally grown on a 10-Ω·cm n-type silicon epitaxial layer. The capacitor was mounted on a TO-5 header along with a temperature sensing diode. This configuration and an inexpensive cryostat used for the measurements have been described previously (NBS Tech. Note 806, pp. 13-16).

The dynathermal current and capacitance response of the gold-doped n-MOS capacitor is shown for various heating rates in figure 7. The gold defect centers were charged by increasing the gate bias to V_{g2} = -30 V from a value V_{g1} = -15 V which was applied at room temperature and held on the capacitor as it was cooled to liquid nitrogen temperature. The value of V_{g1} was such that an inversion layer of holes is formed at the oxide-silicon interface. This layer prevents the fast surface states from acting as hole and electron generation centers. An isothermal C-V plot, shown in figure 8, illustrates the gate voltage for which inversion is achieved.

The dynathermal response of figure 7 indicates the presence of two distinct phenomena. The first occurs at about 225 K when electrons are released from the gold acceptor; this is termed the majority carrier, phase I response. The second occurs at about 280 K where holes govern the generation rate of the gold acceptor; this is termed the minority carrier, phase II response.

The heating rate dependence of the current and capacitance response, as illustrated in the figure, indicates that the peak in the current I_I during the majority carrier, phase I response occurs at emission temperatures which shift from 218 to 235 K. This is in good agreement with values obtained for the gold doped p^+n junction reported previously. The peak in the current during the minority carrier, phase II response occurs at emission temperatures which shift from 273 to 292 K depending upon the heating rate. The capacitance step also shifts with heating rate and for the majority carrier, phase I response, the shift is similar to that observed in the p^+n junction. From the capacitance values C_{2Ii} and C_{2If}, the gold density N_t can be found from the expression originally derived for the case of a p^+n junction [11]

$$N_t = \frac{2(V_{g2} - V_{g1})\ C_1^4\ (C_{2If}^2 - C_{2Ii}^2)\ (e_n + e_p)}{q\varepsilon A^2 (C_1^2 - C_{2If}^2)\ (C_1^2 - C_{2Ii}^2)\ e_n} \tag{11}$$

where e_n and e_p are the electron and hole emission rates [12], q is the electronic charge, ε is the dielectric constant of silicon, and A is the area of the MOS capacitor. For this MOS capacitor it was found that $N_t = 2.2 \times 10^{13}$ cm^{-3}. It is interesting to note that when

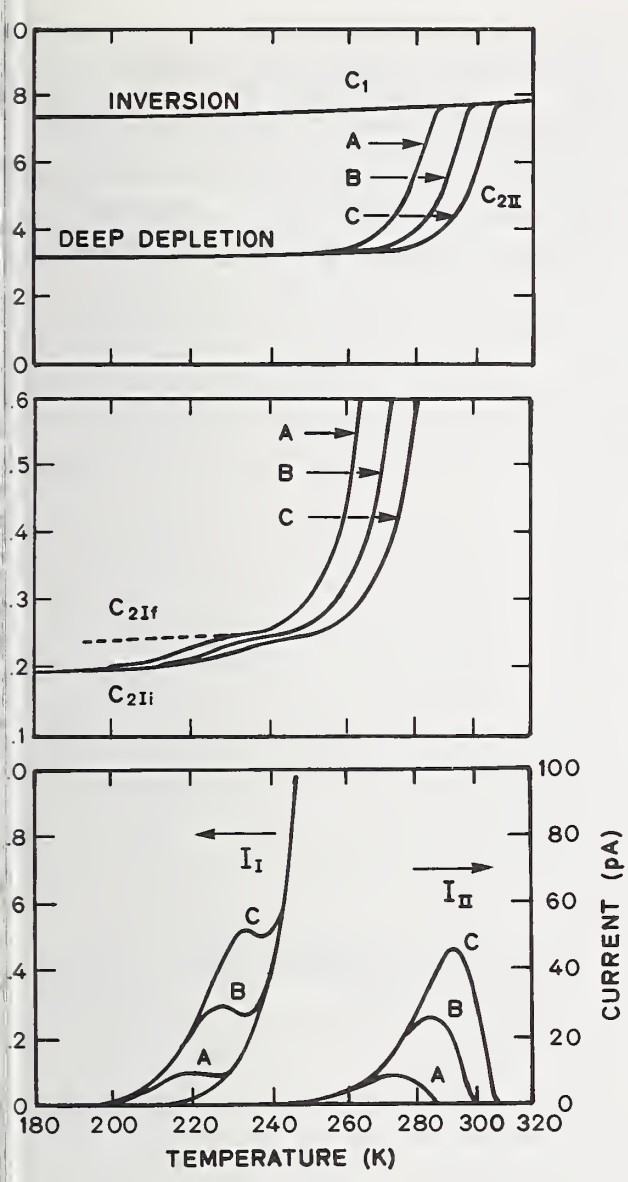
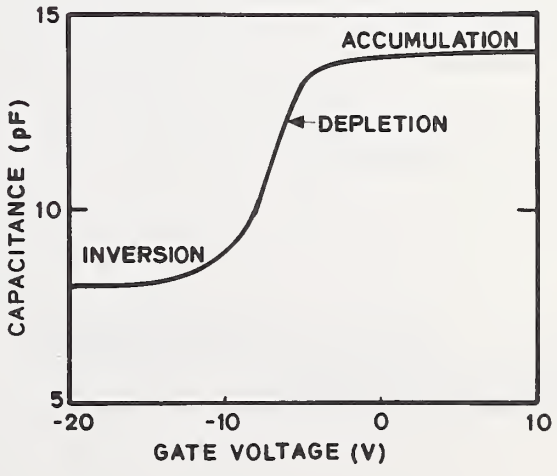


Figure 7. Dynathermal response of a gold-doped silicon n-MOS capacitor showing features due to the gold acceptor. (Heating rate: 1.6 K/s, curves A; 4.8 K/s, curves B; and 9.3 K/s, curves C; Device 2107.7. The left hand current scale refers to the curves labeled I_I and the right hand current scale to the curves labeled I_{II}. The scale of the lower capacitance curves is expanded to show the Phase I capacitance transition which cannot be distinguished on the upper curves. The deep depletion condition, as indicated by the label on the upper capacitance curves, occurs when the potential is changed in a time short compared with the emission time constant at the temperature of the change, in this case ∿77 K. The capacitance curves labeled C_{2Ii}, C_{2If}, and C_{2II} were measured at a gate voltage of V_{g2} = -30 V. The topmost capacitance curve, C_1, was measured at V_{g1} = V_{g2} = -30 V, but would have been the same if measured at V_{g1} = V_{g2} = -15 V.)



gure 8. Isothermal, equilibrium, high-equency capacitance response of a gold-ped silicon n-MOS capacitor measured at om temperature. (Device No. 2107.7.)

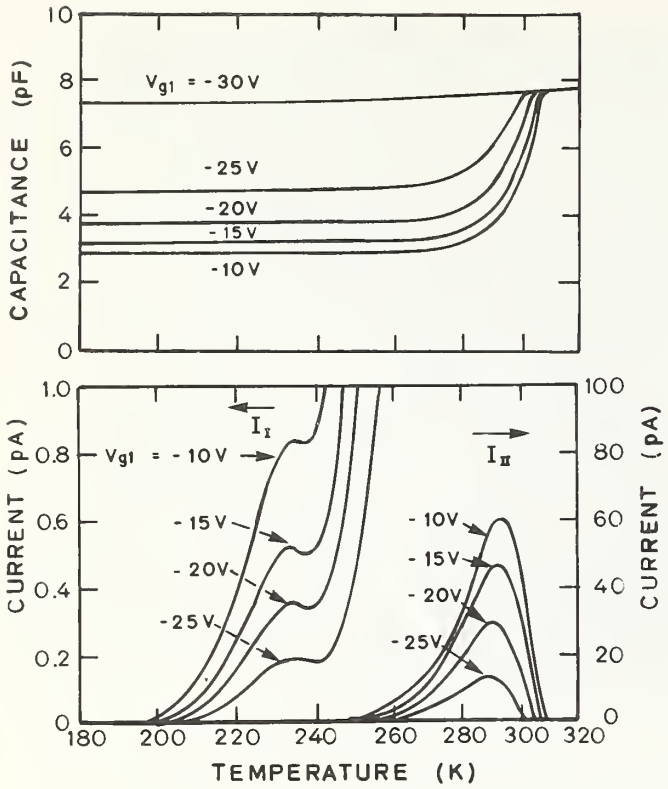


Figure 9. Dynathermal response of a gold-doped silicon n-MOS capacitor showing phase I current and phase II current and capacitance response of the gold acceptor as a function of initial gate voltage, V_{g1}, for a heating rate of 9.3 K/s and final gate voltage of -30 V. (Device No. 2107.7. The curves for V_{g1} = -15 V, correspond to curves C in figure 7.)

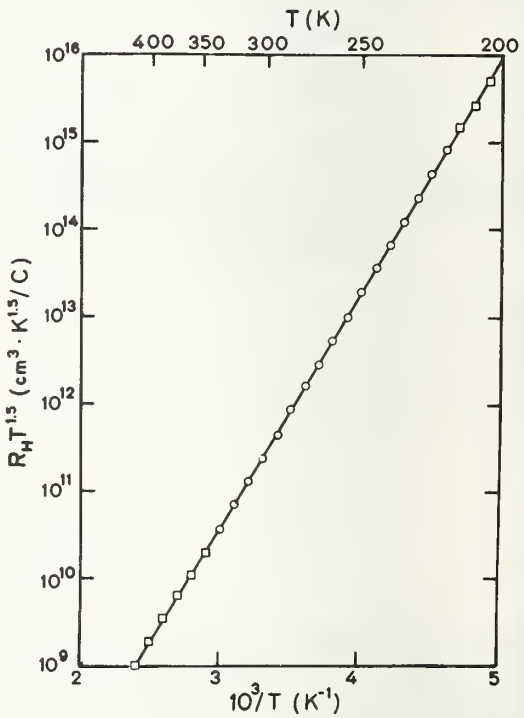


Figure 10. Hall effect activation energy plot for the gold acceptor in n-type silicon. (Specimen 5N950-144.)

he capacitance pulls out of deep depletion and reaches its inversion value, the current hrough the MOS capacitor shuts off.

The bias dependence of the current and capacitance dynathermal response is shown in igure 9 for a heating rate of 9.3 K/s and V_{g2} = -30 V. Since $V_{g1} = V_{g2}$ for the topmost apacitance curve, there is no charging of the space-charge layer. In the figure it is een that the peak in the majority carrier phase I current, I_I, is independent of bias and ccurs at 235 K. The peak in the minority carrier phase II current, I_{II}, is somewhat bias ependent, for this peak depends on the space-charge width which, as seen in the capacitance esponse, is bias dependent. If V_{g1} is more positive than -10 V, hole inversion does not ccur at the oxide-silicon interface and the generation centers there cause excess leakage urrents which greatly distort the current response. (W. E. Phillips and M. G. Buehler)

2. . Energy Level Model for Gold-Doped Silicon

The activation energy of the gold acceptor in silicon was determined from measurements f the Hall coefficient as a function of temperature on a phosphorus-doped specimen with an nitial room temperature resistivity of 5.3 Ω·cm. Gold was evaporated on both sides of the ilicon wafer and diffused at 950°C for 144 h; then both wafer faces were lapped to a depth f 125 μm to remove excess surface gold before ultrasonically cutting a Hall bar for the lectrical measurements. The room temperature resistivity after gold diffusion was .9 × 10^4 Ω·cm. A gold density of 3.3 × 10^{15} cm^{-3} was determined by neutron activation nalysis on a specimen from the same wafer as the Hall bar.

The activation energy of the gold acceptor was computed from the data shown in figure 0 by means of a least squares analysis [13] for the slope. The data points included in the nalysis are shown by circles; the points excluded because of their deviation from linearity re shown as squares. The calculated energy of 0.5381 ± 0.0004 eV represents the value at ero kelvin of the energy difference between the conduction band edge and the gold acceptor evel with the assumption that this difference is a linear function of temperature. The ncertainty in the energy is the square root of the estimated variance of the slope and does ot take into account systematic errors which might be present [14]. The energy difference btained from this specimen is in good agreement with the value of 0.5373 eV measured pre- iously on another specimen (NBS Tech. Note 773, pp. 13-14).

(W. R. Thurber and M. G. Buehler)

5. INSULATOR FILMS

Characterization of silicon dioxide and other insulator films in metal-insulator-semiconductor (MIS) device structures is an essential aspect of obtaining the stable insulator characteristics needed for the reliable operation of MIS integrated circuits. One particularly critical class of problems relates to the radiation sensitivity of thermally grown silicon dioxide in MOS devices.

The observed instability of silicon which is induced by ionizing radiation and is manifested by the build up of positive charge is believed to be due to hole trapping [15]. Optical absorption measurements and electron parametric resonance data indicate that the density of hole traps in silicon dioxide tends to increase with increased sodium concentration. Non-bridging oxygen atoms are known to behave as hole traps and to be enhanced by the presence of alkali impurities [16]. Consequently, the increased density of non-bridging oxygen atoms arising from the presence of sodium contamination seems to be to blame for the observed oxide behavior.

Large concentrations of sodium are located at both the metal and silicon interfaces of dry, thermally grown silicon dioxide [17, 18]. Just how the sodium distribution relates to the radiation sensitivity of an MOS structure needs to be explored. Ion microprobe mass analysis (IMMA) is a highly sensitive technique with which the sodium profile can be examined. There is, however, some concern about perturbing the impurity atom profile during ion sputtering. To assess the nature of this and other problems associated with this application of IMMA, detailed study of this technique is being started in cooperation with the NBS Analytical Chemistry Division. Initially, measurements are being made of several silicon dioxide-silicon structures, one of which was implanted with 80 keV sodium ions to a density 10^{15} cm^{-2}.* This study will employ the ion microprobe mass analyzer at NBS.

Another technique, electron spectroscopy for chemical analysis (ESCA), can lead to a basic understanding of the perturbing effects of sodium on silicon-oxygen bonding and hole trapping. With this technique only a very shallow surface layer is explored. A study of growth characteristics of silicon dioxide in the presence of impurities, such as sodium, is being planned in cooperation with the NBS Physical Chemistry Division.

(D. C. Lewis and A. G. Lieberman)

The vacuum capability of the apparatus to be used for this study has been improved by two orders of magnitude by replacing the elastomer O-rings by machined gold rings. As a consequence, the sensitivity level is now 5 percent of a monolayer or an impurity surface density of about 10^{13} cm^{-2}. Although sodium ion densities 100 times less than this can cause electrically observable effects in MOS devices, it is assumed that data obtained at detectable impurity densities can be extrapolated to situations of lesser density.

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* These specimens consisting of a 0.3-μm thick film of silicon dioxide, grown at 1000°C followed by a 20 min anneal in nitrogen, on a <100> surface of 7 to 13 Ω·cm, *p*-type silicon were supplied by H. L. Hughes of the Naval Research Laboratory.

An Auger electron gun is available which can be added to this ESCA spectrometer to obtain resolutions as small as 0.7 eV, five times better than the resolution of commercially available Auger apparatus. (N. E. Erickson* and J. T. Yates*)

Oxide stability is most often characterized electrically by means of the bias-temperature stress test [19] in which shifts in flat-band voltage of an MOS capacitor are observed after stressing with an applied voltage at some elevated temperature. In preparation for detailed study of this test, a hot-cold stage with appropriate electrical feedthroughs is being designed and constructed. (M. G. Buehler and A. W. Stallings)

A substantial research effort to develop radiation hardened MOS integrated circuits has been supported by various government agencies for the past several years. The results of this work are reported in scattered locations and in a number of different formats. Consequently, it is difficult to obtain a complete picture of the process technologies proposed for producing such circuits and to ascertain their relative merits. At the request of one of the sponsors of the Program, an effort has been initiated to document process technology and test procedures which have been developed under government contract.

(A. G. Lieberman and D. C. Lewis)

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* NBS Physical Chemistry Division

6. TEST PATTERNS

6.1. Process Development

Several modifications were made in the processing procedure as part of a continuing task to demonstrate the application of test patterns in improving and controlling fabrication processes. Run No. 2.3 was made on four 3-Ω·cm, n-type bulk silicon slices and four 10-Ω·cm, n/n^+ epitaxial silicon slices; two slices of each type were doped with gold to a density of about 10^{13} cm^{-3}. The emitter-base junction depth was nominally 0.5 μm and the base-collector junction depth was nominally 1.7 μm. Representative electrical data from both bulk and epitaxial slices without gold doping are summarized in table 2.

Process changes were made to reduce the base and emitter sheet resistance, the metal-to-emitter contact resistance, the back-side contact resistance, and the fixed oxide charge density, each of which was previously higher than the respective target value (NBS Tech. Note 806, pp. 39-41). In most cases, further iterations appear to be required in order to achieve the target values.

It was found that use of a 0.6 percent antimony-doped gold layer evaporated onto the back side of the slice after etching in CP-6 and alloyed for 30 min at 500°C in a nitrogen atmosphere substantially reduced the back-side contact resistance. However, the value achieved on bulk slices remained higher than desired.

Elimination of the staining of the boron-diffused regions prior to phosphorous deposition failed to reduce the metal-to-emitter contact resistance to an acceptable value. The fixed oxide charge density remains at a higher level than desired on most slices. This is due to the poor quality of the deionized water ($\rho \leq 7.5$ MΩ·cm) used in the clean-up and oxidation steps. Improved water treatment is expected to cure this problem.

(R. L. Mattis, M. G. Buehler, T. F. Leedy, and J. Krawczyk)

6.2. Metal-To-Base Contact Resistor Study

As part of a continuing study of the structures on test pattern NBS-2 (NBS Tech. Note 788, pp. 16-17), a series of measurements was made on the metal-to-base contact resistor, structure number 16 on the test pattern. This structure can be understood with the help of the photograph of figure 11 and the schematic cross-section of figure 12. A current, I, is passed through contact pads 1 and 4 and the voltage, V, is measured between contact pads 2 and 3. The substrate is allowed to float electrically during the measurement, and the current is reversed to check for linearity. The current path is indicated in figure 12. The metallization, as seen in the figure, lies on top of the oxide everywhere except in the contact window and in contact pads 1 and 3. Similarly, the p^+ diffused region is under oxide everywhere except for the contact window and the contact pads 1 and 3. The measurement is therefore a Kelvin resistance measurement; the voltage-current ratio (V/I) when multiplied by 6.45 yields the metal-to-base contact resistance in units of microohm·square centimetres for a square contact window 1.00 mil (25.4 μm) on a side.

Table 2 — Measurements on Test Pattern NBS-2; Run No. 2.3

Test Structure[a]	Quantity Measured	Measured Value Bulk	Measured Value Epitaxial	Target Value
14	Base Sheet Resistance, Ω/□	73	87	100±20
15	Emitter Sheet Resistance, Ω/□	1.6	0.2	10±5
16	Metal-to-Base Contact Resistance, ($\mu\Omega \cdot cm^2$)	10.9	11.4	<50
17	Metal-to-Emitter Contact Resistance, ($\mu\Omega \cdot cm^2$)	38.4	43.8	<5
18	Back-side Contact Resistance, Ω	9.0	0.25	<1
12	Fixed Oxide Charge Density, cm^{-2}	5.5×10^{11}	2.5×10^{11}	$(2.5 \pm 0.5) \times 10^{11}$
12	Collector Oxide Thickness, nm	520	500	500±50
12	MOS C-V Collector Doping Density, cm^{-3}	1.7×10^{15}	5.5×10^{14}	—
6	Junction C-V Collector Doping Density, cm^{-3}	1.7×10^{15}	7.5×10^{14}	—
6	Junction Bulk Leakage @ 5 V, nA/cm^2	29	17	<5
—	Base-Collector Junction Depth (μm)	1.71	1.92	

[a] See table 1 and figure 6, NBS Tech. Note 788, pp. 16-17 for identification of test structures.

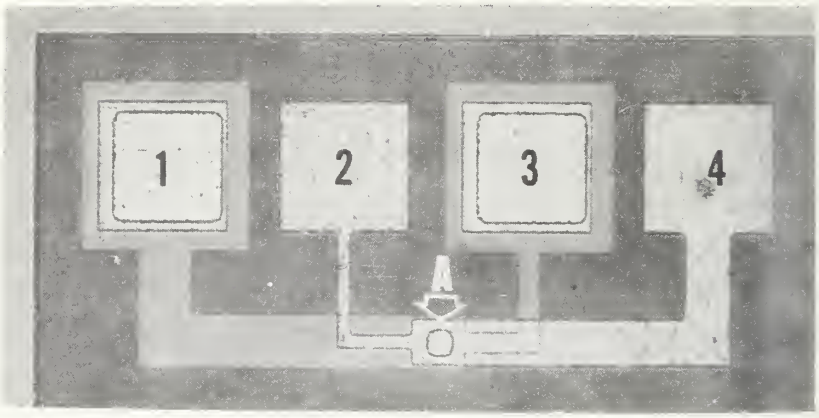

Figure 11. Photomicrograph of the metal-to-base contact resistor, test structure No. 16 of test pattern NBS-2. (The contact window (A) is nominally 1 mil (25 μm) on a side. The center-to-center spacing between adjacent bonding pads (1, 2, 3, 4) is 11 mils (0.28 mm).)

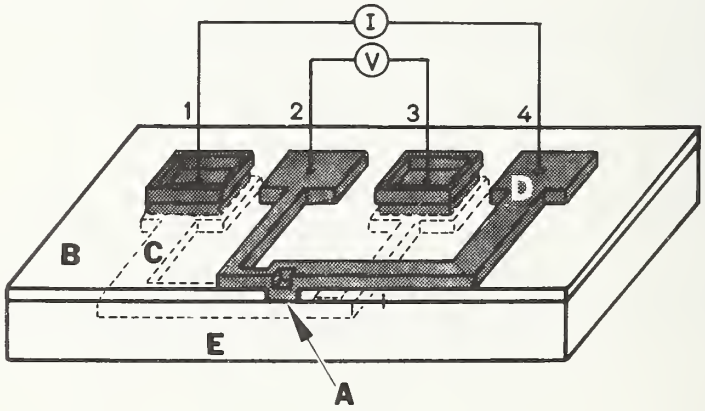

Figure 12. Schematic view of a section through the contact window of the metal-to-base contact resistor test structure pictured in figure 11. (The current path is through pad 4, the metallization stripe (D), the contact window (A), the p^+ diffused layer (C), and contact pad 1. To measure the potential difference, V, contact is made to the metal side of the contact window through the narrow metallization stripe leading to pad 2 and to the diffused-layer side by the narrow diffused region leading to pad 3. The metallization is isolated from the diffused layer and the n-type silicon substrate (E) everywhere except at pads 1 and 3 and the contact window (A) by an oxide layer (B).)

Several experiments were carried out on this test structure. In one experiment, the metal-to-base contact resistance was mapped over a specimen surface in a manner similar to the map of base sheet resistivity reported previously (NBS Tech. Note 806, pp. 41-43). Values of metal-to-base contact resistance were 22.4 ± 2.5 $\mu\Omega\cdot cm^2$ for a base sheet resistance of 182 ± 6 $\Omega/\square$.* This value for contact resistance and the values listed in table 2 are roughly 10 to 20 times larger than ideal values quoted in the literature [20,21] for aluminum on boron-doped silicon. This difference can be attributed, at least in part, to the geometry of the contact structure. Because the current path on either side of the contact is parallel with the plane of the contact interface, only a fraction of the contact area carries a significant current. Hence, the area used to normalize the volt-current ratio to contact resistance is actually substantially less than the window area which was used to obtain the values reported. Because of overetching, the contact windows may be somewhat larger than the nominal size. This also affects the normalization because the actual current carrying area is proportional to the length of the side of the contact area.

In a second experiment it was established that the *n*-type substrate of the test structure must be left floating with no electrical connections in order to confine the return current to the diffused layer.

A third experiment verified the linearity of ΔV as a function of I over the range from 0.1 to 20 mA. This suggests that although it is nonuniform, the current distribution across the contact window area does not change over a considerable range. Consequently, the test structure appears to be suitable as a process monitor which can identify deviations from the nominal contact resistance even though it may not yield absolute values for normalized contact resistance. (F. R. Kelly, R. L. Mattis, and M. G. Buehler)

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* The range of values quoted is for two sample standard deviations on Slice No. 3, Run No. 2.2. The base is a diffused boron layer, nominally 1.7 μm deep.

7. PHOTOLITHOGRAPHY

7.1. Introduction

Failures in the photolithographic processing of semiconductor devices can cause both low production yields and poor device reliability. Most of these failures can be related either to faulty masks or failures of the photoresist to perform as desired. To establish the extent and nature of problems associated with the photolithographic processes, a literature search was initiated, and discussions were held with numerous individuals involved in the use of photolithography in various aspects of the microelectronics industry.

7.2. Mask Inspection

The need for mask inspection methods to detect faulty masks prior to their use in production was determined to be the most critical need. This criticality results from the relatively long time, several days to a few weeks, that is required for the replacement of a faulty mask. Also, because a mask or set of masks is used to produce many successive devices in production, a faulty mask, undetected for only a short time, can produce a relatively large number of defective devices.

For these reasons, the development of methods to inspect and detect faulty masks, prior to their use in production represents a potential cost per part reduction and an increase in yield. Such inspection methods need to include accurate and rapid dimensional measurements to insure the proper alignment and registration of masks used in the successive steps of device manufacture. In addition, these methods need to include a rapid, reliable means of detecting flaws such as pinholes, thereby assuring the use of only high quality masks.

Initial efforts are being directed toward examination of optical and micrometrology problems associated with mask making and mask inspection in the industry with the cooperation of the NBS Optical Physics Division.

7.3. Photoresist Materials

In these discussions it was also determined that measurements of photoresist properties are needed that can be made prior to the use of the resist and interpreted in terms of subsequent resist behavior. The performance and behavior of photoresists are ultimately controlled by the chemistry of the polymers. The most important performance characteristics and their relation to polymer properties are [22-24]:

Adhesion — If the polymer is composed of molecular fractions which are relatively short-chained, solvents, etches, and moisture can more easily permeate the polymer and attack the polymer-wafer surface bonding.

Resolution — Failure of the polymer to form sufficient cross linking can lead to poorly defined edges, low adhesion, and poor resolution through swelling caused by solvent permeation. Poor resolution can also be caused by the presence of large particles of gel or polymeric material. All of

these effects can lower the resistance of the photoresist to acid and moisture attack.

Pinhole propensity — This can be increased by the presence of gel and particulate polymeric material in the resist.

Photosensitivity — Polymer molecules of relatively short chain lengths or failure to have enough photoactive and cross linking sites will cause insufficient cross linking upon exposure and fail to adhere properly. Too many of these sites will cause excessive cross linking and lead to difficulty in completly removing the photoresist.

Wet and dry coating thicknesses — These properties are directly influenced by the viscosity and solids content, both of which are interrelated through the polymer characteristics.

Illumination characteristics also influence the performance of photoresist films. The nteraction of light with the layers and interfaces of composite photoresist-coated wafers an result in light scattering and a subsequent loss in resolution. Light scattered into rotected regions can also result in exposure of the photoresist in undesired regions. Nonniform illumination across the mask-photoresist-wafer composite during exposure can lead to osses in resolution, and over- and under-exposed areas on the same wafer resulting in poor roduction yields.

Initially, the feasibility of using light scattering measurements to monitor the cleaniess, and gel and polymeric particle content of photoresists will be investigated. In ddition, an improved mask is being obtained to facilitate completion of the development and valuation of the test procedure for measuring velocity and acceleration of photoresist pinners (NBS Tech. Note 592, pp. 46-47). (D. B. Novotny)

8. METALLIZATION

The study of tests and test patterns used to determine the adequacy of metal coverage over oxide steps was initiated by studying the literature and discussing the problems associated with quality-of-metallization tests with representatives of the microelectronics industry. One example of the magnitude of the problems associated with improper metallization and metal step coverage is given by Schnable and Keen [25] who reported that 25 percent of the failures observed in a group of bipolar integrated circuits that had undergone operating life tests at rated voltage at 125°C were attributable to open metal interconnections over oxide steps; this was the largest single cause of failure. These tests were reported in 1970; since that time many improvements have been made in metallization processes. For example, tapered oxide steps are now generally used rather than straight steps; properly done, this technique can eliminate thinning of metal over an oxide step [26]. At this time many manufacturers simply inspect metallization of their products on a periodic basis unless otherwise required by a parts buyer.

The different tests described in the literature for evaluating quality of metallization can be divided into three categories:

1. Examination of the metallization on a fabricated device using a scanning electron microscope (SEM).
2. Testing the metallization with a current pulse.
3. Measuring the noise associated with current passing through a metal test stripe.

The problem of metal step coverage has been studied and controlled most often through the use of the SEM [27]. The use of SEM inspection to discriminate between "good" and "bad" metallization has been widely used to design and optimize metallization processes. This technique is well developed and documented. Various standards for SEM inspection have been written; perhaps the most widely referenced is that prepared by Anstead and Adolphsen [28]. Other similar documents are those by Klippenstein and Devaney [29], and Beall [30]. Although the SEM is a useful tool it has several disadvantages which limit its utility in a production environment:

1. The instrument itself is expensive.
2. It requires a highly trained operator.
3. The inspection procedure is slow.
4. The interpretation is subjective.
5. The primary electron beam may damage the active semiconductor regions of the device being inspected.

Despite these drawbacks, it is doubtful that SEM inspection will be supplanted entirely even if other currently envisioned metallization tests are developed. Of the various metallization tests which have been proposed, only SEM inspection gives sufficient information to determine anything other than that the metallization failed.

The current pulse test was developed to circumvent the shortcomings of SEM inspection escribed above. In the pulse test, it is assumed that if metal is thinner, as at an oxide tep, its local resistance is high. Hence, if the stripe is pulsed sufficiently rapidly here is local adiabatic heating at the thinned region which will result in metal burn out f the pulse is long enough and large enough. This is clearly a go/no-go test. The metal an fail this test for a variety of reasons, thinned oxide steps, scratches in the metal, tc.; it is not possible to ascertain why the metal failed from the results of a pulse test.

The current pulse test relies on Joule heating to melt the metallization locally. The eat must be generated adiabatically since the temperature distribution of a metal stripe in teady state is determined principally by parameters of the geometry, oxide, and metal rather han local defects in the metallization.

The utility of the current pulse test is the center of some dispute at this time. The entral unresolved question is how short a current pulse is required to heat a metal defect diabatically. Gurev has reported experiments in which the pulse test was able to discrimiate between 30 and 45 percent metal step coverage [31]; however, in a subsequent series of xperiments he was not able to correlate the results of his tests with the results of SEM nspection [32]. Crosthwait, Ghate, and Smith [33] have reported experiments in which the esults of the current pulse test did not correlate with the results of SEM inspection. In ll these experiments pulse widths of 50 ns or longer were used.

In comparing the results of these experiments with an adiabatic theory, it was found hat the predictions of the theory were not consistent with the experimental results. On he other hand, a simple steady-state model, developed as part of this study, provides a onsistent explanation of the results. This finding suggests that the pulse length used ith the current pulse test must be shortened if the adiabatic approximation is to be valid. o reports of experiments have been found in which pulses shorter than 50 ns were used.

At least four variations of the pulse test have been considered:

1. Nondestructive single pulse — The pulse width and amplitude are adjusted so that acceptable metallization does not burn out; burn out of a test stripe constitutes failure.
2. Resistance change — The pulse width and amplitude are adjusted so that the resistance of a test stripe of acceptable metallization is not affected significantly by the pulse; the resistance is measured before and after the pulse, and a change greater than some specified amount constitutes failure.
3. Destructive single pulse — The pulse width and amplitude are adjusted to burn out even the best metallization; the quality of metallization is determined by the time required for burn out, longer times indicating better quality.

4. Destructive repetitive pulsing — Pulses of constant width are repeated with increasing amplitude until burn out occurs; the quality of metallization is determined by the pulse amplitude required for burn out, higher amplitude indicating better quality.

A difficulty in interpreting the results of the different types of current-pulse experiments is that there are no clear cut experimentally verified relationships between them.

In the current-noise test, current is passed through a metal stripe and the resulting noise is monitored. Experiments with molybdenum and aluminum [26,34] have shown that when the current density is sufficiently large, a metal stripe with defective metallization is much noisier than a stripe with good metallization.

The physical mechanisms which generate the noise are not well understood. To some extent thermal heating of the material may be responsible; however, the marked current dependence of the noise index suggests that other processes, in particular electromigration, may contribute to the noise. It would be desirable if the noise test could measure the propensity of a particular metallization to migrate since metal migration is a common failure mechanism. (D. C. Lewis)

9. WAFER INSPECTION AND TEST

An optical flying-spot scanner is being assembled in preparation for examination of tegrated circuits before and after exposure to the beam of a scanning electron microscope EM). Use of the scanner is expected to assist in evaluation of the susceptibility of in-grated circuits to degradation during SEM inspection and in determination of appropriate erating conditions for use in such inspections.

The scanner is designed to use electromechanically driven mirrors to deflect the beam om a low-powered helium-neon laser in a raster pattern focussed on the integrated circuit be examined. The electrical signal from the integrated circuit which results from the ectron-hole pairs generated by the laser light is displayed on an oscilloscope with a ster sweep in synchronism with the laser raster. A scanner of this type has been described eviously in the literature [35] and has been used to analyze the operation of functioning miconductor devices [35] and to observe process-induced device degradation [36]. However, e present system has considerably improved characteristics including a spot size on the ecimen of 1 μm diameter, a choice of incident wavelength (0.633 or 1.15 μm), a range of ster frame times (10^{-3} to 10^{2} s), and the capability of providing junction currents over e range 10^{-11} to 10^{-4} A. (D. E. Sawyer)

In a continuing search of the technical literature on SEM examination of semiconductor vices, several papers which discuss SEM-induced damage to, or changes in the electrical aracteristics of, devices were collected. (M. J. Wirtz and D. E. Sawyer)

10. DIE ATTACHMENT

10.1. Heat Flow Analysis

The analysis of heat flow to determine the limitations of thermal response techniques for detecting poor die adhesion in mesa diodes bonded to TO-5 headers was completed using the TRUMP thermal analysis computer program [37]. The data given in figure 13 compare the results of the void detection study for mesa diode lots I, J, and L (NBS Tech. Note 717, p. 20) with those of calculations using TRUMP. The structure shown in the insert was used to approximate the true TO-5 header-chip structure. Cylindrical symmetry and circular, centrally located voids were assumed. The shaded area in the model indicates that part of the structure that has a temperature that is above the temperature of the reference point, the outside of the metal shell, for the 10-ms heating power pulse that was used in determining the transient thermal response. The solid curves give the calculated results for the percent increase in steady-state and transient thermal response of devices with a void above that of devices without voids as a function of void area in percent. The data points are the results of measurements performed on the mesa diode chips bonded to the TO-5 headers with various size voids. These points indicate the percent increase in transient thermal response of the devices with a void above the average response of their respective control devices as a function of effective void area in percent. Effective void area was determined by comparing the experimentally determined percent increase in steady-state thermal response of devices with a void above the average response of their respective control devices with the calculated curve. Most of the deviation from the calculated transient response curve is due to the fact that the voids were not all centrally located and that the area around the dimples were not always completely bonded. For example, the triangles represent devices with uncontrolled voids; these devices were analyzed with radiographic techniques and found to have large unbonded regions in addition to the dimpled area.

The approach taken in this analysis differed somewhat from that taken previously (NBS Tech. Note 727, pp. 25-27) where it was assumed that the approximate percent void area was based on the dimple area divided by the available chip bonding area as long as the voided devices were in control. This assumption was made due to the difficulty in accurately predicting the effects of variations in void location, in bonded area around the void, and in thickness of die attachment material itself on the device thermal response. The correspondence of the experimental points with the calculated transient response curve in the figure suggests that the simplified model satisfactorily represents the actual devices under test, so that the system can be calibrated by determining the effective void area from the calculated steady-state thermal response as was done in the present analysis.

10.2 Void Detection in Transistor Die Attachment

Study of the application of thermal response measurements to the detection of voids in transistor die attachment was completed. A second group of three sets of power transistor chips, 60-mils (1.52-mm) square, was bonded onto TO-66 headers with various size dimples ultrasonically machined into the bonding surface to produce, if the bonding were perfect,

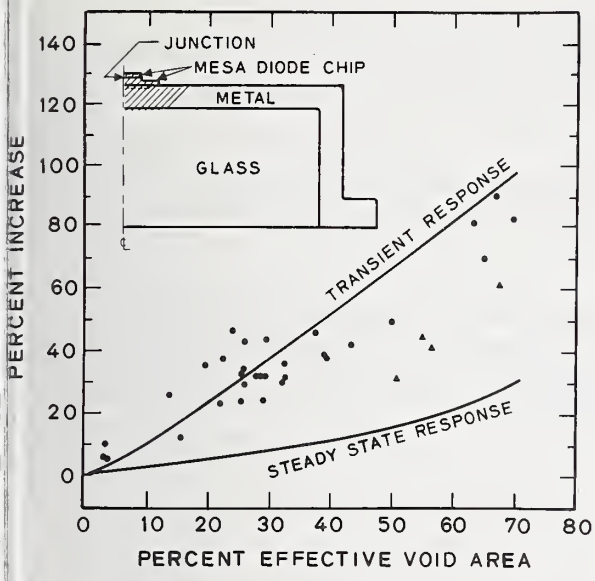


Figure 13. Percent increase in junction-to-case temperature difference of diodes with voids over that of their respective controls measured under steady state and transient conditions as a function of percent effective void area in the diode die attachment. (See text for identification of symbols.)

oid sizes of 15, 25 or 40 percent of the chip bonding surface. Ten control devices with o intentional voids were bonded with each of three sets of devices with various diameter mples.

To determine the pulse width for maximum sensitivity to voids, measurements of steady-tate thermal response and transient thermal response for heating power pulse widths ranging om 1 to 100 ms were made on devices with and without voids. The results indicated that or these transistors a 5-ms heating power pulse gave the maximum sensitivity. Measurements f the change in emitter-base voltage (NBS Tech. Note 743, pp. 23-24) indicated that while ie devices without intentional voids were in control, the devices with various sizes of mples were not. The measured voltage change is proportional to the thermal response if ie temperature coefficient of the emitter-base voltage is assumed to be constant.

The percent relative sample standard deviation for the transient thermal response mea-irement of the controls for the three sets of voided devices ranged from 1.2 to 1.6 percent. or the three sets of devices with voids, the percent relative sample standard deviation nged from 14.8 to 16.9 percent. The percent increase in sensitivity to voids of transient ermal response over the steady-state thermal response measurements ranged from 57 to 9 percent; the grand average was approximately 100 percent. Even in this case where the e attachment is so poor that the increase in sensitivity is less striking, the advantage f the transient thermal response technique over methods requiring heat sinking is neverthe-ss evident.

.3. Summary

This concludes the laboratory phase of the semiconductor device die attachment evalua-ion study. Practical advantages of using the transient thermal response techniques for

screening semiconductor devices for poor die attachment have been demonstrated over the course of this study. It was found that the technique is [38]:

1. Sensitive — It can be used to detect voids as small as 15 percent of the chip bonding area.
2. Convenient — It can be performed on finished devices and requires minimal, if any, heat sinking.
3. Fast — It can be automated.
4. Adaptable — It can be used for testing a wide variety of device types.

(F. F. Oettinger and R. L. Gladhill)

11. INTERCONNECTION BONDING

1. Metallurgical Systems for Ultrasonic Bonding

Characterization of various metallurgical bonding systems of interest for microelectronic devices continued. Last quarter a study was made of one manufacturer's gold wire trasonically bonded to thin film aluminum on silicon oxide substrates. This wire was ind to yield a high bond strength over a very wide range of ultrasonic power (NBS Tech. e 806, pp. 36-38). The result was verified during the present quarter with two more lots gold wire of different manufacture, breaking strengths, and alloy composition.

Tentative results on the ultrasonic bonding characteristics were obtained for gold wire gold thick-film metallization. A satisfactorily wide range of bonding force and ultrasonic power yielded strong bonds with these materials providing the bonding time was increased to about 500 ms or more.

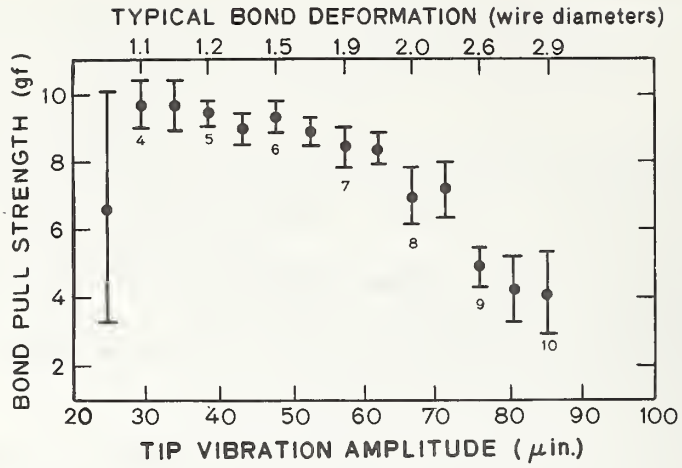
The ultrasonic bonding characteristics of 1-mil (25-μm) diameter aluminum (1% silicon) e to both aluminum thin-film metallization on silicon oxide over silicon and gold thick-m metallization on an alumina ceramic substrate were studied. When bonding silicon dice o hybrid circuits, bonding machine constraints usually require that both the bond to the allization on the die and the bond to the thick-film conductor be made with the same ding force. An extensive bonding machine parameter optimization procedure, involving a ge of bonding force, bonding time, and tool tip vibration amplitude, was carried out for h systems. From figure 14 it is seen that a 25 gf (0.25 N) bonding force, a 45-ms bonding e, and, for example, a 50-μin. (1.3 μm) peak-to-peak tool tip vibration amplitude produced isfactory bonds on both metallizations. Somewhat stronger bonds were obtained on the ck-film gold when a bonding force of 30 gf (0.29 N) was used, but with this force the ds to the thin-film aluminum were significantly weaker. The greater variability in ength of the bonds made to the thick-film gold occurred because of somewhat greater difficulty in controlling the loop height, and, perhaps more importantly, because of the irregular ure of the gold surface as illustrated in the scanning electron micrograph in figure 15.

Studies were also begun using platinum wire on thick-film gold and thin-film aluminum allization. Initial results indicate that platinum wire can be bonded to these metallizations with bonding parameters similar to those of aluminum wire. If these results are confirmed by more complete studies and if no secondary complications occur, it may be that platinum wire should be given further consideration for use in hybrids, since it does not form ermetallic compounds with gold, which can be a major problem with aluminum wire [39].

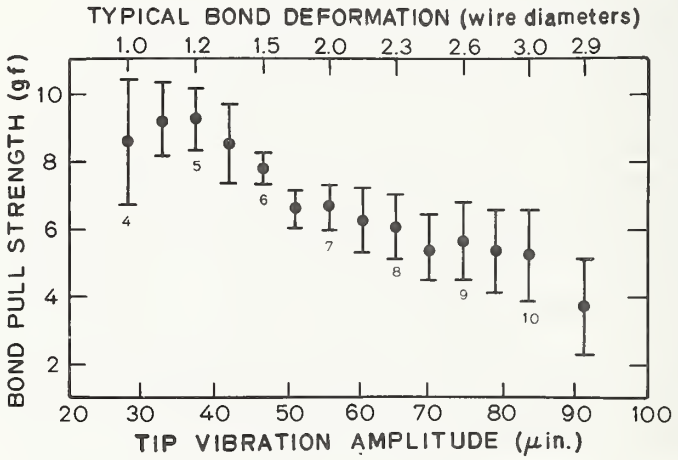
(G. G. Harman and C. A. Main)

2. Burn-out Characteristics of Fine Bonding Wire

The current burn-out properties of round and ribbon aluminum and gold bonding wire were died on 10-mm lengths of wire in air at 23°C. The aluminum wire specimens were obtained m two sources. They contained 1% silicon, 1% magnesium, or $2\frac{1}{2}$% magnesium, or consisted a proprietary alloy. No significant differences in burn out were observed among these oys. The gold wire specimens were of 99.99% purity and were also obtained from two



a) Aluminum wire bonded to thin-film aluminum metallization on silicon dioxide over silicon.



b) Aluminum wire bonded to a 90-percent gold, 10-percent glass binder thick-film metallization on an alumina substrate.

Figure 14. Bond pull strength of ultrasonically bonded, 1-mil (25-μm) diameter aluminum (1% silicon) wire, single-level, double bonds as a function of the peak-to-peak vibration amplitude of the bonding tool tip. (Increasing vibration amplitude corresponds to increasing power; the small numbers below the data points represent settings of the power control on the bonder. The bonding force was 25 gf (0.25 N) and the bonding time was 45 ms. Foot length of the bonding tool used was 4.5 mils (114 μm). The error bars represent one sample standard deviation above and below the mean of 10 to 15 values.)

Figure 15. Scanning electron micrograph of the surface of the thick-film gold metallization used in these ultrasonic bonding experiments. (Magnification: ∿400 X.)

urces. The voltage across the 10-mm length of wire was increased gradually while monitor-
g the current until the wire burned out and ceased conducting.

The burn-out characteristics of the gold wire were as expected. Results are listed in
ble 3 which shows the diameter or cross sectional dimensions, the cross sectional area,
d the current at which the wire burned out.

The aluminum wire, however, burned out in an unusual manner. At one point in the volt-
rrent characteristic, the current decreased abruptly. At this point the wire, which
owed white hot, was far above the melting temperature of aluminum. Although the wire

Table 3 — Burn-Out Current for 10-mm Length of Gold Wire

Cross Sectional Dimensions, in.	(μm)	Cross Sectional Area, in.^{2}	(μm^2)	Burn-Out Current, A
001[a]	(25.)	0.78×10^{-6}	(5.0×10^2)	0.56
001[a]	(25.)	0.78	(5.0)	{0.56 0.56
0015 × 0.0005	(38. × 13)	0.75	(4.8)	0.52
0015 × 0.0005	(38. × 13)	0.75	(4.8)	0.50
.003 × 0.0005	(76. × 13)	1.5	(9.7)	0.89
.003 × 0.001	(76. × 25)	3.0	(19.)	1.34
002[a]	(51.)	3.1	(20.)	1.39
.005 × 0.001	(130. × 25)	5.0	(32.)	2.0
005[a]	(130.)	20.	(130.)	6.1

Diameter

Table 4 — Burn-Out Current for 10-mm Length of Aluminum Wire

Cross Sectional Dimensions, in.	(μm)	Cross Sectional Area, in.^{2}	(μm^2)	Composition	Burn-Out Current,
0.001[a]	(25.)	0.78×10^{-6}	(5.0×10^{-2})	1% Si	0.49
0.001[a]	(25.)	0.78	(5.0)	1% Si	0.39
0.001[a]	(25.)	0.78	(5.0)	1% Si	0.375 0.408
0.001[a]	(25.)	0.78	(5.0)	2.5% Mg	0.35 0.355
0.0015 × 0.0005	(38. × 13)	0.75	(4.8)	1% Si	0.392
0.0015 × 0.0005	(38. × 13)	0.75	(4.8)	1% Si	0.415 0.465
0.0015 × 0.0005	(38. × 13)	0.75	(4.8)	1% Mg	0.375
0.0021 × 0.0004	(53. × 10)	0.84	(5.3)	2.5% Mg	0.37
0.003 × 0.0005	(76. × 13)	1.5	(9.7)	1% Mg	0.565
0.002[a]	(51.)	3.1	(20.)	1% Si	1.15 1.21
0.005 × 0.001	(30. × 20)	5.0	(32.)	1% Si	1.5
0.003[a]	(76.)	9.1	(59.)	b	2.2
0.003[a]	(76.)	9.1	(59.)	1% Si	2.2
0.005[a]	(130.)	20.	(130.)	b	4.75
0.01 × 0.002	(250. × 51)	20.	(130.)	1% Si	4.5
0.01[a]	(250.)	78.	(500.)	b	15.5
0.01[a]	(250.)	78.	(500.)	1% Si	14.7
0.01[a]	(250.)	78.	(500.)	1% Mg	14.6

[a] Diameter

[b] 99% aluminum, impurities unspecified

melted, it apparently developed a thick aluminum oxide sheath that contained and protected the liquid metal. Up to 10 min was required for burn out under these conditions. However, after the melting point had been reached but before burn out, the wire would often open up when the current was switched off or reduced so that the wire temperature dropped below the melting point of aluminum. Consequently the current where the abrupt change occurred was chosen as the practical burn-out current. Data on the various aluminum wires tested are listed in table 4. Figure 16 is a scanning electron micrograph of a section of a 5-mil (1.3 mm) diameter aluminum wire after burn out. The cracked oxide sheath is evident.

(H. K. Kessler)

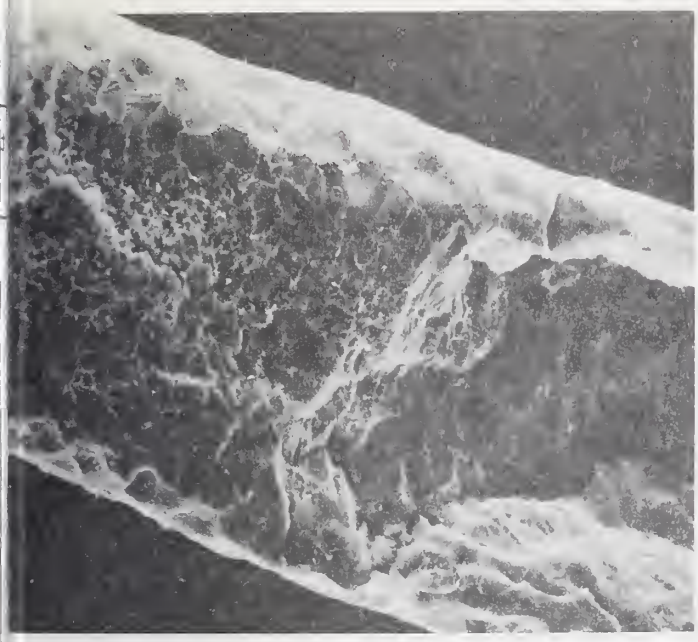


Figure 16. Scanning electron micrograph of a 5-mil (0.13-mm) diameter aluminum wire after burn out on heating to about 1100°C for 3 min showing the oxide surface coating. (Magnification: ∿380 X.)

.3. Dissemination Activities

In addition to the technical activities reported above, dissemination of the methods ıd technology developed for controlling the ultrasonic bonding process and for testing wire ɔnds continued at a high level throughout this period. Visits were made to five industrial ɛganizations, and 23 people visited or called NBS to obtain information in this area. A ımmary report of the work carried out during the past five years was readied for publication ₺0].

(G. G. Harman and H. K. Kessler)

12. HERMETICITY

An assessment of the role of hermeticity and measurements needs was initiated based upon published papers, other agency reports, standards, and direct communications with industrial representatives. The effort to ensure hermeticity represents a significant fraction of device cost, including cost of appropriate package structures, of inspection of package components before assembly, and of fine and gross leak tests after assembly. Further device degradation due to contamination, principally water vapor, from outside the package is a widely recognized failure mode. Yet lack of measurement correlation for the same test method at different stations and for different test methods at the same station, discrepancies in the theory upon which standards for test procedures are based, subjective nature of some preferred test procedures, and scarcity of definitive data linking leak size to device failure were noted.

The theoretical models relating leak size to measured leak rate are in need of revision in several areas. Firstly, while current practice is to compute leak size by laminar (viscous) flow theory for the radioisotope method, and by free molecular flow theory for the helium leak detector method, it should be apparent that such a procedure can produce large differences in computed leak size for any given leak rate. For example, a difference of an order of magnitude or more for a leak in the 10^{-6} atm·cm^3/s range may result for usual conditions of initial pressurization. Transition flow analysis is more appropriate for leak sizes encountered in practice and should provide the basis for both procedures. Secondly, the rate of escape of gas from the package after pressurization needs better definition, particularly for extending the range of these methods to larger leak sizes. Thirdly, at the five and more atmospheres of pressurization often employed, the flow mechanism of helium or krypton tracer gas into the package may differ significantly. Finally, a better understanding of the passage of water vapor through small channels and the correlation to leak sizes determined from leak rates measured with a more ideal gas is needed. Examination of these factors is in progress.

Assistance is being given ASTM Committee F-1 on Electronics in the organization of an interlaboratory evaluation of the helium mass spectrometer method [41] for testing fine capillary leaks in large volume ($\sim$1 cm^3) containers. The experiment is intended particularly to check the Howl and Mann theory [42] for relating measured to actual leak rate.

(S. Ruthberg)

13. THERMAL PROPERTIES OF DEVICES

1. Thermal Resistance Methods

Long-term, single-operator measurements, to check the repeatability of the equipment measuring thermal resistance of transistors by the V_{EB} emitter-only switching technique, e completed. These measurements confirmed the preliminary result reported previously S Tech. Note 806, pp. 51-53) that the repeatability is nearly independent of the magni- e of the measured thermal resistance, but that it is limited by a minimum resolvable ction-to-case temperature difference of a few hundreths degree Celsius.

Twenty-two sets of measurements were made on three single diffused transistors in TO-3 s over a period of three weeks. During the heating, the collector current and voltage e 1 A and 20 V respectively; during calibration, the measuring current was 6 mA and the lector voltage was 2 V. The devices were tested with a case temperature of 60°C and a mea- ing current of 6 mA. The average value and the pooled sample standard deviation of the sured junction-to-case thermal resistance were 0.79 and 0.01°C/W, respectively. (S. Rubin)

Further studies were performed on 12 transistors to compare measurements of thermal istance using the V_{EB} emitter-only switching technique with that of the thermal resistance ived from measurements of peak junction temperature made with the infrared microradiometer. viously such comparisons have been reported for high-current, low-voltage conditions (NBS h. Note 773, pp. 28-29) and high-voltage, low-current conditions (NBS Tech. Note 788, 48-50), both with case temperature of 25°C. In addition, current crowding in three of devices under the high-voltage, low-current conditions was verified (NBS Tech. Note 806, 47-49). In the present study, comparisons were made under high-current, low-voltage ditions at elevated case temperatures. The thermal resistance of each of the devices was sured with a collector-emitter voltage of 20 V and a case temperature sufficient to raise junction temperature to approximately 80 percent of its rated value. The collector cur- t was held at 1 A, except in the case of two low-gain devices for which the collector rent was 0.5 A. The temperature coefficient of the emitter-base junction voltage, V_{EB}, d as the temperature sensitive parameter, was determined first between 25 and 100°C and ond between the multiple of 25°C nearest to the case temperature used during the measure- ts and 175°C, except in the case of two low-gain devices for which the upper limit in the ond determination was 150°C. It was found that the slope of V_{EB} as a function of T_C for onstant collector-emitter voltage can vary slightly for temperatures above 125°C.

The results of the thermal resistance measurements are summarized in table 5, which ts the junction-to-case thermal resistance derived from measurements of V_{EB} using the calibration curves with the thermal resistance derived from the peak junction tempera- e measured with the infrared microradiometer. For the electrical measurements, V_{EB} was sured 50 μs after the heating power was terminated. The difference between the elec- cally measured thermal resistance derived from the low- and high-temperature calibrations that determined from the infrared measurements, expressed as a percentage of the latter, listed in column 3, labeled Δ_ℓ, and column 4, labeled Δ_h, respectively, of table 5. The

maximum difference between the data in columns 3 and 4 is less than 6 percentage points. Th approximation of using the calibration curve for a temperature range between 25 and 100°C also gives a higher, and thus more conservative, value of thermal resistance. The advantage of this calibration procedure is that the temperature controlled heat sink need not be designed for temperatures higher than 100°C. (S. Rubin, D. L. Blackburn, and F. F. Oettinger)

13.2. Analysis

A preliminary study using the TRUMP [37] computer program, undertaken to determine the optimum extrapolation procedure for semiconductor device thermal resistance measurements, indicated that a log-linear extrapolation procedure is appropriate for use on devices that can be approximated by a circular silicon die on an infinite heat sink for the first few hundred microseconds of cooling (NBS Tech. Note 806, pp. 49-51). Further studies were performed taking into account the effects of the change in silicon thermal conductivity with temperature. In addition, a copper slab 0.15 cm thick and the same diameter as the silicon die was added between the silicon and the infinite heat sink which was assumed to be at 0°C. The TRUMP program was again used to calculate the peak surface temperature during the first 200 μs of cooling for heat source areas 100, 42 and 22 percent of the silicon chip surface area. In addition, the average surface temperature of the heat source area, T_{JAVG}, was computed from the TRUMP results as in the previous calculations.

The four extrapolation procedures investigated were log-log, linear-linear, linear-log and log-linear. Again, the last of these, in which the logarithm of the surface temperature is plotted as a linear function of time, yielded the most nearly linear plot; the cooling curves were found to be approximately straight and parallel throughout the interval 20 to 100 μs. The extrapolated values of average temperature, which is usually the quantity determined in electrical measurements of thermal resistance, were 20 and 24 percent lower than the calculated peak temperature at t = 0 for the cases where the heat source area was 42 and 22 percent of the chip surface area, respectively. These values are about the same as found previously for the simpler model. For the case where the entire chip surface comprised the heat source area, the extrapolated value was only 5 percent lower than the computed peak temperature at t = 0. This difference is about half that found for the simpler model.

(F. F. Oettinger and R. L. Gladhill)

13.3. Standardization Activities

To compare the electrically measured thermal resistance with thermal resistance derived from the peak junction temperature, the peak junction temperature of the power transistors used in a preliminary round-robin experiment on thermal resistance measurements was measured with an infrared microradiometer. The results of the round-robin experiment, which was conducted in cooperation with JEDEC Committee JC-25 on Power Transistors, showed that the highest electrically measured thermal resistance is obtained with the V_{EB} emitter-only switching technique (NBS Tech. Note 806, pp. 45-47).

Table 5 — Comparison of Infrared and Electrical Thermal Resistance Measurements

ice lo.	$R_{\theta JC}(IR)$, °C/W	Δ_ℓ, %	Δ_h, %
1	6.5	-19.7	-21.5
3	2.8	-12.1	-15.7
4	3.9	-34.6	-37.9
5	3.9	-15.1	-20.3
6	5.8	-16.7	-17.8
8	8.3	-22.8	-24.3
9	3.6	-8.6	-13.9
0	4.2	-34.5	-36.7
3	4.0	-20.3	-26.0
4	3.7	-12.7	-18.1
5	8.2	-6.3	-8.7
6	7.9	-5.9	-7.8

Table 6 — Comparison of Infrared and Electrical Thermal Resistance Measurements for the Round-Robin Test Devices

Device No.	Case Type	$R_{\theta JC}(IR)$, °C/W	Δ, %
101	TO-3	0.70	-20.0
102	TO-3	0.70	-21.4
103	TO-3	0.78	-21.8
104	TO-3	0.89	-20.2
105	TO-3	1.05	-32.4
106	TO-3	1.61	-23.0
107	TO-3	1.65	-35.8
108	TO-3	1.88	-25.0
109	TO-66	2.03	-14.3
110	TO-66	2.65	-11.7
111	TO-66	2.72	-11.8

The results of the present experiments are presented in the last column of table 6 as e difference between the thermal resistance calculated from the junction temperature de- rmined electrically 50 μs after the termination of power by the V_{EB} emitter-only switching thod and that determined from the infrared measurements, expressed as a percentage of the tter. For reference, thermal resistance, $R_{\theta JC}(IR)$, derived from the infrared measurements also listed in the table. During the power portion of the electrical measurements, the llector-emitter voltage was 20 V and the collector current was 2.0 A, for the devices in -3 cases, or 1.0 A, for the devices in TO-66 cases. For a number of the devices tested, e hottest region on the chip was found to be near the emitter lead. The infrared measure- nt is therefore somewhat uncertain because of possible interference of the emitter lead th the optical path of the infrared microscope. For these measurements this was probably t a serious problem because under the operating conditions used in the study the tempera- re gradients across the active regions of the chip were small so that the hottest region the chip was not well defined. (D. L. Blackburn, S. Rubin, and F. F. Oettinger)

Final revision of the proposed thermal resistance test method for signal diodes was mpleted in preparation for its circulation as JEDEC Semiconductor Committee Letter Ballot -20-73-73. Comments were received on a users guide for making thermal characteristics sts on microelectronics devices, recently letter balloted in JEDEC Committee JC-11 on chanical Standardization, and modifications are being made to incorporate these comments. (F. F. Oettinger)

14. MICROWAVE DIODES

14.1. Repeatability Studies

The mixer conversion loss repeatability studies were continued using a larger number of Schottky-barrier diodes from three manufacturers. These measurements are intended to delineate the measurement system repeatability and to provide a reference level for the diodes to be irradiated for a study of the radiation hardness of Schottky-barrier diodes designed as direct replacements for MIL-type 1N23 series X-band diodes (see 14.2.).

Fifty diodes have been measured to date, ten diodes from each of three manufacturers with a specified overall average noise figure limit of 6.0 dB, and ten diodes from each of two manufacturers with a limit of 6.5 dB. All of the diodes were measured twice for conversion loss, self-bias, local oscillator return loss (SWR), output conductance, and forward current (at a given d-c voltage). The 6.5 dB diodes had previously been measured twice for conversion loss and self-bias only. In addition, photographs were made of the current-voltage characteristics of all diodes, and the junction capacitance was measured at three values of reverse bias for all diodes except those which exhibited a high reverse conductance which reduced the capacitance sensitivity at some bias levels below a usable value at the small signal level required. Some diodes were unsuitable for use in the repeatability studies because they exhibited a high conversion loss (>6 dB)* at the initial or succeeding measurements.

The results of these measurements are summarized in table 7 which lists the mean value and sample standard deviation of the change from the previous measurement. (J. M. Kenney)

14.2. Radiation Hardness Study

At frequencies above several gigahertz, most receivers are now being designed to use Schottky-barrier diodes for mixing. A preliminary study to assess the permanent radiation damage to typical, commercially available, Schottky-barrier diodes on exposure to both fast neutrons (E > 10 keV) and ^{60}Co gamma rays was undertaken in cooperation with the Harry Diamond Laboratories.

The diodes to be studied are of the type designed as direct replacements for MIL type 1N23 series X-band diodes, as have been used in the repeatability studies (see 14.1.). In use, these diodes are mounted in fixed-tuned standard holders [43] which were designed to hold point-contact diodes of the 1N23 type. To facilitate mounting and to select diode polarity, a cap can be attached at either end of the diode.

Diodes for this study were selected from the lots measured in the repeatability study. Only diodes for which the measured conversion loss changed by less than 0.1 dB in repetitive measurements and for which the measured conversion loss never exceeded 6 dB were chosen. A summary of the conversion loss data for the selected diodes is listed in table 8. Diodes were selected in groups of multiples of three from each lot so that equal numbers of diodes

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* The measured conversion loss is approximately 1.5 dB lower than the overall average noise figure.

Table 7 — Change in Conversion Loss on Repetitive Measurements of 1N23-Equivalent Schottky-Barrier Diodes

Lot	Specified Noise Figure Limit, dB	Measurement Repetition	Manufacturer	Mean, dB	Sample Standard Deviation, dB	Number of Measurable Diodes
1	6.0	1	A	-0.058	0.105	9
2	6.0	1	B	0.009	0.032	10
3	6.0	1	C	-0.004	0.027	8
4	6.5	1	A	0.011	0.172	7
4	6.5	2	A	-0.100	0.218	4
4	6.5	3	A	-0.139	0.113	2
5	6.5	1	B	0.001	0.040	9
5	6.5	2	B	0.019	0.051	9
5	6.5	3	B	-0.038	0.030	9

Table 8 — Change in Conversion Loss on Repetitive Measurements of 1N23-Equivalent Schottky-Barrier Diodes Selected for Radiation Hardness Study

Lot	Specified Noise Figure Limit, dB	Measurement Repetition	Manufacturer	Mean, dB	Sample Standard Deviation, dB	Number of Diodes
1	6.0	1	A	-0.002	0.051	6
2	6.0	1	B	0.003	0.029	9
3	6.0	1	C	0.007	0.020	6
4	6.5	1	B	-0.001	0.040	9
4	6.5	2	B	0.019	0.051	9
4	6.5	3	B	-0.038	0.030	9

from each lot could be used for a gamma irradiation group, for a neutron bombardment group, and for an unirradiated control group. An attempt was made to balance the three groups in terms of diode stability, and the assignment of the diodes within the groups was made at random after the groups were formed. It was found that many of the diodes from manufacturer A appeared to be unusually sensitive to mechanical shock, and all but one of the ten 6.5 dB diodes from this source were found not to be acceptable, so that this lot could not be represented.*

In preparation for the irradiation, conversion loss measurements on three of the lots were repeated after removal and reattachment of the cap. Only the "forward" polarity was used, and care was taken to obtain the same cap orientation, in case of asymmetry. The repeatability seemed to be about the same despite this extra factor. The diodes can, therefore, be irradiated without the caps, reducing the size and mass of the irradiated structure and also reducing the possibility of secondary radiation from the diode in the holder, from which only the cap protrudes. (J. M. Kenney and N. J. Berg†)

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* Unfortunately, the first Schottky-barrier diode used in the repeatability studies (NBS Tech. Note 806, pp. 54-55) was from this lot.

† Harry Diamond Laboratories, Washington, D. C. 20438. (Contract S-402391-4.)

15. HIGH-FREQUENCY MEASUREMENTS

Analysis was completed of the results of the interlaboratory comparison of transistor ttering parameter measurements conducted for the Air Force Weapons Laboratory (NBS Tech. es 743, pp. 42-43; 754, p. 35; 773, pp. 34-36; 788, pp. 55-57; and 806, pp. 56-57) [44]. s test was designed to determine the extent of the agreement between transistor measure- ts made in different laboratories by different personnel using the procedure and equip- t normally employed by the participating laboratory. To provide the necessary data each ticipating laboratory measured the S parameters of a set of selected transistors of three es. In addition, each laboratory measured a number of passive devices to provide data the assessment of within-laboratory variability and to assist in identifying the source unacceptably large variability if this proved to be necessary.

S parameters were measured in 100 MHz increments at frequencies from 200 to 2000 MHz. each frequency the four measurements made on the passive devices by each laboratory were raged to obtain a mean for the laboratory, and the within-laboratory sample standard devi- on was calculated as a measure of the dispersion of the data about this mean. The means each of the laboratories were then averaged to obtain the overall mean, and the sample ndard deviation was calculated as a measure of the between-laboratory variability (NBS h. Note 788, p. 56).

The upper frequency limit for measurement of S-parameters on the transistors was 1000 1800 MHz depending on type. Only the between-laboratory variability of the transistor surements was determined, because the transistors were measured only once at each bias frequency. For the magnitudes of the S and h parameters, the sample standard deviation expressed as a percentage of the overall mean to obtain the relative standard deviation coefficient of variation. The sample standard deviation was used as a measure of the iability of the phase measurements.

As an illustration, the variability of the 17 measurements of each of the four S param- rs made on each of the six 2N3960 transistors at a bias current of 2.5 mA by the five ticipating laboratories which used automatic network analyzers is summarized in table 9. maximum, mean, and minimum sample standard deviations obtained in the 102 sets of data each parameter are listed. In addition, the variability of h_{fe} and h_{ie}, calculated from measured S parameters, is indicated. Measurements made by the laboratory which used ual equipment fell within the same range as those made on the automatic systems.

The extreme variability of the s_{11} measurements is due in large part to the variability roduced by the differences in calibration procedures employed by the participants when ng the transistor fixture (NBS Tech. Note 773, p. 35). In addition, the variability of magnitude of s_{21} was excessive because the signal level applied to the transistor base d by one of the participants exceeded the requirements for small-signal conditions.

If these sources of variability are eliminated, for example, by specifying the calibra- n method to be used and by specifying a maximum signal level to the transistor under test, variability of S-parameter measurements could be expected to be considerably reduced.

Table 9 — Variability of Typical S-Parameter Measurements

		All Laboratories		Three Laboratories	
		Magnitude, %	Phase, deg	Magnitude, %	Phase, deg
S_{11}	max	45.9	34.2	7.5	8.2
	mean	12.6	8.8	4.5	1.8
	min	3.5	0.7	0.6	0.1
S_{21}	max	9.9	3.3	5.4	1.7
	mean	2.9	1.1	2.7	0.7
	min	0.9	0.2	0.7	0.1
S_{12}	max	5.2	1.7	6.6	2.2
	mean	2.4	0.9	3.0	0.9
	min	0.9	0.2	0.2	0.1
S_{22}	max	8.9	3.1	4.8	3.5
	mean	4.4	2.0	2.8	2.0
	min	1.6	0.7	0.8	0.5
h_{fe}	max	8.6	5.0	7.0	3.0
	mean	3.4	1.6	2.2	1.1
	min	0.8	0.4	0.2	0.2
h_{ie}	max	23.1	12.0	2.6	3.0
	mean	5.2	3.1	1.0	1.6
	min	1.1	0.5	0.0	0.3

The extent of this reduction is suggested by analyzing the results of the measurements after excluding two laboratories because of apparent calibration anomalies and the 200 MHz data because of the excessive signal level used by one of the remaining laboratories. The last two columns of table 9 contain the results of this analysis.

Examination of data from the other transistor groups and at other biases shows that the results presented in the table are typical of the entire sample used in the interlaboratory comparison. (G. J. Rogers)

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APPENDIX A
SEMICONDUCTOR TECHNOLOGY PROGRAM STAFF

Coordinator: J. C. French*
Secretary: Miss B. S. Hope*
Consultant: C. P. Marsden¶†

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F. R. Kelly×
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APPENDIX B
SEMICONDUCTOR TECHNOLOGY PROGRAM PUBLICATIONS

or Reports

A review of the early work leading to this Program is given in Bullis, W. M., Measure-t methods for the Semiconductor Device Industry — A Review of NBS Activity, NBS Tech. e 511, December, 1969.

Quarterly reports covering the period July 1, 1968, through June 30, 1973, were pub-hed as NBS Technical Notes with the title Methods of Measurement for Semiconductor Mate-ls, Process Control, and Devices. These reports may be obtained from the Superintendent Documents (Catalog Number C.13.46:XXX) where XXX is the appropriate technical note number. rofiche copies are available from the National Technical Information Service (NTIS), ingfield, Virginia 22151.

uarter Ending	NBS Tech. Note	Date Issued	NTIS Accession No.
tember 30, 1968	472	December 1968	AD 681330
ember 31, 1968	475	February 1969	AD 683808
ch 31, 1969	488	July 1969	AD 692232
e 30, 1969	495	September 1969	AD 695820
tember 30, 1969	520	March 1970	AD 702833
ember 31, 1969	527	May 1970	AD 710906
ch 31, 1970	555	September 1970	AD 718534
e 30, 1970	560	November 1970	AD 719976
tember 30, 1970	571	April 1971	AD 723671
ember 31, 1970	592	August 1971	AD 728611
ch 31, 1971	598	October 1971	AD 732553
e 30, 1971	702	November 1971	AD 734427
tember 30, 1971	717	April 1972	AD 740674
ember 31, 1971	727	June 1972	AD 744946
ch 31, 1972	733	September 1972	AD 748640
e 30, 1972	743	December 1972	AD 753642
tember 30, 1972	754	March 1973	AD 757244
ember 31, 1972	773	May 1973	AD 762840
ch 31, 1973	788	August 1973	AD 766918
e 30, 1973	806	November 1973	

rent Publications

As various phases of the work are completed, publications are prepared to summarize the ults or to describe the work in greater detail. Copies of most such publications are ilable and can be obtained on request to the editor or the author.

yer, D. E., Rogers, G. J., and Huntley, L. E., Measurement of Transit Time and Related nsistor Characteristics, Air Force Weapons Laboratory Report AFRL-TR-73-54 (October 1973). ilable from National Technical Information Services, Springfield, Virginia 22151, ession No. AD 914258.

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Forman, R. A., Thurber, W. R., and Aspnes, D. E., The Second Indirect Band Gap in Silicon, to be published in *Solid State Communications*.

APPENDIX C
WORKSHOP AND SYMPOSIUM SCHEDULE

oceedings or Reports of Past Events:

Symposium on Silicon Device Processing, Gaithersburg, Maryland, June 2-3, 1970 — Proceedings: NBS Spec. Publ. 337 (November 1970).

ARPA/NBS Workshop I. Measurement Problems in Integrated Circuit Processing and Assembly, Palo Alto, California, September 7, 1973 — Report: NBS Spec. Publ. 400-3 (February 1974).

lendar of Future Events:

ARPA/NBS Workshop II. Hermeticity, Gaithersburg, Maryland, March 29, 1974. For information, contact H. A. Schafft or S. Ruthberg (301) 921-3625.

Spreading Resistance Symposium, Gaithersburg, Maryland, June 13-14, 1974. (Cosponsored by ASTM Committee F-1 and NBS). For information, contact J. R. Ehrstein (301) 921-3625 or P. H. Langer (215) 439-7131.

ARPA/NBS Workshop III. Test Patterns, Scottsdale, Arizona, September 6, 1974.* For information, contact H. A. Schafft or M. G. Buehler (301) 921-3625.

Tentative date and location.

APPENDIX D
STANDARDS COMMITTEE ACTIVITIES

ASTM Committee F-1 on Electronics

M. G. Buehler, Semiconductor Measurements Subcommittee; Process Controls Section

W. M. Bullis, Editor, Semiconductor Crystals Subcommittee; Secretary, Editorial Subcommittee; Semiconductor Measurements, Semiconductor Processing Materials, Hybrid Microelectronics, and Quality and Hardness Assurance Subcommittees; Insulating Materials Section; Advisory Committee

J. R. Ehrstein, Chairman, Resistivity Section; Semiconductor Crystals, Semiconductor Processing Materials, Semiconductor Measurements, and Hybrid Microelectronics Subcommittees

J. C. French, Chairman, Editorial Subcommittee; Secretary, Advisory Committee; Semiconductor Crystals, Semiconductor Processing Materials, Semiconductor Measurements, Hybrid Microelectronics, and Quality and Hardness Assurance Subcommittees

G. G. Harman, Secretary, Interconnection Bonding Section

B. S. Hope, Committee Assistant Secretary

K. O. Leedy, Chairman, Interconnection Bonding Section

T. F. Leedy, Dielectrics Section

D. C. Lewis, Semiconductor Crystals, Semiconductor Processing Materials, Semiconductor Measurements, Hybrid Microelectronics, and Quality and Hardness Assurance Subcommittees

C. P. Marsden, Committee Secretary; Advisory Committee

R. L. Mattis, Semiconductor Crystals, Semiconductor Measurements, and Editorial Subcommittees

D. B. Novotny, Editor, Semiconductor Processing Materials Subcommittee

W. E. Phillips, Chairman, Lifetime Section; Secretary, Semiconductor Crystals Subcommittee; Semiconductor Processing Materials, Semiconductor Measurements, and Hybrid Microelectronics Subcommittees

S. Ruthberg, Semiconductor Processing Materials, Hybrid Microelectronics, and Quality and Hardness Assurance Subcommittees

A. H. Sher, Semiconductor Crystals, Semiconductor Processing Materials, and Hybrid Microelectronics Subcommittees

W. R. Thurber, Semiconductor Crystals and Semiconductor Measurements Subcommittees

ASTM Committee E-10 on Radioisotopes and Radiation Effects

W. M. Bullis, Subcommittee 7, Radiation Effects on Electronic Materials

J. C. French, Subcommittee 7, Radiation Effects on Electronic Materials

Electronic Industries Association: Solid State Products Division, Joint Electron Device Engineering Council (JEDEC)

J. M. Kenney, Microwave Diode Measurements, Committee JC-21 on UHF and Microwave Diodes

F. F. Oettinger, Chairman, Task Group JC-11.3-1 on Thermal Considerations for Microelectronic Devices, Committee JC-11 on Mechanical Standardization; Technical

Advisor, Thermal Resistance Measurements, Committees JC-22 on Rectifier Diodes and Thyristors, JC-20 on Signal and Regulator Diodes, JC-25 on Power Transistors, and JC-30 on Hybrid Integrated Circuits

S. Rubin, Chairman, Council Task Group on Galvanomagnetic Devices

D. E. Sawyer, Task Group JC-24-5 on Transistor Scattering Parameter Measurement Standards, Committee JC-24 on Low Power Transistors

H. A. Schafft, Technical Advisor, Second Breakdown and Related Specifications, Committee JC-25 on Power Transistors

E Electron Devices Group

J. C. French, Standards Committee

J. M. Kenney, Chairman, Standards Committee Task Force on Microwave Solid-State Devices II (Mixer and Video Detector Diodes)

H. A. Schafft, Chairman, Standards Committee Task Force on Second Breakdown Measurement Standards

E Magnetics Group

S. Rubin, Chairman, Galvanomagnetic Standards Subcommittee

E Parts, Hybrids, and Packaging Group

W. M. Bullis, New Technology Subcommittee, Technical Committee on Hybrid Microelectronics

iety of Automotive Engineers

J. C. French, Subcommittee A-2N on Radiation Hardness and Nuclear Survivability

W. M. Bullis, Planning Subcommittee of Committee H on Electronic Materials and Processes

F. F. Oettinger, Electronic Systems Steering Committee

TC47, Semiconductor Devices and Integrated Circuits

S. Rubin, Technical Expert, Galvanomagnetic Devices; U.S. Specialist for Working Group 5 on Hall Devices and Magnetoresistive Devices

APPENDIX E
SOLID-STATE TECHNOLOGY & FABRICATION SERVICES

Technical services in areas of competence are provided to other NBS activities and oth government agencies as they are requested. Usually these are short-term, specialized services that cannot be obtained through normal commercial channels. Such services provided during the last quarter, which are listed below, indicate the kinds of technology available to the program.

1. Thin Metal Films (J. Krawczyk and T. F. Leedy)

Thin films of a gold-germanium alloy and nickel were evaporated onto gallium arsenide substrates for the Harry Diamond Laboratories.

Thin films of chromium were evaporated onto quartz flats for the NBS Dimensional Technology Section.

2. Ultrasonic Machining (J. Krawczyk and M. Cosman)

Holes were ultrasonically machined into sapphire plates for the Harry Diamond Laboratories.

Holes were ultrasonically machined in thermocouple junctions for the NBS Instrumentation Applications Section.

3. SEM Technical Services (W. J. Keery)

Scanning electron micrographs of marble specimens from the Lincoln Memorial were taken for the NBS Materials and Composites Section.

4. Channel Electron Multipliers and Silicon Nuclear Radiation Detectors (Y. M. Liu)*

Evaluation of channel electron multipliers for the NASA Goddard Space Flight Center continued. The fatigue characteristics (degradation of gain and resolution as a function of radiation exposure) of a wide-mouth multiplier of the type to be used in sounding rocket auroral particle experiments were determined.

A commercial silicon surface barrier detector with keyhole-shaped electrodes on both sides was scanned first with a finely-collimated beam of 1.5-MeV protons to determine edge effects and then uncollimated 14-MeV protons to determine the counting sensitivity of the regions of the device outside the keyhole area.

5. Ribbon Wire Technology (H. K. Kessler)†

Assistance to the Naval Electronics Laboratory Center, San Diego, in the implementation of NBS-developed ribbon wire technology on their pilot production line continued. Pull strength measurements and analysis of data from NBS and NELC results were performed to aid NELC in achieving control of ribbon wire bonding parameters. A five-day visit was also made to NELC to implement control procedures.

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* NBS Cost Center 4254429

† NBS Cost Center 4254448

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16. ABSTRACT (*A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.*)

This quarterly progress report, twenty-first of a series, describes NBS activities directed toward the development of methods of measurement for semiconductor materials, process control, and devices. Principal accomplishments during this reporting period include (1) extension of the technique for measuring thermally stimulated current and capacitance to include measurements on MOS capacitors (2) completion of the development of the thermal response method for evaluation of transistor die attachment, (3) analysis of the interlaboratory comparison of transistor scattering parameter measurements, (4) preliminary review of measurement problems in the photolithographic aspects of semiconductor device processing, of problems associated with certain hermeticity testing procedures, and of methods for evaluating metallization step coverage, and (5) initiation of new activity on characterization of oxide films in MOS structures and analysis of diffusion profiles. Results are also reported on spreading resistance, capacitance-voltage, and sheet resistance measurements; the activation energy of the gold acceptor in silicon; evaluation of the base-to-metal contact resistor test structure; metallurgical systems for ultrasonic bonding; burn-out characteristics of fine gold and aluminum bonding wire; transistor thermal resistance measurements; and microwave diode conversion loss measurements. Supplementary data concerning staff, publications, workshops and symposia, standards committee activities, and technical services are also included as appendices.

17. KEY WORDS (*six to twelve entries; alphabetical order; capitalize only the first letter of the first key word unless a proper name; separated by semicolons*)

Contact resistance; die attachment; dopant profiles; electrical properties; electronics; gold-doped silicon; hermeticity; metallization; methods of measurement; microelectronics; microwave diodes; mobility; MOS devices; oxide films; photomasks; photoresist; resistivity; resistivity standards; scanning electron microscopy; semiconductor devices; semiconductor materials; semiconductor process control; sheet resistance; silicon; S-parameters; spreading resistance; test patterns; thermal resistance; thermally stimulated capacitance; thermally stimulated current; wire bonds.

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