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TRANSISTORIZED BUILDING BLOCKS FOR DATA INSTRUMENTATION

by

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Measurements Automation Section
Information Technology Division

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U. S. DEPARTMENT OF COMMERCE
NATIONAL BUREAU OF STANDARDS

FOREWORD

The volume of data from physical and chemical experimentation being analyzed by means of electronic computers is constantly growing. Reasons for this trend are the production of large volumes of experimental data, the availability of sophisticated computer routines for treating previously obscure details, and the prospect of freeing scarce technical manpower for more creative work. Between the experiment and the computer, however, there is an equipment gap that must be bridged before the full potential of computer analysis of data can be realized by the scientific community.

The equipment problem is complicated by the diverse requirements of scientific laboratories with respect to the types, acquisition rates, measurement precision, display, and ultimate use of the data to be obtained. In addition, not all projects with data handling problems can afford, or efficiently use all of the automatic equipment that could be applied to their particular activities.

The fundamental problem is to achieve a sufficiently high degree of versatility of data handling equipment to permit its use in meeting many different requirements of scientific laboratories. The solution to this problem would permit a large variety of measurement problems to be solved with a minimum investment in equipment, and will tend to minimize the problem of equipment obsolescence.

A promising approach to the accomplishment of this objective is based on a set of compatible electronic modules developed at the National Bureau of Standards. These modules are engineered for flexible interconnection. They operate under the asynchronous control of a supervisory module, equipped with a patch board to govern the control program. Each module contains its own power supply, indicator lights, pluggable printed-circuit logic cards, and standard connectors for control and data signals. This permits the ready assembly of data logging systems tailored to the particular requirements of individual experiments.

This report describes the printed-circuit logic cards.

ACKNOWLEDGEMENTS

The author wishes to express his gratitude to the members of the Measurements Automation Section for their assistance in the preparation of this report, and especially to Don R. Boyle and Alfred L. Koenig for original design work on the new circuits incorporated in this series.

We are also grateful for the many constructive suggestions tendered by other users, both active and potential, in the hope of further improving the utility and applicability of the packages.

ABSTRACT

A fourth family of etched-circuit logic cards has been developed at the National Bureau of Standards. It closely parallels the design criteria and philosophy embodied in previous work, but differs in many respects. Each circuit description is separated physically from the others to facilitate use as an application manual. Specifications, typical uses, graphic symbols, and reliability are discussed in brief.

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National Bureau of Standards

1. INTRODUCTION

National Bureau of Standards Technical Notes 68 and 168 (May 1960 and April 1963, respectively) describe a series of etched-circuit transistor packages for use in construction of small-to-medium sized data acquisition and data processing systems. A related group at NBS has been occupied with design of a series of modules that can be readily assembled into small-scale data acquisition systems. These modules are specifically suited for this purpose, and are therefore not readily applicable to construction of larger machines such as stored-program data processors.

The construction of these modules is different from that described in Notes 68 and 168. Instead of the drawer style used in previous designs, the new devices are built around a card-cage in which 19 printed-circuit logic packages may be mounted, along with a self-contained regulated power supply to provide all necessary operating voltages.

Early modules utilize series 3 packages as described in Note 168, with minor modifications. Late in 1963, it became obvious that use of these cards was very wasteful of space, since they filled only two-thirds of the available volume in a 5-1/4 inch high cage. In addition, experience with series 3 packages indicated that a few logical functions performed by series 3 were superfluous for data-logger design, and that the addition of some others would be advantageous. Care was taken in the physical layout of the cards to insure maximum density of components, and therefore maximum number of circuits per card.

Included in this report is a digest of the new logic symbols approved by the American Standards Association in 1962. These symbols are used throughout this report, which also includes a separate logical diagram and applications information on each of the packages.

2. SPECIFICATIONS

1) All systems constructed from these packages may be operated at a frequency of up to 50kc. Individual cards have higher capabilities. These are noted where applicable.

2) Ambient operating temperatures may be between $0^{o}C$ and $50^{o}C$.

3) Power supply voltages are:

   -12 volts (careful filtering to eliminate high frequency transients in this line is needed).

   + 12 volts.

   These are the nominal values for the voltages. Plus or minus three volt tolerances are permissible in extreme cases, but in any case this voltage, whatever it is, should be reasonably well regulated.

4) Pulse specifications are:

   More positive level: within 1 volt of ground (0 volts).

   More negative level at least -6 volts, at most -12.

   Duration of at least 5 microseconds.

   Rise slope of at least 6 volts per microsecond.

   (Note: Most applications of these packages in data acquisition utilize on dc levels or changes in them, rather than pulses per sec. For this reason, the limit on pulse duration is not a severe restriction.)

Each package is constructed on a plug-in, etched circuit wiring board with a 35 pin hermaphroditic connector integrally mounted, and with test points to accommodate phono-tip probes mounted directly on the card. These test points are connected to the circuit terminals of greatest interest for trouble-shooting.

The basic transistor in use for general purposes is a 2N404. For complementary NPN use, a 2N1302 is satisfactory. For high current applications, a 2N659 is used for very high current, a 2N1039, and for high voltage, a 2N398 are used. The low current, low voltage diodes are type DR435. The high current, high voltage diodes are type 1N2069.

Circuit cards of previous series have required external jumpers or external components to effect most logical functions. A large number of these have been eliminated, some important ones have been retained, and several new ones which promise to be useful have been added.

In general, the circuitry used in the new series is quite similar to that in series 2 and 3. There are enough differences, though, to warrant a complete re-description of the line. In addition, there are several completely new circuits, and extensive modification of a few others.

The series is designated MAD-1 (Measurements Automation Devices).

3. GRAPHIC SYMBOLS FOR LOGIC DIAGRAMS

The module development group has been using logic symbols which conform to the American standard which was approved by the American Standards Association on September 26, 1962. The distinctive shape symbols are used as shown below.

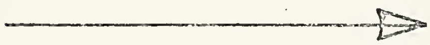
a. Input - Output Symbols

Logic levels are indicated as shown below:


1-state at the more positive potential (current) level.


1-state at the less positive potential (current) level.


1-state indicated by positive potential (current) transition.


1-state indicated by negative potential (current) transition.

Analog inputs are indicated by a plain arrow:

b. Labeling

Card position is indicated inside the symbol.

Pin numbers are indicated outside the symbol and adjacent to respective line.

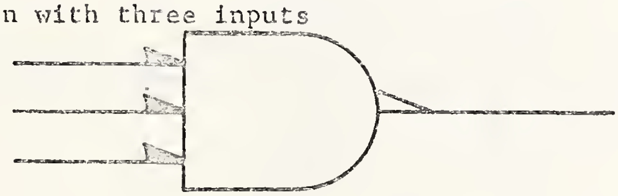
b. Labeling

Card position is indicated inside the symbol.

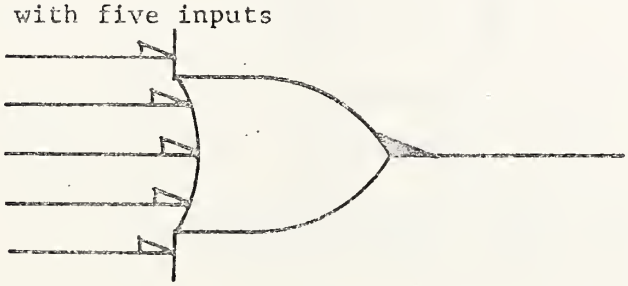
Pin numbers are indicated outside the symbol and adjacent to respective line.

c. AND/OR Inverter

"and" function with three inputs

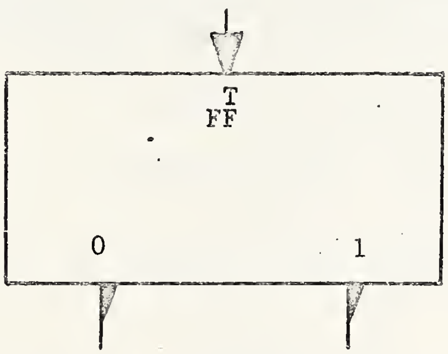


"or" function with five inputs



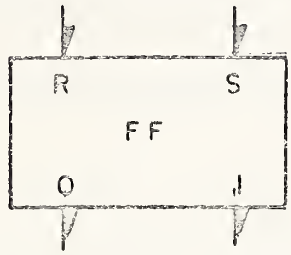
d. Flip-Flop

T input

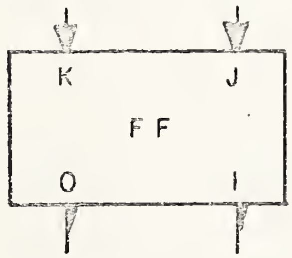


Note: A flip-flop contains a "1" when the 1 output line is in the "1" state.

R-S input (connection directly to transistor base)



J-K input (usually connection to internal pulse gate)

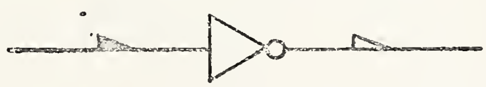


e. One Shot

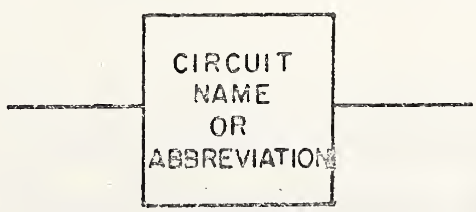
Normal connection

Note: The normal (inactive) state of the ONE-SHOT output is the 0-state. When activated, the output changes to the indicated 1-state, remains there for the characteristic time of the device, and returns to the 0-state.

f. Amplifier (inverting)

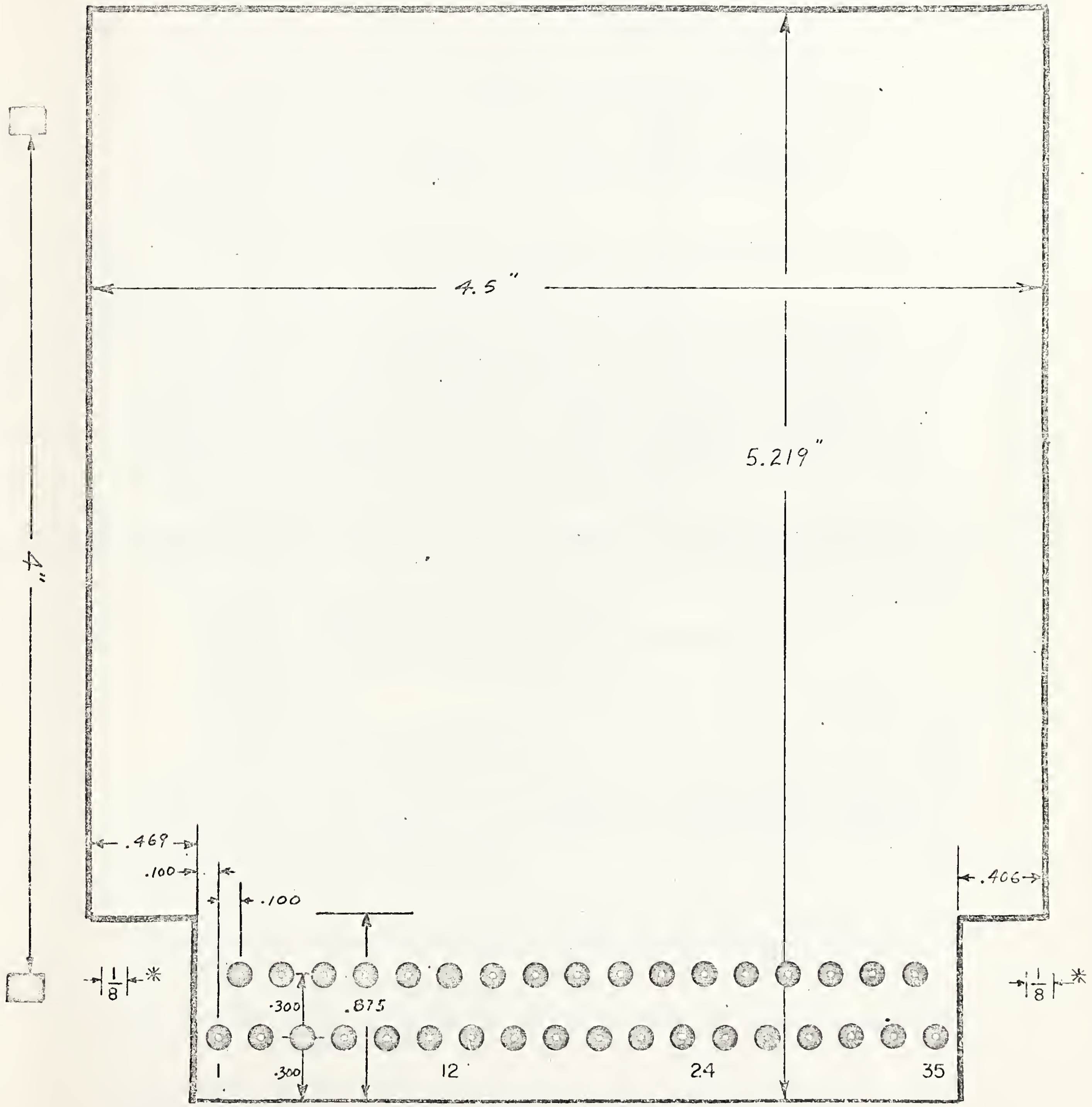


g. Special Purpose-Circuit



MECHANICAL SPECIFICATIONS

Below is a drawing showing the physical dimensions of all cards in series MAD-1b except the ripple/shift and ripple/shift spacer cards. The latter have the same width and connector tongue cutout, but are 10-1/2 inches long. The circles shown are pads for connector mounting, and are uniform for all cards.



* MIN. PERMISSIBLE SPACE FROM EDGE OF CONDUCTOR TO EDGE OF BOARD

Further mechanical specifications are given in the procurement information, which follows.

3. PROCUREMENT SPECIFICATIONS FOR ETCHED-CIRCUIT PACKAGES

S.1 Packages shall be constructed from 1/16th inch copper clad laminate, clad either one side only, or both sides as required, with one ounce of copper per square foot. Completed boards shall be 5-7/32 inches by 4-1/2 inches, except for the ripple register card, which is 10 inches by 4-1/2 inches. All dimensions shall be within plus-or-minus 1/32nd of an inch. Boards shall be made from flame-resistant fiberglass-epoxy type material.

S.2 The etched-circuit conductors should be covered by an electroplate or immersion tin plate before assembly.

S.3 Eyelets shall be installed on all double-clad cards wherever it is necessary to make connections from one side of the board to the other. The eyelets are to be installed and soldered on both sides prior to assembly. Where an eyelet is to be installed without a component, the center hole of the eyelet should not be filled with solder in this process, unless specifically stated in the card description.

S.4 Semiconductors designated in the drawings should be equivalent in all respects to the ones available from the following vendors:

2N404	Texas Instrument or RCA
2N398	RCA (Radio Corporation of America)
2N1302	TI (Texas Instrument)
2N1039	TI
2N659	TI
DR435	General Instrument

It should be noticed that even though many manufacturers produce a given type of transistor with supposedly identical characteristics, in some cases the control of the spread of these characteristics is extremely inadequate.

S.5 All resistors shall be 5 percent tolerance, carbon composition type, and shall be 1/2 watt size except where shown differently on drawings.

S.6 The potentiometer on packages requiring them shall be Bourns Trimet Type 275, or equivalent.

S.7 Capacitors of small values may be of mica, ceramic or mylar if their dimensions are compatible with spacing on the etched-circuit boards-Sprague Series 192P preferred, when possible.

These capacitors shall be within ± 10 percent of the specified values. Capacitors of large values, such as the 2-microfarad capacitor in the one-shot package may be of aluminum or tantalum electrolytic type, or other equivalent type to fit the spacing provided. These capacitors shall be within a tolerance of -15°/o + 100°/o of values specified. All capacitors shall have a minimum working voltage rating of 20 volts d-c.

S.8 Mounting pads (Milton Ross Metal Company "Transipad", or equal) shall be used between the transistors and the etched-circuit board. All other components shall be mounted directly on the board on the side opposite the etched-circuit conductors.

S.9 Both sides of all cards are to be thoroughly cleaned to remove all traces of rosin and foreign material. Ultrasonic cleaning shall <u>not</u> be used for this operation.

S.10 On each card is mounted a male printed circuit connector, supplied by the contractor, Elco No. 00-7022-035-000-001 (no substitutions). At least three of the pins should be staked to the board by splitting and spreading them, but this must not be done in such a manner so as to break the plastic cover of the connector.

S.11 Test jacks indicated are AMP 3-582118-0, 1, 2, etc.

PERFORMANCE

P.1 All transistors and diodes shall be given a simple check prior to installation for the purpose of rejecting open or shorted circuited components. It is only necessary to determine that the transistor exhibits transistor action and that the diodes rectify. Diodes should be checked for compliance with manufacturer's specifications concerning operation with an inverse peak voltage of 20 volts.

P.2 The contractor shall replace without cost to the Government, including transportation, all packages which contain defective components, breaks, or defects in the etched-circuit conductors, or are defective for reasons of poor workmanship.

P.3 The entire order will be rejected by NBS if more than 10 percent of the etched-circuit packages are found to be defective by reason of defective components, breaks or defects in the etched-circuit conductor, or for poor workmanship.

4. SERIES MAD-1B CARDS

Recent advances in semiconductor technology have made possible significant improvements in the performance of series MAD-1 cards. The 2N404, long an industry standby because of its low cost and universal availability, was still undesirable because of poor beta spread and poor high-temperature performance.

The 2N404 is, of course, germanium. The announcement of a silicon PNP transistor with the same characteristics, better beta spread, and same economy prompted a series of experiments. We have tentatively concluded that the 2N3638 transistor will operate as well as the 2N404 in all of our applications. Its higher current-carrying capacity and low $V_{ce\ (sat)}$ make it possible to use it in place of the high cost 2N659 as well. Full acceptance of this device must await large statistical samples. Over 100 packages have been either delivered or ordered, and they are being incorporated into systems as they are received. A separate report on the eventual outcome of these tests will be published after their completion.

Similar tests are also being carried out on the 1N270 gold-bonded germanium diode, which costs half as much as the previously specified DR435, and will also operate at a higher temperature.

Other semiconductor substitutions have been made in the interests of economy, size reduction, or improved characteristics. The changes are summarized in the table below.

MAD-1	MAD-1B
2N404	2N3638 (Fairchild)
DR435	1N270 (Transitron)
2N659	2N3638
2N1302	2N3641 (Fairchild-still under consideration)
2N2926	2N3641 (Fairchild-still under consideration)
1N2069	1N4005 (Motorola)

The above manufacturers cooperated in the development of series MAD-1B, and the statistical studies mentioned above are being carried out with components manufactured by them. As more suppliers become available, they will be incorporated into the testing.

Use of high-temperature components as above has enabled us to rate series MAD-1B as operable at 85° Celsius. The coil driver card has not been changed, and is still rated as 50° C.

5. SERIES MAD-1 LOGIC CARDS

The following sections are self-contained descriptions of each of the cards. They are designed for use either individually or collectively as application, instruction, maintenance and construction manuals. They each follow the format given below.

Logical Function. A brief description of the general uses to which the card is put.

Circuits per Card. Very often, more than one logical unit is contained on one card. This indicates how many there are.

Input Load. Each card is designed to present a uniform load to the circuits preceding it. These loads are specified as follows: one standard logic gate - 3900 ohm sink to ground in parallel with 220 picofarads; one standard pulse gate - .001 microfarads to ground. Cards may present integral multiples of these standard loads to the circuits preceding. This section of the description tells how many and what kind of loads are presented.

Fan-out. Tells how many standard loads may be wired in parallel across the output of each circuit.

Power Requirements. Describes the load on each of the power supplies presented by each circuit.

Logic Diagrams. Shows the logic diagram used for each circuit, in conjunction with the pin numbers for each connection.

Logical Application. A detailed description of the logical functions that can be performed by the card.

Input Signal Requirements. Lists voltage levels, impedances, currents, and rise-and-fall times associated with the card output.

Output Signal Characteristics. Lists voltage levels, impedances, currents, and rise-and -fall times associated with the card output.

Circuit Description. Referring to the schematic diagram, this section details the actual operation of the card.

Trouble Shooting. Some brief hints, plus an insight into the troubles most usually encountered in actual use.

Construction Information. Contains printed circuit artwork, component layout, a parts list, and a photograph.

a. AND/OR Inverter

Logical Function. Each circuit will perform either the NOR function or the NAND function, depending upon the choice of voltage levels to represent logical "1" and "0".

Circuits per Card. Four two-input gates.

Four four-input gates.

Input Load. One standard logic gate.

Fan-Out. Five standard logic gates and four pulse gate loads.

Power Requirements. -12 volts: 20ma for each output at 0 volt; 10ma for each output at -6 volts.

+12 volts: none.

Logic Diagrams. Figures 1 and 2 show the logic diagram and pin numbers.

Logic Application. This is used for virtually all logical gating functions. It will perform either the NOR function or the NAND function, depending upon the choice of voltage levels to represent logical "1" and "0", as shown in the table below.

Function	Input Levels "1"	Input Levels "0"	Output Levels "1"	Output Levels "0"
NAND (Sheffer Stroke)	Pos.	Neg.	Neg.	Pos.
NOR (Pierce)	Neg.	Pos.	Pos.	Neg.

The fact that this circuit can operate in either mode is a consequence of DeMorgan's theorem of Boolean algebra, which states:

$$AB = \overline{(\bar{A} + \bar{B})}$$

Or, in words: and AND function with levels of one polarity is mathematically equivalent to the OR function with levels of the other polarity.

Input Signal Requirements. Positive level: 0 volts to -0.2 volts

Negative level: -6 volts to -12 volts

Imput impedance: 3900 ohms sink to ground shunted by 220 pf.

Output Signal Characteristics.	Positive level:	0 volt to -0.2 volts at approximately 10 ohms (saturated transistor).
	Negative level:	-12 volts at 620 ohms.
	Minimum dv/dt:	6 volts per microsecond (with same rise and fall on input signal).

Circuit Description. The circuit diagram is shown in Figure 3 and is essentially the same as that employed by series 2 and 3 cards. The input diode configuration was chosen to optimize utilization of all components on the card. No provisions were made for increasing the fan-in of these gates, since that function can be duplicated more effectively with a matrix card.

The circuit consists of a simple amplifier preceded by several diodes connected with their anodes in common at the input. If any of the input diodes is energized with -6 volts, that diode will be forward biased and the transistor will be driven into saturation. Consequently, the output terminal will be held to ground via the saturation resistance of the transistor. If all of the input diodes are either open-circuited or held within 0.2 volt of ground, the transistor will be in cut-off and the output terminal will be connected to -12 volts via 620 ohms.

The 220 pf input capacitor serves to speed up the turn-on of the transistor. The 620 ohm base shunt to ground serves to speed up the turn-off by providing a discharge path for the base-emitter diffusion capacitance; and to hold the transistor in cut-off by providing a path for the collector-base leakage current (I_{cbo}).

Trouble Shooting. The following table lists some troubles that may be encountered and suggests probable causes and remedies.

Symptom	Cause	Remedy
Output will not change state	Shorted transistor	Replace
	Open input diode	Replace
Interferes with operation of other cards wired to its input	Shorted input diode	Replace

Construction Information. Figure 4 shows the component layout of the card and the table below lists the required components.

Quantity	Item
8	2N404
24	DR435
10	Test Jacks
16	620ohm Resistors
8	3.9k Resistors
8	220pf (or 200pf) Capacitors.
	Transipads and Circuit Boards.

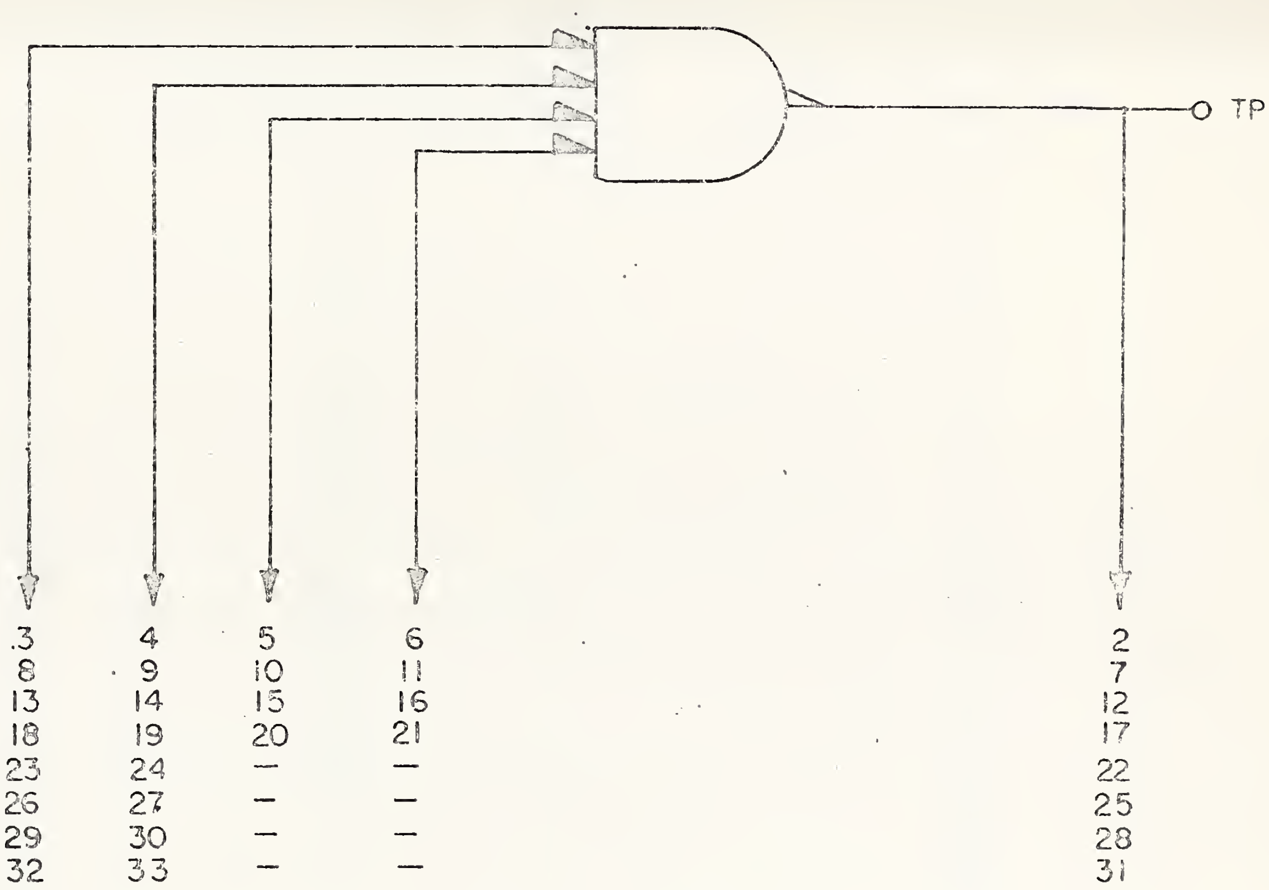


FIGURE 1. AND-OR INVERTER SERIES MAD-1 AS A NAND CIRCUIT

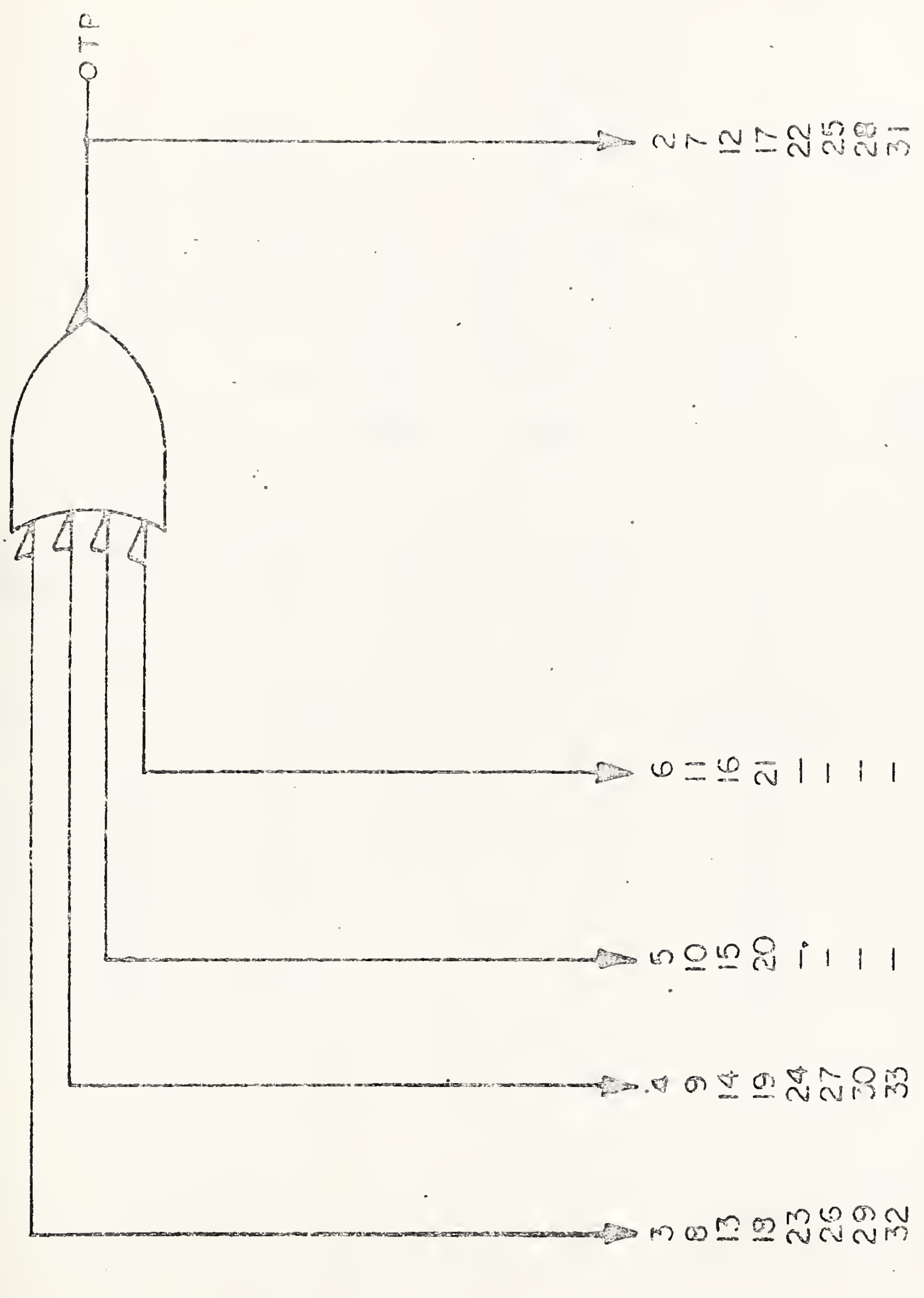
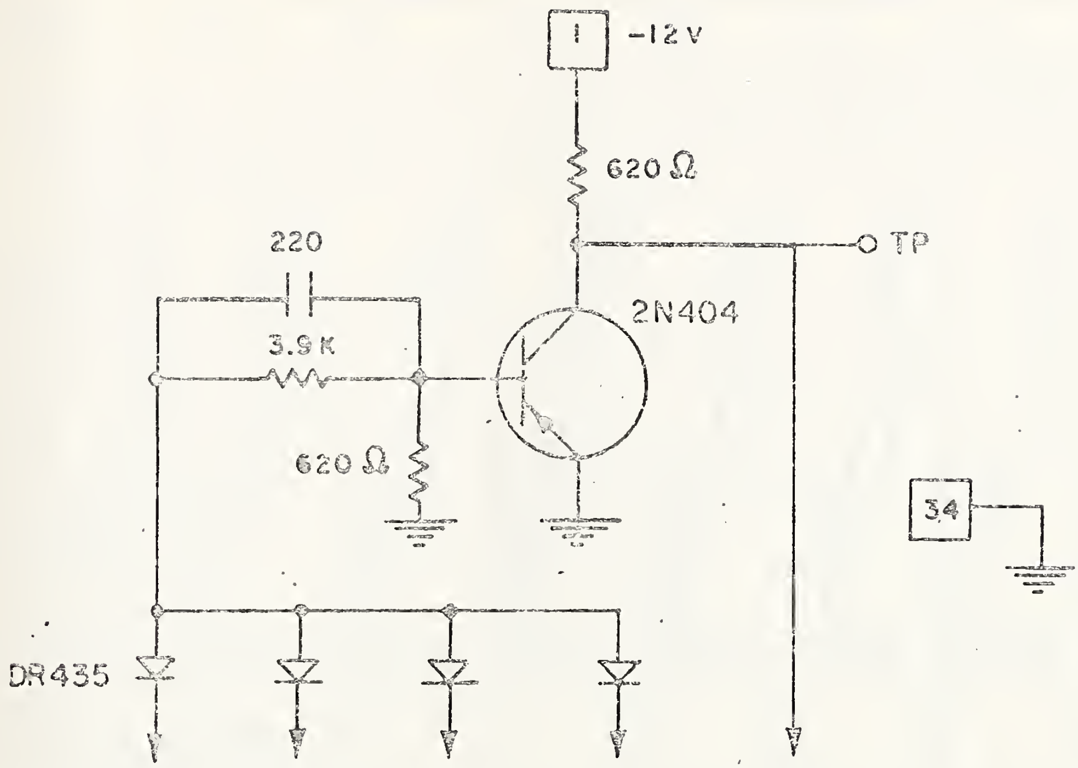
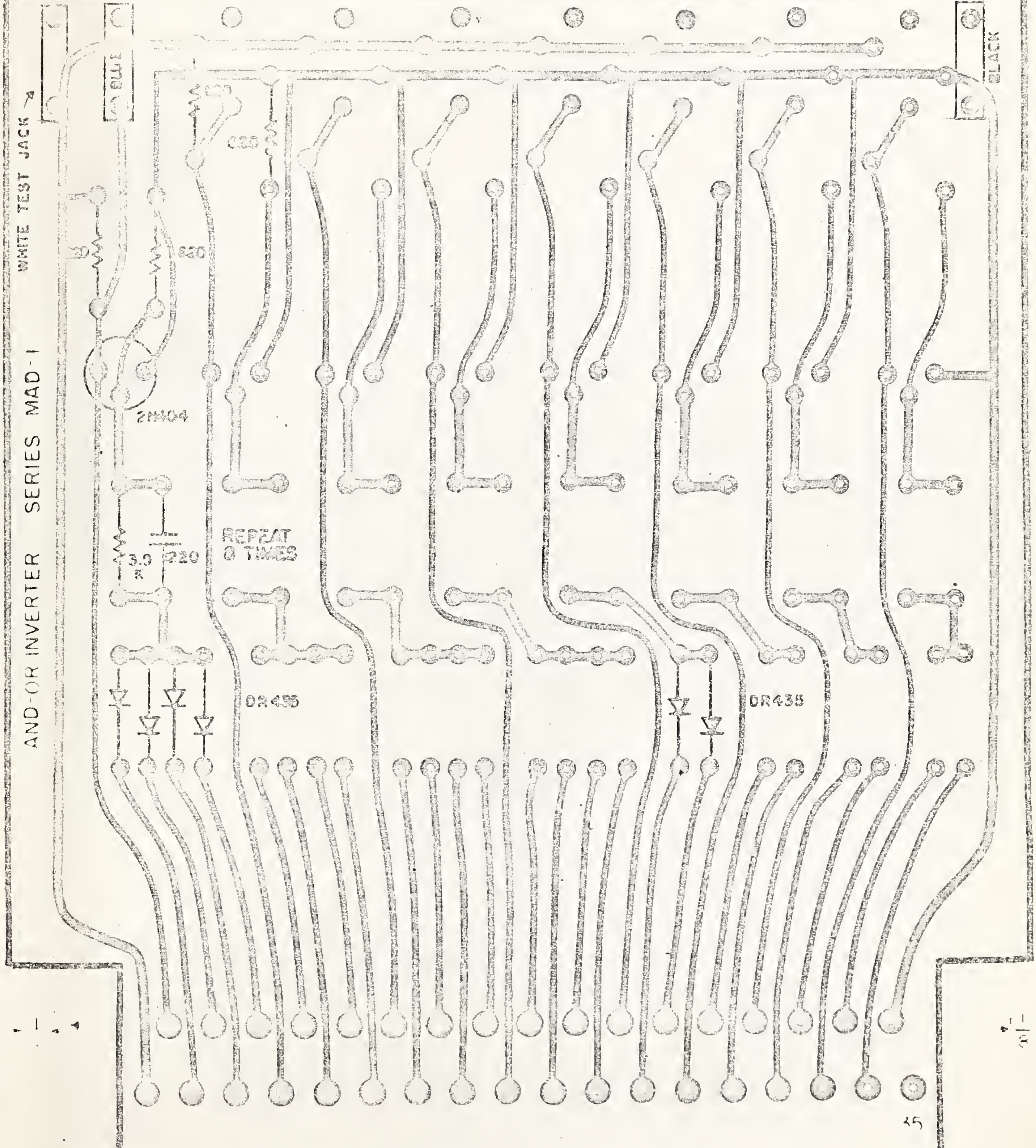


FIGURE 2. AND-OR INVERTER SERIES MAD-I AS A NOR CIRCUIT



CIRCUIT	INPUTS				OUTPUT
1	3	4	5	6	2
2	8	9	10	11	7
3	13	14	15	16	12
4	18	19	20	21	17
5	23	24	–	–	22
6	26	27	–	–	25
7	29	30	–	–	28
8	32	33	–	–	31

FIGURE 3. AND/OR INVERTER SERIES MAD-1



* MIN. PERMISSIBLE SPACE FROM EDGE OF CONDUCTOR TO EDGE OF BOARD

FIGURE 4.

FIGURE 5.

b. Flip-Flop

Logical Function. Each circuit can function as an R-S Flip-Flop, J-K Flip-Flop, T Flip-Flop, or shift register stage.

Circuits per Card. Four

Input Load. One pulse gate.

Fan-Out. Four standard logic gates and four pulse gate loads.

Power Requirements. -12 volts: 92 ma per card.
+12 volts: 2.5 ma per card.

Logic Diagrams. Figures 6 through 9 show the logic diagrams and pin numbers for various configurations.

Logical Application. A flip-flop is a logical binary storage element with two stable states, called 0 and 1. It can have several different types of inputs, the purposes of which are to change it from one state to the other. These configurations are:

J-K: A change from a logical 0 to a logical 1 on the J input will put the flip-flop in the 1 state regardless of its previous state. A change from a logical 0 to a logical 1 on the K input will put the flip-flop in the 0 state, regardless of its previous state. A change from a logical 0 to a logical 1 on both inputs simultaneously will cause the flip-flop to change to whichever state it was not in originally. A change from a logical 1 to a logical 0 on either input will have no effect.

T: A change from a logical 0 to a logical 1 on the T input changes the state of the flip-flop. A change in the other direction has no effect.

R-S: The R-S connection is not normally used without attaching external pulse gates as described below. Not doing so results in a direct connection to the base of the transistors, and may result in damage to them.

Gated: The input gate to the set and reset functions of the flip-flop has two inputs. One of these is sensitive to a logic level, the other only to a positive-going change in level. They perform a delayed AND function no, as follows: If the level input is at logical 0, nothing happens. If the level input is at logical 1, and the "change of level" input experiences a change from logical 0 to logical 1, the gate produces an output no, which will

change the state of the flip-flop if it is not already in the state being energized. A special feature of this gate is that it is not necessary for the "level" input to hold its value while the pulsed input is changing, but rather the gate responds to the value of the "level" input about 5 microseconds before the gate was pulsed. Additional gates (up to 5) may be paralleled at the Base inputs to the flip-flop. These gates are not on the flip-flop card, but are available on the <u>pulse gate</u> card.

When the circuit is in the state called 0, the 0 output line will have a logical "1", and the 1 output line will have a logical "0". When the circuit is in the state called 1, the 0 output line will have a logical "0" and the 1 output line will have a logical "1".

<u>Input Signal Requirements.</u> Positive level: 0 volts to -0.2 volts.

Negative level: -6 volts to -12 volts.

Input impedance: 0.001 uf to ground

Minimum dv/dt: 6 volts per usec., positive slope to trigger.

<u>Output Signal Characteristics.</u> Positive level: 0 volt to -0.2 volts (saturated transistor to ground).

Negative level: -12 volts through 620 ohms.

Minimum dv/dt: 6 volts per usec., (with proper input signal).

<u>Circuit Description.</u> The circuit diagram is given in Figure 10.

Consider the flip-flop itself. Assume that Q_1 is in the cutoff state. The voltage drop across its collector resistor will be small, since no current is flowing through Q_1. For this reason, the voltage at the collector of Q_1 will be very near -12 volts.

On the base of Q_2, there is a voltage divider from the collector of Q_1, through the 3.9k resistor to the base of Q_2, and then through the 33k resistor to +12 volts. If the collector of Q_1 is at -6 volts (or more negative), the base of Q_2 will be carried far enough negative to saturate Q_2. Since the current in a saturated transistor is limited only by the collector load resistor, most of the voltage drop will appear across the load resistor of Q_2, and Q_2's collector will be only a few-tenths of a volt below ground. This, in turn, makes it possible for the 33k resistor connected to the base of Q_1 from the positive bias

supply to hold Q_1 in the cutoff state, where it was assumed to be. The circuit is therefore in a stable state. Symmetry considerations make it obvious that a state with Q_1 "on" and Q_2 "off" is similarly stable. In order to effect a transition from one stable state to another, it is only necessary to drive the "on" transistor into cut-off by applying a positive pulse to its base. This immediately turns the transistor "off", and the positive pulse may be removed, leaving the circuit stable again. The means of forming this pulse and gating it will be discussed.

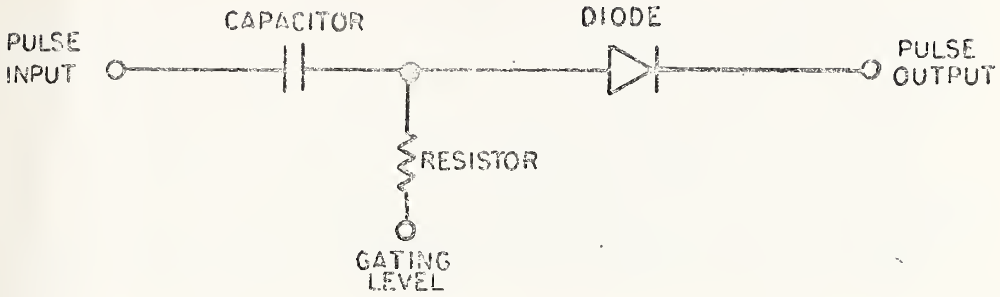
A transistor in the cutoff state has the base-emitter junction reverse biased. The charge carriers have set up an interface across the junction, and the only transfer of charge occurs because of minority carrier leakage. When the biasing of this junction is reversed suddenly, a small time is required for the majority carriers to leave their previous position and migrate to the junction. The effect behaves like a capacitance. Since the time required to "charge" this capacitance measurably affects the response time of the flip-flop, we put a small "speed-up" capacitor across the 3.9k base resistor in each leg. This allows the impulse to be transmitted through a capacitive voltage divider, thus reducing propagation time.

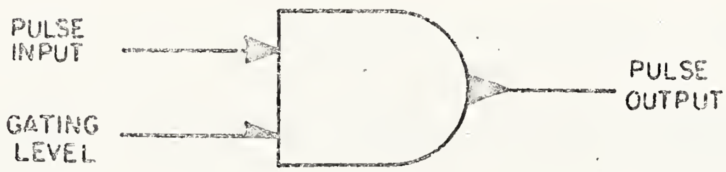
The series MAD-1 flip-flop have attached permanently to each input a pulse gate or steering gate. The diagram below shows the circuit and wave forms for these gates. Note that the steering gate will respond only to the coincidence of a logical "1" on the resistor input and a positive-going transition on the capacitor input. The resulting output is sufficient to cause a flip-flop to transfer states.

Using these gates, it is possible to construct flip-flops in various configurations common in the literature. Most of the modifications are made by adding jumpers to the connector. These configurations are:

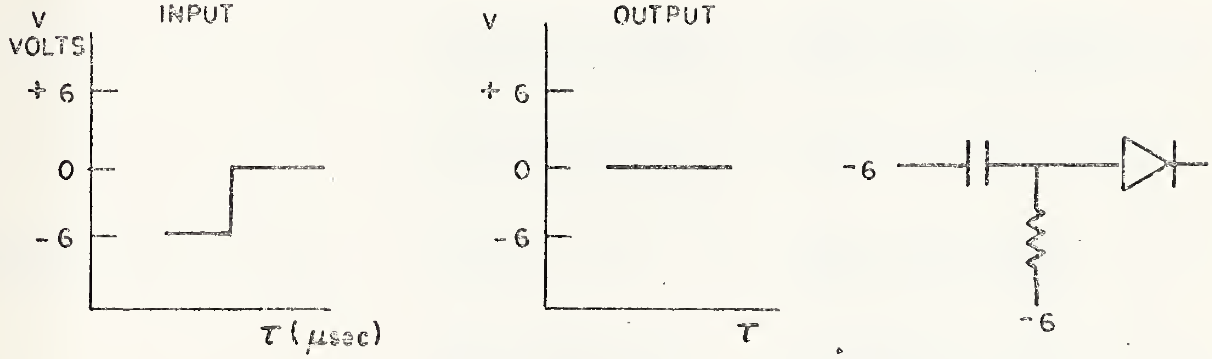
The J-K Flip Flop. If the resistor of a steering gate is connected to the output of the same side of the flip-flop, the R input is changed to a K input, and the S input to a J input. These inputs have the property of gating themselves. If the flip-flop is in the 0 state and the J input is energized, the J gate fires, and the trigger pulse causes a transition. If the flip-flop is in the 1 state and the J input is energized, the J gate does not fire, and no trigger pulse gets through. If now both inputs are energized at once, only the gate whose corresponding transition is "on" will transmit a turnoff pulse. The other will not respond. The result is that ambiguity of the R-S type of circuit is eliminated.

The T circuit is wired by connecting the capacitors from the J and K inputs together. The resulting action is that a positive-going transition on this connection will transfer the flip-flop from whichever state it is in to the other state. This is especially useful in counter circuits.

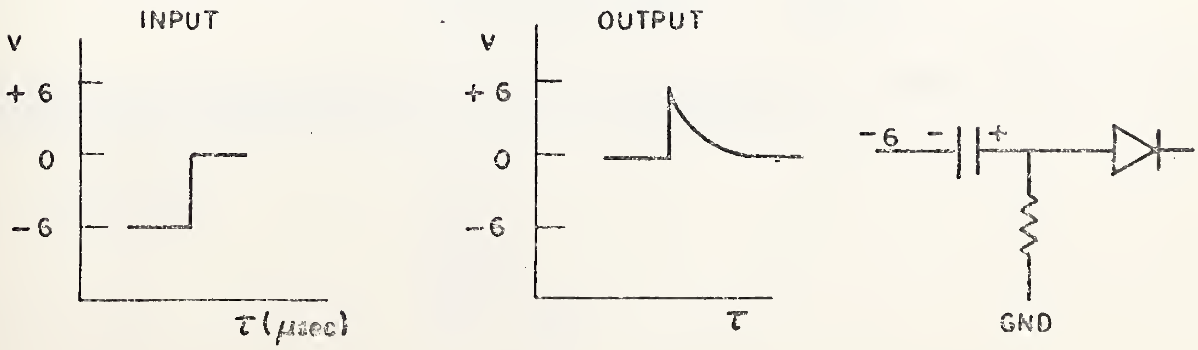




GATE CLOSED



GATE OPEN



If the resistor of the steering gate is not connected to the flip-flop collectors, but instead is wired to the collector of a flip-flop adjacent to it in a chain of similar circuits, a pulse on the capacitor of this gate will cause the flip-flop to assume the state of the previous member of the chain. Since the operation of the gate does not depend on the immediate state of the resistor input, but rather on the recent history (whether or not the capacitor is charged), it is possible to pulse all of the capacitors in the chain at once, thereby causing the contents of the chain to "move over" one position. This is called a shift register.

This gate is the one referred to in the logical applications section as being useful for performing external logic functions.

Trouble Shooting. The following table lists some troubles that may be encountered and suggests probable causes and remedies.

Symptom	Cause	Remedy
Will not change state	Q_1 or Q_2 shorted	Replace (Ohmmeter check will disclose)
" " " "	Insufficient input dv/dt or amplitude	Check driving circuits, check dc beta of transistor
" " " "	Output loading for one side too great	Use output buffer amplifier
Changes state at wrong time	"logical spikes" on inputs	Check with Scope. Redesign Logic to eliminate
" " " "	Inadequate power supply filtering	Decouple all high current and inductive devices from power bus
Will not operate fast enough	Gate resistor disconnected	Jumper on card connector
" " " "	"Speed-up" capacitors wrong value	Replace

Construction Information. Figure 11 shows the component layout of the card, and the table below lists the required components.

Quantity	Item
8	2N404
8	DR435
6	Test Jacks

Quantity	Item
8	620 ohm Resistors 1/2 w 5%
8	33k Resistors
8	3.9k Resistors
8	5.1k Resistors
8	200 pf or 220 pf Capacitors
8	0.001 uf Capacitors
	Transipads and Circuit Board

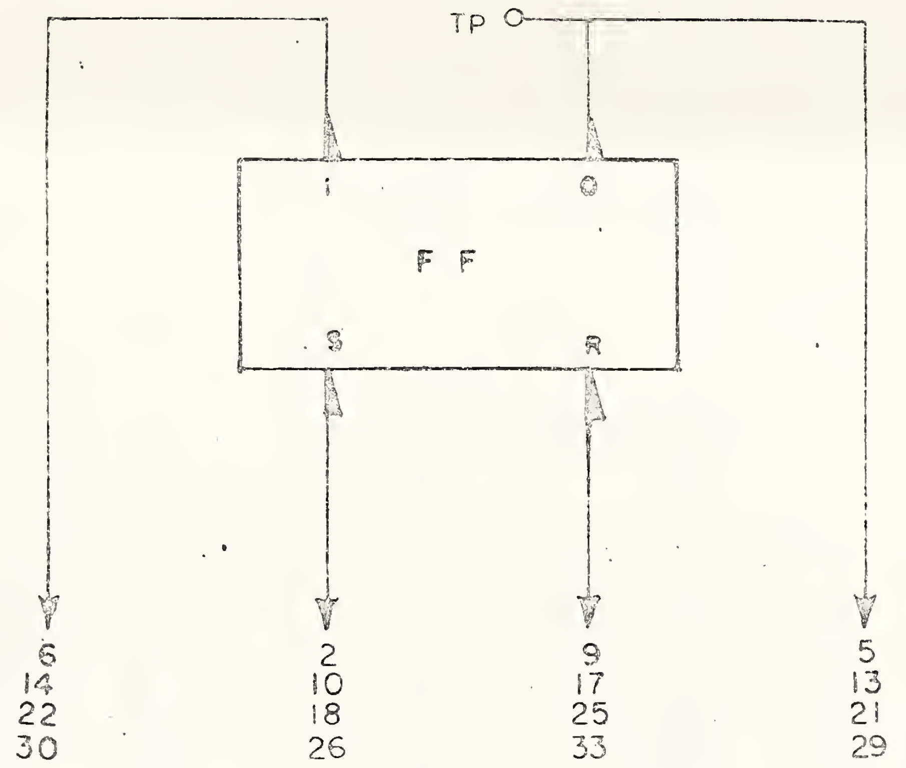


FIGURE 6. FLIP-FLOP SERIES MAD-1 AS AN R-S FLIP-FLOP

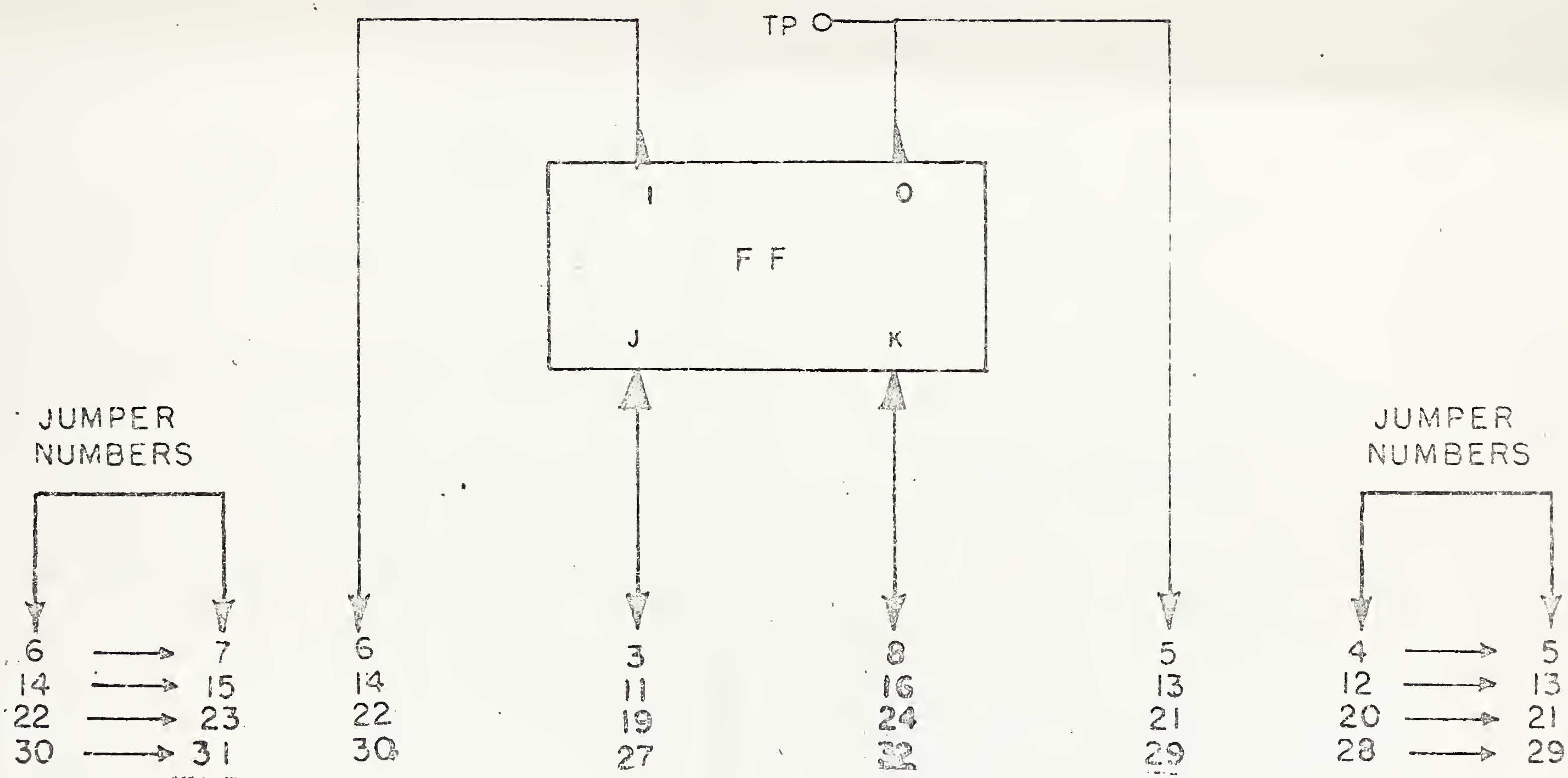


FIGURE 7 FLIP-FLOP SERIES MAD-1 AS A J-K FLIP-FLOP

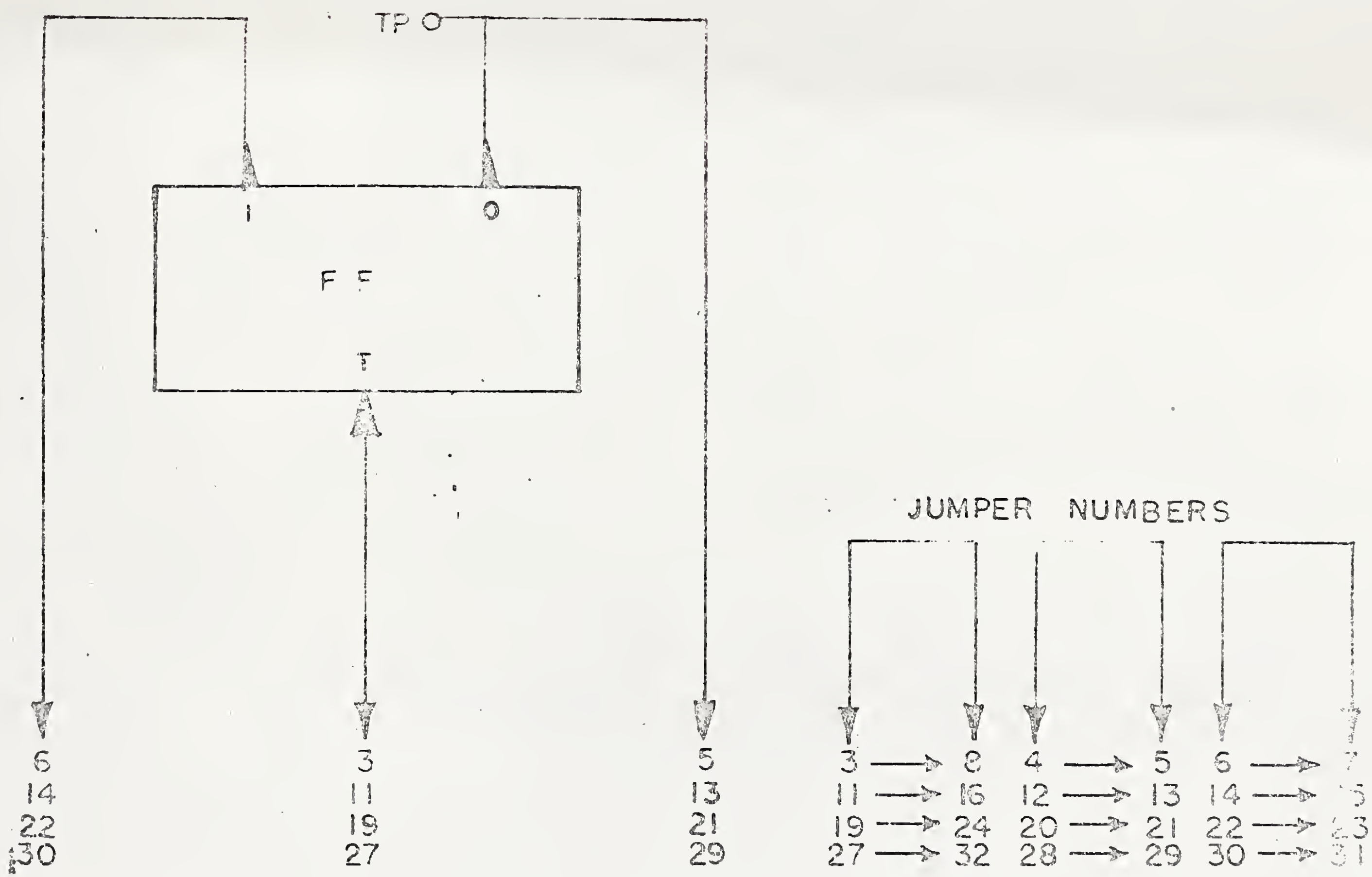


FIGURE 8. FLIP-FLOP SERIES MAD-I AS A T FLIP-FLOP

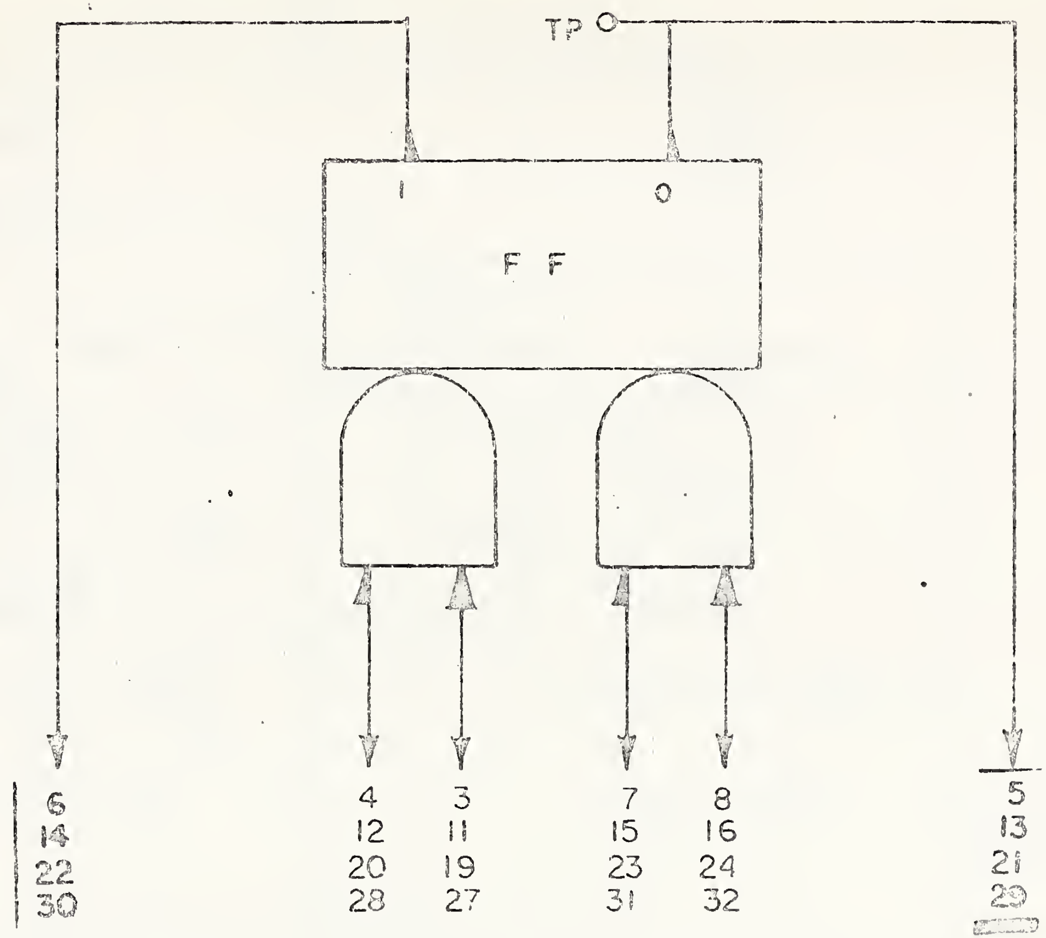
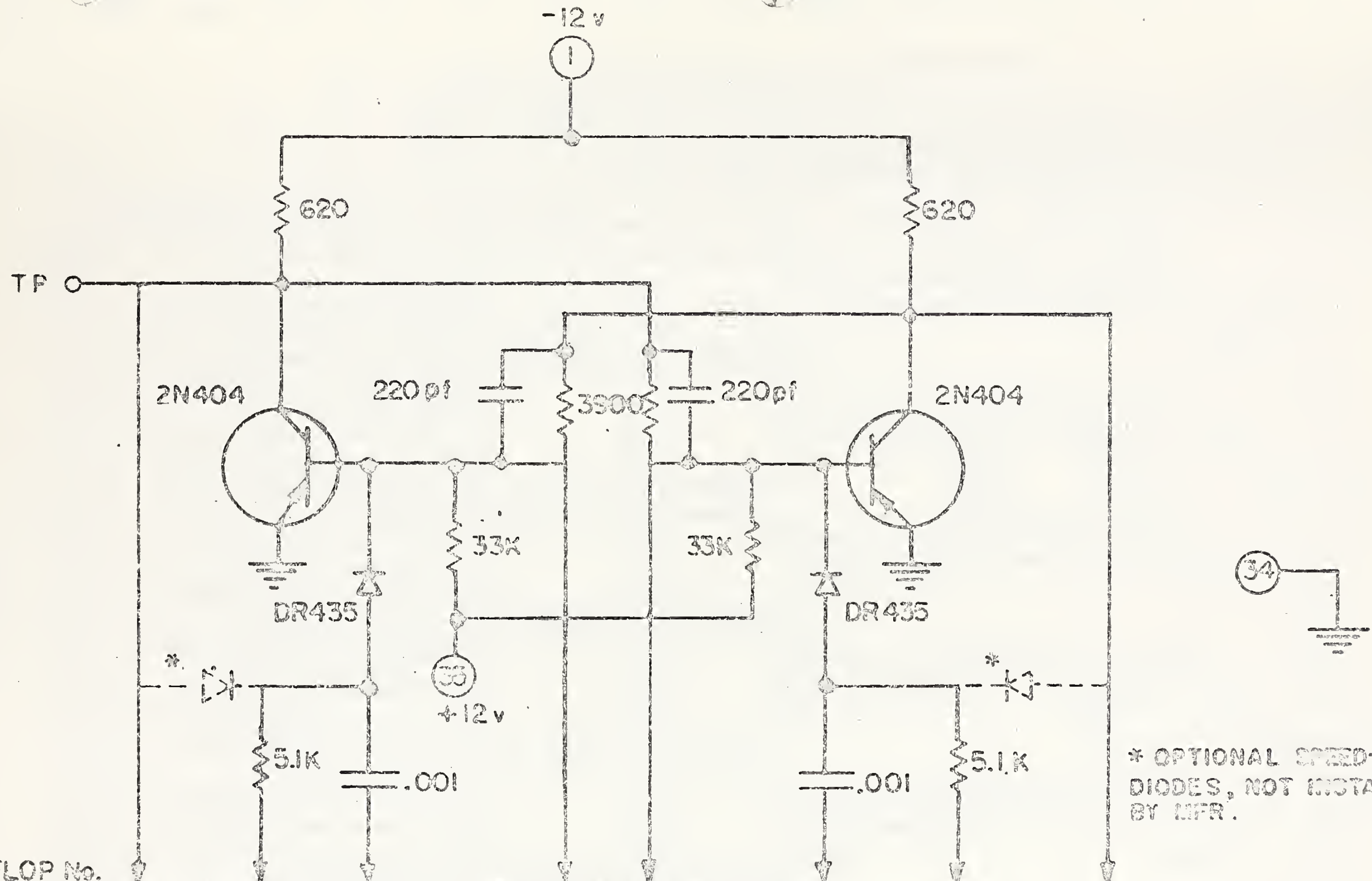


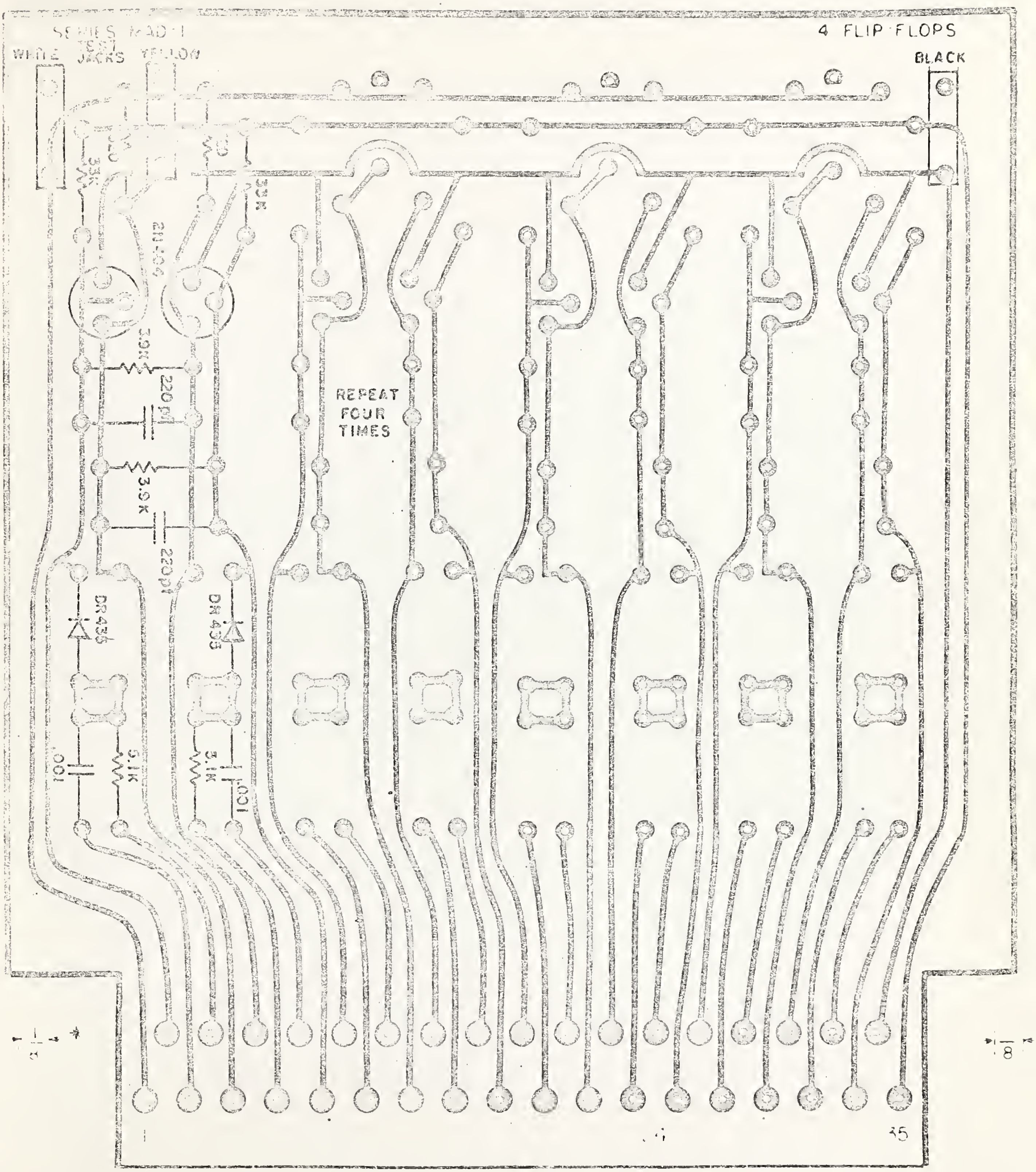
FIGURE 9. FLIP-FLOP SERIES MAD-1 AS A GATED FLIP-FLOP



* OPTIONAL SPEED-UP DIODES, NOT INSTALLED BY MFR.

FLIP-FLOP No.	ZERO OUTPUT	ZERO GATE	J INPUT	ZERO BASE	ONE BASE	K INPUT	ONE GATE	ONE OUTPUT
1	5	4	3	2	9	8	7	6
2	13	12	11	10	17	16	15	14
3	21	20	19	18	25	24	23	22
4	29	28	27	26	33	32	31	30

FIGURE 10. FLIP-FLOP SERIES MAD-1



✱ MIN. PERMISSIBLE SPACE FROM EDGE OF CONDUCTOR TO EDGE OF BOARD

FIGURE 11.

FIGURE 12.

c. Pulse Gate

Logical Function. Each circuit will perform the AND function for one steady logic level and one pulse consisting of a change of level from 0 to 1.

Circuits per Card. Ten.

Input Load. One standard pulse gate.

Fan-Out. To drive one flip-flop.

Power Requirements. None.

Logic Diagrams. Figure 13 shows the logic diagram. Figure 14 shows how up to 5 may be connected to the R or S input of a flip-flop up to five pulse gates.

Logical Application. This circuit is usually used when a simple gate is needed to allow a flip-flop to be either triggered or not triggered when an input pulse appears. It also allows data to be transferred into a flip-flop or group thereof synchronously with some event, as might be encountered in the loading of an entire register at once.

Input Signal Requirements.	Positive level:	0 volts to -0.2 volts
	Negative level:	-6 volts to -12 volts
	Input impedance:	0.001 uf to ground when connected to a flip-flop.

Output Signal Characteristics. Short positive voltage spike for triggering flip-flops.

Circuit Description. The diagram for the circuit is given in Figure 15. Assume that the voltage at the input to the resistor R is -6 volts, and that the input to the capacitor C is being held at -6 volts. The capacitor will not charge. When the input to C experiences a positive transition from -6 volts to ground, the common terminal follows the capacitor to ground. This is still not sufficient to forward-bias the diode, so the gate does not conduct. When the input to R is at ground, the capacitor charges to 6 volts, with the negative side being the capacitor input terminal. When the input to the capacitor does go to ground, the common terminal of the gate also goes up by 6 volts, forward biasing the diode and emitting a short positive pulse, sufficient for triggering a flip-flop.

Trouble Shooting. The following table lists some troubles that may be encountered and suggests probable causes and remedies.

<u>Symptom</u>	<u>Cause</u>	<u>Remedy</u>
Flip-flop triggers on either positive or negative-going signals	Diode shorted	Replace

<u>Construction Information.</u> Figure 16 shows the component layout of the card and the table below lists the required components.

<u>Quantity</u>	<u>Item</u>
10	DR435
10	0.001 uf Capacitors
10	5.1k ohm Resistors
	Circuit Board

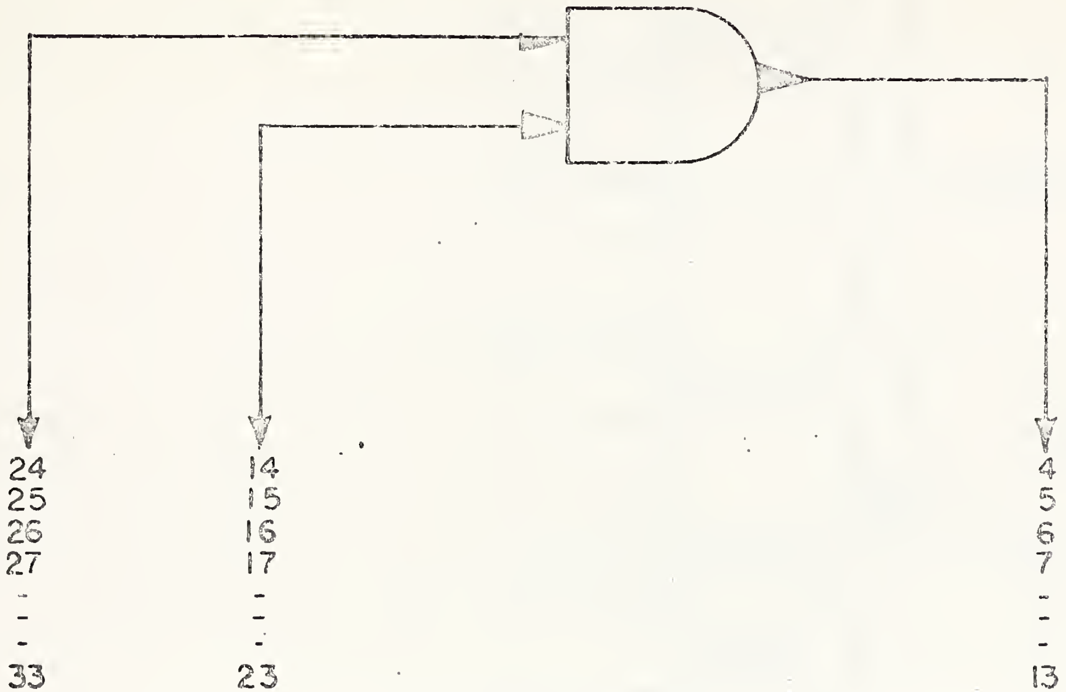


FIGURE 13 PULSE-GATE SERIES MAD-1

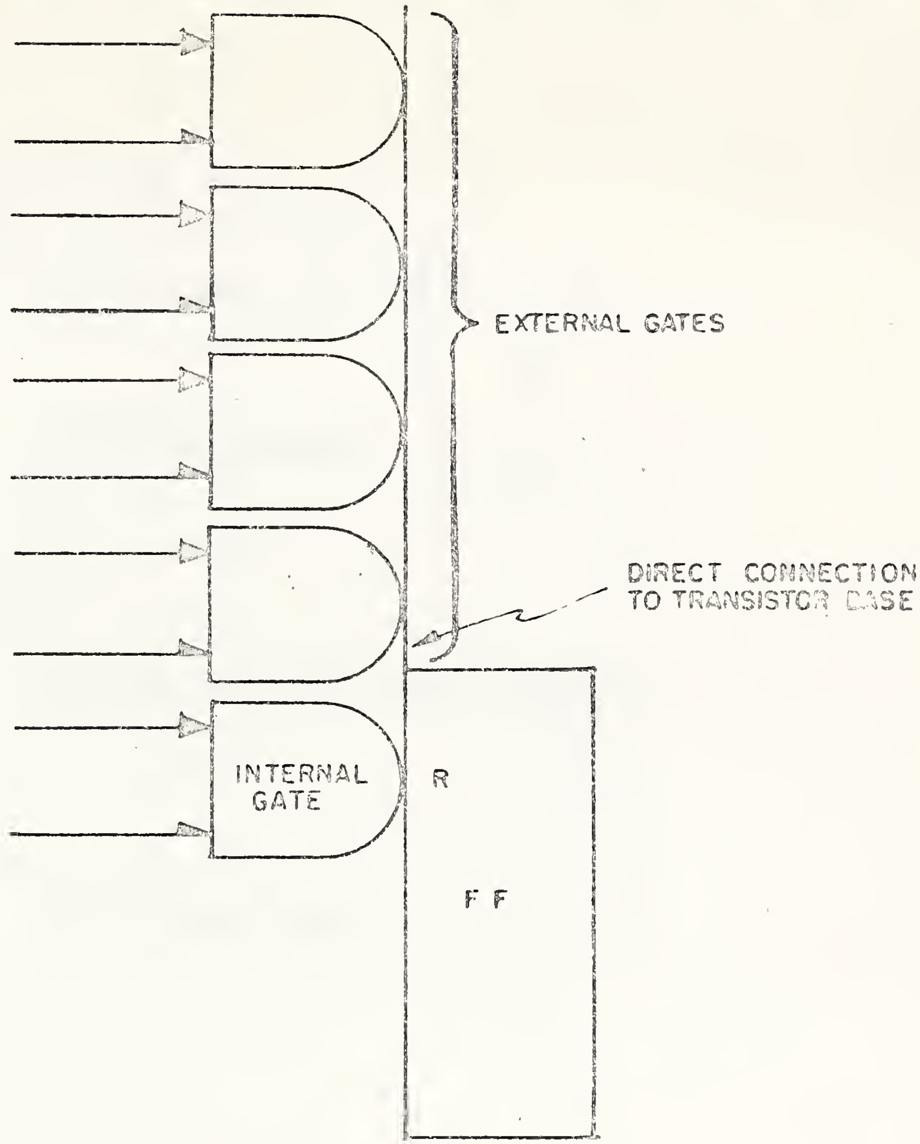
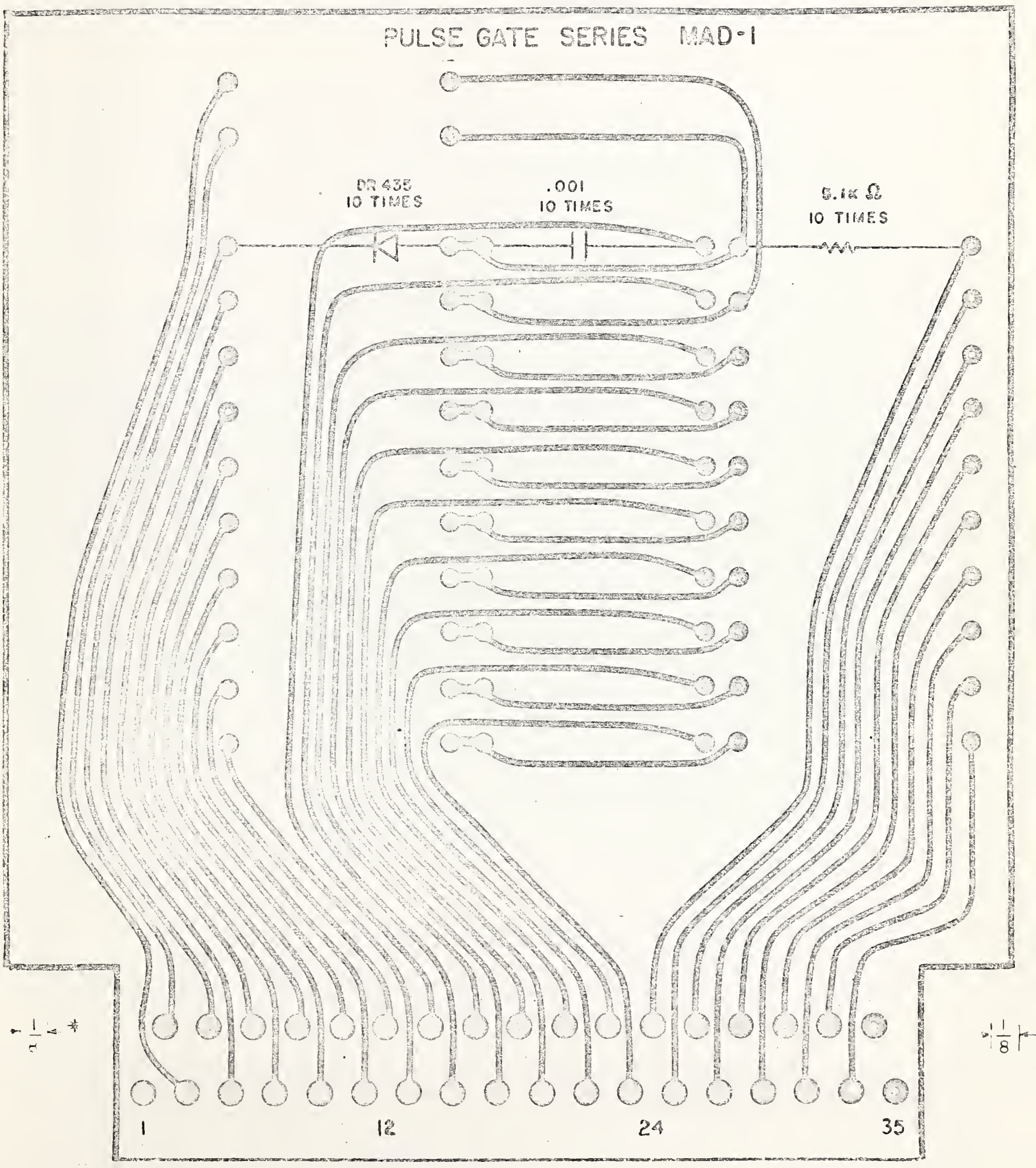


FIGURE 14. FIVE PULSE GATES CONNECTED TO FLIP-FLOP R INPUT

CIRCUIT No.			
1	14	4	24
2	15	5	25
3	16	6	26
4	17	7	27
5	18	8	28
6	19	9	29
7	20	10	30
8	21	11	31
9	22	12	32
10	23	13	33

FIGURE 15. PULSE GATE SERIES MAD - I



✳ MIN. PERMISSIBLE SPACE FROM EDGE OF CONDUCTOR TO EDGE OF BOARD

FIGURE 17.

d. Reed Relays

Logical Function. Each circuit, upon receipt of a proper command, will mechanically close two shielded, isolated circuits.

Circuits per Card. Four.

Input Load. One standard logic gate.

Fan-Out. Mechanical contacts capable of switching 125 milliamps, non-inductive.

Power Requirements. -12 volts: 50 ma standby, 48 ma for each relay energized.
+12 volts: 3 ma.

Logical Diagrams. Figure 18 shows the logic diagram and pin numbers.

Logical Application. This is used in an analog scanning system where several voltages in sequence must be switched (for example) into one analog-to-digital converter. It is also used where it is impossible to connect some common point between the circuit in question and the logic circuits.

Input Signal Requirements. Positive level: 0 volts to -0.2 volts.

Negative level: -6 volts to -12 volts.

Input impedance: 3000 ohms sink to ground.

Output Signal Characteristics. Contact closure, two per circuit. Maximum load 125 ma non-inductive. Bounce: less than 1 millisecond at any operating speed. Vibration noise: 10 millivolts for two milliseconds.

Circuit Description. The diagram is shown in Figure 19.

This package contains four double-pole, single throw dry reed encapsulated relays with an estimated life greater than 10,000,000 operations under a contact load less than 10 ma. The relays are capable of being operated at more than 1,000 Hertz, and at that speed will have less than 500 microseconds of bounce.

In order that low-level signals may be accommodated by these relays, all of the conductors on the card that carry such signals are shielded. This is accomplished by adding guard bands (grounded conductors) on both sides of the lead in question, and by using a double-clad board with the copper on the other side left intact and grounded.

The package contains all of the necessary circuitry to drive the relays, and requires only standard logic levels to activate them. A positive level on the input closes the contacts. A two-input AND gate is built in to simplify synchronization of multiple circuits.

Installation. Because of the size of the reed relays, it is not possible to mount these cards with the connectors on 5/8" centers, as is customary. By alternating them with other cards, however, there will be sufficient room to use 5/8" centers.

Trouble Shooting. The following table lists some troubles that may be encountered and suggests possible causes and remedies.

Sympton	Cause	Remedy
Relay contacts remain closed	Shorted 2N659	Replace
" " " "	Contacts welded closed by large current pulse	Replace - insure that relay is operating within its ratings
Relay contacts remain open	Shorted 2N404	Replace
Contact Resistance Large (> 1 ohm)	Relay at end of life	Replace

Construction Information. Figure 20 shows the component layout of the card and the table below lists the required components.

Quantity	Item
4	2N659
4	2N404
8	DR435
4	IN2069
8	3.9k Resistors
4	1k Resistors
8	33k Resistors
4	100 ohm 5 percent 1 watt Resistors
10	Eyelets, installed
4	Reed Relays
	Transipads & Circuit Board

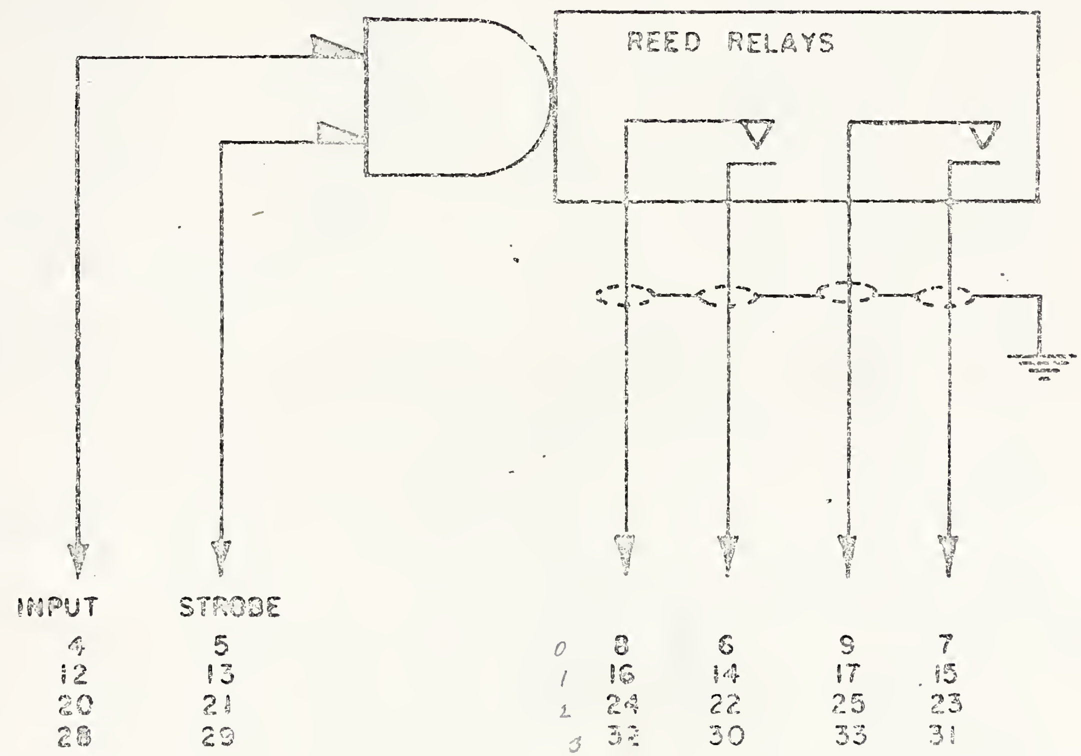


FIGURE 16. REED RELAYS SERIES MAD-1

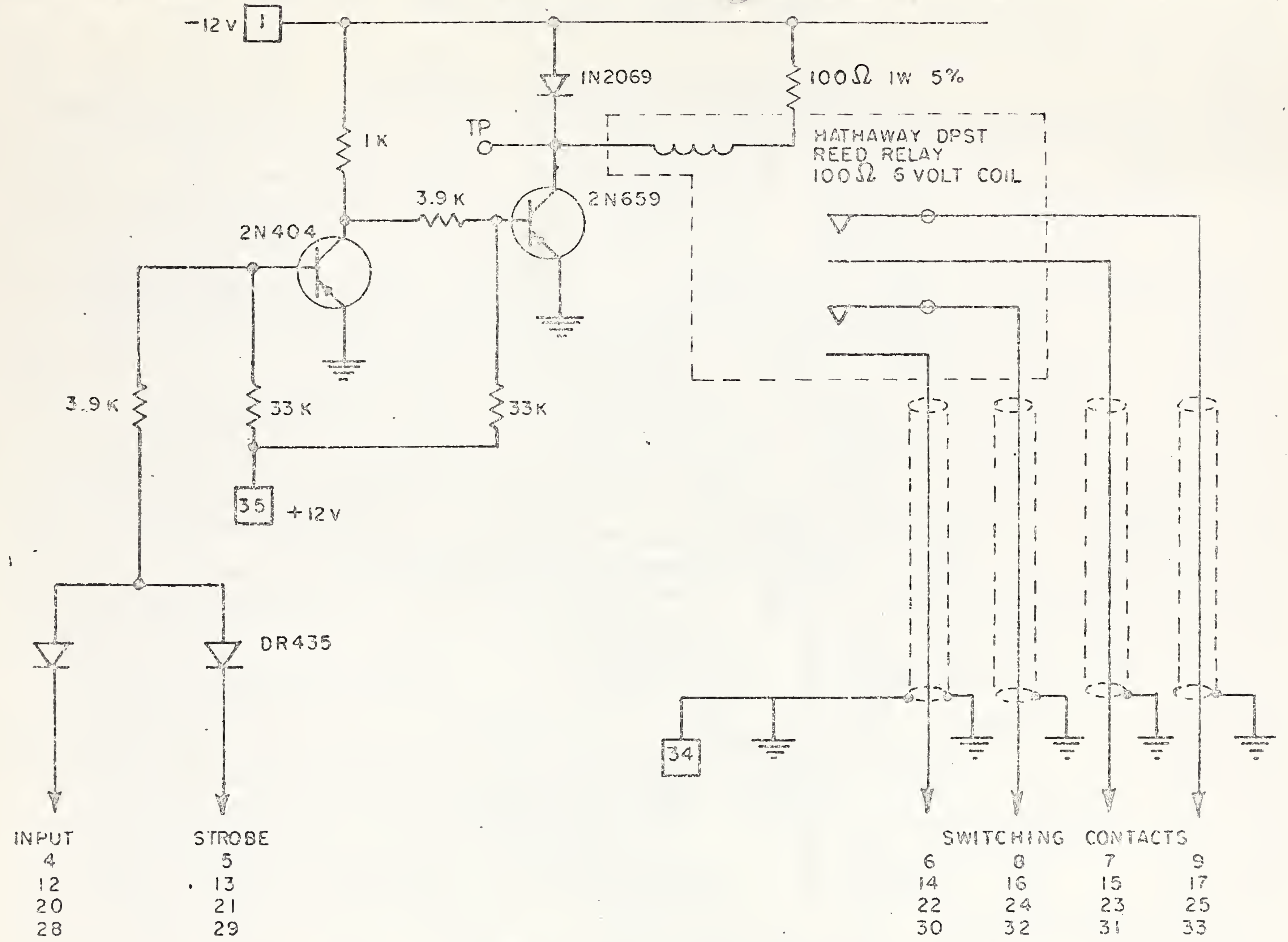


FIGURE 19. REED RELAYS SERIES MAD-1

REED RELAYS SERIES MAD-1

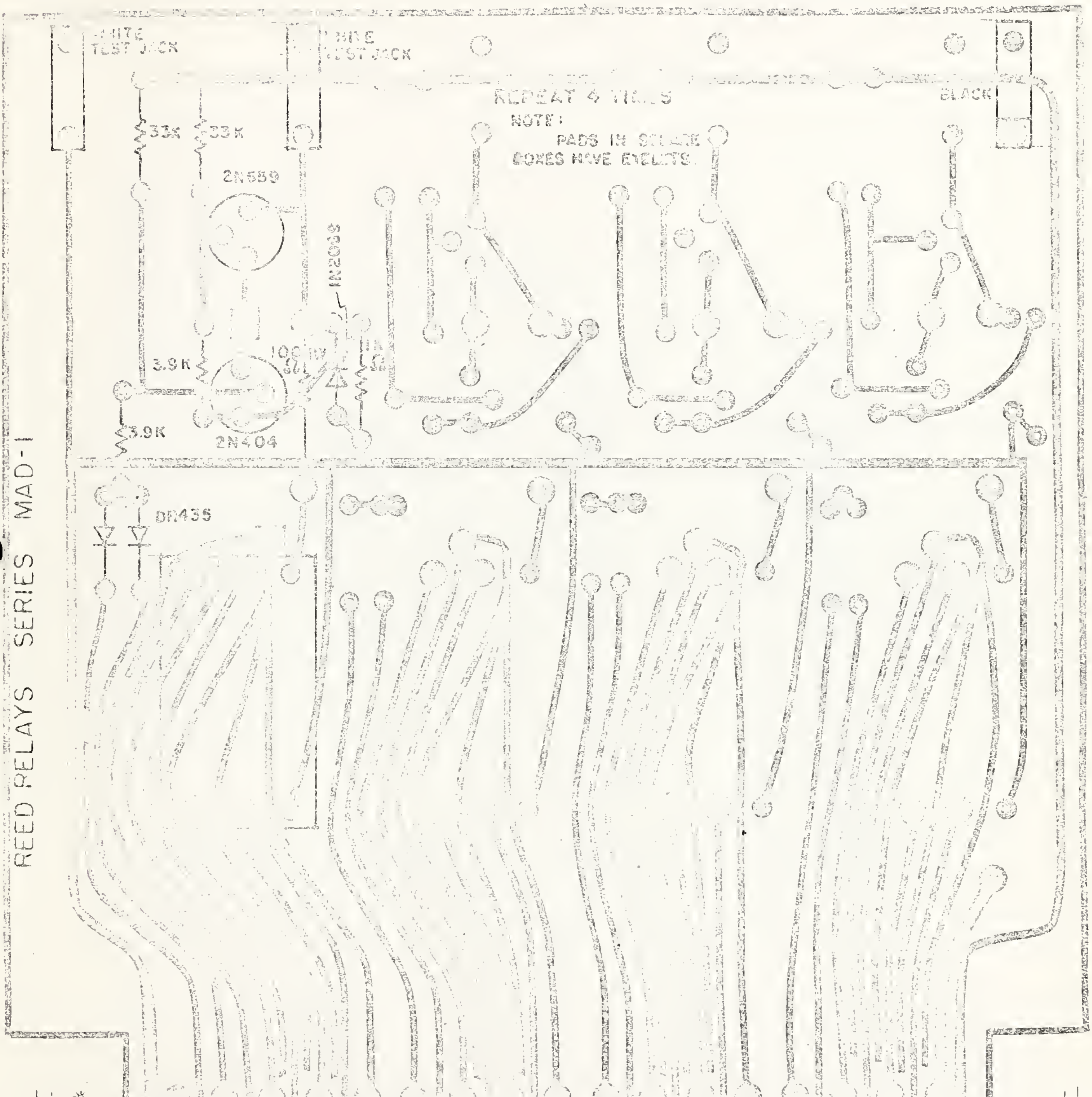


FIGURE 20.

Figure 21.

e. Pulse Gate Driver

Logical Function. This circuit is used to extend the drive or fan-out capabilities of a circuit card.

Circuits per Card. Four.

Input Load. Two standard logic gates.

Fan-Out. 25 standard logic gates and 25 pulse gates.

Power Requirements. -12 volts: Maximum of 60ma per circuit, depending on loading.

+12 volts: 2.5ma.

Logic Diagram. Figure 22 shows the logic diagram and pin numbers.

Logical Application. In general, when pulse gates are used to synchronize a large number of simultaneous operations, as in shifting of registers, all of the gate capacitors are connected to a single line. This line must be held at -6 volts or -12 volts, and then brought to ground. When this transition takes place, a large amount of current flows, much more than a standard card can handle. This circuit is especially designed to drive a large number of loads.

Input Signal Requirements. Positive level: 0 to -0.2 volts.

Negative level: -6 volts to -12 volts.

Input impedance: 2000 ohms sink to ground shunted by 440pf.

Output Signal Characteristics. Positive level: 0 volts to -0.2 volts through a saturated transistor.

Negative level: -12 volts at 200 ohms.

Circuit Description. The circuit is shown in Figure 23.

Although similar to the circuit described in Technical Note 168, the output transistors of this package have been changed to a type with an extremely low R_{CE} (SAT). The circuit operates by connecting the output either to the minus 12 volt line, or to ground. Both paths are through saturated transistors, and therefore ones with low saturation resistance are more desirable.

It was found necessary in some applications to limit the output swing of the package to the region between -6 volts and ground, rather than allowing it to go all the way to -12 volts. A resistor to accomplish this

has been brought out to the connector. To limit the output to 6 volts, this must be jumpered to the adjacent pin, which is ground.

When the input signal is negative, the 2N404 transistor is saturated, and the collector is at ground.. This turns off the upper 2N659. The lower 2N659 is on because it is also connected to the negative input. This effectively shorts the output terminal to ground through the saturated lower 2N659. The 2N659 is a transistor with special characteristics designed so that the collector saturation resistance is very low, on the order of 300 milliohms.

When the input is positive, the 2N404 is cut off, as is the lower 2N659. The upper 2N659 is on, and the output is shorted to the -12 volt supply through the upper 2N659. To limit the negative level of the output to -6 volts, connecting the low side of the resistor shown prevents the voltage at the base of the upper 2N659 from exceeding -6 volts, thereby limiting the collector.

Trouble Shooting. The following table lists some troubles that may be encountered and suggests probable causes and remedies.

Symptom	Cause	Remedy
Output remains at ground	Shorted 2N659 (lower)	Replace
" " " "	Shorted 2N404	Replace
Output remains negative	Shorted 2N659 (upper)	Replace

Construction Information. Figure 24 shows the component layout of the card and the table below lists the required components.

Quantity	Item
8	2N659
4	2N404
6	Test Jacks
8	1.5k Resistors
8	33k Resistors
4	200 Ohm Resistors
8	4.3k Resistors
8	390 pf Capacitors
	Transipads and Circuit Board

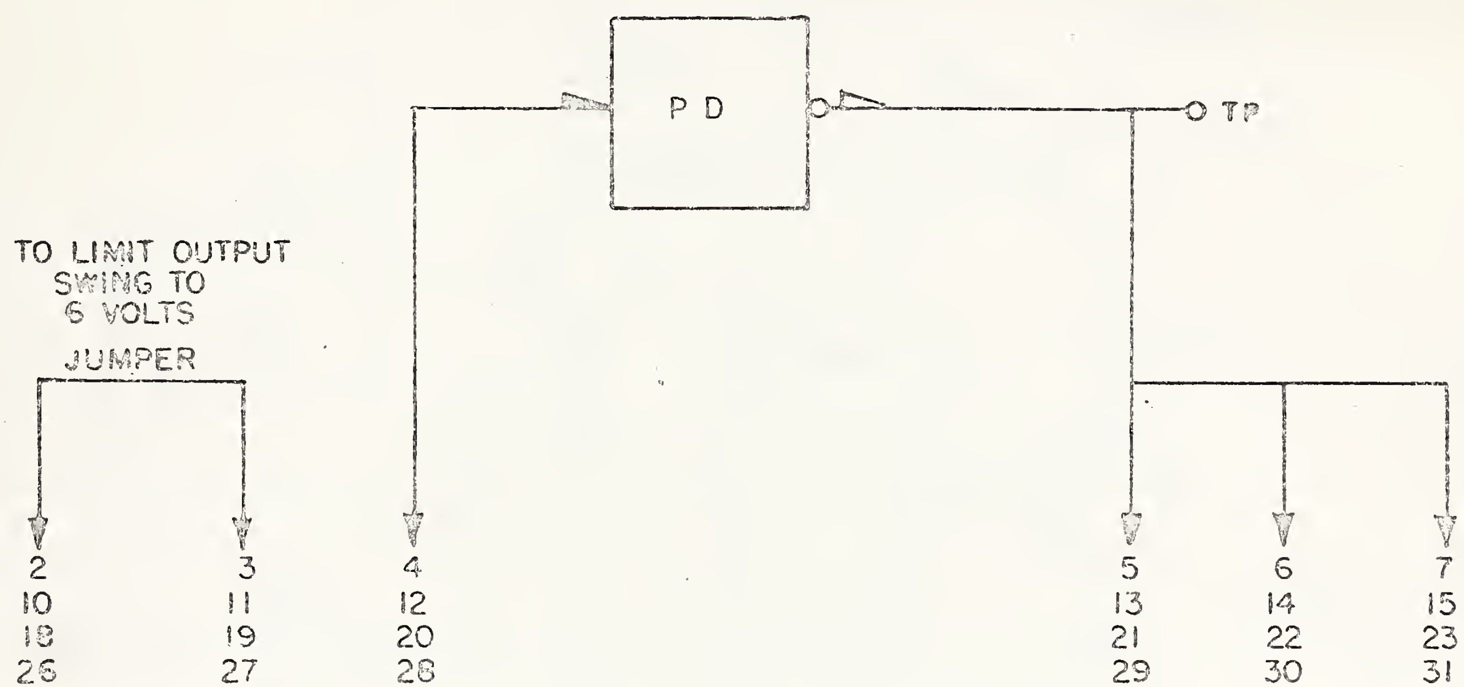
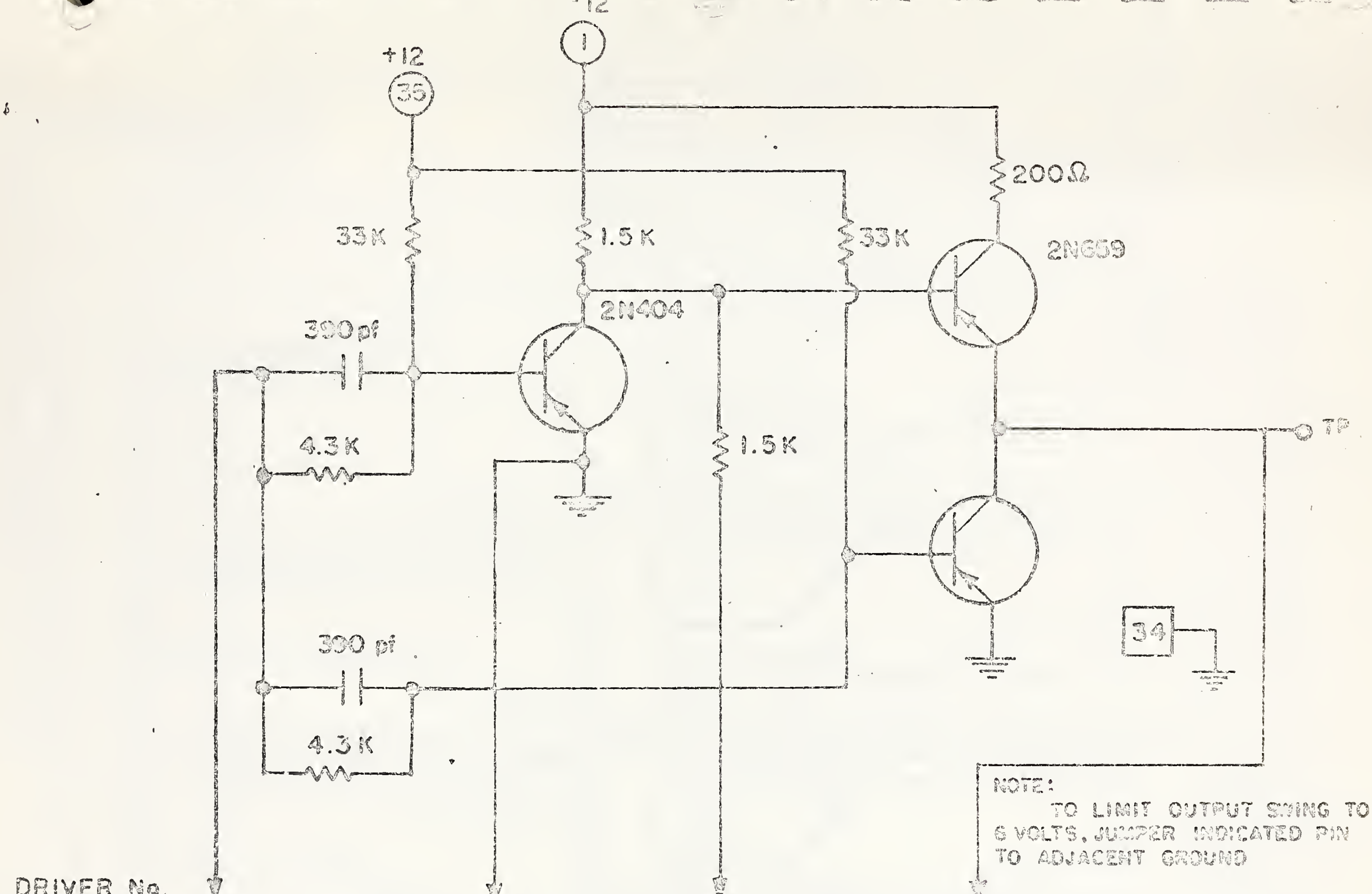
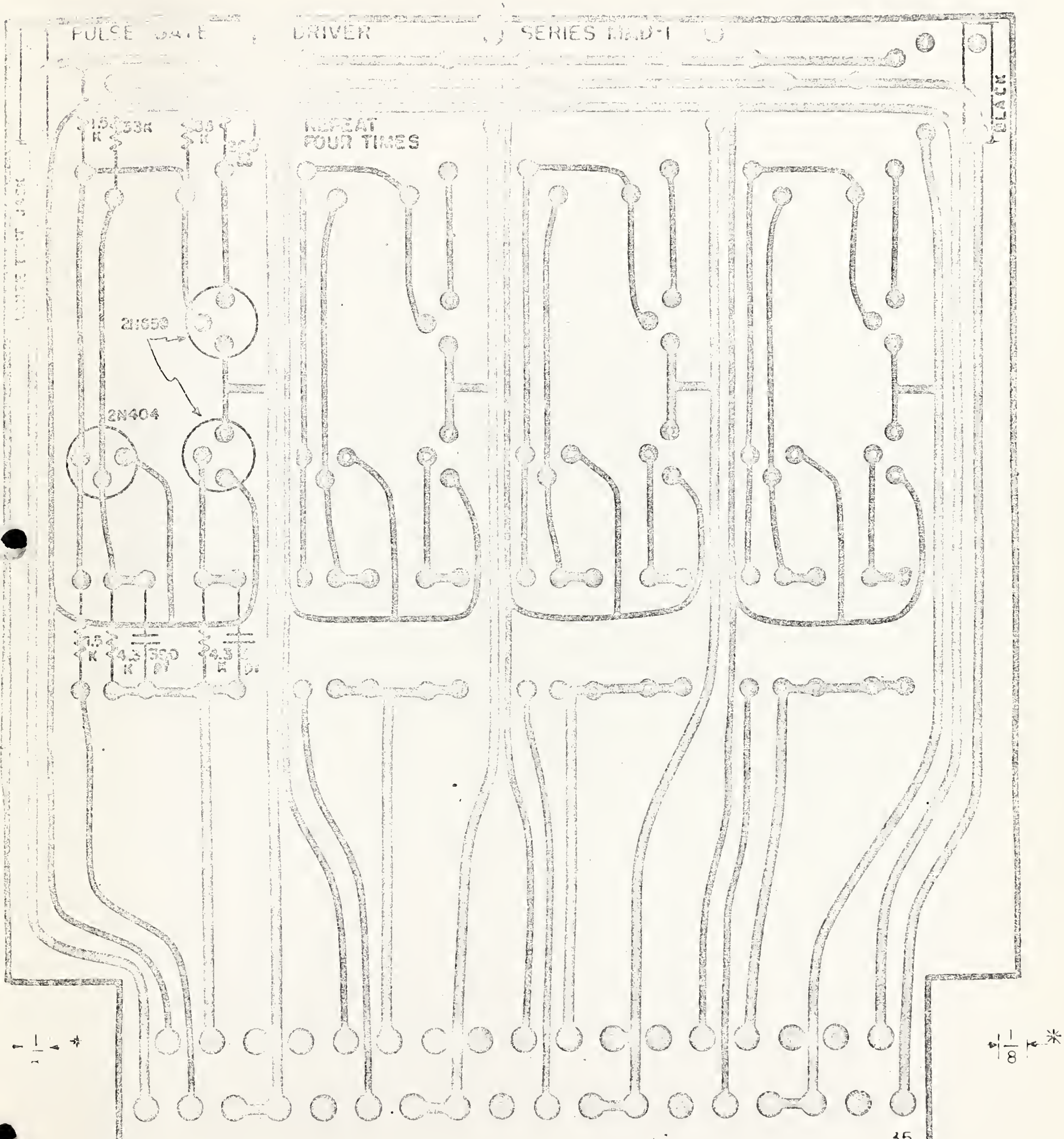


FIGURE 22. PULSE GATE DRIVER SERIES MAD-1



DRIVER No.	INPUT	GROUND	SWING LIMITER	OUTPUTS
1	4	2	3	5,6,7
2	12	10	11	13,14,15
3	20	18	19	21,22,23
4	28	26	27	29,30,31

FIGURE 23. PULSE GATE DRIVER SERIES MAD-1



* MIN. PERMISSIBLE SPACE FROM EDGE OF CONDUCTOR TO EDGE OF BOARD

FIGURE 24.

FIGURE 25.

f. One-Shot

Logical Function. This circuit is used as a timing or delay element. Two circuits may be connected as an oscillator.

Circuits per Card. Two

Input Load. One pulse gate.

Fan-Out. Four standard logic gates and five pulse gates.

Power Requirements. -12 volts: 60 ma per circuit.
+12 volts: 2 ma per circuit.

Logic Diagram. Figure 26 shows the logic diagram and pin numbers.

Logical Application. This circuit is used wherever a certain fixed time must be marked off, either to stop an operation after a certain time, or to start one after a delay. Two may be wired to sequentially start each other after their inherent delay has ended, thus making an oscillator. Basically, it consists of a standard flip-flop which is set by external logic circuitry, and which resets itself at the end of its characteristic time. This time may easily be varied externally.

Input Signal Requirements. Positive level: 0 volts to -0.2 volts.

Negative level: -6 volts to -12 volts.

Input impedance: 0.001 uf to ground.

Minimum dv/dt: 6 volts per microsecond.

Output Signal Characteristics. Positive level: 0 volts to -0.2 volts through saturated transistor.

Negative level: -6 volts to -12 volts.

Circuit Description. The diagram is shown in Figure 27.

This circuit is identical to the modified one-shot described in Technical Note 168. Since our applications involve changes of level, rather than pulses, the trigger output has been left off. Times from 5 microseconds to 5 milliseconds are available using capacitors on the card, and times up to several seconds may be generated with external capacitors, provided that they are low leakage types. An integrally mounted potentiometer is used for fine control of delay time.

Initially, transistors Q_1 and Q_6 are conducting, all others are cutoff. If the input flip-flop is wired as a normal J-K and a positive-going pulse is applied to the J input, the flip-flop changes state, cutting

off Q_1, and turning on Q_2, which cuts off Q_6. This allows whichever timing capacitor is wired in to charge towards a terminal voltage determined by R_1, R_2, and to a small extent the 1k potentiometer.

When the voltage across the timing capacitor exceeds that at the emitter of Q_3, (set by the trimpot), the base-emitter junction of Q_3 is suddenly forward-biased, and Q_3 begins to conduct.

Q_3 then turns on its complement transistor Q_4, which turns on Q_5, clamping the collector of Q_1 to ground, thereby resetting the flip-flop.

Triggering diodes CR1 and CR2 from both the timing circuit and the discharge transistor Q_6 help achieve faster switching of the threshold circuit. These diodes enable the circuit to switch rapidly even when a large timing capacitor is being used.

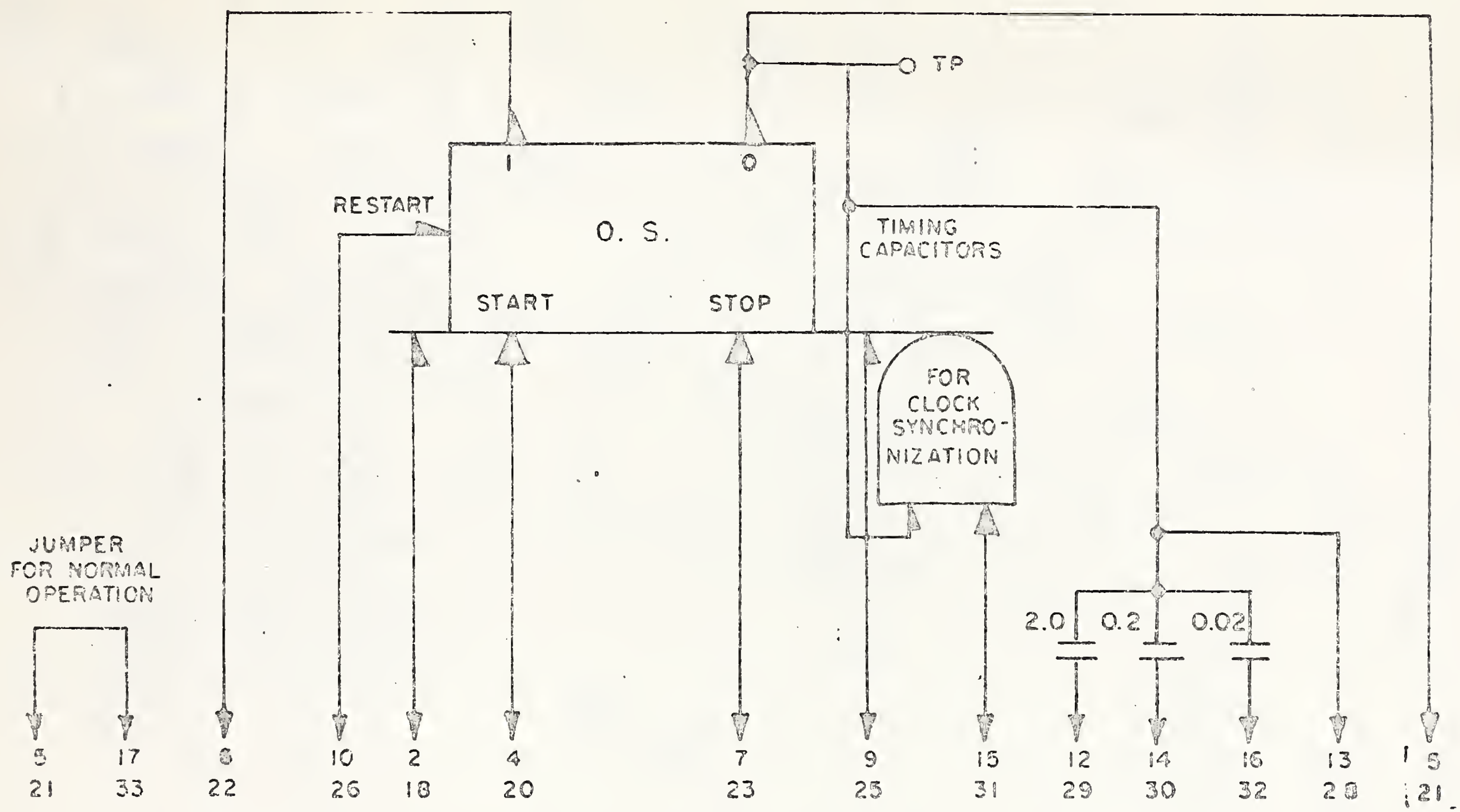
The restart mode of operation permits the capacitor to be discharged and the timing cycle restarted without resetting the flip-flop.

The timing cycle may be ended synchronous to an external pulse train by leaving out the jumper from pin 5 to 17 or 21 to 33, and by attaching the pulse train to pin 15 to 31.

Trouble Shooting. The following table lists some troubles that may be encountered and suggests probable causes and remedies.

Symptom	Cause	Remedy
Flip-flop will not change state when commanded.	Shorted Q_1 or Q_2	Replace
Flip-flop sets but will not reset itself.	No jumper from 5 to 17 or 21 to 33.	Include
Flip-flop sets but will not reset itself.	Shorted Q_6	Replace
Flip-flop sets but will not reset itself.	No capacitor wired in	Wire one in

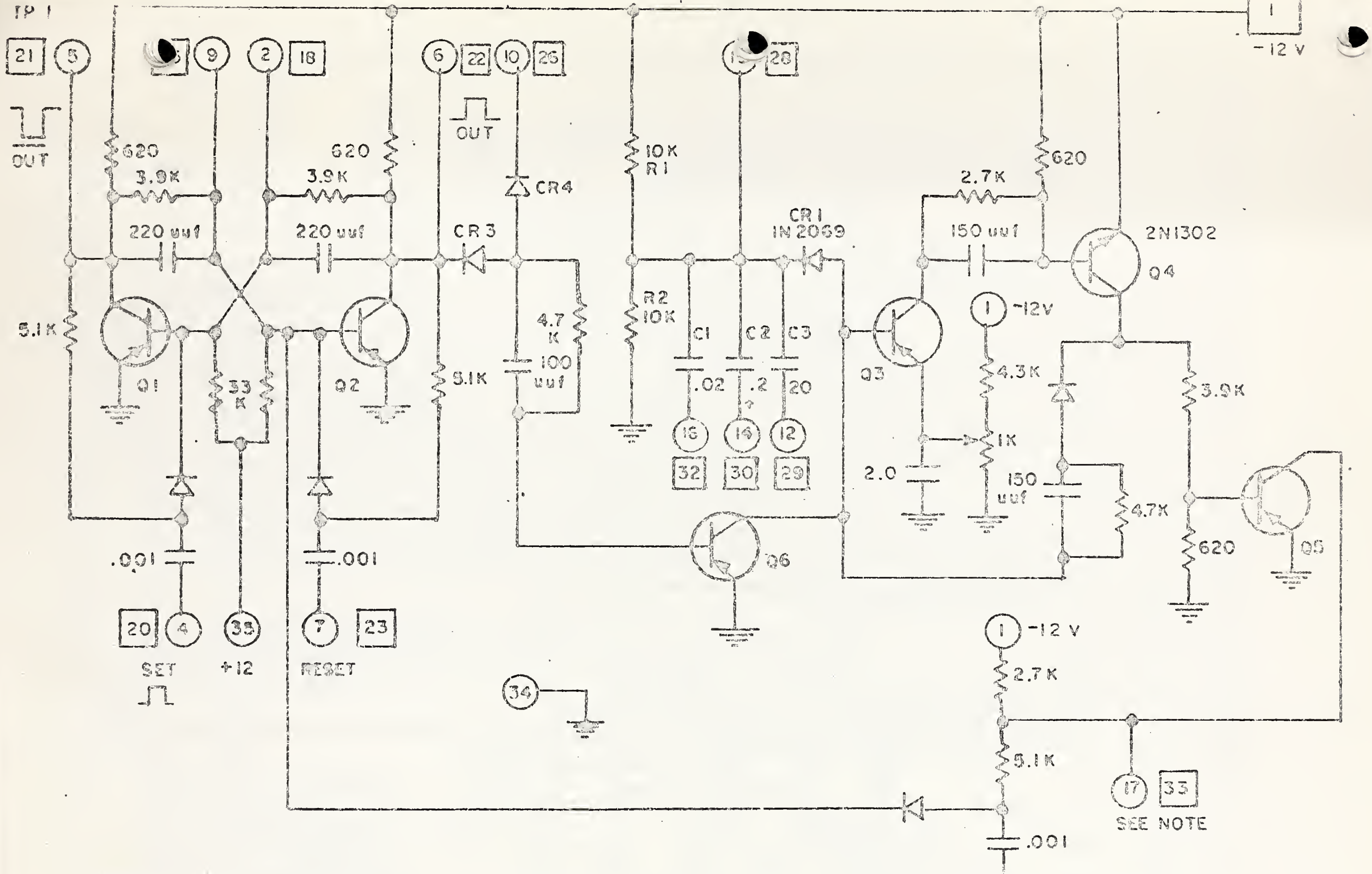
Quantity	Item
12	2N404
2	2N1302
10	DR435
2	1N2069
2	1k ohm Trimpot Series 275
4	Test Jacks
6	3.9k 1/4-watt Resistors
2	3.9k 1/2-watt Resistors
4	33k 1/4-watt Resistors
8	620 ohm 1/2-watt Resistors
6	5.1k 1/4-watt Resistors
4	4.7k 1/4-watt Resistors
4	2.7k 1/4-watt Resistors
2	10k 1/4-watt Resistors
6	.001 uf Capacitors
6	150 pf Capacitors
4	200 pf or 220 pf Capacitors
4	2 uf Electrolytic Capacitors
2	.018 uf Capacitors
2	0.018 uf Capacitors
2	Jumpers
	Transipads and Circuit Board



RUNNING TIME	GROUND PIN
5 usec → 50 usec	16 or 32
50 " → 500 "	14 or 30
500 " → 5 msec	12 or 29

EXTERNAL CAPACITOR TO GND: 13 or 28

FIGURE 26. ONE-SHOT SERIES MAD-1



NOTES:

ALL TRANSISTORS 2N404 UNLESS OTHERWISE SPECIFIED
ALL DIODES DR435 UNLESS SPECIFIED
EXTERNALLY CONNECT PINS 5-17, 21-33 FOR NORMAL AND RESTART OPERATION

FIGURE 27. ONE-SHOT SERIES MAD-1

FIGURE 29.

g. Indicator/Amplifier

Logical Function. This card is used as a buffer amplifier to isolate two circuits, or to provide sufficient drive from a logic level to light a small indicator lamp.

Circuits per Card. Sixteen.

Input Load. One-half standard logic gate.

Fan-Out. When used as an amplifier: Five logic gates and/or five pulse gates.

When used as an indicator driver: One No. 344 incandescent lamp.

Power Requirements. -12 volts: 20 ma for each output at ground.
10 ma for each output at -6 volts.

+12 volts: 5 ma.

Logic Diagrams. Figure 30 shows the logic diagram and pin numbers for use as an amplifier.

Figure 31 shows the logic diagram and pin numbers for use as an indicator driver.

Logical Application. Used as a buffer amplifier with an inverted output. Useful for logical inversion and circuit isolation, its application is more suited for indicator work, since the high impedance amplifier is more noise-free.

Input Signal Requirements. Positive level: 0 volts to -0.2 volts

Negative level: -6 volts to -12 volts.

Input impedance: 8200 ohm sink to ground.

Output Signal Characteristics. Positive level: 0 volts to -0.2 volts through saturated transistor.

Negative level: -12 volts through external load resistor or light from one No. 344 or 1869 incandescent lamp.

Circuit Description. The schematic diagram is shown in Figure 32.

This is a simple transistor inverter. (NOTE: COLLECTOR LOADS SHOULD NOT DRAW MORE THAN 15 ma. At any higher current, the transistor may not be saturated).

Trouble Shooting. The following table lists some troubles that may be encountered and suggests probable causes and remedies.

Symptom	Cause	Remedy
Light remains lit.	Shorted transistor.	Replace
Light will not go on	Insufficient drive.	Check input level; if OK, replace transistor with higher beta unit.

Construction Information. Figure 33 shows the parts layout. The following table lists components necessary for construction.

Quantity	Item
16	2N404
16	8.2k 1/2-watt Resistors
16	33k 1/4-watt Resistors
	Transipads and Circuit Board.

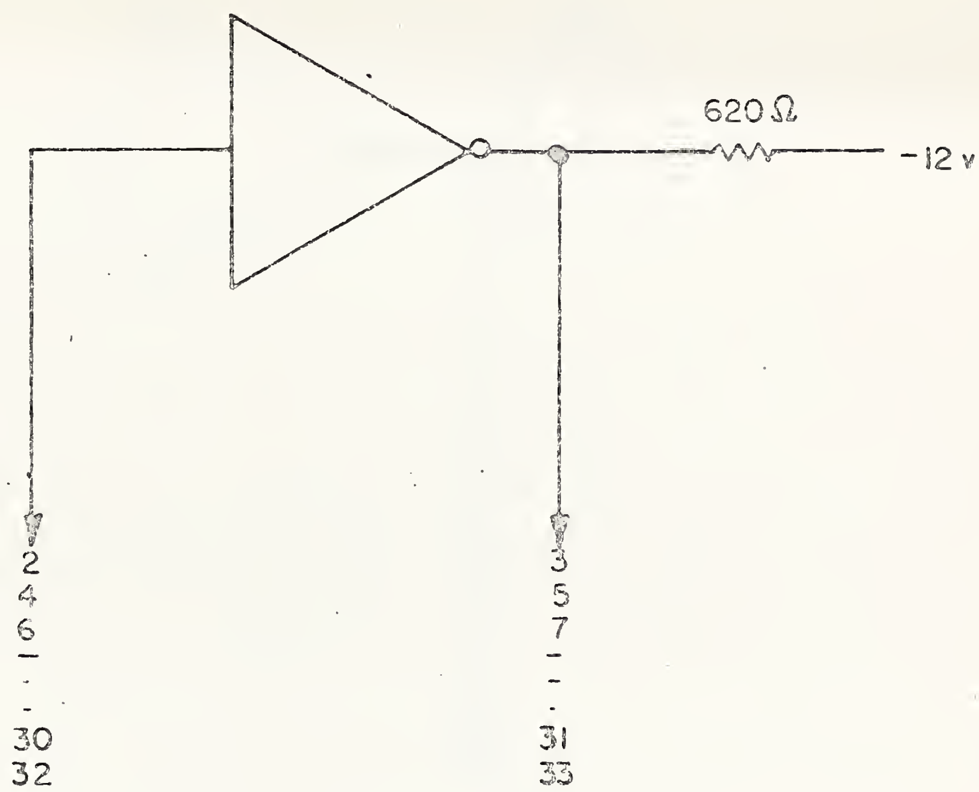


FIGURE 30. INDICATOR/AMPLIFIER SERIES MÅD-1 USED AS AN AMPLIFIER

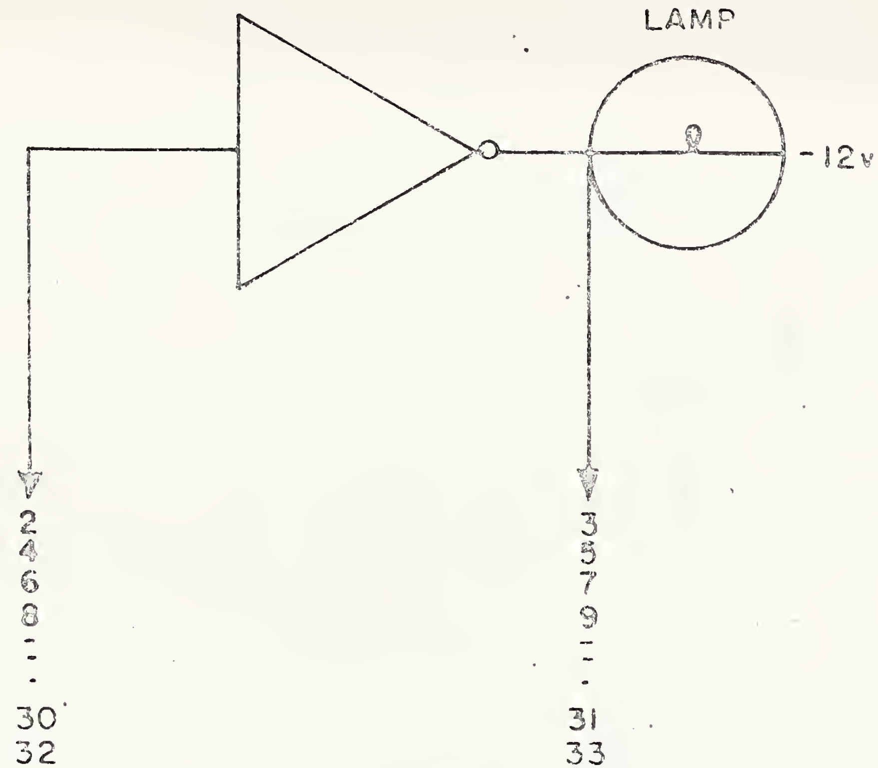
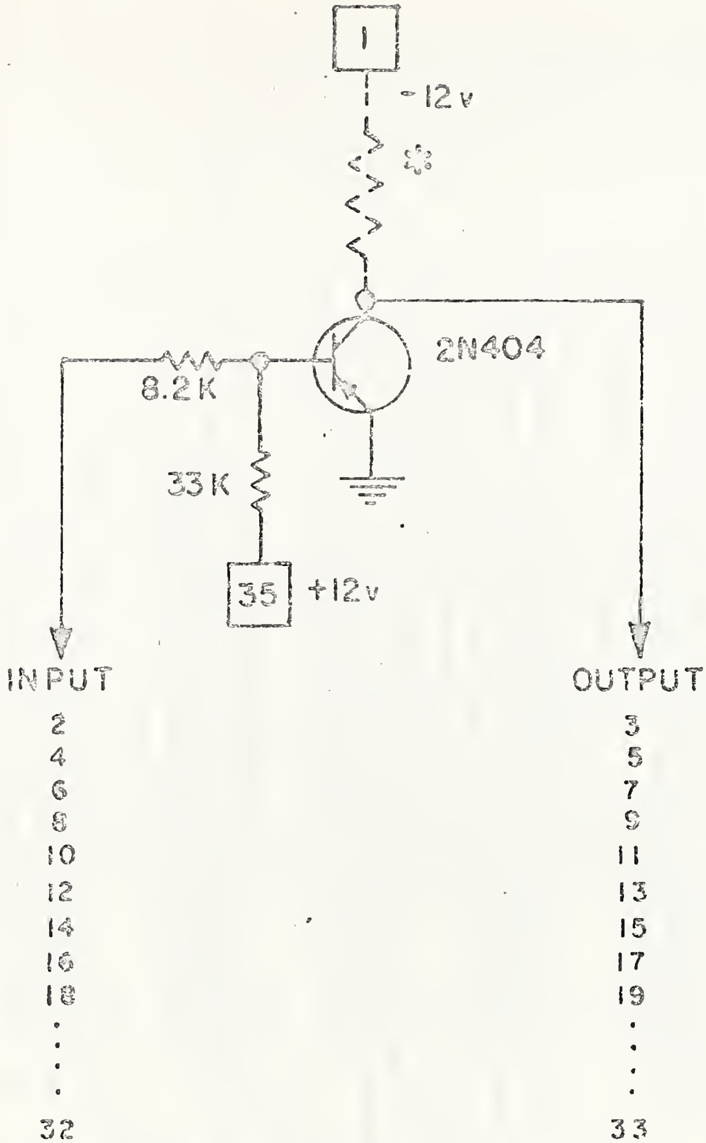


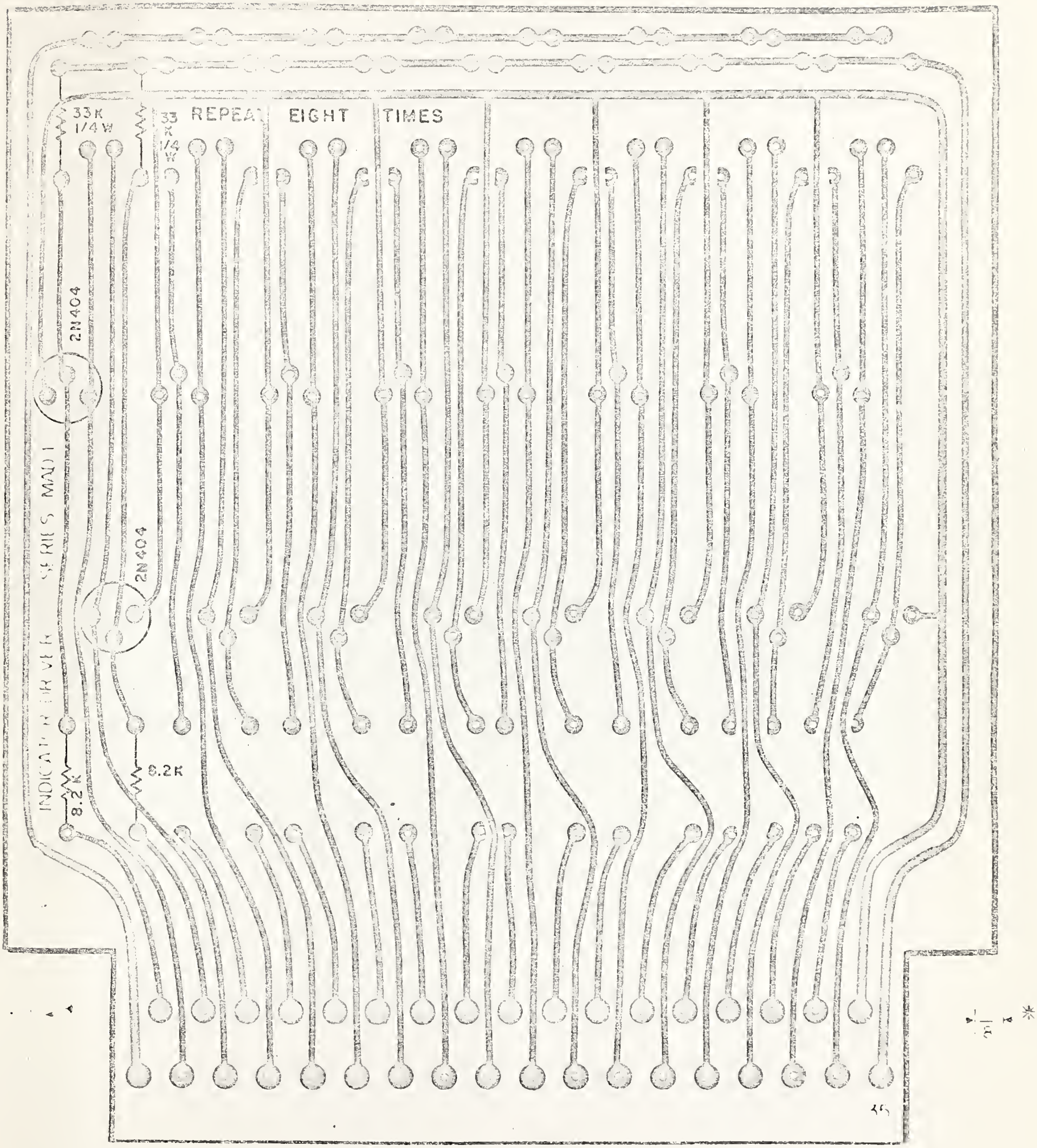
FIGURE 31. INDICATOR/AMPLIFIER SERIES MAD-I USED AS AN INDICATOR DRIVER



NOTES:

ALL TRANSISTORS 2N404
8.2K RESISTORS 1/2 W.
33 K RESISTORS 1/4 W.
* THESE RESISTORS REQUIRED ON CIRCUITS USED AS AMPLIFIERS. (USUALLY 620 Ω)

FIGURE 32. INDICATOR / AMPLIFIER



* MIN. PERMISSIBLE SPACE FROM EDGE OF CONDUCTOR TO EDGE OF BOARD

FIGURE 33.

FIGURE 34.

h. Universal Counter

Logical Function. Counts input pulses in any radix (number base), up to 15 and stores the count.

Circuits per Card. One

Input Load. Two pulse gates for data, one pulse gate for reset input.

Fan-Out. From register storing count: Three logic gates and/or five pulse gates.

From reset/carry line: Five logic gates and/or twenty-five pulse gates.

Power Requirements. -12 volts: 120 ma.
+12 volts: 5 ma.

Logic Diagram. Figure 35 shows the logic diagram and pin numbers.

Logical Application. Most counter cards are set to count in only one radix or number system. A decimal card, for example, will count to 9 and then reset. This card will count to any number up to 15 before resetting, and the number can be set with jumpers on the card. At the end of the count, a 4-microsecond long pulse with a fan-out of 25 gates is emitted from the "carry out" line. A reset input permits premature resetting of the stored count. In addition to the reset output, the contents of the count register are also available. Multi-stage counters are simplified by the presence of the special carry line for cascading.

Input Signal Requirements. Positive level: 0 volts to -0.2 volts.
Negative level: -6 volts to -12 volts
Input impedance: .001 microfarad to ground.
Minimum dv/dt: 6 volts per microsecond.
Minimum pulse width: 4 microseconds.

Output Signal Characteristics.

I. Stored value outputs. Positive level: 0 volts to -0.2 volts.
Negative level: -6 volts to 12 volts.
Output impedance: Positive level: Through saturated transistor to ground.

Negative level: 620 ohms to -12 volts.

II. Reset/carry line output: Pulse

Positive level: 0 volt to -0.2 volt.

Negative level: -12 volts.

Pulse duration: 4 microseconds.

Pulse polarity: Positive going from the negative line level.

Minimum dv/dt: Rise: 60 volts per usec.
Fall: 6 volts per usec.

Output impedance: 0.3 ohms to ground.

Circuit Description. The schematic diagram is shown in Figure 36.

This is a simple, four stage binary counter consisting of four T-input flip-flops, wired in cascade. A gate circuit on the pulse input looks at the contents of the counter. When these contents reach the value set by the patching on the rear connector, the next pulse is prevented from reaching the counter input, and is instead diverted to trigger a four microsecond one-shot which resets the counter by grounding the collectors on the "0" side of each flip-flop through suitable isolating diodes. This output is available to trigger flip-flops or other counters. An extra input directly to the one-shot allows resetting of the counter at any time.

Application Notes. To set the radix of the counter, jumpers should be placed on the rear connector as shown in the logic diagram, Figure 35. An output from each counter stage representing the binary value of the counter is available on the pins shown. THESE OUTPUTS SHOULD NOT BE USED FOR ANY LOGIC EXTERNAL TO THE COUNTER CARD. Subtract one from the binary value of the desired radix and patch this into the pins labelled "AND gate inputs".

Trouble Shooting. The following table lists some troubles that may be encountered and suggests probable causes and remedies.

Symptom	Cause	Remedy
Counter will not count.	Reset pulse occurring on every input pulse.	Check "AND" gate patching.
Counter will not count.	Reset pulse occurring on every input pulse.	Shorted gate transistor - replace.
Counter will not count.	Insufficient input dv/dt.	This card is more susceptible to this problem than many. Increase dv/dt with comparator card or high-impedance amplifier.

Construction Information. Figure 37 shows the component layout. The following table lists the parts necessary for construction.

Quantity	Item
10	2N404
1	2N659
19	DR435
7	Test Jacks
9	33k 1/4-watt Resistors
1	33k 1/2-watt Resistors
9	620 ohm 1/2-watt Resistors
11	3.9k 1/2-watt Resistors
1	3.9k 1/4-watt Resistors
9	5.1k 1/4-watt Resistors
2	1k 1/2-watt Resistors
10	0.001 uf Capacitors
8	200 or 220 pf Capacitors
2	500 pf Capacitors
	Transipads and Circuit Board
11	Jumpers

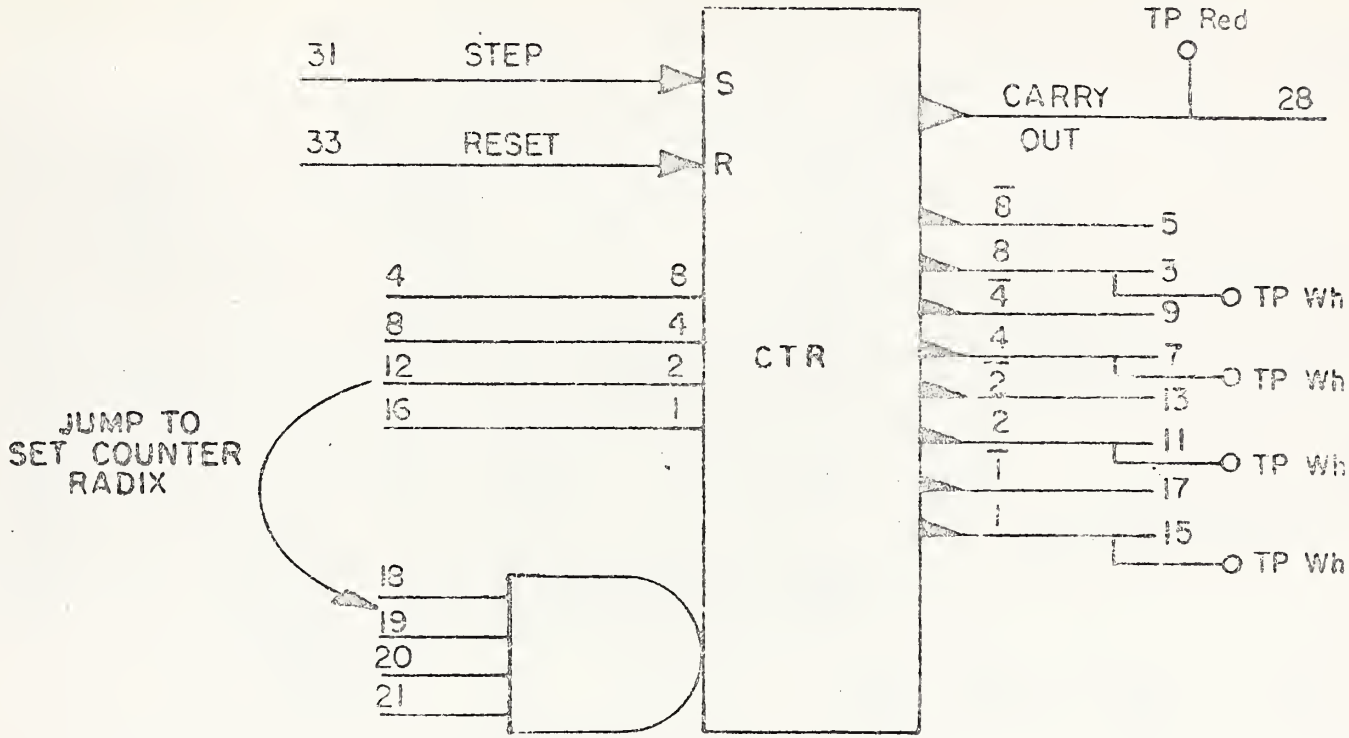


FIGURE 35. UNIVERSAL COUNTER SERIES MAD-1

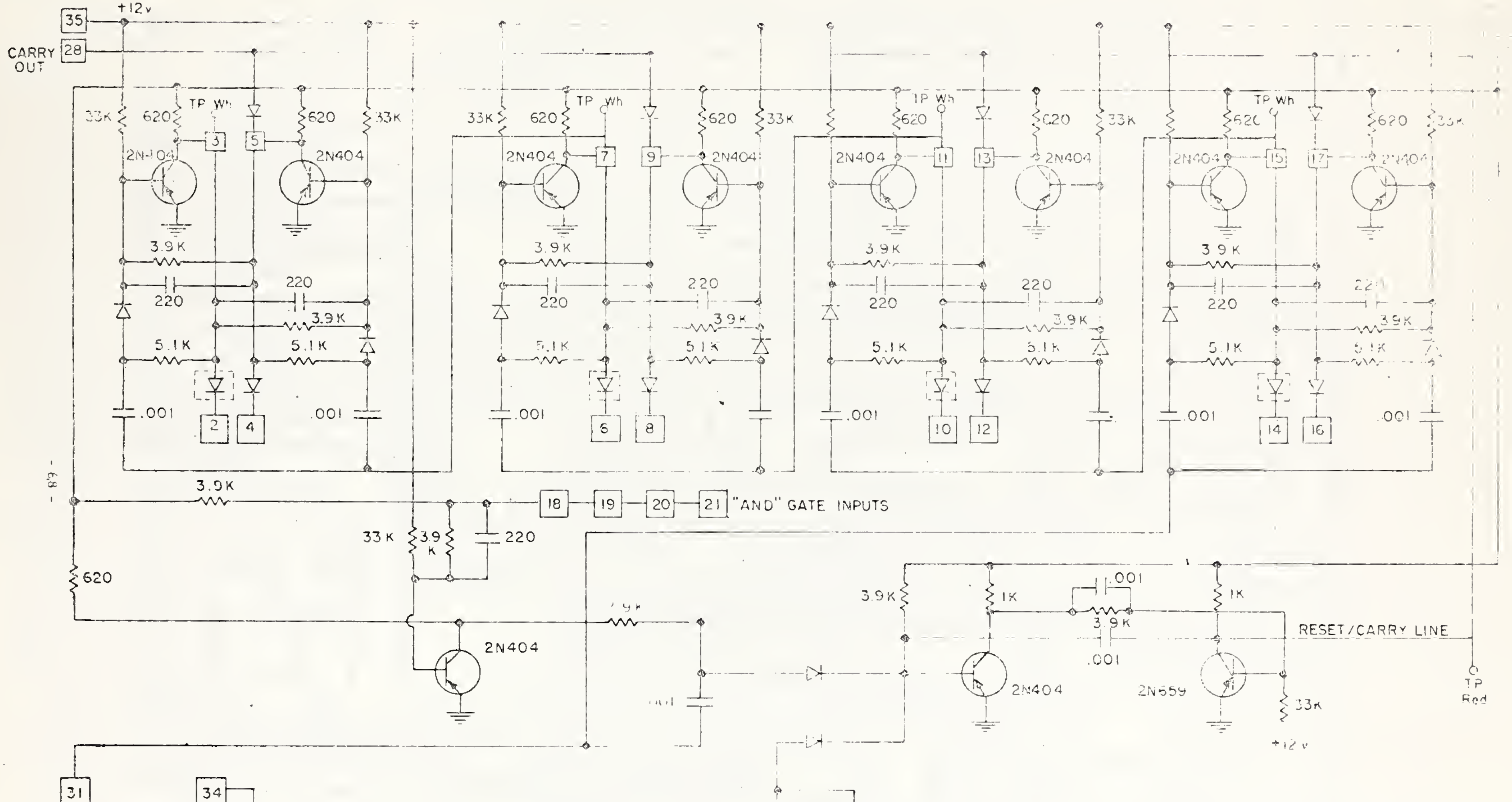
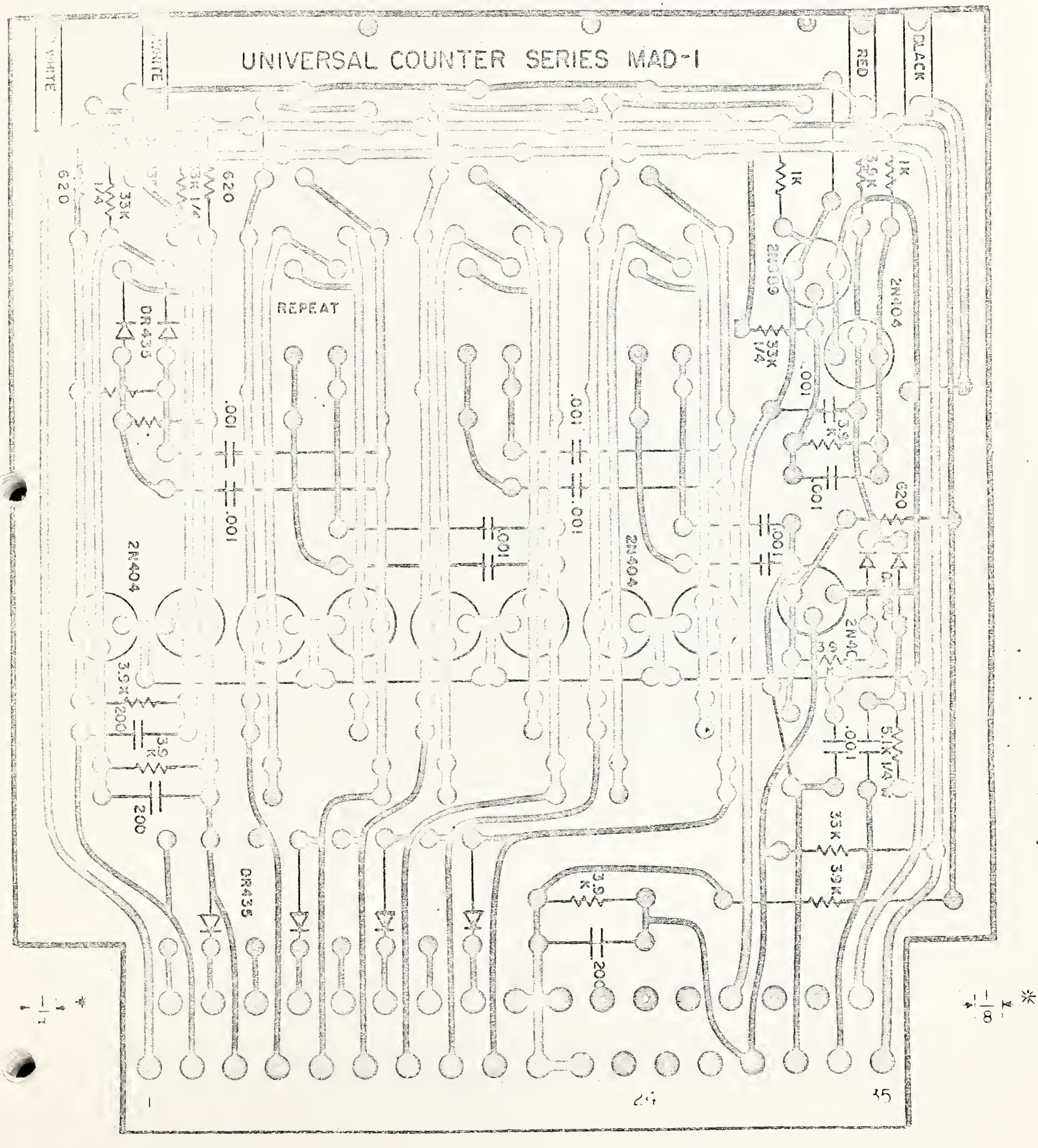


FIGURE 36 UNIVERSAL COUNTER SERIES MAD-1

NOTE: ALL DIODES DR435
ALL RESISTORS 5%
COMPONENTS IN DASHED SQUARES ARE NOT INSTALLED BY MFGR



* MIN. PERMISSIBLE SPACE FROM EDGE OF CONDUCTOR TO EDGE OF BOARD

FIGURE 38.

i. 16 X 16 Matrix

Logical Function. This card is a convenient board on which diodes, resistors, or other components may be mounted. It is laid out to permit connecting up to 16 input lines to any, some, or all of 16 output lines.

Card Layout. Sixteen by sixteen square matrix.

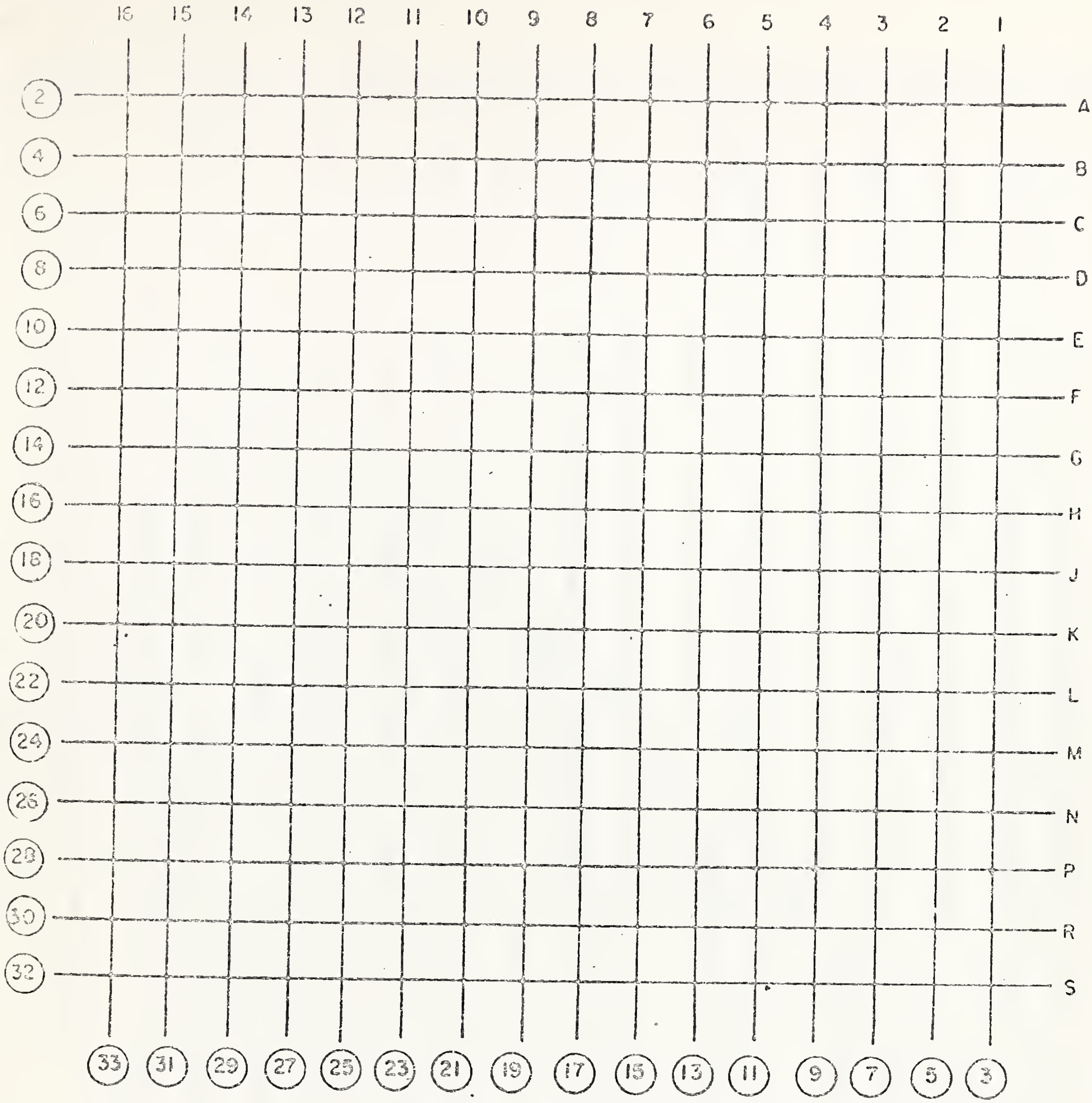
Logic Diagram. Figure 39 shows the logic diagram and pin numbers. This diagram is so designed that copies of it may be used to indicate the component layout used in any given application.

Logical Application. A matrix may, as an example, be used for converting data from one code format to another. A 16 X 16 matrix, in conjunction with amplifiers, may be used to assemble up to 16 characters as unique combinations of up to 16 lines. In other applications, it may be used to mount diodes for large AND or OR gates, and an amplifier placed at the output to restore logical levels.

Circuit Description. Components as desired are mounted on the board with their major axis perpendicular to the card. Horizontal lines are on the top of the card, vertical ones on the bottom. The lines on top are brought electrically through the board with eyelets, and from there to the connector. One lead of each component is soldered to the conductor on the top of the board as the lead passes through. The other lead is soldered to a conductor on the bottom of the board.

Trouble Shooting. Solder joints on the bottom of the board sometimes overflow the boundaries of the printed conductor and short to adjacent conductors. (Some close spacing exists in various places.) Inspection with a magnifying glass generally reveals otherwise mysterious short circuits.

Construction Information. Figure 40 shows the conductor layout of the bottom side of the cards. There are no components supplied, as these vary with application.



MODULE ______________________

CARD LOCATION ________________

FUNCTION ______________________

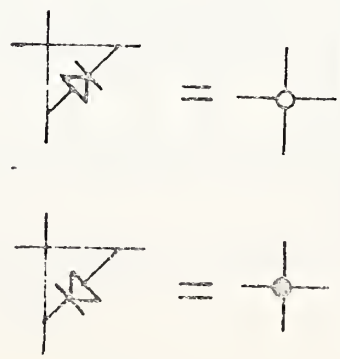
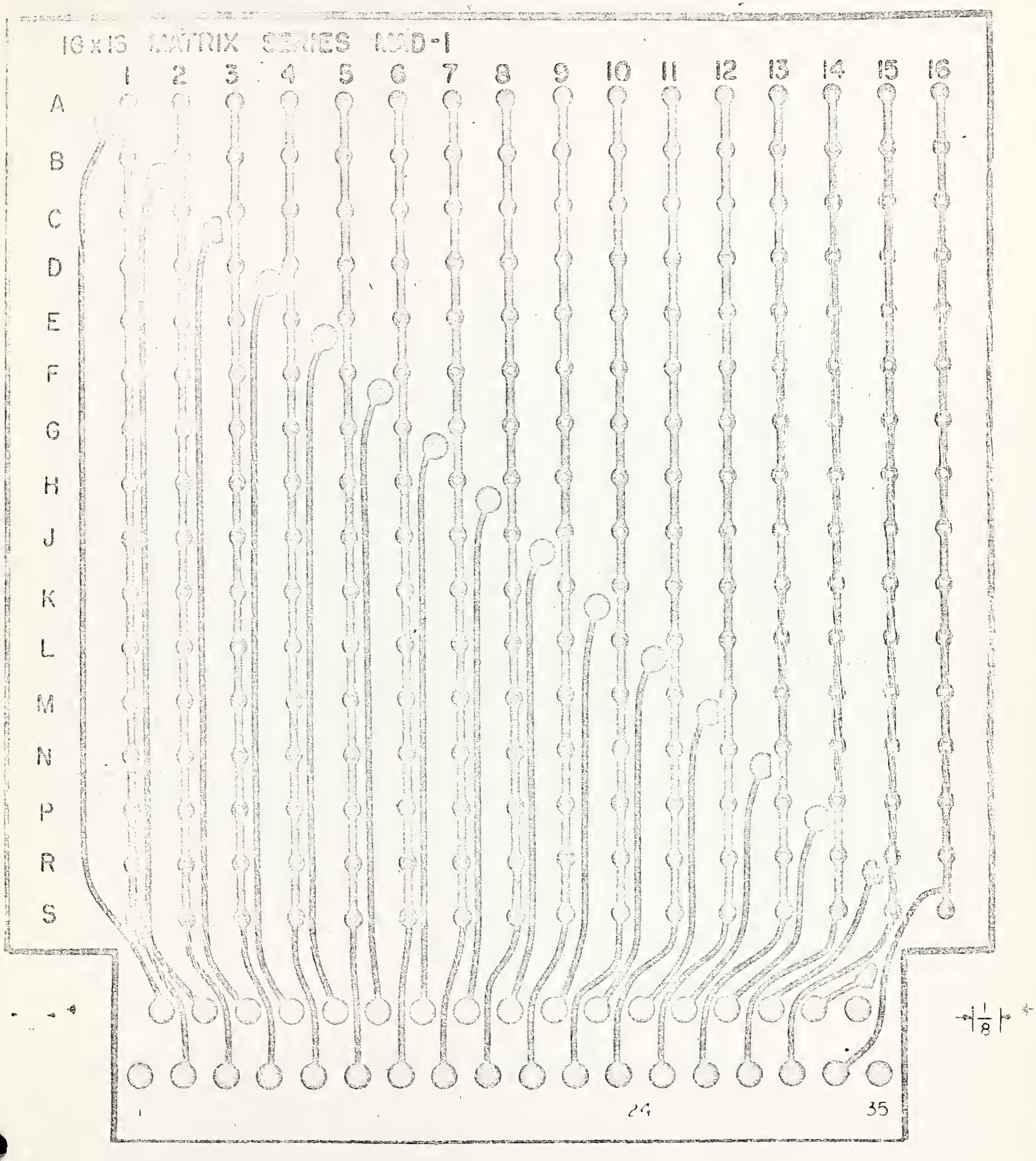


FIGURE 39. 16 x 16 MATRIX SERIES MAD-1



* MIN. PERMISSIBLE SPACE FROM EDGE OF CONDUCTOR TO EDGE OF BOARD

FIGURE 40.

FIGURE 41.

j. Coil Driver

Logical Function. The coil driver provides a means of switching the current in devices requiring up to 1 1/2 amperes of current, with control supplied by ordinary logic levels. The controlled device should have its own power supply.

Circuits per Card. Five.

Input Load. One standard logic gate.

Fan-Out. Not applicable in the normal sense. See Logical Application.

Power Requirements. -12 volts: 12ma for each energized circuit.

+12 volts: 12ma at all times.

Logic Diagram. Figure 42 shows the logic diagram and pin numbers.

Logical Application. This package was originally intended for driving the magnets associated with a paper tape perforator, such as the Teletype BRPE. It is still used in this application, and has found further use driving relays and other high current devices. It is also used to control logic circuits where a line capable of handling large logic currents must be grounded.

Input Signal Requirements. Positive level: 0 volts to -0.2 volts.
Negative level: -6 volts to -12 volts.
Imput impedance: 3900ohms sink to ground shunted by 220pf (standard AND inverter).

Output Signal Characteristics. Positive level: 0 volt at approximately 0.2 ohms (saturated transistor)

Negative level: Depends on external supply. Maximum allowed: -60 volts.

Maximum current capacity to ground:
Absolute maximum: 3.5 amperes
Recommended maximum: 1.5 amperes.

Circuit Description. The circuit diagram is shown in Figure 43. A standard NAND gate is used to drive an intermediate and a power transistor wired in a modified Darlington configuration. The 2N1039 transistor is rated for operation at 3.5 amperes collector current, with a maximum voltage of 60 volts. The heat dissipation facilities on the card in free air are not adequate to maintain a safe junction temperature at this current. Therefore

recommended current is 1.5 amperes per circuit. Since considerable power is dissipated during the transitions from cutoff to saturation and vice-versa, further derating of current carrying capacity should be done at frequencies above 1000 cycles per second. Percentage of "on time" (duty cycle) is not limited.

An arc suppressor diode is brought from the collector of each transistor to a point which should be connected to the common negative terminal of the power supply if the load contains inductive components.

Trouble Shooting. The following table lists some troubles that may be encountered and suggests probable causes and remedies.

Symptom	Cause	Remedy
Output remains grounded.	Shorted 2N1039 or 2N398.	Replace and check 1N2069
Output will not go to ground.	Shorted 2N404.	Replace
Interferes with operation of other cards wired to it.	Shorted DR435.	Replace

Construction Information. Figure 44 shows the component layout of the card and the table below lists the required components.

Quantity	Item
5	2N1039
5	2N398
5	2N404
5	1N2069
10	DR435
5	Test Jacks
5	Wakefield NF205 Dissipators, for 2N1039's
5	10k 1/4-watt Resistors
10	33k 1/4-watt Resistors
5	3k 1/4-watt Resistors
5	3.9k 1/4-watt Resistors
5	1k 1/2-watt Resistors
5	220 (or 200)pf Capacitors
5	500pf Capacitors
6	Jumpers
	Transipads and Circuit Board

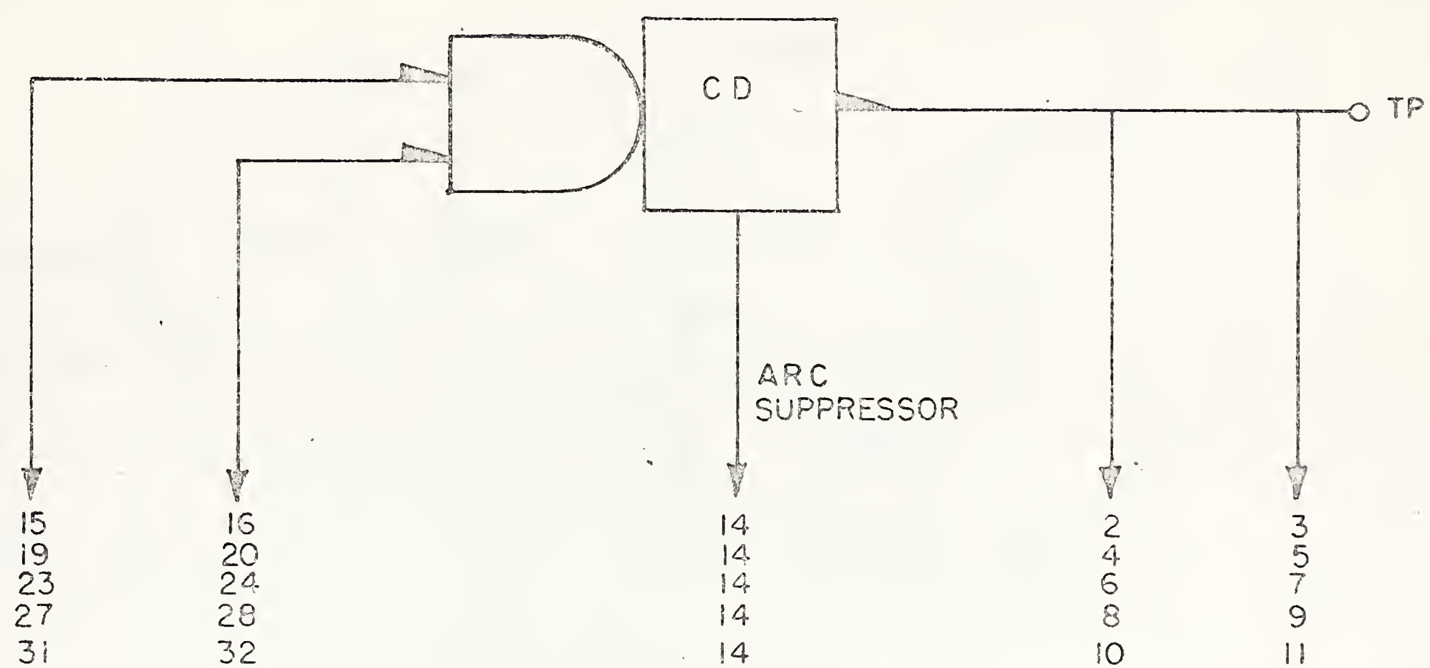
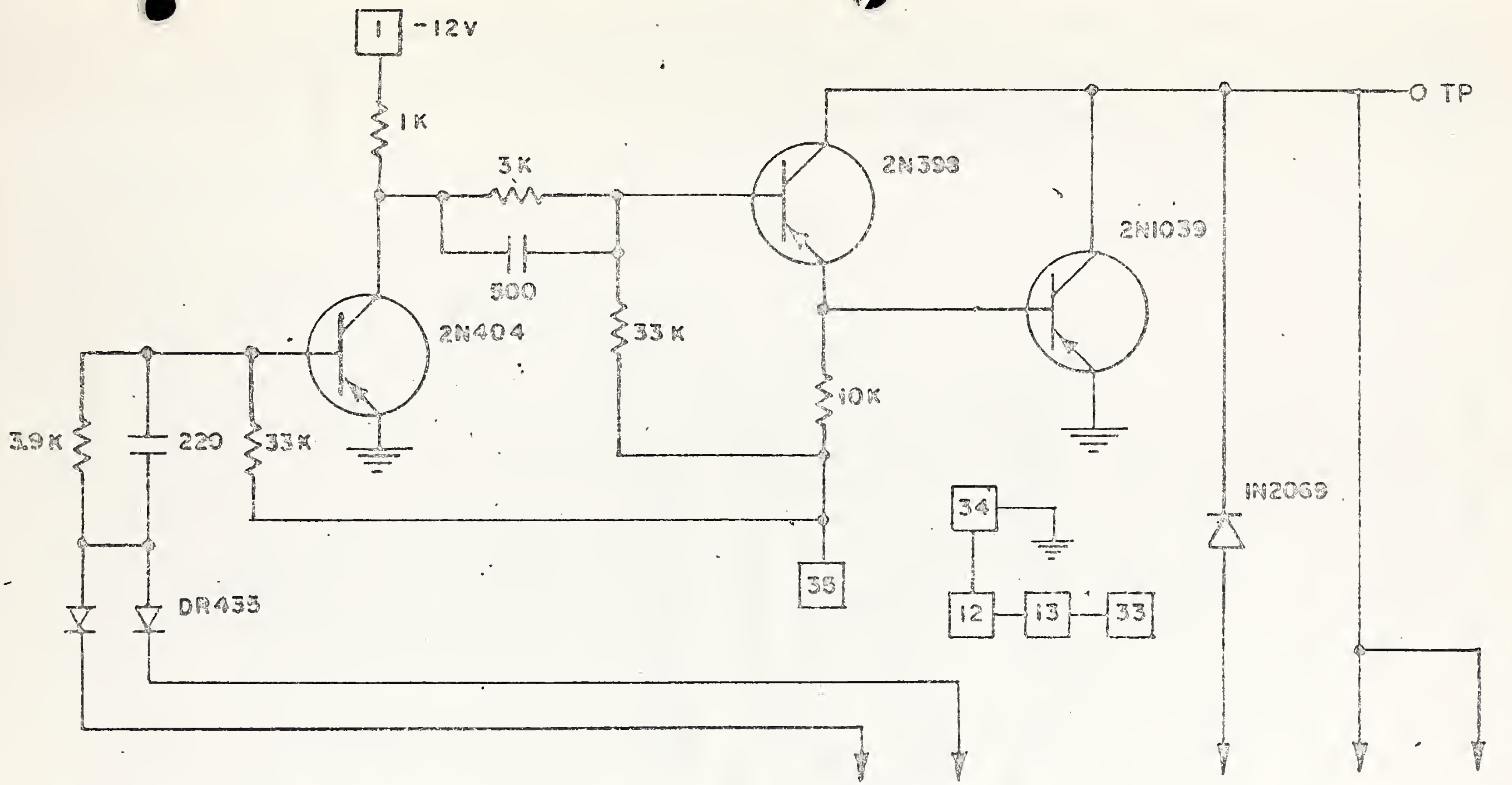


FIGURE 42 COIL DRIVER SERIES MAD-1



CIRCUIT No.	INPUT	STROBE	SUPPRESSOR	OUTPUTS	
1	15	16	14	2	3
2	19	20	14	4	5
3	23	24	14	6	7
4	27	28	14	8	9
5	31	32	14	10	11

FIGURE 43. COIL DRIVER SERIES MAD-1

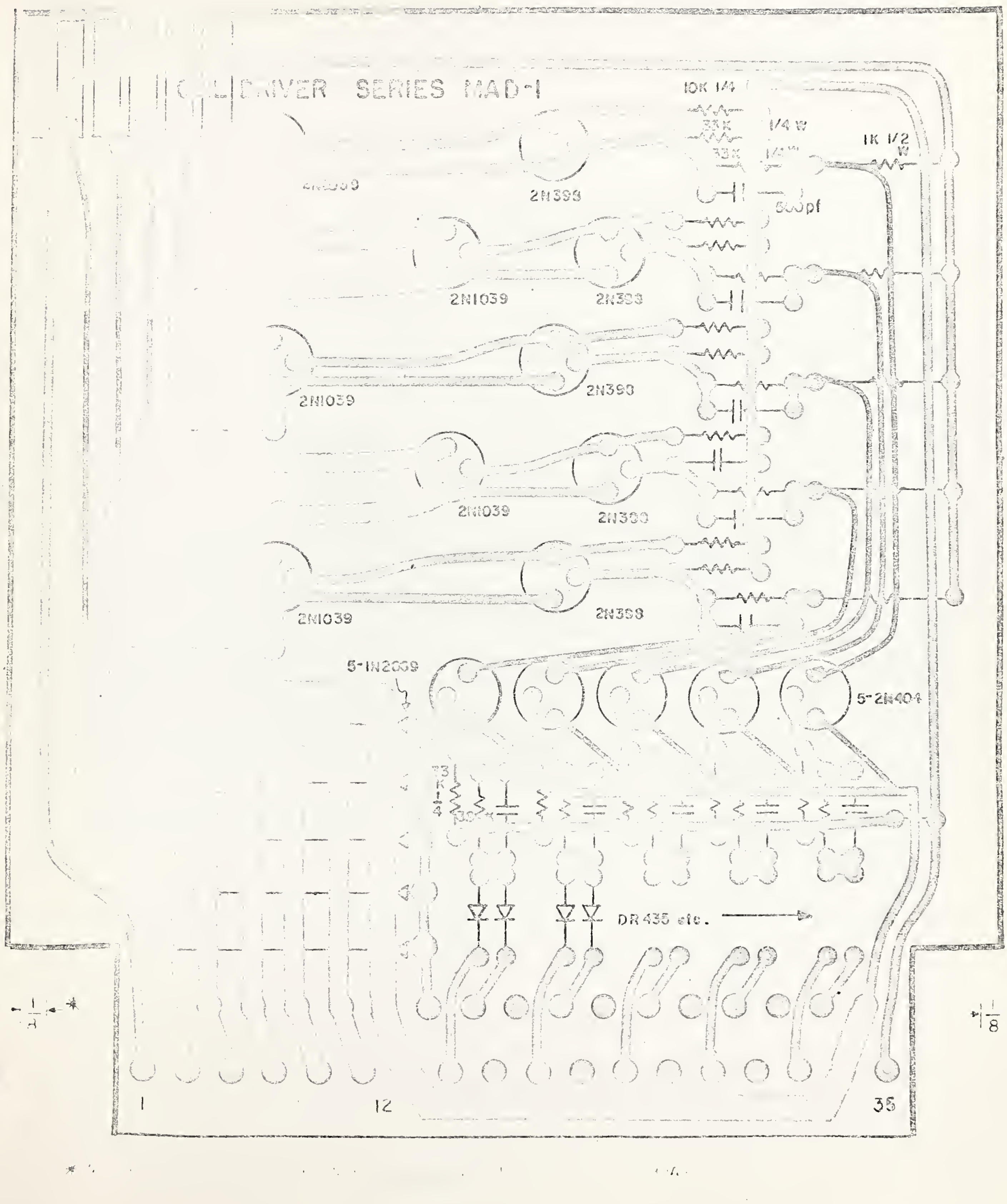

DRIVER SERIES MAD-1
10K 1/4
33K
1/4 W
1K 1/2 W
500pf
2N393
2N1039
5-1N2069
5-2N404
DR 435 etc.
1
12
35
1/8

FIGURE 44.

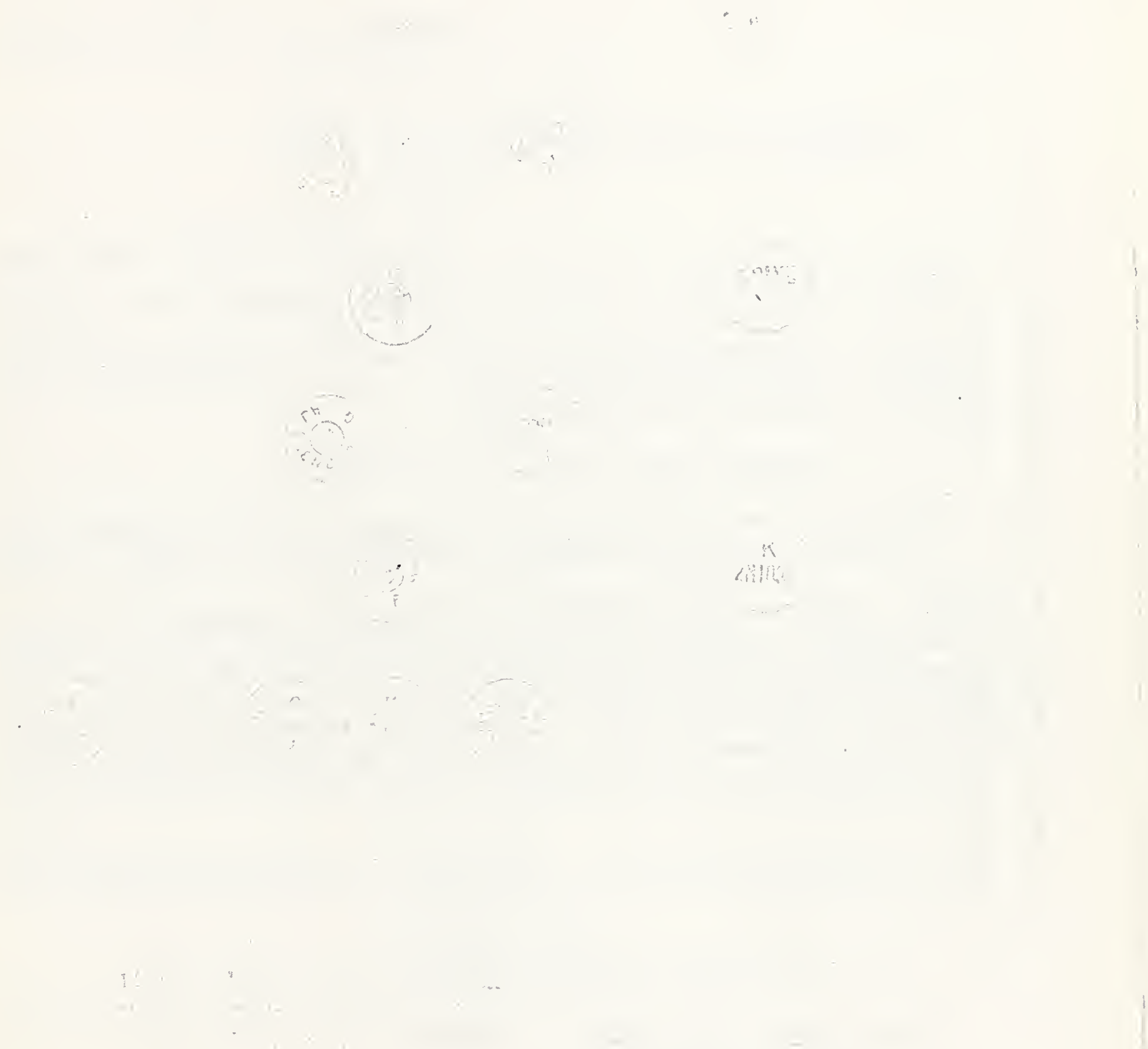


Figure 45.

k. Comparator/Gate

Logical Function. The comparator section sets or resets a flip-flop depending on whether an analog input voltage is more positive or more negative than a reference input. The gate section is two standard AND-OR inverter circuits.

Circuits per Card. Two comparators.

Two three-input gates.

NOTE: detailed information about the gates may be found in the section on the AND/OR inverter.

Input Load. Analog voltage input.

Fan-Out. Four standard logic gates and/or five standard pulse gates.

Power Requirements. -12 volts: 40 ma per comparator, plus 20 ma for each gate output at 0 volt. 10 ma for each gate output at -6 volts.

+12 volts: 20 ma for each comparator.

Logic Diagrams. Figure 46 shows the logic diagram for the comparator section. Figure 47 shows the logic diagram for the gate section.

Logical Application. Whenever a non-standard signal, such as a contact closure or pulse from a magnetic pickup will be used as a logic signal, this circuit will "square it up" and provide completely compatible levels and rise-times. For timing applications, it is useful for squaring the output of sine wave oscillators. A reference level is established either with the internal trimpot or externally. Crossings of this level by the analog input signal cause a change of state of the output flip-flop.

Input Signal Requirements. Analog input: Any voltage between -12 and +12 volts.

Any wave shape.

Any frequency up to 100 kc.

Impedance: 10,000 ohms at dc.
1,500 ohms at 100 kc.

Reference input: Any dc voltage between +12 volts and -12 volts.
Impedance: 10,000 ohms.

Input hysteresis: 0.01 volts at dc.
0.06 volts at 100 kc.

Output Signal Characterisitics. Positive level: 0 volt to -0.2 volt.

Negative level: -6 volts to -12 volts.

Minimum dv/dt: 6 volts per microsecond.

Circuit Description. The circuit diagram is shown in Figure 48.

Normally, a Schmitt trigger circuit would be used in this application. Such a circuit will sometimes display the difficulty that, over a small region near the transition point, the output follows the input signal. This would not guarantee a minimum rise time. For this reason, the classic Schmitt circuit has been modified for this card.

The input signal is resistively mixed with the reference input to produce a single d-c level. This level is applied to an amplifier with a gain of 10 and a d-c reference of +4 volts. The output of this drives a complementary inverted emitter-follower for increased current gain. This stage can either inject current into or rob current from the base of the first flip-flop transistor, changing its state. Two parallel reversed diodes provide conduction except around 0 volts, where the impedance of the combination increases, thus decoupling the flip-flop from the amplifier.

Trouble Shooting. The following table lists some troubles that may be encountered and suggests probable causes and remedies.

Symptom	Cause	Remedy
Output will not change state.	Input d-c level not crossing trigger point.	Jumper E_{ref} from trimpot to reference input. Adjust for proper operation.
Output will not change state.	Shorted flip-flop transistor.	Replace.
Circuit oscillates.	Shorted DR435 in decoupling.circuit.	Replace.

Construction Information. Figure 49 shows the component layout of the card and the table below lists the required components.

Comparator/Gate Card

Single Clad.
Regular Dimensions.
No Special Instructions.

Quantity	Item
8	2N404
2	2N1302
10	DR435
2	Wakefield NF205 Heat Dissipators (for 2N1302's)
6	Test Jacks
2	10k ohm Trimpots
6	3.9k Resistors
8	620ohm Resistors
4	33k 1/4-watt Resistors
2	2k Resistors
2	15k Resistors
2	1k 1/4-watt Resistors
2	3k Resistors
4	10k 1/4-watt Resistors
2	10k 1/2-watt Resistors
2	.001uf Capacitors
4	200 (or 220) pf Capacitors
2	500pf Capacitors
	Transipads and Circuit Board

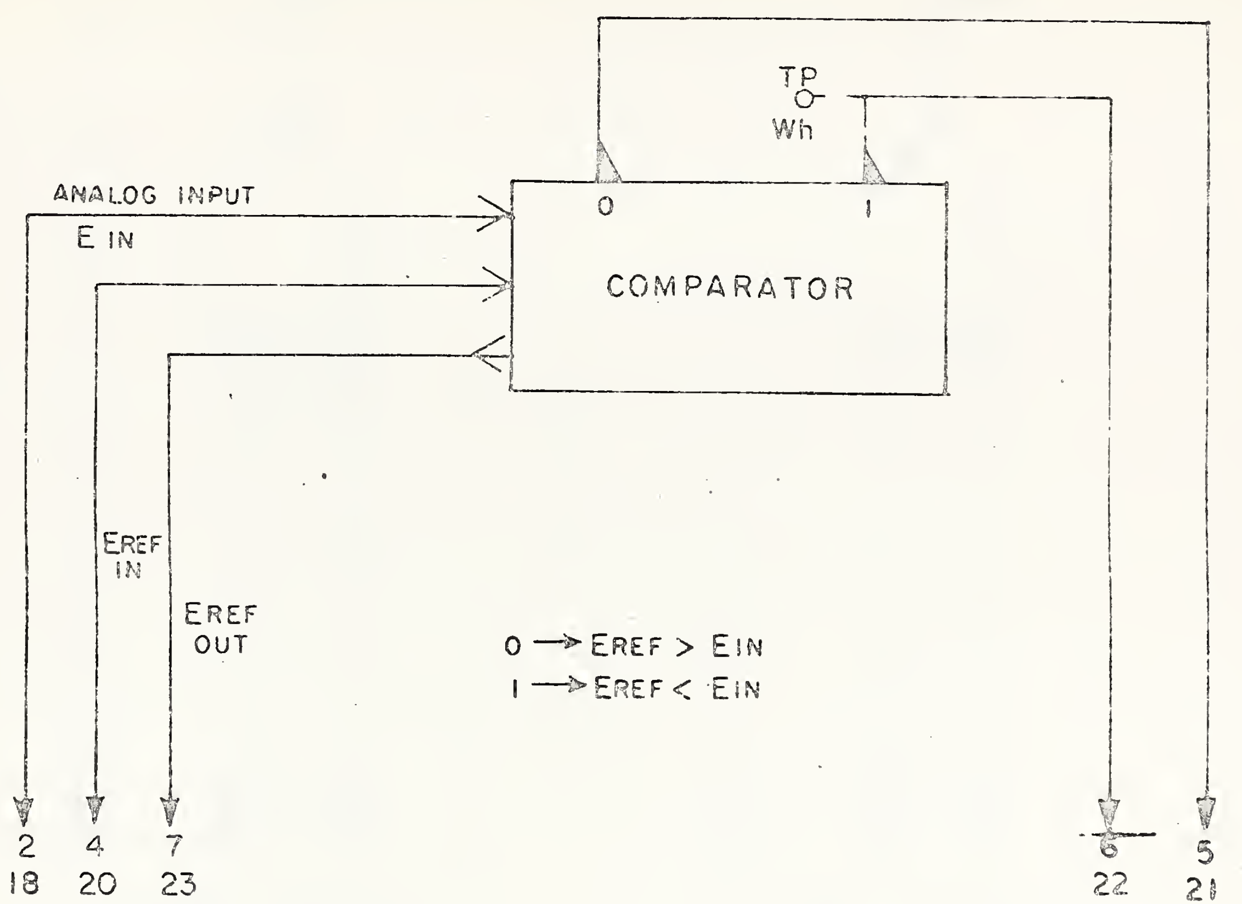
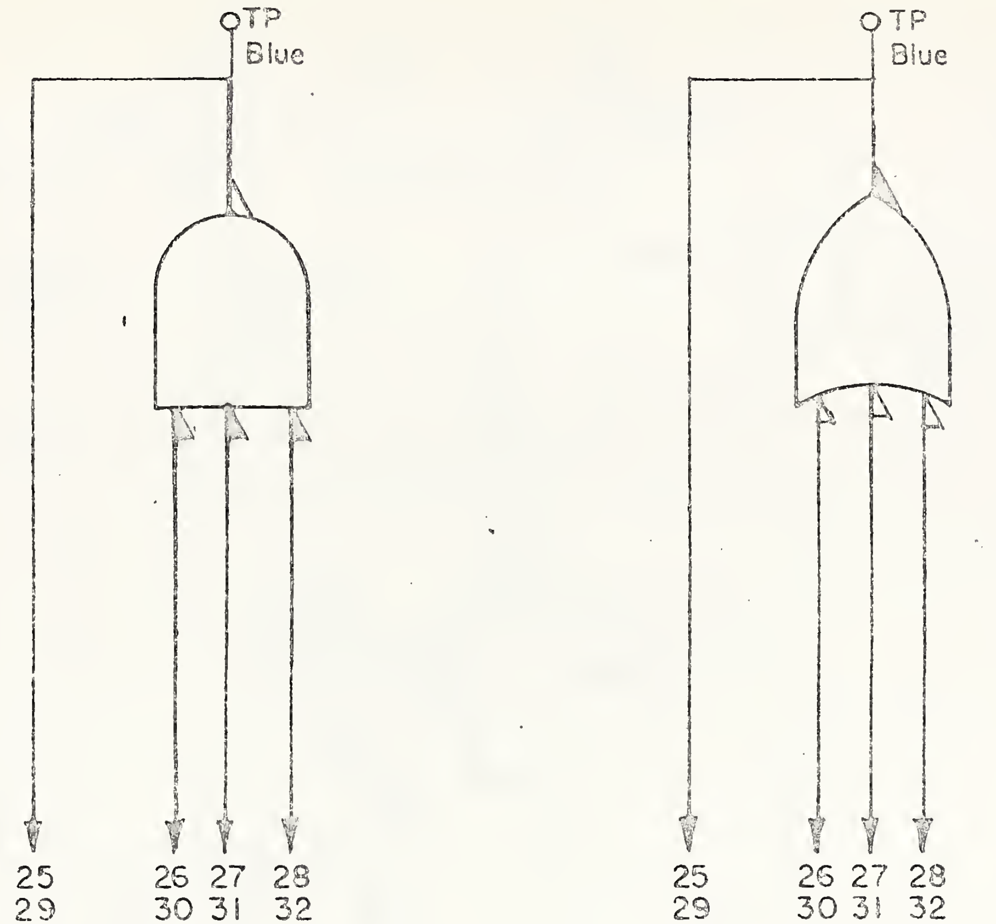


FIGURE 46. COMPARATOR/GATE SERIES MAD-1 COMPARATOR SECTION



AS NAND CIRCUITS AS NOR CIRCUITS

FIGURE 47. COMPARATOR / GATE SERIES MAD-1 GATE SECTION

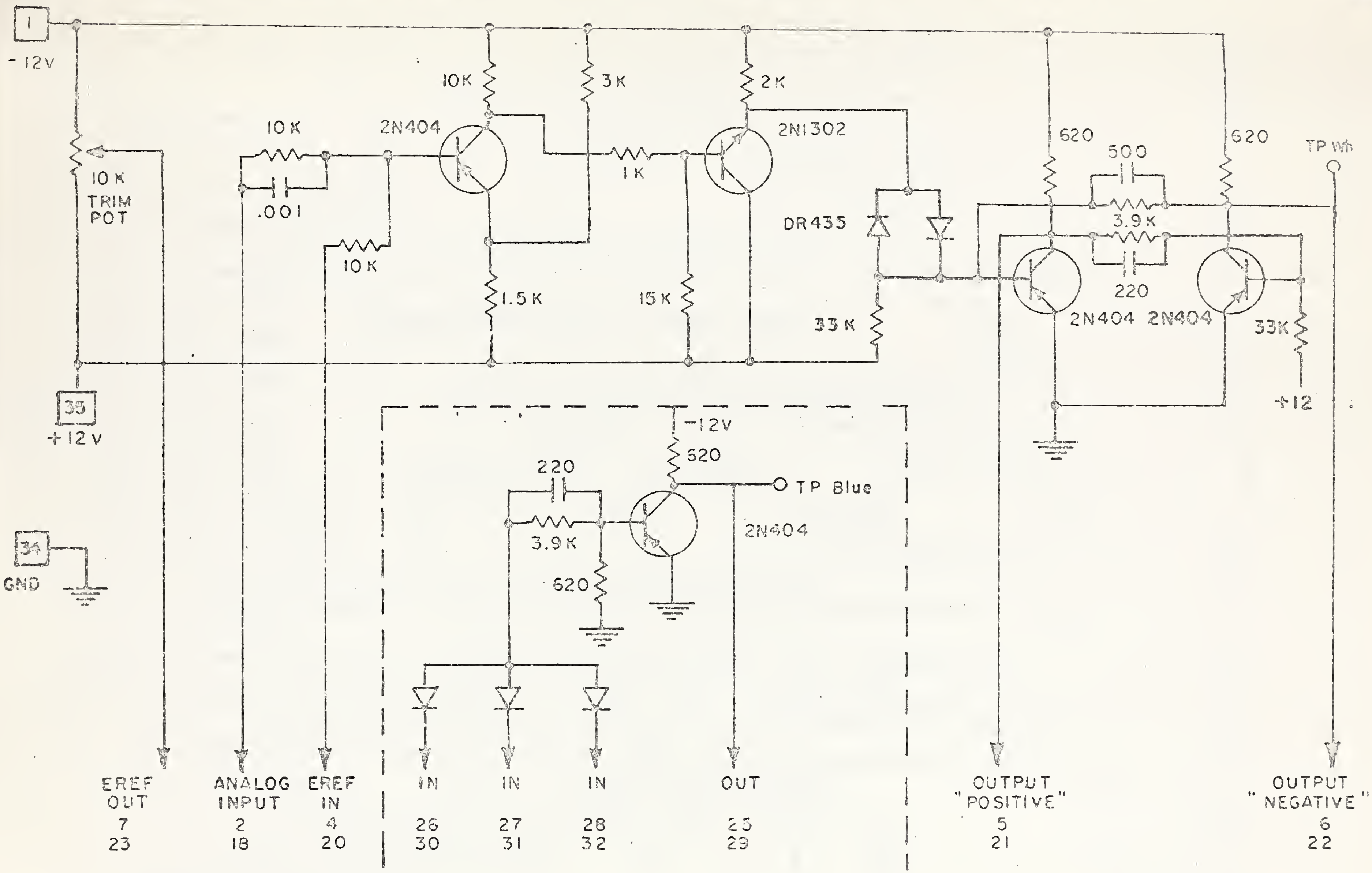
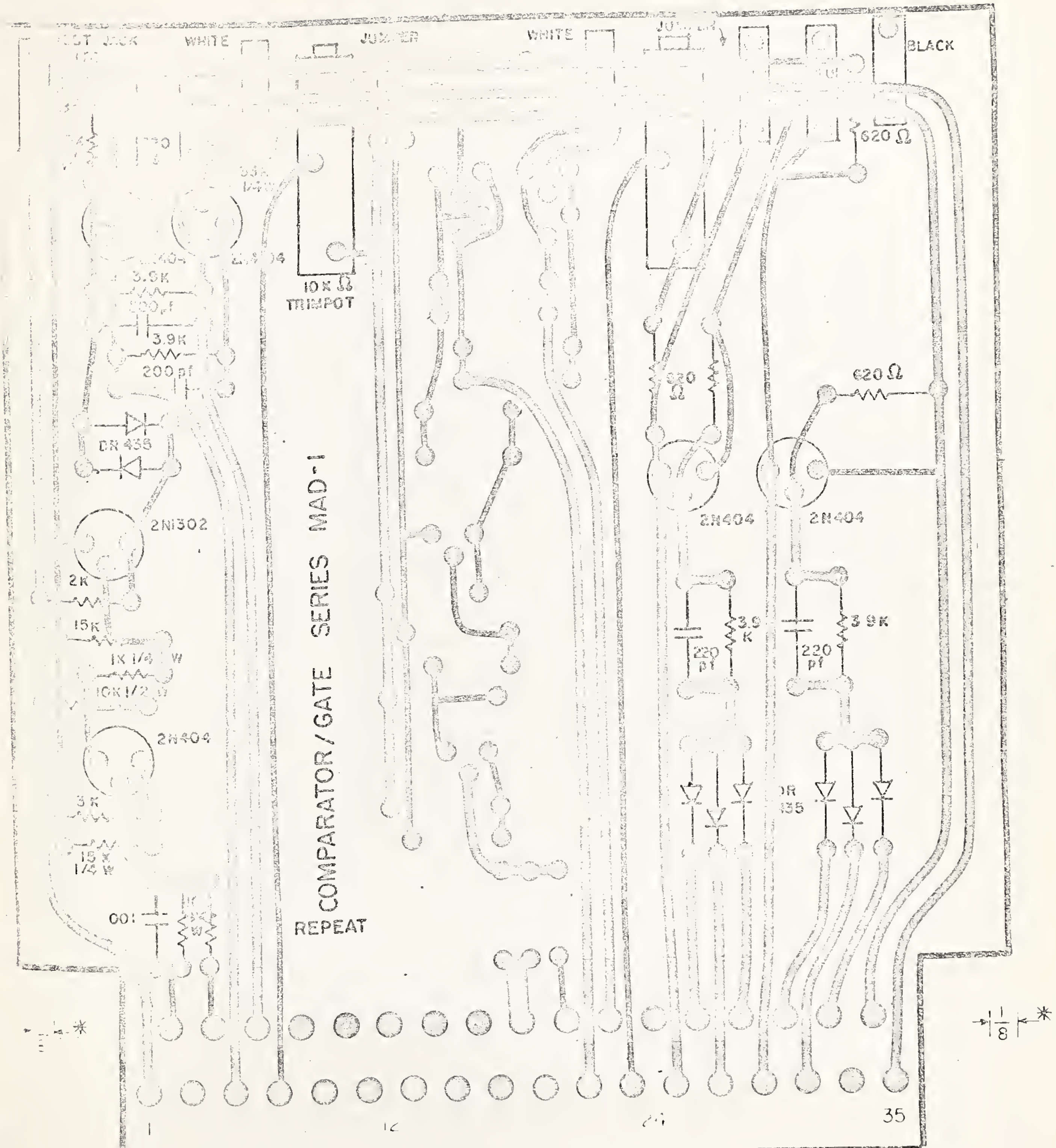


FIGURE 48. COMPARATOR / GATE SERIES MAD-1



∗ MIN. PERMISSIBLE SPACE FROM EDGE OF CONDUCTOR TO EDGE OF BOARD

FIGURE 49.

FIGURE 50.

1. Ripple Register

Logical Function. This card serves as one stage of a four-bit-per-character shift register, or as one stage of a self-shifting register known as a ripple register.

Circuits per Card. One, providing all necessary logical functions, including visual indication.

Input Load.	Data inputs par. and ser. also reset C.	Load input	Sense input	Clock input	$\bar{C}$ in
Pulse gates	1 ea.	5 ea.	0	0	1
Logic gates			1 inverted	1	1

Fan-Out.	Data outputs par. and C out	Sense output
Pulse gates	5	5
Logic gates	4	3

Power Requirements. -12 volts: 140ma.

+12 volts: 5ma.

Logic Diagrams. Figure 51 shows the diagram used to symbolize the circuit when used in applications. Figure 52 shows the internal logic of the card.

Logical Application. A ripple register is a self-shifting register. Data may be loaded into any point, and it will automatically shift until it assumes a position adjacent to previously loaded data. In order that the register be logically able to distinguish a true data character from an empty stage, a special control bit is attached to each stage. If this bit, stored in an integral flip-flop, is a logical 1, the character is valid. If this bit is zero, the stage does not contain data, and previous stages are instructed to shift true data down to fill up empty positions.

Input Signal Requirements. Positive level: 0 volts to -0.2 volts.

Negative level: -6 volts to -12 volts.

Minimum dv/dt: 6 volts per microsecond.

Input impedance: as follows -

Data inputs par. and ser. also C in	Sense in	Clock in	Load	Reset C
5100 ohms	3900 ohms 220 pf	3900 ohms 220 pf	0.005 uf to ground	.001 to ground

Output Signal Characteristics. Positive level: 0 volts to -0.2 volts.
Negative level: -6 volts to -12 volts.

Circuit Description. The circuit diagram is shown in Figure 53.

Data: Four flip-flops on each card are wired in a standard shift-register configuration. These flip-flops may be loaded with parallel, complementary data from an external source. The gates for this are mounted on the card. A common load line pulses all of these gates at once. During shifting, other gates (also on the card) receive a shift pulse from the card's control logic section. These pulses load the data from the previous stage into the stage in question, thereby producing a shift.

In the collector circuit of each data transistor is a No. 80 Brite-eye lamp, bypassed with a 220-ohm resistor. This light is mounted in a black shading bracket at the end of the card. The bracket is designed to mount flush with the front panel of the module in which the card is mounted, and therefore serves as an indicator showing the contents of the register. The lamp is rated at 3 volts, 8 ma. The bypass resistor allows operation to continue unaffected if the bulb burns out.

The data input and output terminals of the data section are wired so that putting groups of these cards in a register is considerably simplified. A uniform manner of wiring, very simple in production and trouble shooting, is thereby insured.

Control: One flip-flop is used to store the control bit that indicates to the module logic whether or not the contents of the card are valid. This bit is set to 1 when a character is loaded. In order to indicate to the card that a valid character is being loaded, the resistor labeled SET C is grounded, and the load bus is then pulsed. (If valid characters will always be loaded, the resistor may be wired to ground.) This gates the load pulse into the flip-flop, and C is set. A shift pulse shifts the contents of C, complemented, to the C bit of the next card down the line, and loads the C bit from the previous card.

A line called the SENSE line goes through each card. The purpose of this is to report to the card the fact that there are points downstream in the register where an invalid character is stored. This fact causes a shift. The sense line coming from downstream is wired to the SENSE IN terminal, where a reversed OR gate (for positive levels) OR's it with the contents of C. This is then inverted twice (once for logical

reasons, once to maintain levels), and is then sent out to SENSE OUT to go to the next card. The next card, therefore, sees a positive sense line if <u>any</u> card downstream from it is empty.

If the sense line in a given card is positive, it indicates that a shift is necessary. The sense line is therefore used to open a regular AND-inverter gate, which allows the next module clock pulse to generate a shift pulse in the card. Only those cards upstream from an invalid character will shift at this time.

When the module is being used as a serializing register, it is necessary to cause a shift after the last character in the register has been used by the system. This is done by externally pulsing the RESET C gate of this character. This immediately "annihilates" the character by making the logic consider it invalid. The register shifts on the next clock pulse.

<u>Trouble Shooting</u>. The following table lists some troubles that may be encountered and suggests probable causes and remedies.

Symptom	Cause	Remedy
Register does not display proper contents.	Burned-out No. 80 lamp.	Replace.
Register does not display proper contents.	Not loading properly.	Check rise-time of load pulse.
Register does not display proper contents.	Shorted transistor in data flip-flop.	Replace.
Register does not display proper contents.	Valid character bit not loaded.	Ground SET C terminal.
Register stops rippling at defective stage.	Shorted transistor in SENSE line.	Replace.
Register stops rippling at defective stage.	Proper negative-going clock pulse not arriving at card.	Check and repair.

Construction Information. Figure 54 shows the component layout on the circuit board. Figure 55 is a mechanical drawing of the lamp bracket holding the indicators. The table below lists the required component.

Quantity	Item
4	Cal-Glo No. 80 Lamp and Brite-Eye C Holders
14	2N404
24	DR435
1	Test Jack
14	33k 1/2-watt Resistors
7	620 ohm Resistors
4	470 ohm Resistors
22	5.1k Resistors
13	3.9k Resistors
3	1k Resistors
4	220 ohm Resistors
20	0.001 uf Capacitors
13	220 pf Capacitors
	Transipads and Circuit Board
1	Lamp Bracket

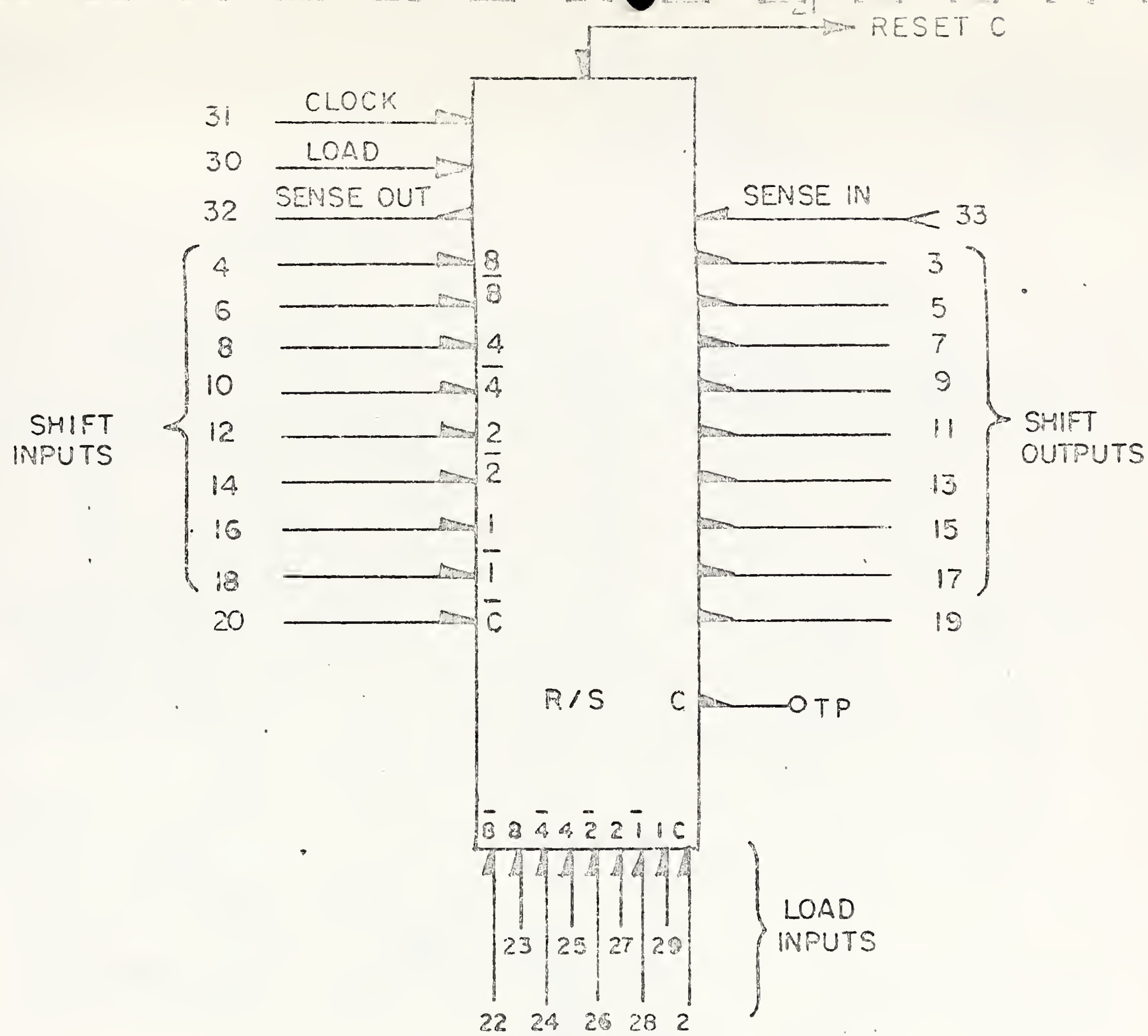


FIGURE 51: RIPPLE SHIFT REGISTER CARD SERIES MAD-1

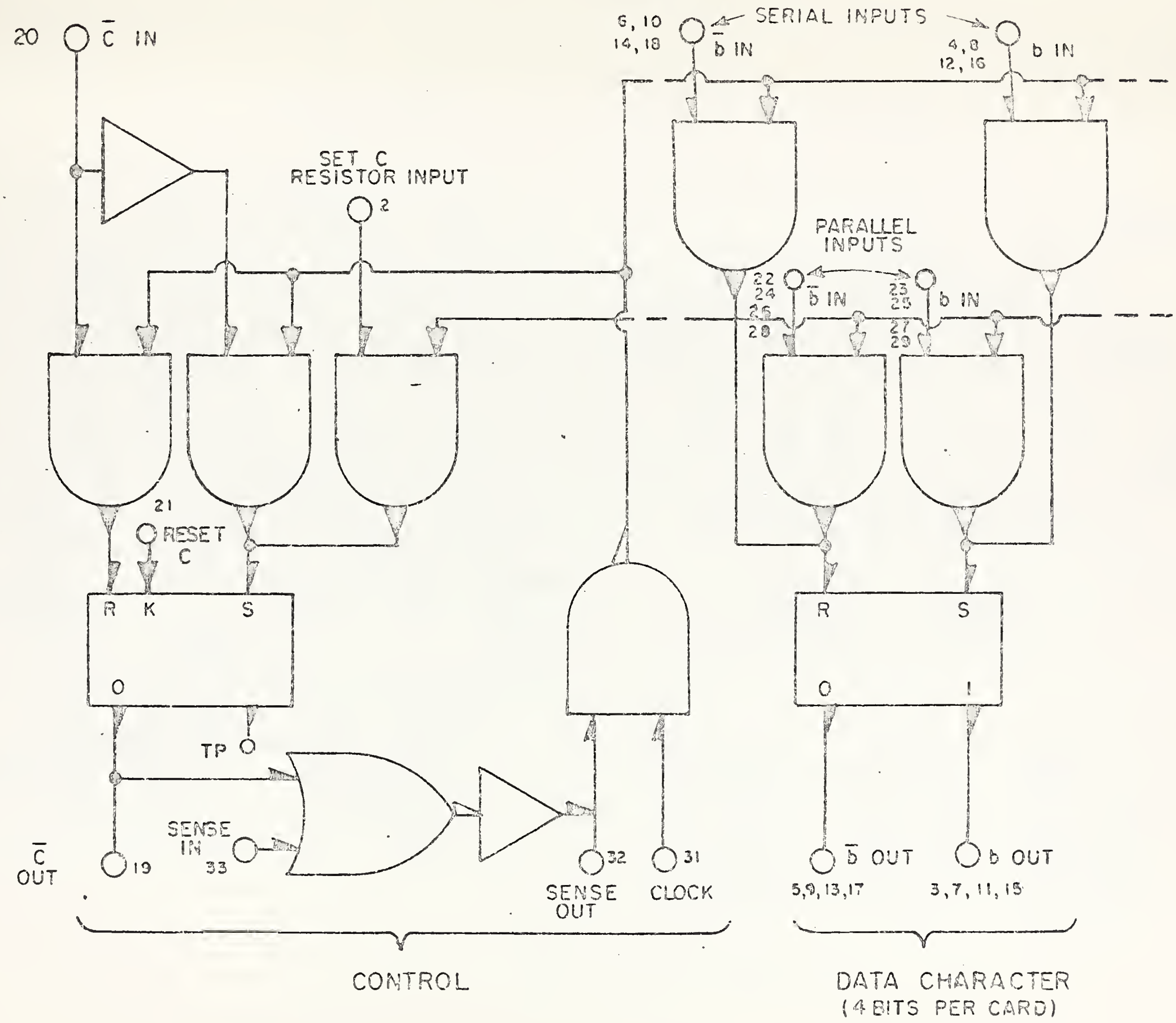


FIGURE 52. RIPPLE/SHIFT SERIES MAD-1 INTERNAL LOGIC

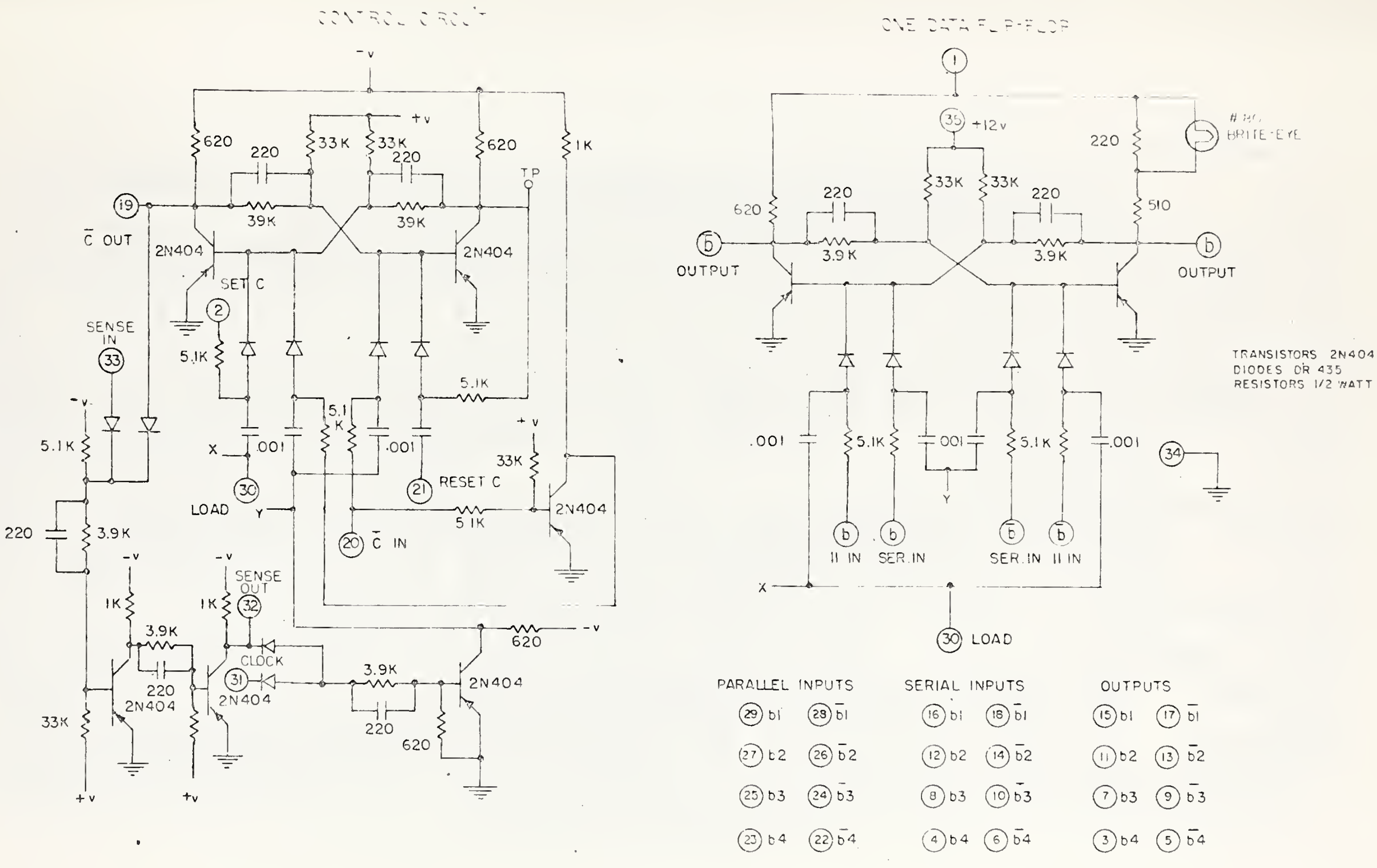


FIGURE 53 RIPPLE/SHIFT REGISTER CARD

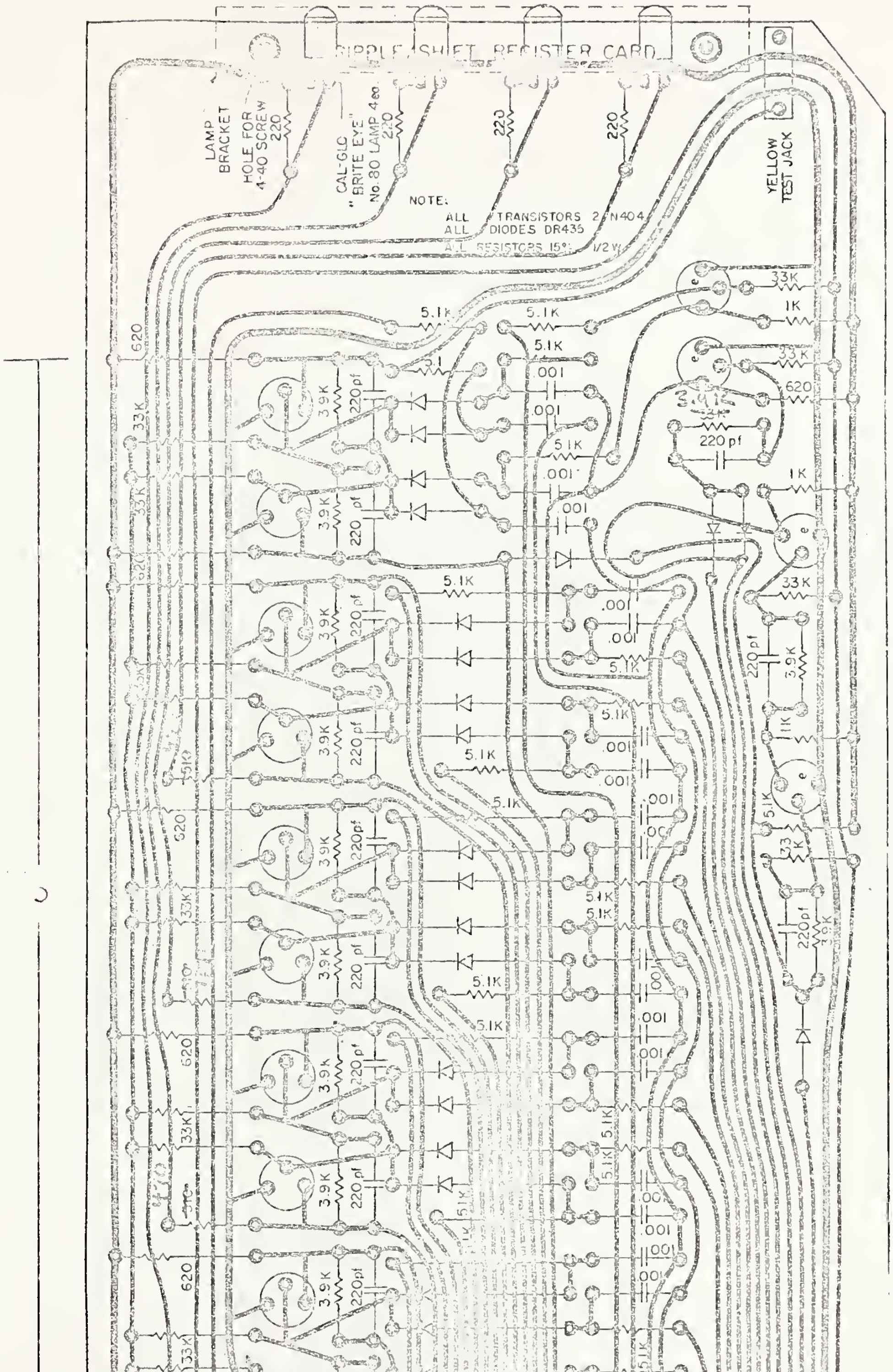


FIGURE 54

ORIG.

LAMP HOLDER

MATERIAL : BLACK LUCITE

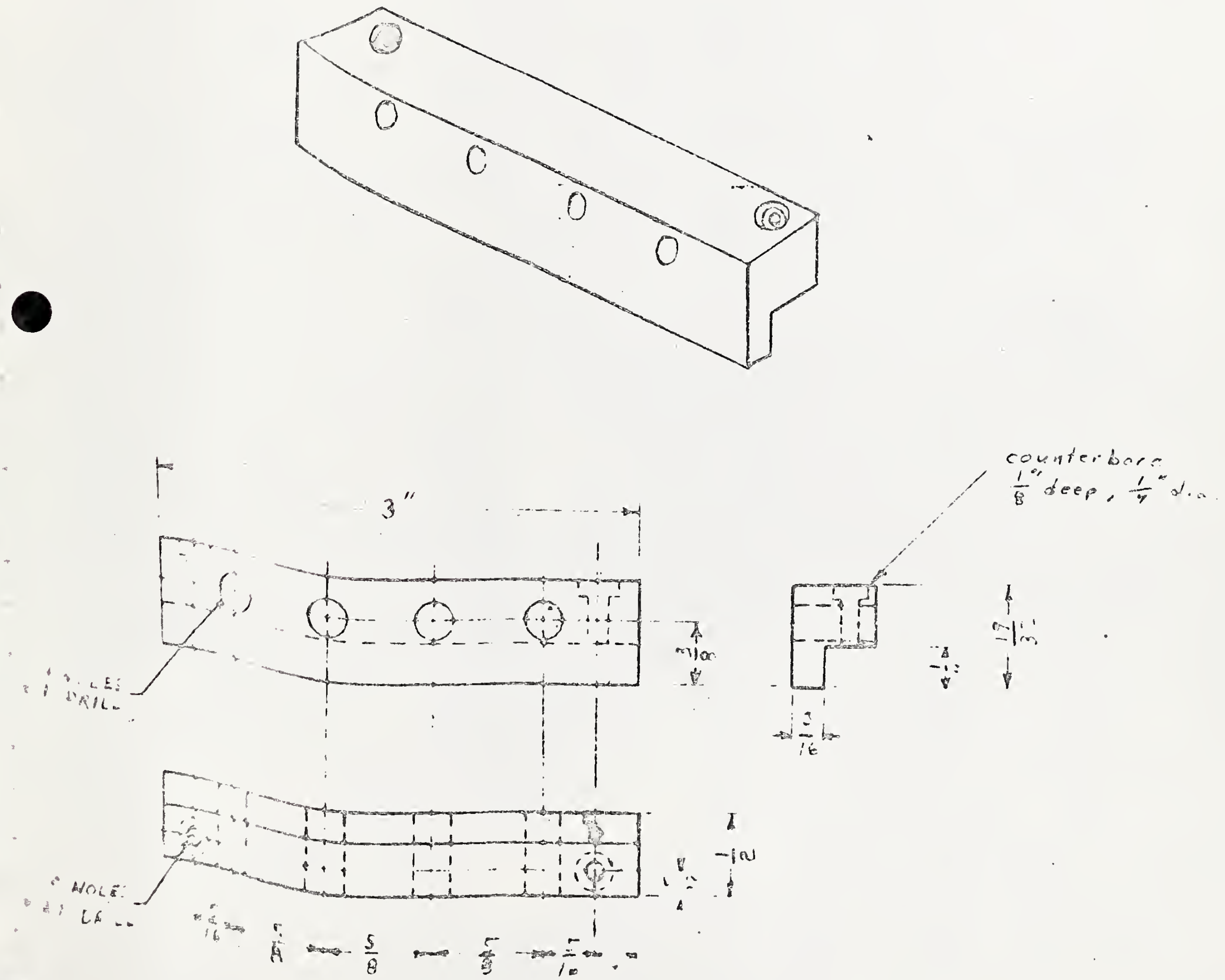


FIGURE 55.

Figure 56.

m. Ripple Spacer Card

Logical Function. To use a ripple register with fewer than the design number of stages, certain jumpers must be wired on the connectors of the omitted cards. In addition, the panel cutout must be filled with a blank spacer matching the indicator bracket. This card fulfills those functions.

Power Requirements. None.

Circuit Description. The following pins are jumpered on the card.

3-4
5-6
7-8
9-10
11-12
13-14
15-16
17-18
19-20
32-33

Construction Information. The dummy lamp bracket conforms to the same mechanical drawing as the proper bracket shown in Figure 55, except that holes for the bulbs are not drilled. Figure 57 shows the layout of the etched conductors on the card.

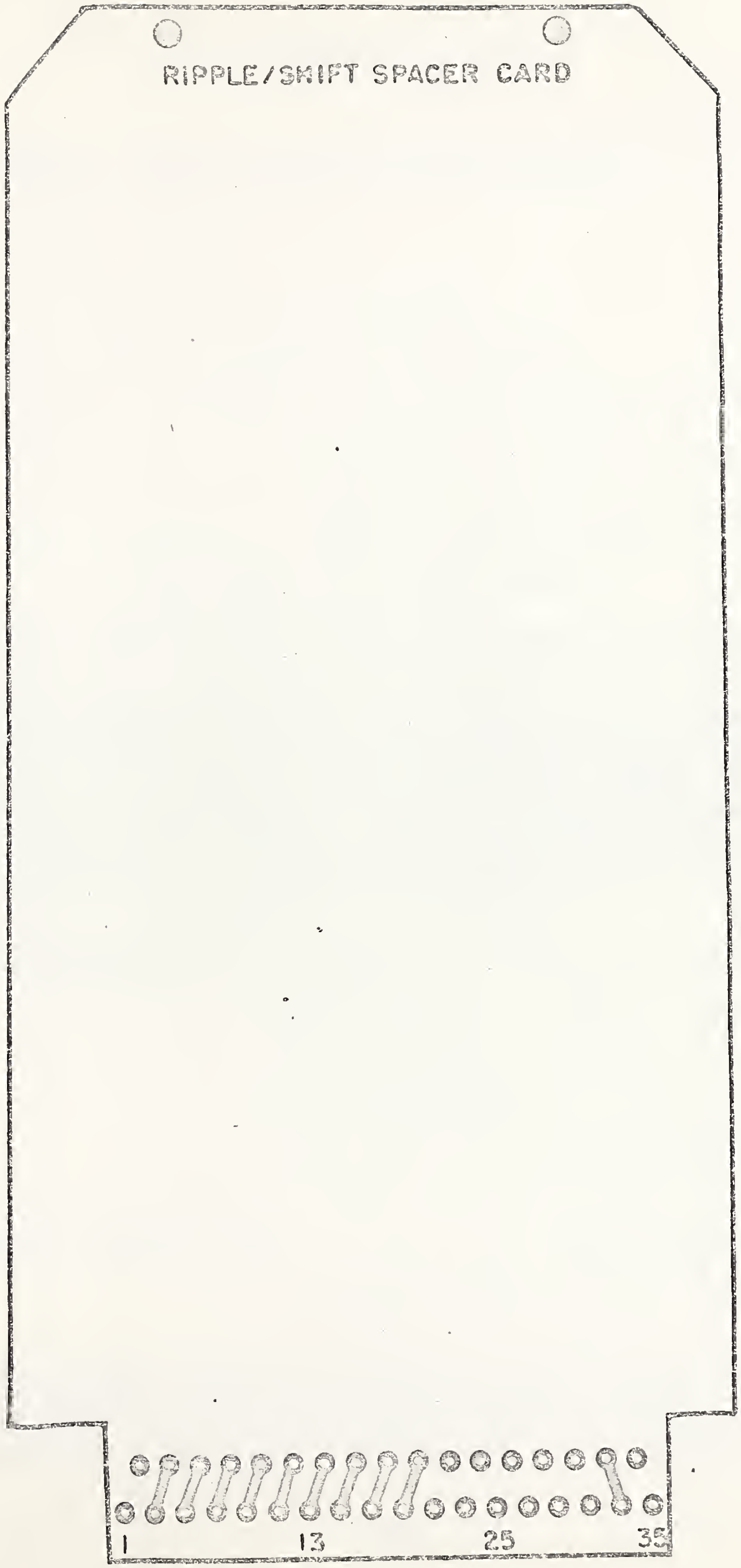


FIGURE 57.

n. High Impedance Amplifier

Logical Function. Each circuit performs the logical inversion, or NOT function, and also acts as a noise-rejecting amplifier.

Circuits per Card. Sixteen.

Input Load. One-quarter of one logic gate.

Fan-Out. Five logic gates and/or five pulse gates.

Power Requirements. -12 volts: 20ma for each output at 0 volt.

10ma for each output at -6 volts.

0ma for each output at -12 volts.

+12 volts: 1.1ma per circuit.

Logic Diagram. Figure 58 gives the logic diagram and pin numbers.

Logical Application. This amplifier is primarily used to generate the Boolean NOT or inversion function. It is also used as a buffer between the output of a diode matrix or other passive logic system, and further logic either active or passive. Its high input impedance, combined with optimum noise rejection, makes it ideal for this application. For a seven-input AND gate, for example, the diodes would be mounted on a matrix card or terminal board and the amplifier would be used to bring the output of the gate to standard levels and impedances.

Input Signal Requirements. Positive level: 0 volt to -0.2 volt.

Negative level: -6 volts to -12 volts.

Input Impedance: 16,000 ohms.

Input noise rejection: around ground: 2 volts.
around -6 volts: 3 volts.

Output Signal Characteristics: Positive level: 0 volts to -0.2 volts at approximately 10 ohms.

Negative level: -12 volts at 620 ohms.

Circuit Description. The circuit diagram is shown in Figure 59. This consists of a simple grounded collector amplifier feeding directly into a simple inverter. The circuit constants have been arranged so that the output will begin changing from -6 volts when the input passes -2.5 volts

going negative, and will reach 0 volts when the input passes -3 volts.

Trouble Shooting. The following table lists some troubles that may be encountered and suggests probable causes and remedies.

Sympton	Cause	Remedy
Output remains at -6 volts.	Shorted input leads.	Check with ohmmeter, repair.
Output remains at ground.	Shorted transistor.	Replace.

Construction Information. Figure 60 shows the component layout of the card. Figure 61 shows the etching on the reverse (component) side of the board. The table lists the required components.

Quantity	Item
32	2N404 Transistors
16	620-ohm, 1/2-watt, 5-percent Resistors.
16	1000-ohm, 1/4-watt, 5-percent Resistors.
16	16,000-ohm, 1/4-watt, 5-percent Resistors.
16	2000-ohm 1/4-watt, 5 percent Resistors
16	10,000-ohm, 1/4-watt, 5 percent Resistors.
16	Test Jacks.
	Transipads and Circuit Board.

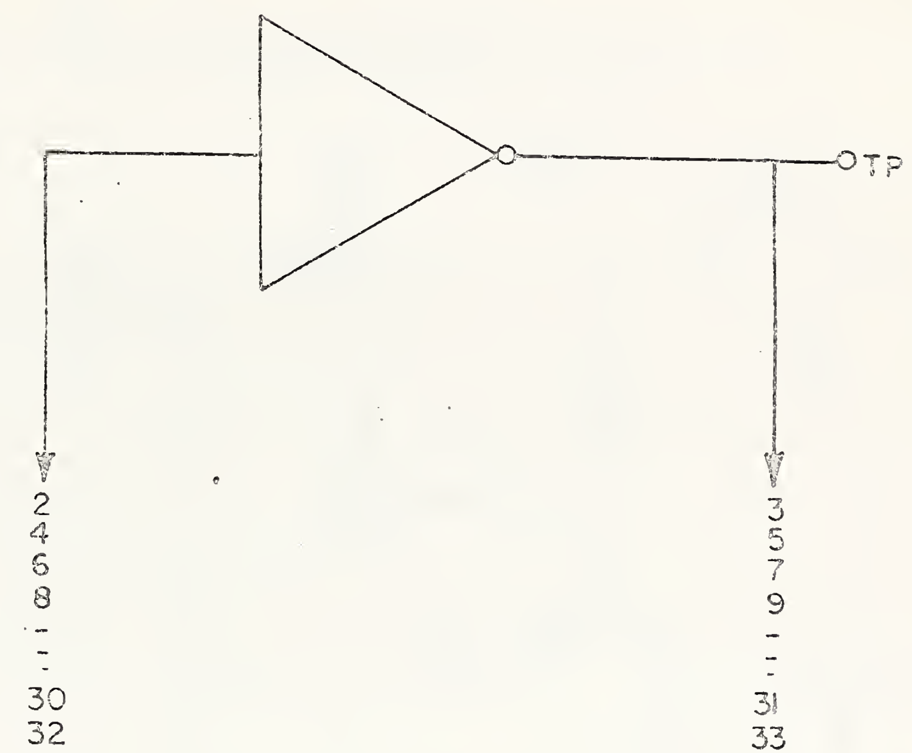


FIGURE 58. HIGH IMPEDANCE AMPLIFIER SERIES MAD-1

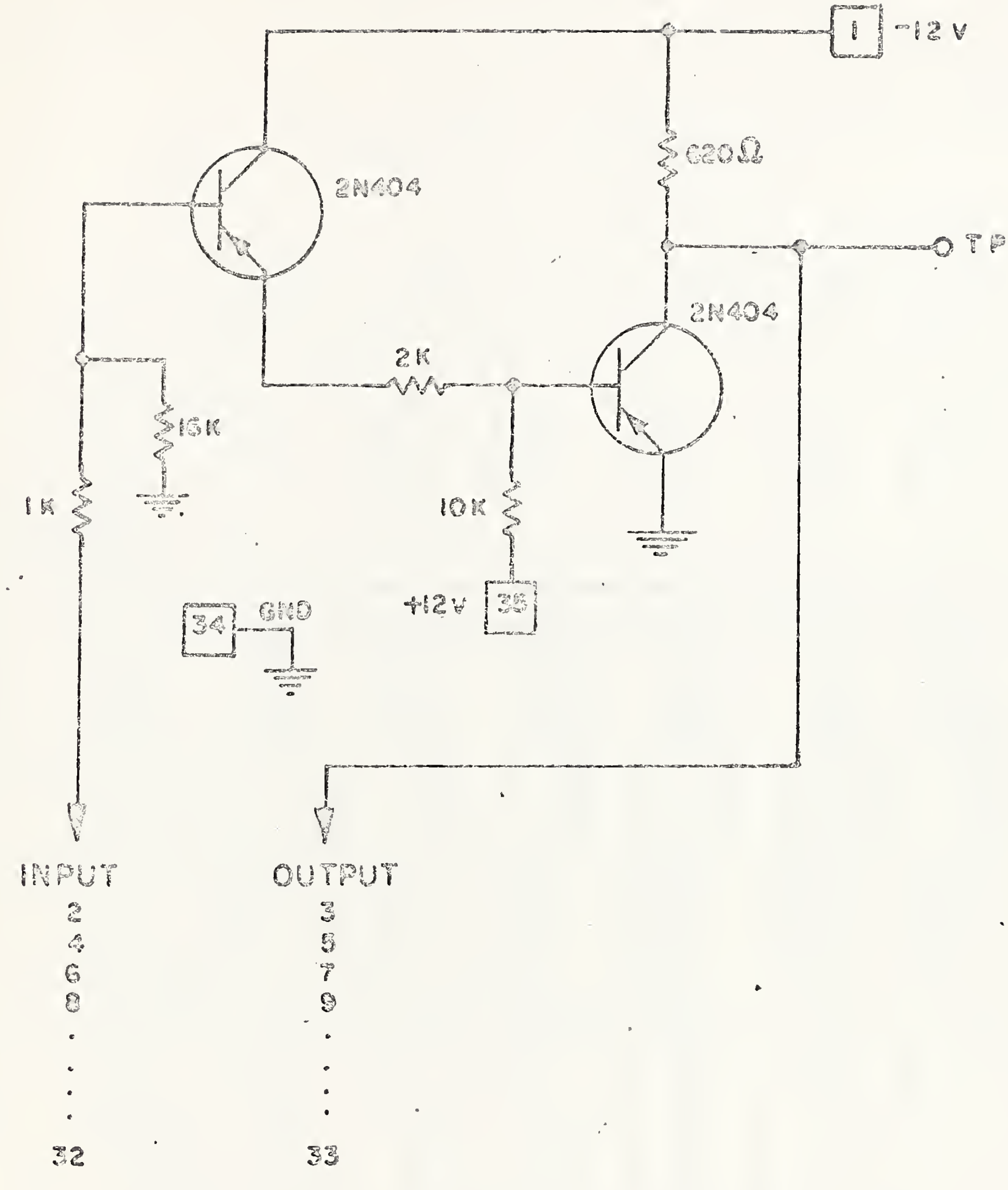


FIGURE 59. HIGH IMPEDANCE AMPLIFIER SERIES MAD-1


16 AMPLIFIERS SERIES MAD-1
GREY
GREY
2N404
2N404
10K 1/4W
EIGHT CIRCUITS (REPEAT EIGHT TIMES)

FIGURE 60.

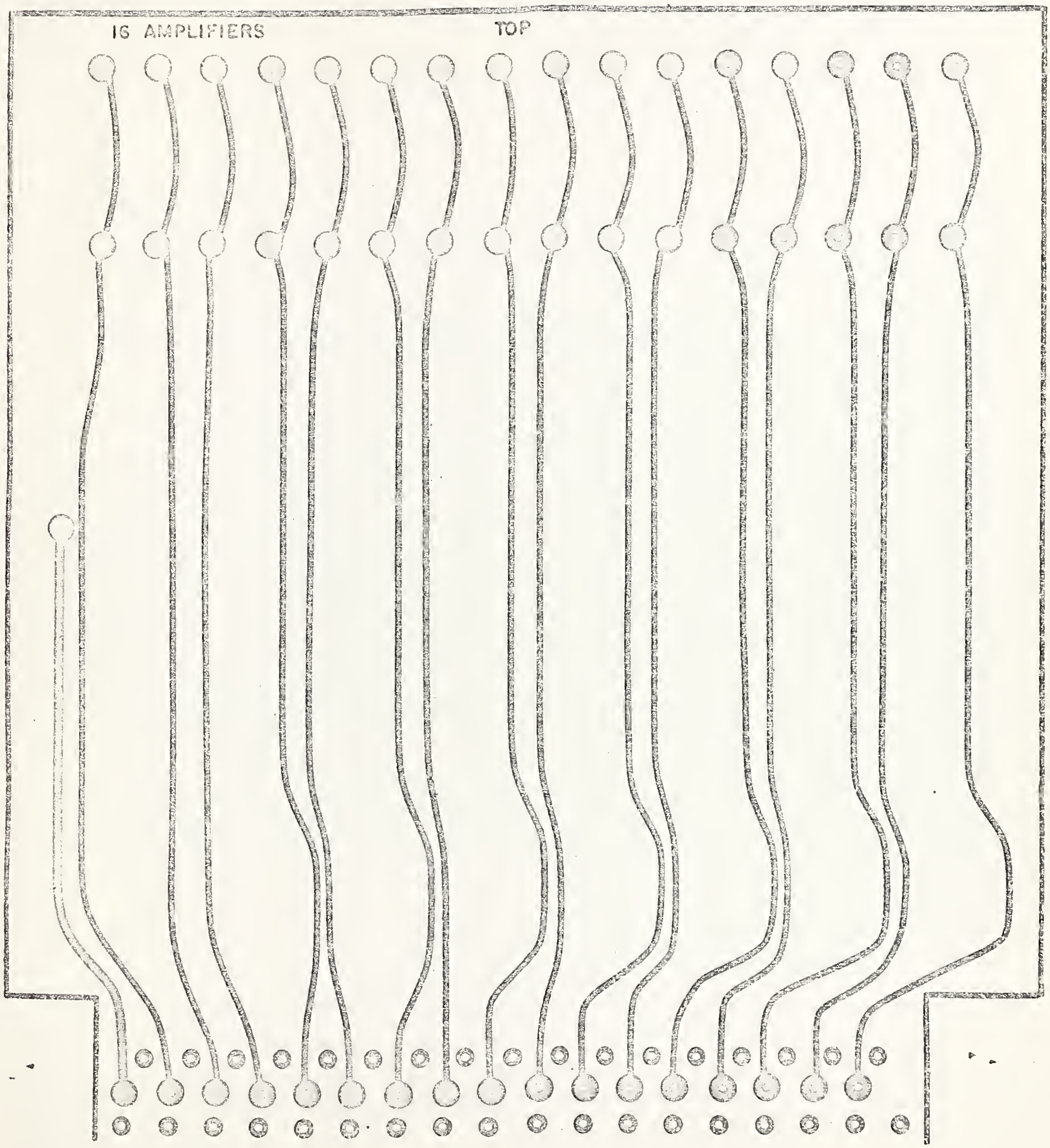


FIGURE 61.

FIGURE 62.

o. Oscillator/One-shot

Logical Function. This circuit is a universal timing device. It can be used as a free-running pulse oscillator, a keyed pulse oscillator, or a one-shot time delay generator.

Circuits per Card. Two.

Input Load. Flip-flop inputs: One standard pulse gate.

Oscillator key inputs: One standard logic gate.

Fan-Out. Flip-flop and oscillator outputs: Four standard logic gates and/or five standard pulse gates.

Power Requirements: -12 volts: 60 ma per circuit.

+12 volts: 9 ma per circuit.

Logic Diagrams. Figures 63 through 65 show the logic diagrams and pin numbers for all three applications.

Logical Application. When wired as a free-running oscillator, it can be used as a clock for the generation of sync pulses for a module or system. It may also be used as a pulse generator for design or trouble-shooting procedures. An external terminal is brought out for the variation of running frequency, and this can be used to operate the card as a voltage-controlled oscillator (VCO).

When wired as a keyed oscillator, it can be used as a clock for some intermittent or controlled function, whenever a string of pulses must be turned on and off. A flip-flop built into the card is most often used to control the oscillator, but logic levels from any source may be used.

When wired as a one-shot, it can be used for all time-delay and time-aperture applications explained in the description of the one-shot card.

Input Signal Requirements:

Positive level: 0 volts to -0.2 volts.

Negative level: -6 volts to -12 volts.

Input impedance: Flip-flop: 0.001μf to ground.

Input Signal Requirements (continued)

Oscillator control input: 3.9k ohms to ground-positive level suppresses oscillation.

Minimum dv/dt: For flip-flop: 6 volts μsec.

Frequency control input: 10,000 ohms.

Output Signal Characteristics.

Positive level: 0 volts to -0.2 volts at approximately 10 ohms.

Negative level: -12 volts at 620 ohms.

Minimum dv/dt: 6 volts per microsecond.

Circuit Description. The circuit diagram is shown in Figure 66. One-half of this circuit is a standard flip-flop as described elsewhere. There are no internal connections to the other half of the circuit. The operation of the flip-flop will not be described here.

Consider for the sake of the description that, originally, the timing capacitors are discharged (-12 volts on either plate), and that Q3, 4, 5, and 6 are all cut off. The timing capacitor charges from the source voltage (internal or external) towards ground. The capacitor "sees" 6.2 volts less than applied because of the action of the zener diode, which is now acting in the reverse direction. This voltage is applied to the emitter of the unijunction transistor Q6, which is not conducting. When the emitter-base 1 voltage of the unijunction reaches the characteristic voltage of that device, it begins to conduct, and starts to discharge the timing capacitor. When it conducts, however, this pulls the base of Q3 negative, and it conducts. This turns on Q4, allowing Q5 to conduct. Q5 discharges the timing capacitor much more quickly than Q6 would be able to do unaided.

When Q3 conducts, it brings pin 17 to ground. If pin 17 is jumpered to pin 16, giving Q3 a 620-ohm collector load, an output pulse of 5 to 10 microsecond width and of standard logic levels will be produced.

If pin 15 is grounded, Q4 turns on, turning on Q5. This low-resistance path appears across the timing capacitors, preventing them from charging. The circuit therefore does not oscillate. This point may be tied to any logic level for use in keying the oscillator. The flip-flop on the card is especially useful for this function, since the oscillator may then be turned on and off by pulses.

NOTE: The first cycle of the oscillator will be longer than the others when it is keyed "on". When the oscillator is not running, the timing capacitors discharge fully. On the second and subsequent cycles of operation, however, the unijunction transistor stops the discharging procedure before completion. The difficulty may be minimized by increasing the charging voltage. When this is done, the incomplete discharging is no less, but it is a smaller fraction of the total voltage, and has a correspondingly smaller effect. Increasing the charging voltage is accomplished by shorting out the zener diode, and by making the timing capacitor smaller.

If pin 17 is connected directly to the collector of the flip-flop, and the extra load resistor on pin 16 is omitted, one-shot action will occur as follows:

If Q1 is jumpered to pin 17 and the flip-flop is in the reset state, then Q1 will be conducting, and the collector of Q3 will be at ground. Q4 will therefore be on, and the oscillator stopped. If the flip-flop is now set, Q1 allows Q4 to turn on and one timing cycle is initiated. At the end of that cycle, Q3 is turned on by Q6 in the normal manner, and as its collector goes to ground, it pulls Q1 with it, thereby resetting the flip-flop and preventing further oscillation.

Trouble Shooting. The following table lists some troubles that may be encountered and suggest probable causes and remedies.

Symptom	Cause	Remedy
Oscillator will not run.	Analog control voltage too negative.	Adjust trimpot on card. Check external control voltage.
Oscillator will not run.	Q5 on, shorting timing capacitor.	Make sure pins 15 and 17 are negative, otherwise oscillator is keyed "off".
One-shot jitter or oscillator frequency drift, especially at varying repetition rates.	Defective zener diode.	Replace.
Wide variation of frequency with temperature.	Defective zener diode.	Replace.

Construction Information. Figure 67 shows the components layout, and the list below shows the required parts.

Quantity	Item
6	2N404 Transistors
4	2N2926 Transistors
2	2N2646 Transistors
2	1N2069 Diodes
10	DR435 Diodes
2	1N1766 Zener Diodes
2	5000-ohm Trimpots
6	620-ohm, 5 percent, 1/2-watt Resistors
6	10k ohm, 5 percent, 1/2-watt Resistors
2	2.7k, 5 percent, 1/2-watt Resistors
2	20-ohm, 5 percent, 1/2-watt Resistors
2	360-ohm, 5 percent, 1/2-watt Resistors
6	3.9k ohm, 5 percent, 1/2-watt Resistors
2	200-ohm, 5 percent, 1/2-watt Resistors
2	2000-ohm, 5 percent, 1/2-watt Resistors
2	5.6k ohm, 5 percent, 1/2-watt Resistors
2	1k ohm, 5 percent, 1/2-watt Resistors
4	5.1k ohm, 5 percent, 1/4-watt Resistors
2	33k ohm, 5 percent, 1/2-watt Resistors
4	220pf disc Ceramic Capacitors
4	.001µf Mylar Capacitors, Sprague 192P
2	.01µf Mylar Capacitors, Sprague 192P
2	0.1µf Mylar Capacitors, Sprague 192P
	Transipads and Circuit Board.

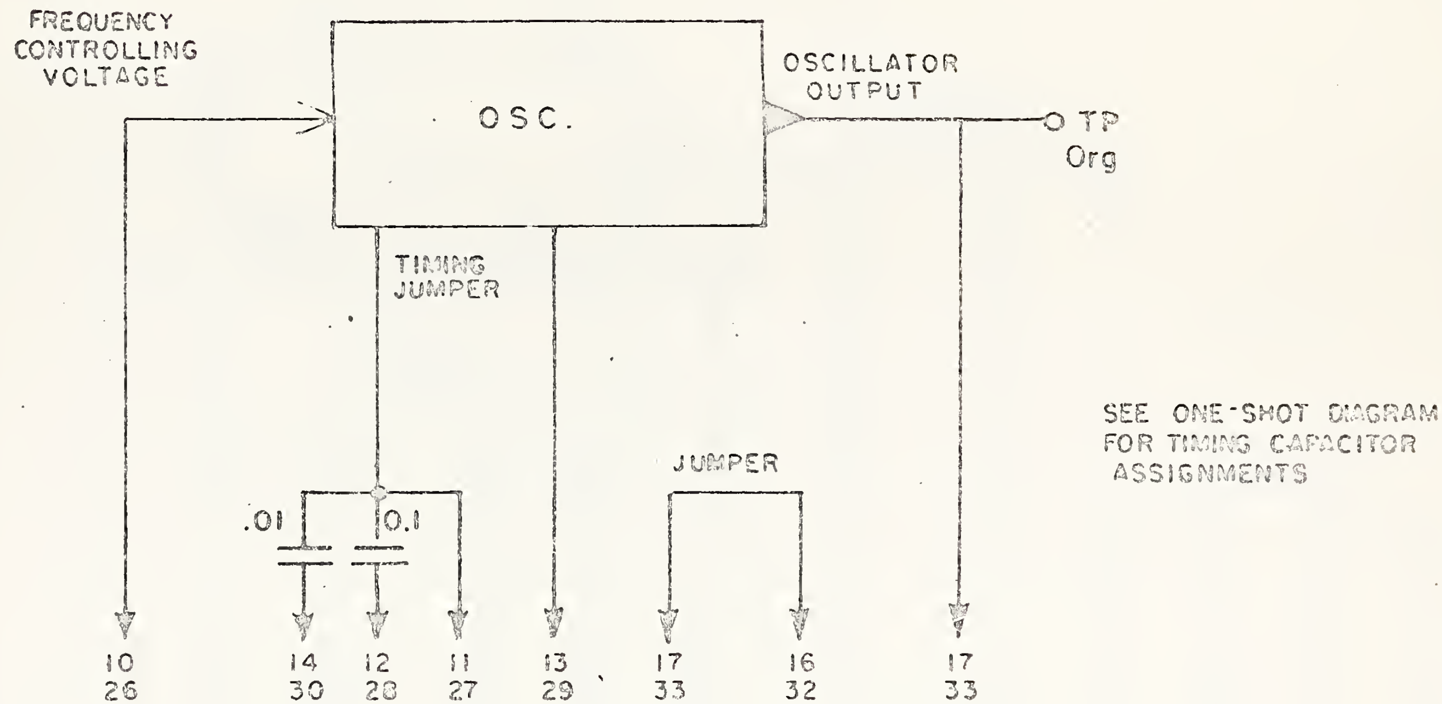
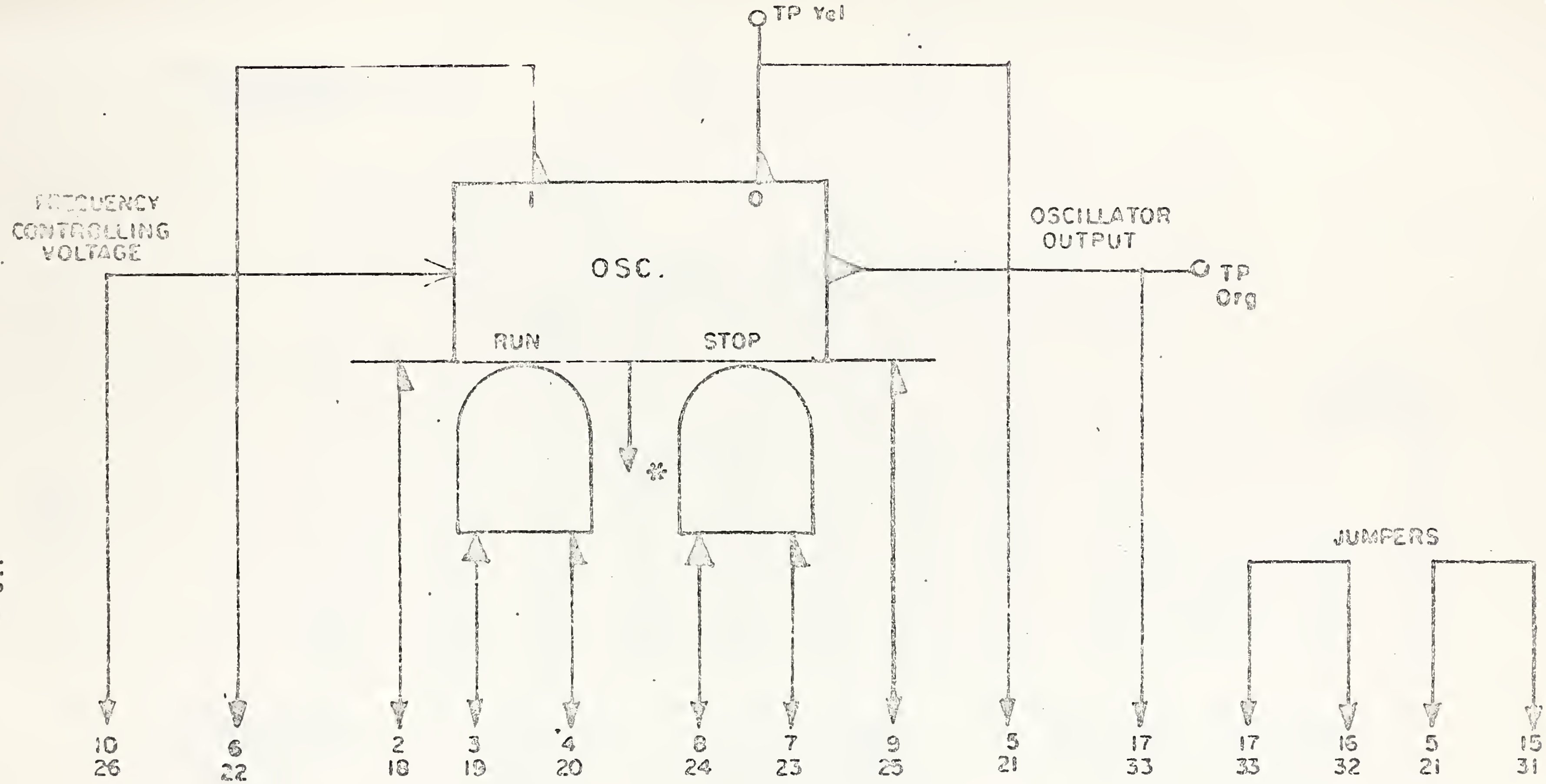
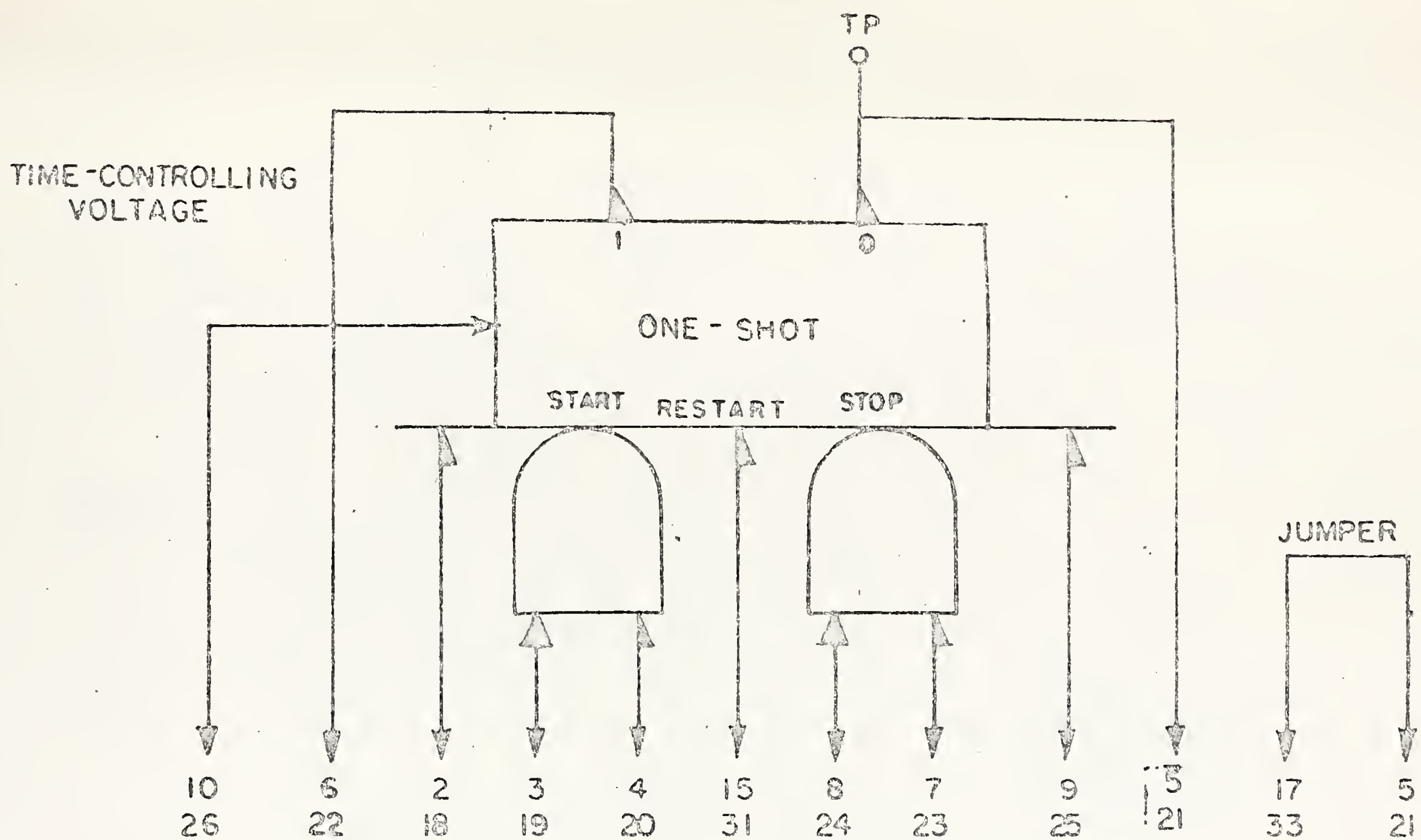


FIGURE 63. OSCILLATOR / ONE-SHOT SERIES MAD-1 AS A FREE-RUNNING OSCILLATOR



* SEE ONE-SHOT DIAGRAM FOR TIMING CAPACITOR ASSIGNMENTS

FIGURE 64. OSCILLATOR/ONE-SHOT SERIES MAD-1 AS A KEYED OSCILLATOR



CAPACITOR	JUMPER	OSC. FREQ.	ONE-SHOT RUN TIME
.001 uf	NONE	20 KC → 200 KC	5 usec → 50 usec
.01 uf	13 → 14 29 → 30	2 KC → 20 KC	50 " → 500 "
0.1 uf	13 → ~~2~~ 12 29 → 28	200 CPS → 2 KC	500 usec → 5 msec

EXTERNAL CAPACITOR FROM 11 → 13
OR 27 → 29 (+ TO PIN 11 AND 27 FOR POLAR CAPACITORS)

FIGURE 65. OSCILLATOR/ONE-SHOT SERIES MAD-1 AS A ONE-SHOT

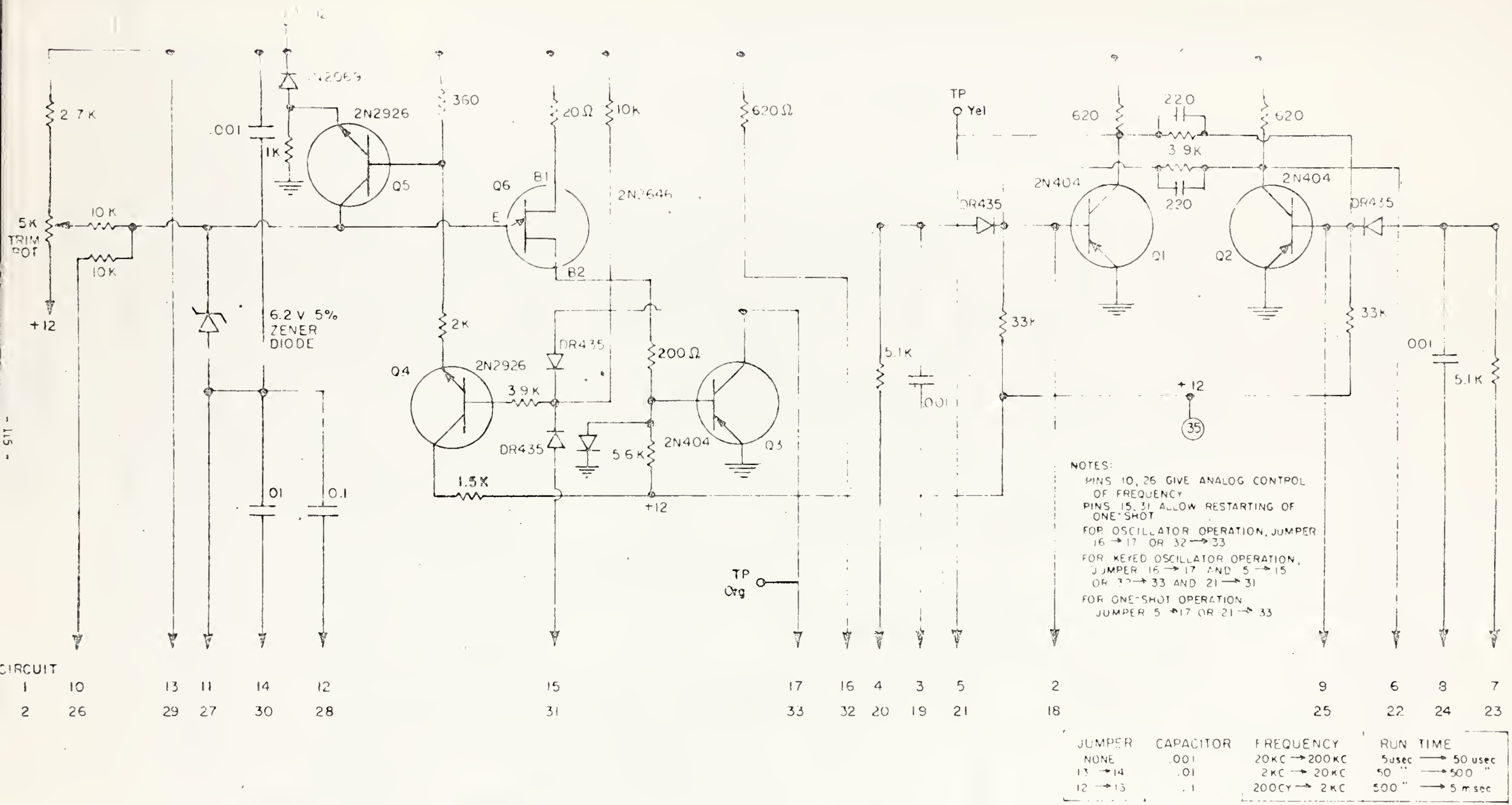
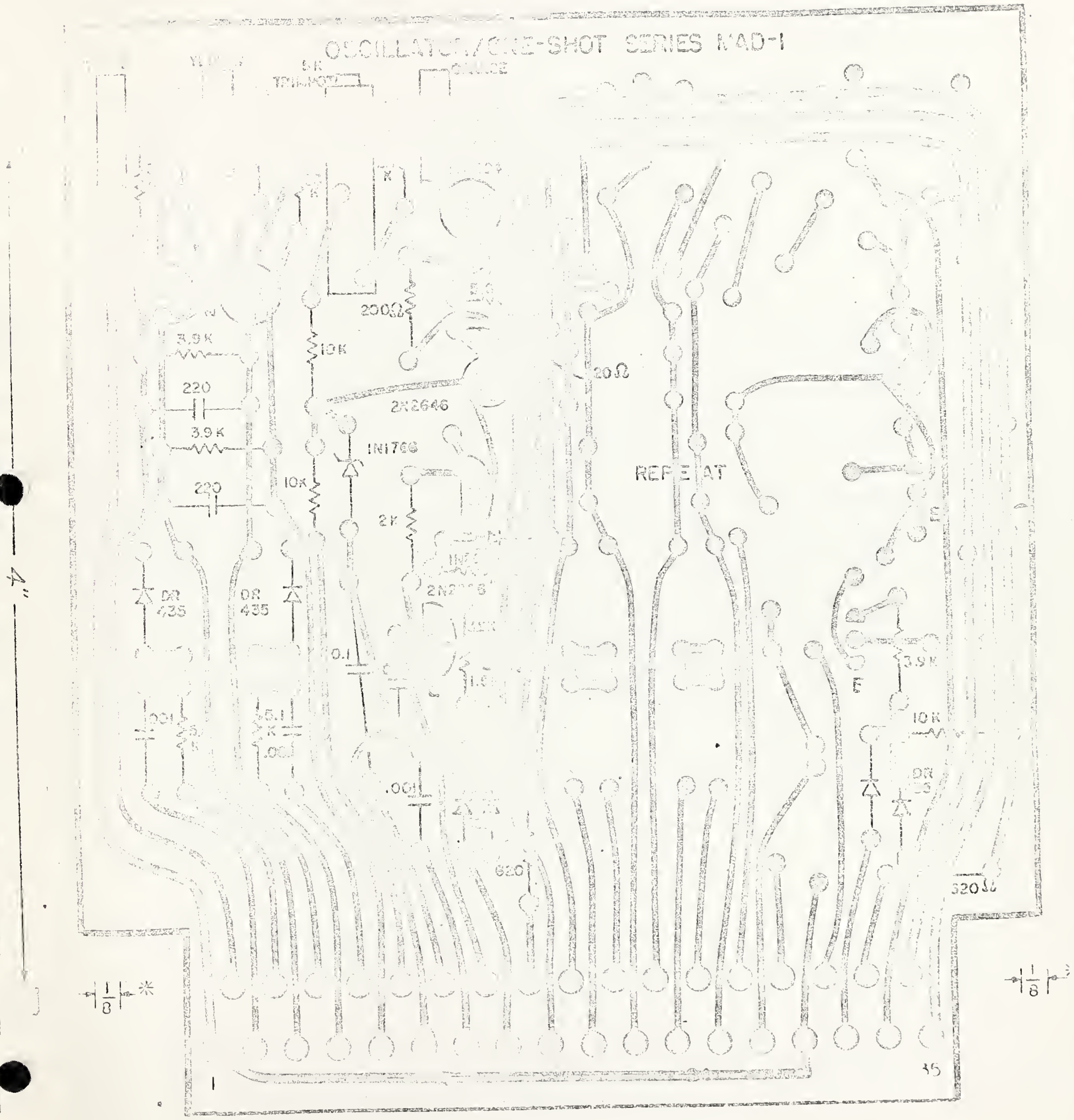


FIGURE 66 OSCILLATOR / ONE SHOT SERIES MAD-1



✳ MIN PERMISSIBLE SPACE FROM EDGE OF CONDUCTOR TO EDGE OF BOARD

FIGURE 67.

Figure 68.