NISTIR 7686

Semiconductor Microelectronics and Nanoelectronics Programs

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July 2010

National Institute of
Standards and Technology
U.S. Department of Commerce

Semiconductor Microelectronics and Nanoelectronics Programs

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U.S. DEPARTMENT OF COMMERCE
Gary Locke, Secretary

National Institute of Standards and Technology
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Disclaimer

Disclaimer: Certain commercial equipment and/or software are identified in this report to adequately describe the experimental procedure. Such identification does not imply recommendation or endorsement by the National Institute of Standards and Technology, nor does it imply that the equipment and/or software identified is necessarily the best available for the purpose.

References: References made to the International Technology Roadmap for Semiconductors (ITRS) apply to the most recent edition, dated 2009.

Semiconductor Industry Association. The International Technology Roadmap for Semiconductors, 2009 edition. SEMATECH: Austin, TX, 2009.

These documents are available on-line at: http://www.itrs.net for downloading.

The reader will notice that there are acronyms and abbreviations throughout this document that are not spelled out due to space limitations. We have listed the acronyms and abbreviations in an appendix at the end of this document.

Contents

Welcome and Introduction

Welcome

The microelectronics industry supplies vital components to the electronics industry and to the U.S. economy, enabling rapid improvements in productivity and in new high technology growth industries such as electronic commerce and biotechnology. The National Institute of Standards and Technology, NIST, in fulfilling its mission of strengthening the U.S. economy, works with industry to develop and apply technology, measurements and standards and applies substantial efforts on behalf of the semiconductor industry and its infrastructure. This report describes the many projects being conducted at NIST that constitute that effort.

Historical Perspective

NIST's predecessor, the National Bureau of Standards (NBS), began work in the mid-1950s to meet the measurement needs of the infant semiconductor industry. While this was initially focused on transistor applications in other government agencies, in the early 1960s the Bureau sought industry guidance from the American Society for Testing and Materials (ASTM) and the U.S. Electronic Industries Association (EIA). ASTM's top priority was the accurate measurement of silicon resistivity. NBS scientists developed a practical nondestructive method ten times more precise than previous destructive methods. The method is the basis for five industrial standards and for resistivity standard reference materials widely used to calibrate the industry's measurement instruments. The second project, recommended by a panel of EIA experts, addressed the "second breakdown" failure mechanism of transistors. The results of this project have been widely applied, including solving a problem in main engine control responsible for delaying the launch of a space shuttle.

From these beginnings, by 1980 the semiconductor metrology program had grown to employ a staff of 60 with a $6 million budget, mostly from a variety of other government agencies. Congressional funding in that year gave NBS the internal means to maintain its semiconductor metrology work. Meeting industrial needs remained the most important guide for managing the program.

Industrial Metrology Needs

By the late 1980s, NBS (now NIST) recognized that the semiconductor industry was applying a much wider range of science and engineering technology than the existing NIST program was designed to cover. The necessary expertise existed at NIST, but in other parts of the organization. In 1991, NIST established the Office of Microelectronics Programs (OMP) to coordinate and fund metrological research and development across the agency, and to provide the industry with easy single point access to NIST's widespread projects. Roadmaps developed by the U.S. Semiconductor Industry Association (SIA) have independently identified the broad technological coverage and growing industrial needs for NIST's semiconductor metrology developments. As the available funding and the scope of the activities grew, the collective name became the National Semiconductor Metrology Program (NSMP), operated by the OMP.

The NSMP has stimulated a greater interest in semiconductor metrology, motivating most of NIST's laboratories to launch additional projects of their own and to cost-share OMP-funded projects. The projects described in this book represent this broader portfolio of microelectronics projects. Most, but not all, of the projects described are partially funded by the NSMP, which is providing a $12 million budget in fiscal year 2008.

Fostering NIST's Relationships with the Industry

NIST's relationships with the SIA, SEMATECH and its subsidiary, International SEMATECH Manufacturing Initiative (ISMI), and the Semiconductor Research Corporation (SRC) are also coordinated through the OMP. Staff from OMP and NIST Laboratories represents NIST on the SIA committees that develop the International Technology Roadmap for Semiconductors (ITRS), as well as on numerous SRC Technical Advisory Boards. NIST staff is also active in the International National Electronics Manufacturers Initiative (iNEMI), the EIA, the International Organization for Standardization (ISO),

and Semiconductor Equipment and Materials International (SEMI). NIST supports the United States National Committee Technical Advisory Group for the International Electrotechnical Commission Technical Committee TC113 on Nanotechnology Standardization for Electrical and Electronic Products and Systems (Technical Advisor, USNC TAG for IEC TC 113 on nanotechnology) by funding the Technical Advisor to that organization.

Learn More About Semiconductor Metrology at NIST

This publication provides summaries of NIST's metrology projects for the silicon semiconductor industry and their suppliers of materials and manufacturing equipment. Each project responds to one or more metrology requirements identified by the industry in sources such as the ITRS. NIST is committed to listening to the needs of industry, working with industry representatives to establish priorities, and responding where resources permit with effective measurement technology and services. For further information, please contact:

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Left to right: Y. Obeng, M. Buckley, J. Martinez de Pinillos.

Lithography Metrology Program

Advances in lithography have largely driven the spectacular productivity improvements of the integrated circuit industry, a steady quadrupling of active components per chip every three years over the past several decades. This continual scaling down of transistor dimensions has allowed more and more components on a chip, lowered the power consumption per transistor, and increased the speed of the circuitry. The shrinking of device dimensions has been accomplished by shortening the wavelength of the radiation used by the lithography exposure tools. The workhorse tools at this point operate at 193 nm. In order to further shrink dimensions liquid immersion tools with water as the immersion fluid have been introduced. Further size reduction through the use of high index fluids, lens materials and photoresist for 193 nm tools are under intense exploration for even higher numerical aperture systems. Looking beyond the deep ultraviolet, extreme ultraviolet radiation (EUV) at 13 nm is being investigated, and demonstration tools are being designed and assembled. At least three alpha tools were shipped to development consortia in 2006. The overall goal of this task is to support these developments in DUV and EUV. The areas of emphasis are characterization of lens materials and immersion fluids, laser calorimetry, radiation detector sensitivity and damage, EUV lens metrology, and metrology for the development of advanced photoresist materials for both DUV and EUV.

Optical Metrology Supporting Advanced Alternative Lithographies

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Eric Benck
S. G. Kaplan

"It's an excellent service NIST has performed for the entire industry. The kind of thing NIST is there for – to identify issues before the train wreck takes place."

Mordechai Rothschild,
Massachusetts Institute
of Technology's
Lincoln Laboratory

Goals

Develop solutions to key optical and optical materials issues confronting the semiconductor lithography industry. These include: development of measurement methods for characterizing the optical properties of deep ultraviolet (DUV) materials, delivering optical measurements of key lithography materials to the high accuracy needed by the industry, investigating exposure effects on the optical properties, including nonlinear effects and exposure damage, and in general exploring optical issues associated with the extension of 193 nm immersion lithography.

Customer Needs

193 nm immersion lithography, with water as the immersion fluid, is now being commercially implemented with numerical apertures near 1.3, enabling the 45 nm technology node. Extension of 193 nm technology to the 32 nm and 22 nm nodes and below is being considered using high-index immersion fluids and optical elements and/or multiple patterning approaches. Accurate measurements of the optical properties, such as refractive index, thermo-optic coefficient, birefringence, and laser durability, are needed for the new materials involved. Even for the conventional materials, the increasingly tightened optical specifications require higher-accuracy measurements of these properties. Alternative maskless optical lithography approaches, e.g., hybrid interference lithography, are being developed, requiring optical materials new to lithography, such as sapphire. The optical properties of these materials have to be characterized, and new optical metrology approaches will need to be developed.

To address these needs, the National Institute of Standards and Technology (NIST), with SEMATECH support, has developed and pursed a DUV metrology program, which now focuses on the optical and optical materials issues confronting the extension of DUV lithography. In addition to developing more accurate optical characterization techniques and delivering more accurate measurements to the industry, the program has a particular focus on developing the metrology technology needed for practical implementation of hybrid interference lithography. This new potentially fully maskless optical lithography approach offers the possibility of enabling commercial fabrication of integrated circuits with leading-edge performance at substantially reduced cost.

The potential challenges for lithographic development are discussed in the 2009 Edition of the International Technology Roadmap for Semiconductors. Page 1 of the Lithography section states: "In 2009 and beyond, maintaining the rapid pace of half-pitch reduction requires overcoming the challenge of improving and extending the incumbent optical projection lithography technology…" Figure LITH3, Lithography Exposure Tool Potential Solutions, lists Innovative 193 nm Immersion Double / Multiple Patterning as potential solutions down to the 16 nm technology node and Interference Lithography as potentially providing solutions down to the 11 nm technology node.

Technical Strategy

Several approaches are being considered to extend 193 nm immersion lithography beyond the 45 nm technology node, including multiple patterning and using high-index lens materials and immersion fluids. All of these approaches require tighter specifications on critical feature alignment and dimensions. This in turn requires tighter specifications on the optical imaging systems and thus on the index properties measurements of the imaging materials. For previous tool generations, NIST has provided index measurements with the 5 ppm absolute accuracy needed for optical design. To address the tighter specifications now needed, NIST has constructed a new minimum-deviation-angle refractometer system with absolute accuracy of better than 1 ppm. Along with improved thermo-optic coefficient and birefringence measurement systems that NIST is constructing, these facilities should satisfy the optical characterization demands for imaging materials for 193 nm lithography extension down to the 16 nm technology node. These facilities will be used to push the state-of-the-art accuracy of optical-materials measurements for all the key optical materials now used by industry. The facilities will also be used to characterize alternative materials, such as new high-index lens and immersion

fluid materials that could be used for resolution extension, and for those optical materials needed for alternative lithographies, such as hybrid interference lithography.

DELIVERABLES:

- Measurement of the refractive index of fused silica, calcium fluoride, and water, as well as high-index fluids and high-index lens materials, with an accuracy of 1 ppm. Accurate measurements of the thermo-optic coefficients of these materials. Ongoing.

The lithography industry has been increasingly concerned about a class of optical issues associated with the non-linear optical response of materials, which can be both problematic and useful. The problematic issues result from the higher laser intensities causing irreversible optical properties changes, e.g., by two photon absorption or by self-trapped exciton effects. These effects have been first confronted in the laser optics, and has resulted in design restrictions to protect the optics. On the other hand, non-linear optical response of materials, e.g., saturable absorption effects, can be exploited for contrast enhancement. Nanoscale oxide crystals exhibit these effects, and use in resist layers or separate layers could enable double-exposure patterning, involving only one etch step for two or multiple exposures. To explore these effects and help with the design of the double exposure materials, NIST is building a Ultra Violet (UV) pump-and-probe facility. This system is based on unique tunable (190 nm to 1000 nm) solid-state Optical Parametric Oscillator (OPO) pump laser systems, along with tunable probe laser systems with synchronous detection and time-delayed detection for time-resolution studies. This work is being done in collaboration with industry partners to explore the general issues and to focus on the most promising directions.

DELIVERABLES:

- 190 nm - 1000 nm pump-and-probe, time-resolution facility operational and begin characterizing the non-linear optical properties of lithography materials and of promising new oxide nano-crystalline materials: 4Q 2010.

The development of the concept of hybrid interference lithography, based on combining laser-interference-pattern illuminations with trim and stitch illuminations, has now shown enough promise that practical feasibility investigations have begun. One key issue is whether sub-200 nm laser systems can be developed with adequate temporal- and spatial-coherence properties to enable large scale (ideally full-chip) high-contrast interference patterns. If this can be demonstrated, then it has to be determined whether the interference-pattern pitch, line straightness, and positioning and orientation can be controlled sufficiently to satisfy registration requirements. We have begun a project in collaboration with industry partners to demonstrate the feasibility of a real-time feedback metrology system to characterize and control the interference patterns sufficiently for commercial production. Realistic physical optics modeling has demonstrated our approach based on interpreting the moire patterns created by the interaction of the illuminated interference pattern with a reference pattern. We are now designing and building a demonstration system.

DELIVERABLES:

- Demonstration of feedback metrology system to characterize and control full-field interference pattern at 100 nm hp: 2Q 2011. Demonstration of system to establish pattern registration meeting specifications at 32 nm hp. 4Q 2011.

Accomplishments

■ We have used the new minimum-deviation refractometer system to make the most accurate (1 ppm uncertainty) measurements of calcium fluoride. Tighter lithography exposure tool design requirements have required higher accuracy measurements of the refractive index of lithography lens materials and required accurate assessments of sample-to-sample index variations. Our measurements delivered the data required for next-generation 193 nm immersion lithography exposure tool design and establishes that we now have the capability to meet the measurement demands for the next several technology node generations.

■ We have established through modeling the spatial-dispersion-induced birefringence and anisotropy issues associated with the use of uniaxial sapphire as a key optical element for new polarized illumination lithography tool designs. (See Fig. 1 a,b,c.) Full lithography simulations by our collaborators have demonstrated substantial practical advantages for lithography optics designs based on using uniaxial sapphire as a last lens element with polarized imaging. These advantages include improved resolution, reduced depolarization-

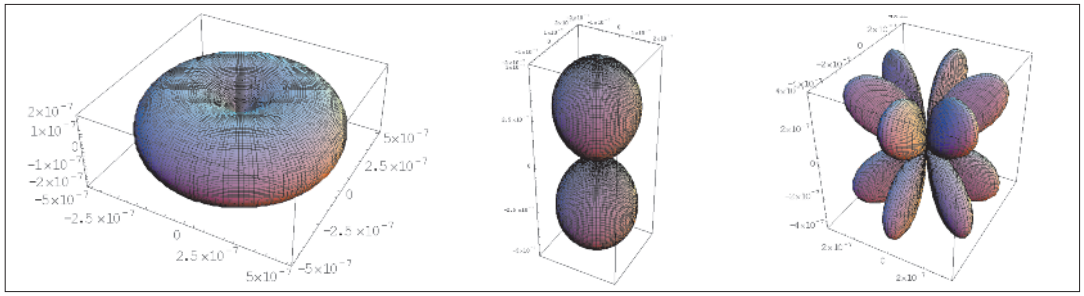

Figure 1a, 1b, and 1c. The three contributions to the index anisotropy of the ordinary ray due to spatial-dispersion effects in sapphire. The sapphire uniaxial axis (z-axis) is vertical. The magnitudes of these surfaces (referred to the origin) give the deviations from isotropy in a given direction. Effects shown in 1a and 1b give distortions with azimuthal symmetry about the z-axis. Only the effect shown by 1c gives azimuthal distortions, which may need to be corrected for.

induced flare, and reduced numbers and sizes of lens elements. We have also been working with sapphire manufactures to demonstrate that sapphire can be produced meeting lithography specifications.

■ To support the development of hybrid interference lithography, we have developed a real-time metrology approach to characterize the full-field laser interference pattern projected on the wafer and to provide feedback to the laser and adaptive optics to establish registration over the field. This approach is based on interpreting the moire pattern resulting from the interaction of the interference pattern with a reference pattern, and realistic physical optics modeling demonstrates that the approach could achieve the required registration specifications.

Collaborations

Carl Zeiss SMT, Wilfried Clauss, ppm accuracy index measurements of litho-grade calcium fluoride. Crystalith, Gabriel Sirat, modeling of polarized, isotropic lithography imaging using sapphire. Crystal Systems, Fred Schmid, characterization and improvement of sapphire for lithography optics. Actinix, James Jacob, development of feedback metrology system for hybrid immersion lithography.

Publications

S. G. Kaplan and J. H. Burnett, *"Optical properties of fluids for 248 nm and 193 nm immersion photolithography,"* Applied Optics 45, 1721 (2006).

John H. Burnett, Simon G. Kaplan, Eric L. Shirley, Deane Horowitz, Wilfried Clauss, Andrew Grenville, and Chris Van Peski, *"High-index optical materials for 193-nm immersion lithography,"* in Optical Microlithography XIX, edited by Donis G. Flagello, Proc. of SPIE Vol. 6154 615418 (SPIE, Bellingham, WA, 2006).

John H. Burnet, Eric C. Benck, Simon G. Kaplan, Gabriel Sirat, and Chris Mack, *"Birefringence issues with uniaxial crystals as last lens elements for high-index immersion lithography,"* SPIE Advance Lithography 7274, 727473 (2009).

James Jacob, John Hoffnagle, John Burnett, Eric Benck, Darrell Armstrong, and Arlee Smith, *"Full-field Liquid Immersion Interference Lithography,"* 6th International Symposium on Immersion Lithography Extensions, Prague, 22-23 October 2009

Metrology Supporting Extreme Ultraviolet Lithography

Technical Contacts:
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C. Tarrio
S. Grantham
S. Hill
R. Vest

Goals

Provide leading-edge EUV metrology for the characterization of sources, optics, detectors, and resist sensitivity; develop tests for predicting optics lifetime and resist qualification.

Customer Needs

An intense international effort is presently underway to install EUVL into commercial production in 2012 at the 22 nm node. ASML has delivered two alpha-generation steppers for initial testing and has orders for six pre-production tools that will begin to ship in the second half of 2010. Several significant challenges to commercialization of EUVL remain, including source power, optics lifetime, and mask fabrication and inspection. The associated metrological challenges include the development of: (1) reliable methods to qualify resists; (2) highly precise extreme ultraviolet (EUV) reflectometry; (3) accurate EUV radiometry for source comparisons, wafer-plane dosimetry, and resist characterization; and (4) predictors of EUV optics lifetimes.

Technical Strategy

1. Qualification of EUV Photoresists

EUVL tool manufacturers need to qualify photoresists based on their potential to degrade tool optics before allowing the resists to be introduced into the tool. A leading tool maker has developed a witness-plate test protocol for resist qualification that measures the degradation of an illuminated optic in the presence of a resist-coated wafer. NIST is in the process of installing a witness plate testing facility at its synchrotron light source (SURF III) for certification by the tool maker.

DELIVERABLES:

- A system to perform witness-plate tests to qualify photoresists (4Q2010).

2. Precise EUV Reflectometry

The NIST/DARPA EUV Reflectometry Facility is located on a multipurpose beamline on the NIST Synchrotron Ultraviolet Radiation Facility (SURF III) storage ring. Currently the NIST/DARPA facility is the only one in the U.S. large enough to measure optics up to 40 cm in diameter and 40 kg in mass. The facility has a demonstrated reflectivity accuracy of 0.3 % and wavelength accuracy of 0.001 nm, with plans underway to improve each in the near future.

The Facility serves the EUVL community by providing accurate measurements of multilayer mirror reflectivity and radiometric measurements on fully assembled instruments. Among the recent activities in support of EUVL is the reflectivity map made of the very large condenser mirror for a leading source manufacturer, the radiometric calibration of the "Flying Circus II" and "E-Mon" radiometers used for the comparison of source outputs, and reflectivity measurements made to determine the reflectivity loss due to resist outgassing. The reflectivity of a typical mirror designed for use in a EUVL stepper is shown in Fig. 1.

DELIVERABLES:

- Full reflectivity maps of EUV mirrors up to 40 cm in diameter and 45 kg in mass on an as needed basis for the EUVL community. Many other types of EUV measurements including EUV filter transmission and cw radiometric calibrations of fully assembled filter radiometers used in source comparisons.

3. EUV Dosimetry

NIST is the primary national source for the radiometric calibration of detectors from the infrared to the soft X-ray regions of the spectrum. The Photon Physics Group is responsible for maintaining the spectral responsivity standards in the far- and extreme-ultraviolet spectral regions,

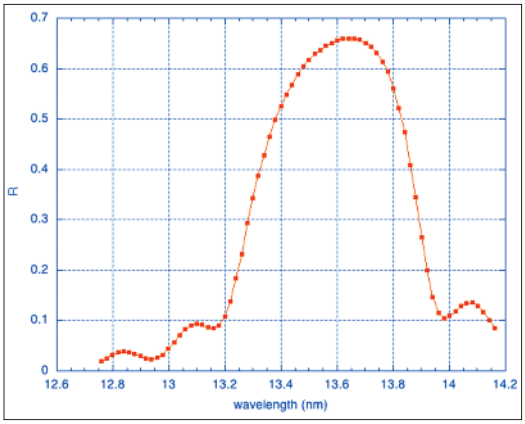

Figure 1. Reflectivity vs. wavelength of a typical MoSi multilayer mirror. The measurement was made at 5° from normal incidence.

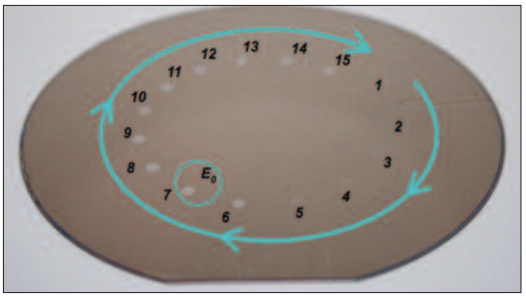

Figure 2. The dose to clear E_0 of a photoresist is determined by exposing multiple spots on a resist-coated Si wafer to increasing doses of EUV radiation. Spots 1 through 6 are underexposed and only partly developed; spots 8 through 15 are overexposed and image quality is degraded. Spot 7 is properly exposed – fully developed with sharp edges – and the corresponding dose is E_0.

including 13.5 nm, the EUVL wavelength of interest. We operate several beamlines at the SURF III synchrotron radiation facility for the calibration of EUV detectors and dosimeter packages.

NIST has recently added the capability to measure the absolute sensitivity of EUV photoresists. Until recently, EUV photoresist sensitivity was referenced to a "standard" photoresist whose sensitivity had last been measured in the 1990s. Late in 2007, scientists at the Advanced Light Source in Berkeley, CA used a NIST-calibrated EUV photodetector to validate this resist-based transfer standard method. Their detector-based measurements indicated that the sensitivity of a modern resist was about twice that obtained using the resist-based calibrations. Subsequently NIST established the capability for the accurate measurement of EUV resist sensitivity to independently validate these surprising results. The NIST measurements confirmed the findings of the much higher resist sensitivity made in Berkeley thus showing the resist-based standard that was used to be erroneous and demonstrating the importance of periodically checking such derived "standards" against measurements traceable to reliably calibrated instruments

DELIVERABLES:

- Photodiodes and other EUV radiometric devices as needed based on customer requests.
- Radiometric calibrations as needed based on customer requests.
- Resist dose to clear E_0 measurements on customer as needed based requests.

4. Study of Factors Affecting EUV Optics Lifetime

NIST has installed two beamlines at the SURF III that can expose capped-multilayer samples to 13.5 nm radiation in an environment of controlled water or hydrocarbon partial pressures. Degradation of the optics performance is determined by measuring the reflectivity loss of exposed multilayers. The photon-induced chemistry on the mirrors is characterized using a range of surface analysis techniques including micro-XPS.

The dominant mechanism of reflectivity loss of optics observed in pre-production tools has been carbon deposition. As shown in Fig. 3, high-dose exposures performed in our facilities have revealed very different rates of carbonization for different gases and a distinctly non-linear, quasi-logarithmic dependence of these rates on partial pressure. Ongoing work is focused on learning more about the pressure and intensity dependence of the carbonization rates in the very low pressure regions to allow for better predictions of such rates in an actual stepper.

Each of the various organic molecules emitted by an irradiated resist or other material in the stepper vacuum will have a different effect on the optics. NIST has devised two new methods in an attempt to identify and quantify both the organic species in a stepper vacuum and those emanating from an irradiated resist. The first uses a vacuum cryotrap to obtain a sample from a stepper vacuum which is later subjected to Gas Chromatography fol-

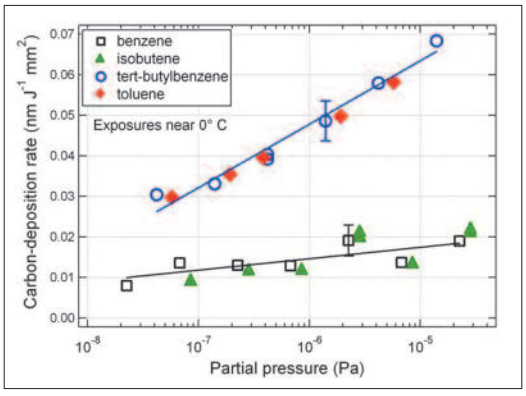

Figure 3. Carbon growth rates on TiO_2-capped trilayers samples for four anticipated contaminant gases. Straight-line fits for benzene and tert-butylbenzene show logarithmic pressure dependence across 3 decades of pressure. The error bars reflect the relative uncertainty due primarily to counting statistics of XPS measurements.

lowed by Mass Spectrometry (GC/MS) analysis in a specially equipped gas chromatograph, and the second uses a special chamber that can be hooked up to an EUV source to irradiate a 4 inch wafer, collect the outgas, and measure the total outgas per unit area by the pressure rise method and quantitatively analyze the collected outgas with the same cryo-trapping plus GC/MS technique as for the stepper vacuum.

DELIVERABLES:

- Identify and quantify EUV resist outgas components for resist manufacturers, tool makers, and
- Rank reflectivity loss as a function of organic species and the presence of mitigating oxidative species according to industry needs.

Collaborations

Rutgers University, Tulane University, CNSE at the State University in New York (Albany), Intel, Fraunhofer Institute, Jena, Germany, and SEMATECH

Publications

S. B. Hill, N. S. Faradzhev, L. J. Richter, and T. B. Lucatorto, *"Complex species and pressure dependence of intensity scaling laws for contamination rates of EUV optics determined by XPS and ellipsometry,"* Proc. SPIE, Vol. 7636, 76360E (2010)

S.B. Hill, N. Faradzhev, C. Tarrio, T.B. Lucatorto, B. Yaskshinkiy, T.E. Madey, and S. Yulin, *"Measuring the EUV-induced contamination rates of TiO_2-capped multilayers by anticipated tool-environment hydrocarbons,"* Proc. SPIE Vol. 7271, 7271-13 (2009).

C. Tarrio, S. Grantham, M. Cangemi, R.E. Vest, T.B. Lucatorto, and N. Harned, Proc. SPIE Vol. 7271, 7271-140 (2009).

C. Tarrio, R.E. Vest, T.B. Lucatorto, and R. Caudillo, *"Tracking down the sources of carbon contamination in EUVL exposure tools,"* Proc. SPIE Vol. 7271, 7271-38 (2009).

S. B. Hill, N. Faradzhev, C. Tarrio, T. B. Lucatorto, B. Yakshinskiy, R. Bartynski, *"EUV-induced carbon contamination of TiO2-capped multilayer optics: highly non-linear scaling and the effects of water vapor,"* poster at 2009 International Symposium on Extreme Ultraviolet Lithography, Prague, The Czech Republic (10/18/09)

S. Grantham, C. Tarrio, R. E. Vest, and T. B. Lucatorto, *"Metrology for EUVL Sources and Tools, in EUV Sources for Lithography,"* V. Bakshi, ed. (SPIE Press, Bellingham, WA, 2006).

Critical Dimension and Overlay Metrology Program

The principal productivity driver for the semiconductor manufacturing industry has been the ability to shrink linear dimensions. A key element of lithography is the ability to create reproducible undistorted images, both for masks and the images projected by these masks onto semiconductor structures. Lithography as a whole, fabricating the masks, printing and developing the images, and measuring the results, currently constitutes ≈35 % of wafer processing costs. The overall task of the Critical Dimension and Overlay Program is to assist the industry in providing the necessary metrology support for current and future generations of lithography technology. These goals include advances in modeling, the provision of next generation critical dimension and overlay artifacts, development of advanced critical dimension and overlay techniques, and comparisons of different critical dimension and overlay measurement techniques.

Currently, critical dimension and overlay measurement improvements have barely kept up with lithography capabilities. To maintain cost effectiveness, continued advances need to be made.

Wafer-level And Mask Critical Dimension Metrology

This project is the single largest project at NIST supporting the semiconductor industry. It involves metrology and artifact development across a broad range of techniques. For this reason, the project is presented in a number of sub-sections, each focusing on a single technology.

These are:

- Model-Based Linewidth Metrology
- Scanning Electron and Ion-Based Dimensional Metrology
- Scanning Probe Microscope-Based Dimensional Metrology
- Optical-Based Photomask Dimensional Metrology
- Scatterometry-Based Dimensional Metrology
- Small Angle X-Ray Scattering-Based Dimensional Metrology
- Grazing Incident X-Ray Scattering-Based Dimensional Metrology
- Atom-Based Dimensional Metrology
- Fabrication and Calibration Metrology for Single-Crystal CD Reference Materials

Model-Based Linewidth Metrology

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J. Villarrubia

""Stack materials, surface condition, line shape and even layout in the line vicinity may affect CD-SEM waveform and, therefore, extracted line CD. These effects, unless they are accurately modeled and corrected, increase measurement variation and total uncertainty of CD SEM measurements."

International Technology Roadmap for Semiconductors, Metrology Section, p. 8 (2009)

Goals

The goal of this project is to address the metrology needs of industry, particularly the U.S. semiconductor industry, in those areas that are particularly model-intensive, such as linewidth, contour, defect, and line edge roughness, where uncertainties on the order of 1 nm are required.

Customer Needs

In the semiconductor electronics industry the term "critical dimension" or "CD" is used nearly interchangeably with linewidth or gate width. Dimensions of the smallest features are critical in a number of respects: For a long time, speed increased with decreasing gate size. Even with decoupling of speed from size for the most advanced devices, size still determines device density. Lithography failures tend to manifest first in the smallest features, so monitoring for process control usually focuses on CD. Contour metrology (measuring the shape of the boundary of printed features) is used to compare printed features to the designed shape. Smaller critical features imply increased importance of small defects, which must be detected and in some cases inspected more closely. Roughness in transistor gates can affect both the values and variation of threshold voltages and leakage currents. Consequently, there is a need to measure widths, shapes, contours, and roughnesses, and a need to select instrument conditions that maximize defect detectability.

Required uncertainties on these dimensions are small. For example in 2011, the industry will need to measure gate electrode widths with total uncertainties, as identified in the International Technology Roadmap for Semiconductors (ITRS, 2009), of approximately 0.5 nm. The 2009 ITRS update specifies that linewidth roughness (LWR), measured as three standard deviations of the CD, must be less than 1.9 nm in 2011 and be measured with no more than 0.39 nm uncertainty.

Feature sizes and shapes must generally be determined from a microscope image. However, the image is not an exact replica of the line. The scanning electron microscope (SEM), scanning probe microscope (SPM), and optical microscope all have image artifacts that are important at the relevant size scales. Dimensional measurements therefore require modeling of the probe/sample interaction in order to correct image artifacts and identify edge locations. Barriers to accurate measurements include inadequate confidence in existing models, the complexity and consequent expense of using some models, inadequately quantified methods divergence, and ignorance of best measurement practices.

Technical Strategy

The most accurate metrology requires good instrumentation and measurement practices designed to minimize error. This is the experimental part, provided by other closely associated projects. It also requires a theoretical part which constitutes the scope of the model-based linewidth metrology project. Models of the measurement process provide an appropriate interpretation of the raw experimental results, an interpretation that includes (prior to the measurement) insight that leads to good measurement practices and (after the measurement) correction and/or quantification of remaining errors. The scope includes the development and improvement of computational models to simulate the artifacts introduced by measuring instruments, inversion of these models (to the extent possible) to deduce the sample geometry that produced a measured image, validation of models by appropriate experiments, development and testing of measurement processes that provide the necessary inputs for model-based deduction of sample width and shape, estimation of uncertainties for the measurement process, assistance to industrial measurements by communication of best practices, and laying of the necessary research groundwork for a future linewidth and/or line shape Standard Reference Material.

We have developed a model-based library (MBL) method of determining linewidth and line shape from top-down SEM images. The top-down measurement configuration is the one employed by industry CD-SEMs. Edge locations tell us a feature's width, its roughness, or in a larger field of view its contour. However, lines with different sidewall geometries appear to have different widths when measured using algorithms that are standard today on CD-SEMs.

"A better understanding of the relationship between the physical object and the waveform analyzed by the instrument is expected to improve CD measurement."

International Technology Roadmap for Semiconductors, Metrology Section, p. 7 (2009)

That is, sidewall variation masquerades as width variation. Accordingly, our method is a model-based algorithm that explicitly accounts for the physics of the interaction of the electron beam with the sample and the effect of sidewall geometry. MBL matches a measured image by interpolating a precomputed library of images. Because interpolation is fast, even computationally intensive models can improve measurements. This method has yielded encouraging results. These results establish a direct link between the quality of SEM models and the accuracy of metrology that can be performed using them.

This has brought renewed focus on the quality of the models. Our original MONSEL model was restricted to samples that fell within well-defined and restricted classes, for example lines of uniform cross section on a layered substrate. Many samples of industrial interest did not meet these restrictions. In 2007, we translated MONSEL to Java (renaming it JMONSEL), and substantially revised the method of geometrical descriptions, thereby extending the capabilities to permit simulation of other industrially important sample shapes, such as rough-edged lines, contact holes, lines with a footing, FinFETs, or defects.

Besides the sample geometry issue, it has become increasingly clear that the physics in existing SEM models was not accurate at energies below a few hundred electron volts. At these energies, electrons in the sample have time to adjust to the incoming electron, effectively screening the interaction and reducing the amount of scattering. Unfortunately, this low energy regime is precisely the one that is important for industrial SEMs, which (owing to the sensitivity of photoresist) employ electron landing energies less than about 1 keV, secondary electron (SE) imaging (which is by definition low energy, since SE are generated with average energies below 50 eV), and strong electric fields to extract SE that escape the sample. Moreover, these model inaccuracies are likely to affect dimensional measurements because they cause such dimensionally relevant parameters as electron escape depths to be greatly underestimated.

We implemented and evaluated a model to correct the aforementioned deficiencies in 2008. Fortunately, the groundwork for an improved model had already been laid in 1960s and 1970s in the form of many-body dielectric function theory (DFT). Those developments were applicable only to a few metals with particularly simple band structure, but NIST's Cedric Powell proposed and David Penn later demonstrated a method for extending DFT to a vastly larger set of materials by using those materials' optically measured dielectric functions. Penn's method later became the basis for a NIST standard reference database (SRD71) of inelastic electron mean free paths. The same model has now been elaborated into JMONSEL's simulator for secondary electron generation and successfully tested for Cu and Si. In 2009 we developed the ability to apply this DFT-based scattering model to insulating materials, and we calculated scattering tables for 15 additional materials. We added the ability to model phonon scattering, charge trapping, and included options for the choice of elastic scattering model.

Many samples of interest have insulating regions, so our 2010 activities are focused on adding a capability to model charging. The previous work on scattering models was a prerequisite for a successful charge model, because inelastic scattering determines the range of incoming electrons (hence where they stop) as well as the number, energy, range, and possible escape of secondary electrons. These all in turn determine the charge distribution within the sample. The charge distribution is, however, only a starting point. From this distribution it is necessary to determine the electric fields and to include the effect of those fields upon the electron trajectories in the simulation. Our work this year also includes some "proof of concept" simulations for defect and contour metrology.

DELIVERABLES:

- Write code to interpolate NIST Standard Reference Database 64 tables for elastic scattering model. 4Q 2009
- Compute scattering tables for materials currently not available (forms of carbon, PMMA). 4Q 2009
- Develop a plan for how to model charging of samples in the SEM. (1Q 2010)
- Develop Java classes to track charges. (2Q 2010)
- Develop code to determine electric fields in the presence of charge distributions (3Q 2010)
- Modify transport algorithms to include the effect of electric fields (3Q 2010)

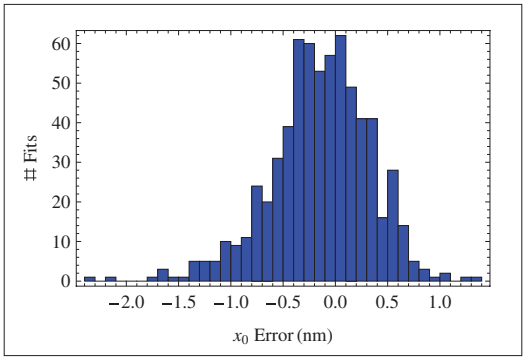

Figure 1. Histograms of edge position error in 662 fits at 1 keV landing energy with a Gaussian beam (standard deviation = 1 nm). Edge positions were determined by 8 different models or model variants for 100 nm tall trapezoidal Si lines with edge angles ranging between 0 ° and 10 °.

- Perform simulations for a sample specified by SEMATECH from their intentional defect array library (1Q 2010)
- Present a paper on errors in contour metrology at • SPIE Advanced Lithography (1Q 2010)
- Provide oral reports to SEMATECH (1Q 2010 and 3Q 2010)
- Make software publicly available (4Q 2010)

Accomplishments

Critical dimension uncertainty associated with the model

The error in a measurement can be divided into a random part and an offset or bias (often called the "systematic" error). The former is easily quantified by repeated measurements of the same feature (a "precision" test). In modern CD-SEMs, it can be a fraction of a nanometer. The latter is not so easily quantified. It is often (with more hope than reason) assumed not to matter in measurement comparisons because it is constant. However, while this error is by definition constant in repeated measurements of the same feature, for two different features (e.g., with different shapes or different environments) these errors need not be the same. That is, the bias can be a function of feature shape, environment, or other variables that were held constant during the precision test. The a priori uncertainty for a crude model, one that says the actual edge is somewhere inside the SEM intensity peak associated with the edge, is on the order of the peak width, 10 nm or more; offsets of this size have been observed in comparisons between SEM and TEM or AFM. If we assigned the edge position based upon the right model (nature's own model) our error would be 0. Unfortunately, we don't know nature's model. There are a number of candidates. Differences between them give some indication in the extent of our uncertainty. A large number of simulations using different models and different edge angles produced results in the Fig.1 histogram. (Widths were within 2 nm 95 % of the time.)

Simulations of intentional defect arrays

Samples fabricated with intentional defects may be used to test defect inspection tools. In Figure 2, the image on the left is from such a sample (courtesy of ISMI). The image on the right was a simulation performed at ISMI request to demonstrate JMONSEL. In formulating the sample geometry that JMONSEL was to simulate, no attempt was made to capture fine details (corner rounding, surface texture) of the actual sample. Nevertheless, there are evident similarities in such image features as edge bloom and darkening of the average brightness in confined spaces.

Contour metrology

JMONSEL simulations indicated that contours of constant brightness in an image of a straight-edged line undergo an apparent shift in position when the edge transitions between a region where it is isolated and one where it has nearby neighbors. The shift is due to the same phenomenon that caused the darkening in Fig. 2. Some of the secondary electrons produced in these areas are recaptured by the sample when they are intercepted by the neighboring structures. This shift is shown in the Fig. 3 simulation. The shift represents a contour metrology error of about 1 nm. In real samples there is a real change in the edge at an isolated/dense transition due to lithography and etch effects. The real change may

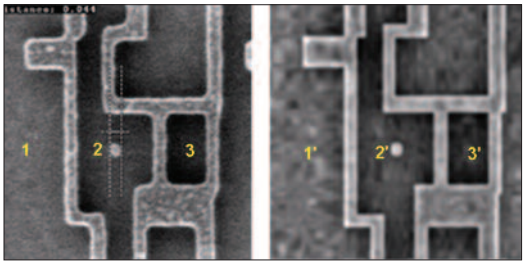

Figure 2. Comparison of measured (left, image courtesy of ISMI) and simulated (right) images of an intentional defect array structure. Neighborhoods 1, 2, and 3 (with primes in the simulation) are progressively more confined and also progressively darker.

"Due to the changing aspect ratios of IC features, besides the traditional lateral feature size (for example, linewidth measurement) full three-dimensional shape measurements are gaining importance and should be available inline."

International Technology Roadmap for Semiconductors, Metrology Section, p. 6 (2009)

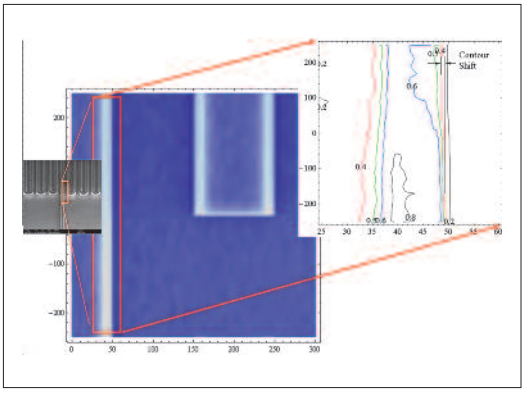

Figure 3. Modeled isolated/dense contour shifts in AMAG6L pattern. The small image at the left is an oblique-incidence SEM image of the sample upon which the simulated sample was based. The upper part of the sample is periodic with nominally 100 nm lines and spaces. A single line is longer than the others, becoming an isolated line in the lower half of the image. The corresponding modeled image is shown in the middle. The indicated region is drawn as a contour plot at the upper right, with the horizontal axis expanded and the shift of one of the contours indicated.

be an order of magnitude larger than the predicted metrology error, so separating the two experimentally is difficult. Nevertheless, careful comparison of SEM and AFM images of the same sample confirm the effect. Moreover, modeling indicates that the error is significantly smaller if the contour edge is assigned using relative instead of absolute intensity.

Collaborations

International SEMATECH

Hitachi, Ltd., Maki Tanaka.

Illinois Institute of Technology, Prof. Xiaoping Qian

Publications

J.S. Villarrubia, R.D. Dixson, and A.E. Vladár, *"Proximity-associated errors in contour metrology,"* Proc. SPIE 7638 (2010).

J.S. Villarrubia and Z.J. Ding, *"Sensitivity of scanning electron microscope width measurements to model assumptions,"* J. Micro/Nanolith. MEMS MOEMS 8, 033003 (2009).

F. Tian, X. Qian, and J. S. Villarrubia, *"Blind estimation of general tip shape in AFM imaging,"* Ultramicroscopy 109, 44-53 (2008).

X. Qian and J. S. Villarrubia, *"General Three-Dimensional Image Simulation and Surface Reconstruction in Scanning Probe Microscopy using a Dexel Representation,"* Ultramicroscopy, 2007.

J. S. Villarrubia, N. W. M. Ritchie, and J. R. Lowney, *"Monte Carlo modeling of secondary electron imaging in three dimensions,"* Proc. SPIE 6518 (2007).

Xiaoping Qian, John Villarrubia, Fenglei Tian, and Ronald Dixson, *"Image Simulation and Surface Reconstruction of Undercut Features in Atomic Force Microscopy,"* Proc. SPIE 6518 (2007).

R. Katz, C. D. Chase, R. Kris, R. Peltinov, J. Villarrubia, and B. Bunday, *"Bias reduction in roughness measurement through SEM noise removal,"* Proc. SPIE 6152, 61524L, (2006)

J. S. Villarrubia and B. D. Bunday, *"Unbiased Estimation of Linewidth Roughness,"* Proc. SPIE 5752, p. 480 (2005).

J. S. Villarrubia, A. E. Vladár, and M. T. Postek, *"Scanning electron microscope dimensional metrology using a model-based library,"* Surf. Interface Anal., 37, p. 951 (2005).

M. Tanaka, J. S. Villarrubia, and A. E. Vladár, *"Influence of Focus Variation on Linewidth Measurements,"* Proc. SPIE 5752, p. 144 (2005).

J. S. Villarrubia, *"Tip Characterization for Dimensional Nanometrology,"* in Applied Scanning Probe Methods, eds. B. Bhushan, H. Fuchs, and S. Hosaka, p. 147 (Springer-Verlag, Berlin Heidelberg 2004).

Scanning Electron and Ion-Based Dimensional Metrology

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Goals

Provide the microelectronics industry with highly accurate scanning electron microscope (SEM) measurement and modeling methods for shape-sensitive measurements and relevant calibration standards with nanometer-level resolution.

Carry out SEM metrology instrumentation development, including improvements in electron and ion optical system, detection, sample stage, and vacuum system.

Conduct research and development of new metrology techniques using digital imaging and networked measurement tools solutions to key metrology issues confronting the semiconductor lithography industry.

Customer Needs

The scanning electron microscope is used extensively in many industries, including the more than $200 billion semiconductor industry in the manufacture and quality control of semiconductor devices. The International Technology Roadmap for Semiconductors (2009) states that "Scanning Electron Microscopy continues to provide at-line and inline imaging for characterization of cross-sectional samples, particle and defect analysis, in-line defect imaging (defect review), and critical dimension (CD) measurements. Improvements are needed for effective CD and defect review (and SEM detection in pilot lines) at or beyond the 45 nm generation." The semiconductor industry needs SEM standard artifacts, specifically those related to instrument magnification calibration, performance and the measurement of linewidth. This entails a multidimensional program including: detailed research on signal generation in the SEM, electron beam-sample interaction modeling, developing NIST metrology instruments for the certification of standards, and developing the necessary artifacts and calibration procedures. The manufacturing of present-day integrated circuits requires that certain measurements be made of structures with dimensions of 45 nm or less with a very high degree of precision. The accuracy of these measurements is also important, but more so in the development and pilot lines. Measurements of the minimum feature size, known as CD, are made to ensure proper device operation. The U.S. industry needs high-precision, accurate, shape-sensitive dimension measurement methods and relevant calibration standards. The SEM Metrology Project supports all aspects of this need since scanning electron microscopy is the key microscopic technique used for sub-100 nm metrology.

Technical Strategy

The Scanning Electron Microscope Metrology Project, a multidimensional project, is being executed through several thrusts fully supported by the semiconductor industry.

1. SEM Magnification Calibration Artifacts: Essential to SEM dimensional metrology is the calibration of the magnification of the instrument. Standard Reference Material (SRM) 2120 is an SEM magnification standard that will function at the low beam voltages used in the semiconductor industry and high beam voltages used in other forms of microscopy. Conventional optical lithography provides the opportunity to produce a large quantity of good quality samples that can be produced inexpensively. Because of the improvements of this technology, it is now possible to produce the finest lines with close to 100 nm width and with 200 nm pitch values. The largest pitch is 1500 µm. In order to make this artifact available (while the final certification details are being completed) the artifact is now released as Reference Material (RM) 8820 (Fig. 1).

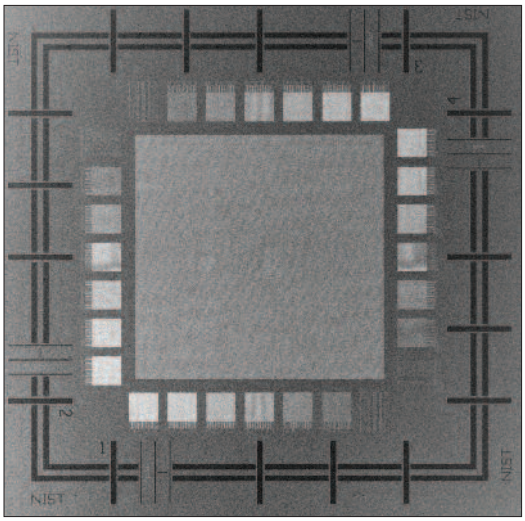

Figure 1. SEM image of the complete RM 8820 Magnification calibration standard reference material.

"Scanning Electron Microscopy (SEM) – continues to provide at-line and in-line imaging … and CD measurements. Improvements are needed … at or beyond the 45 nm generation … Determination of the real 3-D shape…will require continuing advances in existing microscopy …"

International Technology Roadmap for Semiconductors, 2009

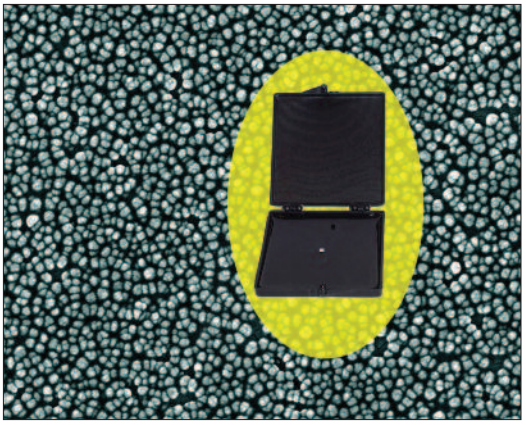

Figure 2. The RM 9081 Sharpness Reference Material.

DELIVERABLES:

- Complete calibration and delivery of a new batch of SRM 2120 samples. 4Q 2010

2. SEM Performance Measurement Artifacts and Software Solutions: This effort included the development of the Reference Material 8091 (Fig. 2.) and evaluation procedures suitable for correctly measuring image sharpness of scanning electron microscopes, especially of those that are used in the semiconductor industry. Currently we are working with ISO to develop robust software solutions that will allow for resolution performance tracking of SEMs. The resolution performance characteristics of the SEM are particularly important to precise and accurate measurements needed for semiconductor processing. As a part of this effort the NIST SEM Resolution Measurement Reference Image Set was worked out to test the resolution measurement software themselves. This Reference Image Set contains a large number of artificial images that were made by taking into account the amount and type of de-focusing, noise, vibration and drift and electron landing energies. Suitable samples are being sought to further improve this type of metrology (Fig. 3). Several samples have been purchased by leading semiconductor manufacturing companies and these measurement artifacts are used in the benchmarking efforts of International SEMATECH. The existence of these samples fosters better understanding, objective measurement and enforcement of SEM spatial resolution performance.

3. SEM Linewidth Measurement Artifacts: Artifacts that are characterized and calibrated to the required levels of uncertainty continue to be focal point of the IC industry's dimensional metrology needs. Therefore, at NIST, it has been a long-term goal to develop and deliver appropriate samples . For a long time, the possibilities were limited by the lack of various technologies available, especially the lack of accurate modeling methods. NIST, through several years of systematic efforts, developed Monte Carlo simulation-based modeling methods that can deliver excellent results. These new methods can deduce the shape of integrated circuit structures from top-down view images through modeling and library-based measurement techniques with an uncertainty of a few nm. In several publications, NIST demonstrated the possibilities and described the power of this measuring approach. Based on the newest results, it is now possible to start to develop the long-awaited relevant line width standard for the semiconductor industry. Reference Material 8120 line width sample will be a relevant sample on 200 mm and 300 mm Si wafers with polySi features with sizes from 1 mm to down to 50 nm. Standard Reference Material 2120 is going to be the calibrated, traceable version for line width measurements. This work is being carried out in cooperation with SEMATECH.

A new effort is underway that is aimed at the development of two new Reference SEMs. One with full-size wafer and mask capability is based

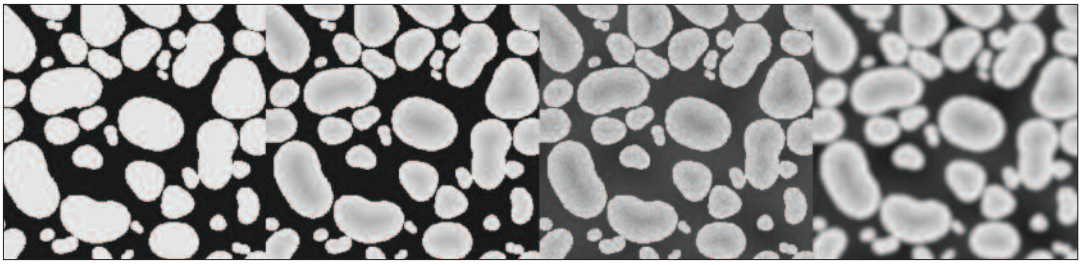

Figure 3. Images that illustrate the image simulation steps for the NIST SEM Resolution Measurement Reference Image Set.

on an environmental SEM (ESEM), which is very important with charging samples such as quartz masks. The other Reference instrument based on a dual-beam SEM, and will be capable to work with mask- and smaller size samples. Both microscopes will use the same type of 38 pm resolution laser interferometry, which provides traceability and it allows for compensation for stage drift and vibration at the nm level. These instruments are now operational, and the work is underway to improve the measurement uncertainty.

DELIVERABLES:

- Fabrication of line width metrology litho artifact suitable for calibration on NIST and external measuring systems for certification of wafer and chip format line width samples. 3Q 2010
- Completion of preliminary measurements on litho samples made by SEMATECH with the new "NIST-MAG" metrology mask. 4Q 2010

4. Helium Ion Microscopy - a Promising New Technique for Semiconductor Metrology and Lithography: The Helium Ion Microscope (HIM) offers a new, potentially disruptive technique for nano-metrology. This methodology presents an approach to measurements for nanotechnology and nano-manufacturing which has several potential advantages over the traditional SEM currently in use in integrated circuit research and manufacturing facilities across the world. Due to the very small, essentially one atom size, very high brightness source, and the shorter wavelength of the helium ions, it is theoretically possible to focus the ion beam into a smaller probe size relative to that of an electron beam of current SEMs. Hence higher resolution is theoretically achievable. In contrast to the SEM, when the helium ion beam interacts with the sample, it generates significantly smaller excitation volume and thus the image collected is more surface sensitive. Similarly to the SEM, the HIM also produces topographic, material, crystallographic, and potential contrast, and offers ways for investigating new sample properties through the use of various detectors. Compared to an SEM, the secondary electron yield is quite high, allowing for imaging at very low beam currents, thus resulting in less sample damage. Additionally, due to the low mass of the helium ion, the He beam does not mill the sample at as high rate as gallium ions that are regularly used for ion milling, but with larger beam currents can be used for finer milling and cutting.

DELIVERABLES:

- Completion of detailed measurements and quality assessment of the imaging, lithography and nano-milling capability of the HIM using amorphous Si litho and other samples made by SEMATECH and phase shifting photomasks. 4Q 2010

Accomplishments

SEM Magnification Calibration Artifacts – Samples for Reference Material 8820 have been made successfully in the past using 193 nm UV lithography, but later attempts with e-beam lithography yielded no useful samples. We delivered to NIST Office of Reference Materials 100 pieces of RM 8820, which were fabricated at International SEMATECH, using 193 nm UV light lithography. The finest features are 100 nm wide with a 200 nm pitch. The largest pitch is 1500 nm. There are a large number of 250 nm wide crosses and grids for distortion and other measurements. Scatterometry patterns with varying pitches will also be available. The features on the conductive Si wafer will be formed from amorphous Si material. These samples give suitable contrast in any SEM to allow the user to set the magnification of the instrument from the smallest to the highest magnifications. The first wafers containing the final design were fabricated by International SEMATECH and found to be useful. These will be calibrated when the new metrology SEM and its laser interferometer sample stage are set up and running properly.

SEM Performance Measurements – After comprehensive studies and experiments a plasma-etching Si called "grass" was chosen for Reference Material 8091 (Fig. 2). This sample has 5 nm to 25 nm size structures as is illustrated in the figure below. There have been 75 samples delivered to the Office of Standard Reference Materials, NIST. A sharpness standard and evaluation procedure have been developed to monitor (or compare) SEM image quality. A NIST kurtosis method, Spectel Company's user-friendly analysis system called SEM Monitor, and University of Tennessee's SMART algorithm can be used with RM 8091. An effort is underway to produce more of these samples. These samples are now available to the public, and many of them are already in use. There is a new ISO standard under development that is introducing a method to reliably measure the resolution performance of SEMs; this method is also working well with RM 8091 samples.

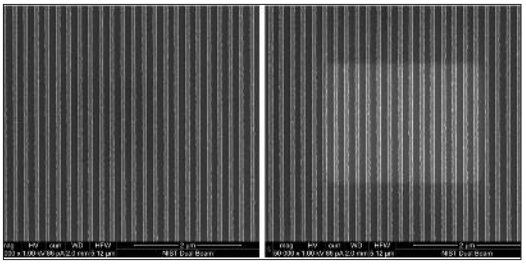

Figure 4. Contamination-free SEM operation. 1 kV, 86 pA SEM images of amorphous Si patterns at the beginning of the test (left) and after 10 minutes (right) of continuous electron beam bombardment. Actual cleaning and more signal are observable. 5 µm field-of-view images.

Contamination Specification for Dimensional Metrology SEMs – Electron beam-induced contamination is one of the most bothersome problems encountered in the use of the scanning electron microscope. Even in "clean-vacuum" instruments it is possible that the image gradually darkens because a polymerized hydrocarbon layer with low secondary electron yield is deposited. This contamination layer can get so thick that it noticeably changes the size and shape of the small structures of current and future state-of-the art integrated circuits (ICs). Contamination greatly disturbs or hinders the measurement process and the erroneous results can lead to wrong process control decisions. NIST has developed cleaning procedures and a contamination specification that offer an effective and viable solution for this problem. By the acceptance, implementation and regular use of these methods it is possible to get rid of electron beam induced contamination.

SEM Linewidth Measurement Artifacts – For correct linewidth measurements accurate modeling methods are indispensable. The existing NIST methods have shown excellent results on polySi samples and they are under further development for higher accuracy. From a top-down view and using our high-accuracy modeling and fitting methods, a cross section of the lines can be determined with uncertainties and discrepancies within a few nm. The match is so good that this method may be capable of eliminating the costly and destructive cross sectional SEM measurements. The candidate sample for linewidth artifact must be relevant to state-of-the-art IC technologies, should have chips on 200 mm and later 300 mm wafers with all process variation and include a meaningful focus-exposure matrix (FEM). The design and the fabrication of the SEMATECH/NIST mask have been successfully completed. After CD-SEM measurements at SEMATECH, cross sectional measurements will be made at NIST. All of these measurements will yield an excellent database for a decision on how to proceed with this wafer type linewidth reference sample. It is likely that by the end of the year 2010 the Reference Material 8120 line width samples will be available. This work is being carried out in close cooperation with SEMATECH.

Development of High Accuracy Laser Interferometer Sample Stage for SEMs – The development of a very fast, very accurate laser stage measurement system facilitates a new method to enhance the image and line scan resolution of SEMs. This method, allows for fast signal intensity and displacement measurements, and can report hundreds of thousands of measurement points in just a few seconds. It is possible then, to account for the stage position in almost real time with a resolution of 0.04 nm. The extent and direction of the stage motion reveal important characteristics of the stage vibration and drift, and helps minimize them. Figure 5 shows the key elements of the laser interferometer of the sample stage, the fiber laser beam delivery, the area detector, the interferometer and the detection scheme. The high accuracy and speed also allow for a convenient and effective technique for diminishing these problems by correlating instantaneous position and imaging intensity. The new measurement technique developed recently gives a possibility for significantly improving SEM-based dimensional measurement quality. Important new discoveries made it possible to correctly understand the motion of the stage at the nm level, and to characterize various settings and fine

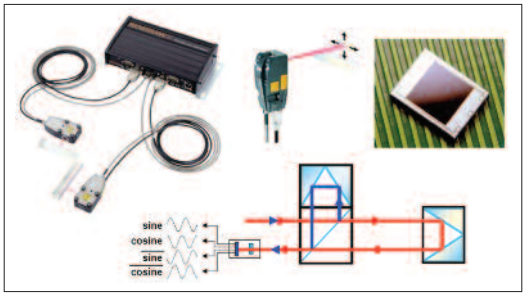

Figure 5. Laser interferometer system of the NIST Reference SEMs. Fiber-based beam delivery (upper left corner) Differential interferometer (upper center) Phase sensitive detector (upper right) and the detection scheme (lower center). (Courtesy of Renishaw Plc.).

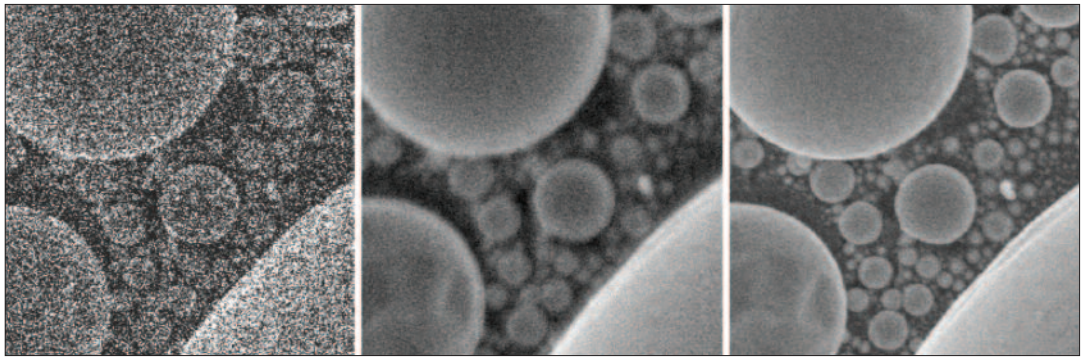

Figure 6. Single image acquired in 11 μs frame time (50 ns pixel dwell time) (left), traditionally averaged 70 images (middle), and the same 70 images averaged with the new, adaptive method (right). 4617 nm field-of-view images.

tune the sample stage, which is critical for high-resolution work.

Development of New Imaging Method with Adaptive Averaging of Super-Fast SEM Images – Modern SEMs acquire images by assigning signal intensity values to pixels that are arranged into a two-dimensional array - a digital image. If the image acquisition is done with long pixel dwell times and/or long frame times, then the image may be blurred and/or distorted. Essentially, all SEM images are taken on moving targets; therefore, unless corrective methods are used, all pixels also contain information that belongs to other pixels. Unfortunately, in most high-magnification SEMs, both high and low frequency motions occur. The high frequency vibrations cause blurring while low frequency drifts lead to distortions. The new imaging method uses adaptive averaging of super-fast SEM images (taken at the highest sampling rates). It finds the shift vectors for all individual images and shifts them to their correct location. The shift vectors are calculated with sub-pixel resolution using cross-correlation of the images computed using the Fourier transform.

Development of Accurate and Highly Repeatable Contour Dimensional Metrology – Optical lithography is printing photo resist features that are significantly smaller than the wavelength of the light used, and therefore it is essential to use optical proximity correction (OPC) methods. This includes modeling and compensation for various errors in the lithography process down to sub-nanometer, essentially atomic levels. Unfortunately, there are many shortcomings of the current SEMs that make it impossible to achieve excellent accuracy and repeatability, especially at high magnifications.

In a recent NIST-SEMATECH project, advanced image and data collection methods were adapted to contour metrology and sound, physics-based modeled measurement methods were developed for accurate and repeatable shape and size measurements on IC resist lines, contact holes and particularly on OPC structures. These methods allow for valid comparisons of the measurement results of various instruments and methods and also serve as the foundation for future calibrations of various artifacts, including wafers and photo masks. Rigorous, Monte Carlo modeling and very fast analog modeling methods were also developed. These make it possible to optimize the measurement parameters and obtain the best contour measurement results.

One important fact of scanning electron microscopy is that structures (e.g. resist lines) that are close to each other influence the amount of signal arriving at the detector. The rigorous NIST model correctly accounts for this and thus it is more accurate. Figure 7 illustrates the intensity dependence upon the proximity of neighbors which is especially relevant for contour metrology. In contour metrology, the position of the edge of a feature is determined at close intervals along its perimeter. In this way, the shape of the boundary of the feature is ascertained. Also, the neighborhood of an edge is not constant along the perimeter of an object except even in the simplest of patterns. Since the perimeter of an object in general traverses varying neighborhoods, the proximity-dependence of edge assignment errors implies that the shapes will be incorrectly determined by some amount.

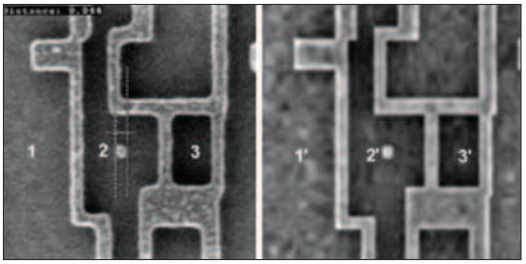

Figure 7. Measured (left, SEM image courtesy of ISMI) and simulated (right) images of OPC-generated structures that illustrate the effects of proximity. Neighborhoods 1, 2, and 3 are progressively more confined and also progressively darker. The thin lines are 30 nm wide.

The reason the intensity profile at an edge depends upon the proximity of neighbors is that some of the paths leading from the sample to the detector are obstructed for electrons that emerge from an edge in close proximity to a neighboring feature. The extent of the obstruction is greater if the neighbor is larger or closer. The effects of such obstruction are easily observable in images. Figure 7, for example, compares real and simulated images of a sample.

Development of Ultra-High Resolution He ion Microscope – The HIM technology is not yet as well optimized, developed or mature as the SEM. As a new technique, HIM is just beginning to show promise and many potentially advantageous applications for integrated circuit and nanotechnology have yet to be exploited. Now, that commercial instrumentation is available, further work is being done on the fundamental science of helium ion beam generation, helium ion beam-specimen interactions, and the signal generation and contrast mechanisms defining the image.

In addition to these areas of work, modeling needs to be developed to correctly interpret the signal generation mechanisms and to understand the imaging mechanisms. These are indispensable for accurate nanometer-level metrology. HIM and SEM have some overlapping territory, but they remain complementary techniques. Helium ion beam microscopy is evolving into new scientific and technology territories, and this new and innovative technology will develop new science and contribute to the progress in integrated circuit and nanotechnology.

Beyond high-resolution imaging, He ion beam is also useful for exposing of resist materials. Figure

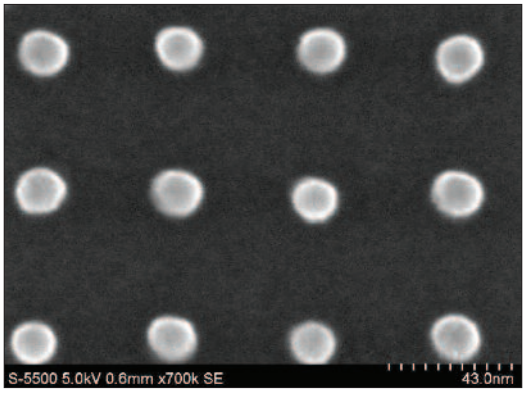

Figure 8. Dense array of 15 nm hydrogen silsesquioxane (HSQ) resist posts generated by He ion lithography. 180 nm field of view (right).

8 shows a dense array of approximately 15 nm diameter hydrogen silsesquioxane (HSQ) resist posts generated by He ion lithography. Smaller structures are also feasible and the sensitivity of resists to ion irradiation can be significantly higher than to electrons. This area is also being pursued to investigate how far ion-beam lithography can be pushed.

Collaborations

International SEMATECH, Advanced Metrology Advisory Group

International Technology Roadmap for Semiconductors; Microscopy and Metrology Sections

Zeiss/ALIS Corp.

FEI Co.

ISO

E. Fjeld Co.

Publications

A. E. Vladár, J. S. Villarrubia, and M. T. Postek *"Development of Accurate and Highly Repeatable Contour Dimensional Metrology for the Scanning Electron Microscope"* Final Report 2010.

J. S. Villarrubia, R. G. Dixson, and A. E. Vladár *"Proximity-associated errors in contour metrology"* SPIE Microlithography 2010.

A. S. Carasso and A. E. Vladar *"Fractional Diffusion, Low Exponent Levy Stable Laws, and 'Slow Motion' Denoising of Helium Ion Microscope Nanoscale Imagery"* In preparation 2010.

M. Oral and A. E. Vladár *"Optimization of SEM Imaging through 3D Modeling of Beam and Sample"* SCANNING Meeting Monterey May 2009.

P. Cizmar, A.E. Vladár and M. T. Postek *"Image Simulation for Testing of SEM Resolution Measurement"* Methods SCANNING Meeting Monterey May 2009.

A. E. Vladár and M. T. Postek *"Development of Reference Critical Dimension Metrology Scanning Electron Microscope"* SEMATECH Final Report 2008.

A. E. Vladár, K. P. Purushotham and M. T. Postek *"Contamination Specification for Dimensional Metrology SEMs"* SPIE Microlithography 2008.

M. T. Postek, A. E. Vladár *"The Potentials of Helium Ion Microscopy for Semiconductor Process Metrology"* SPIE Microlithography 2008.

A. E. Vladár, J. S. Villarrubia, P. Cizmar, M. Oral and M. T. Postek *"Accurate and Traceable Dimensional Metrology with a Reference CD-SEM"* SPIE Microlithography 2008.

M. T. Postek, A. E. Vladar, J. Kramar, W. Ward, L. A. Stern, J. Notte and S. McVey, *"Helium Ion Microscopy: a New Technique for Semiconductor Metrology and Nanotechnology"* Scanning 2007.

M. T. Postek, A. E. Vladar, J. A. Kramar, L. A. Stern, J. Notte, S. McVey, *"The Helium Ion Microscope: A New Tool for Nanotechnology and Nanomanufacturing"* SPIE 2007.

M. T. Postek, A. E. Vladar, J. A. Kramar, L. A. Stern, J. Notte, S. McVey, *"Helium Ion Microscopy: A New Technique for Semiconductor Metrology and Nanotechnology"* International Conference on Frontiers of Characterization and Metrology for Nanoelectronics 2007.

Scanning Probe Microscope-Based Dimensional Metrology

Technical Contacts:
R. Dixson
G. Orji
J. Fu

Goals

Improve the measurement uncertainty of critical-dimension measurements in the semiconductor industry through improvements in scanning probe microscope-based measurements. *The International Technology Roadmap for Semiconductors* (ITRS) identifies dimensional metrology as a key enabling technology for the development of next-generation integrated circuits. For example, according to the 2009 Edition of the ITRS, the goal in 2010 for critical dimension (CD) measurement uncertainty for isolated lines was ± 0.55 nm; this demand tightens to ± 0.35 nm by 2015.

Although most in-line metrology is performed using scanning electron microscopes (SEM) and scatterometry, these instruments are not presently capable of first-principles accuracy. That is, they must be calibrated using reference measurements from a tool or combination of tools which is capable of intrinsic accuracy. Such a tool is now referred to as a reference measurement system (RMS), and the 2009 update of the ITRS highlights the growing importance of an RMS. The use of atomic force microscope (AFM) and transmission electron microscope (TEM) cross measurements section for this purpose – often in combination – is now a fairly common practice in the industry.

The technical focus of this project, development and implementation of scanning probe microscope instrumentation for traceable dimensional metrology, is thus driven by the anticipated industry needs for reduced measurement uncertainty for in-line metrology tools such as the SEM and scatterometer – since these in turn rely on reduced measurement uncertainty for techniques such as AFM that are often implemented as an RM.

Customer Needs

SEM is still the current tool of choice for inspection and metrology of sub-100 nm features in the semiconductor industry. Scatterometry or optical critical dimension (OCD) metrology is also rapidly gaining acceptance as an in-line process metrology tool. Scanning probe microscopes (SPMs) possess unique capabilities, which may significantly enhance the performance of SEMs for in-line CD measurements, and are also emerging as CD measurement tools in their own right. A creative strategy, which successfully harnesses the strong points of both techniques in order to reduce the measurement uncertainty of sub-100 nm features, will help NIST meet the expectations of the semiconductor industry expressed in the current ITRS. As is the case with SEMs, the magnification or scale of an SPM must be calibrated in order to perform accurate measurements. Although many SPMs are commercially available, appropriate calibration standards have lagged. In particular, the availability of traceable pitch, height, and width standards in this regime is limited.

Technical Strategy

The SPM dimensional metrology program consists of three inter-related thrusts: The first two thrusts address SPM dimensional metrology with two in-house research instruments at NIST, and the third thrust involves a partnership with SEMATECH to maintain traceability on a commercially available in-line SPM housed in the manufacturing facility at SEMATECH. The two instruments housed at NIST are a calibrated atomic force microscope (C-AFM) for measurement of pitch and step height and a critical dimension atomic force microscope (CD-AFM) for measurement of linewidth.

The C-AFM is a custom built instrument that has metrology traceable to the wavelength of light for all three axes of motion, and it has provided cal-

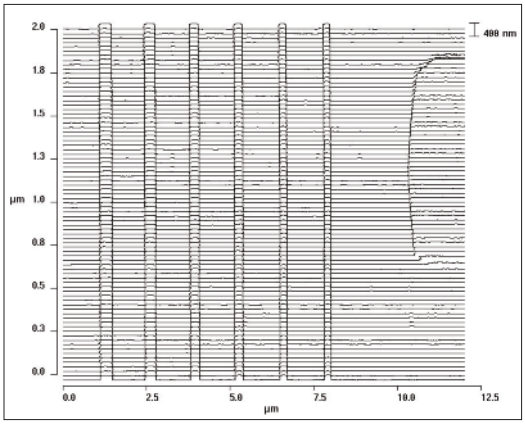

Figure 1. CD-AFM image of a NIST45 SCCDRM specimen which can be used for tip width calibration.

ibrated pitch and height measurements for a variety of nano-scale applications. Pitch measurements in the 1000 nm regime and below can currently be performed with relative standard uncertainties as low as 5×10^{-4}, and step height measurements up to several hundred nanometers can be performed with a relative standard uncertainty now approaching 1×10^{-3}. The C-AFM has participated in two international comparisons of sub-micrometer pitch measurements and one comparison of step height measurements.

DELIVERABLES:

- Performed initial measurements on secondary SRM 2059 photomask – which will be used in a bilateral comparison between NIST and the National Metrology Institute of Germany, Physikalisch-Technische Bundesanstalt (PTB) – using traceable CD-AFM metrology. 3Q2009
- Performed C-AFM measurements on traceable 70 nm pitch standard with A-Star (the NMI in Singapore) and Advanced Surface Microscopy (ASM) – a commercial standards vendor. 4Q2009
- Organized, hosted, and ran an evening panel discussion at SPIE Advanced Lithography Meeting on Strategies for Optimizing the Value of Metrology and Inspection. 1Q2010
- Perform CD-AFM measurements on AMTC masks to support the Nano1 international comparison of linewidth measurements. 3Q2010

The second and third thrusts involve the most commonly used AFM-based method of linewidth metrology in industry: CD-AFM. This type of instrument is more sophisticated than conventional AFM and used a flared shape probe and two-dimensional feedback to image the sidewalls of near-vertical structures. The SXM320 is a prior generation commercially available CD-AFM. Ini-

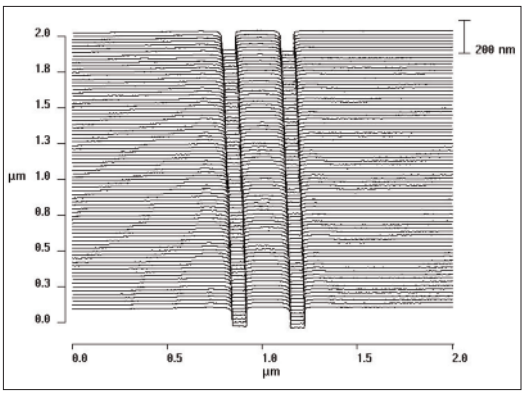

Figure 2. CD-AFM image of a commercial linewidth standard that we measured at NIST to compare the reference calibrations..

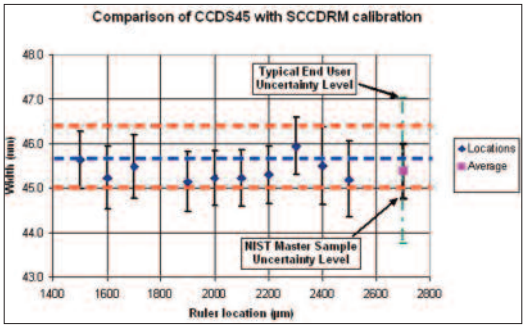

Figure 3. Comparison of SCCDRM master calibration with a commercial CD standard of nominal 45 nm width. The blue line shows the nominal CCDS45 calibration as determined by the vendor and the red dashed lines the expanded uncertainties. The NIST CD-AFM measurements of the CCDS45 used the SCCDRM master calibration. The calibrations are in excellent agreement and within the uncertainties.

tially, this instrument was used to implement the CD-AFM/RMS at SEMATECH during the tenure of Ronald Dixson as the first NIST Guest Scientist there. Now that the instrument is housed at NIST, the uncertainties have been further refined. Currently, pitch measurements can be performed with a relative standard uncertainty of approximately 2×10^{-3}. Step height measurements have a relative standard uncertainty 4×10^{-3}, and linewidth measurements can have standard uncertainties as low as 1 nm. This is a result of the most current release of NIST single crystal critical dimension reference materials (SCCDRM) that was completed in 2005.

The third thrust involves collaboration with ISMI/SEMATECH to establish a traceable CD-AFM (RMS) in their new facilities in Albany. This thrust involves migration of the RMS methodology from the prior Dimension X3D platform to the new Insight3D platform. George Orji, who was the second NIST Guest Scientist at SEMATECH, is continuing to oversee this thrust following his return to NIST.

As is true for the SXM at NIST, the SCCDRM project has resulted in the ability to perform linewidth measurements with a standard uncertainty of 1 nm. The relative uncertainties in pitch and height measurements using the X3D were reduced to 1×10^{-3} and 2×10^{-3}, respectively. Further reductions are anticipated when the RMS methodology is fully implemented on the Insight3D.

DELIVERABLES:

- Collaborated with ISMI/SEMATECH personnel to implement Reference Measurement System (RMS) methodology on the new Insight3D CD-AFM that will be installed in ISMI facilities in Albany. 1Q2010
- Performed new TEM reference width calibration experiment in collaboration with ISMI/SEMATECH and SVTC using an aberration corrected TEM at ORNL. 1Q2010

Accomplishments

■ The NIST/SEMATECH partnership in advancing AFM metrology in semiconductor manufacturing continues. After a tenure of more than three years as the second NIST Guest Scientist at SEMATECH, George Orji returned to NIST in mid 2008. However, he continues to support the RMS implementation on the new CD-AFM in the ISMI/SEMATECH facilities in Albany.

■ As a result of the NIST SCCDRM effort, in which the AFM dimensional metrology project played a central role, CD-AFM linewidth measurements can now be performed with a 1 nm (k = 1) standard uncertainty. This standard for width calibration is now being used on both the X3D and the SXM at NIST. An image of an SCCDRM taken on the SXM320 is shown in Fig. 1. In 2007, we performed a comparison of the SCCDRM master calibration with a commercially available linewidth standard, an image of which is shown in Fig. 2. There was agreement between these two independent calibrations, as shown in Fig. 3.

■ We have used the C-AFM to perform a NIST-internal calibration on a 100 nm pitch grating specimen. This sample was then used to support SEM magnification calibration during the NIST-wide project to develop Reference Materials (RM) of gold nanoparticles. The C-AFM value had an expanded uncertainty (k = 2) of approximately 6×10^{-4}, and this result is currently being used to refine the analysis of the SEM measurements for the official report.

■ Another area of activity involves the study of single atomic Si steps as fundamental height standards in the sub-nanometer regime. In 2006 we published a documentary standard for AFM z-calibration using the single atom steps through the ASTM Subcommittee E42.14 on STM/AFM. This was published by ASTM as E2530-06. Recently, we have expanded this effort to include other materials and we have performed C-AFM measurements on a SiC sample with nominal 1 nm steps. A paper on this effort was presented at the 2010 SPIE Advanced Lithography Conference.

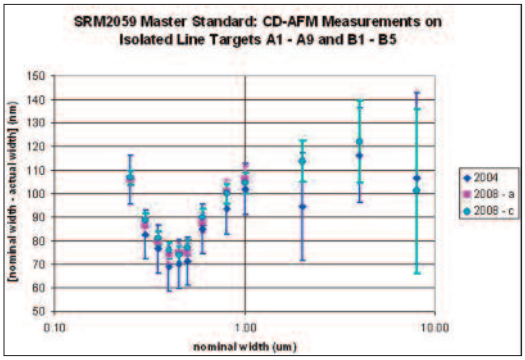

Figure 4. New and original CD-AFM reference measurement on the isolated line targets of SRM 2059 – ranging from 0.25 µm width (A1 feature) up to 8 µm (B5 feature). The error bars represent expanded (k = 2) uncertainties, which have been reduced by approximately ×4 for the smallest features.

■ We continue to provide reference AFM metrology for the SRM 2059 photomask standard. During the tenure of Ronald Dixson as the first NIST Guest Scientist at SEMATECH, we performed traceable CD-AFM measurements on the control mask for the SRM calibration. Subsequently, and following the completion of the SCCDRM project, we have performed new measurements using the CD-AFM at NIST, and we have been able to reduce the AFM uncertainties by almost a factor of five for the smallest features. .This is illustrated in figures 4 and 5.

A paper on the status of the SRM 2059 recalibration effort and our plans for a bilateral comparison of photomask linewidth measurements between NIST and PTB was presented at the Frontiers in Characterization and Metrology for Nanoelectronics Conference in May of 2009

Collaborations

Intel Mask Operations, Santa Clara, CA.

Intel, Hilllsboro, OR.

Intel, Santa Clara, CA.

SEMATECH, Austin, TX.

Veeco Metrology, Santa Barbara, CA.

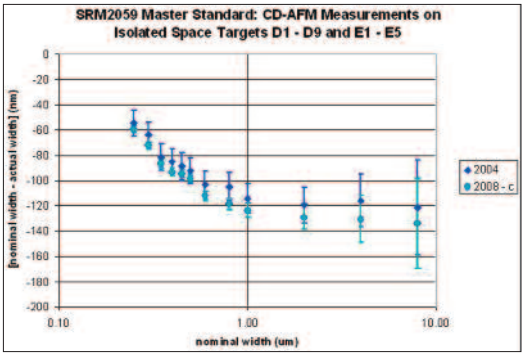

Figure 5. New and original CD-AFM reference measurement on the isolated space targets of SRM 2059 – ranging from 0.25 µm width (D1 feature) up to 8 µm (E5 feature). The error bars represent expanded (k = 2) uncertainties, which have been reduced by approximately × 4 for the smallest features.

IBM Burlington, VT.

IBM Almaden Research Center, San Jose, CA.

ELORET Corp./NASA Ames Research Center, Moffett Field, CA.

Departments of Mechanical Engineering and Chemistry, University of North Carolina, Charlotte, NC.

School of Mechatronic Engineering, Harbin Institute of Technology, Harbin, China.

Recent Publications

J. A. Kramar, R. Dixson, N. G. Orji, *"Scanning Probe Microscope Dimensional Metrology at NIST,"* submitted to Meas. Sci. Technol. (2010).

T. V. Vorburger, A. Hilton, R. G. Dixson, N.G. Orji, J. A. Powell, A. J. Trunek, P. G. Neudeck, P. B. Abel, *"Calibration of 1 nm SiC step height standards,"* to be published in SPIE Proceedings Vol. 7638 (2010).

J. S. Villarrubia, R. G. Dixson, A. E. Vladar, *"Proximity-associated errors in contour metrology,"* to be published in SPIE Proceedings Vol. 7638 (2010).

R. Quintanilha, Y-J. Sohn, B. M. Barnes, R. Attota, R. G. Dixson, R.M. Silver, *"Sub-50-nm critical dimension measurements using a 193-nm angle-resolved scatterfield microscope,"* to be published in SPIE Proceedings Vol. 7638 (2010).

N.G. Orji, R.D. Dixson, B. M. Barnes, and R.M. Silver, *"Traceability: The Kay to Nanomanufacturing,"* Proceedings of the Sixth International Conference on Precision, Meso, Micro and Nano Engineering, Coimbatore, India, December 11-12, pp. 31-35, 2009.

B. Bodermann, D. Bergmann, E. Buhr, W. Häßler-Grohne, H. Bosse, J. Potzick, R. Dixson, R. Quintanilha, M. Stocker, A. Vladar, N. G. Orji, *"Results of an International Photomask Linewidth Comparison of NIST and PTB,"* SPIE Proceedings Vol. 7488, 74881H-1-14 (2009).

N. G. Orji, R. G. Dixson, A. Cordes, B. D. Bunday, J. A. Allgair, *"Measurement Traceability and Quality Assurance in a Nanomanufacturing Environment,"* SPIE Proceedings Vol. 7405, 740505 (2009).

R. Dixson, J. Fu, N. Orji, T. Renegar, A. Zheng, T. Vorburger, A. Hilton, M. Cangemi, L. Chen, M. Hernandez, R. Hajdaj, M. Bishop, A. Cordes, *"Reference Metrology in a Research Fab: The NIST Clean Calibrations Thrust,"* SPIE Proceedings Vol. 7272, 727209-1-12 (2009).

R. Dixson, J. Potzick, N. Orji, *"Recalibration of the SRM 2059 Master Standard using Traceable Atomic Force Microscope Metrology,"* SPIE Proceedings Vol. 7122, 71222Q-1-12 (2008).

J. Potzick, R. Dixson, R. Quintanilha, M. Stocker, A. Vladar, E. Buhr, W. Häßler-Grohne, B. Bodermann, C. G. Frase, H. Bosse, *"International photomask linewidth comparison by NIST and PTB,"* SPIE Proceedings Vol. 7122, 71222P-1-14 (2008).

N. G. Orji, R. G. Dixson, B. D. Bunday, J. A. Allgair, *"Accuracy Considerations for Critical Dimension Semiconductor Metrology,"* SPIE Proceedings Vol. 7042, 70420A-1-11 (2008).

J. Robert, B. Banke, R. Dixson, C. Strocchia-Rivera, *"Traceable Calibration of AFM Step Height Measurements for Integrated Circuit Manufacturing,"* SPIE Proceedings Vol. 6922 (2008).

N. G. Orji, R. G. Dixson, B. D. Bunday, J. A. Allgair, *"Towards Accurate Feature Shape Metrology,"* SPIE Proceedings Vol. 6922 (2008).

R. M. Silver, B. Barnes, A. Heckert, R. Attota, R. G. Dixson, J. Jun, *"Angle Resolved Optical Metrology,"* SPIE Proceedings Vol. 6922 (2008).

R. Attota, R. Silver, R. Dixson, *"Linewidth measurement technique using through-focus optical images,"* Applied Optics Vol. 47, 495-503 (2008).

H. J. Patrick, R. Attota, B. Barnes, T. A. Germer, R. G. Dixson, M. T. Stocker, R. M. Silver, M. R. Bishop, *"Optical critical dimension measurement of silicon grating targets using back focal plane scatterfield microscopy,"* J. Micro/Nanolith. MEMS MOEMS Vol. 7, 013012-1-11 (2008).

M. W. Cresswell, R. A. Allen, W. F. Guthrie, C. E. Murabito, R. G. Dixson, A. Hunt, *"Comparison of SEM and HRTEM CD Measurements Extracted from Test-Structures Having Feature Linewidths from 40 nm to 240 nm,"* IEEE Trans. Instrum. Meas. Vol. 57, 100-109 (2008).

Ronald Dixson, Ndubuisi G. Orji, James Potzick, Joseph Fu, Richard A. Allen, Michael Cresswell, Stewart Smith, Anthony J. Walton, Andreas Tsiamis, *"Photomask Applications of Traceable Atomic Force Microscope Dimensional Metrology at NIST,"* SPIE Proceedings Vol. 6730, 67303D-1-13 (2007).

N. G. Orji, R. G. Dixson, *"Higher Order Tip Effects in Traceable CD-AFM Based Linewidth Measurements,"* Meas. Sci. and Technol. Vol. 18, 448-455 (2007).

N. G. Orji, R. Dixson, B. D. Bunday, J. A. Allgair, *"TEM Calibration Methods for Critical Dimension Standards,"* SPIE Proceedings Vol. 6518, 651810 (2007).

B. Bunday, J. Allgair, E. Soleck, C. Archie, N. G. Orji, J. Beach, O. Adan, R. Peltinov, M. Bar-zvi, J. Swyers, *"The coming of age of tilt CD-SEM,"* SPIE Proceedings Vol. 6518, 65181S (2007).

R. Dixson and N. G. Orji, *"Comparison and uncertainties of standards for critical dimension atomic force microscope tip width calibration,"* SPIE Proceedings Vol. 6518, 651816 (2007).

M. Tanaka, J. S. Villarrubia, and A. E. Vladár, *"Influence of Focus Variation on Linewidth Measurements,"* Proc. SPIE 5752, p. 144 (2005).

Optical-Based Photomask Dimensional Metrology

Technical Contacts:
J. Potzick
R. Silver

Goals

Provide technological leadership to semiconductor and equipment manufacturers and other government agencies by developing and evaluating the methods, tools, and artifacts needed to apply optical techniques to the metrology needs of semiconductor microlithography. One specific goal is to provide the customer with the techniques and standards needed to make traceable dimensional measurements on photomasks and wafers, where appropriate, at the customer's facility. The industry focus areas of this project are primarily the optical- based methods used in overlay metrology, photomask critical dimension metrology, and high-accuracy two-dimensional placement metrology.

Customer Needs

Tighter tolerances on CD measurements in photomask and wafer production place increasing demands on photomask linewidth accuracy. NIST has a comprehensive program to both support and advance the optical techniques needed to make these photomask critical dimension measurements. Accurate feature size metrology on binary photomasks (constituting 85 % of current mask production) becomes increasingly difficult as critical features shrink and their optical proximity correction cousins proliferate. Phase shift and EUV masks present additional challenges.

Improved photomask CD metrology and two-dimensional overlay measurement techniques and standards are needed for measuring and controlling feature size and placement on the wafer and on photomasks. Overlay control is listed in multiple sections of Tables Met 3a and b of the 2007 SIA ITRS as a difficult challenge for <45 nm node processes. In fact, the table shows that there are no known measurement solutions with acceptable uncertainty for image placement and overlay control beyond the 65 nm node. As shown in Tables Met 4a and b, the problems are more acute for long term photomask CD metrology where the industry will soon be encountering metrology problems without known manufacturing solutions.

Technical Strategy

There are three main strategic technical components of this project.

1. Photomask linewidth measurements using the ultraviolet transmission microscope (supported by additional traceable AFM measurements), calibration of NIST Photomask Linewidth Standard SRM 2059 (traceable to the definition of the meter), and the development of calibration methods to provide photomask linewidth measurement uncertainties adequate to meet industry needs.

The technical strategy for photomask linewidth standards is divided into two segments: (a) instrumentation and image model development and (b) design and calibration of standard artifacts.

An ultraviolet transmission microscope (Fig. 1) has been constructed which uses a unique geometry (a Stewart platform) as the main rigid structure. This microscope platform has good vibration characteristics and presents an open mechanical architecture. Higher image contrast, well-defined and uniform background image intensity, and smaller influence of such ancillary parameters as Cr thickness and Cr n and k, offer improved linewidth measurement uncertainties over reflection-mode microscopes.

NIST has supplied a substantial number of photomask linewidth standards worldwide over the past decades. NIST's current chrome-on-quartz photomask linewidth standard, SRM 2059, (Fig. 2, next page) contains isolated linewidth and spacewidth features in the range of 0.25 μm to 32 μm, whose widths have been measured and certified to an uncertainty of <20 nm at the 95 % confidence level.

In response to customers' needs for more accu-

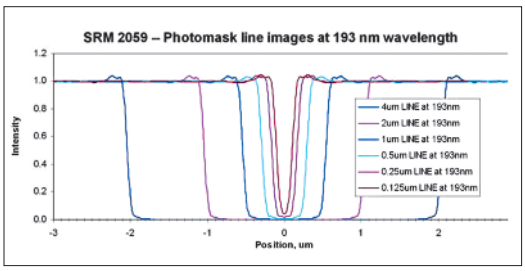

Figure 1. Modeling results for isolated binary photomask lines from 4 μm to 0.125 μm

rate photomask feature size measurements, NIST has worked extensively to improve mask metrology through optical image modeling and improved optical microscope characterization methods. The features on even the highest quality masks exhibit roughness and runout at the chrome edges, compromising the definition of edge and linewidth. In response to these problems, NIST introduced the Neolithography concept 1997: Modeling or emulating the effects of all of the relevant feature properties in both the mask metrology process and the wafer exposure and development processes, using existing and new software tools, can improve feature-size accuracy by establishing accurate simulation results and improving the relationship between mask-feature metrology and the corresponding wafer-feature sizes. This concept (at least in part) can be seen today in the design for manufacturing (DFM) sector of the industry.

In addition, the observed top-to-bottom photomask antireflecting Cr edge runout of 5 nm to 10 nm peak-peak conflicts with the desire for Cr linewidth uncertainty <10 nm; a realistic approach to reconciling this situation is embodied in SEMI Standard P35-1106, Terminology for Microlithography Metrology.

DELIVERABLES:

- Compare and improve the accuracy of the NIST optical Imaging code (developed by Egon Marx) with new Imaging models developed by Thom Germer (NIST) and some commercially available Image models for use in transmission. Ongoing, through 4Q 2010
- Re-evaulate the parametric uncertainty in optical linewidth measurements, using new techniques to remove the small linewidth overemphasis in the previously described metric. Present results at Microscopy and Microanalysis (2008) and other venues; ongoing through 4Q 2010.

2. The second major component is the development of two-dimensional grid calibration standards and associated measurement techniques, including statistical analysis and charge-coupled device (CCD) characterization as used by industry. These individual technical strategies for these components are described next.

We are addressing the challenges of two-dimensional measurements from a couple of directions. The first is the calibration of an artifact standard which is being used to bring two-dimensional-based inspection instruments to the same metric. This effort has developed a standard grid which is now available as a NIST Standard Reference Material, #5001. The artifact can be used by the semiconductor industry to standardize 2-D feature placement measurements. The SRM 5001 was developed as an industry consensus standard grid and calibrated with measurements on a state-of-the-art industry machine followed by verification of the measurements using NIST Linescale Interferometer capabilities which resulted in traceable two-dimensional measurements.

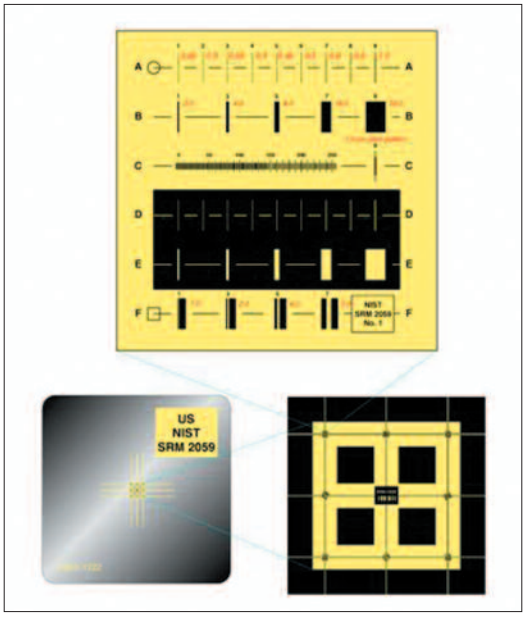

Figure 2. NIST SRM 2059 Photomask Linewidth Standard. Isolated linewidths and spacewidths range from 0.250 μm to 312 μm.

A new generation of grids for the SRMs have been fabricated and measurements have been completed. Each measurement of the grid has data in each of at least two orientations. Rotating the grid 90° between measurements samples a number of the geometric errors of the machine. The remaining geometric sources of uncertainty are the scale and some components of the linearity of each machine axis travel.

Verification of the industry-based grid measurements is done at NIST. The overall scale of the grid is checked with the NIST linescale interferometer, an instrument that is known to provide the most accurate 1-D measurements available in the world. Two sources of uncertainty not captured by these measurements include components of the straightness and effects of the plate bending when fixtured.

We have delivered all of the SRM 5001 grid plates to the Standard Reference Material program. We are now planning the next generation. From the detailed uncertainty budget for SRM 5001 the scale measurements are the largest component and the largest component of the Linescale Interferometer uncertainty budget is the wavelength correction for the index of refraction of the air.

DELIVERABLES:

- Evaluate current 2-dimensional calibration requirements and design a new reticle for development as a two-dimensional calibration reference grid. Develop a technical strategy to lower the overall uncertainty from the two-dimensional calibrations. 4Q 2010

3. To strengthen the foundation of NIST's linewidth measurement traceability and to support the Bureau International des Poids et Mesures (BIPM) Mutual Recognition Arrangement, NIST has become the pilot laboratory for an international intercomparison of submicrometer linewidth measurements, Nano1. National metrology institutes in nine countries around the world are participating. PTB (Physikalisch Technische Bundesanstalt, Germany) has offered to supply two masks manufactured at the Advanced Mask Technology Center GmbH Co. KG (AMTC, Dresden) for the multilateral comparison Nano1 and a separate bilateral comparison between NIST and PTB. Since Nano1 will take several years (allowing 2-3 months for each laboratory, plus overhead), the bilateral comparison is designed to provide more timely data to the AMTC. This bilateral comparison and Nano1 are to be kept as separate and independent as possible. A publication describing this bilateral comparison was given at BACUS 2008 and 2009.

DELIVERABLES:

- The masks from PTB are being measured by AFM (Ron Dixson) and eSEM (Andras Vladar). The Nano1 protocol has been revised to incorporate the AMTC mask. Upon acceptance of the protocol by participating laboratories, Nano1 will commence. 4Q 2010

Accomplishments

■ SRM 2800 Microscope Magnification Standard is a standard-size microscope slide with calibrated pitch features ranging from 1 µm to 1 cm (see Fig. 3). It contains a lithographically produced chrome pitch pattern consisting of a single array of parallel lines with calibrated center-to-center spacings. It contains no linewidth structures. This SRM is intended to be used for the calibration of reticles and scales for optical or other microscopes at the user's desired magnification. The SRM may be used in either transmission or reflection mode optical microscopes, SEMs, or SPMs. Calibration is traceable to the meter through NIST Line Scale Interferometer. Fifty-six units have been calibrated and delivered to the NIST Office of Standard Reference Materials and nearly half of current stock have been sold.

■ The 193 nm reflection mode scatterfield optical microscope is now operational. Preliminary scanning and modeling is now underway as a basis for photomask measurements on the 193 nm tool. A paper was presented at Bacus 2009 showing a comparison of 193 nm reflection mode measurements and UV transmission mode measurements.

■ The UV transmission microscope has been substantially updated with new interferometers including new synchronization hardware. The op-

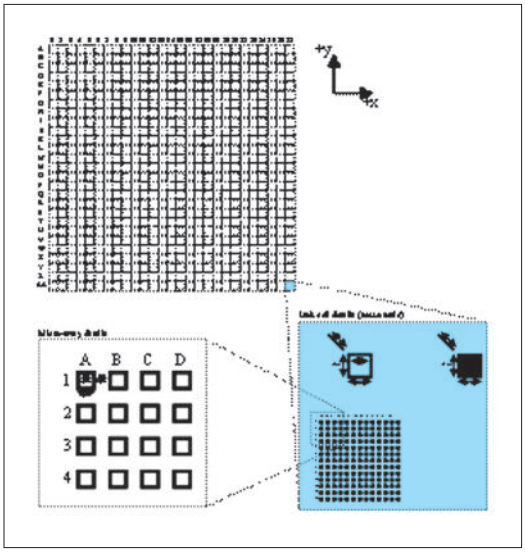

Figure 3. The two dimensional grid photomask standard, now available through the SRM office.

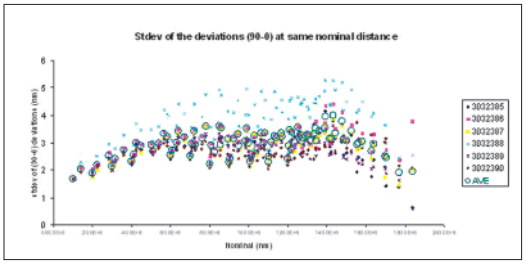

Figure 4. Tool repeatability and mapping data for the two-dimensional mask calibration procedure.

tics has been updated with a flexible conjugate back focal plane to allow for illumination engineering and improved alignment. The instrument has undergone extensive alignment and calibration. The entire computer control system has been updated with a new high speed controller and CCD acquisition capability.

■ The complete set of two-dimensional grid artifacts, known as SRM 5001, has been delivered to the SRM office and are selling well. These 152.4 mm (6 inch) photomasks have been measured on a state-of-the-art I-pro metrology system by the photomask manufacturer. The second set of re-designed 152.4 mm (6 inch) feature placement standards has also been measured and calibrated in close collaboration between NIST and Photronics. The collaboration employs the industry tool and the traceability of the NIST line scale interferometer with appropriate statistical analysis (see Fig. 4).

■ A comprehensive suite of two-dimensional calibration methods for the calibration of optical systems and illumination systems was published based on the SRM 5001 grid calibration methodology. These results and the methodology was published at SPIE Microlithography. These methods are enabling a substantially improved optical calibration and alignment sequence as well as improved modeling inputs for more accurate linewidth measurements.

Collaborations

ISMT, IBM, IVS Schlumberger, KLA-Tencor, Intel, Motorola, AMD, and several other leading manufacturers or tool vendors.

Dr. Mark Davidson, Spectel Research Corp.

PTB (Physikalisch Technische Bundesanstalt, Germany).

AMTC, Dresden, Germany.

Publications

J. Potzick, "Metrology and process control: dealing with measurement uncertainty," SPIE Advanced Lithography, 7638-135 (2010).

Richard Quintanilha, Yeung Joon Sohn, Lowell P. Howard, Michael T. Stocker, Richard M. Silver, James E..Potzick, "Photomask metrology using a 193-nm scatterfield microscope," SPIE/BACUS Photomask Technology Symposium, 7488-55 (2009).

B. Bodermann, D. Bergmann, E. Buhr, W. Häßler-Grohne, H. Bosse, , J. Potzick, , R. Dixson, R. Quintanilha, M. Stocker, A. Vladar, N. G. Orji, "Results of an international photomask linewidth comparison between NIST and PTB," SPIE/BACUS Photomask Technology Symposium, 7488-51 (2009).

Smith, S.; Tsiamis, A.; McCallum, M.; Hourd, A.C.; Stevenson, J.T.M.; Walton, A.J.; Dixson, R.G.; Allen, R.A.; Potzick, J.E.; Cresswell, M.W.; Orji, N.G., "Comparison of Measurement Techniques for Linewidth Metrology on Advanced Photomasks," IEEE Transactions on Semiconductor Manufacturing, 22, 1, pp. 72-79 (2009).

Egon Marx and James Potzick, "Computational Parameters in Simulation of Microscope Images", Progress In Electromagnetics Research Symposium, Beijing, China (2009).

Ronald Dixson, James Potzick, and Ndubuisi Orji, "Re-Calibration Of The SRM 2059 Master Standard Using Traceable Atomic Force Microscope Dimensional Metrology," Frontiers of Characterization and Metrology for Nanoelectronics, Albany, NY (2009).

J. Potzick, "Image library approach to evaluating parametric uncertainty in metrology of isolated feature width," Proceedings of SPIE Metrology, Inspection, and Process Control for Microlithography XXIII, San Jose, Calif. (2009).

J. Potzick, R. Dixson, R. Quintanilha, M. Stocker, A. Vladar, E. Buhrb, W. Häßler-Grohne, B. Bodermann, C. G. Frase, H. Bosse, "International photomask linewidth comparison by NIST and PTB," Procedings SPIE Photomask (BACUS), 7122-97 (2008).

J. Potzick, "Accuracy of Optical Dimensional Metrology at the Nano-scale", Microscopy & Microanalysis 2008 Meeting, Albuquerque, New Mexico (2008).

J. Potzick, "Limits of optical dimensional metrology at the nano-scale," 2nd Tri-National Workshop on Standards for Nanotechnology, Gaithersburg, Md. USA (Feb. 6, 2008).

J. Potzick, B. Grenon, "Nanoscale metrology – theory and practice," Short Course presented at SPIE BACUS 2007, 2008.

R. Dixson, N. G. Orji, J. Potzick, J. Fu, M. Cresswell, R. Allen, S. Smith, A. J. Walton, "Photomask Applications of Traceable Atomic Force Microscope Dimensional Metrology at NIST," SPIE Photomask Technology 27th Annual Symposium, vol. 6730-117 (2007).

J. Potzick, "Linewidth Standards and CD Metrology," Workshop: Critical Dimension Standards: The Past, Present, and Future", SPIE Symposium on Advanced Lithography (2007).

J. Potzick, E. Marx, M. Davidson, “Accuracy in Optical Image Modeling,” Proceedings of SPIE Metrology, Inspection, and Process Control Conference for Microlithography XXI, vol. 6518-39 (2007).

R. Attota, R. M. Silver, J. E. Potzick, “Optical Illumination and Critical Dimension Analysis Using the Through-Focus Focus Metric Method,” SPIE Optics and Photonics Conference (2007).

SEMI Standard P35-1106, Terminology for Microlithography Metrology.

J. Potzick, E. Marx, M. Davidson, “Parametric Uncertainty in Optical Image Modeling,” Proceedings of BACUS Symposium on Photomask Technology, vol. 6349-187 (2006).

J. Potzick., NIST SRM 2059 Certificate (2006).

D. Everett, L. Howard, R. M. Silver, and T. Doiron , NIST SRM 5001 Certificate (2006).

R. M. Silver, B. Barnes, R. Attota, J. Jun, J. Filliben, J. Soto, M. Stocker, P. Lipscomb, E. Marx, H. Patrick, R. Dixson, and R. Larrabee, “The Limits of Image-based Optical Metrology,” Proc. SPIE Intl. Soc. Opt. Eng. Vol. 6152, 61520Z (2006).

R. Attota, R. M. Silver, M. Bishop and R. Dixson, “Optical Critical Dimension Measurement and Illumination Analysis using the Through-focus Focus-metric,” Proc. SPIE Intl. Soc. Opt. Eng. Vol. 6152, 61520K (2006).

Y. J. Sohn, B. Barnes, L. Howard, R. Silver, R. Attota, and M. Stocker, “Kohler Illumination in High Resolution Optical Metrology,” Proc. SPIE Intl. Soc. Opt. Eng. Vol. 6152, 61523S (2006).

P. Lipscomb, J. Allgair, B. Bunday, M. Bishop, R. Silver, R. Attota, and M. Stocker, “Calibration Optical Overlay Measurements,” Proc. SPIE Intl. Soc. Opt. Eng. Vol. 6152, 615211 (2006).

Scatterometry-Based Dimensional Metrology

Goals

Our goals are to: (1) increase the effectiveness of scatterometry and other optical critical dimension (OCD) methods by providing industry with new measurement techniques, improved modeling, and standards; (2) provide assessments of accuracy and sensitivity of various OCD methods; and (3) develop facilities to accurately assess OCD targets.

Customer Needs

Scatterometry is increasingly becoming a preferred method for online critical dimension (CD) metrology. The method relies upon measurements of the reflectance or diffraction of small test grating structures as functions of angle, wavelengths, and/or polarization. By comparing measurement results with an extensive library of theoretical simulations or by performing a real-time regression analysis, tools can extract such line profile parameters as critical dimension, sidewall angle, and height, as well as more detailed descriptions of the sidewall shape.

While scatterometry has gained significant acceptance, it is continuing to grow in utility. However, there are many issues that remain that prevent it from having fundamental traceability. For example, the effects of finite illumination, finite target array size, line-edge and line-width roughness, uncertainties in the optical properties of the materials in the structure, neglect of surface oxides or other layers, radiometric accuracy, and the integrity of the theoretical model all contribute to the final measurement uncertainty in ways that are at this time poorly understood.

Ultimately, the industry needs reference artifacts that can test the validity of the results obtained by scatterometry tools. Such an artifact might consist of a set of gratings that have been characterized by a variety of techniques, including scatterometry, scanning electron microscopy (CD-SEM), atomic force microscopy (CD-AFM), and transmission electron microscopy (TEM). Scatterometry provides a method independent of the others, and if a comprehensive uncertainty budget were developed for the method, it would substantially improve the overall state of dimensional metrology.

Technical Strategy

There are three major strategies for improving the effectiveness of scatterometry. One strategy is to develop efficient models for the diffraction of light by structures on surfaces, so that NIST has state-of-the-art capabilities to perform scatterometry measurements and analysis as well as to provide standard data for a variety of model structures. The second strategy is to assess the sensitivity and accuracy of scatterometry methods to different structures, to provide industry with an understanding of what determines the ultimate sensitivity and accuracy of the methods. Finally, the third strategy is to develop in-house measurement capabilities with the long-term goal to perform scatterometry measurements on reference materials, to perform inter-laboratory comparisons, and to develop the scatterometry technique for other applications.

Specific project elements are defined below:

1. Theoretical Scatterometry Modeling – Rigorous coupled wave (RCW) based theories are the most common methods used to analyze scatterometry data. We have developed in-house capability to perform RCW calculations for arbitrary one-dimensionally and two-dimensionally periodic structures. These codes are being used to generate libraries for profile extraction as well as for test calculations that assess the sensitivity of scatterometry to changes in model parameters or to non-ideal target profiles. We are using these codes to assess the effects of line-edge and line-width roughness, material anisotropy, as well as to perform RCW calculations on three-dimensional structures, such as contact holes. Building upon the SCATMECH library of codes that have been made available on the web for diffuse scattering calculations, we have published the RCW code for one-dimensionally periodic structures and will publish the code for two-dimensionally period structures in the future.

DELIVERABLES:

- Publication of RCW code for two-dimensionally periodic structures in the SCATMECH library. 4Q 2010

Technical Contacts:
T. Germer

2. Assessment of Accuracy and Precision of Scatterometry – Scatterometry relies heavily on prior knowledge of the specific structure being examined. For example, optical properties of all incorporated materials are required for the simulations. Reasonable parameterization of sidewall profiles are required to yield meaningful profiles. The effects of line-edge or line-width roughness are usually ignored. In this program element, we are assessing the impact that each model parameter has on the outcome of the measurement. The goal is to establish an independent uncertainty budget that includes all sources of random and systematic uncertainties. Furthermore, we are assessing the sensitivity limits of scatterometry, to determine how far into the future scatterometry tools can provide critical dimension metrology. A computer program, OCDSense, was written and provided to ISMI member companies to help determine the sensitivity and uncertainty of scatterometry for an arbitrary one-dimensionally periodic grating in any given tool.

DELIVERABLES:

- Develop an uncertainty budget for a scatterometry measurement. 1Q 2011

3. Scatterometry Measurements –We have recently upgraded our laser-based Goniometric Optical Scatter Instrument (GOSI), Fig. 1, used for diffuse scatter measurements, to perform scatterometry measurements on industry-relevant targets on 300 mm wafers. The measurement capabilities include angle-scanned scatterometry at a number of discrete laser wavelengths. This instrument has the capability to perform conical scatterometry measurements and will be used to perform traditional measurements as well as measurements of higher-order, non-specular diffraction and diffuse scatter. Another instrument, a microspot spectroscopic Mueller matrix ellipsometer, was delivered in 2009. A long term goal is to develop reference scatterometry targets, measure them with these instruments, provide accurate determinations of their dimensions and profiles, and have uncertainties placed on the results. Another long term goal is to develop novel measurement modalities that improve the utility of scatterometry. One method we have demonstrated is microscope-based scatterometry using back focal plane imaging. This technique enables collection of multiple diffraction order scatterometry

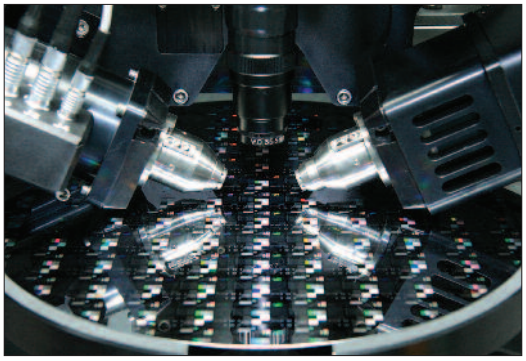

Figure 1. The new micro-spot spectroscopic ellipsometer has pattern recognition capabilities and rotation stages that enables it to perform measurements as a function of rotation angle on a target, improving the confidence in model parameter extraction.

signatures in a single image, can be configured for both dense and isolated targets, and allows scatterometry and image-based metrology to be performed on the same tool. Another technique that we have developed is time-sequenced scatterometry, where we follow the evolution of a grating, for example, an imprinted polymer, while it reflows at elevated temperatures.

DELIVERABLES:

- Intercomparison of scatterometry measurements performed on the spectroscopic ellipsometer with atomic force microscopy. 3Q 2010

Accomplishments

■ We have developed efficient rigorous coupled wave (RCW) software for one- and two-dimensionally periodic structures (arrays of two- and three-dimensional features). Results of the in-house code have been compared with finite difference time domain, surface integral equation, and other RCW implementations. This software is also configured to run on a large cluster computer, so that library generation is possible. The code for one-dimensionally periodic structures has also been extended to allow for anisotropic materials in the structure.

■ As part of our effort in assessing the precision and accuracy of scatterometry, we have performed a study of the sensitivity of scatterometry to CD and sidewall angle for a large number of different measurement modalities, including angle-scanned and wavelength-scanned reflectometry and ellipsometry, for amorphous silicon gate and gate-resist structures. This study in-

cluded parameters appropriate from the 45 nm half-pitch node to the 18 nm half-pitch node. The results demonstrated that scatterometry can achieve the necessary sensitivity to measure dense gratings at these nodes. Future work, however, will be necessary to achieve sufficient sensitivity to isolated features.

■ In the area of scatterometry-based optical critical dimension (OCD) measurement, we have recently measured OCD linewidth of lines in grating targets fabricated using the single-crystal critical dimension reference materials (SCCDRM) process. The SCCDRM implementation, developed by a multi-laboratory collaboration at NIST, provides lines with known geometries – typically vertical sidewalls – defined by the silicon lattice, and has led to development of a prototype linewidth standard for isolated lines designed for use in AFM calibration. We have shown that the linewidth obtained from the OCD technique for these targets is linearly related to linewidth obtained from SEM, with a slope near unity and zero offset (see Fig. 2). Continuing efforts to reduce linewidth roughness of the target, to analyze uncertainties in the OCD measurement, and to evaluate the suitability of these targets for OCD reference materials, are ongoing.

■ We have also extracted OCD linewidth from scatterometry signatures of silicon-on-silicon gratings obtained using back-focal-plane imaging in a microscope. We investigated targets with only specular reflectance (grating pitch 300 nm) and those with both specular and higher-order diffraction (grating pitch 600 nm). Linewidths of 131 nm to 140 nm were obtained, with the back-focal-plane signatures demonstrating nanometer-level sensitivity to linewidth, and a linear relationship of linewidth obtained from scatterfield microscopy to linewidth measured by SEM was shown.

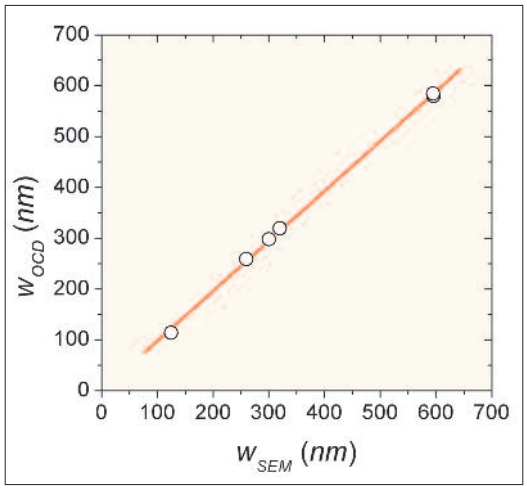

Figure 2. CD linewidth extracted from OCD, wOCD, versus linewidth measured by SEM, wSEM, for six targets on an SCCDRM chip.

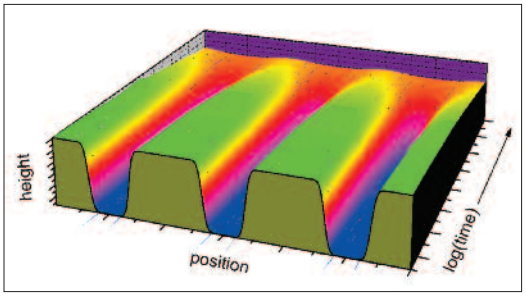

Figure 3. Line profiles measured by scatterometry as a function of time during annealing for a low molecular weight polymer grating at Tg = 100 °C.

■ We developed a time-sequenced spectroscopic ellipsometry technique in which we characterized the reflow of polystyrene gratings while they were being held at their glass transition temperature. Figure 3 shows the profile of such a grating as a function of time. The time evolution of the surface profiles of low and high molecular mass polystyrene gratings were found to differ, due to the different flow, viscosity, and stress relaxation mechanisms present.

■ We have developed computationally efficient methods for numerically averaging over numerical aperture and bandwidth. These methods are required to improve the accuracy of scatterometry measurement.

Collaborations

International Sematech Manufacturing Initiative, Benjamin Bunday, Limits of Scatterometry Study.

Department of Electrical Engineering, Texas A&M University, Professor Krzysztof Michalski, Modeling of Scattering by Lines Having Anisotropic Optical Properties.

Publications

B.C. Bergner, T.A. Germer, and T.J. Suleski, *"Effective medium approximations for modeling optical reflectance from gratings with rough edges,"* J. Opt. Soc. Am. A 27, 1083-1090 (2010).

B.C. Bergner, T.A. Germer, and T.J. Suleski, *"Effect of Line Width Roughness on Optical Scatterometry Measurements,"*

in Metrology, Inspection, and Process Control for Microlithography XXIII, Proc. SPIE 7272, 72720U (2009).

T.A. Germer, H.J. Patrick, R.M. Silver, and B. Bunday, *"Developing an Uncertainty Analysis for Optical Scatterometry,"* in Metrology, Inspection, and Process Control for Microlithography XXIII, Proc. SPIE 7272, 72720T (2009).

H.J. Patrick, T.A. Germer, Y. Ding, H.W. Ro, L.J. Richter, and C.L. Soles, *"In situ measurement of annealing-induced line shape evolution in nanoimprinted polymers using scatterometry,"* in Alternative Lithographic Technologies, Proc. SPIE 7271, 72720T (2009).

H.J. Patrick, T.A. Germer, Y. Ding, H.W. Ro, L.J. Richter, and C.L. Soles, *"Scatterometry for in situ measurement of pattern reflow in nanoimprinted polymer gratings,"* Applied Physics Letters 93, 233105 (2008).

H.J. Patrick, T.A. Germer, M.W. Cresswell, B. Li, H. Huang, and P.S. Ho, *"Extraction of trench geometry and linewidth of nanoscale grating targets in (110)-oriented silicon using angle-resolved scatterometry,"* in Instrumentation, Metrology, and Standards for Nanomanufacturing II, Proc. SPIE 7042, 70420B (2008).

R. Attota, T.A. Germer, and R.M. Silver, *"Through-focus scanning-optical-microscope imaging method for nanoscale dimensional analysis,"* Optics Letters 33, 1990–1992 (2008).

E. Kenyon, M. W. Cresswell, H. Patrick, and T. A. Germer, *"Modeling the effect of finite size gratings on scatterometry measurements,"* in Metrology, Inspection, and Process Control for Microlithography XXII, Proc. SPIE 6922, 69223P (2008).

H. J. Patrick, R. Attota, B. M. Barnes, T. A. Germer, M. T. Stocker, R. M. Silver, and M. R. Bishop, *"Optical Critical Dimension Measurement of Sub-resolution Silicon Grating Targets using Back Focal Plane Imaging Scatterfield Microscopy,"* Journal of Micro/Nanolithography, MEMS, and MOEMS 7, 013012 (2008).

R. Silver, B. Barnes, R. Attota, J. Jun, M. Stocker, E. Marx, and H. Patrick, *"Scatterfield Microscopy for Extending the Limits of Image-based Optical Metrology,"* Applied Optics 46 (20), 4248–4257(2007).

R. A. Allen, H. J. Patrick, M. Bishop, T. A. Germer, and M. W. Cresswell, *"Study of Test Structures for Use as Reference Material in Optical Critical Dimension Applications,"* in 2007 IEEE International Conference on Microelectronic Test Structures, held March 19-22, 2007 in Tokyo, Japan, pp. 20–25 (2007).

T. A. Germer, *"Modeling the effect of line profile variation on optical critical dimension metrology,"* in Metrology, Inspection, and Process Control for Microlithography XXI, Proc. SPIE 6518, 65180Z-1–9 (2007).

H. J. Patrick, T. A. Germer, M. W. Cresswell, R. A. Allen, R. G. Dixson, and M. Bishop, *"Modeling and Analysis of Scatterometry Signatures for Optical Critical Dimension Reference Material Applications,"* in Frontiers of Characterization and Metrology for Nanoelectronics: 2007, Proc. AIP 931, 392–396 (2007).

Y. Ding, H. W. Ro, T. A. Germer, J. F. Douglas, B. Okerberg, A. Karim, C. L. Soles, *"Relaxation behavior of polymer structures fabricated by nanoimprint lithography,"* ACS Nano 1(2), 84–92 (2007).

H. J. Patrick and T. A. Germer, *"Progress towards traceable nanoscale optical critical dimension metrology for semiconductors,"* in Advanced Characterization Techniques for Optics, Semiconductors, and Nanotechnologies III, Angela Duparré, Bhanwar Singh, and Zu-Han Gu, Eds., Proc. SPIE 6672, 66720L-1–9 (2007).

T. A. Germer, *"Effect of line and trench profile variation on specular and diffuse reflectance from a periodic structure,"* J. Opt. Soc. Am. A 24(3), 696–701 (March 2007).

Small Angle X-Ray Scattering

Technical Contacts:
R. L. Jones
W. L. Wu

Goals

To develop a transmission geometry small angle X-ray scattering (SAXS)-based methodology to quickly, quantitatively, and non-destructively measure critical dimensions (CD) and feature shape with sub-nanometer resolution on production scale test samples. The focus is on delivering a technique capable of routine measurement of pattern shape, including critical dimension, sidewall angle, linewidth fluctuations, and line edge roughness, and statistical deviations across large areas in dense high aspect ratio patterns. This method is expected to provide a potential solution for the metrology needs of future semiconductor technology nodes. Further, the wavelengths utilized by SAXS based measurements well complement current metrology tools based on optical scatterometry, SEM, and AFM.

Customer Needs

The drive to reduce feature sizes to sub-50 nm technology nodes continues to challenge metrology techniques for pattern characterization. As outlined in the International Technology Roadmap for Semiconductors, existing techniques such as CD-SEM face significant technical hurdles in quantifying parameters such as Line Edge Roughness (LER) as pattern sizes decrease. Emerging methods based on techniques such as atomic force microscopy are being developed and evaluated. However, uncertainties remain in defining suitable metrology for standardized measurements of both organic and inorganic structures. To address these issues, NIST is evaluating the potential application of small angle X-ray scattering as a measurement tool for both process development and the calibration of standards for current industrial solutions such as CD-SEM.

Technical Strategy

1. Production of sub-30 nm, dense structures for semiconductors, memory, and data storage will demand the control of component size on the level of nm and in some cases sub-nm. These requirements will challenge traditional methods including CD-SEM and optical scatterometry. We are developing a transmission scattering based method capable of Angstrom level precision in critical dimension evaluation over large (50 nm x 50 nm) arrays of periodic structures (see Fig. 1). In contrast to optical scatterometry, SAXS is performed in transmission using a sub-Angstrom wavelength. The high energy of the X-ray source allows the beam to pass through a production quality silicon wafer, and could become amenable to process line characterization. The measurements are performed in ambient conditions, minimizing time required for sample preparation. The current capabilities of commercially available X-ray sources and detectors are sufficient to implement a laboratory scale device

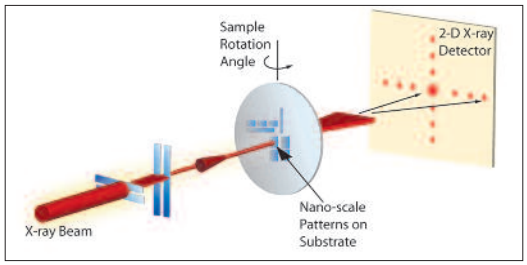

Figure 1. Schematic of the Critical Dimension Small Angle X-ray Scattering (CD-SAXS) configuration. Shown is the collimated high energy X-ray beam passing in transmission through a silicon wafer and scattering from the test pattern on the surface. The scattered X-rays are measured on a 2-dimensional X-ray detector. Cross sectional information is obtained by measuring the sample at varying sample rotation angles as depicted.

Figure 2. The world's first laboratory scale CD-SAXS prototype constructed on the NIST campus. Shown is the rotating anode molybdenum source (left side) used to generate high energy X-rays for transmission measurements on samples measured at varying angles of incidence on a 2-dimensional detector (back right).

capable of high precision measurements. NIST has designed and installed the world's first laboratory scale CD-SAXS device (see Fig. 2).

DELIVERABLES:

- Complete cross-sectional measurements using laboratory scale CD-SAXS instrument on non-planar "FinFET" structures produced in collaboration with Intel. 1Q 2010
- Initiate round robin studies, in collaboration with SEMATECH, to identify the potential limitations of CD-SAXS as a commercially available metrology. Round robin will evaluate the potential capacity CD-SAXS utilizing a range of test samples relevant to semiconductor manufacturing. 4Q 2010

2. Pattern shape metrology is facing new challenges as new 3D structures are emerging including nanometer scale, cyclindrical cross section components, termed "nanowires", suspended in air. These wires are the logical evolution of non-planar architectures such as FinFETs, with nanometer scale dielectric coatings that circumnavigate the cross section of the wire. Effective manufacturing requires characterization of the total pattern shape as well as the dimensions and relative positions of individual layers. CD-SAXS utilizes data taken at a series of angles of incidence to reconstruct the average cross-sectional line shape. Preliminary results from an array of model nanowire structures indicate an ability to measure these complex structures during different stages of processing, providing valuable data on next-generation manufacturing. Ongoing analysis and technique refinement will develop models to quantify with high precision cross sectional shape parameters needed for patterns with multiple, distinct layers to establish the limits of the technique in future technology nodes.

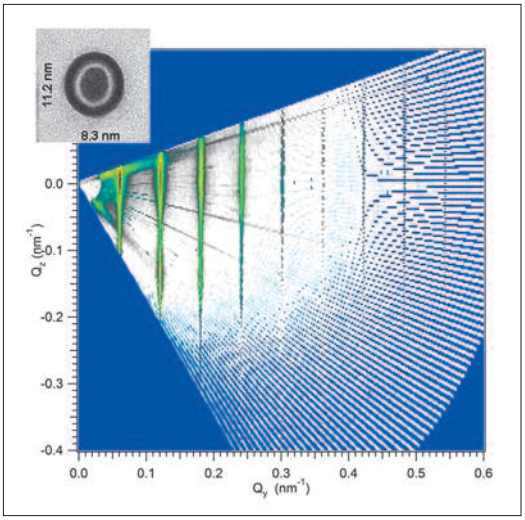

Figure 3. CD-SAXS data from a nanowire array, measured in collaboration with IBM T. J. Watson Research Center. Shown is an intensity contour map plotted in the Qz-Qx plane, where Qz is a scattering vector normal to the substrate and Qx is a scattering vector parallel to the substrate. CD-SAXS measurements are capable of providing high precision measurements of the cross sectional shape of the suspended wires, providing key information for manufacturing and device performance. A representative cross sectional SEM image of a single nanowire is shown in the top left inset.

DELIVERABLES:

- Develop and apply refined CD-SAXS models to model composite nanowires with dielectric coatings. 3Q 2010

Accomplishments

■ We have developed and demonstrated the capabilities of CD-SAXS to provide high precision measurements of pattern pitch, line width, line height, and sidewall angle. The first measurements of sidewall angle were made the Advanced Photon Source (Argonne National Laboratory) in collaboration with the IBM T. J. Watson Research Center (Q. Lin). The protocol involves measurements of the sample over a wide range of incident angles, and reconstructing the Fourier representation of the pattern cross section. For a pattern with trapezoidal cross section, ridges of intensity propagate at twice the sidewall angle. The existence of the ridges is a model independent check on the validity of the trapezoidal model, while different shapes, such as a T-topped line, will produce different scattering patterns. The protocol has been generalized to more arbitrary shapes, including patterns with rounded corners and sidewalls.

■ Our group has also demonstrated a capability to measure correlated fluctuations in line edge position as a measure of line edge roughness. CD-SAXS measurements of a series of line/space patterns with model LER were produced using 193 nm lithography in collaboration with the Advanced Metrology Advisory Group (AMAG) coordinated by SEMATECH. This initial study provided key data on the sensitivity of CD-SAXS to LER, including the development of models for LER and LWR contributions, in lines possessing periodic sidewall roughness with amplitudes of 3 nm. In addition, a methodology and experimental

data was published describing a route to use CD-SAXS as a measure of roughness propagating normal to the substrate. Samples of photoresist line/space patterns were provided by the IBM T. J. Watson Research Center (A. Mahorawala). This type of roughness is commonly observed in photoresists due to imprecise tuning of the underlying anti-reflective coating. Given the ability of CD-SAXS to extract the periodic component of roughness from non-periodic, the technique is capable of quantitatively extracting this component of roughness even when the amplitude is small compared to the random component.

■ NIST has completed the second round-robin measurements of LER in sub-50 nm line/space resist patterns using CD-SAXS. Samples were designed with controlled LER to be measured by CD-SEM and CD-SAXS in blind measurements. Samples were produced in collaboration with Intel and measured by optical scatterometry at Intel, by CD-SEM at SEMATECH, and CD-SAXS at NIST in blind measurements. The data were collected and summarized in a paper presented at the 2008 SPIE Advanced Lithography meeting.

■ Studies have also demonstrated the potential of CD-SAXS to detect and to quantify the extent of sidewall damage of nanoporous low-κ materials patterned into line/space patterns. Previously, NIST had demonstrated that blanket low-κ films exposed to a plasma etch can have a skin layer with increased density and less hydrogen that may reflect the collapse of the pore structure. Since plasma etch effects can lead to an increase in κ, it is important to measure the sidewall structure (porosity, electron density, etc.) of patterned low-κ films. To address this challenge, SEMATECH provided line gratings etched in a candidate low-κ material, then backfilled the trenches with the same candidate low-κ material. This backfilled sample simplifies modeling efforts and highlights the damaged regions to X-rays. These results indicate the potential of CD-SAXS to probe more complex structures such as FinFETs non-destructively for future manufacturing needs.

■ The real time shape evolution of nanoimprinted polymer patterns were measured as a function of annealing time and temperature using Critical Dimension Small Angle X-ray Scattering (CD-SAXS). Periodicity, linewidth, line height, and sidewall angle were determined with nanometer resolution for parallel line/space patterns in poly(methyl methacrylate) (PMMA) both below and above the bulk glass transition temperature (Tg). Heating these patterns below Tg does not produce significant thermal expansion, at least to within the resolution of the measurement. However, above Tg, the fast rate of pattern melting at early time transitions to a slowed rate in longer time regimes. The time dependent rate of pattern melting was consistent with a shape dependent thermal stability, where sharp corners possessing large Laplace pressures accelerate pattern dynamics at early times.

Collaborations

Polymers Division, MSEL, Chengqing Wang, Derek L. Ho, Christopher L. Soles.

Intel Corporation, Kwang-Woo Choi, James Clarke, George Thompson, Melissa Shell, sub-50 nm structures.

SEMATECH, Ben Bunday, Pattern production and correlation to optical scatterometry (also through Advanced Metrology Advisory Group).

Advanced Photon Source, Argonne National Laboratory, Steven Weigand and Denis Keane, Small Angle X-ray Scattering Instrumentation Development.

Molecular Imprints, Doug Resnick. Characterization of sub-50 nm structures including dense arrays of posts.

IBM Yorktown Heights, Qinghuan Lin, Development of pattern shape and sidewall angle metrology.

Publications

C. Wang, K. Choi, Y. Chen, J. Price, D. Ho, R. Jones, C. Soles, E. K. Lin, W.-L. Wu, B. Bunday *"Non-planar high-k dielectric thickness measurements using CD-SAXS"* Proc. SPIE 7272, (2009).

D.L. Ho, C. Wang, E. K. Lin, R. L. Jones and W.-L. Wu, *"A Laboratory Scale Critical-Dimension Small-Angle X-ray Scattering Instrument"*, AIP Conference Proceedings, 931, 382, (2007).

C. Wang, R. L. Jones, E. K. Lin, W.-L. Wu, B. J. Rice, K. Choi, G. M. Thompson, S. J. Weigand, D. T. Keane, *"Characterization of Correlated Line Edge Roughness of Nanoscale Line Gratings using Small Angle X-Ray Scattering,"* J. Appl. Phys. 102, 024901 (2007).

C. Wang, R. L. Jones, E. K. Lin, W.-L. Wu, J. Leu, *"Standing Wave Roughness Characterization in Photoresists by*

Small Angle X-Ray Scattering," Appl. Phys. Lett. 90, 193122 (2007).

Y. Ding, H. W. Ro, J. F. Douglas, R. L. Jones, D. R. Hines, A. Karim, C. L. Soles *"Polymer Viscoelasticity and Residual Stress Effects on Nanoimprint Lithography,"* Adv. Mater. 19, 1377 (2007).

C. Wang, R. L. Jones, E. K. Lin, W.-L. Wu, J. S. Villarrubia, K. Choi, J. S. Clarke, B. J. Rice, M. Leeson, J. Roberts, R. Bristol, B. Bunday, G. Orji, *"Line edge roughness characterization of sub-50 nm structures using CD-SAXS: Round-Robin benchmark results,"* Proc. SPIE 6518, (2007).

R. L. Jones, C. L. Soles, E. K. Lin, W. Hu, R. M. Reano, S. W. Pang, *"Pattern Fidelity in Nanoimprinted Films using CD-SAXS,"* J. Microlith. Microfab. Microsyst. 05, 013001 (2006).

R. L. Jones, W.-L. Wu, C. Wang, E. K. Lin, K.-W. Choi, B. J. Rice, G. M. Thompson, S. J. Weigand, D. T. Keane *"Characterization of Line Edge Roughness using CD-SAXS,"* Proc. SPIE 6152, 215 (2006).

H. W. Ro, Y. Ding, H. J. Lee, D. R. Hines, R. L. Jones, E. K. Lin, A. Karim, W.-L. Wu, C. L. Soles, *"The Role of Stress in Nanoimprint Lithography,"* Proc. SPIE 6151, 348 (2006).

R. L. Jones, T. Hu, C. L. Soles, E. K. Lin, R. M. Reano, S. W. Pang, D. M. Casa, *"Real Time Shape Evolution of Nanoimprinted Polymer Structures during Thermal Annealing,"* 6, 1723 (2006)

Grazing Incidence X-Ray Scattering-Based Dimensional Metrology

Technical Contacts:
W. L. Wu
R. L. Jones

Goals

To develop a grazing incidence small angle X-ray scattering (GI-SAXS)-based methodology to complement normal incidence transmission critical dimension small angle X-ray scattering (CD-SAXS). The focus of the project is to deliver a technique capable of routine measurement of pattern shape, including critical dimension, sidewall angle, depth dependent composition, and statistical deviations across large areas in dense high aspect ratio patterns. In contrast to transmission, and small angle X-ray scattering GI-SAXS is performed in reflection. This configuration results in both significant challenges in data interpretation and vast increases in signal-to-noise; therefore, it makes possible a reduction in measurement time. This method is expected to provide a potential solution for the metrology needs of future semiconductor technology nodes. In comparison with transmission SAXS, a longer X-ray wavelength X-ray beam can be used for GI-SAXS; this will help relax some of the strict optical collimation requirements and help reach high flux at the sample.

Customer Needs

The drive to reduce feature sizes to sub-32 nm technology nodes continues to challenge metrology techniques for pattern characterization. As outlined in the International Technology Roadmap for Semiconductors (http://public.itrs.net), existing techniques such as CD-SEM face significant technical hurdles in quantifying parameters such as Line Edge Roughness (LER) as pattern sizes decrease. Emerging methods based on techniques such as atomic force microscopy are being developed and evaluated. However, uncertainties remain in defining suitable metrology for standardized measurements of both organic and inorganic structures. To address these issues, NIST is evaluating the potential application of small angle X-ray scattering as a measurement tool for both process development and the calibration of reference standards for current industrial solutions such as CD-SEM.

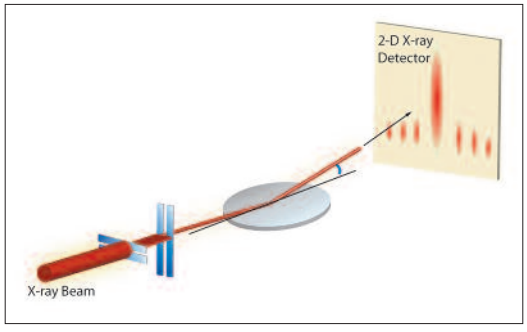

Figure 1. Schematic of the Grazing Incidence Small Angle X-ray Scattering (GI-SAXS) measurement configuration. Shown is the collimated sub-nm wavelength X-ray beam reflecting off the sample at a grazing angle, and the diffraction pattern measured on a 2-dimensional X-ray detector.

Technical Strategy

1. The emergence of viable lithography solutions for sub-32 nm patterning will require sub-nm precision control of CD and pattern shape built within multilayer structures. These requirements will challenge traditional measurement methods including CD-SEM and optical scatterometry. We are developing X-ray based dimensional metrology tools capable of Angstrom level precision in critical dimension evaluation over large (50 nm x 50 nm) arrays of periodic structures. As depicted in figure 1, Grazing Incidence Small Angle X-ray Scattering (GI-SAXS) is performed in reflection, using a configuration similar to current optical-based CD metrology tools. Due to the large interaction of the beam with the sample, generalizable quantitative models of GI-SAXS data are not available. Models to describe the high degree of interaction of the X-ray beam with the sample at grazing incidence will require detailed measurements of instrumental coherence length, resolution functions, and wavelength distribution. In addition, experiments are required to determine the effects of dynamic diffraction. Our approach is to measure the structure of test patterns using both CD-SAXS and grazing incidence geometries. This two measurement approach will provide a unique capability to develop quantitative models to incorporate the effects of dynamic scattering effects characteristic of grazing incidence scattering but absent in transmission scattering. Test samples will leverage results from CD-SAXS studies developed and measured in cooperation with the Advanced Metrology Working Group at SEMATECH and Intel.

DELIVERABLES:

- Develop a quantitative measure of X-ray coherence lengths that can be performed on commercial X-ray reflectometers for periodically patterned substrates of varying pitch. 2Q 2010
- Establish limits of the effective medium approximation that delineates the boundary between dynamic scattering models and kinematic models that employ Born's first approximation. 3Q 2010

2. An emerging metrology need in semiconductor and data storage fabrication is in directed self-assembly (DSA). Here, soft materials such as block copolymers assemble with structure on the order of 10 nm under the influence of a directing field or template. The soft nature of their interfaces and the large areas involved present new metrology challenges as highlighted in the emerging lithography section of the ITRS. With a significantly higher signal to noise ratio, GI-SAXS is capable of providing measurements of dimensions during assembly, providing unique insights into potential process parameters and uniformity of the structures over macroscopic areas. The small electron density contrast of these films prohibit the application of transmission SAXS. As such, our strategy is to develop models for dimensional metrology of block copolymers undergoing directed self-assembly through comparisons of GI-SAXS data to analogous data from transmission small angle Neutron scattering, performed at the NIST Center for Neutron Research.

DELIVERABLES:

- Develop computational methods to accommodate distributions of grain orientation, grain size, and line edge roughness in block copolymers assembled by DSA. 3Q 2010
- Complete transmission small angle neutron scattering (SANS) measurements of block copolymers assembling within physical templates, establishing the role of added homopolymer to relieve elastic stresses and reduce orientational splay. 4Q 2010

Accomplishments

■ Measurements of a block copolymer film assembled near a potential surface transition temperature have been executed. The data shown in figure 2 show GI-SAXS data from a thin film of a poly(styrene-b-methyl methacrylate) block copolymer self-assembled on a silicon substrate. The data indicate a secondary morphology with different pitch at the surface that can be eliminated through an appropriate choice of annealing temperature. The existence of a process dependent secondary morphology is one of the many factors that will make patterning through self-assembly complex. Mapping the process parameter space and its effect on BCP morphology, orientation, and grain size is a key strength of GI-SAXS, which can probe organic, mesoscopically disordered films in relatively short time scales. The polymer is annealed and self-assembles into cylinders that lie parallel to the substrate, but form fingers or spheres at the top surface at high annealing temperatures, but is more stable as a single morphology at lower temperatures. The depth sensitivity of GI-SAXS is an area of great interest being developed by our team.

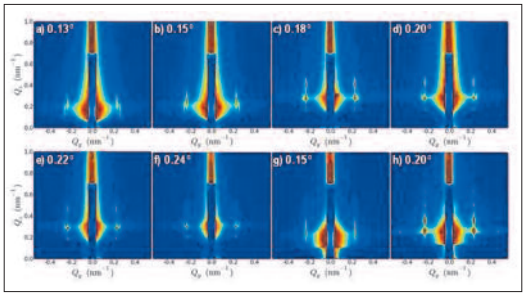

Figure 2. GI-SAXS data from a thin film of a poly(styrene-b-methyl methacrylate) block copolymer on a silicon substrate. In (a - g), the depth of the X-ray beam increases with increasing incidence angle. A primary peak at lower q values represents the spacing of cylinders laying parallel to the substrate. A secondary peak at higher q indicates a secondary morphology with slightly smaller repeat period. The secondary peak becomes less visible with increasing depth. A film annealed at a lower temperature (h) shows no secondary morphology, making it a more ideal candidate for patterning applications.

■ We have completed the initial programming phase of a new algorithm and associated software package that will have the capacity to quantitatively fit an arbitrary structure provided by the user. Current packages are limited to analytically tractable solutions, such as highly disordered or highly ordered systems. Ours will be the first package capable of addressing systems of arbitrary chemistry, ordering, and dimensionality. This will most notably include systems of mesoscopic 3-dimensional ordering at the nanoscale such as in DSA formed block copolymer films.

Collaborations

1Polymers Division, MSEL, R. Joseph Kline, Chengqing Wang, Derek L. Ho, Christopher L. Soles.

Hitachi Global Data Storage, Ricardo Ruiz, GI-SAXS metrology for directed self-assembly.

Intel Corporation, Kwang-Woo Choi, James Clarke, George Thompson, sub-50 nm test structures.

SEMATECH, Ben Bunday, Pattern production and correlation to optical scatterometry (also through Advanced Metrology Advisory Group).

Advanced Photon Source, Argonne National Laboratory, Steven Weigand and Denis Keane, Small Angle X-ray Scattering Instrumentation Development.

Publications

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D.L. Ho, C. Wang, E. K. Lin, R. L. Jones and W.-L. Wu, *"A Laboratory Scale Critical-Dimension Small-Angle X-ray Scattering Instrument,"* AIP Conference Proceedings, 931, 382, (2007).

C. Wang, R. L. Jones, E. K. Lin, W.-L. Wu, B. J. Rice, K. Choi, G. M. Thompson, S. J. Weigand, D. T. Keane, *"Characterization of Correlated Line Edge Roughness of Nanoscale Line Gratings using Small Angle X-Ray Scattering,"* J. Appl. Phys. 102, 024901 (2007).

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C. Wang, R. L. Jones, E. K. Lin, W.-L. Wu, J. S. Villarrubia, K. Choi, J. S. Clarke, B. J. Rice, M. Leeson, J. Roberts, R. Bristol, B. Bunday, G. Orji, *"Line edge roughness characterization of sub-50 nm structures using CD-SAXS: Round-Robin benchmark results,"* Proc. SPIE 6518, (2007).

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H. W. Ro, Y. Ding, H. J. Lee, D. R. Hines, R. L. Jones, E. K. Lin, A. Karim, W.-L. Wu, C. L. Soles, *"The Role of Stress in Nanoimprint Lithography,"* Proc. SPIE 6151, 348 (2006).

R. L. Jones, T. Hu, C. L. Soles, E. K. Lin, R. M. Reano, S. W. Pang, D. M. Casa, *"Real Time Shape Evolution of Nanoimprinted Polymer Structures during Thermal Annealing,"* 6, 1723 (2006).

Atom-Based Dimensional Metrology

Technical Contacts:
R. Silver

Goals

Provide technological leadership to semiconductor and nanoelectronics manufacturers and other government agencies by developing the methods, tools, and artifacts needed to apply leading edge, high-resolution atom-based dimensional measurement methods to meet the metrology needs for advanced lithography. One specific goal is to provide customers with the techniques and standards needed to make traceable dimensional measurements on wafers with nanometer accuracy. We are developing nanometer-scale three-dimensional structures of controlled geometry whose dimensions can be measured and traced directly to the intrinsic crystal lattice. These samples are intended to be dimensionally stable and allow transfer to other measurement tools that can measure the artifacts with dimensions known on the nanometer scale.

Customer Needs

This project responds to the U.S. semiconductor industry's need for length-intensive measurement capabilities and calibration standards in the nanometer scale regime. The new class of scanned probes have unparalleled resolution and present a unique solution to meet the future measurement, test artifact, and calibration standards needs of the nanoelectronics industry. One important application of the high-resolution scanning probe microscope (SPM) methods is in the development of test artifacts and linewidth standards whose dimensions can be measured and traced through the crystal lattice from which they are made.

The work funded in this project is for the development of atom-based test artifacts and linewidth standards to assist in the development of high-resolution imaging techniques and calibration of dimensional metrology tools. One focus of the research is to enable the accurate counting of atom spacings across a feature in a controlled environment and to subsequently transfer that artifact to other measuring instruments as a structure with atomically known dimensions.

An essential element of this project is the fabrication of test artifacts and structures for the development of high resolution imaging methods. It is imperative to enable fabrication methods for sub-10 nm sized features. Several recent developments in optical microscopy, scatterometry and scanning electron microscope (SEM) metrology require test samples with critical dimensions below 10 nm. These test structures are simply not available commercially at this time. In this project we are developing the methods for fabrication of sub-10 nm sized features and etching methods to transfer these patterns into the silicon substrates (see Fig. 1). As critical dimensions continue to shrink, the detailed atomic structure, such as edge roughness or sidewall undercut, of the features to be measured represents a larger portion of the measurement uncertainty. Furthermore, particularly with SEMs and optical critical dimension (CD) tools, the instrument response and the uncertainty in the edge location within an intensity pattern becomes a significant issue due to the increased sensitivity to detailed elements of the edge detection model. The complexity of these physics-based scattering models and large computer resources required for each individual computation necessitates reference samples with known geometry and width. This project is developing samples of known geometry and atomic surface structure that will yield well defined dimensional measurements. One goal is a measurement that results in a specific number of atoms across the line feature or between features. The process being developed allows for samples to be measured in the ultra high vacuum (UHV) environment and then stabilized and subsequently transferred to other instruments.

The methods of atom counting outlined in this project description are non-destructive and are intended to yield samples which can be measured

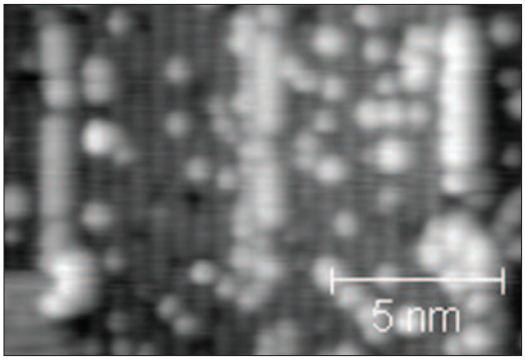


Figure 1. Sub 5 nm scale STM patterned silicon passivation. The structures are now being controlled at the atomic scale.

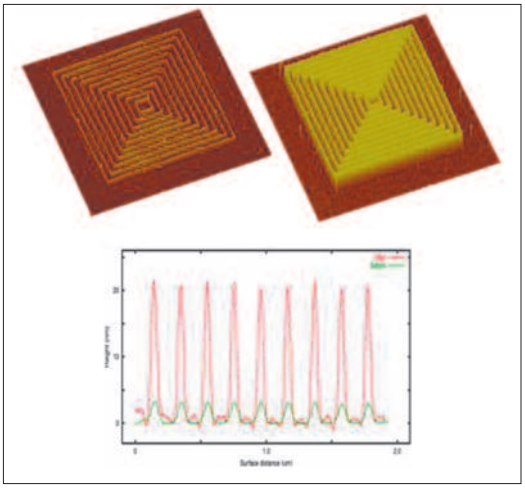


Figure 2. A demonstration of the nanofabrication process with an RIE process used to transfer the patterns into the silicon substrate.

by various instruments such as an SEM optical CD tool with subsequent re-measurement on the atomic scale. This is a unique and important element of this work since there are no other known methods that allow this kind of atomic dimensional measurement without being destructive. In addition, this new method opens up the possibilities of basing the measurement metric on the intrinsic crystal lattice.

Technical Strategy

The technical work is focused into four thrust areas.

1. The development of methods to prepare lithographically patterned three-dimensional structures in semiconductor materials. These structures are being prepared in silicon to allow the patterned features to be commensurate with the underlying crystal lattice. This involves using a combination of advanced photolithography methods or electron beam lithography to pattern larger fiducials and the scanning tunneling microscope (STM) itself to fabricate very small nanometer scale features as shown in Fig. 2.

DELIVERABLES:

- Write features in (100) silicon with critical dimensions smaller than 3 nm. Apply the pattern generation process to depassivate silicon surfaces to demonstrate sub-3 nm critical dimensions using the STM). 4Q 2010
- Work with DARPA, Zyvex and CNST to develop improved methods for etching nanostructures written in silicon. Use Reactive Ion Etching (RIE) techniques to etch features with sub-5 nm dimensions in silicon. 2Q 2011

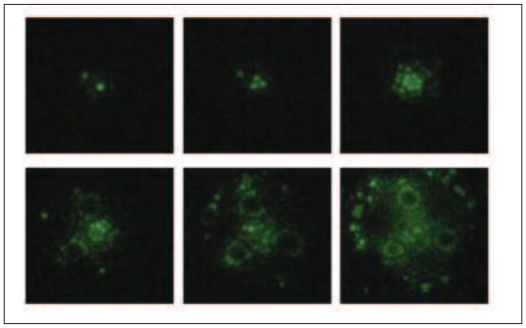


Figure 3. A series of FIM images showing reproducible formation of single atoms and atomic trimer showing formation at the apex of a W (111) single crystal tip.

2. The development of techniques for the preparation of SPM tips with reproducible geometries and the direct characterization of the SPM tip geometry and dimensions on the atomic scale. These well characterized tip probes can then be used to make robust, repeatable measurements on samples with atomic resolution at the sub-nanometer length scale, see Fig. 3. We continue to develop SPM tip etching, field evaporation, and thermal processing procedures to reliably yield stable W (111) or W (110) tips that produce atomic resolution on reconstructed Si surfaces and passivated Si (100) surfaces. These tips are also useful in SEM applications for use as nanotip SEM field emitters. Our tip preparation methods leave us uniquely qualified in this arena.

DELIVERABLES:

- Develop and evaluate new high temperature thermal processes in combination with field Ion-electron cleaning to create atomically sharp W (111) and W (110) tips. Determine the sharpness and stability of these W tips for use in atomic resolution STM imaging. 2Q 2010
- Demonstrate repeatable atomic resolution tip preparation on multiple tips and develop a procedure to regenerate the tips after usage. Evaluate atomic Imaging following multiple tip processes. Evaluate using FIM and STM atomic resolution imaging. 4Q 2010

3. Develop artifacts that can be atom-counted and subsequently measured in other metrology tools such as SEM and atomic force microscope (AFM). The integrity of the line geometry, such as side wall angle, is crucial to having useful artifacts for linewidth specimens. This effort for linewidth artifacts is currently focused on developing Si (100) UHV thermal processing methods with reduced process temperatures which yield atomically ordered surfaces. Current research uti-

lizes in situ processing apparatus from the UHV STM and is concentrated on the reproducible production of atomically ordered Si surfaces and Si (100) step and terrace structures.

DELIVERABLES:

- Use the UHV sample heating and tip preparation capabilities in the Omicron UHV STM system for atomic resolution imaging of Si (100) hydrogen terminated surfaces. Demonstrate routine atomic resolution imaging of UHV H-terminated Si samples. Use the in situ prepared samples from the UHV preparation facility to evaluate improved Si imaging with alternative tip materials and atomic surface reconstructions. 2Q 2010

4. Use the UHV Omicron system and the in-house designed facility to implement thermal processing of micrometer sized fiducial markings. Evaluate a range of mark geometries and process parameters to determine optimal fiducial mark design, see Fig. 4. Apply the fiducial processes to etched silicon features in collaboration with the Zyvex-led DARPA-funded Atomically Precise Manufacturing Consortium. The intent is to provide atomically resolved and precisely imaged quantitative results on etched silicon fiducial structures and determine their application to controlling silicon surface morphology. These micrometer-scale markings act as fiducial structures that can be located using optical tools and electron microscopes.

Accomplishments

■ The atom-based dimensional metrology project is successfully engaged in phase 2 of a 5 year funded Defense Advanced Resource Projects Agency (DARPA) contract to develop massively parallel arrayed tip nanofabrication techniques. This DARPA funded contract is a comprehensive collaborative effort between National Institute of Standards and Techology (NIST), Zyvex, University of Illinois, the University of Texas and other partners. This represents a significant DARPA focus for advanced lithography and metrology on the atomic scale which is fully extensible to atomically precise patterning and metrology to support and enable arrayed tip fabrication at the atomic scale.

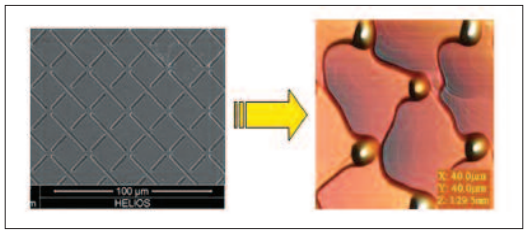


Figure 4. Fiducial marks have been shown to withstand the very high processing temperatures. These marks also have a profound effect on the resulting morphology and recent works is focused on harnessing the fiducial marks to control the atomic terrace sizes.

■ Atomically sharp W (110) and W (111) tips can now be repeatedly prepared with single, two and three atomic configurations at the apex. This is a robust methodology for repeatable atomic resolution UHV tip preparation. This is accomplished using thermal tip processing in the UHV preparation chambers and the field ion field electron microscope (FIFEM). We are currently transferring these techniques to our industry and university collaborators for enhanced atomic resolution tip performance.

■ Two alternative hydrogen cracker designs have been used to disassociate the hydrogen molecules to initiate atomically ordered hydrogen terminated surfaces routinely. Current research is aimed at optimizing the in situ UHV hydrogen termination process and minimizing vacancies or defects to enable nearly perfect long range atomic order. This process stabilizes the surface for several days as well as creating an effective atomic resolution resist.

■ The field ion microscope (FIM) technique is routinely used to analyze and perform the first UHV steps to create single atom apex tips using lower cost W (110) and single crystal W (111) tip. The tungsten tips are heated to moderately high temperatures to reconstruct spontaneously into a pyramidal-like formation with a single atom at the apex. These W tips can be regenerated for repeated use as SPM tips for dimensional analysis on the atomic scale.

■ A poster presentation was given at the 2009 Electron Ion and Photon Beam (EIPBN) conference on the silicon etching processes developed at NIST in the atom-based dimensional metrology project. The presentation covered patterns fabricated with features as small as 10 nm written in hydrogen-terminated silicon surfaces. Also, comprehensive FIM analyses of tip processes were covered. The importance of etching structures in Si (100) is now recognized as one of the essential DARPA funded directions as a part of the atomically precise manufacturing consortium. NIST

will continue to develop lithography methods and plasma-etch methods for sub-5 nm CD features.

■ The atom-based dimensional metrology project has made a substantial step forward in atomic scale patterning. Recent advances in the UHV hydrogen termination process has enabled well aligned atomic surfaces to act as templates for atomic patterning for use in atomic resolution metrology standards. Recent images show a significant advance in the resolution and stability of these surfaces to include individual atom resolution along and within the dimmer rows.

■ We have made significant progress in preparing atomically flat surfaces and obtaining atomic order on Si (100) surfaces. The routine imaging of these surfaces on the atomic scale has been demonstrated successfully in the move of the silicon processing to the more widely used Si (100) surfaces and to use more controlled UHV processing techniques. These results are a substantial step forward in repeatable silicon surface preparation for atomic scale metrology and are now being carried out in collaboration with DARPA and several industry/university researchers. The results, seen in Fig. 5, show the recent progress in atomic resolution imaging and preparation of the Si (100) surfaces and are a primary direction for the DARPA funded research manufacturing community.

■ NIST hosted the Q1 Phase 2 DARPA program review and follow on technical workshop. A two day review and workshop on atomic scale fabrication and metrology for arrayed tip technologies was held at NIST in May involving most of the DARPA funded Automatically Precise Manufacturing Consortium (APMC) as well as invited external guests.

■ Presentation to Texas state technology representatives and business leaders and third quarterly review held for the Atomically Precise Manufacturing Consortium sponsored by DARPA.

Collaborations

DAROPA, Zyvex, University of Illinois, University of Texas, Sematech, IBM, University of Maryland, Dept. of Physics, George Washington University, Dept. of Mech. Eng.

Publications

H. Zhou, J. Fu, and R. M. Silver, *"A Time-resolved Kinetic Monte-Carlo Simulation Study on Si (111) Etching,"* Journal of Physical Chemistry C, Vol. 111, p. 3566 (2007).

S. Chikkamaranahalli, R. Vallance, B. Damazo, and R. M. Silver, *"Damping Mechanisms for Precision Applications in UHV Environment,"* Proc. ASPE Conf., Pitts. PA (2006).

S. Chikkamaranahalli, R. Vallance, B. Damazo, R. M. Silver, and J. Gilsinn, *"Dynamic Modeling and Vibration Analysis of a UHV Scanning Tunneling Microscope,"* Proc. ASPE Conf., Norfolk VA (Oct. 2005).

H. Zhou J. Fu, and R. M. Silver *"The Influence of Defects on the Morphology of Si (111) Etched in NH4F,"* J Chemical Physics B, 109, 23386 (2005).

Fabrication and Calibration Metrology for Single-Crystal CD Reference Materials

Technical Contacts:
M. W. Cresswell

Goals

The goal of this project is to develop test-structure-based reference materials with emphasis on supplying road-map-compliant physical standards for critical-dimension (CD) metrology-tool development and calibration. The specific near-term goal is fabricating, and supplying to the NIST SRM (Standard Reference Material) office for distribution, a quantity of CD reference-features with nominal CDs in the range 20 nm to 160 nm and having 2σ (expanded uncertainties) of less than 1.1 nm by August 2011. The motivating application is primarily AFM-tip calibration but other possible applications that have emerged, since the research was begun, include the monitoring of optical CD metrology (OCD) tools. The technology that this project has developed for fabricating CD reference materials is known as the Single-Crystal CD Reference-Material (SCCDRM) implementation. It is now clear that the SCCDRM format could also be advantageously applied to the development of related nano-artifacts such as step-height standards. An over-arching goal is to fabricate and calibrate a selection of SCCDRM-based artifacts that will be made available to industry and academic users through the NIST SRM Program. This goal will be well-served by the Project's ongoing uncertainty-reduction program which will take advantage of unique and diverse expertise at NIST in alternative primary- and transfer-metrologies such as SAXS (Small-Angle X-Ray Scattering) and angle-resolved optical scatterometry.

Customer Needs

The Semiconductor Industry Association's International Technology Roadmap for Semiconductors (ITRS) 2007 p.39 under "Reference Materials" Section in the Metrology Volume, states that it is critically important to have suitable reference materials available when a measurement is first applied to a technology generation, especially during early materials- and process-equipment development. This project is concerned specifically with ensuring a source of such reference materials to satisfy the stated need throughout the near-term years.

Each generation of ICs is characterized by the transistor gate length whose control to specifications during IC fabrication is a primary determinant of manufacturing success. The roadmap projects the decrease of microprocessor unit (MPU) physical gate lengths used in state-of-the-art IC manufacturing from present levels of 28 nm to 13 nm during the near-term years. Scanning electron microscopes (SEMs) and other systems used for traditional linewidth metrology exhibit measurement uncertainties exceeding specifications for these applications. It is widely believed that the situation can be at least partially managed through the use of reference materials with linewidths traceable to nanometer-level uncertainties. Until now, such reference materials have been unavailable because the technology needed for their fabrication and certification has not been available.

Customers need to replace the carrier-wafer with a monolithic implementation because the former is vulnerable to contamination originating during post-assembly cleaning. Ordinarily this is not a leading concern in AFM-tip calibration, although it cannot be dismissed for SCCDRM use in ultra-clean facilities. Otherwise, tip calibration is becoming widely recognized as an application for which SCCDRM reference materials are well suited. However, an emerging application of interest in the industry is SEM tool calibration. In this application, regular reference-material feature-cleaning is necessary due to the nature of the metrology.

The emerging metrology known as optical-CD (OCD) scatterometry translates broadband light, diffracted from an on-wafer grating patterned into the resist or film, into accurate profiles of the grating's features from which key parameters, such as CD, can be extracted. Whereas currently favored metrology tools such as CD scanning electron microscopes and AFMs require a vacuum wafer environment, OCD metrology does not, and is fast and non-invasive. The possibilities of OCD extend to characterizing the sidewall angle and height of critical features. Until physical standards are available, the full promise of OCD control scatterometry may not be met.

Further details of customer needs that have been identified since the SCCDRM distribution to SE-

MATECH Member Companies in January 2005, and now impact the project's responding technical strategy, are described in the next section.

Technical Strategy

The fundamental SCCDRM technical strategy is to pattern Silicon on Insulator (SOI) device layers with lattice-plane selective etches of the kind used in silicon micro-machining, which provides reference features with quasi-atomically-planar sidewalls. This unique attribute is highly desirable for the intended applications, particularly if sidewall nano-planarity can be further extended to reference-feature segment lengths of up to 2 micrometers. Essential elements of the implementation include starting silicon SOI wafers with the device layer having a (110) orientation, alignment of the reference features to specific lattice vectors, and lithographic patterning with lattice-plane selective etches of the kind used in silicon micro-machining. However, the difficulty of obtaining satisfactory SOI material in larger diameters has driven us towards parallel evaluation of a bulk-wafer starting-material strategy. The roadmap states that measurement and certification of reference materials must be carried out using standardized or well-documented test procedures. The traceability path for dimensional certification of the project's SCCDRMs is responsive to this requirement and originates with measurement of a selection of reference-feature CDs with both Atomic-Force Microscopy (AFM) and high-resolution transmission electron microscopy (HRTEM) imaging. The former technique is highly repeatable and of manageable cost while the latter enables a lattice-plane count that allows expression determination of CD in terms of a traceable distance, which is the periodicity of silicon (111) lattice planes. However, HRTEM is totally destructive and thus is not useful for supplying reference features to end users. The project's traceability strategy thus features state-of-the-art AFM as a transfer metrology to deal with this constraint. Transfer metrology relates CDs extracted by AFM to be traced to SI units through the construction of a so-called calibration curve. An example of such a curve is shown in Fig. 1.

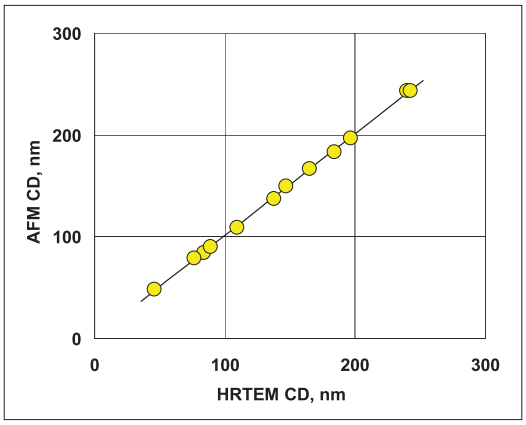


Figure 1. Transfer metrology relates CDs extracted by AFM to be traced to values SI units through the construction of a so-called calibration curve.

To maintain maximum possible accuracy in the transfer-metrology operation, an elaborate reference-feature selection protocol has been established to identify reference features that qualify by virtue of their CD uniformity, as contributors to the construction of the calibration curve, or for delivery to end users. Multiple reference features on a large set of as-patterned test chips are identified initially by high-power optical inspection. This procedure checks primarily for continuity, cosmetics, and apparent uniformity of the narrowest-drawn sets of six features that are incorporated into test structures, which are called HRTEM targets. Drawn feature linewidths range from 350 nm to 600 nm and the "process bias" typically decreases these to etched CDs of between 50 nm and 300 nm. The "best" 10 % of the AFM targets passing optical inspection, and having estimated replicated CDs in the range 50 nm to 200 nm, are then SEM-imaged at 20 K magnification to narrow the selection process further. Digitized profiles of the CDs of top-down SEM images are then extracted at 25 nm intervals. The measurements are transferred to a database, which is then interrogated to identify chips, and AFM targets on them, that have more uniform SEM-CD profiles at the narrower CDs — typically less than 150 nm. Candidate AFM targets identified on each chip are then CD-profiled by AFM. Chips having AFM targets with all six features having superior uniformity are then partitioned into a calibration sub-set and a product subset. All six features of the selected targets on the chips on the calibration sub-set are then subjected to HRTEM imaging. These are the chips whose designated AFM targets are to be used as contributors to the calibration curve. The design of all HRTEM targets enables the capture of six HRTEM images in a single dual-beam FIB-and-thinning

operation. Moreover, since the features on each target are designed such that they are systematically staggered in CD by increments of 30 nm, HRTEM inspection of a single target enables the generation of a 6-point calibration curve spanning a 150 nm range. However, the logistics described above make the CD-traceability path very costly to implement, and hinder the pace of necessary technology advancement. A central problem is that adequate facilities for both HRTEM and AFM tend to have limited availability. Cost becomes substantial when operator/engineering skills, maintenance, down time, etc., are accounted for. For these reasons we have proposed evaluation of two alternative traceability approaches, but this work is currently on the backburner. The first is to identify technically and economically acceptable replacements for either or both of the current primary and transfer metrologies, and the second is to eliminate the need for transfer metrology altogether by calibrating with a single traceable metrology on a 100 % basis. As far as replacing HRTEM as the primary metrology is concerned, we have observed that both SAXS and OCD could provide competitive accuracy for the average CD of features of an SCCDRM grating. Of course, it follows that the uncertainty of a local CD within the grating is then driven by the uniformity of the grating's features. A possible AFM transfer-metrology replacement is CD-SEM. Its superior repeatability for a transfer-metrology application is very attractive while its generally unproven accuracy is inconsequential for this application. Whereas a novel approach to generating a calibration curve for a HRTEM/CD-SEM primary/secondary-metrology implementation has been proposed, the CD-SEM tool's tendency to deposit hydro-carbon contamination remains a central issue. Clearly, verifiable contamination-removal procedures have to be implemented. It appears that scatterometry-based OCD metrology is also feasible as a single traceable metrology for calibration because it is relatively inexpensive and, unlike HRTEM, is non-destructive to apply. However, the issue that the uncertainty of a local reference CD within the grating would be driven by the uniformity of the grating's features needs to be addressed by fabrication-process engineering. While it is not clear that CD-SEM metrology is ready to perform as a primary metrology for the subject application, it appears to be the only possibility for replacing AFM as the transfer metrology for the calibration of isolated lines. On the other hand, this project has proposed a test-structure innovation that would allow the transfer of a measurement of the average CD of a grating metrology to an isolated line. However, the proposed method has not yet been evaluated in the laboratory. Because 200 mm (110) starting material until recently has been unobtainable at an acceptable cost, this project's technical strategy has so far been to dice each 150 mm (110) wafer after lithography and to mount the separate chips in micro-machined standard 200 mm carrier wafers to accommodate the product reference-feature chips. The scheme is shown in Fig. 2. The result is that finished units can be delivered at an acceptable cost. The Project's technical strategy is now evolving towards a monolithic-wafer implementation in response to industry pressure to make SCCDRMs more compatible with automated wafer-handling systems and related end-user requirements. These measures include:

- replacing the carrier-wafer with a monolithic 200 mm wafer implementation evolved from initial development with smaller diameter whole wafers,

- using electron-beam direct-write patterning of a silicon-nitride hard-mask film deposited on bulk-silicon wafers for pattern transfer from database to facilitate CD reduction to 20 nm,

- adopting additional measures to further reduce the uncertainties of calibrated CDs to less than 1.0 nm,

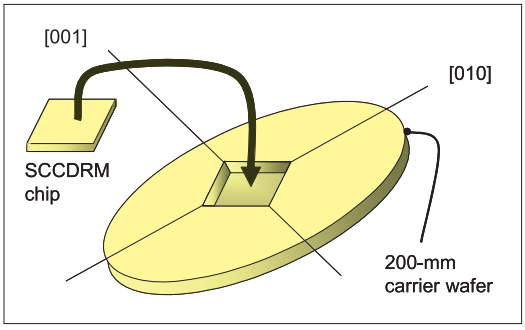


Figure 2. The technical strategy has been to dice each 150 mm (110) wafer after lithography and to mount selected chips in micro-machined standard 200 mm carrier wafers to accommodate the product reference-feature chips.

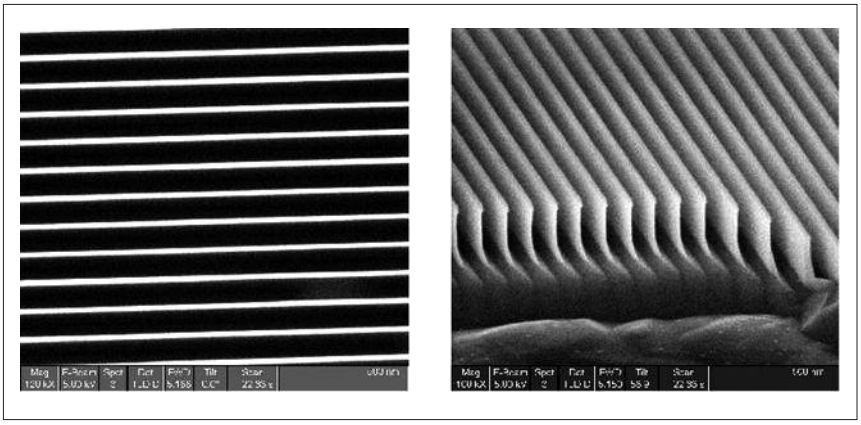


Figure 3. OCD grating section fabricated with SCCDRM technology which exhibits 36-nm lines at 180-nm pitch and having a height of 430 nm. The lithography was performed by collaborating UT-Austin staff using their direct-write e-Beam system.

• demonstrate SEM-deposited hydro-carbon contamination management by the implementation of verifiable contamination-removal procedures,

• improved on-wafer navigation for end-user convenience, and

• improved management of the organic residues that sometimes impair the cosmetic appearance of the reference features and their environment on the wafer and also adversely affect the uncertainty values of the delivered product.

Our strategy takes a page from the roadmap that explicitly states that standards institutions need rapid access to state of the art development and manufacturing capability to fabricate relevant reference materials (ITRS 2005 p. 36 under "Reference Materials.") Likewise, the roadmap states that metrology, process, and standards research institutes, standards organizations, metrology tool suppliers, and the university community should continue to cooperate on standardization and improvement of methods and on production of reference materials (ITRS 2007 p. 2 under "Scope"). One of the products of our prior collaborations is the extraordinary OCD grating section shown in Fig. 3 which exhibits 36 nm lines at 180 nm pitch and having a height of 430 nm. The lithography in this case was done by with MRC's JEOL direct-write e-Beam system at the University of Texas, Austin. Now we have access to the e-beam writer in the NIST Nanofabrication Facility.

DELIVERABLES:

- Design a new mask geometry to accommodate longer etch times to assure that the etchant catches all fast etching planes in sufficient time to produce the theoretical limit to linewidth uniformity as well as to give us better control over the final linewidth - 2Q FY10
- AFM measurement results on a series of linewidth-standard test chips that incorporate all process and handling improvements developed during FY10 - 4Q FY10

Accomplishments

■ We made major improvements to the screening process to establish the optimum of combinations of pattern-transfer factors for driving down reference-feature uncertainties through CD-uniformity enhancement. A major part of the improved screening process was the use of software rather than visual inspection and hand extraction of CD to provide CD-roughness profiles and average CD from SEM images. One benefit of the new screening process is the discovery that sample handling and preparation, including the waiting time between preparation steps, are making a more significant contribution to linewidth non-uniformity than was previously appreciated.

■ Based on the above accomplishment, major changes to the preparation and handling procedures have been introduced and validated. These measures were so successful that we can no longer use the SEM images that we can obtain in the NIST Nanofabrication Facility to optimize the linewidth standard development process, but only to monitor the process for major changes. Instead, we must now rely on AFM measurements by our NIST MEL collaborators.

■ We produced the first batch of chips with grooved-lines following the new preparation and handling procedures. To the first approximation, the grooves and alignment marks worked as planned. For instance, our MEL collaborators told us that their AFM linewidth measurements on the last version of these chips produced in FY09 showed, for the first time, distinctly better linewidth uniformity than what had been typical of the process used to prepare the RM 8111 reference materials. However, the uniformity still does not meet our goal. We have tentatively concluded that the duration of our current silicon etching procedure does not provide sufficient time for the etchant to catch the fast etching

planes as is required to produce the theoretical limit of linewidth uniformity.

■ The project thrust to fabricate reference features on whole wafers has produced first silicon. A hard mask film of 230 nm of silicon nitride was deposited by LPCVD on a selection of (110) wafers. After resist application, three were exposed in the NIST CNST E-beam system, two with a “rosette” pattern to enable identification of <112> vectors in the wafer surface, and one with a sub-100-nm reference-feature pattern. After hard-mask etch and resist strip, the hard-mask pattern was transferred to substrate silicon in a KOH solution to a depth of approximately 250 nm. Optical inspection of the rosette patterns successfully identified the alignment of the lattice <112> direction in the wafer surface to the wafer flats. These directions were readily evident in the two rosette wafers through comparison of the flat-bottom trench width in silicon with the nitride trench widths. This information will ensure correct orientation of the reference-feature patterns relative to the flats on other wafers from the same ingot.

■ As a part of the on-going uncertainty reduction program, the project is developing a new masking process that utilizes localization notches to reduce the position uncertainty of the region of interest in CD reference features, thereby reducing the total linewidth non-uniformity. The process utilizes e-beam lithography, is compatible with monolithic implementation, and targets the extension of the SCCDRM calibration curve down to 20 nm. An electron micrograph of the new SCCDRM hard mask is shown in Fig. 4. The masking process has been implemented on 100 mm bulk wafers and is extensible to 200 mm wafers in both bulk silicon and SOI.

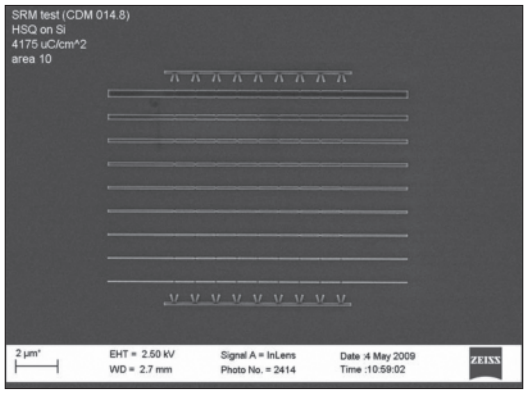


Figure 2. The technical strategy has been to dice each 150 mm (110) wafer after lithography and to mount selected chips in micro-machined standard 200 mm carrier wafers to accommodate the product reference-feature chips.

■ The project published a comprehensive full-length report on the fabrication and calibration of SCCDRM Reference Materials entitled "RM 8111: Development of Prototype Linewidth Standard" in the NIST Journal of Scientific Research. Several other papers on special aspects of the fabrication and calibration, such as test-chip design, AFM metrology, and HRTEM imaging, were presented at the SPIE Spring Symposium of February 2007 and the IEEE International Conference on Microelectronic Test Structures in March 2009. A paper on the subject of etch-process optimization for uncertainty management was presented at the International Electron, Ion, and Photon Beam Technology and Nanofabrication Conference in June 2006. A paper on the comparison of SEM-CD measurements and traceable-AFM CD measurements was published in an IEEE Transactions journal in January 2008. An important first description of fabrication of SCCDRMs on 200 mm bulk wafers which was performed in collaboration with the Scottish Microelectronics Centre was presented at the Frontiers of Characterization and Metrology for Nanoelectronics in March 2007.

Collaborations

The project has been actively collaborating with the Microelectronics Research Center of the University of Texas at Austin (http://www.mrc.utexas.edu/amrc/publications.html) and the Institute for Integrated Micro and Nano Systems at the University of Edinburgh in Scotland (http://www.see.ed.ac.uk/IMNS). These organizations operate the advanced wafer processing tools that we use to address the customer needs referenced in the sections above. Both institutions have highly skilled staff with which we have published recently. In the case of the University of Texas, our collaboration began with using the SCCDRM process to fabricate single-crystal test structures to facilitate a study of electron transport in nickel-silicide features. Since then our collaboration has expanded into the MEMS arena and a ground-breaking study of the impact of nano-structure on the material properties of silicon, principally elasticity and related characteristics. Our interaction with the University of Edinburgh has focused on the fabrication of copper ECD test structures that take advantage of the properties of our SCCDRM technology. In addition, we have jointly published on two types of overlay standard, one of which uses a variant of the SCCDRM process.

We also interact regularly and closely with NIST's Center for Nano Science and Technology, Manufacturing Engineering Laboratory, Physics Laboratory, Materials Science and Engineering Laboratory, and Information Technology Laboratory.

Standards Committee Participation

Standards for Scatterometry Task Force (Michael W. Cresswell).

SEMI International Standards Micro-lithography Committee, member (Richard A. Allen and Michael W. Cresswell).

Publications

B. Li, Z. Luo, P. S. Ho, L. Shi, L. Rabenberg, J. Zhou, R. A. Allen, M. W. Cresswell, *"Controlled Formation and Resistivity Scaling of Nickel Silicide Nanolines"* Nanotechnology, Vol. 20, 7 pp., (25-Feb-2009).

E. Yarimbiyik, H. A. Schafft, R. A. Allen, M. D. Vaudin, M. E. Zaghloul, *"Experimental and Simulation Studies of Resistivity of Nanoscale Copper Films"* Microelectronics Reliability, Vol. 49, pp. 127-134, (19-Feb-2009).

S. Smith, A. Tsiamis, M. McCallum, A. Hourd, J. Stevenson, A. Walton, R. G. Dixson, R. A. Allen, J. E. Potzick, M. W.

Cresswell, N. Orji, "Comparison of Measurement Techniques for Linewidth Metrology on Advanced Photomasks" IEEE Transactions on Semiconductor Manufacturing, Vol. 22, pp. 72-79, (19-Feb-2009).

B. Li, Q. Zhao, H. Huang, Z. Luo, J. Im, M. W. Cresswell, R. A. Allen, M. K. Kang, R. Huang, P. S. Ho, *"Indentation of Single-Crystal Silicon Nanolines: Buckling and Contact Friction at Nanoscale"* Advanced Materials, Vol. 105, No. 7, 7 pp., (08-Apr-2009).

M. W. Cresswell, M. Davidson, G. I. Mijares, R. A. Allen, J. Geist, M. R. Bishop, *"Mapping the Edge-Roughness of Test Structure Features for Nanometer-Level CD Reference-Materials"* Proceedings of the 2009 International Conference on Microelectronic Test Structures, International Conference on Microelectronic Test Structures (ICMTS), Oxnard, CA, United States, 03/30/2009 to 04/02/2009, 6 pp., (02-Apr-2009).

B. J. Shulver, R. A. Allen, A. J. Walton, M. W. Cresswell, J. M. Stevenson, S. Smith, A. S. Bunting, C. Dunare, A. Gundlach, L. I. Haworth, A. W. Ross, and A. J. Snell, IEEE International Conference on Microlectronic Test Structures, March 19-22, 2007, Tokyo, Japan, page 165.

B. J. Shulver, R. A. Allen, A. J. Walton, M. W. Cresswell, J. M. Stevenson, S. Smith, A. S. Bunting, C. Dunare, A. Gundlach, L. I. Haworth, A. W. Ross, and A. J. Snell, IEEE International Conference on Microlectronic Test Structures, March 19-22, 2007, Tokyo, Japan, page 165.

B. J. Shulver, R. A. Allen, A. J. Walton, M. W. Cresswell, J. M. Stevenson, S. Smith, A. S. Bunting, C. Dunare, A. Gundlach, L. I. Haworth, A. W. Ross, and A. J. Snell, IEEE International Conference on Microlectronic Test Structures, March 19-22, 2007, Tokyo, Japan, page 165.

B. J. Shulver, R. A. Allen, A. J. Walton, M. W. Cresswell, J. M. Stevenson, S. Smith, A. S. Bunting, C. Dunare, A. Gundlach, L. I. Haworth, A. W. Ross, and A. J. Snell, IEEE International Conference on Microlectronic Test Structures, March 19-22, 2007, Tokyo, Japan, page 165.

E. Kenyon, M. W. Cresswell, H. Patrick, T. A. Germer, *"Modeling the Effect of Finite Size Gratings on Scatterometry Measurements,"* Proceedings of SPIE Advanced Lithography, SPIE Advanced Lithography, February 24-29, 2008, San Jose, California, 8 pp. (25-FEB-2008).

R. A. Allen, W. F. Guthrie, C. E. Murabito, R. G. Dixson, A. Hunt, *"Comparison of SEM and HRTEM CD Measurements Extracted from Test-Structures Having Feature Linewidths from 40 nm to 240 nm,"* IEEE Trans. Instrum. Meas., Vol. 57, No. 1, pp.100-109 (01-JAN-2008).

B. Li, M. K. Kang, K. Lu, R. Huang, P. S. Ho, R. A. Allen, M. W. Cresswell, *"Fabrication and Characterization of Patterned Single-Crystal Silicon Nanolines,"* NANO Letters, Vol. 8, No. 1, pp.92-98 (07-DEC-2007).

R. A. Allen, R. Dixson, M. W. Cresswell, W. Guthrie, B. J. Shulver, A. S. Bunting, J. T. Stevenson, and A. Walton, *"CD Reference Materials Fabricated on Monolithic 200 mm Wafers for Automated Metrology Tool Applications,"* 2007 International Conference on Frontiers of Characterization and Metrology for Nanoelectronics, Mar 27-29, 2007, Gaithersburg, MD (01-SEP-2007).

R. A. Allen, H. J. Patrick, M. Bishop, T. A. Germer, R. Dixson, W. F. Guthrie, and M. W. Cresswell, *"Study of Test Structures for Use as Reference Materials for Optical Critical Dimension Applications,"* ICMTS IEEE International Conference on Microelectronic Test Structures, April 4-8, 2007, Tokyo, Japan.

B. J. Shulver, A. S. Bunting, A. Gundlach, L. I. Haworth, A. W. Ross, A. J. Smith, A. J. Snell, J. M. Stevenson, A. Walton, M. W. Cresswell, R. A. Allen, *"Extraction of Sheet Resistance and Linewidth from All-Copper ECD Test-Structures Fabricated from Silicon Preforms,"* 2007 International Conference on Microlectronic Test Structures, pp.14-19 (22-MAR-2007).

C. Nwokoye, M. E. Zaghloul, M. W. Cresswell, R. A. Allen, C. E. Murabito, *"A New Critical Dimension Metrology for Chrome-on-Glass Substrates Based ons-Parameter Measurements Extracted from Coplanar Waveguide Test Structures,"* SPIE, Bay Area Chrome Users' Symposium, September 18-22, 2006, Monterey, California, 12 pp. (01-OCT-2006).

M. W. Cresswell, W. Guthrie, R. Dixon, R. A. Allen, C. E. Murabito, J. V. Martinez, *"RM 8111: Development of a Prototype Linewidth Standard,"* Journal of Research (NIST JRES), Vol. 111, No. 3, pp.187-203 (01-MAY-2006).

B. Li, L. Shi, P. S. Ho, J. Zhou, R. A. Allen, M. W. Cresswell, *"Test Structures for Study of Electron Transport in Nickel Silicide Features with Linewidths between 40 nm and 100 nm,"* IEEE ICMTS International Conference on Microelectronic Test Structures, March 06-09, 2006, Austin, Texas, pp.18-23 (01-APR-2006).

B. J. Shulver, A. S. Bunting, A. Gundlach, L. I. Haworth, A. W. Ross, A. J. Snell, J. M. Stevenson, A. J. Walton, R. A. Allen, M. W. Cresswell, *"Design and Fabrication of a Copper Test Structure as a Electrical Critical Dimension Reference,"* Proc., IEEE International Conference on Microelectronic Test Structures, March 06-09, 2006, Austin, Texas, pp.124-129 (01-APR-2006).

JEDEC Standard JESD202, *"Method for Characterizing the Electromigration Failure Time Distribution of Interconnects Under Constant-Current and Temperature Stress,"* March 2006. (Written by H. A. Schafft).

A. E. Yarimbiyik, H. A. Schafft, R. A. Allen, M. E. Zaghloul, and D. L. Blackburn, *"Implementation of Simulation Program for Modeling the Effective Resistivity of Nanometer Scale Film and Line Interconnects,"* NISTIR 7234, February, 2006.

Wafer-Level Overlay and Patterned Defect Metrology

Technical Contacts:
R. Silver

Goals

Provide technological leadership to semiconductor and equipment manufacturers, and other government agencies by developing and evaluating the methods, tools, and artifacts needed to apply optical techniques to the metrology needs of semiconductor microlithography. One specific goal is to provide the customer with the techniques and standards needed to make traceable dimensional measurements on wafers at the customer's facility. The industry focus areas of this project are optical based methods used in overlay metrology, wafer level patterned defect inspection, and critical-dimension (CD) metrology.

Customer Needs

Tighter tolerances on CD measurements in wafer production place increasing demands on linewidth accuracy and on overlay tolerances. A recent industry focus on high-throughput, higher-resolution metrology tools, which enable more dense sampling strategies has led to a comprehensive program at NIST to both support and advance the optical techniques needed to make these high throughput overlay and critical dimension wafer measurements as well as patterned defect inspection measurements (see Fig. 1).

Technical Strategy

The main technical thrust areas are overlay calibration techniques and standards, new advanced wafer level hardware and target designs, and research into advanced methods for patterned defect inspection. The strategic components of the project follow.

1. The development of calibration methods and calibrated overlay structures is one of the primary goals of the project. The technical strategy for calibrated overlay metrology is divided into two components: (a) instrumentation development and development of advanced overlay metrology calibration techniques, and (b) the design and calibration of test patterns and standard artifacts. NIST has developed an overlay metrology tool that has undergone extensive development of the mechanical hardware, optical components, and measurement algorithms to obtain uncertainties comparable to or better than the best industry overlay tools. This optical metrology tool is used to calibrate standards and to support the development of improved measurement algorithms and alignment techniques. Since pattern placement and overlay of the various lithographic levels is monitored with a series of targets, each in a different plane, particular concern is placed on ensuring accurate optical measurements through a large depth of

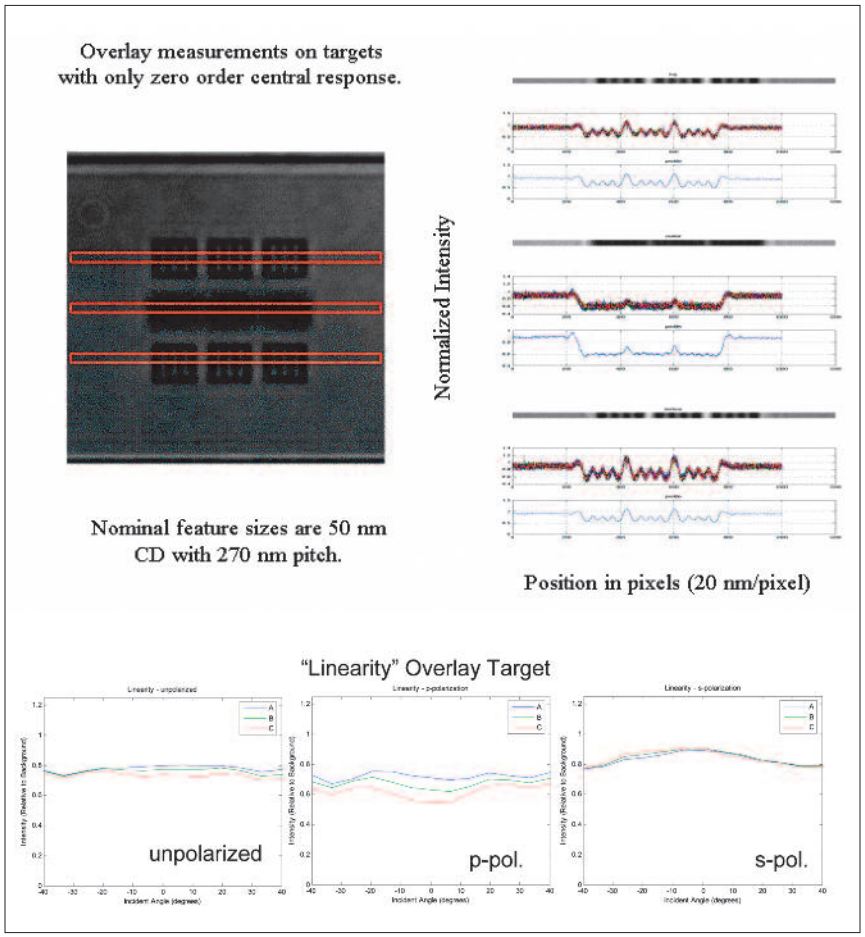


Figure 1. Improved two-dimensional overlay measurement techniques and standards are needed for measuring and controlling overlay capabilities of steppers and separating out the contributions from the photomask. Overlay is listed in multiple sections of Tables Met 3a and b of the 2007 ITRS as a difficult challenge for both >32 nm and <32 nm processes. Overlay measurements have not kept pace with resolution improvements and in-die correlation requirements and will be inadequate for ground rules less than 45 nm. In fact, Table Met 3a shows that no known solutions for overlay output metrology exist beyond the 65 nm node. As shown in Table Met 3b, the problems are more acute for long term CD metrology where the industry is currently encountering metrology problems without known manufacturing solutions.

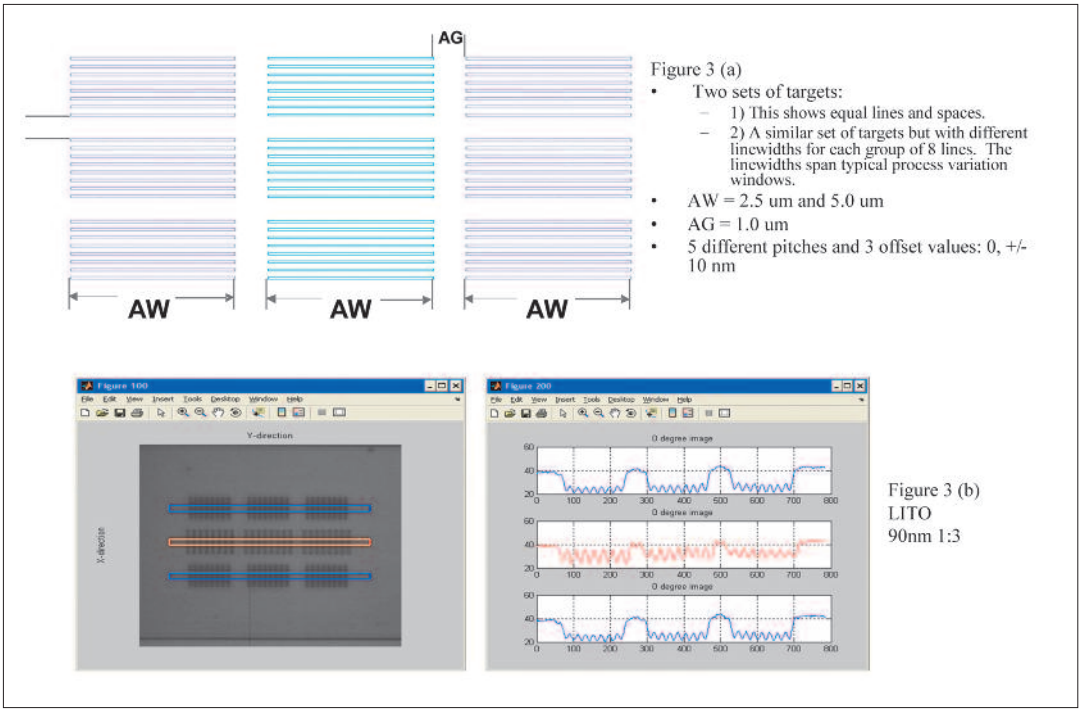


Figure2. A schematic of the target designs is shown in (a). This is one example of several variations of this design. The lower part of the figure shows an image and a set of profiles for a target which reflects higher-order optical content.

focus. Any misalignment in the overlay metrology system will translate into an overlay offset error, referred to as tool induced shift (TIS). Additionally, there are residual errors caused by asymmetries in the targets known as wafer induced shift (WIS). A set of standard artifacts and alignment procedures, developed at NIST and published, has been implemented to assist in aligning overlay measurement systems and minimizing TIS. After alignment, the tool must then be calibrated with standard artifacts to yield accurate overlay measurements. The NIST metrology system used for this is an optical reflection mode instrument, typically operated in a bright field mode. The hardware includes high-resolution image capture with a full field CCD data acquisition system, which has been fully characterized and calibrated. This instrument has been used for detailed analysis of CCD array performance and characterization and several CCD acquisition systems have been evaluated. Many of the techniques developed in the advanced optical imaging section below have been implemented on this tool as well, such as structured illumination and system characterization to enable improved calibrations.

Standard overlay artifacts have been fabricated and calibrated in 200 mm and 300 mm wafers that are now available as SRM 5000. These overlay artifacts are for the calibration of industrial overlay metrology tools, although they have also been used for the calibration of atomic force microscope (AFM) or SEM reference metrology systems. The artifacts have been fabricated in single crystal silicon and provide an array of etched silicon three-dimensional targets. These wafers additionally have an extensive set of characterization targets and research structures developed in close collaboration with SEMATECH and leading semiconductor manufacturers, for an example, Fig. 2. We have also developed a series of new overlay targets and linewidth targets intended to enable the measurement of overlay and linewidth with device-size features. One variation of these targets allows in-chip structures to be placed throughout the active area of a die. These results have been published and collaborative work is progressing to develop the commercial applications to measure overlay using device-size features in targets optimized to be the smallest overall dimension. There is a second flavor of in-chip targets, as shown in Fig. 3, that are arrayed targets composed of device-sized features

DELIVERABLES:

- Complete a comprehensive set of measurements with uncertainties comparable to the best available using new target designs as fabricated on the AMAG 5L reticle. Work with Sematech to evaluate the new target performance and optimize target solutions. 4Q 2010
- Utilize the scanned aperture capability on the overlay microscope to Improve tool alignment and normalization procedures. Use the two-dimensional scanning aperture capability with computer positioning control and auto data acquisition for engineered illumination overlay measurements. 4Q 2010
- Evaluate a range of next generation of overlay target designs for use as wafer standards. Work with industry and Sematech to evaluate the different design considerations and build a consensus for the next generation of calibrated overlay standards. 3Q 2010
- Compare measurement results jointly with SEMATECH for dense structure overlay in comparison to conventional edge based patterns. Evaluate target designs using arrayed overlay targets and use measurements to ascertain across field error contributions in overlay metrology. Q2 2011

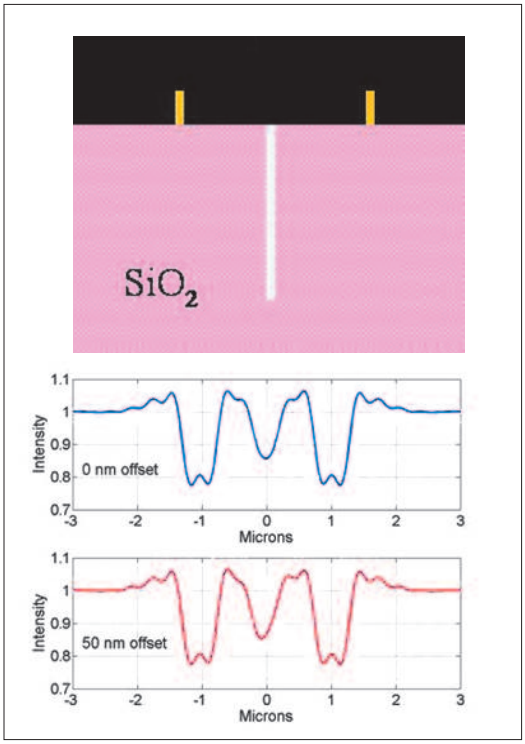


Figure 3. New overlay targets, which occupy less than 2 μm x 2 μm in total space. This is designed to be an in chip target.

Optical modeling is an essential tool for enabling improved optical overlay measurements. Modeling the effects of relevant feature properties and optical instrument characteristics using existing and new software tools, can yield significant improvements in measurement accuracy, as in Fig. 4. NIST has a world class effort in optical modeling that includes the comprehensive comparison of a rigorous coupled wave guide scattering model, a finite difference time domain-based model, a finite element solver and a Maxwell integral equation solver. Three of the models were developed in house and form the basis of our critical dimension, overlay, and patterned defect simulation tools.

DELIVERABLES:

- Compare standard simulations for using 3 different models for three-dimensional structures based on 32 nm node lithography design rules. Use results to identify any simulation errors and to develop improved accuracy for the implementation of three-dimensional scattering model. 3Q 2010
- Use simulation to investigate scatterfield techniques applied to defect inspection. Use three-dimensional modeling techniques to accurately simulate patterned defect inspection using high NA microscopy and coherent imaging methods on alternative optical platforms. 1Q 2011

2. The second component of this project is the development of new, advanced high-resolution optical metrology techniques. A new class of optical measurement techniques known as scatterfield microscopy is being developed at NIST. This optical methodology has been used to demonstrate line width and overlay metrology with targets composed of features smaller than 30 nm critical dimensions. This new approach utilizes structured illumination in parallel with engineered target designs. This technique also includes through focus methods that ac-

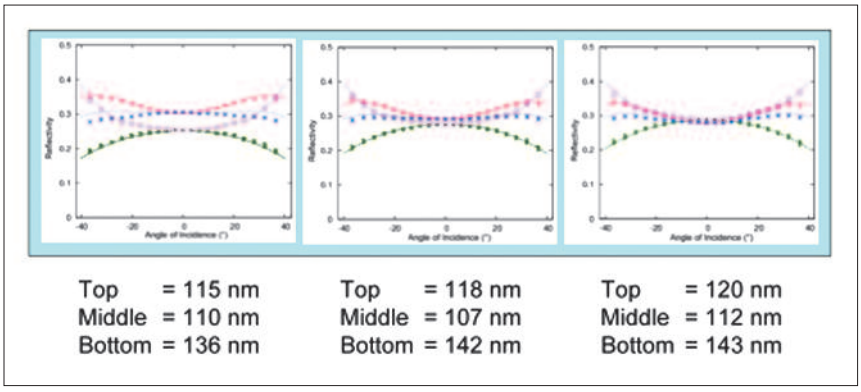


Figure 4. Quantitative parametric modeling results demonstrate consistent agreement on the nanometer scale with AFM reference metrology. More comprehensive data published recently show that nanometer scale sensitivity measurements can be achieved using angle resolved microscopy for nominally 100 nm sized lines and pitches of 300 nm.angle resolved microscopy for nominally 100 nm sized lines and pitches of 300 nm.

quire optical image data from different focal planes. These techniques are well suited for high-resolution microscopy of metrology targets as encountered in semiconductor manufacturing.

A key element of this approach is to develop optical methods that can be suitably applied to device-sized features and advance the extensibility of high throughput optical metrology methods. Current metrology requirements are demanding higher throughput, non-destructive measurements with nanometer sensitivity to enable tighter process control as well as closed-loop integrated process control. The current class of scatterometry and scatterfield optical techniques are now being implemented as solutions to these significant metrology challenges. As a part of this project, we have constructed an optical tool specifically intended to make scatterfield measurements with structured illumination by controlling the frequency content of the illumination fields and of the scattered fields. Fig. 5 shows an example of controlling the frequency content of a sub-resolution overlay target. This effort includes comprehensive optics modeling as well as a new 193 nm optical microscope designed and fabricated in-house.

We have constructed a 193 nm wavelength optical instrument with a flexible architecture for overlay, CD, and patterned defect measurements on a high throughput capable platform. The new design creates a large conjugate back focal plane where a range of scanning and illumination control techniques can be applied. The optics have been custom designed and manufactured to NIST specifications with the appropriate 193 nm coatings. The new laser system and optics are housed in a clean room environment and use a new embedded structural design with superb vibration and temperature control. The goal is ultimate performance in a state of the art short wavelength optical system.

The 193 nm optical tool is now being used extensively to investigate short wavelength optical inspection of patterned defects. This instrument provides significantly higher imaging resolution and simulations show substantial gains in defect detection can be achieved using shorter wavelength imaging. A complete set of pattern-defect analysis algorithms has been developed and extensive collaborations with industry leaders and Sematech have enabled this effort to have a direct impact on the semiconductor industry. State of the art intentional defect arrays provided by Sematech are used to test alternative optical design configurations resulting In improved defect detection.

DELIVERABLES:

- Use the 193 nm optical tool with improved alignment to complete extensive patterned defect inspection evaluation using industry provided wafers. Quantify the gains using different illumination configurations and evaluate both angle-resolved and polarization-resolved defect detection. 3Q 2010
- Complete a comprehensive set of modeling runs to evaluate 193 nm high resolution imaging gains based on 193 nm tool performance. Initiate experimental optical data comparisons with detailed scattering simulations. 4Q 2010
- Model and evaluate the new super-target overlay designs in collaboration with SEMATECH and fabricate test wafers for use by the industry and test target performance. Evaluate similar methods and dense targets for overlay metrology in double patterning. 4Q 2010
- Vertical and horizontal proximity studies have received recent attention as they have uncovered key attributes of scatterometry for overlay complications. These data were reported to Sematech in the investigation of advanced optical overlay metrology using scatterometry and scatterfield techniques. 2Q 2010

3. A final element of this project is development of hybrid electrical-optical test structures to provide a validation between in-line optical metrology and actual device performance. These test structures would not displace in-line metrology, but rather will compliment it; providing a tool to evaluate in-line techniques.

DELIVERABLES:

- Complete initial evaluation of test structure using electrical and AFM metrology. 3Q 2010
- Investigate intercomparison of electrical metrology with optical metrology. 4Q 2010

Accomplishments

■ 193 nm optical tool fully operational. Following design and construction of mechanical and custom optical components the new 193 nm optical metrology tool is now used routinely for high resolution imaging. Extensive alignment and normalization techniques have been implemented.

■ Plenary paper for the SPIE Metrology Inspection and Process Control conference titled: Angle-resolved Optical Metrology using Multi-

Technique Nested Uncertainties. This was the result of extensive interest in the new multi-technique approach to metrology. The paper focused on new quantitative scatterfield measurements and techniques using multi-technique nested uncertainties.

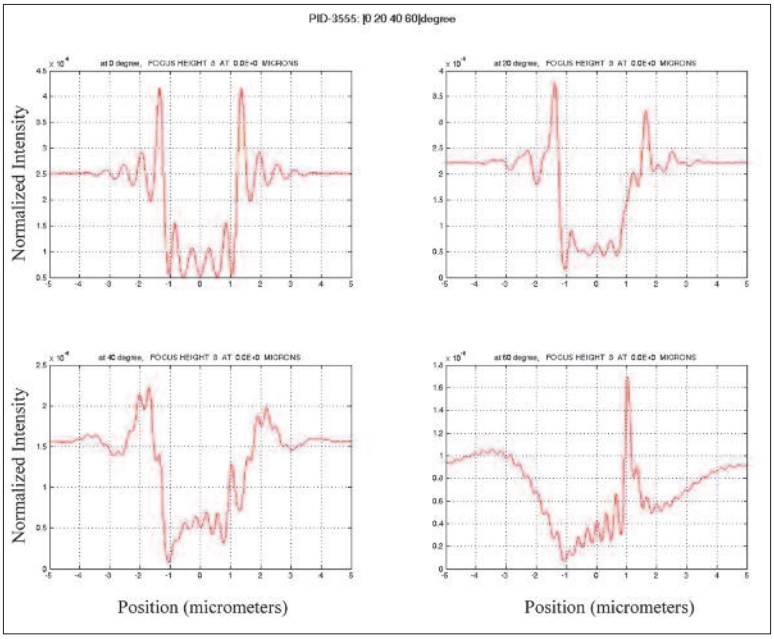


Figure 5. The different panels show the image as a function of illumination angle. The vertical axes are normalized intensity and the horizontal axes are lateral position in micrometers. At the high illumination angles, the higher order diffraction orders are rocked into the collection optics. A dipole or alternative illumination can yield symmetric profiles or overlay which otherwise would show zero order response.

■ Book chapter authored on EUV Metrology. This is a new book published by McGraw Hill and is expected to be the benchmark publication for semiconductor manufacturing challenges using next generation EUV lithography.

■ There have been several external inquiries and interactions from the new method for nesting multiple measurements. This method can improve reference metrology and independent measurements through the use of Bayesian statistical methods that combine measurements into a monolithic measurement that results in a lower uncertainty than the individual measurements.

■ Patent Applied for on "Super resolution overlay targets". Joint NIST/SEMATECH patent has been formally applied for on the new super-resolution overlay target, which has the potential to change the target designs and methodology widely used by the industry.

■ Keynote presentation titled "Improving Optical Measurement Accuracy using Multi-technique Nested Uncertainty" given at an invitation only group of international experts at the 2009 Lithography workshop in Coeur d'Alene, Idaho.

■ Served as Technical Chair for the 2009 International Conference on Microelectronic Test Structures. This conference, in its 23rd year, is the premier conference for electrical test structures for semiconductor applications.

■ A new level of quantitative agreement has been achieved between rigorous modeling and experimental data. Published results demonstrating quantitative agreement for scatterfield measurements of densely arrayed 40 nm CDs and 100 nm sized lines which vary in 1 nm increments. This new level of agreement was achieved using parametric modeling methods and uncertainty analysis at the nanometer scale. This was accomplished by accurate optical characterization/normalization without tunable parameters.

■ Comprehensive development and comparison of NIST electromagnetic scattering models and industry models completed. Researchers in the optical scatterfield competence have both developed and compared model-based simulation results with excellent agreement. Two industrial scattering models as well as the NIST-developed integral Maxwell equation solver and the NIST-developed Rigorous Coupled Wave Analysis (RCWA) model were all compared.

■ The NIST optical metrology project awarded second SEMATECH funded effort to perform an investigation to the fundamental limits of defect inspection techniques using the scatterfield optical microscopy platform and methodology.

■ The through-focus focus-metric technique was advanced using a new differential imaging methodology that demonstrated nanometer sensitivity to features in silicon. The technique of sampling scattered fields through focus for CD measurement and optical system alignment has been implemented at other international metrology laboratories. Applications in overlay and CD metrology are being investigated.

■ The overlay microscope has been converted to scatterfield scanning design. The existing optical overlay instrument has been enhanced with illumination control for improved data acquisition and tool alignment. Techniques for alignment and imaging implemented.

■ The 450 nm illumination scatterfield microscope has been outfitted with a spectroscopic illumination and scanning capability. This is a new scatterfield application developed at NIST specifically for the purpose of using engineered illumination and wavelength scanning. The open architecture microscope allows sophisticated control of the illumination and collection paths.

■ Fuel Cell research funding landed for high throughput scatterfield microscopy of membrane electrode assembly results. This research is directly the result of applying metrology methods developed for the semiconductor industry to challenges in fuel cell fabrication for the energy sector. These nanometrology results demonstrated sensitivity to critical MES manufacturing parameters.

■ Organized a well-attended panel discussion on "Is the end of CMOS is near? Nanotechnology alternatives to CMOS scaling" at this years SPIE Advanced Lithography conference.

■ Authored an invited paper for Laser Focus World titled “Scatterfield optical imaging enables sub-10 nm dimensional metrology”. The paper received an award for “excellence in communications”.

■ Report submitted to SEMATECH for 2010 funding on defect metrology applications of scatterfield microscopy. Scatterfield optics researchers gave a mid-review on the completed comprehensive simulations to investigate applications of scatterfield microscopy to patterned defect inspection. The project has subsequently received substantial funding from other industry leaders for patterned defect detection advancements.

Collaborations

SEMATECH, IBM, Intel, KLA-Tencor, Nanometrics, Applied Materials, Motorola, AMD, and several other leading manufacturers and tool vendors.

University of Edinburgh.

Publications

R. M. Silver, B. M. Barnes, Y. Sohn, R. Quintanilhaa, H. Zhou, C. Deeb, M. Johnson, M. Goodwin, and D. Patel, *“ The Limits and Extensibility of Optical Patterned Defect Inspection,”* Proc. of SPIE Vol. 7638 76380J-1, 2010.

R. M. Silver, *“Scatterfield optical imaging enables sub-10 nm dimensional metrology,”* Laser Focus World, Vol. 45, No 1, January 2009.

Y.J. Sohn, R. Quintanilha, B.M. Barnes, and R.M. Silver, *“193 nm angle-resolved scatterfield microscope for semiconductor metrology,”* Proceedings of SPIE, San Diego, CA, USA: 2009, pp. 74050R-74050R-8.

R.M. Silver, B.M. Barnes, N.F. Zhang and H. Zhou, *“Angle-resolved Optical. Metrology using Multi-technique Nested Uncertianties,”* SPIE Newsroom, 2009

R. Quintanilha, Y. Sohn, B.M. Barnes, L. Howard, and R. Silver, *“Critical dimension measurements using a 193 nm scatterfield microscope,”* Modeling Aspects in Optical Metrology II, Munich, Germany: SPIE, 2009, pp. 73900S-12.

R.M. Silver, B.M. Barnes, H. Zhou, N.F. Zhang, and R. Dixson, *“Angle-resolved optical metrology using multi-technique nested uncertainties,”* Modeling Aspects in Optical Metrology II, Munich, Germany: SPIE, 2009, pp. 73900P-12.

Ravikiran Attota, Thomas A. Germer, and Richard M. Silver, *"Nanoscale measurements with a through-focus scanning optical microscope,"* Future Fab, 30, pp 83-88, (2009).

R.M. Silver, N. Zhang, B. Barnes, H. Zhou N. Heckert R. Dixson, T. Germer, and B. Bunday, *“Improving Optical Measurement Accuracy using Multi Technique Nested Uncertainties,”* SPIE Vol. 7272, p. 1, 2009.

R.M. Silver, H. Zhou, B. Barnes, and R. Attota, *“Three-dimensional OCD Study to Evaluate: The Effects of LER on CD and Contact Hole Measurement Feasibility,”* Sematech Tech Trans. Doc. 08064937A-TR, June 2008.

R. Attota, M. Stocker, R. M. Silver, and A. Heckert, *"Through focus scanning and scatterfield optical methods for advanced overlay analysis,"* SPIE Vol 7272, p. 14 (2009).

B. Barnes, N. Heckert, R. Quintanilha, H. Zhou, and R. M. Silver, Spectroscopic Scatterfield Microscopy, Proc. SPIE Frontiers Conf. Abany NY, 2009.

R. Attota, T. Germer, and R. M. Silver, Through Focus scanning optical microscope imaging method for nanoscale dimensional analysis, Optics Letters 33 (17) p. 1990-1992 (2008).

R. M. Silver, B. Barnes, R. Attota, A. Heckert, and R. Dixson, *"Angle Resolved Optical Metrology,"* Proc. SPIE Advanced Lith., Feb. 2008.

R. M. Silver and A. Vladar, *"EUV Metrology"*, EUV Lithography, (Chapter 6) McGraw Hill, 2009 (in press)

R. Attota, R. M. Silver, and B. Barnes, *"Optical Through Focus Technique that Differentiates Small Changes in Line width, Line Height and Sidewall Angle for CD, Overlay and Defect Metrology Applications",* Proc. SPIE, Vol. 6922 p. 0E (2008).

R. Attota, R. M. Silver, and R. Dixson, *"Linewidth Measurement Technique using Through-focus Optical Images,"* Applied Optics, Vol. 47, pp. 495-503 (2008).

R. M. Silver, B. Barnes, R. Attota, J. Jun, M. Stocker, E. Marx, and H. Patrick, *"Scatterfield Microscopy to Extend the Limits of Image-based Optical Metrology,"* Applied Optics, Vol. 46, 20, pp. 4248-4257 (July 2007).

H. Patrick, R. Attota, B. Barnes, T. Germer, R.G. Dixson, M. Stocker, R. M. Silver, and M. Bishop, *"Optical Critical Dimension Measurement of Silicon Grating Targets using Back Focal Plane Scatterfield Microscopy,*" accepted, J Micor/Nanolith., MEMS and MOEMS 7(1), 013012, 2008.

E. Marx, *"Images of Strips on and Treches in Substrates,"* Applied Optics 46, pp. 5571-5587 (2007).

B. M. Barnes, R. Attota, B. Bunday, L.P. Howard, P. Lipscomb, M.T. Stocker, and R. Silver, *"Zero-Order and Super-Resolved Imaging of Arrayed Nanoscale Lines using Scatterfield Microscopy,"* 2007 Int'l Conf on Frontiers of Characterization and Metrology for Nanoelectronics, AIP (2007).

R. M. Silver, R. Attota, and E. Marx, *"Model-based Analysis of the Limits of Optical Metrology with Experimental Comparisons,"* Proc. SPIE Germany, Vol. 6617, p. 6617OW, June 2007.

B. J. R. Shulver, R. A. Allen, A. J. Walton, M. W. Cresswell, J. T. M. Stevenson, S. Smith, A. S. Bunting, C. Dunare, A. M. Gundlach, L. I. Haworth, A. W. S. Ross, A. J. Snell, *"Array Based Test Structure for Optical-Electrical Overlay Calibration,"* Microelectronic Test Structures, 2007, ICMTS'07, IEEE International Conference, pp. 165-170 (March 2007).

R. M. Silver R. Attota, B. Barnes, and H. Zhou, *"Theoretical Evaluation of Scatterometry for Overlay Applications,"* SEMATECH Tech Transfer Doc, Feb. (2007).

R. M. Silver, T. Germer, R. Attota, B. Barnes, B. Bunday, J. Allgair, E. Marx, and J. Jun, *"Fundamental Limits Optical Critical Dimension Metrology: A Simulation Study,"* SPIE Proc. Feb. Vol. 6518 (2007).

Front-End Processing Metrology Program

The dimensions of the active transistor areas are approaching the spacing between dopant atoms, the stochastic regime, complicating both modeling and doping gradient measurements. Thin dielectric and conducting films are approaching monolayer thicknesses.

As device dimensions continue to shrink, junctions and critical film thicknesses approach the realm of several atoms thick, challenging gradient, thickness and wafer flatness and roughness metrology as well as electrical and reliability characteristics. The current gate stacks, poly silicon over SiO_2 and SiON dielectrics, are being replaced by high-κ metal gate stacks. The overall task is to provide starting wafer dimensional and defect metrology, suitable metrology and reference materials for their dielectrics and junctions, including electrical characterization, gradient, thickness and roughness metrology, and overall reliability metrology.

Modeling, Measurements, and Standards for Wafer Inspection

This is a large project that involves parts that are not reasonably combined in a single document. For this reason, the project is presented in tow sub-sections, each focusing on a single aspect. These are:

- Modeling and Measurements for Wafer Inspection
- Nanoparticle Size Characterization and Standards Development

Modeling and Measurements for Wafer Surface Inspection

Technical Contacts:
T. A. Germer

"The work done by SEMI's Auromatic Surface Inspection Task Force on particle scanner calibration would have been impossible without the support supplied by Dr. Thom Germer of NIST. He used his scatter modeling software and knowledge of the situation to make possible a rewrite of SEMI M53 that dramatically improved it capabilities.""

John Stover
Co-Leader of the SEMI ASI Task Force
The Scatterworks, Inc.

Goals

Our goals are: (1) to provide industry with models, measurements, and standards for particles and other defects in order to improve the inspection of wafer surfaces; (2) to develop facilities to accurately measure particle size and to deposit monosize particles on calibration artifacts to reduce the uncertainty in the sizes of particles used by the semiconductor industry to calibrate scanning surface inspection systems (SSIS); and (3) investigate theoretically and experimentally the behavior of light scattering from particles, defects, and roughness on wafer surfaces.

Customer Needs

The Semiconductor Industry Association's (SIA) International Technology Roadmap for Semiconductors identifies the detection and characterization of defects and particles on wafers to be a potentially show-stopping barrier to device miniaturization. The roadmap specifies polystyrene latex (PSL) equivalent diameter particles that must be detectable on bare silicon, non-metallic films, metallic films, and wafer backsides each year. Currently, no solutions to this inspection problem currently exist for particles on bare silicon, on non-metallic films, and on wafer backsides, while it is anticipated that no acceptable solutions will exist for metallic films in 2010. While the detection sensitivity for defects must be increased, the ability to characterize defects in terms of size, shape, composition, etc., is critical for yield-learning. Defects must be characterized independent of defect location and topology.

With the need to detect smaller defects, the costs of inspecting wafers are skyrocketing. In order for new advances to be implemented in production environments, improvements in sensitivity must be achieved without suffering a tradeoff in throughput and must be cost-effective. The drive towards in-situ sensors for production tools requires techniques which can be effectively miniaturized.

In order that wafer manufacturers and device manufacturers have a common basis for comparing specifications of particle contamination, improved standards for particles are needed.

A recent comparison of the measurements of calibration wafers by 13 different Scanning Surface Inspection System (SSIS) indicated unacceptably large deviation between the SSIS results and the actual particle sizes. This study involved six particle sizes ranging from 88 nm to 290 nm and included the NIST SRM 1963 and two other particles sizes measured by NIST. For the two smallest particle sizes, 88 nm and 100.7 nm, the scanners systematically underestimated the size by about 8 %.

Technical Strategy

There are two major strategies for improving the performance of scanning surface inspection systems. One strategy is to develop a fundamental understanding of optical scattering at surfaces so that tool manufacturers can optimize the performance of their instrumentation, in terms of defect detection limits and discrimination capabilities, to characterize the response of instrumentation to different types of defects, and to develop and calibrate particles of well-defined size and material. Recent work by this group has demonstrated that the polarization of light scattered by particulate contaminants, subsurface defects, and microroughness has a unique signature that can be using to identify the source of scatter. In particular, it was found that small amounts of roughness do not depolarize scattered light. This finding has enabled the development of instrumentation which can collect light over most of the scattering hemisphere, while being blind to microroughness. That instrumentation, for which a patent has been awarded, should result in a factor of two improvement in minimum detectable defect size, especially on rougher surfaces.

A second strategy is to provide leadership in the development of low uncertainty calibration particles for use in calibrating surface scanners. A major focus has been development of the differential mobility analysis (DMA) method for accurately sizing monosize polystyrene spheres. This work together with a SSIS round robin has provided evidence that current SSIS measurements have an unacceptably large uncertainty for particle sizes in the 90 nm to 100 nm size range. The technical focus of our future work will be

Figure 1. The Goniometric Optical Scatter Instrument is a state-of-the-art laser scattering facility.

applying DMA for accurately sizing calibration particle sizes as small as 30 nm, developing methods for generating other types of monosize particles, and developing laser surface scattering methods for quantitative particle sizing.

Specific project elements are defined below:

1. Polarized Light Scattering Measurements – The Goniometric Optical Scatter Instrument (GOSI) enables accurate measurements of the intensity and polarization of scattered light with a wide dynamic range, high angular accuracy, and multiple incident wavelengths (visible and UV) on 300 mm wafers (see Fig. 1). We measure the light scattering properties of well-characterized samples exhibiting interfacial roughness, deposited particles, subsurface defects, dielectric layers, or patterns. The emphasis is on providing accurate data, which can be used to guide the development of light scattering instruments, and to test theoretical models.

2. Theoretical Light Scattering Calculations – Theoretical Light Scattering Calculations – The focus of our theoretical work is on: (a) developing models that accurately predict the polarization and intensity of scattered light, and (b) determining what information can be efficiently and accurately extracted from light scattering measurements. Approximate theories are used in conjunction with more complex techniques to gain an understanding of which parameters affect the light scattering process. Particular cases that are being analyzed include: (a) scattering by defects and roughness associated with dielectric layers, (b) scattering by particulate contamination on bare and oxidized wafers, and (c) scattering by periodic structures.

DELIVERABLES:

- Develop model for scattering by spherical particles embedded in a layer. 2Q 2011

3. Size Distribution Measurements – Differential mobility analysis (DMA) has been shown to be capable of making accurate size measurements for mean particle diameters as small as 50 nm. However, discrepancies have been noticed between PSL measurements using DMA, and measurements using light scattering on the surface of a wafer. These discrepancies are possibly due to the PSL particles deforming on the bottom as they adhere to the wafer. This problem will be investigated by comparing measurements of the PSL particles to measurements of silica particles, which are less likely to deform when they contact the wafer surface. Measurements will be performed using both the DMA and light-scattering instruments.

4. Resource on Particle Science – Over the past five years, the particle-related work has included projects with SEMATECH and particle suppliers to the semiconductor industry. A number of needs by particle related companies were expressed at a NIST particle workshop including redoing the uncertainty assessments of existing particle SRMs and offering a particle sizing calibration service. Providing support for particle needs critical to the semiconductor industry will continue to be a priority.

DELIVERABLES:

- Provide technical support to the SEMI Advanced Surface Inspection task force. 4Q 2010

Accomplishments

■ Completed and certified the measurements for new NIST Standard Reference Materials (SRM). Measured and certified SRM 1964, particles with a nominal diameter of 60 nm. Also measured and certified SRM 1963a, with a nominal diameter of 100 nm, to replace the previous 100 nm SRM 1963, which was corrupted due to agglomeration. SRM 1963a and SRM 1964 are currently available for purchase.

■ Completed initial screening process and preliminary measurements for development of a 30 nm SRM. Identified primary and secondary candidate samples for the 30 nm SRM, based on diameter and distribution measurements. Researched measurement uncertainty for particles smaller than 50 nm and devised strategies for reducing the uncertainty.

■ Developed and improved the NIST Calibration Facility, which uses Differential Mobility Analysis for sizing monodisperse spheres in the size range of 50 nm to 400 nm. Reduced the expanded uncertainty to 1.0 % of the particle size by correlating the slip correction to the measured particle size. Increased resolution and accuracy of measurements through improved equipment and intermediate measurements.

■ Determined that the electrospray technique can produce an aerosol having characteristics optimal for transferring particles in a liquid suspension onto wafers for particle diameters as small as 25 nm. This significant finding enables improved wafer depositions by reducing the number of contaminant residue particles, the number of doublets, and the amount of residue on the particles.

■ Coordinated the experimental design and uncertainty analysis with the University of Minnesota for the first measurement of slip correction of particles smaller than 300 nm. These measurements are critical to improving the accuracy of particle size by the DMA in the nanometer size range.

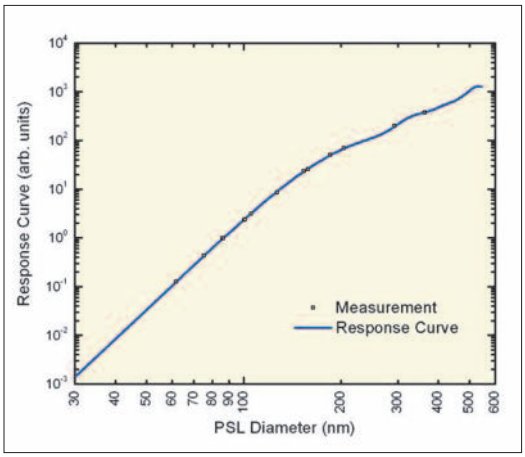
■ In collaboration with the University of Maryland, developed a method for generating pure copper spheres with diameters ranging from 100 nm to 200 nm. These spheres, which mimic real-world particles better than polystyrene, were used to validate particle scattering theories in conditions for which models have a higher degree of uncertainty. Measured polarization and intensity of light scattered from the copper spheres and found good agreement with the Bobbert-Vlieger theory for light scattering from a sphere above a surface.

■ Developed a method, based upon scattering ellipsometry, for quantifying scatter from two sources and demonstrated its use by characterizing the roughness of both interfaces of an SiO2/silicon system. This finding establishes the validity of the light scattering models for roughness in a dielectric film, which in turn limits the detection sensitivity of SSIS instruments. The method was also used to characterize scattering from steel surfaces, demonstrating capability to distinguish between scattering from surface roughness and material inhomogeneity. The method was further used to study the scatter from an anti-conformal polymer film, helping to establish the limits of validity of the scattering theory.

■ Developed the SCATMECH library of C++ routines for light scattering. Published the SCATMECH library, providing a means for distributing scattering models and polarized light calculations to others. From the time of its public availability in March 2000, over 6000 copies of the library have been downloaded from the web. The Modeled Integrated Scatter Tool (MIST), a Windows application for calculating integrated scatter, was released in June 2004.

■ Extended the theory of scattering of a sphere on a surface to axially-symmetric non-spherical particles. Demonstrated that the scattering by a metal particle on a surface is extremely sensitive to the shape of the particle in the region where the particle contacts the surface. This unusual sensitivity to shape must be considered when light scattering tools classify particles for material and size.

■ Performed a light-scattering-based diameter measurement of the NIST 100 nm PSL sphere standard (SRM 1963) deposited onto a silicon



Sample calibration of a commercial wafer scanner using the new SEMI M53 method. The relative expanded uncertainty in particle diameter has been reduced to less than 1 %.

wafer. The measurement results included a thorough assessment of the uncertainties that arise in such measurements. It was found that the uncertainty was dominated by the uncertainty in the shape of the particle on the surface. Results for smaller PSL particles suggest that surface-induced deformation of the particles must be considered.

■ Assisted in revising SEMI M53, a practice for calibrating scanning surface inspection systems, by developing a model-based calibration scheme that matches measured signals from PSL spheres to the predictions of a theoretical model. The accepted model for scattering by the spheres is specified in the standard as that provided by the MIST program. The new method has several advantages over the previous method, including: less sensitivity to changes in availability of specific size standards, improved accuracy, less variability between instruments, and an ability to extract a quantitative accuracy from the calibration. The expanded uncertainty found by applying the calibration to a commercial instrument was better than 1 % of the diameter. (See Fig. 2)

■ Tested the use of silica spheres as a substitute for PSL spheres for calibrating scanning surface inspection systems. PSL spheres exhibit degradation upon repeated ultraviolet exposure, and more inspection tools are using ultraviolet wavelengths. The silica spheres were found to yield comparable calibrations, provided that they are classified with a PSL-sphere-calibrated classifier to reduce their size distribution. The index of refraction of the silica spheres was a byproduct of the measurements and are needed for the calibration.

Collaborations

Hitachi High Technology Corporation, Japan, Akira Hamamatsu, Light Scattering from Rough Surfaces.

Department of Mechanical Engineering, University of Minnesota, Professor David Pui, Generation and Measurement of Nanosize Particles.

National Metrology Institute of Japan, Dr. Kensei Ehara, Nanoparticle Metrology.

Publications

T. A. Germer, C. Wolters, and D. Brayton, *"Calibration of wafer surface inspection systems using spherical silica particles,"* Optics Express 16 (7), 4698–4705 (2008).

T. A. Germer, *"Modeling the effect of line profile variation on optical critical dimension metrology,"* in Metrology, Inspection, and Process Control for Microlithography XXI, Proc. SPIE 6518, 65180Z (2007).

T. A. Germer, *"Effect of line and trench profile variation on specular and diffuse reflectance from a periodic structure,"* J. Opt. Soc. Am. A 24 (3), 696–701 (2007).

Thomas A. Germer, *"Measuring Interfacial Roughness by Polarized Optical Scattering,"* in Light Scattering and Nanoscale Light Scattering, A.A. Maradudin, Ed., (Elsevier, New York, 2007) Chapter 10, pp. 259–284.

M. K. Donnelly, J. C. Yang, *"Screening Candidates for 30 nm Spheres,"* NISTIR 7345, August 2006.

G. W.Mulholland, M. K. Donnelly, C. Hagwood, S. R. Kukuck, and V. A. Hackley, *"Measurement of 100 nm and 60 nm Particle Standards by Differential Mobility Analysis,"* J. Research NIST 111, 257–312, 2006.

Front-End Materials Characterization

This is a large project that involves parts that are not reasonably combined in a single document. For this reason, the project is presented in two sub-sections, each focusing on a single aspect. These are:

- Front-End Materials and Emergining Advanced Materials Characterization
- Micro-and Nanoanalysis of Front End Materials

Front-End Materials and Emerging Advanced Materials Characterization

Technical Contacts:
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Joseph J. Kopanski
Nhan Nguyen

Goals

The goals of this project are to provide the IC industry with more useful and accurate measurements, models, data, and measurement transfer mechanisms for the incorporation of new materials into advanced CMOS, to enable the continuation of scaling, as well as, beyond the limits of scaling. The major near term focus is on the search for new channel materials, new higher-κ dielectrics, metal gates and the integrated structure involving all three material types. Beyond 2011, high-mobility channel materials are expected to replace silicon in CMOS technology. New device structures, such as multi-gate non-planner transistors, are expected to replace the planar MOSFET. Devices based on semiconductor nanowires, carbon nanotubes, III-V quantum-well transistors, or another technology may even be used. The pace of new materials introduction is expected to increase. The introduction of new materials always presents substantial process integration challenges, as well as new reliability concerns. New metrology techniques must be developed to keep pace with all these changes. New measurement techniques are needed to address physical, chemical, optical and electrical properties of these new materials at the device level. Our current goals are:

(1) To improve the measurements of composition and thickness of thin films and interfaces for high-κ/compound metal gates on III-V compound semiconductors, silicon-on-insulator (confined silicon), and strained silicon-germanium.

(2) To improve measurement capabilities (on large custom made test structures) of interface energy barrier, work function, band offset, and interfacial defect structures of high-κ / metal electrode stacks on III-V systems.

(3) To develop high-resolution techniques (such as various kinds of scanning probe microscopy) to measure two-dimensional dopant profiles in advanced devices, strain profiles in channels, work functions and surface potential distributions, and dielectric constants.

(4) To correlate materials properties to the electrical performance of the transistor.

Customer Needs

The semiconductor industry has historically achieved exponential performance gains by aggressively scaling transistor dimensions. However, as devices approach sub-100 nm dimensions, scaling becomes more challenging and new materials are required to overcome the fundamental physical limits of the existing materials. The pace of new materials introduction is increasing as CMOS technology continues to advance. The introduction of new material into CMOS technology is always extremely challenging. For example, the introduction of high-κ/metal gate stack was considered impractical for a very long time. Even as high-κ dielectrics and metal gates went into early production in 2008, the materials and measurement needs for these material systems continue to evolve. The need for alternative channel materials 11 to overcome the carrier-mobility limitations of silicon is expected as early as 20. Non-planar, multi-gate transistors are expected to be required as well. Even new device structures based on nanowires may be needed. In current main-stream CMOS technol-

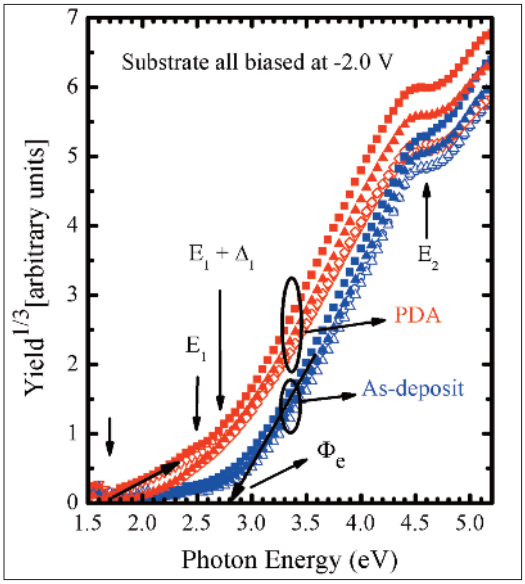

Figure 1. Red-colored and blue-colored symbols are cube root of the IPE yield as a function of photon energy for post-deposition annealed (PDA) and as-deposited $Al2O_3$, respectively. Filled and open symbols correspond to n-type and p-type substrate, respectively. All the IPE data shown were taken with the substrate biased at -2.0 V.

ogy, the use of strain in the channel region to enhance carrier mobility created fundamental materials questions such as determining the stress-strain relationship on the nanoscale. Such questions urgently need new measurement capability to address them. The answer has direct implication for technology decisions in the next generation and beyond.

Front end materials are in the critical path of technology decisions. A wrong decision may not only be expensive, but even disastrous. Facing the increasingly wider choices (or potential technology options), industry needs highly efficient, highly reliable, and highly accurate metrology tools to help them make the right choice. The winter 2007 International Technology Roadmap for Semiconductors (ITRS) conference discussed these trends and the new measurement challenges for Front-End Process Metrology, High κ/ metal gate stacks, alternative channel materials, and emerging research materials and devices. The current most important challenge in III-V nanoelectronics for logic is the compatibility of the III-V material and the high-κ/ metal gate.

III-V compound semiconductor devices have involved into a major part in industrial applications of communication devices as stated in the International Technology Roadmap for Semiconductors (ITRS). High-frequency III-V compound semiconductor devices with nanometer feature sizes have become key components in many high-speed systems. Only recently, III-V metal-oxide-semiconductors (MOS) with high-κ dielectric insulator have been realized as a possibility to replace the Si-based traditional MOS beyond the 22 nanometer technology node.

Technical Strategy

Understanding the physics of the high-κ/metal gate structure on III-Vs is critical to successfully selecting the right dielectric and metal to fabricate and implement the next complex emerging nanoelectronic devices. Within our resources, the approach is to find a way to produce a stable and reliable high-κ dielectric on a III-V substrate. Our focus areas include development of the III-V substrate surface treatment that allows a growth of electronically stable high-κ material and refined metrology methods to determine the interfacial physical, chemical, and electronic properties.

Energy Band Alignment of Metal Gate/ High-κ/III-V compound semiconductor

Intel and IBM have successfully implemented metal gate and high-κ dielectric structures in place of the traditional poly-silicon and thermal SiO_2 for the 45nm manufacturing process. Intel cofounder Gordon Moore stated "The implementation of high-κ and metal materials marks the biggest change in transistor technology since the introduction of poly-silicon gate MOS transistors in the late 1960s." Such successes have opened up the possibility of extending silicon-based CMOS to employ metal gate and high-κ dielectric on high-mobility III-V compound semiconductors for high-speed and high-performance electronic device fabrication. However, the main difficulty that hinders the advancement of GaAs-based metal oxide semiconductor field-effect transistors is the lack of an appropriate oxide as a gate dielectric. There have been many efforts to search for electronically reliable and thermodynamically stable gate dielectrics that can be grown or deposited on GaAs. In addition, the stringent requirement that its fabrication method be compatible with Si-based device processing imposes a greater challenge. Several dielectrics have been investigated including Gd_2O_3, Al_2O_3, and HfO_2. One of the deciding factors for the selection of an appropriate dielectric is the band offsets at the dielectric interfaces with the III-V substrate and the metal gate, which must be large enough to minimize leakage currents.

DELIVERABLES:

- Optical characterization and band alignment determination of Al/Al_2O_3/InP 4Q 2010.

It is believed that III-V MOS devices will significantly outperform scaled Si MOSFETs. Researchers in academia and industrial laboratories, including Intel Inc, Motorola, International SEMATECH, Purdue University, and University of Texas at Dallas, have invested resources to investigate these devices. At the current status, it appears that the key to successful III-V device fabrication is to find a stable and efficient high-κ gate stack on III-V channels. To that effort, in collaboration with Prof. Peide Ye and his research group at Purdue University, we have started investigating the electronic properties of the interface of various high-κ dielectric and III-V substrates using optical and electrical characterization techniques including a novel internal pho-

toemission spectroscopy, vacuum ultraviolet spectroscopic ellipsometry, and traditional electrical methods.

Accomplishments

Recently, in collaboration with Intel and Purdue University, we employed Internal Photoemission Spectroscopy (IPE) and Vacuum Ultraviolet Spectroscopic Ellipsometry (VUV-SE) measurements to establish the energy band offsets at the interfaces of Al_2O_3 as the high-κ dielectric on molecular-epitaxy-grown high-mobility In1-xGaxAs with an Al metal gate. We found that Al_2O_3 provides conduction band and valence band offsets at its interfaces with InGaAs of more than 2 eV, which makes this high-κ dielectric suitable as a gate insulator for III-V MOSFET devices. Furthermore, the effect of post deposition annealing is observed to reduce the band offsets and induce an interfacial layer (See Figure 1). Such interfacial layer results in a much lower band offset at the interface and may lead to enhanced charge injection from InGaAs into the insulation layer. Therefore, the interfacial oxide layer between InGaAs and high-κ dielectric should be avoided or minimized.

Semiconductor Physical Property and Device Electrical Characterization with Scanning Probe Microscopes

The emerging need for alternative channel materials for ultimate CMOS opens up a plethora of materials characterization issues. Strained Si-Ge has already been implemented in current technology-node CMOS, while alternative channel materials such as Ge-on-insulator for PMOS and III-V for NMOS technology have been proposed for ultimate CMOS. Characterization of the complete MOS stack including the work function of the metal gate, the band offsets, and the interfacial defect structures of high-κ combinatorial metal electrode stack systems becomes necessary. Integration of these new materials into existing process lines and their effect on device performance and reliability are key concerns to ensure manufacturability. Steep threshold devices for Green Electronics, FINFET devices, and emerging light emitting and photovoltaic devices all present new device structures with extreme physical characterization challenges.

We are developing and employing several varieties of scanning probe microscopy (SPM) for characterization of critical front end material parameters. SPMs offer the promise of extremely high spatial resolution measurement of local electrical properties. Scanning capacitance microscopy (SCM) remains of interest for measurement of both ultra-shallow junction dopant profiles in silicon as well as in strained Si-Ge and III-Vs. Improvements in this technique are needed to achieve the spatial resolution requested in the ITRS. A new generation of SPM-based methods is possible that integrate measurement instruments directly into SPM tips. We are building on-chip capacitance sensors which can be placed in very close proximity to the AFM cantilevered tips. This will endow the interface between the sensor and the tip with very low stray capacitance. Many traditional capacitance-based measurement methods such as C-V, Spectroscopic Photo-Capacitance, Fourier Transform deep level transient spectroscopy, and other optically pumped spectroscopies may be enabled by such an instrument. This approach may have significant applications to semiconductors for high power and photovoltaics as well.

Another technique of great interest is the scanning Kelvin force microscope (SKFM) for the local measurement of contact-potential difference. If the tip work function is known, the work function of the sample under test can be deduced. We have recently demonstrated test structures with multiple different metals, for example, aluminum ($\varphi Al = 4.28$ eV), chromium ($\varphi Cr = 4.5$ eV), and gold ($\varphi Au = 5.1$ eV). Since the effective work functions of these three metals can be measured with tips of known work function, they can then be employed as a vehicle to determine the work functions of tips that are not known, for example, carbon nanotube tips. Recent work has demonstrated the spatial resolution limits of the SKFM microscope and has suggested a method to improve the spatial resolution. SKFM depends on the capacitance between the tip and the sample, which varies as the inverse square of the separation of the various parts of the tip with the sample. As this is a relatively large-range force, the tip, tip sidewall, and cantilever all contribute significantly to the measured CPD, effectively making measurements that are simultaneously accurate and having high spatial resolution impossible. Several methods for improving the spatial resolution of the SKFM by using the derivative of the force between the tip and sample as the feedback signal are under develop-

ment. If its spatial resolution can be improved, SKFM has many potential applications.

DELIVERABLES:

- Develop scanning Kelvin force microscopy (SKFM) based on a tuning fork AFM in both the normal and lateral oscillation modes at 32 kHz. Demonstrate first Kelvin probe based on a laterally ocsillating tip. Q4 2010.

Conventionally available scanning Kelvin force microscopy (SKFM) suffers from poor spatial resolution due to the capacitive coupling of all parts of the tip/cantilever assembly with the sample. We have demonstrated improved spatial resolution by using carbon nanotube terminated tips and have demonstrated the feasibility of implementing frequency modulated or phase feedback modes of SKFM at atmospheric pressure. Implementation of both these improvements promises higher quality SKFM measurements of contact potential difference than previously available.

DELIVERABLES:

- Work with collaborators at SEMATECH, Xidex Corp., and the CNSE, University of Albany to measure SEMATECH Produced structures with CNT-based tips. Measure dopant profiles in ultra-shallow junction split samples and FINFET test structures with 65 nm and 15 nm channel widths. Demonstrate detection of low-κ plasma etch damage with SKFM and intermittent-contact SCM. Meet written deliverables with SEMATECH. Q3 2010

Beginning in September of 2009, we have a yearlong collaboration to determine the performance of electrically based SPM methods using conductive carbon nanotube tips fabricated by Xidex Corp. using samples fabricated by SEMATECH at the University of Albany. We will compare the performance of these tips with the best currently commercially available. Specific goals include determination of the work function and resistivity of the CNTs, and demonstrating of the use of CNT tips for SCM and SKFM dopant profile measurements of FINFET devices, determination of dielectric constant damage to low-κ dielectrics, and high spatial resolution work function measurements.

ACCOMPLISHMENTS

■ Graduate guest researcher Ilona Sitnitsky from the University of Albany has been in residence at NIST since August 2009. We have measured the resistivity of CNT terminated SPM tips, dopant profiles of ultr-shallow junction splits, and various damaged low-κ test structures. The work that Ilona has conducted at NIST has been the basis of her Master's Thesis with her degree awarded May 2010.

■ Fabricated a test chip with which to determine the current state of the art of capacitance-voltage measurements. The component capacitance of individual nm-scale nanoelectronic devices for future generations of integrated circuitry defies easy measurement. Emerging nanoelectronic devices such as those fabricated from semiconductor nanowires (NWs) and quantum dots, as well as FINFET type devices have capacitances that are much smaller than those measurable by conventional LCR meters. The intrinsic device capacitances of these deep-submicron devices (such as the gate-drain, source-drain, or gate-channel capacitances) determine the operational characteristics of the structures and an accurate knowledge of their values is required for accurate device modeling and predictive computer-aided design. We are developing methods to combine probe stations with the sophisticated capacitance measurement equipment and expertise associated with maintaining the capacitance standard for the farad to enable measurements of critical capacitances in nanoelectronic devices at the aF level.We designed and fabricated a test chip (consisting of an array of metal-oxide-semiconductor (MOS) capacitors and metal-insulator-metal capacitors ranging from 0.3 fF to 1.2 pF) for use in evaluating the performance of new measurement approaches for small capacitances (see Fig. 2). By measuring the complete array of capacitances, a "fingerprint" of capacitance values is obtained (see Fig. 3) which – after correcting these data for pad and other stray capacitances – can be used to assess the relative accuracy and sensitivity of a capacitance measurement instrument or circuit. We have designed and are implementing in a custom integrated circuit charge based capacitance measurement circuits (CBCM) as a means of chip based capacitance measurements that can be accessed through an AFM tip. These devices will be included on a custom design chip holder, bringing the AFM tip to within a few millimeters of the input of the CBCM circuit. Several approaches to automatically compensate the stray capacitance between the tip and sample are included in the initial test CBCM circuits. We hope to duplicate our measurements with stand alone meters using the AFM based CBCM cirucits.

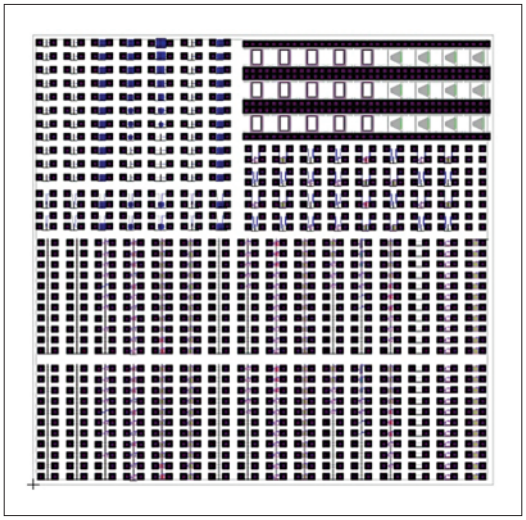

Figure 2. Small capacitance test chip. Chip contains a series of MOS and MIM capacitors designed to test the sensitivity and accuracy of capacitance measurement instruments at levels of 0.1 fF to 1 pF. Devices directly assessable via scanning probe microscopy are in the upper right hand corner for calibration of the scanning capacitance microscope (SCM) and the scanning Kelvin force microscope (SKFM).

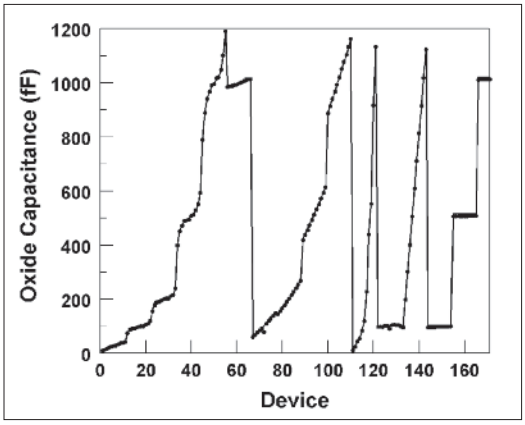

Figure 3. Typical "fingerprint" of the measured oxide capacitance values of the MOS devices on the test chip. Theoretical values of oxide capacitance are plotted as the solid line and the measured values are the plotted points (after correcting for stray and pad capacitances.) This test chip will be used to compare the sensitivity and accuracy of chip-based capacitance measurement circuits to conventional capacitance measurement instruments.

Collaborations

Agilent Technologies and NIST Boulder, Data Interpretation of Scanning Microwave Microscopy measurements for dopant profiling.

Center for Nanophase Materials Sciences, Oak Ridge National Laboratory – User proposal reviewer.

Intel – Electrical and optical characterization of metal gate/ high-κ dielectric / III-V high mobility semiconductors.

Intel – Measurement of ultra shallow dopant profiles using SCM and advanced tips.

International SEMATECH – Optical electrical characterization and energy band alignment of ternary metal gate/high-κ / Silicon.

International SEMATECH, ATDF – Thin oxide depth-profiling by SIMS, backside depth profiling of patterned PMOS wafers.

International SEMATECH – Improvement of the SCM and SKFM techniques for two-dimensional dopant profiling and surface work function measurements.

IBM – Physical and optical characterization of high- κ on Silicon.

MSEL, NIST – Characterization of metal gate/high-κ systems.

National Science Foundation – NIST Research Experience for Undergraduates site: EEEL Summer Undergraduate Research Fellowships

Purdue University – Surface characterization and electrical and optical band offset characterization of metal gate/ high- κ dielectric / III-V high mobility semiconductors.

College of Nanoscale Science and Engineering, University of Albany – Scanning probe microscopy characterization of front end processes and advanced materials.

University of Texas-Dallas – Surface characterization and electrical and optical band offset characterization of metal gate/ high-κ dielectric / III-V high mobility semiconductors.

University of Maryland, College Park – Ultra-thin gate oxide reliability.

Xidex Corp. – Evaluation of carbon nanotube tip for use in SCM and SKFM.

Yale University – Electrical characterization of high-κ systems.

Publications

N. V. Nguyen, M. Xu, O. A. Kirillov, P. D. Ye, C. Wang, K. Cheung, and J. S. Suehle, *"Band offsets of Al_2O_3/InxGa1−xAs (x = 0.53 and 0.75) and the effects of postdeposition annealing"*, Appl. Phys. Lett. 96, 052107 (2010)

J. J. Kopanski, P. McClure, and V. Mancevski, *"Enhanced Spatial Resolution Scanning Kelvin Force Microscopy Using Conductive Carbon Nanotube Tips,"* Proceedings of the International Conference on Frontiers of Characterization and Metrology for Nanoelectronics, pp. 212-216, Albany, NY, May 11-15, 2009, (Oct. 2010).

C. A. Richter, J. J. Kopanski, C. Jiang, Y. Wang, M. Y. Afridi, X. Zhu, D. E. Ioannou, and Q. Li, *"Advanced Capacitance Metrology for Nanoelectronic Device Characterization,"* Proceedings of the International Conference on Frontiers of Characterization and Metrology for Nanoelectronics, pp. 328-332, Albany, NY, May 11-15, 2009, (Oct. 2010).

J. J. Kopanski, M. Y. Afridi, C. Jiang, and C. A. Richter, *"Test Chip to Evaluate Measurement Methods for Small Capacitances,"* Proc. 2009 IEEE Intl. Conf. Microelectron. Test Structures, (Oxnard, CA, Mar. 30- Apr. 2, 2009).

N. V. Nguyen, O. A. Kirillov, W. Jiang, Wenyong Wang, J. S. Suehle, P. D. Ye, Y. Xuan, N. Goel, K.-W. Choi, W. Tsai, and S. Sayan, *"Band offsets of atomic-layer-deposited Al_2O_3 on GaAs and the effects of surface treatment,"* Appl. Phys. Lett. 93, (2008).

J. J. Kopanski and T. R. Walker, *"Scanning Probe Microscopy for Dielectric and Metal Characterization,"* Electrochem. Soc. Trans. 13(2), 213th ECS Meeting, May 18 - May 23, 2008, Phoenix, AZ, Dielectrics for Nanosystems 3: Materials Science, Processing, Reliability, and Manufacturing, Editor(s): D. Misra, H. Iwai, Y. Obeng, T. Chikyow, J. Vanhellemont.

N. V. Nguyen, O. A. Kirillov, W. Jiang, J. E. Maslar, W. A. Kimes, *and J. S. Suehle, "Interface Barrier Determination by Internal Photoemission: Applications to Metal/Oxide/Semiconductor Structure,"* Electrochem. Soc. Trans. 13, (2) 161, March (2008).

N. V. Nguyen, H. D. Xiong, J. S. Suehle, O. A. Kirillov, E. M. Vogel, P. Majhi, and H.-C. Wen,*"Internal Photoemission Spectroscopy of [TaN/TaSiN] and [TaN/TaCN] Metal Stacks,"* Appl. Phys. Lett. 92, 092907 (2008).

S. Sayan,D. Chandler-Horowitz, N. V. Nguyen, and J. R. Ehrstein, *"High sensitivity attenuated total reflection Fourier transform infrared spectroscopy study of ultrathin ZrO2 films: A study of phase change,"* J. Vac. Sci. Technol. A 26, 270, Mar/Apr 2008.

D. H. Hill, R. A. Bartynski, N. V. Nguyen, A. C. Davydov, D. Chandler-Horowitz, and M. M. Frank, *"The relationship between local order, long range order, and sub-band-gap defects in hafnium oxide and hafnium silicate films,"* J. Appl. Phys. 103, May (2008).

J. E. Maslar, W. S. Hurst, D. R. Burgess, W. Kimes, N. V. Nguyen, E. F. Moore, and J. T. Hodges, *"In Situ Gas Phase Diagnostics for Hafnium Oxide Atomic Layer Deposition,"* Electrochem. Soc. Trans. 13, 139, March (2008).

N. V. Nguyen, O. Kirillov, H. D. Xiong, and J. S. Suehle, *"Internal Photoemission Spectroscopy of Metal Gate / High-κ / Semiconductor Interfaces,"* Frontiers of Characterization and Metrology for Nanoelectronics: 2007, AIP Conference Proceedings 931, page 308 (2007).

J.E. Maslar, W.S. Hurst, D.R. Burgess, Jr., W.A. Kimes, N.V. Nguyen, and E.F. Moore, *"In Situ Characterization of Gas-Phase Processes During Hafnium Oxide Atomic Layer Deposition,"* Electrochem. Soc. Trans. 2, 133-143 (2007).

J. J. Kopanski, M. Y. Afridi, S. Jeliazkov, W. Jiang, T. Walker, *"Scanning Kelvin Force Microscopy For Characterizing Nanostructures in Atmosphere,"* Proceedings of the International Conference on Frontiers of Characterization and Metrology for Nanoelectronics, pp. 530-534, Gaithersburg, MD, March 27-29, 2007, (Sept. 2007).

J. J. Kopanski, *"Scanning Capacitance Microscopy for Electrical Characterization of Semiconductors and Dielectrics,"* in the book: Electrical and Electromechanical Characterization by Scanning Probe Microscopy, Springer Science + Business Media, Inc., New York, NY (Feb. 2007).

Micro- and Nanoanalysis of Front End Materials

Technical Contacts:
G. Gillen: SIMS
D. Simons: SIMS
S. Stranick: Confocal Raman microscopy

Goals

To provide industry with new and improved measurements, models, data, and measurement traceability/transfer mechanisms to enable the more useful and more accurate metrology infrastructure needed for select silicon CMOS front-end materials characterization. The major focus is placed on the metrology requirements from the 2009 International Technical Roadmap for Semiconductors (ITRS) expressed as difficult challenges: (1) structural and elemental analysis at the device level, including SIMS, and (2) metrology for advanced gate stacks and other thin films. Additional work will be undertaken as possible on additional important thin films and bulk material properties for silicon and other emerging semiconductors.

(1) To improve capabilities for compositional depth profiling, this project develops new methods for depth-profiling polymeric materials by Secondary Ion Mass Spectrometry (SIMS), defines optimum procedures for ultra-high depth resolution, develops depth-profiling reference materials needed by U.S. industry, and improves the uncertainty of implant dose measurements by SIMS.

(2) To address needs in composition and thickness measurements for thin films and interfaces, this project develops new optical and physical characterization methods, as well as characterizes the accuracy and reliability of existing methods. Materials of interest include high-κ and low-κ materials, polymers, silicon-on-insulator (confined silicon), and strained silicon-germanium. Confocal Raman microscopy is being developd as a non-destructive method for characterization of stress in semiconductor structures.

Customer Needs

This project addresses key material characterization problems associated with the integrated circuits industry's front-end process, particularly new gate stack processes and materials, and metrology for structural and element characterization at the device level, particularly ultra-shallow junctions. Front-end processing requires the growth, deposition, etching, and doping of high quality, uniform, defect-free films. These films may be insulators, conductors, or semiconductors. The 2009 International Technology Roadmap for Semiconductors (ITRS) metrology requirements for Front End Processing, including those associated with 2-D dopant profiling, as well as metrology needs for thermal/thin films, doping technology, SOI, strained-silicon and materials and contamination characterization, are discussed in the Metrology section of the 2009 ITRS.

Since source/drain dopant profiles are a critical factor determining the performance of a transistor, dopant profiling has always been needed by the silicon integrated circuit industry. One-dimensional dopant profiles from SIMS or electrical techniques remain an important process control tool. As transistors are scaled to ever-smaller dimensions, the variation of dopant profiles in two- and three-dimensions also begin to influence device operation. Two- and three-dimensional dopant profiles are now needed to validate models of the processes used to produce ultra-shallow junctions and for accurate device simulations.

SIMS is most likely to provide the solution to precision requirements for 1-D dopant concentration measurements. These goals can be achieved by careful control of SIMS depth-profiling conditions and by developing and making available implant reference materials for common dopant elements.

According to the 2009 ITRS Metrology section, offline secondary ion mass spectroscopy has been shown to provide the needed precision for current generations including ultra-shallow junctions. Two- and preferably three-dimensional profiling are essential for achieving future technology generations. Activated dopant profiles and related TCAD modeling and defect profiles are necessary for developing new doping technology. The ITRS requirements are for at-line dopant profile concentration measurements with precision of 4 % in 2009, decreasing to 2 % precision for the 2010 through 2024 timeframe. The lateral/depth resolutions for 2-D/3-D dopant profiling decrease from 3.5 nm in 2009 to 1.8 nm in 2015. Complete specifications are in Table MET5 of the 2009 Metrology section. The desirability of nondestructive direct measurement of stress in nano-

sized areas of strained silicon is described in the Front End Processes area of the Metrology section, and specific requirements for spatial resolution and throughput are given Table MET5.

Technical Strategy

The 2009 ITRS expressed as difficult challenges: "starting materials metrology and manufacturing metrology are impacted by the introduction of new substrates such as SOI. Impurity detection (especially particles) at levels of interest for starting materials and reduced edge exclusion for metrology tools. CD, film thickness, and defect detection are impacted by thin SOI optical properties and charging by electron and ion beams," and "measurement of complex material stacks and interfacial properties including physical and electrical properties" (Table MET1, Metrology Section). Our focus areas include development of refined metrology methods and standards for SIMS and Raman microscopy, and developing improved X-ray detection capabilities for SEMs and electron microprobes.

Structural And Elemental Analysis At The Device Level

Strained Si processes have become an accepted means for enhancing carrier mobility and thereby improving transistor performance. The ITRS calls for a nondestructive method for measuring stress in nano-sized areas of Si to accelerate process development. Confocal Raman microscopy is a potential in-line method to achieve this goal with the required sensitivity and spatial resolution. We are conducting a systematic investigation to determine the feasibility of this methodology for achieving the metrology goals for stress and strain that are called out in the 2009 ITRS.

DELIVERABLES:

- Apply confocal, atomic force and super resolving Raman microscopy to the characterization of strain in nanostructured Si. 3Q 2010

As integrated circuit dimensions shrink to the sub-micrometer regime, there is continued need for accurate and quantitative dopant depth profiling with ultra-high-depth resolution. To probe shallow dopant profiles in Si and other materials, SIMS instruments typically utilize very low energy primary ion beams to bombard the sample surface. In this case, it is difficult to obtain a well-focused and high current density beam, especially in a magnetic-sector SIMS instrument. Recently, there has been growing interest in using molecular ion beams for depth profiling. When a molecular primary ion beam impacts the surface, it dissociates into its constituent atoms with each atom retaining a fraction of the initial energy of the cluster.

This process can lead to impact energies on the order of a few 10's of electron volts and a corresponding reduction in the depth of penetration of the primary ion. This process may potentially allow for ultra high resolution depth profiling. In this project, we will utilize C_{60}+, Bi_3+ and SF_5+ cluster primary ion beam sources at NIST to sputter depth profile Si, GaAs, SiC, and multiple delta-layer test materials. Some thin-film materials such as metals do not sputter as uniformly as silicon under ion bombardment. In these cases, the achievable depth resolution is limited not by the penetration depth of the primary ion but by the topography induced by the sputtering process itself.

DELIVERABLES:

- Determine optimized parameters for depth-profiling of PMMA/Si bilayer films under cluster ion bombardment. 3Q 2010

Accomplishments

Implementation of C_{60+} Cluster Ion SIMS Capability for SIMS Analysis of Silicon Wafers

Previous efforts using SF_{5+} cluster primary ion sources used for SIMS analysis of both organic and inorganic materials on silicon have been very successful. Minimization of beam-induced damage in organic materials has allowed molecular depth profiling of polymers such as photoresists on silicon and enhanced ion yields for high-molecular weight fragments. Inorganic material analysis has benefited in the area of ultra-shallow depth-profiling as well as for analysis of some particularly difficult systems such as metal multilayers stacks. Continued development of SIMS for higher depth resolution dopant profiling has led to the implementation of a C_{60}+ primary ion source on the NIST magnetic sector SIMS instrument. This ion source produces stable ion beams of C_{60}+ and $C_{60}2$+ at beam energies of 10 keV with typical currents approaching 20 nA under conditions that allow several hundred hours

of operation. The beam can be focused into a spot size of ≈1 μm allowing micrometer spatial scale mapping of patterned silicon wafers. Due to the breakup of the C_{60}+ projectile during impact with the silicon surface, the energy of an individual carbon atom in the cluster is reduced to a few hundred electron volts. This low energy should theoretically provide SIMS depth resolution better than 1 nm. Reduction of the C_{60}+ impact energy to values less than 10 keV to attempt further improvement in depth resolution is foiled by carbon deposition that precludes the acquisition of depth profiles from the wafer sample. However, the deposition effect may be useful for lithographic applications as it allows direct ion beam writing of a conductive carbon layer on silicon. By using C_{60}+ impact energies greater than 10 keV, C_{60}+ SIMS depth profiles have been obtained from a number of semiconductor-related materials including As and B delta-doped structures as well as ion implants of various dopant species. The depth resolution of SIMS depth profiles obtained from these samples has not been as high as expected. To understand the process in more detail, transmission electron microscopy (TEM) studies of C_{60}+-bombarded silicon have been carried out using focused ion beam (FIB)-prepared cross sections of the sample surface. Figure 1 shows a cross sectional TEM image of a silicon wafer bombarded with C_{60}+ at an impact energy of 14.5 keV. The figure indicates that C_{60}+ bombardment of silicon results in the formation of a carbon-rich altered layer that is about 25 nm thick, much greater than the 2 nm range predicted from conventional ion implantation models. Working with Micron Technology and International SEMATECH, we are currently studying the effect of this extended transport of carbon into silicon both from the standpoint of improving the applicability of larger carbon cluster ion beams for SIMS analysis and also as a potential method for direct-write fabrication of SiC films and devices on silicon.

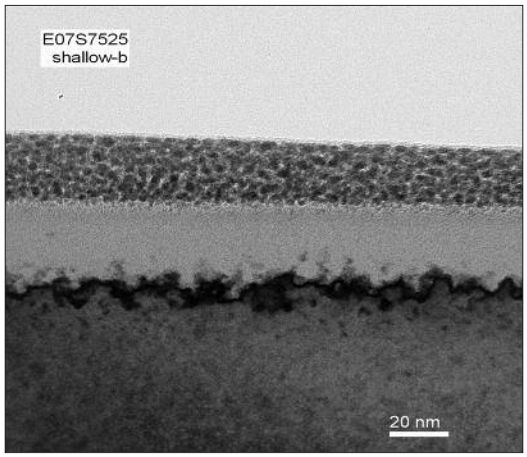

Figure 1. Cross sectional TEM image of C_{60}-bombarded silicon wafer. Top layer is a Pt metal overcoat. Middle layer is C_{60} altered layer. Bottom layer is the silicon substrate.

Molecular Depth Profiling of Photoresist Films Using SIMS

Recent advances in cluster secondary ion mass spectrometry (SIMS) have led to the ability to perform molecular depth profiling for a range of organic materials. Cluster SIMS can provide high sputter yields that remove beam-induced molecular damage as it is created. In time-of-flight SIMS analysis a "dual-beam technique" can be exploited by using a cluster ion beam such as SF_5+ or C_{60}+ for continuous sample erosion and minimal damage accumulation, combined with a highly focused pulsed analysis probe such as Bi_3+ or Au_3+. However, little has been reported concerning the effects imparted by the use of the analysis beam. We have found that increasing the total Bi_3+ fluence beyond 1012 ions/cm^2 within a SIMS dual-beam sputter depth profiling experiment can degrade the quality of the interface widths of a PMMA film on silicon, despite the use of sputter beams such as SF_5+ and C_{60}+ to remove accumulated beam-induced damage. Specifically, Figure 2 shows the effects of steadily increasing amounts of 25 keV Bi_3+ analysis fluence with constant 5 keV SF_5+ sputter fluence. Normalized depth profile data signals of the characteristic PMMA fragment ion at m/z 69 (corresponding to $C_4H_5O^+$) and the substrate silicon ion at m/z 28 are plotted in Figure 2 vs. PMMA film depth. The black and red profiles at the two lowest Bi_3+ fluences have similar shapes and the factor of three increase in analysis beam fluence between them did not degrade the profile shape through the polymer/silicon interface. However, increasing the total analysis fluence to 2.2 x 10^{12} ions/cm^2 (blue profile) shows a degradation of the interface quality and an earlier depth at which silicon signal appears in the profile. Increasing the Bi_3+ analysis fluence to the highest values in the figure (green and grey profiles) shows a trend of earlier silicon and increased interface width. The generation of analysis beam-induced topographic roughness can create paths for substrate ions to be ejected through the overlayer film before the entire film is eroded away by sputtering.

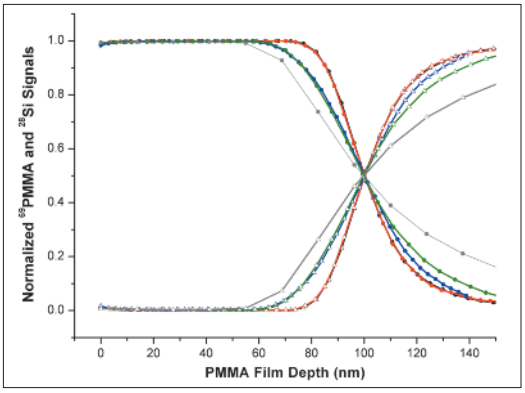

Figure 2. Normalized dual-beam TOF-SIMS depth profiles of PMMA on Si for 5 different fluences of $Bi3^+$ analysis beam. Solid circles –$^{69}C_4H_5O^+$; Open triangles –$^{28}Si^+$.

The characteristic exponential decay lengths of the PMMA signal range from 14.1 nm to 50.5 nm in Figure 2. These data imply that the energetic $Bi3^+$ projectiles generate enough sub-surface molecular damage and/or molecular rearrangement so that cluster sputtering becomes inefficient at removing the analysis-beam-induced effects. This study implies that careful attention must be applied when establishing the instrumental parameters for a molecular depth profiling measurement of an overlayer on silicon. PMMA on Si is a simple system, and it is expected that this behavior will be more pronounced for systems of multiple organic layers where more extensive beam-induced mixing and topographic roughness can accumulate as a function of eroded depth.

A properly defined cluster SIMS measurement can overcome these analysis beam effects and generate depth profiling results of organic and mixed organic/inorganic samples that allow for detailed study of interface chemistries on the nanoscale.

Measurements of Residual Stress Using Confocal Raman Microscopy

Residual stress states are critical in determining the manufacturing yield and operational performance of many advanced silicon (Si)-based devices. Deposition strains and thermal expansion mismatch can generate residual stresses that alter the electronic and mechanical properties of solid-state electronics, infrared optical, and photovoltaic devices. These effects can compromise device functionality although deliberate "stress engineering" can also be used to enhance or tune device performance. In order to optimize the yield and performance of Si devices, measurements of residual stress states are critical. To address this need, work has been focused on the application and advancement of confocal Raman microscopy (CRM) and the protocols that enable the characterization of stress in semiconductor structures. The results of high-resolution, high-density stress mapping of nanoindentations in silicon have been used to validate and calibrate the measured stress. In these studies, high-resolution scans detail the stress distribution around the deformed area of the indentation. The development of hyperspectral peak-fitting algorithms and super-resolution techniques provides stress resolution of approximately 10 MPa lateral spatial resolution approaching 100 nm, and depth resolution approaching 200 nm.

Our current studies extend the mapping of residual stress fields in much greater detail and with greater surface sensitivity. Figure 3 shows the residual stress map obtained on Si(100) from the CRM data, revealing symmetric, anisotropic patterns of alternating compressive (darker) and tensile (lighter) stress lobes adjacent to the contact impression. The impression is indicated by the grayed-out disk from which data were excluded; the presence of multiple Si phases in the impression hinders straightforward data collection and analysis. The residual stress field decreases significantly in intensity with increasing distance from the impression. The symmetry of the stress field is specific to the crystallographic orientation and direction of mechanical loading of the indented Si single crystal. The stress map of these features provides information critical for determining the suitability of a material for a given application. Current efforts are focused on the development of models and the benchmarking of experimental protocols for the complete characterization (tensor field vs. scalar map) of intrinsic and engineered stress states in semiconductors.

Inkjet Printing for Trace Metal Contamination Standards

Prototype reference materials for trace element contamination on silicon surfaces have been prepared using piezoelectric drop-on-demand inkjet printing technology. Reference materials were prepared for 6 different elements (K, Cl, Ni, Cu, Fe, and Au) at surface area concentrations ranging from 10^7 atoms/cm^2 to 10^{15} atoms/cm^2. Each element was prepared on a separate 2.5 cm diameter silicon wafer. The mi-

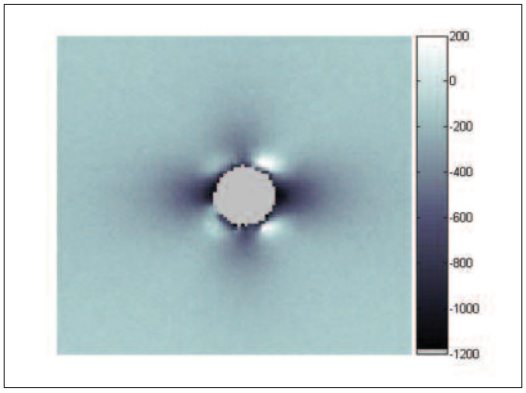

Figure 3. Residual stress field mapped by CRM of single crystal Si indented perpendicular to Si(100) surface plane. Scan sizes: 12.5 µm x 12.5 µm.

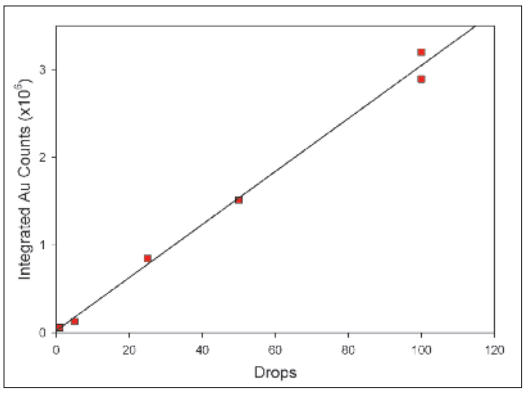

Figure 4. Integrated gold secondary ion counts from depth profiles plotted against the number of droplets dispensed by the inkjet printer. One drop = 1.3 x 10^{12} atoms/cm^2.

crodroplets were dispensed onto specific grid squares that had been previously scribed onto the silicon surface in a finder grid pattern with a laser. Different concentrations of the elements were achieved by printing different numbers of microdroplets in the same location. Dispensing droplets onto specific locations on a finder grid allowed different contaminant concentrations to be located easily and analyzed rapidly by SIMS analysis.

Characterization of these reference materials is in progress. SIMS depth profiles from grid squares containing different numbers of printed droplets show an exponential decay, the amplitude of which scales with the number of droplets applied. Integration of the number of ion counts beneath these profile curves is shown in Figure 4 plotted against the number of droplets printed for concentrations of gold ranging from approximately 1 x 10^{12} atoms/cm^2 to 1 x 10^{14} atoms/cm^2. This plot shows the linear relationship between the measured number of gold ions detected and the number of droplets dispensed.

Collaborations

International SEMATECH, SVTC Technologies – Thin oxide depth-profiling by SIMS, backside depth profiling of patterned PMOS wafers.

Freescale Semiconductor - Evaluation of stress measurements in SiGe structures by confocal Raman Microscopy

Ionoptika – Development of a $C60^+$ primary ion source for advanced semiconductor technology.

MicroFAB Inc – Advanced inkjet printing technology for deposition of trace metal standards on silicon surfaces.

Micron Semiconductor – trace organic detection.

Ultratech - Development of a Si stress reference.

Publications

C.M. Mahoney, "Cluster SIMS Depth Profiling of Stereospecific PMMA Thin Films on Si." Surface and Interface Analysis, in press.

C.M. Mahoney, "Cluster SIMS of Polymers and Related Material," Mass Spectrometry Reviews, 2010, 29, 247-293.

C. Szakal, S.M. Hues, J. Bennett, and G. Gillen, "Effect of Cluster Ion Analysis Fluence on Interface Quality in SIMS Molecular Depth Profiling," J. Phys. Chem. C 114 (2010) 5338-5343.

P.E. Thompson, G.G. Jernigan, D. Simons, P. Chi, B.T. Jonker and G.M.J. Van't Erve, "Phosphorus Doping of Silicon at Substrate Temperatures Above 600° C," Thin Solid Films 518 (2010) S270-S272.

R. B. Marinenko, S. Turner, D.S. Simons, S.A. Rabb, R.L. Zeisler, L.L. Yu, D. E. Newbury, R.L. Paul, N.W.M. Ritchie, S.D. Leigh, M.R. Winchester, D.C. Meier, K.C.K. Scott, D. Klinedinst, and J.A. Small, "Characterization of Si-Ge Films for Use as a National Institute of Standards and Technology Microanalysis Reference Material (RM 8905)," Microscopy and Microanalysis 16 (2010) 1-12.

Y. B. Gerbig, S.J. Stranick, and R.F. Cook, "Measurement of residual stress field anisotropy at indentations in silicon," Scripta Materialia (2010) in press.

Y.B. Gerbig, S.J. Stranick, D.J. Morris, M.D. Vaudin and R. F. Cook , "Effect of crystallographic orientation on

phase transformations during indentation of silicon," J. Materials Res, 24, 1172-1183 (2009).

M.D. Vaudin, Y.B. Gerbig, S.J. Stranick and R. F. Cook , "Comparison of nanoscale measurements of strain and stress using electron back scattered diffraction and confocal Raman microscopy", Appl. Phys. Lett.. 93, 193116 (2008).

D. S. Simons, R. G. Downing, G. P. Lamaze, R. M. Lindstrom, R. R. Greenberg, R. L. Paul, S. B. Schiller and W. F. Guthrie, "Development of Certified Reference Materials of Ion-Implanted Dopants in Silicon for Calibration of Secondary Ion Mass Spectrometers," J. Vac. Sci. Technol. B 25 (2007) 1365-1375.

K. J. Kim, D. W. Moon, C. J. Park, D. Simons, G. Gillen, H. Jin and H. J. Kang, "Quantitative Surface Analysis of Fe-Ni Alloy Films by XPS, AES and SIMS," Surf. .Interface Anal. 39 (2007) 665-673.

K. J. Kim, D. Simons and G. Gillen, "Quantitative Depth Profiling of an Alternating Pt/Co Multilayer and a Pt-Co Alloy Multilayer by SIMS Using a Buckminsterfullerene (C60) Source," Appl. Surf. Sci. 253 (2007) 6000-6005.

C. M. Mahoney, A. J. Fahey and G. Gillen, "Temperature-controlled Depth Profiling of Poly(methylmethacrylate) (PMMA) Using Cluster Secondary Ion Mass Spectrometry (SIMS): I. Investigation of depth profile characteristics," Anal. Chem. 79, 828-836 (2007).

C. M. Mahoney, A. J. Fahey, G. Gillen, C. Xu and J. D. Batteas, "Temperature-controlled Depth Profiling of Poly(methylmethacrylate) Using Cluster Secondary Ion Mass Spectrometry (SIMS): II. An investigation of sputter-induced topography, chemical damage and depolymerization effects," Anal. Chem. 79, 837-845 (2007).

T. Jach, N. Ritchie, J. Ullom, and J. A. Beall, "Quantitative Analysis with the Transition Edge Sensor Microcalorimeter X-ray Detector," Advances in X-ray Analysis 50, 51 (2007).

T. Jach, N. Ritchie, J. Ullom, and J. A. Beall, "Quantitative Analysis with the Transition Edge Sensor Microcalorimeter X-ray Detector," Powder Diffraction 22, 138 (2007).

Advanced Gate Stacks Materials

Technical Contacts:
M. L. Green

Goals

The goals of this project are to develop novel, combinatorially-compatible measurement methods and metrologies that enable the microelectronics industry to select new materials more rapidly and intelligently through use of comprehensive and consistent data sets.

Customer Needs

At present, further scaling (dimensional shrinkage of integrated circuit device elements according to Moore's Law) of Si microelectronics is materials limited. For example, higher mobility substrates (e.g., Ge, GaAs, and strained Si) are needed as replacements for Si, and the traditional gate stack layers (gate dielectric and polycrystalline Si gate electrode) must be replaced with a high-κ gate dielectric and a metal gate electrode. The Si microelectronics industry, and the consumer electronics and information revolution that it fuels, is, at $750 billion, one of the largest sectors of the US (and global) economy. The development of materials with superior properties that enable device scaling and enhanced device performance are key to continued innovation in Si microelectronics.

Currently, there are no rapid measurement techniques to determine the physical and electrical properties of novel metal-oxide-semiconductor (MOS) materials; the availability of such methods would enable rapid selection and optimization of these materials and their commercialization in devices.

Key customers include Sematech, IMEC and major U.S. semiconductor manufacturers such as Intel and Micron. We are very active in promoting the use of combinatorial methodologies with these customers.

Technical Strategy

The CMOSFET device (complementary-metal-oxide-silicon-field-effect-transistor, the workhorse of advanced chips such as Pentium microprocessors), is extremely complex, and the identification of replacement materials with superior properties is difficult due to the large number of candidate materials for either gate stack or high mobility applications. Introduction of new materials is complicated by rigid requirements that they not only possess the requisite physical and electrical properties, but also be manufacturable, thermally stable during processing, and compatible with adjacent material layers. There are no rapid measurement techniques to determine the physical and electrical properties of novel CMOS materials. The availability of such methods would enable the rapid selection and commercialization of such materials. It is imperative to be able to make hundreds or thousands of measurements in parallel, since there are at least that many combinations of novel gate metal electrode/gate dielectric/substrate materials that must be assessed. Further, for some measurements, such as gate metal electrode work function, the most appropriate measurement technique is not apparent. The traditional gate stack layers (SiO_2 gate dielectric and polycrystalline Si gate electrode) in current Si microelectronic devices must be replaced with a high dielectric constant (high-κ) gate dielectric and a metal gate electrode. We will develop combinatorial methodologies to: (1) fabricate compositionally-graded thin film libraries of novel gate metal electrode-high-κ gate dielectric-substrate combinations ("gate stack" structures); and (2) measure the key electronic properties (e.g., work function) and thermal stability of such libraries. In addition, a nanocalorimetry method will be developed to measure thermal stability. Comprehensive data sets of electronic properties as a function of composition will be generated for materials systems identified as high priority by the microelectronics industry.

DELIVERABLES:

- i) Work function determination for Ta-C-N metal gate electrodes, using a single combinatorial library film and newly designed shadow masks, ii) Write software to incorporate finite electric field into model for advanced gate stack. - Q1/10
- i) Measure dielectric constants in ternary library films based on combinations of HfO_2, $Y2O_3$, TiO_2, and Al2O3, ii) Simulate effect of O vacancy on gate stack band structure under applied electrical field – Q2/10
- Analyze band structure of gate stack under electrical field and compare with models for Fermi level pinning – Q3/10
- Work function extraction for Ta-C-N library films on ternary higher-k dielectric films – Q4/10

Accomplishments

We commissioned a state-of-the-art combinatorial tool capable of producing thin film libraries by reactive sputtering or pulsed laser deposition (PLD). Both chambers are equipped with multiple targets, allowing for the deposition of ternary films of metals and nitrides (by sputtering) and oxides (by PLD) with sub-monolayer (0.5 nm) thickness control.

In a screening approach to find higher-κ dielectric materials, combinatorial library films of HfO_2-TiO_2-Y_2O_3 were grown by PLD. The films exhibit visible boundary lines separating amorphous and crystalline regions. By changing the substrate temperature during deposition, we were able to manipulate the boundary and the microstructural properties of the film. Digital photographs of the films, grown at 300 ºC, 400 ºC, 500 ºC, and 600 ºC, are shown in Fig. 1. Visible boundaries are present in each library with the exception of the 300 ºC film. With increasing temperature in those libraries with a visible boundary, the boundary appears to shift and change in 'slope', becoming less 'steep.'

In an approach to finding metal gate electrode materials using combinatorial reactive sputtering, comprehensive structural, chemical, and electrical analyses for the Ta-C-N/HfO_2 system were studied. X-ray fluorescence-yield near-edge spectroscopy (FYNES) was used to quantitatively determine the composition across the libraries. Fig 2 shows the measured fluorescence yields of C and N for four samples: a TaNx film, a CNx film, a Ta-C-N library sample, and a Nylon 6 film. Nylon 6 and CNx show constant C and N fluorescence yields across their sample areas. Likewise, TaNx shows constant N fluorescence yield, as

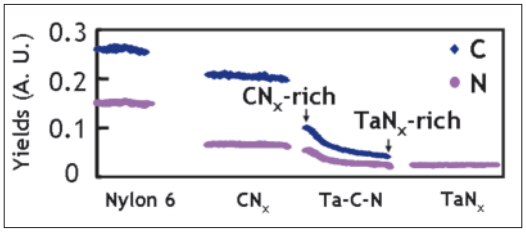

Figure 2. Compositional analysis for the four samples, (a) showing the measured fluorescence yields of C and N from Nylon 6, CN_x, and a Ta-C-N library film, and the fluorescence yields of N from TaN_x, using a FYNES setup.

expected. A small difference is observed, however, between the N yields of the CNx and TaNx samples, most probably due to a difference in their abilities to incorporate N. The Ta-C-N library film, in contrast, yields C and N signals that vary between those of the CNx and TaNx films. The N signal decreases from the CNx–rich end to the TaNx–rich end, consistent with the N variation for the pure CNx and TaNx films. However, the C signal does not vary over a wide range. This can be explained in the following way: 1) the pure CNx and TaNx regions are not achievable in the library film because there is a small gap between the moving shutter and the substrate that allows the introduction of a small amount of material from one target when the other target is in the deposition position, and 2) the resulting small amount of TaNx introduced close to the CNx–rich end of the library film limits the formation of CNx, since a solid solution of Ta(C,N)x is more thermodynamically favorable than CNx.

Collaborations

Joint combinatorial gate stack experiments with Micron, Sematech, and IMEC.

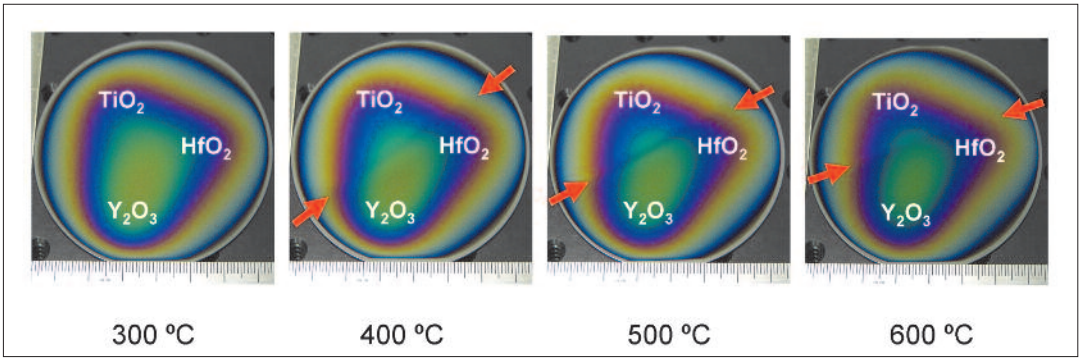

Figure 1. Digital photographs of four HfO_2-TiO_2-$Y2O_3$ library films, each at a different growth temperature. Those library films grown at temperatures greater than 400ºC show a clear boundary separating the TiO_2 amorphous region from the HfO_2-$Y2O_3$ crystalline region.

Publications

K.-S. Chang, M. L. Green, H. M. Lane, I. Levin, C. Jaye, D. A. Fischer, J. R. Hattrick-Simpers, I. Takeuchi, and S. De Gendt, *"Electrical Characterization of Ta-C-N/HfO_2 Advanced Gate Stacks Using Combinatorial Methodology,"* submit to Appl. Phys. Lett. 2010.

K.-S. Chang, M. L. Green, I. Levin, J. R. Hattrick-Simpers, C. Jaye, D. A. Fischer, I. Takeuchi, and S. De Gendt, *"Physical and Chemical Characterization of Combinatorial Metal Gate Electrode Ta-C-N Library Film,"* accepted for publication in Appl. Phys. Lett. (2010).

J. L. Klamo, P. K. Schenck, P.G. Burke, K.-S. Chang, and M. L. Green, *"Manipulation of The Crystallinity Boundary of Pulsed Laser Deposited High-k HfO_2-TiO_2-Y_2O_3 Combinatorial Thin Films,"* J. Appl. Phys. 107 (2010), 054101.

M. L. Green, P. K. Schenck, K.-S. Chang, and J. L. Ruglovsky, and M. Vaudin, *""Higher-κ" dielectrics for advanced silicon microelectronic devices: A combinatorial research study,"* Microelectronic Engineering 86 (2009), 1662.

M. Otani, E. L. Thomas, W. Wong-Ng, P. K. Schenck, K.-S. Chang, N. D. Lowhorn, M. L. Green, and H. Ohguchi, *"A High-Throughput Screening System for Thermoelectric Material Exploration Based on a Combinatorial Film Approach,"* Japanese J. of Applied Physics 48, 05EB02 (2009).

Talk

"(Ta,Al)N Metal Gate and HfO_2-TiO_2-$Y2O_3$ High-k Dielectrics for the Advanced Gate Stacks Using Combinatorial Methodology," K.-S. Chang, National Tsing Hwa University, Hsinchu, Taiwan, 2010 (invited).

"Exploration of Metal Gate and High-k Dielectrics for the Advanced Gate Stacks Using Combinatorial Methodology," K.-S. Chang, National Cheng Kung University, Tainan, Taiwan, 2010 (invited).

"Exploration of Higher-k Dielectrics for the Advanced Gate Stacks Using Combinatorial Pulsed Laser Deposition," M. L. Green, Spring MRS, 2010.

"Exploration of the Ta(C,N)x/HfO_2 Advanced Gate Stack Using Combinatorial Methodology," K.-S. Chang, Spring MRS 2009.

Modeling of Graphene: Beyond-CMOS Devices

Technical Contacts:
M. Green

Goals

The goals of this project are to develop computational methods and software to enable rapid characterization of the structure and quality of graphene, thereby allowing the microelectronics industry to more rapidly realize the potential of graphene as a material for advanced device applications.

Customer Needs

Graphene, a single two-dimensional layer of graphite (carbon, C), has remarkable electronic properties such as high carrier mobility and a novel "pseudospin" degree of freedom. The ITRS Emerging Device Materials Working Group has recently "promoted" graphene to "a material of great interest" for beyond-CMOS technologies, thus targeting it for an enhanced level of funding. Many challenges must be solved, however, before graphene can be commercialized. One major challenge is finding a method for rapid, reproducible growth of high quality graphene. Methods under investigation include the thermal desorption of Si from SiC surfaces; thermal treatment of metal-rich metal carbides with a metal surface commensurate with graphene, and solution-based organic chemical processing. Using the case of graphene growth from SiC as an example, the samples obtained have varying numbers of graphene layers, and various defects within the layers, which can potentially affect device performance. Some graphene defects might be desirable, for example, to control electronic states associated with edges in graphene ribbons, or to bond graphene to a dielectric layers in a pseudospin graphene/dielectric/graphene multilayer structure.

At the recent 2009 Frontiers of Characterization and Metrology for Nanoelectronics (Albany, 5/09) Conference, several relevant measurement needs associated with graphene quality were repeatedly identified: i) measurement of the number of graphene layers present in a sample, ii) measurement of the misorientation between successive graphene layers, iii) measurement of the fluctuations of a graphene structure from ideal planarity, and iv) characterization of defects in graphene. As the performance of graphene-based devices depend very sensitively on their structure, atomic level calculations and models are needed to predict device performance. Not only can modeling lead to the level of understanding necessary for proper device performance, but also it can cut development costs by eliminating inappropriate materials and process schemes.

Technical Strategy

To characterize the structure, growth, and measurable properties of graphene and graphene-dielectric interfaces, this project relies on a range of theoretical and computational methods from ab-initio electronic structure calculations to large scale molecular dynamics simulations. Defects are studied using density functional theory, by relaxing atomic positions of graphene structures with variously introduced defects (e.g., adatom, substitution, vacancies, etc.). The electronic structures (density of states and nature of states at the Fermi level) are simultaneously calculated. By projecting the electronic density of states both spatially and into an energy range, it is possible to simulate scanning tunneling microscope (STM) topograhic images. This is important because symmetry alone is not sufficient to identify a defect from the images; electronic information, and separating electronic information from pure topographic effects is crucial. Additional measurement needs will be addressed by investigating the effects of graphene bilayer relative orientations on their transport properties, and by calculating theoretical Raman spectra for defected graphene structures.

In a similar way, graphene/dielectric interfaces can be modeled, and the effects of graphene defects on the graphene/dielectric interface can be compared to results for perfect graphene. The electronic structure will be determined in each case, and the results will be used as inputs into models for the pseudospintronic states of a graphene bilayer, with the goal of finding a graphene/high-κ dielectric interface suitable for such devices.

Further, experiments have demonstrated that whereas graphene multilayers (technically not graphene at all, but graphite) may result from thermal decomposition of SiC substrate sur-

faces, it is not possible to consistently grow large areas that comprise only a single layer. Also, the growth process is very much influenced by whether the decomposing SiC surface was Si- or C-terminated. The effects of temperature, surface termination, and surface misorientation on the formation of graphene by SiC decomposition will be modeled using molecular dynamics, with the aim of determining conditions favorable for the growth of a large area single monolayer. This is a challenging goal, as it will require the creation of appropriate interatomic potentials for a system with two different atomic species that can be bonded in both 4-fold and 3-fold arrangements.

DELIVERABLES:

- Analyze computed electronic structure of a graphene/Mo atom/graphene sandwich and simulated STM images of said defect. (Q1 10)
- Create software to calculate density of states in graphene (with and without defects) via interpolation scheme. Simulate electronic structure and STM images of single and multiple intercalated metal defects in a 20nm-sized simulation cell (Q2 10)
- Calculate phonon spectra in multilayer graphene as a function of interlayer orientation. Use molecular dynamics (MD) to study desorption of graphene from SiC. (Q3 10)
- Work with NIST and external collaborators to determine a new measurement need(s) for graphene that can be addressed via computational materials science. (Q4 10)

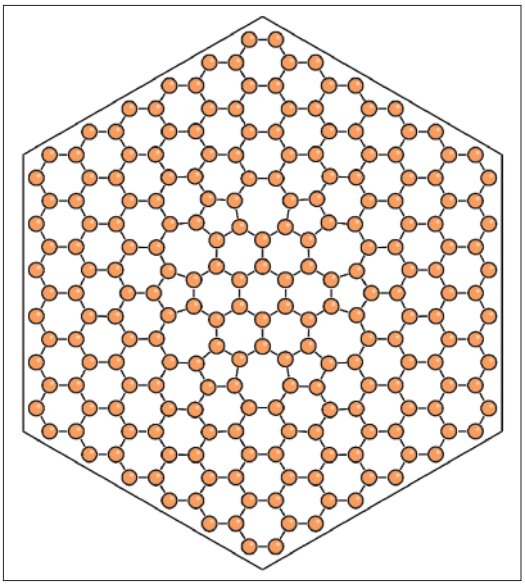

Figure 1. Rotational defect in graphene. The central region of 24 C atoms is rotated.

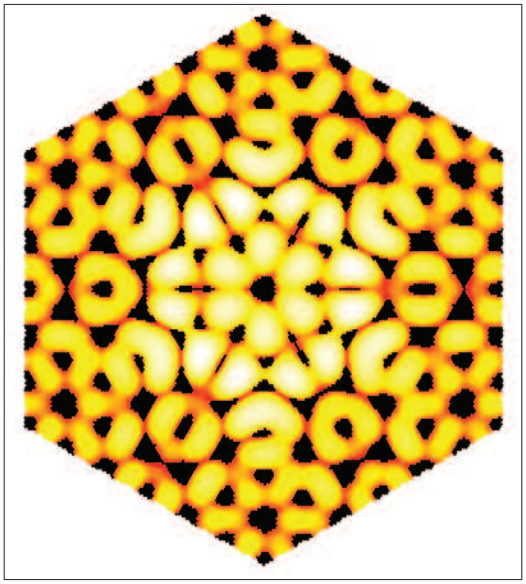

Figure 2. Simulated STM image of the defect shown in Fig. 1

Accomplishments

■ The following three defects in graphene have been identified as having the lowest energies: (1) a Stone-Wales defect (twisted C-C bond generating two pentagons and two heptagons), (2) a rotational defect where the central region of 24 C atoms is rotated, generating six pentagons and six heptagons (Fig. 1), and (3) a C vacancy. Each defect was fully relaxed in both monolayer and bilayer graphene. The STM images corresponding to each defect were simulated. The simulated STM image for the rotational defect (Fig. 2) exhibits all of the features (e.g. dark spokes) observed in experimental images of a common high-symmetry defect of graphene grown on the Si-terminated surface of SiC [Rutter et al., Science 317, 219 (2007)], and is tentatively identified as the origin of this experimental feature.

First-principles calculations of electronic structure are limited to periodic structures with up to hundreds of atoms. This is inadequate to avoid spurious defect-defect interactions that quantitatively affect the results. Therefore, first-principles electronic structure calculations were used to parameterize a tight-bonding model. These parameters are transferable, and the model allows the calculation of the electronic structure of unit cells with thousands of atoms. Fig. 3 shows the predicted electronic structure produced by intercalation of a Mo in bilayer graphene. The detailed quantitative spatial and energy resolution of the simulation allows for more certain identification

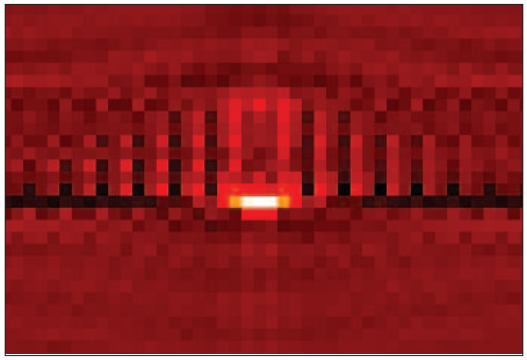

Figure 3. Simulated weighted electronic density of states versus position and energy for a Mo intercalation in bilayer graphene. The data has been binned into pixels that span 0.12 nm in distance (horizontal in figure; defect at center) and 0.1 eV in energy (vertical in figure; Dirac level at center).

of experimental defects. For example, comparison with experimental results allowed us to reject the hypothesis that the experimental high-symmetry defect in graphene is due to Mo intercalation. A similar calculation for the rotational defect, mentioned above, is in progress.

Raman spectra have been calculated for single and multilayer graphene. The frequencies depend on the number of layers, the orientation between layers, and the nature of the stacking. Such results demonstrate the usefulness of graphene as a nondestructive tool for measuring the structure of multilayer graphene. Interatomic potentials for SiC systems were found in the literature. These potentials will allow for molecular dynamics simulation of graphene growth on SiC.

Collaborations

Dr. K.J. Cho, U. Texas Dallas

Drs. J. Stroscio and G. Rutter, NIST

Publications

Eric Cockayne, Gregory M. Rutter, and Joseph A. Stroscio, *"Density Functional Theory Studies of Defects in Graphene"*, 2009 Frontiers of Characterization and Metrology for Nanoelectronics Conference, Albany, NY, May 2009.

Eric Cockayne, Gregory M. Rutter, and Joseph A. Stroscio, *"Characterization of a Single Metal Impurity in Graphene"*, MRS Spring Meeting 2010, San Francisco, CA, April 2010.

Eric Cockayne, Gregory M. Rutter, and Joseph A. Stroscio, *"Characterization of a Single Metal Impurity in Graphene"*, 217th ECS Meeting, Vancouver, BC, Canada, April 2010.

Eric Cockayne, *"Characterization of Impurities in Bilayer Graphene"*, ECS Transactions 28, 87 (2010).

Stress Mapping using Confocal Raman Microscopy and Electron Back-Scatter Diffraction

Technical Contacts:
Robert F. Cook

Goals

Develop the measurement techniques and standards for quantitative nano-scale determination of deformation, strain, and stress that will enable "stress engineering" of microelectronic and microelectromechanical devices.

Customer Needs

Many advanced industries require accurate and precise measurements of the state of deformation, or of strain or stress, in materials in order to improve or control device performance. For example the microelectromechanical systems (MEMS) industry requires knowledge of stress in components in order to optimize the sensitivity of pressure sensors, the output power of energy harvesters, and the reliability of moving components. The semiconductor microelectronics industry has implemented stress-engineered channel structures with increased carrier mobility in field-effect transistors, thereby obviating the need for costly development of new materials sets to improve device performance. Stress engineering of channels was introduced at the 90 nm semiconductor technology node and is expected to play an increasing role in enhancing transistor performance out to the 22 nm node. The optoelectronics industry takes advantage of substrate effects on photonic quantum-well structures to generate differences in strain states and thus changes in the output color and lifetime of visible light-emitting and laser diodes. All of these industries use many different methods to measure deformation and of strain or stress, with little to no reconciliation between measurement methods, and no easy way of verifying the accuracy of measurements on components either on the manufacturing line or in development laboratories.

Technical Strategy

This project will develop measurement methods and standards to enable deformation, strain, and stress measurements to be performed at the nanoscale. Attention will focus on developing techniques for a range of instruments that could be used to make such measurements in the MEMS and microelectronics industries and on obtaining agreement between such instruments and measurements. A particular focus will be the development of strain measurements using electron back scatter diffraction (EBSD) measurements in the scanning electron microscope and stress measurements inferred from shifts or broadening of peaks in Raman spectroscopy using confocal Raman microscopy (CRM).

Mapping of strain and stress distributions is a goal for both techniques and the techniques are complementary: EBSD is surface-localized with about 10 nm (lateral) spatial resolution and requires ultra-high vacuum; CRM provides depth sampling with about 100 nm spatial resolution and operates under ambient conditions. Both techniques have better than 10^{-4} strain resolution (20 MPa stress in Si). These capabilities are unique to NIST. Stress mapping with both techniques is data intensive and a dedicated high performance computer (HPC) cluster will be installed for analysis of EBSD data in particular; a focus here will the parallel implementation of the CrossCourt software to greatly increase mapping speed and accuracy. In addition, the HPC will be used for parallel implementation of finite element analysis (FEA) software to compare models and measurements of stress distributions and to enable tensor stress mapping by CRM.

In addition, a reference material (RM) will be developed based on these and other measurements. Specifically, the RM will allow calibration of instruments that infer film stress from wafer curvature measurements, strain from EBSD measurements or X-ray diffraction (XRD) measurements, or CRM measurements. The RM will be based on the reaction stresses generated in a strain mismatched Si(1−x)Gex epitaxial layer deposited on Si substrates. The target composition of the Si(1−x)Gex layer will be $x \approx 0.2$ and the target thickness will be less than 200 nm, leading to ≈ 1 GPa stress in the layer and < 10 MPa stress in a 700 μm thick Si substrate. Such a film will exhibit great temporal stability as the film thickness is less than that required to initiate misfit dislocations.

Finally, traceability of the stress measurement techniques will be achieved by comparison of deformation inferred from EBSD measurements and direct measurement of deformation by atomic force microscopy (AFM) and X-ray diffraction

(XRD). AFM measurements can be traced to standard reference material dimensional artifacts. Thus a measurement transfer chain of AFM-EBSD-CRM that establishes the accuracy of the techniques will be established. XRD measurements can also be traced to standard reference material lattice artifacts. A second, independent, transfer chain of XRD-EBSD-CRM will also be established.

DELIVERABLES

- Backside etch, verify etch, measure curvature on SiGe-Si development wafers. 4Q2008
- Define requirements for implementing CrossCourt EBSD analysis on new HPC cluster. 4Q2008
- Complete CRM, EBSD, and AFM measurements and modeling on new wedge indentation test structure. 4Q2008
- Complete lithography and dicing on SiGe-Si wafers, perform initial die curvature measurements. 1Q2009
- Perform initial CRM and EBSD measurements on development die. 1Q2009
- Bring HPC cluster up. 1Q2009
- Validate EBSD stress mapping; Validate CRM stress tensor mapping. 2Q2009
- Bring CrossCourt up on HPC. 2Q2009
- Revisit ISMI SiGe test structures 3Q2009
- Design RM 8190 and RM 8191 structures. 3Q2009

ACCOMPLISHMENTS

Quantitative agreement was demonstrated between EBSD, CRM, and AFM stress and deformation measurements on a test vehicle with a simple stress distribution: a linear wedge indentation in Si. A rendered CRM stress map of the indentation is shown in Fig. 1 below. Near the center of the indentation, the deformation state is almost-pure compressive plane-strain and near the ends of the indentation tensile stresses are associated with crack tips.

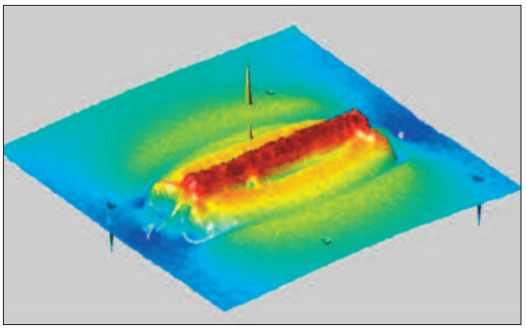

Figure 1. Confocal Raman microscopy stress map of a 20 μm long wedge indentation in Si. Red indicates compression and blue indicates tension.

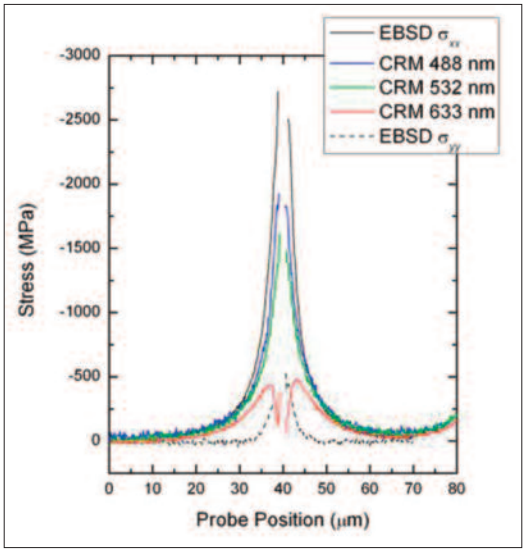

Figure 2. Comparison of stress measurements by confocal Raman microscopy and electron back scatter diffraction adjacent to a wedge indentation in Si.

The simple deformation state enables CRM measurements to be interpreted simply as uniaxial stress and thus compared directly with EBSD measurements. CRM line scans across the indentation using different laser excitation wavelengths enable stress measurements that sample different information volumes—smaller wavelength excitation provides greater surface sensitivity. Such scans are shown in Fig. 2 below and compared with a similar EBSD scan. The agreement between the σxx stress measurements for the most surface sensitive excitation (488 nm) with the EBSD is obvious and is the first such experimental demonstration of the agreement between these techniques. Measurements with the least surface sensitive excitation (633 nm) did not agree with the EBSD measurements near the indentation, and in fact suggests detection of sub-surface cracking.

Additional experiments using AFM to measure the surface topography adjacent to the indentation showed agreement with EBSD measurements of local rotation, also an experimental first. CRM measurements have been refined using an even more surface sensitive excitation source (405 nm laser) and show excellent agreement with full stress tensor EBSD measurements.

Quantitative cross-platform agreement between EBSD, CRM, curvature, and XRD measurements has been demonstrated on a SiGe-Si blanket thin-film test structure in both wafer and die form; XRD curvature measurements have now been refined to generate uncertainties less than 0.3 %. Such agreement demonstrates that the structure is suitable as an RM, and prototype SiGe-Si and SiO2-Si wafers have been fabricated for RM development and lithography of test structures is under way. The curvature measurements are performed using the Ultratech coherent gradient spectroscopy technique and RM development is in collaboration with Ultratech.

EBSD and CRM techniques have been applied to SiGe and W test structures supplied by Sematech and Freescale Semiconductor to assess the ability of methods to measure the stress states of patterned structures with complex deformation states. Agreement between the CRM measurments and FEA models of the full stress tensor has been demonstrated. Such agreement is required for RM development. A specially-designed fixture for EBSD and CRM mapping of loaded test vehicles with known complex stress states has been developed.

Collaborations

Joint wafer- and die-scale deformation, strain, and stress standards development with Ultratech. Joint strain and stress mapping experiments on device test structures with Sematech and Freescale Semiconductor.

Recent Publications

1. *"Stress-Intensity Factor and Toughness Measurement at the Nanoscale using Confocal Raman Microscopy,"* R.F. Cook, Y.B. Gerbig, J. Schoenmaker, and S.J. Stranick, 12th International Conference on Fracture Conference Proceedings, Ottawa, Canada, July, 2009

2. *"Nanomechanical Measurements and Tools,"* R.F. Cook, Nanotechnology Thought Leaders, A to Z of Nanotechnology, www.azonano.com (2010)

Talks

1. *"Stress-Intensity Factor and Toughness Measurement at the Nanoscale using Confocal Raman Microscopy,"* R.F. Cook, Y.B. Gerbig, J. Schoenmaker, S.J. Stranick, 12th International Conference on Fracture, Ottawa, July 2009.

2. *"High Resolution Surface Morphology Measurements using EBSD Cross-Correlation Techniques and AFM,"* M.D. Vaudin, G. Stan, Y.B. Gerbig and R.F. Cook, Microscopy and Microanalysis 2009, Richmond, VA, July, 2009

3. *"Measuring and Mapping Mechanical Properties with Nano-Scale Resolution,"* R.F. Cook, MRS Fall Meeting, Boston, MA, December, 2009.

Interconnect and Packaging Metrology Program

Advances in interconnect and packaging technologies have introduced rapid successions of new materials and processes. A major new technology thrust over the past several years is the move to three dimensional integration. Environmental pressures have led to the reduction and elimination of lead in solder used for attaching chips to packages and packages to circuit boards. The overall task of this program is to provide critical metrology and methodology for mechanical, chemical, metallurgical, electrical, thermal, and reliability evaluations of interconnect and packaging technologies.

The function of packaging is to connect the integrated circuit to the system or subsystem platform, such as circuit board, and to protect the integrated circuit from the environment. The increasing number of input/output (I/O) on circuits with vastly larger scale of integration is forcing ever smaller I/O pitches, the stacking of chips with via hole interconnect, the use of flip chip bonding, and the use of intermediary platforms called interposers. The integration of sensors and actuators onto integrated circuits through MEMS technology and the increasing use of low cost integrated circuits in harsh environments is increasing the complexity of the packaging task. Environmental concerns are forcing the need for development of reliable lead-free solder and other low environmental impact packaging materials. System reliability requirements demand modeling, testing methods, and failure analysis of the integrated circuits before and after packaging. Metrology is a significant component of reliability evaluation.

Atomic Layer Deposition – Process Models and Metrology

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Goals

Develop validated, predictive process models and in situ metrologies for atomic layer deposition processes.

Customer Needs

Atomic layer deposition (ALD) is increasingly being utilized as a method of depositing the thin (nanometer-scale), conformal layers required for many microelectronics applications, including high-κ gate dielectric layers and DRAM dielectric layers. However, significant developmental issues remain for many of these applications. A tool that can potentially help to solve some of these developmental issues is technology computer-aided design (TCAD). TCAD has been identified in the *International Technology Roadmap for Semiconductors (ITRS) 2009 Edition as "one of the few enabling methodologies that can reduce development cycle times and costs."* [ITRS 2009 Edition, Modeling and Simulation, page 1] A TCAD topical area identified in the ITRS 2009 Edition is *"Equipment/feature scale modeling—hierarchy of models that allows the simulation of the local influence of the equipment (except lithography) on each point on the wafer, starting from the equipment geometry and settings."* [ITRS 2009 Edition, Modeling and Simulation, page 1] A difficult challenge related to this topical area is *"Integrated modeling of equipment, materials, feature scale processes and influences on devices, including variability"* [ITRS 2009 Edition, Modeling and Simulation, Table MS1, page 3] with associated issues including *"Fundamental physical data (e.g., rate constants, cross sections, surface chemistry for ULK, photoresists and high-κ metal gate); reaction mechanisms (reaction paths and (by-)products, rates ...), and simplified but physical models for complex chemistry and plasma reaction"* and ALD deposition modeling.[ITRS 2009 Edition, Modeling and Simulation, Table MS1, page 3] In addition, the 2009 ITRS notes that *"a key difficult challenge present across all the modeling areas is that of experimental validation."* [ITRS 2009 Edition, Modeling and Simulation, page 2] Further, with respect to experimental validation, *"One of the major efforts required for better model validation is sensor development and metrology, especially for models predicting the fabrication and behavior of ultra-thin films and ultra-fine structures."* [ITRS 2009 Edition, Modeling and Simulation, page 8] This project is an attempt to assist in solving some ALD developmental issues by developing validated, predictive process models and in situ metrologies for ALD processes.

Technical Strategy

This project involves two general directions of investigation: development of in situ metrologies sensitive to ALD chemistry and development of ALD chemical reaction mechanisms. These two directions are seen as mutually-supportive. It is expected that experimental results that elucidate ALD chemistry will aid in chemical mechanism development and ultimately in process model validation. Further, it is expected that important reaction species will be identified as the understanding of a particular ALD reaction improves, thus facilitating the design of improved process metrologies. While these two directions will be closely coupled for development of a specific ALD chemical reaction mechanism, it will not preclude exploration of non-mutually-supporting aspects of the metrology development and model development directions. For example, fundamental thermochemical and chemical kinetics properties of numerous organometallic compounds potentially suitable for ALD are under investigation. However, it would not be feasible to simultaneously provide experimentally validated ALD process models for all compounds.

Various in situ diagnostics are being evaluated for use in characterizing gas phase and/or surface processes. Gas phase diagnostic development has focused on metrologies that are sensitive to gas phase processes that can be ultimately related to film properties. Such diagnostics can be used to help optimize gas injection conditions rather than simply monitor precursor delivery. ALD process models are being developed by incorporating the detailed chemical reaction mechanisms developed in the course of this project into commercially available computational fluid dynamics (CFD) codes that simulate the gas flow and temperature fields in an ALD reactor. Experimental validation of the overall process model is accomplished by mod-

eling the performance of a custom-built, research-grade ALD reactor with optimized optical accessibility and benchmarking the numerical results with experimental data. HfO2 ALD using tetrakis(ethylmethylamino) hafnium (TEMAH) and water has been selected as the chemical system for primary investigation.

1. A number of diagnostics are being evaluated for sensitivity to ALD chemistry and integration into deposition systems. Mass spectrometry and optical spectroscopic techniques are of particular interest because of their proven utility for in situ monitoring. While sensors that are sensitive to gas phase species, e.g., mass spectrometry and semiconductor laser-based spectroscopic techniques, are more straightforward to integrate into commercial reactors (e.g., in the gas exhaust line), these techniques can only be used to detect volatile species. Hence, it is sometimes difficult to relate the species detected with such techniques to the mechanisms of interest on the growth surface. Hence, both gas-phase-sensitive and surface-sensitive techniques are being evaluated to probe ALD chemistry. The emphasis of these investigations is on development of techniques with high temporal and spatial resolution and the utilization of these techniques to perform in situ measurements during actual deposition processes. The techniques being utilized for investigations of gas phase processes include time-resolved Fourier-Transform infrared (FTIR) spectroscopy, laser-based spectroscopic absorption techniques, bandpass filter-based mid-infrared absorption techniques, and mass spectrometry. The techniques being utilized for investigations of surface processes include time-resolved reflection-absorption IR spectroscopy (RAIRS) and bandpass filter-based mid-infrared absorption techniques. Measurements are preformed in a custom-built, research-grade ALD reactor with optimized accessibility for the various gas-phase-sensitive and surface-sensitive techniques.

DELIVERABLES:

- Evaluation of bandpass filter-based mid-infrared absorption techniques for measuring alkyl amine deposition product concentrations during ALD. 3Q 2010
- Evaluation of bandpass filter-based mid-infrared absorption techniques for measuringTEMAH concentrations during ALD. 3Q 2010
- Evaluation of bandpass filter-based mid-infrared absorption techniques for measuring surface alky-group functionalization during ALD. 4Q 2010

2. The calculation, estimation, and dissemination of fundamental thermochemical and chemical kinetic properties of organometallic compounds with potential application to ALD are an integral aspect of this project. The thermochemical properties and reaction kinetics of most organometallic precursors employed in ALD are poorly characterized. This project obtains these properties through theoretical estimates, comparison with available experimental data, and modeling. This involves compiling the available thermochemical and chemical kinetics data for organometallic precursors and related compounds. These data are supplemented with predictions from quantum calculations of molecular structures, spectroscopic properties, and thermodynamic functions. These quantities are then utilized to develop detailed chemical kinetics models for the decomposition of organometallic precursors and deposition processes leading to thin film growth.

DELIVERABLES:

- Correlate simulated time-resolved non-reacting species concentrations with measured non-reacting species concentrations to validate gas flow models. 3Q2010
- Correlate simulated time-resolved reacting species concentrations with measured reacting species concentrations to validate ALD deposition models. 4Q2010

3. An effort is also being made to investigate the relationship between ALD reactor conditions and concomitant HfO_2 film properties. This relationship is being investigated by correlating the results of a variety of ex situ film characterization measurements to reactor conditions as determined by in situ measurements and numerical modeling of the temperature and flow fields in the reactor. In situ measurement techniques include those techniques being developed for model validation. Ex situ measurement techniques include vacuum ultraviolet spectroscopic ellipsometry (VUV-SE), FTIR spectroscopy, X-ray photoelectron spectroscopy (XPS), X-ray diffractometry, atomic force microscopy, ultraviolet Raman spectroscopy, and various electrical measurements. The data provided by these measurements, spatially resolved when possible, include such film characteristics as thickness, stoichiometry, HfO_2 phases present, degree and type of impurity incorporation, leakage current, and dielectric constant.

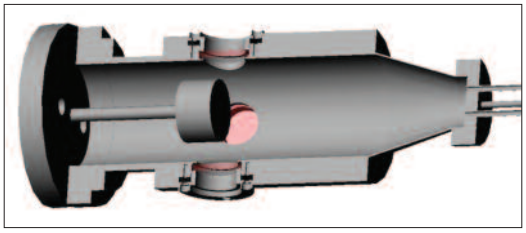

Figure 1. A schematic of the cross section of the reactor as configured with optical windows.

DELIVERABLES:

- Investigate the relationship between HfO_2 ALD process parameters, reactor gas flow and temperature fields, gas phase species identities and concentrations, and resulting ALD film characteristics. Ongoing

Accomplishments

■ ALD Reactor Design — An ALD reactor with diagnostic access near the wafer surface that exhibits operational parameters approximating some industrial single wafer reactors was designed and fabricated. Gas flow in the reactor near the wafer is laminar and parallel to the wafer surface normal with four diagnostic ports oriented perpendicular to the wafer surface normal, as shown in Fig. 1.

Diagnostic access does not significantly perturb gas flow, especially near the wafer surface. Using this reactor, reproducible, high-quality HfO_2 films can be deposited at the same time that in situ measurements are being performed. This reactor is being used to provide data to validate process models and develop metrologies.

■ Hafnium Oxide Film Deposition — ALD HfO_2 films are being deposited under a variety of process conditions using tetrakis(ethylmethylamino) hafnium (TEMAH) and water. Films have been characterized with a number of techniques, including VUV-SE, XPS, FTIR, Raman spectroscopy, X-ray diffractometry, atomic force microscopy, and current-voltage measurements. Ex situ measurement results indicate that this reactor design can be used to reproducibly grow microelectronics-quality HfO_2 films.

■ *In-Situ* Gas Phase Measurements — *In-situ* gas phase FTIR measurements have been performed during HfO_2 film deposition and have been shown to be sensitive to the major gas-phase deposition reactants, TEMAH and water, and the product, methylethylamine.

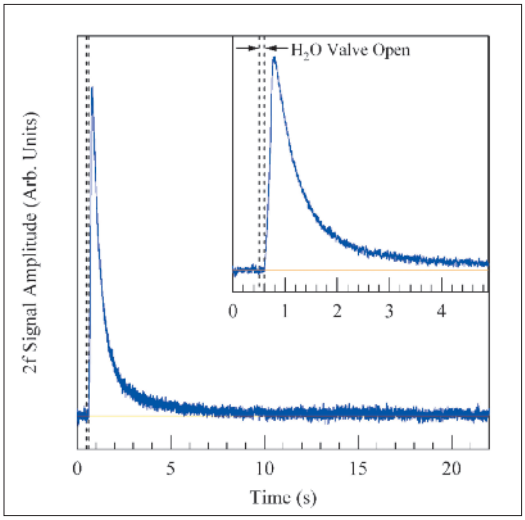

Figure 2. Near-IR diode laser-based water vapor absorption measurements.

In-situ, time-resolved semiconductor laser-based absorption measurements have also been developed to detect all major gas phase species. These techniques have proved particularly sensitive to the deposition reactants. Water vapor absorption was measured in the near-IR spectral region using a distributed feedback diode laser and wavelength modulation spectroscopy, as shown in Fig. 2. TEMAH was measured in the mid-IR spectral region using a quantum cascade laser and amplitude modulation spectroscopy, as shown in Fig. 3.

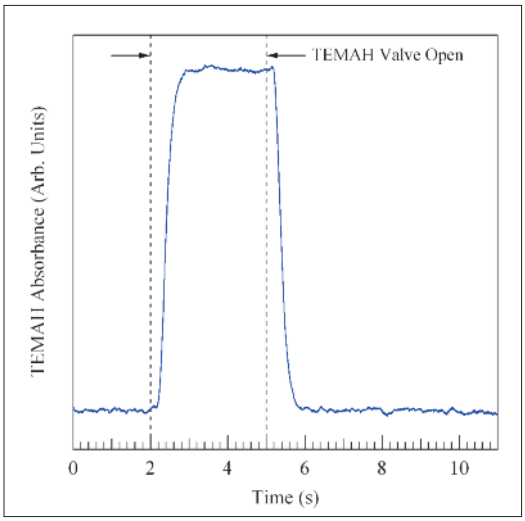

Figure 3. Mid-IR quantum cascade laser-based TEMAH absorption measurements.

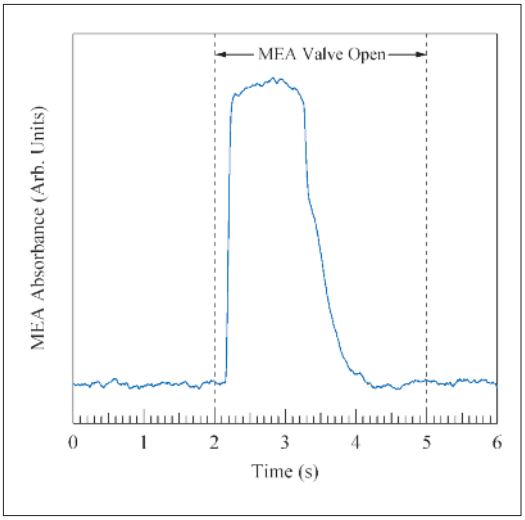

Figure 4. Mid-IR bandpass filter-based methylethylamine absorption measurements.

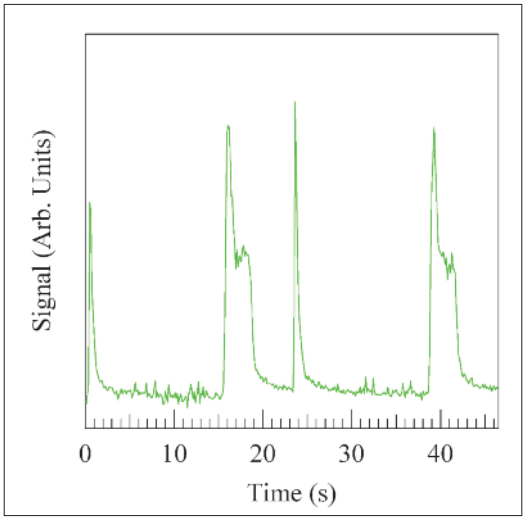

Figure 5. Mass spectrometric measurement of mass-to-charge ratio representative of methylethylamine during ALD cycle.

In-situ, time-resolved bandpass filter-based mid-infrared absorption techniques have also been developed to detect all major gas phase species. These techniques have been found to be more sensitive to alkyl amine deposition products than laser-based measurements. Methylethylamine was measured in the mid-IR spectral region using a broadband infrared source, a bandpass filter, and amplitude modulation spectroscopy, as shown in Fig. 4.

In addition to optical measurements, a quadrupole mass spectrometer has also been used to monitor volatile species present during ALD, including methylethylamine as illustrated in Fig. 5.

■ In-Situ Surface Measurements — *In-situ* surface RAIRS measurements have been performed during HfO_2 film deposition and have been shown to be sensitive to surface functionalization occurring during the ALD process, as shown in Fig. 6, as well as potential impurity-incorporation reactions.

■ ALD Reactor Modeling — Gas flow and temperature profiles in this reactor have been simulated using three dimensional CFD modeling, as shown in Fig. 7. (Please insert Fig. 7 here - see caption below- same as last year) In addition, time-resolved precursor distributions have been modeled. The results from these models have been used to help optimize reactor designs (especially optical window design) and deposition conditions, as well as interpret in-situ measurements.

■ ALD Reaction Mechanism Development — A chemical reaction mechanism describing ALD of HfO_2 from water and TEMAH has been developed and is being refined. A schematic of this mechanism is illustrated in Fig. 8. This mechanism has been used with the three dimensional flow and temperature models to simulate the entire ALD process.

■ ALD Process Model Validation — Initial ALD process model validation has begun by comparing normalized spatially- and temporally-resolved simulated and measured gas phase species distributions, as shown in Fig. 9. (Please insert Fig. 9 here - see caption below - New Figure) Simulations and measurements for distributions of all major gas phase species are being compared under non-reacting and actual deposition conditions.

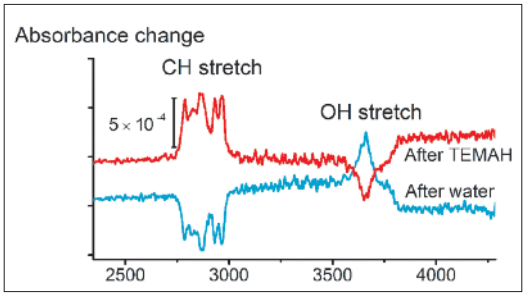

Figure 6. RAIRS spectra during ALD cycles.

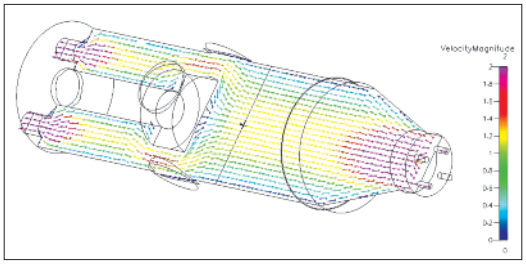

Figure 7. A cross section of the helium carrier gas velocity distribution in the diagnostic-accessible reactor under typical deposition conditions (obtained from a full three dimensional simulation)

■ Chemical Properties Calculations — Molecular structures, vibrational frequencies, and energies for precursors, intermediates, and products have been calculated using quantum chemical methods for ALD of HfO_2 from TEMAH/tetrakis (dimethylamino) hafnium (TDMAH) and water. Comparisons are made between the calculated predictions and experimental data to develop reliable and self-consistent values. A detailed chemical kinetics model for ALD of HfO_2 from TEMAH and water has been developed and is being further refined using reactor model simulations and by comparison with experimental observables.

■ Reference Spectra Development — Reference spectra of TEMAH, methylethylamine, dimethylamine, and diethylamine were recorded in the near-IR and mid-IR spectral regions. The measured mid-IR vibrational frequencies were compared to vibrational frequencies that were calculated with hybrid density function theory. Near-IR spectra are necessary to design semiconductor laser-based spectroscopic techniques utilizing relatively inexpensive telecommunications lasers. Methylethylamine, dimethylamine, and diethylamine spectra are useful as these amines are the primary volatile deposition products of many ALD processes involving alkylamido compounds, e.g., TEMAH and tetrakis(dimethylamido) titanium. This is especially the case for thermal ALD of oxides employing water or nitrides employing ammonia.

■ Database Website — A Website http://kinetics.nist.gov/CKMech has been made available. This site contains bibliographic and thermochemical information for organometallic and other compounds important in semiconductor deposition processes, including organometallic compounds containing hafnium and aluminum.

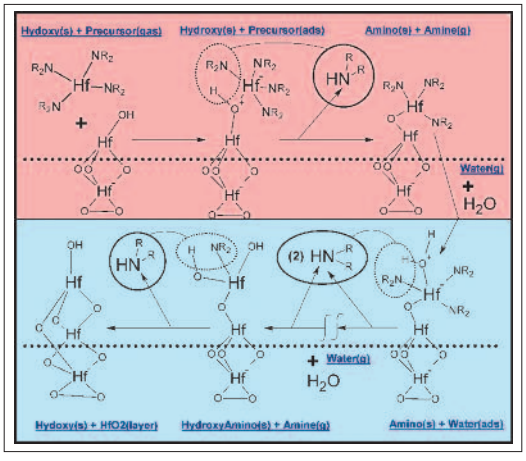

Figure 8. Schematic of HfO_2 ALD chemical mechanism.

Publications

B. A. Sperling, W. A. Kimes, J. E. Maslar, and P. M. Chu, *"Time-resolved Fourier transform spectroscopy of the gas phase during atomic layer deposition,"* Journal of Vacuum Science and Technology A, submitted (2010).

B. A. Sperling, W. A. Kimes, and J. E. Maslar, *"Reflection absorption infrared spectroscopy during atomic layer deposition of HfO_2 films from tetrakis(ethylmethylamido)hafnium and water,"* Applies Surface Science 256, 5035-5041 (2010).

E. J. Heilweil, J. E. Maslar, W. A. Kimes, N. D. Bassim, and P. K. Schenck, *"Characterization of metal oxide nanofilm morphologies and composition by terahertz transmission spectroscopy,"* Optics Letters 34, 1360-1362 (2009).

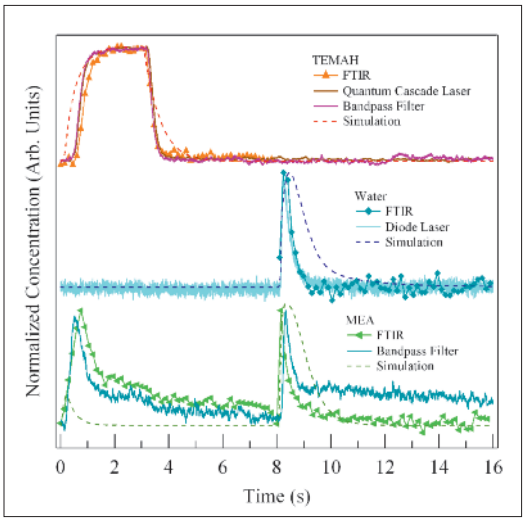

Figure 9. A comparison of normalized simulated and measured gas phase species distributions.

J. E. Maslar, W. S. Hurst, D. R. Burgess, W. A. Kimes, N. V. Nguyen, E. F. Moore, and J. T. Hodges, *"In Situ Gas Phase Diagnostics for Hafnium Oxide Atomic Layer Deposition,"* ECS Transactions 13, 139-149 (2008).

N. V. Nguyen, O. A. Kirillov, W. Jiang, J. E. Maslar, W. A. Kimes, and J. S. Suehle, *"Interface Barrier Determination by Internal Photoemission: Applications to Metal/Oxide/Semiconductor Structure,"* ECS Transactions 13, 161-167 (2008).

Advanced Nanoscale and Mesoscale Interconnects

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D. Josell

Goals

This project is developing solutions to metrology issues confronting integrated circuit manufacturers in the area of interconnect metallization. Present efforts include determining the essential process requirements for superconformal fabrication of high aspect ratio, low resistivity metallizations for both on-chip, chip stacking, and MEMS applications, examining the generality of the superconformal filling mechanism, expanding the applicable materials set, and exploring processes utilizing novel barriers and/or seed geometries. This is complemented by surface chemistry studies aimed at understanding and optimizing the feature-filling process.

Customer Needs

Increasing information technology requirements have yielded a strong demand for faster logic circuits and higher-density memory chips. The low electrical resistivity of copper and the ability of electrodeposition to "superconformally" fill high aspect ratio features has made electrodeposited copper the interconnect material of choice in silicon technology. However, the move to ever-smaller dimensions has led to the rise of new challenges, including fabrication of ever-thinner copper seeds, which are required for the copper superfill process and increased resistivities of the metallizations due to size effects. At the same time a strong movement towards 3-D integration of integrated circuits (i.e. chip stacking) is under way. This involves the replacement of long horizontal conductors by short vertical interconnections; in addition to an improved RC response, the new architecture enables integrations of heterogeneous devices. Many challenges to the fabrication through-silicon-vias (TSV) remain that require an understanding of the surface chemistry of copper. To help overcome these hurdles, the National Institute of Standards and Technology (NIST) is enhancing existing copper technology through improved understanding of the surface chemistry and metrologies for the superfill process, examining new interconnect materials, and pursuing new fabrication techniques such as seedless processing and atomic layer deposition. Similarly, there is also increasing interest in expanding the materials set available for constructing 3-D MEMS architectures. In this regard NIST has begun exploring the integration of ferromagnetic materials into Damascene processing.

Interconnect metallization issues are discussed in the Interconnect section of the 2008 update of the International Technology Roadmap for Semiconductors.

Technical Strategy

To meet future industrial needs, we have, over the life of this project, developed metrology and fully disclosed copper electrolytes that permit characterization of the ability of generic electrolytes to fill features over a wide range of length scales. The derived Curvature Enhanced Accelerator or Adsorbate Coverage (CEAC) mechanism has served as a platform for this understanding. A key element to bottom-up surperfilling is the competition between deposition rate suppressing polymers and rate accelerating sulfonated alkythiols (and/or disulfides) for surface sites. In the case of on-chip interconnects an important consequence of bottom-up superfilling is the overshoot phenomenon known as "momentum plating" that can lead to bump formation above filled features. These bumps greatly hamper subsequent planarization processes. However, the overshoot process may be controlled by the addition of certain cationic surfactants to the copper plating baths. In a related manner, cationic surfactants exert an even greater influence on the filling of larger scale TSV's geometries. We are using a variety of electroanalytical and feature-filling experiments that help establish strategies for quantifying and understanding the influence of surfactants on film growth over a range of length scales. Through this activity the CEAC model was successfully extended to explain and predict the filling behavior during deposition from complex plating baths containing combination of suppressors, accelerators, and levelers.

In parallel with this effort a variety of surface analytical studies, e.g. in-situ STM and XPS, are under way to directly probe the competitive adsorption dynamics between multiple additives and the copper surface in order to provide molecular level insight into additive function and

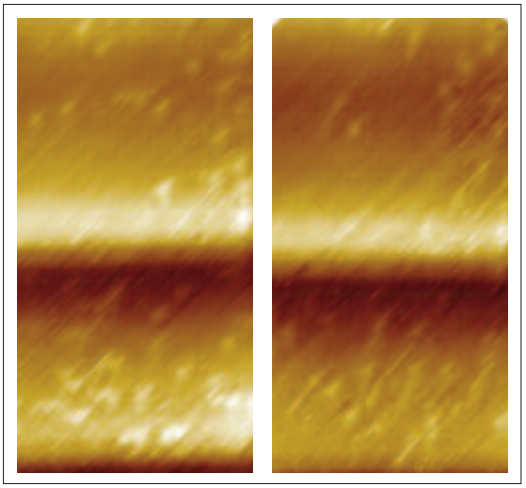

Figure 1a *Figure 1b*

Figure 1a and b. In situ STM images of the surface phase responsible for Cu superfilling. The accelerating sulfonated alkyl disulfide molecules rapidly diffuse as a lattice gas on top of the close packed square lattice of chloride ions, Cl-Cl separation is 0.36 nm, on a Cu (100) surface.)

design. Particular attention is given to the role of potential-dependent adsorption processes that are central to the performance of the copper-pulse plating method used to form TSVs. The competitive and co-adsorption of surfactants relevant to superfilling may be monitored and quantified by voltammetry. These studies are complemented by in-situ STM examinations of the surface structure and dynamics as shown in Fig 1. Close attention is being given to connecting the results of such single crystal studies with feature-filling experiments.

DELIVERABLES:

- Publications using surface and electroanalytical probes to independently quantify adsorbate coverage, and dynamics relevant to superconformal feature filling. 2Q 2010 and 4Q 2010.

The generality of the bottom-up superfilling process to the application of other material systems in ULSI and MEMS remains a subject of great interest. In addition to silver (the only metal with a higher conductivity than copper) and gold (a metallization for wide-bandgap semiconductors) the prospect for deposition of iron group metals (for MEMS and magnetoelectronic circuitry) has been examined. Most recently, a simple solution for integrating nickel, cobalt, nickel-iron and cobalt-iron alloys into the Damascene processing has been demonstrated. As shown in Fig. 2, the addition of a simple benzimidazole derivative to a cobalt-iron plating bath complete filling of trenches while limited deposition occurs on the neighboring free-surface. Most recently an extreme form of bottom-up filling, shown in Fig 3, has been developed based on selective modification of the trench side walls.

DELIVERABLES:

- Publications detailing the deposition of magnetic materials for Damascene metallization. 3Q 2010

In addition to the electrodeposited copper conductor itself, current metallization technology employs a barrier metal and a PVD copper seed. As feature sizes continue to shrink, the resistive barrier materials negatively impact electrical performance, and deposition of, and on, the PVD

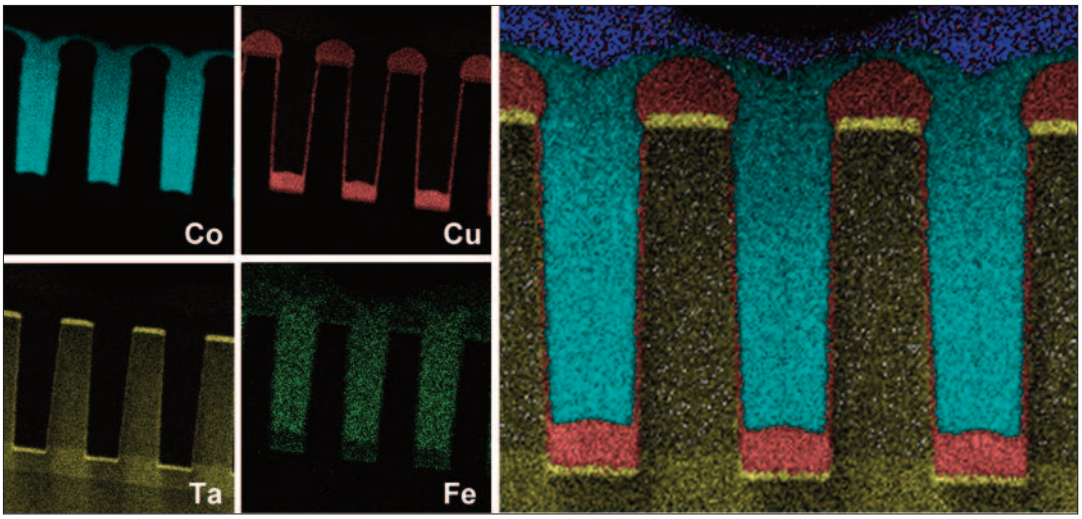

Figure 2, TEM-EDS image of superconformal elcetrodeposition of a Co-Fe alloy in a trench array.

seed becomes problematic. These difficulties are driving a search for alternative barrier/wetting layer materials and processes. Ruthenium is one focus because its electrical and thermal conductivities are approximately twice those of conventional tantalum barriers, it is immiscible with copper, and copper can be electroplated directly on it, eliminating the need for the PVD copper seed layer and the corrosion problems that come with it. In the past we have demonstrated direct copper superfilling on Ru, Os, and Ir barrier/adhesion seed layers as well as appropriate metrological aspects required for process control. This work continues with the evaluation of state-of-the-art ALD WN-Co4N novel barrier materials as shown in Fig 4.

Accomplishments

- Void-free superconformal deposition of nickel, cobalt, nickel-iron and cobalt-iron alloys demonstrated by the addition of benzimidazole derivatives or cationic polymers such as polyethyleneimine to the electrolyte. Filling proceeds by a new mechanism that involves transient breakdown of an inhibiting molecular layer that is coupled with the trench geometry in a manner that enables void-free filling.
- A range of electroanalytical and surface analytical studies under way to quantify the competitive and co-adsorption processes associated with copper superfilling additives. A combination of surface analytical and electroanalytical methods was used to reveal a.) difference in adsorption behavior between rate accelerating thiols versus disulfides, b.) irreversible adsorption of thiols and disulfides versus reversible adsorption of halide and PEG, c.) inhibition of PEG adsorption by a pre-adsorbed sulfonate-terminated thiol or disulfide monolayer film, and d.) displacement of the deposition rate inhibiting PEG layer by adsorption of the sulfonate-terminated thiol or disulfide accelerator.
- The existing CEAC model of superfilling was extended to include the effect of leveling additives along with the metrology required for assessing the kinetics of the competitive adsorption process. The impact of leveling additives on overfill bump formation during trench filling was demonstrated using prototypical cationic surfactants.

Collaborations

L.-Y. Ou Yang, C.H. Lee, J.E. Bonevich, L.J. Richter, P.J. Chen, W.F. Egelhoff: NIST, R. Gordon: Harvard University.

Publications

T.P. Moffat and L.-Y. Ou Yang, "Accelerator Surface Phase Associated with Superconfomral Cu Electrodeposition", J. Electrochem. Soc., 157, D228 (2010).

T.P. Moffat, C.H. Lee and D. Josell, "3-D Metallization by Damascene Electrodeposition," submitted Korean Electrochemical Society, April (2010).

C. H. Lee and T.P. Moffat, *"A Modified Damascene Electrodeposition Process for Bottom-up Filling of Recessed Surface Features"* submitted to Electrochimica Acta, March 2010

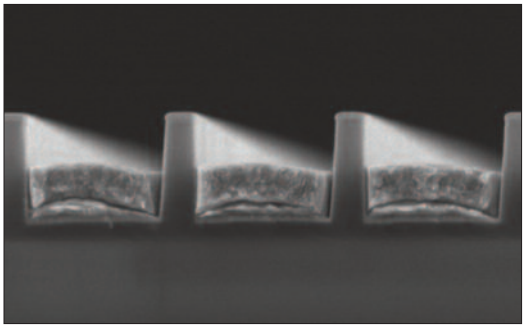

Figure 3. A modified Damascene trench filling process showing exclusive bottom-up deposition.

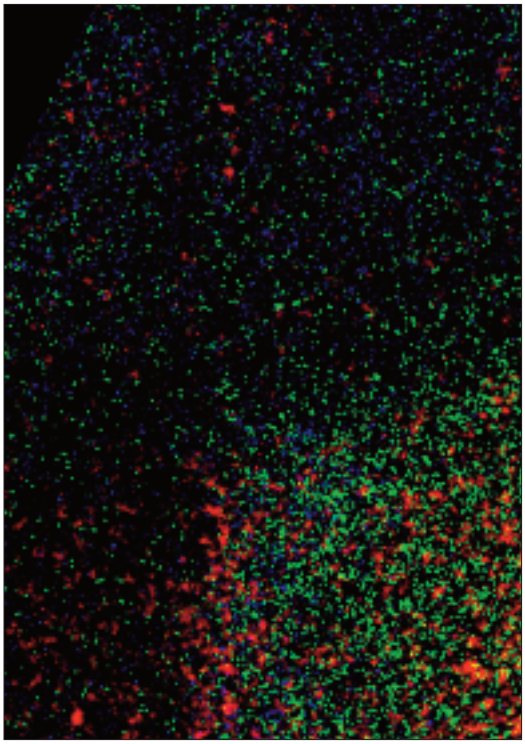

Figure 4 TEM-EDS of Cu filled trench lined with a highly conformal WN/Co4N barrier and Cu seed layer produced by ALD and CVD, respectively.

Daniel Josell, S.H. Brongersma and Z. Tokei, "Size-Dependent Resistivity in Nanoscale Interconnects," Annu. Rev. Mater. Res., 39, 251 (2009).

C.H. Lee, J.E. Bonevich, J.E. Davies and T.P. Moffat, "Superconformal Electrodeposition of Co and Co-Fe Alloys using 2-Mercapto-5-benzimidazaolesulfoncis Acid" (MBIS), J. Electrochem. Soc., 156, D301 (2009).

T.P. Moffat, D. Wheeler and D. Josell, "Superconformal Deposition and the CEAC Mechanism," Dielectric for Nanosystems 3, Materials Science, Processing, Reliability and Manufacturing, D. Misra, H. Iwai, Y. Obeng, T. Chikyow and J. Vanhellemont, Editors,The Electrochemical Society, 13, 129-137 (2008).

T.P. Moffat, D. Wheeler and D. Josell, "Superconformal Film Growth," in Advances in Electrochemistry and Electrochemical Engineering, pg 107-189, R.C. Alkire, D.M. Kolb, P. Ross and J. Lipkowski, Editors, Wiley-VCH, Weinheim, Germany(2008). C.H. Lee, J.E. Bonevich, J.E. Davies and T.P. Moffat, "Magnetic Materials for 3-D Damascene Metallization: Void-free Electrodeposition of Ni and Ni70Fe30 Using 2-Mercapto-5-benzimidazolesulfonic Acid," J. Electrochem. Soc., 155, D499 (2008).

S-K. Kim, J.E. Bonevich, D. Josell and T.P. Moffat, "Electrodeposition of Ni in Submicrometer Trenches," J. Electrochem. Soc., 154, D443 (2007).

T. P. Moffat, D. Wheeler and D. Josell, "Superconformal Film Growth," pg 96-114 in "Electrocrystallization in Nanotechnology," Ed. G. Staikov, Wiley-VCH (2007).

M. Walker, L. J. Richter, and T. P. Moffat, "Potential Dependence of Competitive Adsorption of PEG, Cl-, and SPS/MPS on Cu: An In Situ Ellipsometric Study," Journal of the Electrochemical Society 154(5), D277-D282 (2007).

D. Josell, T. P. Moffat and D. Wheeler, "Superfilling When Adsorbed Accelerators Are Mobile," Journal of the Electrochemical Society, 154(4), D208-D214 (2007).

T. P. Moffat, D. Wheeler, S. K. Kim and D. Josell, "Curvature Enhanced Adsorbate Coverage Mechanism for bottom-up superfilling and bump control in damascene processing," Electrochimica Acta, 53, 145 (2007).

D. Josell, "A paradigm for interconnect geometry to reduce grain boundary resistance," J. Appl. Phys., 100, 123705 (2006).

S.-K. Kim, D. Josell and T. P. Moffat, "Cationic Surfactants for the Control of Overfill Bumps in Cu Superfilling," J. Electrochemical Society, 153 (12), C826-C833 (2006).

S.-K. Kim, D. Josell and T. P. Moffat, "Electrodeposition of Cu in the PEI-PEG-CL-SPS Additive System: Reduction of Overfill Bump Formation During Superfilling," J. Electrochemical Society, 153 (9), C616-C622 (2006).

M. Walker, L. J. Richter, and T. P. Moffat, "Competitive Adsorption of PEG, Cl-, and SPS/MPS on Cu: An In Situ Ellipsometric Study," Journal of the Electrochemical Society 153(8), C557-C561 (2006).

T. P. Moffat, D. Wheeler, S.-K. Km and D. Josell, "Curvature Enhanced Adsorbate Coverage Model for Electrodeposition," Journal of the Electrochemical Society, 153(2) C127-C132 (2006).

D. Josell, D. Wheeler and T. P. Moffat, "Gold Superfill in Submicrometer Trenches: Experiment and Prediction," Journal of the Electrochemical Society, 153(1) C11-C18 (2006).

Nanoimprint Lithography

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Goals

Nanoimprint Lithography (NIL) is rapidly emerging as a low-cost patterning alternative to optical lithography, offering e-beam type resolution in a high-throughout, low-cost nanoscale patterning tool. Patterning resolutions of better than 10 nm have been demonstrated under optimized laboratory conditions. For these reasons NIL now appears on the ITRS roadmap as a candidate new generation lithography (NGL) for the 22 nm node. Optical lithography is a 4× patterning process, where the features on the mold are approximately four times bigger than the patterned feature. By comparison, NIL is a direct write (1×) technology where the feature in the mold directly corresponds to the feature in the pattern. This switch from a 4× to a 1× technology, coupled with a sub-10 nm resolution, greatly heightens CD metrology issues. Even with 4× optical lithography, the ITRS roadmap is facing critical CD metrology roadblocks and the advent of NIL would significantly exacerbate these concerns. One of the primary objectives of this project is to develop the relevant CD metrology methods needed to facilitate the NIL technology. The other objective of this project is to address the measurements issues that are unique for NIL, different from the traditional metrology needs for CMOS fabrication. NIL is a contact lithography method and that comes with very different metrology challenges due to the fact that the imprint mold makes mechanical squeeze-flow contact with the resist. The overall objective of this project is to address the measurement challenges facing NIL, not just for CMOS fabrication but for nanoscale pattering in general.

Customer Needs

The ultimate challenge for any new lithographic patterning technique is to demonstrate an improved patterning resolution. This requires a quantitative comparison of pattern shape. It has already been mentioned above that NIL offers a potential patterning resolution of better than 10 nm, exceeding the capability of current critical dimension (CD) metrology tools to accurately quantify. This significantly exacerbates current CD metrology concerns. With respect to NIL patterning, a unique CD measurement challenge arises. Because NIL is a direct write (1×) technology where the features in the mold directly correspond to the features in the pattern, high resolution CD metrology becomes critical. With optical lithography, the mask features are nominally four times bigger than the printed imaging which somewhat relaxes the resolution requirements for mask inspection tools. Furthermore, the resolution of the final optical lithography pattern depends on a complicated interplay of optical exposure effects, reaction-diffusion process in the latent resist image, and lastly the strength and conditions of the aqueous developer process. It is hard to directly trace small dimensional defects in the mask to the final pattern through this complicated process. On the contrary, NIL is a direct write process where the features in the imprint mold are directly transferred to the patterned resist.

Defects in the mold are directly transferred to the resist pattern. So with NIL, CD metrology must include the fidelity of pattern transfer concept. This means applying high resolution pattern shape measurements to both the imprint master and the resulting imprint. By quantitatively comparing the pattern shapes in the mold and the imprint one can determine if any potential defects are due to the quality of the mold itself or the performance of the resist material. This type of simple, direct comparison is simply not possible with optical lithography, and only possible with NIL through improved CD metrology methods. The next challenge is to quantify how the mechanical forming aspect of NIL differs from optical lithography with respect to measurement issues. One of the unique aspects is that the NIL process requires material flow into nanoscale cavities. This has several effects. First, resists are usually multi-component, reactive mixtures and it is likely that one of the components will have a preference or favorable interaction with the surface of the imprint mold.

This can affect the phase behavior of the resist mixture, or lead to surface-induced effects on the chemical reactions. In these cases it is critical to quantify how confinement and the surface effects influence the reaction within the resist and consequently the ultimate patterning resolution. The second measurement challenge comes from the

fact that resists can be highly viscous liquids that do not readily flow, especially in the case of thermal NIL where the resist is heated to the melt state to induce flow. Imprinting these highly viscous materials induces large shear stresses or flow fields. These shear stresses can be locked into the imprinted patterns as residual stresses, which over extended periods of time have the tendency to relax and induce distortions that compromise the stability of nanoscale structures and deteriorate the CD control. A third measurement problem stems from the fact that the NIL technology has the potential to directly pattern functional, such as nanoporous organolsilicate materials for semiconductor interconnect insulators. By patterning the interconnect material directly through a mechanical forming NIL process, one has the potential to essentially eliminate all of the litho steps in the back end of the line interconnect fabrication process, creating a tremendous cost savings. However, in this direct patterning approach the way that the NIL processes affect the function of the interconnect material, both in terms of critical dimension control and functional porosity properties are of critical importance. Measurements that quantify these effects are critical to advancing such cost-savings technology.

Technical Strategy

In the realm of state-of-the-art lithography, the ability to reliably produce high resolution patterns has been the primary figure of merit for any new patterning technology. This requires measurement methods that quantify and compare pattern quality with nanometer accuracy. As patterning resolution continues to improve, our ability to do this comparison quantitatively becomes a critical roadblock. This is especially true for NIL, where patterning resolution increases dramatically over the incumbent optical lithography. Our ability to pattern is now seriously encumbered by our ability to quantify and new pattern shape measurements are critically needed. To this end we continue to develop a suite of X-ray based metrology tools that include critical dimension small angle X-ray scattering (CD-SAXS) and specular X-ray reflectivity (SXR). Both of these methods are non-destructive and capable of quantifying pattern shape with nm accuracy. The fact that they are reciprocal space measurements means that characterizing smaller patterns becomes easier. When coupled with traditional critical dimensional metrology tools, we have a unique and powerful methodology to quantify the shape and dimensions of nanoscale structures with nm accuracy.

DELIVERABLES:

- Develop and apply shape metrology methods for NIL

NIL is a direct write pattern transfer process. The features in the mold directly transfer the imprint without going through a lens or other image reduction system. Evaluating the quality of the NIL patterning process requires quantitative critical dimension quantification of both the imprint mold and the patterns that it creates. Our CD-SAXS and SXR pattern shape measurement are well suited for quantifying the fidelity of pattern transfer in the imprint. They are both non-destructive methods meaning that mold or the pattern does not have to be sacrificed to quantify the fidelity of pattern transfer. The flexibility of either a transmission (CD-SAXS) or reflection (SXR) measurement means that a wide array of molds and substrates, ranging from thin to very thick, can be quantified. Using these methods it is straight forward to quantify the full pattern profile, including height, width, side wall angles, and periodicity with nm scale precision in both the mold and the imprint. This provides the framework for a highly quantitative fidelity of pattern transfer analysis, thereby providing a powerful tool for evaluating NIL patterning processes.

SXR and CD-SAXS are emerging X-ray based methods with several advantages over other pattern shape metrology tools used in the semiconductor industry. However, there are several disadvantages with these emerging methods as compared with the industry standards like optical scatterometry. One of the primary complaints with SXR and CD-SAXS is that they are slow measurements that require long data collection times or highly intense X-ray sources, typically found at a synchrotron. Additionally, the SXR measurement requires very large pattern fields that are not typical for real device architectures. Optical scatterometry directly overcomes these weaknesses by using intense laser light sources that can be focused into very small, micron-scale spots which enables the rapid characterization of small pattern fields. However, the interpretation of scatterometry data requires extensive libraries of all the possible shape that the nanostructures could be. There is significant benefit in using SXR and CD-SAXS methods to help verify, improve, and develop these scatterometry libraries.

For the nanoscale structures that are relevant for NIL, the size of the pattern is significantly smaller than the wavelength of the laser light which leads to very subtle variations in the psi and delta of the reflected light. To properly interpret the scatterometry data requires highly accurate models. To this end we are working to develop and adapt our SXR and CD-SAXS techniques as an independent method to verify help validate and refine scatterometry models. The increased patterning resolution provided by NIL makes this validation and cross-comparison all the more important.

DELIVERABLES:

- Develop measurement methods to quantify the stability of nanoscale NIL structures

Generating patterns by NIL requires the squeeze-flow of viscous resist liquids into the nanoscale cavities of an imprint mold. Because of these nanoscale dimensions, the shear stresses and/or shear rates that the flowing materials experience are extremely severe. In many instances the filling process is more accurately described as a deformation of the liquid rather than a quiescent flow. Depending on the duration of the imprint process, the material may or may not have sufficient time to relax the flow induced deformation. If deformation relaxation is not achieved, residual stresses are generated and can comprise the physical stability of the pattern later on. Using our CD-SAXS and SXR pattern shape measurements, we have developed an approach to ascertain the levels of residual stress imparted to the pattern by the NIL process. The involves heating the pattern to near it's softening point and quantifying how the pattern shape evolves with time. It is possible to distinguish between the residual stress driven decay and a simple viscous flow. The evolution of the pattern profiles with time is very different in these two limits and from the response we can infer the level of residual stress induced by the imprint process.

These issues of pattern stability can be significantly complicated by the fact that actual resists are never single component systems. They can contain multiple reactive species, catalysts to speed up the reaction, surface tension modifiers, viscosity modifiers, additives to modify the etch resistance, and solvents to facilitate dispensing. While these multicomponent systems are typically co-dissolved into a single solvent, there will always be an energetic preference for one of the components to be near a given surface. Likewise, certain components can also tend to avoid an interface due to differences in the surface energy. When surface segregation occurs, the composition of the resist mixture is locally altered and the performance or function of the resist in that interfacial region is also changed. NIL has the potential to magnify the importance of these interfacial effects because the patterns are generated by placing a high surface energy mold in contact with the resist fluid/film, directly creating an interfacial region. For relatively thick films and large structures, the fraction of the material at the interface is negligible and these effects can often be ignored. However, with the high density of nanoscale features, as encountered in NIL, essentially all of the resist material can be classified as interfacial. The problem can be further exacerbated by the fact that the mold is filled with resist by a rapid squeeze-flow process. This can generate large shear fields that could induce demixing or field flow fractionation of the resist components. To fully optimize the performance of NIL resist materials requires quantitative measurements of the phase behavior within the imprinted nanoscale structures. Measurement techniques that can resolve compositional variations in an imprinted pattern will be critical for future resist developments.

A combination of X-ray and neutron reflectivity measurements in conjunction with CD-SAXS have the potential to detect surface or shear induced demixing of a multi-component imprint materials. With this deliverable we plan to develop these measurements as a way to demonstrate to the community that these interfacial effects are important. We have already described how X-ray reflectivity measurements (SXR) and CD-SAXS can be used to accurately quantify the complete cross-section of the nanostructures fabricated by NIL. Most NIL resist are hydrocarbon mixtures, organic in nature, in which the scattering-length density for each of the components with respect to X-rays is very similar. A subtlety that was not discussed earlier is that this similarity is in part why SXR can be used to quantify the shape of polymeric or organic multi-component patterns. Changes in the scattering length density profile as a function of vertical distance through the pattern can be interpreted in changes in the shape of the lines, not changes in the composition. However, with neutrons this similarity in the scattering length density can be lost. By isotopi-

cally replacing the hydrogen in one of the resist components with deuterium, a very strong change in the neutron scattering length density can be achieved. The power of this hydrogen-deuterium labeling methods comes from the fact that the substitution does not change the X-ray scattering length density. So the combination of CD-SAXS and SXR on a model resist where one of the components is deuterium labeled can still be used to quantify the pattern shape. Once the shape is fully parameterized, the same sample can be measured by neutron reflectivity. In analyzing the neutron reflectivity data, the shape of the pattern will be fixed from the fitting of the X-ray data. Then the resulting fits from the neutron reflectivity data will reveal the variations of the scattering-length density as a function of height through the pattern, i.e., the composition of the deuterium labelled component through the pattern. Using this method it should be possible to distinguish between the different scenarios where the deuterium labeled component segregates to the supporting substrate surface, the upper imprinted surface, or remains molecularly dispersed through the pattern.

DELIVERABLE:

- Apply measurements that evaluate the direct patterning of organosilicate materials relevant for interconnect technologies

Recently there is a growing interest within the community to directly pattern spin-on organosilicate ILD materials by nanoimprint lithography (NIL). It has been shown that by imprinting the ILD material with a multi-level nanoimprint template to directly fabricate a T-gate type structure, one can greatly reduce the number of lithography, deposition, and etching steps in the back end of the line process. This could *significantly* reduce manufacturing costs. Efforts this year will synergistically couple our expertise in thin film nanoporous X-ray metrology with our simultaneous efforts in NIL metrology development. Specifically, we will adapt our XR shape metrology to quantify the fidelity of the nanoimprint process to evaluate the quality of the patterned ILD materials. We will also adapt our XRP measurements on patterned samples to quantify how the NIL process itself affects the pore structure. These measurement techniques will quantify the feasibility of NIL processes for back end of the line interconnect fabrication schemes. This is a topic that all of the major NIL tool companies are actively engaged in.

Accomplishments

This year significant progress was made on the quantitative fidelity of the NIL pattern transfer concept. Our starting point is an imprint master with parallel line-space gratings fabricated into silicon oxide. In real life applications, the original imprint master is rarely used to do actual imprint patterning. Rather, the master is used to generate a handful of daughter molds, copies of the master, which in turn are used for the day-to-day patterning. Using this approach one can extend the life of the costly imprint master. Our approach is to quantify the fidelity of pattern transfer through this process, starting with the original master and going through the daughter mold to the secondary imprint made with the daughter. To create the daughter mold, imprints are made at 200 °C, using the original template, into a spin-on organosilicate film that is similar in composition to the materials that are used for spin-on low k dielectric insulator applications. During the imprinting process material flow occurs while simultaneously the organosilicate material starts to condense into a hard organosilicate cross-linked network. However, the conversion is not complete at 200 °C so free the standing pattern is then further heated to 400 °C in an inert atmosphere to generate a fully cross-linked, hard organosilicate material that can be used as a daughter imprint mold. In the last step the daughter mold is thermally imprinted into a polystyrene film at 150 °C. In the following we apply our SXR and CD-SAXS methodologies to the original master, the organosilicate daughter, and the secondary polystyrene imprint.

Figure 1 compares the cross sectional profiles of the original master relative to the organosilicate (TTSE) daughter mold in the upper panel, and the daughter mold relative to the secondary polystyrene (PS) imprint in the lower panel. These profiles are the quantitative models used to fit the CD-SAXS and SXR data and not schematic drawings. To gage the length scales, the periodicity in each pattern is exactly 200 nm. In the upper panel the white gaps between the black colored master and the blue colored daughter represents shrinkage of the organosilicate pattern relative to the imprint cavities, including any shrinkage that occurred during the imprint as well as during the high temperature vitrification. In other words, these white spaces quantify the loss of fidelity/resolution. In the bottom panel, there is very little shrinkage or loss of fidelity between

the daughter mold and the PS imprint. The profile of the mold and imprint are nearly identical. When considering the patterning mechanism, these observations make sense. The PS is imprinted in the melt state, where the molten PS is an incompressible fluid and there is a conservation of volume. There is also very little shrinkage as the PS cools from the imprint temperature of 150 °C back down to the mold separation temperature of 55 °C. Given this approximately 100 °C temperature swing and difference in the coefficient of thermal expansion between the organosilicate and the PS, one would expect the 70 nm PS lines to shrink by approximately 1 nm relative to the organosilicate mold. This back of the envelope calculation seems consistent with the experimental data indicating that thermal imprinting can yield a very high fidelity of pattern transfer. On the other hand, in the imprinting of the organosilicate material, volume is not conserved. Some shrinkage is observed. The spin-on organosilicate is known to be laden with residual spin casting solvent. It is reasonable that this solvent is released at elevated temperatures during the imprint. Also, the cross-linking of the organosilicate is a condensation reaction where two silanols react and liberate a water molecule. The evolution of residual solvent or water molecules is consistent with the observation of shrinkage during the organosilicate patterning.

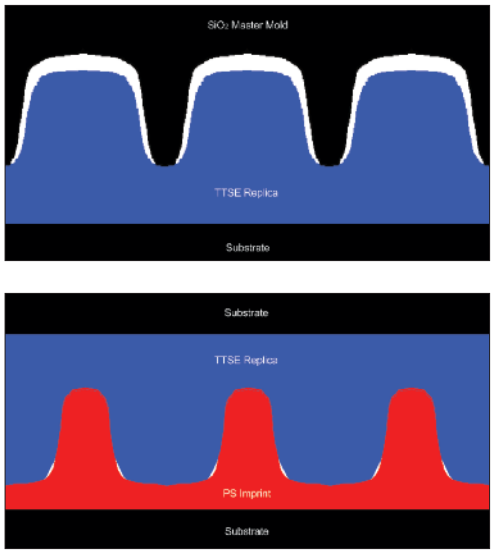


Figure 1. The upper panel compares the cross sectional profiles of the original imprint master mold to the replica or daughter mold imprinted into a high modulus organosilicate material (labeled TTSE here). The lower panel then compares the cross sectional profile of the TTSE daughter mold to the pattern generated through a thermal imprint into a PS film. The white gaps between the mold and the imprint represent the shrinkage or loss in fidelity of the pattern transfer process.
In both panels the pattern periodicity is 200 nmt.

Another technical area in which significant technical progress was made this year was in the complimentary implementation of optical scatterometry as a critical dimension metrology tool for NIL patterning. As discussed above, when comparing X-ray based metrology tools to optical methods, there are well defined advantages and disadvantages to each approach. With respect to scatterometry, one of the major advantages of this technique is in the speed and simplicity with which measurements can be made. The price of these fast measurements is that data interpretation is significantly more complicated compared to the slow but straight forward X-ray techniques. This year we focused on combining SXR pattern shape measurements with scatterometry as a tool to track the real time shape changes as an imprinted pattern is annealed at elevated temperature. With an applied thermal stimulus, an imprinted polymer pattern has the propensity to decay in height and ultimately transform into a smooth surface that minimizes the surface free energy of the system. In a separate project we have been tracking the time evolution of this pattern decay as a metrology to back out the levels of residual stress induced into the patterns by the NIL process. If the decay is consistent with the flow of a viscous liquid, the conclusion is that the patterning process did not induce residual stresses. If the decay occurs faster than what a viscous decay would predict, the conclusion is that the imprint process induces significant levels of residual stress. Without going into the details of this project, it is sufficient to say that a pattern shape metrology that is capable of tracking the real time decay pattern is highly attractive. SXR based methods are inherently slow, requiring at least 30 minutes per measurement which makes in-situ pattern evolution studies difficult. However, scatterometry has the potential or real time pattern shape measurement. In Figure 2, we compare the pattern shape profiles obtain from both scatterometry and SXR. The upper panel in the figure to the left shows a series of line profiles obtain from the same 200 nm pitch PS patterns obtained from both the scatterometry (lines) and the SXR (dots) at a series of different discrete time points

through the annealing process. The two methods are in very close agreement, showing a consistent picture of how the initially rectangular cross sections evolve into a smooth sine wave like function at long times. What is not articulated in this plot is how the SXR model was extremely helpful in establishing the starting point for modeling the scatterometry data.

With confidence in having chosen the correct model to interpret the scatterometry data, we can then harness the real time data collection aspect of the optical method. The lower panel of Figure 2 quantifies the real time evolution of just the pattern height for the thermal decay of both a high (1570 kg/mol) and low (19 kg/mol) molecular mass imprinted polystyrene pattern, as quantified by scatterometry. This type of in-situ characterization is not possible with the SXR method. The height decay data reveals an interesting trend. The high molecular mass pattern decays significantly faster (in this case both samples are annealed at Tg (the glass transaction temperature)) than the lower molecular mass analog, despite the exponentially larger steady state viscosity of the high molecular mass material. This discrepancy directly reflects the residual stress levels in the imprinted pattern. The initially rapid decay of the high molecular mass pattern means that significant levels of residual stress have been stored in the imprinted pattern. After approximately 60 minutes of annealing the exponential decay rate slows down significantly, signifying that the stresses have been relaxed. At that point the relaxation of the low molecular mass pattern becomes faster as would be predicted by simple viscosity argument.

With this ability to rapidly characterize the full pattern shape evolution with scatterometry, we are now in the position to make quantitative comparisons of the performance of different resists materials with respect to the imprint generation of residual stress, the key parameter that impacts nanostructure stability. We are in the process of varying the thermal imprint conditions on a series of model imprint resists where the entanglement molecular mass of the polymeric resist material is systematically varied. The resistance to thermally induced flow of a resist is largely controlled by how entangled the linear chains of the polymeric material are. With optical scatterometry one can rapidly evaluate a wide range of imprint conditions and optimize processes for structurally and mechanically stable imprints. These measurements are revealing that the entanglement density or the entanglement molecular mass of the imprint resist is a key parameter to generate stress free imprints. Highly entangled polymer chains have a large resistance to flow and generate significant residual stress upon mold fill that leads to unstable patterns. Weakly entangled systems flow much more readily and significantly help diminish the levels of residual stress and facilitate robust patterns. This type of understanding was enabled by the high resolution model verification provided by SXR and CD-SAXS, coupled with the rapid data collection and the ability to screen large areas of parameter space with optical scatterometry.

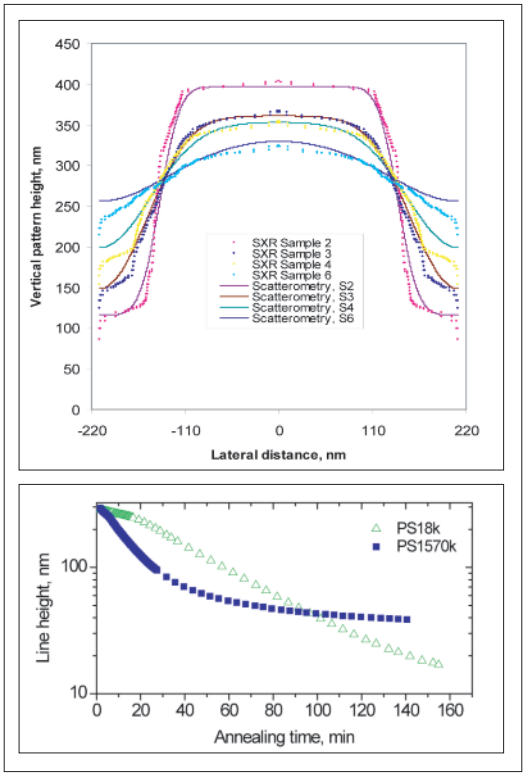
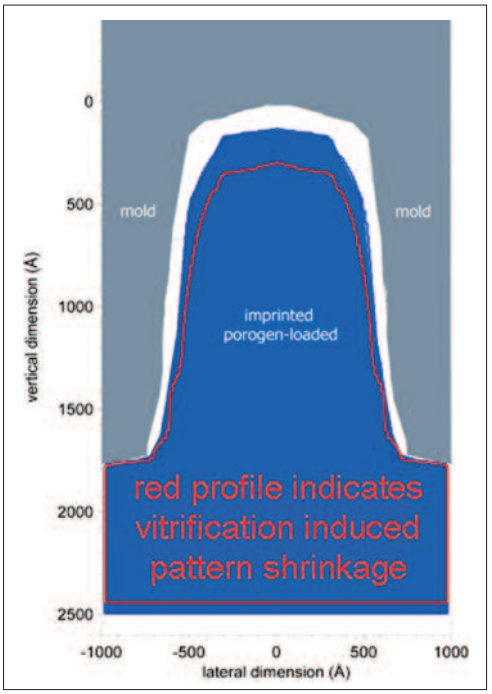


Figure 2. The upper panel compares the cross-sectional profiles obtained through specular X-ray reflectivity (SXR, dots) and optical scatterometry (lines) for a series of PS patterns annealed for increasing amounts of time. With increased annealing the patterns decrease in height and evolve into a sine wave type profile. The lower panel compares how just the pattern height evolves real time, as quantified by scatterometry, for both a low and high molecular mass pattern.

One exciting alternative to directly eliminate or simplify several of the integration steps completely in BEOL processes is to introduce NIL

processes to directly pattern the low-κ dielectric material. As described above, this can completely eliminate several of the etching and ashing processes that result from transferring a resist pattern into a dielectric layer. Directly patterning the dielectric material itself can completely eliminate several of these pattern transfer steps that lead to the increase in the effective k. This year we made two major advances on the direct patterning of ILD materials with NIL. First, the concept of directly patterning the ILD materials was originally introduced in 2006 by Professor Grant Willson's group. However, to date the only examples of this type of patterning have been on very low modulus materials with relatively high dielectric constants that would not be suitable for current ILD applications. This year we made the critical step to show that ILD materials with an intrinsic dielectric constant on the order of 2.0 and a sufficiently high modulus could be directly patterned with NIL with very high fidelity. This demonstration was made possible through high resolution critical dimension measurements on both the NIL mold and the imprinted pattern. Using a combination of SXR and SAXS shape measurements, we showed that the pattern shape in the imprint mold could be transferred to the ILD material with extremely high fidelity, even with a high temperature vitrification stage where the spin on organosilicate is condensed into a hard, ceramic-like material. This vitrification process is usually associated with shrinkage of the material. As shown in the figure above, our measurement show pattern shrinkage in all dimensions, not only relative to the mold immediately after imprinting, but also after the free standing pattern is vitrified at 430 °C. Our pattern shape measurements are able to define the pattern fidelity throughout the entire process. These seminal pattern shape measurements were described in an Advanced Materials article.

Another area in which we continue to be active in is precisely quantifying how the NIL patterning process affects the critical porosity of these low-κ materials. We developed a variant of XRP that is applicable to patterned materials and were able to extract the porosity as a function of pattern height. When combined with complimentary positron annihilation lifetime spectroscopy and cross-sectional transmission electron microscopy (TEM) measurements, this study revealed an NIL induced dense skin of the order of a few nm in thickness on the surface of the porous pattern.



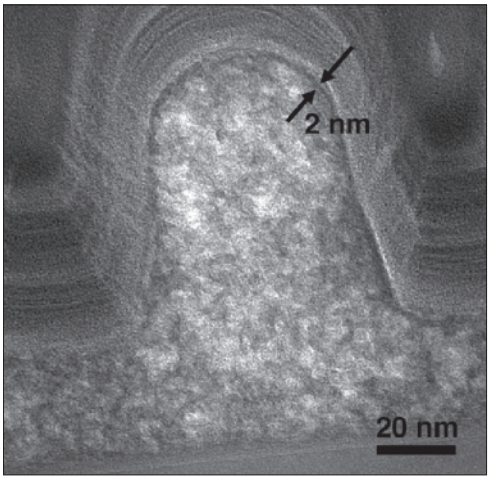


Figure 3. The upper panel shows cross-sectional profiles derived of the as imprinted pattern, before vitrification, (blue) relative to the mold (grey) indicating the shrinkage upon imprinting. The red curve indicates the additional shrinkage that occurs after the high temperature vitrification. The lower panel shows a cross-sectional TEM image of the same patterns, suggesting a dense skin of a few nm thick on top of the porous pattern

The cross sectional TEM image in Figure 3 shows evidence of this dense skin, which is highly attractive from an application point of view. Integration processes often require the addition of a densified skin on the ILD pattern to reduce interdiffusion. That NIL could intrinsically induce this

barrier layer is highly attractive. These findings were also published in Advanced Materials.

Collaborations

Polymers Division, NIST – Hae-Jeong Lee, Hyun Wook Ro, Kenneth Kearns, Chengqing Wang, Wen-li Wu.

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University of Michigan - David Gidley, Richard Laine

Mayaterials, Inc. - Vera Popov, David Krug

Kyoto Institute of Technology – Hiroshi Jinnai.

Publications

H.W. Ro, E.S. Park, C.L. Soles and D.Y. Yoon, *"Structure−Property Relationships for Methylsilsesquioxanes,"* Chem. Mater., 22, 1330 (2010)

K. J. Alvine, Y. Ding, J. F. Douglas, H. W. Ro, B. C. Okerberg, A. Karim, K. A. Lavery, S. Lin-Gibson, C. L. Soles, *"The Effect of Fluorosurfactant on Capillary Instabilities in Nanoimprinted Polymer Patterns,"* J. Polym. Sci.: Part B: Polym. Phys. 47, 2591 (2009).

H. W. Ro, E. S. Park, C. L. Soles, D. Y. Yoon, *"Structure-Property Relationships for Methylsilsesquioxanes,"* Chem. Mater. XXXXX (2009).

W.L. Johnson, S.A. Kim, R. Geiss, C.L. Soles, C. Wang, C.M. Stafford, W.-l. Wu, J.M. Torres, B.D. Vogt, P.R. Heyliger, *"Elastic Constants and Dimensions of Imprinted Polymeric Nanolines Determined from Brillouin Light Scattering,"* Nanotechnology 21, 075703 (2010).

K.J. Alvine, Y. Ding, J.F. Douglas, H.W. Ro, B.C. Okerberg, A. Karim, and C. L. Soles, *"Capillary Instability in Nanoimprinted Polymer Films,"* Soft Matter 5, 2913 (2009).

D.Y. Lee, D.R. Hines, C.M. Stafford, C.L. Soles, E.K. Lin, G.S. Oehrlein, *"Low-Temperature Plasma-Assisted Nanotransfer Printing between Thermoplastic Polymers,"* Advanced Materials, 21 (2009) 2524–2529.

J. Zhou, B. Berry, J.F. Douglas, A. Karim, C. R. Snyder, and C. Soles, *"Nanoscale thermal-mechanical probe determination of 'softening transitions' in thin polymer films,"* Nanotechnology, 19 (2008) 495703.

H.W. Ro, R. L. Jones, H. Peng, H.-J. Lee, E. K. Lin, A. Karim, D.Y. Yoon, D.W. Gidley and C. L. Soles, *"Porosity Characteristics of Ultra-low Dielectric Insulator Films Directly Patterned by Nanoimprint Lithography,"* Emerging Lithographic Technologies XII, Ed. Frank M Schellenberg, Proc. of SPIE, 6921, 69211M (2008).

H.-J. Lee, S. Kim, C.L. Soles, E.K. Lin, W.-L. Wu, *"Exploring the Limitations of X-ray Reflectivity as a Critical Dimension Pattern Shape Metrology,"* Metrology, Inspection, and Process Control for Microlithography XXII, Ed. John Allgair and Christopher Raymond, Proc. of SPIE, 6922, 692224 (2008).

H.W. Ro, H. Peng, K. Nihara, H.-J. Lee, E. K. Lin, A. Karim, D. W. Gidley, H. Jinai, D.Y. Yoon , and C.L. Soles, *"Self–Sealing of Nanoporous Low Dielectric Constant Patterns Fabricated by Nanoimprint Lithography,"* Advanced Materials 20 (2008) 1934.

Y. Ding, H.W. Ro, K.J. Alvine, B.C. Okerberg, J. Zhou, J.F. Douglas, A. Karim, and C.L. Soles, *"Nanoimprint Lithography and the Role of Viscoelasticity in the Generation of Residual Stress in Model Polystyrene Pattern,"* Advanced Functional Materials 18 (2008) 1854.

C.L Soles, Y. Ding, *"Nanoscale Polymer Processing,"* Science, 332, 689 (2008).

H.J. Patrick, T.A. Germer, Y. Ding, H.W. Ro, L.J. Richter, and C.L. Soles, *"Scatterometry for in-situ Measurement of Pattern Reflow in Nanoimprinted Polymers,"* Applied Physics Letters, 93, 233105 (2008).

Interconnect Materials And Reliability Metrology

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"Mechanical properties are key to integration."

Roey Shaviv
Novellus Systems Inc.

Goals

The objectives of this project are: (1) to develop experimental techniques to measure the long term performance of state of the art (copper-based) and future (carbon-based) electronic interconnects in their as-manufactured states, under stressing by heat, electric current, and mechanical loading; and (2) to advance the ability to anticipate and meet interconnect reliability challenges by relating reliability to microstructure and by developing understanding of the relationships between various modes of failure in nanoscale interconnect structures.

Customer Needs

Thin metal films are an essential component of all advanced electronic devices, and perform tasks ranging from routing signal between circuits and systems to providing power/ground paths. Interconnect structures built up on ULSI microchips consist of 12 metal levels now, and will exceed 13 levels in the long term (International Technology Roadmap for Semiconductors (ITRS), 2007, Interconnect, Table INTC2a). These structures are fabricated in conjunction with adjacent layers of materials with very different thermal expansion properties, including exotic materials such as nanoporous low-κ dielectric. Coupled with continued dimensional scaling and increasingly higher operating temperatures, these complex materials systems are often pushed to their limits and are at increasing risk of failure due to thermomechanical and electrical effects. Achieving the necessary reliability therefore remains a continuing Difficult Challenge for Interconnect (see, e.g., Table INTC1 in both the 2007 ITRS and the 2008 ITRS Update). Generally, the industry needs improved failure detection techniques, new testing methodologies, material system modeling, and identification of potentially new damage mechanisms in order to manage failure risk.

Both experimental measurements and modeling and simulation of material behavior are needed, and these efforts need to be complementary. According to the ITRS Roadmap (2007 Edition), Interconnect, p. 39, cost effective first pass design success requires computer-aided design (CAD) tools that incorporate contextual reliability considerations in the design of new products and technologies. The 2005 iNEMI (International Electronics Manufacturing Initiative) Research Priorities document indicates similar needs: "Materials & Reliability and Design" is one of their top five research areas. Emphasized are effects of temperature, cyclic loading, and dimensional scaling.

It is essential that advances in failure mechanism testing, understanding, and modeling be used to provide input data for these new CAD tools. With these data and smart reliability CAD tools, the impact on product reliability of design selections can be evaluated. The message is clear: knowledge of the mechanical response of interconnect materials remains key to successful process integration and product reliability.

Because interconnect materials are formed by thin-film deposition methods, their microstructures, and hence, their mechanical properties, are different from those of bulk materials of the same chemical composition. While the general principles of conventional mechanical testing are applicable to thin films, conventional test equipment and techniques are not. Because vapor-deposited films are of the order of tens to hundreds of nanometers thick, the specimens cannot be handled directly. Furthermore, the specific mechanical response of a patterned interconnect is inherently dependent on the presence of the substrate and dielectric materials in the immediate vicinity. So, techniques specific to lines on silicon substrates are needed, and these must also apply to structures fully encapsulated by dielectric. Developing test methods must eventually be applicable to test structures that can be included in production or development wafers, so that applicability to 'real' materials can be demonstrated.

Void formation is presently recognized as one of the most critical service reliability issues for interconnect structures on leading-edge commercial chips; the mechanical response of the constitutive materials plays an important role in determining susceptibility. Voiding is classified into two types: electromigration-induced, where the flow of electrical current through a mechanically confined line displaces atoms; and stress-induced, where the relaxation of process stresses forms voids.

The Roadmap (2007 Edition), Interconnect, Table INTC2a, foresees interconnect current densities in excess of 2.5 MA/cm^2 in 2014. Continued dimensional scaling of conductors means increasing levels of residual mechanical stress. In both cases, there are no present capabilities to produce products with acceptable reliability.

Radically different materials are being considered for future ULSI devices, as the further development of leading-edge lithography increases in cost and complexity. An example of a radically new material is the carbon nanotube (CNT). While CNTs offer several advantages over copper, their reliability properties remain unaddressed. For example, strong sp^2 bonding leads to very large current-carrying capacities. However, in an as-integrated state, potential failures might then become localized to the carbon-metal contact region. Effective use of these new materials systems will require significant extension of the reliability metrology and analysis toolset to understand and address new kinds of reliability issues. The NIST laboratory research programs that are now developing experimental and analytical techniques to address these challenges.

Technical Strategy

We develop measurement techniques to provide property data on interconnect materials, with emphasis on the properties that impact reliability. Through our testing and data generation, we improve understanding of reliability-relevant relationships between observed behaviors and interconnect microstructure, as influenced by processing conditions specific to the specimen material. We study individual thin films and multilayer interconnect structures on silicon substrates, both obtained from industry and fabricated by researchers within NIST and elsewhere. A very recent undertaking addresses the extension of current and the development of new measurement techniques to characterize the reliability properties of carbon nanotube-based interconnects.

Early efforts in this project resulted in the design and construction of a microtensile testing system, applicable to free-standing thin films, for generating the purest form of mechanical property data. We developed the silicon-frame tensile specimen and the piezo-actuated tensile tester, which operate successfully for specimens 100 μm wide and larger. As practical testing limits for specimens narrower than this were approached, a new technique, the force-probe tensile test, was developed. The apparatus includes a tensile loading system operable within an SEM. This system has been used on specimens as small as 2 μm in width. While we have halted further development of this capability due to reaching further limits in specimen handling ability, we maintain the tool and continue to use it in working with collaborators who seek assistance.

Other measurement capabilities within this project include d.c. and a.c. electromigration and thermomechanical fatigue, utilized for micro- and nanoscale characterization of industrially relevant materials. Our measurements involving electrical current stressing of chip-level interconnects are being used to explore the relationships between electrical, thermal, and mechanical reliability, with the primary test philosophy being to conduct all evaluations directly on as-manufactured structures. High current density a.c. signals are run at low frequencies through Al- and Cu-based electromigration structures in either passivated or unpassivated states. Controlled joule self-heating results in a cyclic strain due to thermal expansion mismatch between the metal lines and their substrates. The associated deformation then leads to severe topographic distortions in unconstrained lines, and can eventually cause open circuit failure. We investigate the effects of current density, frequency, crystallographic orientation, and encapsulant material. The use of advanced analytical techniques including EBSD, SEM, and TEM has revealed surprisingly similar microstructural damage and failure mechanisms in a.c.-stress and microtensile tests. This suggests that electrical tests may be exploited to produce information about the mechanical characteristics of thin films. If this electrical-mechanical test can be made to produce relevant data, it will be of significant benefit because it will be experimentally convienent to electrically stress specimens of a wide range of sizes, including very small and buried specimens. We have continued to improve our electrical measurements, and have begun SEM studies of the failure mechanisms in electrically-tested damascene copper interconnect lines. An intriguing observation from our work is the growth of grains in metal interconnects that have been subjected to a.c. thermal cycling. We are determining whether this can be

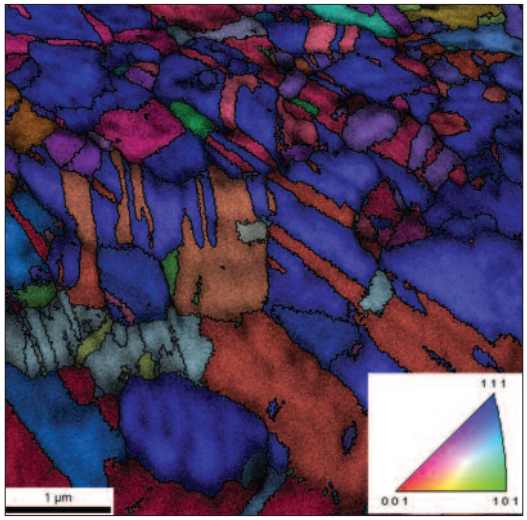

Figure 1. EBSD map of electrodeposited copper film specimen. The colors indicate the surface-normal crystallographic orientation of each pixel, according to the key, inset. Regions of constant color are crystallographic grains. The long, straight, parallel boundaries are twin boundaries.

developed into a method for tailoring local grain structure to impart improved electrical performance.

DELIVERABLES:

- Invited keynote talk, summarizing testing methods, at 7th Pacific Rim International Conference on Advanced Materials and Processes. 3Q 2010
- Conference presentation and/or journal publication on use of a.c. thermal cycling to improve electromigration performance in damascene copper lines. 4Q 2010

ITRS statements suggesting that carbon nanotubes may present solutions to improving interconnect speed, power dissipation, and reliability (Roadmap (2007 Edition), Interconnect, page 50) have driven the extension of our approach to CNT-based systems. We are studying both single CNTs grown directly between two metal contacts as well as patterned CNT bundles that span metal contacts. While the principles we have developed for electrically characterizing metal interconnects apply to CNTs, the microstructural implications are starkly different. For example, since CNTs are known to be able to sustain high current densities for a long time, it may be expected that reliability-compromising material issues could develop within the carbon-metal contact region. Factors such as pre-treating the contact region to improve crystallinity and bonding must be considered. Therefore, we are integrating an extensive amount of TEM characterization into the electrical CNT test development, to obtain a comprehensive understanding of the material response during testing.

DELIVERABLES:

- Journal paper on lifetime behavior of CNT interconnects under high current density stressing. 4Q 2010

Accomplishments

■ Our efforts to develop relevant tests for state of the art interconnect materials are based on first establishing the fundamental materials science of reliability for the systems of interest. Microstructural characterization is therefore critical for defining the applicability of new tests to different materials and properties. Currently, we are improving our measurements for characterizing the microstructure of electrodeposited copper in order to better understand the influence of microstructure on reliability. Figure 1 shows the grain structure of a commercially produced copper film, as mapped out by EBSD. The colors represent local crystallographic orientation, according to the inset. Regions of constant color are single grains. The long, straight, parallel boundaries are twin boundaries.

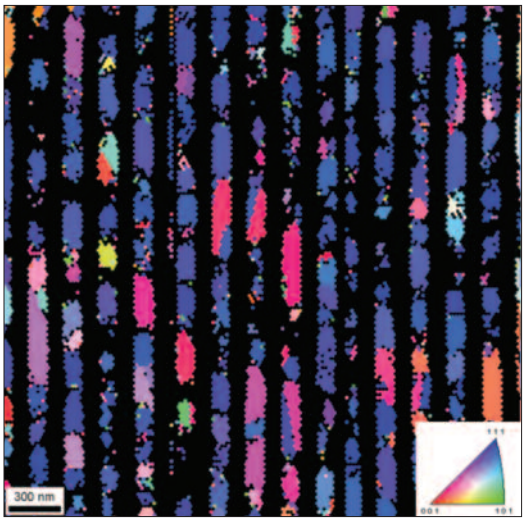

Figure 2. Electron backscatter diffraction map from a section of a 100 nm-wide serpentine line structure. The black regions are the dielectric between the copper lines. The color represents the local crystallographic orientation normal to the plane of the page according to the inserted stereographic triangle. This mapping displays individual grains as colored regions. Note that the grain lengths average about 2.5 times the linewidth.

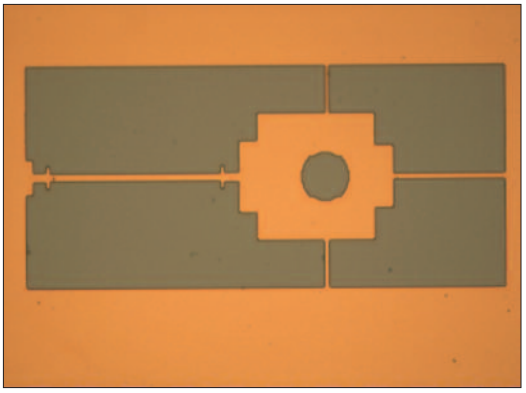

Figure 3. Microtensile specimen of electrodeposited copper produced at NIST. The slender strip on the left is the test section; the tab with the hold is used for loading. The grip section is 10 μm wide by about 200 μm long.

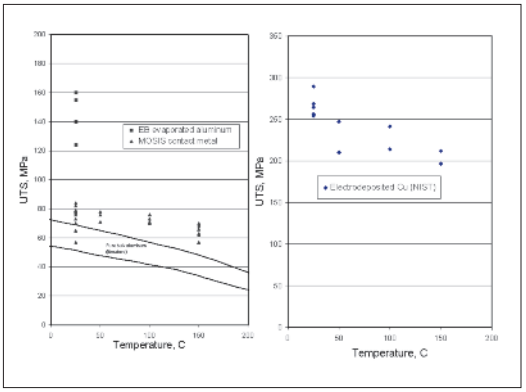

Figure 4. Tensile strength plotted against temperature for microtensile specimens of aluminum contact metal obtained through MOSIS, and electrodeposited copper made at NIST.

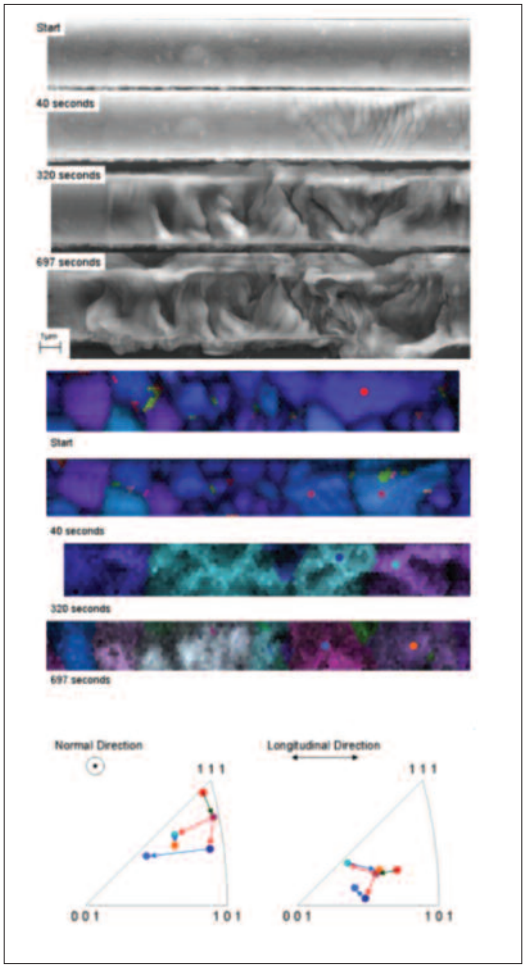

Figure 5. A.C. testing sequence in Al-1Si, showing development of surface offsets, grain size and shape changes, and grain orientation changes, at (0, 40, 320, and 697) seconds of A.C. cycling at about 12 MA/cm^2. Upper images: surface topography by SEM; lower images: same locations, color indicates grain orientation; drawing: changes in crystallographic orientation of grains as indicated.

We found that we could make similar measurements on 100 nm wide copper lines in a damascene structure, Figure 2. The same wafer contained large copper features; these had a grain diameter approximately 2.5 times larger than the grain length along the narrow lines. This result indicates that for the process sequence used on this wafer, the large grain size of the copper overburden did not propagate into the narrow lines. We have learned from our industrial colleagues that our EBSD orientation maps have the highest spatial resolution they have seen - ~ 10 nm.

■ We have demonstrated the applicability of our small-scale microtensile testing techniques to materials now in use within the microelectronics industry - specifically copper, in the form of both sputtered thin films and thick electrodeposits. A microtensile specimen of electrodeposited copper is shown in Figure 3.

We typically find that the strengths are far above the handbook values for pure annealed bulk copper, and the elongations are much lower than the handbook values. For example, increasing the film thickness from 1 μm to 10 μm increases the ductility from around 1 % or less to 5 % or more for a new variety of electrodeposited copper supplied by an industry collaborator. Annealing also changes the tensile properties markedly. We have extended our microtensile test capability to temperatures up to 150 °C. Figure 4 shows ten-

sile strength results for Al-Si contact material, from MOSIS, and electrodeposited copper, made at NIST.

■ Our a.c. tests, typically involving current densities of the order of 10 MA/cm^2, reveal damage phenomena drastically different from that observed in conventional accelerated d.c. electromigration tests. To understand the results, we have pursued crystallographic mapping experiments within a field emission SEM. What has become apparent is the tremendous variation in behavior from grain to grain in a polycrystalline interconnect. We have observed significant growth of selected grains, which are in turn more susceptible to surface offset formation with further cycling (Figure 5), for cases where no rigid dielectric is present.

We have also applied a.c. testing to commercial damascene copper structures. Data from some initial experiments are plotted as lifetime to open circuit vs. cyclic temperature range in Figure 6. On this basis, we found a big difference between vias and lines, but no clear difference between oxide and low-κ dielectric structures. The preliminary conclusion from these tests is that since the combined effects of thermal, electrical, and mechanical stresses need to be accounted for in designing reliable interconnect systems, they must be addressed concurrently in reliability tests as well. Results of our tests in damascene lines also indicate that the a.c. test does in fact excite thermal-mechanical failure mechanisms.

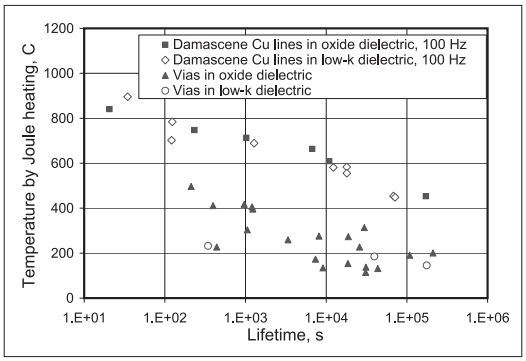

Figure 6. Comparison of lifetimes under high amplitude a.c. of Cu lines and Kelvin vias in damascene structures made with oxide and low-κ dielectric, plotted as cyclic temperature vs lifetime. When plotted in these coordinates, the vias fail at much lower temperatures than the lines in both structures, but the dielectric material does not affect the lifetimes.

Figure 7 shows voids in a damascene copper interconnect line after a.c. stressing. The application of a.c. to copper allows study of void generation; this process is usually obscured in d.c. electromigration tests because the void formation is slower, the failure is more rapid, and the voids move. Preliminary analysis suggests that voids formed by a.c.-induced rapid thermal cycling may be microstructurally similar to those formed by static stress voiding tests. If this is the case, then controlled a.c. stressing may hold potential as an accelerated test for stress voiding.

■ The inevitable approach to dimensional scaling limits for metal interconnects has led to increasing interest in carbon-based materials for interconnect - carbon nanotubes (CNTs) and graphene. As many groups are developing new designs and processing methods for these materials, we are anticipating the need for reliability test methods and data. Two general design philosophies for CNT-based interconnects have emerged: (i) single CNTs spanning closely-spaced metal contacts, and (ii) bundles of CNTs patterned into longer conducting traces. We are adapting our electrical test methods for applicability to both types of structures. A thorough review of the literature has revealed very little in terms of failure mechanisms for CNT-metal systems, even though some people have demonstrated the ability of CNTs to carry high current densities (seemingly indefinitely). Those preliminary findings, while intriguing, may not represent the behavior of CNTs as integrated into operational devices, where interfaces with other materials will be

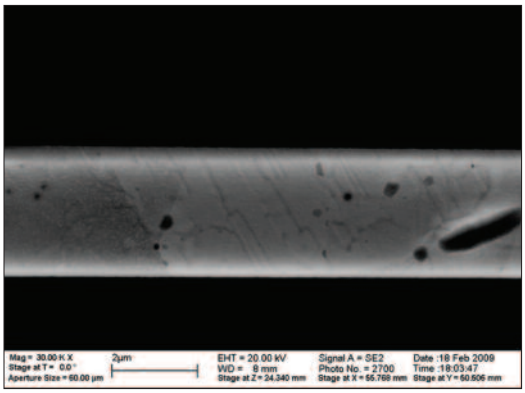

Figure 7. SEM micrograph of a copper damascene line 3 μm wide. This specimen was tested at 100 Hz at a peak current density of 18 MA/cm2. The temperature range was 396 °C, the total von Mises strain range was 0.0091, and the lifetime was 1498 s. Note the voids.

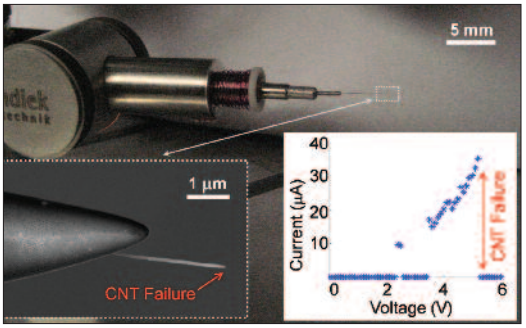

Figure 8. Current-voltage plot from an individual CNT welded to a tungsten probe tip; the failed tube is shown in the inset.

ubiquitous. Figure 8 shows a current-voltage plot from an individual CNT welded to a tungsten probe tip; this multiwalled CNT had failed at a current of approximately 35 µA during a ramping experiment.

Collaborations

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Yung Joon Jung, Northeastern University

Publications

R. L. Graham, G. B. Alers, T. Mountsier, N. Shamma, S. Dhuey, S. Cabrini, R. H. Geiss, D. T. Read, and S. Peddeti, *"Resistivity Dominated by Surface Scattering in Sub-50 nm Cu Wires"* Applied Physics Letters 96, 042116, 2010.

D. T. Read and A. A. Volinsky, *"Measurements for Mechanical Reliability of Thin Films"* Proceedings of NATO Advanced Research Workshop of Security and Reliability of Damaged Structures and Defective Materials, pp. 337-358, 2009.

D. T. Read, R. H. Geiss, and N. Barbosa, *"Constraint Effect in Deformation of Copper Interconnect Lines Subjected to Cyclic Joule Heating"* Journal of Strain Analysis for Engineering Design 44, 543-553, 2009.

R. L. Graham, G. B. Alers, T. Mountsier, N. Shamma, S. Dhuey, S. Cabrini, R. H. Geiss, D. T. Read, and S. Peddeti, *"Resistivity Dominated by Surface Scattering in Sub-50 nm Cu Wires"* Applied Physics Letters 96, 042116, 2010.

D. T. Read and R. H. Geiss, *"Thermal Cycling of Buried Damascene Copper Interconnect Lines by Joule Heating"* Proceedings of NSTI Nanotech 2008, vol. 1, pp. 218-221, 2008.

R. A. Allen, J. C. Marshall, W. A. Baylies, D. T. Read, G. D. Quinn, F. W. DelRio, K. T. Turner, M. Bernasch, J. Bagdahn, "A Standard Method for Measuring Wafer Bond Strength for MEMS Applications" Proc. ECS: E11 - Semiconductor Wafer Bonding 10: Science, Technology, and Applications, Honolulu, HI, United States, 10/12/2008 to 10/18/2008, Vol. 16, No. 8, pp. 449-455.

R. R. Keller, D. C. Hurley, D. T. Read, and P. Rice, "Metrologies for Mechanical Response of Micro- and Nanoscale Systems," in Micro and Nano Mechanical Testing of Materials and Devices, Springer Science+Business Media, edited by F. Yang F and J. C. M. Li, 305-340 (2008).

R. H. Geiss and D. T. Read, *"Microstructure of 100 nm damascene copper overburden and lines,"* in Instrumentation, Metrology, and Standards for Nanomanufacturing, edited by M. Postek and J. Allgair, Proc. of SPIE Vol. 6648 (on CD), 664808-1—664808-8, 2007.

R. H. Geiss and D. T. Read, *"Defect behavior in aluminum interconnect lines deformed thermomechanically by cyclic joule heating,"* Acta Materialia 56 (2), 274-281, 2008.

R. R. Keller, N. Barbosa III,, R. H. Geiss, and D. T. Read, *"An Electrical Method for Measuring Fatigue and Tensile Properties of Thin Films on Substrates,"* Key Engineering Materials, Vols. 345-346 (2007) pp. 1115-1120 (online at http://www.scientific.net).

R. H. Geiss and D. T. Read, *"Need for Standardization of EBSD Measurements for Microstructural Characterization of Thin Film Structures"*, Proceedings of the 2007 International Conference on Frontiers of Characterization and Metrology for Nanoelectronics, edited by D. Seiler et al., AIP Conference Proceedings 931, 168-172, 2007.

D. T. Read and R. H. Geiss, *"Study of Fatigue Behavior of 300 nm Damascene Interconnect using High Amplitude AC Tests,"* in Materials, Process, Integration and Reliability in Advanced Interconnects for Nicro- and Nanoelectronics, edited by Q. Lin, E. Ryan, W. Wu, and D. Yoon, Mat. Res. Soc. Symp. Proc. Vol. 990, 121-126, 2007.

D. T. Read and A. A. Volinsky, *"Thin Films for Microelectronics and Photonics: Physics, Mechanics, Characterization, and Reliability,"* in Micro- and Opto-Electronic Materials and Structures: Physics, Mechanics, Design, Reliability, Packaging, edited by E. Suhir, C.P. Wong, Y.C. Lee, Springer, New York, 2007.

N. Barbosa III, R. R. Keller, D. T. Read, R. H. Geiss, and R. P. Vinci, *"Comparison of Electrical and Microtensile Evaluation of Mechanical Properties of an Aluminum Film,"* Metallurgical Transactions A—Physical Metallurgy 38A (13), 2160-2167, 2007.

R. R. Keller, R. H. Geiss, N. Barbosa III, A. J. Slifka, and D. T. Read, *"Strain-Induced Grain Growth during Rapid Thermal Cycling of Aluminum Interconnects,"* Metallurgical and Materials Transactions A — Physical Metallurgy 38A (13), 2263-2272, 2007.

D. T. Read, R. R. Keller, N. Barbosa III, and R. H. Geiss, *"Nanoindentation Round Robin on Thin Film Copper on Silicon,"* Metallurgical and Materials Transactions A—Physical Metallurgy 38A (13), 2242-2248, 2007.

High Throughput Measurements of Thermoelectric Materials for Cooling Applications

Technical Contacts:
M. L. Green
W. Wong-Ng

20Goals

The objective of this project is to develop standard reference materials (SRMs), measurement methodologies, and comprehensive data sets (Seebeck coefficient, electrical conductivity, thermal conductivity) for thin film and bulk thermoelectric materials to validate measurement accuracy. This will lead to a better understanding of the structure/property relationships and the underlying physics of novel thermoelectric materials, and enable their development for solid state cooling applications. Our approach will facilitate comparison of thermoelectric data between leading laboratories and accelerate the commercialization of these materials.

Customer Needs

One of the most important impediments to further scaling of microelectronic devices is the removal of the prodigious heat dissipated as a result of their operation. Passive heat removal is no longer an option; device mounts and packages must employ active heat removal technology.

Thermoelectric materials, i.e., materials that can directly interconvert thermal and electrical energy, are being developed for two applications: solid state refrigeration, and vehicular engine waste heat recovery for electrical power generation. Solid state refrigeration of microelectronic devices using thermoelectric devices would result in greater operational efficiency and device reliability for the $120B U.S. semiconductor industry. In addition, thermoelectric based cooling devices are environmentally friendly, require minimal maintenance (no moving parts), and reliably offer quiet and compact operation.

Technical Strategy

Currently, the energy conversion efficiency of well-established, bulk thermoelectric materials is too low (<5 %) for device cooling applications. There have been reports of higher conversion efficiencies in thin film materials, but the material properties affecting conversion efficiency, i.e., Seebeck coefficient, S, electrical conductivity, σ, and thermal conductivity, κ, are difficult to quantify or verify in thin film materials. Although there will be only limited applications for thin film thermoelectric cooling devices (because a ΔT of only 40 °C across a 2 μm film represents a thermal gradient of 2×10^7 °C/m, which is not possible to sustain by known thermal management techniques), thin films, especially combinatorial thin films, are useful vehicles for screening of candidate thermoelectric materials.

Our technical strategy is to develop standard reference materials (SRMs), measurement methods, and combinatorial materials methodologies to accelerate the commercial introduction of thermoelectric materials to the microelectronics market place. Thermoelectric SRMs and measurement methods will allow for interlaboratory validation of data, leading to more rapid commercialization of thermoelectric materials for solid-state cooling applications. Measurement methods, especially for the case of thin film thermoelectric materials, are not standardized, and there are currently no methods to accurately and reproducibly (laboratory to laboratory) measure the material properties that determine thermoelectric conversion efficiency, i.e., Seebeck coefficient (S), resistivity (ρ), and thermal conductivity (κ). High throughput combinatorial methodologies will be employed to generate comprehensive data sets (S, ρ, κ) for industrially relevant bulk and thin film thermoelectric materials. We will also collaborate with several industrial, university and government laboratories to generate the appropriate data sets and standard reference materials.

DELIVERABLES:

- Complete design of high temperature Seebeck coefficient and electrical resistance screening tool (1Q 2010)
- Complete hardware development of high temperature Seebeck measurement tool (1Q 2010)
- Complete software development of high temperature Seebeck measurement tool (2Q 2010)
- Complete development of the thermal conductivity screening tool for combinatorial films (3Q 2010)
- Build high temperature Seebeck coefficient and electrical resistance screening tool (4Q 2010)

Accomplishments

In addition to equipping a new laboratory for thermoelectric property measurements, we ac-

complished two other goals: the certification of a bulk Standard Reference Material (SRM) for measurement of the low temperature Seebeck coefficient (chosen through an interlaboratory round robin survey of two candidate materials), and the development of two new thermoelectric metrology apparatuses, a scanning tool for Seebeck coefficient and resistivity measurements, and a scanning frequency domain thermoreflectance tool for thermal conductivity measurements. Both are designed to be combinatorially friendly, i.e., they are measurement techniques that can be made locally and rapidly on a bulk or thin film "library" sample.

The Seebeck coefficient round robin data were analyzed using a parametric model to generate common fitted curves for data generated from various laboratories (laboratories were at AIST (Japan), Michigan State University, Hi-Z Technology Corp., Quantum Design Corp., Clemson University, Naval Systems Weapons Center, U. Maryland, Oak Ridge National Labs, University of South Florida, GM Corp., and University of Michigan) using different measurement techniques and samples from the same batch. Of the two candidate materials, Bi_2Te_3 and Constantan (a copper-nickel alloy), we found that the coefficient of variance for Bi_2Te_3 was smaller across the entire temperature range compared to that of Constantan. Bi_2Te_3 also has a larger Seebeck coefficient than Constantan. We have therefore developed a Seebeck coefficient Standard Reference Material (SRM™), Te-doped Bi_2Te_3 (provided by Marlow Industries), to validate measurement accuracy.

Next, an automated Seebeck coefficient screening tool has been successfully designed and constructed. The tool consists of a probe and an automated translation stage to move the probe in the x, y, and z directions. This tool takes as little as 20 seconds to measure both electrical conductivity and Seebeck coefficient at each sample point; thus, over 1000 sample points can be measured within 6 hours. The tool's measurement capability has been demonstrated for a ternary composition library film of the thermoelectric system $(Ca\text{-}Sr\text{-}La)_3Co_4O_9$. The power factor (equal to the square of the Seebeck coefficient divided by the resistivity) for this material peaks between the Sr- and La-rich regions as shown in Fig. 1. We are currently modifying the thermoelectric probe to further decrease the thermal

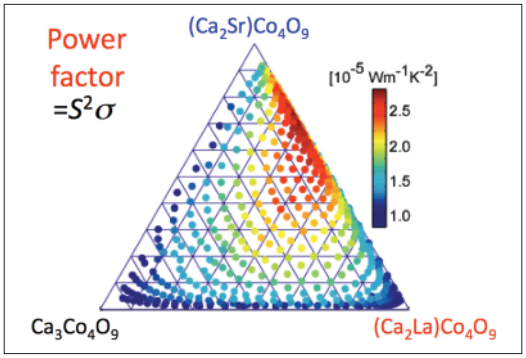

Figure 1. Power factor of a $(Ca,Sr,La)_3Co_4O_9$ film.

measurement uncertainty, and for use at elevated temperatures to enable screening of combinatorial films at their actual operating temperatures.

To complement the Seebeck coefficient screening tool, we have also developed a scanning frequency domain thermoreflectance apparatus that can rapidly and locally (10 micrometer spot size) measure the thermal conductivity of combinatorial thin films. The principle of this technique is illustrated in Fig. 2. To do this, the thermoelectric film is coated with a 100 nm molybdenum layer and locally heated by an intensity modulated (1 MHz) infrared laser; the thermal response of the film is detected by the reflected beam of a second (probe) laser. Evaluation of the phase lag between the thermoreflectance and the heating laser signals enables one to determine the thermal effusivity b, equal to $(\kappa c\rho)^{1/2}$, where c is the specific heat, and ρ the density. A thermal effusivity calibration curve was obtained from bulk samples of SiO_2, $SrTiO_3$, $LaAlO_3$, Al_2O_3, and Si. Using this calibration, and applying a two layer thermal mathe-

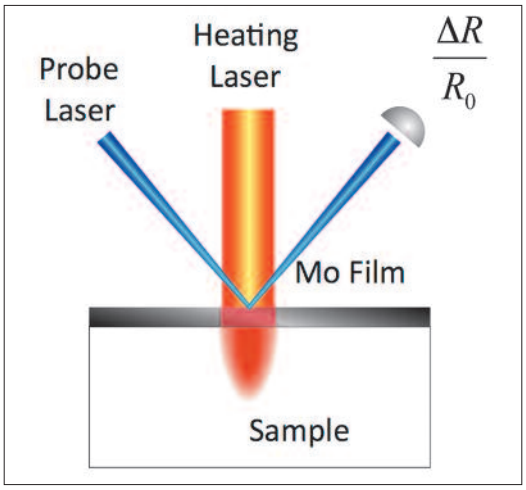

Figure 2. Principle of the frequency domain thermoreflectance technique.

matical model, the thermal conductivity of several materials systems have been measured. The thermal conductivity of an yttria (Y_2O_3)-containing ternary oxide film was first determined. The measured value, 11.96 $J(Kms)^{-1}$, is within about 10 % of the reported value of 12.87 $J(Kms)^{-1}$.

Recently we have succeeded in expanding the capability of the tool to screen thermal conductivity of combinatorial films. Combining the thermal conductivity data from this thermoreflectance apparatus and the thermoelectric screening probe, we can then calculate the energy conversion efficiency for different compositions on the combinatorial film.

The continued development of new thermoelectric materials for high temperature (300 K to 1200 K) power conversion applications requires reliable and accurate characterization of the electrical and thermal transport properties. The deceptive simplicity of measuring the Seebeck coefficient has led to the implementation of numerous non-standardized practices that have further complicated the interlaboratory confirmation of reported high

Figure 3. High-temperature Seebeck coefficient measurement tool.

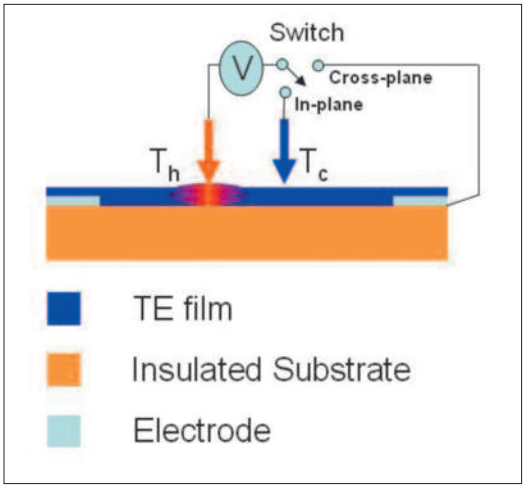

Figure 4. Schematic of the high-temperature Seebeck coefficient screening tool.

conversion efficiency materials in this temperature range. To address these challenges, we have developed an improved thermoelectric probe to systematically evaluate and compare these different characterization methodologies and arrangements. This probe concurrently measures resistivity and Seebeck coefficient from room temperature to 1200 K in a parabolic infrared furnace, incorporating an advanced ceramic probe design, a novel isothermal terminal block, and the sensitive instrumentation required to effectively manage uncertainty in this temperature regime. The apparatus will be used to certify an additional Seebeck coefficient SRM for use at high temperature. Figure 3 illustrates some of the key features of this apparatus.

We are also expanding our thermoelectric measurement capabilities by developing an advanced high temperature thermoelectric screening tool that will concurrently measure resistivity and Seebeck coefficient from room temperature to 900 K, based on the room temperature screening tool prototype. The advanced high temperature screening tool will have improved measurement accuracy and spatial resolution (less than 1mm) in thermoelectric power factor scanning on combinatorial films. Also, the new screening tool is designed to scan combinatorial films in both in-plane and cross-plane direction. A schematic of the apparatus is shown in Fig.4. Final construction of the apparatus is proceeding, and upon completion, will be used to explore and optimize thermoelectric properties for potential candidate materials by a combinatorial approach at high temperature (300 K to 900 K).

Collaborations

Low temperature Seebeck coeffiecient round robin study with eleven labs (AIST (Japan), Michigan State University, Hi-Z Technology Corp., Quantum Design Corp., Clemson University, Naval Systems Weapons Center, U. Maryland, Oak Ridge National Labs, University of South Florida, GM Corp., and University of Michigan).

High temperature Seebeck coefficient effort started with GM Corporations.

Publications

W. Wong-Ng, G. Liu, J. Martin, E. Thomas, N. Lowhorn, and M. Otani, *"Phase Compatibility of the Thermoelectric Compounds in the Sr-Ca-Co-O System,"* J. Appl. Phys. 107, 033508 (2010).

X. Shi, Jiong Yang, S. Bai, Jihui Yang, H. Wang, J. R. Salvador, W. Zhang, L. Chen, and Winnie Wong-Ng, *"On the Design of High Efficiency Thermoelectric Type I Clathrates through Transition Metal Doping,"* Adv. Functional Mater. 20(5), 755-763 (2010).

W. Wong-Ng, J.A. Kaduk, and M. Isobe, *"Reference X-ray Powder Diffraction Pattern of a New High-Pressure Phase, $CaCo_2O_4$,"* Powd Diff. 24(4) 343 (2009).

S. Wang, A. Venimadhav, S. Guo, K. Chen, Q. Li, A. Soukiassian, D.G. Schlom, X.Q. Pan, W, Wong-Ng, M.D. Vaudin, D.G. Cahill, and X.X. Xi, *"Structural and thermoelectric properties of $Bi_2Sr_2Co_2Oy$ thin films on $LaAlO_3$ (100) and fused silica substrates,"* Appl. Phys. Lett. 94 022110 (2009).

E.L. Thomas, W. Wong-Ng, D. Phelan, and J.N. Millican, *"Thermopower of Co-doped $FeSe_{0.82}$"* J. Appl. Phys., 105 (7), 073906 (2009).

N. Lowhorn, W. Wong-Ng, Z.Q. Lu, E. Thomas, M. Otani, M. Green, N. Dilley, J. Sharp, T.N. Tran, *"Development of a Seebeck Coefficient Standard Reference Material"* Appl. Phys. A DOI 10.1007/s00339-009-5191-5 (2009).

Z. Q. J. Lu, N. D. Lowhorn, T. N. Tran, J. Martin, G. S. Nolas et al., *"Statistical Analysis of a Round-Robin Measurement Survey of Two Candidate Materials for a Seebeck Coefficient Standard Reference Material,"* J. Res. Natl. Inst . Stand. Technol., 114, 37 (2009).

M. Beekman, J.A. Kaduk, J. Gryko, W. Wong-Ng and G. S. Nolas, *"Synthesis and Characterization of Framework-Substituted $Cs_8Na_{16}Cu_5Ge_{131}$ Type II Clathrate,"* J. of Alloys and Comp. 470, 365 (2009).

Talks

Thermoelectric and Thermophysical Metrology for Energy Conversion Applications, US-Japan Symposium on International Standardization Toward a Low Carbon Society, February 15, 2010, Tsukuba, Japan (J. Martin)

Evaluation of the methodologies in Seebeck coefficient metrology, March American Physical Society Meeting, Porland, OR, March 19 2010 (J. Martin)

Recent Metrology Research of Thermoelectric Materials at NIST, MS&T 2009, Pittsburgh, PA, October 25-29, 2009 (W. Wong-Ng)

Phase Relation Studies of Energy Materials, MS&T 2009, Pittsburgh, PA, October 25-29, 2009 (W. Wong-Ng)

Development of a Standard Reference Material (SRM□) for Low Temperature Seebeck Coefficient (MRS Spring meeting, San Francisco, CA, April 13-17, 2009 (W. Wong-Ng)

Recent NIST Thermoelectric Research, Interagency Power Group meeting in Arlington, VA April 1, 2009 (W. Wong-Ng)

Phase Equilibria and Structure/Thermoelectric Properties of Compounds in the Ca-Sr-Co-O System (PACRIM 2009, Vancouver, BC, Canada, June 1-5, 2009 (W. Wong-Ng)

Recent Metrology Developments at NIST, ICT2009, July 26-30, Freiburg, Germany (W. Wong-Ng)

Combinatorial Study of Thermoelectric Materials, American Chemical Society, Aug. 17-21, 2009 (W. Wong-Ng)

Survey of High Temperature Thermoelectric Metrology, MRS, San Francisco, CA, April 16, 2009 (J. Martin).

Bi_2Te_3 as a Low Temperature Seebeck Coefficient Standard Reference Material (SRM™), MRS, San Francisco, CA, April 16, 2009 (W. Wong-Ng).

Overview of NIST Thermoelectric Research, 3rd World Materials Research Institute Forum & Energy Symposium (WMRIF), NIST, Gaithersburg, MD June 22-25, 2009 (W. Wong-Ng)

Pb-Free Surface Finishes for Electronic Components: Sn Whisker Growth

Technical Contacts:
W. J. Boettinger
K.-W. Moon
G. R. Stafford
M. E. Williams

"NIST contributions to industry-based tin whisker experiments have helped provide valuable information on the processes responsible for whisker growth. In current iNEMI experiments electron backscatter diffraction (EBSD) measurements by NIST on electroplated tin will be used to correlate the crystallographic orientation of tin grains with their propensity to grow tin whiskers."

Dr. Tom Woodrow,
Associate Technical Fellow
Boeing Research and Technology
Seattle, WA 98124-2207

Goals

The microelectronic industry is faced with an extreme reliability issue due to tin (Sn) whisker induced failures. This project is providing data and materials measurements to improve the reliability of solder interconnects degraded by the switch to lead-free (Pb-free) technology. In particular the state of compressive stress and the localized creep response (whisker growth) of Sn-based, Pb-free electrodeposits are being measured. Industry will use these measurement methods and data to modify processing conditions to mitigate the formation of Sn whiskers.

Customer Needs

Sn is widely used as a coating in the electronics industry because it provides excellent solderability, ductility, electrical conductivity, and corrosion resistance. However, Sn whiskers have been observed to grow spontaneously from Sn electrodeposits and are known to cause short circuits in fine pitched pre-tinned electrical components. In the 1960s, the addition of a few percent of Pb to Sn was found to greatly reduce the tendency to form whiskers. However, recent demand for Pb-free surface finishes for ecological reasons has renewed interest in understanding whisker growth and developing whisker mitigation strategies. It is widely recognized that compressive stress is a necessary, but insufficient, condition for whisker growth.

The U.S. microelectronics industry needs a method to measure stress in the Sn electrodeposited surface finishes of electronic components to predict the propensity of whisker growth before these components are assembled on circuit boards to prevent the loss of both revenue and life from Sn whisker failures. The 2009 International Electronics Manufacturing Initiative (iNEMI), the 2009 IPC technology roadmap and the Department of Defense funded 2009 Lead Free Electronics Manhattan Project clearly articulate the need for Sn whisker research. In order to prevent or mitigate whisker growth, workshops sponsored by industry and academia have reached a consensus list of concerns: understand the influence of electroplating conditions, grain structure/shape/orientation, and compressive stress in the electrodeposits, intermetallic compound (IMC) formation at the Sn/Cu interface, diffusion of Sn, and thermal cycling effects on electroplated components.

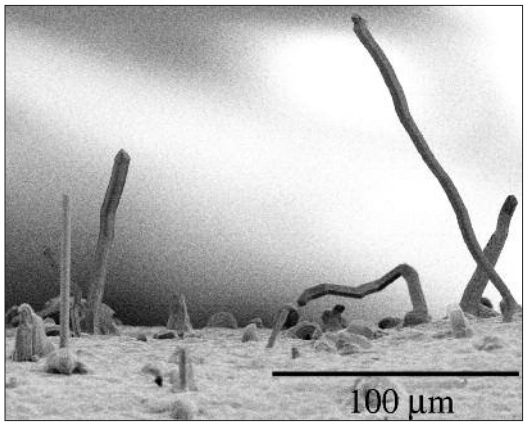

Figure 1. Side view of Sn whiskers on the surface of a bright SnCu electrodeposit.

Mitigation strategies being investigated include the elimination of columnar grain shape and elimination of intermetallic reaction with the substrate. Focused ion beam (FIB) milling removes metal and reveals a cross section of the internal microstructure so that changes in grain structure can be directly correlated to whisker growth. 3-D reconstruction of the FIB cross sectioning cuts has provided insight into the deposit characteristics around the surface eruptions of hillocks, not considered a reliability threat because of their low aspect ratio, and whiskers. Examples of typical hillocks and whiskers are shown in Figures 1 and 2. Also models of stress accumulation and relaxation are used to interpret the stress measurements and describe whisker/hillock growth.

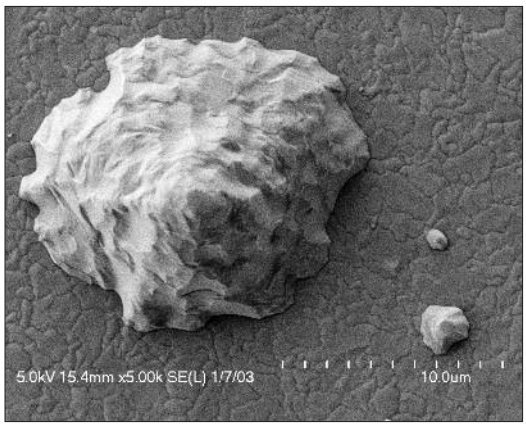

Figure 2. Top view of Sn hillocks on the surface of a 15 um thick bright Sn electrodeposit.

Technical Strategy

Our work on Pb-free electrodeposits is focused on the measurement of stress and modeling Sn grain growth. In the past we have used two independent methods to the measure stress in electrodeposited Sn surface finishes: (1) X-ray measurement and (2) optical stress measurement during and after electrodeposition by wafer curvature technique. Now we have developed a method to combine these two measurement techniques and simultaneously measure the post-deposition stress in Sn and Sn alloy electrodeposits with varying thicknesses as a function of time. Each technique measures a different aspect of the stress; curvature measures the average stress of the entire deposit and x-ray diffraction measures the strain in the top 2 μm of the deposit. Although it is easy to obtain stress values from these techniques, understanding the source of measurement errors is undeveloped. Errors can be a significant fraction of the measured quantity. Electroplated Sn has a preferred crystallographic orientation that can vary depending on plating conditions. Sn is a low melting metal (0.6 TM at RT), with a low yield strength (≈ 30 MPa) that creeps at room temperature. These factors as well as geometrical, diffraction, and optical subtleties complicate both measurement methods.

In addition we will combine our micro-indentation technique, which artificially induces stress in the electrodeposit and stimulates Sn whisker growth, with the microdiffraction beamline at the Argonne National Lab Advanced Photon Source to measure grain orientation and strain around whiskers grown on demand. Modeling efforts are being used to gain fundamental insight into the processes that cause the upward thrust of the Sn during whisker growth.

DELIVERABLES:

- Complete manuscript, "Simultaneous and Time-Resolved Measurement of Stress in Sn and Sn-Cu Electrodeposits Using Cantilever Beams and X-Ray Diffraction." 1Q 2011
- Develop an SEM micro-indentation system to artificially stimulate whisker growth on a Sn electroplated surface finish to observe whisker formation in real time. 4Q 2010
- Complete manuscript, "Sn Whisker Growth: Artificially Induced Stress from Indentation." 4Q 2010

Accomplishments

■ *Stimulation of Sn Whisker Growth Using Micro-Indentation* - Sn whiskers can grow spontaneously from Sn electrodeposits under various conditions. The necessary compressive stress for this growth can come from different sources such as the deposition process, intermetallic growth, or an external mechanical force. We have developed a controlled load micro-indentation technique to artificially stimulate Sn whisker growth on a pure Sn electroplated surface finish on a pure Cu substrate. The whisker location, the initial start time of the growth and the time duration of the growth is well documented. The formation of whiskers in the indentation location occurs within minutes and they grow for approximately 3h to 4h hours. Whisker growth changes with different applied loads. These results indicate a stress threshold for whisker growth. The residual stress field in the Sn has been analyzed with the finite element method and the results suggest the importance of bi-axial compressive stress for whisker and hillock growth.

■ *Simultaneous Measurement of Stress in Electrodeposits* - The simultaneous measurement of stress in bright Sn and Sn-Cu electrodeposits as a function of time was performed using two methods; sin2ψ x-ray diffraction and cantilever beam curvature. The sin2ψ x-ray technique employed an area detector to reduce acquisition time. The x-ray diffractometer is also equipped with a laser device that has been configured to measure the cantilever beam curvature. The stress measured by the two techniques are different: the x-rays (Cu K_α) measure the lattice strain in the top 2 μm of the electrodeposit and the curvature measures the average stress of the entire electrodeposit plus the interfacial intermetallic compound that forms between the Sn and the Cu substrate. Stresses are in the range between 0 MPa and -35 MPa vary considerably with time over a period of 3 days and depend strongly on deposit thickness (3 μm to 15 μm). The stress values obtained simultaneously from the two measurement techniques are compared. A model is being developed to reconcile the different measurements and their time dependences. Most interesting are the results for 7 μm thick deposits that generally show a short term relaxation of the compressive stress followed by a long time increase in compressive stress. The initial stress is due to the plating process itself. This stress begins to relax but at a later time the compressive stress increases due to slow growth of the Cu^6Sn^5 intermetallic between the Sn and the Cu substrate. This is consistent with the ideas of Boettinger, et al., 2005.

■ *Modeling* - The mechanisms of hillock and whisker growth remain largely unknown. In stressed solids, surface evolution is often driven by grain boundary diffusion and can result in growth of hillocks and whiskers. Figure 3 shows possible diffusion paths of Sn atoms to feed the base of a whisker grain. The 3-D path of Sn atoms to relieve stress is along columnar grain faces (arrows) within the deposit. Accretion of Sn on the wedge-shaped grain faces forces the whisker/hillock above the deposit surface.

As a preliminary attempt at modeling this situation, we have preformed molecular dynamic simulation of a simpler geometry. These simulations have been performed to understand the conditions (stress, temperature, grain boundary diffusion, surface diffusion) under which the hillock/whisker growth processes can be initiated. The simulated geometry was a tri-crystal with a wedge-shape surface grain penetrating down the triple line. The applied compressive stress caused the wedge grain to grow upward and out of the surface as in whisker/hillock growth. It was determined that only two of the three interior grain boundaries were capable of supplying Sn atoms to the base of the whisker/hillock grain. Thus the whisker/hillock was pushed up but at an angle to the free surface.

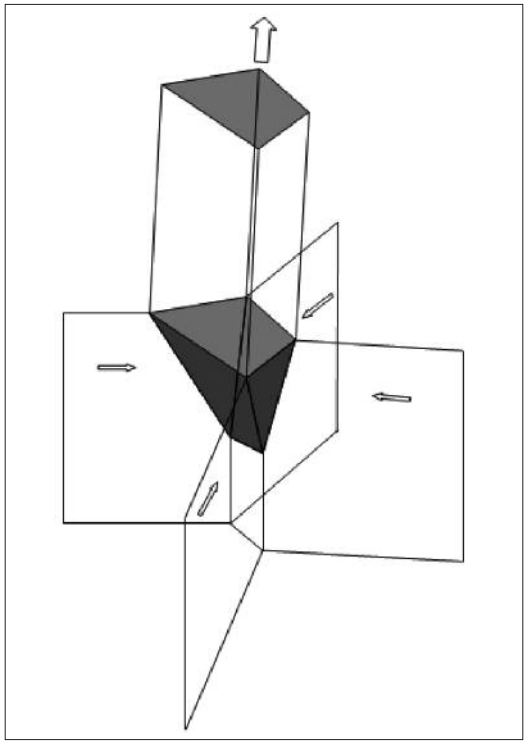

Figure 3. The 3-D path of Sn atoms to relieve stress is along columnar grain faces (arrows) within the deposit. Accretion of Sn on the wedge-shaped grain faces forces the whisker/hillock above the deposit surface.

■ *Focused Ion Beam 3-D Reconstruction* - Whiskers are currently understood to be caused by diffusion of Sn from the interior of the Sn coating along the complex 3-D grain boundary network toward specific but sparse surface grains, which are pushed out of the deposit by accumulation of Sn at their base just beneath the surface. Other surface eruptions and conical hillocks form by the same mechanism but are not a reliability threat because of their low aspect ratio. The diffusion is caused by compressive stress gradients that develop in the Sn due to the plating process itself and due to the reaction of the Sn with the underlying Cu layer to from a Cu^6Sn^5 intermetallic compound. Figure 4 shows a 3-D FIB reconstruction with a cutaway to reveal the internal structure of a Sn hillock and surrounding grains of a bright Sn electrodeposit on a copper substrate. Characterization of the 3-D Sn grain boundary network and the location and shape of the Cu^6Sn^5 particles beneath whiskers and hillocks will assist in the determination of what is unique about the particular Sn grain that develops into a potentially dangerous filament whisker and why it is different from the hundreds of surrounding Sn grains that remain dormant.

■ *Participation in the Lead-Free Manhattan Project* - NIST participated on a team of sixteen nationally recognized expert scientists and engineers on Phases 1 & 2 of the Lead-Free Electronics Manhattan Project (LFMP), sponsored by the Office of Naval Research and the Joint Defense

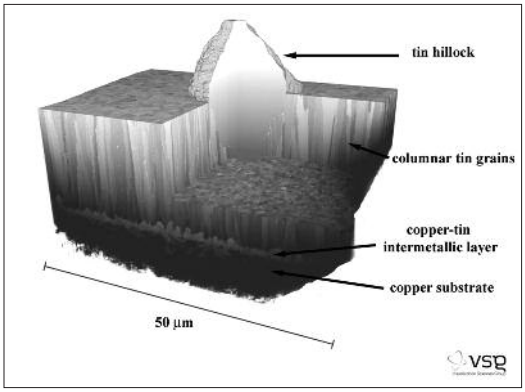

Figure 4. 3-D FIB reconstruction, with cutaway to reveal the internal structure of a Sn hillock and surrounding grains of a bright Sn electrodeposit on a copper substrate.

Manufacturing Technology Panel, to address the serious reliability threat from lead-free solders and surface finishes that are infiltrating critical aerospace and defense systems. In April 2009 Phase 1 of the LFMP identified gaps in current industry best practices for the use of Pb-free solders and surface finishes in the high reliability aerospace and defense programs. Then in August 2009, Phase 2 produced a three year roadmap that addressed the reliability and sustainment risks identified in Phase 1. The third phase of this project, renamed the Lead-free Electronics Risk Reduction Program, has articulated eighty research and development (R&D) tasks needed to address the lead-free technology knowledge gaps. Funding is being sought to implement this R&D program.

■ *Participation in iNEMI working groups* - NIST remains an active participant in the Sn Whisker Group with bi-weekly teleconferences and round robin experiments (members include Alcatel-Lucent, Cisco Systems, Cookson, Delphi Delco, Freescale, Hewlett Packard, IBM, Intel, Intersil, IPC, Motorola, Rohm & Haas Electronic Materials, Soldering Tech, Solectron, Sun Microsystems, Texas Instruments, and Tyco Electronics).

Collaborations

NIST and the Visualization Sciences Group located in Burlington, MA are working together on focused ion beam (FIB) 3-D reconstruction of Sn electrodeposits to characterize the Sn grain boundary network and the location and shape of intermetallic particles beneath whiskers and hillocks to assist in the determination of what is unique about the particular Sn grain that develops into a potentially dangerous filament whisker and why hundreds of surrounding Sn grains remain dormant.

Identification with the Visualization Sciences Group does not imply recommendation or endorsement by the National Institute of Standards and Technology, nor does it imply that the products identified are necessarily the best available for the purpose.

Publications

Marsh, M.P (Visualization Sciences Group, Burlington MA.), Williams, M.E. Moon, K-W, and Boettinger, W.J., *"Image Processing and Quantification in FIB Reconstructions: Tin Whisker and Hillock Case Study,"* Conference Proceedings Microscopy & Microanalysis 2010, August 2010.

Stafford G.R., Shin J.-W., Williams M.E., Moon K.-W., and Boettinger W. J., *"Whisker Formation in Pb-Free Surface Finishes,"* Conference Proceeding for the 217th ECS Meeting in Vancouver, BC, Canada, April 28, 2010.

Moon, K.-W., Kim, S.-K., Williams, M.E., Boettinger, W.J., and Stafford, G.R., *"Effect of Current Density and Electrolyte Concentration on Hillock Growth from Pure Sn Electrodeposits,"* In press J. of Applied Electrochemistry, March 2010.

E. Sandnes, M.E. Williams, M.D. Vaudin and G.R. Stafford, *"Equi-Axed Grain Formation in Electrodeposited Sn-Bi,"* Journal of Electronic Materials, v 37, n 4, April, 2008, p 490-497.

K.-W. Moon, U.R. Kattner, C.A. Handwerker, *"The Effect of Bi Contamination on the Solidification Behavior of Sn-Pb Solders,"* Journal of Electronic Materials, Vol. 36, No. 6, pp.676-681, June 2007.

E. Sandnes, M.E. Williams, U. Bertocci, M.D. Vaudin and G.R. Stafford, *"Electrodeposition of Bismuth from Nitric Acid Electrolyte,"* Electrochimica Acta, Vol. 52, Issue 21, pp. 6221-6228, June 2007.

K.-W. Moon, U.R. Kattner, C. A. Handwerker (Purdue Univ.), *"Chapter 2: Fundamental Properties of Pb-Free Solder Alloys,"* Springer Press, in Pb-Free Soldering, ed J.S. Bath, ISBN978-0-387-32466-1, 2007.

G. R. Stafford, C. Beauchamp, U. Bertocci, E. Sandnes, and W. J. Boettinger, *"Sn Whisker Formation: Stress Generation at the Sn-Cu Interface,"* Spring MRS Meeting, Symposium E: Pb-Free and RoHS-Compliant Materials and Processes for Microelectronics, San Francisco, California, April 9-13, 2007.

M.E. Williams, K-W Moon, W. J. Boettinger, D. Josell, and A. Deal (Lehigh University), *"Hillock and Whisker Growth on Sn and SnCu Electrodeposits on a Substrate Not Forming Interfacial Intermetallic Compounds"*, Journal of Electronic Materials, Vol. 36, No. 3, pp.214-219, Feb. 2007.

W. J. Boettinger, U. R. Katttner, K.-W. Moon and J. H. Perepezko (U. of Wisconsin, Madison), *"Recommended Practice Guide for Differential Thermal Analysis (DTA) and Heat Flux Differential Thermal Analysis (DSC) Measurements of Alloy Melting and Freezing,"* NIST Special Publication Series 960-15, Feb. 2007.

G. R. Stafford, M. E. Williams, C. E. Johnson, K.-W. Moon, U. Bertocci, O. Kongstein, and W. J. Boettinger, *"Whisker Formation in Pb-free Surface Finishes,"* ECS Transactions, v 1, n 13, Green Electrodeposition, 2006, pp 71-85.

M. E. Williams (NIST), V. Schroeder (HP), P. Bush (SUNY

Buffalo), N. Vo (Freescale), H. L. Reynolds (Sun Microsystems), “Tin Whisker Test Method Development,” IEEE-Transactions on Electronics Packaging Manufacturing, V29, 4, 2006, pp 231-238.

Process Metrology Program

Device scaling has been the primary means by which the semiconductor industry has achieved unprecedented gains in productivity and performance quantified by Moore's Law. Until recently only modest changes in the materials used have been made. The industry was able to rely almost exclusively on the three most abundant elements on Earth — silicon, oxygen, and aluminum.

Copper is now predominantly the conductor of choice over aluminum because of its intrinsic higher conductivity. A variety of low-dielectric constant materials are being introduced to reduce parasitic capacitance, replacing silicon dioxide. As dimensions continue to shrink, the traditional silicon dioxide gate dielectric thickness has been reduced to the point where tunneling current has become significant and is compromising the performance of the transistors. This is requiring the introduction of higher dielectric constant materials. Initially the addition of nitrogen to the gate material was sufficient, but now more exotic materials such as transition metal oxides, silicates, and aluminates are being introduced. Additionally, the gate conductor, traditionally polysilicon, is being replaced by metal or metal silicide to eliminate the polysilicon depletion effect. With the replacement of the traditional silicon dioxide/polysilicon gate stack processes with materials capable of supporting ever shrinking geometries, the task of the industry becomes more difficult. The overall task represented by the projects below reflects the need for analytical techniques with unparalleled spatial resolution, accuracy, robustness and ease of use.

Atomic layer deposition processes are increasingly being used for high quality thin dielectrics and conductors. Techniques for understanding the deposition mechanisms and characterizing the compounds that are formed are being developed. Theoretical studies elucidating the thermodynamics and quantum mechanical properties of these compounds are being conducted.

Physical Properties of Metal-Organic Precursors

Goals

Making a microprocessor requires more than half of the elements in the periodic table. Example uses of metallic elements include conductors (Cu), dielectric layers (HfO_2), and barriers (TaN). The metal often arrives at the surface of the silicon wafer as the vapor of a metal-organic precursor compound. The precursor's most important physical property is vapor pressure because it controls the behavior of the vapor delivery device. The goals of this project are:

1. Produce accurate vapor pressure data for relevant precursors at temperatures as high as 200 °C. Such data will improve the modeling of chemical vapor deposition processes and the design and use of bubblers and other devices that deliver precursor vapors.

2. Characterize the thermal stability of metal-organic precursors. The design of these compounds is often challenged by a compromise between stability and adequate volatility.

3. Devise a method for measuring metal-organic vapor pressures that is suitably accurate yet more convenient than existing methods, which are labor intensive and prone to error.

Customer Needs

Precursors for chemical vapor deposition are frequently compounds that, until recently, were either rare or nonexistent. Their vapors are delivered to the process chamber either by direct injection (flash evaporation) or by flowing a carrier gas through a reservoir ("bubbler") that contains the precursor. Enabling the systematic and efficient use of such precursors has created an industrial need for improved property data of these specialty chemicals. Designers and users liquid delivery devices could use such data to optimize the performance of those devices.

Vapor pressure determines the concentration of the precursor-carrier mixture, and it sets a lower limit on the wall temperature of the delivery line and the process chamber. Although high vapor pressures are preferred, the acceptable range is wide. For example, when heated to 100 °C, the vapor pressure of the widely used liquid TEOS (tetraethyl orthosilicate) is 12 kPa. In contrast, a candidate precursor might be considered even if its vapor pressure were 100 times lower.

Other important properties include liquid viscosity and thermal stability. Viscosity can affect the performance of injection systems. Thermal stability is important because the precursor's decomposition rate may limit the process's upper operating temperature and thereby the vapor pressure.

Technical Strategy

NIST will identify and assess the quality of existing data for the vapor pressures of compounds such as Hf $(CH_3CH_2N)_4$ (acronym TEMAH). NIST will also fill gaps in the existing data by developing apparatus capable of accurate vapor pressure measurements. The resulting accurate data will be provided to industry. NIST also will characterize the thermal stability of these compounds and investigate alternate methods to measure vapor pressure.

DELIVERABLES:

- Test system for handling hazardous metal-organic samples. 1Q 2010

The system includes a fume hood for storage, a glove box for loading samples, a zeolite trap for absorbing pumped vapor, and a burner tube for oxidizing vapors desorbed from the trap. Additional components include pressure and temperature interlocks for the oven power and plumbing to exhaust the burner tube, the vacuum pump, the oven, and the mass spectrometer. All components of the system have been tested successfully.

DELIVERABLES:

- Describe apparatus for measuring vapor pressure of metal organic compounds. 2Q 2010

The description, which will be submitted to a peer-reviewed journal, will include measurements

Technical Contacts:
R. Berg

"There is a huge number of liquid or solid organic and organometallic compounds that can be used as precursors for thin films deposition by CVD and ALD gas phase processes. Unfortunately only very few vapor pressure data are available for these molecules and it makes their use in CVD and ALD processes quite tricky. Any project that would bring more vapor pressure data on the table would help CVD and ALD community to develop new processes for addressing new applications"

Herve Guillon, Kemstream

of model organic compounds such as naphthalene and model metal-organics such as TEMAH.

DELIVERABLES:

- Demonstrate ability of gas chromatograph / mass spectrometer for measuring the purity and decomposition rate of metal-organic vapors. 3Q 2010

Some metal-organic precursors are known to decompose at temperatures below 200 °C. The gas chromatograph / mass spectrometer will be used to identify the decomposition products as well as contaminants present in the original sample. A capillary sampling system suitable for metal-organic vapors at 200 °C was built. It includes a modified commercial switching valve, a heated capillary transfer line, and modifications to the plumbing of the gas chromatograph. The next step will include testing the GC/MS with known binary mixtures and coordinating the GC/MS operation with that of the vapor pressure apparatus.

DELIVERABLES:

- Measure the vapor pressures of six metal-organic precursors. 4Q 2010

The first precursors will be ones that have been carefully measured elsewhere. Later precursors will be ones that are either widely used or show promise for wide use in the future.

Accomplishments

The vapor pressure apparatus comprises an oven, a vacuum system, a novel thermoelectric temperature control scheme, capacitance diaphragm pressure gauges, and other instruments. Runs can last more than one week due to (1) the slow evolution of outgassing and decomposition and (2) the two hours required for the in situ pressure gauges to recover from temperature changes. Preliminary measurements on the model organic compounds dodecane and naphthalene agreed with literature values to within 1 %. Preliminary measurements on TEMAH agreed with literature values to within 10 %; achieving a smaller uncertainty will require a better understanding of the sample's decomposition.

Degassing the sample is crucial due to the small volatility of typical precursors. An *in situ* sublimation scheme was successfully demonstrated, and a second scheme based on intermittent pumping was tested for removing the

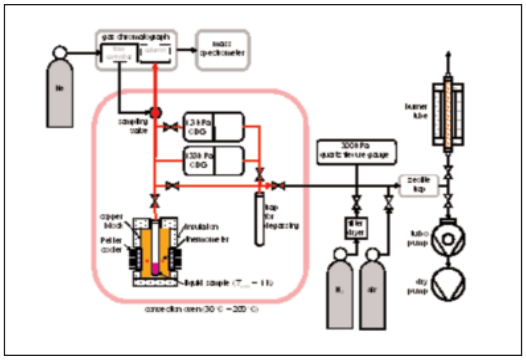

Figure 1. Simplified schematic of the vapor pressure apparatus.

decomposition products of the sample that appear during the vapor pressure measurements.

A method was devised for automatically calibrating the pressure gauges during a vapor pressure run, thereby eliminating errors due to temperature hysteresis. The method relies on a room-temperature reference gauge whose cali

bration can be extrapolated reliably to pressures below 10 kPa.

A collaboration with the Institute of Chemical Technology in Prague was begun. A joint proposal resulted in a grant that will assist the Czech researchers for travel, equipment, and sample preparation; a sample of purified ferrocene has arrived at NIST.

Gas flow measurement research at NIST in support of the semiconductor industry created a quartz capillary flow meter with a hydrodynamic model of unprecedented accuracy. Construction has begun on a prototype primary gas flow meter that will be able to generate and measure gas flows in the range from 0.01 mol/s to 10 mol/s (0.01 sccm to 10 sccm).

Presentations

R.F. Berg, "Viscometry and flow metrology with quartz capillaries", Air Liquide, Newark, DE (30 July 2007).

R.F. Berg, "Capillary flow meter for calibrating spinning rotor gauges", AVS 54th International Symposium, Seattle, WA (18 October 2007).

R.F. Berg, "Capillary flow meter and viscometer for gases", Physikalisch Technischen Bundesanstalt, Berlin, Germany (18 May 2009).

R.F. Berg, "Capillary flow meter and viscometer for gases", Physikalisch Technischen Bundesanstalt, Braunschweig, Germany (19 May 2009).

R.F. Berg, "Vapor pressure apparatus for metal-organic samples", Seventeenth Symposium on Thermophysical Properties, Boulder, CO (23 June 2009).

R.F. Berg, "Vapor pressure apparatus for metal-organic precursors", poster presented at the Spring meeting of the Material Research Society, San Francisco, CA (8 April 2010).

Publications

F. May, R. F. Berg, and M. R. Moldover, "Reference viscosities of H2, CH4, Ar and Xe at low densities," *International Journal of Thermophysics* 28, 1085- 1110 (2007).

R. F. Berg, "Capillary flow meter for calibrating spinning rotor gauges," *Journal of Vacuum Science and Technology* A 26, 1161-1165 (2008).

Analysis Tools and Techniques Program

The continuing shrinking of device dimensions and the rapid inclusion of new materials into device fabrication demands the development of new analytical tools and techniques. The need for new analytical techniques and tools has increased as the components in the transistors approach the low nanometer level and the number of transistors per chip exceeds 1 billion. The development of tools capable of characterizing the structures produced in the laboratories as well as those needed to confirm the manufacturing process require significant improvements. Those used for production also require significant speeds not to slow down the commercial manufacturing. This latter condition may require some sacrifices in the resolution and accuracy of those tools. In addition, more significant modeling that allows us to bridge those areas where measurements can be done to those where knowledge is needed, but measurements cannot be done is critical. Significant improvements in tools capable of analyzing properties of defect particles in the sub-30 nm size are urgently needed. Global and local stress measurement techniques need to be developed.

Thin-Film X-Ray Metrology for Microelectronics

Technical Contacts:
J. P. Cline
D. Windover

Goals

This multi-year collaborative effort between SEMATECH, ISMI, and NIST will provide the semiconductor community with the measurement methodology and calibration capability for accurate thin film characterization using X-ray reflectometry (XRR) and high-resolution X-ray diffraction (HRXRD).

Customer Needs

In recent years, the semiconductor industry has driven scientific advancement in nanometer-scale material coatings to achieve unprecedented uniformity in thickness, control of composition, and unique electrical and mechanical properties. Simultaneous to this rapid advance in thin film processing technologies, the X-ray diffraction user community and instrument manufacturers have collaboratively developed techniques such as XRR and HRXRD that quantitatively measure thin film characteristics such as thickness, density profile, composition, roughness, and strain fields. This NIST-SEMATECH-ISMI effort addresses the industry call for accuracy in thin film characterization (in particular for thickness, density, and roughness determination) and epitaxial layer characterization (in particular for thickness, composition, and lattice strain).

Technical Strategy

NIST addresses the need for XRR and HRXRD standardization and metrology through the production of Standard Reference Materials (SRMs) to aid end users in instrument calibration (see Figure 1). However, production of SRMs requires a substantial instrumentation infrastructure, years of researcher time, and a collaborative community invested in the realization of the SRM to completion. The technical approach to SRM production can be broken into three parallel goals: 1) manufacture of a stable, robust, and well characterized calibration artifact, 2) construction of a stable, well characterized measurement apparatus for performing certification measurements, and 3) development of first principles data analysis procedures with well-founded a priori structural models and statistically verifiable parameter (and model) uncertainty estimates (see Figure 2). To meet goal 1, NIST has established close working relationships with SEMATECH, ISMI, and other industrial and academic partners for developing and manufacturing superlative calibration artifacts for use as SRM feedstock. To meet goal 2, NIST has constructed an X-ray Metrology facility for X-ray measurements traceable to the International System of Units (SI) containing an HRXRD and XRR instrument known as the Ceramics Division Parallel Beam Diffractometer (CDPBD), located in the Advanced Measurement Laboratory (AML) at NIST. To meet goal 3, NIST has collaborated with X-ray industry leaders in developing statistically-sound first principles XRR analysis. These same approaches will be applied to HRXRD analysis in the future (FY10+).

NIST XRR and HRXRD Instrumentation: the CDPBD

Over the past decade, NIST has applied considerable resources to developing the CDPBD for SI-traceable measurements of Powder XRD, Epitaxial HRXRD, and thin-film XRR artifacts for the Standard Reference Materials (SRM) program (see Figure 3). In parallel to this MSEL effort, the Physics Laboratory developed the Physics Laboratory X-Ray Reflectometer (PLXRR), an instrument dedicated to XRR characterization of semiconductor thin-film artifacts (see Figure 4). The PLXRR has been moved to our X-Ray Metrology facility within AML and

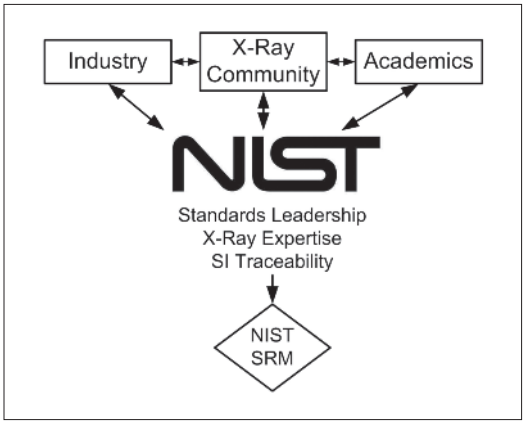

Figure1. Diagram of interactions between NIST and the X-ray community in the production of Standard Reference Materials (SRMs). NIST has many two-way collaborative interactions preliminary to the release of the final product.

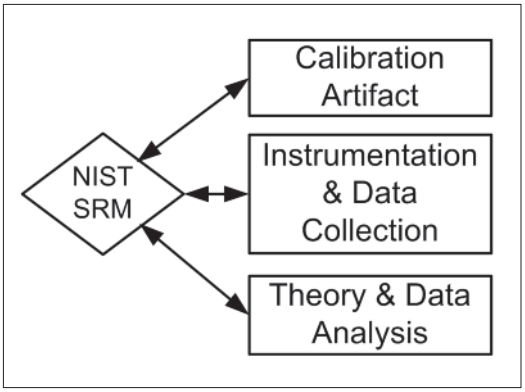

Figure 2. Essential elements of NIST's technical approach to SRM development.

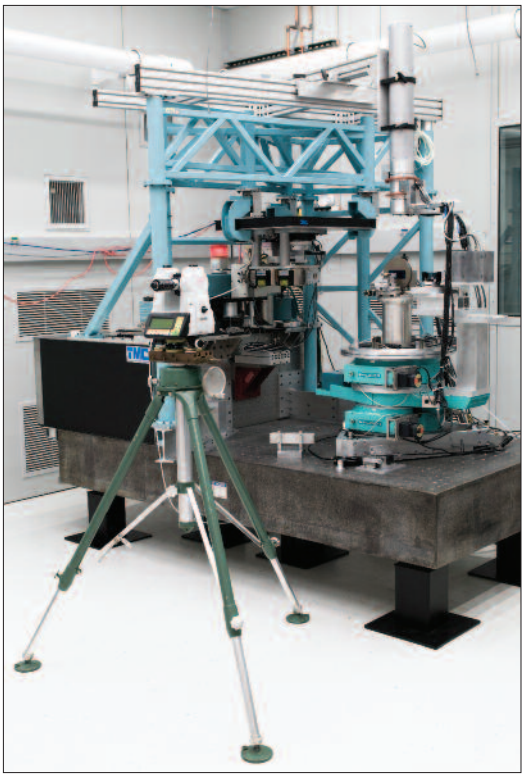

Figure 3. Ceramics Division Parallel Beam Diffractometer (CDPBD) located in the Advanced Measurement Laboratory at NIST seen during alignment of the new spherical air bearing under the goniometers (bottom of green goniometer stack). The X-ray source (near red light in center) is collimated through a monochromator (center, hanging from superstructure) and is diffracted/reflected by a section of a wafer (right) into an analyzer crystal and detector (right). Sample and Detector rotation axes must be coplanar with the incident and diffracted/refracted X-rays. This requires external optical alignment methods using autocollimation, e.g., by a Leika digital theodolite (front,left).

this instrument will be integrated into the XRR SRM effort. This will enable cross-instrument measurement comparisons as part of our certification process.

SI traceability in lattice parameter (HRXRD), d-spacing, or film thickness (XRR), d, requires simultaneously traceability in X-ray wavelength, λ, and in diffraction angle, θ, following Bragg's law: $2d = n\lambda / \sin(\theta)$. The present NIST instrument development project involves establishing SI traceability for both diffraction angle and wavelength on the CDPBD and PLXRR. SI traceability for diffraction angle is achieved using optical encoders on the two rotation stages used to move the sample and detector. The optical encoders' errors are then "mapped" using an external angle reference to generate corrections and uncertainties for each axis. The encoded stages are presently accurate to ± 2.0 μrads (± 0.4 arc seconds). Calibration experiments and collaboration with encoder manufacturers are currently under way to achieve an approximate order of magnitude improvement in accuracy. The first results from this work will soon be used for X-ray measurements (FY10+). SI traceability in wavelength is achieved by constructing a stable, well modeled optics assembly to convert angular and energy divergent radiation from an X-ray source into parallel, monochromatic radiation for use in diffraction or reflection. The CDPBD uses a monochromator

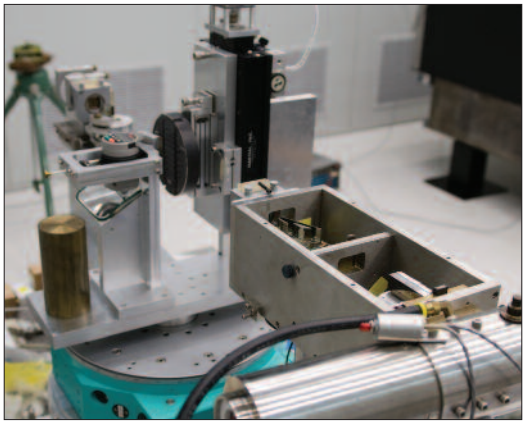

Figure 4. Physics Laboratory X-Ray Reflectometer (PLXRR) seen during relocation to the the Advanced Measurement Laboratory X-Ray Metrology facility. The X-ray source (front, right) is collimated through a mirror and monochromator assembly (front, center rectangular structure) and is reflected by a section of a wafer (vacuum chuck shown rear, center) into a detector (far rear, left).

which uses multiple diffractions from a series of aligned single-crystal Si (220) lattice planes to filter the rotating anode Cu X-ray source into a source of highly-parallel and nearly-single-energy X-rays. SI traceability in X-ray wavelength from the CDPBD is performed using diffraction from a SI-traceable Si (220) reference crystal mounted on the sample stage (whose Si (220) d-spacing has been measured with relative standard uncertainty of 3×10^{-8}). The X-ray wavelength for our instrumentation currently has a relative standard uncertainty of ≈ 1 in 10^{-5} (FY06). Wavelength and angle SI-traceability methods developed for the CDPBD will be implemented on the PLXRR in the future (FY10+). For the certification of the HRXRD SRM we developed a "sequential delta-d method" for reducing the uncertainty of d-spacing of HRXRD measurements due to instrument alignment effects through the use of a WASO 04 reference crystal from the Avogadro Project (See Figure 5). This has allowed for d-spacing measurements with femtometer-scale expanded uncertainties on the CDPBD. Further improvements in angle and wavelength metrology should improve the limits of the NIST instrumentation for HRXRD and XRR measurements in the future. A spherical air bearing base has been incorporated into the CDPBD below the goniometer assembly to allow translation and goniometer tilt to be orthogonal for alignment of XRR and HRXRD measurements. NIST's studies of instrumental alignment parameters and their effect on structural model uncertainty will be used to establish guidelines for instrument-response modeling on commercial instrumentation using future HRXRD and XRR SRMs.

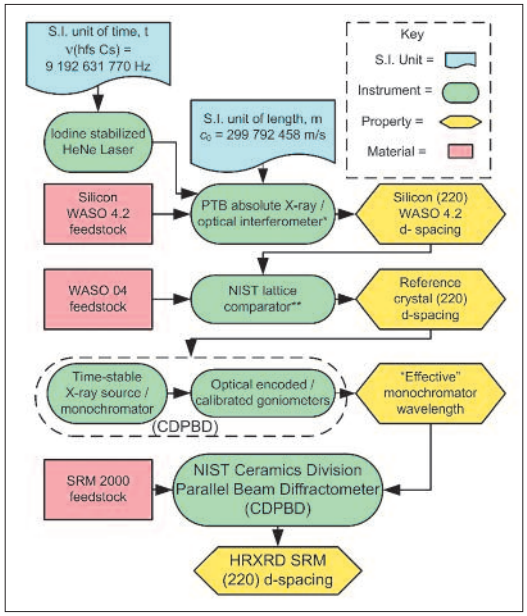

Figure 5. NIST International System of Units (SI)-traceability pathway for high-resolution X-ray diffraction (HRXRD) SRMs using the CDPBD. Measurements from X-ray/optical interferometry at Physikalisch-Technische Bundesanstalt (PTB) in Germany and lattice comparison measurements at NIST provide femtometer-scale expanded uncertainty in lattice spacing (d-spacing) measurements for the SRM.

The HRXRD SRM effort was started nearly a decade ago with collaborations between the NIST Materials Science and Engineering Laboratory (MSEL), the NIST Physics Laboratory, Bede Metrology, and Applied Materials. The approach was to use a commercially viable SiGe epitaxial process as a feedstock structure for a HRXRD SRM. The structure was deposited on 200mm wafers, which were then sectioned into 25 mm x 25 mm specimens after performing HRXRD SRM certification measurements. Structures were produced in FY01 and NIST instrumentation capable of SI-traceable determination of Si substrate d-spacing became available in FY07. The mature, temporally stabilized SiGe feedstock was then measured using transmission and reflection geometries to provide information on both the Si substrate d-spacing and the SiGe epitaxial surface structure.

Due to the extended duration of this SRM project, completion of the certification was divided into two phases to provide a timely product rollout. The goal of the first phase of this SRM was to provide an SI-traceable d-spacing with low expanded uncertainty to aid in basic instrument calibration. If one assumes that the wavelength is relatively stable (possible with, e.g., an epoxy-mounted channel cut monochromator), then SRM 2000 will provide correction for the diffractometer angle. The first phase of the certification was the HRXRD tech transfer in FY08. The second, yet to be completed, certification phase will provide information on the SiGe epitaxial layer for calibration of instrument response (how well the X-ray source is behaving) and short range angle determination (how well the goniometer is behaving) near the (004) Si substrate peak. This calibration information would be most useful in quantitative strain de-

termination using HRXRD. The difficulty here involves determination of the correct structural model for the deposited epilayer. We are currently working with instrument vendors, with external collaborators, and with NIST Synchrotron Methods staff to address this modeling issue (FY10+).

XRR SRM development

During the past decade, NIST and SEMATECH have participated in two parallel XRR research projects requisite to XRR SRM development; a NIST XRR Metrology Study and a NIST/SEMATECH Characterization Study. The goal of both projects will be to use stable, multilayer artifacts supplied by ISMI, SEMATECH, or other semiconductor partners to calibrate measurement instruments used in the semiconductor industry.

The NIST Metrology study consists of in-house XRR (and HRXRD, where possible) characterization with International System of Units (SI)-traceable measurement instrumentation and SI-traceable, first principles data modeling, which is based on Bayesian approaches, providing refinement of instrumental and model parameters as well as providing structural model selection. In parallel, the NIST/SEMATECH Characterization Study combines measurements from NIST, ISMI, SEMATECH, and other semiconductor partners using commercial processline and laboratory XRR instrumentation. NIST then analyzes these data with commercial and NIST-partner-developed metrology software to study the limitations of commercial instrumentation and software modeling. Combining results from both studies will ultimately allow accuracy/traceability and error estimation for commercial instrumentation. This work will also address theoretical XRR modeling limitations and compare software model refinement and model selection approaches. The multi-year collaboration will provide the community with total error budget estimates for a given XRR structural analysis approach and instrumentation. This collaborative work has been underway with SEMATECH (FY05, 06, and 07) and has continued with ISMI and other partners (FY08+). The progress in FY05 included a comprehensive, first principles development of the XRR theory necessary for traceable modeling of data and a first round of measurements on artifacts by commercial and NIST instrumentation. FY06 work explored the application of an approximate Bayesian model selection method to compare the relative probability of different structural models for measured XRR data. Preliminary results with simulated XRR data have shown success in determining the initial structural model used to generate the simulated data. FY07 deliverables included the development of a first XRR prototype SRM for selection of a future SRM feedstock. FY08 deliverables involve development of a second XRR prototype and further development of the NIST XRR modeling approach for establishing parameter uncertainties for samples with surface contamination. In FY09, a theoretical contamination study provided insights into XRR characterization limitations for samples coated with environmental contaminants. In FY09, the study also provided comparisons between the theoretical capabilities of both laboratory and synchrotron instrumentation. Upon development of a successful XRR prototype, we will lead a round-robin with interested industry partners (FY10+).

NIST XRR Metrology Study – The standard NIST approach for reducing uncertainty in a measurement technique involves the generation of a Standard Reference Material (SRM) (see Figure 1). Figure 2 shows the three parallel research aspects needed for the development of an XRR SRM: (1) the manufacture of a robust thin film calibration artifact with a high degree of temporal stability and contamination and/or oxidation resistance, (2) the development of SI-traceable measurement instrumentation, and (3) the creation of an SI-traceable, first principles data analysis approach.

Our collaborative effort with ISMI / SEMATECH allows us to examine structures relevant to the semiconductor industry as candidates for an XRR calibration artifact. NIST has also engaged other national metrology institutes (NMIs) in an effort to assess the temporal stability of international NMI pre-standards. Both PTB of Germany and NMIJ/AIST of Japan have provided us with structures for comparative XRR analysis. In support of this international collaboration, NIST hosted Yasushi Azuma of NMIJ at NIST for several weeks in FY09 for inter-comparison of XRR measurement approaches. This industry, government, and international community cooperative study will help gauge which thin films structures provide stable,

well-defined, refinement parameters suitable for SI-traceable modeling.

NIST, with partners, is currently developing first principles, SI-traceable XRR software to analyze data and refine model and instrument response parameters. XRR analysis is an inverse problem in which we select input parameters for a guessed structural model. This model is then used to simulate data that is compared with measured data to compute the goodness of fit. This process is repeated until a best fit is reached; the best fit model parameters then become the refined model parameters used to describe the structure. Three major questions limit the effectiveness of this current XRR modeling approach: (1) How do we accurately simulate data using a structural model? (2) How do we know which structural model describes the measured structure? (3) How do we accurately compare simulated and measured data? The NIST-led software development effort attempts to answer each of these questions.

To address the model data simulation issue, we have developed XRR modeling based on the elementary Parratt formalism of discrete layer structures and assumed perturbation-based roughness while using the minimum number of layers necessary to effectively describe a structure. This approach will in the future combine XRD, HRXRD and XRR in the same fundamental modeling theory and allow for SI traceability in refined parameters (FY10+). To address the question of model accuracy, we are implementing a Bayesian analysis approach to determine the probability that a given structural model correctly describes a given data set. This model selection component is essential to determining the validity of initial structural assumptions in any XRR analysis. Addressing the third question is of considerable interest. Commercial refinement approaches attempt to optimize a solution through a "chi squared" or other minimization criterion by using e.g., genetic algorithms. This approach attains fast solution times most compatible with process-line requirements, at the loss of statistical data required for parameter uncertainty calculations. NIST, in collaboration with its partners, is developing a statistical sampling based method using a Markov Chain Monte Carlo (MCMC) formalism to generate SI-traceable uncertainty estimations. The MCMC approach is necessary for developing formal Bayesian model selection methods (FY10+) to complement the existing Approximate Bayesian approach.

NIST/SEMATECH XRR Characterization Study – This NIST/SEMATECH project consists of measurements and analysis from commercial instrumentation to allow comparison and calibration transfer from NIST SI traceable measurements and analysis.

The NIST/SEMATECH project combines measurements with commercial process-line and laboratory XRR instrumentation with complimentary compositional analysis results as feedback for comparison with NIST measurements performed in parallel on the same artifacts. The measurement and modeling work at NIST will provide SI-traceable XRR measurements and parameter analysis for artifacts and potential candidate SRMs. The collaboration with ISMI/SEMATECH allows calibration transfer between NIST SI-traceable measurements and process-line instrumentation. NIST will then use results from NIST SI-traceable measurements, ISMI/SEMATECH commercial measurements and modeling, and NIST SI-traceable XRR modeling, to quantify error bounds and overall error budgets on the accuracy and precision possible from commercial instrumentation and commercial modeling software.

Calibration and accuracy determination of commercial instrumentation are the primary goals of this collaboration. To achieve these goals, we need to develop accurate instrument response functions for the commercial instrumentation being calibrated. The instrument response function for commercial instrumentation may be the dominant term in the overall accuracy budget for XRR measurements. To address instrumentation effects on accuracy, work must be performed with different commercial XRR system geometries to discover the mechanical alignment parameters that dominate the error budgets of each system. This will require cooperation from instrument vendors to provide the necessary information or direct measurements of detailed instrument response functions. The incorporation of instrument response parameters into NIST modeling will allow for comparison between traceable measurements at NIST and measurements on commercial instrumentation in

the field. The NIST instrument response function information will be developed through our instrument traceability study discussed earlier. We can then combine specific instrument corrections in the accuracy error budget and use a calibration artifact such as a temporally stable thin film structure measured on the commercial instruments and at NIST to provide instrument calibration and stability monitoring (FY10+ deliverable).

HRXRD and XRR Project Deliverables – The final project results available to SEMATECH will include HRXRD and XRR uncertainty estimates based on NIST HRXRD and XRR software and the calibration artifacts necessary for optimizing the performance of commercial process-line and laboratory XRR instruments. Theoretical uncertainty estimates provided by NIST software and simulated structural data will determine the limitations of XRR applicability for arbitrary multilayer systems on commercial XRR instrumentation (FY10+). Calibration artifacts measured on NIST SI-traceable instrumentation will allow routine system monitoring, alignment, calibration, and instrument response function comparisons to ensure commercial instrument precision and stability. These deliverables will dramatically improve the precision and accuracy of conventional HXRXRD and XRR characterization of multilayer structures which exhibit well-established composition and uniformity (FY10+ deliverables).

DELIVERABLES:

- NIST measurements of NIST HRXRD SRM using novel HRXRD "Bond Method" reciprocal space mapping. 4Q 2009
- NIST collaborative measurements of AIST/NMIJ XRR CRMs. 1Q 2010
- NIST collaborative measurements of ISMI/SEMATECH XRR pre-standard structure. 2Q 2010
- NIST analysis of HRXRD Bond Method reciprocal space mapping. 3Q 2010

Accomplishments

■ In FY05, the CDPBD moved to equipment space in AML at NIST which provides instrument temperature stability of ± 0.02 °C. Preliminary calibration of the angle measurement has been assessed for uncertainty determination (accuracy determination has been completed) and improvements using a new compensation approach have been implemented (FY09). First principles XRR theory development with emphasis on justifying approximations present in commercial XRR software was completed (FY06) and a dynamical scattering based model has been implemented with Monte Carlo Markov Chain (MCMC) methods for structural parameter refinement and formal parameter uncertainty analysis (FY07). A pre-standard XRR test structure has been fabricated by ISMI for NIST SI-traceable measurement (FY08) with a second structure in development (FY09/10) and with SRM development scheduled for the future (FY10+).

■ FY07 Technical transfer: NIST HRXRD pre-standard wafer and measurements to SEMATECH and X-ray industry partners – In FY07, we measured our HRXRD feedstock wafers and provided a wafer and sectioned specimens to SEMATECH along with NIST HRXRD data for collaborative studies. We also provided sectioned specimens to all the major X-ray instrument vendors for internal calibration studies and for independent, complementary measurements on the feedstock. The collaboration between NIST and SEMATECH in Thin-film X-ray Metrology on previous XRR projects has facilitated this sharing of pre-standards with the semiconductor community and with semiconductor tool manufactures at the early stages of SRM production to better achieve the results that the community needs as fast as possible.

■ FY08/09 Technical transfer: NIST HRXRD SRM certification to industry – In FY07, we completed the first phase of certification analysis for our HRXRD SRM. The SRM and the certification reports have been provided to the SRM Program for packaging and release of SRM 2000 for sale to end users and tool manufacturers. This SRM development has involved collaboration with the semiconductor industry (Applied Materials and SEMATECH) and with X-ray tool manufacturers (Jordan Valley / Bede, Bruker, Panalytical, Rigaku, and others) providing NIST with valuable feedback on our approach during the multiyear certification process. The SI-traceable nature of SRM 2000 has allowed us to provide the semiconductor and nanotechnology industries with a nanometer-scale length standard (d-spacing) with femtometer-scale expanded uncertainty, thereby serving as the most accurate, commercially available, nano-scale “meter stick” available today.

Param.	Uncertainty (synchrotron*)	Uncertainty (laboratory*)	U (lab) / U(sync)
t_C	0.64 nm	0.66 nm	1.0
t_{TiN}	0.67 nm	0.62 nm	0.75
$t_{C+ tTiN}$	0.32 nm	0.24 nm	0.75
σ_C	0.033 nm	0.16 nm	4.8
σ_{TiN}	0.50 nm	0.48 nm	0.96
σ_{Si}	0.027 nm	0.20 nm	7.4
ρ_C	0.61 $g^{-1}cm^2$	0.92 $g^{-1}cm^2$	1.5
ρ_{TiN}	1.49 $g^{-1}cm^2$	1.28 $g^{-1}cm^2$	0.86
ρ_{Si}	0.94 $g^{-1}cm^2$	0.94 $g^{-1}cm^2$	1.0

* *Data quality of 8 orders of magnitude over 7 degrees 2θ for Cu radiation (simulated data).*

** *Data quality of 6 orders of magnitude over 5 degrees 2θ for Cu radiation (simulated data).*

Table 1. MCMC comparison of parameter uncertainty estimations for simulated data from a C (0.5 nm) / TiN (20 nm) / Si structure. Note that the uncertainty in thickness for the carbon contamination layer, tc, is larger than the layer thickness.

■ FY09 Technical transfer: NIST parameter uncertainty XRR analysis for surface contamination – In FY07/08 we tested NIST XRR MCMC analysis for simulated and measured data from ISMI / SEMATECH on a SiO_2 / TiN / Si wafer pre-standard structure. In FY09 we addressed the impact of data quality on the refinement of parameter uncertainties for simulated XRR data from a TiN (20 nm) / Si sample. We also tested the effects of a surface carbon contamination layer (0.5 nm) on model parameter uncertainties. The results of the study were presented in a poster at the 2009 Frontiers of Characterization and Metrology for Nanoelectronics, held in Albany, NY. The MCMC analysis provides clear evidence of when parameters are uncorrelated, are highly correlated, and when a given parameter cannot be refined. Table 1 provides estimations of parameter uncertainties for modeling to simulated data for a C (0.5 nm) / TiN (20 nm) / Si substrate data structure for two data qualities: synchrotron (with 8 orders of magnitude data range) and laboratory (6 orders of magnitude). Note that this is a Monte Carlo analysis of simulated data providing the uncertainty estimates to simulated data and should test the ultimate lower limits of XRR modeling. A striking feature in the analysis is that only the buried interface roughness parameters, σ_{TiN} and σ_{Si}, show improvement using synchrotron data (illustrated by high uncertainty ratios in last column - See Table 1). All other uncertainty estimates remain high for both data quality ranges due to uncertainty correlations inherent in the model parameters.

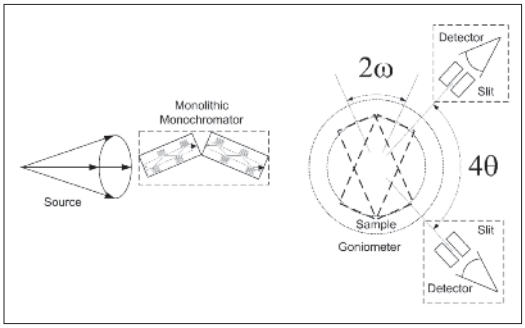

Figure 6. Schematic diagram of Bond Method measurement for HRXRD. A sample is rotated to collect diffraction data (2θ information) from two distinct reflections from the same family of planes. This requires angle measurement accuracy between the two measurements to provide a total (4θ measurement) between reflections.

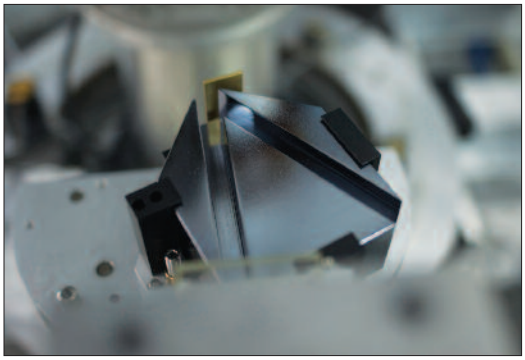

Figure 7. NIST-constructed Si (220) analyzer crystal used for RSMs on the CDPBD. The analyzer was constructed using a Si Boule from the SRM 640d feedstock (for with the d-spacing has been measured to a relative uncertainty of 1 in 3 x 10^8). The large dimensions of the analyzer allow for a large angular acceptance range making RSMs possible without a third rotation axis.

■ FY10 Technical transfer: NIST novel Bond Method HRXRD reciprocal space maps (RSMs) – In FY09 we developed a novel approach to reciprocal space mapping which utilizes the high degree of angle traceability inherent in the CDPBD. Ordinarily, HRXRD RSMs are indexed relative to the strong Si substrate peak represented within a RSM. The peak positions of mis-orientated, strained, or slightly shifted lattice epitaxial layers are indexed relative to the substrate peak

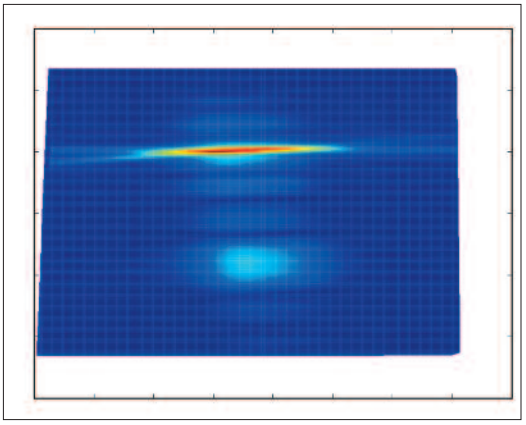

Figure 8. A HRXRD RSM from SRM 2000 for Si (400) showing the strong substrate peak (top) with analyzer and monochromator streaks (long lines through strong peak). The more diffuse peak (lower center) is diffraction from the SiGe epitaxial layer in SRM 2000. The slight tilt to the relative diffraction features shows the misalignment of the SiGe layer to the Si substrate, which is most likely related to the wafer miscut angle. Scales to be determined in formal data release.

position. For the CDPBD, it is possible to complete RSMs on two reflections from the same family of planes, and provide an accurate angle measurement between the two planes. This type of HRXRD determination which employs two 2_q measurements or a so-called 4_q measurement is referred to the Bond Method (see Figure 6). We have expanded this approach to RSMs using a new NIST constructed monolithic analyzer crystal on the detector axis (see Figure 7). We have performed RSMs at two Si (220) reflections for SRM 2000 using the CDBPD (see Figure 8 and 9). This data, will be used in future re-certifications of SRM 2000 to reduce uncertainty estimates for certified reference values. This Bond Method measurement is currently being tested for applicability to XRR measurements. An XRR RSM for a Certified Reference Material from AIST/NMIJ has been collected and is currently under analysis (See Figure 10). The HRXRD and XRR Bond Method RSMs analysis approach is still in development, and formal presentation of this technique sill occur in FY10/11.

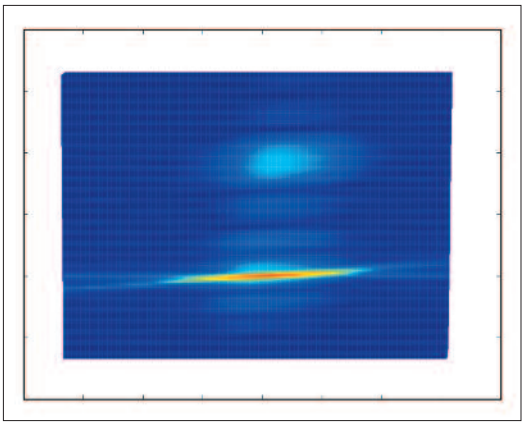

Figure 9. A HRXRD RSM from SRM 2000 from another member of the <400> family showing the strong substrate peak (bottom) with analyzer and monochromator streaks. Note the slight tilt is in the opposite direction for this RSM. Scales to be determined in formal data release.

Collaborations

SEMATECH – PY Hung.

ISMI – Victor Vartanian.

PTB, Peter Thomsen-Schmidt, Michael Krumrey, Burkhard Beckhoff.

LETI – Emmanuel Nolot.

NMIJ/AIST – Toshiyuki Fujimoto & Yasushi Azuma.

Jordan Valley Semiconductor / Bede Scientific Inc. – Matthew Wormington.

Bruker AXS – Assunta Vigliante & Arnt Kern.

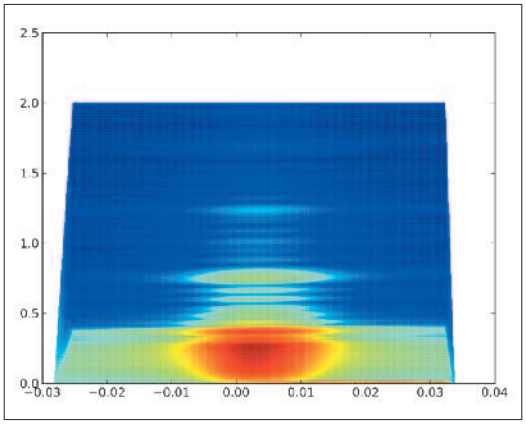

Figure 10. An XRR RSM from a multilayer Certified Reference Material provided by AIST/NMIJ. The colors represented logarithmic changes in intensity and the complicated intensity profile is caused by multiple similar thickness layers in the multilayer structure. Further XRR RSM measurements will be needed before a systematic analysis approach will be possible. Scale angles are in degrees 2θ.

Coruscavi – David L Gil.

Panalytical – Martijn Fransen.

Rigaku MSC – Joe Formica.

Columbia University - I. Cev Noyan

Publications

J.P. Cline, D. Black, D.L. Gil, A. Henins, D. Windover, *"The Application of the Fundamental Parameters Approach as Implemented in TOPAS to Divergent Beam Powder Diffraction Data"* – Materials Science Forum Vol. 651 pp. 201-219 (2010).

D.R. Black, D. Windover, D.L. Gil, J. Filliben, J.P. Cline, *"Standard Reference Material 640d for X-Ray Metrology"* – Advances in X-ray Analysis Vol. 53 pp. TBD (2010).

D.R. Black, D. Windover, A. Henins, D.L. Gil, J. Filliben, J.P. Cline, *"Certification of NIST Standard Reference Material 640d"* – Powder Diffraction Vol. 25 pp. 187-190 (2010).

D. Windover, *"NIST SI-traceable X-Ray Reflectometry (XRR) Measurement Capabilities for Thin Films: Instrumentation and Data Analysis"* – oral presentation at the Japan-U.S. Symposium on International Standardization Toward a Low Carbon Society, Tsukuba, Japan (February, 2010)

D.R. Black, D. Windover, D.L. Gil, A. Henins, E. Kessler, J.P. Cline, *"NIST Standard Reference Material 640d for X-ray Metrology"* – poster presentation at Denver X-Ray Conference, Denver, CO (August, 2009).

J.P. Cline, *"Addressing the Amorphous Content Issue in Quantitative Phase Analysis: The Certification of NIST SRM 676A"* – oral presentation at Denver X-Ray Conference, Denver, CO (August, 2009)

D.L. Gil, *"Characterizing X-ray Mirrors in Reciprocal Space: Results from the NIST X-ray Optics Evaluation Double-Crystal Diffractometer"* – oral presentation at Denver X-Ray Conference, Denver, CO (August, 2009)

D. Windover, *"A High Resolution X-ray Diffraction Standard Reference Material"* – oral presentation at Denver X-Ray Conference, Denver, CO (August, 2009)

D.L. Gil, D. Windover, A. Henins, J.P. Cline, *"Designing an X-ray Reflectometry Standard Reference Material: Effects of Surface Contamination and Data Quality"* – poster presentation at 2009 Frontiers of Characterization and Metrology for Nanoelectronics, Albany, NY (May, 2009).

D. Windover, D.L. Gil, D. Black, A. Henins, J.P. Cline, *"NIST High Resolution X-ray Diffraction Standard Reference Material: SRM 2000"* – poster presentation at 2009 Frontiers of Characterization and Metrology for Nanoelectronics, Albany, NY (May, 2009).

D.L. Gil, D. Windover, J.P. Cline, A. Henins, *"Characterizing x-ray mirrors in reciprocal space: Preliminary results from the NIST X-ray Optics Evaluation Double-Crystal Diffractometer"* – oral presentation at SMEXOS: Simulation Methods for X-ray Optical Systems, Grenoble, France (February 2009).

J. P. Cline, D. Windover, A. Henins, *"NIST Standard Reference Materials for X-Ray Metrology"* – poster presentation at Denver X-Ray Conference, Denver, CO (August, 2008).

D. Windover, D.L. Gil, D. Black, J.P. Cline, A. Henins, *"NIST High Resolution X-ray Diffraction Standard Reference Material: SRM 2000"* – poster presentation at Denver X-Ray Conference, Denver, CO (August, 2008).

D.L. Gil, D. Windover, A. Henins, J.P. Cline, *"Characterizing X-ray mirrors in reciprocal space: Preliminary results from the NIST X-ray optics evaluation double-crystal diffractometer"* – poster presentation at Denver X-Ray Conference, Denver, CO (August, 2008).

D. Windover, D. L. Gil, A. Henins, D. Black, J. P. Cline, P. Xu, M. Wormington, M. Vaudin, Y. Gerbig, R.Cook, E. Kessler, P. Evans, S.J. Stranick, J. Schoenmaker, L. Novotny, *"Standard Reference Materials for thin film metrology"* – invited presentation at ISMI – FMAG meeting, Monterey, CA (February 2008).

J. P. Cline, D. Windover, A. Henins, *"Standard Reference Materials for thin film metrology"* – poster presentation at Denver X-Ray Conference, Denver, CO (August, 2007).

D. L. Gil, D. Windover, J. P. Cline, A. Henins, P. Y. Hung, S. C. Song, R. Jammy, A. Diebold, *"MCMC methods for X-ray reflectometry standards"* – poster presentation at Denver X-Ray Conference, Denver, CO (August, 2007).

D. A. McGillivray, S.C. Yang, D. Windover, D. L. Gil, J. P. Cline, A. Henins, *"Status of the NIST HRXRD SRM: Instrumentation alignment approach"* – poster presentation at Denver X-Ray Conference, Denver, CO (August, 2007).

D. Windover, D. L. Gil, J. P. Cline, A. Henins, N. Armstrong, P. Y. Hung, S. C. Song, R. Jammy, A.

Diebold, *"X-ray reflectometry determination of structural information from atomic layer deposition nanometer-scale*

hafnium oxide thin films" – oral presentation & conference proceedings at Spring 2007 Materials Research Society, San Francisco, CA (April 2007).

D. L. Gil, D. Windover, J. P. Cline, A. Henins, N. Armstrong, P. Y. Hung, S. C. Song, R. Jammy, A. Diebold, *"MCMC method for determining structural information using X-ray reflectometry"* – poster presentation at 2007 Frontiers of Characterization and Metrology for Nanoelectronics, Gaithersburg, MD (March 2007).

D. Windover, D. L. Gil, J. P. Cline, A. Henins, N. Armstrong, P. Y. Hung, S. C. Song, B. H. Lee, R. Jammy, A. Diebold, *"NIST method for determining model-independent structural information by X-ray reflectometry"* – poster presentation & conference proceedings at 2007 Frontiers of Characterization and Metrology for Nanoelectronics, Gaithersburg, MD (March 2007).

D. Windover, D. L. Gil, A. Henins, N. Armstrong, J. P. Cline, *"Prototype standards for X-ray reflectometry: an international perspective revisited"* – poster presentation at Spring International Centre for Diffraction Data, Newtown Square, PA, (March, 2007).

High-Resolution Microcalorimeter X-Ray Spectrometer for Chemical Analysis

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Goals

We will develop new generations of X-ray spectroscopy tools to meet the materials analysis needs of the semiconductor manufacturing industry. Energy-Dispersive Spectrometers (EDS) based on microcalorimeters have the ability to detect photons with high energy resolution and near-unity quantum efficiency. Using these tools, a wide range of materials analysis problems can be solved. In semiconductor manufacturing, improved X-ray materials analysis is needed to identify nanoscale contaminant particles on wafers and to analyze very thin layers of materials and minor constituents. Microcalorimeter EDS improves the spectral resolution by one to two orders of magnitude compared to the semiconductor Si-EDS, the existing industry standard. Such improved resolution combined with energy dispersive operation makes possible direct spectral separation of most overlapping peaks often encountered with Si-EDS in complex multi-element systems. The improved resolution of the microcalorimeter EDS also increases the peak-to-background ratio. Peak shape and shift can be studied to reveal chemical state information.

Developing arrays of X-ray microcalorimeters will enable the acquisition of high statistics spectra in reduced time, improving the efficiency and statistical quality of existing materials analysis applications. Further, large-format arrays (up to 1000 pixels) will make it possible to chemically analyze smaller features and trace constituents, and to track rapidly evolving X-ray spectra for in-process and process-stream monitoring.

The microcalorimeter EDS detector invented at NIST consists of a superconducting thermometer (a superconducting transition-edge sensor (TES) and an X-ray absorber fabricated on a micromachined Si_3N_4 membrane, and cooled to cryogenic temperatures (0.1 K). When X-rays are absorbed in the detector, the resulting heat pulse in the microcalorimeter is measured by the TES thermometer. The change in the temperature of the thermometer is measured by a superconducting quantum interference device (SQUID) amplifier. The temperature pulse height gives a measurement of the energy of the X-ray photon one to two orders of magnitude more sensitive than Si-EDS. The detector is cooled to 0.1 K by a compact adiabatic demagnetization refrigerator. We are presently simplifying this refrigerator to reduce system costs and increase the accessibility of microcalorimeter technology.

Customer Needs

Improved X-ray detector technology has been cited by SEMATECH's Analytical Laboratory Managers Working Group (ALMWG, now Analytical Laboratory Managers Council (ALMC) as one of the most important metrology needs for the semiconductor industry. In the 2009 International Technology Roadmap for Semiconductors, microcalorimeter technology is called out for its ability to measure chemical shifts, and because of its potential for particle and defect analysis. The transition-edge sensor (TES) microcalorimeter X-ray detector developed at NIST has been identified as a primary means of realizing these detector advances, which will greatly improve in-line and off-line metrology tools that currently use semiconductor energy-dispersive spectrometers (EDS). At present, these metrology tools fail to provide fast and unambiguous analysis for particles less than approximately 0.1 μm to 0.3 μm in diameter. Improved EDS detectors such as the TES microcalorimeter are necessary to extend the capabilities of existing SEM-based instruments to meet the analytical requirements for future technology generations. With continued development, microcalorimeter EDS should be able to meet both the near-term and the longer-term requirements of the semiconductor industry for improved particle analysis.

"Prototype microcalorimeter energy dispersive spectrometers (EDS) and superconducting tunnel junction techniques have X-ray energy resolution capable of separating peaks that overlap and cannot be resolved with current generation lithium drifted- silicon EDS detectors. Such new X-ray detectors will allow resolution of slight chemical shifts in X-ray peaks providing chemical information such as local bonding environments. These advances over traditional EDS and some wavelength dispersive spectrometers can enable particle and defect analysis on SEMs located in the clean room." 2009 International Technology Roadmap for Semiconductors

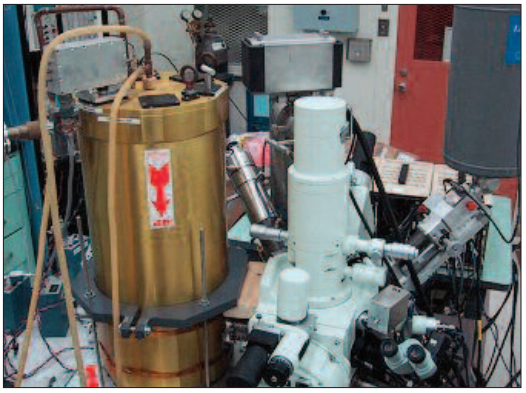

Figure 1. Single-pixel NIST X-ray microcalorimeter system on a scanning-electron microscope. The system was developed in the Electronics and Electrical Engineering Laboratory (EEEL) at NIST, Boulder, and transferred to the Chemical Science and Technology Laboratory (CSTL) at NIST Gaithersburg to be used to study problems of interest to the semiconductor industry.

Technical Strategy

1. The usefulness of single-pixel X-ray microcalorimeter EDS in materials analysis has now been well established in a variety of demonstrations. Arrays of X-ray microcalorimeters for increased collection area and count rate have been demonstrated and their energy resolution is comparable to single sensors. To meet the needs of the semiconductor industry, it is necessary to make both single-pixel and array microcalorimeter systems more widely available. In addition to microcalorimeters, the system requires novel superconducting electronics to instrument the detectors, compact adiabatic demagnetization refrigerators to simplify cooling to milliKelvin operating temperatures, and custom room-temperature electronics and software to process the output signals. Our goal is to develop new generations of detector systems, to transfer them to the Chemical Science and Technology Laboratory (CSTL) in NIST Gaithersburg, Maryland for collaborative use in studying problems of interest to the industry (Fig. 1), and to work with commercial partners in disseminating the technology.

DELIVERABLES:

- Provide continued support and upgrades for the single-pixel microcalorimeter system transferred to CSTL. Provide support for partners working to commercialize microcalorimeter technology and make it more widely available to the semiconductor industry.

2. The operation of microcalorimeter arrays requires multiplexed SQUID readout. A time-domain SQUID multiplexer has previously been demonstrated and been used to successfully read out multiple microcalorimeters under X-ray illumination using a much smaller number of amplifier channels. Significant increases in multiplexer bandwidth and pixel-handling capacity are possible based on evolutionary design improvements. Arrays of several hundred microcalorimeter pixels are now feasible and can realistically be integrated into practical spectrometers.

DELIVERABLES:

- Demonstrate improved SQUID multiplexer performance and multiplexed operation of increasing numbers of microcalorimeters under X-ray illumination. Assembly of spectrometer compatible with up to 256 microcalorimeter pixels (April-June 2010). This spectrometer will later be used for the analysis of technologically relevant materials such as advanced solar cell components.

3. One of the barriers to widespread dissemination of X-ray microcalorimeter instruments is the complexity and cost of the adiabatic demagnetization refrigerator used to cool to 100 mK. The development of an on-chip solid-state microrefrigerator based on superconducting tunnel junctions to cool from 300 mK to 100 mK would greatly simplify the cryogenic system needed for microcalorimeter EDS. Adiabatic demagnetization refrigerators could be replaced by small, simple, and inexpensive 3He systems, which cool to 300 mK, coupled to the solid-state tunnel-junction refrigerator cooling to 100 mK.

Figure 2. Prototype microcalorimeter X-ray spectrometer (left) installed on a scanning electron microscope at the Santa Fe, NM facility of STAR Cryoelectronics.

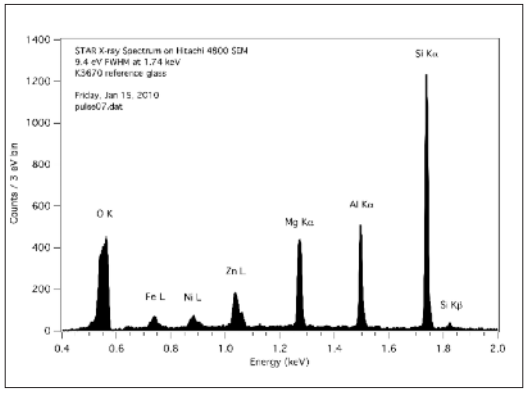

Figure 3. X-ray spectrum of a NIST reference glass produced by the STAR Cryoelectronics microcalorimeter spectrometer.

DELIVERABLES:

- Demonstrate improved performance of tunnel-junction refrigerators and X-ray microcalorimeters cooled by tunnel-junction refrigerators. Demonstration of tunnel junction cooler with temperature reduction close to theoretical maximum (July-Sept. 2010).

Accomplishments

■ We assisted the company STAR Cryoelectronics to assemble and operate a prototype microcalorimeter X-ray spectrometer that can be mounted on a modern scanning electron microscope. A photograph of the installed spectrometer is shown in Fig. 2. The instrument requires no liquid cryogens and consumes only electricity. The spectrometer has demonstrated energy resolution values between 10 eV to 15 eV as shown in the X-ray spectrum of Fig. 3. This prototype instrument represents a breakthrough in the commercial availability of microcalorimeter technology.

■ We developed a simple and compact adiabatic demagnetization refrigerator that is precooled by a mechanical cryocooler. This refrigerator is a component of the spectrometer above. This refrigerator has been successfully commercialized and numerous versions have now been sold worldwide by High Precision Devices, Inc.

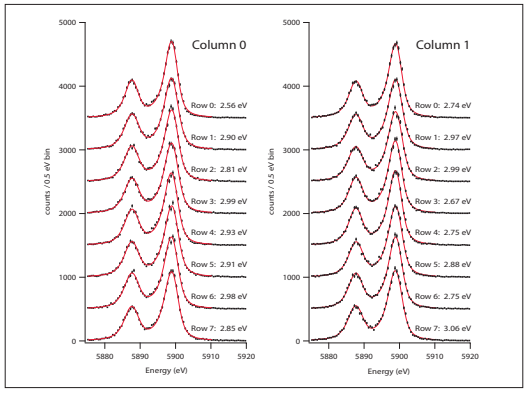

Figure 4.Spectra from 16 microcalorimeter array showing 2.86 eV resolution at 6 keV.

■ We developed a new generation of microcalorimeters that incorporate additional normal metal regions to suppress internal noise. In addition to being more stable and easier to bias, the energy resolution of these microcalorimeters is significantly improved. We demonstrated an energy resolution of 2.4 eV FWHM at 5.9 keV and 2.0 eV at 1.5 keV; these figures are over 30 times better than the best high resolution semiconductor-based detectors currently available.

■ We demonstrated the ability to read out 16 total TES microcalorimeters in two columns with an average energy resolution of 2.86 eV FWHM (Fig. 4).

■ We are assembling an X-ray spectrometer that can accommodate up to 256 microcalorimeter pixels with multiplexed SQUID readout. This spectrometer incorporates numerous improvements to the multiplexer bandwidth (Fig. 5).

■ We have successfully developed an on-chip solid-state refrigerator to cool X-ray mi-

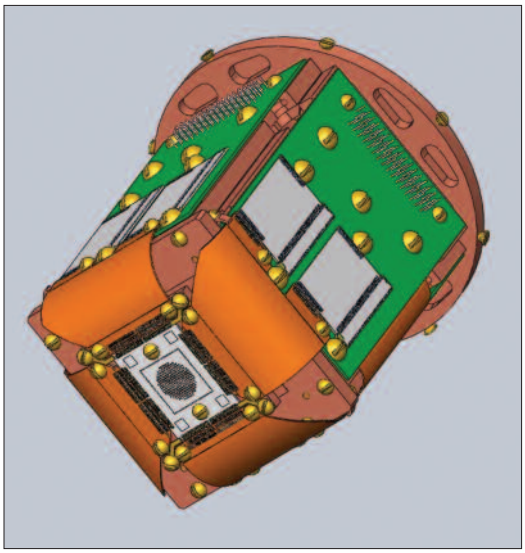

Figure 5. Excerpt from the mechanical design of recently developed X-ray spectrometer compatible with up to 256 microcalorimeter pixels. The figure shows the sensors and SQUID readout circuitry (grey) located at the 50 mK stage of the instrument. The diameter of the circular baseplate is approximately 6 cm.

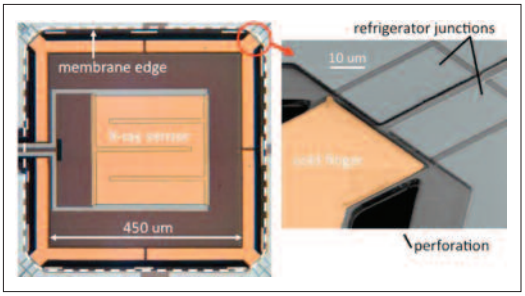

Figure 6. Micrograph showing tunnel junction cooled X-ray microcalorimeter

crocalorimeters from 300 mK to 100 mK. This refrigerator can greatly simplify the cryogenic system needed for microcalorimeter EDS. Adiabatic demagnetization refrigerators can be replaced by small and inexpensive ^{3}He systems coupled to the solid-state refrigerator. Cooling is produced in the devices by the tunneling of electrons through normal-insulator-superconductor junctions. The solid-state refrigerator is fabricated on a silicon wafer using conventional thin-film and photolithographic techniques, has no moving parts, and operates continuously. Recently, we demonstrated solid-state refrigerators able to cool X-ray microcalorimeters over useful temperature ranges, for example, from 260 mK to 160 mK (Fig. 6). We operated an X-ray microcalorimeter cooled by a solid-state refrigerator and demonstrated an energy resolution of 9.5 eV at 5.9 keV, a record for the 260 mK starting temperature of the integrated device. This work has been featured twice on the cover of Applied Physics Letters and once on the cover of Physics Today.

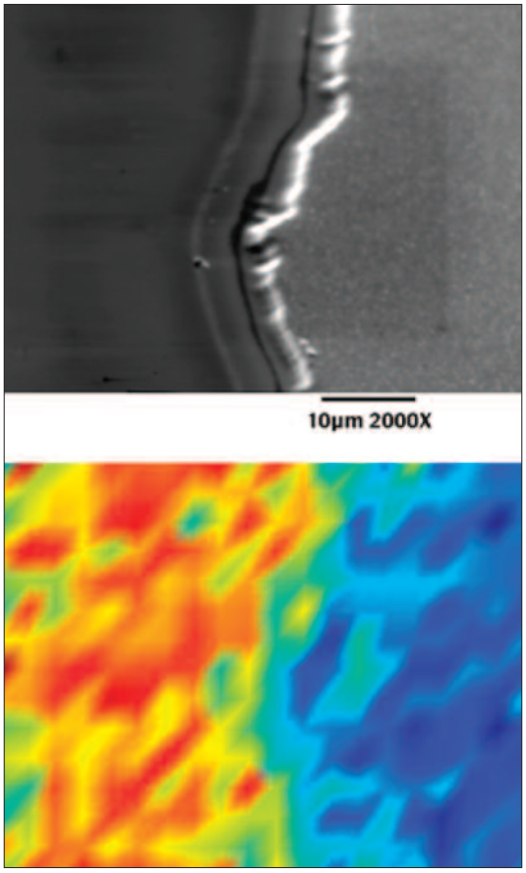

Figure 7. SEM photo (top) of an aluminum film partially covering a sapphire substrate and a false-color map (bottom) of the shift in the mean X-ray energy of the Al Kα peak taken using a microcalorimeter EDS system. The shift in energy is due to the chemical bonding of the aluminum with the oxygen. The average energy shift is ≈0.2 eV.

■ We created a chemical shift map showing the chemical bonding state of Al in a sample containing both Al and Al_2O_3 (see Fig. 7). An aluminum film was deposited on part of a sapphire substrate. A microcalorimeter EDS was used to measure the X-ray spectrum as the electron beam was rastered to form the SEM image. The Al X-ray line position was shifted by a small amount (about 0.2 eV) in the regions containing Al_2O_3 as compared to the regions containing elemental Al. The high energy resolution of the microcalorimeter allowed the shift to be measured, resulting in the false-color image below. The map clearly demonstrates that microcalorimeter EDS can be used to discriminate the chemical bonding state using shifts in the positions of X-ray lines. The result also highlights the need for large-format arrays to increase the data collection rate. The image shown here was acquired over several hours. Images such as this could be acquired much more quickly using an array of microcalorimeters.

Collaborations

Chemical Science and Technology Laboratory, NIST, Gaithersburg, Terry Jach, Lance King, Dale Newbury, John Small, and Eric Steel, the development of microcalorimeter EDS systems.

Publications

M. D. Niemack, J. Beyer, H. M. Cho, W. B. Doriese, G. C. Hilton, K. D. Irwin, C. D. Reintsema, D. R. Schmidt, J. N. Ullom, L. R. Vale, *"Code-division SQUID multiplexing,"* Applied Physics Letters 96, 163509 (2010).

K. D. Irwin, M. D. Niemack, J. Beyer, H. M. Cho, W. B. Doriese, G. C. Hilton, C. D. Reintsema, D. R. Schmidt, J. N. Ullom, L. R. Vale, *"Code-division multiplexing of supercon-*

ducting transition-edge sensor arrays," Superconductor Science & Technology 23, 034004 (2010).

H. Tan, D. Breus, W. Hennig, K. Sabourov, W. K. Warburton, W. B. Doriese, J. N. Ullom, M. K. Bacrania, A. S. Hoover, M. W. Rabin, *"High Rate Pulse Processing Algorithms for Microcalorimeters,"* 2008 IEEE Nuclear Science Symposium - Conference Record, 405 (2009).

T. Jach, J. N. Ullom, and W. T. Elam, *"The microcalorimeter X-ray detector: A true paradigm shift in X-ray spectroscopy,"* Eur. Phys. J. Special Topics 169 (2009) 237-242.

N. A. Miller, G. C. O'Neil, J. A. Beall, G. C. Hilton, K. D. Irwin, D. R. Schmidt, L. R. Vale, J. N. Ullom, *"High resolution x-ray transition-edge sensor cooled by tunnel junction refrigerators,"* Applied Physics Letters 92, 163501 (2008).

N. A. Miller, J. A. Beall, G. C. Hilton, K. D. Irwin, G. C. O'Neil, D. R. Schmidt, L. R. Vale, J. N. Ullom, *"Operation of an X-ray transition-edge sensor cooled by tunnel junction refrigerators,"* J. Low Temperature Physics 151, 635 (2008).

J. N. Ullom, *"Materials analysis with cryogenic sensors,"* Invited review paper for J. Low Temperature Physics 151, 746 (2008).

J. N. Ullom, W. B. Doriese, J. A. Beall, W. D. Duncan, L. Ferreira, G. C. Hilton, R. D. Horansky, K. D. Irwin, T. Jach, B. Mates, N. A. Miller, G. C. O'Neil, C. D. Reintsema, N. Ritchie, D. S. Schmidt, L R. Vale, Y. Xu, B. L. Zink, A. Hoover, C. R. Rudy, D. M. Tournear, D. T. Vo, M. W. Rabin, *"Multiplexed microcalorimeter arrays for precision measurements from microwave to gamma-ray wavelengths,"* Nucl. Instrum. & Methods in Phys. Res. A 579, 161 (2007).

T. Jach, N. Ritchie, J. Ullom, J. A. Beall, *"Quantitative analysis with the transition edge sensor microcalorimeter X-ray detector,"* Power Diffraction, 22, 138 (2007).

T. Jach, J. Ullom, N. Ritchie, J. Beall, *"Quantitative analysis on an electron probe with the NIST transition edge sensor microcalorimeter X-ray detector,"* Proc. Microscopy & Microanalysis 2006, July 30-August 3, Chicago, Illinois.

K. D. Irwin, *"Seeing with Superconductors,"* Scientific American, Nov. (2006).

J. N. Ullom, J. A. Beall, W. B. Doriese, W. D. Duncan, L. Ferreira, G. C. Hilton, K. D. Irwin, G. C. O'Neil, C. D. Reintsema, L. R. Vale, B. L. Zink, *"Optimization of TES Microcalorimeters,"* Nuclear Instruments and Methods A 559, 422 (2006).

W. B. Doriese, J. A. Beall, W. D. Duncan, L. Ferreira, G. C. Hilton, K. D. Irwin, C. D. Reintsema, J. N. Ullom, L. R. Vale, Y. Xu, *"Toward Kilopixel Arrays: 3.8 eV Microcalorimeter Resolution in Eight-Channel SQUID Multiplexer,"* Nuclear Instruments and Methods A 559, 808 (2006).

N. A. Miller, A. M. Clark, D. R. Schmidt, J. A. Beall, G. C. Hilton, K. D. Irwin, L. R. Vale, J. N. Ullom, *"A Practical Electron Tunneling Refrigerator: Cooling of Low Temperature Detectors and Bulk Material,"* Nuclear Instruments and Methods A 559, 633 (2006).

K. D. Irwin, *"Noise Theory of Nonlinear, Nonequilibrium Calorimeters and Bolometers,"* Nuclear Instruments and Methods A 559, 718 (2006).

K. D. Irwin, J. A. Beall, W. B. Doriese, W. D. Duncan, G. C. Hilton, J. A. B. Mates, C. D. Reintsema, D. R. Schmidt, J. N. Ullom, L. R. Vale, B. L. Zink, K. W. Lehnert, *"Microwave SQUID Multiplexer,"* Nuclear Instruments and Methods A 559, 802 (2006).

D. E. Newbury, K. I., G. H., D. A. Wollman, J. A. Small and J. Martinis, *"The Impact of the Transition Edge Sensor Microcalorimeter Energy Dispersive X-ray Spectrometer on Electron Probe Microanalysis,"* a chapter in the book Cryogenic Particle Detection, C. Enss (Ed.), Springer, Berlin, Heidelberg (2005).

K. D. Irwin and G. C. Hilton, *"Transition-Edge Sensors,"* a chapter in the book Cryogenic Particle Detection, C. Enss (Ed.), Springer, Berlin, Heidelberg (2005).

J. N. Ullom, J. A. Beall, W. B. Doriese, W. D. Duncan, L. Ferreira, G. C. Hilton, K. D. Irwin, C. D. Reintsema, L. R. Vale, *"Optimized Transition-Edge X-ray Microcalorimeter with 2.4 eV Energy Resolution at 5.9 keV,"* Appl. Phys. Lett. 87, 194103 (2005).

A. M. Clark, N. A. Miller, A. Williams, S. T. Ruggiero, G. C. Hilton, L. R. Vale, J. A. Beall, K. D. Irwin, J. N. Ullom, *"Cooling of Bulk Material by Electron-Tunneling Refrigerators,"* Appl. Phys. Lett. 86, 173508 (2005).

Protein Biochips for Ultrasensitive Detection of Pathogens with Electrical Detection

Technical Contacts:
J. Robertson,
J. Reiner,
J. Kasianowicz

Goals

The BioeElectronics project at NIST is developing new methods to address cutting-edge measurement needs in healthcare, homeland security, and defense. To accomplish this goal, we are creating new technologies and theories that will enable the sensitive and reliable electrical detection of specific pathogens (e.g., anthrax and other biowarfare agents), their toxins, and biological molecules. The method relies on the use of biological and solid-state nanometer-scale pores for the detection and identification of molecules (e.g., protein, RNA, and DNA) that are unique to a given pathogen, cell type or tissue. This new technology will also enable device development for the rapid screening of potential therapeutic agents against biological weapons of mass destruction.

Customer Needs

As classical transistor miniaturization in the semiconductor reaches it's fundamental limits, the need for increased functionality will begin to dominate the semiconductor industry. Although there are many strategies for such functionality, the most promising is to merge the fields of biotechnology and semiconductor physics. This confluence promises to take advantage of the complexity afforded by biological tools that have resulted from 3.8 billion years of evolution and marry the inherent specificity and functionality of such biologics with the stability and integrability of the semiconductor electronics.

Protein biochips are particularly important for the semiconductor industry as the fundamental limit for miniaturization is already on the order of a single protein with a surface are of $<80\ nm^2$. These proteins can be used in a wide range of applications from single analyte sensing (i.e., detecting a specific protein with its natural complement) to a more generalized solution analogous to mass spectrometry, with the potential to fully transform the field of biosensing.

In addition to the semiconductor industry, small market solutions are urgently needed for the Department of Homeland Security. For instance HLS is urgent need of highly flexible devices for the rapid and reliable detection of biological threats both in a laboratory setting and in the field. These detections schemes must be able to detect biological pathogens to the sub-species level for both threat screening and possible forensic criminal investigations in the case of a bioweapon attack.

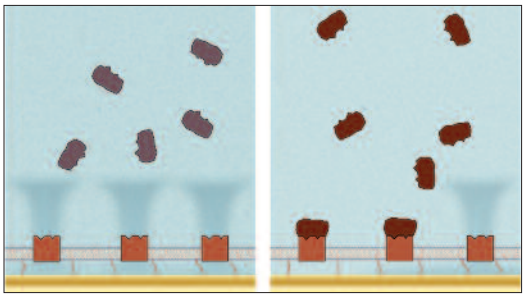

Figure 1. Schematic for the detection scheme for anthrax proteins with a protein based biochip. The specific interaction of two proteins secreted by Bacillus anthracis are used in a lock-and-key mechanism for the specific detection of virulent anthrax.

Technical Strategy

With our partners in DoD labs, universities, and electronics technology companies, we are designing highly-sensitive signal transduction systems that permit both the detection of single bacterial toxin molecules and the discrimination between subtly different target analytes. The initial phase of this research took advantage of proteins that convert the binding of toxins of interest into an easily identified electrical signal. For example, we used one anthrax toxin to detect two other anthrax toxins to better than 1 part in 10^{12} parts of water (see figure 1).

Currently, we are focused on the development of ultra-thin film interfaces that will permit the integration of these protein-based transducers into lab-on-a-chip platforms. This project combines synthetic chemistry, semiconductor processing, self-assembly to produce cell-wall mimics with a range of solid-state or biological nanopores (see figure 2) intimately integrated with nanoengineered semiconductor surfaces and electrodes or signal manipulation and propagation. In essence

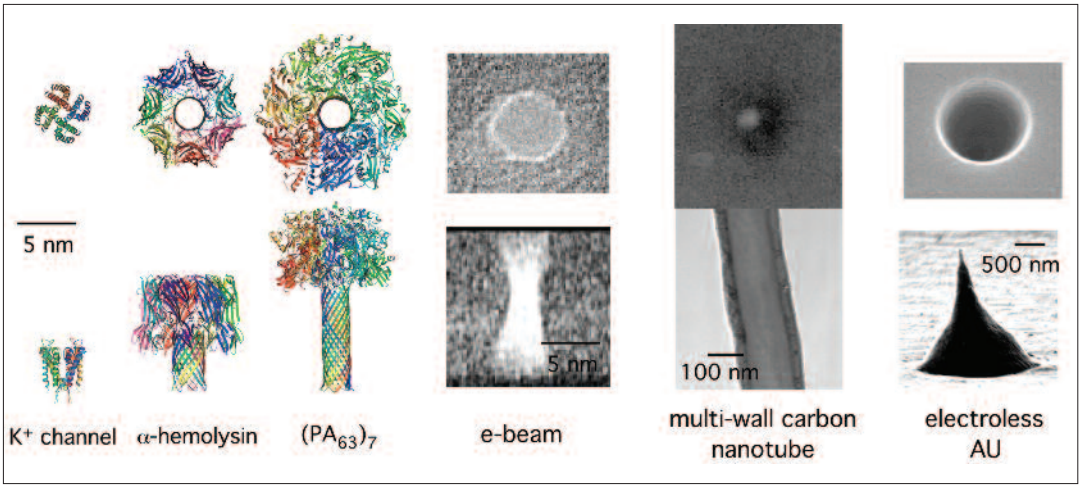

Figure 2. Single molecule mass spectrometry can be performed with a wide variety of natural or synthetic proteins for the rapid determination of a wide variety of biological analytes.

these fabrication techniques are producing biological circuits that can be modeled and understood through traditional physical and semiconductor tools such as SPICE.

DELIVERABLES:

- Chip-based electrical measurement system to detect anthrax toxins at ultra-low concentration.
- Comprehensive theory for single molecule mass spectrometry based on simple electrical measurements.
- Develop an accurate single-molecule method for determining changes in nanopore geometry with sub-Angstrom resolution. This method will help the standardization of solid-state nano pores.

Accomplishments

We developed an electrical-based method for single molecule mass spectrometry to determine the length of single molecules to better than 1.5 Angstrom resolution.

We also used electrochemical impedance spectroscopy and surface plasmon resonance to determine the ability of anthrax proteins to bind to and function in ultra-thin films on gold electrodes.

Collaborations

Drexel University (Philadelphia, PA)

US Army Medical Research Institute for Infectious Diseases (Fort Detrick, MD)

National Cancer Institute (Fort Detrick, MD)

Electronic BioSciences (San Diego, CA)

Flinders University (Adelaide, Australia)

Publications

J.W.F. Robertson, C.G. Rodrigues, V.M. Stanford, K. Rubinson, O.V. Krasilnikov, & J.J. Kasianowicz. 2007. *"Single molecule mass spectrometry in solution using a solitary nanopore,"* Proc. Natl. Acad. Sci. (USA) 104, 8207-8277.

B.J. Nablo, K.M. Halverson, J.W.F. Robertson, T.L., Nguyen, R.G. Panchal, R. Gussio, S. Bavari, O.V. Krasilnikov, & J.J. Kasianowicz. 2008. *"Sizing the Bacillus anthracis PA(63) channel with nonelectrolyte poly(ethylene glycols),"* Biophys. J. 95, 1157-1164.

J.J. Kasianowicz, J.W.F. Robertson, E.R. Chan, J.E. Reiner, & V.M. Stanford. 2008. *"Nanoscopic porous sensors,"* Ann. Rev. Anal. Chem. 1, 737-766.

M. Kim, J.W.F. Robertson, & J.J. Kasianowicz. 2009. "*Single molecule analysis using single nanopores,"* In: Nanofluidics. Nanoscience and Nanotechnology. Eds. Edel, J.B. and A.J. deMello. Royal Society of Chemistry Publishing, Cambridge, UK, pp. 113-138.

S.E. Henrickson, E.A. DiMarzio, Q. Wang, V.M. Stanford, & J.J. Kasianowicz. *"Probing single nanometer-scale pores with polymeric molecular rulers,"* 2010. J. Chem. Phys. 132, 135101.

J.W.F. Robertson, J.J. Kasianowicz, & J.E. Reiner. *"Changes in ion channel geometry resolved to sub-Angstrom levels via single molecule mass spectrometry,"* Submitted.

J.E. Reiner, J.J. Kasianowicz, B.J. Nablo, & J.W.F. Robertson. *"A first-principles theory for nanopore-based single-molecule mass spectrometry,"* Submitted.

Device Design and Characterization Program

As microelectronics pushes into the nanoelectronics regime traditional CMOS reaches fundamental limits; new device structures such as Multi-Gate FETs (MUGFETs), fully depleted and partially depleted silicon-on-insulator, various alloys such as silicon-germanium and silicon-germanium-carbon, strained layers and other exotica such as carbon nanotube, spintronic, and phase change and molectronic device structures need to be characterized. Another addition to the portfolio is the emerging field of organic materials electronics. With all of these changes taking place, NIST has established the Center for Nanoscale Science and Technology (CNST), a multidisciplinary center composed of a research program and the Nanofab, a fee base, shared use user facility with advanced processing and metrology equipment suitable for advancing into the nanotechnology era.

Device Characterization and Reliability

Technical Contacts:
Kin P. Cheung
John S. Suehle

Goals

The goal of the Advanced Device Characterization and Reliability Project is to improve and develop reliability and electrical characterization tools for advanced and emerging CMOS technologies. Deliverables include test methods, diagnostic procedures, reliability data, electrical characterization methods, defect identification and defect generation mechanism, physical models for wear-out, and methodologies to determine energy band diagrams and barrier heights for advanced gate dielectric stack systems.

A specific focus is to increase the understanding of the relationship between gate metal, gate dielectric, and channel materials, their interface properties, and device electrical and reliability measurements.

Customer Needs

The Si microelectronics community is currently faced with major materials challenges to further scaling. The gate stack (i.e, the polysilicon gate, the SiO_2 dielectric, and the silicon substrate) that was the key enabler of integrated circuit technology for half a century, must now be entirely replaced with new materials to achieve higher performance and lower power dissipation. Higher dielectric constant materials will replace SiO_2 as a gate dielectric, metal will replace polycrystalline silicon as a gate electrode, and high mobility materials will replace silicon as a channel material. New device structures such as multigate transistor, raised source and drain, ultra-thin body, etc. will replace the conventional planer MOSFET. Accompanying these enormous changes are new and highly complex reliability issues that must be addressed.

Consumer electronics has been the main driving force for the industry. Everyday life is increasingly relying on electronics. Many functions in modern living demand increased reliability of electronics beyond the traditional standards. Some cannot tolerate any failures. These demanding reliability requirement posts new challenges that the IC industry now must face.

The characterization of current advanced and future CMOS transistors is a major measurement challenge. It is currently not possible, for example, to reliably measure the channel mobility directly on the minimum size transistors. Thus it is difficult to know if the transistor's performance is limited by series resistance or by channel mobility. It is not possible to measure CV directly on such transistors; thus many of the basic transistor parameters must be obtained indirectly. Advanced MOSFET structures may not have a way to contact the substrate, precluding the use of standard electrical characterization techniques. The issue of variability, which is a major issue for advanced CMOS technology, cannot be quantified easily without the ability of making these measurements. The need for new measurement capability is not limited to measuring the ever smaller devices. Measuring faster is also required. High performance is one of the driving forces for continued scaling. High-performance circuits have tight tolerance on transistor parameters. It is recently becoming clear that the transient shift of transistor parameters that can cause circuit failure occurs more easily in advanced CMOS technologies than in older generations of CMOS. It also is becoming clear that reliability assurance requires that the transistor be characterized at operational speed. However, the measurement of transistor parameters at full operational speed is not currently possible. This is a major deficiency that needs to be addressed. Device degradation is intrinsically a stochastic process. Reliability measurements must have good statistics to be useful. This is much more so in advanced CMOS due to variability issues. How to produce useful reliability data is itself a challenge that urgently needs a solution.

Technical Strategy

The main focus for this project is to develop device and reliability characterization methodologies for advanced and emerging CMOS technology.

We continue to improve electrical characterization techniques and methodologies to characterize charge trapping kinetics, threshold voltage, Vt, instability, defect generation rates, spatial and energetic defect profiles, and long term degradation such as time-dependent dielectric breakdown (TDDB) for both patterned

device samples and blanket films obtained from our collaborators. Studies will be conducted to determine the effect of multiple interfaces on stress-induced defect generation and wear-out. It will be determined what technique or combination of techniques provides the most consistent results for all films. The electrical results will be used to validate simulation models and compared to studies from various analytical materials characterization methods.

We will develop new measurement techniques. For example, optical-electrical combination techniques to quantify defects, defect energetics and defect positions. Such techniques are also good for band-alignment study of the gate stack. It can also be used to investigate the interface region specifically. Coupling with pure electrical techniques, a much better picture of what is happening can emerge. Another example is a specialized technique to detect a single defect to enable us to investigate how a single defect affects the behavior of a nano-scale transistor. We are particularly interested in developing new ultra sensitive CV measurement techniques to measure minimum size transistors directly. Another direction of measurement technique development is ultra-high speed measurements of transistor parameters. Finally, we will explore ways to improve the statistical quality of reliability data.

DELIVERABLES:

- Develop a fast, direct, wafer-level method of measuring the channel mobility of ultra-scaled transistors. 1Q 2010
- Develop a fast, direct, wafer-level method of measuring the series resistance of ultra-scaled transistors. 1Q 2010
- Develop an micro electron-spin-resonance spectrometer with drastically enhanced sensitivity to characterize defects In ultra scaled transistors 4Q 2010
- Develop a new electro-reflectance measurement technique for the investigation of defect generation in the high-κ/SiO_2 stack. 3Q 2010
- Conduct time-dependent dielectric breakdown study for deposited oxide SiO_2/SiC system. 4Q 2010
- Conduct electrical characterization and reliability investigation of an advanced transistor having high- κ gate dielectric and alternative channel materials such as InGaAs. 3Q 2010

Accomplishments

Reassess the frequency-dependent charge-pumping technique as a defect depth profiling tool

There has always been a need to profile the defect density in the gate dielectric as a function of depth (from the substrate interface). This need is more acute when high-κ gate stack is introduced to replace the thermally grown SiO_2. There are two main approaches to this task in the literature; both are well established for a long time. One is the low-frequency noise measurement which we showed recently that the common interpretation is not correct and that the method cannot yield depth information of defects. The other is the frequency-dependent charge-pumping method. This method has been the center of a controversy on how deep it probes for a given frequency. We show, using simple physics argument that this method also cannot yield depth information of defects. There are many variations of this method reported in the literature. They too are problematic.

A wafer-level magnetoresistance method for series resistant-free mobility extraction

For advanced CMOS using high-k/metal gate, and/or using alternate channel material, a key question is whether the channel mobility in ultra scaled device is similar to longer channel devices, with which mobility is measured. Tremendous efforts are invested in fixing mobility degradation as measured in long channel device with little assurance that the same problem actually exists in ultra short channel devices. This practice is the result of a lack of method to extract mobility directly from ultra scaled devices. We developed a wafer-level magnetoresistance technique to extract mobility directly from ultra scaled MOSFETs. An important advantage, in addition to being able to make measurement at wafer-level, is

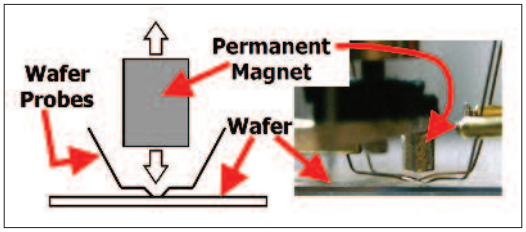

Figure 1. Using a small permanent magnet to provide the magnetic field to enable wafer-level magnetoresistance measurement.

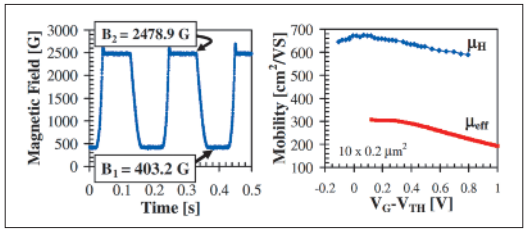

Figure 2.
a) Modulated magnetic field profile in time (magnet is driven by a voice coil);
b) measured Hall mobility as a function of gate overdrive. Also shown are the effective mobility extracted by a conventional method for comparison.

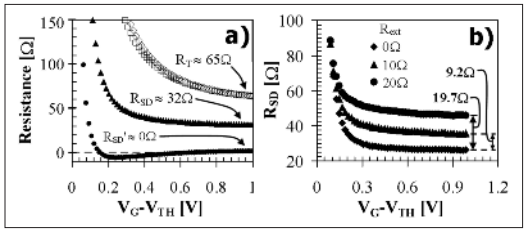

Figure 3. a) Measured total resistance as a function of gate overdrive at two linear drain bias and the extracted series resistance as a function of gate over drive.
b) Added external resistance is accurately reflected in the extracted series resistance, proving the effectiveness of the method.

that our measurement is free from the influence of series resistance for the first time.

A simple and accurate series resistance extraction method

As the channel resistance reduces with scaling and the implementation of various mobility enhancement technologies, series resistance becomes a bigger fraction of the total resistance. It is already a major limiting factor to ON current, and will only get worse. A lot of effort is currently being invested in bringing down the series resistance. However, these efforts are seriously hampered by the lack of reliable series resistance extraction methods. We developed a simple method that is free from unjustifiable assumptions and rely on simple Ig-Vd measurements from a single device.

Standards Committee Participation

JEDEC JC14.2 Committee on Wafer-Level Reliability, Dielectric Working Group, Chairman (John S. Suehle).

Pr fessional Committee Participation

North American Subcommittee Chair, 2011 VLSI- Technology, System and Application Conference (KPC).

Executive Committee Chair, 2009 IEEE International Reliability Physics Symposium (JSS).

2010 ITRS PID TWG in charge of reliability (KPC).

Technical Committee, 2010 IEEE International Conference on Integrated Circuit Design & Technology (KPC).

Technical Committee, 2010 Nano Science & Technology Institute Nanotech Conference (KPC).

Technical committee, 2010 VLSI- Technology, System and Application Conference (KPC).

Tutorial speaker, 2010 IEEE International Reliability Physics Symposium (JC).

Technical Committee, 2009 IEEE International Conference on Integrated Circuit Design & Technology (KPC).

Chairman of Dielectric Working Group, JEDEC JC14.2 Committee on WLR (JSS).

Management Committee IEEE Integrated Reliability Workshop (JSS).

Special Member of Graduate faculty, University of Maryland (JSS).

Special Member of Graduate Faculty, Rutgers University (KPC).

Guest editor for Special Issue IEEE Tran. on Device and Materials Reliability (JSS & KPC).

Editor, IEEE Transactions on Electron Devices (JSS).

Editor, IEEE Tran. on Device and Materials Reliability (KPC).

Collaborations

IBM, Alternative Gate Dielectrics.

Micron, Boise, ID, Characterization of metal gate dielectric systems.

ARL, Characterization of defects and reliability of SiC gate dielectric systems.

GE, Reliability characterization of SiC gate dielectric systems.

Intel, Characterization of high-κ/InGaAs systems.

SEMATECH Characterization of metal gate high-κ systems.

Rutgers University, Characterization of high-κ gate dielectrics.

University of Maryland, College Park, ultrathin gate oxide reliability, combinatorial analysis of advanced gate stacks.

U. Texas at Austin, Optical properties of ZrO_2 and HfO_2 for use as high-κ gate dielectrics.

U. Texas at Dallas, high-κ gate dielectric systems.

Purdue, high-κ on III-V.

Recent Talks/Publications

K. P. Cheung, *"Wafer-level magnetotransport measurement of advanced transistors – making a powerful technique even more powerful,"* 2010 ICSICT, Shanghai, Nov. 2010. Invited.

J.P. Campbell, K.P. Cheung, L.C. Yu, J.S. Suehle, K. Sheng, and A. Oates, *"New Methods for the Direct Extraction of Mobility and Series Resistance from a Single Ultra-Scaled Device,"* VLSI Symp. 2010, Accepted for presentation.

A. Akturk, M. Holloway, S. Potbhare, D. Gundlach, B. Li, N. Goldsman, M. Peckerar, and K. P. Cheung, *"Compact and Distributed Modeling of Cryogenic Bulk MOSFET Operation,"* IEEE Trans. Electron Dev., in press.

J. P. Campbell, *"NBTI: Confusion, Frustration, and . . . Promise?"* Tutorial, IRPS 2010.

J. P. Campbell, *"Gate Dielectrics, The Year in Review."* IRPS 2010.

F. Zhang, K. P. Cheung*, J.P. Campbell, J. Suehle, *"Frequency-Dependent Charge-Pumping: The Depth Question Revisited,"* IRPS 2010, May, 2010.

K. Ng, H. Oda, R. Liu, H. Inoue, and K. P. Cheung, *"Process Integration, Devices, and Structures,"* Special issue ITRS, Future Fab, Jan. 2010.

K. P. Cheung, *"On the 60 mV/dec @300 K Limit for MOSFET Subthreshold Swing."* VLSI Technology, System & Application Symp., April 2010.

N. V. Nguyen, M. Xu, O. A. Kirillov P. D. Ye, C. Wang, K. Cheung, and J. S. Suehle, *"Band Offsets and Offsets of Al_2O_3 / InxGa1-xAs (x = 0.53 and 0.75) and the Effects of Post-Deposition Annealing."* App. Phys. Lett., 96, 052107 (2010).

Akturk, A.; Holloway, M.; Gundlach, D.; Potbhare, S.; Li, B.; Goldsman, N.; Peckerar, M.; Cheung, K.P. *"Distributed numerical modeling of low temperature MOSFET operation ."* International Semiconductor Device Research Symposium, ISDRS , Dec. 2009, MD USA.

C. Wang, L.C. Yu, J.P. Campbell, K.P. Cheung, Y. Xuan, P.D. Ye, J.S. Suehle, and D. W. Zhang, *"An improved fast Id-Vg measurement technology with expanded application range",* IEEE Int. Integrated Reliability Workshop, Oct. 2009.

J.P. Campbell, *"NBTI: Why Won't this Thing Go Away?"*, Tutorial, presented at the IEEE Int. Integrated Reliability Workshop, Stanford Sierra Camp, S. Lake Tahoe, CA, October 18-22, 2009

L.C. Yu, K.P. Cheung, V. Tilak, G. Dunne, K. Matocha, J.P. Campbell, J.S. Suehle, and K. Sheng, *"A fast, simple wafer-level Hall-mobility measurement technique"*, IEEE Int. Integrated Reliability Workshop, Oct. 2009.

L.C. Yu, K.P. Cheung, V. Tilak, G. Dunne, K. Matocha, J.P. Campbell, J.S. Suehle, and K. Sheng, *"Demonstration of a Wafer-level Hall Mobility Measurement Technique"*, IEEE Semiconductor Interface Specialist Conference, December 3-5, 2009, Arlington, VA.

C. Wang, K. P. Cheung, Y. Yuan, P. D. Ye, *"Fast I-V characterization of Inversion-mode $In_{0.75}Ga_{0.25}$MOSFETs with ALD Al_2O_3 as gate dielectric."*, Material Research Society Fall Meeting, Nov 2009.

L.C. Yu, K.P. Cheung, V. Tilak, G. Dunne, K. Matocha, J.P. Campbell, J.S. Suehle, K. Sheng, *"Wafer-level Hall Measurement on SiC MOSFET."* International Conference on Silicon Carbide and Related Materials, Oct. 2009.

L.C. Yu, , K.P. Cheung, G. Dunne, K. Matocha, J.S. Suehle, K. Sheng, *"Gate Oxide Long-Term Reliability of 4H-SiC MOS Devices."*, International Conference on Silicon Carbide and Related Materials, Oct. 2009.

J.P. Campbell, J. Qin, K.P. Cheung, L. Yu, J.S. Suehle, A. Oates, K. Sheng, *"The Origin of Random Telegraph Noise in Highly Scaled nMOSFETs."* International Reliability Physics Symposium April 2009. (Outstanding paper award)

J.P. Campbell, L.C. Yu, K.P. Cheung, J. Qin, J.S. Suehle, A. Oates, K. Sheng, *"Large Random Telegraph Noise in Nano-Scale nMOSFETs Operating in the Sub-Threshold Regime"*, International Conference on Integrated Circuit Design & Technology, 2009.

J.P. Campbell, K.P. Cheung, J.S. Suehle, A.S. Oates, *"The Negative Bias Temperature Instability vs. High-Field Stress Paradigm,"* International Conference on Integrated Circuit Design & Technology, 2009, invited.

L. Yu, K. P. Cheung, J. S. Suehle, J. P. Campbell, K. Sheng, A. J. Lelis, S.-H. Ryu, *"Channel Hot-Carrier Effect of 4H-SiC MOSFET,"* Materials Science Forum Vols. 615-617 (2009) pp 813-816

J.P. Campbell, K.P. Cheung, J.S. Suehle, A. Oates, *"Negative-Bias Temperature Instability Induced Electron Trapping,"* Appl. Phys. Lett. v 93, n 3, , 2008, p 033512.

J.P. Campbell, K.P. Cheung, J.S. Suehle, A. Oates, *"Additional Insight into Device Transient Behavior from Fast-GM Measurements,"* IEEE Electron Dev. Lett., 29(9), 1065(2008).

L. Yu, K. P. Cheung, J. S. Suehle, K. Sheng, *"Intrinsic Oxide Reliability of SiC MOS Devices,"* 2008 International Integrated Reliability Workshop, Oct 2008.

J.P. Campbell, J. Qin, K.P. Cheung, L. Yu, J.S. Suehle, A. Oates, K. Sheng, *"The Origins of Random Telegraph Noise in Highly Scaled SiON nMOSFETs,"* 2008 International Integrated Reliability Workshop, Oct. 2008.

Kin P. Cheung, J.P. Campbell, *"The transient behavior of NBTI - A new prospective,"* International Conference on Solid-State and Integrated-Circuit Technology, Oct. 2008, Beijing, China, Invited.

J.P. Campbell, K.P. Cheung, J.S. Suehle, A. Oates, *"The Fast Initial Threshold Voltage Shift: NBTI or High-Field Stress?"* 2008 IEEE International Reliability Physics Symp., Pheonix, AZ, USA.

H. D. Xiong, Dawei Heh, Shuo Yang, Xiaoxiao Zhu, Moshe Gurfinkel, Gennadi Bersuker, D. E. Ioannou, Curt A. Richter, Kin P. Cheung, and John S. Suehle, *"Stress-induced defect generation in HfO_2/SiO_2 stacks observed by using charge pumping and low frequency noise measurements,"* 2008 IEEE International Reliability Physics Symp., Pheonix, AZ, USA.

Curt A. Richter, Hao D. Xiong, Xiaoxiao Zhu, Wenyong Wang, Vincent M. Stanford, Qiliang Li, D. E. Ioannou, Woong-Ki Hong, and Takhee Lee, *"Measurements for the reliability and electrical characterization of semiconductor nanowires,"* 2008 IEEE International Reliability Physics Symp., Pheonix, AZ, USA, invited paper.

J.P. Campbell, K.P. Cheung, J.S. Suehle, A. Oates, *"Electron Trapping: An Unexpected Mechanism Of NBTI and its Implications,"* 2008 VLSI Technology Symp., Hawaii, USA.

Kin P. Cheung, and John S. Suehle, *"The Challenge of Measuring Defects in Nanoscale Dielectrics,"* invited paper, 2008 Electrochemical Soc. Meeting, Phoenix, AZ, USA.

D.H. Hill and R.A. Bartynski, N.V. Nguyen, Albert C. Davydov, and Deane Chandler-Horowitz, and Martin M. Frank, *"The relationship between local order, long range order, and sub-bandgap defects in hafnium oxide and hafnium silicate films,"* Applied Physics Letters, submitted.

Oana D. Jurchescu, Behrang H. Hamadani, Hao D. Xiong, Sungkyu K. Park, Sankar Subramanian, Neil Zimmerman, John E. Anthony, Thomas N. Jackson, and David J. Gundlach, *"Correlation between microstructure, electronic properties and flicker noise in organic thin film transistors,"* Appl. Phys. Lett., in press.

M. Gurfinkel, H.D. Xiong, K.P. Cheung, J. Suehle, J.B. Bernstein, Yoram Shapira, A.J. Lelis, D. Habersat, N. Goldsman, *"Characterization of transient gate oxide trapping in SiC MOSFETs using fast I-V techniques,"* IEEE Trans. Electron Dev. accepted.

Y. Wang, K. P. Cheung, R. Choi, B.-H. Lee, *"An Accurate Capacitance-Voltage Measurement Method for Highly Leaky Devices,"* IEEE Trans. Electron Dev. submitted.

N. V. Nguyen, H. D. Xiong, J. S. Suehle, and O. Kirillov, E. M. Vogel,P. Majhi and H.-C. Wen, *"Internal Photoemission Spectroscopy of [TaN/TaSiN] and [TaN/TaCN] Metal Stacks,"* Applied Physics Letter, 92, 092907 (2008).

N. V. Nguyen, O. A. Kirillov, W. Jian, J. E. Maslar, W. A. Kimes, and J. S. Suehle, *"Interface Barrier Determination by Internal Photoemission: Applications to Metal/Oxide/Semiconductor Structure,"* Invited paper, 2008 Electrochemical Soc. Meeting, Phoenix, AZ, USA.

J. E. Maslar, W.S. Hurst, D.R. Burgess, W.A. Kimes, N.V. Nguyen, E.F. Moore, J.T. Hodges, *"In Situ Gas Phase Diagnostics for Hafnium Oxide Atomic Layer Deposition,"* Invited paper, 2008 Electrochemical Soc. Meeting, Phoenix, AZ, USA.

J. J. Kopanski, M. Y. Afridi, S. Jeliazkov, W. Jiang, T. Walker, *"Scanning Kelvin Force Microscopy For Characterizing Nanostructures in Atmosphere,"* Proceedings of the International Conference on Frontiers of Characterization and Metrology for Nanoelectronics, pp. 530-534, Gaithersburg, MD, March 27-29, 2007. (Sept. 2007).

N. V. Nguyen, O. Kirillov, H. D. Xiong, and J. S. Suehle, *"Internal Photoemission Spectroscopy of Metal Gate / High-κ / Semiconductor Interfaces,"* Frontiers of Characterization and

Metrology for Nanoelectronics: 2007, AIP Conference Proceedings 931, page 308 (2007).

E. Maslar, W.S. Hurst, D.R. Burgess, Jr., W.A. Kimes, N.V. Nguyen, and E.F. Moore, *"In Situ Characterization of Gas-Phase Processes During Hafnium Oxide Atomic Layer Deposition,"* ECS Transactions, vol 2, 133-143 (2007).

J. J. Kopanski, *"Scanning Capacitance Microscopy for Electrical Characterization of Semiconductors and Dielectrics,"* in the book: Electrical and Electromechanical Characterization by Scanning Probe Microscopy, Springer Science + Business Media, Inc., New York, NY (Feb. 2007).

Hao D. Xiong, Dawei Heh, Moshe Gurfinkel, Qiliang Li, Yoram Shapira, Curt Richter, Gennadi Bersuker, Rino Choi, John S. Suehle, *"Characterization of Electrically Active Defects in High-κ Gate Dielectrics By Using Low Frequency Noise, Charge Pumping, and Fast Id-Vg measurements,"* 2007 15th biannual conference Insulating films on semiconductor, Greece.

Hao D. Xiong, Dawei Heh, Moshe Gurfinkel, Qiliang Li, Yoram Shapira, Curt Richter, Gennadi Bersuker, Rino Choi, John S. Suehle, *"Characterization of Electrically Active Defects in High-κ Gate Dielectrics By Using Low Frequency Noise and Charge Pumping Measurements,"* Microelectronic Engineering, 84, 2230 (2007).

Wenyong Wang, Hao D. Xiong, Monica D. Edelstein, David Gundlach, John S. Suehle, Curt A. Richter, Woong-Ki Hong and Takhee Lee, *"Low-frequency noise characterizations of ZnO nanowire field effect transistors,"* Journal of Applied Physics 101, 044313 2007.

Hao D. Xiong, Wenyong. Wang, Qiliang Li, C.A. Richter, J.S. Suehle , Woong-ki Hong, Takhee Lee, and D. M. Fleetwood, *"Random Telegraph Signals in n-type ZnO Nanowire Field Effect Transistors at Low Temperature,"* Appl. Phys. Lett. 91, p.053107 (2007).

Qiliang Li, X. Zhu, H.D. Xiong, S. M. Koo, D. E. Ioannou, J. J. Kopanski, J. S. Suehle, and C. A. Richter, "Silicon nanowire on oxide/nitride/oxide for memory application," Nanotechnology, 18, 235204 (2007).

Qiliang Li, Sang-Mo Koo, Hao D. Xiong, M. D. Edelstein, J. S. Suehle, X. Zhu, D. E. Ioannou, and C. A. Richter, *"Methods to Characterize the electrical and Mechanical properties of Si Nanowire,"* AIP proceeding for 2007 International Conference on Frontiers of Characterization and Metrology for Nanoelectronics, Gaithersburg.

Qiliang Li, Curt A. Richter, Hao D. Xiong, and John, S. Suehle, *"Nanowire Electromechanical Logic Switch,"* Proceedings of the 7th IEEE International Conference on Nanotechnology, pp. 141-145, August 2-5, 2007, Hong Kong.

H.D. Xiong, Wenyong Wang, Qiliang Li, Curt A. Richter, John S. Suehle, Woong-Ki Hong, Takhee Lee, and Daniel M. Fleetwood, *"Random Telegraph Signals and 1/f Noise in ZnO Nanowire Field Effect Transistors,"* Proceedings of the 7th IEEE International Conference on Nanotechnology, pp. 1139-1143, August 2-5, 2007, Hong Kong.

H.D. Xiong, W. Wang, M. Edelstein, D. Gundlach, J. Suehle, C. A. Richter, W. Hong, and T. Lee, *"Noise in ZnO nanowire field effect transistors,"* Chinanano 2007, Beijing.

Nanoelectronic Device Metrology

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Goals

The overall goal of the Nanoelectronic Device Metrology (NEDM) task is to develop the metrology that will help enable the heterogeneous integration of new nanoelectronic information processing technologies with Complementary Metal Oxide Semiconductor (CMOS) to extend integrated circuit technology to and beyond the end of conventional CMOS dimensional scaling and, eventually, to enable the invention of a new information processing platform technology. Specifically, the NEDM is developing the precise metrology and measurement methods required for the systematic characterization of emerging nanotechnologies such as Si-based nanoelectronics, semiconductor nanowire transistors, carbon-based (e.g., carbon nanotubes, and graphene) electronics, and molecule-based devices.

NIST scientists are deeply involved in a wide range of nanoelectronics research. The goal of the Nanoelectronics Device Metrology (NEDM) project is a fundamental one. Project scientists are developing a total metrology package – a set of new tools, tests, and methods for the coming age of nanoelectronics – that will help nanotechnologies enter the marketplace more quickly. Such a large task is well suited to NIST's uniquely broad expertise and experimental capabilities.

Customer Needs

Nanoscale electronic devices, with components on the billionth-of-a-meter scale, represent one of the most active fields of electronics research. Mainstream CMOS, which is the current basis of ULSI (Ultra-Large-Scale Integration) circuits, is approaching fundamental limits associated with the laws of quantum mechanics and the limitations of fabrication techniques. As stated in the 2007 International Technology Roadmap for Semiconductors (ITRS), "The semiconductor industry is facing two … difficult challenges related to extending integrated circuit technology to and beyond the end of CMOS dimensional scaling. … extending CMOS beyond its ultimately scaled density and functionality by [heterogeneously integrating new information processing technologies with CMOS, and] … [extending] information processing substantially beyond that attainable by CMOS alone using an innovative combination of new devices and architectural approaches … and, eventually, inventing a new information processing platform technology." This need is so strong that a consortium of companies in the Semiconductor Industry Association (SIA) has established the Nanoelectronics Research Initiative (NRI). NIST is teaming with the NRI to accelerate research in nanoelectronics.

The materials traditionally used in Si-based CMOS will not be sufficient to overcome the barriers associated with these difficult challenges. New nm-scale materials will need to be developed, characterized, and incorporated into information processing devices and architectures to extend CMOS performance and/or functionality. It is expressed in the 2009 ITRS that improved metrology tools are needed to enable viable emerging material technologies and guide their evolution. The NEDM aims to provide this critical measurement science.

Two promising beyond-CMOS technologies that each takes a very different fabrication approach are molecule-based devices and Si-based quantum electronic devices. Molecule-based devices are based upon bottom-up fabrication paradigms, while Si-based nanoelectronics are based upon the logical continuation of the top-down fabrication approaches used in CMOS manufacturing. These two approaches bracket the possible manufacturing techniques that will be used to make future nanoelectronic devices.

Many predict that molecule-based devices will have important technological impacts on the computational and communication systems of the future. In these systems, molecules perform the functions of electronic components. Alternatively, research and development for silicon-based nanoelectronics (e.g., Si-nanowire FETs, Si-based RTDs [resonant tunneling diodes], and silicon quantum dots) for the post-CMOS era are currently of interest due to their inherent compatibility with CMOS technology.

Carbon-based materials, particularly graphene and carbon nanotubes (CNTs) have emerged as perhaps the most promising of the research materials for next generation electronics. Graphene (a

recently discovered form of carbon consisting of a single atomic sheet of carbon in a hexagonal lattice) is a high-mobility semi-metal with a distinctive linear energy momentum dispersion relation. Graphene's excellent room-temperature mobility relative to conventional semiconductors makes it a promising high mobility channel replacement material for charge-based transistors. The NIST graphene team is developing electrical metrology to enable the advancement of both conventional charge-based and non-conventional beyond-CMOS graphene-based electronics.

Before bulk carbon nanotubes can fulfill their promise for multifunctional (electronic, electrical, structural, thermal) composites, better methods are needed for purification, dispersion and identification of raw nanotube materials. Predicted nanotube behavior may be compromised by the presence of impurities and molecular defects. Simple, inexpensive and scalable methods are preferred for characterizing bulk material in the presence of impurities and defects. In addition, reproducible measurement results are difficult due to physical contact between the metrology instrument and the nanomaterials. We are working toward purification and dispersal by laser processing rather than wet chemistry. In addition, we continue to pursue non-contact metrology of electronic and optical properties.

Low-dimensional structures such as CNTs and semiconductor nanowires are among the candidates to replace the FET channel in MOSFETs with a higher carrier mobility material than strained Si. The NEDM is utilizing Si-nanowires (SiNWs) as the test platform to develop the measurement science necessary to enable the utilization of quantum confined structures to extend the performance of traditional CMOS devices. In order to have effective test structures for metrology development, we are making advances in experimental NW growth and device fabrication as well as material and device characterization. We are also pursuing GaN nanowire growth, characterization, and integration with conventional Si circuitry. The latter work includes exploration of methods for placement of nanostructures that have the potential to achieve acceptable manufacturing speed, such as inkjet printing.

In all these cases, our project has the capability to offer early guidance to these emerging fields and to assist companies in pursuing productive areas and rejecting problematic ones. Because these fields are not yet mature, as our relatively moderate efforts progress, they can yield large payoffs for the customers.

Technical Strategy

The Nanoelectronic Device Metrology project aims to develop new measuring techniques and standards that are crucial in the effort to develop these technologies to the point where commercial applications become feasible. This task involves determining the critical metrology needs for these exploratory technologies. Ultimately, this project will yield a toolbox of measurement methods that will allow engineers to relate the performance of nanoelectronic devices to the structures and properties of the materials of which they are made.

The NEDM task's technical strategy is to develop innovative measurement methods for specific emerging nanoelectronic systems (i.e., emerging research devices and materials) spanning a range of technologies. By collaborating with NRI-sponsored researchers, NIST will be able to ensure that its programs focus on developing critical measurement tools likely to accelerate advances in this visionary, high risk area of research. Following are brief descriptions of the NEDM's strategies for developing the critically needed measurement tools to enable successful advances in nanoelectronics.

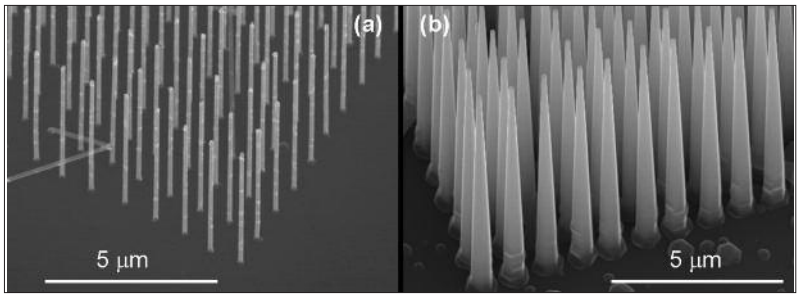

Figure 1. Arrays of Si NW grown at 850 °C from 100 nm Au dots prepared by e-beam lithography. Tapering of Si NWs can be controlled by growth conditions, e.g., $SiCl_4/H_2$ ratio and growth pressure: (a) 600 Torr, (b) 300 Torr.Flip chip lamination to form reliable metal/monolayer/Si molecular junctions.

Develop the electrical and physical metrology of Si-based nanoelectronics. The focus of this task is the basic building blocks of silicon quantum electronic devices (e.g., quantum layers, wires, and dots of silicon surrounded by silicon dioxide). By identifying and addressing the critical metrology issues associated with these basic building blocks, the basis of metrology for future Si-based ULSI nanotechnology will be defined. The NEDM is currently focusing on Si-nanowires (such as shown in Figure 1): their growth, device assembly approaches, and advanced electrical characterization. Our short- and long- term plans include growth of SiGe alloy and Si/Ge core-shell NW heterostructures; development of controlled n- and p- doping of Si and Ge NWs; fabrication of core-shell and axial p/n junction Si nanowire geometries; fabrication of dielectrophoretically assembled and in-situ grown SiNW arrays in microfluidic channels; development of advanced FET NW device structures for sensor applications and development of Si NW based PV and Li-ion battery test platforms. We have developed a simple in situ directed growth method fabricating SiNW devices, and are using it to make and characterize devices (such as high-performance transistors and charge trapping memory structures) incorporating high-κ gate dielectrics such as illustrated in Figure 3. We are developing advanced test structures and improved electrical test methodologies such as (i) advanced capacitance measurement techniques for critical small (aF-scale) capacitances in nanoelectronics devices such as nanowires and (ii) applying improved noise characterization to determine technical validity of innovative nanoelectronic structures and probe-scattering dynamics.

DELIVERABLES:

- Growth of vertically aligned Si NW arrays with controlled geometries (NW length, diameter, shape and separation). Prepare and submit manuscript. 2Q 2010
- Characterize high-κ trapping layer thickness dependence in SiNW-based non-volatile memory devices . Prepare and submit manuscript. 3Q 2010.
- Development of controlled doping of Si nanowires from solid boron- and phosphorus-containing precursors. 3Q 2010.
- Growth and electrical characterization of core-shell and axial p/n junction Si NW device structures. Prepare and submit manuscript. 4Q 2010

Develop robust molecular test structures in order to use them to measure the electrical properties of molecules. The measured electrical properties will be correlated with systematic characterization studies by a variety of advanced analytical probes and the results used to determine charge conduction mechanisms and in the validation of predictive theoretical models.

Develop spectroscopic probes to measure the impact of contact, orbital geometry, and molecular structure of molecular films bound to solid surfaces. Determine the interface dipole and the change to surface work function of molecular films on solid surfaces. A longer term goal is to determine the factors that influence energy level alignment on molecular films bound to metal and semiconductor surfaces.

DELIVERABLES:

- Demonstrate innovative backside FTIR characterization of organic materials in buried metal/molecule/Si junctions.under electrical bias. 3Q 2010.
- Investigate the electrical and physical behavior of a variety of molecules in metal/molecule/Si junctions formed by using flip-chip lamination methods. Prepare and submit manuscript. 3Q 2010.
- Electrically and optically characterize the properties of carbon/molecule/metal junctions formed on glassy carbon. 4Q 2010.

The Nanoelectronics Research Initiative (NRI) has identified the need to develop new materials and devices for post-CMOS electronics and has cited graphene as a promising technology. Graphene non-charged based electronics and controlled fabrication of graphene is the key to successful specific applications that serve industrial post-CMOS needs and NIST quantum electrical standards applications.

Because of its unique properties, graphene may revolutionize aspects of commercial electronics and optoelectronics. The knowledge base and measurement tools to understand the basic physics of graphene, such as the characterization and control of defects, the effect of defects and substrate properties on charge transport, the coupling between charge and photons, and how to measure and optimize device properties (such as electrical contacts) are under development. These are the necessary metrology tools to enable the emergence of promising graphene technologies.

DELIVERABLES:

- Characterize CNT FETs under high current conditions: Gain insights into the impact ionization regime of CNT FETs by studying their noise properties. Prepare and submit manuscript. 4Q 2010
- Controlled development of graphene samples - Acquire fully characterized epitaxial graphene and fully characterized CVD graphene Q3 2010.
- Fabricate graphene devices for multiple measurements: Raman, STM, transport measurements Q3 2010.
- Develop graphene quantum Hall standard. Fabricate metrologically useful graphene quantum Hall standard Q3; Compare graphene quantum Hall device to GaAs-based device Q4 2010.

Establish a quantitative characterization toolbox for practical measurements of bulk nanomaterials building upon non-contact probes recently pioneered at NIST. This toolbox will provide rapid, quantitative methods for identifying CNT properties. Existing measurement tools are neither practical nor useful for current and future large-scale production of nanomaterials. These protocols often rely on physical contact between the test probe and the material under study. However, physical contact between probes and nanomaterials may alter the material property of interest. Advanced, cost effective analytical techniques are needed so that manufacturers, product developers, and regulatory agencies can truly "see" what they have. Photons, being massless and chargeless are an ideal, non-contact probe of nanoscale properties.

Compound semiconductor nanostructure integration with Si circuitry: Specialized functionality can often only be obtained by changing material systems, particularly where photonics interfaces or ultrahigh frequency devices are needed. Heterogeneous integration presents a challenge to realizing many of the benefits of new materials, and the small dimensions of nanowires increase the difficulty. Demonstrations of integration using liquid dispersal and inkjet-like technologies allow NIST and industry partners to identify the key parameters that must be measured and optimized for manufacturable heterogeneous integration.

DELIVERABLES:

- Measure placement yield for semiconductor nanowires using inkjet-like dispersal. 4Q 2010
- Measure photoconductivity of GaN nanowire integrated into Si transistor chip. 4Q 2010

Accomplishments

■ *Silicon-based molecular electronic structures formed by using Flip-Chip lamination.* A substantial barrier to the realization of molecular electronics is the formation of the top metal electrode. We developed a novel approach schematically illustrated in Figure 2 to obtain high-quality silicon-molecule-Au molecular electronic structures. This approach overcomes two limiting challenges and allows (1) the formation of high-quality bi-functional monolayers on silicon and (2) the attachment of a metal electrode to the molecular layers on silicon. We utilize a novel nanotransfer printing (nTP) technique to first obtain ultrasmooth gold films on flexible plastic substrates. This allows us to fabricate dense monolayers by using self-assembly, a process that is not chemically feasible on Si due to the large molecular sticking coefficient. Second, these dense carboxylate-functionalized thiol monolayers on Au are chemically bonded to silicon by using a flip-chip lamination process, overcoming the detrimental aspects observed with conventional metallization (i.e. molecular displacement and metal filament formation). In this way, we are able to obtain dense bifunctional monolayers bonded to both silicon and ultrasmooth gold electrodes under mild conditions.

High-quality monolayers on semiconductor substrates are one of the most promising configurations for future generations of molecular-based devices for semiconductor electronics, biosensing, and optoelectronic applications. These results represent an essential advance in the reproducible fabrication of molecular junctions with high yield and fidelity. In addition, this approach can be extended to a variety of molecules and electrodes extending our impact into many technologies.

■ *Large-scale integration of high-performance silicon nanowire field effect transistors.* A CMOS-compatible self-aligning process was de-

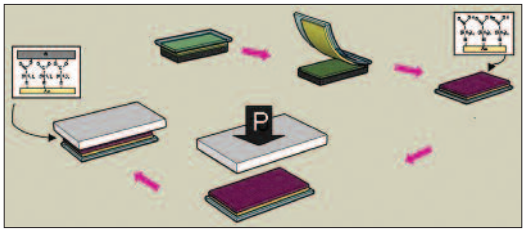

Figure 2. Flip chip lamination to form reliable metal/monolayer/Si molecular junctions.

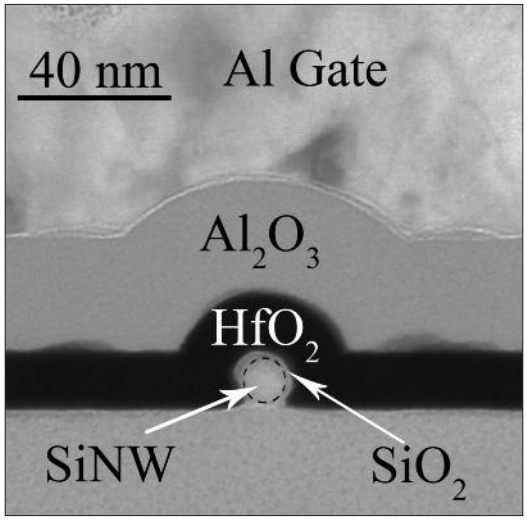

Figure 3. Cross sectional view of a Si-nanowire based SONOS-like memory with a HfO_2 high-K charge-trapping layers.

veloped that enables the large-scale-integration of high-performance nanowire field effect transistors. These SiNW FETs have well-saturated drain currents, steep subthreshold slopes at low drain voltage and a large on/off current ratio (>10^7). When traditional measurements of the drain current versus the applied gate voltage are performed, the observed subthreshold swing is as small as 45 mV/dec, which is substantially beyond the thermodynamic limit (60 mV/dec) of conventional planar MOSFETs. It is believed that these excellent device characteristics are achieved by using a clean integration process and a device structure that allows effective gate–channel–source coupling to tune the source/drain Schottky barriers at the nanoscale.

■ *Nanowire SONOS-Like Memory with high-K Charge-Trapping Layers.* An innovative ''self-aligned" process was developed and used to fabricate Si- nanowire (SiNW) channel, Silicon-Oxide-Nitride-Oxide-Silicon (SONOS)-like, non-volatile memory (NVM) cells with HfO_2, high-κ charge trapping layers formed by using atomic layer deposition (Figure 3). Due to the enhanced electrostatic control of the ''surrounding" gate, the memory cells exhibit high performance characteristics (i.e., large memory windows, fast Program/Erase operations, long retention time and good endurance). Atomic-layer-deposition processes were used to vary the dielectric layer materials and thicknesses in order to determine the importance of the various dielectric layers in the charge-trapping dielectric. Cells with an Al_2O_3 blocking layer outperform cells that have a traditional SiO_2 blocking layer. As the thickness of HfO_2 increases from 5 nm to 30 nm, the charge trap density increases as expected, while the program/erase speed and retention remain the same. This data indicates that the electric field across the tunneling oxide is not affected by HfO_2 thickness.

■ *Engineering the Electron Transport of Silicon-Based Molecular Electronic Devices via Molecular Dipoles.* We demonstrate that charge transport through a CMOS-compatible molecular electronic device is dominated by one of two different transport regimes depending on the dipole of the molecular monolayer in the junction, doping level of the silicon substrate, and bias applied to the device. The two observed transport regimes are: (1) a regime where the transport is limited by the Schottky barrier and the molecular dipole results in a silicon band bending at the junction interface, and (2) a tunneling regime where the molecular dipole creates a small local electric field that screens the electrical transport.

The dipole at the semiconductor-molecule interface is determined by both the dipole of the body of the molecule and the nature of the covalent Si-molecule attachment. We examined the change in work function of the silicon surface after formation of Si-O-C, Si-C-C, and Si-S-C bonded alkyl monolayers and separated charge transfer and dipolar contributions. Core level electronic spectra taken as a function of semiconductor doping reveal shifts in binding energy attributed to molecular bonding. Valence band spectra reveal the work function of the molecule-Si composite as a function of semiconductor doping and atomic tether. By combining valence band spectra with core level spectra, the electronic properties of the molecule-Si system were understood. In particular, the relative contribution of charge transfer due to surface band bending and the polarization due to molecular dipoles were determined. The O, C, and S atomic tethers induce differing amounts of band bending and interface dipoles which can be utilized to engineer the electronic properties of molecule-semiconductor junctions.

■ *Capacitance test structures for on-chip evaluation of nanoelectronic devices:* A test chip to evaluate the performance of new approaches to the measurement of small capacitances (femto-Farads to atto-Farads range) has been designed, fabri-

cated, and systematically characterized. The test chip consists of an array of metal/oxide/semiconductor (MOS) capacitors, metal/insulator/metal (MIM) capacitors, and a series of systematically varying capacitance structures directly accessible by an atomic force microscope probe. The nominal capacitances of the test devices range from 0.3 fF (10^{-15} F) to 1.2 pF (10^{-12} F). Measurement of the complete array of capacitances by using an automatic probe station produces a "fingerprint" of capacitance values from which, after correction for pad and other stray capacitances, the relative accuracy and sensitivity of a capacitance measurement instrument can be evaluated.

■ Magnetotransport properties of suspended graphene characterized: Suspended graphene test devices were successfully fabricated in the NIST NanoFab. Magnetotransport properties were investigated at various temperatures and with respect to the influence of current annealing. Device geometries with two- and four-probe terminals and different aspect ratios were compared and the effects of disorder potential modifications were investigated.

■ Preparation and Evaluation of Graphite Oxide. The reduction of graphite oxide (GO) thin films was evaluated at 220 °C using a combination of infrared (FTIR) and X-ray photoemission spectroscopies (XPS). The results were correlated with electrical resistance measurements (Figure 4). The chemical composition of GO was reduced from $C_8(OH)_3O_{0.8}$ to $C_8(OH)_{0.5}O_{0.3}$ after nearly 24 hours of low temperature processing. The sheet resistance of dropcast GO thin films processed at 220 °C in air was 8 kΩ sq^{-1}, similar to GO reduced at > 800 °C in an inert atmosphere.

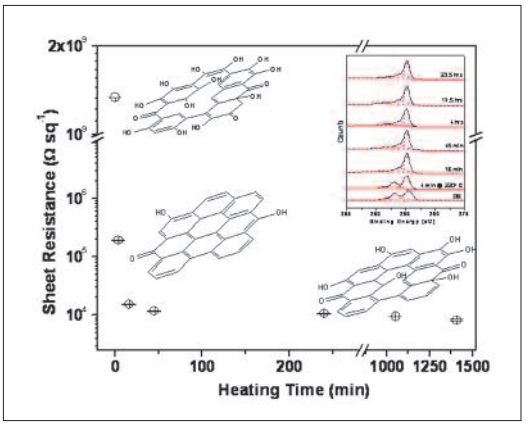

Figure 4. Sheet resistance as a function of GO processing at 220 °C. Inset shows C 1s XP spectral region of GO processed at 220 °C for 0, 4 min, 16 min, 45 min, 4 hrs, 17.5 hrs, and 23.5 hrs.

■ *Investigation of using molecular structure as a dopant in conductive molecular films.* Metal-molecule-metal junctions composed of organic molecular wires formed via self-assembly are relevant in the empirical testing of molecules used in electronics. One key is to understand the way the monolayer structure affects transport through arrays of molecules. We studied how the molecular electronic levels evolve under the influence of molecular substitution, metal substrate, and intermolecular interactions. We used a joint experimental and computational approach to study the electronic structure and electrostatic properties of a series of self-assembled donor and acceptor substituted (oligo)pheneylene-ethynylenethiols on gold. Photoemission spectroscopy was used to determine the energy-level alignment for the monolayers, the change to the work function upon chemisorptions, and the monolayer coverage. Isolated molecule and small cluster calculations were performed to detect changes in geometry, electronic structure, and charge distribution upon chemisorption. The calculated densities of electronic states allowed for the assignment of the higher-lying occupied states provided by the photoemission data. Calculated estimates of the surface, bond dipole, and image potential energies were used to estimate contributions of each to the measured work function change. Good correlation between the experimental and theoretical values was found. Importantly, the results point to a dependence of the dipole contributions on the orientational order of the self assembled monolayer (SAM). One avenue for "doping" molecules has been through substitution. These data also illustrate that substitution of conjugated molecular films does not affect the alignment of the valence molecular states, and other avenues may need to be explored.

■ *Demonstration of synthesis and growth of molecular films with tunable barriers and dipoles.* Two parameters of interest in the design of interfaces are the barriers to charge injection and the work function. In the case of monolayer covered surfaces these two parameters have been difficult to independently tune due to factors such as designing and synthesizing compounds with known valence energies, understanding how these orbitals align when bound to a surface, and predict-

ing how the molecular dipole will alter the metal work function. We have designed a set of experiments to tune both parameters independently by modifying the molecular dipole base while keeping the molecular core constant using substituted biphenyl dithiols. Monolayers were grown on Au and photoemission spectra of each film were measured to determine the position of the highest occupied molecular state and the change in the substrate work function, where the change to the substrate work function is related to the dipole of the molecule. We observed that through isolation of the molecular core from the molecular terminus we were able to tune the substrate work function with no measureable variation in the occupied valence states. The substrate work function was also highly dependent on monolayer coverage. Thus, through careful growth conditions and selection of the molecule both the work function and valence electronic properties can be independently controlled.

■ *Fabrication of vertically-aligned Si nanowire arrays with controlled placement, shape, orientation, and structure.* MSEL group has built a versatile CVD system for fabricating Si, Ge, and SiGe alloy thin films and nanowires (NWs). The system includes a hot-wall horizontal reactor with four independently controlled temperature zones; it is equipped with a computer-controlled gas delivery system. The reactor is designed to be capable of growing Si and SiGe alloys on substrates up to 2" in diameter at atmospheric or reduced pressure. The system utilizes SiH_4 and $SiCl_4$ as Si sources, solid Ge or $GeCl_4$ as Ge sources, solid boron-based and phosphorus-based sources for p- and n- type doping, and H_2 and HCl gases for *in-situ* growth modulation and reactor etching. This set of precursors allows the conduction of NW growth in a wide temperature range from 450 °C to 1050 °C. The reactor design enables rapid growth interruption/restoration, which is essential for realization of abrupt interfaces in fabricated heterostructures, such as axial p/n junctions in NWs.

The new CVD system significantly enhances NEDM's capability of fabricating Si and SiGe nanostructures with desired structural and electronic properties for nano-metrology needs. We have succeeded in growing regularly spaced, vertically aligned Si NW arrays with controlled dimensions, morphology and placement. NW diameter and placement are reliably controlled through lithographically defined arrays of catalytic gold islands, which serve as nucleation sites for VLS (vapor-liquid-solid) grown nanowires. Figure 1 shows two sets of Si NW arrays with prismatic (a) and conical (b) shapes, where the NW shape can be precisely controlled by the growth conditions. Complete control over NW geometries enables fabrication of large-scale, well-defined 3D nanostructured platforms for electronic (logic, memory), energy (photovoltaics, Li-batteries), sensor (bio-, gas, and chemical sensors), and optoelectronic (nano-LEDs and lasers) applications.

We have also studied the kinetics of Rapid Thermal Oxidation (RTO) of Si nanowires. Our results demonstrated that RTO can be employed for rapid fabrication of uniform oxide shells over NWs with controlled thicknesses suitable for device applications. Compared to conventional furnace oxidation, RTO eliminates oxide growth retardation with respect to planar Si and exhibits much weaker dependence of oxide thickness on the Si NW diameter.

■ *Advanced Measurement Methods for Nanowire-Based Nanoelectronic Devices:* Researchers in EEEL's Semiconductor Electronics Division have made advances in the electrical characterization of semiconductor nanowire-based nanoelectronic devices. The researchers demonstrated simple and easily accessible approaches to fabricate and test the nanowire devices. These techniques should enable a large range of scientists to perform research to advance nanowire research and technology. The research efforts were published in the *IEEE Transactions on Electron Devices* special issue on "Nanowire Transistors: Modeling, Device Design, and Technology," November 2008. EEEL researchers, in collaboration with engineers at George Mason University, fabricated the nanowire devices via two unique approaches: one based upon harvesting and positioning nanowires and one based upon the direct growth of nanowires in predefined locations. Test structures were then fabricated and electronically characterized to probe the fundamental properties of the nanowires. Noise measurements obtained by these test structures provided important information about current transport and fluctuations in materials and devices. Noise measurements such as these are a powerful method for probing trapping defects in nanoelectronic devices.

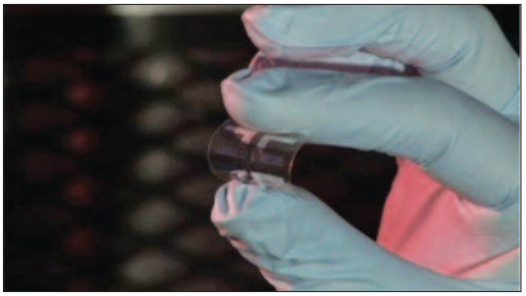

Figure 4. A flexible memristor.

■ *NIST Develops a Flexible Memristor:* We have demonstrated a flexible, solution-processed, nonvolatile, low power, inexpensive, TiO_2-based flexible memory component (Figure 5). The electrical behavior of this component is consistent with a memristor, an electrical device that has been recently touted as the missing fourth circuit element. Our flexible memory device has an operation voltage of less than 10 V, on/off ratios greater than 10,000:1, exhibits memory potential that is nonvolatile for over 1.2 x 106 s, and is operational after 4,000 flexes. This technology has potential advantages over existing flexible memory devices including low power operation, rewritability, and a simple two-terminal room temperature processed device design.

■ *Plasmonics in the optical cleaning of nanotubes.* It has been experimentally observed that amorphous carbon is removed from as-prepared, bulk, single-walled carbon nanotubes by illumination with 248 nm (5 eV) UV light. The process by which this occurs has not yet been rigorously identified before now. We have used a combination of experiments and modeling to explain how localized surface plasmon pairs can be induced at the surfaces of nanotubes. The 248 nm light near the resonant frequency of one of these plasmon pairs for small diameter nanotubes causes a large electric field enhancement in the vicinity of the tubes. The enhanced field increases the rate at which sp^2 bonds in the amorphous carbon are excited into a state from which the carbon is more easily oxidized. Classical electromagnetics, in conjunction with density functional theory, is used to quantify the field enhancement and the relationship between laser wavelength and nanotube radius which will result in cleaning.

■ *Measurement of photoconductive lifetimes of nanomaterial by non-contact methods.* Cheaper, better (non contact), and faster techniques are urgently needed to address properties of bulk nanomaterials. Accurate measurements of electrical properties and identification of transport phenomena are critical for engineering improvements and the efficient development of organic photoconductive materials. Measuring, understanding, and controlling the recombination lifetimes of nanotube and polymer composite films are essential for the progress of bulk nanotube electronics. We have implemented the method of resonantly coupled photoconductive decay (RCPCD) to measure the photoconductive behavior of bulk carbon nanotubes and carbon nanotube composites. The measurements provide a method, means, and information relevant to intrinsic and extrinsic bulk properties - independent of electrical contacts. Our objective is to use this metrology to understand and document the influence of nanotube morphology and charge transfer to maximize the photoconductive lifetime.

Initially presented at the America Frontiers of Engineering in Kobe, Japan (sponsored by the National Academy of Engineering), more recent results were shown at the 2009 spring MRS conference. We have begun assembling a second-generation RCPCD with collaborators at the Colorado School of Mines. (RCPCD is described as the impedance coupling between an antenna driven at frequencies between 400 and 1000 MHz and the photoconductive material, which is in the proximity of the antenna. The antenna is a component of a very high-Q resonant system, and the sample becomes coupled to the antenna system. The sample is mounted on a moveable platform such that the system resonant frequency may be changed by varying the sample coupling.)

■ *Optical properties of organic photovoltaics based on carbon nanostructures.* Improving the quantum efficiency of organic photovoltaics is a requirement for large-scale commercial use. It has been established that doping of conjugated-polymer films with single-walled carbon nanotubes (SWCNTs) facilitates exciton dissociation and electron transport. Accurate measurement of important extrinsic device properties such as absorbance with respect to film thickness and SWCNT concentration is necessary for informing our expectations for intrinsic photovoltaic efficiency. This is also the basis for modeling the role of the photoactive layer and maximizing the efficiency of the device. In this work, we explicitly measured the absolute absorbance of photoactive films by depositing them on a pyroelectric detec-

tor and modeled the optical function of the doped films based on Kramers-Kronig analysis. Raman spectroscopy, UV-VIS absorption, and four-point probe measurements provide further characterization of nanotube concentration and homogeneity of our films. Our study provides direct quantitative measurements traceable to NIST standards, which demonstrates that variations in the intrinsic efficiency of the photoactive layer directly correlate to the extrinsic efficiency of the SWCNT-polymer photovoltaics.

■ *NIST Team Proves Bridge from Conventional to Molecular Electronics Possible:* Molecular electronic devices were fabricated by using silicon of the same crystalline orientation as that used in standard microelectronics (CMOS) technology, Si (100). This breakthrough demonstrated that a single layer of organic molecules can be assembled on the same sort of substrate used in conventional microchips. The ability to use a silicon crystal substrate that is compatible with the industry-standard CMOS (complementary metal oxide semiconductor) manufacturing technology paves the way for hybrid CMOS-molecular device circuitry ─ necessary precursor to a "beyond CMOS" totally molecular technology ─ to be fabricated in the near future. Because the probable first step in the realization of molecular electronic devices will involve their integration with existing CMOS technology, it is imperative that molecular devices be fabricated using CMOS compatible materials, such as 100-oriented silicon. It was demonstrated that organic monolayers can be assembled on Si (100) that are comparable in quality, aliphatic monolayer coverage, and extent of substrate oxidation to those assembled on the more extensively studied, but CMOS-incompatible, Si (111) crystal face. Monolayers assembled on the CMOS-compatible Si (100) were characterized via spectroscopic monolayer characterization, as well as through the fabrication of Si (100)-based molecular electronic devices that exhibited molecule-dependent electrical characteristics.

■ *Laser-induced purification of single wall carbon nanotubes (SWCNTs).* We have further investigated the purification of as-prepared single-walled carbon nanotubes (SWCNTs) by exposure to ultra-violet (UV) light of various wavelengths in different atmospheres. Our initial work demonstrated that the excitation of the collective electron oscillations of the p-plasmon in the nanotubes by the 248 nm photons results in non-thermal removal of carbon impurities. Our recent results from 193 nm pulsed laser light and 254 nm continuous wave (CW) light supports the importance of resonance of photon energy with the π plasmon of sp^2 bonded carbon atoms, as well as demonstrates the importance of atmosphere, and the pulsed nature of the light. Analysis of Raman spectroscopy data has shown that the carbon impurities are more efficiently removed by the pulsed light for the same number of photons than by the CW light for roughly the same wavelength. We continue to investigate the photothermal, photophysical, and photochemical influences for the mechanism of purification of SWCNTs. We have considered differences in the thermal transport, including thermal conductivity, specific heat, and thermal diffusivity of carbon nanotubes compared with the thermal transport properties of impurity carbons. We have found that upon pulsed heating the nanotubes experience a smaller temperature increase than do other carbon impurities, and this difference enables the selective oxidation of the carbon impurities. The importance of the resonance of the p-plasmon of sp^2 carbon with the incident photons has also been a large focus of our work. The production of hot electrons and the simultaneous decrease in electron density as electrons are excited into an antibonding state of the carbon sp^2 bond is also considered. We continue to work closely with our theoretical collaborators at the Colorado School of Mines in order to provide a theoretical understanding to our experimental findings.

■ *Rapid and inexpensive identification of bulk carbon nanotubes.* The photoconductive recombination lifetimes of CNT thin films as a function of wavelength were measured by resonant-coupled photoconductive decay (RCPCD) method. The carrier recombination lifetime is a fundamental property of carbon nanotubes which is typically determined by contact-based techniques or spectroscopic methods. The RCPCD measurement is based on a pump-probe technique in which an optical pump and a low frequency microwave probe are employed and is well suited to characterization of bulk and extrinsic material properties. Our results demonstrate the role of purification and the effect of the interaction of nanotubes and polymers in thin films of multi-walled carbon nanotube and single-walled carbon nanotubes. Possible mechanisms describing the interaction of photoexcited carriers in the nanotube

polymer composites are currently under investigation. We have reported the wavelength dependence of photoconductive lifetimes at meetings of the American Vacuum Society and the Materials Research Society. Raman spectroscopy and UV-VIS absorption measurements provide further identification and characterization of nanotube samples to enable correlation of nanotube properties with the efficiency of charge transport.

A dielectric resonator-based measurement method for determining the electrical conductivity of carbon nanotubes at microwave to millimeter frequencies has been demonstrated. This measurement method is not limited by the metal conductor contact resistances or impedance mismatch commonly encountered in the measurement of single nanotubes. The measurement of carbon nanotubes yielded conductivities of approximately 0.08 × 107 S/m.

■ *Placement of Nanowires with Inkjet-based Dispersal.* We have placed GaN nanowires onto conventional silicon circuitry using liquid drop dispersal (see Figure 6). The nanowires were grown with catalyst-free molecular beam epitaxy, which produces defect-free material with well-defined conductivity. The nanowires are photoconductive due to changes in the surface depletion region when illuminated with light above the GaN band gap of 3.4 eV. The silicon transistor shown in the figure has been used as a transimpedance amplifier to read out this signal. This proof-of-principle experiment, along with others using picoliter drop dispensers, show that nanowires can tolerate these highly manufacturable placement procedures and that integration with Si transistors will succeed. We have also demonstrated low-threshold, high on/off current ratio FETs fabricated from single GaN nanowires.

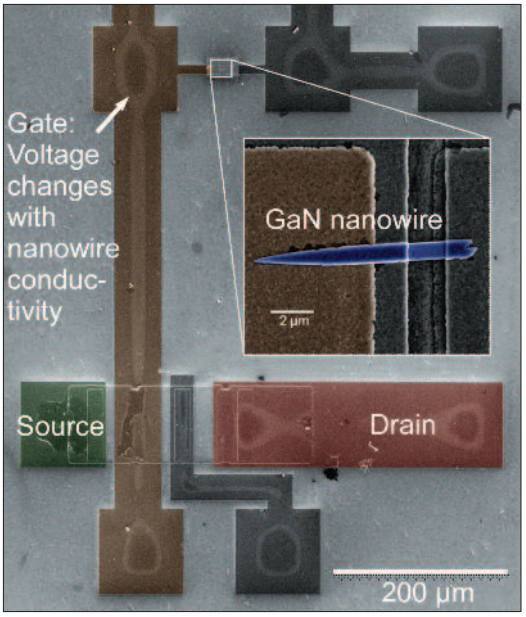

Figure 6. GaN nanowire integrated into silicon transistor circuit.

Collaborations

Colorado School of Mines, Prof. Mark Lusk, Ab initio studies of pi plasmon role in bundling, functionalization and optical properties of carbon nanotubes.

Colorado School of Mines, Richard Ahrenkiel, Resonantly coupled photoconductive decay lifetime measurements of CNTs and CNT-polymer composites.

Columbia, Prof. Philip Kim, Graphene-based resistance standards.

George Mason University, Prof. Qiliang Li, Novel nanowire devices and test structures.

Gwangju Institute of Science and Technology, Korea, Prof. Takhee Lee, Scattering processes in ZnO nanowire.

Hewlett-Packard, R. Stanley Williams et al., Characterization of advanced crossbar technologies.

National Renewable Energy Laboratory, A. C. Dillon, Optical properties of CNT materials.

NIST Division 838, Dr. James Kushmerick, Molecular charge transport.

NIST, Division 852, Dr. Robert Cook. CR-AFM mechanical characterization of Si and Si/SiO2 NW structures

NIST, Division 620. Dr. Nikolay Zhitenev. Characterization of Si NW based photovoltaic platforms

Notre Dame, Alan Seabaugh, Graphene-based transistors.

Princeton University, Prof. Antoine Kahn, Validating the unoccupied valence electronic structure of molecules on metals.

Purdue University, Prof. David Janes, Hybrid Si-molecular devices and test structures.

Rice University, Prof. James Tour, Valence level alignment and identification of the charge carriers of molecules on metal surfaces.

University of California, Riverside, Dr. Nosang Myng. Surface modification of SiNWs by galvanic displacement

University of Colorado, Prof. Charles Rogers and Prof. Victor Bright, mechanical properties of nanowires and RF electronics.

University of Maryland, Prof. Ellen Williams, Contacts to enable molecular electronics.

University of Minnesota, Prof. William Gerberich. In-situ TEM mechanical testing of Si NWs

University of Notre Dame, Prof. Greg Snider, Si single-electron device fabrication.

University of Texas, Prof. Eric Vogel, Si nanowire and graphene-based field effect transistors.

Virginia Polytechnic Institute and State University, R. L. Mahajan, Laser treatments of CNT materials.

Publications

G. Stan, S. Krylyuk, A. Davydov, R. Cook, *"Compressive stress effect on the radial elastic modulus of oxidized Si nanowires",* Nano Letters 10 2031-2037 (2010) [JUN 2010].

M. Coll, C. A. Richter, and C. A. Hacker, *"Thermal stability of confined flip-chip laminated omega-functionalized monolayers,"* Journal of Vacuum Science & Technology B, vol. 27, pp. 2826-31, Nov 2009 [NOV 2009].

Q. L. Li, X. X. Zhu, Y. Yang, D. E. Ioannou, H. D. Xiong, D. W. Kwon, J. S. Suehle, and C. A. Richter, *"The large-scale integration of high-performance silicon nanowire field effect transistors,"* Nanotechnology, 20 Oct 2009, 415202 (5pp) [OCT 14, 2009].

Curt A. Richter, JJ Kopanski, Chong Jiang, Yicheng Wang, MY Afridi, Xiaoxiao Zhu, DE Ioannou, and Qiliang Li, *"Advanced Capacitance Metrology for Nanoelectronic Device Characterization,"* Frontiers of Characterization and Metrology for Nanoelectronics: 2009 Book Series: AIP CONFERENCE PROCEEDINGS Volume: 978 Pages: 328-332 Published: 2009. [OCT 2009].

M. Coll, L.H. Miller, L.J. Richter, D.R. Hines, O.D. Jurchescu, N. Gergel-Hackett, C.A. Richter and C.A. Hacker, *"Formation of Silicon-Based Molecular Electronic Structures using flip-chip Lamination"* Journal of the American Chemical Society, vol. 131, pp. 12451-12457, Sep 2009.

Xiaoxiao Zhu, D. Gu, Qiliang Li, D. E. Ioannoua, H. Baumgart, J. S. Suehle, C. A. Richter, *"Silicon Nanowire NVM with High-k Gate Dielectric Stack,"* Microelectronic Engineering 86 1957-1960 (2009) [JUL 2009].

N. Gergel-Hackett, B. Hamadani, B. Dunlap, J. Suehle, C. Richter, C. Hacker, D. Gundlach. *"A flexible solution-processed memristor,"* IEEE Electron Device Letters, Vol. 30, No. 7. Posted online the week of June 8, 2009. [JUL 2009].

J.Kopanski, M. Yaqub Afridi, Chong Jiang, and Curt A. Richter, *"Test Chip to Evaluate Measurement Methods for Small Capacitances,"* Proceedings of the 2009 International Conference on Microelectronic Test Structures, pp. 39-42 (2009) [MAR 2009].

S. Krylyuk, A. Davydov, I. Levin, A. Motayed, M. D. Vaudin, *"Rapid Thermal Oxidation of Silicon Nanowires,"* Applied Physics Letters 94 (6), 063113 (2009) [FEB 2009].

M. Coll; Hacker, CA; Miller, LH; Hines, DR; Williams, ED; Richter, C.A. *"Ultrasmooth gold as a top metal electrode for molecular electronic devices,"* ECS Transactions, 16 (25) 139-146 (2009) [FEB 2009].

Wenyong Wang and Curt A. Richter *"Magnetic Tunnel Junctions with Self-Assembled Molecules,"* J. Nanosci. Nanotechnol. 9(4), 1008-1010 (2009) [FEB 2009].

H. D. Xiong, W. Wang, J. S. Suehle, C. A. Richter, W. Hong, and T. Lee, *"Noise in ZnO Nanowire Field Effect Transistors,"* J. Nanosci. Nanotechnol. 9(4), 1041-1044 (2009) [FEB 2009].

X. Zhu, Y. Yang, Q. Li, D. E. Ioannou, J. S. Suehle, C. A. Richter, *"Silicon Nanowire NVM Cell Using High-k Dielectric Charge Storage Layer,"* Microelectronic Engineering 85 2403-2405 (2008) [DEC 2008].

Curt A. Richter, Hao D. Xiong, Xiaoxiao Zhu, Wenyong Wang, Vincent M. Stanford, Woong-Ki Hong, Takhee Lee, D.E. Ioannou and Qiliang Li, *"Metrology for the Electrical Characterization of Semiconductor Nanowires,"* IEEE Trans on Electron Devices 55 (11), 3086-3095 (2008) [NOV 2008].

Lam H Yu, Nadine Gergel-Hackett, Christopher D. Zangmeister, Christina A. Hacker, Curt A Richter, James G Kushmerick, Molecule-induced interface states dominate charge transport in Si-alkyl-metal junctions, Journal of Physics: Condensed Matter, 20, 374114 (2008) [SEP 17 2008].

Chang-Yong Choi, Won-Ju Cho, Sang-Mo Koo, John S. Suehle, Curt A. Richter, Qiliang Li, Eric M. Vogel, *"Three-dimensional simulation study of the improved on/off current ratio in silicon nanowire field-effect transistors,"* Journal of the Korean Physical Society [SEPT 2008].

C. Risko, C.D. Zangmeister, Y. Yao, T.J. Marks, J.M. Tour, M.A. Ratner, R.D. van Zee, *"Experimental and theoretical identification of valence energy levels and interface dipole trends for a family of (oligo)phenylene-ethynylenethiols adsorbed on gold,"* J. Phys. Chem. C. 112, (34) 13215 (28-Aug-2008) [AUG 2008].

Scott, A.; Hacker, C.A.; Janes, D.B.; *"In-situ structural characterization of metal-molecule-silicon junctions using backside infrared spectroscopy,"* J. Phys. Chem. C, 2008, 112(36), 14021-14026(jp-2008-01715s).

N. Gergel-Hackett, C.D. Zangmeister, C. A. Hacker, L. J. Richter, Curt A. Richter, *"Demonstration of Molecular Assembly on Si (100) for CMOS-Compatible Molecule-Based Electronic Devices,"* J. Am. Chem. Soc.; (Communication); 2008; 130(13); 4259-4261 (APR 2008).

C. A. Richter, H. D. X.iong, X. Zhu, W. Wang, V. M. Stanford, Q. Li, D.E. Ioannou, W.-K. Hong, T. Lee *"Measurements for the Reliability and Electrical Characterization of Semiconductor Nanowires,"* Proceedings of the IEEE International Reliability Physics Symposium 2008, 39-45 (APR 2008).

E. Hourdakis, J. A. Wahl, and N. M. Zimmerman, *"Lack of charge offset drift is a robust property of Si single electron transistors,"* Appl. Phys. Lett. 92, 062102 (FEB 2008).

W. Wang, A. Scott, N. Gergel-Hackett, C. A. Hacker, D. B. Janes, and C. A. Richter, *"Probing Molecules in Integrated Silicon-Molecule-Metal Junctions by Inelastic Tunneling Spectroscopy,"* Nano Letters 8 (2), 478-484, 2008 (FEB 2008).

K. Ramadurai, C. L. Cromer, L. A Lewis, *"High-performance carbon nanotube coatings for high-power laser radiometry,"* J. Appl. Phys. 103, 013103 (3-JAN-2008).

Power Semiconductor Device Metrology

Technical Contacts:
A. Hefner

"In 2002, Dr. Calvin Carter of Cree Inc. received the US National Medal of Technology from President George W. Bush for: "his exceptional contributions to the development of Silicon Carbide wafers, leading to new industries in wide band-gap semiconductors and enabling other new industries in … more efficient/compact power supplies, and higher efficiency power distribution/transmissio n systems."

Goals

The goal of the project is to develop electrical and thermal measurement techniques, measurement equipment, and theoretical models in support of the development and application of advanced power semiconductor devices.

Customer Needs

There are significant technical requirements for more efficient, higher voltage power semiconductor devices. The application needs range from more efficient power supplies for computers and consumer appliances, to electric automobile power converters, to more efficient power generation, transmission and distribution, including many emerging Smart Grid applications. As the North American power grid rapidly transitions to a significant fraction of the power delivered to the grid through power electronics inverters rather than rotation machines (from < 0.2 % to >10% over the next decade) power electronics technologies will play an increasingly critical role. Rapid technical advances are °ccurring in the development of new power semiconductor materials, fabrication processes, and device designs to address these needs. With the introduction of these new materials and designs come new requirements for characterizing the performance and reliability of the fabricated devices. The most exciting, and potentially revolutionary, development in this area is the rapid progress in the development of wide band-gap semiconductor materials for power semiconductor devices. Wide band-gap semiconductors such as silicon-carbide (SiC) have long been envisioned as the material of choice for next-generation power devices. Recent advances in single crystal SiC material and fabrication technology have ushered in a new era of wide band-gap power semiconductor devices. This has led to the commercialization of SiC power Schottky diode products in the 400 V to 1200 V range and to the development of High-Voltage, High-Frequency (HV-HF) power devices with 10 kV, 20 kHz power switching capability. The emergence of HV-HF devices with such capability is expected to revolutionize industry and military power generation, transmission, and distribution by extending the use of switch-mode power conversion technology, with its superior efficiency and control capability, to high voltage applications. Several industry and government programs are currently under way to accelerate the development and application insertion of SiC power semiconductor devices. The goal of the DARPA Wide-Band-gap Semiconductor Technology High Power Electronics Program (WBST-HPE) is to develop half-bridge power semiconductor modules with 15 kV, 110 A, 20 kHz switching capability. The recently awarded WBST-HPE Phase 3 effort (http://www.darpa.mil/baa/baa06-30.html) anticipates that this semiconductor technology will enable the HV-HF switching required for a Solid State Power Substation (SSPS). The Electric Power Research Institute (EPRI) also identified the benefits of HV-HF semiconductor technology, which include advanced distribution automation using solid-state distribution transformers with significant new functional capabilities and power quality enhancements, and the Department of Energy has identified HV-HF power devices as an enabling technology for alternative energy sources and energy storage systems, as well as transmission and distribution systems.

Technical Strategy

The strategy of the NIST project is to support the measurement infrastructure of the power semiconductor and energy systems technology industries by developing and evaluating measurement methods and techniques where suitable ones do not exist for characterizing critical electrical and thermal properties of power semiconductor devices. This includes electrical, thermal, and safe operating limit characterization, establishing performance metrics, and developing methods for extracting device model parameters. The NIST project also establishes the theoretical foundation required for development of advanced power semiconductor devices, and develops circuit simulation models for emerging power semiconductor devices to aid in the rapid adoption and effective utilization of new technologies. NIST is taking a lead role in developing the device metrology and performance metrics

necessary for industry and government HV-HF semiconductor device development efforts and in the evaluation of potential future impacts power semiconductor technologies requiring future investment.

Metrology High-Voltage High-Frequency Switching Devices

The emergence of HV-HF power devices presents unique challenges in metrology and specification of device electrical and thermal requirements. NIST has recently developed unique world-class laboratory facilities for characterization of HV-HF SiC power switching devices including: a) 25 kV variable-pulse-width curve tracer, b) 15 kV 100 A 50 ns inductive and resistive load switching tester, c) 4 kV, 50 A, 10 ns diode reverse recovery tester, d) pulsed and multi-channel long term diode forward current stress and monitoring systems, e) high-speed high-power Temperature Sensitive Parameter module package measurement system, and f) rapid thermal cycling/sh°ck module package stress system.

Support Programs to Develop HV-HF Semiconductor Devices and Applications

A major driving force spearheading the development of HV-HF power devices is the ongoing DARPA WBST-HPE program f°cused on developing the technology deemed necessary to enable SSPS for future Navy warships. Conventional distribution approaches being considered for the next generation of aircraft carriers employ a 13.8 kV a.c. power distribution that is stepped down to 465 V a.c. by using large (6 ton and 10 m3) 2.7 MW transformers. Substantial benefits in power quality enhancement, advanced functionality, size, and weight are anticipated by replacing this transformer with an all solid state design. NIST played a key role in WBST-HPE Phase 1 and has been selected to be the exclusive device and package evaluation and metrology lab for the Phase 2 and 3 programs for 2005 through 20010. A new NIST/DOE program was recently established with the DOE Solid State Energy Conversion Aliance (SECA) to analyze advanced power electronic component technologies needed for 300 MW Power Conversion Systems (PCS) to enable future Near Zero Emission Fuel Cell Based Power Plants Fueled with Coal-Derived Gas. The extremely large PCS is required to convert the 700 V, 1000 A DC power output of one thousand fuel cell modules to the 345 kV AC power transmission level.

DELIVERABLES:

- Participate in coordinating the effective utilization of DARPA HPE Phase 2 devices in the SSPS power converter developed by the HPE Phase 3 contractor team. 3Q 2010
- Perform analysis to identify advanced high-megawatt PCS technologies requiring investment to meet the goals of the DOE Solid State Energy Conversion Alliance (SECA) and FutureGen programs for near-zero emission central station fuel cell power plants. 4Q 20010
- Provide leadership to the Interagency Advanced Power Group, Electrical Systems Working Group and in establishing an industry roadmap for High Megawatt Power Converters. 3Q 20010

Perform Measurements on Selected HV-HF Samples

NIST continues to serve as the exclusive device deliverable evaluation lab for the DARPA WBST HPE Phase 3 program providing data and analysis critically important to evaluate contractors and plan future programs. NIST evaluates device performance and provides feedback to contractor and DARPA program manager as well as the potential component users in government and industry. The NIST characterization data and analysis has continually identified critical technology advancements required to meet DARPA program goals such as recommendations to improve surface passivation, reducing internal gate resistance, improving p-i-n power diode (diode made with p-type to intrinsic to n-type semiconductor junctions) speed, transitioning program goal from p-i-n to Schottky diodes, and specific design parameter targets for MOSFET and IGBT (insulated gate bipolar transistor) designs. The NIST HV-HF characterization results are routinely used in by DARPA in planning documents and by the device developers in publications. NIST is also performing measurements on the prototype devices that were previously determined by NIST to provide enhanced performance in High Megawatt converters for renewable/clean generators (FY06-07 NIST/SECA HMW FC Plant Power Conditioning System Technology Impact Study) and developing models based on these measured results to perform simulations validating the previous NIST performance predictions.

DELIVERABLES:

- Developed unique test equipment and focused performance evaluations critically important to understanding degradation and failure mechanisms and identifying die screening methods for the DARPA HPE Phase III program. 1Q 2010
- Performed initial screening tests to determine the impact of dV/dt on dynamic blocking failures for DARPA Phase III 100 A, 10 kV SiC MOSFET/JBS power module deliverables. 1Q 2010

Advanced Power Device Models for Advanced Plug-in Vehicle Converters and Inverters

Accurate and robust device models for circuit and system simulations are needed to evaluate the impact of the new semiconductor technology on advanced plug-in vehicle converters and inverters performance. NIST develops the generic physics-based models for the SiC and Si power semiconductor devices that are provided in commercial circuit and system simulation software. In addition, NIST also develops model parameter extraction methods and softwares needed to perform model parameter extraction for specific devices. The NIST model parameter extraction tools have recently been used to characterize Si CoolMOS™ and diodes. These models were used as a virtual prototype in support of electro-thermal-mechanical simulation and reliability for advanced plug-in vehicle converters and inverters.

DELIVERABLES:

- Performed forward conduction characteristics, performed parameter extraction, and validated the 200 A, 600 V Si PiN diodes for the FreedomCAR project. 1Q2010
- Performed output characteristics, capacitor-voltage measurement, performed parameter extraction, and validated the 60 A, 650 V Si CoolMOS™ transistor for the FreedomCAR project. 2Q2010

Metrology for SiC Device Degradation and Reliability

A critical step in characterizing and modeling the degradation in power electronic modules as a result of temperature cycling has been the development of an accelerated testing profile that can be used on a generic test sample for model calibration and validation. This profile damages package interfaces by passive temperature cycling at various ramp rates over a temperature range from 25 °C to 200 °C. This profile uses the Temperature Sensitive Parameter (TSP) system to evaluate package damage effects by determining the change in the transient junction temperature of Si and SiC MOSFETs and IGBTs. The test continuously measures the gate-source voltage throughout a power pulse, and then converts this to a temperature waveform based upon results of a calibration procedures. These measurements of the increase in the transient junction temperature of Si and SiC MOSFETs and IGBTs with thermal cycling damage are coupled to electrothermal modeling of the package stack. The thermal conductivities of the layers of the package stack are varied in the electrothermal model until the measured transient junction temperature behavior is matched. This permits the identification of the interfaces that are damaged due to the controlled thermal cycling along with the development of a quantified model representing the extent of the damage.

DELIVERABLES:

- Develop an accelerated testing protocol for assessing package power cyceling damage in power modules. Develop electro-thermal-mechanical degradation modeling principles. Enhance the high-speed temperature sensitive parameter method and test apparatus to serve as a method for monitoring degradation of package thermal interfaces. 4Q2010

Accomplishments

■ NIST played a key role in planning and coordinating activities of the DARPA HPE program on high voltage SiC power devices including: Evaluated contractor performance for DARPA WBST HPE Phase 2. Participated in planning and writing Broad Area Announcement (BAA) for DARPA WBST HPE Phase-3 programs and presented status of SiC power devices at the Phase 3 Industry Bidder Briefing day. Served as Member of DARPA/ONR Solid State Power Substation (SSPS) Government Independent Design Panel. Participated in planning ONR Mantech SiC Power Device manufacturability program.

■ NIST leading industry and other Federal Agencies in coordinating activities in High Megawatt Power Conversion Systems. Planned and held the first High Megawatt Converter workshop at NIST with participants from major government and industry programs requiring advanced power converter technologies for high megawatt power conversion systems. Hefner (NIST) serves as the Chairman of the Interagency Task Force for High Megawatt Power Conversion systems. Also, he previously served as panel member for DOE Program on SiC-based Inverters in Near Zero Emission Fuel Cell Based Power Plants Fueled with Coal-Derived Gas. NIST played a key role in reinitiating the of Interagency Advanced Power Group (IAPG) Electrical Systems Working Group (ESWG) to coordinate federal programs in high-megawatt PCS technology (meeting held at NIST on April 21-25, 2008). NIST also held a High-Megawatt Power Converter Technology R&D Roadmap Workshop on April 8, 2008, to provide guidance in developing

the PCS technology for grid connectivity of Alternate/Clean Energy sources and associated grid converters for distributed generation.

■ High voltage clamped inductive and resistive switching test bed developed. A low parasitic inductance 15 kV switching test system for clamped inductive and resistive SiC MOSFET switching characterization was developed and integrated into the 25 kV safety-interlocked curve-tracer system. A low parasitic capacitance temperature-controlled test fixture with 20 kV voltage isolation and 350 °C maximum controllable temperature was also included to enable investigation of HV-HF device characteristics at elevated operating temperature. The hardware is controlled by the NIST virtual curve-tracer instrumentation software.

■ NIST unique HV-HF device metrology demonstrated unprecedented performance of DARPA WBST-HPE: The NIST high voltage curve tracer and the NIST high-voltage high-frequency (HVHF) switching test systems were used to demonstrate the unprecedented performance of DARPA WBST-HPE MOSFETs, e.g., 10 kV, 12 A, 50 ns inductive load switching shown in Fig. 1. Typical high voltage silicon devices require several microseconds to switch at 6.5 kV maximum. Significant advances in materials, device design and HV-HF metrology were required for this achievement.

■ NIST contributed to device design required to improve 10 kV SiC rectifier reverse recovery speed: NIST provided guidance on techniques for improving the reverse recovery time (switching speed) of 10 kV SiC rectifiers developed by the

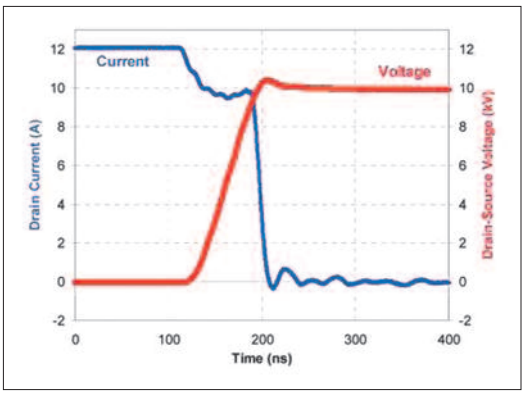

Figure 1. NIST measurement of the unprecedented performance of the SiC power MOSFETs switching at 10 kV, 12 A and 200 °C in less than 75 ns.

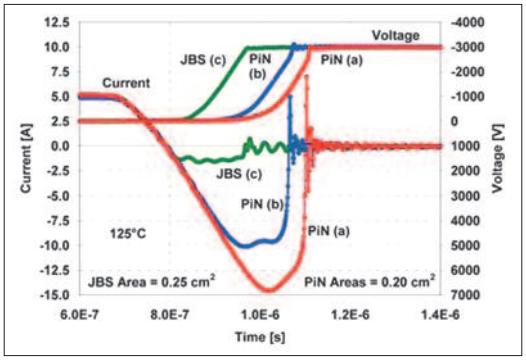

Figure 2. Comparison of reverse recovery time for two different 10 kV SiC PiN diodes, (a) and (b), and a 10 kV JBS SiC diode (c), all at 125 °C.

HPE program. The guidance included structure changes to control the plasma distribution during reverse recovery in PiN diodes as well as the recommendation that the program be refocused toward Junction Barrier Schottky (JBS) diodes. NIST characterized the reverse recovery performance of the various diode designs that were produced using the NIST 4 kV, 50 A, 10 ns diode reverse recovery tester. Results indicate that the reverse recovery charge (area under the negative portion of the current waveform shown in Fig. 2 is reduced using plasma engineering but only the JBS diode is capable of 20 kHz operation.

■ NIST HV-HF SiC models were used to simulate system performance: NIST's metrology, device modeling, and parameter extraction tools have resulted in software models for the HV-HF devices that are being produced by the DARPA WBST HPE program. These models are being used by industry and government to simulate

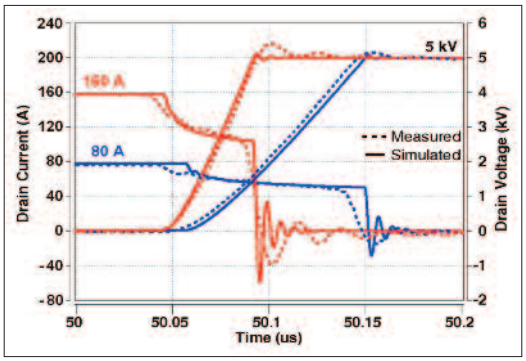

Figure 3. Comparison of scaled measured (dashed) and simulated (solid) inductive-load switching turn-off waveforms for a 100 A, 10 kV SiC MOSFET. Both tests were performed at 25 °C with a clamp voltage of 5 kV and drain currents of 80 A (blue) and 160 A (red), respectively.

the performance of future power distribution and conversion systems enabled by the new HV-HF semiconductor device technology. Fig. 3, Fig. 4, and Fig. 5 show the comparison of the model with measured results. These models were used to optimize the 100 A, 10 kV half bridge power module and to design the SSPS HPE Phase 3 and are being used to simulate various PCS architectures to help identify technologies that need to be developed to reduce the cost of future PCS systems for alternate/clean energy systems.

■ Measured forward conduction characteristics, performed parameter extraction, and performed model validation for a 200 A, 600 V Si PiN diodes for the FreedomCAR project. Fig. 6 demonstrated the comparison of measured (dashed) simulated (solid) forward conduction characteristics at 25 °C, 50 °C, 75 °C, 100 °C, 125 °C, and 150 °C for a 600 V, 200 A Si PiN diode.

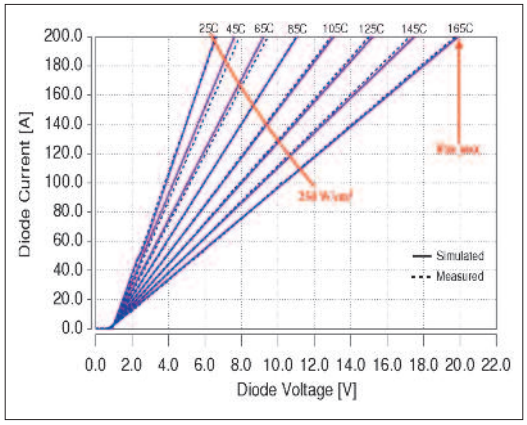

Figure 4. Comparison of scaled measured (dashed) and simulated (solid) forward conduction characteristics at 25 °C, 45 °C, 65 °C, 85 °C, 105 °C, 125 °C, 145°C, and 165 °C for a 100 A, 10 kV SiC junction barrier Schottky (JBS) diode.

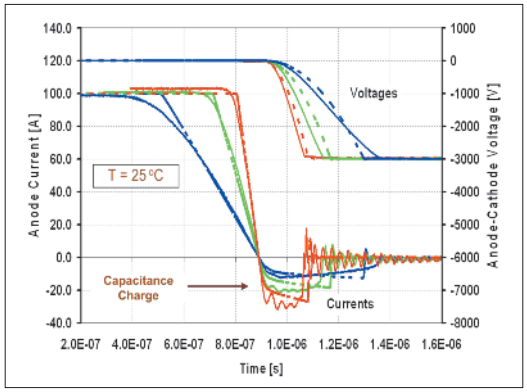

Figure 5. Comparison of scaled measured (solid) and simulated (dashed) reverse recovery at 25 °C for a 100 A, 10 kV SiC JBS diode.

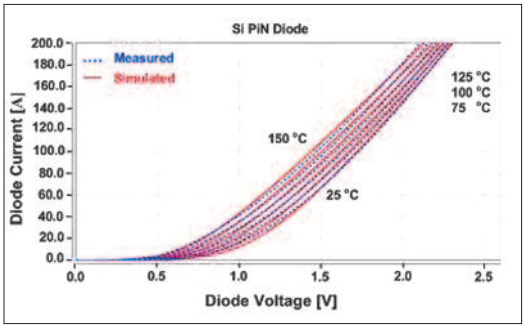

Figure 6. Comparison of measured (dashed) simulated (solid) forward conduction characteristics at 25 °C, 50 °C, 75 °C, 100 °C, 125 °C, and 150 °C for a 600 V, 200 A Si PiN diode.

■ Measured output characteristics, performed parameter extraction, and performed model validation a 650 V, 60 A Si CoolMOSTM for the FreedomCAR project. Fig. 7 and 8 demonstrated the comparison of measured (dashed) simulated (solid) output characteristics at 25 °C and 150 °C, respectively for a 60 A, 650 V Si CoolMOSTM transistor.

■ Performed capacitance-voltage and inductive switching measurements for a 650 V, 60 A Si

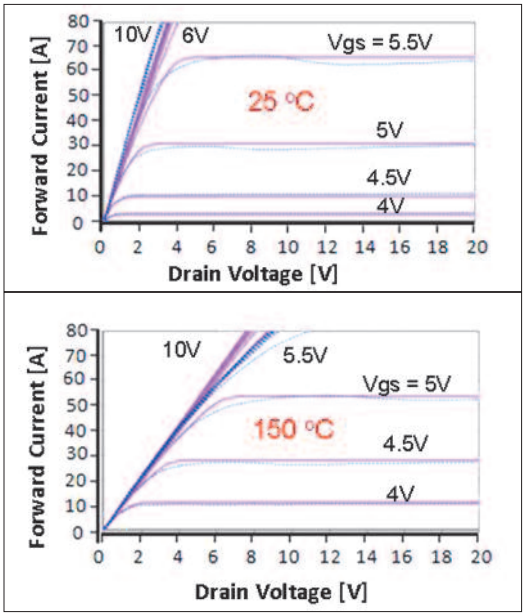

Figure 7 and 8. Comparison of measured (dashed) simulated (solid) output characteristics at 25 °C and 150 °C, respectively for a 60 A, 650 V Si CoolMOSTM transistor.

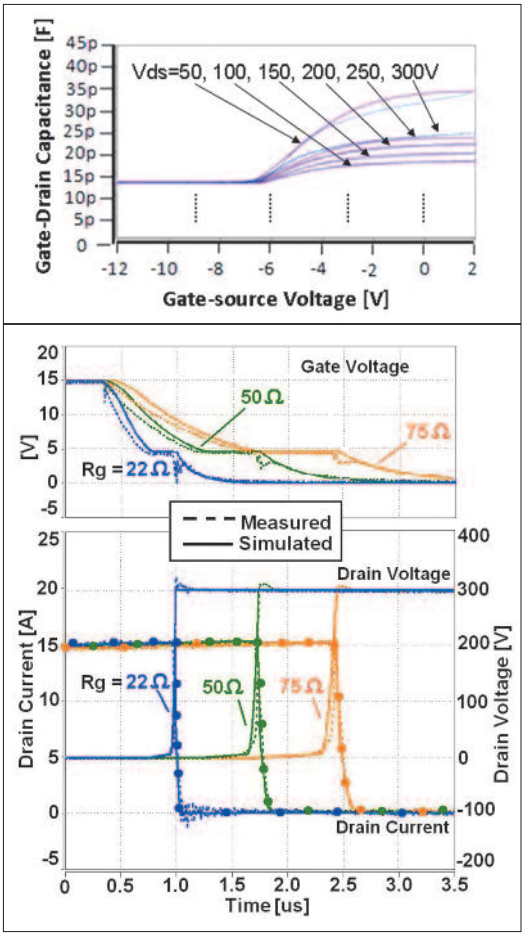

Figure 9 and 10. The gate-drain capacitance versus gate-source voltage and the inductive switching behaviors for various gate resistors, respectively for a 650 V, 60 A Si CoolMOSTM.

CoolMOSTM for the FreedomCAR project. Figs 9 and 10 demonstrated the gate-drain capacitance versus gate-source voltage and the inductive switching behaviors for various gate resistors, respectivly for a 650 V, 60 A Si CoolMOSTM.

■ Developed unique test equipment and focused performance evaluations critically important to understanding degradation and failure mechanisms and identifying die screening methods for the DARPA HPE Phase III program. Performed soak and relax experiments on die identified as weak by the package integrator for the HPE program to determine the cause of the defect.

■ Performed initial screening tests to determine the impact of dV/dt on dynamic blocking failures for DARPA Phase III 100 A, 10 kV SiC MOSFET/JBS power module deliverables.

■ Developed physics-based, transient, electro-thermal simulation capability for high-voltage, high-current SiC bipolar power devices. A Physics-based TCAD simulations capability has been developed by NIST for high-voltage, high-current SiC power semiconductor devices. This capability has been applied to the electro-thermal study of SiC power thyristors operating under high-current, pulsed-power conditions.

Collaborations

UMD/CALCE – Reliability modeling

VA Tech – Soft switching module

Delphi – High current density module

NREL – Cooling technology

Azure Dynamics – System Integration

Synopsys Inc., SiC power device modeling and parameter extraction for IGBT library component models.

CREE, Characterization and application of SiC power devices.

Northrop Grumman Corp., Characterization and application of SiC power devices.

Virginia Tech., Silicon and SiC power device utilization.

Powerex, Power semiconductor device packaging.

DARPA/ONR/Navsea, SiC power devices for SSPS and other applications.

GE CRD, SiC power devices for robust integrated power electronic systems.

University of Puerto Rico Mayagüez, Electro-thermal simulation of power electronic systems.

University of Wisconsin Madison, SiC power system simulation.

Purdue University/Carnegie Mellon University/Vanderbilt University/Auburn University, Development of process technologies for SiC power devices Electric Power Research Institute, power semiconductor devices for solid state intelligent universal transformer.

Department of Energy, electric vehicle power electronics and power converters for 300 MW fuel cell generation plant.

Stanford University, numerical simulation of SiC power semiconductor devices.

Army Research lab, Pulsed power semiconductor devices.

Publications

Nanying Yang, Tam Duong, Jeong-O Jeong, Jose M. Ortiz, Allen Hefner, Kathleen Meehan, *"Automated Parameter Extraction Software for Silicon and High-Voltage Silicon Carbide Power Diodes,"* has been accepted to submit in the Proceedings of the 2010 IEEE Workshop on Control and Modeling for Power Electronics (COMPEL), June 27-30, 2010, Boulder, Colorado.

Nanying Yang, Jose M. Ortiz, Tam Duong, Allen Hefner, Kathleen Meehan, *"Modeling the Inter-Electrode Capacitances of Si CoolMOSTM Transistors for Circuit Simulation of High Efficiency Power Systems,"* has been accepted in the Proceedings of the 2010 IEEE Energy Conversion Congress and Exposition (ECCE), September 12-16, 2010, Atlanta, Georgia.

M. Hernández-Mora, B. Grummel, J. M. Ortiz-Rodríguez, A. R. Hefner, Jr., D. Berning, P. McCluskey, *"Computer-Controlled Thermal Cycling Tool to Aid in SiC Module Package Characterization,"* to be submitted in the Proceedings of the IEEE COMPEL Workshop 2010, IEEE COMPEL 2010, Boulder, CO, United States, 06/28/2010 to 06/30/2010

Parrish Ralston, Tam Duong, Nanying Yang, David Berning, Colleen Hood, Allen Hefner and Kathleen Meehan, *"A New Power Diode Model Parameter Extraction Software Package,"* in the Proceedings of the 2009 IEEE Energy Conversion Congress and Exposition (ECCE), September 20-24, 2009, San Jose, California.

D. W. Berning, T. H. Duong, J. M. Ortiz-Rodríguez, A. Rivera-López, and A. R. Hefner, *"High-Voltage Isolated Gate Drive Circuit for 10 kV, 100 A SiC MOSFET/JBS Power Modules,"* in Proceedings of the 43th Annual Meeting of the IEEE Industry Applications Society (IAS 2008),October 5, 2008 in Edmonton, Alberta, Canada.

A. R. Hefner *"Power Conditioning System Technologies for High-Megawatt Fuel Cell Plants,"* in Proceedings of DOE 9th Annual Solid State Energy Conversion Alliance (SECA) Workshop, August 5, 2008.

A. R. Hefner, *"Advanced Power Conditioning System Technologies for High-Megawatt Fuel Cell Power Plants,"* in Proceedings of the 2008 Power Engineering Society (PES) General Meeting, July 20, 2008.

J. M. Ortiz-Rodríguez, M. Hernández-Mora, T. H. Duong, S. G. Leslie, and A. R. Hefner, *"Thermal Network Component Models for 10 kV SiC Power Module Packages,"* in the Proceedings of the 2008 IEEE Power Electronics Specialists Conference (PESC), June 15-19, 2008, Island of Rhodes, Greece.

T. H. Duong, J. M. Ortiz-Rodriguez, R. N. Raju, and A. R. Hefner, *"Electro-thermal Simulation of a 100 A, 10 kV Half-Bridge SiC MOSFET/JBS Power Module,"* in the Proceedings of the 2008 IEEE Power Electronics Specialists Conference (PESC), June 15-19, 2008, Island of Rhodes, Greece.

Allen R. Hefner, *"Performance Analysis of 10 kV, 100 A SiC Half-Bridge Power Modules,"* in the Proceedings of the Government Microcircuit Applications and Critical Technology Conference (GOMACTech) 2008, March 17-20, 2008, Las Vegas, NV, pp. 361-364.

T. H. Duong, A. Rivera-López, A. R. Hefner, J. M. Ortiz-Rodríguez, *"Circuit Simulation Model for a 100 A, 10 kV Half-bridge SiC MOSFET/JBS Power Module,"* in the Proceedings of the 2008 IEEE Applied Power Electronics Conference (APEC), February 24–28, 2008, Austin, TX, pp. 913-917.

L. M. Hillkirk, A. R. Hefner, R. W. Dutton, *"Physics-based Numerical Simulation for Design of High-Voltage, Extremely-High Current Density SiC Power Devices,"* IEEE Proceeding of the International Semiconductor Device Research Symposium 2007 (ISDRS 2007), Vol. 9, Washington DC, USA.

L. M. Hillkirk, A.R. Hefner, R. W. Dutton, S. B. Bayne, and H. O'Brien, *"Electro-Thermal, Transient, Mixed-Mode 2-D Simulation Study of SiC Power Thyristors Operating Under Pulsed-Power Conditions,"* Proceedings of the 2007 IEEE International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2007), Sept. 2007, Vienna, Austria, Vol. 12, pp. 181-184.

Tam H. Duong, David W. Berning, A. R. Hefner, Jr., and Keyue M. Smedley, *"Long-Term Stability Test System for High-Voltage, High-Frequency SiC Power Devices,"* Proceedings of the 2007 IEEE Applied Power Electronics Conference (APEC 2007), February 25–March 1, 2007, Anaheim, CA, pp. 1240-1246.

J. M. Ortiz-Rodríguez, T. Duong, A. Rivera-López, and A. R. Hefner, *"High-Voltage, High-Frequency SiC Power MOSFETs Model Validation,"* in the Proceedings of the 2007 IEEE Power Electronics Specialists Conference (PESC), Orlando, FL.

Madelaine Hernández-Mora, Adwoa Akuffo, Colleen Hood, José M. Ortiz-Rodríguez, and Allen Hefner, *"Experimental Evaluation of SiC PiN Diode Forward Bias Degradation and Long Term Stability,"* in the Proceedings of the 2007 IEEE Power Electronics Specialists Conference (PESC), Orlando, FL.

Allen R. Hefner and Sharon Beermann-Curtin, *"Status of the DARPA WBST High Power Electronics Program in SiC Device Development and Technology Transition,"* Proceedings of the Government Microcircuit Applications and Critical Technology Conference (GOMACTech) 2007, March 19-22, 2007, Lake Buena Vista, FL.

Hefner Jr. A. R., Sei-Hyung, R., Brett H., Berning D. W., Hood C. E., Ortiz-Rodriguez J. M., Rivera-Lopez A., Duong T., Akuffo A., Hernandez M., *"Recent Advances in High-Voltage, High-Frequency Silicon-Carbide Power Device,"* Proceedings of the 2006 IEEE Industry Applications Society (IAS) Annual Meeting, October 08-12, 2006, Tampa, FL, pp. 330-337.

Berning D. W., Hefner Jr. A. R., Rodriguez J., Hood C. E., Rivera A., *"Generalized Test Bed for High-Voltage, High-Power SiC Device Characterization,"* Proceedings of the 2006 IEEE Industry Applications Society (IAS) Annual Meeting,October 08-12, 2006, Tampa, FL, pp. 338-345.

Duong T., Hefner Jr. A. R., and Berning D. W., *"Automated Parameter Extraction Software For High-Voltage, High-Frequency SiC Power MOSFETs,"* Proceedings of the 2006 IEEE Workshop on Computers in Power Electronics (COMPEL), July 16-19, 2006, Troy, NY, pp. 205-211.

Ortiz-Rodriguez J. M., Hefner Jr. A. R., Berning D. W., Hood C. E., and Olcum S., *"Computer-Controlled Characterization of High-Voltage, High-Frequency SiC Devices,"* Proceedings of the 2006 IEEE Workshop on Computers in Power Electronics (COMPEL), July 16-19, 2006, Troy, NY, pp. 300-305.

Hefner Jr. A. R., *"Status of High-Voltage, High-Frequency Silicon-Carbide Power Devices,"* Proceedings of the Government Microcircuit Applications and Critical Technology Conference (GOMACTech) 2006, San Diego, CA, March 20-23, 2006, pp. 232-235.

Organic Electronics and Photovoltaics Metrology

Technical Contacts:
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D. Gundlach
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Goals

Organic electronic devices are increasingly incorporated into commercial prototypes and are projected to revolutionize integrated circuits through new applications that take advantage of low-cost, high-volume manufacturing, nontraditional substrates, and designed functionality. A critical need has emerged for new diagnostic probes, tools, and methods to address new technological challenges. Organic electronics adoption will be advanced considerably by the development of an integrated and interdisciplinary suite of measurement methods to correlate device performance with the structure, properties, and chemistry of critical materials and interfaces. NIST will guide the development of standard test methods and provide the fundamental measurements needed for the rational and directed development of materials and processes to realize the potential of organic electronics and photovoltaics.

Customer Needs

An exciting array of new devices and applications are now possible with the development of electronic devices using organic materials because they are amenable to low-cost, high volume manufacturing, incorporation on flexible substrates, and designed functionality. Completely new technologies are under development including printable large-area displays, wearable electronics, paper-like electronic newspapers, ubiquitous integrated sensors, and radio-frequency identification tags. Market estimates range from $10 billion to $30 billion (B) globally by 2010 to 2015, with applications in displays, logic, and lighting. Organic light emitting diodes for displays and lighting form the first generation of products, projected to grow from approximately $0.5 B today to $3 B in 2010. Market expansions to $250 B by 2025 have been estimated should major technology and business barriers be overcome. An emerging application for organic electronics is in low-cost photovoltaic cells, which have the potential to significantly reduce the costs of solar cell manufacturing. At this stage, new materials and processes are evolving rapidly to optimize device performance, ease processing limitations, and demonstrate frontier applications. However, systematic progress in organic electronics and photovoltaics is challenging because of the enormous range of potential materials (from polymers to nanocomposites) and manufacturing methods (roll-to-roll printing, fluidic self-assembly, micro-contact printing, laser ablative printing, and ink-jet printing).

A key technical barrier is the lack of correlation between device performance and the structure, properties, and chemistry of critical materials in the bulk and at interfaces. Without this knowledge, guided improvements in materials, processing, and device design are not possible and meaningful standard test protocols cannot be developed. Characterizing the chemically complex (mostly carbon-based) soft interfaces in organic devices is critical to proper interpretation of carrier transport behavior. Identifying and controlling specific contributions to performance variation requires metrology unavailable to device manufacturers and spanning multiple disciplines that include device physics, chemistry, and materials science.

Technical Strategy

The NIST program focuses on the organic field effect transistor (OFET) and the bulk heterojunction organic photovoltaic (OPV) device as model systems. The OFET is the basic building block of circuitry, and the characteristics and issues that arise during OFET development are transferable to other organic electronic devices because performance is also dominated by molecular design, microstructure, chemistry, and resulting electronic structure in the bulk and at critical device interfaces. The OPV device is significantly different than the OFET because its active layer is a blend with a complex nanoscale structure. NIST is engaged in complementary activities to address the primary technical barriers facing the adoption of organic electronics and photovoltaics: unique measurements of organic materials and interfaces for both structure and chemistry and electronic properties; and the development of an integrated measurement test platform to correlate device performance with the processing conditions, microstructure, and primary chemical structure of organic semiconductors.

1. Correlating structure to performance for OFETs: The basic OFET consists of thin layers (20 nm to 50 nm thick) of disparate materials including the organic semiconductor, dielectric, electrode, and substrate. OFET performance and operational stability critically depend upon charge transport and material interactions between inorganic and organic materials, particularly at semiconductor/dielectric and semiconductor/metal interfaces. Detailed interfacial structure information (electronic structure, molecular orientation, interfacial roughness, interfacial chemistry), correlated with electronic properties is required to predict performance. Correlation development is organized by the paradigm shown in Figure 1, where the microstructure and electronic consequences of variations in chemical structure and processing are precisely measured, and then fed back to our customers to inform further development.

We are developing a suite of powerful measurement methods including X-ray, neutron, optical probes, and electrical tests to characterize critical organic interfaces. Changes in interfacial structure, chemistry, and orientation are correlated with OFET electrical performance. Near-edge X-Ray Absorption Fine Structure (NEXAFS) spectroscopy and nonlinear optical techniques are ideally suited for nondestructive characterization of organic interfaces for chemistry, orientation, and structure. NEXAFS can distinguish chemical bonding in the light elements and measure the orientation of interfacial molecules. Spectroscopic ellipsometry (SE) is a powerful tool to study the electronic state of molecules and evaluate how the transition dipoles of electronic excitations are oriented with respect to film geometry. Polarized infrared absorption (IR) spectroscopy provides both configuration and orientation information for many chemical moieties common to organic electronics materials. Specular and grazing X-ray diffraction (XRD) measurements measure long range positional order to describe unit cell configuration and domain size information. Scanning probe techniques such as atomic force microscopy provide surface morphology information to assess domain shape, size, and spacings. Microscopy techniques such as transmission electron microscopy (TEM) can be used to evaluate the nanoscale organization of crystalline domains in a semiconductor layer. Transient optical-electrical measurements employing a novel time-of-flight test structure design for OFETs can be used to study in-plane charge transport as a function of electric field and charge carrier filling. Finally, small-signal capacitance-voltage analysis of the contact and channel properties of OFETs provides unprecedented insight to the electronic structure, charge trapping, and transport at the semiconductor-gate dielectric interface, and is complimentary to DC electrical measurements which are widely used to evaluate material and device performance.

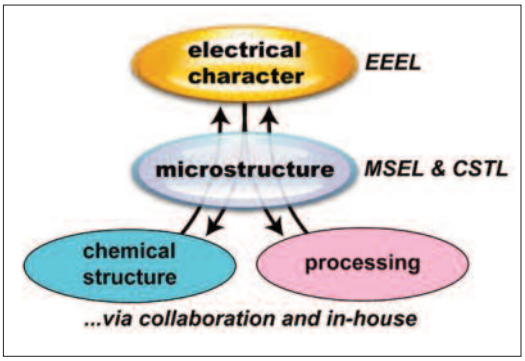

Figure 1. Project paradigm.

DELIVERABLES:

- Complete bias stress electrical measurements of small molecule single crystal semiconductors using scanning Kelvin probe microscopy. 1Q 2010
- Complete detailed structure and electrical measurements on spray deposited poly(thiophene) OFETs. 2Q 2010
- Complete detailed study examining consequences of mechanical strain (flexure) on organic semiconductor structure and electrical characteristics. 3Q 2010
- Complete detailed structure and electrical measurements of stretch oriented (plastically-deformed) poly(thiophene) OFETs. 4Q 2010

2. Correlating structure to performance for OPV devices: One of the most ubiquitous types of OPV device has an active layer that is a blend of an absorbing material and an electron acceptor. The chemical potential offset between the two materials must be sufficient to drive exciton dissociation at the absorber / acceptor interface. The exciton diffusion length is typically quite short in organic absorbers, so excitons can only be harvested if they are formed within ≈ 10 nm of an interface. Since the light path must be at least 100 nm for reasonable absorption of solar radiation, these characteristics necessitate a finely divided architecture where small domains

(≈ 10 nm) are distributed through a thick film (100 to 300 nm), typically called a bulk heterojuction (BHJ). Controlling the morphology of a BHJ film is a critical technology barrier to the introduction of new materials for OPV devices.

We are developing methods for performing structure measurements of BHJ films for OPV devices. NEXAFS, SE, and neutron reflectivity will evaluate the vertical distribution of the two phases and identify which components are in contact with the cathode and anode. XRD will measure the crystalline orientation of the polymer absorber, which affects both its absorbance and the anisotropy of its hole mobility. Morphology characterization measurements such as small angle scattering and TEM will be used to study the three-dimensional architecture of the BHJ film. Transistor measurements will be used to evaluate the transport that occurs in the interfacial layers of the BHJ film. Novel, chemically-selective electro-absorption spectroscopy will be used to determine the field distribution and degradation mechanisms in OPV devices. These results will be correlated to calibrated measurements of OPV device efficiency. These measurements will be combined to determine how the chemical nature of the BHJ components, and how they are processed, affect OPV device performance.

DELIVERABLES:

- Complete study examining the consequences of BHJ aging on its chemistry and morphology, and the OPV device performance. 2Q 2010
- Complete study determining the extent of phase separation in BHJ OPV devices using spin diffusion NMR spectroscopy, 2Q 2010
- Determine how solvent additives affect film microstructure and morphology in BHJ films, and correlate to OFET transport characteristics. 4Q 2010

Accomplishments

DF-TEM imaging combined with a pixel-by-pixel image analysis was used to map crystalline grain orientations within annealed spin-cast poly (2,5-Bis(3-alkylthiophen-2-yl)thieno[3,2-b]thiophene (pBTTT) thin films. pBTTT polymers, a class of state-of-the-art solution-processable semiconducting polymers with field-effect hole mobility as high as 0.1-1 cm^2/Vs, are an important target for spatially-resolved grain measurements because they appear highly crystalline in XRD, and in AFM they exhibit wide terraces that appear to extend laterally several hundreds of nanometers. Accurate determination of lateral grain size, however, has not been possible by these techniques. Two films of a pBTTT with tetradecyl side chains that were processed differently to create different terrace sizes as observed by AFM. Smaller terraces appear on an annealed pBTTT film (≈ 25 nm thick) cast from a 4 mg/ml solution in a solvent pair of 1:8 o-dichlorobenzene to chloroform by volume (SP), whereas larger terraces appeared on an annealed pBTTT film (≈ 15 nm thick) cast from a 5 mg/ml solution in pure 1,2,4-trichlorobenzene (TCB). Both films were subjected to the same thermal annealing procedure (180 °C for 5 min). The grain size in both films was evaluated and directly correlated with charge carrier hopping activation energy extracted from variable-temperature charge-carrier-mobility measurements. It stands out clearly from these maps (see figure 2) that grain orientation changes smoothly across the length scale of a transistor device, rationalizing the fact that pBTTT-C14 films composed of distinctly different sized grains have similar mobility and activation energy, due to the presence of percolated charge transport pathways in both films. The importance of gradient transition of grain orientations in semiconducting polymers needs to be further examined with a broader grain size range.

1H spin diffusion NMR was used to estimate the domain size distribution for BHJ active layers. Bulk samples of regioregular poly(3-hexylthiophene) (P3HT) and phenyl-[6,6]-C60 butyric acid methyl ester (PCBM) were prepared and annealed at several temperatures, and a distribution of domain sizes was observed that ranged over hundreds

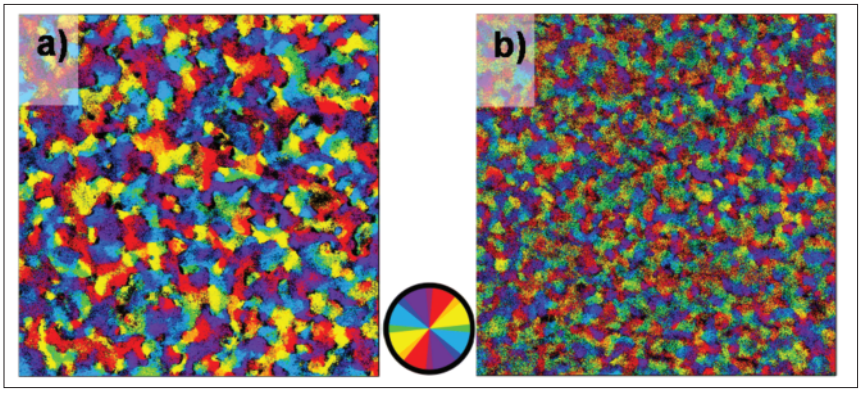

Figure 2. Dark-field TEM orientation plots showing the dependence of the gradient orientation transitions of pBTTT on film processing

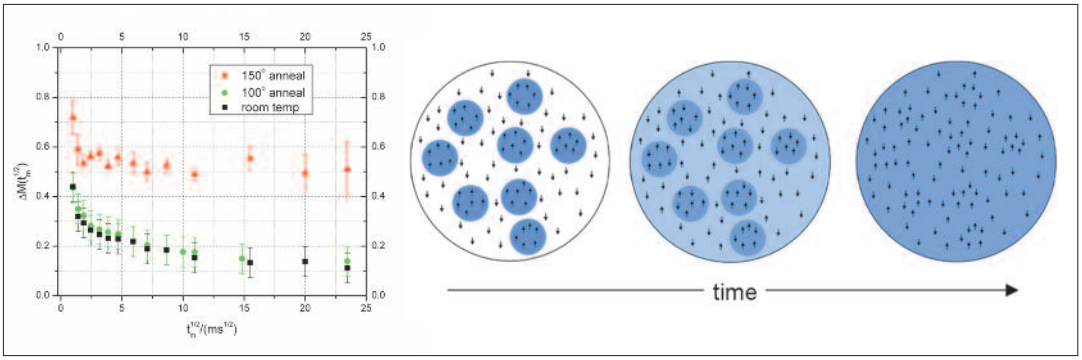

Figure 3. NMR spin diffusion plot showing affect of annealing on the intermixing of P3HT and PCBM.

of nanometers using 1H spin diffusion NMR. Unannealed samples were found to exhibit a large amount of PCBM in small domains (1 to 5 nm) and smaller amounts in moderate (tens of nm) and large (>100 nm) domains (see figure 3). Annealing the samples at 100 °C had no effect on the morphology as evidenced from 1H spin diffusion NMR, grazing-incidence diffraction, and calorimetry, but phase separation was observed after annealing at 150 °C. Even with this higher temperature processing, the 1H NMR showed conclusively that phase separation remained incomplete; this finding was confirmed with photoluminescence quenching measurements. These results demonstrate that 1H solid-state NMR is a powerful means to measure the structure of BHJ blends. We are currently extending this work to thinner, more technologically relevant BHJ films for direct correlation to device properties.

Collaborations

Polymers Division, MSEL –David Germack, Chad Snyder, Steve Hudson, Joseph Kline.

Semiconductor Electronics Division, EEEL – Curt Richter, Oleg Kirillov.

Ceramics Division, MSEL – Daniel A. Fischer.

Surface and Microanalysis Science Division, CSTL – James Kushmerick

Plextronics – Darrin Laird, Sergey Li Imperial College - Iain McCulloch, Martin Heeney, Natalie Stingelin, Thomas Anthopolous.

Stanford Synchrotron Radiation Laboratory – Michael Toney, Sandia National Laboratory - Julia Hsu

University of Kentucky – John Anthony, Penn State University – Tom Jackson.

Publications

Nieuwendaal, et al., *"Measuring the Extent of Phase Separation in Poly-3-Hexylthiophene/Phenyl-C-61-Butyric Acid Methyl Ester Photovoltaic Blends with H-1 Spin Diffusion NMR Spectroscopy,"* Chemistry of Materials 22 (2010) 2930–2936.

Germack, et al., *"Interfacial Segregation in Polymer/Fullerene Blend Films for Photovoltaic Devices,"* Macromolecules 43 (2010) 3828-3836.

Teague, et al., *"Probing Stress Effects In Single Crystal Organic Transistors by Scanning Kelvin Probe Microscopy,"* Applied Physics Letters 96 (2010) 203305.

Chan, et al., *"High Performance Airbrush Organic Thin Film Transistors,"* Applied Physics Letters 96 (2010) 133304.

Dhagat, et al., *"Influence of Dielectric Surface Chemistry on the Microstructure and Carrier Mobility of an n-Type Organic Semiconductor,"* Advanced Functional Materials 19 (2010) 2365-2372.

Lloyd, et al. *"Improved Efficiency in Poly(3-hexylthiophene)/Zinc Oxide Solar Cells via Lithium Incorporation,"* J. Phys. Chem. C, 113 (2009) 17608-17612

Jurchescu, et al., *"Using Polymorphs to Explore the Effect of Crystal Packing on Charge Transport in Molecular Organic Semiconductors,"* Physical Review B. 80 (2009) 085201.

Germack, et al., *"Substrate-Dependent Interface Composition and Charge Transport in Films for Organic Photovoltaics,"* Applied Physics Letters 94 (2009) 233303.

McCulloch, et al., *"Semiconducting Thienothiophene Copolymers: Design, Synthesis, Morphology and Performance in Thin Film Organic Transistors,"* Advanced Materials 21 (2009) 1091-1109.

DeLongchamp, et al., *"Controlling the Orientation of Terraced Nanoscale "Ribbons" of a Poly(thiophene) Semiconductor,"* ACS Nano 3 (2009) 780-787.

Teague, et al., *"Surface Potential Imaging of Solution Processable Acene-Based Thin Film Transistors,"* Advanced Materials 20 (2008) 4513-4516.

Jurchescu, et al., *"Organic Single Crystal Field-effect Transistors of a Soluble Anthradithiophene,"* Chemistry of Materials 20 (2008) 6733–6737.

Lucas, et al., *"Thin film microstructure of a solution processable pyrene-based organic semiconductor,"* Chemistry of Materials 20 (2008) 5743-5749.

Park, et al., *"Structural characterization of conjugated polyelectrolyte electron transport layers by NEXAFS spectroscopy,"* Advanced Materials 20 (2008) 2491.

DeLongchamp, et al., *"The Molecular Basis of Mesophase Ordering in High Performance Semiconducting Polymers,"* Macromolecules 41 (2008) 5709-5715.

Micro- and Nano-Electro-Mechanical Technology Metrology

Technical Contacts:
J. Marshall
C. McGray
R. Allen

"Having seen your proposed work and timetable for producing the (MNT 5-in-1) SRM, we support your work in this area and see value in the semiconductor and MEMS arena."

Mark Crockett,
Applied Materials

Goals

The objective of this project is the development of test structures, test methodologies, and standard reference materials (SRMs) for the characterization of Micro-Electro-Mechanical Systems (MEMS) and Nano-Electro-Mechanical Systems (NEMS) fabrication processes. Since these two technologies differ primarily by scale, they are often referred to as Micro-Nano Technology (MNT). Full characterization of an MNT process requires accurate measurement of a large set of material properties, including: Young's modulus, residual stress, thermal coefficients, surface roughness, density, and Poisson's ratio. In addition, process, device, and packaging parameters must be accurately determined. These parameters include as-fabricated dimensions and wafer bond strength. Ideally these measurements would be quickly performed in the manufacturing line, with large enough sample size to allow characterization of process variation.

Customer Needs

To choose high-impact areas for project resources, customer needs are determined using multiple venues including external conference and workshop attendance and leadership, organizing NIST workshops, and participation in SEMI and ASTM standards organizations.

Members of this team organized a NIST workshop on Microrobotics in June 2008, were on the organizing committee for the SEMI International MEMS Workshop in July 2008, and served as Technical Chair of the 2009 IEEE International Conference on Microelectronic Test Structures. In addition, they have participated in SEMI and ASTM standards development activities and attended numerous conferences and workshops – including the 2010 International Conference on Microelectronic Test Structures, 2009 Conference on Wafer Bonding, 2009 CALCE MEMS Reliability Workshop, METRIC 2009, PRIME 2008, and the 2008 Solid-State Sensors, Actuators, and Microsystems Workshop – which have emphasis on MNT-related technologies.

As part of a broader NIST initiative to determine the metrology needs of U.S. companies, two NIST U.S. Measurement System (USMS) workshops were held in 2005 and 2006 relating to MNT metrology. The first USMS Workshop was held in Pittsburgh, PA on September 22, 2005, immediately after the Metric 2005 Conference. Representatives from a number of companies with interest in MNT technologies attended and were asked to help define and prioritize the metrological needs of the MNT community. From the gathered workshop inputs and subsequent discussions approximately seven measurement needs (MNs) were crafted. One need of particular interest to this project concerns material property measurements for "fabless" MEMS. The concept of fabless MEMS is one in which a company can have devices produced via a foundry rather than their own, expensive (over $100 million), fabrication facility. This is similar to the IC foundry model, which has been successfully implemented in the semiconductor industry. A report describing the outputs of this USMS Workshop was published in the MEMS Industry Group (MIG) 5-year anniversary report.

The second USMS Workshop was held on March 15, 2006, during Pittcon, in Orlando, Florida. This meeting was targeted at metrology needs for microfluidics applications. Representatives from seven companies presented their metrology needs in this rapidly growing field. During this meeting, a need for dimensional metrology was stated. Many of the proposed microfluidic applications depend upon accurately knowing the dimensions of the measurement device.

Technical Strategy

Overview: The MNT standardization efforts in SEMI's North American MEMS Standards Committee include the following:

SEMI MS1-0307 on wafer-to-wafer bonding alignment targets,

"We have more than 100 unique MEMS customers, from Fortune 500 companies to small university labs, and believe the proposed (MNT 5-in-1) standard would be of high interest to all of them."

Erik Novak,
Veeco

SEMI MS2-1109 on step height measurements,

SEMI MS3-0310 on MEMS terminology,

SEMI MS4-1109 on Young's modulus measurements,

SEMI MS5-1107 on critical wafer bond toughness,

SEMI MS6-0308 on design and materials for interfacing microfluidic systems,

SEMI MS7-0708 on microfluidic interfaces to electronic device packages, and

SEMI MS8-0309 on hermeticity of MEMS packages.

Other SEMI MNT standardization efforts include a Young's Modulus and Step Height Round Robin Experiment and a Wafer Bond Strength Round Robin Experiment to obtain precision and bias data to validate the pertinent standards.

NIST: Currently, there are four major standardization thrusts at NIST in the MNT Project:

- The development of the MNT 5-in-1 Standard Reference Materials (SRMs), which includes test structures for five standard test methods on one test chip. For this work, updates are periodically made to the SED MEMS Calculator Web pages.

- The development of an SRM targeted at users of SEMI standard MS5, Test Method for Wafer Bond Strength Measurements Using Micro-Chevron Test Structures and the development of the Micro-Chevron SRM utilizing this standard test method. In addition, the MNT project will continue leadership in maintaining and updating MS5, as necessary.

- Development of electrically based dimensional metrology techniques for features fabricated using MEMS processes.

- Development of metrology tools for the characterization of the motion of MEMS devices, with emphasis on touching motion, including cutting edge microrobotics research and development leading to standardization efforts.

Specific details associated with each of these activities are presented in the Accomplishments section.

DELIVERABLES:

Deliverables associated with the development of the MNT 5-in-1 SRM(s):

- Draft of the quality documentation and certificates required for the SRMs. 3Q 2010
- Publication of updated MS2: Test Method for Step Height Measurements of Thin Films. 1Q2010
- Publication of updated MS4: Standard Test Method for Young's Modulus Measurements of Thin, Reflecting Films Based on the Frequency of Beams in Resonance. 1Q2010
- Submit an SRM design to MEMSCAP for fabrication. 1Q 2010
- Update the SED MEMS Calculator Web Pages. 3Q 2010
- Post-process, if necessary, and package viable SRM chips atop a PZT. 3Q 2010
- Obtain traceability for the SRMs. 3Q 2010
- Measure the viable, packaged SRM chips after any traceability issues are properly resolved. 3Q 2010

Deliverables associated with the development of the Micro-Chevron SRM:

- Present an invited talk at the at 2009 Conference on Wafer Bonding describing results of round robin. 1Q2010
- Publication of updated MS5: Test Method for Wafer Bond Strength Measurements Using Micro-Chevron Test Structures. 2Q2010
- Prepare design and test plan for SRM development. 1Q2010

Deliverables associated with the development of standard methods for measuring presence and extent of voids in bonded wafer pairs in support of 3D interconnect and MEMS packaging

- Participate in team identifying potential metrologies and laboratories. 1Q2010
- Prepare design elements of design for test chip. 3Q2010

Deliverable associated with dimensional metrology for MEMS-processed devices:

- Evaluate dimensional metrology structures incorporated on MNT 5-in-1 SRM design. 3Q 2010

Deliverable associated with characterization of MEMS motion, including touching motion and untethered MEMS devices (MEMS-scale robots):

- Characterization of step length and uniformity of untethered MEMS devices (microrobots). 3Q2010

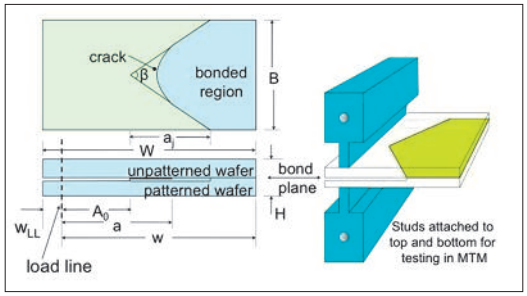

Figure 1. Micro-chevron test structure showing key dimensions and mounting for testing in a materials testing machine (MTM).

- Publish an article describing metrology challenges of microrobots and other touching MEMS devices. 3Q2010
- Organize a competition of nanogram-scale robotics at the 2010 IEEE ICRA Conference. 3Q2010

Accomplishments

■ *Young's modulus measurements:* SEMI standard MS4 obtains Young's modulus from resonating cantilevers oscillating out-of-plane. It applies to films, such as found in MEMS materials, which can be imaged using a non-contact optical vibrometer, stroboscopic interferometer, or an instrument comparable to one of these. A round robin experiment was performed to obtain precision and bias data for validation of the standard. The results of this round robin are incorporated within an article for publication in the NIST Journal of Research.

■ *Calculations of residual stress and its gradient:* SEMI standard MS4 also provides for residual stress and stress gradient calculations. These calculations require the Young's modulus value obtained in the standard and values for residual strain (using ASTM E 2245) and strain gradient (using ASTM E 2246). High values of residual stress lead to failure mechanisms in ICs such as electromigration, stress migration, and delamination. Knowledge of the residual stress values can be used to improve the yield in CMOS fabrication processes.

■ *Wafer bond void measurement:* Participation on team that has identified fourteen laboratories and multiple metrology tools and techniques for a side-by-side comparison of methods for identifying and characterizing void between bonded wafers.

■ *Leadership of revision of SEMI MS-5:* A revised version of SEMI MS5: Test Method for

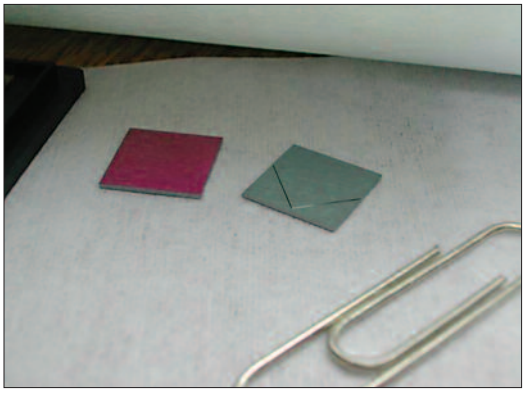

Figure 2. Micro-chevron test structure after testing in a materials testing machine (MTM).

Wafer Bond Strength Measurements Using Micro-Chevron Test Structures was published as MS5-0310 in March 2010. This revision included the precision and bias statement derived from the round robin completed in 2009 as well as numerous clarifications and corrections suggested by participants in the round robin.

■ *Leadership role in the IEEE International Conference on Microelectronic Test Structures:* This conference, which brings together metrology experts from the semiconductor and MEMS community, was founded by NBS staff in the mid-1980s. MNT staff member Allen serves on the technical committee and chaired two sessions at the 2010 meeting. He will be general chair for the 2012 meeting, which will be the 25th anniversary meeting of this conference.

■ *Leadership role in the METRIC 2010 Conference:* Served on the steering committee in planning the conference.

■ *Leadership role in the METRIC 2009 Conference:* Served on the steering committee in planning the conference and co-chaired a working group on Technical Challenges in the Product Development Cycle.

■ *Led development of standard for critical wafer bond toughness:* SEMI standard MS5-1107 uses micro-chevron test structures which consist of two materials, typically two silicon wafers bonded together. The main characteristic of the test structure is the wedge-like structure (which gives it its name) in the bond interface. Studs or blocks are glued to either side of the test structure and positioned in the material testing machine where the test structure is pulled apart

(see Figure 1). The maximum load is measured and the critical wafer bond toughness is calculated, which is a measure of the wafer bond strength. The measurement technique described in this standard can be used to determine a preferred bonding technique and can also be used to obtain spatial information on bonding quality across a wafer.

■ *Organized round robin for precision and bias statement for SEMI MS5:* An eight-laboratory round robin is underway to determine precision and bias for SEMI MS5. This international team includes industrial and academic participants. An image of a post-test micro-chevron test structure is shown in Figure 2.

■ *Step height and thickness measurements:* A round robin experiment was performed to obtain precision and bias data for validation of the SEMI MS2 step height standard. The results of this round robin are incorporated within an article for publication in the NIST *Journal of Research*. Step height measurements using MS2 are incorporated in an electro-physical technique to find the thicknesses of all the layers in a 1.5 µm commercial CMOS foundry process. Figure 3 shows a test chip design with thickness test structures along the top edge of the chip. A design rendition of a sample thickness test structure is given in Fig. 4a, with its cross section given in Fig. 4b. Relatively low values for combined standard uncertainty u_c (between 0.20 nm and 150 nm for a given processing run) have been found. In addition, an earlier version of this technique has been supported via the successful optimization of the Young's modulus values for the various layers in the process. As a rule of thumb, the electrical approach (that obtains thicknesses from capacitance, sheet resistance, and resistivity values) is preferred for thicknesses with u_c values less than or equal to 0.035 nm. This corresponds somewhat to the layers, such as the poly2-to-poly1 oxide and the poly2 layers, which tend to be fabricated earlier in the processing sequence. The capacitances for the oxide layers fabricated earlier in the processing sequence are typically higher and thus easier to measure accurately. For capacitances less than or equal to 24.7 aF/nm^2, the physical approach (that obtains thicknesses from step height measurements) is preferred. The electro-physical technique is detailed in a 39-page paper.

■ *Young's modulus measurements from composite beams:* The test chip design given in Fig. 3 includes cantilevers ranging in length from 100 µm to 400 nm. Plots of Young's modulus versus length for each layer exhibit very good results. The optimized Young's modulus results are stable as a function of length and within the realm of acceptability. Figure 5 shows these plots for metal-1 and metal-2. The data points given at L=500 nm represent the averages from two previous chip submissions. The error bars on the data points represent a plus or minus one sigma variation. The minimum and maximum bounds rep-

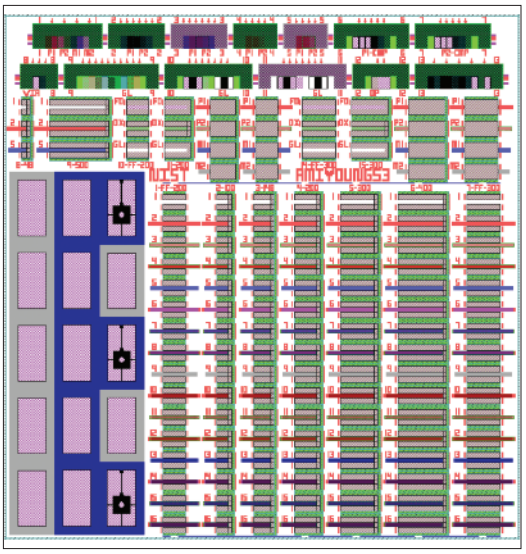

Figure 3. CMOS test chip design incorporating thickness test structures, cantilevers, fixed-fixed beams, and tensile test structures.

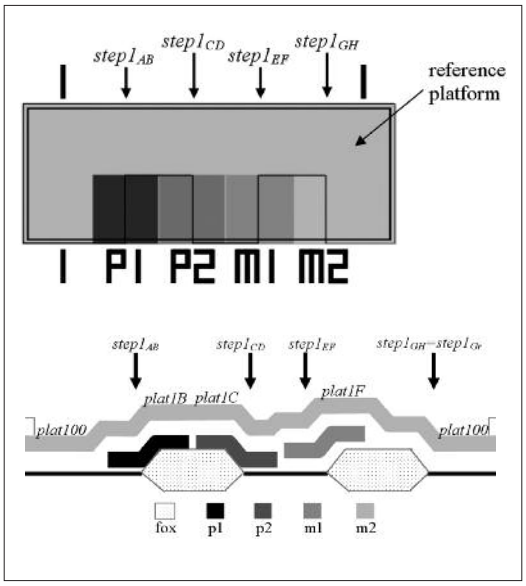

Figure 4. For a thickness test structure: a) a design rendition and b) a cross section.

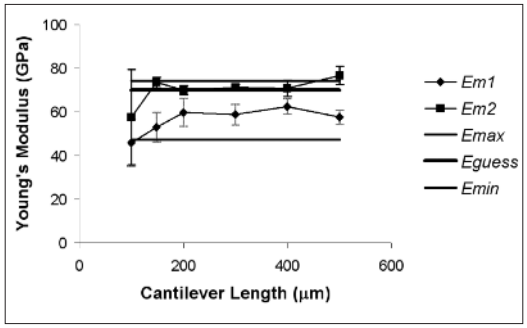

Figure 5. Figure 5. Optimized Young's modulus values for metal1 and metal2 versus length.

resent values given in the literature. The line represented by *"Eguess"* is the initial value used in the optimization. An initial result from tensile tests done by David Read at NIST-Boulder found an average metal-1 and metal-2 Young's modulus value of 63 GPa, which falls nicely between the metal-1 and metal-2 lines in Fig. 5.

■ *SED MEMS Calculator Web pages:* The SED MEMS Calculator Web site includes access to data sheets on which calculations can be performed that go hand-in-hand with select MEMS standards or standards-related work. A symbol can be spotted on the Web site that easily locates material associated with the MNT 5-in-1 SRM.

■ *MNT 5-in-1 SRMs:* Currently, there are two different MNT 5-in-1 SRM designs; one for a bulk-micromachining CMOS MEMS process via MOSIS (see Fig. 6) and the other for a surface-micromachining MEMS process at MEMSCAP (see Fig. 7). The MNT 5-in-1 SRM contains MEMS structures with five specific well-defined geometric and material properties. The five parameters associated with the MNT 5-in-1 SRM are in-plane length, residual strain, strain gradient, step-height, and Young's modulus. The first three parameters have been standardized in ASTM as E 2244, E 2245, and E 2246, respectively. The fourth and fifth parameters have been standardized in SEMI as MS2 and MS4, respectively. The five measurements will be taken at NIST on the MNT 5-in-1 SRM and delivered to the customer along with a certificate and the pertinent SED MEMS Calculator data sheets (completed with NIST data) in order for the customer to compare their in-house measurements with those taken at NIST, thereby validating their use of the documentary standards. Customers, including design companies, equipment manufacturers, and fabrication services, have expressed

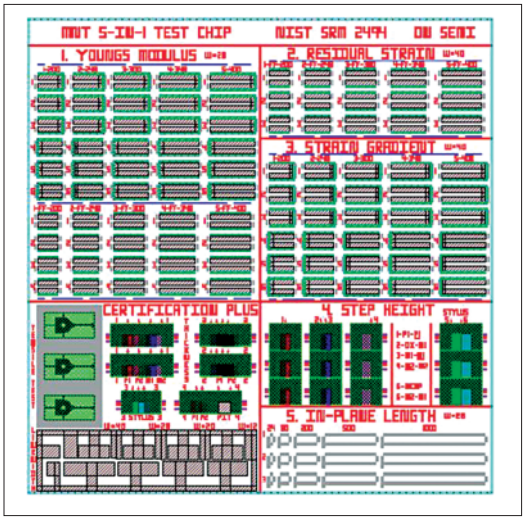

Figure 6. MNT 5-in-1 SRM design for a bulk-micromachining CMOS MEMS process.

support for this SRM. This is an interlaboratory effort, involving several of NIST's laboratories.

■ *Micro-chevron SRM:* A proposal was crafted for the development of a micro-chevron SRM for the calibration of critical wafer bond toughness and a micro-chevron test structure (see Figs. 1 and 2) was designed and fabricated for use in this destructive test. Wafer-wafer bonding is a mainstay for MEMS design and fabrication. MEMS components, such as acceleration sensors, gyroscopes, micropumps, or microvalves that are increasingly found in smart automotive and navigation control systems, and medical devices, which typically use wafer bonding technologies. Due to being subjected to mechanical stresses, the industrial appli-

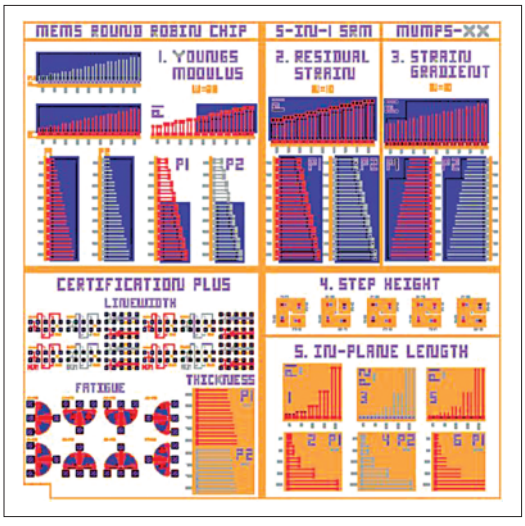

Figure 7. MNT 5-in-1 SRM design for a surface-micromachining MEMS process.

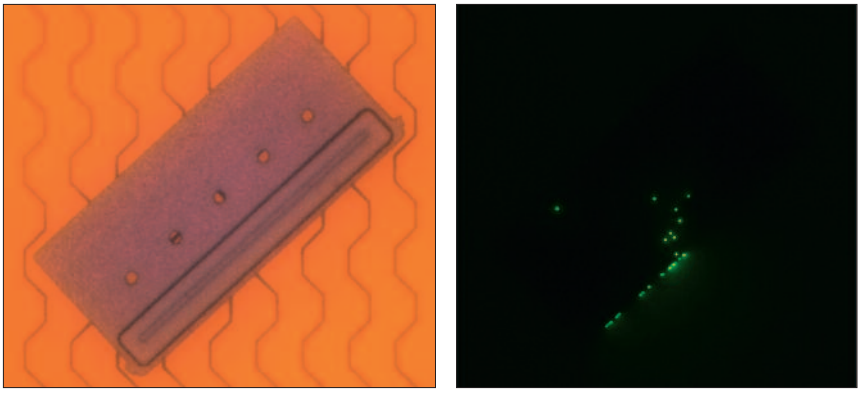

Figure 8. White light and fluorescent micrographs of a tagged untethered scratch drive actuator. The fluorescent tags produce images with well-defined point sprea d functions.

cations of these components require a high mechanical strength and high reliability of the wafer-bonded interface. For a knowledge of the strength determining factors (such as fatigue and stress corrosion) of wafer bonding, for quality control, and for the development of new bonding technologies, a method for determining the strength of such bonds is important to producers and users of MEMS devices, of wafer bonding equipment, and of wafer materials.

■ Dimensional metrology for MEMSs: In the area of dimensional metrology for microfluidics, the MNT Metrology Project has undertaken development of dimensional metrology test structures and techniques. The goal of this work is standard test structures, methods, and analysis techniques such as exist for semiconductor devices.

■ Microrobotics Competitions: In the area of microrobotics, the MNT project founded and leads an annual series of competitions between MEMS-scale microrobots. The competition series, which began in 2007, has produced an increasing variety of novel microrobotic technologies and MEMS actuators, garnering extensive press coverage in print, television, and internet media. The upcoming 2010 competition, which is focused on microassembly, has seen an unprecedented seven teams from institutes around the globe whose technologies have successfully passed qualifying tests.

■ NIST Workshop on MicroRobotics: A workshop was organized by members of the MNT project and held before the 2008 Hilton Head Sensors, Actuators, and Microsystems Workshop. Approximately 40 researchers from industry and academia heard eight invited talks from leaders in the nascent field of microrobotics.

■ Microrobotics Metrology: A method has been devised for applying fluorescent tags to microrobotic devices, allowing fluorescent microscopy techniques to be used for nanometer-precision microrobot position measurements.

Collaborations

Collaborators for the development of the MNT 5-in-1 Standard Reference Materials (SRMs):

MOSIS Integrated Circuit Fabrication Service, 4676 Admiralty Way, Marina del Rey, CA, Dr. P. Thomas Vernier

MEMSCAP Inc., 4021 Stirrup Creek Drive, Suite 120, Durham, NC, Buzz Hardy

Polytec Inc, 16400 Bake Parkway, Irvine, CA, Eric Lawrence

SIOS MeBtechnik GmbH, Am Vogelherd 46, D-98693 Ilmenau, Germany, Dr. Denys Dontsov

Veeco Metrology, 2650 E. Elvira Rd, Tucson, AZ, Dr. Erik Novak

Zygo Corporation, Laurel Brook Rd, Middlefield, CT, Dr. Eric Felkel

NIST Boulder, Materials Science and Engineering Laboratory, Materials Reliability Division, Dr. David T. Read

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Langer Silicon Solutions, Allentown, PA, Paul Langer

Univ. of Wisconsin, Dr. Kevin Turner

Fraunhofer Inst. (Germany), Dr. Joerg Bagdahn

NIST Gaithersburg, Materials Science and Engineering Laboratory, Ceramics Division, Dr. George Quinn

University of Illinois, Dr. Gavin Horn

SUSS Microtec (Vermont), Dr. Shari Farrens

X-Fab Semiconductor Foundries, Dr. Roy Knechtel

Medtronic (Arizona), Mike Mattes, Ralph Danzi

Collaborators for the development of a standard for identifying and characterizing voids between bonded wafers:

BayTech Group, 98 Jericho Road, Weston, MA, Winthrop A. Baylies

NIST Boulder, Materials Science and Engineering Laboratory, Materials Reliability Division, Dr. David T. Read

Univ. of Wisconsin, Dr. Kevin Turner

SEMATECH, Albany, NY, Andy Rudack

Langer Silicon Solutions, Allentown, PA, Paul Langer

Collaborators for the cutting edge robotics research and development which will lead to standardization efforts

Carnegie Mellon University, Nanorobotics Laboratory, Dr. Metin Sitti

Carnegie Mellon University, Electrical and Computer Engineering Department, Dr. Gary Fedder

U.S. Naval Academy, Dr. Samara Firebaugh

ETH Zürich, Dr. Brad Nelson

Simon Fraser University, Dr. Ash Parameswaran

Johns Hopkins University, Dr. Andreas Andreou

Universite de Sherbrooke, Dr. Luc Fréchette

University of Waterloo, Dr. Mustafa Yavuz and Dr. Omar Ramahi

PRESENTATIONS

■Presentation of an invited talk *"A Round Robin Experiment to Provide Precision and Bias for SEMI MS5: Test Method for Wafer Bond Strength Measurements using Micro-Chevron Test Structures"* describing the results of the round robin to provide a precision and bias statement to SEMI standard MS5-1107, Wafer Bond Strength Measurement at the 2009 Conference on Wafer Bonding for Microrsystems, 3D, and Wafer Level Integration in Grenoble, France.

■ Presentation of an invited talk *"MEMS Standards Development at the National Institute of Standard and Technology"* at the CALCE MEMS Reliability Workshop on October 12, 2009.

■ Presentation of an invited talk *"Wafer Bonding Standardization"* describing the development of the SEMI standard MS5-1107, Wafer Bond Strength Measurement at the 2007 Conference on Wafer Bonding for MEMS and Wafer Level Integration in Halle, Germany.

PUBLICATIONS

SED MEMS Calculator Web site: http://www.eeel.nist.gov/812/test-structures/MEMSCalculator.htm.

J. Marshall, R. Allen, C. McGray, and J. Geist, *"MEMS Young's Modulus and Step Height Measurements with Round Robin Results,"* for publication in the NIST Journal of Research (being reviewed).

B. Li, Q. Zhao, H. Huang, Z. Luo, J. Im, M. W. Cresswell, R. A. Allen, M. K. Kang, R. Huang, P. S. Ho, *"Indentation of Single-Crystal Silicon Nanolines: Buckling and Contact Friction at Nanoscale"* Journal of Applied Physics, 105 (2009) 075310.

SEMI MS4, *"Test Method for Young's Modulus Measurements of Thin, Reflecting Films Based on the Frequency of Beams in Resonance,"* November 2009. (Visit http://www.semi.org for ordering information.)

SEMI MS2, *"Test Method for Step Height Measurements of Thin Films,"* November 2009. (Visit http://www.semi.org for ordering information.)

R. A. Allen, J. C. Marshall, W. A. Baylies, D. T. Read, G. D. Quinn, F. W. DelRio, K. T. Turner, M. Bernasch, J. Bagdahn, *"A Standard Method for Measuring Wafer Bond Strength for MEMS Applications"* Proc. ECS: E11 - Semiconductor Wafer Bonding 10: Science, Technology, and Applications, Proc. ECS: E11 - Semiconductor Wafer Bonding 10: Science, Technology, and Applications, Honolulu, HI, United States, 10/12/2008 to 10/18/2008, Vol. 16, No. 8, pp. 449-455, (23-Dec-2008).

J. C. Marshall, D. L. Herman, P. T. Vernier, D. L. DeVoe, and M. Gaitan, *"Young's Modulus Measurements in Standard IC CMOS Processes using MEMS Test Structures,"* IEEE Electron Device Letters 28 (11), 960-963 (2007).

J. C. Marshall and P. T. Vernier, *"Electro-physical Technique for Post-fabrication Measurements of CMOS Process Layer Thicknesses,"* NIST Journal of Research, vol. 112, no. 5, 2007, p. 223-256. SEMI MS5-1107, "Test Method for Wafer Bond Strength Measurements Using Micro-Chevron Test Structures," November 2007.

MEMS Industry Group (MIG) 5-Year Anniversary Report, *"Standardization and the Study of the U.S. Measurement System for Micro Nano Technologies,"* September 2006.

J. C. Marshall, R. I. Scace, and W. A. Baylies, *"MEMS Length and Strain Round Robin Results with Uncertainty Analysis,"* NISTIR 7291, January 2006.

ASTM E08, *"E 2444 Standard Terminology Relating to Measurements Taken on Thin, Reflecting Films,"* Annual Book of ASTM Standards, Vol. 03.01, 2006. (Also available via http://www.astm.org.)

ASTM E08, *"E 2246 Standard Test Method for Strain Gradient Measurements of Thin, Reflecting Films Using an Optical Interferometer,"* Annual Book of ASTM Standards, Vol. 03.01, 2006. (Also available via http://www.astm.org.)

ASTM E08, *"E 2245 Standard Test Method for Residual Strain Measurements of Thin, Reflecting Films Using an Optical Interferometer,"* Annual Book of ASTM Standards, Vol. 03.01, 2006. (Also available via http://www.astm.org.)

ASTM E08, *"E 2244 Standard Test Method for In-Plane Length Measurements of Thin, Reflecting Films Using an Optical Interferometer,"* Annual Book of ASTM Standards, Vol. 03.01, 2006. (Also available via http://www.astm.org.)

NIST's Center for Nanoscale Science and Technology Nanofab

Technical Contacts:
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V. Luciani

Goals

The NIST Center for Nanoscale Science (CNST) and Technology supports the development of nanotechnology from discovery to production. The Center operates a national nanofabrication and measurement facility, the NanoFab, complemented by a multidisciplinary research staff. The NanoFab is an economical, shared use facility accessible to all through a simple application process, providing researchers rapid access to a comprehensive suite of state-of-the-art tools and processes for nanofabrication. While the NanoFab provides access to commercial tools, the CNST's research scientists and engineers are creating the next generation of nanoscale measurement instruments and fabrication methods, which are made available through collaboration. The CNST provides:

Essential measurement and fabrication instrumentation and methods to support all phases of nanotechnology development.

Experts in a wide variety of disciplines; from physics, chemistry, materials science, molecular biology, computer science, and electrical, mechanical, chemical and aeronautical engineering.

A world-class, 60 000 square foot (5500 m^2) nanofabrication facility—with over 19 000 square feet (1,800 m^2) of cleanroom laboratory space.

A hub linking the nanotechnology community to the comprehensive measurement expertise throughout NIST.

Customer Needs

The CNST was established in May of 2007 to accelerate innovation in nanotechnology-based commerce. Its mission is to support the development of nanotechnology through research on measurement and fabrication methods, standards, and technology, and by operating a state-of-the-art nanofabrication facility, the NanoFab. The Center, located in NIST's Advanced Measurement Laboratory Complex on the Gaithersburg, MD campus, promotes innovation by using a multidisciplinary approach to research, maintaining a staff of the highest caliber, and leveraging its efforts by collaborating with others.

Figure 1.The CNST is located in the NIST Advanced Measurement Laboratory Complex, including the NanoFab cleanroom seen on the left. (Photo courtesy HDR Architecture, Inc./Steve Hall © Hedrich Blessing.)

The CNST mission is guided by an understanding that rapid commercial development of nanotechnology—in particular, the speed with which industry can bring a specific new nanotechnology from discovery to production—depends critically on the availability and efficacy of applicable metrology tools and processes at each stage of the transition. Developing these tools and processes will have an immediate and significant impact on the commercial viability of nanotechnologies in a diverse array of fields, such as electronics, computation, information storage, medical diagnostics and therapeutics, and national security and defense.

Technical Strategy

The CNST operates as a multidisciplinary center for developing and disseminating new nanoscale measurement and fabrication technologies, with the goal of increasing the competitiveness of U.S. industry in nanotechnology and nanomanufacturing. By creating a strong research program and establishing a national shared-use nanofabrication facility, the CNST aims to close gaps in the understanding of nanoscale phenomena, and thereby accelerate innovation in a wide range of applications with broad societal impact.

CNST research scientists and engineers are creating the next generation of nanoscale measurement instruments. Based on the collective input of our customers, analysis of ongoing research and advice from NIST's Nanotechnology Strate-

gic Working Group, the CNST is currently giving priority to the following three research areas:

Future Electronics. In support of continued growth in the electronics industry beyond complementary metal-oxide-semiconductor (CMOS) technology, CNST researchers are developing new methods to create and characterize devices, architectures, and interconnects for graphene, nanophotonic, nanoplasmonic, spintronic, and other future electronics.

Nanofabrication and Nanomanufacturing. The Center is advancing the state of the art in nanomanufacturing by developing measurement and fabrication tools for both lithographic ("top-down") and directed assembly ("bottom-up") approaches.

Nano-Enabled Energy Conversion, Storage, and Transport Devices. CNST researchers are creating new methods for elucidating light-matter interaction, charge and energy transfer processes, catalytic activity, and interfacial structure at the nanoscale in energy-related devices.

The Center's Research Project Leaders include experts in atomic-scale characterization and manipulation; electro-fluidic control of nanoparticles; environmental transmission electron microscopy; laser-atom manipulation; modeling and simulation of nanofabrication; nanofabrication; nanomagnetic dynamics; nanomagnetic imaging; nanomaterials for energy storage and conversion; nanophotonics; nanoplasmonics; nanoscale electronic and ionic transport; fluctuations and nanoscale control; nanotribology and nanomanufacturing; optical micro- and nanoelectromechanical systems; theory, modeling, and simulation of nanostructures; and thermoelectrics and photovoltaics.

The NanoFab provides researchers access to and training on the advanced tool set required for cutting-edge nanotechnology development. It is located in a large, dedicated cleanroom — with all the tools operated within an 8000 square feet (750 m2) class 100 space — and in adjacent laboratories. These laboratories include superior vibration, temperature, humidity control, and air quality. Over 65 major tools are available for e-beam lithography, photolithography, nanoimprint lithography, metal deposition, plasma etching, atomic layer deposition, chemical vapor diffusion, wet chemistry, and silicon micro/nanomachining. The facility is accessible through a straightforward application process designed to get users into the cleanroom in a few weeks. It is open from 7 am to 7 pm, Monday through Friday (normal operating hours will be expanded to midnight in the second half of 2010).

A comprehensive list of the NanoFab equipment is included below. Of particular note are the electron beam lithography tools, which include a Vistec VB300 in the cleanroom with <10 nm linewidth and a JEOL JBX-6300FS system with comparable capabilities outside the cleanroom. Other important capabilities are enabled by a Zeiss NVision 40 focused ion beam (FIB) system incorporating a Gemini scanning electron microscope and four-channel gas injection system. It can accommodate from mm-sized samples to 100 mm-diameter wafers for nanometer scale patterning, etching, nanomanipulation, and TEM sample preparation.

NanoFab Equipment

Figure 2. A plasma etching bay in the NanoFab's class 100 cleanroom.

Lithography

E-beam Lithography System: Vistec VB300

E-beam Lithography System: JEOL JBX-6300FS*

Laser Pattern Generator: Heidelberg DWL-66FS

Nano-Imprint Lithography Tool: Nanonex NX-2000

Nanonex Ultra-100 Integrated UV-Ozone Cleaner/Molecular Vapor Coater

Contact Aligners (2): Suss Microtec MA6 and MA8

Spinners (2): Laurell Technologies Series WS-400 and WS-500

Spinner/Hotplate: Brewer Science CEE Model 100CB

Process Benches (2): E-Beam Resist Processing Stations*

Furnaces

General Thermal Oxidation and Diffusion (Bank 2)

CMOS Thermal Oxidation and Diffusion (Bank 1)

Low Pressure Chemical Vapor Deposition (LPCVD) Furnace (Bank 3)

Rapid Thermal Annealer: Modular Process Technology

PECVD-Unaxis 790

Metal Deposition

Sputterers (2): Denton Vacuum Discovery 22 and Discovery 550

E-beam Evaporators (2): Denton Infinity 22

Wet Chemistry

Heated Wet Chemical Benches (2): 2 m and 2.4 m

KOH/TMAH Wet Etch Bench: Reynoldstech

Acid Etch Bench: Reynoldstech

Spin Rinse Dryers: Semitool PSC-101

HF Vapor Etcher: AMMT*

Dry Etch

Deep RIE: Unaxis SHUTTLELINE DSEII

Metal RIE: Unaxis 790

Silicon RIE: Unaxis 790

Multipurpose RIE Systems (2): OxfordICP Metal Etcher: Unaxis SHUTTLELINE ICP

XeF2 Silicon Etch: Xactix Xetch e1 Series

Microwave Plasma System: PVA Tepla 300

Specialty Tools

Atomic Layer Deposition: Oxford FlexALRPT

Parylene Deposition System: Specialty Coating Systems PDS-2010

Wafer Bonder: Suss Microtec SB6e

Focused Ion Beam: Zeiss NVision 40

Inspection

Stress Measurement Tool: Toho Technology FLX-2320

Table-top SEM: Hitachi TM-1000

Scanning Electron Microscope: Zeiss Ultra-60 FESEM w/EDS

Transmission Electron Microscope: FEI Titan*

Atomic Force Microscopes (2): Veeco Dimension 3000, Dimension 3100

Contact Angle Goniometer

Spectroscopic Ellipsometer: Woollam XLS-100

Reflectometers (3): Filmetrics, Nanometrics, Angstrom Sun

Contact Profilometer: Dektak 6M

Optical Microscope with Image Capture: Nikon

Four-Point Probes (2): Jandel RM2

High Power Inspection Microscopes: Olympus

High Power Nomarski Microscope: Nikon

Post Process

Wafer Dicing Saw: Disco Model 341

Wire Bonder: Kulicke and Soffa Model 4526

Critical Point Dryer

DELIVERABLES:

*New tools to be operational in 4Q2010

Disclaimer

Certain commercial equipment, and software, are identified in this documentation to describe the subject adequately. Such identification does not imply recommendation or endorsement by the National Institute of Standards and Technology, nor does it imply that the equipment identified is necessarily the best available for the purpose.

Metrology for Spintronic Devices

Technical Contacts:
W. Rippard
M. Pufall

Goals

The overall goal of the Metrology for Spintronic Devices program is to develop the metrological tools that will enable the development of electronic devices that exploit the electron spin degree of freedom in addition to its charge. Present spintronic devices include magnetic random access memory (MRAM), hard-disk drive read heads, and other highly compact magnetic memory devices. In addition, spintronic devices also present an avenue towards replacing conventional complementary metal oxide semiconductor (CMOS) technology as device dimensions shrink into the deep nanometer regime, with the development of entirely new device structures such as nanoscale microwave components for on-chip spectral analysis, nanoscale timing elements, and microwireless communication architectures. In each case, a fundamental understanding of the interactions between a spin-polarized current and ferromagnetic metals and semiconductors is a necessity. The particular goal of this project is to develop the metrology and perform the fundamental measurements to enable the development of these spin-based devices.

Customer Needs

MRAM has been incorporated into commercial electronics since late 2006 and has the potential to enter the marketplace as a low-power "green" memory in future electronics. It is expected that the present circuit architecture, which relies on switching (writing) using applied magnetic fields, will not be viable beyond the 65 nm lithography node. This limitation arises from the scaling laws associated with the stability of the magnetic structures used in MRAM devices: As the device dimensions are decreased, the magnetic elements are required to have increased stability against thermal fluctuations. This, in turn, requires larger writing fields, which cannot be supported in the present device architecture. It is projected that *spin transfer* induced switching will be essential for device scaling beyond the 2013-2015 timeframe (ITRS roadmap 2009). While this switching mechanism is very promising, it has only been an active area of research for the last few years, and although certain aspects of the switching processes are well understood, others are not. The main thrust of our program in this area is to develop metrologies that will help us to understand the physics of spin transfer switching, and so enable the development of spin transfer based MRAM (spin-RAM) for the commercial market.

In order for spin-RAM to be technically viable at the smallest device sizes, the fundamental metrology to characterize the intrinsic scaling laws associated with the spin transfer effect need to be developed. In particular, methods to definitively relate threshold switching currents to fundamental materials properties need to be developed, materials damping parameters need to be measured at the device level, and the detailed angular variation of the spin torque needs to be understood. Furthermore, methods must be developed that can reliably predict write error rates and accidental "read disturbs" with accuracies approaching 1 part in 109 from simple and rapid measurements. Developing these capabilities is the focus of this program which will enable the reduction of device switching currents (which are limited by available transistor source currents), as well as the underlying mechanisms causing variations in device-to-device behaviors.

These measurements and techniques have been somewhat developed in all-metallic systems with conventional in-plane magnetized ferromagnetic alloys. However, it is expected that tunnel junction structures will be required for commercial applications and novel magnetic materials (e.g., perpendicularly magnetized materials, highly spin-polarized materials) may be needed. To aid in the exploration and optimization of new materials and device processes, new wafer-level techniques are needed for non-destructively and rapidly measuring their ferromagnetic resonance properties, ideally with a high spatial resolution. This program's efforts will be particularly focused on developing metrologies to better understand device to device switching variations that may result from device processing or materials variations, by developing a large area scanned probe ferromagnetic resonance (FMR) measurement system.. In addition, we will extend our measurements to elucidate the behavior of devices having perpendicularly magnetized films and magnetic tunnel junction structures.

Technical Strategy

The technical strategy is to develop the metrology and perform the fundamental measurements to characterize and understand the effects of spin-polarized currents in spin-based magnetic nanostructures. Particular attention will be paid to measuring the intrinsic scaling laws associated with device switching times in magnetic tunnel junction MRAM structures and to develop measurement techniques that will allow accurate prediction of rare switching events through rapid device screening. A clear understanding of the role that thermal contributions play in determining the critical current densities and switching mechanisms will be essential for future scaling of these devices. Additional measurements will investigate the effects of shaped switching pulses and developing metrologies to measure the ferromagnetic resonance (FMR) response of individual nanoscale MRAM elements and how that response can be used to predict its switching characteristics. These measurements will directly address the role of patterning techniques and anisotropy variations in determining the switching distribution of MRAM elements. These metrologies will provide a basis for scaling of MRAM devices below the 65 nm node. Our technical work will also focus on evaluating the potential of emerging nanoscale spintronic devices for replacing/augmenting CMOS in the deep nanometer regime.

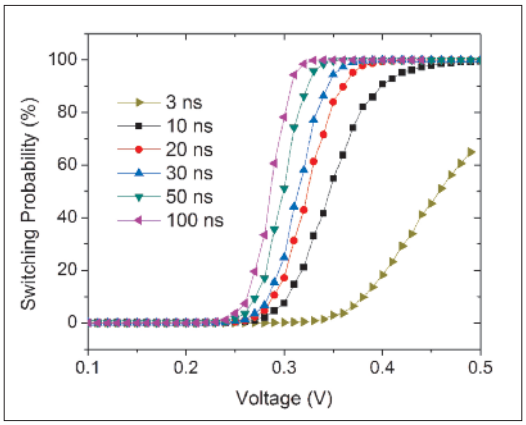
DELIVERABLES:

- Metrology to determine switching error rates and read error distribution tails in spin-RAM devices with accuracy of 1 part in 106 (Q1, 2010)
- Metrology to determine and compare thermal stability factor (delta) of spin-RAM elements determined by field switching and high speed current switching. (Q2, 2010)
- Compare thermal activation model for switching at ns time scales with measurements in spin-RAM devices performed at 300 K and 4 K and determine heating effects. (Q3 2010)

Accomplishments

High-Speed, Current-Induced Switching for MRAM Devices: We have developed the capabilities to fabricate and measure sub-ns switching in spin-RAM structures having critical dimensions below 50 nm with statics approaching 1 part in 109. The newly developed measurement techniques represent roughly a factor of 104 increase in the data acquisition rate. Because the switching probabilities can be measured with such increased statistical averaging, the resulting switching probability distributions can be determined very accurately. These measurements are allowing extremely detailed comparisons between theoretical models and measured device behavior that have not been previously available. We have found that while the basic features of the switching distributions can be described by present models, the tails of the distributions, i.e., rare events in which a device is accidentally written during a "read" operation or is not correctly written during a "write" process at the level of 1 event in greater than 106 attempts (Fig. 1), are not correctly captured by present theory. It is precisely these errors, and their device-to-device variation, that need to be understood for successful implementation of spin-RAM in the future. To date, the only method to reliably ascertain these rates is by directly measuring them, which is a time-intensive process. The metrologies that we are developing in this program aim to screen for such events using rapid (MHz) high-statistics measurements as well as microwave (GHz) spectroscopic techniques allow fast and complete device characterization. These measurements will allow for improved device design and reliability for future MRAM at the 65 nm node and beyond.

Damping in Magnetic Nanostructures: One of the critical parameters in determining the threshold switching current in magnetic devices is the magnetic damping parameter; the larger the damping in the system, the larger the current required to switch the device. While material dependent



Insert Fig. 1 here with caption: Figure 1. Measured switching probability from the anti-parallel to parallel state as a function of pulse voltage for times between 3ns to 100 ns. Each data point corresponds to 105 switching attempts.

damping parameters have been routinely measured in macro/microscopic devices, very little is known about how damping is affected when device sizes are decreased to the nanometer length scale. As device dimensions are decreased, the surfaces of the devices become increasingly important. This is particularly the case for damping in magnetic nanostructures. Nanomagnetic devices will typically have oxidation of the ferromagnetic materials on at least some of their sides, and ferromagnetic oxides are well known sources of damping. Recently some researchers have shown indirect evidence that the magnetic damping in magnetic nanostructures can be increased by more than a factor of ten relative to that of macroscopic devices. We have recently developed the metrology capabilities to directly measure the magnetic damping of individual magnetic devices having essentially arbitrary dimensions. Our measurements have shown that (at room temperature) while oxidation actually has a negligible effect, shape variations in nanoscale devices increase the apparent damping by roughly a factor of two. These data suggest that nanoscale patterning defects will become a significant factor in determining the device performance in future generation magnetic nanostructures.

Thermal Stability of Magnetic Nanostructures: Accurate measurement of the thermal stability factor Δ (the *minimum* energy required to switch a magnetic bit divided by k_BT) of a magnetic nanostructure is important for determining the time that information can be reliably retained. Differences in Δ of only a few percent can translate into information being retained for 10 years or only a few, since the stability time goes as e^{Δ}. In larger magnetic structures, defining this minimum is relatively straightforward since the lowest energy switching trajectory is well-separated from the multitude of alternative routes. However, as the size of storage elements are reduced into the nanometer regime nearly all physically realizable switching trajectories lie within a few k_BT of each other, complicating both the measurement and its analysis. Additionally, while the stability of a magnetic bit must be considered in terms of years, the switching of it must be performed on the order of nanoseconds. On such short timescales the thermal energy in an individual bit can no longer be considered as constant or uniform. Instead, the magnetic fluctuations in a device must be considered as resulting from thermal energy being transferred into a finite number of magnetic eigenmodes in the device (Fig. 2), with their relative amplitudes changing with time. The relative strength of theses spatially different modes is expected to give rise to different switching characteristics. Such spatial and temporal fluctuations clearly lead to stochastic switching behaviors in these structures, which is presently only partially understood. One goal of this program is to perform detailed measurements in well-controlled device environments in order to better understand how these thermal disturbances affect the switching characteristics of MRAM devices and next-generation media for hard disk drives.

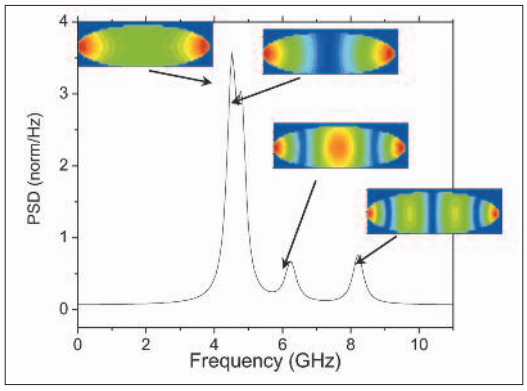


Figure 2. Calculated average spectrum and resonant spatial modes of 50 x 150 x 2 nm³. The magnetization amplitude is shown in a false colors scale with larger amplitude shown in red and zero amplitude shown in blue.

Collaborations

IBM: MRAM device imaging and thermal induced noise in tunnel-junction based MRAM devices. Freescale Semiconductor: MRAM device imaging and incorporating magnetic tunnel junctions into MRAM devices. Grandis and Intel: Statistical methods to determine thermal stability and error rates in spin-RAM devices.

Hitachi Global Storage Technologies: high-speed switching in all-metallic MRAM devices, high frequency head design

U. S. Army Research Laboratory: high frequency impedance measurements.

Publications

Nanoscale spintronic devices also provide an opportunity for the development of dense non-volatile memory elements as well as new spin-enabled nanoscale microwave devices, such as microwave sources and mixers for timing, communications, and spectral analysis applications. In addition, they also provide one potential avenue towards replac-

ing/augmenting conventional CMOS devices in the deep nanometer regime. As such, we expect spintronic devices to have a great impact on the semiconductor industry, particularly as device dimensions shrink into the nanoscale. The goal of this project is to provide the fundamental metrology and measurements to enable the development of this wide range of devices and applications.

Publications

W. H. Rippard, A. M. Deac, M. R. Pufall, J. M. Shaw, M. W. Keller, G. E.W. Bauer, and C. Serpico, *"Spin-transfer dynamics in spin valves with out-of-plane magnetized CoNi free layers,"* Physical Review B, 81, 014426 (2010).

R. Heindl and W. H. Rippard, *"Emerging Devices Based on Spin Transfer Torque Effect,"* ECS Transactions Graphene and Emerging Materials for Post-CMOS Applications, 19, 21-32 (2009).

M. L. Schneider, W. H. Rippard, M. R. Pufall, T. Cecil, T. J. Silva, and S. E. Russek, *"Temperature dependence of spin-torque-driven self-oscillations,"* Physical Review B, 80, 144412 (2009).

M. W. Keller, A. B. Kos, T. J. Silva, W. H. Rippard, and M. R. Pufall, *"Time domain measurement of phase noise in a spin torque oscillator,"* Applied Physics Letters, 94, 193105 (2009).

J. Sierra, G. Aliev, R. Heindl, S. Russek, and W. Rippard, *"Broadband ferromagnetic resonance linewidth measurement of magnetic tunnel junction multilayers,"* Applied Physics Letters, 94, 012506, 2009).

R. Heindl, S. E. Russek, T. J. Silva, W. H. Rippard, J. A. Katine, and M. J. Carey, *"Size dependence of intrinsic spin transfer switching current density in elliptical spin valves,"* Applied Physics Letters, 92, 262504 (2008).

M. R. Pufall, M. L. Schneider, W. H. Rippard, and S. E. Russek, *"Low-field current-hysteretic oscillations in spin-transfer nanocontacts,"* 75, 140404R (2007).

M. L. Schneider, M. R. Pufall, W. H. Rippard, S. E. Russek, and J. A. Katine, *"Thermal effects on the critical current of spin torque switching in spin valve nanopillars,"* Applied Physics Letters 90, 092504 (2007).

W. H. Rippard, M. R. Pufall, and S. E. Russek, *"Comparison of frequency, linewidth, and output power in measurements of spin-transfer nanocontact oscillators,"* Physical Review B 74, 224409 (2006).

M. R. Pufall, W. H. Rippard, S. E. Russek, S. Kaka, and J. A. Katine, "Electrical measurement of spin-wave interactions of proximate spin transfer nanooscillators," Physical Review Letters 97, 087206 (2006).

S. Kaka, M. R. Pufall, W. H. Rippard, T. J. Silva, S. E. Russek, and J. A. Katine, "Mutual phase-locking of microwave spin torque nano-oscillators," Nature 437, 389-392 (2005).

W. H. Rippard, M. R. Pufall, S. Kaka, T. J. Silva, S. E. Russek, and J. A. Katine, *"Injection locking and phase control of spin transfer nano-oscillators,"* Physical Review Letters 95, 067203 (2005).

S. Kaka, M. R. Pufall, W. H. Rippard, T. J. Silva, S. E. Russek, J. A. Katine, and M. Carey, *"Spin transfer switching of spin valve nanopillars using nanosecond pulsed currents,"* Journal of Magnetism and Magnetic Materials 286, 375-380 (2005).

S. E. Russek, S. Kaka, W. H. Rippard, M. R. Pufall, T. J. Silva, and M. Donahue, *"Micromagnetic modeling of nano-contact spin-transfer oscillators,"* San Jose, Magnetism and Magnetic Materials Conference, ES-25, 2005.

Magneto-resistance and spin transport in non-traditional tunnel devices

Technical Contacts:
J.M. Pomeroy

Goals

The goal of the project is to explore non-traditional methods for creating high-transparency tunnel junctions, optimize spin transport through these junctions, and test fundamental limits of the tunneling process in the thin barrier limit. In addition to exploring non-traditional fabrication schemes, novel metrologies are explored to better quantify the role and performance of spin in these device systems.

Customer Needs

Since the introduction of giant magneto-resistive (GMR) hard drive read heads in 2000, spin transport devices have been a part of the technological mainstream. These devices produce a substantial difference in the device resistance due to the remnant magnetic field from a bit stream on the hard drive platter. As the read head is scanned over the platter surface, the pattern of high and low resistances produced by the GMR device maps directly to the information stored on the hard drive. These CIP-GMR (current in plane) read heads fueled an ambitious increase in hard drive information density over several years, but ultimately pushed beyond limits of CIP-GMR feasibility. Consequently, tunneling magneto-resistance (TMR) based read heads were introduced in 2005 to enable new generations of increased density hard drives. Similar to the GMR-based hard drives, TMR read heads exhibit a change in resistance corresponding to the remnant field of the bit stream on the hard drive platter. TMR-based devices use a metal-insulator-metal tunnel junction interface that results in relatively high resistances and resistance-area (RA) products (the mathematical product of the resistance and cross sectional area). As a result, as the hard drive industry moves to higher density generations, the corresponding reduction in the TMR head size acts to increase the resistance and decrease the effective bandwidth. These technical limitations have resulted in dim prospects for extensive reliance on TMR read heads and a re-investment in a modified current-perpendicular to the plane (CPP) GMR-type read head. While the TMR read heads exhibit RA products that are undesirably large, the CPP GMR heads currently have undesirably small RA products. An ideal middle ground for future hard drive read heads would come from *a layer structure with an intermediate RA product that still exhibits good magnetic field sensitivity with high bandwidths and low power dissipation.*

Magneto-resistive hard drive read heads and the bourgeoning MRAM industry are both spintronic devices, where information is stored, processed, or transferred using electron spin rather than charge. As the semiconductor industry moves "beyond CMOS," successful discovery and implementation of spin processing and data transmission systems rely on yet to be developed systems for spin transport and accumulation. As the most effective means of injecting spin yet discovered*, tunnel junctions figure to be prominent players in spin information processing, demanding spin metrology systems and exquisite understanding of spin transport mechanisms.*

Technical Strategy

High transparency (low electrical resistance) tunnel junctions that preserve (or improve, i.e., spin filter) spin polarization and enable spin-based information technology are of intense technological interest as magnetic sensors, MRAM memory, and for direct spin-degree-of-freedom information processing. As tunnel junctions reach the lower limits of barrier thickness (atomic sizes), both practical limitations related to uniformity of deposition and long standing reliance on the WKB

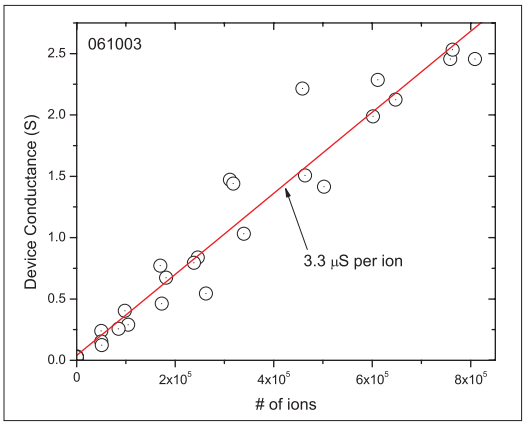


Figure 1. Ion based tunnel barrier modification can adjust the electrical conductance of magnetic tunnel junction over a range spanning several orders of magnitude, providing an economical means of exploring the properties of tunnel barriers in the extreme limit of thin barriers.

(Wentzel, Kramers and Brillouin) approximations of tunneling pose new challenges. Rather than pursue conventional approaches to increasing tunnel junction transparency through uniform deposition of a thinner barrier, we are utilizing a unique process approach where a robust and reproducible tunnel barrier (typically 1.5 nm thick) is deposited and then irradiated with ions. The irradiation process relies on the deposition of the ion's neutralization energy (as much as 52 keV per ion), thinning a nanometer-sized area of the base tunnel junction to yield a tunnel junction only Angstroms thick whose conductance dominates the electrical performance of the whole device. Applying this approach, a single layer structure can be tuned to a user-selected conductance value spanning many orders of magnitude by adjusting the irradiation parameters. This strategy provides a test bed for optimizing the spin transport and understanding the role of spin scattering in the limit of ultra-thin tunnel barriers. At present, our research is establishing the benefits and limitations of the irradiation-based processing approach, the impacts on magnetic tunnel junction performance while developing the technical competence to integrate unique high-polarization and spin filtering materials and establishing new metrologies for quantifying systems with spin-dominated performance. Future work will focus on optimizing spin injection and accumulation through tunnel barriers and establishing cornerstones for absolute spin polarization measurements and broader spin metrology.

DELIVERABLES:

- Develop physical model for electronic energy deposition in ultra-thin insulating films that accounts for observed dependences on tunnel barrier thickness, stoichiometry, and ion charge state (electronic energy). 2Q 2010
- Deploy and develop process recipes for new generation of oxygen plasma chamber – the tunability of the ion process, as well as the base tunnel junction reliability sensitively depends on the oxidation process. In the work to date, the oxygen plasma chamber processing has been the limiting factor on ultimate device performance. 2Q 2010
- Evaluate the TMR of devices modified with different charge states – prior measurements suggest that the magnetic properties of the MTJs should be insensitive to the charge state in the irradiation, and this is a direct test. 3Q 2010
- Complete the process development of niobium based MTJs and begin ion irradiation. 3Q 2010
- Magneto-resistance first order reversal curve (MR-FORC) characterization of NVE devices and delivery of results . 3Q 2010

Accomplishments

■ *Selectable resistance area product spanning four orders of magnitude from a single process recipe* – An economical method for producing variable transparency tunnel junctions from a single tunnel barrier recipe is demonstrated in Fig. 1. The data in the figure correspond to a set of MTJ devices with a ≈ 1.0 nm tunnel barrier sandwiched between adjacent cobalt layers. Similar data has been taken for tunnel barriers at thicknesses ranging from 0.9 nm to 1.7 nm and for a range of different barrier stoichiometries. The compilation of these data shows that for a single charge state, the conductance increases less for tunnel barriers with higher starting RA products. Different combinations of materials deposited, different thicknesses, magnetic behaviors, and exchange biases have been explored to establish the universal applicability of the process technique. Current voltage measurements and temperature dependence both indicate that the devices remain tunnel junctions after the irradiation (rather than metallic point contacts) and retain the high quality of the initial barrier. Accumulated data suggests that the reproducibility of the irradiation process is limited by the tunnel barrier preparation, rather than the ion adjustment, motivating the deployment of an improved plasma oxidation chamber (see deliverables).

■ *Magneto-resistance in conduction channels produced by ion irradiation measured* – The value of selectable RA product tunnel junctions is dramatically increased if they are useful as magnetic sensors. The data in Fig. 2 are taken on

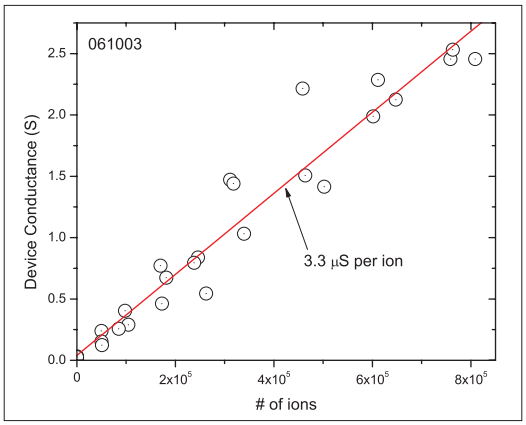


Figure 2. Magneto-resistance plot from a magnetic tunnel junction device who resistance has been lowered with ion irradiation demonstrating that the ion process is capable of producing usable sensor devices.

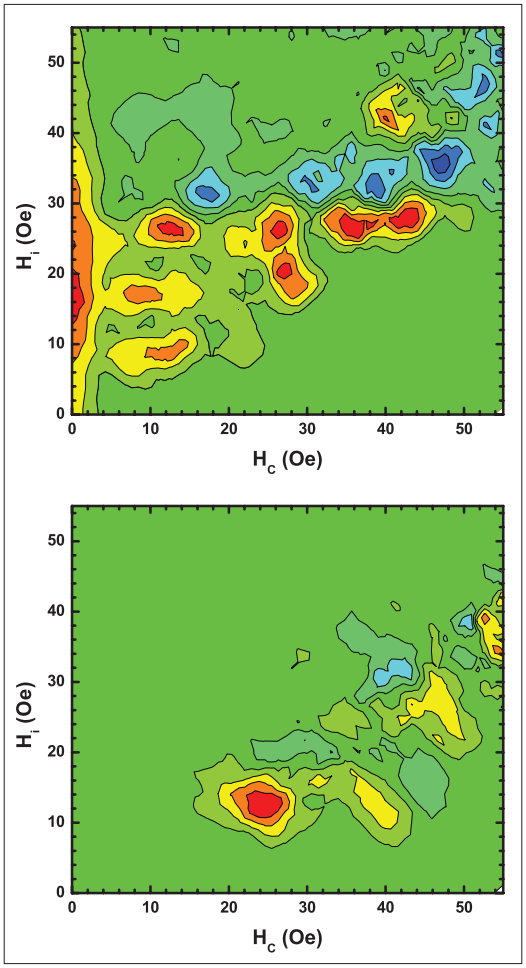


Figure 3. MR-FORC plots from two CoFeB/MgO/FeCoB based MTJs that are identical except the device shown in the upper panel was annealed and the lower was not.

a device whose resistance is a factor of three lower than the base tunnel junction resistance but which still exhibits robust magneto-resistance. Exploration of the magneto-resistance for varying barrier properties indicates that for some tunnel barriers, the irradiation produces conductance channels that preserve spin polarization. Preservation of spin polarization appears to be related to the barrier material stoichiometry and preparation methods. A detailed future study is expected to revisit this topic once the improved oxygen plasma chamber is operational.

■ *Tunability of conductance channels by variation of ion charge state measured* – While all the results demonstrated utilize highly charged ions, the role of the charge state provides an additional degree of freedom, and therefore additional control. Since the barrier reduction process relies on the ion's neutralization energy much more than on kinetic energy, the rate of change of the tunnel junction conductance depends strongly on the ion's charge state. Each charge state conductance change (slope in Fig. 1) that depends exponentially on the charge state. For the range of charge states studied, the conductance added per ion spans a range of more than three orders of magnitude, from 1.5 nS/ion to 5 μS/ion.

■ *Visualization of MTJ magnetic switching properties by MR-FORC* – MR-FORC has been pioneered as a method for visualizing the magnetic switching characteristics in fully patterned, electrically functioning MTJs. An example is shown in Fig. 3 where an annealed MTJ and an unannealed MTJ that are otherwise identical in material stack, size and measurement exhibit very different switching distributions. The color scale in the plots represents the density of magnetic switching as a function of the coercive field (Hc) and the interaction field (Hi). In the annealed sample, the soft magnetic layer act much more uniformly than the unannealed case, where the dynamics are much more fragmented.

Collaborations

A collaboration using MR-FORC to characterize commercial devices produced by NVE Corporation, Eden Prairie, MN is ongoing.

An active and ongoing collaboration also exists with Prof. C. Sosolik of the Clemson University Department of Physics and Astronomy.

The work described here has benefited from interactions with many other NIST personnel, including N. Zimmerman, E. Tiesinga, J. Gillaspy, J. Tan, M. Stiles, J. Read, and W. Egelhoff.

Publications

Lake, R.E., J.M. Pomeroy, and C.E. Sosolik, *"Energy dissipation of highly charged ions on Al oxide films,"* Journal of Physics-Condensed Matter, 2010. 22(8).

Pomeroy, J.M., T.C. White, H. Grube, J.C. Read and J.E. Davies, *"Magnetoresistance based first-order reversal curve analysis of magnetic tunnel junctions,"* Applied Physics Letters, 2009. 95(2): p. 022514-3.

Pomeroy, J.M., and H. Grube, *"Negative resistance" errors in four-point measurements of tunnel junctions and other crossed-wire devices,"* Journal of Applied Physics, 2009. 105(9): p. 094503-8.

Pomeroy, J.M., and H. Grube, *"Highly Charged Ion (HCI) Modified Tunnel Junctions,"* AIP Conference Proceeding Series, 2009. 1099: p. 520.

Pomeroy, J.M., and H. Grube, *"HCI potential energy sputtering measured with magnetic tunnel junctions,"* Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms, 2009. 267(4): p. 642-645.

Pomeroy, J.M., A.C. Perrella, H. Grube, and J.D. Gillaspy, *"Gold nanostructures created by highly charged ions,"* Physical Review B, 2007. 75: p. 241409R.

Pomeroy, J.M., H. Grube, A.C. Perrella, C.E. Sosolik, and J.D. Gillaspy, *"Transport and STM measurements of HCI modified materials,"* Nuclear Instruments & Methods in Physics Research Section B-Beam Interactions with Materials and Atoms, 2007. 256(1): p. 319-323.

Pomeroy, J.M., H. Grube, A.C. Perrella, and J.D. Gillaspy, *"Selectable resistance-area product by dilute highly charged ion irradiation,"* Applied Physics Letters, 2007. 91(7): p. 073506.

Pomeroy, J.M., H. Grube, A.C. Perrella, and J.D. Gillaspy, *"STM and transport measurements of highly charged ion modified materials. Nuclear Instruments & Methods in Physics Research Section B-Beam Interactions with Materials and Atoms,"* 2007. 258: p. 189-193.

Pomeroy, J.M., H. Grube, and A.C. Perrella, *"Spatial and electronic characterization of nano-features created by highly charged ions,"* Radiation Effects and Defects in Solids, 2007. 162(7-8): p. 473-481.

Grube, H., J.M. Pomeroy, A.C. Perrella, and J.D. Gillaspy, *"Highly Charged Ion Modified Magnetic Tunnel Junctions,"* Materials Research Society Symposium Proceedings, 2007. 960: p. 0960-N08-02.

BioElectronics Metrology

Technical Contacts:
D. R. Reyes
J. Hong
M. Gaitan

Goals

There is rapidly growing interest in the application of microelectronics and integrated circuit-based fabrication methods to manipulate and monitor biological processes. This emerging field of bioelectronics will require new competencies in the NIST laboratories to support metrology and standardization. Our goal over the next five years is to develop an internal competency in this field and to establish links with industrial partners in order to position NIST to coordinate the development of a bioelectronics metrology roadmap. Towards this end, we are developing a versatile bioelectronic platform with integrated electronic and microfluidic components that will enable a broad range of quantitative cellular assays, ultimately at the single-cell level. We will characterize the performance of the platform and then use it in collaboration with stake holders to study single-cell response to various toxins. These measurement methods will also facilitate fundamental understanding of the behavior of heterogeneous cell populations and cellular interactions, and will enhance NIST's capabilities to address emerging measurement needs for the medical and pharmaceutical industries. This effort will result in new metrology tools and test methods to support growing commercial industries that use high throughput methods for determining drug efficacy and toxicity.

Customer Needs

Cell-based assays are a primary tool used by the pharmaceutical industry to measure therapeutic drug efficacy and cytotoxicity. These time-consuming and labor-intensive assays currently involve millions of cells in each culture reservoir. This leads to some inherent measurement biases since the collective response only represents the average for the whole population and, for example, cells at different stages of development will respond differently to stimuli. A true paradigm shift is to utilize micro- and nano-fabrication technologies to perform these experiments on single cells or small cell clusters in continuous flow microfluidic systems with integrated microsensors and MEMS. Single-cell assays will isolate the parameters affecting cell response and allow the various subpopulations present in bulk cultures to be distinguished. Single-cell assays, when multiplexed, will allow for more rapid identification of drugs and drug targets.

Technical Strategy

Recent scientific reports reference describe the ability to stimulate electronically and probe single cell activity and to transport, sort, and position single cells. These capabilities have resulted in significant advances in biological sciences and medicine. An excellent example is patch clamp technology that has revolutionized the field of electrophysiology. Advances in microfabrication methods have recently led to the development of patch clamp arrays and other automated on-chip techniques; however, the widespread adoption of more complex integrated systems for biologically relevant measurements continues to face technological hurdles. These include complicated materials integration issues (maintaining a biocompatible environment for cells within the in-vitro measurement systems, developing stable and drift-free electrodes for accurate measurements in varied buffer solutions, etc.) the difficulty of accurately determining the electrical/electromagnetic response of integrated electronic/MEMS/fluidic systems, and issues related to reproducible fabrication of integrated devices. By addressing these critical measurement infrastructure needs, NIST will accelerate the development of powerful new bioelectronic platforms and techniques.

Our technical approach is to integrate microelectronic, MEMS, and microfluidic systems with cells to achieve a new level of control over the electronic/biological interfaces under study. We will develop methods to adhere and grow cells in defined patterns in a biological hybrid in-vitro environment that incorporates microelectronic circuits, both electrochemical and RF, to stimulate and sense cell activity. Microchannel networks will be used to transport the biological specimens to exact locations and to deliver precise amounts of chemicals or drugs to the local cellular environment. These techniques will allow us to apply precise electrical, electromagnetic, and chemical stimulation to the cells and to measure their metabolic, electrical, and physiological responses. We focused our initial research efforts on the study of retinal (neuronal)

cells, and currently, we are working with other mammalian cells such as fibroblasts (NIH-3T3) and epithelial cells, specifically embryonal carcinoma P19 cells.

DELIVERABLES:

- Investigate cell viability on natural occurring, synthetic and hybrid cell adhesive polymeric surfaces after exposure to dielectrophoretic conditions, to produce a system capable of long-term cell viability. 1Q 2010
- Assess the effects of dielectrophoresis (DEP) conditions on cells after exposure to sucrose and electric fields in a system that incorporates the polymeric cell adhesive material, studied in the previous quarter, with DEP trapping forces. 2Q2010
- Develop a platform comprising electronic cell manipulation (DEP) and a microenvironment capable of long-term cell experimentation for applications such as cell differentiation. 3Q 2010
- Assess the robustness of the DEP/microfluidic platform. 4Q 2010

We have designed and microfabricated devices that enable us to trap and pattern cells instantaneously using electronic tools and polymeric surfaces. The system combines microfluidic networks with indium tin oxide electrodes (ITO) and hybrid cell adhesion surfaces to obtain a device capable of trapping cells dielectrophoretically, while holding them in position after dielectrophoresis (DEP) conditions are removed. The purpose of this device is to pattern cells electronically, expose them selectively to chemical or electrical stimuli, and study them for long-term periods. Long-term experiments are necessary when desired cell studies, such as cell differentiation, require long-term exposure to morphogens (a differentiation signaling molecule) and, therefore, viable cells for more than 2 to 3 days. This platform is built by photolithographically patterning ITO electrodes on a glass substrate. Then, the hybrid cell adhesive material (HCAM) is deposited. The HCAM is comprised of 4 layers of polyelectrolytes followed by a layer of fibronectin, and ending with a layer of the cationic polyelectrolyte polyallyl amine hydrochloride (PAH). The device is sealed using a microchannel network made from polydimethyl siloxane (PDMS) that is bound to the glass/ITO substrate. DEP trapping is then carried out by resuspending cells in sucrose and allowing them to flow over the electrodes in the microchannel. Trapping occurs when the ITO electrodes are energized, at the optimal frequency, and the P19 cells flow at distance where they can sense the electric fields. Once the cells have adhered to the HCAM, the medium in the system can be changed from sucrose to cell growth medium. The P19 cells that were trapped using the DEP forces and the HCAM will remain anchored on the surface when the exchange of media occurs. P19 cells have shown to be viable for 6 to 8 days, and we have observed that the HCAM allows not only for the successful adhesion and proliferation of cells, but also for the differentiation of P19 cells into neuron-like cells. Assessing the optimum DEP device conditions for long-term cellular experiments would render this type of bioelectronic platform more accessible and more appealing to researchers not only inside NIST, but also to the biomedical electronic industries as well as researchers in the academia.

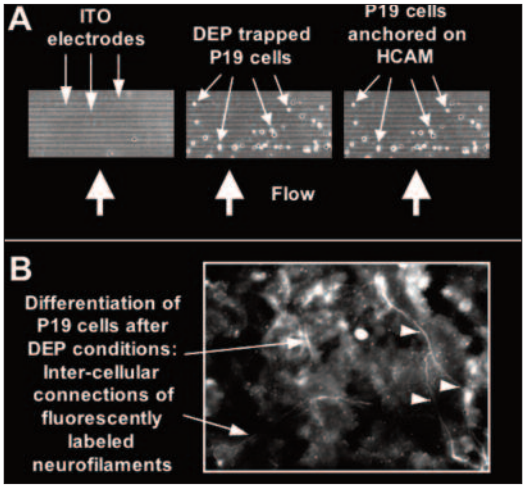


Figure 1. A) Images of DEP ITO electrodes before (left panel), during (middle panel) and after (right panel) the trapping of P19 cells under constant flow in microfluidic channels. DEP forces were used to first attract the cells onto the surface (middle panel). The hybrid cell adhesive material (HCAM) then holds the cells in place after the DEP forces are removed (right panel). The sucrose is exchanged with cell growth media and the P19 cells remain attached on the HCAM surface. B) P19 cells on the HCAM were cultured after seeding in sucrose (a low conductivity medium needed for DEP trapping to occur) and later replaced with cell culture medium. The cells were induced and differentiation occurred 6 to 8 days after the induction process was initiated. The image shows immunostained neurofilament processes (see arrows and arrowheads) that formed after differentiation, and their connections between cells.

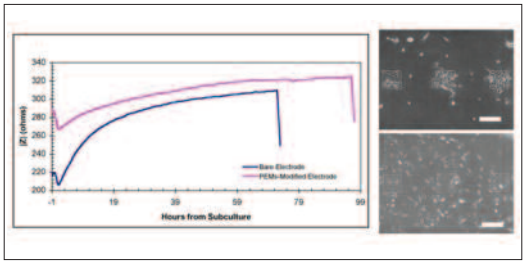


Figure 2. Magnitude of impedance of NIH-3T3 fibroblast cell growth on unmodified (blue line) and EMs-modified devices (red line) at 1000 Hz. The sharp decrease in impedance observed in both curves denote the detachment of NIH-3T3 fibroblast cells from the electrode surface after trypsin addition. (Right panel) NIH-3T3 fibroblast cells growing on unmodified gold electrodes (top) and PEMs-modified electrodes (bottom).

We developed a method to monitor NIH-3T3 fibroblast cell growth on gold electrodes using impedance spectroscopy. In this measurement technique, individual cells are represented as resistive and capacitive elements, which increase the impedance of the system as the number of cells increase. The two-electrode system was fabricated using photolithographic techniques and is comprised of thin-film gold electrodes with an underlying TiW adhesion layer. The system was then passivated with an oxide layer, which was etched through to define and expose the electrode active areas. Fibroblast cells (NIH-3T3) were able to grow directly onto the gold surface, and as they adhered and multiplied, the impedance of the system increased. Cells preferentially grew on the bare gold surface and not on the oxide. However, the oxide surface can be rendered biocompatible with the use of polyelectrolyte multilayers (PEMs), leading to successful measurements of cell growth with impedance spectroscopy (Fig. 1). Thus, the fabricated cell confluence detector demonstrates the ability to monitor cell adhesion and growth with impedance measurements. Future work will focus on the use of this system to monitor cytotoxic effect, of a variety of chemicals, using impedance spectroscopy to detect cell detachment from the surface.

Rapid temperature cycling of fluids is essential for increasing the throughput of chemical and biochemical processes and chemical synthesis such as polymerase chain reaction (PCR). In micro total analysis systems (μTAS), temperature cycling is typically implemented by external heating blocks or by integrated microresistive heating elements (microreactors). Our new approach for temperature cycling of microfluidic systems is based on delivering microwave heating energy using a microwave transmission line. A microwave coplanar waveguide is integrated with a surface mounted elastomeric microfluidic channel. This approach will have application to microwave assisted chemistries, which have recently been shown (in macro-scale devices) to have several advantages over conventional resistive heating approaches. These advantages include the ability to deliver heat directly to the fluid (and not to the surrounding medium), requiring lower temperatures to implement a chemical reaction and exhibitingof more uniform heating profiles. Recently, we have demonstrated, in a different microchip format, the use of microwave heating for the amplification of human DNA (PCR). We are currently working towards the integration of other processes, such as cell lysis and DNA extraction, into a microfluidic system.

Publications

G. I. Mijares, D. R. Reyes, J. Geist, M. Gaitan "Polyelectrolyte Multilayer-Treated Electrodes for Real-Time Electronic Sensing Cell Proliferation", Journal of Research, 115, 63-71, 2010.

G. Crivat, S. M. Da Silva, D. R. Reyes, L. E. Locascio, M. Gaitan, N. Rosenzweig, Z. Rosenzweig "Quantum Dot FRET-Based Probes in Thin Films Grown in Microfluidic Channels" J. Amer. Chem. Soc. 132 (5): 1460-1461, 2010.

J. J. Shah, M. Gaitan, J. Geist "Generalized Temperature Measurement Equations for Rhodamine B Dye Solution and Its Application to Microfluidics" Anal. Chem. 81 (19): 8260-8263, 2009.

D. R. Reyes, G. I. Mijares, K. A. Briggman, J. Geist and M. Gaitan "Electrical Manipulation of Gold Nanoparticles for Microfluidic Applications," Proc. MicroTAS 2008 Conference, San Diego, CA, pp. 233-235, 2008.

B. J. Nablo, K. M. Halverson, J. W. F. Robertson, T. L. Nguyen, R. G. Panchal, R. Gussio, S. Bavari, O. V. Krasilnikov, J. J. Kasianowicz. "Sizing the Bacillus anthracis PA(63) channel with nonelectrolyte poly(ethylene glycols)," Biophysical J., 95, 1157-1164, 2008.

L.P.Hromada, Jr., B.J. Nablo, J.J. Kasianowicz, M.A. Gaitan and D.L. DeVoe. "Single molecule measurements within individual membrane-bound ion channels using a polymer-based bilayer lipid membrane chip," Lab Chip, 8, 602–608, 2008.

J. J. Shah, S. G. Sundaresan, D. R. Reyes, J. Geist, M. V. Rao, M. Gaitan, “Continuous-wave Microwave Dielectric Heating of Fluids in Integrated Microfluidic System,” J. Micromechanics and Microengineering 17, 2224-2230, 2007.

P.-A. Auroux, D. R. Reyes, J. J. Shah, M. Gaitan, “Fast and High Efficient Microfluidic PCR by Microwave Dielectric Heating,” In Proceedings of Micro Total Analysis Systems 2007, Chemical and Biological Microsystems Society, Paris, France, pp 1237-1239, 2007.

J. W. F Robertson, C.G. Rodrigues, V. M. Stanford, K. Rubinson, O. V. Krasilnikov and J. J. Kasianowicz. “Single molecule mass spectrometry in solution using solitary nanopores,” Proc. Natl. Acad. Sci. (USA), 104, 8207-8211, 2007.

System Design and Test Metrology Program

Lead counts of several thousand per chip and test frequencies in the microwave regime challenge current test methodologies. The addition of new functions to provide system on-chip solution poses additional testing challenges. The overall task is to develop test methodologies to address these new requirements.

Accurate at-speed test methodology of digital integrated circuits is a critical requirement. Traditional methods utilizing integrated circuit (IC) contact probing technology requires large contact pads incompatible with current IC designs. The development of alternative probing approaches through noncontact and intermittent probing techniques appear very promising. However, to implement these techniques, solving the at-speed test calibration issues is crucial. With the challenges facing designers and the rising costs of development, it is essential to develop accurate testing strategies.

Temperature Sensor Metrology And BIST

Technical Contacts:
M. Y. Afridi
J. Geist

"For this technology (microhotplate-based gas-sensor) to be successful, temperature control is of the highest importance."

Charles J. Taylor

Goals

The purpose of this project is to develop metrology needed for microhotplate temperature sensors that are compatible with standard CMOS technologies and also provide an interface for on-chip built-in self test (BIST) for applications requiring microhotplate integrity check and self calibration. Polysilicon or aluminum layers which are readily available in standard CMOS technologies are not suitable for long-term reliable temperature measurements due to drift in TCR value at high temperatures (250 ºC to 400 ºC). On the other hand, platinum thin film temperature sensors, which are not available in standard CMOS technologies, exhibit excellent stability over a wide temperature range, -200 ºC to 650 ºC. There is a need to develop new post-processing steps to integrate platinum-based temperature sensors into a standard CMOS microhotplate to measure microhotplate temperature, to demonstrate that the resulting temperature sensors are sufficiently stable to be accurately calibrated, and to adapt them to BIST.

Customer Needs

The customer will be any organization that requires accurate microhotplate temperatures above 250 ºC. For instance, accurate microhotplate temperature measurements are crucial for the discrimination and quantification of gas species by low-cost, microhotplate-based, metal-oxide gas sensors. The fabrication and calibration methods developed as a result of this work will be essential for the realization of many homeland security and military objectives.

Professor Charles J. Taylor of Pomona College said:

"Molecular chemisorption and chemical reactions taking place on the gas-sensor surface change the electrical properties of the sensing film, thus providing an opportunity to identify an analyte and to determine its concentration. Since chemisorption and surface reactions are temperature dependent, it is possible to tune sensor selectivity and sensitivity by controlling operating temperature. Further-more, using temperature-programmed sensing, it is possible to identify analytes based on matching data acquired at multiple temperatures to "molecular fingerprints". Without good temperature control, the matches may be ambiguous and the identity of the analyte may be lost. In addition, any studies performed where temperature is a variable in the experiment such as the deposition of materials by chemical vapor deposition onto the microhotplates, would be more difficult to reproduce without adequate temperature control."

Technical Strategy

To achieve the project goals, CMOS compatible post processing techniques will be developed to integrate different platinum-based temperature sensors including resistive and platinum-rhodium thermocouples into the microhotplate structures. Also, microhotplate BIST and calibration procedures will be developed and tested.

1. A series of standard CMOS microhotplates with integrated platinum temperature sensors will be developed and tested. The Microhotplate design will be compatible with BIST operation. The micro-hotplates will be fabricated in 1.5 μm CMOS technology through the MOSIS-AMI foundry service, post-processed in the NIST Nano-Fabrication facility, and calibrated and characterized in the EEEL SED Gas Sensor Characterization laboratory.

DELIVERABLES:

- CMOS microhotplate test structures with integrated platinum-based temperature sensors. 4Q 2008 1.

2. To develop and test BIST procedures for microhotplate integrity test and temperature calibrations.

DELIVERABLES:

- A report describing BIST performance and calibration results for the microhotplate temperature sensors. 2Q 2009

3. An enhanced microhotplate characterization laboratory will be set up and configured to test and calibrate microhotplate tempera-

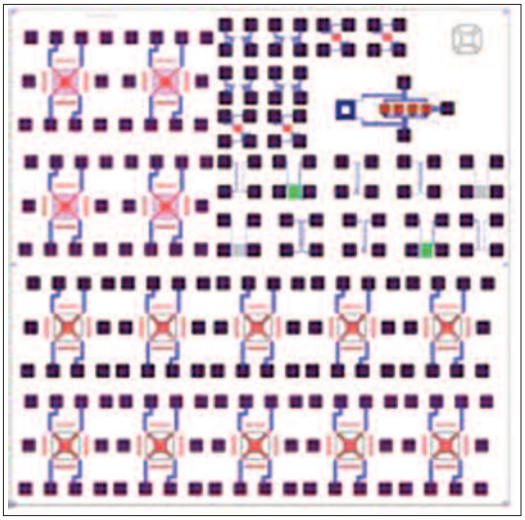


Figure 1. Layout of test structures for testing complementary approaches to microhotplate temperature sensor Built-In Self Test (BIST).

ture sensors and to measure BIST performance.

DELIVERABLES:

- A well equipped and automated laboratory setup for microhotplate characterization. 4Q 2009

4. Design analog and digital circuits to integrate control, measure, and BIST functionality for the microhotplate platform.

DELIVERABLES:

- Integrated microhotplate test structures with on-chip digital and analog electronics to control, measure, and perform BIST functionality test. 4Q 2010

5. Design and implement the microhotplate test structures in a submicron standard CMOS technology and test temperature-sensor BIST functionality.

DELIVERABLES:

- An integrated submicron CMOS temperature sensor BIST chip and its performance results. 4Q 2011

Accomplishments

■ A test chip was designed and submitted to be fabricated in a standard 1.5 micrometer CMOS technology. The chip includes complementary temperature sensor designs to be evaluated for their performance, stability, and BIST functionality.

■ CMOS microhotplate test structures chips were fabricated, post-processed, and tested for design integrity. The microhotplates were further post processed to integrate different serpentine design patterns to produce platinum resistive temperature sensors.

■ A preliminary design of platinum/rhodium-based thermocouple, over a microhotplate structure, was implemented and tested. A rhodium film was deposited through a shadow mask over a platinum electrode originally intended as a gas-sensor film electrode to create a platinum-rhodium thermocouple on a microhotplate as shown in Fig. 3 and Fig.4. The platinum/rhodium thermocouple and the thermal efficiency of the microhotplate were calibrated as microhotplate temperature sensors and the long-term stability of the calibrations verified by comparing the temperature measured by these two independent temperature sensors. The results showed that microhotplate thermal efficiency in conjunction with a thermocouple is

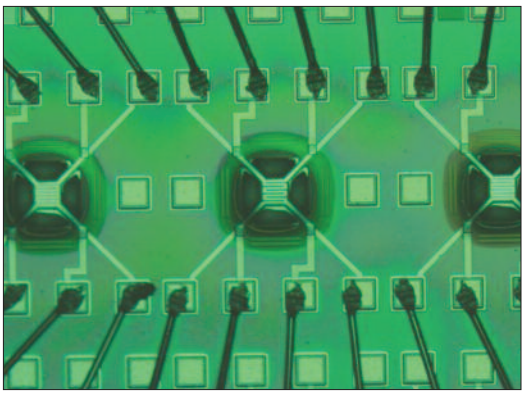


Figure 2. A micrograph of a wire-bonded chip showing different serpentine platinum resistive temperature sensors over microhotplate structures.

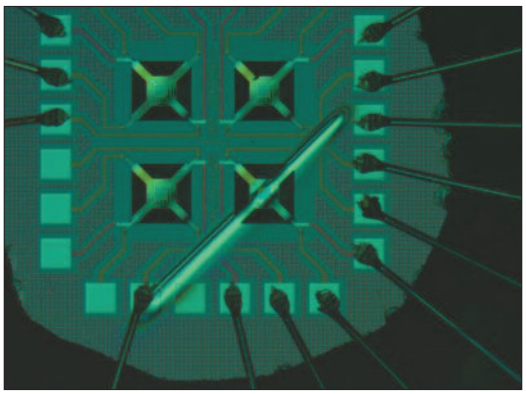


Figure 3. A micrograph of a platinum/rhodium-base thermocouple chip.

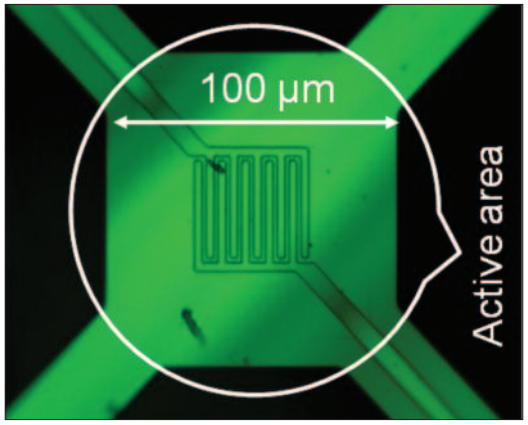


Figure 4. A close-up view of the interdigitated platinum electrode that can be seen through the rhodium film that was used to form a thermocouple on the active area of the microhotplate.

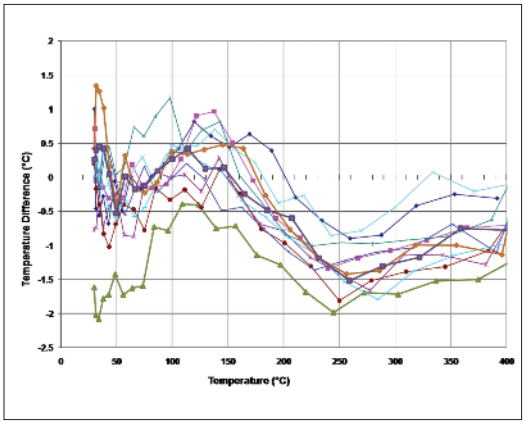


Figure 5. Differences between the microhotplate temperatures based on the long-term calibration of the platinum-rhodium thermocouple and those based on the long-term calibration of the thermal resistance of the heater legs at 11 different times during a period of 3 months.

suitable for implementing microhotplate temperature sensor BIST as shown in Fig. 5.

■ A NIST Tech Beat article was published and was also posted as top news on the Commerce Department main web page:

"Novel Temperature Calibration Improves NIST Microhotplate Technology

Researchers at the National Institute of Standards and Technology (NIST) have developed a new calibration technique that will improve the reliability and stability of one of NIST's most versatile technologies, the microhotplate. The novel NIST device is being developed as the foundation for miniature yet highly accurate gas sensors that can detect chemical and biological agents, industrial leaks and even signs of extra-terrestrial life from aboard a planetary probe…"

Publications

Jon Geist and Muhammad Afridi, *"Temperature-Programmed Gas-Sensing With Microhotplates: an Opportunity to Enhance Microelectronic Gas Sensor Metrology,"* CP1173, Frontiers of Characterization and Metrology for Nanoelectronics: pp 207-211, 2009.

Afridi, M.; Montgomery, C.B.; Cooper-Balis, E.; Semancik, S.; Kreider, K.G.; Geist, J., *"Analog BIST Functionality for Microhotplate Temperature Sensors,"* Electron Device Letters, IEEE , vol.30, no.9, pp.928-930, Sept. 2009.

M. Yaqub Afridi, Christopher B. Montgomery, Elliott Cooper-Balis, Steve Semancik, Jon Geist, and Alim Fatah, *"Cmos Microhotplate Technology For Chemical And Biological Agent Detection,"* Chemical and Biological Defense Physical Science & Technology Conference 17-21 November 2008 -New Orleans, Louisiana.

J. Geist, M. Afridi, A. Varma and A. Hefner, *"Simple Thermal-Efficiency model for CMOS-Microhotplate Design,"* in Journal of Research at NIST, Vol 111(3), pp. 243, 2006.

M. Afridi, A. Hefner, J. Geist, C. Ellenwood, A. Varma, B. Jacob, *"Microhotplate-Based Sensor Platform for Submicron SoC Designs"* IEEE International Semiconductor Device Research Symposium (ISDRS), pp. 500-501, 2005.

Yaqub Afridi, Allen Hefner, Colleen Ellenwood, Richard Cavicchi, Stephen Semancik *"Characterization System for Embedded Gas-sensor Systems-on-a-Chip"* GOMACTECH 2005, pp. 94-97, 2005.

At-Speed Test of Digital Integrated Circuits

Technical Contacts:
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P. Kabos
P. Hale

"As electronic devices shrink into the nanometer size scales and integrated circuits operate at multi-GHz clock rates, probing their internal characteristics is becoming both more critical and far more difficult than ever before."

Travis M. Eiles, Ph.D.
Intel Corp.

Goals

Develop and demonstrate metrology for the at-speed tests of digital integrated circuits and printed circuit boards. The program will focus on the essential metrology issues of at-speed digital integrated circuit tests. It will apply its results to characterizing and calibrating probes as well as development of broadband metrology tools at both the micrometer and nanometer scales. This includes scanning probe microscopes (SPMs) capable of characterization of near field distribution, doping profiles, defects, complex heterostructured materials at nanoscale, and influence of advanced processing (e.g. FIB) on performance of at-speed electronics based on novel materials and technologies for extended CMOS and beyond CMOS electronics. The program will also demonstrate methods for applying probe calibrations in the time domain for eye testing with well quantified performance.

Customer Needs

In the device debug and characterization world, a key challenge is the development of diagnostic tools, particularly for timing information. The 2007 International Technology Roadmap for Semiconductors (ITRS) Metrology section points out that "Metrology was the first semiconductor technology area to work routinely in the area of nanoelectronics. This is because a variation in features size one tenth of the nominal dimension often results in significant changes in device properties." The 2009 ITRS elaborates, "Metrology is needed to characterize the atomic and nanoscopic 3D structure, composition, and properties of emerging research materials (ERM). Also needed are non-destructive methods for characterizing the local nanoscopic structure of embedded materials, interfaces and defects, as well as platforms that enable simultaneous measurement of complex nanoscopic properties." (ITRS ERM 2009, p. 36).

On the subject of interconnects, the 2007 roadmap states "Interconnects, including all of the IC structures necessary to connect from silicon to the boards and boxes of the outside world, have become a potential performance roadblock for the continuation of the semiconductor industry on the Moore's Law curve."

With the increasing reduction in feature (and defect) sizes well below optical wavelengths, rapidly increasing failure analysis throughput times, reduction in failure analysis efficiency, and approaching practical physical limits to other physical techniques (pica, laser probes), the industry is reaching a strategic inflection point for the semiconductor business where the criticality of design for test and test enabled diagnostics and yield learning becomes paramount (2009 ITRS Test and Test Equipment Section, page 7). Detecting systemic defects is one of the difficult challenges. Electrical test-based diagnostics and learning is becoming increasingly more important. Parametric related feedback is needed for: (1) device and interconnect parameters; and (2) design-process interactions. To keep pace, improvements and breakthroughs in existing tools/techniques is necessary. In-chamber (SEM) and atomic-force-microscope probing at the nanoscale are required to characterize minimum-sized transistors (4 probe points) and SRAM cells (5 or more points) at first contact level are required for circuit probing. The socket and wafer probe are also serious bandwidth bottlenecks for multi-gigahertz testing and additional R&D is needed in these areas. For key challenges the research and development is urgently required to bring to the market cost-effective probe technologies directed at trends in product offerings and the testing environment. One of the challenges is that the traditional probe technologies do not have the necessary electrical bandwidth for higher frequency devices. At the top end are RF devices, requiring up to 40 GHz.

The critical topics in 2009 ITRS Metrology section are: 3D metrology with reference methods, including film thickness and profile; composition and stress in e.g. burried channels, standardization of measurements, properties of low dimensional materials, microscopy and feature/size function, time resolved magnetic measurements, dimensional and temporal resolution of local structures and dynamics. There Is no single technique that would cover all the required metrolog-

ical challenges. We are focusing our metrology methods on development of nondestructive tools for materials characterization, control of interfacial layers, dopant positions, defects, and atomic concentrations relative to device dimensions working at their operating frequencies. We are developing alternative scanning probing approaches that use high-impedance probes, noncontact probes, atomic-force and scanning tunneling microscopes that detect the device response to either electric or magnetic fields. However, while the uncalibrated field measurements performed by these probing systems are suitable for field mapping the device design requires quantitative information at these scales. This is a very difficult task, whichh we are trying to address.

Solving the critical at-speed test calibration issues will add enormous value to the probing systems currently being used or developed for high-performance digital integrated circuits. Developing characterization and calibration methods for the developed metrology will help speed up the development and implementation of these new measurement tools, and so create a new paradigm for the at-speed test of high-speed digital integrated circuits.

Technical Strategy

In collaboration with the relevant industrial partners we are developing calibration artifacts with precisely known high-frequency voltages and circuits suitable for characterizing and calibrating near field scanning probe systems and samplers of all types. We are focusing on fundamental calibration issues: transforming the response of the probes to the electric and magnetic fields into accurate voltages and currents inside the measurement system and/or circuit. Figure 1 shows a result of the high-speed metrology we have developed, an on-chip waveform measurement to 200 GHz.

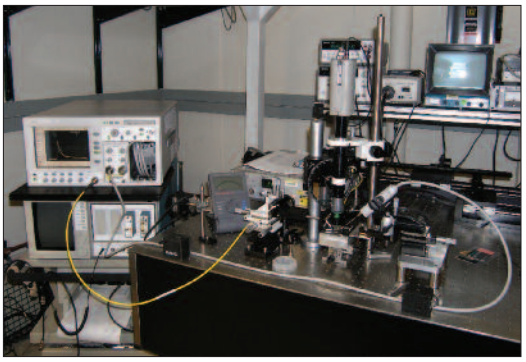

Figure 1. Three on-chip waveform measurements performed with our electro-optic sampling system.

We will first apply the characterization and calibration procedures to conventional high-impedance probes. To facilitate the development and test of electric and magnetic probes with nanoscale resolution, we have constructed a universal SPM test bed for these probes. We are applying our characterization procedures to miniature SPM probes suspended on custom cantilevers designed for high frequency measurements on the nanoscale. Finally, we plan to tie our metrology back to fully characterized electro-optic sampling measurements.

Traceability for frequency response is provided to 110 GHz in coaxial transmission media and beyond on wafer through the NIST electro-optic sampling system. After calibration and correction, the measurement is traceable to fundamental physical principles. For accurate digital signal characterization, loss and mismatch effects of cables, probes and test fixtures must be "de-embedded". This technique is common in the microwave (frequency domain) world, but can cause uncharacterized distortions for time-domain waveforms such as the eye patterns. We will develop standard metrics for characterizing the accuracy of de-embedding loss and mismatch in time-domain waveforms. We will then characterize standard practices for optimizing the procedure of de-embedding .

Accomplishments

We have demonstrated a novel frequency-domain method for measuring time-domain delay of dispersive calibration artifacts for differential delay. This frequency-domain approach can also account for pulse shape and source and load impedance effects. We have also demonstrated a method to propagate uncertainty in the NIST Timebase Calibration Software through to various pulse parameters and have demonstrated differential delay calibrations of a dispersive calibration artifact with < 1 ps standard uncertainty.

We have developed, fabricated, and tested a non-invasive AFM scanning probe for measuring local microwave power.

We have developed a method of characterizing and calibrating conventional high-impedance probes for low-invasive waveform measurements.

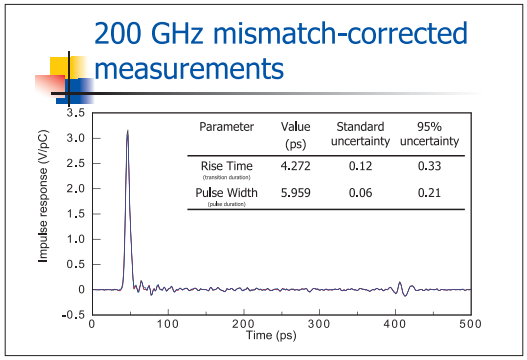

Figure 2. Measurement system used to verify the functionality of our photoconductive switches.

We have applied our high-impedance-probe characterization method to a probe mounted on an atomic-force microscope.

We have constructed an SPM universal test bed.

We have demonstrated a calibrated measurement of an on-wafer pulsed waveform up to 200 GHz using electro-optic sampling.

We have developed a procedure for testing high-impedance probes directly on our electrooptic sampling system. This system has a calibrated bandwidth of 200 GHz.

We have demonstrated a method for correcting oscilloscope time-base jitter, drift, and distortion.

We have fabricated fast photoconductive switches and demonstrated a rise time of better than 5 ps, largely exceeding our goal of constructing generator chips useable to 50 GHz. We will use these to construct a portable and calibrateable on-chip pulse source for characterizing high-impedance probes at the micrometer and nanometer length scales, Fig. 2.

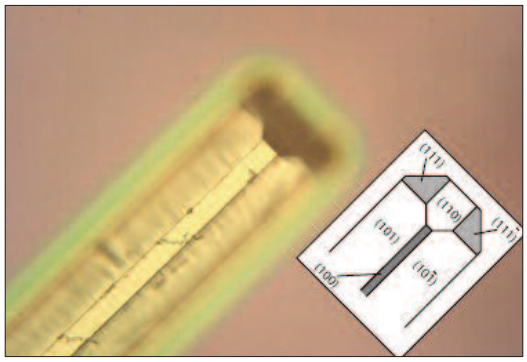

Figure 3. The Fiber-optic trench with integrated 45-degree mirror.

We developed the fabrication process for creating the MEMS chips with integrated 45-degree mirrors and trenches for fiber alignment, Fig. 3.

We assembled the fiber optic interferometer for the measurement of the deflection of the cantilevers including the thermal feedback control.

We built a magneto-optic Kerr effect setup for imaging of current distributions in microwave circuits.

We modified a commercial AFM for measurement of mechanical resonances of micro/nano oscillators.

In collaboration with Agilent Technologies we developd the calibration procedure for calibration of the capacitance measurements with scanning microwave microscope (Figure 4).

Publications

P. D. Hale and A. Dienstfrey, "Waveform metrology and a quantitative study of regularized deconvolution," To appear in Instrum. Meas. Technol. Conf. 2010, I2MTC '10, IEEE.

J. A. Jargon, P. D. Hale, and C. M. Wang, "Correcting sampling oscilloscope timebase errors with a passively mode-locked laser phase-locked to a microwave oscillator," IEEE Trans. Instrum. Meas., vol. 59, no. 4, pp. 916-922, Apr. 2010.

P. D. Hale, A. Dienstfrey, C. M. Wang, D. F. Williams, A. Lewandowski, D. A. Keenan, and T. S. Clement, "Traceable waveform calibration with a covariance-based uncertainty analysis," IEEE Trans. Instrum. Meas., vol. 58, no. 10, pp. 3554-3568, Oct. 2009.

C. M. Wang, P. D. Hale, and D. F. Williams, "Uncertainty of timebase corrections," IEEE Trans. Instrum. Meas., vol. 58, no. 10, pp. 3468-3472, Oct. 2009.

P. D. Hale and C.M. Wang, "Calculation of pulse parameters and propagation of uncertainty," IEEE Trans. Instrum. Meas., vol. 58, no. 3, pp.639-648, Mar. 2009.

J. Jargon, C. M. Wang, and P. D. Hale, "A robust algorithm for eye-diagram analysis," IEEE J. Lightwave Technol. vol 26, no. 21, pp3592-3600, Nov. 1, 2008.

T.M. Wallis, H. Nembach, A. Imtiaz, D. Gu, Kabos, K. Bertness, N. Sanford, P. Blanchard, "Broadband Characterization of Nanowires," CPEM '08 Broomfield Colorado June 2008

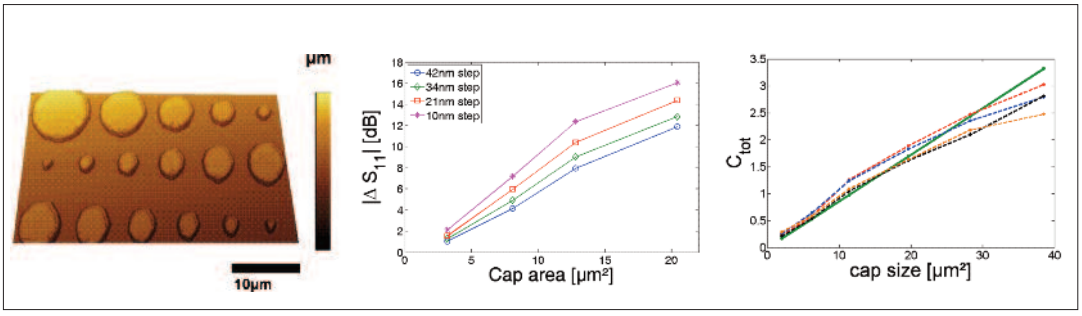

Figure 4. Left AFM image of part of the NIST chip designed for Scanning Microwave Microscope calibration. Measured reflection coefficient as a function of the cap size (middle), and de-embedded total capacitance as a

Arkadiusz Lewandowski, Dennis LeGolvan, T. Mitch Wallis, Atif Imtiaz, and Pavel Kabos. "Measurement of Extreme Impedance" ARFTG conference proceedings, Seatle 2008

T. Mitch Wallis, Arkadiusz Lewandowski,"Statistical Measurement Techniques for Equivalent Source Mismatch of 1.85 mm Power Splitter" ARFTG conference proceedings 2008.

T. M. Wallis, A. Imtiaz, H. T. Nembach, P. Rice and P. Kabos, "Metrology for high frequency electronics," Proceedings of the 2007 International Conference on Frontiers of Characterization and Metrology for Nanoelectronics, pp. 525-529, Gaithersburg, MD, March 2007.

P. Rice, T. M. Wallis, S. E. Russek, and P. Kabos, "Broadband Electrical Characterization of Multiwalled Carbon Nanotubes and Contacts," Nano Letters, 7, 1076 (2007).

A.Imtiaz, T. Baldwin, H. T. Nembach, T. M. Wallis, and P.Kabos, "Near-field microwave microscope measurements to characterize bulk material properties," Applied Physics Letters, 90, 243105 (2007).

Simone Lee, T. Mitch Wallis, John Moreland, Pavel Kabos, and Y. C. Lee, "Asymmetric Dielectric Trilayer Cantilever Probe for Calorimetric High-Frequency Field Imaging," IEEE JMEMS 16, pp. 78 -86, (2007).

T. S. Clement, P. D. Hale, D. F. Williams, C. M. Wang, A. Dienstfrey, and D. A. Keenan, "Calibration of sampling oscilloscopes with high-speed diodes," IEEE Trans. Microwave Theory and Tech., Vol. 54, pp. 3173-3181, Aug. 2006.

A. Dienstfrey, P. D. Hale, D. A. Keenan, T. S. Clement, and D. F. Williams, "Minimum-phase calibration of sampling oscilloscopes," IEEE Trans. Microwave Theory and Tech., Vol 54, pp. 3197-3208, Aug. 2006.

D. F. Williams, A. Lewandowski, T. S. Clement, C. M. Wang, P. D. Hale, J. M. Morgan, D. A. Keenan, and A. Dienstfrey, "Covariance-based uncertainty analysis of the NIST electrooptic sampling system," IEEE Trans. Microwave Theory and Tech., Vol. 54, pp.418-491, Jan. 2006.

D. F. Williams, H. Khenissi, F. Ndagijimana, K. A. Remley, J. P. Dunsmore, P. D. Hale, C. M. Wang, and T. S. Clement, "Sampling-Oscilloscope Measurement of a Microwave Mixer with Single-Digit Phase Accuracy," IEEE Transactions on Microwave Theory and Techniques, Vol. 54, no. 3, pp. 1210-1217, Mar. 2006.

P. D. Hale, C. M. Wang, D. F. Williams, K. A. Remley, and J. Wepman, "Compensation of random and systematic timing errors in sampling Oscilloscopes," IEEE Transactions on Instrumentation and Measurement, Vol. 55, no. 6, pp. 2146-2154, Dec. 2006.

S. Lee, Y. C. Lee, T. M. Wallis, J. Moreland, and P. Kabos, "Near field imaging of high-frequency fields with calorimetric cantilever probes," Journal of Applied Physics, 99, pp. 08H306-1-08H306-3, (2006).

D. F. Williams, P. D. Hale, T. S. Clement, and J. M. Morgan, "Calibrated 200 GHz Waveform Measurement," IEEE Trans. Microwave Theory and Tech., April 2005.

T. M. Wallis, J. Moreland, W. Riddle, and P. Kabos, "Microwave power imaging with ferromagnetic calorimeter probes on bimaterial cantilevers," Journ. of Mag. and Magn. Mater, vol 286, pp. 320-323 (2005).

P. Kabos, T.M. Wallis, A. Imtiaz, A. Lewandowski, R. Ginley and D. LeGolvan, Dazhen Gu, Chin-Jen Chiang, Paul Rice, Ki-chul Kim, Dejan Filipovic, "Broadband Characterization of High-Impedance Nanoscale Systems,", Invited talk IMS, Boston, June 2009, USA.

P. Kabos, T.M. Wallis, A. Imtiaz, A. Lewandowski, R. Ginley and D. LeGolvan, Dazhen Gu, Chin-Jen Chiang, Paul Rice, Ki-chul Kim, Dejan Filipovic, "High Frequency metrology at nanoscale: Calibration, model validation and device charac-

terization," Invited talk at European Microwave Conference, September 2009, Rome, Italy.

Atif Imtiaz, Mitch Wallis, Sang H. Lim, Jonathan Chisum, Zoya Popovic and Pavel Kabos "Near-field Antenna as a Scanning Microwave Probe for Characterization of Materials and Devices,", Invited talk, European Conference on Antennas and Propagation, April 2010, Barcelona, Spain.

K. Kim, T.M.Wallis, P. Rice, C-J. Chiang, A. Imtiaz, P. Kabos, and D.S. Filipovic, "A framework for broadband characterization of individual nanowires," Microwave and Wireless Components Letters, 20, 178, (2010).

H.P. Huber, M. Moertelmaier, T.M. Wallis, C.J. Chiang, M. Hochleitner, A. Imtiaz,Y.J. Oh, K. Schilcher, M. Dieudonne, J. Smoliner, P. Hinterdorfer, S.J. Rosner, H. Tanbakuchi, P.Kabos, F. Kienberger "Calibrated nanoscale capacitance measurements using a scanning microwave Microscope," Submitter do Review of Scientific Instruments. (April 2010).

Thermal Measurements and Packaging Reliability

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B. Grummel
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Goals

Our goal is to provide the semiconductor industry with information, guidance, and tools necessary to characterize and model the behavior of features and interfaces in packaging and on-chip that are thermally stressed. Advanced temperature measurement methods are developed and transferred to industry to meet the need to characterize semiconductor device and package temperature with increased temporal and spatial resolution. Electro-thermal models and modeling methodologies are also developed and transferred to industry to meet the increased need to model the interaction of electrical and thermal behavior of the device and package.

Overcoming thermal limitations has recently become a major issue in CMOS-based microelectronic circuits because: (1) power levels in CPUs have reached the same levels as in power devices; (2) power density nonuniformities are leading to hot spots in microprocessors as well as power ICs; (3) new materials with different thermal properties are being introduced; (4) many new and future technologies (e.g., SOI, 3-D integration) tend to isolate power dissipating elements thermally; and (5) shrinking dimensions and increasing frequency of ICs are causing significant power dissipation in the interconnects. To address these issues, reliable methods for measuring and modeling the temperature distribution in ICs and power devices are required.

A broad range of temperature measurement techniques are investigated by this project and several unique temperature measurement system requirements have been identified and demonstrated by NIST. High speed transient thermal imaging methods are being developed for measuring localized heating effects at the semiconductor chip surface. This enables the measurement of transient heating events such as burst operation of IC Functional Unit Blocks (FUBs) and enables the measurement of transient current constriction failure events in RF and high power devices. This thermal imaging methodology can serve as a basis for measurement standards. Additionally, methods are being developed to evaluate the heat transfer across package layer interfaces using high-speed temperature sensitive parameter (TSP) measurements. This is important for in situ measurement of heat transfer performance degradation after various levels of thermal stress such as power cycling, thermal cycling and thermal shock.

Customer Needs

The trend in electronics is toward components of higher density and smaller size using less expensive materials. Materials used in packaging and interconnects are many and display a variety of thermal responses that are not always compatible. This makes interconnect lines and package interfaces particularly vulnerable to thermomechanical fatigue failures. This project seeks to offer support through modeling and verification of the thermal performance of devices and packages and the development of new thermal measurement methods to meet the needs of the semiconductor industry.

The 2009 ITRS Modeling and Simulation Executive Summary, p.60 states that:

- "The development of new modeling capability generally requires long-term research, and increasingly interdisciplinary activities, which can be carried out best in an academic or a laboratory setting. For this reason, a vigorous research effort at universities and independent research institutes is a prerequisite for success in the modeling area, together with a close cooperation with industry…"

- "Modeling and simulation is the virtual counterpart of semiconductor device and chip fabrication and characterization: Computer programs are used to predict … strain … of devices, their electrical performance and reliability, and finally the behavior of circuits and systems."

- "… reliability issues get more important at all levels of simulation and, moreover, reliability problems at device, circuit, or package level are partly based on details of fabrication processes and their variations…"

Temperature measurements for microelectronic devices are more important today than they ever

have been. It always has been true that extreme temperature places limits on the operating range of nearly all devices, but today, increasing power dissipation and power densities threaten to create temperatures that block continued progress according to "Moore's Law." Clearly, new and innovative methods for cooling chips and packages must be found along with new materials and circuit designs, and architectures for decreasing the power dissipation and operating temperature. Equally as clear, we must have accurate and well-understood methods for measuring the temperature of devices to aid in the development of these new techniques and materials.

The need to measure operating temperature of a semiconductor device can be divided into the following four broad categories: (1) predicting reliability or operating life of device, (2) measuring material/device thermal properties in situ, (3) confirming or determining the operating limits or thermal performance of a device, and (4) validating thermal models for device, chip, and system performance. Thermal measurements on small, <10 μm, structures are needed due to the high density of current and future interconnect and packaging designs. Heat transfer information at interfaces, such as those seen at solder/intermetallic interfaces and Direct Bonded Copper (DBC) isolation layer is needed for modeling of future package designs.

One of the challenges for the 2009 ITRS Modeling and Simulation has been specifically renamed to *"Electrical-thermal-mechanical modeling for interconnect and packaging". "Reliability Modeling"* has also been added in the Modeling and Simulation guide of the 2009 ITRS.

NIST first introduced the concept of dynamic electro-thermal semiconductor models and package thermal network component models in the early 1990s to address this need and this methodology has been used extensively by industry to model the behavior of a variety of semiconductor devices and packages.

The 2009 ITRS Design guide mentions:

- in *Design Challenge, Crosscutting Challenges* #4, p.5: "Issues include…thermal impact on device off-currents and interconnect resistivities, and substrate coupling. A basic Design Technology challenge is to improve characterization, modeling, analysis… at all levels of design."

- in *Cross-cut TWG Issues, Modeling and Simulation,* p.35: "Simulation should further contribute to the assessment of the impact of parasitics, delay variations, noise, and reliability issues, including thermal effects during operation."

The 2009 ITRS Modeling and Simulation Executive Summary mentions Interconnect Difficult Challenges in Table ITWG9, p.46:

- in *Achieving necessary reliability*: "New materials, structures, and processes create new chip reliability (electrical, thermal, and mechanical) exposure. Detecting, testing, modeling, and control of failure mechanisms will be key."

- in *Integration of new processes and structures, including interconnects for emerging devices*: "Combinations of materials and processes used to fabricate new structures create integration complexity. The increased number of levels exacerbate thermomechanical effects."

The 2009 ITRS Modeling and Simulation Executive Summary mentions *Assembly and Packaging Difficult Challenges* in Table ITWG11, p.50-51:

- in *Coordinated design tools and simulators to address chip, package, and substrate co-design*: " Integrated analysis tools for transient thermal analysis and integrated thermal mechanical analysis" and "Models for reliability prediction".

- in *High current density packages*: "Electromigration will become a more limiting factor. It must be addressed through materials changes together with thermal/mechanical reliability modeling" and "Thermal dissipation"

Measurement of localized and transient heating is also becoming increasingly important in high performance ICs as it is becoming prohibitive to remove the heat that would be dissipated if the entire IC was operated continuously at the full power density level. System techniques that dynamically operate all or part of the chip at reduced power, such as dynamic voltage scaling or clock

gating, require experimental evaluation of the rapid transient heating and thermal diffusion from locally heated FUBs.

As the power density of semiconductor devices continues to rise, modeling the interaction of electrical and thermal behavior of the device and package also increases in importance.

The 2009 ITRS Design guide, *Design Challenge, Crosscutting Challenges* #2-(2), p. 4 states that: "Increasing power densities worsen thermal impact on reliability and performance…"

Modeling transient heating effects has also become much more important in predicting the thermal cycling effect on reliability and in understanding the impact of dynamic power dissipation within devices.

The 2009 ITRS Modeling and Simulation guide, in *Electrical-thermal-mechanical- modeling for interconnections and packaging*, p.6, states that: "Performance and reliability of integrated circuits is increasingly affected by interconnects and packaging. Electrical, thermal, and mechanical properties highly interact with each other and must therefore be simulated together. Reliability issues requiring modeling include …, stress voiding, integrity and adhesion of thin films …, package fracture ... Thin stacked dies request new or largely extended simulation tools."

The 2009 ITRS Modeling and Simulation guide, in Interconnects and *Integrated Passives Modeling*, states that:

- (p.15) "This (interconnects) refers both to their electrical performance and to their reliability, and in turn requires coupled electrical, mechanical, and thermal simulation. … Both electrical performance and reliability are critically influenced by process conditions and material properties including the microstructure of copper and (porous) low-κ materials. … The modeling of the performance and reliability of interconnects is required."

- (p. 16) "Of high priority are the coupled thermal and mechanical performance properties of thin multi-layer films. …The mechanical properties of these thin films, such as fatigue, fracture, and stress voiding, also affect reliability performance. Thermal cycling can trigger fractures that may not be foreseen. … Simulation tools are needed to study these effects more effectively than by experiment alone. The change to low-κ dielectrics with low thermal conductivity has placed much more emphasis on combined electrical and thermal modeling in the suite of modeling and simulation tools needed for interconnect technology development. … Progress has been recently observed and will allow to acquire more predictive models."

- (p. 17) "Interconnect performance simulation is getting especially difficult because the problem widely spans in four respects, as follows:

  - o An increased coupling of electrical and thermal-mechanical simulation is necessary.

  - o The final target is performance and reliability at least at chip level.

  - o The various levels of interconnect simulation need suitably to be coupled with design in a bi-directional manner.

  - o Simultaneous simulation of interconnects and packaging becomes more important.

- (p.19) "The introduction of low-κ dielectrics with low thermal conductivity increases the need for thermal analysis. ICs generating increasing amounts of heat will transfer more of that heat to packages that will be challenged to dissipate it, and in turn the package will transfer heat to the system. This attribute also requires co-design tools that facilitate simultaneous analysis. Inherent and thermally induced mechanical stresses throughout the layer stack must be identified and modeled. The low-κ dielectrics often have reduced mechanical integrity, while at the same time thermal stresses are more severe. The stresses are especially enhanced with non-uniform heating induced by the die, by current bottlenecks in the ground and power planes, and with reduced thermal conductivity."

The 2009 ITRS Modeling and Simulation guide, in *Reliability Modeling*, p. 22, states that:

- "As reliability issues become more and more important for the semiconductor industry modeling is increasingly requested to provide de-

sign tools not only to achieve better device performance but also more robust reliability margins… Considerable amount of work has been done to address reliability issues of like low-k line-to-line insulation degradation under bias-temperature stress, thermal dissipation, thermo-mechanical mismatch with the surrounding materials, low yield strength leading to delamination, cracking and extrusion,… As the number of materials and interfaces increases, major long-term reliability hazards are related to thermal cycles, thermal dissipation, interfacial delamination, and thermo-mechanical mismatch within the package and with the assembly… the need for multiscale simulation methodologies is increasing."

Technical Strategy

1. Develop models for fundamental wear-out mechanisms in semiconductor packages. The increasing power density in semiconductor devices can lead to higher temperatures and wider temperature swings, which generate higher stresses and strains in the power module packages. These higher stresses degrade the packaging materials leading to both reduced package lifetime and higher thermal stresses on the die. Models for these failure mechanisms must be calibrated and validated, especially for new die attach materials and stack layer configurations.

DELIVERABLES:

- Establish multi-laboratory cooperation for advancement of fundamental understanding of semiconductor package wear-out mechanisms. 1Q 2010
- Develop generic predictive failure models for wire bonds, die attach interfaces, substrate interfaces. 2Q 2010

2. Outline metrology for data and verification of wear-out models. In order to obtain the necessary data to calibrate and validate the thermo-mechanical models, multiple power module samples must be exposed to accelerated test stressing at a variety of levels and ramp rates that replicate accelerated wear and aging of the materials in the power modules. Degradation of the modules under test will be assessed via a suite of electrical, thermal and physical measurements that are both non-destructive (e.g. acoustic microscopy, temperature-sensitive parameter measurements, etc.) and destructive (e.g. cross-sectional cutting for microscopic visual inspection) at intervals of thermal cycling. Correlations will be drawn between the physical observations of degradations, the thermal effects of that degradation, and the electrical impact of that degradation. To complete this task, it is crucial to delineate the appropriate steps to generate the desired effects and acquire results without damaging the devices prematurely and allowing maximum data acquisition through the test duration.

DELIVERABLES :

- Modify the unique NIST high-speed Thermal Shock/Thermal Cycling system to provide controlled variables necessary for failure model dependencies. 2Q 2010
- Perform Design-of-Experiments analysis to characterize full thermal cycling dependencies for die attach failure. 3Q 2010
- Develop monitoring methodology to assess degradation including thermal, electrical and other non-destructive analytical techniques. 4Q 2010
- Begin thermal cycling experiments necessary to enhance predictive die-attach failure model. 4Q 2010

3. Develop simulation tools for calculation of advanced technology package lifetime in application environments. Once the predictive thermo-mechanical models have been developed from the thermal cycling experimental data, they can be combined with existing NIST electro-thermal models to generate a more realistic and comprehensive modeling tool for assessing the lifetime of advanced technology packages.

DELIVERABLES:

- Develop a methodology for integrating package reliability models into electro-thermal models. 3Q 2010
- Build a test case lifetime prediction scenario including electro-thermo-mechanical model and a simulation file with a complex power function representing exposure. 4Q 2010

4. Perform analysis of packaging technologies for high performance applications. Approaches will be explored to adapt these protocols and mechanisms for electro-thermal-mechanical modeling of power electronic devices and systems to a wide range of high performance applications, including solid state lighting.

DELIVERABLES:

- Scoping document describing failure mechanisms of high performance packaging structural features. 3Q 2010

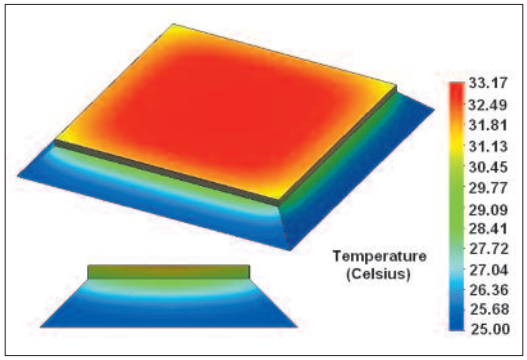

Figure 1. Finite-element 3D CAD transient and steady-state thermal modeling is being used to aid in the development of the Saber electro-thermal models for the devices used in electric car power modules

- Coordinate with industry and Federal agencies to define the predictive package lifetime needs for the following applications ITRS, LED lighting, and power electronic modules for Alternate Energy and smart grid application. 4Q 2010

Accomplishments

■ The UM/CALCE and NIST have joined researchers to share laboratory instrumentation and perform measurements needed to identify and model package degradation mechanisms. Discussion is ongoing with Delphi and Virginia Tech on test bed systems for analysis. Discussions with NREL, Delphi, Azure Dynamics, and Powerex have been made on applying the process to their applications. Presentations on these joined efforts will be shown at the IAPG meeting in May, 2010.

■ Models for wirebonds and die attach, and substrate have been evaluated and adapted for this study.

■ The thermal cycling system at NIST has been improved to allow the independent setting of cycle control parameters like dwell times and the heating and cooling rates.

■ Thermal cycling protocol has been developed for maximizing information on electrical performance degradation as a function of aging..

■ Thermal cycling has been performed on various packages. TSP measurements were acquired during the cycling process to monitor changes in electrical performance. These changes can be correlated to package failure mechanisms in order to create a predictive model.

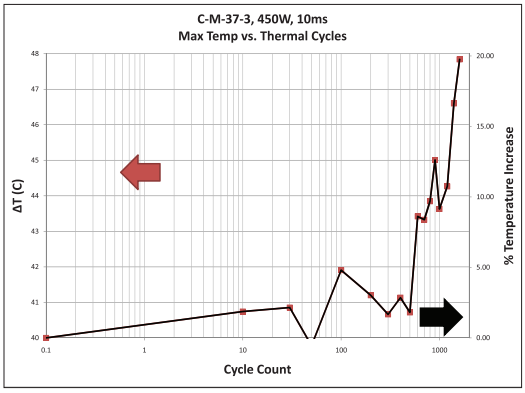

Figure 2. Temperature-sensitive parameter (TSP) measurements show how the junction temperature of a power device is affected as thermal cycling progresses on its package, altering its heat dissipation ability with time.

■ Failure mechanisms of power electronic packaging structures at different temperature ramp rates are being validated, and the correlation of power device failure mechanisms to high performance packaging is being conducted.

■ Preliminary electro-thermal simulations have been made for the power module of the electrical vehicle drive.

Collaborations

University of Maryland CALCE Electronic Products and Systems Center: Patrick McCluskey

Virginia Tech: Jason Lai

University of Central Florida: Z. John Shen

American Competitiveness Institute (ACI), Navy ManTech Center: Barry Thaler

General Electric R&D: Ravisekhar Raju.

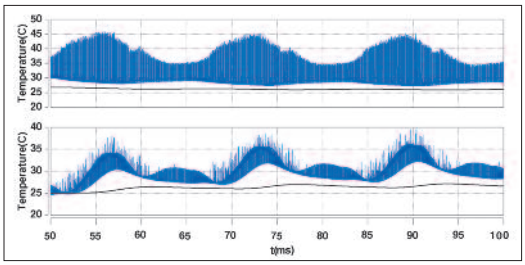

Figure 3. "Electro-thermal simulation example of a ½ sine wave conduction time of one main switch and its auxiliary switch for the electric vehicle drive. The average power for the main switch is about 106 W and the auxiliary is about 61W.")

Powerex: Scott Leslie

Quantum Focus Instruments Corporation:

Cree Inc.

Publications

J. M. Ortiz-Rodríguez, M. Hernández-Mora, T. Duong, S. G. Leslie, and A. R. Hefner, *"Thermal Network Component Models for 10 kV SiC Power Module Packages,"* in the Proceedings of the 2008 IEEE Power Electronics Specialists Conference (PESC), June 15-19, 2008, Island of Rhodes, Greece.

T. H. Duong, J. M. Ortiz-Rodriguez, R. N. Raju, and A. R. Hefner, *"Electro-thermal Simulation of a 100 A, 10 kV Half-Bridge SiC MOSFET/JBS Power Module,"* in the Proceedings of the 2008 IEEE Power Electronics Specialists Conference (PESC), June 15-19, 2008, Island of Rhodes, Greece.

N. Barbosa III and A. J. Slifka, *"Spatially- and Temporally-Resolved Thermal Imaging of Cyclically Heated Interconnects by Use of Scanning Thermal Microscopy (SThM),"* submitted to Microscopy Research and Technique.

A. R. Hefner and S. Beermann-Curtin, *"Status of the DARPA WBST High Power Electronics Program in SiC Device Development and Technology Transition,"* Proceedings of the Government Microcircuit Applications and Critical Technology Conference (GOMACTech) 2007, March 19-22, 2007, Lake Buena Vista, FL, pp. 185-188.

M. Hernández-Mora, A. Akuffo, C. E. Hood, J. M. Ortiz-Rodríguez, and A. Hefner, *"Experimental Evaluation of SiC PiN Diode Forward Bias Degradation and Long Term Stability,"* 2007 IEEE Power Electronics Specialists Conference (PESC), 17-21 June, 2007, Orlando, FL, pp. 61-65.

A.R. Hefner, R. Sei-Hyung, H. Brett, D.W. Berning, C. E. Hood, J. M. Ortiz-Rodriguez, A. Rivera-Lopez, T. Duong, A. Akuffo, M. Hernández-Mora, *"Recent Advances in High-Voltage, High-Frequency Silicon-Carbide Power Device,"* Proceedings of the 2006 IEEE Industry Applications Society (IAS) Annual Meeting, October 8-12, 2006, Tampa, FL, pp. 330-337.

R. R. Keller, R. H. Geiss, N. Barbosa III, A. J. Slifka, and D. T. Read, *"Strain-Induced Grain Growth during Rapid Thermal Cycling of Aluminum Interconnects,"* Paper presented at the 2006 TMS Annual Meeting, April 2006.

Manufacturing Support Program

Cross-cutting all manufacturing disciplines is the need for supporting information technology and processing capabilities. The transition to 300 mm fabs, single-wafer lots, and the extensive use of foundries has made efficient information handling and automation indispensable to the production process. Information technology touches nearly every aspect of semiconductor production and distribution, including process control, tool to tool interconnect, automated material handling and tracking, reticle management, and information interchange across the supply chain. NIST is working with the International Semiconductor Industry Initiative (ISMI, a subsidiary of SEMATECH) to provide and maintain an on-line engineering statistical handbook to support process control, and is working with industry on standards required to support information flow across the "engineering chain," and to provide standards for secure electronic diagnostic data and for coherent time synchronization on the factory floor.

Product Authentication Information Management

Technical Contacts:
Y. Li-Baboud
E. Simmon
Y. Obeng
A. Griesser

Goals

The project's objective is to realize interoperable and secure exchange of information through participation in standards development and research of information models for capturing the necessary information for authentication of electronics and electronic components throughout its product lifecycle.

Customer Needs

Distinguishing the genuine article from counterfeit is increasingly challenging, and accurate product authentication will require efficient access to information. Central to this objective is the management of the information needed for product authentication. It is imperative to have integrated information flow throughout the product life cycle, from conception to disposal, such that relevant data would be securely yet readily available to the necessary parties from manufacturers to end-users to customs and other law enforcement officers. In order for information management to be an effective tool for product authentication, international government entities and global supply chain stakeholders must ensure accessibility and traceability of pertinent product identity information.

Technical Strategy

A solution to the counterfeiting problem will require a layered approach to provide prevention, detection, and mitigation while maintaining a viable tradeoff between cost and risk. The project will work with industry to determine challenges and priorities in addressing counterfeit issues. Through discussions with industry and government stakeholders, the project will gather information on the current landscape, threats, challenges, priorities and potential solutions in addressing counterfeit electronic products. The overall information integration strategy necessary for developing collaborative anti-counterfeiting countermeasures is shown in Figure 1.

DELIVERABLES:

- Participate in workshops to determine the current landscape, threats, challenges and priorities in addressing counterfeit electronic products in the supply chain. 3Q 2010

The project will continue to participate in industry standards activities, including SEMI Anti-Counterfeiting TF to develop a common architecture for product authentication through authentication service providers. The project will also participate in the electronics industry anti-counterfeiting efforts, including IPC. Other industry standards will also be of interest in order to leverage lessons learned and ensure interoperability of product authentication information in the global supply chain as shown in Figure 1.

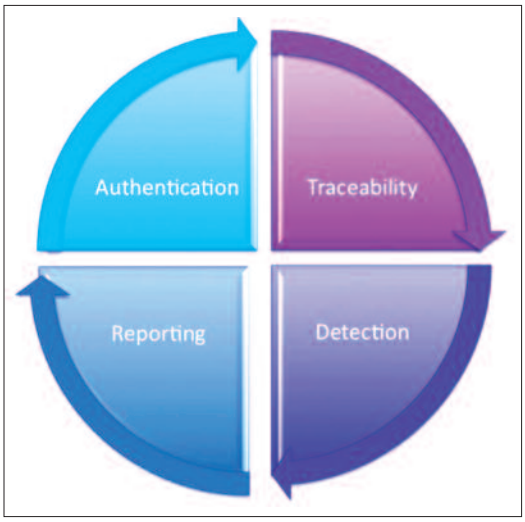

Figure 1. Managing diverse types of information strengthens product identification.

Another thrust is to bring interoperability among disparate information sources on product identity. Information models by developing a concrete understanding of the counterfeiting problem, product authentication requirements, and other information needs based on input from industry and government stakeholders. The project will strive to develop and propose an integrated information flow throughout the product life cycle, from conception to disposal, such that relevant data would be securely yet readily available to the necessary parties from manufacturers to end-users to customs and other law enforcement officers.

DELIVERABLES:

- Participate and review standards activities related to anti-counterfeiting, SEMI, ISO, NEMI, IPC. 4Q 2010
- Develop a data model describing security assurance attributes for assessing product authentication solutions. 4Q 2010

Accomplishments

■ Participated in ISO TC247 for Fraud Countermeasures and Control.

Co-hosted NIST-SEMI Product Authentication Information Management Workshop, February 17-18, 2009, in Gaithersburg, MD.

Participated in the SEMI T20 Specification for System Architecture on Product Authentication of Semiconductor and Related Products development.

Presentations and Publications

Y. Obeng, *"SEMI ACTF Activities,"* NIST-SEMI Product Authentication Information Management Workshop, February 2009.

E. Simmon, *"Counterfeit Avoidance Management: An IPC Perspective,"* NIST-SEMI Product Authentication Information Management Workshop, February 2009.

E. Simmon. *"Secure Authentication Codes",* SEMICON West, July 2008.

Y. Li-Baboud. *"Product Lifecycle Identity Management,"* Symposium on Prevention, Detection and Mitigation of Counterfeit Electronic Components, September 2008.

Next Generation Factory Data Quality

Technical Contacts:
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J. Amelot F. el Osbi
M. Mason
C. Vasseur

Goals

The project's objective is to facilitate the development of standards and guidelines to achieve reliable data quality for supporting present and Next-Generation Factory (NGF) data quality needs. The project aims to educate the industry about technology integration and related issues on meeting industry requirement as well as developing prototype and test bed environments for research data quality issues such as time synchronization and data time-stamping.

Customer Needs

The industry NGF goals include 50 percent reduction in cycle time, along with 30 percent reduction in cost of manufacturing. However, increasing wafer sizes, decreasing critical dimensions, and new material introduction all challenge higher initial yield, lower manufacturing costs, and time to market demands. Among the key issues driving the challenges are monitoring and maintaining surface uniformity, decreasing process tolerance windows, as well as increasing process and equipment complexity.

Advancing next-generation semiconductor manufacturing will require data to be collected and analyzed in real-time from a rising confluence of data streams, due to narrowing tolerance windows, new material introduction, and novel processing techniques. Some of the pertinent sources include process equipments and their operational subsystems, in-line metrology, and factory environmental conditions. The retrieved data is vital for designing new processes, maintaining optimal equipment and processing capabilities, controlling the equipment, providing information for rapid yield learning, and expediting handoff of process technology for volume production.

Managing the data proliferation will be critical in realizing the anticipated benefits of greater data accessibility. Extrapolating intelligent correlations from volumes of data in a timely manner requires a common, efficient method of merging the data.

"The stringent engineering requirement is driving need for more data that would result in so-called data explosion. It is critical not only to collect necessary data but also to develop intelligent analysis and algorithms to identify and use the right signals to make data driven decisions, and reuse such intelligence as models in later occasions." *2009 ITRS, Factory Integration*, p. 8.

The quality of the data, including contextual data, impacts the ability to make optimal automated processing quality control decisions in real-time. One aspect of data quality is the ability to acquire accurate time stamps for effectively diagnosing problems and determining other types of cause-effect relationships for Advanced Process Control (APC) applications, especially in the realm of Fault Detection Classification (FDC) and Virtual Metrology (VM). The Equipment Data Acquisition (EDA) interface where data collection rates can increase to 10,000 data points per second, one millisecond time stamp accuracy is required. An inaccurate time stamp potentially renders the data invalid for many data mining and other analysis applications, yet there continues to be a wide variation in time stamping accuracies among semiconductor manufacturing systems. A robust infrastructure to support accurate time stamps will provide the means to better exploit the increased data availability in next generation semiconductor manufacturing. Such an infrastructure will require an efficient clock synchronization architecture for maintaining time on all related clocks within the process and metrology tools as well as in the manufacturing site.

Technical Strategy

Through participation in the SEMI Data Quality Task force, this project will continue to support standards development to ensure factory equipment and equipment components can reliably and consistently provide quality data and metadata.

The initial focus area included the exploration of data time-stamping, data acquisition and data fusion through an embedded sensor and control system, as shown in Figure 1, to pinpoint the key issues and challenges impacting data quality for a generic embedded sensor and control system. The research will examine the flow of sensor data as it is processed using analog-to-

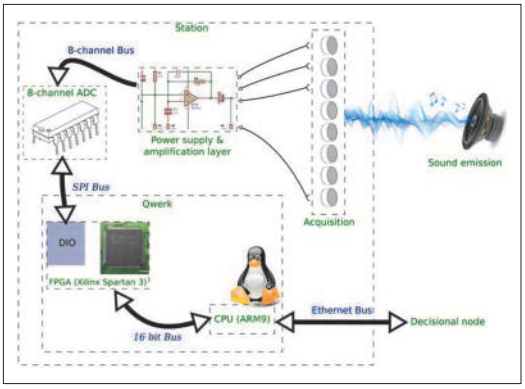

Figure 1 .Integration architecture of sensor board and embedded system, where analog acoustic data is time-stamped at the FPGA and packaged for analysis at the control node.

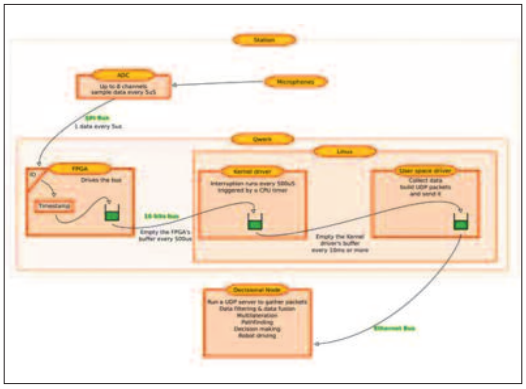

Figure 2. Data flow of sensor data acquisition including the sampling frequencies and processing latencies throughout the system.

digital conversion, FPGA, and an embedded processor (Figure 2) to determine the key data bottlenecks and various methods to ensure the quality of the data is maintained throughout the system in order to make accurate and intelligent decisions. The findings would provide insights in how to integrate embedded sensor technologies to provide tested potential solutions for meeting next-generation data quality requirements. Additionally, a distributed sensor and control network enables NIST to research system optimizations for effective data collection, sensor data fusion, and real-time control. In parallel to the technical development, a survey report based on industry feedback next-generation factory requirements is also provided to detail research opportunities for meeting NGF requirements related to data quality.

DELIVERABLES:

- Present a NIST seminar on improving embedded system data quality. 1Q 2010

Accurate time stamping requires a reliable and accurate clock synchronization methodology. Research on practical application and performance testing of the synchronization protocols would determine the impact of various computing factors (e.g., CPU usage, network traffic, constraints of sensors and embedded systems, etc.) on distributed clock synchronization performance.

The second focus area is establishing a distributed clock synchronization test bed. The Engineering Research Center at the University of Michigan has been collaborating with NIST in conducting studies on the accuracies achievable with software-based time synchronization protocols in industrial networks. To fully understand the impact of data quality on automated decision-making, a distributed sensor and control environment is being developed along with an evolving factory simulation system. The work will have practical benefits in ensuring the potential solutions and new industry standards are feasible and effective in achieving accurate clock synchronization and data time stamping.

The test bed will provide a research environment to explore mainstream time synchronization protocols and methods to optimize accuracy and cost tradeoffs. The synchronization protocols to be explored include IEEE 1588, Precision Clock Synchronization Protocol for Networked Measurement and Control Systems, and NTP, Network Time Protocol.

DELIVERABLES:

- Draft research paper on using time synchronization for factory control. 2Q 2010

Conformance to industry standards would enable more effective interoperability among factory automation systems. To enable a method to evaluate and provide guidance on improving conformance to current and future implementations, the project is also working with ISMI on the development of a prototype metadata quality assessment tool, where one of the objectives is for assessing conformance to SEMI equipment metadata standards and ISMI guidelines. The tool development was suggested by ISMI.

DELIVERABLES:

- Continue development of the metadata quality scorecard tool based on SEMI standards and ISMI guidelines. 4Q 2010

Accomplishments

Developed a prototype equipment metadata scorecard tool for validation of guidelines and SEMI standards compliance.

Established a sensor network testbed to study data quality issues and recommended practices relevant to timing in embedded sensor systems.

Developed EDA Factory Data Collection Simulation software for testing and developing recommend practices for network performance data quality aspects.

"Using Network Time Protocol (NTP): Introduction and Recommended Practices" was published as an ISMI Technical Report in February 2006, and updated in May 2008.

SEMI E148 Specification for the Definition of Time Synchronization Method and Format.

"Time Synchronization in Manufacturing Networks" at the Network Performance Workshop, University of Michigan, April 2006.

Collaborations

Harvey Wohlwend, Gino Crispieri, Lance Rist, International SEMATECH Manufacturing Initiative

James Moyne Engineering Research Center, University of Michigan Ann Arbor

Alan Weber, Alan Weber and Associates

Ecole Supérieure d'Informatique et Applications de Lorraine Nancy, France

Presentations and Publications

D. Anand, Sharma, D., Li-Baboud, Y., and Moyne J. *"EDA performance and clock synchronization over a wireless network: Analysis, experimentation and application to semiconductor manufacturing,"* Proceedings of IEEE International Symposium on Precision Clock Synchronization for Measurement, Control and Communication 2009, October 12-16, 2009.

J. Amelot and Y. Li-Baboud. *"Improving Data Quality in Embedded Sensor Systems"*, AEC/APC Symposium, September 27-30, 2009.

D. Sharma, D. Anand, Y. Li-Baboud and J. Moyne. *"Real-time Synchronized Control Testbed for Semiconductor Manufacturing,"* AEC/APC Symposium, September 27-30, 2009.

Y. Li-Baboud, A.Weber, P. McGuire, J. Amelot, and J. Le Guen. *"Assessment of Industry Research Priorities for Intelligent Sensors and Control"*, AEC/APC Symposium, October 4-8, 2008.

Y. Li-Baboud, X. Zhu, D. Anand, S. Hussaini, and J. Moyne. *"Semiconductor Manufacturing Equipment Data Acquisition Simulation for Timing Performance Analysis,"* Proceedings of IEEE International Symposium on Precision Clock Synchronization for Measurement, Control and Communication 2008, September 24-26, 2008.

Y. Li, *"Using NTP: Introduction and Recommended Practices,"* ISMI Technology Transfer, May 2008.

V. Anandarajah, N. Kalappa, S. Hussaini, R. Sangole, J. Baboud, Y. Li, and J. Moyne. *"Precise Time Synchronization in Semiconductor Manufacturing,"* Proceedings of the IEEE International Symposium on Precision Clock Synchronization for Measurement Control and Communication, October 1-3, 2007, Vienna, Austria.

N. Kalappa, V. Anandarajah, J. Baboud, Y. Li, and J. Moyne. *"Fab-Wide Network Time Synchronization – Simulation and Analysis,"* AEC/APC Symposium, September 15-20, 2007, Indian Wells, CA.

Engineering Chain Management in the Semiconductor Industry

Goals

This project investigates and documents key issues related to electronic data exchange, supply chain communication, and other automation standardization needs confronting the semiconductor industry. The objective of this project is to facilitate the evolution of an integrated semiconductor "Engineering Chain" which provides each partner with the data needed to make business decisions in a timely manner.

Customer Needs

Increasing technological requirements have led the semiconductor industry to seek further means of cost savings by improving factory productivity, streamlining business models, and accelerating their supply chain. The growing complexity of product development and manufacturing models in parallel with shrinking product lifecycles further exacerbates the challenges the industry faces. Maximizing interoperability among automation systems in the factory and data exchange throughout the entire manufacturing chain (see Figure 1) will become a greater issue for realizing the semiconductor industry's requirements to reduce time, inventory, and therefore costs.

A growing area of concern for the semiconductor industry is the growing trend towards legislation that seeks to minimize the environmental impact of manufacturing. This can range from legislation that bans the use of hazardous substances, to mandating tracking of resources (energy and water), to mandating the use of energy efficient designs. Examples include the European Union's new Registration, Evaluation, Authorization, and Restriction of Chemicals (REACh) regulation and China's Administrative Measure on the Control of Pollution Caused by Electronic Information Products (often referred to as China RoHS). REACh alone will have significant impact as it will require registration and safety evaluations of more than 100 000 substances and will likely lead to banning substances of very high concern. For most of these pieces of environmental legislation, companies will only be able to prove compliance through the exchange of extensive amounts of product and manufacturing data. This can only be achieved through the development of new standards that span the entire supply chain.

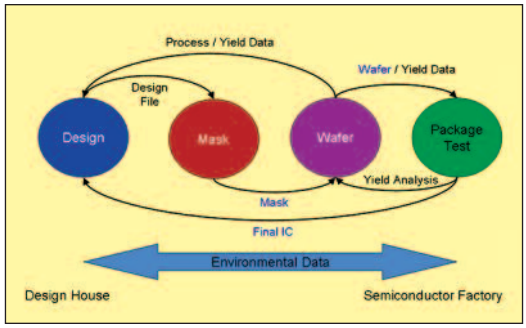

Figure 1. Engineering Chain: Semiconductor Data Exchange Needs Engineering Chain: Semiconductor Data Exchange Needs.

Furthermore, the semiconductor industry is also seeking to control costs and improve semiconductor yields through the development of advanced Factory Information and Control Systems (FICS). Next generation FICS are expected to be able to collect information from equipment that will enable intelligent automated decision-making concerning factory resources. (This will require data quality assurance). Materials will be processed and dispatched to equipment in a way to minimize production-equipment idle time thus maximizing factory output. In addition, FICS will allow factories to be more reconfigurable as needed even to the point of being able to modifying wafer processes on a wafer-by-wafer basis. This is even more important with the expected transition to 450 mm. Developing these FICS will require a greater level of interoperability and data exchange within the semiconductor factory.

Technical Strategy

To help the industry achieve their goal of effective partnerships within an Engineering Chain, this project engages in industry efforts that would benefit from NIST's neutrality, multi-industry expertise, and broad and detailed knowledge of the Information Technology (IT) standards development process.

DELIVERABLES:

- Chair the Information Management Systems (IMS) TWG of the 2011 iNEMI Roadmap. 4Q 2010

Technical Contacts:
J. Messina
K. Brady
E. Simmon

"Rapid changes in semiconductor technologies, business requirements, and the need for faster product delivery, high mix, and volatile market conditions are making effective and timely factory integration to meet accelerated ramp and yield targets more difficult over time."

(ITRS) 2009 Factory Integration, p.1.

Factory Integration Difficult Challenge: Increasing global restrictions on environmental issues 2009

(ITRS) 2009 Factory Integration, p. 4.

Attendance at workshops, conferences, and standards meetings held by key organizations in the semiconductor community such as International SEMATECH (ISMT), Semiconductor Equipment Materials International (SEMI), and RosettaNet provides opportunities to assess current areas of IT standards development. As the industry moves towards utilization of mainstream computing technologies including eXtensible Markup Language (XML) and Simple Object Access Protocol (SOAP), the project provides guidance in leveraging existing best practices from other industries and promoting collaborations among industry partners for mutual benefit. The investigation also includes an informal survey of semiconductor supply chain partners including designers, chip manufacturers, and equipment suppliers to gauge their existing practices, requirements and priorities. Site visits will provide an opportunity for key industry figures to share their vision of how IT standards would expedite advancement of new technologies and business models.

DELIVERABLES:

- Work with organizations such as SEMI, IPC, IEC, and RosettaNet to identify standards needs for developing areas such as environmental compliance, anti-counterfeiting activities, and data quality. 4Q 2010

One priority area for the electronics industry is how to respond and comply with emerging environmental legislation being established around the world. The key to complying with most of this new generation of environmental regulations is to collect data throughout a product's lifecycle. This will necessitate the development of new data exchange standards in order to ensure the free flow of environmental data throughout the supply and manufacturing chains. Building on its ties to academia, industry, and governmental agencies the IIEDM project will seek to coordinate industry's response in developing the needed standards. Due to NIST's neutrality and the IIEDM's leadership positions in key standards development bodies (IEC, IPC, etc) the project is in a unique position to both increase industry participation in the standards development process as well as work to avoid duplication of effort due to redundant standards development activities.

DELIVERABLES:

- Develop supporting software tools and software translators to assist the Electronics Industry with new and emerging environmental legislation. 2Q 2010

Accomplishments

Completed a new series of modular declaration standards (IPC 1750 series) used to exchange environmental data throughout the entire supply chain all the way from raw materials to final producers.

Developed and built a free software tool called “Scriba”. The Scriba tool was created to be the new reference implementation for the IPC 1752 version 2.0 Material Declaration standard.

Delivered talk on "Drivers for Environmental Information Exchange: A Electronics Manufacturing Perspective" at the ISMI Manufacturing Symposium in October 2009.

Organized and hosted a series of NIST Product Authentication Information Management (PAIM) Workshops.

In conjunction with IPC Corp., NIST developed the IPC 1752 v1.0 material declaration standard that supports the exchange of RoHS environmental legislation through the engineering chain.

Created a tutorial on how to improve the semiconductor standards development process through the use of XML and UML. This tutorial has been taught as a class at both NIST and various SEMI standards workshops.

Collaborations

Alan Weber, Alan Weber & Associates.

ITRS Factory Integration Technical Working Group.

SEMI.

SEMATECH.

IPC.

Publications

Sharma, Deepak, Anand, Dhananjay, Li-Baboud, Ya-Shian, Moyne, James Dr., *"EDA Performance and Clock Synchronization Over a Wireless Network: Analysis, Experimentation and Application to Semiconductor Manufacturing"*, ISPCS 2009, Brescia, Italy, 10/12/2009 - 10/16/2009.

Sharma, Deepak, Anand, Dhananjay, Li-Baboud, Ya-Shian, Moyne, James Dr., *"A Time Synchronization Testbed to Define and Stan-*

dardize Real-Time Model-Based Control Capabilities in Semiconductor Manufacturing", AEC/APC Symposium, Ann Arbor, MI, US, 9/29/2009 - 9/30/2009.

E. D. Simmon, J. V. Messina, *"Expanding Environmental Information Management: Meeting Future Requirements"*, 16th ISPE International Conference on Concurrent Enginnering, Taipei, Taiwan, 7/20/2009 to 7/24/2009.

E. D. Simmon, J. V. Messina, *"Harmonizing Environmental Data Exchange Standards: Lessons Learned from the electronics Industry"*, The Eighth International Conference on EcoBalance, The Eighth International Conference on EcoBalance, Tokyo, Japan, 12/10/2008 to 12/12/2008.

E. D. Simmon, J. V. Messina, M. L. Aronoff, M. Cox, *"Environmental Trends Affecting Electronics Manufacturing"* Fab Engineering and Operations, No. 4, (01-Aug-2008).

J. V. Messina , E. Simmon, E., K. Brady, *"Information Management for Environmental Concerns and Regulatory Requirements"* FEO Magazine, Feb 2008.

NIST/SEMATECH e-Handbook of Statistical Methods

Goals

The goal of the NIST/SEMATECH e-Handbook of Statistical Methods project is to produce an online resource to help scientists and engineers incorporate statistical methods into their work more efficiently. Electronic publication and a practical, example-driven format were chosen to make the e-Handbook readily accessible to its target audiences in industry, including the semiconductor industry in particular.

Customer Needs

Semiconductor manufacturing requires extraordinary discipline in process control.

For example, a typical integrated circuit manufacturing process involves several hundred steps. These steps may include as many as thirty lithographic levels, which require extremely precise alignment with respect to one another. Tight process control is essential to produce a functional circuit. SEMATECH has recognized the importance of statistical process control in semiconductor manufacturing and has developed and maintained expertise in this field since its inception in 1988. Two of the more difficult issues impeding routine implementation of these techniques, however, include educating the users and making the tools easy to use.

Technical Strategy

NIST and SEMATECH formed a collaboration under the umbrella Cooperative Research and Development Agreement (CRADA), combining the general expertise in engineering statistics at NIST with the semiconductor manufacturing expertise resident at SEMATECH.

DELIVERABLES:

- Update and maintain the e-Handbook on-line. 4Q 2010
- Continue development of a new chapter on evaluation of measurement uncertainty. 4Q 2010
- Complete updating of examples using the open-source statistics software R. 4Q 2010

Accomplishments

Since release of the final version, work has focused on publicizing the e-Handbook and responding to user feedback. Recent work has focused on the updating of the examples using the open-source statistics sofware, R. The new material is just under half complete and should be ready for release in about one more year (Figs. 1 and 2). The web version of the e-Handbook received 9202869 hits during the last 12 months and over 9500 e-Handbook compact disks were distributed to industrial, government, and academic users all over the world while the e-Handbook was supported in CD format. Publicity on

```
##############################################################################
## weibull-8.4.1.3.R
## AUTHOR: Antonio Possolo
## MODIFICATION: 2006 Nov 04
## HANDBOOK: 8.4.1.3. A Weibull maximum likelihood estimation example
## http://www.itl.nist.gov/div898/handbook/apr/section4/apr413.htm
##############################################################################

      .
      .
      .

## (3) Survival curve (Kaplan-Mier)
ys = survfit(y ~ 1, type="kaplan-meier")
summary(ys)
plot(ys, xlab="Hours", ylab="Survival Probability")

## (4) Weibull Probability Plot
p = ppoints(failures, a=0.3)
plot(failures, -log(1-p), log="xy",
     xlab="Hours", ylab="Cumulative Hazard")

## (5) Weibull Fit
yw = survreg(y ~ 1, dist="weibull")
summary(yw)

      .
      .
      .

## (9) Probability density of fitted model
curve(dweibull(x, shape=betaHAT, scale=etaHAT),
        from=0, to=muHAT+6*sigmaHAT,
        xlab="Hours", ylab="Probability Density")
```

Figure 1. Snippets of R code from an analysis of Weibull reliability data from the e-Handbook.

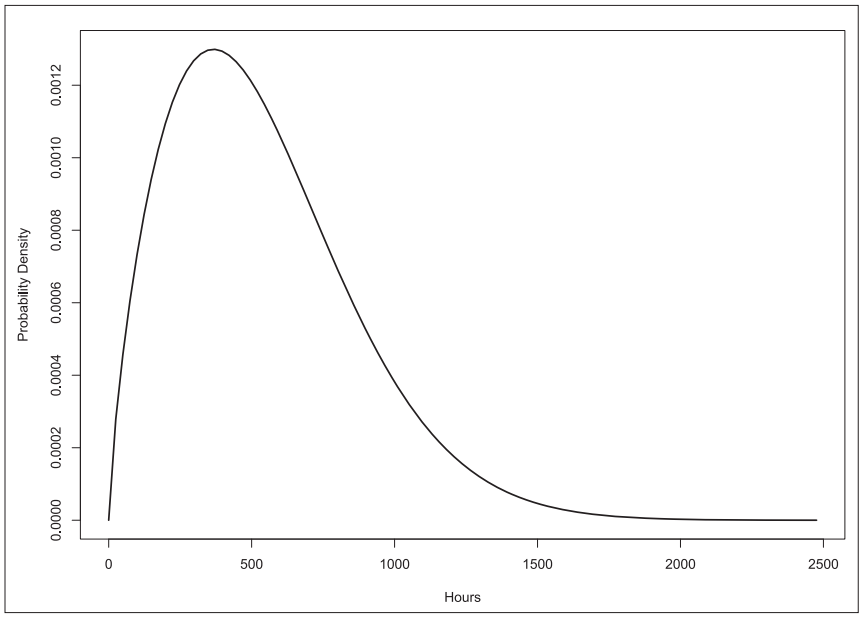

Figure 2. Probability density for Weibull reliability example plotted using R.

Technical Contacts:
W. F. Guthrie
A. Heckert
J. J. Filliben
J. Splett
C. Cleraux

"The online engineering statistics handbook is very useful and I make reference to it often in my position as an R&D engineer at a medical device company."

Josh Molho, Ph.D.
Pelikan Technologies

"I reviewed the e-Handbook on the net and I am very impressed with the content, organization and consolidation of the statistical methods."

Jack Lewis
Microchip Technology Inc

the e-Handbook has appeared in Science, Quality Digest, MicroMagazine.com, States News Service, National Science Digital Library Report for Math, Engineering, and Technology, and American Statistician.

Collaborations

International SEMATECH, Paul Tobias, Jack Prins, Chelli Zey; project planning, organization, writing and editing. Motorola, Pat Spagon; project planning, organization, and writing.

AMD, Barry Hembree; project planning, organization, writing and editing.

Publications

NIST/SEMATECH e-Handbook of Statistical Methods, M. Carroll Croarkin and Paul Tobias, editors, http://www.nist.gov/stat.handbook/.

Photovoltaic program

The overall aim of the PV industry is to broaden commercial adoption by reducing the cost of solar electricity; the forecasted industry growth shows the costs of photovoltaic (PV) modules decreasing by 8% to 14% yearly for the foreseeable future. A combination of an increase in cell efficiency and a significant reduction of manufacturing costs will be required for the PV industry to reach the overall cost targets. Current PV technology must be optimized for cost and performance efficiency, and new technologies must be accelerated from R&D to production. These changes include, but are not limited to, more effective use of materials, more productive manufacturing equipment, and more advanced processes. The overall task of the Photovoltaic Program is to assist the industry in meeting the productivity and module efficiency gains needed to meet the forecasted cost and performance targets. These goals include advances in new materials introduction, new material integration schemes, metrology to characterize fundamental electronic and opto-electronic properties, and increased knowledge of degradation and failure mechanisms limiting the long-term functionality of PV modules.

Metrology to Enable Advanced Generation 2 & 3 Photovoltaics

Technical Contacts:
Nhan V. Nguyen
David Gundlach

Goals

To develop electro-optical metrology that can provide accurate measurements of the electro-optical properties of photovoltaics (PV) materials and devices, as a function of device processing, to enable manufacturability. In this newly created project, we have begun developing instrumentation, measurements, and modeling by combining electrical and optical techniques to perform external quantum efficiency (EQE), electro-absorption and reflection (EAR), spectroscopic ellipsometry (SE), and internal photoemission (IPE). Concurrently, we are establishing impedance and current-voltage spectroscopic techniques to elucidate the electronic structure, importantly, electrically active in-gap states, and charge transport properties.

Customer Needs

Photovoltaics have recently emerged as the leading alternative source of electrical power fossil fuels. Investments in PV technology have rapidly increased worldwide in recent years. Although the first solar cell was invented for more than 50 years ago, there remain substantial gaps towards the economical exploitation of sunlight as a practical alternative source of power. Specifically researchers and manufacturers must develop and/or improve performance, efficiency, reliability, manufacturability, and to reduce cost. There remain many fundamental scientific issues to be addressed, and many are currently being investigated worldwide. For example, despite the major advances that have been made to enable the commercialization of thin-film PV technologies many critical issues still need to be addressed.

Technical Strategy

In general, there is a need to relate the performance of PV devices to the methods and materials used to produce them. The relationship is extremely complex and difficult to resolve without direct measurement of the pertinent properties / metrics. Since the working mechanism of PV devices is to convert photons to mobile electric charge, it is obvious that the electronic and optical properties of the materials would be key to their performance. In this early stage of this project, we have begun to screen the different characterization methods, that employ both electronic and optical techniques, which will be then applied to thin-film and devices used in the second generation of PV materials and devices such as the CdS/CdTe system, and the third generation of PV that incorporates nano structures or nano-scale patterning to greatly enhance power conversion efficiency.

DELIVERABLES:

- Establish electro absorption spectroscopy, 4Q, 2010

Collaborations

Metallurgy Division - Daniel Josell, Jonathan Guyer, Albert Davydov

Center for Nanoscale Science and Technology - Nikolai Zhitenev, Behrang Hamadani

Surface and Microanalysis Science Division, CSTL – Lee Richter

Wright Center for Photovoltaics Innovation and Commercialization, the University of Toledo, OH - Robert Collins

Process Monitoring of Nanoparticles for Photovoltaics Manufacturing

Technical Contacts:
M. Sobolewski

Goals

To provide measurement techniques for electrical monitoring of the average size and density of nanoparticles in situ during plasma deposition of thin film photovoltaic materials, thereby enabling manufacturers either to eliminate nanoparticles from processes where they are detrimental or to optimally control their size in processes where they are beneficial or essential.

Customer Needs

In recent decades, the price of photovoltaic modules has fallen by more than a factor of ten. Nevertheless, to accelerate their deployment, further reductions in price are needed. Solar cells made by depositing thin films on inexpensive glass, metal, or plastic substrates have lower production costs than single crystal or multicrystalline cells, but they also have lower power conversion efficiencies. Consequently, much effort in industry is dedicated to increasing the efficiency of thin film cells (for example by using multi-junction cells) while maintaining, and further decreasing, their low production cost.

Plasma-enhanced chemical vapor deposition (PECVD) is a particularly useful method for film deposition used by the semiconductor and other industries. In many applications, PECVD deposition rates are relatively low, too low for economical production of solar cells. Nevertheless, by using very high frequencies (VHF) to excite the plasma or by raising the pressure, growth rates can be increased, making PECVD economically competitive for solar cell manufacturing.

In PECVD processes, molecules may react not only on the substrate surface but also in the gas, producing particles which grow from sub-nanometer size up to many nanometers. Indeed, the growth conditions that produce the high deposition rates needed for low cost production often tend to be the conditions most favorable for particle nucleation and growth in the gas phase. The particles are important because they can reach the substrate surface and be incorporated into the growing film, changing its composition, crystallinity, and topography. In many PECVD processes the effects of the particles on the films are deleterious. More recently, however, it has been suggested that incorporation of nanoparticles into films grown by PECVD may in fact be beneficial in some cases, notably, in the nanocrystalline silicon films that are used for multi-junction silicon-based cells. The efforts of manufacturers to either eliminate or to use and optimize the nanoparticles are limited, however, because of a lack of reliable, practical methods for monitoring the size and density of nanoparticles *in situ* in PECVD plasmas.

Technical Strategy

Measuring the light scattered from an individual, micron-sized particle can give information about its size, but this technique cannot determine the average size of a large collection of smaller particles immersed in plasma. Under such conditions, light scattering is still useful for detecting that particles are present, and determining where in the plasma they are located, but it does not give quantitative information about their numbers or their size. Furthermore, for particle sizes approaching 1 nm and below, even detecting the particles becomes difficult — requiring complicated photon-counting methods — or impossible.

Particles in plasmas can also be detected electrically. Capture of electrons by particles reduces the electron density in the plasma, while collisions between electrons and particles reduce the electron mobility. These changes in turn affect the impedance and other electrical properties of the plasma, including measured currents or voltages. Indeed, in several studies, changes in currents or voltages have been measured and related to the generation, movement, or loss of particles from the plasma. Nevertheless, there has been little systematic study in this area. Detailed experimental and modeling investigations are needed to allow changes in electron density to be distinguished from changes in electron mobility. Such work would, in turn, allow electrical measurements to simultaneously determine the average size and number density of nanoparticles.

In this project, we plan to perform such experimental and modeling investigations of the interaction of nanoparticles and electrons in plasmas,

develop electrical monitoring techniques for nanoparticles, and demonstrate their utility for photovoltaics manufacturing.

The first part of this effort is the development and validation of electrical measurements for nanoparticle monitoring. This work will be performed in plasma equipment already present at NIST. Minor modifications will be needed to enable operation in the very high frequency (VHF) range that is most relevant for economical production. Nanoparticles will be generated by injecting well-controlled bursts of reactive gases into inert gas plasmas. Varying the amount of reactive gas that is introduced in a burst allows the ultimate particle size to be varied. First, the generation and transport of particles will be characterized by laser light scattering and electrical measurements. Then, models will be developed to analyze the electrical measurements and identify changes in electron density and electron mobility. This modeling work draws on the extensive expertise in electrical modeling of plasmas already available at NIST. The model results will be validated by comparisons with simultaneous measurements made by microwave techniques and/or invasive probes. Then, models that relate the charging and transport of nanoparticles to their size will be used to implement methods for inferring the average size and average number density of the particles from the electrical data. The resulting model predictions for particle size will be tested by collecting particles on substrates and measuring them *ex situ* with a scanning electron microscope. In addition to providing a much needed, validated method for electrical monitoring of nanoparticle size, successful completion of phase 1 may also provide improved methods for controlling particle size, either by modulating the gas flows or pulsing the plasma.

DELIVERABLES:

- Provide a practical measurement method for electrically monitoring the average size and density of nanoparticles in plasmas. 4Q 2011

In the second part of the work, we will demonstrate and evaluate electrical monitoring of nanoparticles during PECVD deposition of amorphous and nanocrystalline silicon thin films for photovoltaic applications. This work will be done in a plasma reactor better suited than present equipment for such depositions. It will use substrate heating, higher pressures, and a different geometry better suited for scaling VHF plasmas to larger areas. The crystallinity, composition, and topography of films grown by PECVD will be analyzed *ex situ* by Raman spectroscopy, Fourier transform infrared spectroscopy, and scanning electron microscopy. Comparison of film properties with nanoparticle sizes determined from electrical measurements will allow the utility of electrical monitoring to be assessed. Then, the silicon thin films will be fabricated into device structures, and the device properties relevant to solar cells (e.g., minority carrier lifetime) will be measured. Comparison with these device properties with information about the nanoparticles present during film growth will provide a final test of the usefulness of the electrical monitoring of nanoparticles.

DELIVERABLES:

- Provide tests and evaluations of the usefulness of the monitoring technique in the manufacturing of photovoltaic thin film materials and cells. 2Q 2013

In another, more radical, approach, PECVD growth of a film on a substrate is entirely replaced by gas-phase plasma synthesis of nanoparticles. The particles, which are collected downstream on a screen, can then be sintered into a continuous layer or dispersed across a surface to form a noncontinuous array of isolated quantum dots. The resulting quantum dot solar cell may allow more than one electron-hole pair to be generated by each incident photon. If generation of multiple electron-hole pairs is practical (and if a way is found to collect them efficiently) quantum dot solar cells could provide a substantial improvement in efficiency and reduction in cost compared to crystalline and thin-film cells. Electrical techniques for monitoring nanoparticles in plasmas would also be of use in the gas-phase plasma synthesis of nanoparticles for these quantum dot cells. If practical quantum dot solar cells are realized, the work on PECVD of silicon thin-films could be re-directed, during the project or after its completion, towards gas-phase plasma synthesis of nanoparticles for quantum dot cells.

Accomplishments

This new project has only recently begun (in April 2010). Thus it would be premature to list

accomplishments. It should be noted, however, that the work will draw on the extensive record of NIST accomplishments in prior years in the area of electrical measurements and modeling of plasmas. These prior accomplishments include extensive measurement and modeling work done in NIST laboratories, as well as work done jointly with semiconductor equipment manufacturers in their research and development facilities.

Abbreviations and Acronyms

A.C.	alternating current
ADR	adiabatic demagnetization refrigerator
AEM	analytical electron microscopy
AES	auger-electron spectroscopy
AFM	atomic force microscope
ALMWG	Analytical Laboratory Managers Working Group (ISMT)
AMAG	Advanced Metrology Advisory Group (ISMT)
ANSI	American National Standards Institute
ARXPS	angle resolved X-ray photoelectron spectroscopy
ASPE	American Society of Professional Engineers
ATP	Advanced Technology Program (NIST)
BCB	benzocyclobutene
BESOI	bond and etch-back silicon-on-insulator
BGA	ball-grid array
BIPM	Bureau International des Poids et Mésures
BIST	built-in self-test
BST	barium strontium titanate
C-AFM	calibrated atomic force microscope (NIST)
C-V	capacitance-voltage
CAD	computer-aided design
CCD	charge-coupled device
CD	critical dimension
CMOS	complementary metal oxide semiconductor
CMP	chem-mechanical polishing
CNT	carbon nanotubes
CPU	central processing unit
CRADA	Cooperative Research and Development Agreement
CRDS	cavity ring-down spectroscopy
CSP	chip-scale package
CTCMS	Center for Theoretical and Computational Materials Science (NIST)
CVD	chemical vapor deposition
D.C.	direct current
DFT	design-for-test
DMA	differential mobility analyzer
DRAM	dynamic random-access memory
DSP	digital signal processing
DUV	deep ultraviolet
EBSD	electron backscatter diffraction
EELS	electron energy loss spectroscopy
EDC	embedded decoupling capacitance
EDS	energy-dispersive spectroscopy

Abbreviations and Acronyms (cont'd)

EMC	electromagnetic compatibility
EMI	electromagnetic interference
EPMA	electron probe microanalysis
EUV	extreme ultraviolet
FIFEM	field ion field emission microscope
FIM	field ion microscope
FWHM	full-width half-maximum
GIXR/SE	grazing incidence X-ray reflection/spectrascopic ellipsometry
GIXPS	grazing incidence X-ray photoelectron spectroscopy
HRTEM	high resolution transmission electron microscope
HSQ	hydrogen silsesquoxane
I-V	current-voltage
IC	integrated circuit
IGBT	insulated-gate bipolar transistor
IETS	Inelastic Electron Tunneling Spectroscopy
IPC	Association Connecting Electronics Industries
ISMT	International SEMATECH
ISO	International Organization for Standardization
ITRS	International Technology Roadmap for Semiconductors
LEED	low-energy electron diffraction
LER	line-edge roughness
LFPG	low frost-point generator
LOCOS	local oxidation of silicon
LPP	laser-produced plasma
LPRT	light-pipe radiation thermometer
MBE	molecular beam epitaxy
MEMS	micro-electro-mechanical systems
MFC	mass flow controller
MMIC	millimeter and microwave integrated circuits
MOS	metal-oxide-semiconductor
MOSFET	metal-oxide-semiconductor field-effect transistor
MPU	microprocessor unit
MUX	multiplex
NCMS	National Center for Manufacturing Sciences
NDP	neutron depth profiling
NGL	next generation lithography
NEMI	National Electronics Manufacturing Initiative
NIST	National Institute of Standards and Technology
NSMP	National Semiconductor Metrology Program
NLO	non-linear optical
NSOM	nearfield scanning optical microscopy

OMAG	Overlay Metrology Advisory Group (ISMT)
PED	Precision Engineering Division (NIST)
PLIF	planar laser-induced fluorescence
PMI	phase-measuring interferometer
PTB	Physikalisch-Technische Bundesanstalt
PZT	lead zirconium titanate
QM	quantum mechanics
RAM	random-access memory
RGA	residual gas analyzer
RLGC	distributed resistance, inductance, conductance, and capacitance
RTA	rapid thermal annealing
RTP	rapid thermal processing
SANS	small-angle neutron scattering
SBIR	Small Business Innovative Research
SCM	scanning capacitance microscope
SEM	scanning electron microscope
SHG	second harmonic generation
SIA	Semiconductor Industry Association
SIMOX	separation by implantation of oxygen
SIMS	secondary-ion mass spectrometry
SoC	system-on-a-chip
SOI	silicon on insulator
SPM	scanning probe microscope
SRC	Semiconductor Research Corporation
SRM®	Standard Reference Material
SSHG	surface second-harmonic generation
SSIS	surface-scanning inspection system
STM	scanning tunneling microscope
SURF III	Synchrotron Ultraviolet Radiation Facility III
TCAD	technology computer-aided design
TDDB	time-dependent dielectric breakdown
TDR	time-domain reflectometry
TEM	transmission electron microscope
TFTC	thin-film thermocouple
TOF	time-of-flight
TMAH	tetramethyl ammonium hydroxide
UHV	ultra-high vacuum
ULSV	ultra-large scale integration
UV	ultraviolet
WMS	wavelength modulation spectroscopy
VUV	vacuum ultraviolet
XPS	X-ray photoelectron spectroscopy
XRR	X-ray reflectometry

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