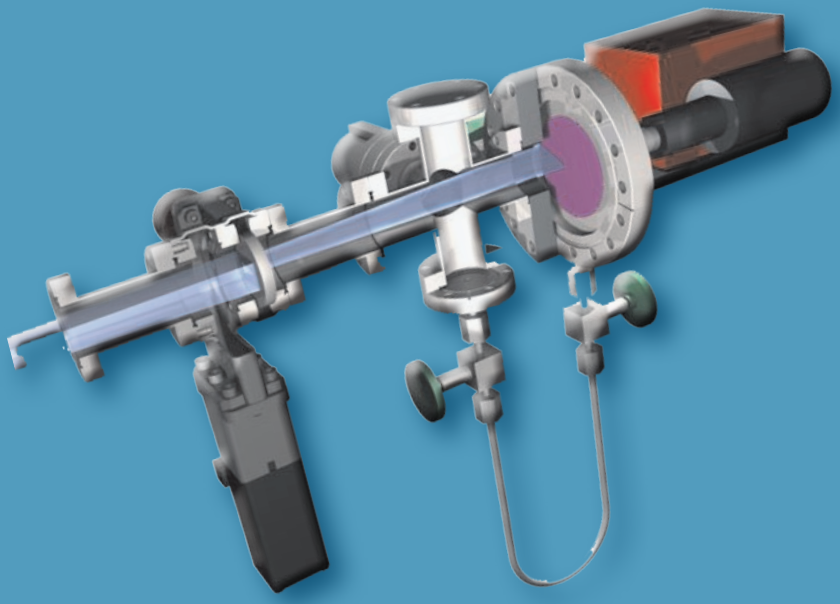
NISTIR 7604

Semiconductor Microelectronics and Nanoelectronics Programs



Edited by
Joaquin V. Martinez de Pinillos
Yaw S. Obeng
and Michele L. Buckley
July 2009

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National Institute of Standards and Technology
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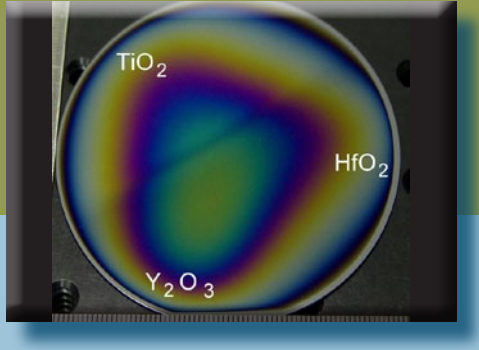

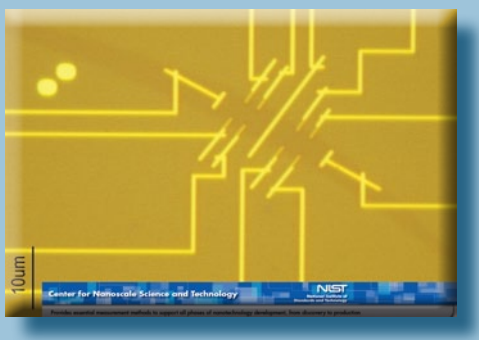

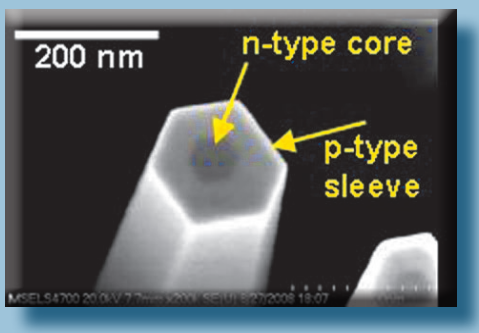

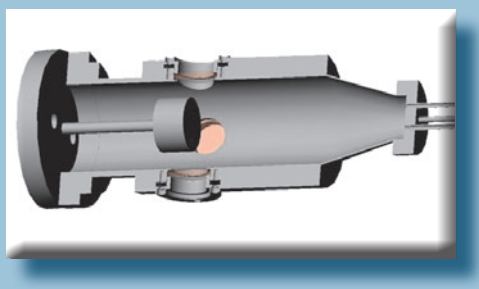

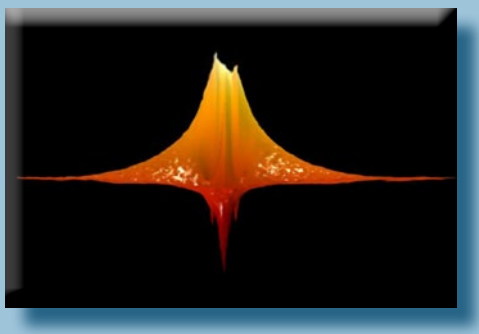

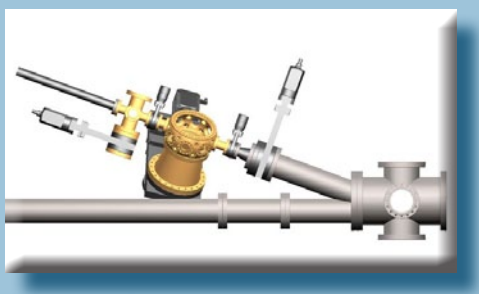

On the cover (From Top Right-Hand Side Top to Bottom):

1. *Thin film combinatorial "library" film for investigation of the dielectric properties of the HfO_2-TiO_2-Y_2O_3 ternary oxide system. The "library" film contains most of the compositions in this ternary system, and enables rapid screening of potential compositions for CMOS and DRAM applications.*
2. *Graphene Hall bar developed at NIST by undergraduate students.*
3. *Core-sleeve p-n GaN nanowire heterostructure. n-type Si-doped core and p-type Mg-doped sleeve are indicated. Core grown by MBE at NIST-Boulder, sleeve subsequently overgrown by HVPE at NIST-Gaithersburg.*
4. *A schematic of the cross section of an Atomic Layer Deposition reactor as configured with optical windows.*
5. *A 3D rendering of the stress field, as measured by confocal Raman microscopy, that surrounds a wedge indentation on Si(100).*
6. *End station on a synchrotron beamline for lifetime testing of EUV optics. Optics placed in gold-plated chamber are subjected to EUV irradiation in controlled atmospheres containing contaminants typical of those expected to be found in a commercial stepper.*

Middle Figure:

7. *End station on a synchrotron beamline to expose and measure outgassing from an EUV resist. The four-inch wafer sitting inside the cut away drawing of the flange is uniformly exposed with a prescribed EUV dose as the outgas is collected in the U-tube at the bottom of the figure.*

Semiconductor Microelectronics and Nanoelectronics Programs

NISTIR 7604

July 2009

U.S. DEPARTMENT OF COMMERCE
Gary Locke, Secretary

National Institute of Standards and Technology
Patrick D. Gallagher, Deputy Director

Disclaimer

Disclaimer: Certain commercial equipment and/or software are identified in this report to adequately describe the experimental procedure. Such identification does not imply recommendation or endorsement by the National Institute of Standards and Technology, nor does it imply that the equipment and/or software identified is necessarily the best available for the purpose.

References: References made to the International Technology Roadmap for Semiconductors (ITRS) apply to the most recent edition, dated 2007.

Semiconductor Industry Association. *The International Technology Roadmap for Semiconductors, 2007 edition.* SEMATECH: Austin, TX, 2007.

These documents are available on-line at: http://www.itrs.net for downloading.

The reader will notice that there are acronyms and abbreviations throughout this document that are not spelled out due to space limitations. We have listed the acronyms and abbreviations in an appendix at the end of this document.

Contents

Welcome and Introduction

Welcome

The microelectronics industry supplies vital components to the electronics industry and to the U.S. economy, enabling rapid improvements in productivity and in new high technology growth industries such as electronic commerce and biotechnology. The National Institute of Standards and Technology, NIST, in fulfilling its mission of strengthening the U.S. economy, works with industry to develop and apply technology, measurements and standards and applies substantial efforts on behalf of the semiconductor industry and its infrastructure. This report describes the many projects being conducted at NIST that constitute that effort.

Historical Perspective

NIST's predecessor, the National Bureau of Standards (NBS), began work in the mid-1950s to meet the measurement needs of the infant semiconductor industry. While this was initially focused on transistor applications in other government agencies, in the early 1960s the Bureau sought industry guidance from the American Society for Testing and Materials (ASTM) and the U.S. Electronic Industries Association (EIA). ASTM's top priority was the accurate measurement of silicon resistivity. NBS scientists developed a practical nondestructive method ten times more precise than previous destructive methods. The method is the basis for five industrial standards and for resistivity standard reference materials widely used to calibrate the industry's measurement instruments. The second project, recommended by a panel of EIA experts, addressed the "second breakdown" failure mechanism of transistors. The results of this project have been widely applied, including solving a problem in main engine control responsible for delaying the launch of a space shuttle.

From these beginnings, by 1980 the semiconductor metrology program had grown to employ a staff of 60 with a $6 million budget, mostly from a variety of other government agencies. Congressional funding in that year gave NBS the internal means to maintain its semiconductor metrology work. Meeting industrial needs remained the most important guide for managing the program.

Industrial Metrology Needs

By the late 1980s, NBS (now NIST) recognized that the semiconductor industry was applying a much wider range of science and engineering technology than the existing NIST program was designed to cover. The necessary expertise existed at NIST, but in other parts of the organization. In 1991, NIST established the Office of Microelectronics Programs (OMP) to coordinate and fund metrological research and development across the agency, and to provide the industry with easy single point access to NIST's widespread projects. Roadmaps developed by the U.S. Semiconductor Industry Association (SIA) have independently identified the broad technological coverage and growing industrial needs for NIST's semiconductor metrology developments. As the available funding and the scope of the activities grew, the collective name became the National Semiconductor Metrology Program (NSMP), operated by the OMP.

The NSMP has stimulated a greater interest in semiconductor metrology, motivating most of NIST's laboratories to launch additional projects of their own and to cost-share OMP-funded projects. The projects described in this book represent this broader portfolio of microelectronics projects. Most, but not all, of the projects described are partially funded by the NSMP, which is providing a $12 million budget in fiscal year 2008.

Fostering NIST's Relationships with the Industry

By the late 1980s, NBS (now NIST) recognized that the semiconductor industry was applying a much wider range of science and engineering technology than the existing NIST program was designed to cover. The necessary expertise existed at NIST, but in other parts of the organization. In 1991, NIST established the Office of Microelectronics Programs (OMP) to coordinate and fund metrological research and development across the agency, and to provide the industry with easy single point access to NIST's widespread projects. Roadmaps developed by the U.S. Semiconductor Industry Association

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Fostering Nist's Relationships With the Industry

NIST's relationships with the SIA, SEMATECH and its subsidiary, International SEMATECH Manufacturing Initiative (ISMI), and the Semiconductor Research Corporation (SRC) are also coordinated through the OMP. Staff from OMP and NIST Laboratories represents NIST on the SIA committees that develop the International Technology Roadmap for Semiconductors (ITRS), as well as on numerous SRC Technical Advisory Boards. NIST staff is also active in the International National Electronics Manufacturers Initiative (iNEMI), the EIA, the International Organization for Standardization (ISO), and Semiconductor Equipment and Materials International (SEMI). NIST supports the United States National Committee Technical Advisory Group for the International Electrotechnical Commission Technical Committee TC113 on Nanotechnology Standardization for Electrical and Electronic Products and Systems (Technical Advisor, USNC TAG for IEC TC 113 on nanotechnology) by funding the Technical Advisor to that organization.

Learn More About Semiconductor Metrology at NIST

This publication provides summaries of NIST's metrology projects for the silicon semiconductor industry and their suppliers of materials and manufacturing equipment. Each project responds to one or more metrology requirements identified by the industry in sources such as the ITRS. NIST is committed to listening to the needs of industry, working with industry representatives to establish priorities, and responding where resources permit with effective measurement technology and services. For further information, please contact:

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Lithography Metrology Program

Advances in lithography have largely driven the spectacular productivity improvements of the integrated circuit industry, a steady quadrupling of active components per chip every three years over the past several decades. This continual scaling down of transistor dimensions has allowed more and more components on a chip, lowered the power consumption per transistor, and increased the speed of the circuitry. The shrinking of device dimensions has been accomplished by shortening the wavelength of the radiation used by the lithography exposure tools. The workhorse tools at this point operate at 193 nm. In order to further shrink dimensions liquid immersion tools with water as the immersion fluid have been introduced. Further size reduction through the use of high index fluids, lens materials and photoresist for 193 nm tools are under intense exploration for even higher numerical aperture systems. Looking beyond the deep ultraviolet, extreme ultraviolet radiation (EUV) at 13 nm is being investigated, and demonstration tools are being designed and assembled. At least three alpha tools were shipped to development consortia in 2006. The overall goal of this task is to support these developments in DUV and EUV. The areas of emphasis are characterization of lens materials and immersion fluids, laser calorimetry, radiation detector sensitivity and damage, EUV lens metrology, and metrology for the development of advanced photoresist materials for both DUV and EUV.

Metrology Supporting Deep Ultraviolet Lithography

Technical Contacts:
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S. G. Kaplan

"It's an excellent service NIST has performed for the entire industry. The kind of thing NIST is there for – to identify issues before the train wreck takes place."

Mordechai Rothschild,
Massachusetts Institute
of Technology's
Lincoln Laboratory

Goals

Develop solutions to key optical materials issues confronting the semiconductor lithography industry. These include development of measurement methods for characterizing the optical properties of deep ultraviolet (DUV) materials, delivering optical measurements of key lithography materials to the high accuracy needed by the industry, and investigating exposure effects on the optical properties, including nonlinear effects and exposure damage.

Customer Needs

Increasing information technology requirements have created a strong demand for faster logic circuits and higher-density memory chips. This demand has led to the introduction of DUV laser-based lithographic tools for semiconductor manufacturing. These tools, which employ KrF (248 nm) and ArF (193 nm) excimer lasers, have led to an increased demand for accurate optical measurements at DUV laser wavelengths.

193 nm immersion lithography, with water as an immersion fluid, is now being commercially implemented with numerical apertures near 1.3, enabling the 45 nm technology node. Extension of 193 nm technology to the 32 nm and 22 nm nodes is being considered, using double patterning and/or high-index immersion fluids and optical elements. In any case, requirements will be tightened for the optical material quality and for the accuracy of measurements of the optical properties, such as birefringence, refractive index, and thermo-optic coefficient. If the high-index materials approach is pursued, accurate measurements for the properties of these new materials are needed. In addition, accurate determination of the optical properties of new materials will be needed for metrology tools to be developed for these feature sizes, and for alternative leading edge lithography technologies, such as interference lithography.

To support these efforts, the National Institute of Standards and Technology (NIST), with

SEMATECH support, has developed a DUV metrology program focusing on the characterization of DUV optical materials.

The potential challenges for lithographic development are discussed in the 2007 International Technology Roadmap for Semiconductors. Page 1 of the Lithography section states: "Significant technical challenges exist in extending optical projection lithography at 193 nm wavelength using high-index immersion lenses…." The need for advancing metrology in lithography is discussed on page 1 of the Metrology section: "Metrology continues to enable research, development, and manufacture of integrated circuits. The pace of feature size reduction and the introduction of new materials and structures challenge existing measurement capability."

Technical Strategy

High-accuracy measurements of the index properties of UV materials are required for the design of DUV lithography systems. NIST has been providing absolute index measurements at 193 nm and 157 nm with an accuracy of about 5 ppm to the industry using its DUV minimum-deviation-angle refractometer. To improve on this absolute accuracy, NIST has constructed a new state-of-the-art minimum-deviation system and separately developed a complementary system based on a vacuum ultraviolet (VUV) Fourier transform spectrometer and synchrotron radiation as a continuum source (see Fig. 1). The minimum-deviation system enables measurements to an accuracy of 1 ppm. Using an index measurement with this system at one wavelength, the FT spectrometer system determines the entire dispersion curve from the visible through the VUV (down to 150 nm) to this accuracy. These systems are built with accurate temperature control to determine the thermo-optic coefficients.

DELIVERABLES:

- Measurement of the refractive index of fused silica, calcium fluoride, and water, as well as high-index fluids and high-index lens materials, with an accuracy of 1 ppm. Accurate measurements of the thermo-optic coefficients of these materials. Ongoing.

Taking full advantage of the potential resolution gain with immersion lithography may require using high-index materials for the last lens element, though as yet no such material has been demonstrated at 193 nm. Even with double patterning approaches being projected to satisfy the

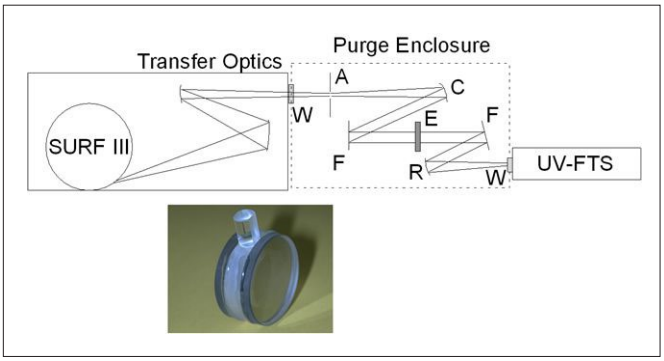

Figure 1a

Figure 1a and 1b. Optical layout and etalon cell design (E) for interferometric measurements of refractive indices of fluids using synchrotron radiation source, SURF III. b) VUV Fourier transform (FT) spectrometer used with synchrotron radiation source for index measurements.

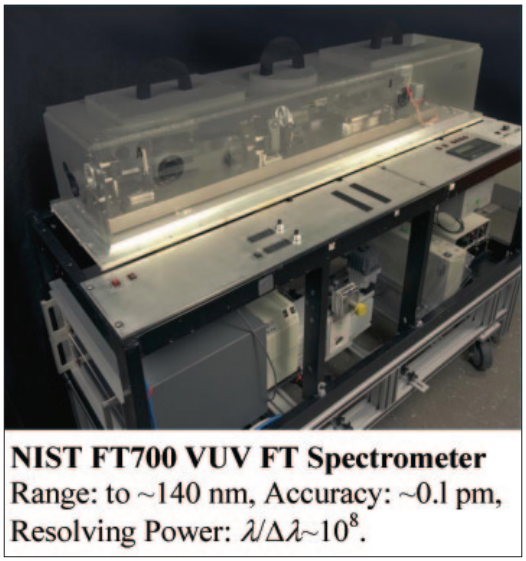

Figure 1b

requirements of the 32 nm technology node, the high-index materials approach is complementary to this and can be used to extend one further generation or can be used to widen the depth of focus and process window (relax k1 factors). To address this possibility we have, with the support of SEMATECH, undertaken and completed a survey of candidate materials. As a result of this work, we have identified two very promising materials, ceramic spinel and lutetium aluminum garnet (LuAG). Both materials have index near 2.0 at 193 nm and have the potential for high optical quality at this wavelength. In addition, the intrinsic birefringence is low for LuAG and negligible for ceramic spinel. We are continuing to characterize the complete UV optical properties of these materials and other candidate materials. Since high-NA immersion lithography requires polarized illumination, a further high-index candidate material becomes possible, namely sapphire, a uniaxial crystal. Though a naturally birefringent material, selectively polarized illumination enables a restriction to the isotropic ordinary rays, and low-aberration optics becomes possible. In addition, the high natural birefringence has the advantage of minimizing the impact to imaging of the residual undesired polarization, a serious issue with isotropic lens materials. Sapphire is also being considered for key optical components for interference lithography. To assess the suitability of sapphire for lithography optics, we are working with leading UV sapphire suppliers to characterize its complete optical properties, including any spatial-dispersion-induced anisotropy effects.

DELIVERABLES:

- Fully characterize the 193 nm optical properties of LuAG, ceramic spinel, and sapphire: 2Q 2010.

A number of double-patterning approaches are being developed to extend 193 nm lithography to the 32 nm technology node and beyond. Chief difficulties with these approaches are the reduced process windows involved and the increased cost of two resist-processing steps per double-patterned layer. New nonlinear materials may provide some amelioration to these difficulties. Saturable absorbing materials used for contrast enhancement layers could increase process windows, and materials with high nonlinear response to 193 nm radiation, incorporated into the resist processing, could enable double-exposure technology to be implemented with one only resist-processing step per layer. We are setting up a pump-and-probe system with a unique tunable 193 solid-state laser in order to characterize the nonlinear response of promising nonlinear 193 nm materials. We developed a collaboration with a nanotechnology company to explore the potential for these applications of promising nonlinear materials based on nanocrystals.

DELIVERABLES:

- 193 nm pump-and-probe system operational and begin characterizing the nonlinear optical properties of promising nanocrystals: 2Q 2010.

An absolute light source in the DUV range based on synchrotron radiation using NIST's Synchrotron Ultraviolet Radiation Facility (SURF III) has been established using a dedicated beamline at SURF III. The flux of the DUV radiation at this

beamline can be known to very high accuracy through the well established equations governing the behavior of the synchrotron radiation. The beamline is designed for customer calibration of a variety of DUV instruments to assist the development of the DUV lithography such as monochromators, discharge lamps, and irradiance meters. The spectral range covers all of the current important wavelengths for semiconductor industry such at 248 nm, 193 nm, 157 nm, down to 13 nm. The uncertainty of such calibration is better than 1 % in the case of deuterium lamp calibration.

DELIVERABLES:

- Provide customer DUV calibration for discharge lamps, monochromators, and irradiance meters using SURF III source-based beamline with highest accuracy. Ongoing

Accomplishments

■ We have used our Hilger-Chance refractometer system to assist the industry in the search for appropriate high-index fluids (with n greater than water, 1.4366 at 193 nm) for possible use in immersion lithography resolution extension. Several promising fluids have been developed by industry, and we have characterized their UV optical properties. Recently we have worked with the suppliers to demonstrate that several of these candidate fluids have stable optical properties over multiple exposure runs. As a result of our high-index materials survey (see Fig. 2), we have identified two very promising high-index 193 nm transmitting materials with low intrinsic birefringence, that can potentially enable immersion lithography extension. These candidates are ceramic spinel and lutetium aluminum garnet (LuAG). We have demonstrated that both materials have good 193 nm optical properties, including sufficiently low spatial-dispersion-induced ("intrinsic") birefringence. Due to the results of our measurements, LuAG and ceramic spinel are now being assessed by the industry for this application.

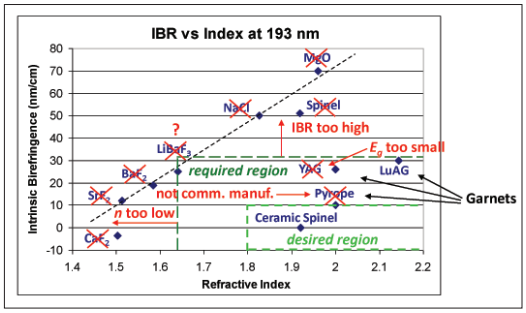

Figure 2. Measurements of refraction index versus intrinsic birefringence (IBR) for several candidate optical materials. Of these, only LuAG and cramic spinel meet the requirements of high 193 nm transparency, high index, and low IBR.

■ We have constructed a radiometric facility tailored for the DUV range using a beamline at NIST's SURF III with the radiation measurement scale derived from a high-accuracy cryogenic radiometer. The beamline is designed for general-purpose high-accuracy measurements. We have used this facility to measure DUV material properties such as transmission and reflectance. Examples of such measurements include DUV mirrors, windows, filters, and also the transmission and absorption of liquids that could be used for immersion lithography. On the detector side, we have calibrated and characterized a variety of DUV detectors such as solid state photodetectors, solar-blind detectors, photoconductive detectors, and pyroelectric detectors. We also performed irradiance calibrations for DUV irradiance meters.

■ We have also developed the capability to characterize the nonlinear response of 193 nm and 248 nm excimer laser detectors based on the correlation method. The method and system solves measurement difficulties associated with the temporal and spatial fluctuations of excimer laser pulse energy. Using this system, one can easily discover problems such as those due to the incident pulse energy, range discontinuities associated with detector gain, and detector background noise (see Fig. 3).

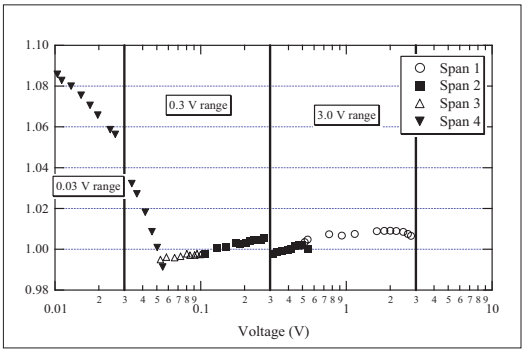

Figure 3. Nonlinearity measurement result of a 193 nm pulsed laser energy detector. CF is the correction for the detector's nonlinear response. The response is measured in four spans, covering 2.5 meter settings. The large degree of nonlinearity at the low end of the meter range is due to background effects.

Collaborations

DuPont, Roger French, immersion photolithography fluid development. Schott Lithotec, Lutz Partier, high index lithography materials development.

Publications

S. G. Kaplan and J. H. Burnett, *"Optical properties of fluids for 248 nm and 193 nm immersion photolithography,"* Applied Optics 45, 1721 (2006).

John H. Burnett, Simon G. Kaplan, Eric L. Shirley, Deane Horowitz, Wilfried Clauss, Andrew Grenville, and Chris Van Peski, *"High-index optical materials for 193-nm immersion lithography,"* in Optical Microlithography XIX, edited by Donis G. Flagello, Proc. of SPIE Vol. 6154 615418 (SPIE, Bellingham, WA, 2006).

John H. Burnet, Eric C. Benck, Simon G. Kaplan, Gabriel Sirat, and Chris Mack, *"Birefringence issues with uniaxial crystals as last lens elements for high-index immersion lithography"*, SPIE Advance Lithography 7274, 727473 (2009).

Metrology Supporting Extreme Ultraviolet Lithography

Goals

Provide leading-edge metrology for the development and characterization of sources, optical components, and dosimeters used in Extreme Ultraviolet Lithography (EUVL). (EUVL utilizes radiation at 13.4 nm.)

Customer Needs

An intense international effort is presently underway to install EUVL into commercial production in 2012 at the 22 nm node. ASML has delivered two alpha-generation steppers for initial testing, one to SEMATECH in Albany and one to IMEC in Belgium. Several significant challenges to commercialization of EUVL remain, including source power, optics lifetime, and optics and mask fabrication. The associated metrological challenges include the development of: (1) highly precise extreme ultraviolet (EUV) reflectometry; (2) accurate EUV radiometry for source comparisons, wafer-plane dosimetry, and resist characterization; and (3) predictors of EUV optics lifetimes.

Technical Strategy

1. Precise EUV Reflectometry

The NIST/DARPA EUV Reflectometry Facility is located on a multipurpose beamline on the NIST Synchrotron Ultraviolet Radiation Facility (SURF III) storage ring. Currently the NIST/DARPA facility is the only one in the U.S. large enough to measure optics up to 40 cm in diameter and 40 kg in mass. The facility has a demonstrated reflectivity accuracy of 0.3 % and wavelength accuracy of 0.001 nm, with plans underway to improve each in the near future.

The Facility serves the EUVL community by providing accurate measurements of multilayer mirror reflectivities and radiometric measurements on fully assembled instruments. Among the recent activities in support of EUVL is the reflectivity map made of the very large condenser mirror for a leading source manufacturer, the radiometric calibration of the "Flying Circus II" and "E-Mon" radiometers used for the comparison of source outputs, and reflectivity measurements made to determine the reflectivity loss due to resist outgassing. The reflectivity of a typical mirror designed for use in a EUVL stepper is shown in Fig. 1.

DELIVERABLES:

- Full reflectivity maps of EUV mirrors up to 40 cm in diameter and 45 kg in mass on an as needed basis for the EUVL community. Many other types of EUV measurements including EUV filter transmission and cw radiometric calibrations of fully assembled filter radiometers used in source comparisons.

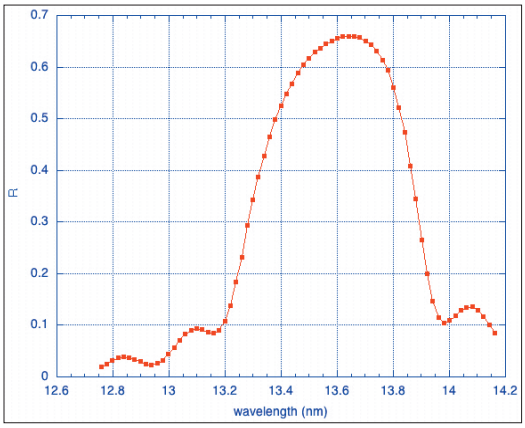

Figure 1. Reflectivity vs. wavelength of a typical MoSi multilayer mirror. The measurement was made at 5° from normal incidence.

2. EUV Dosimetry

NIST is the primary national source for the radiometric calibration of detectors from the infrared to the soft X-ray regions of the spectrum. The Photon Physics Group is responsible for maintaining the spectral responsivity standards in the far- and extreme-ultraviolet spectral regions, including 13.5 nm, the EUVL wavelength of interest. We operate several beamlines at the SURF III synchrotron radiation facility, a quasi-cw source, as well as a laser-produced plasma source that is pulsed with a 10ns pulse length. With these facilities, we can calibrate EUV detectors and dosimeter packages under either cw or pulsed conditions.

NIST has recently added the capability to measure the absolute sensitivity of EUV photoresists. Until recently, EUV photoresist sensitivity was referenced to a "standard" photoresist whose sensitivity had last been measured in the 1990s. Late in 2007, scientists at the Advanced Light Source in Berkeley, CA used a NIST-calibrated EUV photodetector to validate this resist-based

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C. Tarrio
S. Grantham
S. Hill
R. Vest

transfer standard method. Their detector-based measurements indicated that the sensitivity of a modern resist was about twice the obtained using the resist-based calibrations. Subsequently NIST established the capability for the accurate measurement of EUV resist sensitivity to independently validate these surprising results. The NIST measurements confirmed the findings of the much higher resist sensitivity made in Berkeley thus showing the resist-based standard that was used to be erroneous and demonstrating the importance of periodically checking such derived "standards" against measurements traceable to reliably calibrated instruments

DELIVERABLES:

- Photodiodes and other EUV radiometric devices as needed basised on customer requests
- Radiometric calibrations as needed basised on customer requests
- Resist dose to clear Eo measurements on customer as needed basised requests

3. Study of Factors Affecting EUV Optics Lifetime

One of the potential showstoppers for commercialization of EUVL is the degradation of the multilayer-mirror stepper optics. The mirrors lose reflectivity because adsorbed contaminant gases such as hydrocarbons and water are cracked by the energetic (13.5 nm) photons. This leads to growth of an amorphous carbon layer on the optics surfaces or to oxidation. The former effect is largely reversible; however, the latter is not. Unfortunately, these ambient contaminants cannot be eliminated by baking because the alignment of the mirror stack cannot be maintained to the necessary submicron tolerances at elevated temperatures and because of the presence of the organic species in the outgassing from the resist coated wafer as it is being exposed.

The oxidation and carbonization are actually competing processes, and preliminary demonstrations have shown that the addition of a hydrocarbon can result in the deposition of a sacrificial layer of carbon that inhibits the oxidation of the cap layer that is used to protect the optic. The present strategy by the stepper manufacturers is to attempt to find a point in the oxidation-carbonization balance that leaves an oxidation-resistant cap layer, such as ruthenium, undamaged.

To study the effectiveness of such a strategy and to better understand the underlying processes responsible for mirror degradation, NIST has installed two beamlines at the Synchrotron Ultraviolet Radiation Facility (SURF III) that can expose capped-multilayer samples to ≈ 6 mW/mm^2 of 13.5 nm radiation in an environment of controlled water or hydrocarbon partial pressures up to 6.7×10^{-4} Pa. To date the most oxidation-resistant capping layers available have been ≈ 2 nm of ruthenium or ≈ 2 nm of titanium dioxide. Our exposure facility has demonstrated that multilayers with these capping layers suffer approximately one-tenth the reflectivity loss of bare Si-capped multilayers when exposed for ≈ 100 h under rather aggressive oxidation conditions of 1×10^{-4} Pa of water vapor. In addition to measuring the reflectivity loss of exposed multilayers, the photon-induced chemistry on the mirrors is characterized using a range of surface analysis techniques including micro XPS.

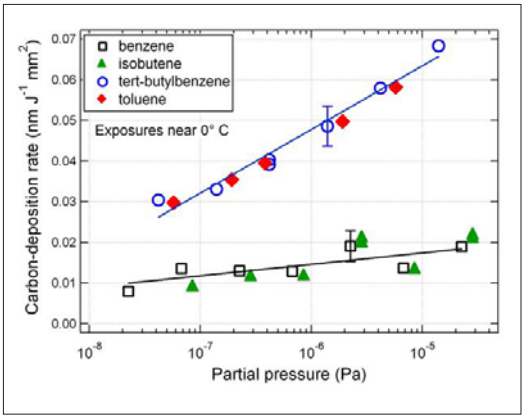

Figure 2. Carbon growth rates on TiO^2-capped trilayers samples for four anticipated contaminant gases. Straight-line fits for benzene and tert-butylbenzene show logarithmic pressure dependence across 3 decades of pressure. The error bars reflect the relative uncertainty due primarily to counting statistics of XPS measurements.

The dominant mechanism of reflectivity loss of optics observed in pre-production tools has been carbon deposition. As shown in figure 2, high-dose exposures performed in our facilities have revealed very different rates of carbonization for different gases and a distinctly non-linear, quasi-logarithmic dependence of these rates on partial pressure. Ongoing work is focused on learning more about the pressure dependence of the carbonization rates in the very low pressure regions to allow for better predictions of such rates in an actual stepper.

Each of the various organic molecules emitted by an irradiated resist or other material in the stepper vacuum will have a different effect on the optics. NIST has devised two new methods in an attempt to identify and quantify both the organic species in a stepper vacuum and those emanating from an irradiated resist. The first uses a vacuum cryo-trap to obtain a sample from a stepper vacuum which is later subjected to Gas Chromatography followed by Mass Spectrometry (GC/MS) analysis in a specially equipped gas chromatograph, and the second uses a special chamber that can be hooked up to an EUV source to irradiate a 4 inch wafer, collect the outgas, and measure the total outgas per unit area by the pressure rise method and quantitatively analyze the collected outgas with the same cryo-trapping plus GC/MS technique as for the stepper vacuum.

In addition to expanding our facilities, we have also established very fruitful collaborations with experts in surface science both within and outside the NIST community.

DELIVERABLES:

- Identify and quantify EUV resist outgas for resist manufacturers, tool makers, and tool users on an as needed basis.
- Rank reflectivity loss as a function of organic species and the presence of mitigating oxidative species according to industry needs.

Collaborations

Rutgers University, Tulane University, CNSE at the State University in New York (Albany), Intel, Fraunhofer Institute, Jena, Germany, and SEMATECH

Publications

S.B. Hill, N. Faradzhev, C. Tarrio, T.B. Lucatorto, B. Yaskshinkiy, T.E. Madey, and S. Yulin, "Measuring the EUV-induced contamination rates of TiO2-capped multilayers by anticipated tool-environment hydrocarbons," Proc. SPIE Vol. 7271, 7271-13 (2009).

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C. Tarrio, R.E. Vest, T.B. Lucatorto, and R. Caudillo, "Tracking down the sources of carbon contamination in EUVL exposure tools," Proc. SPIE Vol. 7271, 7271-38 (2009).

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R. E. Vest, S. Hill, and S. Grantham, "Saturation effects in solid-state photodiodes and impact on EUVL pulse energy measurements," Metrologia 43, S84-S88 (2006).

C. Tarrio and S. Grantham, "A synchrotron beamline for extreme-ultraviolet multilayer mirror endurance testing," Rev. Sci. Instrum. 76, 056101 (2005).

Polymer Photoresist Fundamentals for Next-Generation Lithography

Technical Contacts:
V. M. Prabhu
E. K. Lin
W. L. Wu

"[This team has] made seminal contributions to the field of lithography in elucidating the effects that contribute to line edge roughness using the unique technical capabilities and know-how of NIST. Their successful cooperation with industry partners and research organizations has been both scientifically outstanding as well as a model of how to implement such joint research efforts."

Ralph Dammel, AZ Electronics

Goals

In this project, we are developing an integrated program involving fundamental studies of photoresist materials to be correlated with resist performance metrics impacting next generation photolithography. We work closely with industrial collaborators to develop and apply high spatial resolution and chemically specific measurements to understand varying material properties and process kinetics at nanometer scales and to provide high quality data needed in advanced modeling programs. This program provides a detailed foundation for the rational design of materials and processing strategies for the fabrication of sub 32 nm structures. The unique measurement methods we apply include specular and off-specular X-ray and neutron reflectivity (XR, NR), small-angle neutron scattering (SANS), near-edge X-ray absorption fine structure (NEXAFS) spectroscopy, quartz crystal microbalance (QCM), solid state nuclear magnetic resonance (NMR), atomic force microscopy (AFM), infrared variable angle spectroscopic ellipsometry (IR-VASE), polarization-modulation infrared reflectance spectroscopy (PMIRRAS) and matrix assisted laser desorption/ionization time of flight mass spectrometry (MALDI-TOF MS). Our efforts focus on the fundamentals of polymeric materials and processes that control the resolution of the photolithography process including: (1) the photoresist architecture and polymer conformation within sub 32 nm structures; (2) the spatial segregation and distribution of critical photoresist components; (3) the transport and kinetics of photoresist components, and the deprotection reaction interface over nanometer distances; (4) the material sources of line-edge roughness (LER), a measure of the ultimate resolution of the lithographic process; (5) the polymer physics of the developer solution and the dissolution process; and (6) influence of moisture on the thermophysical properties of interfaces as applicable to immersion lithography. These data are needed to meet future lithographic requirements of sub 32 nm imaging layers and critical dimensions.

Customer Needs

Photolithography remains the driving and enabling technology in the semiconductor industry to fabricate integrated circuits with ever decreasing feature sizes. Today, current fabrication facilities use chemically-amplified photoresists, complex and highly tuned formulations of a polymer film loaded with photoacid generators (PAGs) and other additives. Upon exposure of the photoresist film through a mask, the PAG creates acidic protons. A post-exposure bake is then applied and the acid protons diffuse and catalyze a deprotection reaction on the polymer that alters its solubility for development in an aqueous base solution. These reaction-diffusion and development processes must be understood and controlled at the nanometer length scale to fabricate integrated circuits. Chemically amplified resists are also deposited onto bottom anti-reflection coatings (BARCs). Interactions and component transport between the BARC and resist layer can lead to loss of profile control or pattern collapse. Detailed studies of these interaction and transport mechanisms are needed to design materials for the successful fabrication of sub 32 nm structures.

There are significant challenges in extending this technology to fabricate the smaller feature sizes (sub 32 nm) needed to continue increasing performance in integrated circuits. First, new radiation sources with shorter wavelengths, 193 nm or extreme-ultraviolet (EUV), require photoresist films nearing 100 nm thickness to ensure optical transparency and uniform illumination. In these ultra-thin films, confinement can induce deviations in several key materials parameters such as the macromolecular chain conformation, glass transition temperature, component distribution, and transport properties. Furthermore, the required resolution for a sub 32 nm feature will be on the order of 2 nm, approaching the macromolecular dimensions of the photoresist polymers. It is not yet clear how deviations due to confinement will affect the ultimate resolution in these photoresist films. Additionally, the material sources of feature resolution (line-edge roughness (LER) and line-width roughness (LWR)) and profile control need to be identified and understood to ensure the success of needed patterning technologies.

The requirements for advanced photoresists are discussed in the 2007 International Technol-

"[This team has] made ground breaking contributions to the fundamental understanding of resist line edge roughness —a technological bottleneck that threatens to derail the continuing miniaturization of the semiconductor devices."

Qinghuang Lin, IBM

"... I just finished a presentation for AMD on your work. Every time I look at it, the framework that has been established seems more and more valuable for future work. ... AMD is a huge proponent of what you have done."

Karen Turnquest, AMD, SEMATECH, Lithography

ogy Roadmaps for Semiconductors on page 10, Lithography Section. Table LITH2 on "Lithography Difficult Challenges" for resist materials at < 32 nm indicates three issues (1) Resist and antireflective coating materials composed of alternatives to PFAS compounds, (2) Limits of chemically amplified resist sensitivity for < 32 nm half-pitch due to acid diffusion length, and (3) materials with improved dimensional and LWR control.

Technical Strategy

In this project, model photoresist materials are used to validate the new measurement methods. Model materials (applicable to 193 nm and EUV lithography) address several important fundamental questions including the thermal properties of ultra-thin films as a function of film thickness and substrate type, the conformation of polymer chains confined in ultra-thin films, the surface concentration of PAGs, the diffusion and the deprotection reaction kinetics, and the physics of the development process. These results provide a basis for understanding the material property changes that may effect the development of lithography for sub-32 nm structures using thin photoresist imaging layers. Detailed experimental investigation of the interaction between model photoresists and BARC materials is also required to optimize the materials factors impacting lithographic performance. Each process step requires an interdisciplinary array of experimental techniques to measure the polymer chemistry and physics in thin films as shown in Fig. 1.

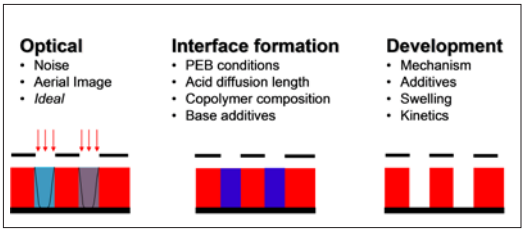

Figure 1. Key lithographic process steps studied for materials fundamentals.

DELIVERABLES:

- Publish methods to analyze polymer multilayers by IR variable-angle spectroscopic ellipsometry (IR-VASE). 1Q2009
- Publish molecular glass / photoacid generator dispersion extent by solid state NMR. 1Q2009
- Contribute photoresist section for invited book chapter on Nanoelectronics Lithography for the Handbook of Nanophysics. 1Q2009
- Publish manuscript on the application of synthetic mica as thin film substrates for solid state NMR; techniques for photoresist/ photoacid generator dispersion. 2Q2009
- Advance the metrics for EUV photoresists for sub-22 nm features using experimental approaches. 2Q2009
- Apply reaction kinetics models to analyze commercial EUV photoresists as a function of dose, PEB time, and component concentration. 2Q2009
- Obtain specially deuterated molecular glass resists through collaboration. 2Q2009
- Develop mass spectrometry to characterize molecular glass resist polydispersity. 2Q2009
- Quantitatively compare photoacid diffusion lengths of molecular glass resists with traditional polymeric chemically amplified resists.4Q2009
- Characterize the photoacid diffusion length in molecular resist using neutron reflectivity with nanometer resolution. 4Q2009.

Accomplishments

■ EUV photoresist polymers are expected for imaging at the 22 nm node and smaller, however, resists are challenged to simultaneously meet resolution, dose sensitivity, and LER requirements. Similar to 193 nm (dry and immersion) lithography, the deprotection reaction front profile at the interface between exposed and unexposed resist is a critical factor. However, EUV photoresists in particular use high PAG loading and expect to use lower EUV doses. The effect of architecture or pixel size may also play a crucial role to achieve higher fidelity imaging. The fundamentals of critical additives, such as photodegradable bases, photoacid generator (PAG) structure, and contrasting architecture, shown in Fig. 2, are investigated.

■ The deprotection reaction front profile was The deprotection reaction front profile was measured with nanometer resolution by combining neutron reflectivity and Fourier transform infrared (FTIR) spectroscopy on a bilayer structure that mimics the lithographic line-edge (Fig. 3) prepared with model EUV and 193 nm photoresists. The upper layer of the structure is loaded with the photoacid generator. Upon exposure and baking, the acid diffuses into the lower layer and catalyzes the deprotection reaction. The protecting group leaves the film upon reac-

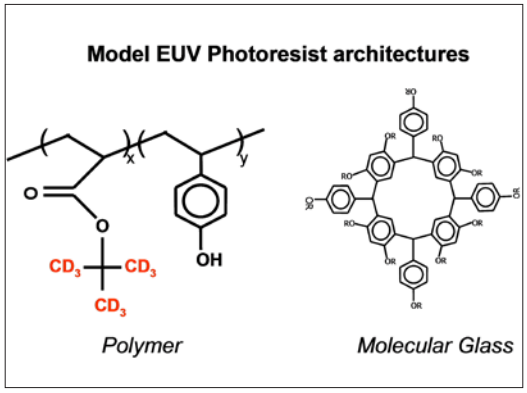

Figure 2. Two contrasting architectures of photoresist materials, but with similar chemistry: molecular glass and polymeric chemically amplified resist.

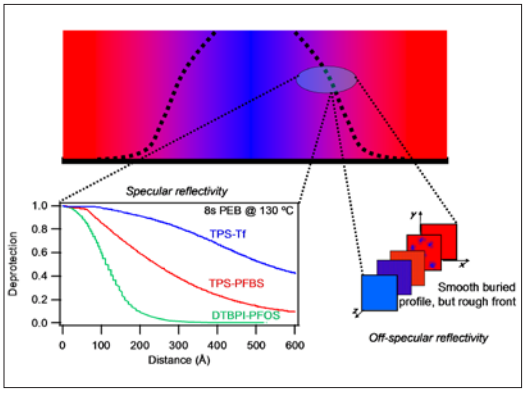

Figure 3. Specular neutron reflectivity results of the nanometer scale deprotection profile shape dependence on photoacid generator size: TPS-Tf < TPS-PFBS < DTBPI-PFOS; Highlight of the buried chemical heterogeneity measured at the reaction-front by off-specular reflectivity. These high-resolution experimental data help verify current advanced reaction-diffusion models.

tion. The contrast to neutrons results from the reaction allowing for measurement of the reaction front. By comparing the reaction front to the developed film profile, we obtain important insight into both the spatial extent of the reaction and the development process itself. These data, which are the first available with this spatial resolution, are needed for the development of process control over nanometer length scales. We find that the reaction front broadens with time while the surface roughness of the developed structure remains relatively sharp. Additionally, we find that the reaction front width is dependent upon resist chemistry and PAG size as shown in Fig. 3. Neutron reflectivity was demonstrated to have sufficient chemical sensitivity and spatial resolution to measure the interfacial structure on sub-nm length scales.

■ A combination of specular and off-specular neutron reflectivity was used to measure the buried lateral roughness of the reaction-diffusion front in a model EUV photoresist. Compositional heterogeneities at the latent reaction-diffusion front have been proposed as a major cause of LER in photolithographic features. We measured the longitudinal and lateral compositional heterogeneities of a latent image, revealing the buried lateral length scale as well as the amplitude of inhomogeneity at the reaction-diffusion front. These measurements aid in determining the origins of LER formation, while exploring the material limits of the current chemically amplified photoresists. These unique measurement methods aid in determining the specific influence of photoresist components, resist chemistry, and the reaction-diffusion process.

■ In addition to applying depth profiling methods, the kinetics of the deprotection reaction were studied as a function of copolymer composition with FTIR spectroscopy. Three methacrylate-based copolymers with varying compositions of acid-labile and non-reactive (lactone) monomers were studied. A mathematical model was developed to analyze the acid catalyzed deprotection kinetics with respect to coupled reaction rate and acid-diffusion processes. The first order reaction rate constant decreases as the non-reactive comonomer content is increased. Additionally, the extent of reaction appears self-limiting as verified by a slowing down that requires an acid-trapping chemical equation to model the data. An example is shown in Fig. 4 (next page). This composition-dependent reaction constant indicates a strong interaction of the acid with the increasingly polar resist matrix that drastically reduces acid transport. The reduced acid transport is consistent with hydrogen bonding between photoacid and methacrylic acid product. These results demonstrate a correlation between the polymer microstructure and acid catalyzed kinetics. These measurements are necessary for analysis of coupled reaction-diffusion processes. Finally, the models were applied to understand the limiting spatial extent of photoacid diffusion at the model line edge determined by neutron reflectivity. These measurement methods have been successfully applied to commercial EUV photoresist materials to predict the acid diffusion length.

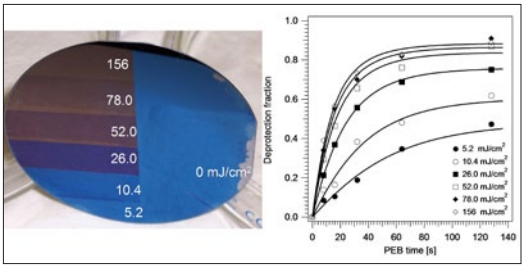

Figure 4. Wafer after exposure to varied DUV dose and fixed baking time. The color change represents slight changes in film thickness with extent of reaction. Quantification of the extent of reaction (deprotection fraction) versus post-exposure bake time for model 193 nm resist for varying dose.

■ The chemical latent image determines the nanoscale regions of resist that are soluble in the aqueous base developer solution that produces the final pattern. As these feature dimensions approach sub-32 nm, however, a possible trade-off among process variables may limit photoresists from achieving less than 2 nm LWR design criteria. A central assumption in these resolution limit models is a direct transfer of the chemical latent image heterogeneity to the feature. Insight into the mechanism of development, rinse, and drying at a gradient line edge was achieved by neutron reflectivity with nm resolution. Direct measurements of the highly swollen photoresist polymer, deuterium labeled developer (d-TMA+) and aqueous solvent profiles at the developed line-edge clearly highlights a residual swelling fraction with spatial dimensions that exceed the radius of gyration (Rg) of the photoresist polymer (Fig.5).

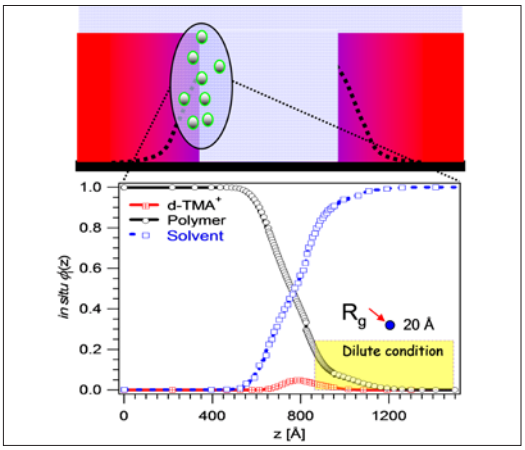

Figure 5. Neutron reflectivity results of the in situ composition profiles of resist, developer ions, and solvent at the model line-edge highlighting a residual swelling fraction.

■ The final surface roughness is formed by the collapse of this highly associated phase during the drying process. However, an ideal collapse and elimination of surface roughness was not observed. The mechanism of a simple transfer of roughness from the latent image to the developed image is challenged by these data. Future simulations and models should include both percolation and penetration of developer and an associative polymer behavior due to the heterogeneity and large hydrophobicity difference of resist components. Extending these concepts to previous latent image analysis imply the smallest residual swelling fraction provides the lowest roughness. This can be achieved through resist and optical design to provide the highest latent image profile slope. Quartz crystal microbalance measurements, a transferable measurement method, provides an added capability to measure the kinetics of swelling and collapse, however, the profile and chemical specificity are exclusively obtained with NR.

■ NEXAFS measurements were used to measure the surface concentration and depth profile of photoresist and BARC components and the surface reaction kinetics in model photoresist polymers as a function of common processing conditions. A significant advantage of the NEXAFS measurement is the capability of separating interfacial and bulk signals within the same sample and experiment. The instrument located at Brookhaven National Laboratory beam line U7A as shown in Fig. 6. NEXAFS measurements of interfacial chemistry are possible because of the limited escape depth of produced secondary electrons. By separately observing the electron and fluorescence yield, the chemistry at the surface (2 nm) and bulk (200 nm) may be determined. Different chemistries may be observed by examining the near-edge X-ray spectra of light elements such as carbon, oxygen, fluorine, and nitrogen. In this way, changes in the surface chemistry relative to the bulk film can be investigated as a function of lithographic processing steps such as exposure and heating. We have found that fluorinated PAG molecules preferentially segregate to the film surface. The relative amount of segregation is dependent upon the specific polymer chemistry and PAG size. In addition, NEXAFS analysis of residual layers arising from BARC-resist component transport and interactions enable detailed analysis of potential mechanisms leading to loss of profile control. UV exposure, post-exposure bake, and a novel atmosphere controlled chamber have been developed to test environmental stabil-

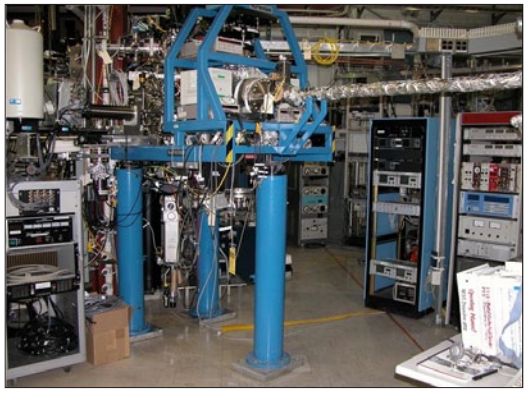

Figure 6. NEXAFS instrument at the U7A beam line, Brookhaven National Laboratory, National Synchrotron Light Source. Image courtesy of Dr. Daniel Fischer

ity against model airborne contaminants and its influence on in situ processing.

■ NEXAFS measured the surface concentration and depth profile of photoacid generators for advanced 193 nm photoresist materials for immersion lithography. These measurements quantify the influence of water immersion on surface composition and the loss of these critical components. NEXAFS on-wafer analysis combined with liquid chromatography/mass spectrometry (LC/MS) demonstrate that the equilibrium water solubility of photoacid generators with varying perfluoroalkyl length does not serve as the appropriate selection criteria for immersion lithography; rather the segregation of photoacid generators to the top few nanometers provides the majority of leaching as shown in Fig. 7. Additionally, the effects of critical top coats were also investigated to understand the segregation and retention of additives.

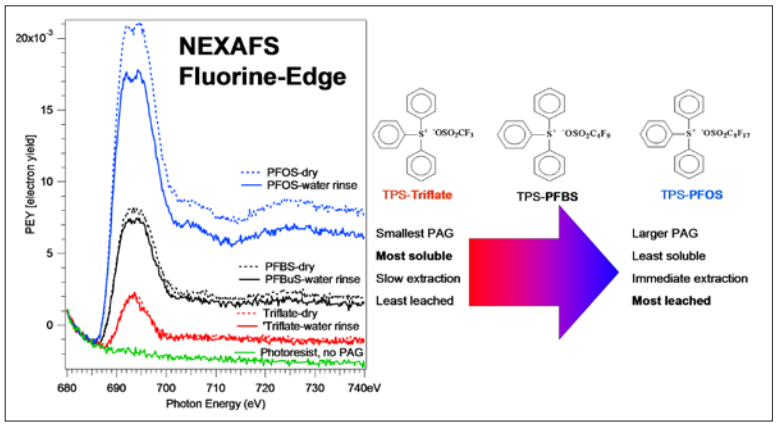

Figure 7. NEXAFS fluorine-edge results that quantify the PAG leaching from the surface due to water immersion. The series of PAGs tested for immersion lithography is shown as a function of equilibrium water solubility, extraction from thin films, and NEXAFS surface composition analysis.

■ Characterization of bulk scale mixing is necessary for understanding future photoresist materials as feature dimensions are reduced to sub-32 nm. The intimacy of mixing of PAG and model photoresist were probed by solid state proton NMR methods based on inversion-recovery, solid-echo -spin diffusion, and chemical-shift-based-spin-diffusion pulse sequences. The effect of resist architecture for EUV lithography was investigated as a function of molecular glass core structures (see Fig. 8). The PAG miscibility in several protected and deprotected versions was discovered in these new classes of resist materials. Phase separation of the PAG into enriched-domains was never seen; the PAG was always finely distributed. A maximum diameter for any PAG clustered into spherical domains was estimated to be 4 nm, far too small to reflect thermodynamic incompatibility. Hence, PAG blended samples are deduced to be thermodynamically compatible, with differential solubility in the preparation solvent the most likely candidate for producing the significant inhomogeneities in PAG concentration observed in a few samples.

■ Since EUV photoresists do not yet meet requirements on exposure-dose sensitivity, line-width roughness, and resolution, fundamental studies are required to quantify the trade-offs in materials properties and processing steps for problems such as high photoacid generator loadings and the use of very thin films. Furthermore, new processing strategies such as altering developer strength and composition may enable increased resolution. In this work, model photoresists are formulated without base quenchers to investigate the influence of PAG loading and developer strength on EUV lithographically printed images performed at the Advanced Light Source of Lawrence Berkeley National Laboratory. Measurements of line-width roughness and developed line-space patterns highlight a combined PAG loading and developer strength dependence that reduce LWR in a non-optimized photoresist.

■ Typically photoresist polymers have statistical molecular mass distribu-

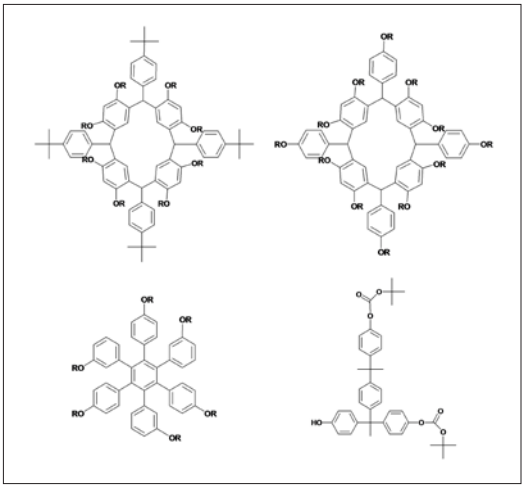

Figure 8. Model molecular glass with three different core architectures studied for intimacy of PAG mixing by NMR methods.

tions. Since novel calix[4]resorcinarenes have multiple sites for functionalization, a similar polydispersity in molecular mass may result. In this case the phenol groups are protected with acid sensitive tert butoxycarbonyl (R = tBOC) groups to less than completion in order to optimize spin coating, substrate adhesion, and exposure dose sensitivity. Therefore, rather than a distribution in chain length, the molecule will be characterized by a molecular mass distribution reflecting the degree of functionalization distribution. The MALDI-TOF mass spectrometry methods developed at NIST have characterized the polydispersity in the degree of functionalization for a series of calix[4]resorcinarene molecular glass resists. An example is shown in Fig. 9 for three different average protection levels of the resist shown in the inset. This enables quantitative comparison between formulations for polydispersity that impact resolution, line edge roughness, and defects.

■ Further, in collaboration with the Optical Technology Division, we have investigations of correlations between the latent image and developed image in EUV exposed line/space features. The latent images of isolated lines produced by EUV lithography are characterized by atomic force microscopy through the features in topology caused by change in film thickness that occurs upon deprotection. The resulting latent-image deprotection gradient, based on line cross-sections, and latent-image line-width roughness provide metrics and insight into ways to optimize the lithographic process. The results from a model poly(hydroxystyrene-co-tert-butylacrylate) resist and a model calix[4]resorcinarene molecular glass type resist show the general applicability of the metric before development as shown in Fig.10.

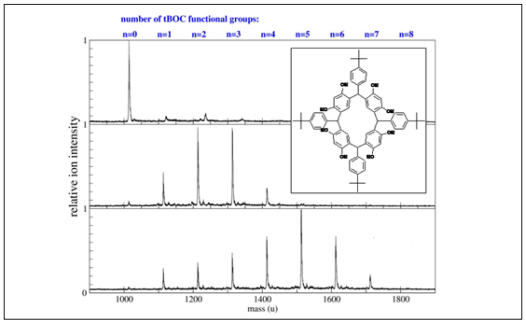

Figure 9. Mass spectrometry for three different average functionalization of the molecular glass resist shown. The well-defined mass spectra peaks differ by one protection group highlight the ability to measure the distribution between 0 and 8 tBOC functional group.

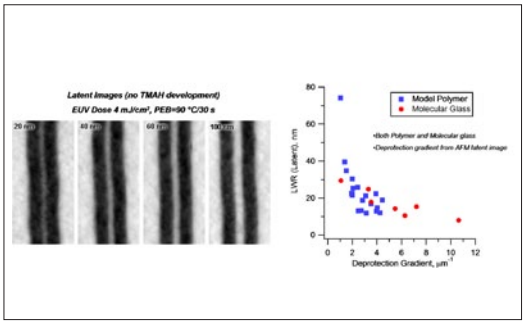

Figure 10. AFM latent images after tip deconvolution of dark field isolated lines in the model polymer resist. Nominal critical dimension appears in each image. While all lines are resolved in the latent image, only the 60 nm and wider lines remain after development at this dose: EUV exposure of 4 mJ/cm^2 and PEB was 90 °C for 30 s. Images are 1 micron by 2 microns with a 20 nm black to white z-scale. Analysis of the latent-image LWR versus deprotection gradient for contrasting resists.)

Collaborations

Polymers Division, NIST – Shuhui Kang, David VanderHart, Christopher Soles, William Wallace, Kathleen Flynn, Charles Guttman

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Center for Neutron Research, NIST – Sushil K. Satija

Optical Technology Division, NIST – John Woodward

Cornell University – Christopher Ober

Oak Ridge National Laboratory, Center for Nanoscale Materials Science – Peter Bonnesen

SEMATECH – Karen Turnquest

IBM Almaden Research Center – Hiroshi Ito, Robert D. Allen, William D. Hinsberg

AZ Electronics – Ralph Dammel, Frank Houlihan

DuPont Electronic Polymers L.P. – Jim Sounik, Michael T. Sheehan

Intel – CRADA 1893 (Polymers Division) and CRADA 1892 (Optical Technology Division)

SEMATECH – Agreement 309841 OF (completed 11/06)

Publications

S. Kang, V.M. Prabhu, W.-l. Wu, E.K. Lin, K.-W. Choi, M. Chandhok, T.R. Younkin, W. Yueh, *"Characterization of the photoacid diffusion length,"* Proc. of SPIE, 7273, 72733U (2009).

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Critical Dimension and Overlay Metrology Program

The principal productivity driver for the semiconductor manufacturing industry has been the ability to shrink linear dimensions. A key element of lithography is the ability to create reproducible undistorted images, both for masks and the images projected by these masks onto semiconductor structures. Lithography as a whole, fabricating the masks, printing and developing the images, and measuring the results, currently constitutes ≈35 % of wafer processing costs. The overall task of the Critical Dimension and Overlay Program is to assist the industry in providing the necessary metrology support for current and future generations of lithography technology. These goals include advances in modeling, the provision of next generation critical dimension and overlay artifacts, development of advanced critical dimension and overlay techniques, and comparisons of different critical dimension and overlay measurement techniques.

Currently, critical dimension and overlay measurement improvements have barely kept up with lithography capabilities. To maintain cost effectiveness, continued advances need to be made.

Wafer-level And Mask Critical Dimension Metrology

This project is the single largest project at NIST supporting the semiconductor industry. It involves metrology and artifact development across a broad range of techniques. For this reason, the project is presented in a number of sub-sections, each focusing on a single technology.

These are:

- Model-Based Linewidth Metrology
- Scanning Electron and Ion-Based Dimensional Metrology
- Scanning Probe Microscope-Based Dimensional Metrology
- Optical-Based Photomask Dimensional Metrology
- Scatterometry-Based Dimensional Metrology
- Small Angle X-Ray Scattering-Based Dimensional Metrology
- Grazing Incident X-Ray Scattering-Based Dimensional Metrology
- Atom-Based Dimensional Metrology
- Fabrication and Calibration Metrology for Single-Crystal CD Reference Materials

Model-Based Linewidth Metrology

Technical Contacts:
J. Villarrubia

Goals

The goal of this project is to address the metrology needs of industry, particularly the U.S. semiconductor industry, in those areas that are particularly model-intensive, such as linewidth and line edge roughness metrology with uncertainties on the order of 1 nm.

Customer Needs

A feature's width is one of its fundamental diA feature's width is one of its fundamental dimensional characteristics. Width measurement is important in a number of industries including the semiconductor electronics industry, with worldwide sales of $250 billion in 2008 [Semiconductor Industry Association]. As a measure of its importance in that industry, consider the term "critical dimension" or "CD" is used nearly interchangeably with linewidth or gate width.

To support present and future semiconductor technologies, industry needs to measure gate electrode widths with total uncertainties, as identified in the International Technology Roadmap for Semiconductors (ITRS, 2008 update), of approximately 0.42 nm. Neither NIST nor any other national laboratory presently offers a wafer linewidth measurement service or SRM with uncertainty at this level. In addition to measuring linewidths, the semiconductor industry has needs for measuring linewidth variation, that is, linewidth roughness (LWR). LWR in transistor gates has been linked to increased off-state leakage current and to threshold voltage variation. The 2008 ITRS update specifies that LWR, measured as three standard deviations of the CD, must be less than 2.12 nm in 2009 and be measured with no more than 0.42 nm uncertainty.

A line's width must generally be determined from its image. However, the image is not an exact replica of the line. The scanning electron microscope (SEM), scanning probe microscope (SPM), and optical microscope all have image artifacts that are important at the relevant size scales. Physical linewidth determination therefore requires modeling of the probe/sample interaction in order to correct image artifacts and identify edge locations. Barriers to accurate linewidth determination include inadequate confidence in existing models, the complexity and consequent expense of using some models, inadequately quantified methods divergence, and ignorance of best measurement practices. Barriers to accurate LWR measurement include random errors due to noise or sampling and poorly understood measurement artifacts such as measurement bias that comes from treating random edge assignment errors as a component of roughness (a false "noise roughness").

Technical Strategy

The most accurate metrology requires good instrumentation and measurement practices designed to minimize error. This is the experimental part, provided by other closely associated projects. It also requires a theoretical part which constitutes the scope of the model-based linewidth metrology project. Models of the measurement process provide an appropriate interpretation of the raw experimental results, an interpretation that includes (prior to the measurement) insight that leads to good measurement practices and (after the measurement) correction and/or quantification of remaining errors. The scope includes the development and improvement of computational models to simulate the artifacts introduced by measuring instruments, inversion of these models (to the extent possible) to deduce the sample geometry that produced a measured image, validation of models by appropriate experiments, development and testing of measurement processes that provide the necessary inputs for model-based deduction of sample width and shape, estimation of uncertainties for the measurement process, assistance to industry linewidth measurement by communication of best practices, and laying of the necessary research groundwork for a future linewidth and/or line shape Standard Reference Material.

We have developed a model-based library (MBL) method of determining linewidth and line shape from top-down SEM images. The top-down measurement configuration is the one employed by industry CD-SEMs. Edge locations tell us the line's width (the "CD" desired by industry). However, lines with different sidewall geometries appear to have different widths when measured using algorithms that are standard today on CD-SEMs. That is, sidewall variation masquerades as width variation. Accordingly, our method is a model-based

"Stack materials, surface condition, line shape, and even layout in the line vicinity may affect CD-SEM waveform and, therefore, extracted line CD. These effects, unless they are accurately modeled and corrected, increase measurement variation and total uncertainty of CD SEM measurements."

International Technology Roadmap for Semiconductors, Metrology Section, p. 10 (2007)

"A better understanding of the relationship between the physical object and the waveform analyzed by the instrument is expected to improve CD measurement."

International Technology Roadmap for Semiconductors, Metrology Section, p. 8 (2007)

algorithm that explicitly accounts for the physics of the interaction of the electron beam with the sample and the effect of sidewall geometry. MBL matches a measured image by interpolating a precomputed library of images. Because interpolation is fast, even computationally intensive models can benefit measurements. This method has yielded encouraging results. These results establish a direct link between the quality of SEM models and the accuracy of metrology that can be performed using them.

This has brought renewed focus on the quality of the models. Our original MONSEL model was restricted to samples that fell within well-defined and restricted classes, for example lines of uniform cross section on a layered substrate. Many samples of industrial interest did not meet these restrictions. In 2007, we translated MONSEL to Java (renaming it JMONSEL), and substantially revised the method of geometrical descriptions, thereby extending the capabilities to permit simulation of other industrially important sample shapes, such as rough-edged lines, contact holes, lines with a footing, and FinFETs (e.g., see Fig. 1).

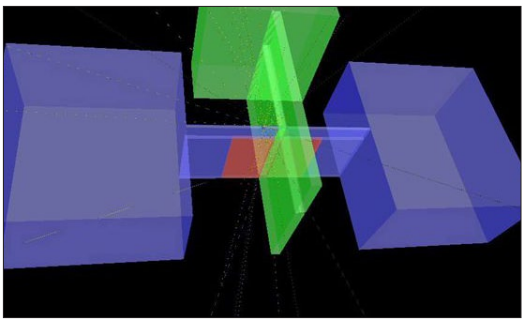

Figure. 1. An overview of a FinFET model showing Si source and drain (left and right boxes), a thin connecting Si fin with HfO^2 gate oxide, and a metal (TiN) gate electrode with a crossing fin-like contact. The substrate (not shown, but coincident with the bottom of the pictured structures) is Si.

Besides the sample geometry issue, it has become increasingly clear that the physics in existing SEM models was not accurate at energies below a few hundred electron volts. At these energies, electrons in the sample have time to adjust to the incoming electron, effectively screening the interaction and reducing the amount of scattering. Unfortunately, this low energy regime is precisely the one that is important for industrial SEMs, which (owing to the sensitivity of photoresist) employ electron landing energies less than about 1 keV, secondary electron (SE) imaging (which is by definition low energy, since SE are generated with average energies below 50 eV), and strong electric fields to extract SE that escape the sample. Moreover, these model inaccuracies are likely to affect dimensional measurements because they cause such dimensionally relevant parameters as electron escape depths to be greatly underestimated.

Implementing and evaluating a model to correct the aforementioned deficiencies was the work of the first part of 2008. Fortunately, the groundwork for an improved model had already been laid in the1960s and 1970s in the form of many-body dielectric function theory (DFT). Those developments were applicable only to a few metals with particularly simple band structure, but NIST's Cedric Powell proposed and David Penn later demonstrated a method for extending DFT to a vastly larger set of materials by using those materials' optically measured dielectric functions. Penn's method later became the basis for a NIST standard reference database (SRD71) of inelastic electron mean free paths. The same model has now been elaborated into JMONSEL's simulator for secondary electron generation and successfully tested for Cu and Si, as described below.

Use of the DFT model requires dielectric function data to be collected for materials of interest. The data are then input to a calculation that determines scattering tables for those materials. These tables are in turn used by JMONSEL for performing simulations. The bulk of the work planned for 2009 consists of extending our capability with the improved model to a much larger set of materials—a process that includes collecting dielectric function data and doing the calculations for as many industry-relevant materials as possible. Dimensional results using the new model are also being compared to the results using previous models in order to ascertain the extent of differences. We also plan to begin laying groundwork for a charge modeling capability.

DELIVERABLES:

- Develop a SEM detector model for SEMs that employ efficient extraction fields. 4Q 2008
- Develop model variants (plausible variations of our existing SEM models). 4Q 2008
- Simulate linescans using the model variants 4Q 2008

- Assess the sensitivity of model-based CD measurements to the choice of model variant. 1Q 2009
- Present a paper at SPIE Advanced Lithography on the sensitivity of measurements to choice of model. 1Q 2009
- Locate existing sources of optical data for materials of interest in semiconductor manufacturing. 2Q 2009
- Use Penn extension of dielectric function theory to compute electron scattering tables from data for materials of interest in semiconductor manufacturing 3Q 2009.
- Survey literature for physics models of charging in the SEM, determine which are a priori best, and make a plan to incorporate these into JMONSEL. 3Q 2009.

Accomplishments

In early 2008 we discovered inaccuracies in the existing binary scattering model used by our SEM simulator, particularly at low energies. We diagnosed the source of these inaccuracies were due to the absence of screening in the binary scattering model that we were using. We therefore implemented a dielectric function theory (DFT) module in the JMONSEL SEM simulator. This is a "many-body" theory. I.e., in contrast to binary scattering models, it incorporates the effect of interactions between the target electrons, including screening. We determined procedures to compute scattering tables using DFT and used these procedures

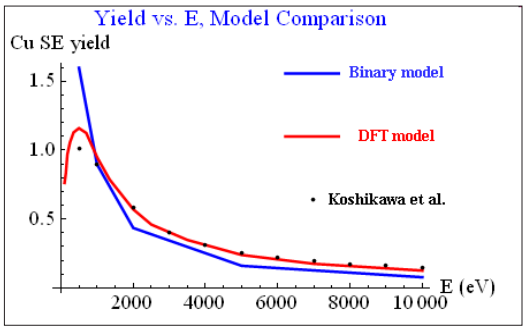

Figure. 2. Yield vs. energy as measured (points) and as calculated with a binary scattering model (blue) and the dielectric function theory using Penn's method (red)..

to determine tables for copper in the single-pole approximation. We obtained tables for silicon via collaboration. We performed simulations to compare the new model to previous ones. One such comparison, in Fig. 2, shows improved agreement with experiment in the calculated yield vs. incident energy on copper. The improvement is more significant because the binary model had one adjustable parameter, which was used to produce agreement with experiment at 1 keV, whereas the DFT model did not.

Figure 3 shows improved agreement in the calculated secondary electron emission spectrum from copper. The measured spectrum (Goto et al.) is the thin black curve. Two DFT models are shown, differing only in their treatment of the surface potential barrier (gradual vs. abrupt). Both of these agree better with the measurement than do the alternatives, one based upon a binary scattering model and the other based upon a phenomenological approach in which two adjustable parameters are chosen to give the best match to measured yield vs. energy (as in Fig. 2).

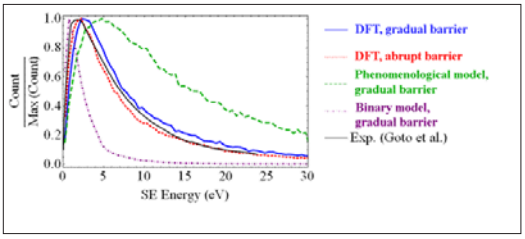

Figure. 3. Energy spectra of emitted secondary electrons on Cu with incident 1 keV electrons: comparison of several models to experiment.

Getting a model to simultaneously match yields at many energies, as in Fig. 2, and reproduce measured spectra, as in Fig. 3, has been difficult in the past, even when the models have included adjustable parameters. The DFT model's improved fit even without such parameters suggests the physics in the model is closer to nature. This in turn can be reasonably expected to lead to better dimensional metrology. The sensitivity of such metrology to the choice of model is the subject of current study.

Collaborations

International SEMATECH

Hitachi, Ltd., Maki Tanaka.

Illinois Institute of Technology, Prof. Xiaoping Qian

"Due to the changing aspect ratios of IC features, besides the traditional lateral feature size (for example, linewidth measurement) full three-dimensional shape measurements are gaining importance and should be available inline."

International Technology Roadmap for Semiconductors, Metrology Section, p. 8 (2007)

Recent Publications

F. Tian, X. Qian, and J. S. Villarru¬bia, "Blind estimation of general tip shape in AFM imaging," Ultramicroscopy **109**, 44-53 (2008).

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Scanning Electron and Ion-Based Dimensional Metrology

Technical Contacts:
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J. S. Villarrubia
M. T. Postek

Goals

Provide the microelectronics industry with highly accurate scanning electron microscope (SEM) measurement and modeling methods for shape-sensitive measurements and relevant calibration standards with nanometer-level resolution.

Carry out SEM metrology instrumentation development, including improvements in electron and ion optical system, detection, sample stage, and vacuum system.

Conduct research and development of new metrology techniques using digital imaging and networked measurement tools solutions to key metrology issues confronting the semiconductor lithography industry.

Customer Needs

The scanning electron microscope is used extensively in many types of industry, including the more than $200 billion semiconductor industry in the manufacture and quality control of semiconductor devices. The International Technology Roadmap for Semiconductors (2007) states that "Scanning Electron Microscopy continues to provide at-line and inline imaging for characterization of cross-sectional samples, particle and defect analysis, inline defect imaging (defect review), and critical dimension (CD) measurements. Improvements are needed for effective CD and defect review (and SEM detection in pilot lines) at or beyond the 45 nm generation." The semiconductor industry needs SEM standard artifacts, specifically those related to instrument magnification calibration, performance and the measurement of linewidth. This entails a multidimensional program including: detailed research of the signal generation in the SEM, electron beam-sample interaction modeling, developing NIST metrology instruments for the certification of standards, and developing the necessary artifacts and calibration procedures. The manufacturing of present-day integrated circuits requires that certain measurements be made of structures with dimensions of 45 nm or less with a very high degree of precision. The accuracy of these measurements is also important, but more so in the development and pilot lines. The measurements of the minimum feature size, known as CD, are made to ensure proper device operation. The U.S. industry needs high-precision, accurate, shape-sensitive dimension measurement methods and relevant calibration standards. The SEM Metrology Project supports all aspects of this need since scanning electron microscopy is key microscopic technique used for sub-100 nm metrology.

Technical Strategy

The Scanning Electron Microscope Metrology Project, a multidimensional project, is being executed through several thrusts fully supported by the semiconductor industry.

1. SEM Magnification Calibration Artifacts: Essential to SEM dimensional metrology is the calibration of the magnification of the instrument. Standard Reference Material (SRM) 2120 is an SEM magnification standard that will function at the low beam voltages used in the semiconductor industry and high beam voltages used in other forms of microscopy (Fig. 1). Conventional optical lithography provides a chance for large amount of good quality samples to be produced inexpensively. Because of the improvements of this technology, it is now possible to produce the finest lines with close to 100 nm width and with 200 nm pitch values. The largest pitch is 1500 µm. In order to make this artifact available (while the final certification details are being completed) the artifact is now released as Reference Material (RM) 8820.

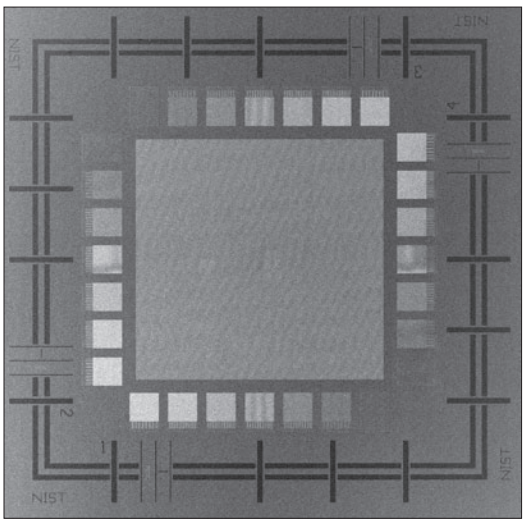

Figure 1. SEM image of the complete RM 8820 Magnification calibration standard reference material.

"Scanning Electron Microscopy (SEM) – continues to provide at-line and in-line imaging … and CD measurements. Improvements are needed … at or beyond the 45 nm generation … Determination of the real 3-D shape…will require continuing advances in existing microscopy …"

International Technology Roadmap for Semiconductors, 2007

DELIVERABLES:

- Upon availability of suitable quality samples, completion calibration and delivery of a batch of SRM 2120 samples. 4Q 2009

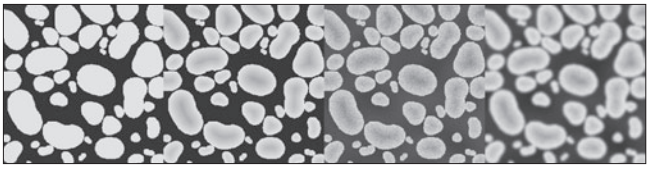

Figure 3. Images that illustrate the image simulation steps for the NIST SEM Resolution Measurement Reference Image Set.

2. SEM Performance Measurement Artifacts and Software Solutions: This effort included the development of the Reference Material 8091 (Fig. 2.) and associated evaluation procedures suitable for correctly measuring image sharpness of scanning electron microscopes, especially of those that are used in the semiconductor industry. Currently we are working with ISO to develop robust software solutions that will allow for resolution performance tracking of SEMs. The resolution performance characteristics of the SEM are particularly important to precise and accurate measurements needed for semiconductor processing. As a part of this effort the NIST SEM Resolution Measurement Reference Image Set was developed to test resolution measurement software. This Reference Image Set contains a large number of artificial images that were made by taking into account the amount and type of de-focusing, noise, vibration and drift and electron landing energies. Suitable samples are being sought to further improve this type of metrology (Fig. 3). Several samples have been purchased by leading semiconductor manufacturing companies and these measurement artifacts are used in the benchmarking efforts of International SEMATECH. The existence of these samples fosters better understanding, objective measurement and enforcement of SEM spatial resolution performance.

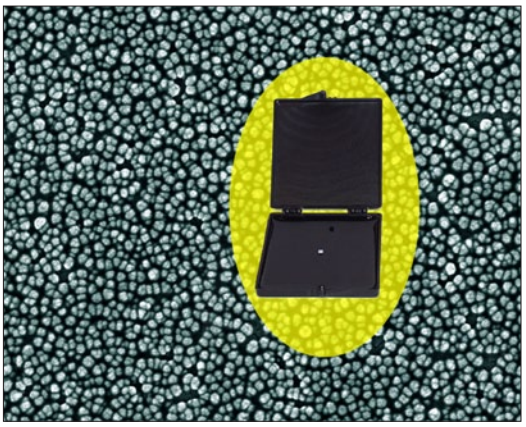

Figure 2. The RM 9081 Sharpness Reference Material.

3. SEM Linewidth Measurement Artifacts: Artifacts that are characterized and calibrated to the required small levels of uncertainty were and are in the focal point of the IC industry's dimensional metrology needs. Therefore, at NIST, it has been a longer-term goal to develop and deliver appropriate samples. For a long time, the possibilities were limited by the lack of various technologies available, especially the lack of accurate modeling methods. NIST, through several years of systematic efforts, developed Monte Carlo simulation-based modeling methods that can deliver excellent results. These new methods can deduce the shape of integrated circuit structures from top-down view images through modeling and library-based measurement techniques with a few nm of accuracy. In several publications, NIST demonstrated the possibilities and described the power of this approach. Based on the newest results, it is possible to start to develop the long-awaited relevant line width standard for the semiconductor industry. Reference Material 8120 line width samples will be a relevant sample on a 200 mm and 300 mm Si wafer with polySi features with sizes from 1 mm to down to 50 nm. Standard Reference Material 2120 is going to be the calibrated, traceable version for line width measurements. This work is being carried out in cooperation with SEMATECH.

A new effort is underway that is aimed at the development of two new Reference SEMs. One with full-size wafer and mask capability is based on an environmental SEM (ESEM), which is very advantageous with charging samples such as quartz masks. The other Reference instrument based on a dual-beam SEM, will be able to work with mask- and smaller size samples. Both microscopes will use the same type of 38 pm resolution laser interferometer, which provides traceability and allows for the compensation of stage drift and vibration at the nm level. These instruments are now operational, and work is underway to improve the measurement uncertainty.

DELIVERABLES:

- Fabrication of line width metrology litho artifact suitable for calibration on NIST and external measuring systems for certification of wafer and chip format line width samples. 3Q 2009
- Completion of preliminary measurements on litho samples made by SEMATECH with the new "NIST-MAG" metrology mask. 4Q 2009

4. **Helium Ion Microscopy - a Promising New Technique for Semiconductor Metrology and Lithography:** The Helium Ion Microscope (HIM) offers a new, potentially disruptive technique for nano-metrology. This methodology presents an approach to measurements for nanotechnology and nano-manufacturing which has several potential advantages over the traditional scanning electron microscope (SEM) currently in use in integrated circuit research and manufacturing facilities across the world. Due to the very small, essentially one atom size, very high brightness source, and the shorter wavelength of the helium ions, it is theoretically possible to focus the ion beam into a smaller probe size relative to that of an electron beam of current SEMs. Hence higher resolution is theoretically achievable. In contrast to the SEM, when the helium ion beam interacts with the sample, it generates significantly smaller excitation volume and thus the image collected is more surface sensitive. Similarly to the SEM, the HIM also produces topographic, material, crystallographic, and potential contrast, and offers ways for investigating previously inaccessible properties of the sample through the use of various detectors. Compared to an SEM, the secondary electron yield is quite high, allowing for imaging at very low beam currents, thus resulting in less sample damage. Additionally, due to the low mass of the helium ion, the He beam does not mill the sample at as high rate as gallium ions that are regularly used for ion milling, but with larger beam currents can be used for finer milling and cutting.

DELIVERABLES:

- Completion of detailed measurements and quality assessment of the imaging, lithography and nano-milling capability of the HIM using amorphous Si litho and other samples made by SEMATECH and phase shifting photomasks. 4Q 2009

Accomplishments

■ **SEM Magnification Calibration Artifacts** – Samples for Reference Material 8820 have been made in the once successfully, but later attempts with e-beam lithography yielded no further useful samples. We delivered to NIST Office of Reference Materials 100 pieces of RM 8820, which were fabricated at International SEMATECH using 193 nm UV light lithography. The finest features are 100 nm wide with a 200 nm pitch. The largest pitch is 1500 µm. There are a large number of 250 nm wide crosses and grids for distortion and other measurements. Scatterometry patterns with varying pitches will also be available. The features on the conductive Si wafer will be formed from amorphous Si material. These samples give suitable contrast in any SEM to allow the user to set the magnification of the instrument from the smallest to the highest magnifications. The first wafers containing the final design were fabricated by International SEMATECH and found to be useful. With the arrival of the new metrology SEM and its laser interferometer sample stage these will be calibrated.

■ **SEM Performance Measurements** – After comprehensive studies and experiments a plasma-etching Si called "grass" was chosen for Reference Material 8091 (Fig. 2). This sample has 5 nm to 25 nm size structures as is illustrated in the figure below. There have been 75 samples delivered to the Office of Standard Reference Materials, NIST. A sharpness standard and evaluation procedure have been developed to monitor (or compare) SEM image quality. A NIST kurtosis method, Spectel Company's user-friendly analysis system called SEM Monitor, and the University of Tennessee's SMART algorithm can be used with RM 8091. An effort is underway to produce more of these samples. These samples are now available to the public, and many of them are already in use. There is a new ISO standard under development that is introducing a method to reliably measure the resolution performance of SEMs; this method is also working well with RM 8091 samples.

■ **Contamination Specification for Dimensional Metrology SEMs** – Electron beam-induced contamination is one of the most bothersome problems encountered in the use of the scanning electron microscope (SEM). Even in "clean-vacuum" instruments it is possible that the image gradually darkens because a polymerized hydrocarbon layer with low secondary electron yield is deposited. This contamination layer can get so thick that it noticeably changes the size and shape of the small structures of current and future state-of-the art integrated circuits (ICs). Contamination greatly

disturbs or hinders the measurement process and the erroneous results can lead to wrong process control decisions. NIST has developed cleaning procedures and a contamination specification that offer an effective and viable solution for this problem. By the acceptance, implementation and regular use of these methods it is possible to get rid of electron beam induced contamination.

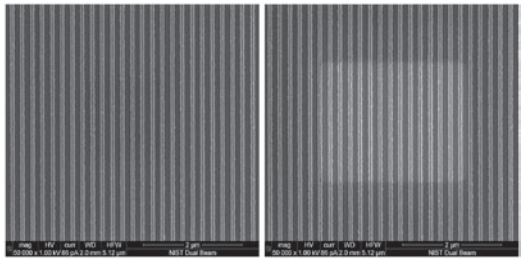

Figure 4. Contamination-free SEM operation. 1 kV, 86 pA SEM images of amorphous Si patterns at the beginning of the test (left) and after 10 minutes (left) of continuous electron beam bombardment. Actual cleaning and more signal are observable. 5 µm field-of-view images.

■ **SEM Linewidth Measurement Artifacts** – For correct linewidth measurements accurate modeling methods are indispensable. The existing NIST methods have shown excellent results on polySi samples and they are under further development for higher accuracy. From a top-down view and using our high-accuracy modeling and fitting methods, a cross section of the lines can be determined with few nm uncertainties and discrepancies. The match is so good that this method may be capable of eliminating the costly and destructive cross sectional SEM measurements. The candidate sample for linewidth artifact must be relevant to state-of-the-art IC technologies, should have chips on 200 mm and later 300 mm wafers with all process variation and include a meaningful focus-exposure matrix (FEM). The design and the fabrication of the SEMATECH/NIST mask have been successfully completed. After CD-SEM measurements at SEMATECH, cross sectional measurements will be made at NIST. All of these measurements will yield an excellent database for a decision on how to proceed with this wafer type linewidth reference sample. It is conceivable that by the end of the year 2009 the Reference Material 8120 line width samples will be available. This work is being carried out in close cooperation with SEMATECH.

■ **Development of High Accuracy Laser Interferometer Sample Stage for SEMs** – The development of a very fast, very accurate laser stage measurement system facilitates a new method to enhance the image and line scan resolution of SEMs. This method, allows for fast signal intensity and displacement measurements, and can report hundreds of thousands of measurement points in just a few seconds. It is possible then, to account for the stage position in almost real time with a resolution of 0.04 nm. The extent and direction of the stage motion reveal important characteristics of the stage vibration and drift, and helps minimize them. Figure 5 illustrates the short-term motion of the sample stage, the left side of the figure depicts the location of the stage and the right side is the density distribution of the location of the stage during 1 minute of dwell time. The field-of-views are 2 nm for all images. The high accuracy and speed also allow for a convenient and effective technique for diminishing these problems by correlating instantaneous position and imaging intensity. The new measurement technique developed recently gives a possibility for significantly improving SEM-based dimensional measurement quality. Important new discoveries made it possible to correctly understand the motion of the stage at the nm level, and the characterization of various settings and fine tuning of the sample stage, which is critical for high-resolution work.

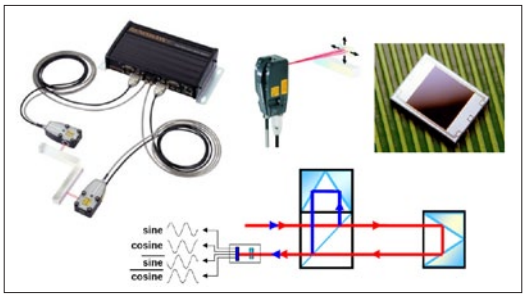

Figure 5. Laser interferometer system of the NIST Reference SEMs. Fiber-based beam delivery (upper left corner) Differential interferometer (upper center) Phase sensitive detector (upper right) and the detection scheme (lower center). (Courtesy of Renishaw Plc.)

■ **Development of New Imaging Method with Adaptive Averaging of Super-Fast SEM Images –** Modern SEMs acquire images by assigning signal intensity values to pixels that are arranged into a two-dimensional array - a digital image. If the image acquisition is done with

long pixel dwell times and/or long frame times, then the image may be blurred and/or distorted. Essentially, all SEM images are taken on moving targets; therefore, unless corrective methods are used, all pixels also contain information that belongs to other pixels. Unfortunately, in most high-magnification SEMs, both high and low frequency motions occur. The high frequency vibrations cause blurring while low frequency drifts lead to distortions. The new imaging method uses adaptive averaging of super-fast SEM images (taken at the highest sampling rates). It finds the shift vectors for all individual images and shifts them to their correct location. The shift vectors are calculated with sub-pixel resolution using cross-correlation of the images computed with the Fourier transform.

Figure 6 shows a single image collected in 11 μs, the results of traditional and adaptive image averaging. The image obtained with the new method is clearly sharper. Details that can hardly be seen with the traditional method stand out.

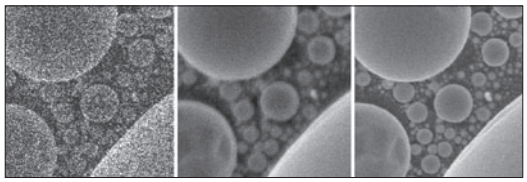

Figure 6. Single image acquired in 11 μs frame time (50 ns pixel dwell time) (left), traditionally averaged 70 images (middle), and the same 70 images averaged with the new, adaptive method (right). 4617 nm field-of-view images

■ **Development of Ultra-High Resolution He Ion Microscope** – HIM technology is not yet as optimized, developed or as mature as the SEM. As a new technique, HIM is just beginning to show promise and many potentially advantageous applications for integrated circuit and nanotechnology have yet to be exploited. Now that commercial instrumentation is available, further work is being done on the fundamental science of helium ion beam generation, helium ion beam-specimen interactions, and the signal generation and contrast mechanisms defining the image.

In addition to these areas of work, modeling needs to be developed to correctly interpret the signal generation mechanisms and to understand the imaging mechanisms. These are indispensable for accurate nanometer-level metrology. HIM and SEM have some overlapping territory, but they remain complementary techniques. Helium ion beam microscopy is opening new scientific and technology territories, and this new and innovative technology will develop new science and contribute to progress in integrated circuit and nanotechnology.

Beyond high-resolution imaging, He ion beam is also useful for exposing of resist materials. Figure 7 shows dense array of approximately 15 nm diameter hydrogen silsesquioxane (HSQ) resist posts generated by He ion lithography. Smaller structures are also feasible and the sensitivity of resists to ion irradiation can be significantly higher than to electrons. This is also being pursued to investigate how far ion-beam lithography can be pushed.

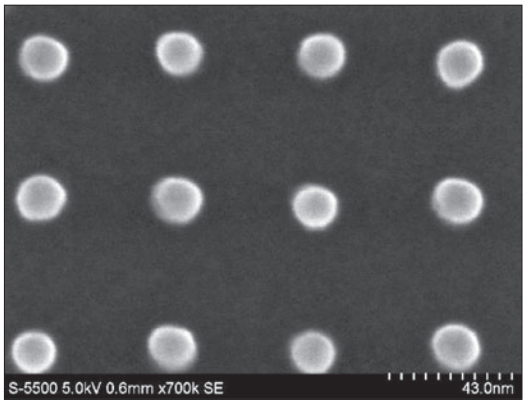

Figure 6. Single image acquired in 11 μs frame time (50 ns pixel dwell time) (left), traditionally averaged 70 images (middle), and the same 70 images averaged with the new, adaptive method (right). 4617 nm field-of-view images

Collaborations

International SEMATECH, Advanced Metrology Advisory Group.

International Technology Roadmap for Semiconductors; Microscopy and Metrology Sections.

Zeiss/ALIS Corp.

FEI Co.

ISO.

E. Fjeld Co.

Recent Publications

M. Oral and A. E. Vladár *"Optimization of SEM Imaging through 3D Modeling of Beam and Sample"* SCANNING Meeting Monterey May 2009.

P. Cizmar, A.E. Vladár and M. T. Postek *"Image Simulation for Testing of SEM Resolution Measurement"* Methods SCANNING Meeting Monterey May 2009.

A. E. Vladár and M. T. Postek *"Development of Reference Critical Dimension Metrology Scanning Electron Microscope"* SEMATECH Final Report 2008.

A. E. Vladár, K. P. Purushotham and M. T. Postek *"Contamination Specification for Dimensional Metrology SEMs"* SPIE Microlithography 2008.

M. T. Postek, A. E. Vladár *"The Potentials of Helium Ion Microscopy for Semiconductor Process Metrology"* SPIE Microlithography 2008.

A. E. Vladár, J. S. Villarrubia, P. Cizmar, M. Oral and M. T. Postek *"Accurate and Traceable Dimensional Metrology with a Reference CD-SEM"* SPIE Microlithography 2008.

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Scanning Probe Microscope-Based Dimensional Metrology

Technical Contacts:
R. Dixson
G. Orji
J. Fu

Goals

Improve the measurement uncertainty of critical-dimension measurements in the semiconductor industry through improvements in scanning probe microscope-based measurements. *The International Technology Roadmap for Semiconductors* (ITRS) identifies dimensional metrology as a key enabling technology for the development of next-generation integrated circuits. For example, according to the 2007 update, the goal in 2009 for critical dimension (CD) measurement uncertainty for isolated lines was ± 0.42 nm; this demand tightens to ± 0.29 nm by 2012.

Although most in-line metrology is performed using scanning electron microscopes (SEM) and scatterometry, these instruments are not presently capable of first-principles accuracy. That is, they must be calibrated using reference measurements from a tool or combination of tools which is capable of intrinsic accuracy. Such a tool is now referred to as a reference measurement system (RMS), and the 2007 update of the *ITRS* highlights the growing importance of an RMS. The use of atomic force microscope (AFM) and transmission electron microscope (TEM) cross measurements section for this purpose – often in combination – is now a fairly common practice in the industry.

The technical focus of this project, development and implementation of scanning probe microscope instrumentation for traceable dimensional metrology, is thus driven by the anticipated industry needs for reduced measurement uncertainty for in-line metrology tools such as the SEM and scatterometer – since these in turn rely on reduced measurement uncertainty for techniques such as AFM that are often implemented as an RMS.

Customer Needs

SEM is still the current tool of choice for inspection and metrology of sub-micrometer features in the semiconductor industry. Scatterometry or optical critical dimension (OCD) metrology is also rapidly gaining acceptance as an in-line process metrology tool. Scanning probe microscopes (SPMs) possess unique capabilities, which may significantly enhance the performance of SEMs for in-line CD measurements, and are also emerging as CD measurement tools in their own right. A creative strategy, which successfully harnesses the strong points of both techniques in order to reduce the measurement uncertainty of sub-micrometer features, will help NIST meet the expectations of the semiconductor industry expressed in the current *ITRS*. As is the case with SEMs, the magnification or scale of an SPM must be calibrated in order to perform accurate measurements. Although many SPMs are commercially available, appropriate calibration standards have lagged. In particular, the availability of traceable pitch, height, and width standards in this regime is limited.

Technical Strategy

The SPM dimensional metrology program consists of three inter-related thrusts: The first two thrusts address SPM dimensional metrology with two in-house research instruments at NIST, and the third thrust involves a partnership with SEMATECH to maintain traceability on a commercially available in-line SPM housed in the manufacturing facility at SEMATECH. The two instruments housed at NIST are a calibrated atomic force microscope (C-AFM) for measurement of pitch and step height and a critical dimension atomic force microscope (CD-AFM) for measurement of linewidth.

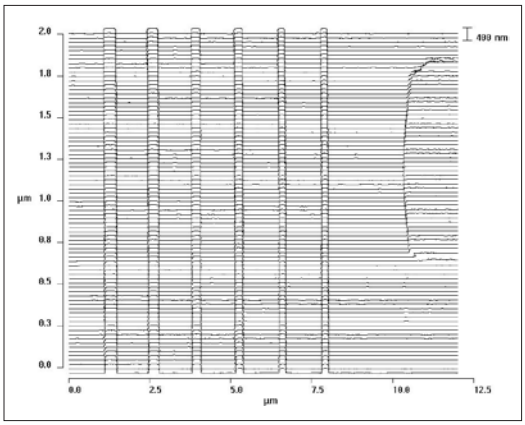

Figure 1. CD-AFM image of a NIST45 SCCDRM specimen which can be used for tip width calibration.

The C-AFM is a custom built instrument that has metrology traceable to the wavelength of light for all three axes of motion, and it has provided

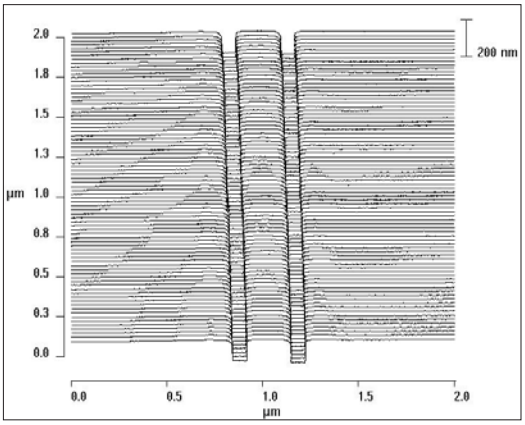

Figure 2. CD-AFM image of a commercial linewidth standard that we measured at NIST to compare the reference calibrations.

calibrated pitch and height measurements for a variety of nano-scale applications. Pitch measurements in the micrometer regime and below can currently be performed with relative standard uncertainties as low as 5×10^{-4}, and step height measurements up to several hundred nanometers can be performed with a relative standard uncertainty approaching 1×10^{-3}. The C-AFM has participated in two international comparisons of sub-micrometer pitch measurements and one comparison of step height measurements.

DELIVERABLES:

- Performed initial re-measurement of SRM 2059 photomask master standard (control mask) using traceable CD-AFM at NIST. 3Q2008
- Presented paper on results of AFM re-calibration of SRM 2059 control mask at SPIE/BACUS Photomask Technology conference. 4Q2008
- Organized, hosted, and ran an evening panel discussion at SPIE Advanced Lithography Meeting on challenges in contour metrology. 1Q2009
- Performed initial measurements on secondary SRM 2059 photomask – which will be used in a bilateral comparison between NIST and the National Metrology Institute of Germany, Physikalisch-Technische Bundesanstalt (PTB) – using traceable CD-AFM metrology. 1Q2009
- Collaborate with ISMI/SEMATECH personnel to perform source evaluation of new Insight3D CD-AFM that will be installed in ISMI facilities in Albany. 2Q2009
- Perform CD-AFM measurements on AMTC masks to support the Nano1 international comparison of linewidth measurements. 3Q2009
- Participate in comparison of traceable 70 nm pitch standard with A-Star (the NMI in Singapore) and Advanced Surface Microscopy (ASM) – a commercial standards vendor. 4Q2009

The second and third thrusts involve the most commonly used AFM-based method of linewidth metrology in industry: CD-AFM. This type of instrument is more sophisticated than conventional AFM and used a flared shape probe and two-dimensional feedback to image the sidewalls of near-vertical structures. The SXM320 is a prior generation commercially available CD-AFM. Initially, this instrument was used to implement the CD-AFM/RMS at SEMATECH during the tenure of Ronald Dixson as the first NIST Guest Scientist there. Now that the instrument is housed at NIST, the uncertainties have been further refined. Currently, pitch measurements can be performed with a relative standard uncertainty of approximately 2×10^{-3}. Step height measurements have a relative standard uncertainty 4×10^{-3}, and linewidth measurements can have standard uncertainties as low as 1 nm. This is a result of the most current release of NIST single crystal critical dimension reference materials (SCCDRM) that was completed in 2005.

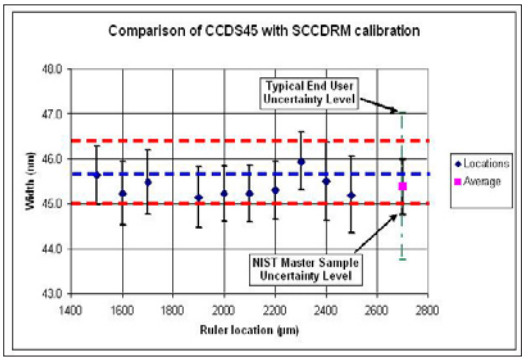

Figure 3. Comparison of SCCDRM master calibration with a commercial CD standard of nominal 45 nm width. The blue line shows the nominal CCDS45 calibration as determined by the vendor and the red dashed lines the expanded uncertainties. The NIST CD-AFM measurements of the CCDS45 used the SCCDRM master calibration. The calibrations are in excellent agreement and within the uncertainties.

The third thrust involves collaboration with ISMI/SEMATECH to establish a traceable CD-AFM (RMS) in their new facilities in Albany. This thrust involves migration of the RMS methodology from the prior Dimension X3D platform to the new Insight3D platform. George Orji, who was the second NIST Guest Scientist at SEMATECH, is continuing to oversee this thrust following his return to NIST.

As is true for the SXM at NIST, the SCCDRM project has resulted in the ability to perform linewidth measurements with a standard uncertainty of 1 nm. The relative uncertainties in pitch and height measurements using the X3D were reduced to 1×10^{-3} and 2×10^{-3}, respectively. Further reductions are anticipated when the RMS methodology is fully implemented on the Insight3D.

DELIVERABLES:

- Presented a paper at SPIE Advanced Lithography Conference on the possible migration of NIST dimensional calibrations to instruments available in the NanoFab to better serve customers in the semiconductor industry. 2Q2009
- Present paper at the SPIE Instrumentation, Metrology, and Standards for Nanomanufacturing Conference on strategies for traceability implementation and quality assurance in the manufacturing environment. 3Q2009

Accomplishments

■ The NIST/SEMATECH partnership in advancing AFM metrology in semiconductor manufacturing continues. After a tenure of more than three years as the second NIST Guest Scientist at SEMATECH, George Orji returned to NIST in mid 2008. However, he will continue to support the RMS implementation on the new CD-AFM in the ISMI/SEMATECH facilities in Albany.

■ As a result of the NIST SCCDRM effort, in which the AFM dimensional metrology project played a central role, CD-AFM linewidth measurements can now be performed with a 1 nm (k = 1) standard uncertainty. This standard for width calibration is now being used on both the X3D and the SXM at NIST. An image of an SCCDRM taken on the SXM320 is shown in Fig. 1. In 2007, we performed a comparison of the SCCDRM master calibration with a commercially available linewidth standard, an image of which is shown in Fig. 2. There was agreement between these two independent calibrations, as shown in Fig. 3.

■ We have used the C-AFM to perform a NIST-internal calibration on a 100 nm pitch grating specimen. This sample was then used to support SEM magnification calibration during the NIST-wide project to develop Reference Materials (RM) of gold nanoparticles. The C-AFM value had an expanded uncertainty (k = 2) of approximately 6×10^{-4}, and this result is currently being used to refine the analysis of the SEM measurements for the official report.

■ Another area of activity involves the study of single atomic Si steps as fundamental height standards in the sub-nanometer regime. In 2006 we published a documentary standard for AFM z-calibration using the single atom steps through the ASTM Subcommittee E42.14 on STM/AFM. This was published by ASTM as E2530-06. Recently, we have expanded this effort to include other materials and we have performed some preliminary measurements on a SiC sample with nominal 1 nm steps. This activity is ongoing.

■ We continue to provide reference AFM metrology for the SRM 2059 photomask standard. During the tenure of Ronald Dixson as the first NIST Guest Scientist at SEMATECH, we performed traceable CD-AFM measurements on the control mask for the SRM calibration. Subsequently, and following the completion of the SCCDRM project, we have performed new measurements using the CD-AFM at NIST, and we have been able to reduce the AFM uncertainties by almost a factor of five for the smallest features. .This is illustrated in figures 4 and 5.

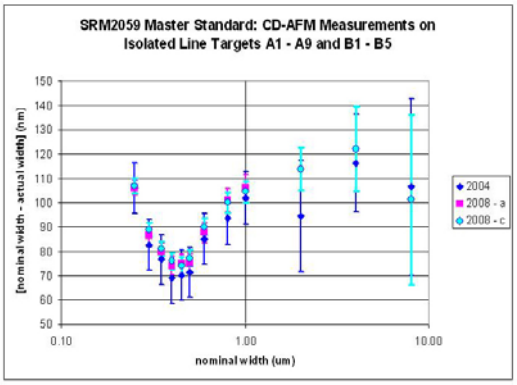

Figure 4. Stitched composite slope image from two images of a linewidth sample taken with a carbon nanotube tip. Measurements performed by J. Fu; sample developed by M. Cresswell and R. Allen; probe developed by C. Nguyen of ELORET/NASA Ames.

A paper on the status of the SRM 2059 recalibration effort and our plans for a bilateral comparison of photomask linewidth measurements between NIST and PTB was presented at the Frontiers in Characterization and Metrology for Nanoelectronics Conference in May of 2009

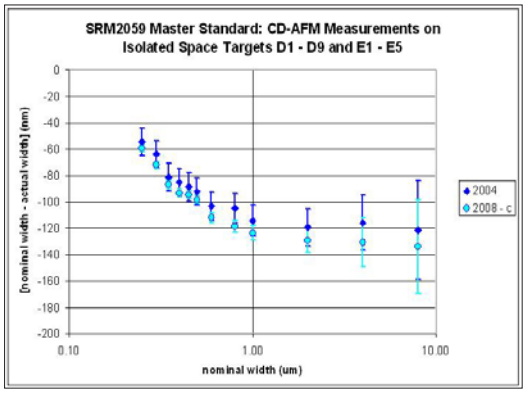

Figure 5. New and original CD-AFM reference measurement on the isolated space targets of SRM 2059 – ranging from 0.25 µm width (D1 feature) up to 8 µm (E5 feature). The error bars represent expanded (k = 2) uncertainties, which have been reduced by approximately ×4 for the smallest features.

Collaborations

Intel Mask Operations, Santa Clara, CA.

Intel, Hilllsboro, OR.

Intel, Santa Clara, CA.

SEMATECH, Austin, TX.

Veeco Metrology, Santa Barbara, CA.

IBM Burlington, VT.

IBM Almaden Research Center, San Jose, CA.

ELORET Corp./NASA Ames Research Center, Moffett Field, CA.

Departments of Mechanical Engineering and Chemistry, University of North Carolina, Charlotte, NC.

School of Mechatronic Engineering, Harbin Institute of Technology, Harbin, China.

Recent Publications

R. Dixson, J. Fu, N. Orji, T. Renegar, A. Zheng, T. Vorburger, A. Hilton, M. Cangemi, L. Chen, M. Hernandez, R. Hajdaj, M. Bishop, A. Cordes, *"Reference Metrology in a Research Fab: The NIST Clean Calibrations Thrust,"* SPIE Proceedings Vol. 7272, 727209-1-12 (2009).

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N. G. Orji, R. G. Dixson, *"Higher Order Tip Effects in Traceable CD-AFM Based Linewidth Measurements,"* Meas. Sci. and Technol. Vol. 18, 448-455 (2007).

N. G. Orji, R. Dixson, B. D. Bunday, J. A. Allgair, *"TEM Calibration Methods for Critical Dimension Standards,"* SPIE Proceedings Vol. 6518, 651810 (2007).

B. Bunday, J. Allgair, E. Soleck, C. Archie, N. G. Orji, J. Beach, O. Adan, R. Peltinov, M. Bar-zvi, J. Swyers, *"The coming of age of tilt CD-SEM,"* SPIE Proceedings Vol. 6518, 65181S (2007).

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Optical-Based Photomask Dimensional Metrology

Technical Contacts:
J. Potzick
R. Silver

Goals

Provide technological leadership to semiconductor and equipment manufacturers and other government agencies by developing and evaluating the methods, tools, and artifacts needed to apply optical techniques to the metrology needs of semiconductor microlithography. One specific goal is to provide the customer with the techniques and standards needed to make traceable dimensional measurements on photomasks and wafers, where appropriate, at the customer's facility. The industry focus areas of this project are primarily the optical based methods used in overlay metrology, photomask critical dimension metrology, and high-accuracy two-dimensional placement metrology.

Customer Needs

Tighter tolerances on CD measurements in photomask and wafer production place increasing demands on photomask linewidth accuracy. NIST has a comprehensive program to both support and advance the optical techniques needed to make these photomask critical dimension measurements. Accurate feature size metrology on binary photomasks (constituting 85 % of current mask production) becomes increasingly difficult as critical features shrink and their optical proximity correction cousins proliferate. Phase shift and EUV masks present additional challenges.

Improved photomask CD metrology and two-dimensional overlay measurement techniques and standards are needed for measuring and controlling feature size and placement on the wafer and on photomasks. Overlay control is listed in multiple sections of Tables Met 3a and b of the 2007 SIA ITRS as a difficult challenge for <45 nm node processes. In fact, the table shows that there are no known measurement solutions with acceptable uncertainty for image placement and overlay control beyond the 65 nm node. As shown in Tables MET4a and b, the problems are more acute for long term photomask CD metrology where the industry will soon be encountering metrology problems without known manufacturing solutions.

Technical Strategy

There are three main strategic technical components of this project.

1. Photomask linewidth measurements using the ultraviolet transmission microscope, calibration of NIST Photomask Linewidth Standard SRM 2059, and the development of calibration methods to provide photomask linewidth measurement uncertainties adequate to meet industry needs.

The technical strategy for photomask linewidth standards is divided into two segments: *(a)* instrumentation and image model development and *(b)* design and calibration of standard artifacts.

An ultraviolet transmission microscope (Fig. 1) has been constructed which uses a unique geometry (a Stewart platform) as the main rigid structure. This microscope platform has good vibration characteristics and presents an open mechanical architecture. Higher image resolution, reduced transmission of UV light through the chrome, and reduced instrument vibration offer improved linewidth measurement uncertainties over reflection-mode microscopes.

NIST has supplied a substantial number of photomask linewidth standards worldwide over the past decade. NIST's current chrome-on-quartz photomask linewidth standard, SRM 2059, (Fig. 2, next page) contains isolated linewidth and spacewidth features in the range of 0.25 µm to

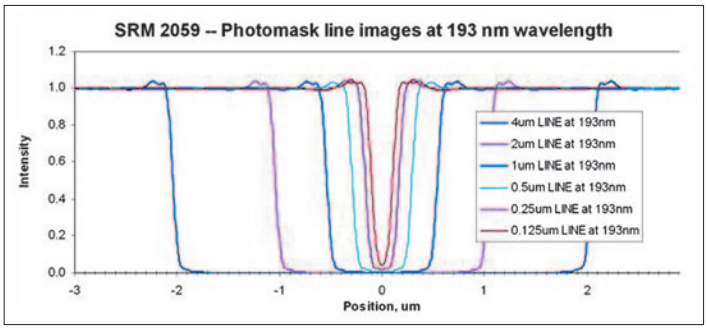

Figure 1. Modeling results for isolated binary photomask lines from 4µm to 0.125µm.

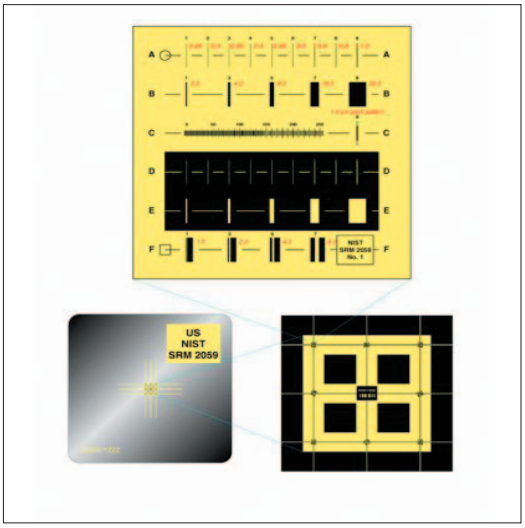

Figure 2. NIST SRM 2059 Photomask Linewidth Standard. Isolated linewidths and spacewidths range from 0.250 um to 312 um.

32 µm, whose widths have been measured and certified to an uncertainty of <20 nm at the 95 % confidence level.

In response to customers' needs for more accurate photomask feature size measurements, NIST has worked extensively to improve mask metrology through optical image modeling and improved optical microscope characterization methods. The features on even the highest quality masks exhibit roughness and runout at the chrome edges, compromising the definition of edge and linewidth. In response to these problems, NIST introduced the Neolithography concept 1997: Modeling or emulating the effects of all of the relevant feature properties in both the mask metrology process and the wafer exposure and development processes, using existing and new software tools, can improve feature-size accuracy by establishing accurate simulation results and improving the relationship between mask-feature metrology and the corresponding wafer-feature sizes. This concept (at least in part) can be seen today in the design for manufacturing (DFM) sector of the industry.

DELIVERABLES:

- Compare and improve the accuracy of the NIST optical scattering code (developed by Egon Marx) with new scattering models developed by Spectel, Thom Germer (NIST), and others for use in transmission. Ongoing, through 4Q 2009
- Re-evaulate the parametric uncertainty in optical linewidth measurements, using new techniques to remove the small-linewidth overemphasis in the previously described metric. Present results at Microscopy and Microanalysis, 4Q 2008; ongoing through 4Q 2009.

2.The second major component is the development of two-dimensional grid calibration standards and associated measurement techniques, including statistical analysis and charge-coupled device (CCD) characterization as used by industry. These individual technical strategies for these components are described next.

We are addressing the challenges of two-dimensional measurements from a couple of directions. The first is the calibration of an artifact standard which is being used to bring two-dimensional based inspection instruments to the same metric. This effort has developed a standard grid which is now available as a NIST Standard Reference Material, #5001. The artifact can be used by the semiconductor industry to standardize 2-D feature placement measurements. The SRM 5001 was developed as an industry consensus standard grid and calibrated with measurements on a state-of-the-art industry machine followed by verification of the measurements using NIST Linescale Interferometer capabilities which resulted in traceable two-dimensional measurements.

A new generation of grids for the SRMs have been fabricated and measurements have been completed. Each measurement of the grid has data in each of at least two orientations. Rotating the grid 90° between measurements samples a number of the geometric errors of the machine. The remaining geometric sources of uncertainty are the scale and some components of the linearity of each machine axis travel.

Verification of the industry-based grid measurements is done at NIST. The overall scale of the grid is checked with the NIST linescale interferometer, an instrument that is known to provide the most accurate 1-D measurements available in the world. Two sources of uncertainty not captured by these measurements include components of the straightness and effects of the plate bending when fixtured.

We have delivered all of the SRM 5001 grid plates, to the Standard Reference Material program. We are now planning the next generation. From the detailed uncertainty budget for SRM 5001 the scale measurements are the largest component and the largest component of the Lines-

cale Interferometer uncertainty budget is the wavelength correction for the index of refraction of the air.

The refractive index depends on the air pressure, temperature, relative humidity, CO_2 concentration, and the presence of small polarizable molecules like hydrocarbons (ethanol, methanol, and other cleaning agents). The correction for air pressure, temperature and relative humidity are made routinely, but the uncertainty from these three is currently at the state of the art and a significant reduction in the uncertainty is unlikely. CO_2 and other molecules are difficult to quantify and are generally ignored.

NIST is currently developing a method to lower the uncertainty substantially in an absolute refractometer from the wavelength correction. The method is based on variable-length Fabry-Perot (FP) refractometers. The variable-length differential FP (VLDFP) can be used to calibrate a simple fixed-length cavity near atmospheric pressure. The fixed-length cavity will then provide substantially improved pressure measurements relative to current state-of-art down to about 1 Pa. The VLDFP-- or a simple fixed-length cavity calibrated with the VLDFP-- will also be the most accurate device in the world for measuring refractive index of air, which is a limiting step in practical realization of the meter. The capability of the device can be convincingly verified at an uncertainty that is orders of magnitude better than current state-of-art for refractive index measurement.

DELIVERABLES:

- The old cavities were made with fused silica mirror substrates optically contacted to zerodur spacers. The choice of materials gave rise to several problems, including poor temporal stability. We have purchased ULE rods to replace the zerodur in our new system and will use ULE for the mirror substrates to avoid thermally induced stress. 4Q 2008
- We are upgrading to Pound-Drever Hall (PDH) locking so as to alleviate a number of servolocking problems. This work is underway: we have the optical components in place and are currently building electronics for detecting the PDH signal and adjusting the laser frequency with a double-pass AOM (acousto-optic modulator). The new system will be completed and tested against previous performance. 2Q 2009

3. To strengthen the foundation of NIST's linewidth measurement traceability and to support the *Bureau International des Poids et Mesures* (BIPM) Mutual Recognition Arrangement, NIST has become the pilot laboratory for an international intercomparison of submicrometer linewidth measurements, Nano1. National metrology institutes in nine countries around the world are participating. PTB (*Physikalisch Technische Bundesanstalt,* Germany) has offered to supply two masks manufactured at the Advanced Mask Technology Center GmbH Co. KG (AMTC, Dresden) for the multilateral comparison *Nano1* and a separate bilateral comparison between NIST and PTB. Since *Nano1* will take several years (allowing 2-3 months for each laboratory, plus overhead), the bilateral comparison is designed to provide more timely data to the AMTC. This bilateral comparison and *Nano1* are to be kept as separate and independent as possible. A publication describing this bilateral comparison was given at BACUS 2008.

DELIVERABLES:

- Upon delivery of the masks from PTB, they will be measured by AFM (Ron Dixson) and optically in the UV microscope. The Nano1 protocol will be revised to incorporate the AMTC mask. Upon acceptance of the protocol by participating laboratories, Nano1 will commence. 3Q 2009

Accomplishments

■ SRM 2800 Microscope Magnification Standard is a standard-size microscope slide with calibrated pitch features ranging from 1 μm to 1 cm (see Fig. 3). It contains a lithographically produced chrome pitch pattern consisting of a single array of parallel lines with calibrated center-to-center spacings. It contains no linewidth structures. This SRM is intended to be used for the calibration of reticles and scales for optical or other microscopes at the user's desired magnification. The SRM may be used in either transmission or reflection mode optical microscopes, SEMs, or SPMs. Calibration is traceable to the meter through NIST Line Scale Interferometer. Fifty-six units have been calibrated and delivered to the NIST Office of Standard Reference Materials and nearly half of current stock have been sold.

■ The 193 nm reflection mode scatterfield optical microscope is now operational. Preliminary scanning and modeling is now underway as a basis for photomask measurements on the 193 nm tool. A paper will be presented at Bacus 2009 showing a comparison of 193 nm reflection mode measurements and UV transmission mode measurements.

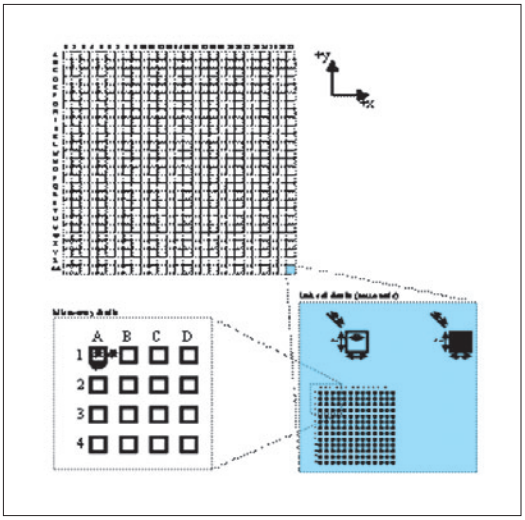

Figure 3. The two dimensional grid photomask standard, now available through the SRM office.

■ The UV transmission microscope has been substantially updated with new interferometers including new synchronization hardware. The optics has been updated with a flexible conjugate back focal plane to allow for illumination engineering and improved alignment. The instrument has undergone extensive alignment and calibration using new methods for background normalization developed at NIST. The entire computer control system is being updated with a new high speed controller and CCD acquisition capability.

■ The complete set of two-dimensional grid artifacts, known as SRM 5001, has been delivered to the SRM office and are selling well. These 152.4 mm (6 inch) photomasks have been measured on a state-of-the-art I-pro metrology system by the photomask manufacturer. The second set of re-designed 152.4 mm (6 inch) feature placement standards has also been measured and calibrated in close collaboration between NIST and Photronics. The collaboration employs the industry tool and the traceability of the NIST line scale interferometer with appropriate statistical analysis (see Fig. 4).

■ In close collaboration with SEMATECH, we have completed a comprehensive report using optical methods for the calibration of phase shifting photomasks. This includes modeling and measurements in transmission and reflection. This document is available through SEMATECH as a tech transfer document.

■ A comprehensive suite of two-dimensional calibration methods for the calibration of optical systems and illumination systems was published based on the SRM 5001 grid calibration methodology. These results and the methodology was published at *SPIE Microlithography*. These methods are enabling a substantially improved optical calibration and alignment sequence as well as improved modeling inputs for more accurate linewidth measurements.

■ A new set of comparator algorithms was completed that enabled the SRM 5001 calibrations to be finished with the Nikon 5i tool in collaboration with the industry Ipro system. The comprehensive analysis capabilities for centerline and edge detection methods with a complete uncertainty statement and remaining reticles was delivered to the SRM office. The standard scale correction and new mapping software was implemented for the Nikon 5i system. The set of two-dimensional calibration grids was measured with a complete uncertainty analysis.

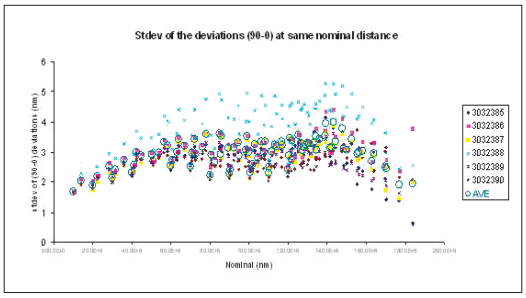

Figure 4. Tool repeatability and mapping data for the two-dimensional mask calibration procedure.

Collaborations

ISMT, IBM, IVS Schlumberger, KLA-Tencor, Intel, Motorola, AMD and several other leading manufacturers or tool vendors.

Dr. Mark Davidson, Spectel Research Corp.

PTB *(Physikalisch Technische Bundesanstalt, Germany)*.

AMTC, Dresden, Germany.

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Scatterometry-Based Dimensional Metrology

Goals

Our goals are to: (1) increase the effectiveness of scatterometry and other optical critical dimension (OCD) methods by providing industry with new measurement techniques, improved modeling, and standards; (2) provide assessments of accuracy and sensitivity of various OCD methods; and (3) develop facilities to accurately assess OCD targets.

Customer Needs

Scatterometry is increasingly becoming a preferred method for online critical dimension (CD) metrology. The method relies upon measurements of the reflectance or diffraction of small test grating structures as functions of angle, wavelengths, and/or polarization. By comparing measurement results with an extensive library of theoretical simulations or by performing a real-time regression analysis, tools can extract such line profile parameters as critical dimension, sidewall angle, and height, as well as more detailed descriptions of the sidewall shape.

While scatterometry has gained significant acceptance, it is continuing to grow in utility. However, there are many issues that remain that prevent it from having fundamental traceability. For example, the effects of finite illumination, finite target array size, line-edge and line-width roughness, uncertainties in the optical properties of the materials in the structure, neglect of surface oxides or other layers, radiometric accuracy, and the integrity of the theoretical model all contribute to the final measurement uncertainty in ways that are at this time poorly understood.

Ultimately, the industry needs reference artifacts that can test the validity of the results obtained by scatterometry tools. Such an artifact might consist of a set of gratings that have been characterized by a variety of techniques, including scatterometry, scanning electron microscopy (CD-SEM), atomic force microscopy (CD-AFM), and transmission electron microscopy (TEM). Scatterometry provides a method independent of the others, and if a comprehensive uncertainty budget were developed for the method, it would substantially improve the overall state of dimensional metrology.

Technical Strategy

There are three major strategies for improving the effectiveness of scatterometry. One strategy is to develop efficient models for the diffraction of light by structures on surfaces, so that NIST has state-of-the-art capabilities to perform scatterometry measurements and analysis as well as to provide standard data for a variety of model structures. The second strategy is to assess the sensitivity and accuracy of scatterometry methods to different structures, to provide industry with an understanding of what determines the ultimate sensitivity and accuracy of the methods. Finally, the third strategy is to develop in-house measurement capabilities with the long-term goal to perform scatterometry measurements on reference materials, to perform inter-laboratory comparisons, and to develop the scatterometry technique for other applications.

Specific project elements are defined below:

1. **Theoretical Scatterometry Modeling** – Rigorous coupled wave (RCW) based theories are the most common methods used to analyze scatterometry data. We have developed in-house capability to perform RCW calculations for arbitrary one-dimensionally and two-dimensionally periodic structures. These codes are being used to generate libraries for profile extraction as well as for test calculations that assess the sensitivity of scatterometry to changes in model parameters or to non-ideal target profiles. We are using these codes to assess the effects of line-edge and line-width roughness, material anisotropy, as well as to perform RCW calculations on three-dimensional structures, such as contact holes. Building upon the SCATMECH library of codes that have been made available on the web for diffuse scattering calculations, we have published the RCW code for one-dimensionally periodic structures and will publish the code for two-dimensionally period structures in the future.

DELIVERABLES:

- Publication of RCW code for two-dimensionally periodic structures in the SCATMECH library. 4Q 2009

Technical Contacts:
T. Germer

2. Assessment of Accuracy and Precision of Scatterometry – Scatterometry relies heavily on prior knowledge of the specific structure being examined. For example, optical properties of all incorporated materials are required for the simulations. Reasonable parameterization of sidewall profiles are required to yield meaningful profiles. The effects of line-edge or line-width roughness are usually ignored. In this program element, we are assessing the impact that each model parameter has on the outcome of the measurement. The goal is to establish an independent uncertainty budget that includes all sources of random and systematic uncertainties. Furthermore, we are assessing the sensitivity limits of scatterometry, to determine how far into the future scatterometry tools can provide critical dimension metrology. A computer program, OCDSense, was written and provided to ISMI member companies to help determine the sensitivity and uncertainty of scatterometry for an arbitrary one-dimensionally periodic grating in any given tool.

DELIVERABLES:

- Provide initial sensitivity report to ISMI for sensitiv-
  Publish a version of OCDSense for two-dimension-
  ally periodic structures. 3Q 2009

3. Scatterometry Measurements – We have recently upgraded our laser-based We have recently upgraded our laser-based Goniometric Optical Scatter Instrument (GOSI), Fig. 1, used for diffuse scatter measurements, to perform scatterometry measurements on industry-relevant targets on 300 mm wafers. The measurement capabilities include angle-scanned scatterometry at a number of discrete laser wavelengths. This instrument has the capability to perform conical scatterometry measurements and will be used to perform traditional measurements as well as measurements of higher-order, non-specular diffraction and diffuse scatter. Another instrument, a microspot spectroscopic ellipsometer, will be delivered in 2009. A long term goal is to develop reference scatterometry targets, measure them with these instruments, provide accurate determinations of their dimensions and profiles, and have uncertainties placed on the results. Another long term goal is to develop novel measurement modalities that improve the utility of scatterometry. One method we have demonstrated is microscope-based scatterometry using back focal plane imaging. This technique enables collection of multiple diffraction order scatterometry signatures in a single image, can be configured for both dense and isolated targets, and allows scatterometry and image-based metrology to be performed on the same tool. Another technique that we have developed is time-sequenced scatterometry, where we follow the evolution of a grating, for example, an imprinted polymer, while it reflows at elevated temperatures.

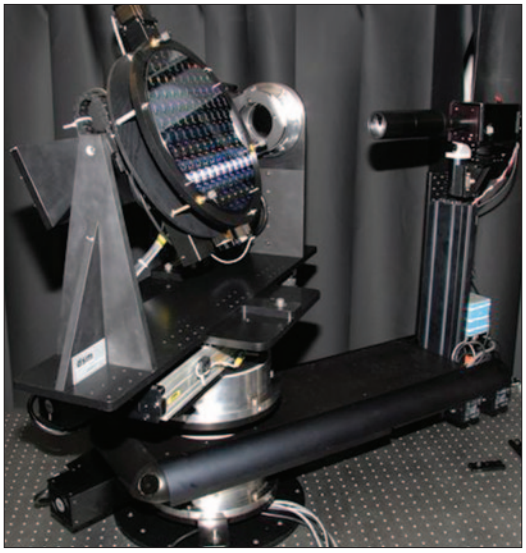

Figure 1. The new Goniometric Optical Scatter Instrument (GOSI) is a reference reflectometer for diffuse and specular scattering measurements having 300 mm sample capability.

DELIVERABLES:

- Construction of a spectroscopic scatterometry capability at NIST. 3Q 2009

Accomplishments

■ We have developed efficient rigorous coupled wave (RCW) software for one- and two-dimensionally periodic structures (arrays of two- and three-dimensional features). Results of the in-house code have been compared with finite difference time domain, surface integral equation, and other RCW implementations. This software is also configured to run on a large cluster computer, so that library generation is possible. The code for one-dimensionally periodic structures has also been extended to allow for anisotropic materials in the structure.

■ As part of our effort in assessing the precision and accuracy of scatterometry, we have performed a study of the sensitivity of scatterometry to CD and sidewall angle for a large number of different measurement modalities, including angle-scanned and wavelength-scanned reflectometry and ellipsometry, for amorphous silicon gate and gate-resist structures. This study included parameters

appropriate from the 45 nm half-pitch node to the 18 nm half-pitch node. The results demonstrated that scatterometry can achieve the necessary sensitivity to measure dense gratings at these nodes. Future work, however, will be necessary to achieve sufficient sensitivity to isolated features.

■ In the area of scatterometry-based optical critical dimension (OCD) measurement, we have recently measured OCD linewidth of lines in grating targets fabricated using the single-crystal critical dimension reference materials (SCCDRM) process. The SCCDRM implementation, developed by a multi-laboratory collaboration at NIST, provides lines with known geometries – typically vertical sidewalls – defined by the silicon lattice, and has led to development of a prototype linewidth standard for isolated lines designed for use in AFM calibration. We have shown that the linewidth obtained from the OCD technique for these targets is linearly related to linewidth obtained from SEM, with a slope near unity and zero offset (see Fig. 2). Continuing efforts to reduce linewidth roughness of the target, to analyze uncertainties in the OCD measurement, and to evaluate the suitability of these targets for OCD reference materials, are ongoing.

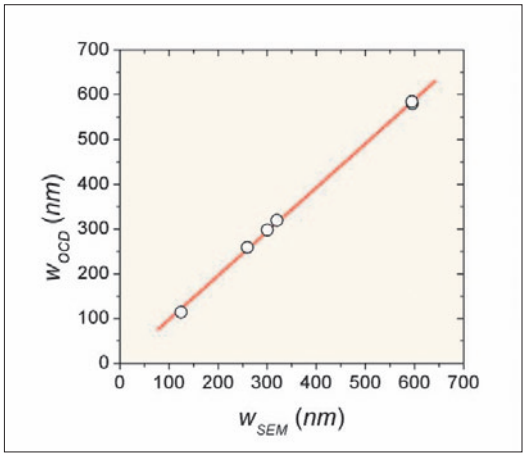

Figure 2. CD linewidth extracted from OCD, wOCD, versus linewidth measured by SEM, wSEM, for six targets on an SCCDRM chip.

■ We have also extracted OCD linewidth from scatterometry signatures of silicon-on-silicon gratings obtained using back-focal-plane imaging in a microscope. We investigated targets with only specular reflectance (grating pitch 300 nm) and those with both specular and higher-order diffraction (grating pitch 600 nm). Linewidths of 131 nm to 140 nm were obtained, with the back-focal-plane signatures demonstrating nanometer-level sensitivity to linewidth, and a linear relationship of linewidth obtained from scatterfield microscopy to linewidth measured by SEM was shown.

■ We developed a time-sequenced spectroscopic ellipsometry technique in which we characterized the reflow of polystyrene gratings while they were being held at their glass transition temperature. Figure 3 shows the profile of such a grating as a function of time. The time evolution of the surface profiles of low and high molecular mass polystyrene gratings were found to differ, due to the different flow, viscosity, and stress relaxation mechanisms present.

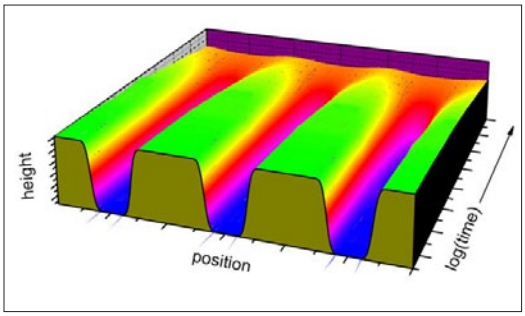

Figure 3. Line profiles measured by scatterometry as a function of time during annealing for a low molecular weight polymer grating at Tg = 100 °C.

Collaborations

International Sematech Manufacturing Initiative, Benjamin Bunday, Limits of Scatterometry Study.

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Small Angle X-Ray Scattering-Based Dimensional Metrology

Technical Contacts:
R. L. Jones
W. L. Wu

Goals

To develop a transmission geometry small angle X-ray scattering (SAXS)-based methodology to quickly, quantitatively, and non-destructively measure critical dimensions (CD) and feature shape with sub-nanometer resolution on production scale test samples. The focus is on delivering a technique capable of routine measurement of pattern shape, including critical dimension, sidewall angle, linewidth fluctuations, and line edge roughness, and statistical deviations across large areas in dense high aspect ratio patterns. This method is expected to provide a potential solution for the metrology needs of future semiconductor technology nodes. Further, the wavelengths utilized by SAXS based measurements well complement current metrology tools based on optical scatterometry, SEM, and AFM.

Customer Needs

The drive to reduce feature sizes to sub-50 nm technology nodes continues to challenge metrology techniques for pattern characterization. As outlined in the International Technology Roadmap for Semiconductors, existing techniques such as CD-SEM face significant technical hurdles in quantifying parameters such as Line Edge Roughness (LER) as pattern sizes decrease. Emerging methods based on techniques such as atomic force microscopy are being developed and evaluated. However, uncertainties remain in defining suitable metrology for standardized measurements of both organic and inorganic structures. To address these issues, NIST is evaluating the potential application of small angle X-ray scattering as a measurement tool for both process development and the calibration of standards for current industrial solutions such as CD-SEM.

Technical Strategy

1. Production of sub-30 nm, dense structures for semiconductors, memory, and data storage will demand the control of component size on the level of nm and in some cases sub-nm. These requirements will challenge traditional methods including CD-SEM and optical scatterometry. We are developing a transmission scattering based method capable of Angstrom level precision in critical dimension evaluation over large (50 μm x 50 μm) arrays of periodic structures (see Fig. 1). In contrast to optical scatterometry, SAXS is performed in transmission using a sub-Angstrom wavelength. The high energy of the X-ray source allows the beam to pass through a production quality silicon wafer, and could become amenable to process line characterization. The measurements are performed in ambient conditions, minimizing time required for sample preparation. The current capabilities of

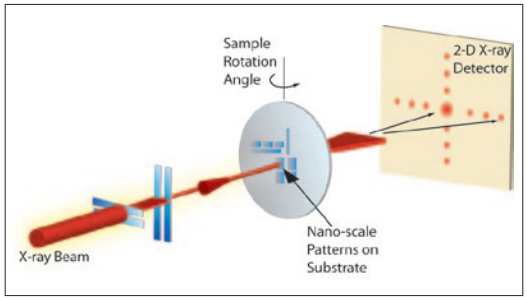

Figure 1. Schematic of the Critical Dimension Small Angle X-ray Scattering (CD-SAXS) configuration. Shown is the collimated high energy X-ray beam passing in transmission through a silicon wafer and scattering from the test pattern on the surface. The scattered X-rays are measured on a 2-dimensional X-ray detector. Cross sectional information is obtained by measuring the sample at varying sample rotation angles as depicted.

Figure 2. The world's first laboratory scale CD-SAXS prototype constructed on the NIST campus. Shown is the rotating anode molybdenum source (left side) used to generate high energy X-rays for transmission measurements on samples measured at varying angles of incidence on a 2-dimensional detector (back right).

commercially available X-ray sources and detectors are sufficient to implement a laboratory scale device capable of high precision measurements. NIST has designed and installed the world's first laboratory scale CD-SAXS device.

DELIVERABLES:

- Publish evaluation results from laboratory scale Complete and publish cross-sectional measurements using laboratory scale CD-SAXS instrument on patterns produced with EUV lithography as part of round-robin study with SEMATECH and Intel. 1Q 2009

2. Pattern shape metrology is facing new challenges as new 3D structures are emerging including FinFETs covered with nanometer thick layers of high-k materials (see Fig. 3). Effective manufacturing requires characterization of the total pattern shape as well as the dimensions and relative positions of individual layers. CD-SAXS features a capability to non-destructively probe test patterns with multiple materials. These measurements utilize data taken at a series of angles of incidence to reconstruct the average cross-sectional line shape. Preliminary results from an array of model tri-gate structures indicate an ability to measure these complex structures during different stages of processing, providing

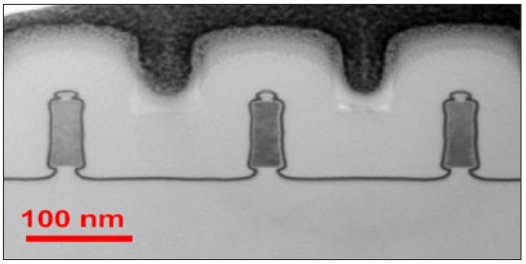

Figure 3. Cross sectional TEM image of a model non-planar architecture (i.e. "FinFET" or tri-gate) utilized as part of the round-robin measurements in collaboration with Intel and SEMATECH. CD-SAXS measurements are capable of providing the thickness of the dielectric layer (dark thin conformal layer in image) with sub-nm precision

valuable data on next-generation manufacturing. Ongoing analysis and technique refinement will develop models to quantify with high precision line shape parameters needed for patterns with multiple, distinct layers to establish the limits of the technique in future technology nodes.

DELIVERABLES:

- Develop and apply refined CD-SAXS models to incorporate the effects of multilayer coatings on line tops and sidewalls. 1Q 2009
- Complete CD-SAXS measurements of model non-planar architecture structures as a function of sidewall angle with thin conformal outer high-k layers. 4Q 2009

Accomplishments

■ We have developed and demonstrated the capabilities of CD-SAXS to provide high precision measurements of pattern pitch, linewidth, line height, and sidewall angle. The first measurements of sidewall angle were made at the Advanced Photon Source (Argonne National Laboratory) in collaboration with the IBM T. J. Watson Research Center (Q. Lin). The protocol involves measurements of the sample over a wide range of incident angles and reconstructing the Fourier representation of the pattern cross section. For a pattern with trapezoidal cross section, ridges of intensity propagate at twice the sidewall angle. The existence of the ridges is a model independent check on the validity of the trapezoidal model, while different shapes, such as a T-topped line, will produce different scattering patterns. The protocol has been generalized to more arbitrary shapes, including patterns with rounded corners and sidewalls.

■ Our group has also demonstrated a capability to measure correlated fluctuations in line edge position as a measure of line edge roughness. CD-SAXS measurements of a series of line/space patterns with model LER were produced using 193 nm lithography in collaboration with the Advanced Metrology Advisory Group (AMAG) coordinated by SEMATECH. This initial study provided key data on the sensitivity of CD-SAXS to LER, including the development of models for LER and LWR contributions, in lines possessing periodic sidewall roughness with amplitudes of 3 nm. In addition, a methodology and experimental data were published describing a route to use CD-SAXS as a measure of roughness propagating normal to the substrate. Samples of photoresist line/space patterns were provided by the IBM T. J. Watson Research Center (A. Mahorawala). This type of roughness is commonly observed in photoresists due to imprecise tuning of the underlying anti-reflective coating. Given the ability of CD-SAXS to extract the periodic component of

roughness from non-periodic, the technique is capable of quantitatively extracting this component of roughness even when the amplitude is small compared to the random component.

■ NIST has completed the second round-robin measurements of LER in sub-50 nm line/space resist patterns using CD-SAXS. Samples were designed with controlled LER to be measured by CD-SEM and CD-SAXS in blind measurements. Samples were produced in collaboration with Intel and measured by optical scatterometry at Intel, by CD-SEM at SEMATECH, and CD-SAXS at NIST in blind measurements. The data were collected and summarized in a paper presented at the 2008 SPIE Advanced Lithography meeting.

■ Studies have also demonstrated the potential of CD-SAXS to detect and to quantify the extent of sidewall damage of nanoporous low-κ materials patterned into line/space patterns. Previously, NIST had demonstrated that blanket low-κ films exposed to a plasma etch can have a skin layer with increased density and less hydrogen that may reflect the collapse of the pore structure. Since plasma etch effects can lead to an increase in κ, it is important to measure the sidewall structure (porosity, electron density, etc.) of patterned low-κ films. To address this challenge, SEMATECH provided line gratings etched in a candidate low-κ material, then backfilled the trenches with the same candidate low-κ material. This backfilled sample simplifies modeling efforts and highlights the damaged regions to X-rays. These results indicate the potential of CD-SAXS to probe more complex structures such as FinFETs non-destructively for future manufacturing needs.

■ The real time shape evolution of nanoimprinted polymer patterns were measured as a function of annealing time and temperature using Critical Dimension Small Angle X-ray Scattering (CD-SAXS). Periodicity, linewidth, line height, and sidewall angle were determined with nanometer resolution for parallel line/space patterns in poly(methyl methacrylate) (PMMA) both below and above the bulk glass transition temperature (Tg). Heating these patterns below Tg does not produce significant thermal expansion, at least to within the resolution of the measurement. However, above Tg, the fast rate of pattern melting at early time transitions to a slowed rate in longer time regimes. The time dependent rate of pattern melting was consistent with a shape dependent thermal stability, where sharp corners possessing large Laplace pressures accelerate pattern dynamics at early times.

Collaborations

Polymers Division, MSEL, Chengqing Wang, Derek L. Ho, Christopher L. Soles.

Intel Corporation, Kwang-Woo Choi, James Clarke, George Thompson, Melissa Shell, sub-50 nm structures.

SEMATECH, Ben Bunday, Pattern production and correlation to optical scatterometry (also through Advanced Metrology Advisory Group).

Advanced Photon Source, Argonne National Laboratory, Steven Weigand and Denis Keane, Small Angle X-ray Scattering Instrumentation Development.

Molecular Imprints, Doug Resnick. Characterization of sub-50 nm structures including dense arrays of posts.

IBM Yorktown Heights, Qinghuan Lin, Development of pattern shape and sidewall angle metrology.

Publications

C. Wang, K. Choi, Y. Chen, J. Price, D. Ho, R. Jones, C. Soles, E. K. Lin, W.-L. Wu, B. Bunday *"Non-planar high-k dielectric thickness measurements using CD-SAXS"* Proc. SPIE 7272, (2009).

D.L. Ho, C. Wang, E. K. Lin, R. L. Jones and W.-L. Wu, *"A Laboratory Scale Critical-Dimension Small-Angle X-ray Scattering Instrument"*, AIP Conference Proceedings, 931, 382, (2007).

C. Wang, R. L. Jones, E. K. Lin, W.-L. Wu, B. J. Rice, K. Choi, G. M. Thompson, S. J. Weigand, D. T. Keane, *"Characterization of Correlated Line Edge Roughness of Nanoscale Line Gratings using Small Angle X-Ray Scattering,"* J. Appl. Phys. 102, 024901 (2007).

C. Wang, R. L. Jones, E. K. Lin, W.-L. Wu, J. Leu, *"Standing Wave Roughness Characterization in Photoresists by Small Angle X-Ray Scattering,"* Appl. Phys. Lett. 90, 193122 (2007).

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C. Wang, R. L. Jones, E. K. Lin, W.-L. Wu, J. S. Villarrubia, K. Choi, J. S. Clarke, B. J. Rice, M. Leeson, J. Roberts, R. Bristol, B. Bunday, G. Orji, *"Line edge roughness characterization of sub-50 nm structures using CD-SAXS: Round-Robin benchmark results,"* Proc. SPIE 6518, (2007).

R. L. Jones, C. L. Soles, E. K. Lin, W. Hu, R. M. Reano, S. W. Pang, *"Pattern Fidelity in Nanoimprinted Films using CD-SAXS,"* J. Microlith. Microfab. Microsyst. 05, 013001 (2006).

R. L. Jones, W.-L. Wu, C. Wang, E. K. Lin, K.-W. Choi, B. J. Rice, G. M. Thompson, S. J. Weigand, D. T. Keane *"Characterization of Line Edge Roughness using CD-SAXS,"* Proc. SPIE 6152, 215 (2006).

H. W. Ro, Y. Ding, H. J. Lee, D. R. Hines, R. L. Jones, E. K. Lin, A. Karim, W.-L. Wu, C. L. Soles, *"The Role of Stress in Nanoimprint Lithography,"* Proc. SPIE 6151, 348 (2006).

R. L. Jones, T. Hu, C. L. Soles, E. K. Lin, R. M. Reano, S. W. Pang, D. M. Casa, *"Real Time Shape Evolution of Nanoimprinted Polymer Structures during Thermal Annealing,"* 6, 1723 (2006).

Grazing Incidence X-Ray Scattering-Based Dimensional Metrology

Technical Contacts:
W. L. Wu
R. L. Jones

Goals

To develop a grazing incidence small angle X-ray scattering (GI-SAXS)-based methodology to complement normal incidence or transmission SAXS for quantitatively and non-destructively measuring critical dimensions (CD) and feature shape with sub-nanometer resolution on production scale test samples. The focus is on delivering a technique capable of routine measurement of pattern shape, including critical dimension, sidewall angle, depth dependent composition, and statistical deviations across large areas in dense high aspect ratio patterns. In contrast to transmission, and small angle X-ray scattering GI-SAXS is performed in reflection, and this configuration results in both significant challenges in data interpretation and vast increases in signal-to-noise; therefore, it makes possible a reduction in measurement time. This method is expected to provide a potential solution for the metrology needs of future semiconductor technology nodes. In comparison with transmission SAXS, a longer X-ray wavelength X-ray beam can be used for GI-SAXS; this will help relax some of the strict optical collimation requirements and help reach high flux at the sample.

Customer Needs

The drive to reduce feature sizes to sub-32 nm technology nodes continues to challenge metrology techniques for pattern characterization. As outlined in the International Technology Roadmap for Semiconductors (http://public.itrs.net), existing techniques such as CD-SEM face significant technical hurdles in quantifying parameters such as Line Edge Roughness (LER) as pattern sizes decrease. Emerging methods based on techniques such as atomic force microscopy are being developed and evaluated. However, uncertainties remain in defining suitable metrology for standardized measurements of both organic and inorganic structures. To address these issues, NIST is evaluating the potential application of small angle X-ray scattering as a measurement tool for both process development and the calibration of reference standards for current industrial solutions such as CD-SEM.

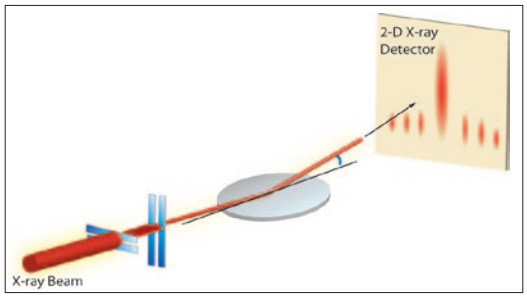

Figure 1. Schematic of the Grazing Incidence Small Angle X-ray Scattering (GI-SAXS) measurement configuration. Shown is the collimated sub-nm wavelength X-ray beam reflecting off the sample at a grazing angle, and the diffraction pattern measured on a 2-dimensional X-ray detector.

Technical Strategy

1. The emergence of viable lithography solutions for sub-32 nm patterning will require sub-nm precision control of CD and pattern shape built within multilayer structures. These requirements will challenge traditional measurement methods including CD-SEM and optical scatterometry. We are developing X-ray based dimensional metrology tools capable of Angstrom level precision in critical dimension evaluation over large (50 μm x 50 μm) arrays of periodic structures. As depicted in figure 1, Grazing Incidence Small Angle X-ray Scattering (GI-SAXS) is performed in reflection, using a configuration similar to current optical-based CD metrology tools. Due to the large interaction of the beam with the sample, generalizable quantitative models of GI-SAXS data are not available. Models to describe the high degree of interaction of the X-ray beam with the sample at grazing incidence will require detailed measurements of instrumental coherence length, resolution functions, and wavelength distribution. In addition, experiments are required to determine the effects of dynamic diffraction. Our approach is to measure the structure of test patterns using both CD-SAXS and grazing incidence geometries. Utilizing data from both CD-SAXS and GI-SAXS will provide a unique capability to develop quantitative models to incorporate the effects of dynamic scattering effects characteristic of grazing incidence scattering but absent in transmission scattering. Test samples will leverage results from CD-SAXS studies developed and measured in cooperation with the Advanced Metrology Working Group at SEMATECH and Intel.

DELIVERABLES:

- Evaluate the magnitude of the dynamic effects observed in GI-SAXS measurements through systematic comparisons of transmission and grazing incidence measurements on the same sample. 2Q 2009
- Implement integral equation model based approach to model and quantitatively fit GI-SAXS data. 4Q 2009

2. An emerging metrology need in semiconductor and data storage fabrication is in directed self-assembly (DSA). Here, soft materials such as block copolymers assemble with structure on the order of 10 nm under the influence of a directing field or template. The soft nature of their interfaces and the large areas involved present new metrology challenges as highlighted in the emerging lithography section of the ITRS. With a significantly higher signal to noise ratio, GI-SAXS is capable of providing measurements of dimensions during assembly, providing unique insights into potential process parameters and uniformity of the structures over macroscopic areas. The small electron density contrast of these films prohibit the application of transmission SAXS. Our strategy is to develop models for dimensional metrology of block copolymers undergoing directed self-assembly through comparisons of GI-SAXS data to analogous data from transmission small angle Neutron scattering, performed at the NIST Center for Neutron Research.

DELIVERABLES:

- Complete CD-SAXS measurements of test patterns produced by optical lithography with high precision transmission scattering models. 2Q 2008
- Complete GI-SAXS measurements of the same test patterns used in CD-SAXS deliverable item listed above. 4Q 2008
- Evaluate the magnitude of the dynamic effects observed in GI-SAXS measurements and start to develop the theoretical framework for quantitative data analysis. 4Q 2008

Accomplishments

■ Measurements of a block copolymer film assembling under a thermal gradient have been executed using both small angle neutron scattering (SANS) and grazing incidence small angle x-ray scattering (GI-SAXS). The data shown in figure 2 describe the evolution of a thin film of poly(styrene-b-methyl methacrylate) (PS-b-PMMA) that orders in a cylindrical morphology. The cylinders are densely packed at nearly a 1:1 ratio, and can be selectively etched into the underlying substrate. GI-SAXS measurements capture the evolution of structure during directed assembly, demonstrating the effectiveness of thermal gradients in controlling orientation and grain size in DSA. Analogous measurements from small angle neutron scattering (SANS), performed at the NIST Center for Neutron Research, are providing key information on dynamic scattering effects to aid the development of quantitative models for GI-SAXS in this application.

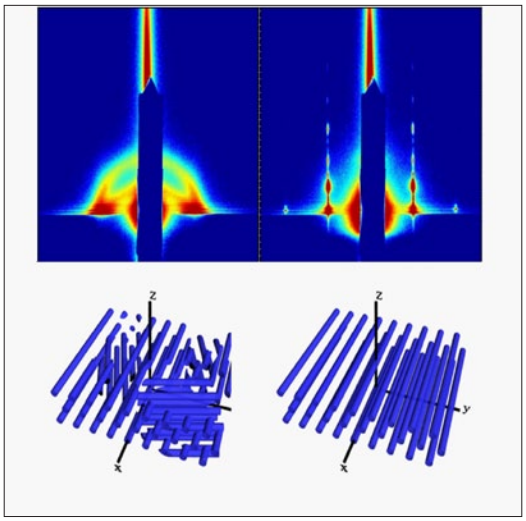

Figure 2. GI-SAXS data measured on a block copolymer film at varying stages of directed assembly. In the detector images (top), the beam is reflected vertically with the directly reflected beam blocked by a beamstop to prevent detector damage. The scattered intensity is shown for a film of poly(styrene-b-methyl methacrylate) as it orders under a thermal gradient. The early time data (left) shows cylinders with a repeat period of 38 nm ordered with micron size grains, where the grains are isotropically oriented. After longer anneal times, the cylinders adopt a single orientation parallel to the substrate and in the direction of the beam (right).

■ We have completed the construction and preliminary alignment tests of a sample stage with alignment microscope and detector accessories suitable for performing high precision GI-SAXS measurements. Initial measurements of a test sample in both transmission CD-SAXS geometry demonstrate the additional complexity and potential information content of grazing incidence measurements.

Collaborations

Polymers Division, MSEL, R. Joseph Kline, Chengqing Wang, Derek L. Ho, Christopher L. Soles.

Hitachi Global Data Storage, Ricardo Ruiz, GI-SAXS metrology for directed self-assembly.

Intel Corporation, Kwang-Woo Choi, James Clarke, George Thompson, sub-50 nm test structures

SEMATECH, Ben Bunday, Pattern production and correlation to optical scatterometry (also through Advanced Metrology Advisory Group).

Advanced Photon Source, Argonne National Laboratory, Steven Weigand and Denis Keane, Small Angle X-ray Scattering Instrumentation Development.

Recent Publications

C. Wang, K. Choi, Y. Chen, J. Price, D. Ho, R. Jones, C. Soles, E. K. Lin, W.-L. Wu, B. Bunday *"Non-planar high-k dielectric thickness measurements using CD-SAXS"* Proc. SPIE 7272, (2009).

D.L. Ho, C. Wang, E. K. Lin, R. L. Jones and W.-L. Wu, *"A Laboratory Scale Critical-Dimension Small-Angle X-ray Scattering Instrument,"* AIP Conference Proceedings, 931, 382, (2007).

C. Wang, R. L. Jones, E. K. Lin, W.-L. Wu, B. J. Rice, K. Choi, G. M. Thompson, S. J. Weigand, D. T. Keane, *"Characterization of Correlated Line Edge Roughness of Nanoscale Line Gratings using Small Angle X-Ray Scattering,"* J. Appl. Phys. 102, 024901 (2007).

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R. L. Jones, C. L. Soles, E. K. Lin, W. Hu, R. M. Reano, S. W. Pang, *"Pattern Fidelity in Nanoimprinted Films using CD-SAXS,"* J. Microlith. Microfab. Microsyst. 05, 013001 (2006).

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R. L. Jones, T. Hu, C. L. Soles, E. K. Lin, R. M. Reano, S. W. Pang, D. M. Casa, *"Real Time Shape Evolution of Nanoimprinted Polymer Structures during Thermal Annealing,"* 6, 1723 (2006).

Atom-Based Dimensional Metrology

Technical Contacts:
R. Silver

Goals

Provide technological leadership to semiconductor and nanoelectronics manufacturers and other government agencies by developing the methods, tools, and artifacts needed to apply leading edge, high-resolution atom-based dimensional measurement methods to meet the metrology needs for advanced lithography. One specific goal is to provide customers with the techniques and standards needed to make traceable dimensional measurements on wafers with nanometer accuracy. We are developing nanometer-scale three-dimensional structures of controlled geometry whose dimensions can be measured and traced directly to the intrinsic crystal lattice. These samples are intended to be dimensionally stable and allow transfer to other measurement tools that can measure the artifacts with dimensions known on the nanometer scale.

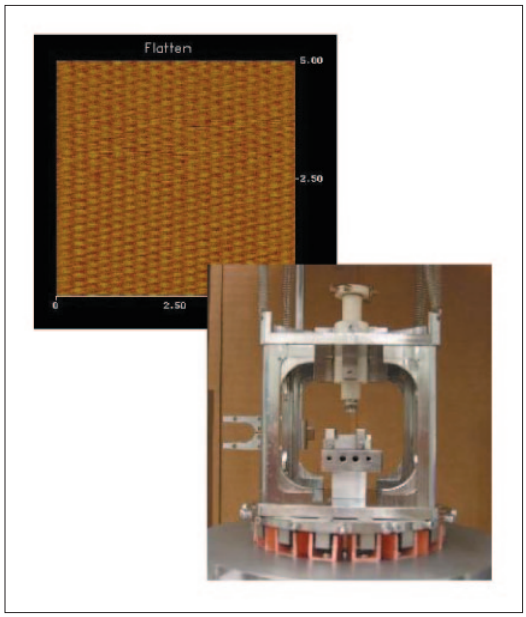


Figure 1. A new STM structure design has been implemented to improve the atomic scale imaging and structural characteristics. This system will provide improved nanometer scale interferometer-based imaging and measurement capabilities.

Customer Needs

This project responds to the U.S. industry need for length-intensive measurement capabilities and calibration standards in the nanometer scale regime. The new class of scanned probes have unparalleled resolution and present a unique solution to meet the future measurement, test artifact, and calibration standards needs of the nanoelectronics industry. One important application of the high-resolution SPM methods is in the development of test artifacts and linewidth standards whose dimensions can be measured and traced through the crystal lattice from which they are made. In addition, these high-resolution tools can be coupled directly to a unique NIST-designed picometer resolution interferometer (Fig. 1).

The work funded in this project is for the development of atom-based test artifacts and linewidth standards to assist in the development of high-resolution imaging techniques and calibration of dimensional metrology tools. One focus of the research is to enable the accurate counting of atom spacings across a feature in a controlled environment and to subsequently transfer that artifact to other measuring instruments as a structure with atomically known dimensions.

An essential element of this project is the fabrication of test artifacts and structures for the development of high resolution imaging methods. It is imperative to enable fabrication methods for sub-10 nm sized features. Several recent developments in optical microscopy, scatterometry and SEM metrology require test samples with critical dimensions below 10 nm. These test structures are simply not available commercially at this time. In this project we are developing the methods for fabrication of sub-10 nm sized features and etching methods to transfer these patterns into the silicon substrates (see Fig. 2, next page). As critical dimensions continue to shrink, the detailed atomic structure, such as edge roughness or sidewall undercut, of the features to be measured represents a larger portion of the measurement uncertainty. Furthermore, particularly with SEMs and optical CD tools, the instrument response and the uncertainty in the edge location within an intensity pattern becomes a significant issue due to the increased sensitivity to detailed elements of the edge detection model. The complexity of these physics-based scattering models and large computer resources required for each individual computation make the concept of reference samples with known geometry and width essential. This project is developing samples of

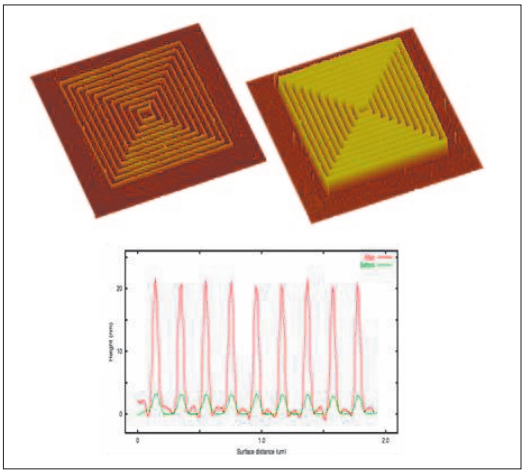


Figure 2. A demonstration of the nanofabrication process with an RIE process used to transfer the patterns into the silicon substrate.

known geometry and atomic surface structure that will yield well defined dimensional measurements. One goal is a measurement that results in a specific number of atoms across the line feature or between features. The process being developed allows for samples to be measured in the UHV environment and then stabilized and subsequently transferred to other instruments.

The methods of atom counting and high-resolution interferometry outlined in this project description are non-destructive and are intended to yield samples which can be measured by various instruments such as an SEM optical CD tool with subsequent re-measurement on the atomic scale. This is a unique and important element of this work since there are no other known methods that allow this kind of atomic dimensional measurement without being destructive. In addition, this new method opens up the possibilities of basing the measurement metric on the intrinsic crystal lattice.

Technical Strategy

The technical work is focused into four thrust areas.

1. The development of methods to prepare lithographically patterned three-dimensional structures in semiconductor materials. These structures are being prepared in silicon to allow the atomic surface order, which is commensurate with the underlying crystal lattice. This involves using either advanced photolithography methods, electron beam lithography, or the STM itself to fabricate very small nanometer scale features as shown in Fig. 2.

DELIVERABLES:

- Write features in (100) silicon with critical dimensions smaller than 5 nm. Apply the pattern generation process and etch features for use as test structures using the Scanning Tunneling Microscope (STM). 4Q 2009
- Work with DARPA, Zyvex and CNST to develop improved methods for etching nanostructures written in silicon. Use Reactive Ion Etching (RIE) techniques to etch features with sub-5 nm dimensions in silicon. 2Q 2010

2. The development of techniques for the preparation of SPM tips with reproducible geometries and the direct characterization of the SPM tip geometry and dimensions on the atomic scale. These well characterized tip probes can then be used to make robust, repeatable measurements on samples with atomic resolution at the sub-nanometer length scale, see Fig. 3. We continue to develop SPM tip etching, field evaporation, and cleaning procedures which reliably yield stable W (111) tips and produce atomic resolution on Si (7x7) surfaces and 2x1 reconstructed Si (100) surfaces. These tips are also useful in SEM applications for use as nanotip SEM field emitters. Our tip preparation methods leave us uniquely qualified in this arena.

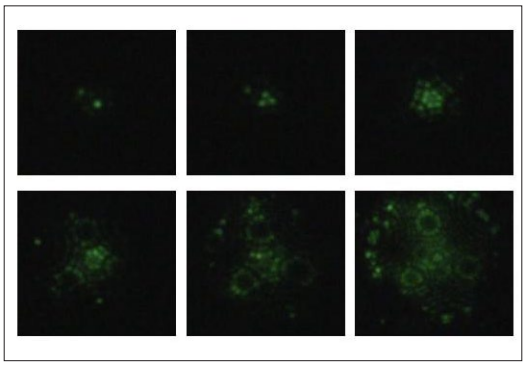


Figure 3. A series of FIM images showing reproducible formation of single atoms and atomic trimer showing formation at the apex of a W (111) single crystal tip.

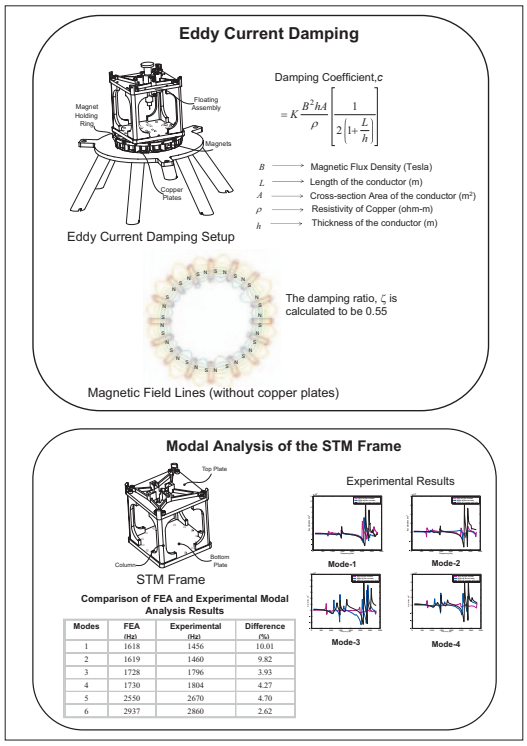
DELIVERABLES:

- Develop and evaluate new N2 field evaporation and etching methods for W (111) single crystal tungsten tips. Determine the sharpness and stability of these W tips for use in atomic resolution STM imaging. 2Q 2009
- Evaluate single atom tips using noble metal materials reconstructed on the end of W tips. Evaluate using FIM and STM atomic resolution imaging. 3Q 2009

3. Development of artifacts that can be atom counted and subsequently measured in other metrology tools such as SEM and AFM. The integrity of the line geometry, such as side wall angle, is crucial to having useful artifacts for linewidth specimens. This effort for linewidth artifacts is currently focused on developing Si (111) wet chemical processing methods with reduced process temperatures which yield atomically ordered surfaces. The use of wet chemical processing has been demonstrated on atomically ordered Si surfaces at significantly reduced temperatures. Current research utilizes in situ processing apparatus from the UHV STM and concentrating on the reproducible production of atomically ordered Si surfaces and Si (100) step and terrace structures.

DELIVERABLES:

- Use the UHV sample heating and tip preparation capabilities in the Omicron UHV STM system for atomic resolution imaging of Si (111) hydrogen terminated surfaces. Investigate atomic resolution imaging of UHV H-terminated Si samples. Use the in situ prepared samples from the UHV preparation facility to evaluate improved Si imaging with alternative tip materials and atomic surface reconstructions. 3Q 2009



Modes	FEA (Hz)	Experimental (Hz)	Difference (%)
1	1618	1456	10.01
2	1619	1460	9.82
3	1728	1796	3.93
4	1730	1804	4.27
5	2550	2670	4.70
6	2937	2860	2.62

Figure 4. Dynamics simulation results used to optimize the mechanical structure and damping mechanism. Finite element modeling with experimental verification is an important tool to achieve atomic resolution and stability.

4. Develop the UHV Omicron system and the in-house designed facility for improved robust atomic resolution imaging, (see Figs. 4 and 5). The new imaging and sample processing capabilities are being developed and applied to etched silicon features in collaboration with the Zyvex-led DARPA-funded Atomically Precise Manufacturing Consortium. The intent is to provide atomically resolved and precisely imaged quantitative results on etched silicon substrates. These nano-meter-scale standard artifacts with atomically ordered surfaces will then act as linewidth or magnification calibration samples.

Accomplishments

■ The atom-based dimensional metrology project is successfully engaged in a 3 phase 5 year funded DARPA contract to develop massively parallel arrayed tip nanofabrication techniques. This DARPA funded contract is a comprehensive collaborative effort between NIST, industry leader Zyvex, University of Illinois, the University of Texas and other partners. This represents a significant DARPA focus for advanced lithography and metrology on the atomic scale which is fully extensible to atomically precise patterning and metrology to support and enable arrayed tip fabrication at the atomic scale.

■ Atomically sharp W (111) tips can now be repeatedly prepared with single, two and three atomic configurations at the apex. This is now a robust methodology for repeatable UHV tip preparation. This was accomplished using the tip processing capability in the UHV STM system and the field ion field electron microscope (FIFEM). We are working with industry and university leaders to evaluate alternative technologies for atomic resolution tip performance.

■ A hydrogen cracker that disassociates the hydrogen molecules to initiate atomically ordered hydrogen terminated surfaces has been installed. Current research is aimed at optimizing the in situ UHV hydrogen termination process. This is an important step in realizing robust H surface termination processes in a UHV environment. This process stabilizes the surface for several days as well as creating an effectively atomic resolution resist.

■ We have used the field ion microscope (FIM) techniques to analyze single atom tips using noble metal atoms reconstructed at the apex of

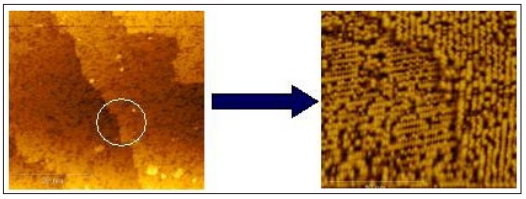


Figure 5. Atomic resolution image of a Si (100) surface prepared in vacuum. Current research within the DARPA funded effort is focused on atomic scale fabrication and measurements of these widely used substrates that are based on the intrinsic crystal lattice.

a single crystal W (111) tip. The noble metal atoms are heated to a moderately high temperature to reconstruct spontaneously into a pyramidal formation with a single atom at the apex. These W tips will be directly characterized for use as SPM tips with dimensional analysis on the atomic scale.

■ An invited poster presentation was given at this years EIPBN conference on the silicon etching processes developed at NIST in the atom-based dimensional metrology project. The presentation covered patterns fabricated with features as small as 10 nm written in hydrogen-terminated silicon surfaces. Also, comprehensive FIM analyses of tip processes were covered. The importance of etching structures in Si (100) is now recognized as one of the essential DARPA funded directions as a part of the atomically precise manufacturing consortium. NIST will continue to develop lithography methods and plasma-etch methods for sub-5 nm CD features.

■ A workshop from the SPIE Nanotechnology Working Group on massively arrayed nanofabrication techniques for future semiconductor manufacturing was held at Microlithography 2008. The workshop was organized by Rick Silver and Chris Soles included presentations and a panel discussion involving several industry and University leaders. The Nanotechnology Working Group is chaired by Rick Silver and Chris Soles and has served as a forum for developing and applying nanotechnology related manufacturing and fabrication elements which will directly benefit the semiconductor industry.

■ We have prepared atomically flat surfaces and obtained atomic order on Si (100) surfaces. The routine imaging of these surfaces on the atomic scale is a new focus to both move the silicon processing to the more widely used Si (100) surfaces and to use more controlled UHV processing techniques. These results are a substantial step forward in repeatable silicon surface preparation for atomic scale metrology and are now being carried out in collaboration with DARPA and several industry/university researchers. The results, seen in Fig. 5, show the recent progress in atomic resolution imaging and preparation of the Si (100) surfaces and are a primary direction for the DARPA funded research manufacturing community.

■ An in-depth paper was published in the Journal of Physical Chemistry. The paper is a comprehensive set of experimental and theoretical analyses of the preparation of silicon surfaces. This work was carried out in large part by Post Doc Hui Zhou and in collaboration with the University of Maryland, Department of Physics. This paper follows on a paper published in late 2005 in the Journal of Physical Chemistry titled "The Influence of defects on the morphology of Si (111) Etched in NHF". In this new paper we have extended the kinetic Monte-Carlo simulation method to study the etching dynamics of Si (111) surfaces in NH4F in a time-resolved basis. We have examined the step-flow dynamics of Si (111) etching using various simulation window sizes for variety of miscut angles and miscut orientations as well as those parameters which affect the formation of etch pits.

■ A paper was presented to the ASPE special topics conference by Summanth Chikkamaranahalli, a graduate student from the George Washington University. The paper is a comprehensive analysis of damping and precision structures for use in STMs and atomic scale imaging. The analysis and modeling have been used in the development of the NIST STM for the atom-based dimensional metrology project. The scanning tunneling microscope was designed by the NIST team in collaboration with Prof. Vallance at the George Washington University. The finite-element analysis (FEA), static and dynamics analysis using Promechanica packages gave the researchers quantitative tools to evaluate and develop the STM imaging head, and larger mechanical structure.

Collaborations

DAROPA, Zyvex, University of Illinois, University of Texas, Sematech, IBM, University of Maryland, Dept. of Physics, George Washington University, Dept. of Mech. Eng.

Publications

H. Zhou, J. Fu, and R. M. Silver, *"A Time-resolved Kinetic Monte-carlo Simulation Study on Si (111) Etching,"* Journal of Physical Chemistry C, Vol. 111, p. 3566 (2007).

S. Chikkamaranahalli, R. Vallance, B. Damazo, and R. M. Silver, *"Damping Mechanisms for Precision Applications in UHV Environment,"* Proc. ASPE Conf., Pitts. PA (2006).

S. Chikkamaranahalli, R. Vallance, B. Damazo, R. M. Silver, and J. Gilsinn, *"Dynamic Modeling and Vibration Analysis of a UHV Scanning Tunneling Microscope,"* Proc. ASPE Conf., Norfolk VA (Oct. 2005).

H. Zhou J. Fu, and R. M. Silver *"The Influence of Defects on the Morphology of Si (111) Etched in NH4F,"* J Chemical Physics B, 109, 23386 (2005).

Fabrication and Calibration Metrology for Single-Crystal CD Reference Materials

Technical Contacts:
M. W. Cresswell

Goals

The goal of this project is to develop test-structure-based reference materials with emphasis on supplying road-map-compliant physical standards for critical-dimension (CD) metrology-tool development and calibration. The specific near-term goal is fabricating, and supplying to the NIST SRM (Standard Reference Material) office for distribution, a quantity of CD reference-features with nominal CDs in the range 20 nm to 160 nm and having 2σ (expanded uncertainties) of less than 1.1 nm by September 2009. The motivating application is primarily AFM-tip calibration but other possible applications that have emerged, since the research was begun, include the monitoring of CD SEM and optical CD metrology (OCD) tools. The technology that this project has developed for fabricating CD reference materials is known as the Single-Crystal CD Reference-Material (SCCDRM) implementation. It is now clear that the SCCDRM format could also be advantageously applied to the development of related nano-artifacts such as step-height standards. An over-arching goal is to fabricate and calibrate a selection of SCCDRM-based artifacts that will be made available to industry and academic users through the NIST SRM Program. This goal will be well-served by the Project's ongoing uncertainty-reduction program which will take advantage of unique and diverse expertise at NIST in alternative primary- and transfer-metrologies such as SAXS (Small-Angle X-Ray Scattering) and angle-resolved optical scatterometry.

Customer Needs

The Semiconductor Industry Association's International Technology Roadmap for Semiconductors (ITRS) 2007 p.39 under "Reference Materials" Section in the Metrology Volume, states that it is critically important to have suitable reference materials available when a measurement is first applied to a technology generation, especially during early materials- and process-equipment development. This project is concerned specifically with ensuring a source of such reference materials to satisfy the stated need throughout the near-term years.

Each generation of ICs is characterized by the transistor gate length whose control to specifications during IC fabrication is a primary determinant of manufacturing success. The roadmap projects the decrease of microprocessor unit (MPU) physical gate lengths used in state-of-the-art IC manufacturing from present levels of 28 nm to 13 nm during the near-term years. Scanning electron microscopes (SEMs) and other systems used for traditional linewidth metrology exhibit measurement uncertainties exceeding specifications for these applications. It is widely believed that the situation can be at least partially managed through the use of reference materials with linewidths traceable to nanometer-level uncertainties. Until now, such reference materials have been unavailable because the technology needed for their fabrication and certification has not been available.

Customers need to replace the carrier-wafer with a monolithic implementation because the former is vulnerable to contamination originating during post-assembly cleaning. Ordinarily this is not a leading concern in AFM-tip calibration, although it cannot be dismissed for SCCDRM use in ultra-clean facilities. Otherwise, tip calibration is becoming widely recognized as an application for which SCCDRM reference materials are well suited. However, an emerging application of interest in the industry is SEM tool calibration. In this application, regular reference-material feature-cleaning is necessary due to the nature of the metrology.

The emerging metrology known as optical-CD (OCD) scatterometry translates broadband light, diffracted from an on-wafer grating patterned into the resist or film, into accurate profiles of the grating's features from which key parameters, such as CD, can be extracted. Whereas currently favored metrology tools such as CD scanning electron microscopes and AFMs require a vacuum wafer environment, OCD metrology does not, and is fast and non-invasive. The possibilities of OCD extend to characterizing the sidewall angle and height of critical features. Until physical standards are available, the full promise of OCD control scatterometry may not be met.

Further details of customer needs that have been identified since the SCCDRM distribution to SEMATECH Member Companies in January 2005, and now impact the project's responding technical strategy, are described in the next section.

Technical Strategy

The fundamental SCCDRM technical strategy is to pattern Silicon on Insulator (SOI) device layers with lattice-plane selective etches of the kind used in silicon micro-machining, which provides reference features with quasi-atomically-planar sidewalls. This unique attribute is highly desirable for the intended applications, particularly if sidewall nano-planarity can be further extended to reference-feature segment lengths of up to 2 micrometers. Essential elements of the implementation include starting silicon SOI wafers with the device layer having a (110) orientation, alignment of the reference features to specific lattice vectors, and lithographic patterning with lattice-plane selective etches of the kind used in silicon micro-machining. However, the difficulty of obtaining satisfactory SOI material in larger diameters has driven us towards parallel evaluation of a bulk-wafer starting-material strategy. The roadmap states that measurement and certification of reference materials must be carried out using standardized or well-documented test procedures. The traceability path for dimensional certification of the project's SCCDRMs is responsive to this requirement and originates with measurement of a selection of reference-feature CDs with both Atomic-Force Microscopy (AFM) and high-resolution transmission electron microscopy (HRTEM) imaging. The former technique is highly repeatable and of manageable cost while the latter enables a lattice-plane count that allows expression determination of CD in terms of a traceable distance, which is the periodicity of silicon (111) lattice planes. However, HRTEM is totally destructive and thus is not useful for supplying reference features to end users. The project's traceability strategy thus features state-of-the-art AFM as a transfer metrology to deal with this constraint. Transfer metrology relates CDs extracted by AFM to be traced to SI units through the construction of a so-called calibration curve. An example of such a curve is shown in Fig. 1.

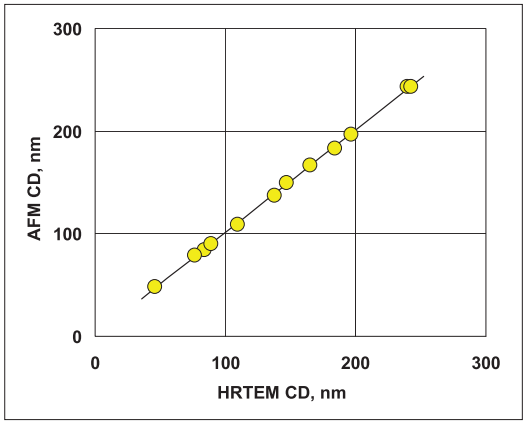


Figure 1. Transfer metrology relates CDs extracted by AFM to be traced to values SI units through the construction of a so-called calibration curve.

To maintain maximum possible accuracy in the transfer-metrology operation, an elaborate reference-feature selection protocol has been established to identify reference features that qualify by virtue of their CD uniformity, as contributors to the construction of the calibration curve, or for delivery to end users. Multiple reference features on a large set of as-patterned test chips are identified initially by high-power optical inspection. This procedure checks primarily for continuity, cosmetics, and apparent uniformity of the narrowest-drawn sets of six features that are incorporated into test structures, which are called HRTEM targets. Drawn feature linewidths range from 350 nm to 600 nm and the "process bias" typically decreases these to etched CDs of between 50 nm and 300 nm. The "best" 10 % of the AFM targets passing optical inspection, and having estimated replicated CDs in the range 50 nm to 200 nm, are then SEM-imaged at 20 K magnification to narrow the selection process further. Digitized profiles of the CDs of top-down SEM images are then extracted at 25 nm intervals. The measurements are transferred to a database, which is then interrogated to identify chips, and AFM targets on them, that have more uniform SEM-CD profiles at the narrower CDs — typically less than 150 nm. Candidate AFM targets identified on each chip are then CD-profiled by AFM. Chips having AFM targets with all six features having superior uniformity are then partitioned into a calibration sub-set and a product subset. All six features of the selected targets on the chips on the calibration sub-set are then subjected to HRTEM imaging. These are the chips whose designated AFM targets are to be used as contributors to the calibration curve. The design of all HRTEM targets enables the capture of six HRTEM images in a single dual-beam FIB-and-thinning operation. Moreover, since the features on each target are designed such that they are systematically staggered in CD by increments of 30 nm, HRTEM inspection of a single target enables the generation of a 6-point calibration curve spanning a 150 nm range. However, the logistics described above make the CD-traceability path very costly to implement, and hinder the pace

of necessary technology advancement. A central problem is that adequate facilities for both HRTEM and AFM tend to have limited availability. Cost becomes substantial when operator/engineering skills, maintenance, down time, etc., are accounted for. For these reasons we have proposed evaluation of two alternative traceability approaches. The first is to identify technically and economically acceptable replacements for either or both of the current primary and transfer metrologies, and the second is to eliminate the need for transfer metrology altogether by calibrating with a single traceable metrology on a 100 % basis. As far as replacing HRTEM as the primary metrology is concerned, we have observed that both SAXS and OCD could provide competitive accuracy for the average CD of features of an SCCDRM grating. Of course, it follows that the uncertainty of a local CD within the grating is then driven by the uniformity of the grating's features. A possible AFM transfer-metrology replacement is CD-SEM. Its superior repeatability for a transfer-metrology application is very attractive while its generally unproven accuracy is inconsequential for this application. Whereas a novel approach to generating a calibration curve for a HRTEM/CD-SEM primary/secondary-metrology implementation has been proposed, the CD-SEM tool's tendency to deposit hydro-carbon contamination remains a central issue. Clearly, verifiable contamination-removal procedures have to be implemented. It appears that scatterometry-based OCD metrology is also feasible as a single traceable metrology for calibration because it is relatively inexpensive and, unlike HRTEM, is non-destructive to apply. However, the issue that the uncertainty of a local reference CD within the grating would be driven by the uniformity of the grating's features needs to be addressed by fabrication-process engineering. While it is not clear that CD-SEM metrology is ready to perform as a primary metrology for the subject application, it appears to be the only possibility for replacing AFM as the transfer metrology for the calibration of isolated lines. On the other hand, this project has proposed a test-structure innovation that would allow the transfer of a measurement of the average CD of a grating metrology to an isolated line. However, the proposed method has not yet been evaluated in the laboratory. Because 200 mm (110) starting material until recently has been unobtainable at an acceptable cost, this project's technical strategy has so far been to dice each 150 mm (110) wafer after lithography and to mount the separate chips in micro-machined standard 200 mm carrier wafers to accommodate the product reference-feature chips. The scheme is shown in Fig. 2. The result is that finished units can be delivered at an acceptable cost. The Project's technical strategy is now evolving towards a monolithic-wafer implementation in response to industry pressure to make SCCDRMs more compatible with automated wafer-handling systems and related end-user requirements. These measures include:

- replacing the carrier-wafer with a monolithic 200 mm wafer implementation evolved from initial development with smaller diameter whole wafers,

- replacing the buried oxide of SOI wafers with a buried boron diffusion having an epitaxial silicon layer deposited over it or a heavy deep boron implantation prior to wafer etch,

- using electron-beam direct-write patterning of a silicon-nitride hard-mask film deposited on bulk-silicon wafers for pattern transfer from database to facilitate CD reduction to 20 nm,

- adopting additional measures to further reduce the uncertainties of calibrated CDs to less than 1.0 nm,

- demonstrate SEM-deposited hydro-carbon contamination management by the implementation of verifiable contamination-removal procedures,

- improving the reference feature's CD uniformity to enable certifying the CD of an extended length of reference feature,

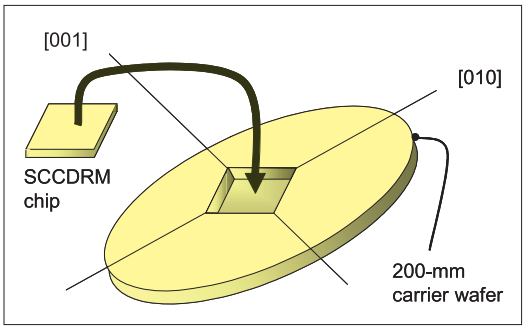


Figure 2. The technical strategy has been to dice each 150 mm (110) wafer after lithography and to mount selected chips in micro-machined standard 200 mm carrier wafers to accommodate the product reference-feature chips.

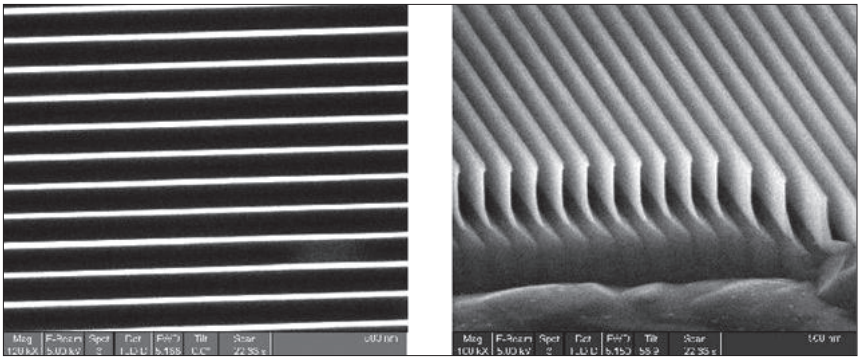


Figure 3. OCD grating section fabricated with SCCDRM technology which exhibits 36-nm lines at 180-nm pitch and having a height of 430 nm. The lithography was performed by collaborating UT-Austin staff using their direct-write e-Beam system.

- improved on-wafer navigation for end-user convenience,

- calibrating a selection of OCD gratings that are replicated at the same time as the isolated lines,

- improved management of the organic residues that sometimes impair the cosmetic appearance of the reference features and their environment on the wafer and to some extent adversely affect the uncertainty values of the delivered product, and

- evaluate a novel test structure concept to allow the extraction of isolated-line CDs from grating-based CD-metrology.

Implementing these aggressive strategic elements will continue to benefit from innovative teaming with other laboratories. Our strategy takes a page from the roadmap that explicitly states that standards institutions need rapid access to state of the art development and manufacturing capability to fabricate relevant reference materials (ITRS 2005 p. 36 under "Reference Materials.") Likewise, the roadmap states that metrology, process, and standards research institutes, standards organizations, metrology tool suppliers, and the university community should continue to cooperate on standardization and improvement of methods and on production of reference materials (ITRS 2007 p. 2 under "Scope".) In response to this mandate, we have developed a unique relationship with the Microelectronics Research Center (MRC) at the University of Texas in Austin. One of the products of our collaboration is the extraordinary OCD grating section shown in Fig. 3 which exhibits 36 nm lines at 180 nm pitch and having a height of 430 nm. The lithography in this case was done by with MRC's JEOL direct-write e-Beam system.

DELIVERABLES:

- Apply electron-beam direct-write patterning of hard-mask films on whole wafers to enable replicated-CD reductions to 20 nm. 4Q 2008
- Evaluate buried boron-diffusion etch-stops or depositing an epitaxial film over a heavily deep-boron implanted silicon for enhancing the quality of SCCDRM reference features. 2Q 2009
- Repeat and refine the screening experiment to establish the optimum selection of combinations of pattern-transfer factors, including, for example, etch concentration and temperature, for driving down reference-feature uncertainties through CD-uniformity enhancement. 3Q 2009
- Design, fabricate, and evaluate innovative SCCDRM-based test structures that enable tracing the CDs of isolated lines from whole-grating measurements by OCD or SAXS, for example. 4Q 2009
- Document an appropriate scheme to manage hydro-carbon contamination which CD-SEM tools are observed to deposit. 4Q 2009
- Implement and evaluate software to provide CD-roughness profiles and average CD from multiple-feature images to facilitate selection of isolated lines having superior qualities for use as reference features. 1Q 2009
- Investigate contribution of factors such as the roughness of the linewidths of hard-mask features to the quality of features replicated in SCCDRM processes. 3Q 2009

Accomplishments

■ The project thrust to fabricate reference features on whole wafers has produced first silicon. A hard mask film of 230 nm of silicon nitride was deposited by LPCVD on a selection of (110) wafers. After resist application, three were exposed in the NIST CNST E-beam system, two with a "rosette" pattern to enable identification of <112> vectors in the wafer surface, and one with a sub-100-nm reference-feature pattern. After hard-mask etch and resist strip, the hard-mask pattern was transferred to substrate silicon in a KOH solution to a depth of approximately 250 nm. Optical inspection of the rosette patterns successfully identified the alignment of the lattice <112> direction in the wafer surface to the wafer flats. These directions were readily evident in the two rosette wafers through comparison of the flat-bottom trench width in silicon with the nitride trench widths. This information will ensure correct orientation of the reference-feature patterns relative to the flats on other wafers from the same ingot.

■ Although we are winding down the fabrication of SOI-chip-based SCCDRMs mounted in carrier wafers, some further effort has successfully been applied to the elimination of a troublesome process defect. This defect manifests itself as staining of the exposed buried-oxide field surfaces, which is bad enough in itself. Unfortunately, it is always accompanied by deterioration of the quality of replicated reference features, which often isn't apparent until quite late in the process cycle. The occurrence of the staining problem has always appeared unrelated to the process conditions. However, very recently we have discovered that a major factor is the length of time that the KOH solution is retained in the quartz reflux system. No adverse effects are observed for up to approximately two weeks, regardless of the usage of the solution. After that time elapses, the staining symptoms and the accompanying deterioration of the reference features becomes very evident. We have simply done an end-run around the issue by mixing a fresh KOH solution at least once a week. Since we started doing this, we have observed an unexpected benefit in a higher etch-survival rate of sub 30 nm features and also an indication of less CD-roughness.

■ Throughout this report, the importance of reducing the residual line-width roughness of SCCDRM features replicated in (110) silicon substrates has been stressed. We now believe that a major contributor to residual line-width roughness is the line-edge roughness of the corresponding hard-mask features. Therefore we have arranged for several chips to have extensive AFM metrology performed on their oxide hard-mask features. At the 50 nm average-CD level, the oxide-feature line-widths certainly exhibit CD variations amounting up to 20 nm more. It is highly likely that this hard-mask roughness is at least partially transferred to the replicated silicon reference features, the extent to which can be ascertained after KOH etching. If transference is found to occur, at least some effort will be diverted into hard-mask-feature CD-roughness control.

■ A new project thrust is collaboration with the Optical Physics Group at NIST responds to industry expressions of interest in acquiring SCCDRM-based standards to facilitate the development of, and monitor the performance of OCD tools. This new CD-metrology medium is increasingly popular in the semiconductor- and mask-manufacturing communities. Suitable gratings have been co-fabricated on the same chips as the isolated-line reference features that are reported elsewhere in this document. The results of our continuing collaboration have been reported in two papers listed in the last section here, and a third paper has been accepted for an industry conference in August, 2008.

■ We commented above on the need to develop specialized image-processing software to rapidly extract CD-roughness profiles and average CD. A start on this mission has been made by comparing SEM- and HRTEM-CD measurements extracted from a wide selection of SCCDRM test-structures having feature line-widths ranging from 40 nm to 240 nm. Details are provided in a 2008 publication among those listed herein.

■ As mentioned above we have been investigating SAXS as an alternative primary metrology for calibrating the line-widths of SCCDRM features. In the next paragraph, we summarize the scope of our recent accomplishments with the University of Texas in Austin. During precursory research, we had earlier transferred our SCCDRM-fabrication process to facilitate a study of electron transport in silicide materials. Subsequently, UT-Austin had applied basically the same process to the fabrication of gratings, similar to that which has been shown in Figure 3 herein, for nano-materials research. We then asked for some of the gratings to be forwarded for SAXS-based CD metrology at the synchrotron at Argonne National Laboratory by staff of the NIST Polymers Division. Preliminary beamline exposures were very encouraging. Based on the position of over 20 diffraction peaks that were observed, the pitch of the grating was determined to be 179.8 nm, a value very close to the specified value of 180 nm. The X-ray data could not be modeled adequately with a grating model characterized by uniform lines having 0 ° sidewall angles. However, adding trapezoidal bottoms to the vertical-sidewall trenches improved the fitting to some extent. This requirement is entirely consistent with known geometrical features of trenches etched in SCCDRM gratings replicated on bulk material. In addition, asymmetrical sidewall angles and variations in linewidth, seemed to be needed to improve the fit of the observed diffraction patterns to those modeled. These observations are entirely consistent with known characteristics of gratings patterned by EB lithography in a mode susceptible to prox-

imity effects and combined with slight off-axis sawing of the wafers from the ingot. Thus nano-scale geometrical anomalies of the properties of the gratings revealed by the SAXS metrology were credibly explained by orientation and processing issues that might not have been detected by any other means. In the end, SAXS metrology revealed that, with a simple rectangular line cross-section model, the height of the grating features was 490 ± 10 nm and their line-width was 26.5 nm. Both values were very close to those extracted from SEM images.

■ The project published a comprehensive full-length report on the fabrication and calibration of SCCDRM Reference Materials entitled RM 8111: Development of Prototype Linewidth Standard in the NIST Journal of Scientific Research. Several other papers on special aspects of the fabrication and calibration, such as test-chip design, AFM metrology, and HRTEM imaging, were presented at the SPIE Spring Symposium of February, 2007, and the IEEE International Conference on Microelectronic Test Structures in March, 2009. A paper on the subject of etch-process optimization for uncertainty management was presented at the International Electron, Ion, and Photon Beam Technology and Nanofabrication Conference in June, 2006. A paper on the comparison of SEM-CD measurements and traceable-AFM CD measurements was published in an IEEE Transactions journal in January, 2008. An important first description of fabrication of SCCDRMs on 200 mm bulk wafers which was performed in collaboration with the Scottish Microelectronics Centre was presented at the Frontiers of Characterization and Metrology for Nanoelectronics in March 2007.

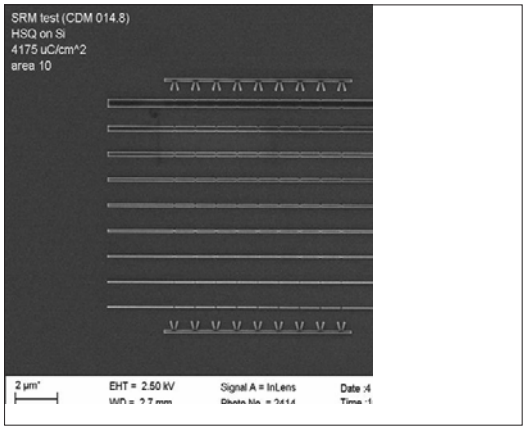


Figure 4. Electron-beam-patterned SCCDRM hard mask, utilizing localization notches to reduce line-width non-uniformity. The smallest features have a pre-etch width of 21 nm.

■ As a part of the on-going uncertainty reduction program, the project is developing a new masking process that utilizes localization notches to reduce the position uncertainty of the region of interest in CD reference features, thereby reducing the total linewidth non-uniformity. The process utilizes e-beam lithography, is compatible with monolithic implementation, and targets the extension of the SCCDRM calibration curve down to 20 nm. An electron micrograph of the new SCCDRM hard mask is shown in Fig. 4. The masking process has been implemented on 100 mm bulk wafers, and is extensible to 200 mm wafers in both bulk silicon and SOI.

Collaborations

The project has been actively collaborating with the Microelectronics Research Center of the University of Texas at Austin (http://www.mrc.utexas.edu/amrc/publications.html), and the Institute for Integrated Micro and Nano Systems at the University of Edinburgh in Scotland (http://www.see.ed.ac.uk/IMNS). These organizations operate the advanced wafer processing tools that we use to address the customer needs referenced in the sections above. Both institutions have highly skilled staff with both of which we have published recently. In the case of the University of Texas, our collaboration began with using the SCCDRM process to fabricate single-crystal test structures to facilitate a study of electron transport in nickel-silicide features. Since then, our collaboration has expanded into the MEMS arena and a ground-breaking study of the impact of nano-structure on the material properties of silicon, principally elasticity and related characteristics. Our interaction with the University of Edinburgh has recently focused on the fabrication of copper ECD test structures that take advantage of the properties of our SCCDRM technology. In addition, we have jointly published on two types of overlay standard, one of which uses a variant of the SCCDRM process.

We are interacting with the CAD and reticle staff the ISMI Subsidiary of SEMATECH, (http://ismi.sematech.org/) who have invited us to share space on a new reticle for their SVGL 193 nm Step-and-Scan lithography tool to fabricate an advanced generation of SCCDRMs for distribution to the member companies, as well as for possible calibration and distribution from NIST as SRMs.

We also interact regularly and closely with NIST's Physics, Materials Engineering and Information Technology Laboratories (http://www.mel.nist.gov/ and http://www.itl.nist.gov/) with whom we shared an intramural ATP program award to reduce the certified CDs and uncertainties of SCCDRMs

through fabrication refinements. We are collaborating with staff of the nanofabrication facility at NIST's Center for Nanoscale Science and Technology of our uncertainty-reduction program, and in developing a monolithic implementation of the SCCDRM process.

Standards Committee Participation

Standards for Scatterometry Task Force (Michael W. Cresswell).

SEMI International Standards Micro-lithography Committee, member (Richard A. Allen and Michael W. Cresswell).

Recent Publications

B. J. Shulver, R. A. Allen, A. J. Walton, M. W. Cresswell, J. M. Stevenson, S. Smith, A. S. Bunting, C. Dunare, A. Gundlach, L. I. Haworth, A. W. Ross, and A. J. Snell, IEEE International Conference on Microlectronic Test Structures, March 19-22, 2007, Tokyo, Japan, page 165.

E. Kenyon, M. W. Cresswell, H. Patrick, T. A. Germer, *"Modeling the Effect of Finite Size Gratings on Scatterometry Measurements,"* Proceedings of SPIE Advanced Lithography, SPIE Advanced Lithography, February 24-29, 2008, San Jose, California, 8 pp. (25-FEB-2008).

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Wafer-Level and Overlay Metrology

Goals

Provide technological leadership to semiconductor and equipment manufacturers, and other government agencies by developing and evaluating the methods, tools, and artifacts needed to apply optical techniques to the metrology needs of semiconductor microlithography. One specific goal is to provide the customer with the techniques and standards needed to make traceable dimensional measurements on wafers at the customer's facility. The industry focus areas of this project are primarily optical based methods used in overlay metrology and optical, wafer level critical-dimension (CD) metrology.

Customer Needs

Tighter tolerances on CD measurements in wafer production place increasing demands on linewidth accuracy and on overlay tolerances. A recent industry focus on high-throughput, higher-resolution metrology tools, which enable more dense sampling strategies has led to a comprehensive program at NIST to both support and advance the optical techniques needed to make these high throughput overlay and photomask/wafer critical dimension measurements (see Fig. 1).

Technical Strategy

The main technical thrust areas are overlay calibration techniques and standards, new advanced wafer level target designs, and research into new methods for measuring overlay. The strategic components of the project follow.

1. The development of calibration methods and calibrated overlay structures is one of the primary goals of the project. The technical strategy for calibrated overlay metrology is divided into two components: (a) instrumentation development and development of advanced overlay metrology calibration techniques, and (b) the design and calibration of test patterns and standard artifacts. NIST has developed an overlay metrology tool that has undergone extensive development of the mechanical hardware, optical components, and measurement algorithms to obtain uncertainties comparable to or better than the best industry overlay tools. This optical metrology tool is now used to calibrate standards and to support the development of improved measurement algorithms and alignment techniques. Since pattern placement and overlay of the various lithographic levels is monitored with a series of targets, each in a different plane, particular concern is placed on ensuring accurate optical measurements through a large depth of focus. Any misalignment in the overlay metrology system will translate into an overlay offset error, referred to as tool induced shift (TIS). Additionally, there are residual errors caused by asymmetries in the targets known as wafer induced shift (WIS). A set of standard

Technical Contacts:
R. Silver
R. Allen

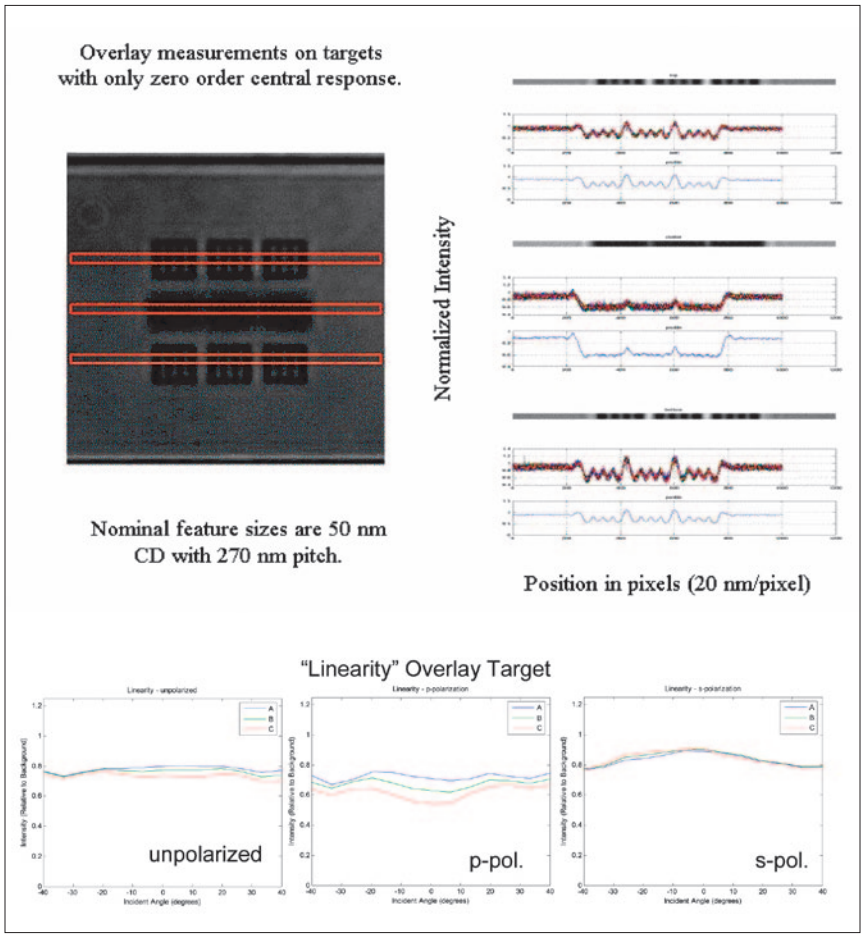

Figure 1. Improved two-dimensional overlay measurement techniques and standards are needed for measuring and controlling overlay capabilities of steppers and separating out the contributions from the photomask. Overlay is listed in multiple sections of Tables Met 3a and b of the 2007 ITRS as a difficult challenge for both >32 nm and <32 nm processes. Overlay measurements have not kept pace with resolution improvements and in-die correlation requirements and will be inadequate for ground rules less than 45 nm. In fact, Table Met 3a shows that no known solutions for overlay output metrology exist beyond the 65 nm node. As shown in Table Met 3b, the problems are more acute for long term CD metrology where the industry is currently encountering metrology problems without known manufacturing solutions.

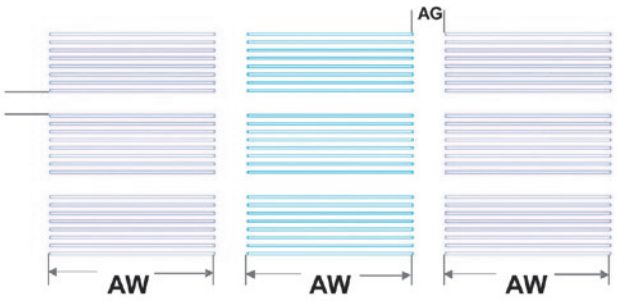

Figure 2 (a)

- Two sets of targets:
  1) This shows equal lines and spaces.
  2) A similar set of targets but with different linewidths for each group of 8 lines. The linewidths span typical process variation windows.
- AW = 2.5 um and 5.0 um
- AG = 1.0 um
- 5 different pitches and 3 offset values: 0, +/-10 nm

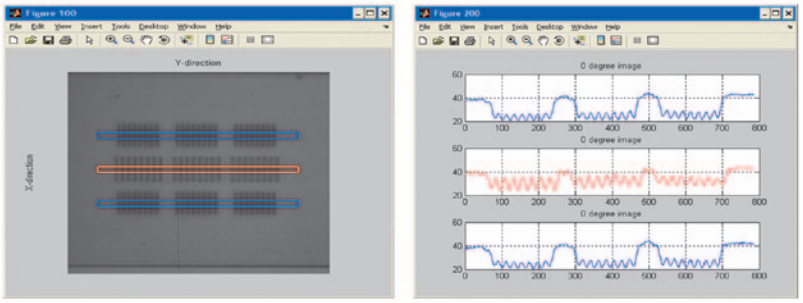

Figure 2 (b)
LITO
90nm 1:3

Figure 2. A schematic of the target designs is shown in (a). This is one example of several variations of this design. The lower part of the figure shows an image and a set of profiles for a target which reflects higher-order optical content.

artifacts and alignment procedures, developed at NIST and published, has been implemented to assist in aligning overlay measurement systems and minimizing TIS. After alignment, the tool must then be calibrated with standard artifacts to yield accurate overlay measurements. The NIST metrology system used for this is an optical reflection mode instrument, typically operated in a bright field mode. The hardware includes high-resolution image capture with a full field CCD data acquisition system, which has been fully characterized and calibrated. This instrument has been used for detailed analysis of CCD array performance and characterization and several CCD acquisition systems have been evaluated. Many of the techniques developed in the advanced optical imaging section below have been implemented on this tool as well, such as structured illumination and system characterization to enable improved calibrations.

Standard overlay artifacts have been fabricated and calibrated in 200 mm and 300 mm wafers that are now available as SRM 5001. These overlay artifacts are for the calibration of industrial overlay metrology tools, although they have also been used for the calibration of atomic force microscope (AFM) or SEM reference metrology systems. The artifacts have been fabricated in single crystal silicon and provide an array of etched silicon three-dimensional targets. These wafers additionally have an extensive set of characterization targets and research structures developed in close collaboration with SEMATECH and leading semiconductor manufacturers, for an example, Fig. 2. We have also developed a series of new overlay targets and linewidth targets intended to enable the measurement of overlay and linewidth with device-size features. One variation of these targets allows in-chip structures to be placed throughout the active area of a die. These results have been published and collaborative work is progressing to develop the commercial applications to measure overlay using device-size features in targets optimized to be the smallest overall dimension. There is a second flavor of in-chip targets, as shown in Fig. 3, that are arrayed targets composed of device-sized features

DELIVERABLES:

- Install wavelength-scanning monochromator for the visible light scatterfield optical microscope. Demonstrate multi-wavelength measurement capabilities using the full scanning illumination mode. 3Q 2009
- Develop scanned aperture capability on the overlay microscope. Install two-dimensional aperture

scanning capability with computer positioning control and auto data acquisition. 2Q 2009

- Evaluate second generation of overlay wafer standards. Work with industry and consult Sematech for new design considerations and build a consensus for a second overlay standard. 4Q 2009
- Develop methods jointly with SEMATECH for dense structure overlay that do not rely on conventional edge based patterns. Evaluate target designs using arrayed overlay targets. Q2 2009

Optical modeling is an essential tool for enabling improved optical overlay measurements. Modeling the effects of relevant feature properties and optical instrument characteristics using existing and new software tools, can yield significant improvements in measurement accuracy, as in Fig. 4, NIST has a world class effort in optical modeling that includes the comprehensive comparison of two rigorous coupled wave guide scattering models, a finite difference time domain-based model and a Maxwell integral equation solver. Two of the models are developed in house and form the basis of our critical dimension and overlay simulation tools.

DELIVERABLES:

- Compare zero order and blank silicon reflectivity curves for 3 different models. Use results to develop improved accuracy modes and evaluate implementation of three-dimensional scattering model. 4Q 2009
- Apply scatterfield techniques to defect inspection. Use three-dimensional modeling techniques to accurately simulate patterned defect inspection on an optical microscope platform. 3Q 2009

2. The second component of this project is the development of new, advanced high-resolution optical metrology techniques. A new class of optical measurement techniques known as scatterfield microscopy is being developed at NIST. This optical methodology has been used to demonstrate line width and overlay metrology with targets composed of features smaller than 30 nm critical dimensions. This new approach utilizes structured illumination in parallel with engineered target designs. The technique is well suited for high-resolution microscopy of metrology targets as encountered in semiconductor manufacturing.

A key element of this approach is to develop optical methods that can be suitably applied to device-sized features and advance the extensibility of high throughput optical metrology methods. Current metrology requirements are demanding

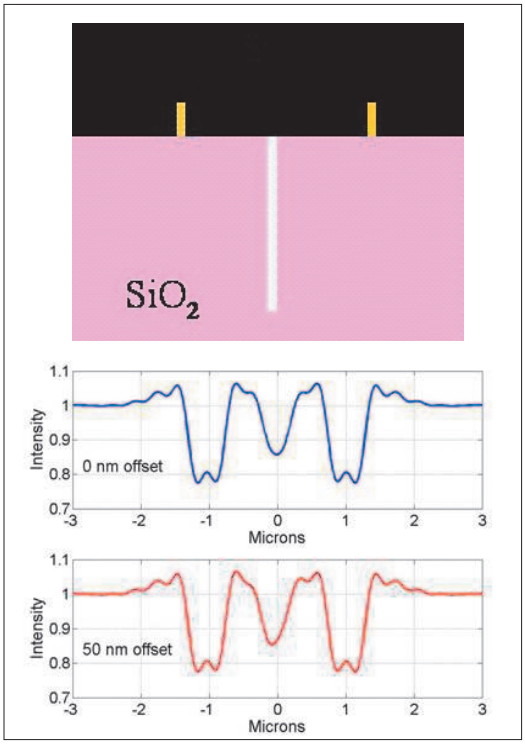

Figure 3. New overlay targets, which occupy less than 2 μm x 2 μm in total space. This is designed to be an in chip target.

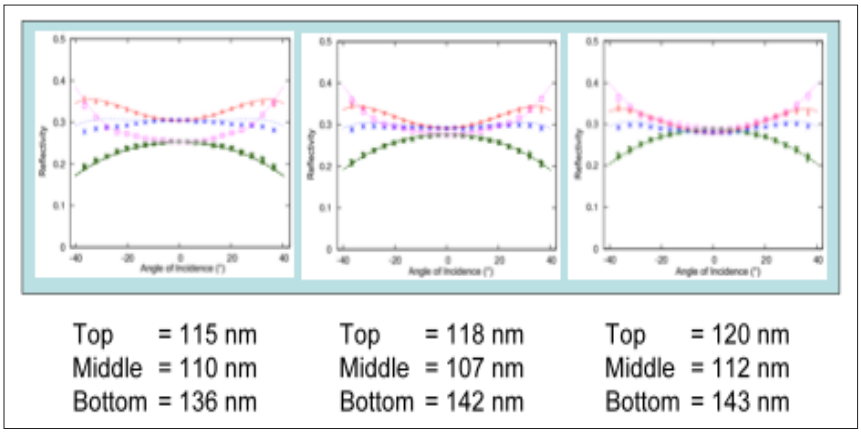

Figure 4. Quantitative parametric modeling results demonstrate consistent agreement on the nanometer scale with AFM reference metrology. More comprehensive data published recently show that nanometer scale sensitivity measurements can be achieved using angle resolved microscopy for nominally 100 nm sized lines and pitches of 300 nm.

higher throughput, non-destructive measurements with nanometer sensitivity to enable tighter process control as well as closed-loop integrated process control. The current class of scatterometry and scatterfield optical techniques are now viewed as solutions to these significant metrology challenges. As a part of this project, we have constructed a new optical tool specifically intended to make this type of scatterfield mea-

surement with structured illumination that controls the frequency content of the illumination fields and of the scattered fields. Fig. 5 shows an example controlling the frequency content of a sub-resolution overlay target. This effort includes comprehensive optics modeling as well as a new 193 nm optical microscope designed and fabricated in-house. The optical design work includes a thorough examination of illumination effects and accurate methods to prepare optical illumination fields.

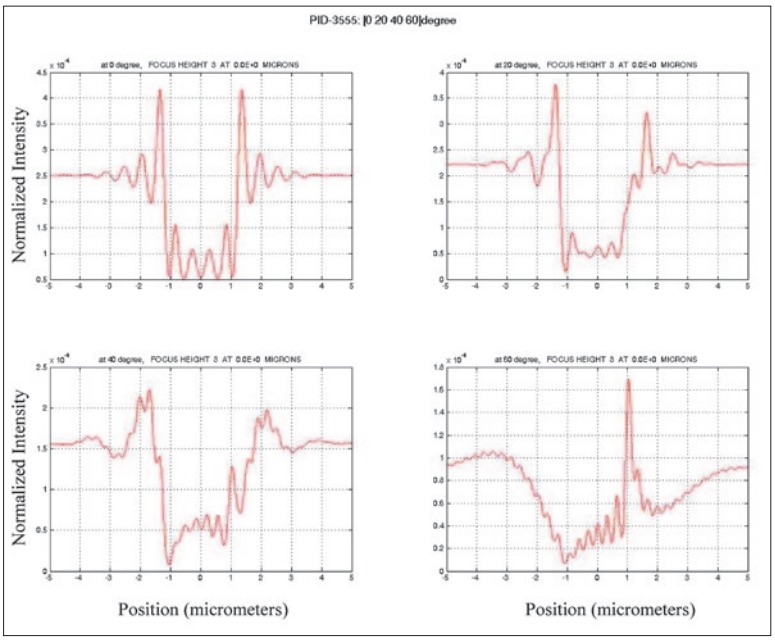

Figure 5. The different panels show the image as a function of illumination angle. The vertical axes are normalized intensity and the horizontal axes are lateral position in micrometers. At the high illumination angles, the higher order diffraction orders are rocked into the collection optics. A dipole or alternative illumination can yield symmetric profiles or overlay which otherwise would show zero order response.

We have constructed a 193 nm wavelength optical instrument with a flexible architecture for overlay and CD measurements on a high throughput capable platform. The new design creates a large conjugate back focal plane where a range of scanning and illumination control techniques can be applied. The optics have been custom designed and manufactured to NIST specifications with the appropriate 193 nm coatings. The new laser system and optics are housed in a clean room environment and using a new embedded structural design with superb vibration and temperature control, the goal is ultimate performance in a state of the art optical system.

DELIVERABLES:

- Refine alignment and assembly procedures for the 193 nm optical tool and improve alignment from optical design work based on optical layout using Zemax. Fully characterize the illumination field of the microscope at 193 nm and publish results. 3Q 2009
- Implement modeling techniques on the 193 nm optical data and do detailed theory to experiment comparisons. 4Q 2009
- Operate the 450 nm optical tool with the full optical normalization and correction algorithms. Use parametric modeling and demonstrate quantitative agreement. 4Q 2008
- Model new overlay supertarget designs and provide SEMATECH and industry with results. 1Q 2009

3. A final element of this project is development of hybrid electrical-optical test structures to provide a validation between in-line optical metrology and actual device performance. These test structures would not displace in-line metrology, but rather will compliment it; providing a tool to evaluate in-line techniques.

DELIVERABLES:

- Complete initial evaluation of test structure using electrical and AFM metrology. 3Q 2009
- Investigate intercomparison of electrical metrology with optical metrology. 4Q 2009

Accomplishments

■ Served as Technical Chair for the 2009 International Conference on Microelectronic Test Structures. This conference, in its 23rd year, is the premier conference for electrical test structures for semiconductor applications.

■ 193 nm optical tool assembled and demonstrated first light. Following design and and fabrication of all major mechanical systems and custom optical train components for the new 193 nm optical metrology tool, the optical train has now been assembled, aligned and imaging was demonstrated.

■ A manuscript entitled "Through Focus scanning optical microscope imaging method for nanoscale dimensional analysis" accepted and appeared in the leading journal Optics Letters, 2008.

■ Book chapter authored on EUV Metrology. This is a new book published by McGraw Hill and is expected to be the benchmark publication for semiconductor manufacturing challenges using next generation EUV lithography.

■ There have been several external inquiries and invitations to present the new method for nesting multiple measurements. This method can improve reference metrology and independent measurements through the use of Bayesian statistical methods that combine measurements into a monolithic measurement that results in a lower uncertainty than the individual measurements.

■ Patent Applied for on "Super resolution overlay targets". Joint NIST/SEMATECH patent has been formally applied for on the new super-resolution overlay target, which has the potential to change the target designs and methodology widely used by the industry.

■ 2008 SPIE Advanced Lithography submission elevated to the plenary presentation for the 2009 Metrology Inspection and Process Control conference. The topic of Multi-technique Nested Uncertainties is now being recognized as an essential new needed direction for semiconductor manufacturing.

■ A new level of quantitative agreement has been achieved between rigorous modeling and experimental data. Published results demonstrating quantitative agreement for scatterfield measurements of densely arrayed 100 nm sized lines which vary in 1 nm increments. This new level of agreement was achieved using parametric modeling methods and uncertainty analysis at the nanometer scale. This was accomplished by accurate optical characterization/normalization without tunable parameters.

■ Comprehensive development and comparison of NIST electromagnetic scattering models and industry models completed. Researchers in the optical scatterfield competence have both developed and compared model-based simulation results with excellent agreement. Two industrial scattering models as well as the NIST-developed integral Maxwell equation solver and the NIST-developed Rigorous Coupled Wave Analysis (RCWA) model were all compared.

■ Engineered dipole illumination to control optical image content for overlay metrology was demonstrated in image-based measurements. Leading metrology tool makers are now implementing this approach.

■ The through-focus focus-metric technique was advanced using a new differential imaging methodology that demonstrated nanometer sensitivity to features in silicon. The technique of sampling scattered fields through focus for CD measurement and optical system alignment has been implemented at other international metrology laboratories. Applications in overlay and CD metrology are being investigated.

■ The overlay microscope has been converted to scatterfield scanning design. The existing optical overlay instrument has been enhanced with illumination control for improved data acquisition and tool alignment. Techniques for alignment and imaging implemented.

■ The 450 nm illumination scatterfield microscope has been outfitted with a spectroscopic illumination and scanning capability. This is a new scatterfield application developed at NIST specifically for the purpose of using engineered illumination and wavelength scanning. The open architecture microscope allows sophisticated control of the illumination and collection paths.

■ SEMATECH Tech Transfer document highlighted work from NIST optical research staff. A recent document "Summary of 2006 NIST/SEMATECH Studies of Next Generation Overlay Metrology" authored by SEMATECH highlighted a number of recent advances by the Scatterfield competence project. The report details collaborations between NIST, SEMATECH and the semiconductor industry.

■ NIST Competence Program staff has met with several leading optical metrology tool manufacturers regarding recent advances in scatterfield microscopy. The companies include among others KLA-Tencor, Nanometrics, Soluris, Nova and Applied Materials. Metrology instrument makers are now adopting and implementing various elements of the scatterfield optical design. Scatterfield researchers are now funded to

develop nanomanufacturing applications for fuel cell production.

■ SEMATECH contract completed for overlay metrology applications of scatterfield microscopy and scatterometry for overlay. External funding from SEMATECH member companies was used to research scatterfield and scatterometry applications for high resolution arrayed overlay targets and measurements.

■ Report submitted to SEMATECH on defect metrology applications of scatterfield microscopy. Scatterfield competence researchers completed the comprehensive simulations to investigate applications of Scatterfield microscopy to patterned defect inspection. SEMATECH subsequently funded a second round of contracted research.

Collaborations

SEMATECH, IBM, Intel, KLA-Tencor, Nanometrics, Applied Materials, Motorola, AMD, and several other leading manufacturers and tool vendors.

University of Edinburgh.

Publications

R.M. Silver, N. Zhang, B. Barnes, H. Zhou N. Heckert R. Dixson, T. Germer, and B. Bunday, *"Improving Optical Measurement Accuracy using Multi Technique Nested Uncertainties"*, SPIE Vol. 7272, p. 1, 2009.

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B. J. R. Shulver, R. A. Allen, A. J. Walton, M. W. Cresswell, J. T. M. Stevenson, S. Smith, A. S. Bunting, C. Dunare, A. M. Gundlach, L. I. Haworth, A. W. S. Ross, A. J. Snell, *"Array Based Test Structure for Optical-Electrical Overlay Calibration,"* Microelectronic Test Structures, 2007, ICMTS'07, IEEE International Conference, pp. 165-170 (March 2007).

R. M. Silver R. Attota, B. Barnes, and H. Zhou, *"Theoretical Evaluation of Scatterometry for Overlay Applications,"* SEMATECH Tech Transfer Doc, Feb. (2007).

R. M. Silver, T. Germer, R. Attota, B. Barnes, B. Bunday, J. Allgair, E. Marx, and J. Jun, *"Fundamental Limits Optical Critical Dimension Metrology: A Simulation Study,"* SPIE Proc. Feb. Vol. 6518 (2007).

Front-End Processing Metrology Program

The dimensions of the active transistor areas are approaching the spacing between dopant atoms, the stochastic regime, complicating both modeling and doping gradient measurements. Thin dielectric and conducting films are approaching monolayer thicknesses.

As device dimensions continue to shrink, junctions and critical film thicknesses approach the realm of several atoms thick, challenging gradient, thickness and wafer flatness and roughness metrology as well as electrical and reliability characteristics. The current gate stacks, poly silicon over SiO_2 and SiON dielectrics, are being replaced by high-κ metal gate stacks. The overall task is to provide starting wafer dimensional and defect metrology, suitable metrology and reference materials for their dielectrics and junctions, including electrical characterization, gradient, thickness and roughness metrology, and overall reliability metrology.

Wafer and Chuck Flatness Metrology

Goals

Develop measurement support for 300 mm diameter silicon wafers used in lithography applications. This project provides measurement and technology infrastructure to support the measurement of wafer thickness variation of 300 mm silicon wafers, and surface flatness of chucked wafers. The same system can be used to address thickness metrology needs for the emerging 450 mm silicon wafers.

Customer Needs

With the evolution of exposure tools for optical lithography towards larger numerical apertures, the semiconductor industry expects continued demand for improved wafer flatness at the exposure site. The allowable site flatness, SFQR (26 mm x 8 mm) for 300 mm wafers is expected to be less than 45 nm by 2010 and it may be as low as 25 nm by 2015 according to the International Technology Roadmap for Semiconductors (ITRS 2007). A transition to wafers with 450 mm diameter is expected to begin in 2012. The projected SFQR for 300 mm silicon wafers and future 450 mm presents a challenge for both wafer polishing and metrology tools, which must be capable of meeting the specifications. We are addressing the need for standard 300 mm wafers with calibrated thickness variation with the Improved Infrared Interferometer (IR3) at NIST. The interferometer is used for independent, traceable wafer thickness calibrations, which enable manufacturers of wafers and wafer metrology instruments to certify the performance of their metrology instruments. Silicon wafers with 450 mm diameter can be measured with the same system by combining several 300 mm sub-aperture measurements. In addition, thickness variation measurements of silicon wafers can be combined with models of wafer/chuck interactions to determine the flatness of low surface area wafer vacuum chucks, which is difficult to measure directly. The surface flatness of chucked wafers can be measured using NIST's "eXtremely accurate CALIBration InterferometeR" (XCALIBIR).

Technical Strategy

1. The Improved Infrared Interferometer (IR3) was developed at NIST for the characterization of the thickness variation of silicon wafers with diameters up to 300 mm. The IR3 interferometer is an infrared phase-shifting interferometer, operating at a wavelength of 1550 nm which measures the thickness of low-doped silicon wafers up to 300 mm diameter in a single measurement (see Fig. 1 and Fig. 2). The interferometer may be used in several configurations with collimated and spherical test wave-fronts. The collimated wave-front mode is the current

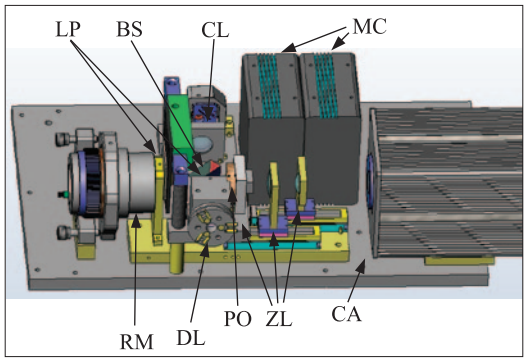

Figure 1. Solid model of NIST's improved infrared interferometer (IR3). The main components of the interferometer are indicated: collimator lens (CL), polarizing beam splitter (BS), λ /4-plates (LP), reference mirror for the Twyman-Green mode (RM), diverger lens (DL), polarizer (PO), zoom lens (ZL), motion controllers for the zoom lens (MC), and camera (CA). The size of the base plate is approximately 20 cm × 30 cm.

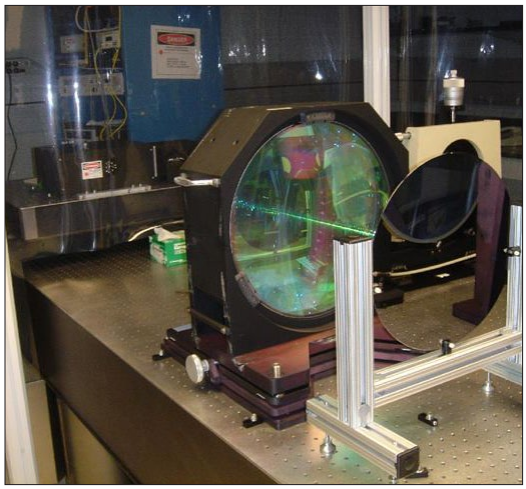

Figure 2. Test arm of the IR3 interferometer. shown are the collimator lens and the beam expander together with a 300 mm silicon wafer. The insensitivity of the measurement to vibration permits the use of a simple wafer mount.

Technical Contacts:
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Q. Wang
J. Soons

"NIST continues to support the effort to bring quantitative standards and measurement practices to the semiconductor wafer metrology area. Their support in the area of wafer thickness metrology has led to unprecedented levels of thickness correction on industry standard 300 mm Si wafers, when combined with deterministic finishing technologies such as MRF. The collaboration with NIST has been a significant and crucial component to the success of this effort."

Paul Dumas and Marc Tricard
QED Technologies –
A subsidiary of Cabot
Microelectronics Corp,
Rochester, NY

focus of the project. In this method, the planar infrared wave-front is normally incident on the wafer. A portion of the beam is reflected from the front wafer surface, while the rest passes through the wafer and reflects from the rear surface. The interference of these two wave-fronts produces fringes and, by wavelength phase shifting, allows calculation of the wafer thickness variation.

DELIVERABLES:

- Develop methods for the thickness calibration of 450 mm silicon wafers. 4Q 2009
- Implement metrology methods for very thin wafers with thickness < 500 µm 4Q2009
- Implement a method for the separation of wafer thickness variation and wafer refractive index variation. 4Q 2009
- Wafer calibrations will be made for customers upon request in future years.

2. Measurements of the flatness of chucked wafers are made with XCALIBIR, a general purpose, 300 mm aperture phase measuring interferometer operating with visible light at 633 nm. The interferometer is housed in a clean room, which eliminates dust particles between chuck and wafer. The results are used to evaluate the influence of wafer-chuck interactions on the chucked wafer flatness.

Accomplishments

■ IR3 has undergone a major upgrade that enables us to address the metrology needs for 300 mm diameter wafers. A collimator lens has been installed that can illuminate the entire surface of a 300 mm wafer and allows us to make a measurement of the wafer's thickness variation in a single measurement. The imaging system of the interferometer now can measure wafers with larger slopes, and the spatial resolution of the detector was doubled to 2 pixels/mm. Further improvements will be aimed at reducing the noise level and at improving the measurement uncertainty. In addition, a new laser with wide tuning range will make it possible to measure very thin wafers. The optical components in the IR3 interferometer were improved to reduce the measurement noise. Wavelength phase-shifting has been implemented and a TTV map repeatability of 5 nm peak to valley has been achieved for 300 mm wafers. The IR3 interferometer is now housed in a clean room, which enables us to make calibration measurements of wafers supplied by industry customers.

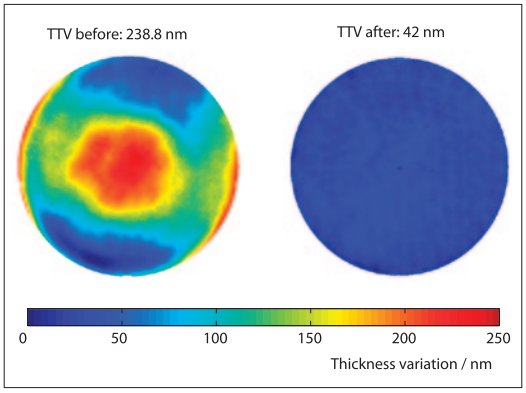

Figure 3. Wafer thickness variation of a 300 mm silicon wafer before and after sub-aperture polishing. The total thickness variation was reduced from 238 nm to 42 nm over a 292 mm aperture (4 mm edge exclusion).

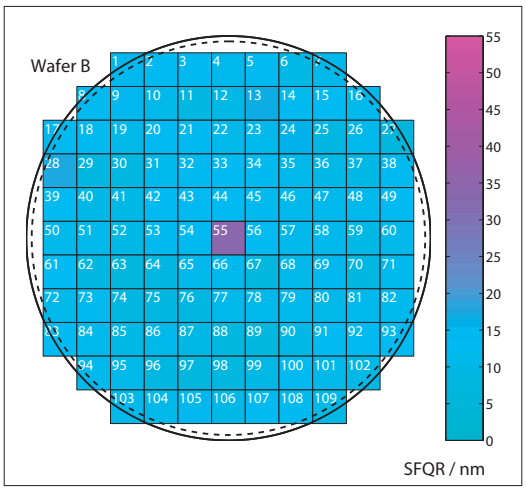

Figure 4. SFQR of the wafer shown in Fig. 3 after sub-aperture finishing for 25 mm x 25 mm sites with the same edge exclusion (4 mm) as in Fig. 3.

■ The flatness of 200 mm and 300 mm diameter wafers on pin chucks was explored using the XCALIBIR interferometer in a collaboration with Wavefront Sciences Inc., Albuquerque, NM.

■ IR3 was used to develop a sub-aperture magneto-rheological polishing process for the finishing of 300 mm wafers with ultra-low thickness variation in collaboration with QED Technologies. Figure 3 shows that a total thickness variation (TTV) of about 40 nm could be achieved. The Square focal plane range square focal plane range (SFQR) resulting from the thickness variation (assuming an ideal chuck) is shown in Fig. 4. These results demonstrate that a suitable sub-aperture finishing process can

achieve the exposure site flatness expected by the ITRS for 2015.

Collaborations

During the course of this project, we have interacted with several companies on problems relating to wafer flatness metrology and chucked wafer flatness.

WaveFront Sciences: Flatness measurements of free form and chucked wafers for the validation of a metrology tool developed by WaveFront Sciences.

MEMC Electronic Materials: Wafer thickness standard development.

Siltronic: Wafer thickness standard development.

Intel: Development of very thin silicon thickness standards.

QED Technologies: Development of ultra-flat 300 mm silicon wafers.

Lumetrics: Evaluation of Lumetrics thickness gauging technology for wafer thickness metrology.

Publications

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Q. Wang, U. Griesmann, and R. S. Polvani, *"Interferometric Thickness Calibration of 300 mm Silicon Wafers,"* Proceedings of the ASPE Topical Meeting on Precision Interferometric Metrology, Middletown, CT (2005).

U. Griesmann, Q. Wang, and T. D. Raymond, *"Optical Flatness Metrology for 300 mm Silicon Wafers,"* AIP Proceedings of the 2005 Conference on Characterization and Metrology for ULSI Technology, University of Texas, Richardson, TX, USA (2005).

D. R. Neal, P. Pulaski, T. D. Raymond, D. A. Neal, Q. Wang, and U. Griesmann, *"Testing highly aberrated large optics with a Shack-Hartmann wavefront sensor,"* Proc. SPIE 5162, 129-138 (2003).

T. L. Schmitz, A. Davies, C. J. Evans, and R. E. Parks, *"Silicon wafer thickness variation measurements using the National Institute of Standards and Technology infrared interferometer,"* Opt. Eng. 42, 2281-90 (2003).

Modeling and Measurements for Wafer Surface Inspection

Technical Contacts:
T. A. Germer

"The work done by SEMI's Auromatic Surface Inspection Task Force on particle scanner calibration would have been impossible without the support supplied by Dr. Thom Germer of NIST. He used his scatter modeling software and knowledge of the situation to make possible a rewrite of SEMI M53 that dramatically improved it capabilities."

John Stover

Co-Leader of the SEMI ASI Task Force

The Scatterworks, Inc.

Goals

Our goals are: (1) to provide industry with models, measurements, and standards for particles and other defects in order to improve the inspection of wafer surfaces; (2) to develop facilities to accurately measure particle size and to deposit monosize particles on calibration artifacts to reduce the uncertainty in the sizes of particles used by the semiconductor industry to calibrate scanning surface inspection systems (SSIS); and (3) investigate theoretically and experimentally the behavior of light scattering from particles, defects, and roughness on wafer surfaces.

Customer Needs

The Semiconductor Industry Association's (SIA) International Technology Roadmap for Semiconductors identifies the detection and characterization of defects and particles on wafers to be a potentially show-stopping barrier to device miniaturization. The roadmap specifies polystyrene latex (PSL) equivalent diameter particles that must be detectable on bare silicon, nonmetallic films, metallic films, and wafer backsides each year. Currently, no solutions to this inspection problem currently exist for particles on bare silicon, on non-metallic films, and on wafer backsides, while it is anticipated that no acceptable solutions will exist for metallic films in 2010. While the detection sensitivity for defects must be increased, the ability to characterize defects in terms of size, shape, composition, etc., is critical for yield-learning. Defects must be characterized independent of defect location and topology.

With the need to detect smaller defects, the costs of inspecting wafers are skyrocketing. In order for new advances to be implemented in production environments, improvements in sensitivity must be achieved without suffering a tradeoff in throughput and must be cost-effective. The drive towards in-situ sensors for production tools requires techniques which can be effectively miniaturized.

In order that wafer manufacturers and device manufacturers have a common basis for comparing specifications of particle contamination, improved standards for particles are needed. A recent comparison of the measurements of calibration wafers by 13 different Scanning Surface Inspection System (SSIS) indicated unacceptably large deviation between the SSIS results and the actual particle sizes. This study involved six particle sizes ranging from 88 nm to 290 nm and included the NIST SRM 1963 and two other particles sizes measured by NIST. For the two smallest particle sizes, 88 nm and 100.7 nm, the scanners systematically underestimated the size by about 8 %. The SIA roadmap specifies the need for accurate calibration particles to size critical semiconductor components scaling to 32 nm or smaller by as early as 2008.

Technical Strategy

There are two major strategies for improving the performance of scanning surface inspection systems. One strategy is to develop a fundamental understanding of optical scattering at surfaces so that tool manufacturers can optimize the performance of their instrumentation, in terms of defect detection limits and discrimination capabilities, to characterize the response of instrumentation to different types of defects, and to develop and calibrate particles of well-defined size and material. Recent work by this group has demonstrated that the polarization of light scattered by particulate contaminants, subsurface defects, and microroughness has a unique signature that can be using to identify the source of scatter. In particular, it was found that small amounts of roughness do not depolarize scattered light. This finding has enabled the development of instrumentation which can collect light over most of the scattering hemisphere, while being blind to microroughness. That instrumentation, for which a patent has been awarded, should result in a factor of two improvement in minimum detectable defect size, especially on rougher surfaces.

A second strategy is to provide leadership in the development of low uncertainty calibration particles for use in calibrating surface scanners. A major focus has been development of the differential mobility analysis (DMA) method for accurately sizing monosize polystyrene spheres. This work together with a SSIS round robin has provided evidence that current SSIS measurements have an unacceptably large uncertainty for particle sizes in the 90 nm to 100 nm size

range. The technical focus of our future work will be applying DMA for accurately sizing calibration particle sizes as small as 30 nm, developing methods for generating other types of monosize particles, and developing laser surface scattering methods for quantitative particle sizing.

Specific project elements are defined below:

1. Polarized Light Scattering Measurements – The Goniometric Optical Scatter Instrument (GOSI) enables accurate measurements of the intensity and polarization of scattered light with a wide dynamic range, high angular accuracy, and multiple incident wavelengths (visible and UV) on 300 mm wafers (see Fig. 1). We measure the light scattering properties of well-characterized samples exhibiting interfacial roughness, deposited particles, subsurface defects, dielectric layers, or patterns. The emphasis is on providing accurate data, which can be used to guide the development of light scattering instruments, and to test theoretical models.

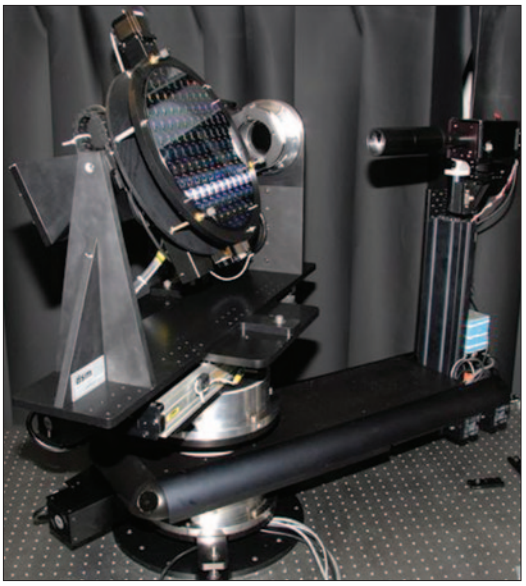

Figure 1. The Goniometric Optical Scatter Instrument is a state-of-the-art laser scattering facility.

2. Theoretical Light Scattering Calculations – Theoretical Light Scattering Calculations – The focus of our theoretical work is on: (a) developing models that accurately predict the polarization and intensity of scattered light, and (b) determining what information can be efficiently and accurately extracted from light scattering measurements. Approximate theories are used in conjunction with more complex techniques to gain an understanding of which parameters affect the light scattering process. Particular cases that are being analyzed include: (a) scattering by defects and roughness associated with dielectric layers, (b) scattering by particulate contamination on bare and oxidized wafers, and (c) scattering by periodic structures.

DELIVERABLES:

- Develop model for scattering by spherical particles embedded in a layer. 4Q 2009

3. Size Distribution Measurements – Differential mobility analysis (DMA) has been shown to be capable of making accurate size measurements for mean particle diameters as small as 50 nm. However, discrepancies have been noticed between PSL measurements using DMA, and measurements using light scattering on the surface of a wafer. These discrepancies are possibly due to the PSL particles deforming on the bottom as they adhere to the wafer. This problem will be investigated by comparing measurements of the PSL particles to measurements of silica particles, which are less likely to deform when they contact the wafer surface. Measurements will be performed using both the DMA and light-scattering instruments.

4. Resource on Particle Science – Over the past five years, the particle-related work has included projects with SEMATECH and particle suppliers to the semiconductor industry. A number of needs by particle related companies were expressed at a NIST particle workshop including redoing the uncertainty assessments of existing particle SRMs and offering a particle sizing calibration service. Providing support for particle needs critical to the semiconductor industry will continue to be a priority.

DELIVERABLES:

- Provide technical support to the SEMI Advanced Surface Inspection task force. 4Q 2009

Accomplishments

■ Completed and certified the measurements for new NIST Standard Reference Materials (SRM). Measured and certified SRM 1964, particles with a nominal diameter of 60 nm. Also measured and certified SRM 1963a, with a nominal diameter of 100 nm, to replace the previous 100 nm SRM 1963, which was corrupted due to agglomeration. SRM 1963a and SRM 1964 are currently available for purchase.

■ Completed initial screening process and preliminary measurements for development of a 30 nm SRM. Identified primary and secondary candidate samples for the 30 nm SRM, based on diameter and distribution measurements. Researched measurement uncertainty for particles smaller than 50 nm and devised strategies for reducing the uncertainty.

■ Developed and improved the NIST Calibration Facility, which uses Differential Mobility Analysis for sizing monodisperse spheres in the size range of 50 nm to 400 nm. Reduced the expanded uncertainty to 1.0 % of the particle size by correlating the slip correction to the measured particle size. Increased resolution and accuracy of measurements through improved equipment and intermediate measurements.

■ Determined that the electrospray technique can produce an aerosol having characteristics optimal for transferring particles in a liquid suspension onto wafers for particle diameters as small as 25 nm. This significant finding enables improved wafer depositions by reducing the number of contaminant residue particles, the number of doublets, and the amount of residue on the particles.

■ Coordinated the experimental design and uncertainty analysis with the University of Minnesota for the first measurement of slip correction of particles smaller than 300 nm. These measurements are critical to improving the accuracy of particle size by the DMA in the nanometer size range.

■ In collaboration with the University of Maryland, developed a method for generating pure copper spheres with diameters ranging from 100 nm to 200 nm. These spheres, which mimic real-world particles better than polystyrene, were used to validate particle scattering theories in conditions for which models have a higher degree of uncertainty. Measured polarization and intensity of light scattered from the copper spheres and found good agreement with the Bobbert-Vlieger theory for light scattering from a sphere above a surface.

■ Developed a method, based upon scattering ellipsometry, for quantifying scatter from two sources and demonstrated its use by characterizing the roughness of both interfaces of an SiO_2/silicon system. This finding establishes the validity of the light scattering models for roughness in a dielectric film, which in turn limits the detection sensitivity of SSIS instruments. The method was also used to characterize scattering from steel surfaces, demonstrating capability to distinguish between scattering from surface roughness and material inhomogeneity. The method was further used to study the scatter from an anti-conformal polymer film, helping to establish the limits of validity of the scattering theory.

■ Developed the SCATMECH library of C++ routines for light scattering. Published the SCATMECH library, providing a means for distributing scattering models and polarized light calculations to others. From the time of its public availability in March 2000, over 6000 copies of the library have been downloaded from the web. The Modeled Integrated Scatter Tool (MIST), a Windows application for calculating integrated scatter, was released in June 2004.

■ Extended the theory of scattering of a sphere on a surface to axially-symmetric non-spherical particles. Demonstrated that the scattering by a metal particle on a surface is extremely sensitive to the shape of the particle in the region where the particle contacts the surface. This unusual sensitivity to shape must be considered when light scattering tools classify particles for material and size.

■ Performed a light-scattering-based diameter measurement of the NIST 100 nm PSL sphere standard (SRM 1963) deposited onto a silicon wafer. The measurement results included a thorough assessment of the uncertainties that arise in such measurements. It was found that the uncertainty was dominated by the uncertainty in the shape of the particle on the surface. Results for smaller PSL particles suggest that surface-induced deformation of the particles must be considered.

■ Assisted in revising SEMI M53, a practice for calibrating scanning surface inspection systems, by developing a model-based calibration scheme that matches measured signals from PSL spheres to the predictions of a theoretical model. The accepted model for scattering by the spheres is specified in the standard as that provided by the MIST program. The new method has several advantages over the previous method, including: less sensitivity to changes in availability of specific size standards, improved accuracy, less

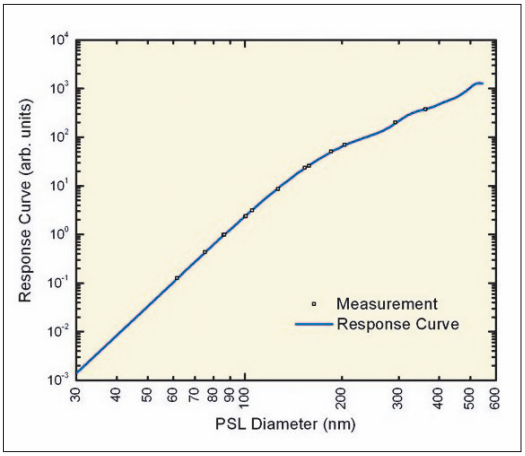

Figure. 2. Sample calibration of a commercial wafer scanner using the new SEMI M53 method. The relative expanded uncertainty in particle diameter has been reduced to less than 1 %.

variability between instruments, and an ability to extract a quantitative accuracy from the calibration. The expanded uncertainty found by applying the calibration to a commercial instrument was better than 1 % of the diameter.

■ Tested the use of silica spheres as a substitute for PSL spheres for calibrating scanning surface inspection systems. PSL spheres exhibit degradation upon repeated ultraviolet exposure, and more inspection tools are using ultraviolet wavelengths. The silica spheres were found to yield comparable calibrations, provided that they are classified with a PSL-sphere-calibrated classifier to reduce their size distribution. The index of refraction of the silica spheres was a byproduct of the measurements and are needed for the calibration.

Collaborations

Hitachi High Technology Corporation, Japan, Akira Hamamatsu, Light Scattering from Rough Surfaces.

Department of Chemical Engineering, University of Maryland, Professor Sheryl H. Ehrman, Validation of Scattering Theory Using Novel Monodisperse Particles.

Department of Mechanical Engineering, University of Minnesota, Professor David Pui, Generation and Measurement of Nanosize Particles.

National Metrology Institute of Japan, Dr. Kensei Ehara, Nanoparticle Metrology.

Recent Publications

T. A. Germer, C. Wolters, and D. Brayton, "*Calibration of wafer surface inspection systems using spherical silica particles,"* Optics Express 16 (7), 4698–4705 (2008).

T. A. Germer, *"Modeling the effect of line profile variation on optical critical dimension metrology,"* in Metrology, Inspection, and Process Control for Microlithography XXI, Proc. SPIE 6518, 65180Z (2007).

T. A. Germer, *"Effect of line and trench profile variation on specular and diffuse reflectance from a periodic structure,"* J. Opt. Soc. Am. A 24 (3), 696–701 (2007).

Thomas A. Germer, *"Measuring Interfacial Roughness by Polarized Optical Scattering,"* in Light Scattering and Nanoscale Light Scattering, A.A. Maradudin, Ed., (Elsevier, New York, 2007) Chapter 10, pp. 259–284.

M. K. Donnelly, J. C. Yang, *"Screening Candidates for 30 nm Spheres,"* NISTIR 7345, August 2006.

G. W.Mulholland, M. K. Donnelly, C. Hagwood, S. R. Kukuck, and V. A. Hackley, *"Measurement of 100 nm and 60 nm Particle Standards by Differential Mobility Analysis,"* J. Research NIST 111, 257–312, 2006.

Front-End Materials Characterization

This is a large project that involves parts that are not reasonably combined in a single document. For this reason, the project is presented in two sub-sections, each focusing on a single aspect. These are:

- Front-End Materials and Emergining Advanced Materials Characterization
- Micro-and Nanoanalysis of Front End Materials

Front-End Materials and Emerging Advanced Materials Characterization

Technical Contacts:
Kin P. Chueng
Joseph J. Kopanski
Nhan Nguyen

Goals

The goals of this project are to provide the IC industry with more useful and accurate measurements, models, data, and measurement transfer mechanisms for the incorporation of new materials into advanced CMOS, to enable the continuation of scaling, as well as, beyond the limits of scaling. The major near term focus is on the search for new channel materials, new higher-κ dielectrics, metal gates and the integrated structure involving all three material types. Beyond 2011, high-mobility channel materials are expected to replace silicon in CMOS technology. New device structures, such as multi-gate non-planner transistor, are expected to replace the planar MOSFET. Devices based on semiconductor nanowires, carbon nanotubes, III-V quantum-well transistors, or another technology may even be used. The pace of new materials introduction is expected to increase. The introduction of new materials always presents substantial process integration challenges, as well as new reliability concerns. New metrology techniques must be developed to keep pace with all these changes. New measurement techniques are needed to address physical, chemical, optical and electrical properties of these new materials at the device level. Our current goals are:

(1) To improve the measurements of composition and thickness of thin films and interfaces for high-κ/compound metal gates on III-V compound semiconductors, silicon-on-insulator (confined silicon), and strained silicon-germanium.

(2) To improve measurement capabilities (on large custom made test structures) of interface energy barrier, work function, band offset, and interfacial defect structures of high-κ / metal electrode stacks on III-V systems.

(3) To develop high-resolution techniques (such as various kinds of scanning probe microscopy) to measure two-dimensional dopant profiles in advanced devices, strain profiles in the channel, work function and surface potential distribution, and dielectric constant.

(4) To correlate materials properties to the electrical performance of the transistor.

Customer Needs

The semiconductor industry has historically achieved exponential performance gains by aggressively scaling transistor dimensions. However, as devices approach sub-100 nm dimensions, scaling becomes more challenging and new materials are required to overcome the fundamental physical limits of the existing materials. The pace of new materials introduction is increasing as CMOS technology continues to advance. The introduction of new material into CMOS technology is always extremely challenging. For example, the introduction of high-κ/ metal gate stack was considered impractical for a very long time. Even as high-κ dielectrics and metal gates went early production in 2008, the materials and measurement needs for these material systems continue to evolve. The need for alternative channel materials is expected as early as 2011 to overcome the carrier-mobility limitations of silicon. Non-planar, multi-gate transistors are expected to be required as well. Even new device structures based on nanowires may be needed. In current main-stream CMOS technology, the use of strain in the channel region to enhance carrier mobility created fundamental materials questions such as determining the stress-strain relationship on the nanoscale. Such questions urgently need new measurement capability to address them. The answer has direct implication on technology decisions in the next generation and beyond.

Front end materials are in the critical path of technology decisions. A wrong decision may not only be expensive, but also disastrous. Facing the increasingly wider choices (or potential technology options), industry needs highly efficient, highly reliable, and highly accurate metrology tools to help them make the right choice. The winter 2007 International Technology Roadmap for Semiconductors (ITRS) conference discussed these trends and the new measurement challenges for Front-End Process Metrology, High κ/ metal gate stacks, alternative channel materials, and emerging research materials and devices. The current most important challenge in III-V nanoelectronics for logic is the compatibility of the III-V and the high-κ/ metal gate.

III-V compound semiconductor devices have involved into a major part in industrial applications of the communication devices as stated in the International Technology Roadmap for Semiconductors (ITRS). High-frequency III-V compound semiconductor devices with nanometer feature sizes have become key components in many high-speed systems. Only recently, III-V metal-oxide-semiconductor (MOS) with high-κ dielectric as insulator has been realized as a possibility to replace the Si-based traditional MOS beyond the 22 nanometer technology node.

Technical Strategy

Understanding the physics of the high-κ/metal gate structure on III-Vs is critical to successfully selecting the right dielectric and metal to fabricate and implement the next complex emerging nanoelectronic devices. Within our resources, the approach is to find a way to produce a stable and reliable high-κ dielectric on a III-V substrate. Our focus areas include development of the III-V substrate surface treatment that allows a growth of electronically stable high-κ material and refined metrology methods to determine the interfacial physical, chemical, and electronic properties.

Energy Band Alignment of Metal Gate/High-κ/III-V compound semiconductor

Intel and IBM have successfully implemented metal gate and high-κ dielectric in place of the traditional poly-silicon and thermal SiO_2 into the 45nm manufacturing process. Intel cofounder Gordon Moore stated "The implementation of high-κ and metal materials marks the biggest change in transistor technology since the introduction of poly-silicon gate MOS transistors in the late 1960s." Such successes have opened up the possibility of extending silicon-based CMOS to employ metal gate and high-κ dielectric on high-mobility III-V compound semiconductors for high-speed and high-performance electronic device fabrications. However, the main difficulty that hinders the advancement of GaAs-based metal oxide semiconductor field-effect transistors is the lack of an appropriate oxide as a gate dielectric. There have been many efforts to search for electronically reliable and thermodynamically stable gate dielectrics that can be grown or deposited on GaAs. In addition, the stringent requirement that its fabrication method be compatible with Si-based device processing imposes a greater challenge. Several dielectrics have been investigated including Gd_2O_3, Al_2O_3, and HfO_2. One of the deciding factors for the selection of an appropriate dielectric is the band offsets at the dielectric interfaces with the III-V substrate and the metal gate, which must be large enough to minimize leakage currents.

DELIVERABLES:

- Optical characterization and band alignment determination of $Al/Al_2O_3/In_{1-x}Ga_xAs$ 2Q, 2009

It is believed that III-V MOS devices will significantly outperform the scaled Si MOSFETs. Researchers in academia and industrial laboratories, including Intel Inc, Motorola, International SEMATECH, Purdue University, and University

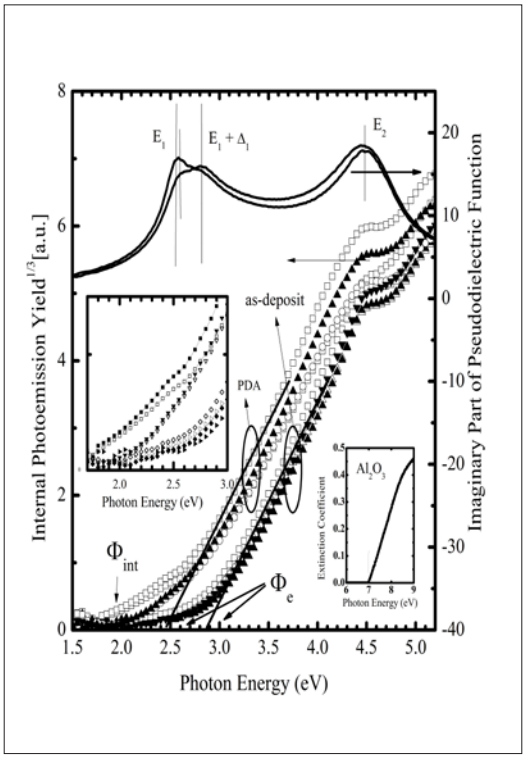

Figure. 1. Internal Photoemission Spectroscopy and Vacuum Ultraviolet Spectroscopic Ellipsometry Studies of Al_2O_3/ $In_xGa_{1-x}As$: Φ_es are energy thresholds of photoelectron transition from the top valence band of InGaAs to the bottom conduction band of Al_2O_3. Post-deposition annealing (PDA) decreases Fe as compared with that of as-deposited Al_2O_3 and also increases the interfacial layer resulting in a lower threshold Φ_{int} (left inset figure). The influence of the direct optical transitions (E_1, $E_1+\Delta_1$, and E_2) of InGaAs on the electron photoemission is also observed. Combining the measured barrier height and the measured bandgap of Al_2O_3, we can establish the band alignment of a metal oxide semiconductor (MOS) device of $Al/Al_2O_3/ In_xGa_{1-x}As$.)

of Texas at Dallas, have invested resources to investigate these devices. At the current status, it appears that the key to a successful III-V device fabrication is to find a stable and efficient high-κ gate stack on III-V channels. To that effort, in collaboration with Prof. Peide Ye and his research group at Purdue University, we have started investigating the electronic properties of the interface of various high-κ dielectric and III-V substrates using optical and electrical characterization techniques including a novel internal photoemission spectroscopy, vacuum ultraviolet spectroscopic ellipsometry, and traditional electrical methods.

Accomplishments

Recently, in collaboration with Intel and Purdue University, we employed Internal Photoemission Spectroscopy (IPE) and Vacuum Ultraviolet Spectroscopic Ellipsometry (VUV-SE) measurements to establish the energy band offsets at the interfaces of Al_2O_3 as the high-κ dielectric on molecular-epitaxy-grown high-mobility $In_{1-x}Ga_xAs$ with Al metal gate. We found that Al_2O_3 provides conduction band and valence band offsets at its interfaces with InGaAs of more than 2 eV, which makes this high-κ dielectric suitable as a gate insulator for III-V MOSFET devices. Furthermore, the effect of post deposition annealing is observed to reduce the band offsets and induce an interfacial layer (See Figure 1). Such interfacial layer results in a much lower band offset at the interface and may lead to enhanced charge injection from InGaAs into the insulation layer. Therefore, the interfacial oxide layer between InGaAs and high-κ dielectric should be avoided or minimized.

Semiconductor Material and Device Electrical Characterization with Scanning Probe Microscopes

The emerging need for alternative channel materials for ultimate CMOS opens up a plethora of materials characterization issues. Strained Si-Ge has already been implemented in current technology-node CMOS, while alternative channel materials such as Ge-on-insulator for PMOS and III-V for NMOS technology have been proposed for ultimate CMOS. Characterizatiotn of the complete MOS stack from the work function of the metal gate, the band offsets, and the interfacial defect structures of high-κ combinatorial metal electrode stacks systems becomes necessary. Integration of these new materials into existing process lines and their effect on device performance and reliability are key concerns to ensure manufacturability.

We are developing and employing several varieties of scanning probe microscopy (SPM) for characterization of critical front end material parameters. SPMs offer the promise of extremely high spatial resolution measurement of local electrical properties. Scanning capacitance microscopy (SCM) remains of interest for measurement of both the ultra-shallow junction dopant profiles in silicon as well as in strained Si-Ge and III-Vs. Improvements in this technique are needed to achieve the spatial resolution requested in the ITRS. A new generation of SPM-based methods is possible that integrate measurement instruments directly into SPM tips. We are building on-chip capacitance sensors which can be placed in very close proximity to the AFM cantilevered tips. This will enable interface between the sensor and the tip with very low stray capacitance. Many traditional capacitance-based measurement methods such as C-V, deep level transient spectroscopy, and optically pumped spectroscopies may be enabled by such an instrument. This approach may have significant applications to semiconductors for high power and photovoltaics as well.

Another technique of great interest is the scanning Kelvin force microscope (SKFM) for the local measurement of contact-potential difference. If the tip work function is known, the work function of the sample under test can be deduced. We have recently demonstrated test structures with multiple different metals, for example, aluminum (φ_{Al} = 4.28 eV), chromium (φ_{Cr} = 4.5 eV), and gold (φ_{Au} = 5.1 eV). Since the effective work functions of these three metals can be measured with tips of known work function, they can then be employed as a vehicle to determine the work functions of tips that are not known, for example, carbon nanotube tips. Recent work has demonstrated the spatial resolution limits of the SKFM microscope and has suggested a method to improve the spatial resolution. SKFM depends on the capacitance between the tip and the sample, which varies as the inverse square of the separation of the various parts of the tip with the sample. As this is a relatively large-range force, the tip, tip sidewall, and cantilever all contribute significantly to the measured CPD, effectively making measurements that are simultaneously accurate and having high spatial resolution im-

possible. Several methods for improving the spatial resolution of the SKFM by using the derivative of the force between the tip and sample as the feedback signal are under development. If spatial resolution can be improved, SKFM has many potential applications.

DELIVERABLES:

Deliver ultimate Kelvin force microscopy data acquisition methods for use in ambient atmosphere. Implement and publish advanced data acquisition methods using external feedback loops and advanced (carbon nanotube and nanowire based) tips. Determine the absolute accuracy of contact potential difference measurements and spatial resolution possible with these techniques. Q4, 2009

Conventionally available scanning Kelvin force microscopy (SKFM) suffers from poor spatial resolution due to the capacitive coupling of all parts of the tip/cantilever assembly with the sample. We have demonstrated improved spatial resolution by using carbon nanotube terminated tips and have demonstrated the feasibility of implementing frequency modulated or phase feedback modes of SKFM at atmospheric pressure. Implementation of both these improvements promises higher quality SKFM measurements of contact potential difference than previously available.

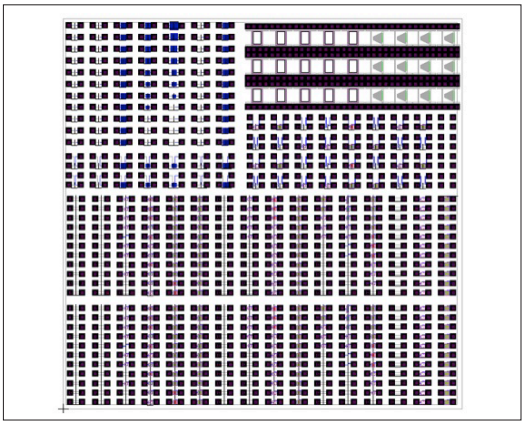

Figure 2. Small capacitance test chip. Chip contains a series of MOS and MIM capacitors designed to test the sensitivity and accuracy of capacitance measurement instruments at levels of 0.1 fF to 1 pF. Devices directly assessable via scanning probe microscopy are in the upper right hand corner for calibration of the scanning capacitance microscope (SCM) and the scanning Kelvin force microscope (SKFM).

DELIVERABLES:

Work with collaborators at SEMATECH, Xidex Corp., and the University of Albany to measure SEMATECH produced structures with CNT-based tips. In particular, determine spatial resolution enhancement with best CNT tips; accuracy and spatial resolution of work function measurements; improvements to dopant profiling; and investigate SCM/SKFM to measure etching- induced dielectric constant damage to low-κ dielectrics. Q3, 2010

Beginning in September of 2009, we have a year-long collaboration to determine the performance of electrically based SPM methods using conductive carbon nanotube tips fabricated by Xidex Corp. using samples fabricated by SEMATECH at the University of Albany. We will compare the performance of these tips with the best currently commercially available. Specific goals include determining the work function and resistivity of

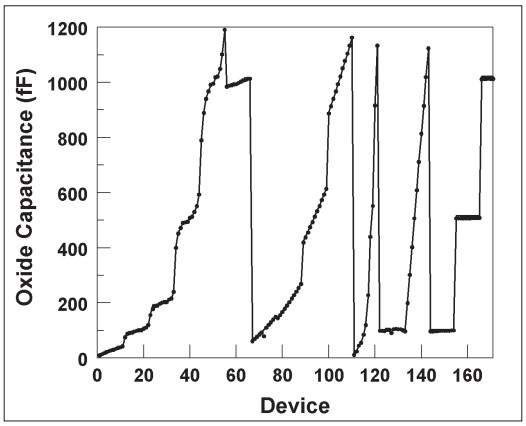

Figure 3. Typical "fingerprint" of the measured oxide capacitance values of the MOS devices on the test chip. Theoretical values of oxide capacitance are plotted as the solid line and the measured values are the plotted points (after correcting for stray and pad capacitances.) This test chip will be used to compare the sensitivity and accuracy of chip-based capacitance measurement circuits to conventional capacitance measurement instruments.

the CNTs, and demonstration of the use of CNT tips for SCM and SKFM dopant profile measurements, determination of dielectric constant damage to low-κ dielectrics, and high spatial resolution work function measurements.

Accomplishments

• Fabricated a test chip with which to determine the current state of the art of capacitance-voltage measurements. The component capacitance of individual nm-scale nanoelectronic devices for future generations of integrated circuitry defies easy measurement. Emerging nanoelectronic devices such as those fabricated from semiconductor nanowires (NWs) and quantum dots, as

well as FINFET type devices have capacitances that are much smaller than those measurable by conventional LCR meters. The intrinsic device capacitances of these deep-submicron devices (such as the gate-drain, source-drain, or gate-channel capacitances) determine the operational characteristics of the structures and an accurate knowledge of their values is required for accurate device modeling and predictive computer-aided design. We are developing methods to combine probe stations with the sophisticated capacitance measurement equipment and expertise associated with maintaining the capacitance standard for the farad to enable measurements of critical capacitances in nanoelectronic devices at the aF level.

We designed and fabricated a test chip (consisting of an array of metal-oxide-semiconductor (MOS) capacitors and metal-insulator-metal capacitors ranging from 0.3 fF to 1.2 pF) for use in evaluating the performance of new measurement approaches for small capacitances (see Fig. 2). By measuring the complete array of capacitances, a "fingerprint" of capacitance values is obtained (see Fig. 3) which – after correcting these data for pad and other stray capacitances – can be used to assess the relative accuracy and sensitivity of a capacitance measurement instrument or circuit. We are implementing various approaches to on-chip capacitance measurement that promise substantial improvement over traditional probe-station-based measurements. A significant challenge will be to use the AFM tip to interface the capacitance sensor with devices fabricated on another chip.

Collaborations

Center for Nanophase Materials Sciences, Oak Ridge National Laboratory – User proposal reviewer.

Intel – Electrical and optical characterization of metal gate/high-κ dielectric / III-V high mobility semiconductors.

Intel – Measurement of ultra shallow dopant profiles using SCM and advanced tips.

International SEMATECH – Optical electrical characterization and energy band alignment of ternary metal gate/high-κ / Silicon.

International SEMATECH, ATDF – Thin oxide depth-profiling by SIMS, backside depth profiling of patterned PMOS wafers.

International SEMATECH – Improvement of the SCM and SKFM techniques for two-dimensional dopant profiling and surface work function measurements.

IBM – Physical and optical characterization of high- κ on Silicon.

MSEL, NIST – Characterization of metal gate/high-κ systems.

National Science Foundation – NIST Research Experience for Undergraduates site: EEEL Summer Undergraduate Research Fellowships

Purdue University – Surface characterization and electrical and optical band offset characterization of metal gate/ high- κ dielectric / III-V high mobility semiconductors.

University of Albany – Scanning probe microscopy characterization of front end processes and advanced materials.

University of Texas-Dallas – Surface characterization and electrical and optical band offset characterization of metal gate/ high-κ dielectric / III-V high mobility semiconductors.

University of Maryland, College Park – Ultra-thin gate oxide reliability. Xidex Corp. – Evaluation of carbon nanotube tip for use in SCM and SKFM.

Yale University – Electrical characterization of high-κ systems.

Recent Publications

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N. V. Nguyen, O. A. Kirillov, W. Jiang, Wenyong Wang, J. S. Suehle, P. D. Ye, Y. Xuan, N. Goel, K.-W. Choi, W. Tsai, and S. Sayan, *"Band offsets of atomic-layer-deposited Al_2O_3 on GaAs and the effects of surface treatment,"* Appl. Phys. Lett. 93, (2008).

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S. Sayan,D. Chandler-Horowitz, N. V. Nguyen, and J. R. Ehrstein, *"High sensitivity attenuated total reflection Fourier transform infrared spectroscopy study of ultra-thin ZrO_2 films: A study of phase change,"* J. Vac. Sci. Technol. A 26, 270, Mar/Apr 2008.

D. H. Hill, R. A. Bartynski, N. V. Nguyen, A. C. Davydov, D. Chandler-Horowitz, and M. M. Frank, *"The relationship between local order, long range order, and sub-band-gap defects in hafnium oxide and hafnium silicate films,"* J. Appl. Phys. 103, May (2008).

J. E. Maslar, W. S. Hurst, D. R. Burgess, W. Kimes, N. V. Nguyen, E. F. Moore, and J. T. Hodges, *"In Situ Gas Phase Diagnostics for Hafnium Oxide Atomic Layer Deposition,"* Electrochem. Soc. Trans. 13, 139, March (2008).

N. V. Nguyen, O. Kirillov, H. D. Xiong, and J. S. Suehle, *"Internal Photoemission Spectroscopy of Metal Gate / High-κ / Semiconductor Interfaces,"* Frontiers of Characterization and Metrology for Nanoelectronics: 2007, AIP Conference Proceedings 931, page 308 (2007).

J.E. Maslar, W.S. Hurst, D.R. Burgess, Jr., W.A. Kimes, N.V. Nguyen, and E.F. Moore, *"In Situ Characterization of Gas-Phase Processes During Hafnium Oxide Atomic Layer Deposition,"* Electrochem. Soc. Trans. 2, 133-143 (2007).

J. J. Kopanski, M. Y. Afridi, S. Jeliazkov, W. Jiang, T. Walker, *"Scanning Kelvin Force Microscopy For Characterizing Nanostructures in Atmosphere,"* Proceedings of the International Conference on Frontiers of Characterization and Metrology for Nanoelectronics, pp. 530-534, Gaithersburg, MD, March 27-29, 2007, (Sept. 2007).

J. J. Kopanski, *"Scanning Capacitance Microscopy for Electrical Characterization of Semiconductors and Dielectrics,"* in the book: Electrical and Electromechanical Characterization by Scanning Probe Microscopy, Springer Science + Business Media, Inc., New York, NY (Feb. 2007).

S.-E. Park, N. V. Nguyen, J. J. Kopanski, J. S. Suehle, and E. M. Vogel, *"Comparison of scanning capacitance microscopy and scanning Kelvin probe microscopy in determining two-dimensional doping profiles of Si homostructures,"* J. Vac. Sci Tech. B, vol. 24, p. 404, (2006).

J. Ehrstein, C. Richter, D. Chandler-Horowitz, E. Vogel, C. Young, S. Shah, D. Maher, B. Foran, P. Y. Hung, and A. Diebold, *"A Comparison of Thickness Values for Very Thin SiO_2 Films by Using Ellipsometric, Capacitance-Voltage, and HRTEM Measurements,"* J. Electrochem. Soc., vol. 153, p. F12, 2006.

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Micro- and Nanoanalysis of Front End Materials

Goals

To provide industry with new and improved measurements, models, data, and measurement traceability/transfer mechanisms to enable the more useful and more accurate metrology infrastructure needed for select silicon CMOS front-end materials characterization. The major focus is placed on metrology requirements from the 2007 International Technical Roadmap for Semiconductors (ITRS) expressed as difficult challenges: (1) structural and elemental analysis at the device level, including SIMS and EFTEM, and (2) metrology for advanced gate stacks and other thin films. Additional work will be undertaken as possible on additional important thin films and bulk material properties for silicon and other emerging semiconductors.

(1) To improve capabilities for compositional depth profiling, this project develops new methods for depth-profiling polymeric materials by Secondary Ion Mass Spectrometry (SIMS), defines optimum procedures for ultra-high depth resolution, develops depth-profiling reference materials needed by U.S. industry, and improves the uncertainty of implant dose measurements by SIMS.

(2) To address needs in composition and thickness measurements for thin films and interfaces, this project develops new optical and physical characterization methods, as well as, characterizes the accuracy and reliability of existing methods. Materials of interest include high-κ and low-κ materials, polymers, silicon-on-insulator (confined silicon), and strained silicon-germanium. Energy-filtered Transmission Electron Microscopy (EFTEM) is being developed as a chemical tomography tool for determining 3-D elemental distributions in advanced materials.

Customer Needs

This project addresses key material characterization problems associated with the integrated circuits industry's front-end process, particularly new gate stack processes and materials, and metrology for structural and element characterization at the device level, particularly ultra-shallow junctions. Front-end processing requires the growth, deposition, etching, and doping of high quality, uniform, defect-free films. These films may be insulators, conductors, or semiconductors. The 2007 International Technology Roadmap for Semiconductors (ITRS) near-term difficult challenges for front-end processes include: *metrology issues associated with gate dielectrics film thickness and gate stack electrical and materials characterization and metrology issues associated with 2-D dopant profiling. Metrology needs for thermal/thin films, doping technology, SOI, and strained-silicon are discussed in the Metrology section of the 2007 ITRS.*

Since source/drain dopant profiles are a critical factor determining the performance of a transistor, dopant profiling has always been needed by the silicon integrated circuit industry. One-dimensional dopant profiles from SIMS or electrical techniques remain an important process control tool. As transistors are scaled to ever-smaller dimensions, the variation of dopant profiles in two- and three-dimensions also begin to influence device operation. Two- and three-dimensional dopant profiles are now needed to validate models of the processes used to produce ultra-shallow junctions and for accurate device simulations.

SIMS is most likely to provide the solution to precision requirements for 1-D dopant concentration measurements. These goals can be achieved by careful control of SIMS depth-profiling conditions and by developing and making available implant reference materials for common dopant elements.

The 2007 ITRS Metrology section identifies structural and elemental analysis at devices dimensions (for example 3-D dopant profiling) as one of the difficult near-term challenges (Table MET1). Offline secondary ion mass spectroscopy has been shown to provide the needed precision for current generations including ultra-shallow junctions. Two- and preferably three-dimensional profiling is essential for achieving future technology generations. Activated dopant profiles and related TCAD modeling and defect profiles are necessary for developing new doping technology. The ITRS requirements are for

Technical Contacts:
G. Gillen: SIMS
D. Simons: SIMS
I Anderson: EFTEM
S. Stranick: Confocal Raman microscopy

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Veeco

at-line dopant profile concentration measurements with precision of 4 % in 2007, decreasing to 2 % precision for the 2010 through 2018 timeframe. The lateral/depth resolutions for 2-D/3-D dopant profiling decrease from 2.5 nm in 2007 to 1.4 nm in 2012. Complete specifications are given for the short term in Table MET5a and for the long term in Table MET5b of the 2007 Metrology section. The need for advances in image and spectral modeling for TEM and STEM applied to 3-D atomic imaging and spectroscopy is discussed under Emerging Research Materials and Devices in the Metrology section of the 2007 ITRS. The desirability of nondestructive direct measurement of stress in nano-sized areas of strained silicon is described in the Front End Processes area of the Metrology section, and specific requirements are given for the first time in Tables MET5a and MET5b.

Technical Strategy

The 2007 ITRS expressed as difficult challenges: "starting materials metrology and manufacturing metrology are impacted by the introduction of new substrates such as SOI. Impurity detection (especially particles) at levels of interest for starting materials and reduced edge exclusion for metrology tools. CD, film thickness, and defect detection are impacted by thin SOI optical properties and charging by electron and ion beams," and "measurement of complex material stacks and interfacial properties including physical and electrical properties" (Table MET1, Metrology Section). Our focus areas include development of refined metrology methods and standards for SIMS and TEM and developing improved X-ray detection capabilities for SEMs and electron microprobes.

STRUCTURAL AND ELEMENTAL ANALYSIS AT THE DEVICE LEVEL, INCLUDING SIMS AND HRTEM

The revolutionary changes in device technology needed to sustain long-term improvements in the performance of nanoelectronics demand the development of new more sophisticated nanometer- and sub-nanometer-scale metrology solutions. New device technologies comprise new materials and novel three-dimensional (3D) geometries in the medium term, and a full-scale break from the CMOS paradigm in the long term. We are developing new techniques for 3D characterization using existing 2D projection-based nanometer-scale metrology tools such as conventional or scanning transmission electron microscopy. Specifically, we are using a state-of-the-art energy-filtered TEM to develop a method for creating 3D chemical tomography with nanometer spatial resolution.

DELIVERABLES:

- Perform correlative electron microscopy and atom probe tomography analysis on FinFET with external collaborator. 3Q 2009

2. Strained Si processes have become an accepted means for enhancing carrier mobility and thereby improving transistor performance. The ITRS calls for a nondestructive method for measuring stress in nano-sized areas of Si to accelerate process development. Confocal Raman microscopy is a potential in-line method to achieve this goal with the required sensitivity and spatial resolution. We are conducting a systematic investigation to determine the feasibility of this methodology for achieving the metrology goals for stress and strain that are called out for the first time in the 2007 ITRS.

DELIVERABLES:

- Determine the full vectoral representation of a stress profile in nanostructured Si using confocal Raman microscopy. 3Q 2009

As integrated circuit dimensions shrink to the sub-micrometer regime, there is continued need for accurate and quantitative dopant depth profiling with ultra-high-depth resolution. To probe shallow dopant profiles in Si and other materials, SIMS instruments typically utilize very low energy primary ion beams to bombard the sample surface. In this case, it is difficult to obtain a well-focused and high current density beam, especially in a magnetic-sector SIMS instrument. Recently, there has been growing interest in using molecular ion beams for depth profiling. When a molecular primary ion beam impacts the surface, it dissociates into its constituent atoms with each atom retaining a fraction of the initial energy of the cluster.

This process can lead to impact energies on the order of a few 10's of electron volts and a corresponding reduction in the depth of penetration of the primary ion. This process may potentially allow for ultra high resolution depth profiling. In this project, we will utilize C_{60}+ and Bi_3+ cluster primary ion beam sources at NIST to sputter depth profile Si, GaAs, SiC, and multiple delta-layer test materials. Some thin-film materials

such as metals do not sputter as uniformly as silicon under ion bombardment. In these cases, the achievable depth resolution is limited not by the penetration depth of the primary ion but by the topography induced by the sputtering process itself.

DELIVERABLES:

- Determine influence of experimental parameters on optimal depth resolution for PMMA/Si bilayer films under cluster ion bombardment. 2Q 2009

Accomplishments

Implementation of C_{60}+ Cluster Ion SIMS Capability for SIMS Analysis of Silicon Wafers

Previous efforts using SF_5^+ cluster primary ion sources used for SIMS analysis of both organic and inorganic materials on silicon have been very successful. Minimization of beam-induced damage in organic materials has allowed molecular depth profiling of polymers such as photoresists on silicon and enhanced ion yields for high-molecular weight fragments. Inorganic material analysis has benefited in the area of ultra-shallow depth-profiling as well as for analysis of some particularly difficult systems such as metal multilayers stacks. Continued development of SIMS for higher depth resolution dopant profiling has led to the implementation of a C_{60}+ primary ion source on the NIST magnetic sector SIMS instrument. This ion source produces stable ion beams of C_{60}+ and C_{60^2}+ at beam energies of 10 keV with typical currents approaching 20 nA under conditions that allow several hundred hours of operation. The beam can be focused into a spot size of ≈1 μm allowing micrometer spatial scale mapping of patterned silicon wafers. Due to the breakup of the C_{60}+ projectile during impact with the silicon surface, the energy of an individual carbon atom in the cluster is reduced to a few hundred electron volts. This low energy should theoretically provide SIMS depth resolution better than 1 nm. Reduction of the C_{60}+ impact energy to values less than 10 keV to attempt further improvement in depth resolution is foiled by carbon deposition that precludes the acquisition of depth profiles from the wafer sample. However, the deposition effect may be useful for lithographic applications as it allows direct ion beam writing of a conductive carbon layer on silicon. By using C_{60}+ impact energies greater than 10 keV, C_{60}+ SIMS depth profiles have been obtained from a number of semiconductor-related materials including As and B delta-doped structures as well as ion implants of various dopant species. The depth resolution of SIMS depth profiles obtained from these samples has not been has high as expected. To understand the process in more detail, transmission electron microscopy (TEM) studies of C_{60}+-bombarded silicon have been carried out using focused ion beam (FIB)-prepared cross sections of the sample surface. Figure 1 shows a cross sectional TEM image of a silicon wafer bombarded with C_{60}+ at an impact energy of 14.5 keV. The figure indicates that C_{60}+ bombardment of silicon results in the formation of a carbon-rich altered layer that is about 25 nm thick, much greater than the 2 nm range predicted from conventional ion implantation models. Working with Micron Technology and International SEMATECH, we are currently studying the effect of this extended transport of carbon into silicon both from the standpoint of improving the applicability of larger carbon cluster ion beams for SIMS analysis and also as a potential method for direct-write fabrication of SiC films and devices on silicon.

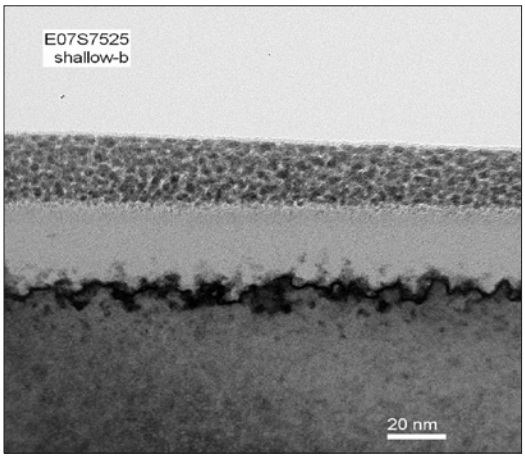

Figure 1. Cross sectional TEM image of C_{60}-bombarded silicon wafer. Top layer is a Pt metal overcoat. Middle layer is C_{60} altered layer. Bottom layer is the silicon substrate.

Molecular Depth Profiling of Photoresist Films Using SIMS

Recent advances in cluster secondary ion mass spectrometry (SIMS) have led to the ability to perform molecular depth profiling for a range of organic materials. Cluster SIMS can provide high sputter yields that remove beam-induced molecular damage as it is created. In time-of-flight SIMS analysis a "dual-beam technique"

can be exploited by using a cluster ion beam such as SF_5+ or C_{60}+ for continuous sample erosion and minimal damage accumulation, combined with a highly focused pulsed analysis probe such as Bi_3+ or Au_3+. However, little has been reported concerning the effects imparted by the use of the analysis beam. We have found that increasing the total Bi_3+ fluence beyond 1012 ions/cm^2 within a SIMS dual-beam sputter depth profiling experiment can degrade the quality of the interface widths of a PMMA film on silicon, despite the use of sputter beams such as SF_5+ and C_{60}+ to remove accumulated beam-induced damage. Specifically, Figure 2 shows the effects of steadily increasing amounts of 25 keV Bi_3+ analysis fluence with constant 5 keV SF_5+ sputter fluence. Normalized depth profile data signals of the characteristic PMMA fragment ion at m/z 69 (corresponding to C_4H_5O+) and the substrate silicon ion at m/z 28 are plotted in Figure 2 vs. PMMA film depth. The black and red profiles at the two lowest Bi_3+ fluences have similar shapes and the factor of three increase in analysis beam fluence between them did not degrade the profile shape through the polymer/silicon interface. However, increasing the total analysis fluence to 2.2 x 10^{12} ions/cm^2 (blue profile) shows a degradation of the interface quality and an earlier depth at which silicon signal appears in the profile. Increasing the Bi_3+ analysis fluence to the highest values in the figure (green and grey profiles) shows a trend of earlier silicon and increased interface width. The generation of analysis beam-induced topographic roughness can create paths for substrate ions to be ejected through the overlayer film before the entire film is eroded away by sputtering.

The characteristic exponential decay lengths of the PMMA signal range from 14.1 nm to 50.5 nm in Figure 2. These data imply that the energetic Bi_3+ projectiles generate enough sub-surface molecular damage and/or molecular rearrangement so that cluster sputtering becomes inefficient at removing the analysis-beam-induced effects. This study implies that careful attention must be applied when establishing the instrumental parameters for a molecular depth profiling measurement of an overlayer on silicon. PMMA on Si is a simple system, and it is expected that this behavior will be more pronounced for systems of multiple organic layers where more extensive beam-induced mixing and topographic roughness can accumulate as a function of eroded depth.

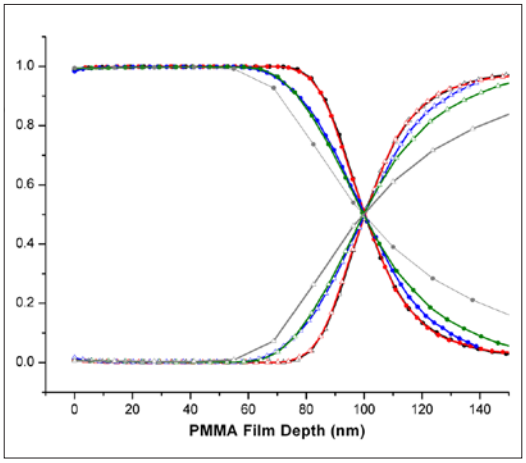

Figure 2. Normalized dual-beam TOF-SIMS depth profiles of PMMA on Si for 5 different fluences of Bi_3+ analysis beam. Solid circles – $^{69}C_4H_5O^+$; Open triangles – $^{28}Si^+$.

A properly defined cluster SIMS measurement can overcome these analysis beam effects and generate depth profiling results of organic and mixed organic/inorganic samples that allow for detailed study of interface chemistries on the nanoscale.

Nanoscale Stress Measurements using Confocal Raman Microscopy

To optimize yield and reliability in microelectronic, photonic, and microelectromechanical devices, measurement tools and metrology must be developed that can accurately detail the stress state of a material on the nanoscale. To address this need, work has been focused on the application and advancement of confocal Raman microscopy and the protocols that enable the characterization of stress in semiconductor structures. The results of high-resolution, high-density stress mapping of nanoindentations in silicon have been used to begin the validation and calibration of the measured stress. In these studies, high-resolution scans detail the stress distribution around the deformed area of the indentation as well as the stress fields that result from accommodation of higher loads, e.g. fracture. Hyperspectral peak-fitting algorithms and super-resolution techniques have been developed that provide stress resolution of approximately 10 MPa, lateral spatial resolution approaching 100 nm, and depth resolution approaching 300 nm. Indentation and crack field stress distributions have been measured and the results agree well with analytical models. The effects of indentation load for both spherical and

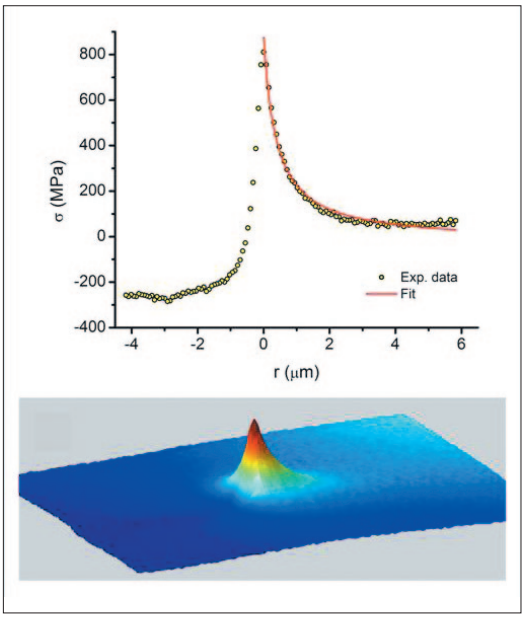

Figure 3. Hyperspectral Raman microscopy stress measurement on Si(100). Bottom: 3D stress map with 128 x 128 spectra over a 10 μm x 10 μm area of a nanoindentation. Top: Line scan of stress and model fit.

pyramidal indentation and crystal orientation have been demonstrated on Si(100) and Si(111) surfaces. Figure 4 shows the results of a hyperspectral Raman microscopy stress measurement on Si(100) over a 10 μm x 10 μm area. The color image (bottom) is of a region of a nanoindentation that includes a crack tip. The stress map of this feature and more importantly the functional form of the stress field falloff (shown at the top) provides information (stress-intensity factor and thus toughness) critical for determining the suitability of a material for a given application. Current efforts are focused on the development of models and the benchmarking of experimental protocols for the complete characterization (tensor field vs. scalar map) of intrinsic and engineered stress states in semiconductors.

Inkjet Printing for Trace Metal Contamination Standards

Prototype reference materials for trace element contamination on silicon surfaces have been prepared using piezoelectric drop-on-demand inkjet printing technology. Reference materials were prepared for 6 different elements (K, Cl, Ni, Cu, Fe, and Au) at surface area concentrations ranging from 10^7 atoms/cm^2 to 10^{15} atoms/cm^2. Each element was prepared on a separate 2.5 cm diameter silicon wafer. The microdroplets were dispensed onto specific grid squares that had been previously scribed onto the silicon surface in a finder grid pattern with a laser. Different concentrations of the elements were achieved by printing different numbers of microdroplets in the same location. Dispensing droplets onto specific locations on a finder grid allowed different contaminant concentrations to be located easily and analyzed rapidly by SIMS analysis.

Characterization of these reference materials is in progress. SIMS depth profiles from grid squares containing different numbers of printed droplets show an exponential decay, the amplitude of which scales with the number of droplets applied. Integration of the number of ion counts beneath these profile curves is shown in Figure 6 plotted against the number of droplets printed for concentrations of gold ranging from approximately 1 x 10^{12} atoms/cm^2 to 1 x 10^{14} atoms/cm^2. This plot shows the linear relationship between the measured number of gold ions detected and the number of droplets dispensed.

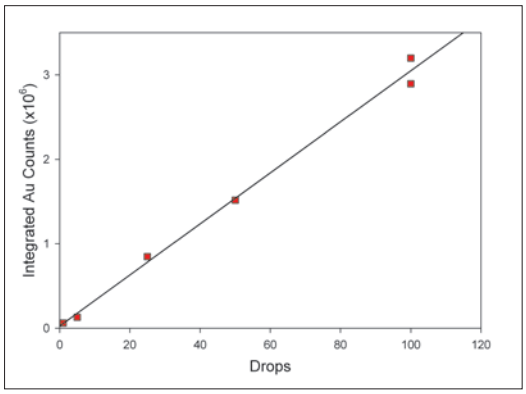

Figure 4. Integrated gold secondary ion counts from depth profiles plotted against the number of droplets dispensed by the inkjet printer. One drop = 1.3 x 10^{12} atoms/cm^2.

Low-Loss Energy-Filtered TEM Spectral Imaging for Chemical Imaging of FinFET Devices

Energy-filtered transmission electron microscopy (EFTEM) provides an attractive means for characterizing CMOS Extension and Beyond CMOS device structures because of its sub-nanometer spatial resolution, flexible applicability to both lithographic and free-standing nanostructures, chemically sensitive contrast, and three-dimensional (3D) characterization

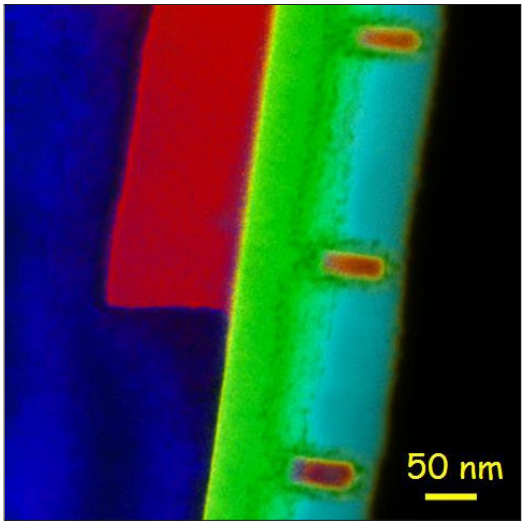

Image 5a

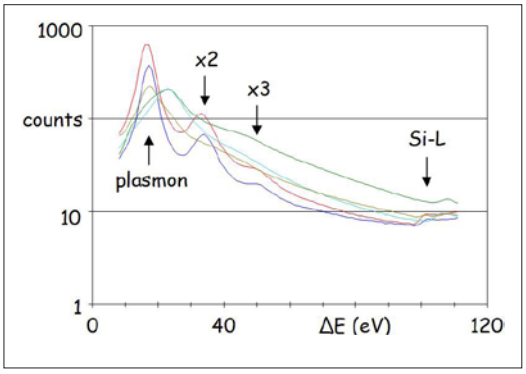

Image 5b

Figure 5. EFTEM low-loss spectral image: (a) image and (b) spectral components. See text for details.

capability when combined with tomography methods. EFTEM core-loss imaging provides phase identification based on compositional contrast, and when combined with spectral imaging (SI) methods, where a series of EFTEM images spanning a large spectral range is acquired, has been shown to provide quantitative discrimination between compositionally distinct phases. However, quantification is complicated by plural scattering, which is significant when the specimen thickness is a large fraction (>0.5) of the inelastic mean free path, which is a major limitation given the strong plasmon resonance for silicon. EFTEM low-loss SI provides a means of characterizing this plural scattering, as well as providing alternative chemical imaging contrast based on electronic structure rather than composition.

An EFTEM low-loss SI of an array of FinFET devices is shown in Fig. 5. A series of 512×512 pixel EFTEM images was acquired in the spectral range from 8 eV to 112 eV, with a 3 eV energy window and a 1 eV energy increment. This energy range spans the entire low-loss region and the Si-L2,3 edge. The image series was registered using edge-filtered cross-correlation and analyzed by linear multivariate statistical analysis, which discriminates distinct spectral regions by their spectral shapes. Regions of the specimen exhibiting distinct spectral signatures are shown in Fig. 5a, while the corresponding spectra are shown in Fig. 5b. The spectrally distinct regions comprise two pure silicon regions, corresponding generally to the silicon fins (red) and the single-crystal substrate (blue), the silicon oxide (green) and silicon oxynitride (cyan) phases, and the interface (yellow) between the electrically semiconducting and insulating regions. Note that the characteristic K edges of nitrogen and oxygen were not acquired, so that the spectral discrimination is based on plasmon resonances and the signal level and chemical shift of the Si-L edge.

Plural scattering is clearly evident from the presence of the spectral peaks at twice (2×) and three (3×) times the energy of the sharply peaked plasmon resonance in the pure silicon phases. This nonlinear response provides a challenge to quantification and tomography, but can be removed by spectral deconvolution, which is facilitated if the SI is extended on the low-energy end to profile across the zero-loss peak. The discrimination of the oxide and oxynitride phases from the silicon is remarkable, given that the anion spectral signatures were not acquired. The high-κ hafnium oxide dielectric phase is not spectrally distinguished, although this high atomic number phase is evident in the bright-field image from mass thickness contrast. The identification of a distinct interfacial component indicates that the spectral response of the interface is not a simple linear combination of those of the adjacent phases.

Collaborations

Aerospace Corporation – TEM-based chemical imaging.

International SEMATECH, SVTC Technologies – Thin oxide depth-profiling by SIMS, backside depth profiling of patterned PMOS wafers.

Freescale Semiconductor - Evaluation of stress measurements in SiGe structures by confocal Raman Microscopy

Ionoptika – Development of a C_{60}+ primary ion source for advanced semiconductor technology.

MicroFAB Inc – Advanced inkjet printing technology for deposition of trace metal standards on silicon surfaces.

Micron Semiconductor – trace organic detection.

Ultratech - Development of a Si stress reference.

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Advanced Gate Stacks Materials

Technical Contacts:
M. L. Green

Goals

The goals of this project are to develop novel, combinatorially-compatible measurement methods and metrologies that enable the microelectronics industry to select new materials more rapidly and intelligently through use of comprehensive and consistent data sets.

Customer Needs

At present, further scaling (dimensional shrinkage of integrated circuit device elements according to Moore's Law) of Si microelectronics is materials limited. For example, higher mobility substrates (e.g., Ge, GaAs, and strained Si) are needed as replacements for Si, and the traditional gate stack layers (gate dielectric and polycrystalline Si gate electrode) must be replaced with a high-κ gate dielectric and a metal gate electrode. The Si microelectronics industry, and the consumer electronics and information revolution that it fuels, is, at $750 billion, one of the largest sectors of the US (and global) economy. The development of materials with superior properties that enable device scaling and enhanced device performance are key to continued innovation in Si microelectronics.

Currently, there are no rapid measurement techniques to determine the physical and electrical properties of novel metal-oxide-semiconductor (MOS) materials; the availability of such methods would enable rapid selection and optimization of these materials and their commercialization in devices.

Key customers include Sematech, IMEC and major U.S. semiconductor manufacturers such as Intel and Micron. We are very active in promoting the use of combinatorial methodologies with these customers.

Technical Strategy

The CMOSFET device (complementary-metal-oxide-silicon-field-effect-transistor, the workhorse of advanced chips such as Pentium microprocessors), is extremely complex, and the identification of replacement materials with superior properties is difficult due to the large number of candidate materials for either gate stack or high mobility applications. Introduction of new materials is complicated by rigid requirements that they not only possess the requisite physical and electrical properties, but also be manufacturable, thermally stable during processing, and compatible with adjacent material layers. There are no rapid measurement techniques to determine the physical and electrical properties of novel CMOS materials. The availability of such methods would enable the rapid selection and commercialization of such materials. It is imperative to be able to make hundreds or thousands of measurements in parallel, since there are at least that many combinations of novel gate metal electrode/gate dielectric/substrate materials that must be assessed. Further, for some measurements, such as gate metal electrode work function, the most appropriate measurement technique is not apparent. The traditional gate stack layers (SiO_2 gate dielectric and polycrystalline Si gate electrode) in current Si microelectronic devices must be replaced with a high dielectric constant (high-κ) gate dielectric and a metal gate electrode. We will develop combinatorial methodologies to: (1) fabricate compositionally-graded thin film libraries of novel gate metal electrode-high-κ gate dielectric-substrate combinations ("gate stack" structures) ; and (2) measure the key electronic properties (e.g., work function) and thermal stability of such libraries. In addition, a nanocalorimetry method will be developed to measure thermal stability. Comprehensive data sets of electronic properties as a function of composition will be generated for materials systems identified as high priority by the microelectronics industry.

DELIVERABLES:

- Determine work functions in the TaC_xN_{1-x}/HfO_2/Si advanced CMOS gate stack - Q1/09
- Demonstration of SiO_2 thickness gradient film, by wet etching and ellipsometry, for more accurate work function determination – Q2/09
- Work function measurements in TaC_xN_{1-x}/HfO_2/Si advanced CMOS gate stack using NIST SiO_2 gradient films – Q3/09
- Electrical characterization of ternary gate dielectrics from the "higher-κ" TiO_2-HfO_2-Y_2O_3 -Al_2O_3 gate dielectric system – Q4/09

Accomplishments

We commissioned a state-of-the-art combinatorial tool capable of producing thin film libraries by reactive sputtering or pulsed laser deposition (PLD). Both chambers are equipped with multi-

ple targets, allowing for the deposition of ternary films of metals and nitrides (by sputtering) and oxides (by PLD) with sub-monolayer (0.5 nm) thickness control. The microelectronics industry has identified HfO_2, Hf-Si-O, and Hf-Si-O-N, among other high-κ gate dielectrics, as the leading candidate replacement materials for SiO_2; however, the selection of gate electrode materials to replace polysilcon is less advanced. Thus, we have focused our efforts on gate electrode materials, specifically metalloids ($Ta_{1-x}Al_xNy$ system).

We have demonstrated the efficiency of the combinatorial methodology applied to $Ta_{1-x}Al_xN_y$ alloys as metal gates on HfO_2 for CMOS applications. To the best of our knowledge, this is the first time combinatorial methodology has been applied to systematically extract Φ_m for the CMOS advanced gate stack. Figure 1 shows, using x-ray microdiffraction, that over the range of the compositional variable, x, achieved in our

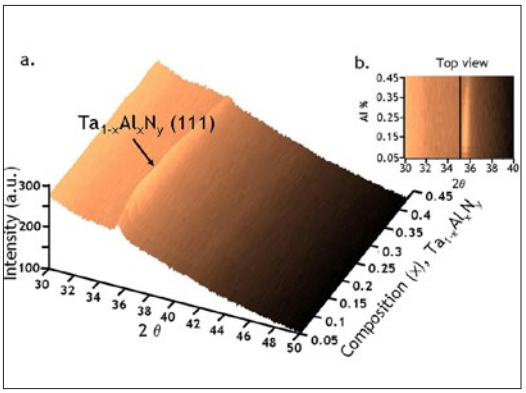

Figure 1. Characterization of the phase structure of the $Ta_{1-x}Al_xN_y$ library film. a), a 3-D plot of the $Ta_{1-x}Al_xN_y$ composition spread, as determined by scanning x-ray microdiffraction, and b) top view of the plot from 2θ = 30° to 2θ = 40°.

combinatorial library film, the metal gate electrode film appears to be a solid solution of TaN and AlN. $Ta_{1-x}Al_xN_y/HfO_2$ (3 nm) /SiO_2 (4, 5, 6, or 10) nm capacitor libraries were fabricated by reactive sputtering $Ta_{1-x}Al_xN_y$ onto HfO_2 through a shadow mask. A standard program was used to fit C-V characteristics to over 2,000 MOSCAPS to extract EOT and V_{fb}. The EOT maps indicate that only limited interaction between the gate stack layers took place below 950 °C RTA. In figure 2, Φ_m of the $Ta_{1-x}Al_xN_y$ library is shown as function of the compositional variable, x, for $0.05 \leq x \leq 0.50$, after forming gas, and 900 °C and 1000 °C RTA treatments. After 1000 °C RTA, only Φ_m for compositions ($0.30 \leq x \leq 0.50$) could

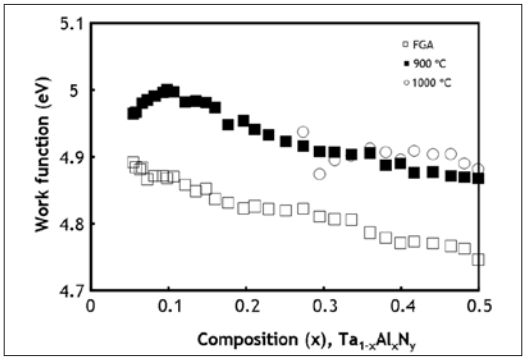

Figure 2. A plot of the extracted work functions (Φ_m) for the $Ta_{1-x}Al_xN_y$ metal gate electrode system, as a function of Al content. Φ_m were extracted after FGA, 900 °C, and 1000 °C thermal treatments. Φ_m with $x < 0.3$ after 1000°C could not be mapped due to degradation of the capacitor characteristics.

be electrically tested due to MOSCAP failures as a result of the high anneal temperature. Our results show that Φ_m can be tuned as a function of gate metal composition as well as annealing condition. The fixed oxide charges in the SiO_2/Si interfaces show reasonably small values after 900 °C anneal. We suggest that $Ta_{0.9}Al_{0.1}N_{1.24}$ has potential to replace polysilicon for PMOS applications.

Collaborations

Joint combinatorial gate stack experiments with Intel, Micron, Sematech and IMEC.

Publications

K.-S. Chang, M. L. Green, P. K. Schenck, H. M. Lane, J. Hattrick-Simpers, C. Jaye, J. Woicik, D. A. Fischer, I. Takeuchi, and S. De Gendt, *"Exploration of the Ta(C,N)$_x$/HfO$_2$ Advanced Gate Stack Using Combinatorial Methodology"*, in preparation for submission to Electron Device Letters.

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L. P. Cook, R. Cavicchi, M. L. Green, C. Montgomery, W. Egelhoff, *"Thin-Film Nanocalorimetry: A New Approach to the Evaluation of Interfacial Stability for Nanoelectronic Applications,"* Frontiers of Characterization and Metrology for Nanoelectronics, p. 151, American Institute of Physics/NIST Conference, 2007.

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Talks

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"Combinatorial study of metal gate electrodes on HfO_2 for the advanced gate stack," K.-S. Chang, Spring MRS 2008 (invited)

"Combinatorial Methodology for the Exploration of Metal Gate Electrodes on HfO_2 for the Advanced Gate Stack," K.-S. Chang, ECS Meeting, May 2008 (invited).

Advanced Plasma Process Metrology

Technical Contacts:
M. Sobolewski

"NIST is one of the leaders in plasma processing related research in the U.S. They have capability to thoroughly understand plasma behavior using a variety of diagnostics tools."

Peter Ventzek
TEL, Inc

Goals

To provide advanced measurement techniques, data, and models needed to characterize plasma etching and deposition processes important to the semiconductor industry, enabling continued progress in model-based reactor design, process development, and process control.

Customer Needs

To fabricate future generations of devices, the semiconductor industry requires improvements in plasma etching and deposition processes. Plasma processes and equipment face increasingly stringent requirements due to the need to maintain high device yields at decreasing feature sizes, the introduction of new dielectric materials, and the constant pressure to keep production efficiency high. To meet these challenges, the International Technology Roadmap for Semiconductors (ITRS, 2007 update) identifies a need for better, more predictive modeling of the impact of equipment on process results (Modeling and Simulation section, page 4 and Tables MS1, MS2a, and MS2b). To obtain more reliable predictions of the chemical, physical, and electrical properties of processing plasmas, the dependence of these properties on processing equipment, and the effect of these properties on process results, further progress in model development and validation is required. The ITRS also identifies a need for development of robust sensors and process controllers (Metrology section, Table MET1 and pages 39-41, and Modeling and Simulation section, page 7) that are able to convert large quantities of raw data into information useful for improving manufacturability and yield.

TECHNICAL STRATEGY

Our multifaceted program provides numerous outputs to assist our customers, including advanced measurement methods, high-quality experimental and fundamental data, and reliable, well-tested models of plasma behavior.

First, we develop and evaluate a variety of *measurement techniques* that provide industry and academia with methods to characterize the chemical, physical, and electrical properties of plasmas. The techniques we develop include improved laboratory diagnostic measurements for use in research and development, as well as more robust, non-perturbing measurements for use in process monitoring and control in manufacturing applications.

In addition to measurement techniques, we also provide *data* necessary for gaining an understanding of complex plasma properties and for testing and validating plasma models. The data help semiconductor manufacturers and plasma equipment manufacturers to better understand and control existing processes and tools and help them to develop new ones. The experimental data we provide are measured under well-defined conditions in highly characterized standard plasma reactors. Our reactors include capacitively coupled cells as well as inductively coupled, high-density plasma reactors, one of which is shown in Fig. 1.

Finally, we are engaged in the development and validation of plasma *models*. Such efforts concentrate on modeling of plasma sheaths, the thin regions at the boundary of the plasma. Sheaths play a dominant role in determining discharge electrical properties and the properties of the highly energetic ions that are necessary for plasma etching. More accurate sheath models are needed to better predict and optimize discharge electrical characteristics and ion kinetic energies. Sheath models are also used to develop new types of process monitoring techniques based on radio-frequency electrical measurements.

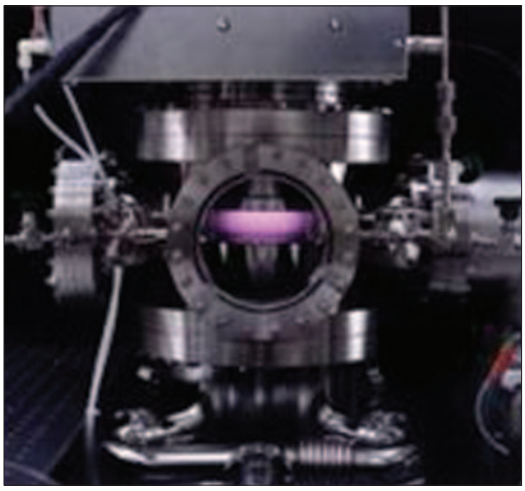

Figure 1. One of the inductively coupled plasma reactors in our laboratory.

Our ongoing and planned efforts focus on measurement, data, and modeling challenges in the following specific areas:

"The NIST plasma process metrology group has helped us to understand the fundamental physical and chemical processes that are important to electronics materials and semiconductor processing industries."

Bing Ji,
Air Products and
Chemicals, Inc.

1. Recently, several new kinds of wafer-based sensor technologies have been developed and commercialized. These technologies allow the integration onto test wafers of sensors that can measure important plasma and process parameters such as ion flux, ion energy, and wafer temperature. Integration of multiple sensors allows measurement of the uniformity of these parameters across the wafer area. Such wafer-based sensors are playing an increasingly important role in the development and characterization of plasma processes and equipment. Often, however, the principles of operation of these sensors are not completely understood. Consequently, the reproducibility and accuracy of sensor measurements may be in doubt. A better fundamental understanding of these sensors, together with more rigorous, quantitative analysis of errors that may be present, could lead to improvements in sensor design and could greatly increase the use of such sensors in industry. In previous years, in collaboration with sensor manufacturers, we have investigated the operation of wafer-based sensors for temperature and ion flux. Our present efforts in this area are focused on the validation of on-wafer measurements of ion energy distributions. We will compare a commercial, wafer-based sensor for ion energy to independent measurement techniques of known accuracy that we have developed in previous years. The comparisons will allow us to identify and quantify the sources of uncertainty in the commercial, wafer-based sensor.

DELIVERABLES:

Evaluate the accuracy of wafer-based sensors for ion energy in rf-biased, inductively coupled plasma reactor. 3Q 2009

2. We are also engaged in a fundamental investigation of electrical measurements for detection of plasma etching endpoints. In plasma etching, one requires an endpoint signal that indicates the layer to be etched is fully consumed, so that the etch can be stopped before it proceeds to etch or damage underlying layers. Endpoint detection is typically accomplished with optical techniques such as optical emission spectroscopy. Electrical measurements, however, are less expensive to implement and may have other benefits when used in place of or in combination with optical emission. Unfortunately, the origins of the electrical changes that occur at endpoint are not well understood. Consequently, it is difficult to determine which of the many possible electrical signals that could be used for endpoint detection are the most reliable, and how reliable they are. To answer these questions, we are engaged in experiments and numerical modeling (as described below) to determine the fundamental origin of the electrical changes observed at and near endpoint. The work provides recommendations for the plasma etching industry that identify, based on fundamental reasons, which electrical signals are the most reliable for endpoint detection.

DELIVERABLES:

Complete studies determining the origin of electrical changes observed during etching and report the findings in an archival publication. 3Q 2009

Complete evaluations of electrical methods for endpoint detection and report them in an archival publication. 3Q 2009

3. In previous years, an electrical measurement technique had been developed at NIST for in-situ, noninvasive monitoring of the ion current and ion energy at the surface of actual production wafers during plasma processing. Numerous tests and demonstrations of the technique (described below) have been successfully performed. The technology used by the technique can be considered to be mature, and its development complete. One source of uncertainty in the technique, ion-induced emission of electrons from wafer surfaces, can now be quantified more precisely than was possible previously, thanks to our recent work on electrical detection of plasma etching endpoints. The endpoint studies provide accurate estimates of emission yields from plasma-exposed silicon and silicon dioxide surfaces. Measured values of emission yield, and a rigorous analysis of the effect of emission yield on the uncertainty of the noninvasive monitoring technique, will be provided in a publication, along with other results of the endpoint studies.

DELIVERABLES:

Report electron emission yields for plasma-exposed silicon and silicon dioxide, and quantify the resulting uncertainties in ion current and ion energy obtained from the noninvasive monitoring technique. 3Q 2009

ACCOMPLISHMENTS

We have recently completed a fundamental investigation of electrical detection of plasma etching endpoints, using experiments as well as numerical modeling. The experiments were performed during fluorocarbon plasma etches of silicon dioxide films on silicon substrates in an rf-biased, inductively coupled plasma reactor. A complete

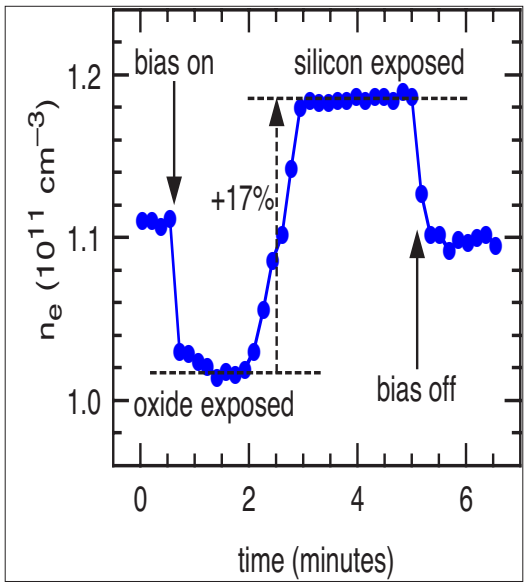

Figure 2. Variation of plasma electron density with time during etching of a thermally grown silicon dioxide film of thickness 600 nm on a silicon substrate, in a 50% Ar, 50% CF_4 plasma at a pressure of 1.3 Pa (10 mTorr), a source power of 220 W, and a bias frequency of 10 MHz."

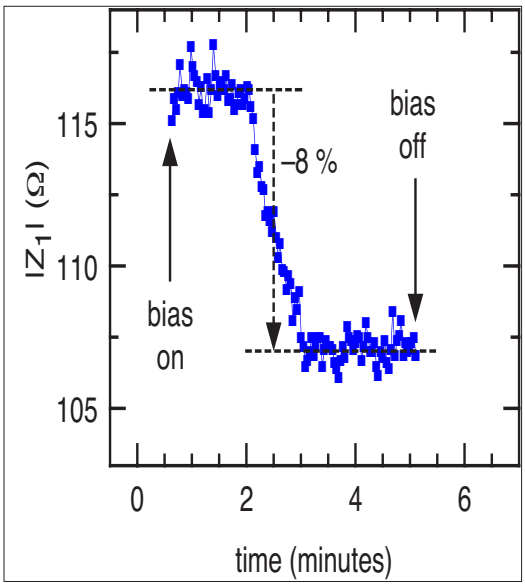

Figure 3. The magnitude of the fundamental (10 MHz) rf bias impedance during the same etch as Fig. 2

set of electrical parameters, for the rf bias as well as the inductive source, were measured during etching. Simultaneously, the electron density in the plasma was measured using a wave cutoff probe. This probe, developed in collaboration with KRISS, the Korea Research Institute of Standards and Science, allows small changes in electron density to be measured with good accuracy and precision, on a time scale of a few seconds. Unlike Langmuir probe measurements, which are commonly used for measuring electron density, cutoff measurements do not suffer from problems with rf compensation or deposition of insulator layers on probe surfaces. When an etch breaks through the oxide and exposes the underlying silicon, changes in the gas-phase densities of etch products and reactants cause the electron density to increase (Fig. 2). This increase, and an accompanying increase in ion current, has a large effect on the measured electrical signals, such as the rf bias fundamental impedance (Fig. 3). Using a numerical model and measurements made at varying bias frequencies, the effect on the electrical signals of changes in electron density can be distinguished from smaller effects caused by other parameters that vary at endpoint. These include the electron temperature, average ion mass, and the ion-induced emission of electrons from the wafer surface. Together, the measurements and models provide, for the first time, a full determination of the fundamental origin of the electrical changes observed at and near endpoint. The work provides recommendations for the plasma etching industry that identify, based on fundamental reasons, which electrical signals are the most reliable for endpoint detection.

We have completed the development and testing of an electrical measurement technique for in-situ, noninvasive monitoring of the ion current and ion energy at the surface of actual production wafers during plasma processing. This technique relies on noninvasive, non-perturbing measurements of the radio-frequency (rf) current and voltage applied to plasma reactors. The rf measurements are compatible with commercial reactors and they contain valuable information about the current and energy of the ions that bombard wafers during processing. Values for the total ion current and ion energies are obtained by analyzing the current and voltage signals using electrical models of the plasma and its sheaths. To validate the technique, experiments in an rf-biased, inductively coupled plasma reactor have been performed both with and without silicon wafers loaded in the reactor, on a metallic wafer chuck as well as an insulating chuck that is similar to commercial electrostatic chucks. Plasma potentials, sheath voltages, total ion flux, and ion energy distributions obtained from the rf measurements have been compared against

independent measurements and shown to be in good agreement. The technique has been used to monitor long-term drift in ion energy and total ion flux. We have also monitored the more rapid changes that occur when the pressure, power, and gas flow are perturbed in ways that mimic equipment faults (see Figs. 4 and 5). Smaller changes in ion energy and total ion flux that occur during plasma etch processes have also been monitored. Fast algorithms have been developed, in which all model computations are done beforehand, rather than in real-time during processing. This improvement reduces the cycle time of the measurements far below 1 s, making it suitable for use even in processes that are very short or in close-loop control schemes that require fast feedback. As a result of these tests and demonstrations, the monitoring technology can be considered to be mature, and its development complete. Opportunities may exist for NIST to collaborate with industrial partners on future applications of the monitoring technique in industry.

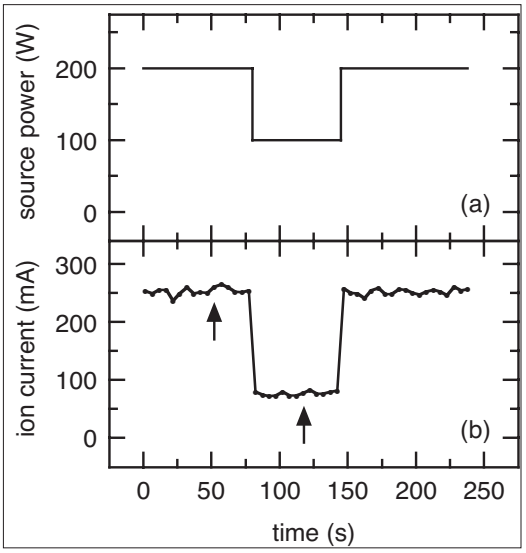

Figure 4. Effect of (a) variations in inductive source power on (b) total ion current at the wafer surface, as measured by the noninvasive technique, for a 50 % Ar, 50 % CF_4 plasma at a pressure of 1.3 Pa (10 mTorr), a bias frequency of 10 MHz, and a bias power of 10 W.

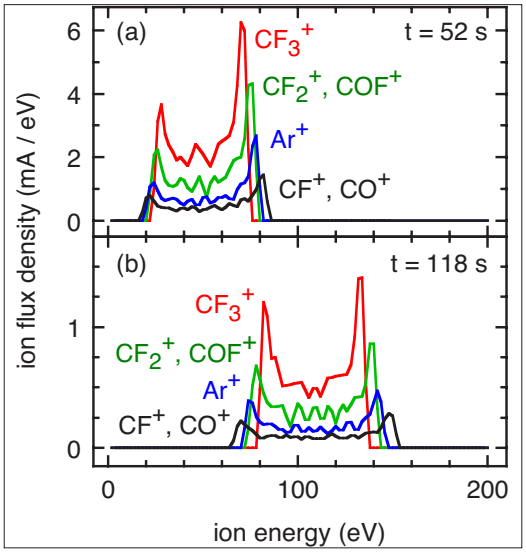

Figure 5. Ion energy distributions from the noninvasive monitoring technique, obtained during the experiment shown in Fig. 2, at (a) 52 s and (b) 118 s after the start of the experiment. The distribution for CF_2^+ and COF^+ has been expanded vertically by a factor of 3, for clarity.

Fundamental data continue to be distributed to plasma modelers throughout industry and academia via the Web-based NIST "Electron Interactions with Plasma Processing Gases" database. This Web site has experienced tens of thousands of hits throughout its history.

RECENT PUBLICATIONS

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for ULSI Technology, (American Institute of Physics, Melville, NY, 2005) pp. 333-337.

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Modeling of Graphene: Beyond-CMOS DevicesFraction

Technical Contacts:
Eric Cockayne

Goals

The goals of this project are to develop computational methods and software to enable rapid characterization of the structure and quality of graphene, thereby allowing the microelectronics industry to more rapidly realize the potential of graphene as a material for advanced device applications.

CUSTOMER NEEDS

Graphene, a single two-dimensional layer of graphite (carbon, C), has remarkable electronic properties such as high carrier mobility and a novel "pseudospin" degree of freedom. The ITRS Emerging Device Materials Working Group has recently "promoted" graphene to "a material of great interest" for beyond-CMOS technologies, thus targeting it for an enhanced level of funding. Many challenges must be solved, however, before graphene can be commercialized. One major challenge is finding a method for rapid, reproducible growth of high quality graphene. Methods under investigation include the thermal desorption of Si from SiC surfaces; thermal treatment of metal-rich metal carbides with a metal surface commensurate with graphene, and solution-based organic chemical processing. Using the case of graphene growth from SiC as an example, the samples obtained have varying numbers of graphene layers, and various defects within the layers, which can potentially affect device performance. Some graphene defects might be desirable, for example, to control electronic states associated with edges in graphene ribbons, or to bond graphene to a dielectric layers in a pseudospin graphene/dielectric/graphene multilayer structure.

At the recent 2009 Frontiers of Characterization and Metrology for Nanoelectronics (Albany, 5/09) Conference, several relevant measurement needs associated with graphene quality were repeatedly identified: i) measurement of the number of graphene layers present in a sample, ii) measurement of the misorientation between successive graphene layers, iii) measurement of the fluctuations of a graphene structure from ideal planarity, and iv) characterization of defects in graphene. As the performance of graphene-based devices depend very sensitively on their structure, atomic level calculations and models are needed to predict device performance. Not only can modeling lead to the level of understanding necessary for proper device performance, but also it can cut development costs by eliminating inappropriate materials and process schemes.

TECHNICAL STRATEGY

To characterize the structure, growth, and measurable properties of graphene and graphene-dielectric interfaces, this project relies on a range of theoretical and computational methods from ab-initio electronic structure calculations to large scale molecular dynamics simulations. Defects are studied using density functional theory, by relaxing atomic positions of graphene structures with variously introduced defects (e.g., adatom, substitution, vacancies, etc.). The electronic structures (density of states and nature of states at the Fermi level) are simultaneously calculated. By projecting the electronic density of states both spatially and into an energy range, it is possible to simulate scanning electron microscope (SEM)

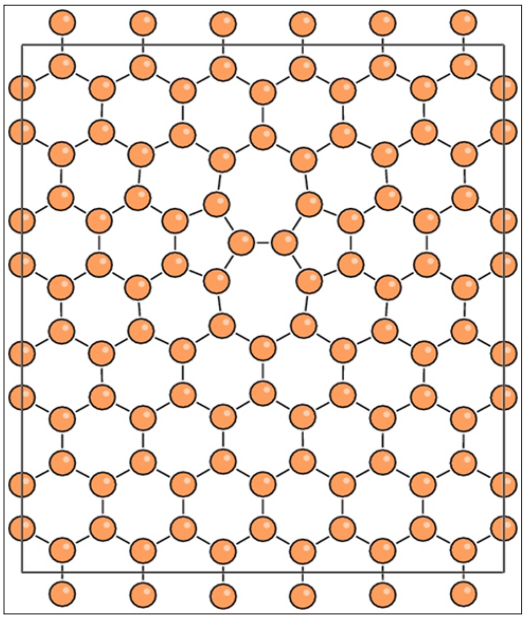


Figure 1. Stone-Wales defect in graphene, where two pentagons and two heptagons meet (top center).

topograhic images. This is important because symmetry alone is not sufficient to identify a defect from the images; electronic information, and separating electronic information from pure topographic effects is crucial. Additional measurement needs will be addressed by investigating the effects of graphene bilayer relative orientations on their transport properties, and by calculating theoretical Raman spectra for defected graphene structures.

In a similar way, graphene/dielectric interfaces can be modeled, and the effects of graphene defects on the graphene/dielectric interface can

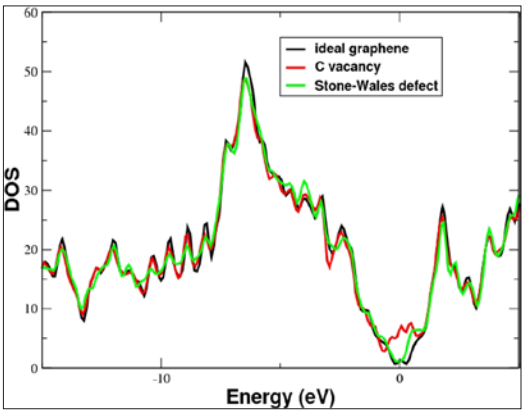


Figure 2. Calculated electronic density of states for ideal graphene, graphene with a carbon vacancy, and graphene with a Stone-Wales defect.

be compared to results for perfect graphene. The electronic structure will be determined in each case, and the results will be used as inputs into models for the pseudospintronic states of a graphene bilayer, with the goal of finding a graphene/high-κ dielectric interface suitable for such devices.

Further, experiments have demonstrated that whereas graphene multilayers (technically not graphene at all, but graphite) may result from thermal decomposition of SiC substrate surfaces, it is not possible to consistently grow large areas that comprise only a single layer. Also, the growth process is very much influenced by whether the decomposing SiC surface was Si- or C-terminated. The effects of temperature, surface termination, and surface misorientation on the formation of graphene by SiC decomposition will be modeled using molecular dynamics, with the aim of determining conditions favorable for the growth of a large area single monolayer. This is a challenging goal, as it will require the creation of appropriate interatomic potentials for a system with two different atomic species that can be bonded in both 4-fold and 3-fold arrangements.

DELIVERABLES

- Calculate local atomic and electronic structure for various defects in graphene (Q1 09)
- Run test molecular dynamic simulations on Si- and C-terminated SiC surfaces (Q2 09)
- Calculate relaxed interfacial structures of graphene/SiO_2, graphene/Al_2O_3, and graphene/HfO_2. Perform these calculations for both single and bilayer graphene, and with and without defects (Q3 09)
- Use computation to predict effects of defects in single and bilayer graphene on Raman spectra. (Q4 09)

ACCOMPLISHMENTS

The following defects in graphene have been studied: a vacancy, a Stone-Wales defect (Fig.1), a grain boundary, a C-Si-C intrabond, a Si for C substitution, and a Mo adatom. The defects involving Si were chosen due to the likelihood of incomplete Si burnoff in the fabrication of graphene from SiC, and the metal adatom was chosen to model a particular high symmetry defect observed in experimental SEM images.

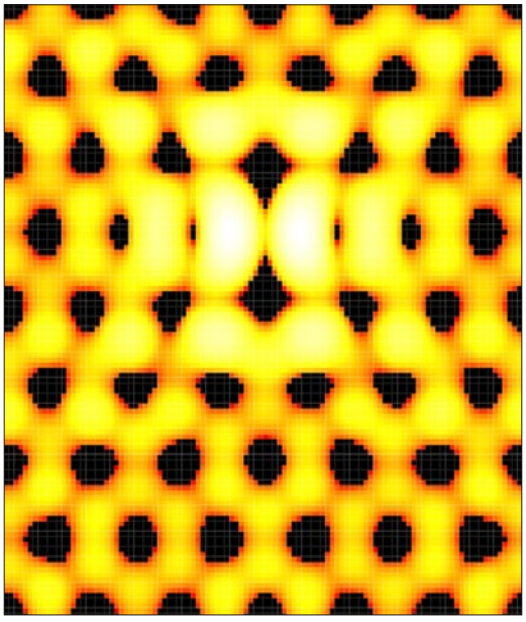


Figure 3. Simulated SEM topographic image of a Stone-Wales defect in graphene, showing two-fold symmetry similar to that for some experimentally observed defects.

We calculate that the defects are energetically costly: at room temperature, for example, vacancy creation is 8.4 eV, and a Stone-Wales defect 5.1 eV. Calculated electronic density of states (Fig. 2) show in general that defects that maintain the 3-fold coordination of every carbon atom tend to maintain a low density of states near the Dirac point (the minimum near zero energy in Fig. 2), while defects that break bonding, such as a carbon vacancy, tend to exhibit significant density of states at the Dirac point.

Finally, topographic SEM images were simulated for all of the defects studied, as a function of simulated probe tip bias voltage. The simulated images (see Fig. 3) show strong similarities to those observed experimentally by Rutter et al. [Science 317, 219 (2007)], but a definitive assignment will require more refined calculations.

COLLABORATORS

Dr. K.J. Cho, U. Texas Dallas

Drs. J. Stroscio and G. Rutter, NIST

TALKS:

Eric Cockayne, Gregory M. Rutter, and Joseph A. Stroscio, "Density Functional Theory Studies of Defects in Graphene", 2009 Frontiers of Characterization and Metrology for Nanoelectronics Conference, Albany, NY, May 2009.

Stress Mapping using Confocal Raman Microscopy and Electron Back-Scatter Diffraction

Technical Contacts:
Robert F. Cook

Goals

Develop the measurement techniques and standards for quantitative nano-scale determination of deformation, strain, and stress that will enable "stress engineering" of microelectronic and microelectromechanical devices.

Customer Needs

Many advanced industries require accurate and precise measurements of the state of deformation, or of strain or stress, in materials in order to improve or control device performance. For example the microelectromechanical systems (MEMS) industry requires knowledge of stress in components in order to optimize the sensitivity of pressure sensors, the output power of energy harvesters, and the reliability of moving components. The semiconductor microelectronics industry has implemented stress-engineered channel structures with increased carrier mobility in field-effect transistors, thereby obviating the need for costly development of new materials sets to improve device performance.

Stress engineering of channels was introduced at the 90 nm semiconductor technology node and is expected to play an increasing role in enhancing transistor performance out to the 22 nm node. The optoelectronics industry takes advantage of substrate effects on photonic quantum-well structures to generate differences in strain states and thus changes in the output color and lifetime of visible light-emitting and laser diodes. All of these industries use many different methods to measure deformation and of strain or stress, with little to no reconciliation between measurement methods, and no easy way of verifying the accuracy of measurements on components either on the manufacturing line or in development laboratories.

Technical Strategy

This project will develop measurement methods and standards to enable deformation, strain, and stress measurements to be performed at the nano-scale. Attention will focus on developing techniques for a range of instruments that could be used to make such measurements in the MEMS and microelectronics industries and on obtaining agreement between such instruments and measurements. A particular focus will be the development of strain measurements using electron back scatter diffraction (EBSD) measurements in the scanning electron microscope and stress measurements inferred from shifts or broadening of peaks in Raman spectroscopy using confocal Raman microscopy (CRM).

Mapping of strain and stress distributions is a goal for both techniques and the techniques are complementary: EBSD is surface-localized with about 10 nm (lateral) spatial resolution and requires ultra-high vacuum; CRM provides depth sampling with about 100 nm spatial resolution and operates under ambient conditions. Both techniques have better than 10^{-4} strain resolution (20 MPa stress in Si). These capabilities are unique to NIST. In addition, a reference material (RM) will be developed based on these and other measurements. Specifically, the RM will allow calibration of instruments that infer film stress from wafer curvature measurements, strain from EBSD measurements or X-ray diffraction (XRD) measurements, or CRM measurements. The RM will be based on the reaction stresses generated in a strain mismatched Si(1−x)Gex epitaxial layer deposited on Si substrates. The target composition of the Si(1−x)Gex layer will be x 0.2 and the target thickness will be less than 200 nm, leading to 1 GPa stress in the layer and < 10 MPa stress in a 700 μm thick Si substrate. Such a film will exhibit great temporal stability as the film thickness is less than that required to initiate misfit dislocations.

DELIVERABLES

- Develop EBSD and CRM strain measurement techniques for SiGe epitaxial layers. 4Q2008
- Correlate EBSD strain measurement with CRM measurements obtained using 405 nm excitation. 1Q2009
- Develop first prototype of CRM stress measurement system for 200 mm wafers. 2Q2009
- Develop polarized CRM method to determine full stress tensor and validate with EBSD measurements. 3Q2009
- Complete feasibility study of SiGe structure for deformation, strain, and stress standard. 3Q2009

Accomplishments

Quantitative agreement was demonstrated between EBSD and CRM stress measurements on a test vehicle with a simple stress distribution: a linear wedge indentation in Si. A rendered CRM stress map of the indentation is shown in Fig. 1 below. Near the center of the indentation, the deformation state is almost-pure compressive plane-strain and near the ends of the indentation tensile stresses are associated with crack tips.

The simple deformation state enables CRM measurements to be interpreted simply as uniaxial stress and thus compared directly with EBSD measurements. CRM line scans across the indentation using different laser excitation wavelengths enable stress measurements that sample different information volumes—smaller

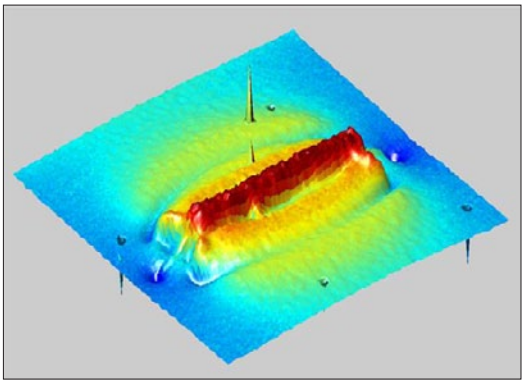


Figure 1. Confocal Raman microscopy stress map of a 20 μm long wedge indentation in Si. Red indicates compression and blue indicates tension.

wavelength excitation provides greater surface sensitivity. Such scans are shown in Fig. 2 below and compared with a similar EBSD scan. The agreement between the σxx stress measurements for the most surface sensitive excitation (488 nm) with the EBSD is obvious and is the first such experimental demonstration of the agreement between these techniques and was published in Ref. 1 below. Measurements with the least surface sensitive excitation (633 nm) did not agree with the EBSD measurements near the indentation, and in fact suggests detection of sub-surface cracking.

Additional experiments using atomic force microscopy to measure the surface topography adjacent to the indentation showed agreement with EBSD measurements of local rotation, also an experimental first. An even more surface sensitive excitation source (405 nm laser)

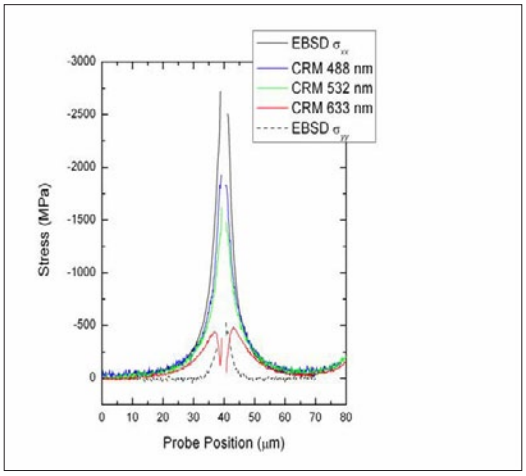


Figure 2. Comparison of stress measurements by confocal Raman microscopy and electron back scatter diffraction adjacent to a wedge indentation in Si.

has been implemented with all-new dedicated CRM optics.

Quantitative cross-platform agreement between EBSD, CRM, curvature, and XRD measurements has been demonstrated on a SiGe-Si blanket thin-film test structure in both wafer and die form. Such agreement demonstrates that the structure is suitable as an RM, and prototype SiGe-Si and SiO_2-Si wafers have been fabricated for RM development. The curvature measurements are performed using the Ultratech coherent gradient spectroscopy technique and RM development is in collaboration with Ultratech.

EBSD and CRM techniques have been applied to SiGe and W test structures supplied by Sematech and Freescale Semiconductor to assess the ability of methods to measure the stress states of patterned structures with complex deformation states. Agreement between the two techniques is more limited in these cases, and the measurements indicate the necessity for a full tensor analytical framework for measurement interpretation. Such a framework is in development, along with a specially-designed fixture for EBSD and CRM mapping of loaded test vehicles with known complex stress states.

Collaborations

Joint wafer- and die-scale deformation, strain, and stress standards development with Ultratech. Joint strain and stress mapping experiments on device test structures with Sematech and Freescale Semiconductor.

Recent Publications

1. *"Comparison of Nanoscale Measurements of Strain and Stress using Electron Back Scattered Diffraction and Confocal Raman Microscopy,"* M.D. Vaudin, Y.B. Gerbig, S.J. Stranick, and R.F. Cook, Appl. Phys. Letters 93 (2008) 193116.

2. *"Effect of crystallographic orientation on phase transformations during indentation of silicon,"* Y.B Gerbig, S.J. Stranick, D.J. Morris, M.D. Vaudin, and R.F. Cook, J. Mater. Res., 24 (2009) 1172-1183.

Talks

1. *"Measuring Strain at the 10−4 Level with Great Spatial Resolution,"* M.D. Vaudin, S.J. Stranick, Y.B. Gerbig, R F. Cook, MRS Fall Meeting, Boston, MA, December, 2008

2. *"Stress imaging of deformation and crack defects in silicon by confocal Raman spectroscopy"*,Y.B. Gerbig, R.F. Cook, M.D. Vaudin, J. Schoenmaker, and S.J. Stranick, MRS Fall Meeting, Boston, MA, December, 2008

3. *"Deformation, strain, and stress mapping with nanoscale spatial resolution using diffraction, spectroscopy, and scanned probe microscopy,"* R.P. Koseski, M.D. Vaudin, S.J. Stranick, G. Stan, and R.F. Cook, MRS Spring Meeting, San Francisco, CA, April, 2009

4. *"Development of Wafer- and Die-Scale Standards for Deformation, Strain, and Stress,"* R.F. Cook, S.J. Stranick, M.D. Vaudin, and D.M. Owen, MRS Spring Meeting, San Francisco, CA, April, 2009; also at Ultratech, April 2009.

Interconnect and Packaging Metrology Program

Advances in interconnect and packaging technologies have introduced rapid successions of new materials and processes. A major new technology thrust over the past several years is the move to three dimensional integration. Environmental pressures have led to the reduction and elimination of lead in solder used for attaching chips to packages and packages to circuit boards. The overall task of this program is to provide critical metrology and methodology for mechanical, chemical, metallurgical, electrical, thermal, and reliability evaluations of interconnect and packaging technologies.

The function of packaging is to connect the integrated circuit to the system or subsystem platform, such as circuit board, and to protect the integrated circuit from the environment. The increasing number of input/output (I/O) on circuits with vastly larger scale of integration is forcing ever smaller I/O pitches, the stacking of chips with via hole interconnect, the use of flip chip bonding, and the use of intermediary platforms called interposers. The integration of sensors and actuators onto integrated circuits through MEMS technology and the increasing use of low cost integrated circuits in harsh environments is increasing the complexity of the packaging task. Environmental concerns are forcing the need for development of reliable lead-free solder and other low environmental impact packaging materials.

System reliability requirements demand modeling, testing methods, and failure analysis of the integrated circuits before and after packaging. Metrology is a significant component of reliability evaluation.

Atomic Layer Deposition – Process Models and Metrology

Technical Contacts:
J. E. Maslar
D. R. Burgess, Jr.

Goals

Develop validated, predictive process models and in situ metrologies for atomic layer deposition processes.

Customer Needs

Atomic layer deposition (ALD) is increasingly being utilized as a method of depositing the thin (nanometer-scale), conformal layers required for many microelectronics applications, including high-κ gate dielectric layers and DRAM dielectric layers. However, significant developmental issues remain for many of these applications. One potential solution to some ALD developmental issues is technology computer-aided design (TCAD). TCAD has been identified in the *International Technology Roadmap for Semiconductors (ITRS) 2007 Edition as "one of the few enabling methodologies that can reduce development cycle times and costs."*[ITRS 2007 Edition, Modeling and Simulation, page 1] A TCAD topical area identified in the ITRS 2007 Edition is *"Equipment/feature scale modeling—hierarchy of models which allows the simulation of the local influence of the equipment (except lithography) on each point on the wafer, starting from the equipment geometry and settings."*[ITRS 2007 Edition, Modeling and Simulation, page 1] A difficult challenge related to this topical area is *"Integrated modeling of equipment, materials, feature scale processes and influence on devices, including variability"*[ITRS 2008 Update, Modeling and Simulation, Table MS1, page 56] with associated issues including *"Fundamental physical data (e.g., rate constants, cross sections, surface chemistry for ultra low-k (ULK), photoresists and high-κ metal gate); reaction mechanisms (reaction paths and (by-products, rates ...), and simplified but physical models for complex chemistry and plasma reaction"* and ALD deposition modeling.[ITRS 2008 Update, Modeling and Simulation, Table MS1, page 56] In addition, the 2007 ITRS notes that *"a key difficult challenge across all modeling areas is that of experimental validation."*[ITRS 2007 Edition, Modeling and Simulation, page 2] Further, with respect to experimental validation, *"One of the major efforts required for better model validation is sensor development and metrology, especially for models predicting the fabrication and behavior of ultra-thin films and ultra-fine structures."[ITRS 2007 Edition, Modeling and Simulation, page 7]* This project is an attempt to assist in solving some ALD developmental issues by developing validated, predictive process models and in situ metrologies for ALD processes.

Technical Strategy

This project involves two general directions of investigation: development of in situ metrologies sensitive to ALD chemistry and development of ALD chemical reaction mechanisms. These two directions are seen as mutually-supportive. It is expected that experimental results that elucidate ALD chemistry will aid in chemical mechanism development and ultimately in process model validation. Further, it is expected that important reaction species will be identified as the understanding of a particular ALD reaction improves, thus facilitating the design of improved process metrologies. While these two directions will be closely coupled for development of a specific ALD chemical reaction mechanism, it will not preclude exploration of non-mutually-supporting aspects of the metrology development and model development directions. For example, fundamental thermochemical and chemical kinetics properties of numerous organometallic compounds potentially suitable for ALD are under investigation. However, it would not be feasible to simultaneously provide experimentally validated ALD process models for all compounds.

Various in situ diagnostics are being evaluated for use in characterizing gas phase and/or surface processes. Gas phase diagnostic development has focused on metrologies that are sensitive to gas phase processes that can be ultimately related to film properties. Such diagnostics can be used to help optimize gas injection conditions rather than simply monitor precursor delivery. ALD process models are being developed by incorporating the detailed chemical reaction mechanisms developed in the course of this project into commercially available computational fluid dynamics (CFD) codes that simulate the gas flow and temperature fields

in an ALD reactor. Experimental validation of the overall process model is accomplished by modeling the performance of a custom-built, research-grade ALD reactor with optimized optical accessibility and benchmarking the numerical results with experimental data. HfO_2 ALD using tetrakis(ethylmethylamino) hafnium (TEMAH) and water has been selected as the chemical system for primary investigation.

1. A number of diagnostics are being evaluated for sensitivity to ALD chemistry and integration into deposition systems. Mass spectrometry and optical spectroscopic techniques are of particular interest because of their proven potential for in situ monitoring. While sensors that are sensitive to gas phase species, e.g., mass spectrometry and semiconductor laser-based spectroscopic techniques, are more straightforward to integrate into commercial reactors (e.g., in the gas exhaust line), these techniques are only sensitive to volatile and relatively stable species. Hence, it is sometimes difficult to relate the species detected with such techniques to the mechanisms of interest on the growth surface. Hence, both gas-phase-sensitive and surface-sensitive techniques are being evaluated to probe ALD chemistry. The suitability of Fourier-Transform infrared (FTIR) spectroscopy and laser-based spectroscopic techniques for probing ALD surface processes under actual deposition conditions is being investigated. In situ, time-resolved reflection-absorption IR spectroscopy (RAIRS) has been demonstrated to be useful to probe surfaces during ALD. In addition, the suitability of mass spectrometry, FTIR spectroscopy, and semiconductor laser-based spectroscopic techniques for probing gas phase ALD processes and how best to relate gas phase species to important surface processes is being investigated. Measurements are preformed in a custom-built, research-grade ALD reactor with optimized accessibility for the various gas-phase-sensitive and surface-sensitive techniques.

DELIVERABLES:

- Evaluation of quantum cascade laser-based measurements for measuring TEMAH concentrations during ALD. 3Q 2009
- Evaluation of quantum cascade laser-based measurements for measuring surface amino-group functionalization during ALD. 4Q 2009
- Evaluation of time-resolved, in situ RAIRS measurements for probing HfO_2 ALD surface processes. 4Q 2009
- Evaluation of time-resolved, in situ diode laser absorption spectroscopy for measurements of water vapor during ALD processes. Ongoing
- Evaluation of mass spectrometry measurements for probing HfO_2 ALD gas phase processes. Ongoing

2. The calculation, estimation, and dissemination of fundamental thermochemical and chemical kinetic properties of organometallic compounds with potential application to ALD are an integral aspect of this project. The thermochemical properties and reaction kinetics of most organometallic precursors employed in ALD are poorly characterized. This project obtains these properties through theoretical estimates, comparison with available experimental data, and modeling. This involves compiling the available thermochemical and chemical kinetics data for organometallic precursors and related compounds. These data are supplemented with predictions from quantum calculations of molecular structures, spectroscopic properties, and thermodynamic functions. These quantities are then utilized to develop detailed chemical kinetics models for the decomposition of organometallic precursors and deposition processes leading to thin film growth.

DELIVERABLES:

- Compute heats of reactions and barriers to reaction steps leading to carbon and nitrogen impurity incorporation. 4Q2009
- Incorporate mechanistic steps into the ALD chemical reaction mechanism model for carbon and nitrogen impurity incorporation. 4Q2009

3. An effort is also being made to investigate the relationship between ALD reactor conditions and concomitant HfO_2 film properties. This relationship is being investigated by correlating the results of a variety of ex situ film characterization measurements to reactor conditions as determined by in situ measurements and numerical modeling of the temperature and flow fields in the reactor. In situ measurement techniques include those techniques being developed for model validation. Ex situ measurement techniques include vacuum ultraviolet spectroscopic ellipsometry (VUV-SE), FTIR spectroscopy, X-ray photoelectron spectroscopy (XPS), X-ray diffractometry, atomic force microscopy, ultraviolet Raman spectroscopy, and various electrical measurements. The data provided by these measurements, spatially resolved when possible, include such film characteristics as thickness, stoichiometry, HfO_2 phases present, degree and type of impurity incorporation, leakage current,

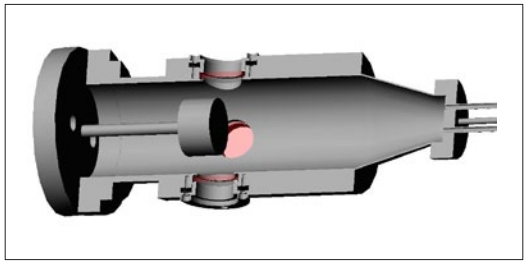


Figure 1. A schematic of the cross section of the reactor as configured with optical windows.

and dielectric constant.

DELIVERABLES:

- Investigate the relationship between HfO_2 ALD process parameters, reactor gas flow and temperature fields, gas phase species identities and concentrations, and resulting ALD film characteristics. Ongoing

Accomplishments

■ ALD Reactor Design — An ALD reactor with diagnostic access near the wafer surface that exhibits operational parameters approximating some industrial single wafer reactors was designed and fabricated. Gas flow in the reactor near the wafer is laminar and parallel to the wafer surface normal with four diagnostic ports oriented perpendicular to the wafer surface normal, as shown in Fig. 1.

■ Diagnostic access does not significantly perturb gas flow, especially near the wafer surface. Using this reactor, reproducible, high-quality HfO_2 films can be deposited at the same time that in situ measurements are being performed. This reactor is being used to provide data to validate process models and develop metrologies.

■ Hafnium Oxide Film Deposition — ALD HfO_2 films are being deposited under a variety of process conditions using tetrakis(ethylmethylamino) hafnium (TEMAH) and water. Films have been characterized with a number of techniques, including VUV-SE, XPS, FTIR, Raman spectroscopy, X-ray diffractometry, atomic force microscopy, and current-voltage measurements. Ex situ measurement results indicate that this reactor design can be used to reproducibly grow microelectronics-quality HfO_2 films.

■ *In-Situ* Gas Phase Measurements — *In-situ* gas phase FTIR measurements have been performed during HfO_2 film deposition and have been shown to be sensitive to the major gas-phase deposition reactants, TEMAH and water, and products, methylethylamine.

■ In addition, in-situ, time-resolved semiconductor laser-based absorption measurements have been developed to detect all gas phase reactants and products. Water vapor absorption was measured near-IR spectral region using a distributed feedback diode laser and wavelength modulation spectroscopy, as shown in Fig. 2

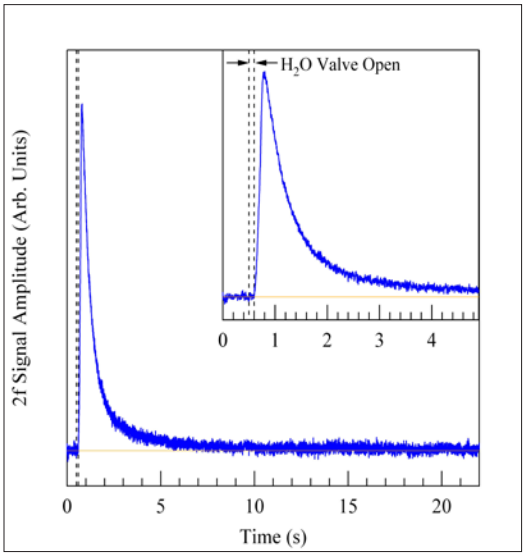


Figure 2. Near-IR diode laser-based water vapor absorption measurements.

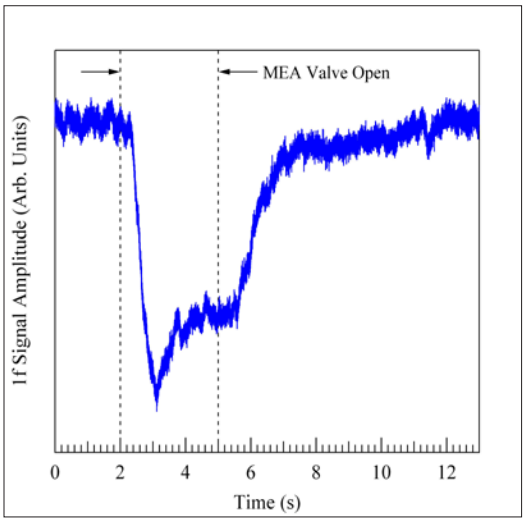


Figure 3. Near-IR diode laser-based methylethylamine absorption measurements.

Methylethylamine was measured in the in the near-IR spectral region using a distributed feedback diode laser and amplitude modulation spectroscopy, as shown in Fig. 3

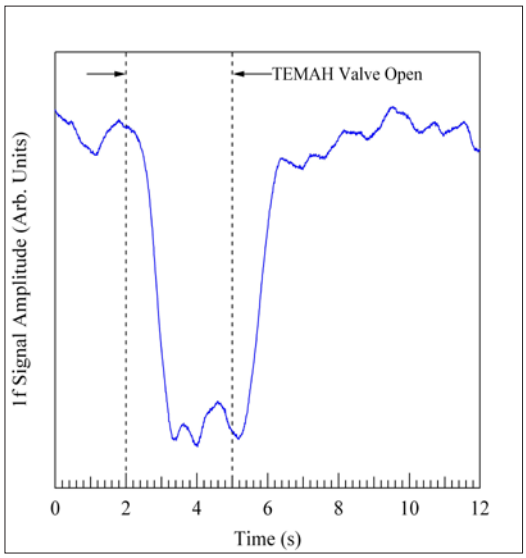


Figure 4. Mid-IR quantum cascade laser-based TEMAH absorption measurements.

TEMAH was measured in the mid-IR spectral region using a quantum cascade laser and amplitude modulation spectroscopy, as shown in Fig. 4

In addition to optical measurements, a quadrupole mass spectrometer has also been used to monitor volatile species present during ALD, including methylethylamine as illustrated in Fig. 5

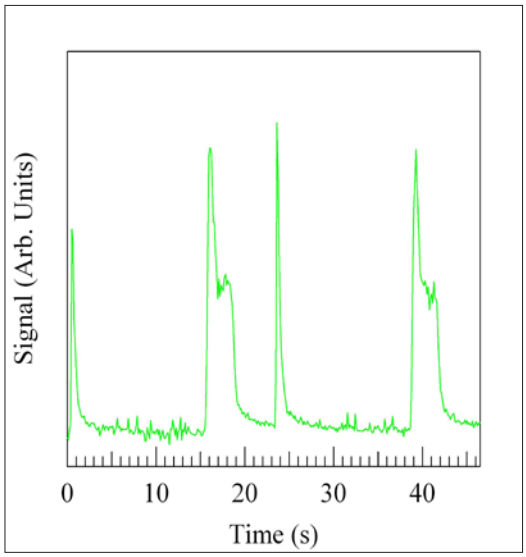


Figure 5. Mass spectrometric measurement of mass-to-charge ratio representative of methylethylamine during ALD cycle.

■ In-Situ Surface Measurements — In-situ surface RAIRS measurements have been performed during HfO_2 film deposition and have been shown to be sensitive to surface functionalization occurring during the ALD process, as shown in Fig. 6, as well as potential impurity-incorporation reactions.

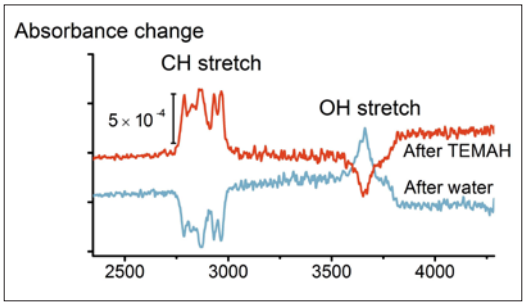


Figure 6. RAIRS spectra during ALD cycles.

■ ALD Reactor Modeling — Gas flow and temperature profiles in this reactor have been simulated using three dimensional CFD modeling, as shown in Fig. 7. In addition, time-resolved precursor distributions have been modeled. The results from these models have been used to help optimize reactor designs (especially optical window design) and deposition conditions, as well as interpret in-situ measurements.

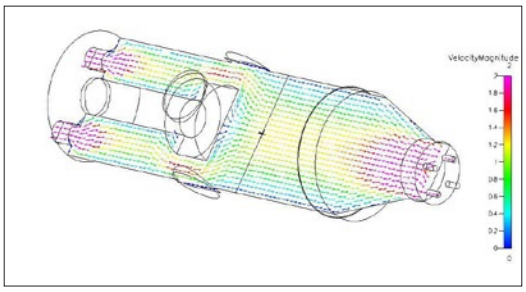


Figure 7. A cross section of the helium carrier gas velocity distribution in the diagnostic-accessible reactor under typical deposition conditions (obtained from a full three dimensional simulation

■ ALD Reaction Mechanism Development — A chemical reaction mechanism describing ALD of HfO_2 from water and TEMAH has been developed and is being refined. A schematic of this mechanism is illustrated in Fig. 8 (next page). This mechanism has been used with the three dimensional flow and temperature models to simulate the entire ALD process.

■ Chemical Properties Calculations — Molecular structures, vibrational frequencies, and

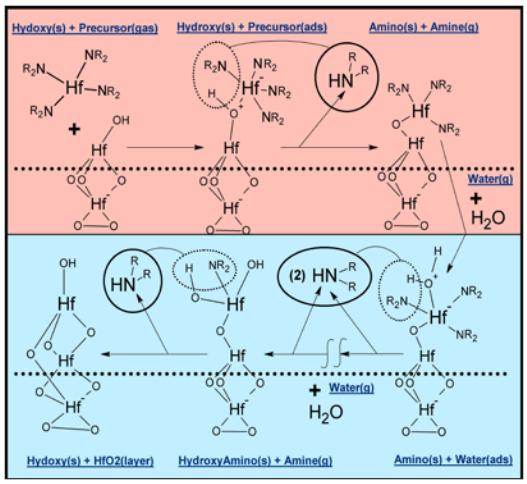


Figure 8. Schematic of HfO_2 ALD chemical mechanism.

energies for precursors, intermediates, and products have been calculated using quantum chemical methods for ALD of HfO_2 from TEMAH/tetrakis(dimethylamino) hafnium (TDMAH) and water. Comparisons are made between the calculated predictions and experimental data to develop reliable and self-consistent values. A detailed chemical kinetics model for ALD of HfO_2 from TEMAH and water has been developed and is being further refined using reactor model simulations and by comparison with experimental observables.

■ Reference Spectra Development — Reference spectra of TEMAH, MEA, dimethylamine and diethylamine (volatile products of the tetrakis(diethylamino) hafnium and water reaction) were recorded in the near-IR and mid-IR spectral regions. The measured mid-IR vibrational frequencies were compared to vibrational frequencies that were calculated with hybrid density function theory. Near-IR spectra are necessary to design semiconductor laser-based spectroscopic techniques utilizing relatively inexpensive telecommunications lasers. MEA, dimethylamine, and diethylamine spectra are useful for other than just HfO_2 ALD from Hf-containing alkyl amines. These compounds are the primary reaction products in water-based thermal ALD employing other metal alkyl amines, e.g., tetrakis(diethylamino) zirconium and tetrakis(ethylmethylamino) silicon.

■ Database Website — A Website http://kinetics.nist.gov/CKMech has been made available. This site contains bibliographic and thermochemical information for organometallic and other compounds important in semiconductor deposition processes, including organometallic compounds containing hafnium and aluminum.

Recent Publications

E. J. Heilweil, J. E. Maslar, W. A. Kimes, N. D. Bassim, and P. K. Schenck, *"Characterization of metal oxide nanofilm morphologies and composition by terahertz transmission spectroscopy,"* Optics Letters 34, 1360-1362 (2009).

J. E. Maslar, W. S. Hurst, D. R. Burgess, W. A. Kimes, N. V. Nguyen, E. F. Moore, and J. T. Hodges, *"In Situ Gas Phase Diagnostics for Hafnium Oxide Atomic Layer Deposition,"* ECS Transactions 13, 139-149 (2008).

N. V. Nguyen, O. A. Kirillov, W. Jiang, J. E. Maslar, W. A. Kimes, and J. S. Suehle, *"Interface Barrier Determination by Internal Photoemission: Applications to Metal/Oxide/Semiconductor Structure,"* ECS Transactions 13, 161-167 (2008).

Advanced Nanoscale and Mesoscale Interconnects

Technical Contacts:
T. P. Moffat
D. Josell

Goals

This project is developing solutions to metrology issues confronting integrated circuit manufacturers in the area of interconnect metallization. Present efforts include determining the essential process requirements for superconformal fabrication of high aspect ratio, low resistivity metallizations for both on-chip, chip stacking, and MEMS applications, examining the generality of the superconformal filling mechanism, expanding the applicable materials set, and exploring processes utilizing novel barriers and/or seed geometries. This is complemented by surface chemistry studies aimed at understanding and optimizing the feature-filling process.

Customer Needs

Increasing information technology requirements have yielded a strong demand for faster logic circuits and higher-density memory chips. The low electrical resistivity of copper and the ability of electrodeposition to "superconformally" fill high aspect ratio features has made electrodeposited copper the interconnect material of choice in silicon technology. However, the move to ever-smaller dimensions has led to the rise of new challenges, including fabrication of ever-thinner copper seeds, which are required for the copper superfill process and increased resistivities of the metallizations due to size effects. At the same time a strong movement towards 3-D integration of integrated circuits (i.e. chip stacking) is under way. This involves the replacement of long horizontal conductors by short vertical interconnections; in addition to an improved RC response, the new architecture enables integrations of heterogeneous devices. Many challenges to the fabrication through-silicon-vias (TSV) remain that require an understanding of the surface chemistry of copper. To help overcome these hurdles, the National Institute of Standards and Technology (NIST) is enhancing existing copper technology through improved understanding of the surface chemistry and metrologies for the superfill process, examining new interconnect materials, and pursuing new fabrication techniques such as seedless processing and atomic layer deposition. Similarly, there is also increasing interest in expanding the materials set available for constructing 3-D MEMS architectures. In this regard NIST has begun exploring the integration of ferromagnetic materials into Damascene processing.

Interconnect metallization issues are discussed in the Interconnect section of the 2008 update of the International Technology Roadmap for Semiconductors.Technical

Technical Strategy

To meet future industrial needs, we have, over the life of this project, developed metrology and fully disclosed copper electrolytes that permit characterization of the ability of generic electrolytes to fill features over a wide range of length scales. The derived Curvature Enhanced Accelerator or Adsorbate Coverage (CEAC) mechanism has served as a platform for this understanding. A key element to bottom-up surperfilling is the competition between deposition rate suppressing polymers and rate accelerating sulfonated alkythiols (and/or disulfides) for surface sites. In the case of on-chip interconnects an important consequence of bottom-up superfilling is the overshoot phenomenon known as "momentum plating" that can lead to bump formation above filled features. These bumps greatly hamper subsequent planarization processes. However, the overshoot process may be controlled by the addition of certain cationic surfactants to the copper plating baths. In a related manner, cationic surfactants exert an even greater influence on the filling of larger scale TSV's geometries. We are using a variety of electroanalytical and feature-filling experiments that help establish strategies for quantifying and understanding the influence of surfactants on film growth over a range of length scales. Through this activity the CEAC model was successfully extended to explain and predict the filling behavior during deposition from complex plating baths containing combination of suppressors, accelerators, and levelers.

In parallel with this effort a variety of surface analytical studies, *e.g. in-situ* STM and XPS, are under way to directly probe the competitive adsorption dynamics between multiple additives and the copper surface in order to provide mo-

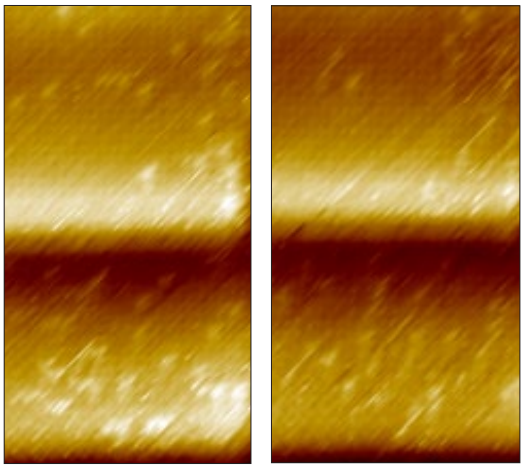


Figure 1a *Figure 1b*

Figure 1a and b. In situ STM images of the surface phase responsible for Cu superfilling. The accelerating sulfonated alkyl disulfide molecules rapidly diffuse as a lattice gas on top of the close packed square lattice of chloride ions, Cl-Cl separation is 0.36 nm, on a Cu (100) surface.)

DELIVERABLES:

- Publications using surface and electroanalytical probes to independently quantify adsorbate coverage and dynamics relevant to superconformal feature filling. 4Q 2009.

The generality of the bottom-up superfilling process to the application of other material systems in ULSI and MEMS remains a subject of great interest. In addition to silver (the only metal with a higher conductivity than copper) and gold (a metallization for wide-bandgap semiconductors) the prospect for deposition of iron group metals (for MEMS and magneto-electronic circuitry) has been examined. Most recently, a simple solution for integrating nickel, cobalt, nickel-iron and cobalt-iron alloys into the Damascene processing has been demonstrated. As shown in Fig. 2, the addition of a simple benzimidazole derivative to a cobalt-iron plating bath complete filling of trenches while limited deposition occurs on the neighboring free-surface.

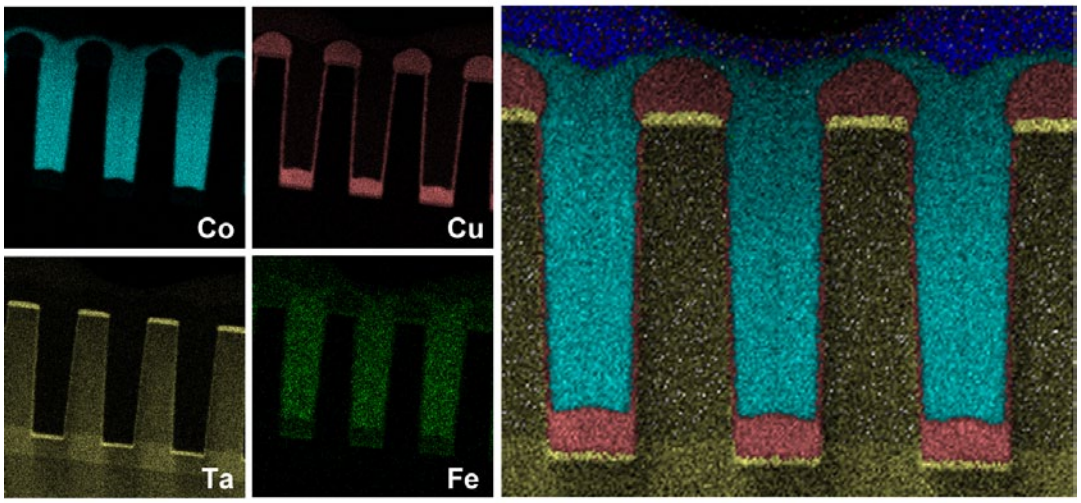


Figure 2, TEM-EDS image of superconformal electrodeposition of a Co-Fe alloy in a trench array.

lecular level insight into additive function and design. Particular attention is given to the role of potential-dependent adsorption processes that are central to the performance of the copper pulse plating method used to form TSVs. The competitive and co-adsorption of surfactants relevant to superfilling may be monitored and quantified by voltammetry. These studies are complemented by in-situ STM examinations of the surface structure and dynamics as shown in Fig 1. Close attention is being given to connecting the results of such single crystal studies with feature-filling experiments.

DELIVERABLES:

- Publications detailing the deposition of magnetic materials for Damascene metallization. 1Q 2009 and 4Q 2008

In addition to the electrodeposited copper conductor itself, current metallization technology employs a barrier metal and a PVD copper seed. As feature sizes continue to shrink, the resistive barrier materials negatively impact electrical performance, and deposition of, and on, the PVD seed becomes problematic. These difficulties are driving a search for alternative

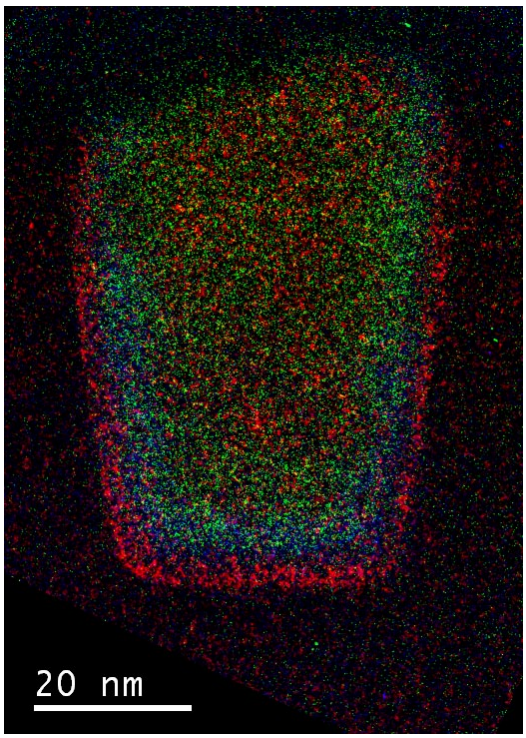


Figure 3. TEM-EDS of Cu filled trench lined with a highly conformal WN/Co4N barrier and Cu seed layer produced by ALD and CVD, respectively.

barrier/wetting layer materials and processes. Ruthenium is one focus because its electrical and thermal conductivities are approximately twice those of conventional tantalum barriers, it is immiscible with copper, and copper can be electroplated directly on it, eliminating the need for the PVD copper seed layer and the corrosion problems that come with it. In the past we have demonstrated direct copper superfilling on Ru, Os, and Ir barrier/adhesion seed layers as well as appropriate metrological aspects required for process control. This work continues with the evaluation of state-of-the-art ALD WN-Co4N novel barrier materials as shown in Fig 3.

Accomplishments

■ Void-free superconformal deposition of nickel, cobalt, nickel-iron and cobalt-iron alloys demonstrated by the addition of benzimidazole derivatives or cationic polymers such as polyethyleneimine to the electrolyte. Filling proceeds by a new mechanism that involves transient breakdown of an inhibiting molecular layer that is coupled with the trench geometry in a manner that enables void-free filling.

■ A range of electroanalytical and surface analytical studies under way to quantify the competitive and co-adsorption processes associated with copper superfilling additives. A combination of surface analytical and electroanalytical methods was used to reveal a.) difference in adsorption behavior between rate accelerating thiols versus disulfides, b.) irreversible adsorption of thiols and disulfides versus reversible adsorption of halide and PEG, c.) inhibition of PEG adsorption by a pre-adsorbed sulfonate-terminated thiol or disulfide monolayer film, and d.) displacement of the deposition rate inhibiting PEG layer by adsorption of the sulfonate-terminated thiol or disulfide accelerator.

■ The existing CEAC model of superfilling was extended to include the effect of leveling additives along with the metrology required for assessing the kinetics of the competitive adsorption process. The impact of leveling additives on overfill bump formation during trench filling was demonstrated using prototypical cationic surfactants.

■ Invited review articles on "Size-Dependent Resistivity in Nanoscale Interconnects" and "Superconformal Film Growth."

Collaborations

C.H. Lee, J.E. Bonevich, D. Wheeler, M.L. Walker, L.J. Richter, P.J. Chen, W.F. Egelhoff: NIST. Christian Witt: AMD. R. Gordon: Harvard University. Rohm and Haas Electronic Materials.

Recent Publications

Daniel Josell, S.H. Brongersma and Z. Tokei, Annu. Rev. Mater. Res., 39, In Press (2009).

C.H. Lee, J.E. Bonevich, J.E. Davies and T.P. Moffat, *"Superconformal Electrodeposition of Co and Co-Fe Alloys using 2-Mercapto-5-benzimidazaolesulfoncis Acid"* (MBIS), J. Electrochem. Soc., in press (2009).

T.P. Moffat, D. Wheeler and D. Josell, *"Superconformal Deposition and the CEAC Mechanism,"* Dielectric for Nanosystems 3, Materials Science, Processing, Reliability and Manufacturing, D. Misra, H. Iwai, Y. Obeng, T. Chikyow and J. Vanhellemont, Editors,The Electrochemical Society, 13, 129-137 (2008).

T.P. Moffat, D. Wheeler and D. Josell, *"Superconformal Film Growth,"* in Advances in Electrochemistry and Electrochemical Engineering, pg 107-189, R.C. Alkire, D.M. Kolb,

P. Ross and J. Lipkowski, Editors, Wiley-VCH, Weinheim, Germany(2008). C.H. Lee, J.E. Bonevich, J.E. Davies and T.P. Moffat, *"Magnetic Materials for 3-D Damascene Metallization: Void-free Electrodeposition of Ni and Ni70Fe30 Using 2-Mercapto-5-benzimidazolesulfonic Acid,"* J. Electrochem. Soc., 155, D499 (2008).

S-K. Kim, J.E. Bonevich, D. Josell and T.P. Moffat, *"Electrodeposition of Ni in Submicrometer Trenches,"* J. Electrochem. Soc., 154, D443 (2007).

T. P. Moffat, D. Wheeler and D. Josell, *"Superconformal Film Growth,"* pg 96-114 in "Electrocrystallization in Nanotechnology," Ed. G. Staikov, Wiley-VCH (2007).

M. Walker, L. J. Richter, and T. P. Moffat, *"Potential Dependence of Competitive Adsorption of PEG, Cl-, and SPS/MPS on Cu: An In Situ Ellipsometric Study,"* Journal of the Electrochemical Society 154(5), D277-D282 (2007).

D. Josell, T. P. Moffat and D. Wheeler, *"Superfilling When Adsorbed Accelerators Are Mobile,"* Journal of the Electrochemical Society, 154(4), D208-D214 (2007).

T. P. Moffat, D. Wheeler, S. K. Kim and D. Josell, *"Curvature Enhanced Adsorbate Coverage Mechanism for bottom-up superfilling and bump control in damascene processing,"* Electrochimica Acta, 53, 145 (2007).

D. Josell, *"A paradigm for interconnect geometry to reduce grain boundary resistance,"* J. Appl. Phys., 100, 123705 (2006).

S.-K. Kim, D. Josell and T. P. Moffat, *"Cationic Surfactants for the Control of Overfill Bumps in Cu Superfilling,"* J. Electrochemical Society, 153 (12), C826-C833 (2006).

S.-K. Kim, D. Josell and T. P. Moffat, *"Electrodeposition of Cu in the PEI-PEG-CL-SPS Additive System: Reduction of Overfill Bump Formation During Superfilling,"* J. Electrochemical Society, 153 (9), C616-C622 (2006).

M. Walker, L. J. Richter, and T. P. Moffat, *"Competitive Adsorption of PEG, Cl-, and SPS/MPS on Cu: An In Situ Ellipsometric Study,"* Journal of the Electrochemical Society 153(8), C557-C561 (2006).

T. P. Moffat, D. Wheeler, S.-K. Km and D. Josell, *"Curvature Enhanced Adsorbate Coverage Model for Electrodeposition,"* Journal of the Electrochemical Society, 153(2) C127-C132 (2006).

D. Josell, D. Wheeler and T. P. Moffat, *"Gold Superfill in Submicrometer Trenches: Experiment and Prediction,"* Journal of the Electrochemical Society, 153(1) C11-C18 (2006).

Nanoimprint Lithography

Technical Contacts:
C. L. Soles

Goals

Nanoimprint Lithography (NIL) is rapidly emerging as a low-cost patterning alternative to optical lithography, offering e-beam type resolution in a high-throughout, low-cost nanoscale patterning tool. Patterning resolutions of better than 10 nm have been demonstrated under optimized laboratory conditions. For these reasons NIL now appears on the ITRS roadmap as a candidate NGL for the 22 nm node. Optical lithography is a 4× patterning process, where the features on the mold are approximately four times bigger than the patterned feature. By comparison, NIL is a direct write (1×) technology where the feature in the mold directly corresponds to the feature in the pattern. This switch from a 4× to a 1× technology, coupled with a sub-10 nm resolution, greatly heightens CD metrology issues. Even with 4× optical lithography, the ITRS roadmap is facing critical CD metrology roadblocks and the advent of NIL would significantly exacerbate these concerns. One of the primary objectives of this project is to develop the relevant CD metrology methods needed to facilitate the NIL technology. The other objective of this project is to address the measurements issues that are unique for NIL, different from the traditional metrology needs for CMOS fabrication. NIL is a contact lithography method and that comes with very different metrology challenges due to the fact that the imprint mold makes mechanical squeeze-flow contact with the resist. The overall objective of this project is to address the measurement challenges facing NIL, not just for CMOS fabrication but for nanoscale pattering in general.

CUSTOMER NEEDS

The ultimate challenge for any new lithographic patterning technique is to demonstrate an improved patterning resolution. This requires a quantitative comparison of pattern shape. It has already been mentioned above that NIL offers a potential patterning resolution of better than 10 nm, exceeding the capability of current critical dimension (CD) metrology tools to accurately quantify. This significantly exacerbates current CD metrology concerns. With respect to NIL patterning, a unique CD measurement challenge arises. Because NIL is a direct write (1×) technology where the features in the mold directly correspond to the features in the pattern, high resolution CD metrology becomes critical. With optical lithography, the mask features are nominally four times bigger than the printed imaging which somewhat relaxes the resolution requirements for mask inspection tools. Furthermore, the resolution of the final optical lithography pattern depends on a complicated interplay of optical exposure effects, reaction-diffusion process in the latent resist image, and lastly the strength and conditions of the aqueous developer process. It is hard to directly trace small dimensional defects in the mask to the final pattern through this complicated process. On the contrary, NIL is a direct write process where the features in the imprint mold are directly transferred to the patterned resist.

Defects in the mold are directly transferred to the resist pattern. So with NIL, CD metrology must include the fidelity of pattern transfer concept. This means applying high resolution pattern shape measurements to both the imprint master and the resulting imprint. By quantitatively comparing the pattern shapes in the mold and the imprint one can determine if any potential defects are due to the quality of the mold itself or the performance of the resist material. This type of simple, direct comparison is simply not possible with optical lithography, and only possible with NIL through improved CD metrology methods. The next challenge is to quantify how the mechanical forming aspect of NIL differs from optical lithography with respect to measurement issues. One of the unique aspects is that the NIL process requires material flow into nanoscale cavities. This has several effects. First, resists are usually multi-component, reactive mixtures and it is likely that one of the components will have a preference or favorable interaction with the surface of the imprint mold.

This can affect the phase behavior of the resist mixture, or lead to surface-induced effects on the chemical reactions. In these cases it is critical to quantify how confinement and the surface effects influence the reaction within the resist and consequently the ultimate patterning resolution. The second measurement challenge comes from the fact that resists can be highly viscous liquids that do not readily flow, especially in the

case of thermal NIL where the resist is heated to the melt state to induce flow. Imprinting these highly viscous materials induces large shear stresses or flow fields. These shear stresses can be locked into the imprinted patterns as residual stresses, which over extended periods of time have the tendency to relax and induce distortions that compromise the stability of nanoscale structures and deteriorate the CD control. A third measurement problem stems from the fact that the NIL technology has the potential to directly pattern functional, such as nanoporous organolsilicate materials for semiconductor interconnect insulators. By patterning the interconnect material directly through a mechanical forming NIL process, one has the potential to essentially eliminate all of the litho steps in the back end of the line interconnect fabrication process, creating a tremendous cost savings. However, in this direct patterning approach the way that the NIL processes affect the function of the interconnect material, both in terms of critical dimension control and functional porosity properties are of critical importance. Measurements that quantify these effects are critical to advancing such cost-savings technology.

TECHNICAL STRATEGY

In the realm of state-of-the-art lithography, the ability to reliably produce high resolution patterns has been the primary figure of merit for any new patterning technology. This requires measurement methods that quantify and compare pattern quality with nanometer accuracy. As patterning resolution continues to improve, our ability to do this comparison quantitatively becomes a critical roadblock. This is especially true for NIL, where patterning resolution increases dramatically over the incumbent optical lithography. Our ability to pattern is now seriously encumbered by our ability to quantify and new pattern shape measurements are critically needed. To this end we continue to develop a suite of X-ray based metrology tools that include critical dimension small angle X-ray scattering (CD-SAXS) and specular X-ray reflectivity (SXR). Both of these methods are non-destructive and capable of quantify quantifying pattern shape with nm accuracy.

The fact that they are reciprocal space measurements means that characterizing smaller patterns becomes easier. When coupled with traditional critical dimensional metrology tools, we have a unique and powerful methodology to quantify the shape and dimensions of nanoscale structures with nm accuracy.

DELIVERABLE:

- Perform CD-SAXS measurements on NIL relevant patterns with sub 50 nm features and quantitatively demonstrate the fidelity of pattern transfer concept.

NIL is a direct write pattern transfer process. The features in the mold are directly transferred the imprint without going through a lens or other image reduction system. Evaluating the quality of the NIL patterning process requires quantitative critical dimension quantification of both the imprint mold and the patterns that it creates. Our CD-SAXS and SXR pattern shape measurement are well suited for quantifying the fidelity of pattern transfer in the imprint. They are both non-destructive methods meaning that mold or the pattern does not have to be sacrificed to quantify the fidelity of pattern transfer. The flexibility of either a transmission (CD-SAXS) or reflection (SXR) measurement means that a wide array of molds and substrates, ranging from thin to very thick, can be quantified. Using these methods it is straight forward to quantify the full pattern profile, including height, width, side wall angles, and periodicity with nm scale precision in both the mold and the imprint. This provides the framework for a highly quantitative fidelity of pattern transfer analysis, thereby providing a powerful tool for evaluating NIL patterning processes.

DELIVERABLE:

- Compare optical scatterometry to X-ray based pattern shape metrology for NIL patterns

SXR and CD-SAXS are emerging X-ray based methods with many advantages over the typical pattern shape metrology tools used in the semiconductor industry. However, there are several disadvantages with these emerging methods as compared with the industry standards like optical scatterometry. One of the primary complaints with SXR and CD-SAXS is that they are slow measurements that require long data collection times or highly intense X-ray sources, typically found at a synchrotron.

Additionally, the SXR measurement requires very large pattern fields that are not typical for real device architectures. Optical scatterometry directly overcomes these weaknesses by using intense laser light sources that can be focused into very small, micron-scale spots which enables

the rapid characterization of small pattern fields. However, the interpretation of scatterometry data requires extensive libraries of all the possible shape that the nanostructures could be. There is significant benefit in using SXR and CD-SAXS methods to help verify, improve, and develop scatterometry libraries. For the nanoscale structures that are relevant for NIL, the size of the pattern is significantly smaller than the wavelength of the laser light which leads to very subtle variations in the psi and delta of the reflected light. To properly interpret the scatterometry data requires highly accurate models. SXR and CD-SAXS provide an independent method to verify these models with nm accuracy. The increased patterning resolution provided by NIL makes this validation and cross-comparison all the more important.

DELIVERABLE:

- Adapt neutron and x-ray reflectivity measurements to quantify shear induced demixing of multi-component imprint materials

Resists are never single component systems. They can contain multiple reactive species, catalysts to speed up the reaction, surface tension modifiers, viscosity modifiers, additives to modify the etch resistance, and solvents to facilitate dispensing. While these multicomponent systems are typically co-dissolved into a single solvent, there will always be an energetic preference for one of the components to be near a given surface. Likewise, certain components can also tend to avoid an interface due to differences in the surface energy. When surface segregation occurs, the composition of the resist mixture is locally altered and the performance or function of the resist in that interfacial region is also changed. NIL has the potential to magnify the importance of these interfacial effects because the patterns are generated by placing a high surface energy mold in contact with the resist fluid/film, directly creating an interfacial region. For relatively thick films and large structures, the fraction of the material at the interface is negligible and these effects can often be ignored. However, with the high density of nanoscale features, as encountered in NIL, essentially all of the resist material can be classified as interfacial. The problem can be further exacerbated by the fact that the mold is filled with resist by a rapid squeeze-flow process. This can generate large shear fields that could induce demixing or field flow fractionation of the resist components. To fully optimize the performance of NIL resist materials requires quantitative measurements of the phase behavior within the imprinted nanoscale structures. Measurement techniques that can resolve compositional variations in an imprinted pattern will be critical for future resist developments.

A combination of X-ray and neutron reflectivity measurements in conjunction with CD-SAXS have the potential detect surface or shear induced demixing of a multi-component imprint materials. With this deliverable we plan to develop these measurements as a way to demonstrate to the community that these interfacial effects are important. We have already described how X-ray reflectivity measurements (SXR) and CD-SAXS can be used to accurately quantify the complete cross-section of the nanostructures fabricated by NIL. Most NIL resist are hydrocarbon mixtures, organic in nature, in which the scattering-length density for each of the components with respect to X-rays is very similar. A subtlety that was not discussed earlier is that this similarity is in part why SXR can be used to quantify the shape of polymeric or organic multi-component patterns. Changes in the scattering length density profile as a function of vertical distance through the pattern can be interpreted in changes in the shape of the lines, not changes in the composition. However, with neutrons this similarity in the scattering length density can be lost. By isotopically replacing the hydrogen in one of the resist components with deuterium, a very strong change in the neutron scattering length density can be achieved. The power of this hydrogen-deuterium labeling methods comes from the fact that the substitution does not change the X-ray scattering length density. So the combination of CD-SAXS and SXR on a model resist where one of the components is deuterium labeled can still be used to quantify the pattern shape. Once the shape is fully parameterized, the same sample can be measured by neutron reflectivity. In analyzing the neutron reflectivity data, the shape of the pattern will be fixed from the fitting of the X-ray data. Then the resulting fits from the neutron reflectivity data will reveal the variations of the scattering-length density as a function of height through the pattern, i.e., the composition of the deuterium labelled component through the pattern. Using this method it should be possible to distinguish between the different scenarios where the deuterium labeled component segregates to the supporting substrate surface, the upper imprinted surface, or remains molecularly dispersed through the pattern.

DELIVERABLE:

- Develop FTIR methods to quantify the degree of cross-linking/extent of reaction in step-and-flash imprint resists

The resists for the step and flash, or step and repeat, forms of NIL are typically reactive monomeric liquids designed to fill the NIL mold cavities via capillary wetting and then be cross-linked inside the mold through the exposure to ultraviolet (UV) radiation. During UV exposure, the resist transforms from a low viscosity liquid to a high modulus solid in a set period of time. The UV dose needs to be sufficient to maximize the degree of cross-linking in the patterns. Higher extents of conversion lead to higher modulus patterns that hold their shape better and resist distortion. However, throughput is always a concern with NIL in comparison to fast optical lithography methods and one cannot afford to over-expose the patterns just to ensure that the reaction is driven to completion. Measurements that quantify the degree of cross-linking within the nanoscale cavities of the mold are critical to optimize NIL processes. As the imprint features become significantly smaller than 50 nm, these types of measurements will be even more critical as the reaction kinetics are expected to be a function of the cavity size. The reaction mechanisms at the nanoscale will probably be different and this will impact the resist performance. Fourier transform infrared (FTIR) spectroscopy methods that are capable of quantifying reaction kinetics under these strong states of confinement are being developed.

DELIVERABLE:

- Characterize the fidelity and porosity of nanoporous material patterned by nanoimprint lithography.

Recently there is a growing interest within the community to directly pattern spin-on organosilicate ILD materials by nanoimprint lithography (NIL). It has been shown that by imprinting the ILD material with a multi-level nanoimprint template to directly fabricate a T-gate type structure, one can greatly reduce the number of lithography, deposition, and etching steps in the back end of the line process. This could *significantly* reduce manufacturing costs. Efforts this year will synergistically couple our expertise in thin film nanoporous X-ray metrology with our simultaneous efforts in NIL metrology development. Specifically, we will adapt our XR shape metrology to quantify the fidelity of the nanoimprint process to evaluate the quality of the patterned ILD materials. We will also adapt our XRP measurements on patterned samples to quantify how the NIL process itself affects the pore structure. These measurement techniques will quantify the feasibility of NIL processes for back end of the line interconnect fabrication schemes. This is a topic that all of the major NIL tool companies are actively engaged in.

ACCOMPLISHMENTS

This year significant progress was made on the quantitative fidelity of the NIL pattern transfer concept. Our starting point is an imprint master with parallel line-space gratings fabricated into silicon oxide. In real life applications, the original imprint master is rarely used to do actual imprint patterning. Rather, the master is used to generate a handful of daughter molds, copies of the master, which in turn are used for the day-to-day patterning. Using this approach one can extend the life of the costly imprint master. Our approach is to quantify the fidelity of pattern transfer through this process, starting with the original master and going through the daughter mold to the secondary imprint made with the daughter. To create the daughter mold, imprints are made at 200 °C, using the original template, into a spin-on organosilicate film that is similar in composition to the materials that are used for spin-on low k dielectric insulator applications. During the imprinting process material flow occurs while simultaneously the organosilicate material starts to condense into a hard organosilicate cross-linked network. However, the conversion is not complete at 200 °C so free the standing pattern is then further heated to 400 °C in an inert atmosphere to generate a fully cross-linked, hard organosilicate material that can be used as a daughter imprint mold. In the last step the daughter mold is thermally imprinted into a polystyrene film at 150 °C. In the following we apply our SXR and CD-SAXS methodologies to the original master, the organosilicate daughter, and the secondary polystyrene imprint.

Figure 1 compares the cross sectional profiles of the original master relative to the organosilicate (TTSE) daughter mold in the upper panel, and the daughter mold relative to the secondary polystyrene (PS) imprint in the lower panel. These profiles are the quantitative models used to fit the CD-SAXS and SXR data and not schematic drawings. To gage the length scales, the periodicity in each pattern is exactly 200 nm. In the upper panel the white gaps between the black colored master and the blue colored daughter represents shrinkage of the organosilicate pattern relative to the imprint cavities, including any shrinkage that

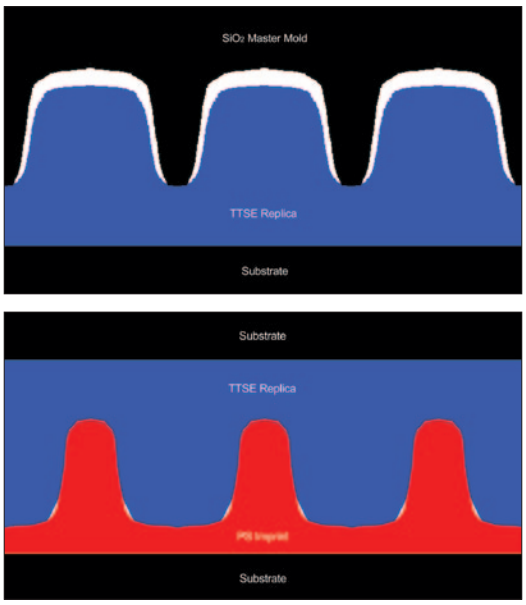


Figure 1. The upper panel compares the cross sectional profiles of the original imprint master mold to the replica or daughter mold imprinted into a high modulus organosilicate material (labeled TTSE here). The lower panel then compares the cross sectional profile of the TTSE daughter mold to the pattern generated through a thermal imprint into a PS film. The white gaps between the mold and the imprint represent the shrinkage or loss in fidelity of the pattern transfer process. In both panels the pattern periodicity is 200 nmt.

occurred during the imprint as well as during the high temperature vitrification. In other words, these white spaces quantify the loss of fidelity/resolution. In the bottom panel, there is very little shrinkage or loss of fidelity between the daughter mold and the PS imprint. The profile of the mold and imprint are nearly identical. When considering the patterning mechanism, these observations make sense. The PS is imprinted in the melt state, where the molten PS is an incompressible fluid and there is a conservation of volume. There is also very little shrinkage as the PS cools from the imprint temperature of 150 °C back down to the mold separation temperature of 55 °C. Given this approximately 100 °C temperature swing and difference in the coefficient of thermal expansion between the organosilicate and the PS, one would expect the 70 nm PS lines to shrink by approximately 1 nm relative to the organosilicate mold. This back of the envelope calculation seems consistent with the experimental data indicating that thermal imprinting can yield a very high fidelity of pattern transfer. On the other hand, in the imprinting of the organosilicate material, volume is not conserved. Some shrinkage is observed. The spin-on organosilicate is known to be laden with residual spin casting solvent. It is reasonable that this solvent is released at elevated temperatures during the imprint. Also, the cross-linking of the organosilicate is a condensation reaction where two silanols react and liberate a water molecule. The evolution of residual solvent or water molecules is consistent with the observation of shrinkage during the organosilicate patterning.

Another technical area in which significant technical progress was made this year was in the complimentary implementation of optical scatterometry as a critical dimension metrology tool for NIL patterning. As discussed above, when comparing X-ray based metrology tools to optical methods, there are well defined advantages and disadvantages to each approach. Using both methods in tandem, where the strength in one approach is used to overcome the weakness of the other, can be a powerful approach. With respect to scatterometry, one of the major advantages of this technique is in the speed and simplicity with which measurements can be made. The price of these fast measurements is that data interpretation is significantly more complicated compared to the slow but straight forward X-ray techniques. This year we focused on combining SXR pattern shape measurements with scatterometry as a tool to track the real time shape changes as an imprinted pattern is annealed at elevated temperature. With an applied thermal stimulus, an imprinted polymer pattern has the propensity to decay in height and ultimately transform into a smooth surface that minimizes the surface free energy of the system. In a separate project we have been tracking the time evolution of this pattern decay as a metrology to back out the levels of residual stress induced into the patterns by the NIL process. If the decay is consistent with the flow of a viscous liquid, the conclusion is that the patterning process did not induce residual stresses. If the decay occurs faster than what a viscous decay would predict, the conclusion is that the imprint process induces significant levels of residual stress. Without going into the details of this project, it is sufficient to say that a pattern shape metrology that is capable of tracking the real time decay pattern is highly attractive. SXR based methods are inherently slow, requiring at least 30 minutes per measurement which makes in-situ pattern evolution studies difficult. However, scatterometry has the potential or real time pattern shape measurement. In Figure 2,

we compare the pattern shape profiles obtain from both scatterometry and SXR. The upper panel in the figure to the left shows a series of line profiles obtain from the same 200 nm pitch PS patterns obtained from both the scatterometry (lines) and the SXR (dots) at a series of different discrete time points through the annealing process. The two methods are in very close agreement, showing a consistent picture of how the initially rectangular cross sections evolve into a smooth sine wave like function at long times. What is not articulated in this plot is how the SXR model was extremely helpful in establishing the starting point for modeling the scatterometry data.

With confidence in having chosen the correct model to interpret the scatterometry data, we are now in the position to harness the real time data collection aspect of the optical method. The lower panel of the of Figure to the left quantifies the real time evolution of just the pattern height for the thermal decay of both a high (1570 kg/mol) and low (19 kg/mol) molecular mass imprinted polystyrene pattern, as quantified by scatterometry. This type of in-situ characterization is not possible with the SXR method. The height decay data reveals an interesting trend. The high molecular mass pattern decays significantly faster (in this case both samples are annealed at Tg) than the lower molecular mass analog, despite the exponentially larger steady state viscosity of the high molecular mass material. This discrepancy directly reflects the residual stress levels in the imprinted pattern. The initially rapid decay of the high molecular mass pattern means that significant levels of residual stress have been stored in the imprinted pattern. After approximately 60 minutes of annealing the exponential decay rate slows down significantly, signifying that the stresses have been relaxed. At that point the relaxation of the low molecular mass pattern becomes faster as would be predicted by simple viscosity argument

One exciting alternative to directly eliminate or simplify several of the integration steps completely in BEOL processes is to introduce NIL processes to directly pattern the low-κ dielectric material. As described above, this can completely eliminate several of the etching and ashing processes that result from transferring a resist pattern into a dielectric layer. Directly patterning the dielectric material itself can completely eliminate several of these pattern transfer steps that lead to the increase in the effective k. This year we made two major advances on the direct patterning of

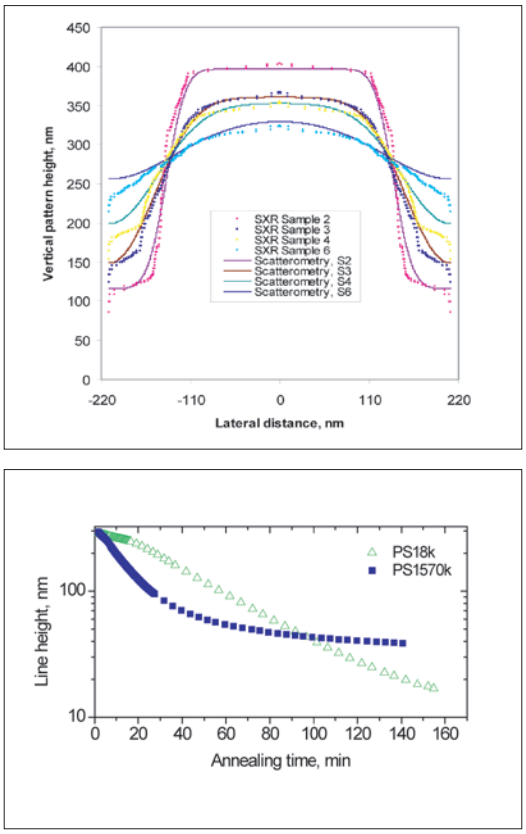
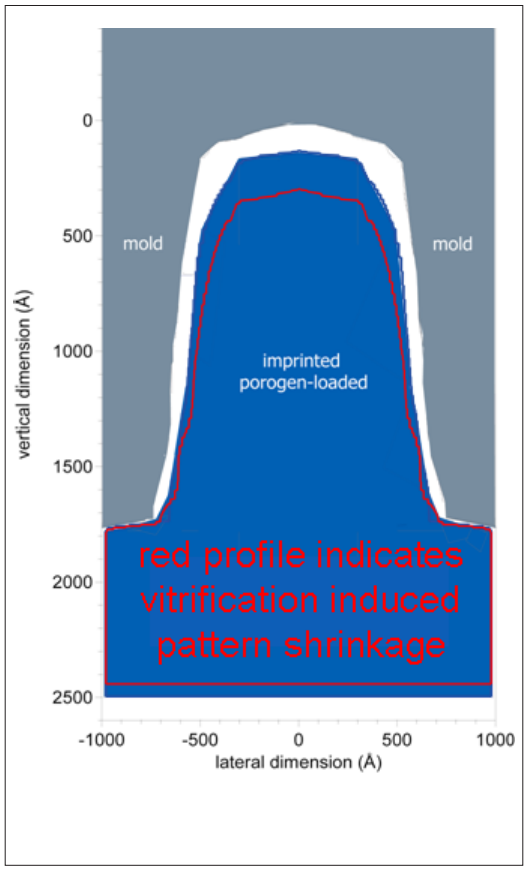


Figure 2. The upper panel compares the cross-sectional profiles obtained through specular X-ray reflectivity (SXR, dots) and optical scatterometry (lines) for a series of PS patterns annealed for increasing amounts of time. With increased annealing the patterns decrease in height and evolve into a sine wave type profile. The lower panel compares how just the pattern height evolves real time, as quantified by scatterometry, for both a low and high molecular mass pattern.

ILD materials with NIL. First, the concept of directly patterning the ILD materials was originally introduced in 2006 by Professor Grant Willson's group. However, to date the only examples of this type of patterning have been on very low modulus materials with relatively high dielectric constants that would not be suitable for current ILD applications. This year we made the critical step to show that ILD materials with an intrinsic dielectric constant on the order of 2.0 and a sufficiently high modulus could be directly patterned with NIL with very high fidelity. This demonstration was made possible through high resolution critical dimension measurements on both the NIL mold and the imprinted pattern. Using a combination of SXR and SAXS shape measurements, we showed



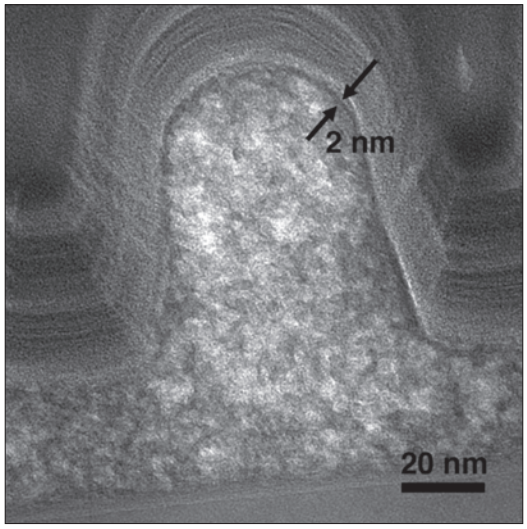


Figure 3. The upper panel shows cross-sectional profiles derived of the as imprinted pattern, before vitrification, (blue) relative to the mold (grey) indicating the shrinkage upon imprinting. The red curve indicates the additional shrinkage that occurs after the high temperature vitrification. The lower panel shows a cross-sectional TEM image of the same patterns, suggesting a dense skin of a few nm thick on top of the porous pattern

that the pattern shape in the imprint mold could be transferred to the ILD material with extremely high fidelity, even with a high temperature vitrification stage where the spin on organosilicate is condensed into a hard, ceramic-like material. This vitrification process is usually associated with shrinkage of the material. As shown in the figure above, our measurement show pattern shrinkage in all dimensions, not only relative to the mold immediately after imprinting, but also after the free standing pattern is vitrified at 430 °C. Our pattern shape measurements are able to define the pattern fidelity throughout the entire process. These seminal pattern shape measurements were described in a high profile Advanced Materials article.

Our second seminal contribution this year was in quantifying how the NIL patterning process affects the critical porosity of these low-κ materials. We developed a variant of XRP that is applicable to patterned materials and were able to extract the porosity as a function of pattern height. When combined with complimentary positron annihilation lifetime spectroscopy and cross-sectional transmission electron microscopy (TEM) measurements, this study revealed an NIL induced dense skin of the order of a few nm in thickness on the surface of the porous pattern. The cross sectional TEM image in Figure 3 shows evidence of this dense skin, which is highly attractive from an application point of view. Integration processes often require the addition of a densified skin on the ILD pattern to reduce interdiffusion. That NIL could intrinsically induce this barrier layer is highly attractive. These findings were also published in a second Advanced Materials article.

Collaborations

Polymers Division, NIST – Hae-Jeong Lee, Hyun Wook Ro, Jing Zhou, Ronald L. Jones, Chengqing Wang, Wen-li Wu.

University of Massachusetts-Amherst – James Watkins.

Seoul National University – Kookheon Char, Do Yoon.

University of Michigan - David Gidley, Richard Laine.

Kyoto Institute of Technology – Hiroshi Jinnai.

Recent Publications

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Interconnect Materials And Reliability Metrology

Technical Contacts:
T. P. Moffat
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"Mechanical properties are key to integration."

Roey Shaviv
Novellus Systems Inc.

Goals

The objectives of this project are: (1) to develop experimental techniques to measure the material properties that control the reliability of thin conducting and insulating films in interconnects under mechanical, thermal, and electrical stresses; these include basic tensile properties, elastic modulus by both static and dynamic means, residual stresses and strains, fatigue and fracture resistance, and thermomechanical response; and (2) to advance the ability to anticipate and meet interconnect reliability challenges by relating thin film reliability to microstructure and by developing understanding of the relationships between various modes of failure in nanoscale interconnect structures.

Customer Needs

Thin films are an essential component of all advanced electronic devices. Interconnect structures built up on ULSI microchips consist of 11 thin-film layers now, and will reach 15 layers in the long term (International Technology Roadmap for Semiconductors, 2007, Interconnect, Table INTC2b). These structures are fabricated using adjacent layers of materials with very different thermal expansion coefficients, exotic materials such as nanoporous low-κ dielectric, and operate at ever higher temperatures. Both experimental measurements and modeling and simulation of material behavior are needed, and these efforts need to be complementary. According to the Roadmap (2007 Edition), Interconnect, p. 39, Cost effective first pass design success requires computer-aided design (CAD) tools that incorporate contextual reliability considerations in the design of new products and technologies. It is essential that advances in failure mechanism understanding and modeling, which result from the use of improved modeling and test methodologies, be used to provide input data for these new CAD tools. With these data and smart reliability CAD tools, the impact on product reliability of design selections can be evaluated. The 2005 iNEMI (International Electronics Manufacturing Initiative) Research Priorities document reports a similar need. The top five research areas listed by iNEMI include Materials & Reliability and Design. Under Design, the top five research priorities include Mechanical and Reliability Modeling, p. 16. Appendix C of the document has a detailed section on Reliability, Mechanical Analysis, and Simulation, p. 44, which emphasizes the need for material characterization and reliability prediction. Key considerations in this paragraph and elsewhere in the document are effects of temperature and of cyclic loading and effects of size scaling. The iNEMI document specifically calls out the need to predict and understand failures in MEMS devices, p. 39. The message is clear: understanding and modeling of mechanical performance and potential failure modes in these devices require knowledge of the mechanical behavior of the films. This issue of mechanical modeling is likely to increase in significance with the growing integration of interconnect between the chip and the package, with their disparate material sets, and with the push into exotic nanoscale materials.

Void formation is presently recognized as a critical service reliability issue for interconnect structures on leading-edge commercial chips. It is classified into two types: electromigration voiding, where the flow of electrical current has a predominant role; and stress-induced voiding, where the relaxation of process-induced stresses plays the key role. The *ITRS Roadmap (2007 Edition), Interconnect, Table INTC2a*, foresees interconnect current densities of 2.25 MA/cm^2 in 2013, with no present capability to produce products with acceptable reliability.

Because the films are formed by physical vapor deposition, electrodeposition, or spin-on deposition, their microstructures, and hence, their mechanical properties, are different from those of bulk materials of the same chemical composition. While the general principles of conventional mechanical testing are applicable to thin films, conventional test equipment and techniques are not. Because vapor-deposited films are of the order of 0.1 to 1 μm thick, the failure loads are of the order of gram-forces or less, and the specimens cannot be handled directly. So, techniques specific to films on silicon substrates are needed. Developing test methods must eventually become applicable to test structures that can be included in production or development wafers, so that applicability to 'real' materials can be

demonstrated. The intent of our goal of testing specimens similar in size to structures on actual production devices is to maximize the relevance of our results. Industry needs test methods that are efficient and integrable in the fab environment. We see nanoindentation and high-amplitude a.c. measurements as candidates to become routine, or perhaps even on-line, methods. Compared to these, the microtensile test is more laborious, but it provides unambiguous results. We will continue to promote and offer the microtensile test as a reference method, while developing methods to extract needed material property information from the more integrable methods such as nanoindentation and high-amplitude a.c. testing.

We held a second nanomaterials workshop entitled Materials Characterization for Nanoscale Reliability, 14–16 August 2007, to gauge customer interest in the available tools, and needs for new tools, for characterization of nanomaterials, which, of course, encompasses advanced interconnect structures at both current and foreseen size scales. Microelectronics manufacturers were represented, along with universities, national laboratories, and more general commercial interests. The referenced report, from the similarly-themed 2004 workshop, gives the details, but two key messages for this research project were the widespread adoption of nanoindentation for material characterization, and the serious consideration given to atomic-scale materials engineering. New messages from the 2007 workshop were the need for all materials analysis tools to provide nanometer resolution, so that, for example, chemical variation across interfaces could be examined, and the need for ongoing cooperation between measurement laboratories and industry.

Radically different materials and material technologies are being considered for future ULSI devices, as the further development of leading-edge lithography increases in cost and complexity. An example of a radically new material is the carbon nanotube. An example of a new material technology is self-assembly. Effective use of these new materials systems will require significant extension of the reliability metrology and analysis toolset to understand and address new kinds of reliability issues. The NIST laboratory research programs, which back up the near-term metrology developments described here, are beginning to develop experimental and analytical techniques to address these challenges; NIST management is encouraging these developments through the new strategic focus area in nanotechnology.

Technical Strategy

We are developing a variety of measurement techniques to provide material property data on interconnect materials. In testing and exercising these techniques, we develop data that are valuable in themselves, and we also develop our understanding of the relationship between the observed behavior and the microstructure, as influenced by processing conditions specific to the specimen material at hand. We study individual thin films and multilayer interconnect structures on silicon substrates, both obtained from industry and fabricated by researchers within NIST and elsewhere. Specimens of CMOS structures have been obtained through the MOSIS service run by UCLA (Fig. 1).

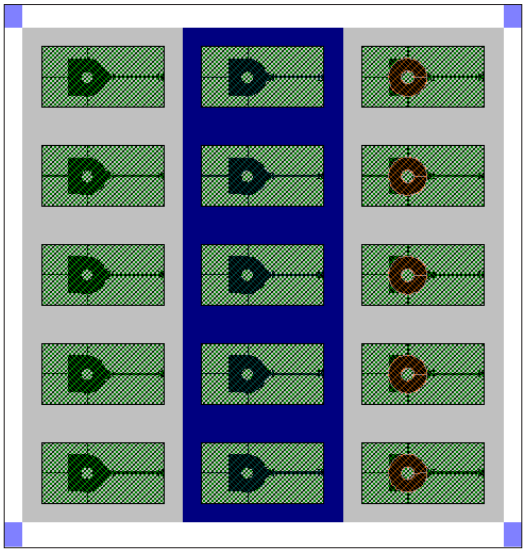

Figure 1. Test chip produced in the 1.2 μm AMI CMOS process available through the MOSIS service.

Measurement capabilities operating within this project include microtensile testing, d.c. and a.c. thermomechanical fatigue and micro- and nanoscale characterization of industrially relevant materials. We have developed the silicon-frame tensile specimen and the piezo-actuated tensile tester, which operate successfully for specimens 100 μm wide and larger. Because problems were encountered with specimens narrower than 100 μm, a new technique, called the force-probe tensile test technique, has been developed. The apparatus includes a tensile loading system operable within the SEM. This system has now been

used on specimens as small as 2 μm wide. The microtensile test provides complete and unambiguous mechanical design data.

Multiple wafer sections containing patterned specimen geometries of electrodeposited copper and other materials were received directly from our counterparts in industry during the past year. We have reported initial measurement results directly to the industrial collaborators, and received feedback about what they are interested in. For example, with an industrial collaborator, we are performing an extensive study of the variability of the mechanical properties of electrodeposited copper, to determine the effect of deposition conditions, surface treatment, and other relevant variables

DELIVERABLES:

- A joint industry-NIST publication on the effect of processing variables on the mechanical properties of thick electrodeposited copper. 3Q 2009

Our measurements involving alternating current stressing of chip-level interconnects are being used to explore the relationships between electrical, thermal, and mechanical reliability. High current density a.c. signals are run at low frequencies through Al- and Cu-based electromigration structures in either passivated or unpassivated states. Joule self-heating results in a cyclic strain due to thermal expansion mismatch between the metal lines and their substrates. The associated deformation then leads to severe topographic distortions in unconstrained lines, and can eventually cause open circuit failure. We investigate the effects of current density, frequency, crystallographic orientation, and encapsulant material. The use of advanced analytical techniques including EBSD, SEM, and TEM has revealed surprisingly similar microstructural damage and failure mechanisms in a.c.-stress and microtensile tests. This indicates at least the possibility that electrical tests may be exploited to produce information about the mechanical characteristics of thin films. If this electrical-mechanical test can be made to produce relevant data, it will be of significant benefit because of the experimental convenience of electrical stressing on specimens of a wide range of sizes, including very small and subsurface specimens. We have continued to improve our electrical measurements, and have begun SEM studies of the failure mechanisms in electrically-tested damascene copper interconnect lines.

DELIVERABLES:

- Conference presentation with short paper on application of electron backscatter diffraction to measurement of grain size and texture in copper damascene lines down to 25 nm wide. 2Q 2009

For the relatively simple situation of a few-micrometer wide aluminum line on a silicon substrate, the ultimate strength value can be estimated from the a.c. test by extrapolating the results back to one loading cycle, and correcting for the residual stress present in the line-on-substrate specimen. However, physical differences between the a.c. and microtensile tests include: thermomechanical vs mechanical stressing; elevated and variable temperature in the a.c. test; residual stresses in the film on substrate vs none in the free-standing tensile specimen; substrate constraint causing biaxial loading as well as additional strengthening in the a.c. test; and cyclic loading vs monotonic strain to failure. By more realistic treatment of these differences, in measurements on specimens of different materials with different grain sizes and different line widths, we will quantify the uncertainty with which static mechanical properties can be deduced from the a.c. test. As a point of reference, the rule of thumb used to estimate ultimate tensile strength from nanoindentation hardness is only useful for detecting trends, and does not provide a generally applicable quantitative estimate of the tensile strength.

DELIVERABLES:

- Book chapter on Metrologies for Mechanical Re-
- Technical journal paper on damage mechanisms in copper damascene lines subjected to high a. c. current density. 3Q 2009

Accomplishments

■ Progress in recent years on measurements of the mechanical behavior of thin films has put us in the position of starting to be able to make various kinds of critical comparisons among our results: results for the same materials in different laboratories; results for similar materials from different sources; results for the same property by different measurement methods; and experimental results versus numerical simulations. These comparisons are necessary to reach our goals of providing accurate and believable measurement techniques and an understanding of the results. Microstructural characterization is critical for defining the applicability of test results for different materials and test techniques. Currently, we are improving our measurements for charac-

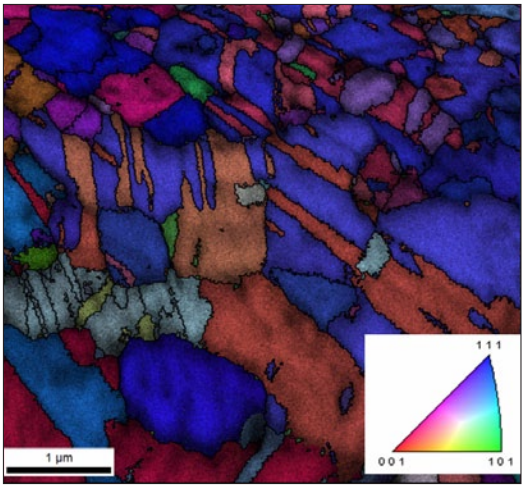

Figure 2. EBSD map of electrodeposited copper film specimen. The colors indicate the surface-normal crystallographic orientation of each pixel, according to the key, inset. Regions of constant color are crystallographic grains. The long, straight, parallel boundaries are twin boundaries.

terizing the microstructure of electrodeposited copper in order to better understand the influence of microstructure on reliability. Figure 2 shows the grain structure of a commercially produced copper film, as mapped out by EBSD. The colors represent local crystallographic orientation, according to the inset. Regions of constant color are metallographic grains. The long, straight, parallel boundaries are twin boundaries.

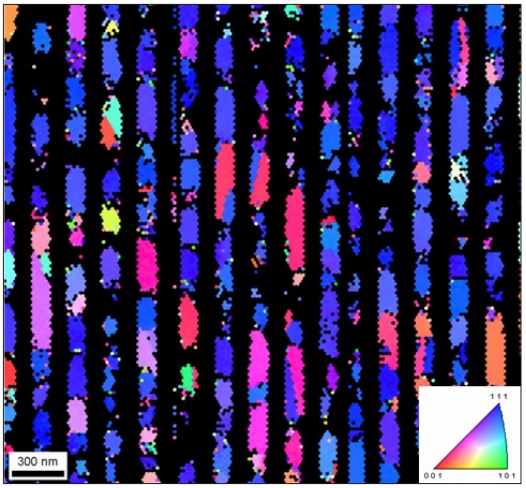

Figure 3. Electron backscatter diffraction map from a section of a 100 nm serpentine line structure. The black regions are the dielectric between the copper lines. The color represents the local crystallographic orientation normal to the plane of the page according to the inserted stereographic triangle. This mapping displays individual grains as colored regions. Note that the grain lengths average about 2.5 times the linewidth.

We found that we could make similar measurements on 100 nm wide copper lines in a damascene structure, Figure 3. The same wafer contained large copper features; these had a grain diameter approximately 2.5 times larger than the grain length along the narrow lines. This result indicates that for the process sequence used on this wafer, the large grain size of the copper overburden did not propagate into the narrow lines

■ Based on input received at our 2004 workshop on Reliability Issues in Nanomaterials, an international round robin to assess interlaboratory reproducibility of measurements of hardness and elastic modulus by instrumented indentation, on thin film materials typical of those used in interconnect structures in microelectronic devices, has been conducted; a technical publication reporting the results has been published. A specimen film selected after consultation with a group of experts in the field, consisting of a copper film with a platinum passivation layer, was contributed by Sandia National Laboratory. Open participation was solicited by e-mail to over 100 laboratories. Fragments of the specimen wafer were distributed to approximately 30 laboratories around the world. The goal was to obtain results representative of the experience of a "typical customer" using a testing laboratory. Approximately 25 laboratories conducted tests and contributed reports. The results have been analyzed with assistance from the NIST Statistical Engineering Division. The scatter in modulus and hardness are much larger from laboratory to laboratory than within laboratories; Fig. 4 shows the hardness data. This result indicates that comparisons of instrumented indentation results from different laboratories should be

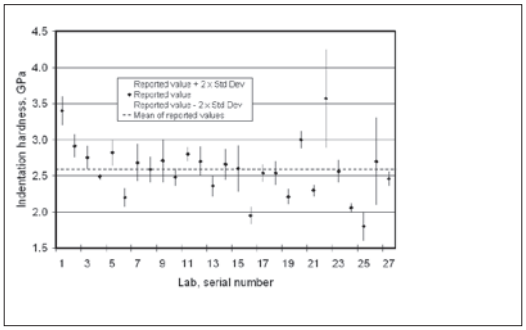

Figure 4. Reported results for indentation hardness of the round robin specimen material, a Cu film on a silicon substrate. The error bars at each data point span a total range of 4 times the standard deviation reported for multiple indentations. The average of the reported hardness values is 2.59 GPa.

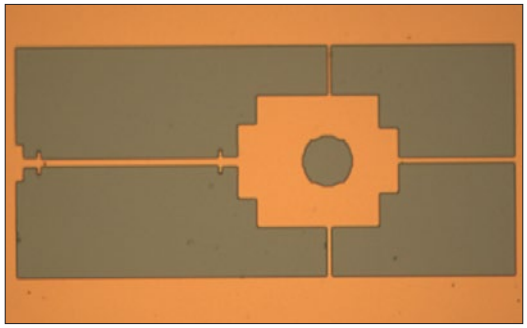

Figure 5. Microtensile specimen of electrodeposited copper produced at NIST. The slender strip on the left is the test section; the tab with the hold is used for loading. The grip section is 10 µm wide by about 200 µm long.

treated with caution, and that further investigation is needed to identify the sources of the scatter.

■ We have been working to demonstrate the applicability of our small-scale mechanical testing techniques to materials recently introduced in the microelectronics industry, specifically copper, in the form of both sputtered thin films and thick electrodeposits. A microtensile specimen of electro deposited copper is shown in Fig. 5.

We typically find that the strength values are far above the handbook values for pure annealed bulk copper, and the elongations are much lower than the handbook values. Increasing the film thickness from, for example, 1 µm to 10 µm, increases the ductility from around 1 % or less to 5 % or more. These data were obtained in microtensile tests of a new variety of electrodeposited copper supplied by an industry collaborator. Annealing also changes the tensile properties markedly. We have extended our microtensile test capability to temperatures up to 150 °C. Figure 6 shows re-

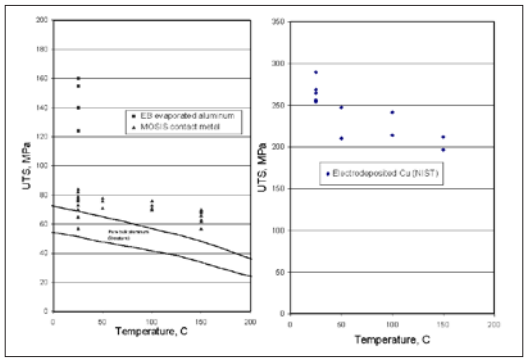

Figure 6. Tensile strength plotted against temperature for microtensile specimens of aluminum contact metal obtained through MOSIS, and electrodeposited copper made at NIST.

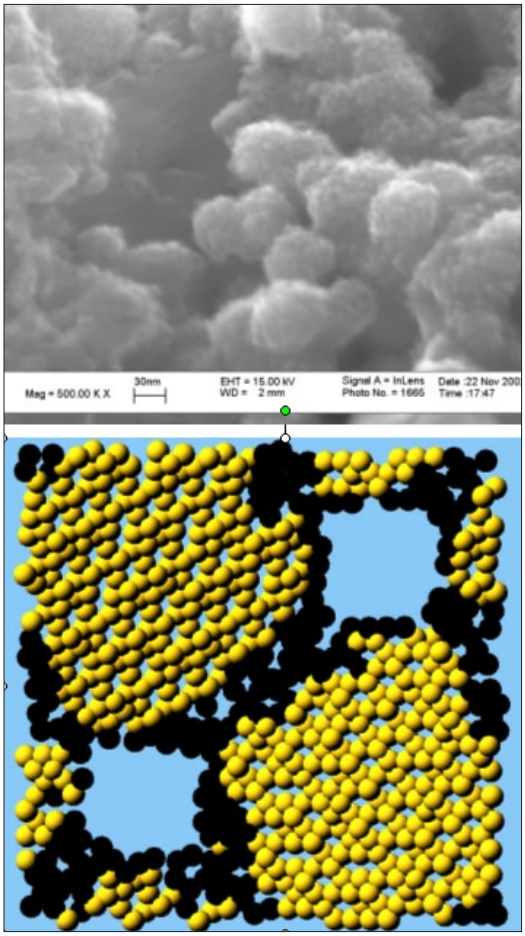

Figure 7. (a) High-resolution SEM image of electrodeposited copper specimen made at NIST. The original magnification was 500,000. The copper "balls" are 30 nm to 50 nm in diameter. (b) Atomistic model simulating the morphology and mechanical behavior of this copper electrodeposit. The atoms shown as copper-colored have near-normal facecentered-cubic crystal environments; the atoms shown as black are also copper atoms, but their local crystallographic symmetry is lower. Through the use of periodic boundary conditions, this 23000 atom model simulates a specimen of indefinite size.

cent results for contact Al-Si, from MOSIS, and electrodeposited copper, made at NIST.

The demonstrated applicability of the force-probe technique to a variety of specimen materials and temperatures leads us to think that this technique and its complementary specimen geometry may become a standard method for microtensile testing.

Figure 7a shows a high-resolution SEM image of the surface of an electrodeposited (ED) cop-

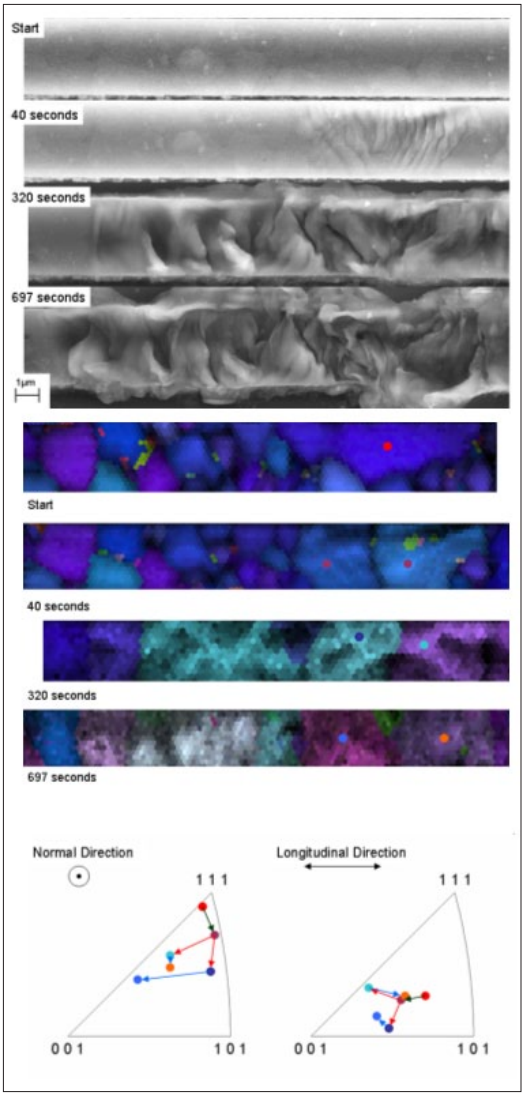

Figure 8. A.C. testing sequence in Al-1Si, showing development of surface offsets, grain size and shape changes, and grain orientation changes, at 0, 40, 320, and 697 seconds of A.C. cycling at about 12 MA/cm^2. Upper images: surface topography by SEM; lower images: same locations, color indicates grain orientation; drawing: changes in crystallographic orientation of grains as indicated.

per specimen made at NIST. The distinctive morphology, an array of joined spheres, may not be representative of normal production material. But it may represent, in an exaggerated form, microstructural features commonly present in ED copper. Its crystallographic symmetry, lattice parameter, and mechanical properties all appeared normal when measured by standard techniques. Figure 7b shows an atomistic model that simulates the mechanical behavior of this morphology, though at a smaller scale. The atoms shown as solid black are in regions of low face-centered-cubic symmetry, while the atoms shown in color are surrounded by near-perfect fcc structure. This simulation presents a possible explanation for our measured value of the elastic constant of ED copper, which is lower than the bulk value.

■ Our a.c. tests continue to reveal damage phenomena drastically different from that observed in conventional d.c. electromigration tests. To understand the results, we have pursued crystallographic mapping experiments within a field emission SEM, due to the generous amount of information that can be obtained with such an approach. What has become apparent is the tremendous variation in behavior from grain to grain. We have observed significant growth of selected grains in a polycrystalline interconnect, which subsequently become more susceptible to surface offset formation with further cycling (Fig. 8).

Accompanying such grain growth is a re-orienting of some grains, into a more accommodating orientation for slip activity. In other words, grain re-orienting seems to provide a larger resolved shear stress on a particular grain. Many factors interact to control the processes leading to catastrophic failure by open circuit, at a site where the interconnect cross section has decreased very significantly due to deformation. We are attempting to construct a model describing the roles of these factors, including strength of individual grains (grain size), ease of slip within individual grains (grain orientation), and prevalence of dislocation sources (grain boundary structures, surrounding grain constraints). The end goal is to offer a scheme for predicting where an open circuit should be expected, given the initial grain structure of the interconnect.

We are exploring the applicability of the a.c. test to commercial damascene copper structures. In these initial experiments we have plotted the data as lifetime to open circuit vs cyclic temperature range in Fig. 9. On this basis, we found a big difference between vias and lines, but no difference between oxide and low-κ dielectric structures. The preliminary conclusion from these tests is that the combined effects of thermal, electrical, and mechanical stresses need to be accounted for in designing reliable interconnect systems. The damage sequence shown in Fig. 8 is much different from electromigration. Results of our tests in damascene lines also indicate that the a.c. test excites thermal-mechanical failure mechanisms. Our a. c. tests of wide lines typically use current densities of 10 MA/cm^2 and higher. Figure 10 shows voids

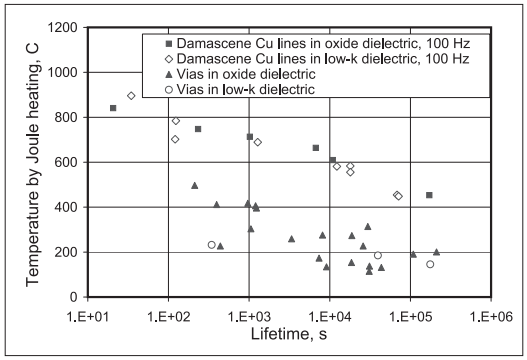

Figure 9. Comparison of lifetimes under high amplitude a.c. of Cu lines and Kelvin vias in damascene structures made with oxide and low-κ dielectric, plotted as cyclic temperature vs lifetime. When plotted in these coordinates, the vias fail at much lower temperatures than the lines in both structures, but the dielectric material does not affect the lifetimes.

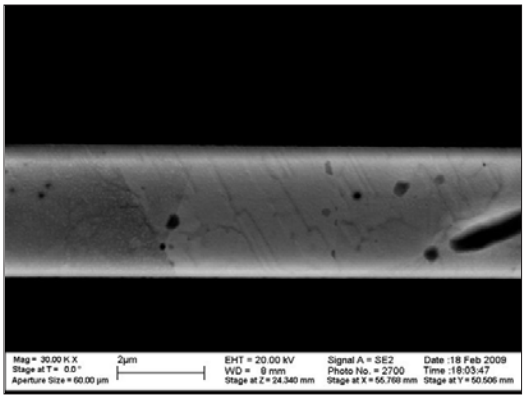

Figure 10. SEM micrograph of a copper damascene line 3 μm wide. This specimen was tested at 100 Hz at a peak current density of 18 MA/cm^2. The temperature range was 396 °C, the total von Mises strain range was 0.0091, and the lifetime was 1498 s. Note the voids.

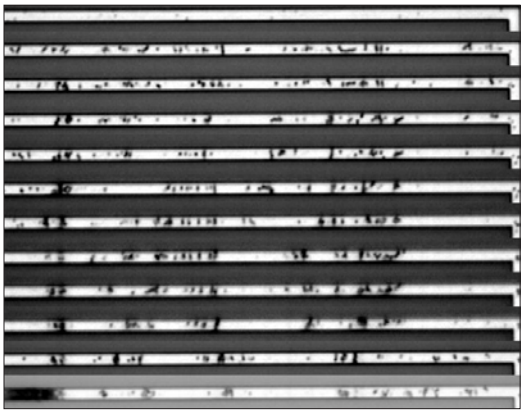

Figure 11. Time-lapse sequence showing rapid voiding (dark spots) in an a. c. test of a damascene copper line in SiO_2 dielectric. Line dimensions, 3 x 0.5 μm; peak current density, 16 A/cm^2; lifetime, 1946 s; temperature range, 403 °C.

in a damascene copper interconnect line after a. c. stressing. The application of a. c. to copper allows study of the void generation process; this process is obscured in d. c. electromigration tests because the void formation is slower, the failure is more rapid, and the void move more. Figure 11 shows a time sequence of optical images of voids forming in a copper line stressed by a. c. We explored the a new type of mathematical model of the electromigration process, based on peridynamics. This approach incorporates mechanisms considered in existing finite element and atomistic models, and avoids some of the disadvantages of these approaches. The major missing component was a physics-based model for how vacancies form and accumulate into voids. Our studies of void generation in copper will contribute to understanding the effects of electric current and temperature on void formation, growth, and motion. We have designed and fabricated special specimens to isolate the direct effect of electrical current from the thermal-mechanical effects. Figure 12 shows this "proximity effect" specimen. It consists of a heater, made of polysilicon or tungsten, and a test line; these are in thermal contact, but not in electrical contact. A.c. in the heater line applies thermal cycles to the test line. The purpose of the very long sections is to create a large constant-temperature zone free from end effects. Although the test line

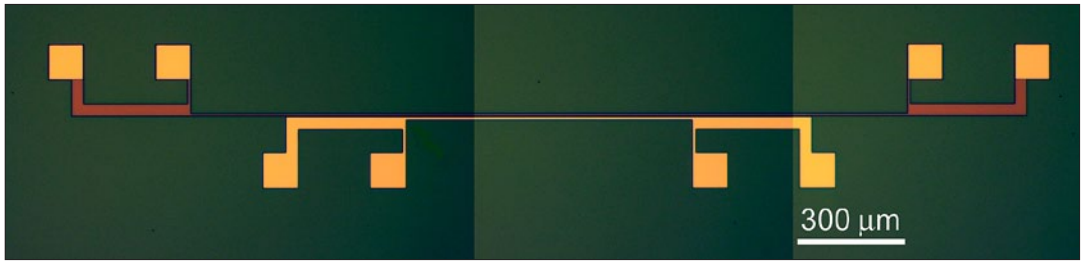

Figure 10. "Proximity effect" specimen for cyclic thermal-mechanical stressing. The upper, longer line is the heater; the lower line is the material to be examined.

in this example is a conductor, this design also allows dielectrics to be thermo-mechanically cycled.

Collaborations

Roey Shaviv and Tom Mountsier, Novellus Inc.

Intel Corp., Hillsboro, OR, Sadasivan Shankar.

Freescale, Inc., AISL, Tempe, AZ, Vijay Sarihan and Aric Buchta.

University of New Mexico, Prof. Walter Gerstle.

MOSIS Integrated Circuit Fabrication Service, 4676 Admiralty Way, Marina del Rey, CA, Dr. Tom Veriner.

Recent Publications

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D. Read and R. Geiss, *"Thermal Cycling of 300 nm Buried Damascene Copper Interconnect Lines by Joule Heating"*, in Nanotechnology 2008 (Conference) Volume 1, 2008, 218-221.

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N. Barbosa III, R. R. Keller, D. T. Read, R. H. Geiss, and R. P. Vinci, *"Comparison of Electrical and Microtensile Evaluation of Mechanical Properties of an Aluminum Film,"* Metallurgical Transactions A—Physical Metallurgy 38A (13), pp. 2160-2167, 2007.

R. R. Keller, R. H. Geiss, N. Barbosa III, A. J. Slifka, and D. T. Read, *"Strain-Induced Grain Growth during Rapid Thermal Cycling of Aluminum Interconnects,"* Metallurgical and Materials Transactions A — Physical Metallurgy 38A (13), 2263-2272, 2007.

D. T. Read, R. R. Keller, N. Barbosa III, and R. H. Geiss, *"Nanoindentation Round Robin on Thin Film Copper on Silicon,"* Metallurgical and Materials Transactions A—Physical Metallurgy 38A (13), 2242-2248, 2007.

High Throughput Measurements of Thermoelectric Materials for Cooling Applications

Technical Contacts:
M. L. Green
Winnie Wong-Ng

Goals

The objective of this project is to develop standard reference materials (SRMs), measurement methodologies, and comprehensive data sets (Seebeck coefficient, electrical conductivity, thermal conductivity) for thin film and bulk thermoelectric materials to validate measurement accuracy. This will lead to a better understanding of the structure/property relationships and the underlying physics of novel thermoelectric materials, and enable their development for solid state cooling applications. Our approach will facilitate comparison of thermoelectric data between leading laboratories and accelerate the commercialization of these materials.

Customer Needs

One of the most important impediments to further scaling of microelectronic devices is the removal of the prodigious heat dissipated as a result of their operation. Passive heat removal is no longer an option; device mounts and packages must employ active heat removal technology.

Thermoelectric materials, i.e., materials that can directly interconvert thermal and electrical energy, are being developed for two applications: solid state refrigeration, and vehicular engine waste heat recovery for electrical power generation. Solid state refrigeration of microelectronic devices using thermoelectric devices would result in greater operational efficiency and device reliability for the $120B U.S. semiconductor industry. In addition, thermoelectric based cooling devices are environmentally friendly, require minimal maintenance (no moving parts), and reliably offer quiet and compact operation.

Technical Strategy

Currently, the energy conversion efficiency of well-established, bulk thermoelectric materials is too low (<5 %) for cooling device applications. There have been reports of higher conversion efficiencies in thin film materials, but the material properties affecting device conversion efficiency, i.e., Seebeck coefficient, S; electrical conductivity, σ; and thermal conductivity, κ, are difficult to quantify or verify in thin film materials. Although there will be only limited applications for thin film thermoelectric cooling devices (because a ΔT of only 40 °C across a 2 μm film represents a thermal gradient of 2×10^7 °C/m, which is not possible to sustain by known thermal management techniques), thin films, especially combinatorial thin films, are useful vehicles for screening of candidate thermoelectric materials.

Our technical strategy is to develop standard reference materials (SRMs), measurement methods, and combinatorial materials methodologies to accelerate the commercial introduction of thermoelectric materials to the microelectronics market place. Thermoelectric SRMs and measurement methods will allow for interlaboratory validation of data, leading to more rapid commercialization of thermoelectric materials for solid-state cooling applications. Measurement methods, especially for the case of thin film thermoelectric materials, are not standardized, and there are currently no methods to accurately and reproducibly (laboratory to laboratory) measure the material properties that determine thermoelectric conversion efficiency, i.e., Seebeck coefficient (S), resistivity (ρ), and thermal conductivity (κ). High throughput combinatorial methodologies will be employed to generate comprehensive data sets (S, ρ, κ) for industrially relevant bulk and thin film thermoelectric materials. We will also collaborate with several industrial, university and government laboratories to generate the appropriate data sets and standard reference materials.

DELIVERABLES:

- Continue development of the thermal conductivity screening tool (including software) by testing the homogeneity of a representative film (1Q 2009)
- Complete low temperature Seebeck coefficient SRM (2Q 2009)
- Design and build high-temperature Seebeck coefficient measurement tool (3Q 2009)
- Complete development of the thermal conductivity screening tool (4Q 2009)

Accomplishments

In addition to equipping a new laboratory for thermoelectric property measurements, we accomplished two other goals: the certification of a bulk Standard Reference Material (SRM) for measurement of the low temperature Seebeck coefficient (chosen through an interlaboratory round robin survey of two candidate materials), and the development of two new thermoelectric metrology apparatuses, a scanning tool for Seebeck coefficient and resistivity measurements, and a scanning frequency domain thermoreflectance tool for thermal conductivity measurements. Both are designed to be combinatorially friendly, i.e., they are measurement techniques that can be made locally and rapidly on a bulk or thin film "library" sample.

The Seebeck coefficient round robin data were analyzed using a parametric model to generate common fitted curves for data generated from various laboratories (laboratories were at AIST (Japan), Michigan State University, Hi-Z Technology Corp., Quantum Design Corp., Clemson University, Naval Systems Weapons Center, U. Maryland, Oak Ridge National Labs, University of South Florida, GM Corp., and University of Michigan) using different measurement techniques and samples from the same batch. Of the two candidate materials, Bi_2Te_3 and Constantan (a copper-nickel alloy), we found that the coefficient of variance for Bi_2Te_3 was smaller across the entire temperature range compared to that of Constantan. Bi_2Te_3 also has a larger Seebeck coefficient than Constantan. We have therefore developed a Seebeck coefficient Standard Reference Material (SRM™), Te-doped Bi_2Te_3 (provided by Marlow Industries), to validate measurement accuracy.

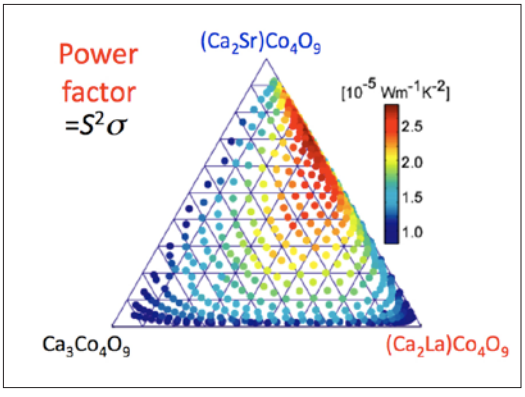

Figure 1. Power factor of a $(Ca,Sr,La)_3Co_4O_9$ film

Certification measurements were performed using two different techniques on 10 samples randomly selected from a batch of 390 bars, providing certified Seebeck coefficient values from 10 to 390 K. The primary measurement methodology utilized a modified Quantum Design PPMS and a custom, steady state, multiple gradient sweep technique. Secondary measurements were also performed using our commercial (PPMS, Quantum Design Corp.) tool, in a transient test mode.

Next, an automated Seebeck coefficient screening tool has been successfully designed and constructed. The tool consists of a probe and an automated translation stage to move the probe in the x, y, and z directions. This tool takes as little as 20 seconds to measure both electrical conductivity and Seebeck coefficient at each sample point; thus, over 1000 sample points can be measured within 6 hours. The tool's measurement capability has been demonstrated for a ternary composition library film of the thermoelectric system $(Ca\text{-}Sr\text{-}La)_3Co_4O_9$. The power factor (equal to the square of the Seebeck coefficient divided by the resistivity) for this material, Fig.1, is seen to peak between the Sr- and La-rich regions. We are currently modifying the thermoelectric probe to further decrease the thermal measurement uncertainty, and for use at elevated temperatures to enable screening of combinatorial films at their actual operating temperatures.

To compliment the Seebeck coefficient screening tool, we have also developed a scanning frequency domain thermoreflectance apparatus that can rapidly and locally (10 micrometer spot size) measure the thermal conductivity of combinatorial thin films. The principle of this technique is illustrated in Fig. 2, and a schematic of the apparatus is shown in Fig. 3. To do this, the thermoelectric film is coated with a 100 nm molybdenum layer and locally heated by an intensity modulated (1 MHz) infrared laser; the thermal response of the film is detected by the reflected beam of a second (probe) laser. Evaluation of the phase lag between the thermoreflectance and the heating laser signals enables one to determine the thermal effusivity b, equal to $(\kappa c\rho)^{1/2}$, where c is the specific heat, and ρ the density. A thermal effusivity calibration curve was obtained from bulk samples of SiO_2, $SrTiO_3$, $LaAlO_3$, Al_2O_3, and Si. Using this calibration, and applying a two layer

thermal mathematical model, the thermal conductivity of an yttria (Y_2O_3)-containing ternary oxide film was then determined. The measured value, 11.96 J(Kms)$^{-1}$, is within about 10 % of the reported value of 12.87 J(Kms)$^{-1}$. Combining the thermal conductivity data from this thermoreflectance apparatus and the thermoelectric screening probe, we can then calculate the energy conversion efficiency for different compositions on the combinatorial film.

We are also expanding our thermoelectric measurement capabilities by developing an advanced high temperature thermoelectric metrology apparatus that will concurrently measure resistivity and Seebeck coefficient from room temperature to 1200 K. Final construction of the apparatus is proceeding according to schedule and upon completion, will be used to certify an additional Seebeck coefficient SRM for use at high temperature (300 K – 1200 K).

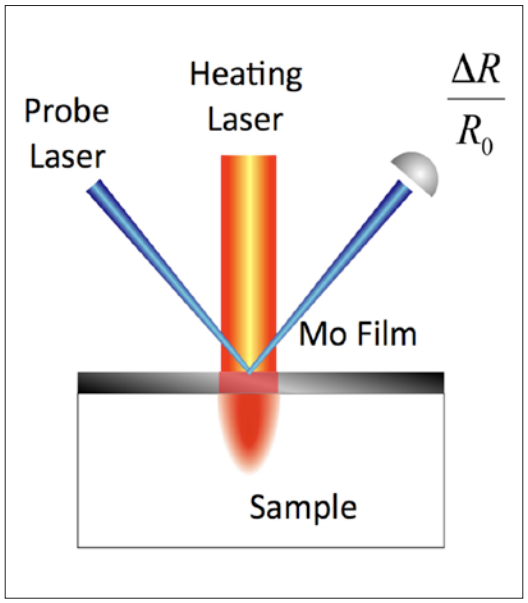

Figure 3. Schematic of the frequency domain thermoreflectance apparatus

We are also expanding our thermoelectric measurement capabilities by developing an advanced high temperature thermoelectric metrology apparatus that will concurrently measure resistivity and Seebeck coefficient from room temperature to 1200 K. Final construction of the apparatus is proceeding according to schedule and upon completion, will be used to certify an additional Seebeck coefficient SRM for use at high temperature (300 K – 1200 K).

Collaborations

- Low temperature Seebeck coeffiecient round robin study with eleven labs (AIST (Japan), Michigan State University, Hi-Z Technology Corp., Quantum Design Corp., Clemson University, Naval Systems Weapons Center, U. Maryland, Oak Ridge National Labs, University of South Florida, GM Corp., and University of Michigan).

- High temperature Seebeck coefficient effort started with GM CorporatioRecent Talks/Publications.

Publications and Talks

Publications

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Talks

Survey of High Temperature Thermoelectric Metrology, MRS, San Francisco, CA, April 16, 2009 (J. Martin).

Bi_2Te_3 as a Low Temperature Seebeck Coefficient Standard Reference Material (SRM™), MRS, San Francisco, CA, April 16, 2009 (W. Wong-Ng).

High-throughput screening system for Thermoelectric Material Exploration Based on Composition-Spread Approach M. Otani, N. D. Lowhorn, E. Thomas, W. Wong-Ng, P. K.

Schenck, and M. L. Green, eTherm 1st International Symposium on Thermodesign and Thermophysical Property for Electronics, June 18, 2008, Tsukuba, Japan (M. Otani).

High-throughput Seebeck Coefficient Screening System for thermoelectric materials Combinatorial Library Films, NIST Technology Transfer Showcase (TEDCO), April 8, 2008, NIST, Gaithersburg, MD (M. Otani).

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High-Throughput Seebeck Coefficient Screening System for Thermoelectric Materials Combinatorial Library Films, Thermoelectric Symposium, MRS, Nov. Boston, MA 2007 (M. Otani).

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Crystal Chemistry and Crystallography of the Type-II Clathrate, $Cs_8Na_{16}Ge_{136-x}A_{gx}$, and a Novel Phase, $Na_{1-x}Ge_{3+z}$, American Crystallographic Association annual meeting, Salt Lake City, Utah, July 22-26, 2007 (W. Wong-Ng).

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Pb-Free Surface Finishes for Electronic Components: Sn Whisker Growth

Goals

The microelectronic industry is faced with an extreme reliability issue due to Sn whisker induced failures. This project is providing data and materials measurements to improve the reliability of solder interconnects degraded by the switch to Pb-free technology. In particular the state of compressive stress and the localized creep response (whisker growth) of Sn-based, Pb-free electrodeposits are being measured. Industry will use these measurement methods and data to modify processing conditions to mitigate the formation of Sn whiskers.

Customer Needs

Sn is widely used as a coating in the electronics industry because it provides excellent solderability, ductility, electrical conductivity, and corrosion resistance. However, Sn whiskers have been observed to grow spontaneously from Sn electrodeposits and are known to cause short circuits in fine pitched pre-tinned electrical components. In the 1960s, the addition of a few percent of Pb to Sn was found to greatly reduce the tendency to form whiskers. However, recent demand for Pb-free surface finishes for ecological reasons has renewed interest in understanding whisker growth and developing whisker mitigation strategies. It is widely recognized that compressive stress is a necessary, but insufficient, condition for whisker growth.

The U.S. microelectronics industry needs a method to measure stress in the Sn electrodeposited surface finishes of electronic components to predict the propensity of whisker growth before these components are assembled on circuit boards to prevent the loss of both revenue and life from Sn whisker failures. The 2009 International Electronics Manufacturing Initiative (iNEMI), and 2006–2007 IPC technology roadmaps clearly articulate the need for Sn whisker research. In order to prevent or mitigate whisker growth, workshops sponsored by industry and academia have reached a consensus list of concerns: understand the influence of electroplating conditions, grain structure/shape/orientation, and compressive stress in the electrodeposits, intermetallic compound (IMC) formation at the SnCu interface, diffusion of Sn, and thermal cycling effects on electroplated components.

Mitigation strategies being investigated include the elimination of columnar grain shape and elimination of intermetallic reaction with the substrate. Focused ion beam (FIB) milling removes metal and reveals a cross section of the internal microstructure so that changes in grain structure can be directly correlated to whisker growth. Also models of stress accumulation and relaxation are used to interpret the stress measurements and describe whisker/hillock growth.

Technical Strategy

Our work on Pb-free electrodeposits is focused on the measurement of stress and modeling Sn grain growth. Two methods are currently used for electrodeposited Sn surface finishes: (1) X-ray measurement. (2) Optical stress measurement during and after electrodeposition by wafer curvature technique. Although it is easy to obtain stress values from these techniques, understanding the source of measurement errors is undeveloped. Errors can be a significant fraction of the measured quantity. Electroplated Sn has a preferred crystallographic orientation that can vary depending on plating conditions. Sn is a low melting metal (0.6 TM at RT), with a low yield strength (~ 30 MPa) that creeps at room temperature. These factors as well as geometrical, diffraction, and optical subtleties complicate both measurement methods. The techniques also have disparate temporal and spatial resolution that measure different aspects of the stress. Modeling efforts are being used to gain fundamental insight into the processes that cause the upward thrust of the Sn during hillock and whisker growth.

DELIVERABLES:

- Complete manuscript, “Effect of Current Density and Electrolyte Concentration on Hillock Growth from Pure Sn Electrodeposits.” 2Q 2009
- Collect data using simultaneous wafer curvature and x-ray diffraction stress measurements on a series of Sn and Sn alloy electrodeposits with varying thicknesses. 3Q 2009
- Complete manuscript, “Stimulation of Sn Whisker Growth Using Micro-indentation.” 4Q 2009
- Complete manuscript, “A Comparison of Stress Measurement in Sn and Sn Alloy Electrodeposits Using Cantilever Beams and X-Ray Diffraction.” 1Q 2010

Technical Contacts:
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G. R. Stafford
M. E. Williams

“NIST’s involvement in the iNEMI Tin Whisker project work has been a great asset to the team. Their diligence in generating and sharing data has been instrumental in making progress in this field. They are a great technical asset and are always willing to help design tests and generate data when needed”.

Dr. Richard D. Parker
Lead Technologist, Delphi Electronics & Safety
Advanced Assembly Technologies
Kokomo, IN 46904-9005

Accomplishments

■ *NIST workshop "Methods for measuring residual stress in Sn and Sn alloy electrodeposits"* – NIST sponsored a workshop in April 2008 to assess the state of the art of measurement methods of residual stress in Pb-free electrodeposits. Thirty researchers from industry, government labs and universities attended. The benefits and difficulties with both X-ray diffraction (sine squared Ψ) and wafer/beam curvature methods of stress measurement were discussed. Topics included: precision and accuracy of measurements; interpretation of measurements, e.g. spatial resolution, macro- and micro- stress; orientation (texture) effects; grain shape effects, stress gradients in the deposit; and Sn-Cu intermetallic growth induced stress. Although it is easy to obtain stress values from these techniques, understanding the source of measurement errors and the interpretation of the results is underdeveloped. Some conclusions of the workshop are:

- Need technique for obtaining diffraction information from controlled depths of the electrodeposit.
- Need microdiffraction method that can measure local lattice rotation and strain.
- A best practice guide for x-ray measurement of stress in Sn electrodeposits should be prepared.
- Need to assess the effect of non-uniformity of the diffraction cone and the impact of the cone portion used on the accuracy and precision of x-ray stress measurements.
- Measured curvature is due to contributions of several different layers in the electrodeposit not just Sn and these other contributions need to be separated.
- Get more federal funding for coordinated effort.
- Select a definitive experiment to measure stress and orientation in individual grains in Sn and compare results to average stress measured with the sin2 ψ method.

■ *Stimulation of Sn Whisker Growth Using Micro-indentation* - Sn whiskers can grow spontaneously from Sn electrodeposits under various conditions. The necessary compressive stress for this growth can come from different sources such as the deposition process, intermetallic growth, or an external mechanical force. We used micro-indentation to apply varying loads to the Sn electrodeposit with three different indenter shapes: a sharpened tubular indenter, standard 0.5 mm ball indenter and a Berkovich indenter. At certain loads, whisker growth was observed within minutes around the indent. The location of the whiskers around the indent were then correlated to the residual stresses predicted using finite elemental modeling (FEM) for the tube and ball indenters. The results of this work suggest the importance of the bi-axial in-plane compressive stress for whisker and hillock growth.

■ *Measurement of Stress in electrodeposits* - We have measured the stress of electrodeposited bright Sn and Sn alloys as a function of time for several days after plating with two different techniques: sin2 ψ x-ray diffraction and cantilever beam deflection. The deflection of the cantilever beam is a measure of the average stress in the film. The x-ray diffraction method measures the lattice strain in a volume of Sn near the surface of the electrodeposit. The preferred orientation of the deposits and the low stress levels (~ 10 MPa) presented many challenges for this technique. A protocol for simultaneous stress measurements using both methods has been developed. Most interesting are the results for 7 μm thick deposits that generally show a short term relaxation of the compressive stress followed by a long time increase in compressive stress. The initial stress is due to the plating process itself. This stress begins to relax but at a later time the compressive stress increases due to slow growth of the Cu_6Sn_5 intermetallic between the Sn and the Cu substrate. This is consistent with the ideas of Boettinger, et al., 2005.

■ *Current Study* - The effect of current density and tin methanesulfonate concentration on the plating efficiency, hillock density, columnar grain size, crystallographic texture, and residual stress is measured. We employed the rotating-disc electrode method to obtain uniform mass transport in a reproducible manner. In particular we investigate situations that include transport

limited growth at less than full plating efficiency. High current with a plating efficiency of ~60 % was found to produce large compressive residual stress yet very few hillocks. In the present study we evaluate the effect of current density and the Sn^{2+} concentration in the electrolyte.

■ *Modeling - The mechanisms of hillock and whisker gro*wth remain largely unknown. In stressed solids, surface evolution is often driven by grain boundary diffusion and can result in growth of hillocks and whiskers. Figure 1 shows possible diffusion paths of Sn atoms to feed the base of a whisker grain. The 3-D path of Sn atoms to relieve stress is along columnar grain faces (arrows) within the deposit. Accretion of Sn on the wedge-shaped grain faces forces the whisker/hillock above the deposit surface.

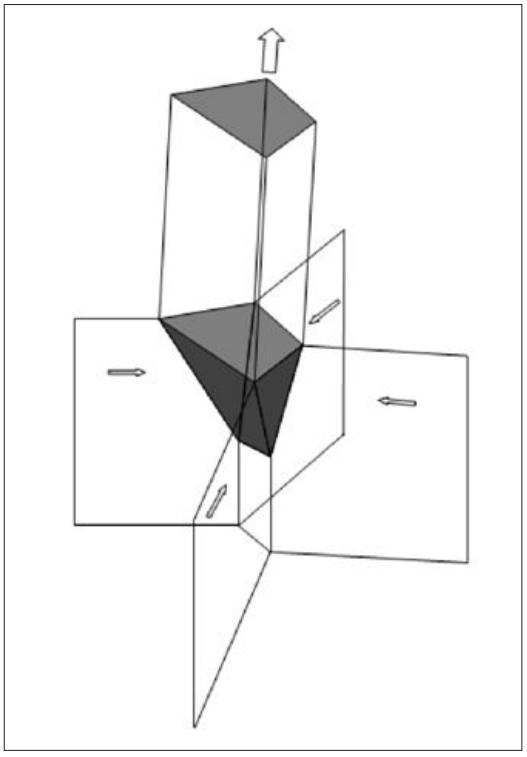

Figure 1. The 3-D path of Sn atoms to relieve stress is along columnar grain faces (arrows) within the deposit. Accretion of Sn on the wedge-shaped grain faces forces the whisker/hillock above the deposit surface.

As a preliminary attempt at modeling this situation we have preformed molecular dynamic simulation of a simpler geometry. These simulations have been performed to understand the conditions (stress, temperature, grain boundary diffusion, surface diffusion) under which the hillock/whisker growth processes can be initiated. The simulated geometry was a tri-crystal with a wedge-shape surface grain penetrating down the triple line. The applied compressive stress caused the wedge grain to grow upward and out of the surface as in whisker/hillock growth. It was determined that only two of the three interior grain boundaries were capable of supplying Sn atoms to the base of the whisker/hillock grain. Thus the whisker/hillock was pushed up but at an angle to the free surface.

■ *Participation in iNEMI working groups* - NIST remains an active participant in the Sn Whisker Group with bi-weekly teleconferences and round robin experiments (members include Alcatel-Lucent, Cisco Systems, Cookson, Delphi Delco, Freescale, Hewlett Packard, IBM, Intel, Intersil, IPC, Motorola, Rohm & Haas Electronic Materials, Soldering Tech, Solectron, Sun Microsystems, Texas Instruments, and Tyco Electronics).

Collaborations

In an effort to develop a standard X-ray diffraction method to measure stress in Sn electrodeposits we are conducting round robin experiments with Dr. Robert Hilty of Tyco Electronics located in Middletown, PA.

NIST provided advice and expertise to Univ. of Maryland group for the production of fast growing whisker samples of Sn-Cu electrodeposits on Zn substrates for tests of acrylic conformal coatings. These samples can reduce the evaluation time of the coatings used by industry as a whisker mitigation method to prevent whisker related failures of electronic devices.

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Univ.), *"Chapter 2: Fundamental Properties of Pb-Free Solder Alloys",* Springer Press, in Pb-Free Soldering, ed J.S. Bath, ISBN978-0-387-32466-1, 2007.

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Process Metrology Program

Device scaling has been the primary means by which the semiconductor industry has achieved unprecedented gains in productivity and performance quantified by Moore's Law. Until recently only modest changes in the materials used have been made. The industry was able to rely almost exclusively on the three most abundant elements on Earth — silicon, oxygen, and aluminum.

Copper is now predominantly the conductor of choice over aluminum because of its intrinsic higher conductivity. A variety of low-dielectric constant materials are being introduced to reduce parasitic capacitance, replacing silicon dioxide. As dimensions continue to shrink, the traditional silicon dioxide gate dielectric thickness has been reduced to the point where tunneling current has become significant and is compromising the performance of the transistors. This is requiring the introduction of higher dielectric constant materials. Initially the addition of nitrogen to the gate material was sufficient, but now more exotic materials such as transition metal oxides, silicates, and aluminates are being introduced. Additionally, the gate conductor, traditionally polysilicon, is being replaced by metal or metal silicide to eliminate the polysilicon depletion effect. With the replacement of the traditional silicon dioxide/polysilicon gate stack processes with materials capable of supporting ever shrinking geometries, the task of the industry becomes more difficult. The overall task represented by the projects below reflects the need for analytical techniques with unparalleled spatial resolution, accuracy, robustness and ease of use.

Water and other contaminants at extremely low levels in process gases present serious manufacturing difficulties. Accurate calibration of water vapor and other contaminants at extremely low vapor pressures is required.

Atomic layer deposition processes are increasingly being used for high quality thin dielectrics and conductors. Techniques for understanding the deposition mechanisms and characterizing the compounds that are formed are being developed. Theoretical studies elucidating the thermodynamics and quantum mechanical properties of these compounds are being conducted.

Low Concentration of Humidity Standards

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"The LFPG is the 'Gold' standard for moisture generation and after the round robin experiments it is possible for the industry to talk about moisture measurements that can be compared to the standard."

Suhas Ketkar,
Air Products and Chemicals

Goals

The primary objective is to establish quantitative standards enabling the accurate measurement of trace quantities of water vapor ($< 10^{13}$ molecules cm^{-3}). This effort supports the development and application of commercial humidity sensors used for gas purity measurements and inline monitoring and process control — functions that are relevant to minimizing wafer misprocessing.

Customer Needs

Measurement needs and technical challenges for airborne molecular contamination (AMC) in semiconductor wafer processing spanning the next 15 years are given in the 2007 International Technology Roadmap for Semiconductors (ITRS) http://public.itrs.net/. A key measure of technological progress defined in the ITRS is yield enhancement (YE) which is the process of improving baseline yield for a given technology generation from R&D yield level to mature yield. AMC affects YE and constitutes a major impediment to wafer environment contamination control particularly for 300 mm wafer manufacturing processes. VLSI Research Inc. estimates that "a 1 % yield increase equates to $1M per day additional profits for a modern 300 mm fabrication line," The Chip Insider®. The ITRS also states "The impact of AMC on wafer processing can only be expected to become more deleterious as device dimensions decrease. There is a need for better AMC monitoring instrumentation ... to measure AMC at the part per trillion level … low cost, routine monitoring may be required as devices approach molecular dimensions." Target impurity levels relevant to wafer environmental contamination control for a number of AMC including H_2O, THC, CO_2 and other AMCs in various bulk gases, which are given in ITRS Tables YE 9a and b, quantify the measurement needs in a variety of wafer production processes. Of these impurities, water vapor is one of the most ubiquitous and difficult to eliminate. Similarly, the Semiconductor Equipment Manufacturers International (SEMI) has standards describing the production and delivery and value assignment of ultra-high purity gases for semiconductor manufacturing http://downloads.semi.org/PUBS/SEMIPUBS.NSF/webstandardsgases. These standards illustrate the stringent requirements for gas purity measurements in semiconductor processes. We also note a new emphasis (beginning with the 2004 ITRS) on epitaxial processes that use gases as source materials, including SiGe and III-V semiconductor requirements for power amplifiers and extension of physical models to III-V semiconductors.

Although a variety of high sensitivity sensors of water vapor are available, most do not directly measure water in the gas phase. Rather, they typically respond to moisture-induced changes in bulk or surface properties associated with the adsorption of water vapor. Consequently, a rigorous first-principles determination of sensor response is often precluded, thus compromising accuracy. Moreover, since many such devices exhibit drift and poor reproducibility, frequent recalibration is required. Interpretation of these measurements is also complicated by complex physical interactions of water vapor with technical surfaces in transfer lines, in reaction chambers and in sensor housings.

Technical Strategy

The development of accurate and robust water vapor sensors requires well-characterized reference standards against which such devices can be evaluated. This should include a primary method of measurement for water vapor concentration and a complementary method yielding high-precision and stable sources of water vapor. By providing access and traceability to the unique capabilities at NIST discussed below, instrument manufacturers and sensor users can assess the overall performance and accuracy of their measurements.

Our strategy is to establish complementary capabilities in high-precision generation and measurement of water vapor. To address these respective needs, we have developed a thermodynamically based humidity source and the high-sensitivity optical absorption measurement methods discussed below. The thermodynamic humidity source, known as the Low Frost-Point Generator (LFPG) (see Fig. 1 and Fig. 2), serves as the project cornerstone and is capable of delivering 3 nmol to 3 mmol of water vapor per mole of dry gas. Here the water vapor concentration in a gas stream is precisely controlled by active regulation of the saturator temperature and pressure. As such, the LFPG is ideally suited for testing the performance of various sensing and humidity generation technologies. To date, it is has been used to characterize water vapor measurement

and generation systems at the research and development stage as well as commercial devices. In its standard mode of operation, the LFPG is currently limited to generating greater than 3 nmol mol^{-1} of water vapor in N^2 based on the minimum achievable temperature of the saturator. We now regularly generate humidity levels below 1 nmol mol^{-1} using dry-gas dilution of the water vapor/gas mixtures produced by the LFPG output stream.

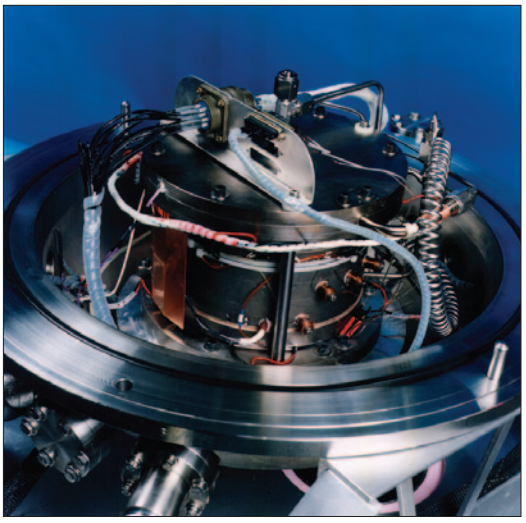

Figure 1. NIST Low Frost-Point (humidity) Generator.

A common technology used by the semiconductor industry for delivering controlled quantities of water vapor is based upon the controlled permeation of water vapor (called permeation tube generator (PTG)) through a material, followed by mixing and dilution with a dry gas of known flow rate. We have constructed a calibration system for water permeation tubes, comparing permeation tubes to the LFPG using a commercial water vapor sensor as a nulling device. This approach constitutes an efficient and low-cost mechanism for the dissemination of NIST trace humidity standards.

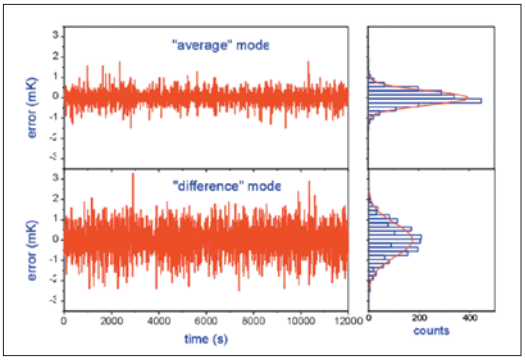

Figure 2. Steady state response of saturator control thermometers in NIST Low Frost-Point Humidity Generator.

1. As part of the NIST mission to provide reliable measurement standards, we compare our standards with those of other nations. These international comparisons are conducted under strict guidelines, with all results blind to the participants until the completion of the comparison.

DELIVERABLES:

- Commission calibration service. 2Q 2008

2. In its standard mode of operation, the LFPG is currently limited to generating greater than 3 nmol mol^{-1} of water vapor in N_2 based on the minimum achievable temperature of the saturator. We now regularly generate pmol mol^{-1}-levels of humidity using dry-gas dilution of the water vapor/gas mixtures produced by the LFPG output stream. We have validated the technique and established the uncertainties with a variety of self-consistency tests. Development of gas-handling manifolds with ultra-low adsorption/desorption of water will be a key focus of our work in the next year.

DELIVERABLES:

- Complete a pilot study for an international comparison of humidity generators for the concentration range (10 to 10000) nmol mol^{-1}. 4Q 2009
- Complete paper on pilot study results for the concentration range (10 to 10000) nmol mol^{-1}. 2Q 2010

2. To complement our established capability in precision generation of trace humidity levels, we are developing absolute techniques based upon the absorption of visible and near-infrared laser radiation. Water vapor has an absorption spectrum comprising thousands of distinct vibrational absorption transitions in this spectral region. Thus, the concentration of water vapor can be readily determined in terms of measurements of sample absorbance and independently determined absorption line intensities. Recent advances in source and detector technology, and new spectroscopic techniques that extend the sensitivity of laser absorption measurements now enable the precise sensing of water vapor at concentrations below 1010 molecules cm^{-3}. To account for line broadening effects, and mitigate interference effects associated with absorption by other species the most precise absorption measurements require that individual transitions be spectrally resolved. This demands a technique having a frequency resolution much smaller than the characteristic widths of the absorption transitions,

and requires that the frequency intervals in the measured spectrum be accurately determined. By combining high spectral resolution with high precision absorbance measurements, the water vapor concentration can be found independently of the composition of the carrier gas. Of the optical absorption methods, cavity ring-down spectroscopy (CRDS) is expected to be the most suitable for a primary method (Fig. 3). CRDS is a cavity-enhanced optical absorption technique that has high sensitivity, fast response, and probes a compact well-defined volume. It is important to emphasize that under certain conditions, CRDS can exhibit exceptional spectral resolution, enabling detailed measurements of absorption line shape. To this end, we have developed a refined version of CRDS called frequency-stabilized cavity ring-down spectroscopy (FS-CRDS). Here, the ring-down cavity is actively length stabilized, the probe laser is frequency locked to the ring-down cavity, and the frequency axis of the spectra is based upon the longitudinal mode spacing of the ring-down cavity. Taking advantage of the high spectral resolution afforded by FS-CRDS, various line shape effects such as speed-dependent pressure-broadening and collisional narrowing of these transition line shapes by various media can now be quantified.

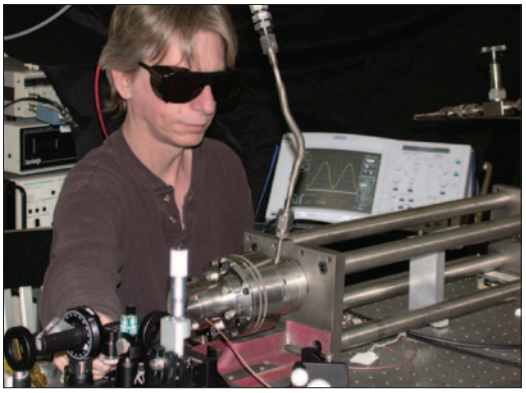

Figure 3. Frequency-stabilized CRDS system.

We are making low uncertainty measurements of near-infrared water vapor line intensities from FS-CRDS spectra of water vapor samples provided by the LFPG humidity standard. We are also comparing our FS-CRDS measurements (10 nmol mol^{-1} to 10 mmol mol^{-1} molar fraction range of water vapor) with those measured by a commercial CRDS-based hygrometer.

DELIVERABLES:

- Fabricate new cell with reduced background levels. 3Q 2009.
- Using new cell, perform direct comparison of FS-CRDS system with commercial CRDS system 4Q 2009
- Using FS-CRDS apparatus with new cell, quantify the correlation between water vapor concentration and LFPG frost-point temperature. 1Q 2010

3. Moisture contamination is a serious problem in phosphine, arsine, silane, ammonia, and similar gases used in the epitaxial growth of high-purity semiconductor layers. Gas manufacturers have been lacking adequate instruments to refine their products, and end-users are unable to measure contamination in transferring gases from cylinder to process tool. The critical concentrations of the impurities are not well known; however, it is believed that >10 nmol mol^{-1} oxygen or water in most process gases is undesirable. Optical methods for measuring the moisture impurity concentrations combine high sensitivity and straight-forward traceability through the LFPG absorption line strength measurements. Researchers at NIST have developed a CRDS system similar to the ones described in the previous sections but linked with a semiconductor crystal growth system to measure H_2O at very low concentrations in semiconductor source gases. The system was rebuilt in 2005-2006 to improve performance, to enable side-by-side tests with commercial instrumentation, and to allow greater flexibility in correlating gas purity with semiconductor growth results. We have completed measurements the lineshape, absorption coefficients, and frequency of optical transitions for water, phosphine, arsine, and ammonia in the vicinity of 940 nm. This information is critical to facilitate the use of high-sensitivity spectroscopy techniques in these gases.

Our ongoing research with state-of-the-art lasers allows us to try new spectral regions and methods that have not previously been explored with cavity resonance spectroscopy. While cavity ring-down spectroscopy offers high sensitivity with minimal calibration, it is generally only practical over a single molecular absorption line and therefore limited to the detection of a single molecular species. The broadband cavity-enhanced absorption methods being developed by Jun Ye's team at JILA in Boulder, CO, are being applied in our laboratory to measure multiple impurities in arsine. Matheson collaborators are also contributing to this effort to measure H_2O, CO_2, C_2H_6, CH_4, SiH_4, and H_2S in arsine. The JILA method makes use of a custom frequency comb laser tunable from 1700 to 1900 nm. Future

plans include exploration of the mid-IR region near 2700 nm for greater sensitivity. The CRDS capability should ultimately lead to improvements in semiconductor source gas purity, which will allow crystal growers to choose less expensive growth conditions without sacrificing optical emission efficiency and yield in LEDs, semiconductor lasers, and photodetectors.

DELIVERABLES:

- Publish arsine and phosphine spectra with pressure broadening coefficients for line at 943.082 nm. 4Q2009

Test frequency comb laser for sensitivity to H_2O, CH_4, CO_2, C_2H_6 , SiH_4, and H_2S in arsine. 3Q 2009

Accomplishments

■ In FY 2008, we investigated fifteen H2O transition line shapes and line intensities using the 1380-nm FS-CRDS apparatus in conjunction with the LFPG primary humidity standard. We measured line intensities with relative standard uncertainties <0.4 %, and obtained 1.5 % agreement between these measurements and ab initio water vapor intensity calculations.

■ We have constructed a permeation tube calibration facility (see Fig. 4). The purpose of this system is to provide measurement traceability for industrial users of permeation tube humidity generators. The calibration system comprises a custom PTG, the LFPG and either a high-sensitivity quartz crystal microbalance (QCM) or commercial CRDS hygrometer. The water-containing permeation tubes to be calibrated are placed inside the temperature-stabilized PTG oven. Water vapor diffuses from the tube surface into a precisely controlled stream of purified N_2. The diluent gas flow rate is adjusted so that the water vapor concentration produced by the PTG is equivalent to that produced by the LFPG, as measured by the QCM. From these measurements the water permeation rate of the tube under test can be determined in terms of the known LFPG output. As seen in Fig. 5, the calibrations derived from this system are repeatable to approximately 1 %, which is significantly superior to traditional gravimetric methods. We have performed multiple replicate runs with this system, and have used the resulting data to complete the uncertainty analysis of this system.

Figure 4. New PTG calibration apparatus.

■ A new strategy for pmol mol^{-1} (ppt)-level humidity generation has been successfully implemented. The approach, shown in Fig. 6, involves the controlled dilution of water vapor/gas mixtures produced by the LFPG, using a flow dilution system similar to that incorporated within the PTG calibration system described above. At mole fractions below 10^{-9}, the uncertainty in water vapor mole fraction is dominated by water vapor background produced by adsorption/desorption of water on internal plumbing surfaces and by water vapor remaining in the diluent after purification. We performed three sets of measurements to validate the method. First, the same nominal output concentration was produced while varying both the water vapor concentration produced by the Low Frost-Point Generator and the level of flow dilution. Deviations from a constant concentration were measured. Second,

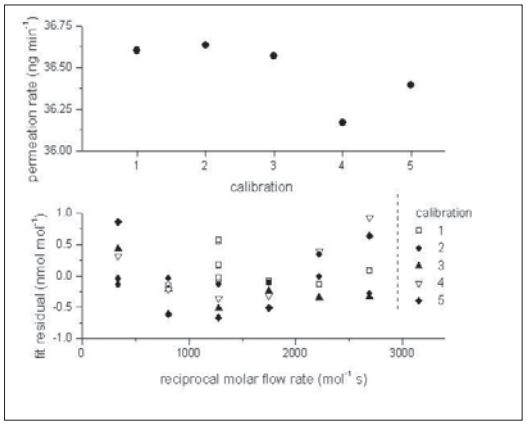

Figure 5. Calibration repeatability (top) and deviations from the fitting function (bottom) of a water-vapor permeation tube in the NIST Permeation Tube Calibration Facility.

the calculated water vapor mole fraction of the diluted generator output was compared against the reading of a commercial hygrometer based on cavity ring-down spectroscopy. Third, we measured the water remaining in the diluent gas after purification at various flowrates both with and without an additional cryotrap. An approximate water background of 0.3×10^{-9} was inferred from the data, and the results were consistent within the combined uncertainty of the LFPG output and the water background.

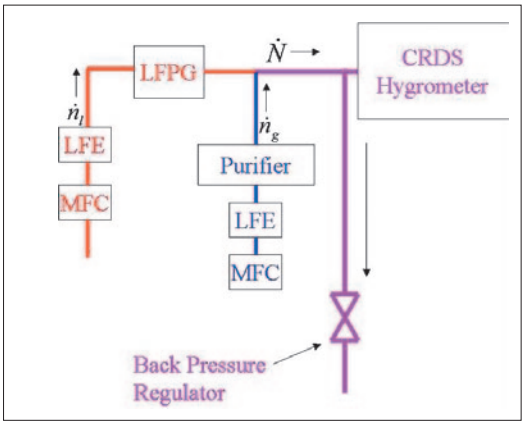

Figure 6. Dilution system for extending the LFPG operating range to pmol mol^{-1} levels.

■ The LFPG uncertainty analysis is based on the uncertainties in temperature and pressure within the LFPG saturator, ice vapor pressure, and the enhancement factor for mixtures of water vapor and air. However, this analysis neglects background effects associated with the transient adsorption and desorption of water vapor from internal surfaces in the flow manifold located downstream of the LFPG. For the lowest range considered, such processes may significantly affect the water vapor concentration in the sample gas delivered by the LFPG to test instrumentation. In collaboration with Air Products Inc., we quantified the magnitude of this water vapor background using atmospheric pressure ionization mass spectrometry (APIMS). The results, shown in Fig. 7, indicate that the background contribution to H_2O from system components downstream of the LFPG was less than 0.2 nmol/mol. These measurements also demonstrated that linearity deviations of the LFPG output H_2O mole fraction are less than 0.1 nmol/mol.

■ We are participating in two international comparisons of humidity generation stan-

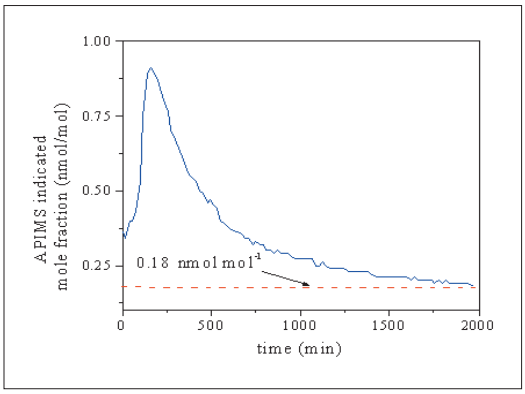

Figure 7. APIMS measurement of LFPG background H_2O concentration showing decay to steady state level.

dards. Measurements of test gas produced by the LFPG were performed at frost-point temperatures between -50 ºC and -10 ºC and were included in a key comparison of humidity generators that was organized by Working Group 6 of the Consultative Committee on Thermometry (CCT), part of the Bureau International des Poids et Mesures (BIPM). We are also participating in an exploratory study of trace humidity generators over the humidity concentration range from 10 to 20000 parts per billion of water vapor in nitrogen. Four national metrology institutes are participating, including NIST, the National Physical Laboratory (NPL,UK), Physikalisch-Technische Bundesanstalt (PTB, Germany), and the National Metrology Institute of Japan (NMIJ, Japan). NIST and NPL are acting as pilot laboratories in this study.

■ We have successfully developed an FS-CRDS system with automated spectral scanning capability to measure the absorption coefficient of trace quantities of water vapor. In FY 2005 the FS-CRDS method was used to probe H_2O absorption transitions in the 935 nm spectral region, and a spectral resolution of 50 kHz and reproducibility better than 0.25 % were demonstrated. In conjunction with humidity standards for determination of water vapor concentration, these spectroscopic measurements yielded relative uncertainties in line intensities less than 0.5 %. Figure 8 shows measured spectra (symbols) and theoretical spectra (solid lines) for a pair of overlapping water vapor absorption transitions, each case corresponding to a given total gas pressure (with N_2 as the buffer gas). These results illustrate that the spectral resolution and linearity of the FS-CRDS method enable

precise quantification of pressure broadening, collisional narrowing and asymmetries of the absorption line shape, thus minimizing systematic errors in the determination of number density and line intensity that typically arise from instrumental line broadening effects. Also, detection limits less than 10 nmol mol^{-1} of H_2O in N_2 have been demonstrated, using the relatively weak absorption lines near 935 nm. In FY 2006, we constructed a portable FS-CRDS apparatus to probe H_2O absorption in the 1.39 µm region, and we tested its performance using a transfer standard permeation tube water vapor source and a transfer standard hygrometer linked to the LFPG. We measured spectra with signal to noise ratios exceeding 2500:1 and we demonstrated a water vapor detection limit of 0.7 nmol mol-1. In another FS-CRDS study in FY 2006, we made high-resolution measurements of blended water vapor spectra demonstrating the ability to deconvolute closely space overlapping lines. In this study, line intensities were determined with relative uncertainties of 0.6 %.

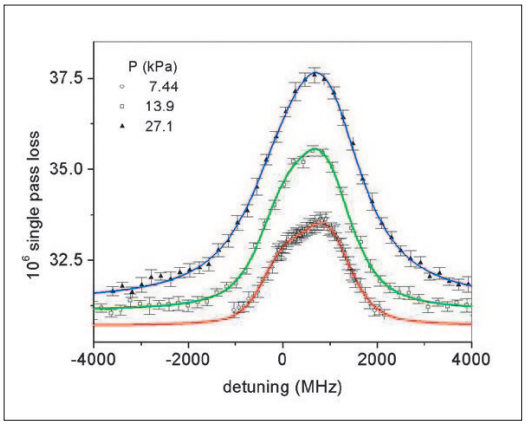

Figure 8. High-resolution FSSM-CRDS spectrum of a pair of pressure-broadened water vapor absorption transitions. Symbols are experimental points, and lines are Voigt fits to the measured profiles.

■ In collaboration with Matheson Tri-Gas and Tiger Optics, we demonstrated sensitivity of less than 10 nmol/mol for H_2O in phosphine using commercially available instrumentation, the first such measurement with this low sensitivity (see Fig. 9).

■ We have identified the best absorption lines for water vapor concentrations in the toxic gases phosphine and arsine in the 940 nm spectral region. Testing of both arsine and phosphine in this spectral region indicated that the least overlap with host gas lines, and hence the highest sensitivity to water contamination, is present for the H_2O line at 943.082 nm. Future experiments will characterize this line for pressure broadening coefficients and ultimate sensitivity limits. Figure 10 shows the pressure broadening effect for typical H_2O spectra in arsine.

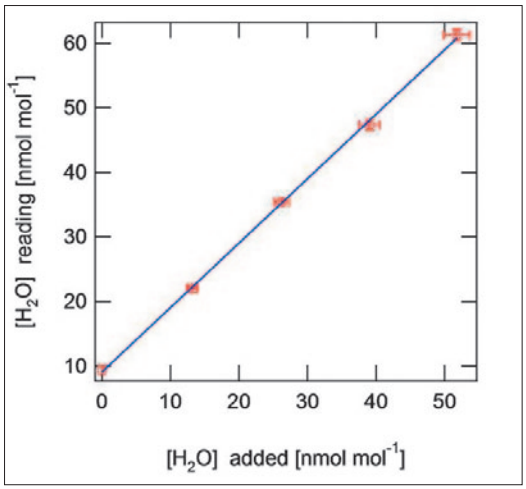

Figure 9. Response curve for commercial instrument measuring H_2O in phosphine with sensitivity of 1.3 nmol mol^{-1}.Zero offset of 9 nmol mol^{-1} is most likely from residual H_2O in phosphine.

Collaborations

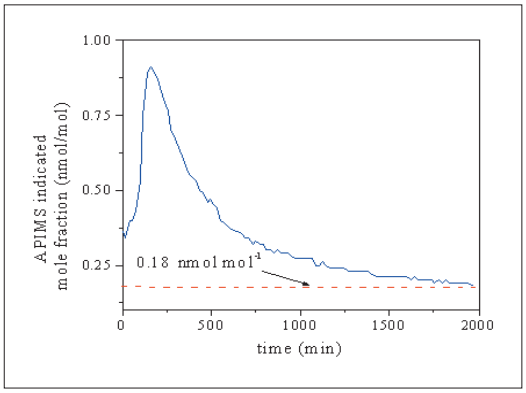

Figure 10. Pressure dependence of the absorbance spectra for H_2O in arsine showing feasibility of measuring H_2O concentrations on the order of 50 nmol mol^{-1} of various process pressures.

Air Products and Chemicals Inc., Seksan Dheandhanoo; APIMS measurements of trace moisture and characterization of semiconductor gas purity.

Matheson Tri-Gas, Mark Raynor and Jun Feng; CRDS measurements of trace moisture in phosphine.

Joint Institute for Laboratory Astrophysics (JILA), University of Colorado and NIST, Boulder, Prof. Jun Ye, Kevin Cossel, Florian Adler, cavity enhancement broadband absorption measurements for detection of multiple impurities.

Tiger Optics, Yu Chen; CRDS measurements of trace moisture in phosphine.

Dow Chemical, Linh Le and J. D. Tate; CRDS measurements for process gas control RH Systems, Robert Hardy; Characterization of low range chilled-mirror hygrometers and humidity generators for standards laboratories.

Southwest Sciences Inc, Chris Hovde.; Development of wavelength modulation laser hygrometer for trace H_2O sensing.

Tiger Optics, Calvin Krusen ; evaluation of commercial CRDS technology.

Air Products and Chemicals Inc.; CRDS measurements of trace H_2O in corrosive process gases.

Restek Corporation, David Smith; drydown rates for stainless steel tubing.

Publications

D. Lisak, D.K. Havey and J.T. Hodges, *"High-accuracy spectroscopic line parameters of water vapor for rotation-vibration transitions near 7180 cm^{-1},"* Physical Review A., in press.

R. Ciuryło, D. Lisak, and J.T. Hodges, *"Semi-classical line shape models of rovibrational H_2O spectroscopy tested using frequency-stabilized cavity ring-down spectroscopy,"* Proceedings of the 19th International Conference on Spectral Line Shapes, June 15-20, 2008, Valladolid Spain.

J. T. Hodges, D. Lisak, N. Lavrentieva, A. Bykov, L. Sinitsa, J. Tennyson, R. J. Barber, R. N. Tolchenov, *"Comparison between theoretical calculations and high-resolution measurements of pressure broadening for near-infrared water spectra,"* Journal of Molecular Spectroscopy, J. Mol. Spec. 249, 86-94 (2008).

G.E. Scace and W. W. Miller, *"Calibration of Water Permeation Tubes,"* NIST Special Publication 250-82 (2008).

G.E. Scace and W. W. Miller, *"Reducing the Uncertainty of Industrial Trace Humidity Generators through NIST Permeation-Tube Calibration,"* Int. J. Thermophys. 29, 1544 (2008).

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D. Lisak and J. T. Hodges, *"High-resolution cavity ring-down spectroscopy measurements of blended H_2O transitions,"* Appl. Phys. B 88, 317 -325 (2007).

H. H. Funke, M.W. Raynor, K.A. Bertness, and Y. Chen, *"Detection of Trace Water Vapor in High-Purity Phosphine using Cavity Ring-down Spectroscopy,"* Applied Spectroscopy, 61 (2007): p. 419-423.

G. E. Scace, W. W.Miller, *"Reducing the Uncertainty of Industrial Trace Humidity Generators through NIST Permeation-Tube Calibration,"* International Journal of Thermophysics, DOI 10.1007/s10765-007-0339-z.

J. T. Hodges and D. Lisak, *"Frequency-stabilized cavity ring-down spectrometer for high-sensitivity measurements of water vapor concentration,"* Applied Physics B, 85, 375 (2006).

G. E. Scace, *"Generating Parts per Trillion Levels of Water Vapor in Nitrogen,"* in Proc. 5th International Symposium on Humidity and Moisture, Rio de Janiero, 2006 (on CD, ISBN 978-85-86920-04-2).

J. T. Hodges and G. E. Scace, *"Developing advanced humidity standards to measure trace water vapor in specialty gases,"* Micro, 24, 59 (2006).

D. Lisak, J. T. Hodges and R. Ciurylo *"Comparison of semi-classical line shape models to rovibrational H_2O spectra measured by frequency-stabilized cavity ring-down spectroscopy,"* Phys. Rev. A., 73, 012507 (2006).

Physical Properties of Liquid Precursors

Technical Contacts:
R. Berg

Goals

New materials used in gas phase processes will require new measurements and standards for their efficient delivery to the wafer surface. The National Institute of Standards and Technology (NIST) is supplementing its project to measure the thermophysical properties of semiconductor gases with a new effort to measure the relevant properties of liquid precursors. Vapor pressure is the most important property because it controls the behavior of vapor delivery devices. Therefore, the project's first goal is to produce accurate vapor pressure data for relevant liquid precursors from room temperature to as high as 200 °C. Such data will improve the modeling of chemical vapor deposition processes and the design and use of bubblers and other devices that deliver precursor vapors. Other goals are to characterize the thermal stability of liquid precursors and to devise a method for measuring vapor pressure that is suitably accurate yet more convenient than existing methods.

Customer Needs

Precursors for chemical vapor deposition are frequently liquid compounds that, until recently, were either rare or nonexistent. Their vapors are delivered to the process chamber either by direct injection (flash evaporation) or by bubbling a carrier gas through the liquid held in a "bubbler." Anecdotes from companies that either sell liquid precursors or sell the associated process equipment had suggested an industrial need for improved property data of these specialty chemicals. Designers and users of mass flow controllers, bubblers, and other gas and liquid delivery devices could use such data to optimize the performance of those devices.

Vapor pressure determines the concentration of the precursor-carrier mixture produced by a bubbler, and it sets a lower limit on the wall temperature of the delivery line and process chamber. Although high vapor pressures are preferred, the acceptable range is wide. For example, when heated to 100 °C, the vapor pressure of the widely used liquid TEOS (tetraethyl orthosilicate) is PV(100 °C) = 12 kPa. In contrast, a candidate precursor might be considered even if its vapor pressure were 100 times lower, say PV(100 °C) = 0.1 kPa.

Other important properties include liquid viscosity and thermal stability. Viscosity can affect the performance of injection systems. Thermal stability is important because the precursor's decomposition rate may limit the process's upper operating temperature and thereby the vapor pressure.

This work is guided in part by the output of a workshop organized by NIST at Semicon West 2006 with the goal of soliciting directions for research on the physical properties of gases and liquid precursors. A report of the workshop is available at *http://www.cstl.nist.gov/div836/836.06/*. Although some precursors, such as TEOS, have been used for many years and have well known properties, others are poorly characterized because they were only recently created or identified. As an example of the resulting diversity, precursors used recently by researchers to make hafnium oxide have included hafnium nitrate, hafnium chloride, tetrakis-dimethylamino hafnium, and tetrakis-diethylamino hafnium. The diversity inherent in research and the proprietary concerns of precursor manufacturers are considerations in selecting a precursor to characterize. Several workshop participants suggested that NIST first measure the example precursors named by the SEMI task force on precursor specifications (Liquid Chemicals committee / Europe). The workshop report lists some of those examples, and a broader range of precursor examples is listed in the supplementary table of precursors attached to the ITRS. The workshop participants pointed out that, in addition to vapor pressure, other important properties include thermal stability, liquid viscosity, and materials compatibility.

Technical Strategy

NIST will identify and assess the quality of existing vapor pressure data of compounds such as Hf $[(CH_3)_2N]_4$ (acronym TDMAH). NIST will also fill gaps in the existing data by developing apparatus capable of accurate vapor pressure measurements. The resulting accurate databases will be provided to industry. NIST also will investigate alternate methods to measure vapor pressure.

DELIVERABLES:

- Test scheme for handling hazardous metal-organic samples. 1Q 2009

Tested components of the scheme will include a safety interlock for the oven power, a zeolite trap, a burner tube to decompose effluent from the trap, and glove box procedures for loading and unloading samples.

DELIVERABLES:

- Identify existing vapor pressure data. 2Q 2009

Existing data can be found in journal publications, the NIST Chemistry WebBook, NIST standard reference database 87, and other databases. The applicability of estimation techniques, such as group contribution methods, will be examined.

DELIVERABLES:

- Integrate gas chromatograph / mass spectrometer for measuring the purity and decomposition rate of metal-organic vapors. 3Q 2009

Some metal-organic precursors are known to decompose at temperatures below 200 °C. The new system will use a gas chromatograph / mass spectrometer to identify the decomposition products as well as contaminants present in the original sample. The capillary sampling system, which will be suitable for metal-organic vapors at 200 °C, will include a modified commercial switching valve, and a heated capillary transfer line. The integration includes modifying the plumbing of the gas chromatograph so that a sample of vapor can be captured in the oven and sent through the heated line to the GC inlet. It also includes coordinating operation of the vapor pressure measurements with that of the GC/MS.

DELIVERABLES:

- : Investigate alternate methods to measure vapor pressure. 4Q 2009

The initial investigation will include an estimate of the method's uncertainty and the identification of sources of systematic error. The leading candidate is speed-of-sound measurements of a mixture comprising the equilibrium vapor plus one atmosphere of an inert gas.

Accomplishments

■ The vapor pressure apparatus, which consists of an oven, a vacuum system, a novel thermoelectric temperature control scheme, capacitance diaphragm pressure gauges, and other appropriate instrumentation, operates reliably for runs lasting multiple days. Such runs are needed due to the long time required for the in situ pressure gauges to recover from temperature changes. A technical committee reviewed the proposed handling of metal-organic samples for safety. Their recommendation for an oven power interlock that is tied to oven temperature and exhaust suction pressure has been implemented. Temperature stability within the requirement of 20 mK was demonstrated up to 200 °C, and measurements of the vapor pressure of water showed agreement with accepted values up to the gauge limit of 100 kPa (at 100 °C). Measurements with dodecane, a model low-pressure compound, demonstrated the ability to measure vapor pressures less than 10 Pa, but deviations from literature values were as large as 5 %. The deviations were traced to outgassing from valve tips made of polyimide, and the valves will be replaced.

■ Gas flow measurement research at NIST in support of the semiconductor industry created a quartz capillary flow meter with a hydrodynamic model of unprecedented accuracy. A recent spin-off is a capillary flow meter that provides a 0.1 sccm reference gas flow for calibrating spinning rotor vacuum gauges.

Publications

R. F. Berg, *"Capillary flow meter for calibrating spinning rotor gauges,"* Journal of Vacuum Science and Technology A 26, 1161- 1165 (2008).

Analysis Tools and Techniques Program

The continuing shrinking of device dimensions and the rapid inclusion of new materials into device fabrication demands the development of new analytical tools and techniques. The need for new analytical techniques and tools has increased as the components in the transistors approach the low nanometer level and the number of transistors per chip exceeds 1 billion. The development of tools capable of characterizing the structures produced in the laboratories as well as those needed to confirm the manufacturing process require significant improvements. Those used for production also require significant speeds not to slow down the commercial manufacturing. This latter condition may require some sacrifices in the resolution and accuracy of those tools. In addition, more significant modeling that allows us to bridge those areas where measurements can be done to those where knowledge is needed, but measurements cannot be done is critical. Significant improvements in tools capable of analyzing properties of defect particles in the sub-30 nm size are urgently needed. Global and local stress measurement techniques need to be developed.

Thin-Film X-Ray Metrology for Microelectronics

Technical Contacts:
J. P. Cline
D. Windover

Goals

This multi-year collaborative effort between SEMATECH, ISMI, and NIST will provide the semiconductor community with the measurement methodology and calibration capability for accurate thin film characterization using X-ray reflectometry (XRR) and high-resolution X-ray diffraction (HRXRD).

Customer Needs

In recent years, the semiconductor industry has driven scientific advancement in nanometer-scale material coatings to achieve unprecedented uniformity in thickness, control of composition, and unique electrical and mechanical properties. Nanotechnology is the fastest growth area of industry in the United States today. Simultaneous to this rapid advance in thin film processing technologies, the X-ray diffraction user community and instrument manufacturers have collaboratively developed techniques such as XRR and HRXRD that quantitatively measure thin film characteristics such as thickness, density profile, composition, roughness, and strain fields. This NIST-SEMATECH-ISMI effort addresses the industry call for accuracy in thin film characterization (in particular for thickness, density, and roughness determination) and epitaxial layer characterization (in particular for thickness, composition, and lattice strain).

Technical Strategy

NIST addresses the need for XRR and HRXRD standardization and metrology through the production of Standard Reference Materials (SRMs) to aid end users in instrument calibration (see Figure 1). However, production of SRMs requires a substantial instrumentation infrastructure, years of researcher time, and a collaborative community invested in the realization of the SRM to completion. The technical approach to SRM production can be broken into three parallel goals: 1) manufacture of a stable, robust, and well characterized calibration artifact, 2) construction of a stable, well characterized measurement apparatus for performing certification measurements, and 3) development of first principles data analysis procedures with well-founded a priori structural models and statistically verifiable parameter (and model) uncertainty estimates (see Figure 2). To meet goal 1, NIST has established close working relationships with SEMATECH, ISMI, and other industrial and academic partners for developing and manufacturing superlative calibration artifacts for use as SRM feedstock. To meet goal 2, NIST has constructed an X-ray Metrology facility for X-ray measurements traceable to the International System of Units (SI) containing an HRXRD and XRR instrument known as the Ceramics Division Parallel Beam Diffractometer (CDPBD), located in the Advanced Measurement Laboratory (AML) at NIST. To meet goal 3, NIST has collaborated with X-ray industry leaders in developing statistically-sound first principles XRR analysis. These same approaches will be applied to HRXRD analysis in the future (FY09+).

NIST XRR and HRXRD Instrumentation: the CDPBD

Over the past decade, NIST has applied considerable resources to developing the CDPBD for SI-traceable measurements of Powder XRD, Epitaxial HRXRD, and thin-film XRR artifacts for the Standard Reference Materials (SRM) program (see Figure 3). In parallel to this MSEL effort, the Physics Laboratory developed the Physics Laboratory X-Ray Reflectometer (PLXRR), an instrument dedicated to XRR characterization of semiconductor thin-film artifacts (see Figure 4). The PLXRR has been moved to our X-Ray

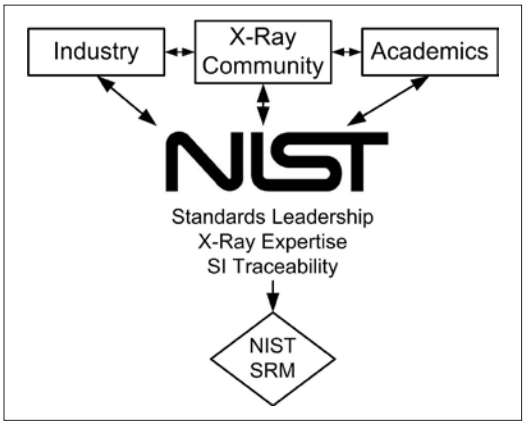

Figure1. Diagram of interactions between NIST and the X-ray community in the production of Standard Reference Materials (SRMs). NIST has many two-way collaborative interactions preliminary to the release of the final product.

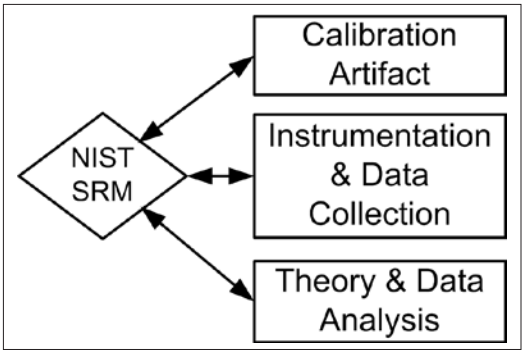

Figure 2. Essential elements of NIST's technical approach to SRM development.

Metrology facility within AML and this instrument will be integrated into the XRR SRM effort. This will enable cross-instrument measurement comparisons as part of our certification process.

Figure 3. Ceramics Division Parallel Beam Diffractometer (CDPBD) located in the Advanced Measurement Laboratory at NIST seen during alignment of the new spherical air bearing under the goniometers (bottom of green goniometer stack). The X-ray source (near red light in center) is collimated through a monochromator (center, hanging from superstructure) and is diffracted/reflected by a section of a wafer (right) into an analyzer crystal and detector (right). Sample and Detector rotation axes must be coplanar with the incident and diffracted/refracted X-rays. This requires external optical alignment methods using autocollimation, e.g., by a Leika digital theodolite (front,left).

SI traceability in lattice parameter (HRXRD), d-spacing, or film thickness (XRR), d, requires simultaneously traceability in X-ray wavelength, λ, and in diffraction angle, θ, following Bragg's law: $2d = n\lambda / \sin(\theta)$. The present NIST instrument development project involves establishing SI traceability for both diffraction angle and wavelength on the CDPBD and PLXRR. SI traceability for diffraction angle is achieved using optical encoders on the two rotation stages used to move the sample and detector. The optical encoders' errors are then "mapped" using an external angle reference to generate corrections and uncertainties for each axis. The encoded stages are presently accurate to $\pm$ 2.0 µrads ($\pm$ 0.4 arc seconds). Calibration experiments and collaboration with encoder manufacturers are currently under way to achieve an approximate order of magnitude improvement in accuracy. The first results from this work will soon be used for X-ray measurements (FY09). SI traceability in wavelength is achieved by constructing a stable, well modeled optics assembly to convert angular and energy divergent radiation from an X-ray source into parallel, monochromatic radiation for use in diffraction or reflection. The CDPBD uses a monochromator with Si (220), 2/4-bounce channel-cut crystals to filter the rotating anode Cu source into a source of highly parallel, single energy X-rays. SI traceability in X-ray wavelength from the CDPBD is performed using an SI-traceable reference crystal (whose d-spacing has been measured with relative standard uncertainty of 3×10^{-8}). The X-ray wavelength for our

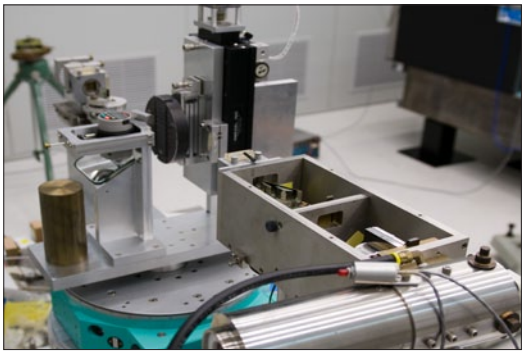

Figure 4. Physics Laboratory X-Ray Reflectometer (PLXRR) seen during relocation to the the Advanced Measurement Laboratory X-Ray Metrology facility. The X-ray source (front, right) is collimated through a mirror and monochromator assembly (front, center rectangular structure) and is reflected by a section of a wafer (vacuum chuck shown rear, center) into a detector (far rear, left).

instrumentation currently has a relative standard uncertainty of ≈ 1 in 10^{-5} (FY06). Wavelength and angle SI-traceability methods developed for the CDPBD will be implemented on the PLXRR in the future (FY09+). For the certification of the HRXRD SRM we developed a "sequential delta-d method" for reducing the uncertainty of d-spacing of HRXRD measurements due to instrument alignment effects through the use of a WASO 04 reference crystal from the Avogadro Project (See Figure 5). This has allowed for d-spacing measurements with femtometer-scale expanded uncertainties on the CDPBD. Further improvements in angle and wavelength metrology should improve the limits of the NIST instrumentation for HRXRD and XRR measurements (FY09). A spherical air bearing base has been incorporated into the CDPBD below the goniometer assembly to allow translation and goniometer tilt to be orthogonal for alignment of XRR and HRXRD measurements. NIST's studies of instrumental alignment parameters and their effect on structural model uncertainty will be used to establish guidelines for instrument response modeling on commercial instrumentation using future HRXRD and XRR SRMs.

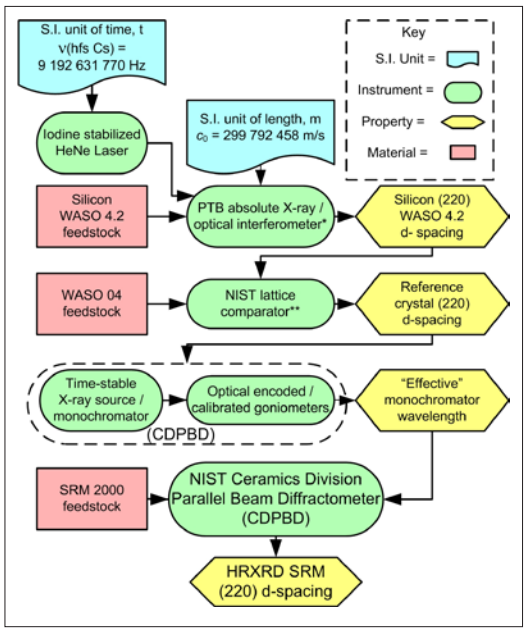

Figure 5. NIST International System of Units (SI)-traceability pathway for high-resolution X-ray diffraction (HRXRD) SRMs using the CDPBD. Measurements from X-ray/optical interferometry at Physikalisch-Technische Bundesanstalt (PTB) in Germany and lattice comparison measurements at NIST provide femtometer-scale expanded uncertainty in lattice spacing (d-spacing) measurements for the SRM.

The HRXRD SRM effort was started nearly a decade ago with collaborations between the NIST Materials Science and Engineering Laboratory (MSEL), the NIST Physics Laboratory, Bede Metrology, and Applied Materials. The approach was to use a commercially viable SiGe epitaxial process as a feedstock structure for a HRXRD SRM. The structure was deposited on 200mm wafers, which were then sectioned into 25mm x 25 mm specimens after performing HRXRD SRM certification measurements. Structures were produced in FY01 and NIST instrumentation capable of SI-traceable determination of Si substrate d-spacing became available in FY07. The mature, temporally stabilized SiGe feedstock was then measured using transmission and reflection geometries to provide information on both the Si substrate d-spacing and the SiGe epitaxial surface structure.

Due to the extended duration of this SRM project, completion of the certification was divided into two phases to provide a timely product rollout. The goal of the first phase of this SRM was to provide an SI-traceable d-spacing with low expanded uncertainty to aid in basic instrument calibration. If one assumes that the wavelength is relatively stable (possible with, e.g., an epoxy-mounted channel cut monochromator), then SRM 2000 will provide correction for the diffractometer angle. The first phase of the certification was the HRXRD tech transfer in FY08. The second, yet to be completed, certification phase will provide information on the SiGe epitaxial layer for calibration of instrument response (how well the X-ray source is behaving) and short range angle determination (how well the goniometer is behaving) near the (004) Si substrate peak. This calibration information would be most useful in quantitative strain determination using HRXRD. The difficulty here involves determination of the correct structural model for the deposited epilayer. We are currently working with instrument vendors, with external collaborators, and with NIST Synchrotron Methods staff to address this modeling issue (FY09+).

XRR SRM DEVELOPMENT

The XRR effort involves two parallel characterization projects being performed on normally identical, temporally stable, multilayer artifacts supplied by ISMI, SEMATECH, or other semiconductor partners. The NIST project consists of in-house XRR (and HRXRD, where possible)

characterization with International System of Units (SI)-traceable measurement instrumentation and SI-traceable, first principles data modeling including Bayesian analysis providing refinement of instrumental and model parameters as well as structural model selection. In parallel to this NIST measurement project, ISMI, SEMATECH, and semiconductor partners will measure or have measurements performed using commercial process-line and laboratory XRR instrumentation and NIST will analyze these data with commercial software to study the limitations of commercial instrumentation and software modeling. Combining results from both studies will ultimately allow accuracy/traceability and error estimation for commercial instrumentation. This work will also address theoretical XRR modeling limitations and compare software model refinement and model selection approaches. The multi-year collaboration will provide the community with total error budget estimates for a given XRR structural analysis approach and instrumentation. This collaborative work has been underway with SEMATECH (FY05, 06, and 07) and has continued with ISMI and other partners (FY08+). The progress in FY05 included a comprehensive, first principles development of the XRR theory necessary for traceable modeling of data and a first round of measurements on artifacts by commercial and NIST instrumentation. FY06 work explored the application of an approximate Bayesian model selection method to compare the relative probability of different structural models for measured XRR data. Preliminary results with simulated XRR data have shown success in determining the initial structural model used to generate the simulated data. FY07 deliverables included the development of a first XRR prototype SRM for selection of a future SRM feedstock. FY08 deliverables involve development of a second XRR prototype and further development of the NIST XRR modeling approach for establishing parameter uncertainties for samples with surface contamination. Upon development of a successful XRR prototype, we will lead a round-robin with interested industry partners (FY09).

NIST XRR Study – The standard NIST approach for reducing uncertainty in a measurement technique involves the generation of a Standard Reference Material (SRM) (see Figure 1). Figure 2 shows the three parallel research aspects needed for the development of an XRR SRM: (1) the manufacture of a robust thin film calibration artifact with a high degree of temporal stability and contamination and/or oxidation resistance, (2) the development of SI-traceable measurement instrumentation, and (3) the creation of an SI-traceable, first principles data analysis approach.

Our collaborative effort with ISMI / SEMATECH allows us to examine structures relevant to the semiconductor industry as candidates for an XRR calibration artifact. NIST has also engaged other national metrology institutes (NMIs) in an effort to assess the temporal stability of international NMI pre-standards. Both PTB of Germany and NMIJ/AIST of Japan have provided us with structures for comparative XRR analysis. This cooperative study will help gauge which thin films structures provide stable, well-defined, refinement parameters suitable for SI-traceable modeling.

NIST is currently developing first principles, SI-traceable XRR software to analyze data and refine model and instrument response parameters. XRR analysis is an inverse problem in which we select input parameters for a guessed structural model. This model is then used to simulate data that is compared with measured data to compute the goodness of fit. This process is repeated until a best fit is reached; the best fit model parameters then become the refined model parameters used to describe the structure. Three major questions limit the effectiveness of this current XRR modeling approach: (1) How do we accurately simulate data using a structural model? (2) How do we know which structural model describes the measured structure? (3) How do we accurately compare simulated and measured data? The NIST software development effort attempts to answer each of these questions.

To address the model data simulation issue, we have developed XRR modeling based on the elementary Parratt formalism of discrete layer structures and assuming perturbation-based roughness while using the minimum number of layers necessary to describe a structure. This approach will in the future combine XRD, HRXRD and XRR in the same fundamental modeling theory and allow for SI traceability in refined parameters (FY09+). To address the question of model accuracy, we are implementing a Bayesian analysis approach to determine the probability that a given structural model correctly describes a given data set. This model selection component is essential to determining the validity of initial structural as-

sumptions in any XRR analysis. Addressing the third question is of considerable interest. Commercial refinement approaches attempt to optimize a solution through a "chi squared" or other minimization criterion by using e.g., genetic algorithms. This approach attains fast solution times most compatible with process-line requirements, at the loss of statistical data required for parameter uncertainty calculations. NIST, in collaboration with several companies, is developing a statistical sampling based method using a Markov Chain Monte Carlo (MCMC) formalism to generate SI-traceable uncertainty estimations. The MCMC approach is necessary for developing formal Bayesian model selection methods (FY09+) to complement the existing Approximate Bayesian approach.

NIST/SEMATECH XRR Study – The NIST/SEMATECH project consists of measurements and analysis from commercial instrumentation to allow comparison and calibration transfer from NIST SI traceable measurements and analysis.

The NIST/SEMATECH project combines measurements with commercial process-line and laboratory XRR instrumentation with complimentary compositional analysis results as feedback for comparison with NIST measurements performed in parallel on the same artifacts. The measurement and modeling work at NIST will provide SI-traceable XRR measurements and parameter analysis for artifacts and potential candidate SRMs. The collaboration with SEMATECH allows calibration transfer between NIST SI-traceable measurements and process-line instrumentation. NIST will then use results from NIST SI-traceable measurements, SEMATECH commercial measurements and modeling, and NIST SI-traceable XRR modeling, to quantify error bounds and overall error budgets on the accuracy and precision possible from commercial instrumentation and commercial modeling software.

Calibration and accuracy determination of commercial instrumentation are the primary goals of this collaboration. To achieve these goals, we need to develop accurate instrument response functions for the commercial instrumentation being calibrated. The instrument response function for commercial instrumentation may be the dominant term in the overall accuracy budget for XRR measurements. To address instrumentation effects on accuracy, work must be performed with different commercial XRR system geometries to discover the mechanical alignment parameters that dominate the error budgets of each system. This will require cooperation from instrument vendors to provide the necessary information or direct measurements of detailed instrument response functions. The incorporation of instrument response parameters into NIST modeling will allow for comparison between traceable measurements at NIST and measurements on commercial instrumentation in the field. The NIST instrument response function information will be developed through our instrument traceability study discussed earlier. We can then combine specific instrument corrections in the accuracy error budget and use a calibration artifact such as a temporally stable thin film structure measured on the commercial instruments and at NIST to provide instrument calibration and stability monitoring (FY09+ deliverable).

HRXRD and XRR Project Deliverables – The final project results available to SEMATECH will include HRXRD and XRR uncertainty estimates based on NIST HRXRD and XRR software and the calibration artifacts necessary for optimizing the performance of commercial process-line and laboratory XRR instruments. Theoretical uncertainty estimates provided by NIST software and simulated structural data will determine the limitations of XRR applicability for arbitrary multilayer systems on commercial XRR instrumentation (FY09+). Calibration artifacts measured on NIST SI-traceable instrumentation will allow routine system monitoring, alignment, calibration, and instrument response function comparisons to ensure commercial instrument precision and stability. These deliverables will dramatically improve the precision and accuracy of conventional HXRXRD and XRR characterization of multilayer structures which exhibit well-established composition and uniformity (FY09+ deliverables).

DELIVERABLES:

- NIST analysis of NIST XRR pre-standard measurements. 4Q 2008
- NIST analysis of XRR parameter uncertainty for contaminated samples. 2Q 2009
- NIST release of HRXRD SRM for sale. 3Q 2009 • NIST / ISMI / SEMATECH development of second XRR pre-standard structure. 4Q 2009

Accomplishments

■ In FY05, the CDPBD moved to equipment space in AML at NIST which provides instrument temperature stability of ± 0.02 °C. Preliminary

Quantity	Certified Value	Expanded Uncertainty $U(i)$ for $k = 2$	Description
d_{SRM}	0.192 016 1 nm (at 22.5 °C)	0.000 008 7 nm	Si (220) transmission case d-spacing of SRM 2000
ξ_{SRM} ξ	4.360 mrad	0.027 mrad	Magnitude of wafer miscut (polar form)
ϕ_{SRM}	-359.5 mrad	16 mrad	Direction of wafer miscut (polar form)
x_{SRM}	-1.534 mrad	72 µrad	Tilt of wafer miscut in x-plane (Cartesian form)
y_{SRM}	4.0810 mrad	19 µrad	Tilt of wafer miscut in y-plane (Cartesian form)
$\theta_{surf\ aceSRM(004)}$	0.604 785 rad	0.000 076 rad	Angle from wafer surface to Si (004) reflection peak

Table 1. Certified reference values for SRM 2000 Si Substrate d-spacing (220).

calibration of the angle measurement has been assessed for uncertainty determination (accuracy determination has been completed) and improvements using a new compensation approach will be implemented (FY08). First principles XRR theory development with emphasis on justifying approximations present in commercial XRR software was completed (FY06) and a dynamical scattering based model has been implemented with Monte Carlo Markov Chain (MCMC) methods for structural parameter refinement and formal parameter uncertainty analysis (FY07). A pre-standard XRR test structure has been fabricated by ISMI for NIST SI-traceable measurement (FY08) with a second structure in development (FY09) and with SRM development scheduled for the future (FY09+).

■ FY07 Technical transfer: NIST HRXRD pre-standard wafer and measurements to SEMATECH and X-ray industry partners – In FY07, we measured our HRXRD feedstock wafers and provided a wafer and sectioned specimens to SEMATECH along with NIST HRXRD data for collaborative studies. We also provided sectioned specimens to all the major X-ray instrument vendors for internal calibration studies and for independent, complementary measurements on the feedstock. The collaboration between NIST and SEMATECH in Thin-film X-ray Metrology on previous XRR projects has facilitated this sharing of pre-standards with the semiconductor community and with semiconductor tool manufactures at the early stages of SRM production to better achieve the results that the community needs as fast as possible.

■ FY08/9 Technical transfer: NIST HRXRD SRM certification to industry – In FY07, we completed the first phase of certification analysis for our HRXRD SRM (see Table 1). The SRM and the certification reports have been provided to the SRM Program for packaging and release of SRM 2000 for sale to end users and tool manufacturers. This SRM development has involved collaboration with the semiconductor industry (Applied Materials and SEMATECH) and with X-ray tool manufacturers (Jordan Valley / Bede, Bruker, Panalytical, Rigaku, and others) providing NIST with valuable feedback on our approach during the multiyear certification process. The SI-traceable nature of SRM 2000 has allowed us to provide the semiconductor and nanotechnology industries with a nanometer-scale length standard (d-spacing) with femtometer-scale expanded uncertainty, thereby serving as the most accurate, commercially available, nano-scale "meter stick" available today.

■ FY09 Technical transfer: NIST parameter uncertainty XRR analysis for surface contamination – In FY07/08 we tested NIST XRR MCMC analysis for simulated and measured data from ISMI / SEMATECH on a SiO_2 / TiN / Si wafer pre-standard structure. In FY09 we addressed the impact of data quality on the refinement of parameter uncertainties for simulated XRR data from a TiN (20 nm) / Si sample. We also tested the effects of a surface carbon contamination layer (0.4 nm) on model parameter uncertainties. The results of the study will be published in conference proceeding for the 2009 Frontiers of Characterization and Metrology for Nanoelectronics, held in Albany, NY. The MCMC analysis provides clear evidence of when parameters are uncorrelated (carbon layer roughness and TiN thickness in Figure 6), are highly correlated (Carbon contamination thickness and TiN thickness in Figure 7), and when a given parameter cannot be refined (Si density in Figure 8).

COLLABORATIONS

SEMATECH – PY Hung.

ISMI – Victor Vartanian.

PTB, Precision Metrology – Peter Thomsen-Schmidt.

LETI – Emmanuel Nolot.

NMIJ/AIST – Toshiyuki Fujimoto.

Jordan Valley Semiconductor / Bede Scientific Inc. – Matthew Wormington.

Bruker AXS – Assunta Vigliante & Arnt Kern.

Coruscavi – David L Gil.

Panalytical – Martijn Fransen.

Rigaku MSC – Joe Formica.

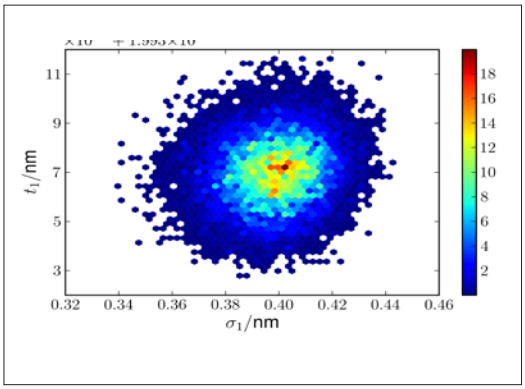

Figure 6. 2-dimensional histogram of probability distribution functions for TiN thickness and surface roughness in an XRR model showing no parameter correlation.

Publications

D.L. Gil, D. Windover, A. Henins, J.P. Cline, *"Designing an X-ray Reflectometry Standard Reference Material: Effects of Surface Contamination and Data Quality"* – poster presentation at 2009 Frontiers of Characterization and Metrology for Nanoelectronics, Albany, NY (May, 2009).

D. Windover, D.L. Gil, D. Black, A. Henins, J.P. Cline, *"NIST High Resolution X-ray Diffraction Standard Reference Material: SRM 2000"* – poster presentation at 2009 Frontiers of Characterization and Metrology for Nanoelectronics, Albany, NY (May, 2009).

D.L. Gil, D. Windover, J.P. Cline, A. Henins, *"Characterizing x-ray mirrors in reciprocal space: Preliminary results from the NIST X-ray Optics Evaluation Double-Crystal Diffractometer"* – oral presentation at SMEXOS: Simulation Methods for X-ray Optical Systems, Grenoble, France (February 2009).

J. P. Cline, D. Windover, A. Henins, *"NIST Standard Reference Materials for X-Ray Metrology"* – poster presentation at Denver X-Ray Conference, Denver, CO (August, 2008).

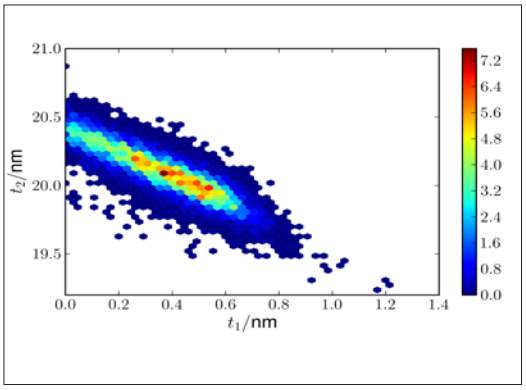

Figure 7. 2-dimensional histogram of probability distribution functions for surface carbon contamination layer and TiN thickness in an XRR refinement showing a high degree of parameter correlation.

D. Windover, D.L. Gil, D. Black, J.P. Cline, A. Henins, *"NIST High Resolution X-ray Diffraction Standard Reference Material: SRM 2000"* – poster presentation at Denver X-Ray Conference, Denver, CO (August, 2008).

D.L. Gil, D. Windover, A. Henins, J.P. Cline, *"Characterizing X-ray mirrors in reciprocal space: Preliminary results from the NIST X-ray optics evaluation double-crystal diffractometer"* – poster presentation at Denver X-Ray Conference, Denver, CO (August, 2008).

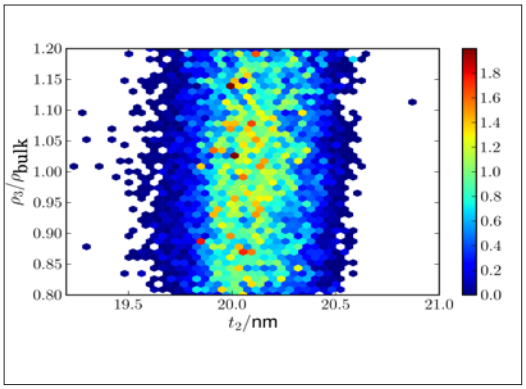

Figure 8. 2-dimensional histogram of probability distribution functions for TiN thickness and Si substrate density in an XRR model showing poor parameter refinement (no peak) for Si substrate density.

D. Windover, D. L. Gil, A. Henins, D. Black, J. P. Cline, P. Xu, M. Wormington, M. Vaudin, Y. Gerbig, R.Cook, E. Kessler, P. Evans, S.J. Stranick, J. Schoenmaker, L. Novotny, *"Standard Reference Materials for thin film metrology"* – invited presentation at ISMI – FMAG meeting, Monterey, CA (February 2008).

J. P. Cline, D. Windover, A. Henins, *"Standard Reference Materials for thin film metrology"* – poster presentation at Denver X-Ray Conference, Denver, CO (August, 2007).

D. L. Gil, D. Windover, J. P. Cline, A. Henins, P. Y. Hung, S. C. Song, R. Jammy, A. Diebold, *"MCMC methods for X-ray reflectometry standards"* – poster presentation at Denver X-Ray Conference, Denver, CO (August, 2007).

D. A. McGillivray, S.C. Yang, D. Windover, D. L. Gil, J. P. Cline, A. Henins, *"Status of the NIST HRXRD SRM: Instrumentation alignment approach"* – poster presentation at Denver X-Ray Conference, Denver, CO (August, 2007).

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D. L. Gil, D. Windover, J. P. Cline, A. Henins, N. Armstrong, P. Y. Hung, S. C. Song, R. Jammy, A. Diebold, *"MCMC method for determining structural information using X-ray reflectometry"* – poster presentation at 2007 Frontiers of Characterization and Metrology for Nanoelectronics, Gaithersburg, MD (March 2007).

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P. Xu, D. Windover, N. Armstrong, M. Wormington, A. Henins, J. P. Cline, *"Progress on the NIST High Resolution X-Ray Diffraction Standards"* – poster presentation at Denver X-Ray Conference, Denver, CO, (August, 2006).

D. Windover, N. Armstrong, A. Henins, J. P. Cline, *"NIST X-Ray Reflectometry Metrological Analysis Approach"* – poster presentation at Denver X-Ray Conference, Denver, CO, (August, 2006).

High-Resolution Microcalorimeter X-Ray Spectrometer for Chemical Analysis

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Goals

We will develop new generations of X-ray spectroscopy tools to meet the materials analysis needs of the semiconductor manufacturing industry. Energy-Dispersive Spectrometers (EDS) based on microcalorimeters have the ability to detect photons with high energy resolution and near-unity quantum efficiency. Using these tools, a wide range of materials analysis problems can be solved. In semiconductor manufacturing, improved X-ray materials analysis is needed to identify nanoscale contaminant particles on wafers and to analyze very thin layers of materials and minor constituents. Microcalorimeter EDS improves the spectral resolution by one to two orders of magnitude compared to the semiconductor Si-EDS, the existing industry standard. Such improved resolution combined with energy dispersive operation makes possible direct spectral separation of most overlapping peaks often encountered with Si-EDS in complex multi-element systems. The improved resolution of the microcalorimeter EDS also increases the peak-to-background ratio. Peak shape and shift can be studied to reveal chemical state information.

Developing arrays of X-ray microcalorimeters will enable the acquisition of high statistics spectra in reduced time, improving the efficiency and statistical quality of existing materials analysis applications. Further, large-format arrays (up to 1000 pixels) will make it possible to chemically analyze smaller features and trace constituents, and to track rapidly evolving X-ray spectra for in-process and process-stream monitoring.

The microcalorimeter EDS detector invented at NIST consists of a superconducting thermometer (a superconducting transition-edge sensor (TES) and an X-ray absorber fabricated on a micromachined Si_3N_4 membrane, and cooled to cryogenic temperatures (0.1 K). When X-rays are absorbed in the detector, the resulting heat pulse in the microcalorimeter is measured by the TES thermometer. The change in the temperature of the thermometer is measured by a superconducting quantum interference device (SQUID) amplifier. The temperature pulse height gives a measurement of the energy of the X-ray photon one to two orders of magnitude more sensitive than Si-EDS. The detector is cooled to 0.1 K by a compact adiabatic demagnetization refrigerator. We are presently simplifying this refrigerator to reduce system costs and increase the accessibility of microcalorimeter technology.

Customer Needs

Improved X-ray detector technology has been cited by SEMATECH's Analytical Laboratory Managers Working Group (ALMWG, now Analytical Laboratory Managers Council (ALMC) as one of the most important metrology needs for the semiconductor industry. In the 2007 International Technology Roadmap for Semiconductors, microcalorimeter technology is called out for its ability to measure chemical shifts, and because of its potential for particle and defect analysis. The transition-edge sensor (TES) microcalorimeter X-ray detector developed at NIST has been identified as a primary means of realizing these detector advances, which will greatly improve in-line and off-line metrology tools that currently use semiconductor energy-dispersive spectrometers (EDS). At present, these metrology tools fail to provide fast and unambiguous analysis for particles less than approximately 0.1 μm to 0.3 μm in diameter. Improved EDS detectors such as the TES microcalorimeter are necessary to extend the capabilities of existing SEM-based instruments to meet the analytical requirements for future technology generations. With continued development, microcalorimeter EDS should be able to meet both the near-term and the longer-term requirements of the semiconductor industry for improved particle analysis.

"Prototype microcalorimeter energy dispersive spectrometers (EDS) and superconducting tunnel junction techniques have X-ray energy resolution capable of separating peaks that overlap and cannot be resolved with current generation lithium drifted- silicon EDS detectors. Such new X-ray detectors will allow resolution of slight chemical shifts in X-ray peaks providing chemical information such as local bonding environments. These advances over traditional EDS and some wavelength dispersive spectrometers can enable particle and defect analysis on SEMs located in the clean room." **2007 International Technology Roadmap for Semiconductors**

Technical Strategy

1. The usefulness of single-pixel X-ray microcalorimeter EDS in materials analysis has now been well established in a variety of demonstrations. Arrays of X-ray microcalorimeters for increased collection area and count rate have been demonstrated and their energy resolution is comparable to single sensors. To meet the needs of the semiconductor industry, it is necessary to make both single-pixel and array microcalorimeter systems more widely available. In addition to microcalorimeters, the system requires novel superconducting electronics to instrument the detectors, compact adiabatic demagnetization refrigerators to simplify cooling to milliKelvin operating temperatures, and custom room-temperature electronics and software to process the output signals. Our goal is to develop new generations of detector systems, to transfer them to the Chemical Science and Technology Laboratory (CSTL) in NIST Gaithersburg, Maryland for collaborative use in studying problems of interest to the industry (Fig. 1), and to work with commercial partners in disseminating the technology.

DELIVERABLES:

- Provide continued support and upgrades for the single-pixel microcalorimeter system transferred to CSTL. Provide support for partners working to commercialize microcalorimeter technology and make it more widely available to the semiconductor industry.

2. The Adiabatic Demagnetization Refrigerator (ADR) that provides 0.1 K operating temperatures is a crucial part of a microcalorimeter system. Recently, it has become possible to precool the ADR with a push-button mechanical cryocooler whose only consumable is electricity. The combination of an ADR with a mechanical cooler eliminates the need for liquid cryogens, simplifies microcalorimeter operation, and is an important step to in-line process monitoring. Our goal is to continue to improve the design and increase the capabilities of refrigeration systems for microcalorimeter detectors.

Figure 1. Single-pixel NIST X-ray microcalorimeter system on a scanning-electron microscope. The system was developed in the Electronics and Electrical Engineering Laboratory (EEEL) at NIST, Boulder, and transferred to the Chemical Science and Technology Laboratory (CSTL) at NIST Gaithersburg to be used to study problems of interest to the semiconductor industry.

DELIVERABLES:

- Design an adiabatic demagnetization refrigerator cooled by a pulse tube mechanical cryocooler with the cooling capacity for 1,000 microcalorimeter sensors (July-Sept. 2009).

3. One of the barriers to widespread dissemination of X-ray microcalorimeter instruments is the complexity and cost of the adiabatic demagnetization refrigerator used to cool to 100 mK. The development of an on-chip solid-state microrefrigerator based on superconducting tunnel junctions to cool from 300 mK to 100 mK would greatly simplify the cryogenic system needed for microcalorimeter EDS. Adiabatic demagnetization refrigerators could be replaced by small, simple, and inexpensive 3He systems, which cool to 300 mK, coupled to the solid-state tunnel-junction refrigerator cooling to 100 mK.

DELIVERABLES:

- Demonstrate improved performance of tunnel-junction refrigerators and X-ray microcalorimeters cooled by tunnel-junction refrigerators. Demonstration of tunnel junction cooler with temperature reduction close to theoretical maximum (July-Sept. 2009).

4. The operation of microcalorimeter arrays requires multiplexed SQUID readout. A time-domain SQUID multiplexer has previously been demonstrated and been used to successfully read out multiple microcalorimeters under X-ray illumination using a much smaller number of amplifier channels. Significant increases in multiplexer bandwidth and pixel-handling capacity are possible based on evolutionary design improvements.

DELIVERABLES:

- Demonstrate improved SQUID multiplexer performance and multiplexed operation of increasing numbers of microcalorimeters under X-ray illumination. Fabrication and testing of low power

SQUID series arrays (Oct-Dec. 2008). Demonstration of 2x24 multiplexed calorimeter array with sub-ms detector response (July-Sept. 2009).

Accomplishments

■ We designed and built an adiabatic demagnetization refrigerator that is precooled by a mechanical cryocooler. This simple and compact system is operated by the push of a button and requires no liquid cryogens. This refrigerator has been successfully commercialized and numerous versions have now been sold worldwide by High Precision Devices, Inc.

We demonstrated undegraded operation of a high resolution microcalorimeter inside a mechanically-cooled demagnetization refrigerator. We also mounted a mechanically-cooled demagnetization refrigerator on a scanning electron micro-

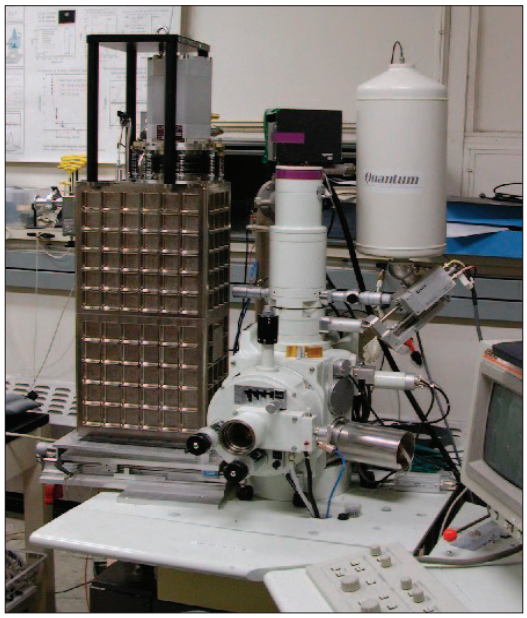

Figure 2. Cryogen-free adiabatic demagnetization refrigerator (left) undergoing vibration testing on a scanning electron microscope.

scope and demonstrated near perfect imaging at high magnification. A photograph of the pulse tube cooled demagnetization refrigerator undergoing vibration testing on an electron microscope is shown in Fig. 2.

■ We developed a new generation of microcalorimeters that incorporate additional normal metal regions to suppress internal noise. In addition to being more stable and easier to bias, the energy resolution of these microcalorimeters is significantly improved. We demonstrated an energy resolution of 2.4 eV FWHM at 5.9 keV. and 2.0 eV at 1.5 keV; these figures are over 30 times better than the best high resolution semiconductor-based detectors currently available.

We continue to support the microcalorimeter system installed on a CSTL scanning electron microscope in Gaithersburg, Maryland. We have also provided support to the company STAR Cryoelectronics who are working to commercialize microcalorimeter technology. Previously, we tested X-ray microcalorimeters fabricated by STAR Cryoelectronics and demonstrated an energy resolution better than 15 eV at 6 keV. More recently, we tested a complete microcalorimeter amplifier chain made by STAR Cryoelectronics and demonstrated excellent performance.

■ We demonstrated the ability to read out 16 total TES microcalorimeters in two columns with an average energy resolution of 2.86 eV FWHM (Fig. 3).

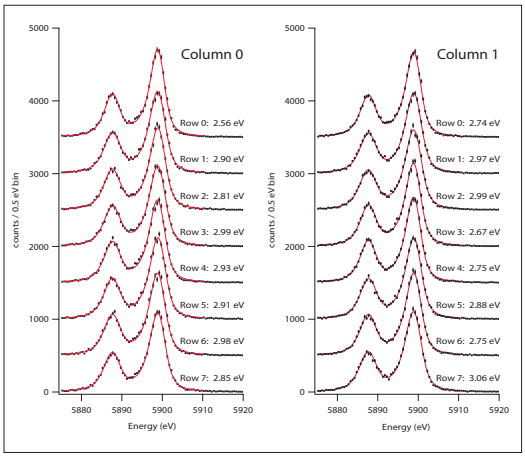

Figure 3. Spectra from 16 microcalorimeter array showing 2.86 ev resolution at 6 kev.

■ With evolutionary improvements to the basic architecture, our time-division SQUID multiplexer will be able to read out 32 detectors per channel with 4 eV resolution or better. We have built a test apparatus to house and read out up to 128 microcalorimeter pixels and are preparing to demonstrate multiplexed operation of 48 high-resolution microcalorimeters with sub-ms response times using only two read-out channels (Fig. 4)

■ We recently demonstrated SQUID array current amplifiers that dissipate significantly

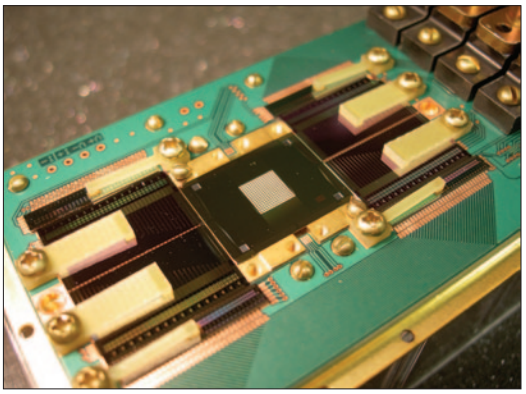

Figure 4. 128 pixel microcalorimeter array and multiplexed readout circuitry.

less power than previous generations. These new amplifiers can be positioned adjacent to the sensors at the coldest stage of the refrigerator so as to increase the system bandwidth and the number of multiplexed pixels (Fig. 5).

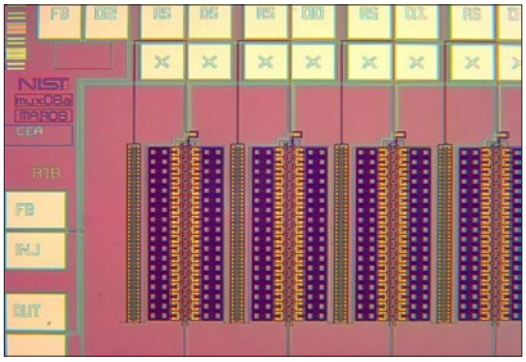

Figure 5. lower power squid current amplifier for higher bandwidth operation. The vertical scale is about 2 mm.

■ We have successfully developed an on-chip solid-state refrigerator to cool X-ray microcalorimeters from 300 mK to 100 mK. This refrigerator can greatly simplify the cryogenic system needed for microcalorimeter EDS. Adiabatic demagnetization refrigerators can be replaced by small and inexpensive 3He systems coupled to the solid-state refrigerator. Cooling is produced in the devices by the tunneling of electrons through normal-insulator-superconductor junctions. The solid-state refrigerator is fabricated on a silicon wafer using conventional thin-film and photolithographic techniques, has no moving parts, and operates continuously. Recently, we demonstrated solid-state refrigerators able to cool X-ray microcalorimeters over useful temperature ranges, for example, from 260 mK to 160 mK (Fig. 6)

■ We operated the X-ray microcalorimeter and demonstrated an energy resolution of 9.5 eV at 5.9 keV, a record for the 260 mK starting temperature of the integrated device. This work has been featured twice on the cover of *Applied Physics Letters* and once on the cover of *Physics Today*

■ We created a chemical shift map showing the chemical bonding state of Al in a sample containing both Al and Al_2O_3 (see Fig. 7). An aluminum film was deposited on part of a sapphire substrate. A microcalorimeter EDS was used to measure the X-ray spectrum as the electron beam was rastered to form the SEM image. The Al X-ray line position was shifted by a small amount (about 0.2 eV) in

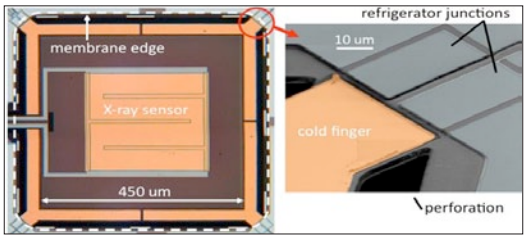

Figure 6.Micrograph showing tunnel junction cooled x-ray microcalorimeter

the regions containing Al_2O_3 as compared to the regions containing elemental Al. The high energy resolution of the microcalorimeter allowed the shift to be measured, resulting in the false-color image below. The map clearly demonstrates that microcalorimeter EDS can be used to discriminate the chemical bonding state using shifts in the positions of X-ray lines. The result also highlights the need for large-format arrays to increase the data collection rate. The image shown here was acquired over several hours. Images such as this could be acquired much more quickly using an array of microcalorimeters.

COLLABORATIONS

Chemical Science and Technology Laboratory, NIST, Gaithersburg, Terry Jach, Lance King, Dale Newbury, John Small, and Eric Steel, the development of microcalorimeter EDS systems.

PUBLICATIONS

H. Tan, D. Breus, W. Hennig, K. Sabourov, W. K. Warburton, W. B. Doriese, J. N. Ullom, M. K. Bacrania, A. S. Hoover, M. W. Rabin, *"High Rate Pulse Processing Algorithms for Microcalorimeters,"* submitted to IEEE Transactions on Nuclear Science (2008).

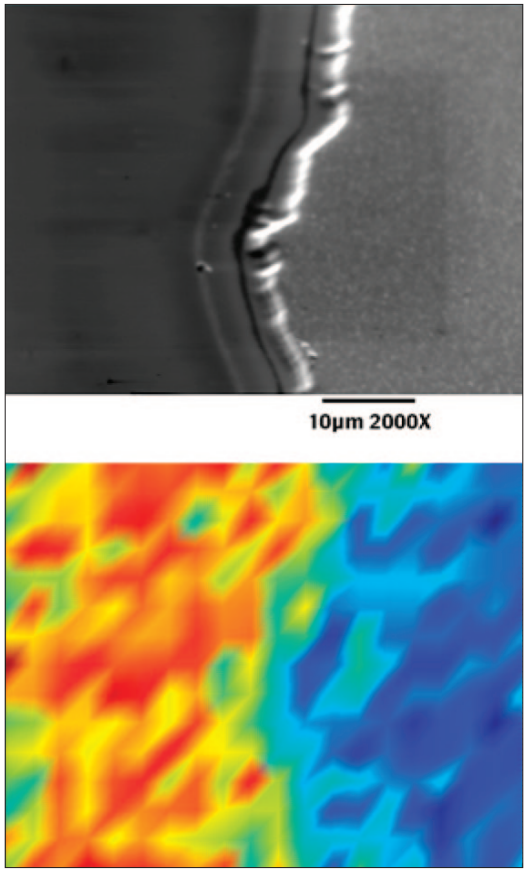

Figure 7. SEM photo (top) of an aluminum fi lm partially covering a sapphire substrate and a false-color map (bottom) of the shift in the mean X-ray energy of the Al Kα peak taken using a microcalorimeter EDS system. The shift in energy is due to the chemical bonding of the aluminum with the oxygen. The average energy shift is ~0.2 eV.

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Device Design and Characterization Program

As microelectronics pushes into the nanoelectronics regime traditional CMOS reaches fundamental limits; new device structures such as Multi-Gate FETs (MUGFETs), fully depleted and partially depleted silicon-on-insulator, various alloys such as silicon-germanium and silicon-germanium-carbon, strained layers and other exotica such as carbon nanotube, spintronic, and phase change and molectronic device structures need to be characterized. Another addition to the portfolio is the emerging field of organic materials electronics. With all of these changes taking place, NIST has established the Center for Nanoscale Science and Technology (CNST), a multidisciplinary center composed of a research program and the Nanofab, a fee base, shared use user facility with advanced processing and metrology equipment suitable for advancing into the nanotechnology era.

Device Characterization and Reliability

Technical Contacts:
Kin P. Cheung
John S. Suehle

Goals

The goal of the Advanced Device Characterization and Reliability Project is to improve and develop reliability and electrical characterization tools for advanced and emerging CMOS technologies. Deliverables include test methods, diagnostic procedures, reliability data, electrical characterization methods, defect identification and defect generation mechanism, physical models for wear-out, and methodologies to determine energy band diagrams and barrier heights for advanced gate dielectric stack systems.

A specific focus is to increase the understanding of the relationship between gate metal, gate dielectric, and channel materials, their interface properties, and device electrical and reliability measurements.

Customer Needs

The Si microelectronics community is currently faced with major materials challenges to further scaling. The gate stack (i.e, the polysilicon gate, the SiO_2 dielectric, and the silicon substrate) that was the key enabler of integrated circuit technology for half a century, must now be entirely replaced with new materials to achieve higher performance and lower power dissipation. Higher dielectric constant materials will replace SiO_2 as a gate dielectric, metal will replace polycrystalline silicon as a gate electrode, and high mobility materials will replace silicon as a channel material. New device structures such as multi-gate transistor, raised source and drain, ultra-thin body, etc. will replace the conventional planer MOSFET. Accompanying these enormous changes are new and highly complex reliability issues that must be addressed.

Consumer electronics has been the main driving force for the industry. Everyday life is increasingly relying on electronics. Many functions in modern living demand increased reliability of electronics beyond the traditional standards. Some cannot tolerate any failures. These demanding reliability requirement posts new challenges that the IC industry now must face.

The characterization of current advanced and future CMOS transistors is a major measurement challenge. It is currently not possible, for example, to reliably measure the channel mobility directly on the minimum size transistors. Thus it is difficult to know if the transistor's performance is limited by series resistance or by channel mobility. It is not possible to measure CV directly on such transistors; thus many of the basic transistor parameters must be obtained indirectly. Advanced MOSFET structures may not have a way to contact the substrate, precluding the use of standard electrical characterization techniques. The issue of variability, which is a major issue for advanced CMOS technology, cannot be quantified easily without the ability of making these measurements. The need for new measurement capability is not limited to measuring the ever smaller devices. Measuring faster is also required. High performance is one of the driving forces for continued scaling. High-performance circuits have tight tolerance on transistor parameters. It is recently becoming clear that the transient shift of transistor parameters that can cause circuit failure occurs more easily in advanced CMOS technologies than in older generations of CMOS. It also is becoming clear that reliability assurance requires that the transistor be characterized at operational speed. However, the measurement of transistor parameters at full operational speed is not currently possible. This is a major deficiency that needs to be addressed. Device degradation is intrinsically a stochastic process. Reliability measurements must have good statistics to be useful. This is much more so in advanced CMOS due to variability issues. How to produce useful reliability data is itself a challenge that urgently needs a solution.

Technical Strategy

The main focus for this project is to develop device and reliability characterization methodologies for advanced and emerging CMOS technology.

We continue to improve electrical characterization techniques and methodologies to characterize charge trapping kinetics, threshold voltage, Vt, instability, defect generation rates, spatial and energetic defect profiles, and long term degradation such as time-dependent dielectric breakdown (TDDB) for both patterned device samples and blanket films obtained from our collaborators. Studies will be conducted to determine the effect of multiple interfaces on stress-induced defect generation and wear-out. It will be determined

what technique or combination of techniques provides the most consistent results for all films. The electrical results will be used to validate simulation models and compared to studies from various analytical materials characterization methods.

We will develop new measurement techniques. For example, optical-electrical combination techniques to quantify defects, defect energetics and defect positions. Such techniques are also good for band-alignment study of the gate stack. It can also be used to investigate the interface region specifically. Coupling with pure electrical techniques, a much better picture of what is happening can emerge. Another example is a specialized technique to detect a single defect to enable us to investigate how a single defect affects the behavior of a nano-scale transistor. We are particularly interested in developing new ultra sensitive CV measurement techniques to measure minimum size transistors directly. Another direction of measurement technique development is ultra-high speed measurements of transistor parameters. Finally, we will explore ways to improve the statistical quality of reliability data.

DELIVERABLES:

- Develop a fast, direct, wafer-level method of measuring the channel mobility of ultra-scaled transistors. 3Q 2009
- Develop a fast, direct, wafer-level method of measuring the series resistance of ultra-scaled transistors. 3Q 2009
- Develop an ultra-fast and ultra-sensitive capacitance probe to measure CV curve of minimum size transistors directly, as well as to study transient CV shifts after the stopping of electrical stress. 3Q 2009
- Develop a new electro-reflectance measurement technique for the investigation of defect generation in the high-κ/SiO_2 stack. 4Q 2009
- Conduct time-dependent dielectric breakdown study at lower field for the SiO_2/SiC system. 2Q 2009
- Conduct long term stability study of SiC power MOSFET. 3Q 2009
- Conduct electrical characterization and reliability investigation of an advanced transistor having high-κ gate dielectric and alternative channel materials such as InGaAs. 2Q 2009

Accomplishments

Investigate the origin of random telegraph noise and 1/f noise in MOSFET

Random telegraph noise (RTN) is expected to increase as the MOSFET continues to shrink. It has already been shown to be a serious reliability issue for SRAM as well as Flash memory. RTN and its related phenomenon, 1/f noise, have been used as a way to profile defects in the gate dielectric. The move to high-κ/metal gate for advanced CMOS technology makes defect profiling a pressing need. As a result, increasingly more groups turn to 1/f noise to probe the defects. These trends make the understanding of the physical origin of RTN and 1/f much more important than ever. Experiments conducted at NIST on ultra-scaled transistors with 1.4 nm nitrided oxide gate dielectrics have clearly shown that the most commonly used model in the last half a century to explain RTN and 1/f noise cannot be correct. Upon careful consideration, we found that none of the alternative models ever proposed can work either. This result forces all the previous reported results to be re-interpreted. Without a valid model for RTN and 1/f noise, there is no guidance to rely upon to deal with the increasingly serious problem encountered in ultra-scaled devices.

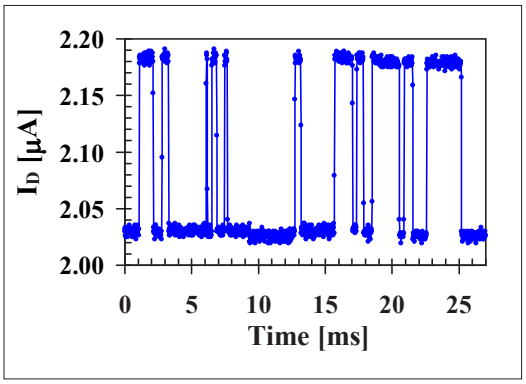

Figure 1. Random telegraph noise in the drain current of an ultra-scaled nMOSFET

Confirm the severity of RTN in subthreshold operation

Ultra-low power devices and circuits are highly desirable for portable application as well as medical application. One approach to ultra-low power is to operate at subthreshold regime of the MOSFET. This approach is being taken increasingly seriously. However, there are many challenges and the design community is taking more and more of these challenges into account. One issue is the greatly increased RTN in the subthreshold region of operation. This has been theoretically predicted but not experimentally verified. Experiments at NIST have confirmed the theoretical prediction that the magnitude of RTN increases as gate overdrive decreases. This is clearly a serious

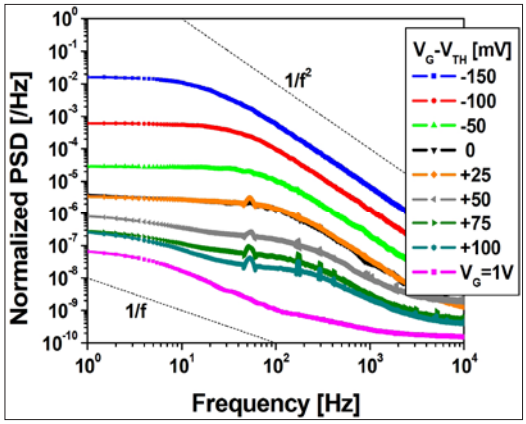

Figure 2. Measured noise power spectral density for a wide range of gate overdrive

limitation for ultra-low power circuit technique based on subthreshold operation.

Giant RTN effect observed

With an ultra-scaled transistor, it is well known that there are very few dopant atoms within the channel region. The statistical fluctuation of the number of dopants in a channel is a well recognized problem in ultra-scaled devices. The result is an increase in threshold voltage fluctuation – a serious problem. The placement of the few dopant atoms within the channel is largely random, leading to a random local field distribution. Another factor that affects the local field distribution is the random placement of charged defects. There is a finite probability that the two factors that affect the local field exist in proximity of each other and thereby amplify the overall effect. As the

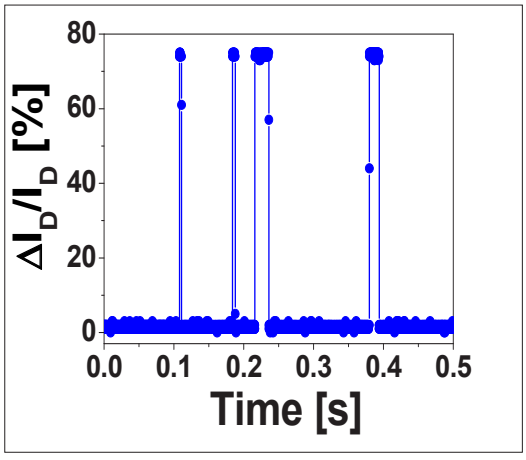

Figure 3. Giant RTN with almost 80 % modulation of drain current

device shrinks, the possibility that the combine effect will pinch off the channel increases. Such an event leads to giant fluctuation in the drain current. Using an ultra-scaled device, this phenomenon was confirmed at NIST recently. This is another problem area that confronts the future of CMOS technology.

A wafer-level Hall effect measurement for mobility extraction

The Hall measurement is a well established method for mobility extraction, and mobility extraction is of fundamental importance in device development. Yet a Hall measurement is rarely done because it is very inconvenient to perform. Specialized equipment that is both bulky and expensive is needed. Most of the time, the wafer needs to be diced and packaged before a Hall measurement can be done. We developed a wafer-level Hall measurement method that can be done with standard wafer probe stations. The only requirement is a small permanent magnet roughly 1 cm^3 in size mounted on a positioner just like

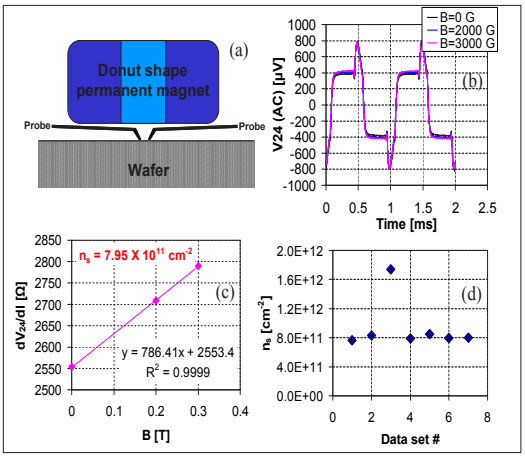

Figure 4. (a) the added magnet on top of the standard probes; (b) Hall voltage at various magnetic fields with drain bias modulation; (c) Hall voltage as a function of magnetic field showing the zero field offset; (d) extracted sheet charge density under repeated measurements at 10 V gate bias (the one high point is at 15 V gate bias)

standard probes. Fig. 4(a) shows the magnet positioning just above the standard probes. Moving the magnet up and down allows the magnetic field to be adjusted. Hall measurement is done at constant gate bias and a modulating drain bias. The as measured voltage across the Hall contacts is shown in fig. 4(b). Because of the small magnetic field, this voltage should be small. It is not small because of the asymmetry of the Hall structure. Fig 4(c) shows the Hall voltage as a function of magnetic field. The zero field offset is the component due to asymmetry. From the slope, one can extract the sheet resistance. Fig. 4(d) shows the

repeatability of the sheet carrier density extraction. Each measurement is completely independent (probes are all raised in between) but on the same SiC MOSFET Hall bar. Gate bias was set at 10 V (VTH = 7.5V) except the one high point for which the gate bias was 15 V. Mobility extraction can then be done (with the sheet resistance measured independently).

Standards Committee Participation

JEDEC JC14.2 Committee on Wafer-Level Reliability, Dielectric Working Group, Chairman (John S. Suehle).

Professional Committee Participation

North American Subcommittee Chair, 2010 VLSI- Technology, System and Application Conference (KPC).

Executive Committee Chair, 2009 IEEE International Reliability Physics Symposium.

2009 ITRS PID TWG in charge of reliability (KPC).

Technical Committee, 2009 IEEE International Conference on Integrated Circuit Design & Technology (KPC).

Technical Committee, 2009 Nano Science & Technology Institute Nanotech Conference (KPC).

Technical committee, 2009 VLSI- Technology, System and Application Conference (KPC).

General Chair, 2008 IEEE International Reliability Physics Symposium (JSS).

Technical Committee Vice Chair, 2008 IEEE International Reliability Physics Symposium (KPC).

Tutorial speaker, 2008 IEEE International Reliability Physics Symposium (KPC).

Technical Program Committee Chair 2008 IEEE International Electron Device Meeting (JSS).

Technical Committee, 2008 IEEE International Conference on Integrated Circuit Design & Technology (KPC).

Technical Committee, 2008 Nano Science & Technology Institute Nanotech Conference (KPC).

Chairman of Dielectric Working Group, JEDEC JC14.2 Committee on WLR (JSS).

Management Committee IEEE Integrated Reliability Workshop (JSS).

Special Member of Graduate faculty, University of Maryland (JSS).

Special Member of Graduate Faculty, Rutgers University (KPC).

Guest editor for Special Issue IEEE Tran. on Device and Materials Reliability (JSS & KPC).

Editor, IEEE Transactions on Electron Devices (JSS).

Collaborations

IBM, Alternative Gate Dielectrics.

Micron, Boise, ID, Characterization of metal gate dielectric systems.

ARL, Characterization of defects and reliability of SiC gate dielectric systems.

GE, Reliability characterization of SiC gate dielectric systems.

Intel, Characterization of high-κ/InGaAs systems.

SEMATECH Characterization of metal gate high-κ systems.

Rutgers University, Characterization of high-κ gate dielectrics.

University of Maryland, College Park, ultrathin gate oxide reliability, combinatorial analysis of advanced gate stacks.

U. Texas at Austin, Optical properties of ZrO_2 and HfO_2 for use as high-κ gate dielectrics.

U. Texas at Dallas, high-κ gate dielectric systems.

Purdue, high-k on III-V.

Recent Talks/Publications

K. P. Cheung, "On the 60 mV/dec @300 K Limit for MOSFET Subthreshold Swing," submitted to IEEE Electron Dev. Lett.

J.P. Campbell, J. Qin, K.P. Cheung, L. Yu, J.S. Suehle, A. Oates, K. Sheng, "The Origin of Random Telegraph Noise in Highly Scaled nMOSFETs." International Reliability Physics Symposium April 2009.

J.P. Campbell, L.C. Yu, K.P. Cheung, J. Qin, J.S. Suehle, A. Oates, K. Sheng, "Random Telegraph Noise in the Sub-Threshold Operation of Nano-scale nMOSFETs," Electron Dev. Lett., Submitted.

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J.P. Campbell, K.P. Cheung, J.S. Suehle, A.S. Oates, *"The Negative Bias Temperature Instability vs. High-Field Stress Paradigm,"* International Conference on Integrated Circuit Design & Technology, 2009, invited.

L. Yu, K. P. Cheung, J. S. Suehle, J. P. Campbell, K. Sheng, A. J. Lelis, S.-H. Ryu, *"Channel Hot-Carrier Effect of 4H-SiC MOSFET"*, Materials Science Forum Vols. 615-617 (2009) pp 813-816

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J.P. Campbell, K.P. Cheung, J.S. Suehle, A. Oates, *"Additional Insight into Device Transient Behavior from Fast-GM Measurements,"* IEEE Electron Dev. Lett., 29(9), 1065(2008).

L. Yu, K. P. Cheung, J. S. Suehle, K. Sheng, *"Intrinsic Oxide*

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J.P. Campbell, J. Qin, K.P. Cheung, L. Yu, J.S. Suehle, A. Oates, K. Sheng, *"The Origins of Random Telegraph Noise in Highly Scaled SiON nMOSFETs"*, 2008 International Integrated Reliability Workshop, Oct. 2008.

Kin P. Cheung, J.P. Campbell, *"The transient behavior of NBTI - A new prospective"*, International Conference on Solid-State and Integrated-Circuit Technology, Oct. 2008, Beijing, China, Invited.

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H. D. Xiong, Dawei Heh, Shuo Yang, Xiaoxiao Zhu, Moshe Gurfinkel, Gennadi Bersuker, D. E. Ioannou, Curt A. Richter, Kin P. Cheung, and John S. Suehle, *"Stress-induced defect generation in HfO_2/SiO_2 stacks observed by using charge pumping and low frequency noise measurements,"* 2008 IEEE International Reliability Physics Symp., Pheonix, AZ, USA.

Curt A. Richter, Hao D. Xiong, Xiaoxiao Zhu, Wenyong Wang, Vincent M. Stanford, Qiliang Li, D. E. Ioannou, Woong-Ki Hong, and Takhee Lee, *"Measurements for the reliability and electrical characterization of semiconductor nanowires"*, 2008 IEEE International Reliability Physics Symp., Pheonix, AZ, USA, invited paper.

J.P. Campbell, K.P. Cheung, J.S. Suehle, A. Oates, *"Electron Trapping: An Unexpected Mechanism Of NBTI AND ITS Implications,"* 2008 VLSI Technology Symp., Hawaii, USA.

Kin P. Cheung, and John S. Suehle, *"The Challenge of Measuring Defects in Nanoscale Dielectrics,"* invited paper, 2008 Electrochemical Soc. Meeting, Phoenix, AZ, USA.

D.H. Hill and R.A. Bartynski, N.V. Nguyen, Albert C. Davydov, and Deane Chandler-Horowitz, and Martin M. Frank, *"The relationship between local order, long range order, and sub-bandgap defects in hafnium oxide and hafnium silicate films"*, Applied Physics Letters, submitted.

Oana D. Jurchescu, Behrang H. Hamadani, Hao D. Xiong, Sungkyu K. Park, Sankar Subramanian, Neil Zimmerman, John E. Anthony, Thomas N. Jackson, and David J. Gundlach, *"Correlation between microstructure, electronic properties and flicker noise in organic thin film transistors"*, Appl. Phys. Lett., in press.

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Y. Wang, K. P. Cheung, R. Choi, B.-H. Lee, *"An Accurate Capacitance-Voltage Measurement Method for Highly Leaky Devices,"* IEEE Trans. Electron Dev. submitted.

N. V. Nguyen, H. D. Xiong, J. S. Suehle, and O. Kirillov, E. M. Vogel,P. Majhi and H.-C. Wen, *"Internal Photoemission Spectroscopy of [TaN/TaSiN] and [TaN/TaCN] Metal Stacks"*, Applied Physics Letter, 92, 092907 (2008).

N. V. Nguyen, O. A. Kirillov, W. Jian, J. E. Maslar, W. A. Kimes, and J. S. Suehle, *"Interface Barrier Determination by Internal Photoemission: Applications to Metal/Oxide/Semiconductor Structure",* Invited paper, 2008 Electrochemical Soc. Meeting, Phoenix, AZ, USA.

J. E. Maslar, W.S. Hurst, D.R. Burgess, W.A. Kimes, N.V. Nguyen, E.F. Moore, J.T. Hodges, *"In Situ Gas Phase Diagnostics for Hafnium Oxide Atomic Layer Deposition"*, Invited paper, 2008 Electrochemical Soc. Meeting, Phoenix, AZ, USA.

J. J. Kopanski, M. Y. Afridi, S. Jeliazkov, W. Jiang, T. Walker, *"Scanning Kelvin Force Microscopy For Characterizing Nanostructures in Atmosphere,"* Proceedings of the International Conference on Frontiers of Characterization and Metrology for Nanoelectronics, pp. 530-534, Gaithersburg, MD, March 27-29, 2007. (Sept. 2007).

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J. J. Kopanski, *"Scanning Capacitance Microscopy for Electrical Characterization of Semiconductors and Dielectrics,"* in the book: Electrical and Electromechanical Characterization by Scanning Probe Microscopy, Springer Science + Business Media, Inc., New York, NY (Feb. 2007).

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Nanoelectronic Device Metrology

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Goals

The overall goal of the Nanoelectronic Device Metrology (NEDM) task is to develop the metrology that will help enable the heterogeneous integration of new nanoelectronic information processing technologies with Complementary Metal Oxide Semiconductor (CMOS) to extend integrated circuit technology to and beyond the end of conventional CMOS dimensional scaling and, eventually, to enable the invention of a new information processing platform technology. Specifically, the NEDM is developing the precise metrology and measurement methods required for the systematic characterization of emerging nanotechnologies such as Si-based nanoelectronic, semiconductor nanowire transistors, carbon-based (e.g., carbon nanotubes, and graphene) electronics, and molecule-based devices.

NIST scientists are deeply involved in a wide range of nanoelectronics research. The goal of the Nanoelectronics Device Metrology (NEDM) project is a fundamental one. Project scientists are developing a total metrology package – a set of new tools, tests, and methods for the coming age of nanoelectronics – that will help nanotechnologies enter the marketplace more quickly. Such a large task is well suited to NIST's uniquely broad expertise and experimental capabilities.

Customer Needs

Nanoscale electronic devices, with components on the billionth-of-a-meter scale, represent one of the most active fields of electronics research. Mainstream CMOS, which is the current basis of ULSI (Ultra-Large-Scale Integration) circuits, is approaching fundamental limits associated with the laws of quantum mechanics and the limitations of fabrication techniques. As stated in the 2007 International Technology Roadmap for Semiconductors (ITRS), "The semiconductor industry is facing two … difficult challenges related to extending integrated circuit technology to and beyond the end of CMOS dimensional scaling. … extending CMOS beyond its ultimately scaled density and functionality by [heterogeneously integrating new information processing technologies with CMOS, and] … [extending] information processing substantially beyond that attainable by CMOS alone using an innovative combination of new devices and architectural approaches … and, eventually, inventing a new information processing platform technology." This need is so strong that a consortium of companies in the Semiconductor Industry Association (SIA) has established the Nanoelectronics Research Initiative (NRI). NIST is teaming with the NRI to accelerate research in nanoelectronics.

The materials traditionally used in Si-based CMOS will not be sufficient to overcome the barriers associated with these difficult challenges. New nm-scale materials will need to be developed, characterized, and incorporated into information processing devices and architectures to extend CMOS performance and/or functionality. It is expressed in the 2007 ITRS that improved metrology tools are needed to enable viable emerging material technologies and guide their evolution. The NEDM aims to provide this critical measurement science.

Two promising beyond-CMOS technologies that each takes a very different fabrication approach are molecule-based devices and Si-based quantum electronic devices. Molecule-based devices are based upon bottom-up fabrication paradigms, while Si-based nanoelectronics are based upon the logical continuation of the top-down fabrication approaches used in CMOS manufacturing. These two approaches bracket the possible manufacturing techniques that will be used to make future nanoelectronic devices.

Many predict that molecule-based devices will have important technological impacts on the computational and communication systems of the future. In these systems, molecules perform the functions of electronic components. Alternatively, research and development for silicon-based nanoelectronics (e.g., Si-nanowire FETs, Si-based RTDs [resonant tunneling diodes], and silicon quantum dots) for the post-CMOS era are currently of interest due to their inherent compatibility with CMOS technology.

Carbon-based materials, particularly graphene and carbon nanotubes (CNTs) have emerged as perhaps the most promising of the research materials for next generation electronics. Graphene (a recently discovered form of carbon consisting of a single atomic sheet of carbon in a hexagonal lattice) is a high-mobility semi-metal with a distinctive linear energy momentum dispersion relation. Graphene's excellent room-temperature

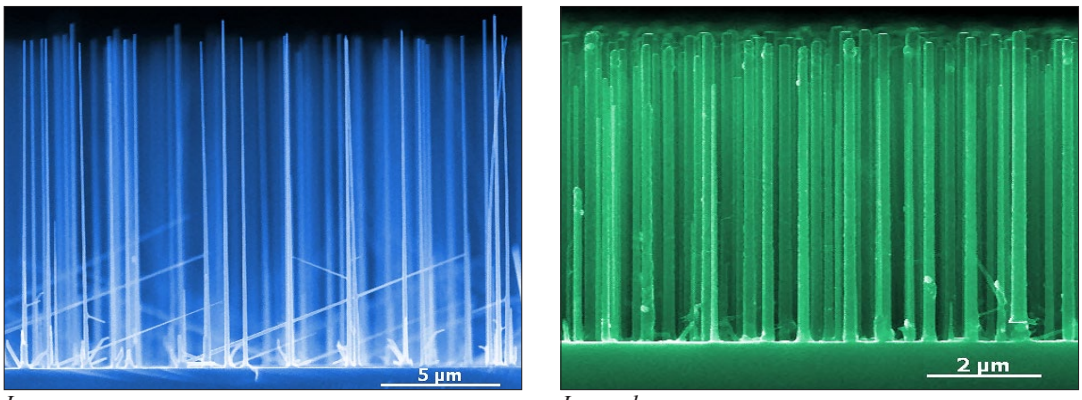

Image a *Image b*

Figure 1. Si NW arrays grown in the CVD reactor from SiC_{l4} precursor at 850 °C. Note how NW shape changes from a) to b) with increasing SiC_{l4} concentration.

mobility relative to conventional semiconductors makes it a promising high mobility channel replacement material for charge-based transistors. The NIST graphene team is developing electrical metrology to enable the advancement of both conventional charge-based and non-conventional beyond-CMOS graphene-based electronics.

Before bulk carbon nanotubes can fulfill their promise for multifunctional (electronic, electrical, structural, thermal) composites, better methods are needed for purification, dispersion and identification of raw nanotube materials. Predicted nanotube behavior may be compromised by the presence of impurities and molecular defects. Simple, inexpensive and scalable methods are preferred for characterizing bulk material in the presence of impurities and defects. In addition, reproducible measurement results are difficult due to physical contact between the metrology instrument and the nanomaterials. We are working toward purification and dispersal by laser processing rather than wet chemistry. In addition, we continue to pursue non-contact metrology of electronic and optical properties.

Low-dimensional structures such as CNTs and semiconductor nanowires are among the candidates to replace the FET channel in MOSFETs with a higher carrier mobility material than strained Si. The NEDM is utilizing Si-nanowires (SiNWs) as the test platform to develop the measurement science necessary to enable the utilization of quantum confined structures to extend the performance of traditional CMOS devices. In order to have effective test structures for metrology development, we are making advances in experimental NW growth (as shown in Figures 1 & 2) and device fabrication as well as material and device characterization.

In all these cases, our project has the capability to offer early guidance to these emerging fields and to assist companies in pursuing productive areas and rejecting problematic ones. Because these fields are not yet mature, as our relatively moderate efforts progress, they can yield large payoffs for the customers.

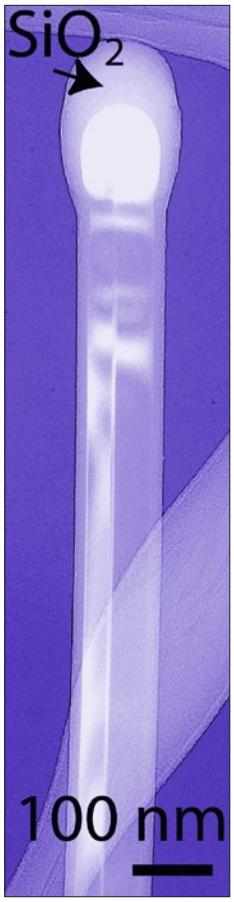

Figure 2. TEM images of SiNWs oxidized for 5 min at 900 °C in RTO furnace

Technical Strategy

The Nanoelectronic Device Metrology project aims to develop new measuring techniques and standards that are crucial in the effort to develop these technologies to the point where commercial applications become feasible. This task involves determining the critical metrology needs for these exploratory technologies. Ultimately, this project will yield a toolbox of measurement methods that will allow engineers to relate the performance of nanoelectronic devices to

the structures and properties of the materials of which they are made.

The NEDM task's technical strategy is to develop innovative measurement methods for specific emerging nanoelectronic systems (i.e., emerging research devices and materials) spanning a range of technologies. By collaborating with NRI-sponsored researchers, NIST will be able to ensure that its programs focus on developing critical measurement tools likely to accelerate advances in this visionary, high risk area of research. Following are brief descriptions of the NEDM's strategies for developing the critically needed measurement tools to enable successful advances in nanoelectronics.

Develop the electrical and physical metrology of Si-based nanoelectronics. The focus of this task is the basic building blocks of silicon quantum electronic devices (e.g., quantum layers, wires, and dots of silicon surrounded by silicon dioxide). By identifying and addressing the critical metrology issues associated with these basic building blocks, the basis of metrology for future Si-based ULSI nanotechnology will be defined. The NEDM is currently focusing on Si-nanowires: their growth, device assembly approaches, and advanced electrical characterization. Our short- and long- term plans include growth of SiGe alloy and Si/Ge core-shell NW heterostructures; development of controlled n- and p- doping of Si and Ge NWs; fabrication of *in-situ* grown SiNW arrays in microfluidic channels and development of advanced FET NW device structures for sensor applications. We have developed a simple in situ directed growth method fabricating SiNW devices, and are using it to make and characterize devices (such as high-performance transistors and charge trapping memory structures) incorporating high-κ gate dielectrics such as illustrated in Figure 3. We are developing advanced test structures and improved electrical test methodologies such as (i) advanced capacitance measurement techniques for critical small (aF-scale) capacitances in nanoelectronics devices such as nanowires and (ii) applying improved noise characterization to determine technical validity of innovative nanoelectronic structures and probe-scattering dynamics.

DELIVERABLES:

- Characterize steep sub-threshold Si-nanowire transistors for logic applications. Prepare and submit manuscript. 3Q 2009.
- Characterize SiNW-based charge trapping memory devices incorporating high-κ gate dielectric stacks. Prepare and submit manuscript. 4Q 2009.
- Development of controlled doping of Si and Ge nanowires from solid boron- and phosphorus-containing precursors. 4Q 2009.
- Growth of SiGe nanowires with axial and radial modulation of Ge content. Q2 2010.

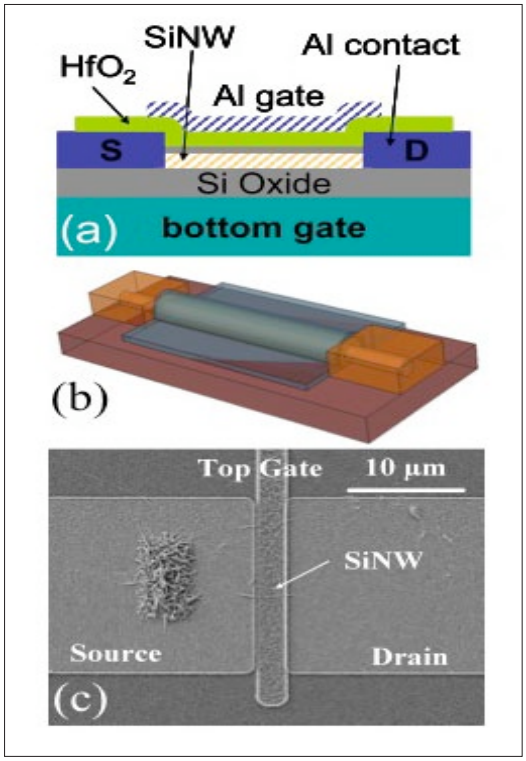

Figure 3. SiNW FET formed by directed self-assembly.

Develop robust molecular test structures in order to use them to measure the electrical properties of molecules. The measured electrical properties will be correlated with systematic characterization studies by a variety of advanced analytical probes and the results used to determine charge conduction mechanisms and in the validation of predictive theoretical models.

DELIVERABLES:

- Systematically characterize critical parameters to optimize flip-chip lamination methods for reliably forming metal/molecule/Si junctions. 3Q 2009.
- Investigate the effect of dipolar changes and interfacial charge-transfer at the molecule-semiconductor interface with chemical and/or electrical probes to understand critical factors for semiconductor-based molecular electronic junctions. Prepare manuscript. 1Q 2010.

Develop spectroscopic probes to measure the impact of contact, orbital geometry, and molecular structure of molecular films bound to solid surfaces. Determine the interface dipole and the change to surface work function of molecular films on solid surfaces. A longer term goal is to determine the factors that influence energy level alignment on molecular films bound to metal and semiconductor surfaces.

DELIVERABLES:

- Measure the hole-injection barriers to molecular layers bound with multiple bonding groups onto metallic surfaces. 2Q 2009
- Determine and model effect bonding chemistry and surface coverage have on the change to surface work function of molecular films on metallic surfaces. 3Q 2009

Because of its unique properties, graphene may revolutionize aspects of commercial electronics and optoelectronics. The knowledge base and measurement tools to understand the basic physics of graphene, such as the characterization and control of defects, the effect of defects and substrate properties on charge transport, the coupling between charge and photons, and how to measure and optimize device properties (such as electrical contacts) are under development. These are the necessary metrology tools to enable the emergence of promising graphene technologies.

DELIVERABLES:

- Characterize CNT FETs under stress: Gain insights into the nanoelectronic reliability of CNT FETs by studying their noise properties under high voltages and currents. 3Q 2009
- Test quality of exfoliated graphene quantum Hall effect devices for use as resistance standards. 3Q 2009
- Fabricate and electrically characterize suspended graphene devices to eliminate substrate interactions. 2Q 2010

Establish a quantitative characterization toolbox for practical measurements of bulk nanomaterials building upon non-contact probes recently pioneered at NIST. This toolbox will provide rapid, quantitative methods for identifying CNT properties. Existing measurement tools are neither practical nor useful for current and future large-scale production of nanomaterials. These protocols often rely on physical contact between the test probe and the material under study. However, physical contact between probes and nanomaterials may alter the material property of interest. Advanced, cost effective analytical techniques are needed so that manufacturers, product developers, and regulatory agencies can truly "see" what they have. Photons, being massless and chargeless are an ideal, non-contact probe of nanoscale properties.

Accomplishments

■ *Silicon-based molecular electronic structures formed by using Flip-Chip lamination.* A substantial barrier to the realization of molecular electronics is the formation of the top metal electrode. We developed a novel approach to obtain high-quality silicon-molecule-Au molecular electronic structures schematically shown in Figure 4. This approach overcomes two limiting challenges and allows (1) the formation of high-quality bi-functional monolayers on silicon and (2) the attachment of a metal electrode to the molecular layers on silicon. We utilize a novel nanotransfer printing (nTP) technique to first obtain ultrasmooth gold films on flexible plastic substrates. This allows us to fabricate dense monolayers by using self-assembly, a process that is not chemically feasible on Si due to the large molecular sticking coefficient. Second, these dense carboxylate-functionalized thiol monolayers on Au are chemically bonded to silicon by using a flip-chip lamination process, overcoming the detrimental aspects observed with conventional metallization (i.e. molecular displacement and metal filament formation). In this way, we

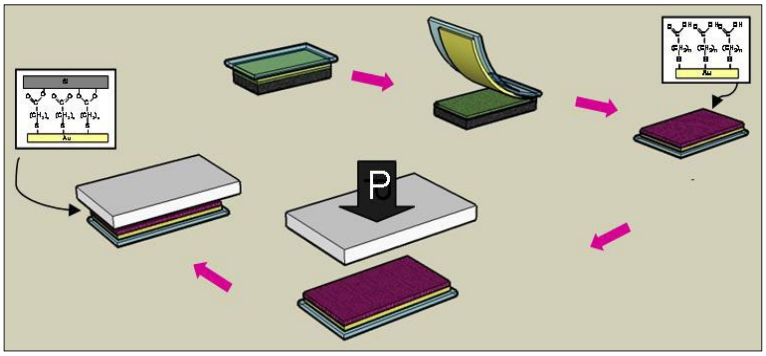

Figure 4. Flip chip lamination to form reliable metal/monolayer/Si molecular junctions.

are able to obtain dense bifunctional monolayers bonded to both silicon and ultrasmooth gold electrodes under mild conditions.

High-quality monolayers on semiconductor substrates are one of the most promising configurations for future generations of molecular-based devices for semiconductor electronics, biosensing, and optoelectronic applications. These results represent an essential advance in the reproducible fabrication of molecular junctions with high yield and fidelity. In addition, this approach can be extended to a variety of molecules and electrodes extending our impact into many technologies.

■ *Capacitance test structures for on-chip evaluation of nanoelectronic devices:* A test chip to evaluate the performance of new approaches to the measurement of small capacitances (femto-Farads to atto-Farads range) has been designed, fabricated, and systematically characterized. The test chip consists of an array of metal/oxide/semiconductor (MOS) capacitors, metal/insulator/metal (MIM) capacitors, and a series of systematically varying capacitance structures directly accessible by an atomic force microscope probe. The nominal capacitances of the test devices range from 0.3 fF (10^{-15} F) to 1.2 pF (10^{-12} F). Measurement of the complete array of capacitances by using an automatic probe station produces a "fingerprint" of capacitance values from which, after correction for pad and other stray capacitances, the relative accuracy and sensitivity of a capacitance measurement instrument can be evaluated.

■ *Investigation of using molecular structure as a dopant in conductive molecular films.* Metal-molecule-metal junctions composed of organic molecular wires formed via self-assembly are relevant in the empirical testing of molecules used in electronics. One key is to understand the way the monolayer structure effects transport through arrays of molecules. We studied how the molecular electronic levels evolve under the influence of molecular substitution, metal substrate, and intermolecular interactions. We used a joint experimental and computational approach to study the electronic structure and electrostatic properties of a series of self-assembled donor and acceptor substituted (oligo)pheneylene-ethynylenethiols on gold. Photoemission spectroscopy was used to determine the energy-level alignment for the monolayers, the change to the work function upon chemisorptions, and the monolayer coverage. Isolated molecule and small cluster calculations were performed to detect changes in geometry, electronic structure, and charge distribution upon chemisorption. The calculated densities of electronic states allowed for the assignment of the higher-lying occupied states provided by the photoemission data. Calculated estimates of the surface, bond dipole, and image potential energies were used to estimate contributions of each to the measured work function change. Good correlation between the experimental and theoretical values was found as illustrated in Figure 5. Importantly, the results point to a dependence of the dipole contributions on the orientational order of the self assembled monolayer (SAM). One avenue for "doping" molecules has been through substitution. These data also illustrate that substitution of conjugated molecular films does not affect the alignment of the valence molecular states, and other avenues may need to be explored.

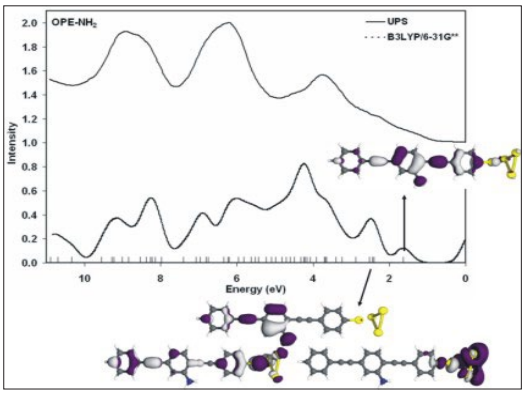

Figure 5. Comparison between the photoemission spectrum (top) and theory (bottom) for an OPE; the vertical bars refer to the shifted energies of the occupied molecular orbitals. Molecular orbitals densities for the first few valence orbitals are also provided

■ *Demonstration of synthesis and growth of molecular films with tunable barriers and dipoles.* Two parameters of interest in the design of interfaces are the barriers to charge injection and the work function. In the case of monolayer covered surfaces these two parameters have been difficult to independently tune due to factors such as designing and synthesizing compounds with known valence energies, understanding how these orbitals align when bound to a surface, and predicting how the molecular dipole will alter the metal work function. We have designed a set of experiments to tune both parameters in-

dependently by modifying the molecular dipole base while keeping the molecular core constant using substituted biphenyl dithiols. Monolayers were grown on Au and photoemission spectra of each film were measured to determine the position of the highest occupied molecular state and the change in the substrate work function, where the change to the substrate work function is related to the dipole of the molecule. We observed that through isolation of the molecular core from the molecular terminus we were able to tune the substrate work function with no measureable variation in the occupied valence states. The substrate work function was also highly dependent on monolayer coverage. Thus, through careful growth conditions and selection of the molecule both the work function and valence electronic properties can be independently controlled.

■ *New reactor for growing doped Si, Ge, and SiGe nanowire heterostructures.* S. Krylyuk and A. Davydov have built a versatile CVD system for fabricating Si, Ge, and SiGe alloy thin films and nanowires (NWs). The system includes a hot-wall horizontal reactor with four independently controlled temperature zones; it is equipped with a computer-controlled gas delivery system. The reactor is designed to be capable of growing Si and SiGe alloys on substrates up to 2" in diameter at atmospheric or reduced pressure. The system utilizes SiH_4 and $SiCl_4$ as Si sources, solid Ge or $GeCl_4$ as Ge sources, solid boron-based and phosphorus-based sources for p- and n- type doping, and H_2 and HCl gases for *in-situ* growth modulation and reactor etching. This set of precursors allows the conduction of NW growth in a wide temperature range from 450 °C to 1050 °C. The reactor design enables rapid growth interruption/restoration, which is essential for realization of abrupt interfaces in fabricated heterostructures, such as axial p/n junctions in NWs.

The new CVD system significantly enhances NEDM's capability of fabricating Si and SiGe nanostructures with desired structural and electronic properties for nano-metrology needs. We have succeeded in growing vertically aligned Si NW arrays with controlled dimensions and morphology (NW length, diameter, shape, and degree of tapering). Fig. 1 shows two sets of Si NWs with conical (a) and prismatic (b) shapes, where the NW shape is controlled by concentration of $SiCl_4$ source in the reactor. We have also studied the kinetics of Rapid Thermal Oxidation (RTO) of Si nanowires (see Fig. 2). Our results demonstrated that RTO can be employed for rapid fabrication of uniform oxide shells over NWs with controlled thicknesses suitable for device applications. Compared to conventional furnace oxidation, RTO eliminates oxide growth retardation with respect to planar Si and exhibits much weaker dependence of oxide thickness on the Si NW diameter.

■ *Advanced Measurement Methods for Nanowire-Based Nanoelectronic Devices:* Researchers in EEEL's Semiconductor Electronics Division have made advances in the electrical characterization of semiconductor nanowire-based nanoelectronic devices. The researchers demonstrated simple and easily accessible approaches to fabricate and test the nanowire devices. These techniques should enable a large range of scientists to perform research to advance nanowire research and technology. The research efforts were published in the *IEEE Transactions on Electron Devices* special issue on "Nanowire Transistors: Modeling, Device Design, and Technology," November 2008. EEEL researchers, in collaboration with engineers at George Mason University, fabricated the nanowire devices via two unique approaches: one based upon harvesting and positioning nanowires and one based upon the direct growth of nanowires in predefined locations. Test structures were then fabricated and electronically characterized to probe the fundamental properties of the nanowires. Noise measurements obtained by these test structures provided important information about current transport and fluctuations in materials and devices. Noise measurements such as these are a powerful method for probing trapping defects in nanoelectronic devices.

■ *NIST Develops a Flexible Memristor:* We have demonstrated a flexible, solution-processed, nonvolatile, low power, inexpensive, TiO_2-based flexible memory component. The electrical behavior of this component is consistent with a memristor, an electrical device that has been recently touted as the missing fourth circuit element. Our flexible memory device has an operation voltage of less than 10 V, on/off ratios greater than 10,000:1, exhibits memory potential that is nonvolatile for over 1.2×10^6 s, and is operational after 4,000 flexes. This technology has potential advantages over existing flexible memory devices including low power operation, rewritability, and a simple two-terminal room temperature processed device design.

■ *Plasmonics in the optical cleaning of nanotubes.* It has been experimentally observed that amorphous carbon is removed from as-prepared, bulk, single-walled carbon nanotubes by illumination with 248 nm (5 eV) UV light. The process by which this occurs has not yet been rigorously identified before now. We have used a combination of experiments and modeling to explain how localized surface plasmon pairs can be induced at the surfaces of nanotubes. The 248 nm light near the resonant frequency of one of these plasmon pairs for small diameter nanotubes causes a large electric field enhancement in the vicinity of the tubes (Figure 6). The enhanced field increases the rate at which sp^{-2} bonds in the amorphous carbon are excited into a state from which the carbon is more easily oxidized. Classical electromagnetics, in conjunction with density functional theory, is used to quantify the field enhancement and the relationship between laser wavelength and nanotube radius which will result in cleaning.

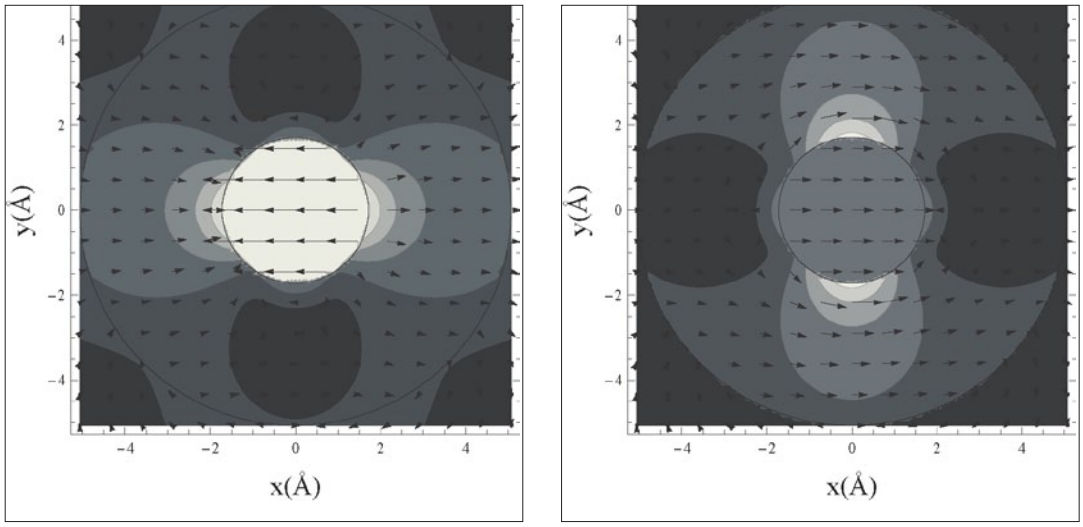

Image 6a *Image 6b*

Figure 6. Modeling the field enhancement surrounding a carbon nanotube in the presence of 248 nm (5 eV) excimer laser. The electric field in the infinite hollow conducting cylinder for a resonance at 5eV a) and at 6eV b) for the diameter of a (5,5) nanotube. It is noteworthy that both resonances have constructive and destructive interference between the surface plasmons.

■ *Measurement of photoconductive lifetimes of nanomaterial by non-contact methods.* Cheaper, better (non contact), and faster techniques are urgently needed to address properties of bulk nanomaterials. Accurate measurements of electrical properties and identification of transport phenomena are critical for engineering improvements and the efficient development of organic photoconductive materials. Measuring, understanding, and controlling the recombination lifetimes of nanotube and polymer composite films are essential for the progress of bulk nanotube electronics. We have implemented the method of resonantly coupled photoconductive decay (RCPCD) to measure the photoconductive behavior of bulk carbon nanotubes and carbon nanotube composites. The measurements provide a method, means, and information relevant to intrinsic and extrinsic bulk properties - independent of electrical contacts. Our objective is to use this metrology to understand and document the influence of nanotube morphology and charge transfer to maximize the photoconductive lifetime.

Initially presented at the America Frontiers of Engineering in Kobe, Japan (sponsored by the National Academy of Engineering), more recent results were shown at the 2009 spring MRS conference. We have begun assembling a second-generation RCPCD with collaborators at the Colorado School of Mines. (RCPCD is described as the impedance coupling between an antenna driven at frequencies between 400 and 1000 MHz and the photoconductive material, which is in the proximity of the antenna. The antenna is a component of a very high-Q resonant system, and the sample becomes coupled to the antenna system. The sample is mounted on a moveable platform such that the system resonant frequency may be changed by varying the sample coupling.)

■ *Optical properties of organic photovoltaics based on carbon nanostructures.* Improving the quantum efficiency of organic photovoltaics is a requirement for large-scale commercial use. It has been established that doping of conjugated-polymer films with single-walled carbon nanotubes (SWCNTs) facilitates exciton dissociation and electron transport. Accurate measurement of important extrinsic device properties such as absorbance with respect to film thickness and SWCNT concentration is necessary for informing our expectations for intrinsic photovoltaic efficiency. This is also the basis for modeling the role of the photoactive layer and maximizing the efficiency of the device. In this work, we explicitly measured the absolute absorbance of photoactive films by depositing them on a pyroelectric detector and modeled the optical function of the doped films based on Kramers-Kronig analysis. Raman spectroscopy, UV-VIS absorption, and four-point probe measurements provide further characterization of nanotube concentration and homogeneity of our films. Our study provides direct quantitative measurements traceable to NIST standards, which demonstrates that variations in the intrinsic efficiency of the photoactive layer directly correlate to the extrinsic efficiency of the SWCNT-polymer photovoltaics.

■ *NIST Team Proves Bridge from Conventional to Molecular Electronics Possible:* Molecular electronic devices were fabricated by using silicon of the same crystalline orientation as that used in standard microelectronics (CMOS) technology, Si (100). This breakthrough demonstrated that a single layer of organic molecules can be assembled on the same sort of substrate used in conventional microchips. The ability to use a silicon crystal substrate that is compatible with the industry-standard CMOS (complementary metal oxide semiconductor) manufacturing technology paves the way for hybrid CMOS-molecular device circuitry ─ necessary precursor to a "beyond CMOS" totally molecular technology ─ to be fabricated in the near future. Because the probable first step in the realization of molecular electronic devices will involve their integration with existing CMOS technology, it is imperative that molecular devices be fabricated using CMOS compatible materials, such as 100-oriented silicon. It was demonstrated that organic monolayers can be assembled on Si (100) that are comparable in quality, aliphatic monolayer coverage, and extent of substrate oxidation to those assembled on the more extensively studied, but CMOS-incompatible, Si (111) crystal face. Monolayers assembled on the CMOS-compatible Si (100) were characterized via spectroscopic monolayer characterization, as well as through the fabrication of Si (100)-based molecular electronic devices that exhibited molecule-dependent electrical characteristics.

■ *IETS Used to Probe Molecular Layers of Metal-Molecule-Silicon Devices:* In collaboration with researchers from Purdue, we demonstrated for the first time the use of IETS to probe transport properties of molecular layers in integrated metal-molecule-silicon (MMS) devices with molecules assembled directly to silicon contacts. The results provide direct experimental confirmation that the chemical integrity of the monolayer is preserved and that the molecules play a direct role in electronic conduction through the devices.

Molecular electronics has drawn significant attention for nanoelectronic and sensing applications. A hybrid technology where molecular devices are integrated with traditional semiconductor microelectronics is a particularly promising approach for these applications. Key challenges in this area include developing devices in which the molecular integrity is preserved, developing in situ characterization techniques to probe the molecules within the completed devices, and determining the physical processes that influence carrier transport. Traditional techniques for analyzing monolayer quality on silicon substrates such as X-ray photoelectron spectroscopy (XPS) and scanning probe techniques are surface-specific. Certain spectroscopic measurements of buried molecular layers can be performed, but they require device areas on the order of mm2, which are unsuitable for integrated metal-molecule semiconductor (MMS) devices in the micro- or nano-scale. The recent advance by EEEL-Purdue researchers has utilized the IETS technique for the first time to examine the transport in solid-state MMS devices with dimensions in the micro scale. Their experimental results not only successfully confirmed the organic species incorporated in the samples, but also revealed certain effects from the silicon electrode, presenting valuable information on the physics influencing carrier transport in these molecule/Si hybrid structures. The NIST study has established IETS as a critical nondestructive experimental method for the investigation of integrated semiconductor devices with active organic components and will assist

in the development of future feasible silicon–based molecular electronic devices.

■ *Spin-Polarized Inelastic Electron Tunneling Spectroscopy of a Molecular Spintronic Device Investigated by EEEL Researchers.* Researchers at NIST have fabricated and characterized molecular-monolayer magnetic tunnel devices. Molecular spintronic systems were fabricated by sandwiching a self-assembled monolayer of octanethiol between two ferromagnetic electrodes in a nanopore, demonstrating that single molecules can be used as the ultimate building blocks for spintronic devices. By using inelastic electron tunneling spectroscopy (IETS), Wenyong Wang and Curt Richter have obtained the first unambiguous experimental evidence of the existence of molecular species in such magnetic tunnel junctions. Tunneling spectroscopy was also utilized to investigate the spin-polarized inelastic electron tunneling processes in the molecular devices. The measurements revealed that inelastic scattering due to molecular vibrations is likely the main cause of an observed junction magnetoresistance bias-dependence. These results illustrate that such inelastic scattering events must be accounted for when predicting the performance of practical molecular spintronic devices. Molecular electronic devices with spin-dependent tunneling transport behavior offer an innovative and extremely enticing direction towards spin electronics, from both fundamental and technological points of view. Due to the weak spin-orbital and hyperfine interactions in molecules, the spin coherence over time and distance could be preserved much longer in molecular nanosystems than in traditional semiconductors, which makes them a suitable playground for spin manipulations.

■ *Laser-induced purification of single wall carbon nanotubes (SWCNTs).* We have further investigated the purification of as-prepared single-walled carbon nanotubes (SWCNTs) by exposure to ultra-violet (UV) light of various wavelengths in different atmospheres. Our initial work demonstrated that the excitation of the collective electron oscillations of the p-plasmon in the nanotubes by the 248 nm photons results in non-thermal removal of carbon impurities. Our recent results from 193 nm pulsed laser light and 254 nm continuous wave (CW) light supports the importance of resonance of photon energy with the π plasmon of sp^2 bonded carbon atoms, as well as demonstrates the importance of atmosphere, and the pulsed nature of the light. Analysis of Raman spectroscopy data has shown that the carbon impurities are more efficiently removed by the pulsed light for the same number of photons than by the CW light for roughly the same wavelength. We continue to investigate the photothermal, photophysical, and photochemical influences for the mechanism of purification of SWCNTs. We have considered differences in the thermal transport, including thermal conductivity, specific heat, and thermal diffusivity of carbon nanotubes compared with the thermal transport properties of impurity carbons. We have found that upon pulsed heating the nanotubes experience a smaller temperature increase than do other carbon impurities, and this difference enables the selective oxidation of the carbon impurities. The importance of the resonance of the p-plasmon of sp^2 carbon with the incident photons has also been a large focus of our work. The production of hot electrons and the simultaneous decrease in electron density as electrons are excited into an antibonding state of the carbon sp^2 bond is also considered. We continue to work closely with our theoretical collaborators at the Colorado School of Mines in order to provide a theoretical understanding to our experimental findings.

■ *Rapid and inexpensive identification of bulk carbon nanotubes.* The photoconductive recombination lifetimes of CNT thin films as a function of wavelength were measured by resonant-coupled photoconductive decay (RCPCD) method. The carrier recombination lifetime is a fundamental property of carbon nanotubes which is typically determined by contact-based techniques or spectroscopic methods. The RCPCD measurement is based on a pump-probe technique in which an optical pump and a low frequency microwave probe are employed and is well suited to characterization of bulk and extrinsic material properties. Our results demonstrate the role of purification and the effect of the interaction of nanotubes and polymers in thin films of multi-walled carbon nanotube and single-walled carbon nanotubes. Possible mechanisms describing the interaction of photoexcited carriers in the nanotube polymer composites are currently under investigation. We have reported the wavelength dependence of photoconductive lifetimes at meetings of the American Vacuum Society and the Materials Research Society. Raman spectroscopy and UV-VIS absorption

measurements provide further identification and characterization of nanotube samples to enable correlation of nanotube properties with the efficiency of charge transport.

A dielectric resonator-based measurement method for determining the electrical conductivity of carbon nanotubes at microwave to millimeter frequencies has been demonstrated. This measurement method is not limited by the metal conductor contact resistances or impedance mismatch commonly encountered in the measurement of single nanotubes. The measurement of carbon nanotubes yielded conductivities of approximately 0.08×107 S/m.

■ *Valence level alignment and identification of the charge carriers of molecules on metal surfaces*. We have systematically studied the valence level alignment for two bonding chemistries as a function of metal work function. Using ultraviolet photoemission spectroscopy we measured the energies of the highest occupied delocalized state for three thiol-linked molecules on Ag, Cu, Au, and Pt, which span a work function range of over 1 eV. These results showed that alignment of the occupied electronic structure is independent of the metal work function, but is dependent on the electronic structure of the molecule. We also observed a linear dependence on the change of the metal work function, where the higher work function metals exhibited a larger work function change. Taken together these data suggest that the molecule plays a larger role than the contact material in molecule-based devices. For the second bonding scheme we used isocyanide chemistry. Here we observed a shift of the occupied valence structure to deeper (higher) binding energies compared to those observed with thiol that is independent of the metal work function. This shift suggests that the charge carrier (holes vs. electrons) can be controlled using molecule-metal bonding chemistry. To test this we assembled molecules in crossed-wired molecular junctions on Ag, Au, and Pt and observed that the transition from direct tunneling to field emission is correlated with the unoccupied valence states in isocyanide-bound monolayers. In other words, the charge carriers are electrons for isocyanide-linked films; whereas, the carriers are holes in thiol-bound monolayers. These data show that photoemission spectroscopies can be utilized for prediction of some transport properties.

■ *Validating the unoccupied valence electronic structure of molecules on metals*. The metal-molecucle interface is key to understanding and controlling charge transport in nanoscale junctions. Here, the occupied and unoccupied valence electronic structure of a chemisorbed molecular layer on metals was measured using a combination of ultraviolet photoemission, two-photon photoemission (2PPE), and inverse photoemission (IPE) spectroscopies. By using both 2PPE and IPE the ionization processes between the two complimentary techniques was able to be determined. We observe that 2PEE and IPE give a very nuanced picture of the unoccupied electronic structure of the interfacial region. The excitation mechanism of each technique must be properly understood in order to reliably predict the unoccupied states involved in charge transport. Using both techniques we were able to assign and calculate the unoccupied electronic structure, and detail the electronic processes that arise in each measurement.

■ *Novel approach to investigate buried metal-organic interfaces for molecule-based devices.* We have developed and used a novel approach to investigate the top metal contact in metal-organic monolayer devices. In the emerging arena of molecular electronics, detailed characterization of organic monolayers encapsulated between two electrodes is necessary to correlate the electrical responses of molecular devices with the fundamental physical properties of the monolayers. The technique, a novel, straightforward optical measurement, p-polarized backside reflection absorption infrared spectroscopy (pb-RAIRS) developed at NIST, takes advantage of the natural infrared transparency of Si wafers to enable vibrational characterization of monolayer films after deposition of technologically relevant metal electrodes. This technique is applicable to any metal/molecule/substrate system where the substrate is IR transparent. The validation of the pb-RAIRS technique, via the molecular test bed, has resulted in new thrusts such as the application of the technique to the investigation of the metal/high-κ interface for advanced CMOS electronics.

COLLABORATIONS

Colorado School of Mines, Prof. Mark Lusk, *Ab initio* studies of pi plasmon role in bundling, functionalization and optical properties of carbon nanotubes.

Colorado School of Mines, Richard Ahrenkiel, Resonantly coupled photoconductive decay lifetime measurements of CNTs and CNT-polymer composites.

Columbia, Prof. Philip Kim, Graphene-based resistance standards.

George Mason University, Prof. Qiliang Li, Novel nanowire devices and test structures.

Gwangju Institute of Science and Technology, Korea, Prof. Takhee Lee, Scattering processes in ZnO nanowire.

Hewlett-Packard, R. Stanley Williams et al., Characterization of advanced crossbar technologies.

National Renewable Energy Laboratory, A. C. Dillon, Optical properties of CNT materials.

NIST Division 838, Dr. James Kushmerick, Molecular charge transport.

Notre Dame, Alan Seabaugh, Graphene-based transistors.

Princeton University, Prof. Antoine Kahn, Validating the unoccupied valence electronic structure of molecules on metals.

Purdue University, Prof. David Janes, Hybrid Si-molecular devices and test structures.

Rice University, Prof. James Tour, Valence level alignment and identification of the charge carriers of molecules on metal surfaces.

University of Maryland, Prof. Ellen Williams, Contacts to enable molecular electronics.

University of Notre Dame, Prof. Greg Snider, Si single-electron device fabrication.

University of Texas, Prof. Eric Vogel, Si nanowire and graphene-based field effect transistors.

Virginia Polytechnic Institute and State University, R. L. Mahajan, Laser treatments of CNT materials.

Yale University, Prof. M. A. Reed, Robust molecular electronic test structures.

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Xiaoxiao Zhu, D. Gu, Qiliang Li, D. E. Ioannoua, H. Baumgart, J. S. Suehle, C. A. Richter, *"Silicon Nanowire NVM with High-k Gate Dielectric Stack,"* Microelectronic Engineering 86 1957-1960 (2009) [JUL 2009].

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Power Semiconductor Device Metrology

Technical Contacts:
A. Hefner

Goals

The goal of the project is to develop electrical and thermal measurement methods, measurement equipment, and theoretical models in support of the development and application of advanced power semiconductor devices.

Customer Needs

There are significant technical requirements for more efficient, higher voltage power semiconductor devices. The application needs range from more efficient power supplies for computers and consumer appliances, to electric automobile power converters, to more efficient power generation, transmission and distribution. Rapid technical advances are occurring in the development of new power semiconductor materials, fabrication processes, and device designs to address these needs. With the introduction of these new materials and designs come new requirements for characterizing the performance and reliability of the fabricated devices.

The most exciting, and potentially revolutionary, development in this area is the rapid progress in the development of wide band-gap semiconductor materials for power semiconductor devices. Wide band-gap semiconductors such as silicon-carbide (SiC) have long been envisioned as the material of choice for next-generation power devices. Recent advances in single crystal SiC material and fabrication technology have ushered in a new era of wide band-gap power semiconductor devices. This has led to the commercialization of SiC power Schottky diode products in the 400 V to 1200 V range and to the development of High-Voltage, High-Frequency (HV-HF) power devices with 10 kV, 20 kHz power switching capability. The emergence of HV-HF devices with such capability is expected to revolutionize industry and military power generation, transmission, and distribution by extending the use of switch-mode power conversion technology, with its superior efficiency and control capability, to high voltage applications.

(Sidebar quotation) *"In 2002, Dr. Calvin Carter of Cree Inc. received the US National Medal of Technology from President George W. Bush for: "his exceptional contributions to the development of Silicon Carbide wafers, leading to new industries in wide band-gap semiconductors and enabling other new industries in ... more efficient/compact power supplies, and higher efficiency power distribution/transmission systems."*

Several industry and government programs are currently under way to accelerate the development and application insertion of SiC power semiconductor devices. The goal of the DARPA Wide-Band-gap Semiconductor Technology High Power Electronics Program (WBST-HPE) is to develop half-bridge power semiconductor modules with 15 kV, 110 A, 20 kHz switching capability. The recently awarded WBST-HPE Phase 3 effort is using this semiconductor technology to enable the HV-HF switching required for a Solid State Power Substation (SSPS). The Electric Power Research Institute (EPRI) also identified the benefits of HV-HF semiconductor technology, which includes advanced distribution automation using solid-state distribution transformers with significant new functional capabilities and power quality enhancements, and the Department of Energy has identified HV-HF power devices as an enabling technology for alternative/clean energy sources and energy storage systems, as well as transmission and distribution systems.

Technical Strategy

The strategy of the NIST project is to support the measurement infrastructure of the power semiconductor and energy systems technology industries by developing and evaluating measurement methods and techniques where suitable ones do not exist for characterizing critical electrical and thermal properties of power semiconductor devices. This includes electrical, thermal, and safe operating limit characterization, establishing performance metrics, and developing methods for extracting device model parameters. The NIST project also establishes the theoretical foundation required for development of advanced power semiconductor devices, and develops circuit simulation models for emerging power semiconductor devices to aid in the rapid adoption and effective utilization of new technologies. NIST is taking a lead role in developing the device metrology and performance metrics necessary for industry and government HV-HF semiconductor device development efforts and in the evaluation of potential future impacts of power semiconductor technologies requiring future investment.

Metrology for High-Voltage High-Frequency Switching Devices

The emergence of HV-HF power devices presents unique challenges in metrology and specification of device electrical and thermal requirements. NIST has recently developed unique world-class laboratory facilities for characterization of HV-HF SiC power switching devices including: a) 25 kV variable-pulse-width curve tracer, b) 15 kV 100 A 50 ns inductive and resistive load switching tester, c) 4 kV, 50 A, 10 ns diode reverse recovery tester, d) pulsed and multi-channel long term diode forward current stress and monitoring systems, e) high-speed high-power Temperature Sensitive Parameter module package measurement system, and f) rapid thermal cycling/shock module package stress system. As HV-HF semiconductor devices and modules continue to advance, NIST develops and transfers to industry new measurement methods and procedures to characterize application performance.

DELIVERABLES:

- Develop low-parasitic-capacitance inductors and a double-pulse gate drive circuit needed for performing inductive turn-on and turn-off switching for 50-100 A, 10 kV SiC power MOSFET modules with 50 ns switching time. 2Q2009
- Develop High-Voltage CV Measurement System including high-voltage safety interlock system and operator status light warning system with the capability to characterize capacitance of 100 A, 10 kV half-bridge SiC MOSFET/JBS modules. 3Q2009
- Transfer HV-HF test systems and characterization procedures to other members of the DARPA WBST-HPE technical team including Cree, GE, and Powerex. 4Q2010

Support Programs to Develop and Apply HV-HF Semiconductor Devices

A major driving force spearheading the development of HV-HF power devices is the ongoing DARPA WBST-HPE program focused on developing the technology deemed necessary to enable SSPSs for future Navy warships. Conventional distribution approaches being considered for the next generation of aircraft carriers employ a 13.8 kV AC power distribution that is stepped down to 465 V AC by using large (6 ton and 10 m3) 2.7 MW transformers. Substantial benefits in power quality enhancement, advanced functionality, size, and weight are anticipated by replacing this transformer with an all solid state design. NIST played a key role in WBST-HPE Phase 1 and has been selected to be the exclusive device and package evaluation and metrology laboratory for the Phase 2 and 3 programs for 2005 through 2010.

The Obama Administration has established alternate/clean energy sources and the Smart Grid as national priorities. NIST and DOE recently initiated an Industry Roadmap Committee for High-Megawatt Power Conditioning Systems (PCS) and reestablished the Interagency Advanced Power Group's Electrical Systems Working Group to provide industry and federal guidance in identifying power electronics technologies requiring development for these future energy systems. NIST/DOE programs have also recently been established to determine advanced power electronic component technologies needed for 300 MW Power Conditioning Systems (PCS) to enable future Near Zero Emission (including CO2) Fuel Cell Based Power Plants fueled with coal-derived gas. Extremely large PCSs will be required to convert the 700 V, 1000 A DC power output of one thousand fuel cell modules to the 345 kV AC power transmission level. Large PCS systems (>30 MW) will also be required for electric drive motors used to compress CO_2 for pipeline transportation and sequestration applications.

DELIVERABLES:

- Lead an interagency scoping study to identify SiC power semiconductor technologies requiring investment for high-megawatt applications. 4Q2010
- Provide leadership to the Industry Roadmap Committee for High-Megawatt Power Conditioning Systems and serve as Chairman of the Interagency Advanced Power Group to aid in Smart Grid deployment of renewable energy sources. 2Q2011

Characterize Electrical Performance of DARPA HPE Device Deliverables

NIST continues to serve as the exclusive device and package deliverable evaluation lab for the DARPA WBST-HPE Phase 3 program providing data and analysis critically important to evaluate contractors and plan future programs. NIST evaluates device performance and provides feedback to the contractors and DARPA program manager as well as the potential component users in government and industry. NIST characterization data and analysis has continually identified critical technology advancements required to meet DARPA program goals such as recommendations to improve surface passivation, reducing

internal gate resistance, improving p-i-n power diode (diode made with p-type to intrinsic to n-type semiconductor junctions) speed, transitioning program goal from p-i-n to Schottky diodes, inclusion of a low voltage series blocking diode to prevent reverse conduction in the high-voltage SiC MOSFET, and specific design parameter targets for MOSFET and IGBT (insulated gate bipolar transistor) designs. The NIST HV-HF characterization results are routinely used by DARPA in planning documents and by the device developers in publications.

DELIVERABLES:

- Characterize DARPA WBST-HPE Phase 3 power module deliverables including measurement of drain and gate leakage, output and forward conduction, reverse recovery, switching, CV, and model parameter extraction. 4Q2010

SiC Power Device Models for Power Converter Simulation

Accurate and robust circuit simulator models for SiC semiconductor devices are needed to evaluate the impact of the new semiconductor technology on power converter system performance. NIST develops the generic physics-based models for the SiC power semiconductor devices that are provided in commercial circuit and system simulation software. In addition, NIST also develops model parameter extraction methods needed to measure the physical and structural parameters of specific devices. The NIST model parameter extraction tools are used to characterize SiC power MOSFETs and diodes introduced by the DARPA WBST-HPE Phase 2 and 3 programs. These models are used as virtual prototypes to optimize module design and to simulate the performance of the modules within the SSPS enabling concurrent system design and enabling the evaluation of module stress for system fault conditions. NIST also develops models for semiconductor devices and custom packages used for advanced plug-in vehicle power converters being developed by industry and DOE vehicle technology programs.

DELIVERABLES:

- Develop electro-thermal module model for ultra-high efficient inverter module to be used in hybrid vehicle soft switching inverter and perform parameter extraction and model validation for the devices and package elements of the modules. 4Q2009
- Complete development of unified DIode Model Parameter extrACtion Tool (DIMPACT) and apply the tool to model and evaluate suitable diodes for the hybrid vehicle soft switching inverter being developed for the FreedomCar program and the HPE program. 3Q2009
- Apply NIST developed n-channel SiC IGBT model and parameter extraction procedure to evaluate research device samples. 2Q2011

Metrology for SiC Device Degradation and Reliability

Although significant progress has been made in improving the quality of the SiC starting material and fabricated devices, a major concern for devices with minority carrier injection is the degradation in the electrical characteristics after prolonged forward bias conduction. The degradation occurs from latent material defects such as Basal Plane Dislocations (BPDs) that result in the formation and growth of stacking faults activated by excess-carrier recombination. NIST develops automated stress and degradation monitoring systems to assess degradation of SiC devices. The monitoring methods include forward conduction voltage drop, switching reverse recovery characteristics, and pulsed thermal imaging of current uniformity.

Other major safe operating area (SOA) and reliability concerns for HV-HF devices include stability of devices under long term high-temperature reverse bias, long term impact of high dv/dt plus high voltage on package and insulator materials, and dynamic impact ionization and current constriction under switching events. NIST develops unique test systems and procedures to address HV-HF semiconductor device and module robustness and applies these procedures to evaluate vulnerability of the devices for stress produced during system fault conditions.

DELIVERABLES:

- Develop high-voltage, high frequency dielectric leakage test system including high-voltage safety interlocks and operator status light warning system. 2Q2009
- Develop forward bias stress and degradation monitoring systems for 100 A, 10 kV SiC power modules including High Temperature Operating Lifetime (HTOL) and High Temperature Gate Bias (HTGB). 3Q2010

Accomplishments

■ The NIST model parameter extraction tools have recently been used to characterize SiC power MOSFETs and diodes introduced by the DARPA WBST-HPE Phase 2 and 3 programs. These models were used as a virtual prototype to perform simulations of a 2.7 MW SSPS by

the DARPA/ONR/Navsea WBST-HPE Government Independent Panel providing the basis for the HPE Phase 3 Broad Area Announcement. The models are also used by the DARPA HPE Phase 3 contractors to optimize the module electrical and thermal performance, and to simulate the electrical and thermal stress on the modules during system fault conditions. The models are also being used as part of the NIST/DOE advanced High Megawatt PCS technology evaluation and for use in the plug-in electric vehicle power train and bidirectional vehicle-to-grid power converters.

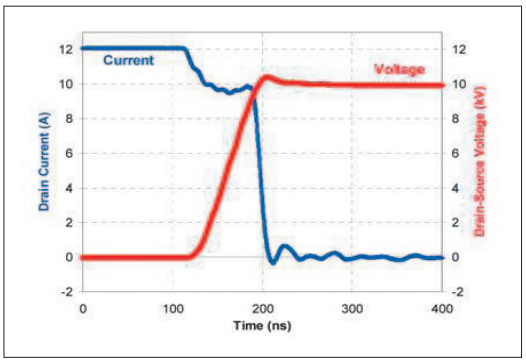

Figure 1. NIST measurement of the unprecedented performance of the SiC power MOSFETs switching at 10 kV, 12 A and 200 ¡C in less than 75 ns.

■ NIST played a key role in planning and coordinating activities of the DARPA HPE program on high voltage SiC power devices including: Evaluated contractor performance for DARPA WBST-HPE Phase 2. Participated in planning and writing Broad Area Announcement (BAA) for DARPA WBST- HPE Phase-3 programs and presented status of SiC power devices at the Phase 3 Industry Bidder Briefing day. Also presented the status of the DARPA HPE program at GomacTech in 2005, 2006, 2007, and 2008 and presented the status of HV-HF semiconductor devices at the IEEE Industry Applications Society Meeting (this paper received the 2006 William M. Portnoy Award). Served as Member of DARPA/ONR Solid State Power Substation (SSPS) Government Independent Design Panel. Participated in planning ONR Mantech SiC Power Device Manufacturability Program.

■ NIST is leading industry and other Federal Agencies in coordinating activities in High Megawatt Power Conditioning Systems. NIST in collaboration with DOE, EPRI, and the Army Corp of Engineers planned and held the following workshops that were held at NIST:

• The first workshop, entitled High Megawatt Converter Workshop was held at NIST on January 24, 2007. During the workshop, the participants of the workshop agreed that a federal interagency task group for high-megawatt power converter technologies could play an important role in this area and that an industry roadmap process should be initiated.

• The second workshop, entitled High-Megawatt Converter Technology R&D Roadmap Workshop, was held on April 8, 2008. This workshop resulted in the formation of a committee to develop a roadmap for the R&D necessary to support development of low-cost, high-megawatt PCSs needed for alternate/clean energy sources and the power grid.

• The third workshop, entitled NSF Workshop on Advanced Power Conditioning for Alternate Energy Systems, was held on May 28-29, 2008. It brought together academic leaders in alternate energy, the power grid and advanced power conditioning technology and resulted in the development of priorities for future NSF sponsored research.

• The fourth workshop entitled Workshop on Future Large CO_2 Compression Systems was held at NIST on March 30-31, 2009. This was the first workshop to address the advanced compression machinery, electric motors, and motor drive electronics technologies required for future large (> 30 MW) CO_2 compression systems.

■ NIST played a key role in reinitiating the Interagency Advanced Power Group (IAPG) Electrical Systems Working Group (ESWG) to coordinate federal programs in high-megawatt PCS technology, and held 6 meetings in 2008 -2009 including the meeting held at NIST on April 21-25, 2008.

■ High voltage clamped inductive and resistive switching test bed developed. A low parasitic inductance 15 kV switching test system for clamped inductive and resistive SiC MOSFET switching characterization was developed and integrated into the 25 kV safety-interlocked curve-tracer system. A low parasitic capacitance temperature-controlled test fixture with 20 kV voltage isolation and 350 °C maximum controllable temperature was also included to enable

investigation of HV-HF device characteristics at elevated operating temperature. The hardware is controlled by the NIST virtual curve-tracer instrumentation software.

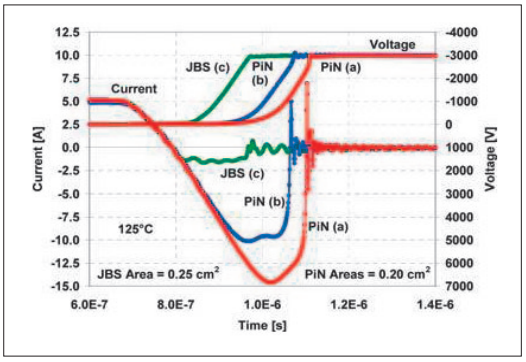

Figure 2. Comparison of reverse recovery time for two different 10 kV SiC PiN diodes, (a) and (b), and a 10 kV JBS SiC diode (c), all at 125 ¡C.

■ NIST unique HV-HF device metrology demonstrated unprecedented performance of DARPA WBST-HPE: The NIST high voltage curve tracer and the NIST high-voltage high-frequency (HV-HF) switching test systems were used to demonstrate the unprecedented performance of DARPA WBST-HPE MOSFETs, e.g., 10 kV, 12 A, 50 ns inductive load switching shown in Fig. 1. Typical high voltage silicon devices require several microseconds to switch at 6.5 kV maximum. Significant advances in materials, device design and HV-HF metrology were required for this achievement.

■ NIST contributed to device design required to improve 10 kV SiC rectifier reverse recovery speed: NIST provided guidance on techniques for improving the reverse recovery time (switching speed) of 10 kV SiC rectifiers developed by the HPE program. The guidance included structure changes to control the plasma distribution during reverse recovery in PiN diodes as well as the recommendation that the program be refocused toward Junction Barrier Schottky (JBS) diodes. NIST characterized the reverse recovery performance of the various diode designs that were produced using the NIST 4 kV, 50 A, 10 ns diode reverse recovery tester. Results indicate that the reverse recovery charge (area under the negative portion of the current waveform shown in Fig. 2 is reduced using plasma engineering but only the JBS diode is capable of 20 kHz operation.

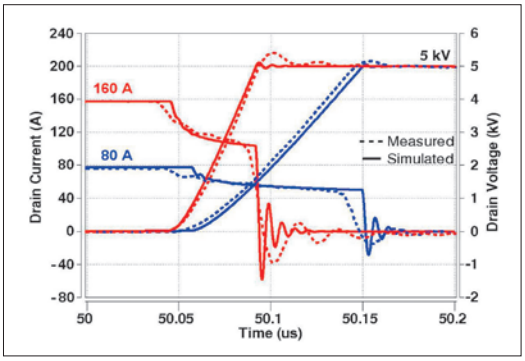

Figure 3. Comparison of scaled measured (dashed) and simulated (solid) inductive-load switching turn-off waveforms for a 100 A, 10 kV SiC MOSFET. Both tests were performed at 25 ¡C with a clamp voltage of 5 kV and drain currents of 80 A (blue) and 160 A (red), respectively

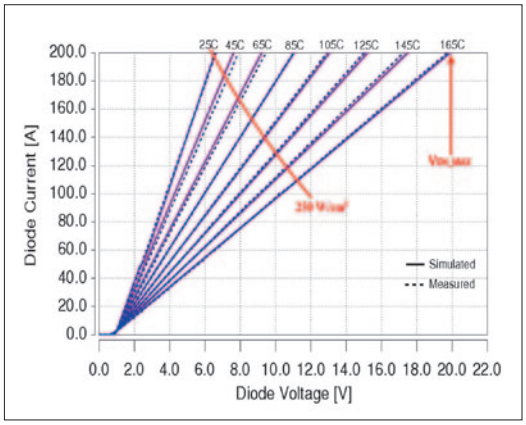

Figure 4. Comparison of scaled measured (dashed) and simulated (solid) forward conduction characteristics at 25 ¡C, 45 ¡C, 65 ¡C, 85 ¡C, 105 ¡C, 125 ¡C, 145¡C, and 165 ¡C for a 100 A, 10 kV SiC junction barrier Schottky (JBS) diode.

■ NIST HV-HF SiC models were used to simulate system performance: NIST's metrology, device modeling, and parameter extraction tools have resulted in software models for the HV-HF devices that are being produced by the DARPA WBST-HPE program. These models are being used by industry and government to simulate the performance of future power distribution and conversion systems enabled by the new HV-HF semiconductor device technology. Fig. 3, Fig. 4, and Fig. 5 show the comparison of the model with measured results. These models were used to optimize the 100 A, 10 kV half bridge power module and to design the SSPS HPE Phase 3 and are being used to simulate various PCS architectures to help identify technologies that need to be developed to reduce the cost of future PCS systems for alternate/clean energy systems.

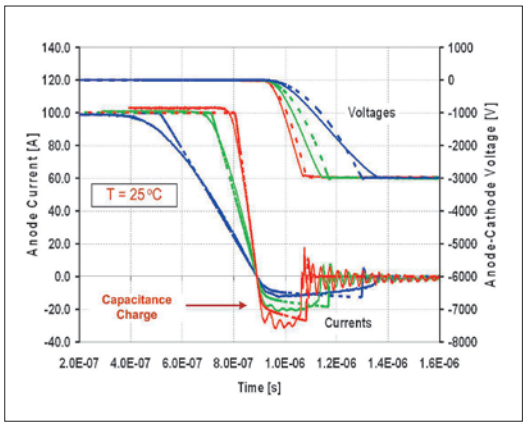

Figure 5. Comparison of scaled measured (solid) and simulated (dashed) reverse recovery at 25 ¡C for a 100 A, 10 kV SiC JBS diode.

■ Extended capabilities of IMPACT parameter extraction software. The capabilities of the parameter extraction software, IMPACT, were extended to include MOSFETS (in addition to IGBTs) and three prototypes of SiC material (in addition to Si). The parameter extraction hardware was also extended to enable capacitance versus gate- and drain-voltage characterization up to 5 kV.

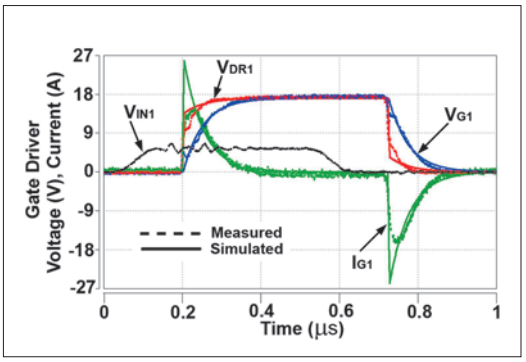

Figure 6. Gate driver current and voltage simulated (solid) and measured (dashed) waveforms.

■ Demonstrated a HV-HF isolated gate drive circuit for 10 kV, 100 A SiC MOSFET/JBS power modules for the first time. The new high-voltage isolated gate drive circuit for characterization of high-voltage, high-frequency 10kV, 100A SiC MOSFET/JBS half-bridge power modules to be used in the SSPS has been developed. This new gate driver has many features that include 30 kV voltage-isolation required for use as a high-side MOSFET driver in a 13.8 kV AC stacked converter configuration. The gate drive circuit enables gate resistance of less than 0.5 Ω required to achieve 100 ns switching for the modules as shown in Fig. 6. The gate drive circuit has less than 5 pF common mode capacitance enabling it to be used as a high side gate driver for a 5 kV in 50 ns switch without excessive common mode current (conducted EMI).

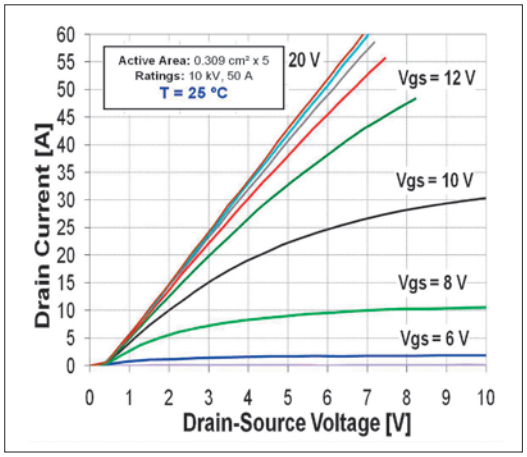

Figure 7. Measured output characteristics at 25 ¡C for a 10 kV, 50 A SiC MOSFET

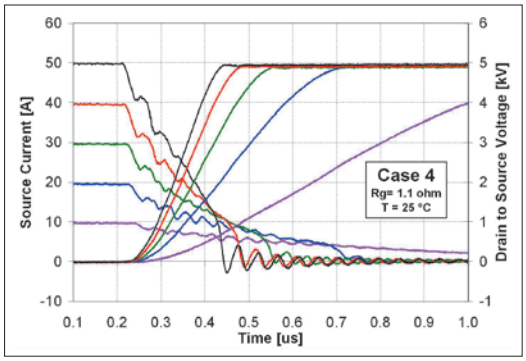

Figure 8. Measured inductive-load switching turn-off switching waveforms at 25 ¡C for a 10 kV, 50 A SiC MOSFET.

■ Characterized static and dynamic performance of the first 50 A, 10 kV SiC MOSFET/JBS power module ever made. Fig. 7 shows the measured 10 kV, 50 A SiC MOSFET output characteristics at 25 °C, and Fig. 8 shows the inductive-load switching turn-off waveforms for the 10 kV, 50 A SiC MOSFET in the power module.

■ Developed physics-based, transient, electro-thermal simulation capability for high-voltage, high-current SiC bipolar power devices. A Physics-based TCAD simulations capability has been developed by NIST for high-voltage, high-

current SiC power semiconductor devices. This capability has been applied to the electro-thermal study of SiC power thyristors operating under high-current, pulsed-power conditions as shown in Fig. 9. The use of electro-thermal, physics-based device and circuit modeling is fundamental in the study of the operating limits of SiC power devices.

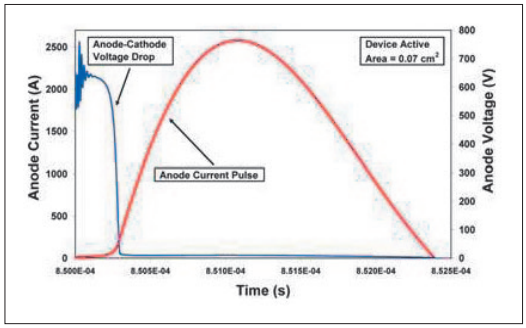

Figure 9. SiC thryristor anode voltage and anode current pulsed-power waveforms.

Collaborations

Synopsys Inc., SiC power device modeling and parameter extraction for IGBT library component models.

CREE, Characterization and application of SiC power devices. Northrop Grumman Corp., Characterization and application of SiC power devices. Virginia Tech., Silicon and SiC power device utilization. Powerex, Power semiconductor device packaging.

DARPA/ONR/Navsea, SiC power devices for SSPS and other applications.

GE CRD, SiC power devices for robust integrated power electronic systems.

University of Puerto Rico Mayagüez, Electro-thermal simulation of power electronic systems.

University of Wisconsin Madison, SiC power system simulation.

Purdue University/Carnegie Mellon University/Vanderbilt University/Auburn University, Development of process technologies for SiC power devices Electric Power Research Institute, power semiconductor devices for solid state intelligent universal transformer.

Department of Energy, electric vehicle power electronics and power converters for 300 MW fuel cell generation plant.

Stanford University, numerical simulation of SiC power semiconductor devices. Army Research lab, Pulsed power semiconductor devices.

Publications

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Organic Electronics and Photovolatics Metrology

Technical Contacts:
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Goals

Organic electronic devices are increasingly incorporated into commercial prototypes and are projected to revolutionize integrated circuits through new applications that take advantage of low-cost, high-volume manufacturing, nontraditional substrates, and designed functionality. A critical need has emerged for new diagnostic probes, tools, and methods to address new technological challenges. Organic electronics adoption will be advanced considerably by the development of an integrated and interdisciplinary suite of measurement methods to correlate device performance with the structure, properties, and chemistry of critical materials and interfaces. NIST will guide the development of standard test methods and provide the fundamental measurements needed for the rational and directed development of materials and processes to realize the potential of organic electronics and photovoltaics.

Customer Needs

An exciting array of new devices and applications are now possible with the development of electronic devices using organic materials because they are amenable to low-cost, high volume manufacturing, incorporation on flexible substrates, and designed functionality. Completely new technologies are under development including printable large-area displays, wearable electronics, paper-like electronic newspapers, ubiquitous integrated sensors, and radio-frequency identification tags. Market estimates range from $10 billion to $30 billion (B) globally by 2010 to 2015, with applications in displays, logic, and lighting. Organic light emitting diodes for displays and lighting form the first generation of products, projected to grow from approximately $0.5 B today to $3 B in 2010. Market expansions to $250 B by 2025 have been estimated should major technology and business barriers be overcome. An emerging application for organic electronics is in low-cost photovoltaic cells, which have the potential to significantly reduce the costs of solar cell manufacturing. At this stage, new materials and processes are evolving rapidly to optimize device performance, ease processing limitations, and demonstrate frontier applications. However, systematic progress in organic electronics and photovoltaics is challenging because of the enormous range of potential materials (from polymers to nanocomposites) and manufacturing methods (roll-to-roll printing, fluidic self-assembly, micro-contact printing, laser ablative printing, and ink-jet printing).

A key technical barrier is the lack of correlation between device performance and the structure, properties, and chemistry of critical materials in the bulk and at interfaces. Without this knowledge, guided improvements in materials, processing, and device design are not possible and meaningful standard test protocols cannot be developed. Characterizing the chemically complex (mostly carbon-based) soft interfaces in organic devices is critical to proper interpretation of carrier transport behavior. Identifying and controlling specific contributions to performance variation requires metrology unavailable to device manufacturers and spanning multiple disciplines that include device physics, chemistry, and materials science

Technical Strategy

The NIST program focuses on the organic field effect transistor (OFET) and the bulk heterojunction organic photovoltaic (OPV) device as model systems. The OFET is the basic building block of circuitry, and the characteristics and issues that arise during OFET development are transferable to other organic electronic devices because performance is also dominated by molecular design, microstructure, chemistry, and resulting electronic structure in the bulk and at critical device interfaces. The OPV device is significantly different than the OFET because its active layer is a blend with a complex nanoscale structure. NIST is engaged in complementary activities to address the primary technical barriers facing the adoption of organic electronics and photovoltaics: unique measurements of organic materials and interfaces for both structure and chemistry and electronic properties; and the development of an integrated measurement test platform to correlate device performance with the processing conditions, microstructure, and primary chemical structure of organic semiconductors.

1. Correlating structure to performance for OFETs: The basic OFET consists of thin layers (20 nm to 50 nm thick) of disparate materials including the organic semiconductor, dielectric,

electrode, and substrate. OFET performance and operational stability critically depend upon charge transport and material interactions between inorganic and organic materials, particularly at semiconductor/dielectric and semiconductor/metal interfaces. Detailed interfacial structure information (electronic structure, molecular orientation, interfacial roughness, interfacial chemistry), correlated with electronic properties is required to predict performance. Correlation development is organized by the paradigm shown in Figure 1, where the microstructure and electronic consequences of variations in chemical structure and processing are precisely measured, and then fed back to our customers to inform further development.

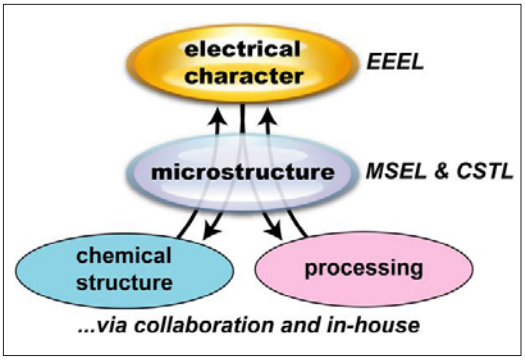

Figure 1. Project paradigm

We are developing a suite of powerful measurement methods including X-ray, neutron, optical probes, and electrical tests to characterize critical organic interfaces. Changes in interfacial structure, chemistry, and orientation are correlated with OFET electrical performance. Near-edge X-Ray Absorption Fine Structure (NEXAFS) spectroscopy and nonlinear optical techniques are ideally suited for nondestructive characterization of organic interfaces for chemistry, orientation, and structure. NEXAFS can distinguish chemical bonding in the light elements and measure the orientation of interfacial molecules. Spectroscopic ellipsometry (SE) is a powerful tool to study the electronic state of molecules and evaluate how the transition dipoles of electronic excitations are oriented with respect to film geometry. Polarized infrared absorption (IR) spectroscopy provides both configuration and orientation information for many chemical moieties common to organic electronics materials. Specular and grazing X-ray diffraction (XRD) measurements measure long range positional order to describe unit cell configuration and domain size information. Scanning probe techniques such as atomic force microscopy provide surface morphology information to assess domain shape, size, and spacings. Microscopy techniques such as transmission electron microscopy (TEM) can be used to evaluate the nanoscale organization of crystalline domains in a semiconductor layer. Finally, small-signal capacitance-voltage analysis of the contact and channel properties of OFETs provides unprecedented insight to the electronic structure, charge trapping, and transport at the semiconductor-gate dielectric interface, and is complimentary to DC electrical measurements which are widely used to evaluate material and device performance.

DELIVERABLES:

- Initiate activity examining consequences of mechanical strain (flexure) on organic semiconductor structure and electrical function. 2Q 2009
- Complete structural and electrical measurements of small molecule semiconductors with microstructure that is strongly influenced by electrode chemistry. 3Q 2009
- Complete correlation between TEM images of domain structure and activated transport behavior in films of liquid crystalline poly(thiophene). 3Q 2009
- Complete detailed structure measurements of printed liquid crystalline poly(thiophene) OFETs. 4Q 2009

2. Correlating structure to performance for OPV devices: One of the most ubiquitous types of OPV device has an active layer that is a blend of an absorbing material and an electron acceptor. The chemical potential offset between the two materials must be sufficient to drive exciton dissociation at the absorber / acceptor interface. The exciton diffusion length is typically quite short in organic absorbers, so excitons can only be harvested if they are formed within ≈ 10 nm of an interface. Since the light path must be at least 100 nm for reasonable absorption of solar radiation, these characteristics necessitate a finely divided architecture where small domains (≈ 10 nm) are distributed through a thick film (100 to 300 nm), typically called a bulk heterojuction (BHJ). Controlling the morphology of a BHJ film is a critical technology barrier to the introduction of new materials for OPV devices.

We are developing methods for performing structure measurements of BHJ films for OPV devices. NEXAFS, SE, and neutron reflectivity will evaluate the vertical distribution of the two phases and identify which components are in contact with the cathode and anode. XRD will

measure the crystalline orientation of the polymer absorber, which affects both its absorbance and the anisotropy of its hole mobility. Morphology characterization measurements such as small angle scattering and TEM will be used to study the three-dimensional architecture of the BHJ film. Transistor measurements will be used to evaluate the transport that occurs in the interfacial layers of the BHJ film. These results will be correlated to calibrated measurements of OPV device efficiency. These measurements will be combined to determine how the chemical nature of the BHJ components, and how they are processed, affect OPV device performance.

DELIVERABLES:

- Determine how dielectric surface energy affects interface segregation in BHJ films, and correlate to OFET transport characteristics. 2Q 2009
- Determine how the surface energy of the hole transport layer affects segregation in BHJ films, and correlate to OPV device characteristics. 3Q 2009
- Initiate activity examining the consequences of BHJ aging on its chemistry and morphology, and the OPV device performance. 4Q 2009.

Accomplishments

A strategy was developed to successfully determine the molecular mechanism of performance enhancement in the thermal annealing of the currently highest-performing polymer semiconductor, poly (2,5-bis(3-tetradecylthiophene-2-yl) thieno[3,2-b]thiophene) (pBTTT-C14), in collaboration with Merck Chemicals. Microstructure development throughout a heating cycle was characterized in-situ by specular XRD to follow changes in the film order perpendicular to the substrate, while a combination of in-situ polarized absorption spectroscopies (IR, visible, and X-ray) were applied to determine changes in the configurations and orientations of the side chains and conjugated backbone. This combined approach allowed characterization of virtually all aspects of film structure as they change with temperature. We found that the overall layer structure dramatically improved upon entering the mesophase at ≈ 140 °C. Surprisingly, high levels of backbone order, p-stacking, and field effect mobility were maintained throughout the transition. The polarized IR measurement revealed that the molecular mechanism of the performance enhancement was the melting of the alkane side chains, which must be completed before the layers can reorganize. This requirement is consistent with the significant level of side chain interdigitation in the crystalline phase. Crystalline and interdigitated side chains can be regarded as rigid links extending vertically that constrain the lateral motions of backbones and packed backbone layers. Only when the side chains are completely melted can the backbones freely move, to eliminate packing defects in a smectic-like liquid crystalline state. Upon cooling, the side chains recrystallize to capture and maintain the high level of layer order/alignment achieved in the mesophase (Fig 2). Side chain interdigitation therefore provides a general mechanism to achieve and then preserve layer order, because it both allows "repairs" to defective or small crystals that form during solidification from solution and then "locks in" the order. Further advances in polymer semiconductor synthesis must consider the interplay among 1) the backbone / side chain interactions driving layer order, 2) side chain crystallinity and interdigitation (influenced by attachment density and possibly attachment point) that provide a mechanism for three-dimensional crystallization, and 3) the mesophase and its smetic-like structure that permits lateral domain growth.

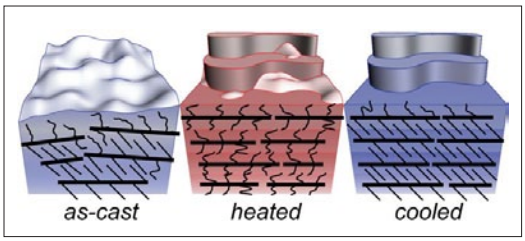

Figure 2. pBTTT annealing mechanism

Initial work in OPV was completed with a study of interface composition in BHJ films composed of regioregular poly(3-hexylthiophene) (P3HT) and phenyl-[6,6]-C60 butyric acid methyl ester (PCBM). A series of model substrate with varying surface energy were used to cast a 1:1 blend of P3HT and PCBM. The interfacial segregation of the P3HT:PCBM blend was studied using NEXAFS spectroscopy to identify interfacial composition. The bottom interfaces were examined by a delamination technique; the high sensitivity of NEXAFS spectroscopy to organic contamination allowed us to verify successful delamination. We found that the bottom interface composition of P3HT:PCBM is strongly affected by the substrate surface energy upon which the film is cast. On low surface energy substrates, the bottom interface is P3HT-rich, whereas on high surface energy substrates, the bottom interface is

PCBM-rich (see Fig 3). The top (air) interface was P3HT-rich in all cases. These results can be rationalized using a simple segregation model for miscible polymer blends, where the differences in surface energies between the blend components control the segregation behavior. The interface composition results were compared to OFET measurements of the BHJ, where the model surfaces were used as dielectric preparations. On the high surface energy dielectric, P3HT:PCBM exhibited ambipolar transport consistent with that of PCBM. On the low surface energy dielectric, P3HT:PCBM exhibited hole-transport consistent with that of P3HT. These results show that, while OFETs are a valuable probe of charge transport, they are unlikely to provide useful information about bulk transport, because the composition of the accumulation layer depends on the substrate (e.g. dielectric) chemistry and does not reliably reflect the BHJ interior. These results also have important implications for OPV device design because they indicate that the BHJ interface composition in conventional geometries is reversed from the ideal phases that should contact the

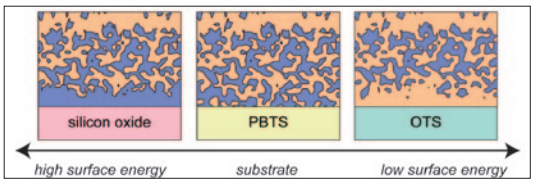

Figure 3. The vertical domain distribution of P3HT (orange) and PCBM (blue).

cathode and anode (e.g., the BHJ self-organizes "upside down"). Further, any materials modifications targeting injection barriers via work function engineering may have the unintended consequence of altering the BHJ interface composition.

Collaborations

Polymers Division, MSEL –David Germack, Chad Snyder, Steve Hudson, Joseph Kline.

Semiconductor Electronics Division, EEEL – Curt Richter, Oleg Kirillov, Oana Jurchescu, Calvin Chan.

Ceramics Division, MSEL – Daniel A. Fischer.

Surface and Microanalysis Science Division, CSTL – James Kushmerick Plextronics – Darrin Laird, Sergey Li Imperial College - Iain McCulloch, Martin Heeney, Natalie Stingelin, Thomas Anthopolous.

Stanford Synchrotron Radiation Laboratory – Michael Toney.

Corning – Sue Gasper, He Mingqian.

University of Kentucky – John Anthony.

Penn State University – Tom Jackson.

Publications

Germack, et al., "*Substrate-dependent interface composition and charge transport in films for organic photovoltaics"* Applied Physics Letters (2009) in press.

McCulloch, et al., *"Semiconducting Thienothiophene Copolymers: Design, Synthesis, Morphology and Performance in Thin Film Organic Transistors,"* Advanced Materials 21 (2009) 1091-1109.

DeLongchamp, et al., *"Controlling the Orientation of Terraced Nanoscale "Ribbons" of a Poly(thiophene) Semiconductor"* ACS Nano 3 (2009) 780-787.

Teague, et al., *"Surface Potential Imaging of Solution Processable Acene-Based Thin Film Transistors,"* Advanced Materials 20 (2008) 4513-4516.

Jurchescu, et al., *"Organic Single Crystal Field-effect Transistors of a Soluble Anthradithiophene,"* Chemistry of Materials 20 (2008) 6733–6737.

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Park, et al., *"Structural characterization of conjugated polyelectrolyte electron transport layers by NEXAFS spectroscopy"* Advanced Materials 20 (2008) 2491.

Delongchamp, et al., *"The Molecular Basis of Mesophase Ordering in High Performance Semiconducting Polymers,"* Macromolecules 41 (2008) 5709-5715.

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Hamadani et al. *"Insights into the characterization of polymer-based organic TFTs using C-V analysis,"* Applied Physics Letters 92 (2008) 203303.

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Gundlach et al. *"Contact-induced crystallinity for high-performance soluble acene-based transistors and circuits,"* Nature Materials 7 (2008) 216-221.

Jung et al. *"The Effect of Interfacial Roughness on the Thin Film Morphology and Charge Transport of High-Performance Polythiophenes,"* Advanced Functional Materials 18 (2008) 742-750.

Micro- and Nano-Electro-Mechanical Technology Metrology

Goals

The objective of this project is the development of test structures, test methodologies, and standard reference materials (SRMs) for the characterization of Micro-Electro-Mechanical Systems (MEMS) and Nano-Electro-Mechanical Systems (NEMS) fabrication processes. Since these two technologies differ primarily by scale, they are often referred to as Micro-Nano Technology (MNT). Full characterization of an MNT process requires accurate measurement of a large set of material properties, including: Young's modulus, residual stress, thermal coefficients, surface roughness, density, and Poisson's ratio. In addition, process, device, and packaging parameters must be accurately determined. These parameters include as-fabricated dimensions and wafer bond strength. Ideally these measurements would be quickly performed in the manufacturing line, with large enough sample size to allow characterization of process variation.

Customer Needs

To choose high-impact areas for project resources, customer needs are determined using multiple venues including external conference and workshop attendance and leadership, organizing NIST workshops, and participation in SEMI and ASTM standards organizations.

Members of this team organized a NIST workshop on Microrobotics in June 2008, were on the organizing committee for the SEMI International MEMS Workshop in July 2008, and served as Technical Chair of the 2009 IEEE International Conference on Microelectronic Test Structures. In addition, they have participated in SEMI and ASTM standards development activities and attended numerous conferences and workshops – including METRIC 2009, PRIME 2008, and the 2008 Solid-State Sensors, Actuators, and Microsystems Workshop – which have emphasis on MNT-related technologies.

As part of a broader NIST initiative to determine the metrology needs of U.S. companies, two NIST U.S. Measurement System (USMS) workshops were held in 2005 and 2006 relating to MNT metrology. The first USMS Workshop was held in Pittsburgh, PA on September 22, 2005, immediately after the Metric 2005 Conference. Representatives from a number of companies with interest in MNT technologies attended and were asked to help define and prioritize the metrological needs of the MNT community. From the gathered workshop inputs and subsequent discussions approximately seven measurement needs (MNs) were crafted. One need of particular interest to this project concerns material property measurements for "fabless" MEMS. The concept of fabless MEMS is one in which a company can produce devices via a foundry rather than their own, expensive (over $100 million), fabrication facility. This is similar to the IC foundry model, which has been successfully implemented in the semiconductor industry. A report describing the outputs of this USMS Workshop was published in the MEMS Industry Group (MIG) 5-year anniversary report.

The second USMS Workshop was held on March 15, 2006, during Pittcon, in Orlando, Florida. This meeting was targeted at metrology needs for microfluidics applications. Representatives from seven companies presented their metrology needs in this rapidly growing field. During this meeting, a need for dimensional metrology was stated. Many of the proposed microfluidic applications depend upon accurately knowing the dimensions of the measurement device.

Technical Strategy

Overview: The MNT standardization efforts in SEMI's North American MEMS Standards Committee include the following:

- SEMI MS1-0307 on wafer-to-wafer bonding alignment targets,
- SEMI MS2-0307 on step height measurements,
- SEMI MS3-0307 on MEMS terminology,
- SEMI MS4-1107 on Young's modulus measurements,
- SEMI MS5-1107 on critical wafer bond toughness,

Technical Contacts:
J. Marshall
C. McGray
R. Allen

"Having seen your proposed work and timetable for producing the (MNT 5-in-1) SRM, we support your work in this area and see value in the semiconductor and MEMS arena."

Mark Crockett,
Applied Materials

"We have more than 100 unique MEMS customers, from Fortune 500 companies to small university labs, and believe the proposed (MNT 5-in-1) standard would be of high interest to all of them."

Erik Novak,
Veeco

- SEMI MS6-0308 on design and materials for interfacing microfluidic systems,

- SEMI MS7-0708 on microfluidic interfaces to electronic device packages, and

- SEMI MS8-0309 on hermeticity of MEMS packages.

Other SEMI MNT standardization efforts include a Young's Modulus and Step Height Round Robin Experiment and a Wafer Bond Strength Round Robin Experiment to obtain precision and bias data to validate the pertinent standards.

An additional activity in SEMI's MNT standardization effort is the identification of standards related to MNT technology. SEMI is attempting to identify these standards and incorporate them into SEMI's "Standard of Standards." This Standard of Standards, which will list MNT standards from all standardization bodies and be maintained by the North American MEMS Standards Committee, will serve to guide industry and researchers to existing standards and highlight areas where standards may be needed.

NIST: Currently, there are four major standardization thrusts at NIST in the MNT Project:

1. The development of the MNT 5-in-1 Standard Reference Materials (SRMs), which includes the validation of the Young's modulus and step height standards (SEMI MS4 and SEMI MS2, respectively) and updates to the SED MEMS Calculator Web pages.

2. The development of the SEMI standard MS5, Test Method for Wafer Bond Strength Measurements Using Micro-Chevron Test Structures and the development of the Micro-Chevron SRM utilizing this standard test method.

3. Dimensional metrology for microfluidics.

4. Cutting edge robotics research and development leading to standardization efforts. Specific details associated with each of these activities are presented in the Accomplishments section.

DELIVERABLES:
To develop the prototype MNT 5-in-1 SRM(s):

- Monitor (or if appropriate perform) the post processing of the SRM chips. 4Q 2009
- Measurements of prototype SRM chips to test the viability of the test structures. 4Q 2009
- Explore available packaging options for the SRMs. 3Q 2009
- If appropriate i) submit SRM design modifications for fabrication and ii) update the SED MEMS Test Structures Web Pages. 3Q 2009

To coordinate a Young's Modulus and Step Height Round Robin:

- If appropriate, update the Round Robin User's Guide. 1Q 2009
- For the Young's modulus standard, provide i) draft instructions for use with a stroboscopic instrument, if appropriate, and ii) draft modifications to the existing standard for use with a dual beam vibrometer. 1Q 2009
- Initiate the round robin after the round robin chips are packaged. 1Q 2009

Deliverables associated with the development of the Micro-Chevron SRM:

- Complete international round robin to achieve a precision and bias statement for SEMI MS5 2Q2009.
- Prepare modifications of MS5-1107 to reflect results from international round robin. 2Q2009

Deliverable associated with dimensional metrology for microfluidics:

- Prototype test chip for microfluidics dimensional metrology. 3Q 2009

Deliverable associated with cutting edge robotics research and development which will lead to standardization efforts:

- Experiments to measure the step characteristics of MEMS-scale robots. 3Q2009
- Organize a competition of nanogram-scale robotics at the 2009 RoboCup competition. 4Q2009

Accomplishments

■ *Young's modulus measurements*: SEMI standard MS4-1107 obtains Young's modulus from resonating cantilevers oscillating out-of-plane. It applies to films, such as found in MEMS materials, which can be imaged using a non-contact optical vibrometer, stroboscopic interferometer, or an instrument comparable to one of these. A round robin experiment is being performed to obtain precision and bias data in order to validate the standard.

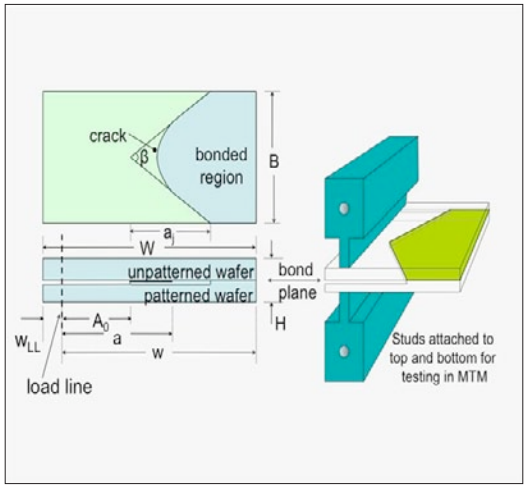

Figure 1. Micro-chevron test structure showing key dimensions and mounting for testing in a materials testing machine (MTM).

■ *Calculations of residual stress and its gradient:* SEMI standard MS4-1107 also provides for residual stress and stress gradient calculations. These calculations require the Young's modulus value obtained in the standard and values for residual strain (using ASTM E 2245) and strain gradient (using ASTM E 2246). High values of residual stress lead to failure mechanisms in ICs such as electromigration, stress migration, and delamination. Knowledge of the residual stress values can be used to improve the yield in CMOS fabrication processes.

■ *Led development of standard for critical wafer bond toughness:* SEMI standard MS5-1107 uses micro-chevron test structures which consist of two materials, typically two silicon wafers bonded together. The main characteristic of the test structure is the wedge-like structure (which gives it its name) in the bond interface. Studs or blocks are glued to either side of the test structure and positioned in the material testing machine where the test structure is pulled apart (see Fig. 1). The maximum load is measured and the critical wafer bond toughness is calculated, which is a measure of the wafer bond strength. The measurement technique described in this standard can be used to determine a preferred bonding technique and can also be used to obtain spatial information on bonding quality across a wafer.

■ *Organized round robin for precision and bias statement for SEMI MS5:* An eight-laboratory round robin is underway to determine precision and bias for SEMI MS5. This international team includes industrial and academic participants. An image of a post-test micro-chevron test structure is shown in Figure 2.

■ *Presentation of an invited talk* "Wafer Bonding Standardization" describing the development of the SEMI standard MS5-1107, Wafer Bond Strength Measurement at the 2007 Conference on Wafer Bonding for MEMS and Wafer Level Integration in Halle, Germany.

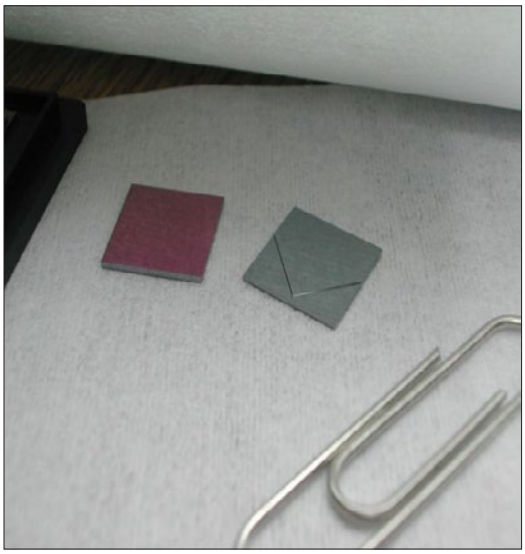

Figure 2. Micro-chevron test structure after testing in a materials testing machine (MTM).

■ *Step height and thickness measurements:* A round robin experiment is being performed to obtain precision and bias data in order to validate the SEMI MS2 step height standard. Step height measurements using MS2 are incorporated in an electro-physical technique to find the thicknesses of all the layers in a 1.5 µm commercial CMOS foundry process. Figure 3 shows a test chip design with thickness test structures along the top edge of the chip. A design rendition of a sample thickness test structure is given in Fig. 4a, with its cross section given in Fig. 4b.) Relatively low values for combined standard uncertainty uc (between 0.20 nm and 150 nm for a given processing run) have been found. In addition, an earlier version of this technique has been supported via the successful optimization of the Young's modulus values for the various layers in the process. As a rule of thumb, the electrical approach (that obtains thicknesses from capacitance, sheet resistance, and resistivity values) is preferred for thicknesses with uc values less than or equal to 0.035 µm. This corresponds

somewhat to the layers, such as the poly2-to-poly1 oxide and the poly2 layers, which tend to be fabricated earlier in the processing sequence. The capacitances for the oxide layers fabricated earlier in the processing sequence are typically higher and thus easier to measure accurately. For capacitances less than or equal to 24.7 aF/μm^2, the physical approach (that obtains thicknesses from step height measurements) is preferred. The electro-physical technique is detailed in a 39-page paper.

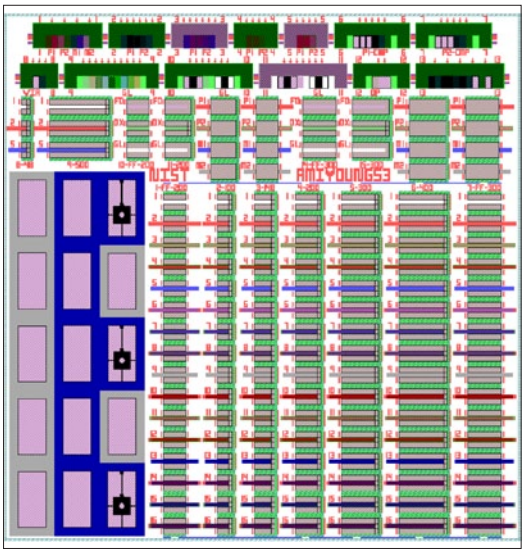

Figure 3. CMOS test chip design incorporating thickness test structures, cantilevers, fixed-fixed beams, and tensile test structures.

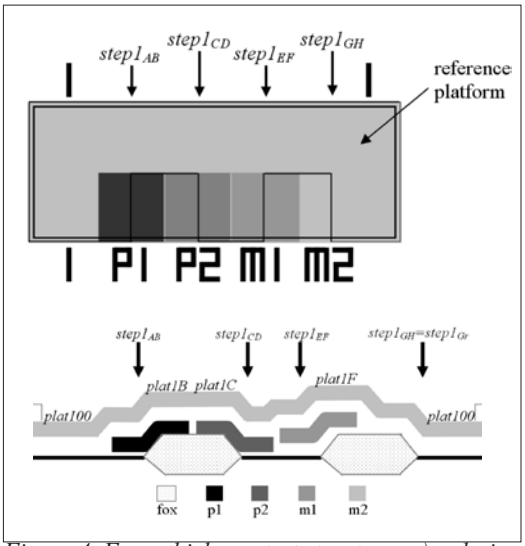

Figure 4. For a thickness test structure: a) a design rendition and b) a cross section.

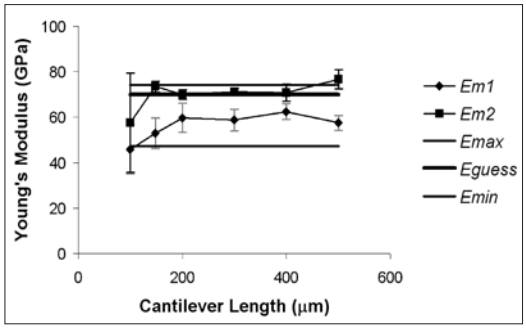

Figure 5. Optimized Young's modulus values for metal1 and metal2 versus length.

■ *Young's modulus measurements from composite beams:* The test chip design given in Fig. 3 includes cantilevers ranging in length from 100 μm to 400 μm. Plots of Young's modulus versus length for each layer exhibit very good results. The optimized Young's modulus results are stable as a function of length and within the realm of acceptability! Figure 5 shows these plots for metal1 and metal2. The data points given at L=500 μm represent the averages from two previous chip submissions. The error bars on the data points represent a plus or minus one sigma variation. The minimum and maximum bounds represent values given in the literature. The line represented by 'Eguess' is the initial value used in the optimization. An initial result from tensile tests done by David Read at NIST-Boulder found an average metal1 and metal2 Young's modulus value of 63 GPa, which falls nicely between the metal1 and metal2 lines in Fig. 5.

■ *SED MEMS Calculator Web pages:* The SED MEMS Calculator Web site includes access to data sheets on which calculations can be performed that go hand-in-hand with select MEMS standards or standards-related work. A symbol can be spotted on the Web site that easily locates material associated with the MNT 5-in-1 SRM.

■ *MNT 5-in-1 SRMs:* Currently, there are two different MNT 5-in-1 SRM designs; one for a bulk-micromachining CMOS MEMS process via MOSIS (see Fig. 6) and the other for a surface-micromachining MEMS process at MEMSCAP (see Fig. 7). Prototype CMOS MNT 5-in-1 SRMs doubled as the Young's Modulus and Step-Height Round Robin Test Chips.

The MNT 5-in-1 SRM contains MEMS structures with five specific well-defined geometric

and material properties. The five parameters associated with the MNT 5-in-1 SRM are in-plane length, residual strain, strain gradient, step-height, and Young's modulus. The first three parameters have been standardized in ASTM as E 2244, E 2245, and E 2246. The fourth and fifth parameters have been standardized in SEMI as MS2-0307 and MS4-1107. The five measurements will be taken at NIST on the MNT 5-in-1 SRM and delivered to the customer along with a certificate and the pertinent SED MEMS Calculator data sheets (completed with NIST data) in order for the customer to compare their in-house measurements with those taken at NIST, thereby validating their use of the documentary standards. Customers, including design companies, equipment manufacturers, and fabrication services, have expressed support for this SRM. This is an interlaboratory effort, involving several of NIST's laboratories.

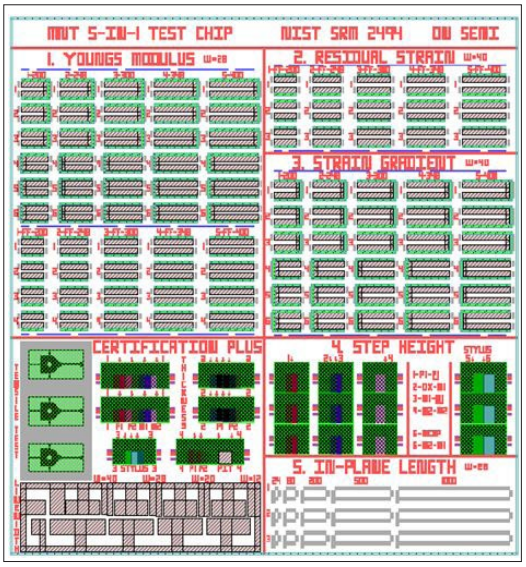

Figure 6. MNT 5-in-1 SRM design for a bulk-micromachining CMOS MEMS process.

■ *Micro-chevron SRM:* A proposal was crafted for the development of a micro-chevron SRM for the calibration of critical wafer bond toughness and a micro-chevron test structure (see Figs. 1 and 2) was designed and fabricated for use in this destructive test. Wafer-wafer bonding is a mainstay for MEMS design and fabrication. MEMS components, such as acceleration sensors, gyroscopes, micropumps, or microvalves that are increasingly found in smart automotive and navigation control systems, and medical devices, which typically use

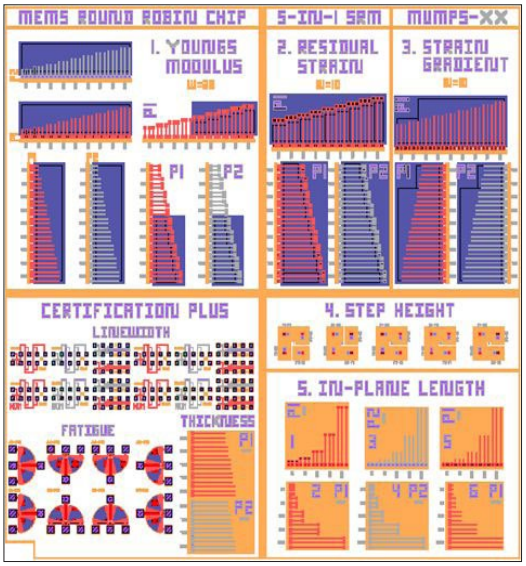

Figure 7. MNT 5-in-1 SRM design for a surface-micromachining MEMS process.

wafer bonding technologies. Due to being subjected to mechanical stresses, the industrial applications of these components require a high mechanical strength and high reliability of the wafer-bonded interface. For a knowledge of the strength determining factors (such as fatigue and stress corrosion) of wafer bonding, for quality control, and for the development of new bonding technologies, a method for determining the strength of such bonds is important to producers and users of MEMS devices, of wafer bonding equipment, and of wafer materials.

■ *Dimensional metrology for MEMSs:* In the area of dimensional metrology for microfluidics, the MNT Metrology Project has undertaken development of dimensional metrology test structures and techniques. The goal of this work is standard test structures, methods, and analysis techniques such as exist for semiconductor devices.

■ *MicroRobotics:* In the area of MicroRobotics, the MNT project held the first-ever competition between nanogram-scale microrobots. The competition was held in association with the 2007 RoboCup International Championships in Atlanta, GA in July, 2007. The competition produced novel microrobotic technologies and MEMS actuators, and received extensive press coverage from CNN, MSNBC, ABC News, and 117 affiliates of the Associated Press. In addition, the event was re-

ported on the front page of the DoC website. The competition revealed technological challenges and metrology needs, including the following:

1. Environmental control for microrobotics stations.

2. Techniques for imaging trapped charge in dielectric surfaces and films.

3. Assessment of contact mechanics in sliding-mode micromechanical actuators.

4. Integrated control of magnetic fields in microrobot operating environments.

5. Bandwidth multiplexing for capacitively-coupled microrobotic devices.

■ *Microrobotics U.S. Open 2008:* A second MicroRobotics demonstration was held as part of the 2008 RoboCup U.S. Open, held in Pittsburgh, PA, in May 2008. Teams from Carnagie Mellon University and the U.S. Naval Academy demonstrated recent developments in MicroRobotic actuation including a robot capable of moving in a fluidic environment.

■ *NIST Workshop on MicroRobotics:* A workshop was organized by members of the MNT project and held before the 2008 Hilton Head Sensors, Actuators, and Microsystems Workshop. Approximately 40 researchers from industry and academia heard eight invited talks from leaders in the nascent field of microrobotics.

■ *2009 IEEE International Conference on Microelectronic Test Structures:* A member of the MNT project served as technical chair of this international conference, now in its 23rd year. This conference has expanded in recent years to include a significant number of papers on MNT technologies.

Collaborations

Collaborators for the development of the MNT 5-in-1 Standard Reference Materials (SRMs) MOSIS Integrated Circuit

Fabrication Service, 4676 Admiralty Way, Marina del Rey, CA, Dr. P. Thomas Vernier

MEMSCAP Inc., 4021 Stirrup Creek Drive, Suite 120, Durham, NC, Buzz Hardy

NIST Boulder, Materials Science and Engineering Laboratory, Materials Reliability Division, Dr. David T. Read

Pennsylvania State University, University Park, PA, Dr. Christopher L. Muhlstein

Collaborators for the development of the Micro-Chevron SRM:

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Univ. of Wisconsin, Dr. Kevin Turner

Fraunhofer Inst. (Germany), Dr. Joerg Bagdahn

NIST Gaithersburg, Materials Science and Engineering Laboratory, Ceramics Division, Dr. George Quinn

University of Illinois, Dr. Gavin Horn

SUSS Microtec (Vermont), Dr. Shari Farrens

X-Fab Semiconductor Foundries, Dr. Roy Knechtel

Medtronic (Arizona), Mike Mattes, Ralph Danzi

Collaborators for the cutting edge robotics research and development which will lead to standardization efforts

Carnegie Mellon University, Nanorobotics Laboratory, Dr. Metin Sitti

Carnegie Mellon University, Electrical and Computer Engineering Department, Dr. Gary Fedder

U.S. Naval Academy, Dr. Samara Firebaugh

ETH Zürich, Dr. Brad Nelson

Simon Fraser University, Dr. Ash Parameswaran

Johns Hopkins University, Dr. Andreas Andreou

Universite de Sherbrooke, Dr. Luc Fréchette

University of Waterloo, Dr. Mustafa Yavuz and Dr. Omar Ramahi

Publications

SED MEMS Calculator Web site: http://www.eeel.nist.gov/812/test-structures/MEMSCalculator.htm.

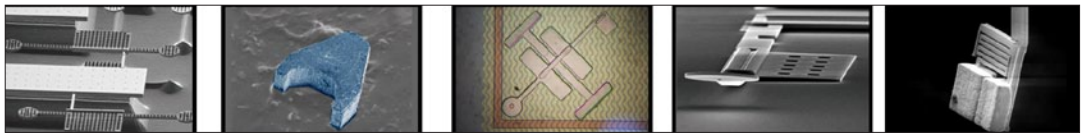

Figure 8. The five micro robots that competed in the 2007 RoboCup International Championships Nanogram Demonstration League in July 2007.

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NIST's Center for Nanoscale Science and Technology Nanofab

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Goals

The NIST Center for Nanoscale Science and Technology supports the development of nanotechnology from discovery to production. The Center includes a Research Program and a national nanofabrication facility, the NanoFab. The Research Program develops innovative nanoscale measurement and fabrication capabilities, and is accessible via collaboration with CNST scientists. The NanoFab is a fee-based, shared use facility accessible to all through a simple application process, providing researchers rapid access to a comprehensive suite of state-of-the-art tools and processes for nanofabrication. The CNST provides:

- Essential measurement and fabrication methods, standards, and technology to support all phases of nanotechnology development.
- Experts in a wide variety of disciplines; from physics, chemistry, materials science, molecular biology, computer science, and electrical, mechanical, chemical and aeronautical engineering.
- A world-class, state-of-the-art nanofabrication facility—with over 19,000 square feet (1,800 m^2) of cleanroom laboratory space.
- A hub linking the nanotechnology community to the comprehensive measurement expertise within all the NIST Laboratories.

Customer Needs

The CNST was established in May of 2007 to accelerate innovation in nanotechnology-based commerce. Its mission is to support the development of nanotechnology through research on measurement and fabrication methods, standards, and technology, and by operating a state-of-the-art nanofabrication facility, the NanoFab. The Center, located in NIST's Advanced Measurement Laboratory Complex on the Gaithersburg, MD campus, promotes innovation by using a multidisciplinary approach to research, maintaining a staff of the highest caliber, and leveraging its efforts by collaborating with others.

The CNST mission is guided by an understanding that rapid commercial development of nanotechnology—in particular, the speed with which industry can bring a specific new nanotechnology from discovery to production—depends critically on the availability and efficacy of applicable metrology tools and processes at each stage of the transition. Developing these tools and processes will have an immediate and significant impact on the commercial viability of nanotechnologies in a diverse array of fields, such as electronics, computation, information storage, medical diagnostics and therapeutics, and national security and defense.

Figure 1.The CNST is located in the NIST Advanced Measurement Laboratory Complex, including the NanoFab cleanroom seen on the left. (Photo courtesy HDR Architecture, Inc./Steve Hall © Hedrich Blessing.)

Technical Strategy

The CNST operates as a multidisciplinary center for developing and disseminating new nanoscale measurement and fabrication technologies, with the goal of increasing the competitiveness of U.S. industry in nanotechnology and nanomanufacturing. By creating a strong research program and establishing a national shared-use nanofabrication facility, the CNST aims to close gaps in the understanding of nanoscale phenomena, and thereby accelerate innovation in a wide range of applications with broad societal impact.

The CNST Research Program is initially focused in the following three areas:

- Future Electronics. In support of continued growth in the electronics industry beyond complementary metal-oxide-semiconductor (CMOS) technology, CNST researchers are developing new methods to create and characterize devices, architectures, and interconnects for graphene, nanophotonic, nanoplasmonic, spintronic, and other future electronics.

- Nanofabrication and Nanomanufacturing. The Center is advancing the state of the art in nanomanufacturing by developing measurement and fabrication tools for both lithographic ("top-down") and directed assembly ("bottom-up") approaches.

- Energy Storage, Transport and Conversion. The CNST is building a program that will create new methods for elucidating light-matter interaction, charge and energy transfer processes, catalytic activity, and interfacial structure at the nanoscale in energy-related devices.

Within the CNST's Research Program, it has established initial core competencies in atomic-scale characterization and manipulation; laser-atom manipulation; nanophotonics; nanoplasmonics; optical micro and nanoelectromechanical systems (MEMS and NEMS); nanomagnetic imaging and dynamics; directed assembly; nanoscale stochastic processes; nanoscale electronic and ionic transport; and theory, modeling and simulation of nanostructures.

The NanoFab provides researchers access to and training on the advanced tool set required for cutting-edge nanotechnology development. It is located in a large, dedicated cleanroom — with all the tools operated within an 8,000 square feet (750 m^2) class 100 space — and in adjacent laboratories. These laboratories include superior vibration, temperature, and humidity control and air quality. Over fifty tools are available for e-beam lithography, photolithography, nanoimprint lithography, metal deposition, plasma etching, chemical vapor diffusion, wet chemistry, and silicon micro/nanomachining. The facility is accessible through a straightforward application process designed to get users into the cleanroom in a few weeks. It is open from 7 am to 7 pm, Monday through Friday (note that hours can be expanded to support access needs.)

A comprehensive list of the NanoFab equipment is included below. Of particular note are the electron beam lithography tools, which include a Vistec VB300 in the cleanroom with <10 nm line width, and a JEOL JBX-6300FS system with comparable capabilities that will become available in the second half of 2009. Other important capabilities are enabled by a Zeiss NVision 40 focused ion beam (FIB) system incorporating a Gemini scanning electron microscope and four-channel gas injection system. It can accommodate from mm-sized samples to 100 mm-diameter wafers for nanometer scale patterning, etching, nanomanipulation, and TEM sample preparation.

NanoFab Equipment

Figure 2. A plasma etching bay in the NanoFab's class 100 cleanroom.

Lithography

- E-beam Lithography System: Vistec VB300
- E-beam Lithography System: JEOL JBX-6300FS*
- Laser Pattern Generator: Heidelberg DWL-66FS
- Nano-Imprint Lithography Tool: Nanonex NX-2000
- Nanonex Ultra-100 Integrated UV-Ozone Cleaner/Molecular Vapor Coater
- Contact Aligners (2): Suss Microtec MA6 and MA8
- Spinners (2): Laurell Technologies Series WS-400 and WS-500
- Spinner/Hotplate: Brewer Science CEE Model 100CB
- Process Benches (2): E-Beam Resist Processing Stations*

Furnaces

- General Thermal Oxidation and Diffusion (Bank 2)

- CMOS Thermal Oxidation and Diffusion (Bank 1)
- Low Pressure Chemical Vapor Deposition (LPCVD) Furnace (Bank 3)
- Rapid Thermal Annealer: Modular Process Technology
- PECVD-Unaxis 790

Metal Deposition

- Sputterers (2): Denton Vacuum Discovery 22 and Discovery 550
- E-beam Evaporator: Denton Infinity 22
- Thermal Evaporator: Denton Discovery 22

Wet Chemistry

- Heated Wet Chemical Benches (2): 2 m and 2.4 m
- KOH/TMAH Wet Etch Bench: Reynoldstech
- Acid Etch Bench: Reynoldstech
- Spin Rinse Dryers: Semitool PSC-101

Dry Etch

- Deep RIE: Unaxis SHUTTLELINE DSEII
- Metal RIE: Unaxis 790
- Silicon RIE: Unaxis 790
- Multipurpose RIE Systems (2): Oxford*
- ICP Metal Etcher: Unaxis SHUTTLELINE ICP
- XeF_2 Silicon Etch: Xactix Xetch e1 Series
- Microwave Plasma System: PVA Tepla 300

Specialty Tools

- Atomic Layer Deposition: Oxford FlexALRPT*
- Parylene Deposition System: Specialty Coating Systems PDS-2010
- Wafer Bonder: Suss Microtec SB6e
- Focused Ion Beam: Zeiss NVision 40

Inspection

- Stress Measurement Tool: Toho Technology FLX-2320
- Table-top SEM: Hitachi TM-1000
- Scanning Electron Microscope: Zeiss Ultra-60 FESEM
- Atomic Force Microscopes (2): Veeco Dimension 3000, Dimension 3100
- Contact Angle Goniometer
- Spectroscopic Ellipsometer: Woollam XLS-100
- Reflectometers (2): Filmetrics, Nanometrics
- Contact Profilometer: Dektak 6M
- Optical Microscope with Image Capture: Nikon
- Four-Point Probes (2): Jandel RM2
- High Power Inspection Microscopes: Olympus
- High Power Nomarski Microscope: Nikon*

Post Process

- Wafer Dicing Saw: Disco Model 341
- Wire Bonder: Kulicke and Soffa Model 4526
- Critical Point Dryer

DELIVERABLES:

- *New tools to be operational in 4Q2009

Disclaimer: Certain commercial equipment, and software, are identified in this documentation to describe the subject adequately. Such identification does not imply recommendation or endorsement by the National Institute of Standards and Technology, nor does it imply that the equipment identified is necessarily the best available for the purpose.

Metrology for Spintronic Devices

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Goals

The overall goal of the Metrology for Spintronic Devices program is to develop the metrological tools that will enable the development of electronic devices that exploit the electron spin degree of freedom in addition to its charge. Present spintronic devices include magnetic random access memory (MRAM), hard-disk drive read heads, and other highly compact magnetic memory devices. In addition, spintronic devices also present an avenue towards replacing conventional complementary metal oxide semiconductor (CMOS) technology as device dimensions shrink into the deep nanometer regime, with the development of entirely new device structures such as nanoscale microwave components for on-chip spectral analysis, nanoscale timing elements, and microwireless communication architectures. In each case, a fundamental understanding of the interactions between a spin-polarized current and ferromagnetic metals and semiconductors is a necessity. The particular goal of this project is to develop the metrology and perform the fundamental measurements to enable the development of these spin-based devices.

Customer Needs

MRAM elements have been incorporated into commercial since late 2006. It is expected that the present circuit architecture, which relies on switching (writing) using applied magnetic fields, will not be viable beyond the 65 nm lithography node. This limitation arises from the scaling laws associated with the stability of the magnetic structures used in MRAM devices: As the device dimensions are decreased, the magnetic elements are required to have increased stability against thermal fluctuations. This, in turn, requires larger writing fields, which cannot be supported in the present device architecture. It is projected that spin transfer induced switching will be essential for device scaling beyond the 2011-2012 timeframe. While this switching mechanism is very promising, it has only been an active area of research for the last few years, and although certain aspects of the switching processes are well understood, others are not. The main thrust of this program is to develop metrologies that will enable the development of spin transfer based MRAM (spin-RAM) for the commercial market.

In order for spin-RAM to be technically viable at the smallest device sizes, the fundamental metrology to characterize the intrinsic scaling laws associated with the spin transfer effect need to be developed. In particular, methods to definitively relate threshold switching currents to fundamental materials properties need to be developed, materials damping parameters need to be measured at the device level, and the detailed angular variation of the spin torque needs to be understood. These measurement methods will enable the reduction of device switching currents (which are limited by available transistor source currents), as well as the underlying mechanisms causing variations in device-to-device behaviors. These measurements and techniques have been somewhat developed in all-metallic systems with conventional in-plane magnetized ferromagnetic alloys. However, it is expected that tunnel junction structures will be required for commercial applications and novel magnetic materials (e.g., perpendicularly magnetized materials, highly spin-polarized materials) may be needed. Furthermore, new techniques for non-destructively and rapidly measuring the ferromagnetic resonance properties of magnetic materials at the wafer level are needed. This program's efforts will be particularly focused on developing metrologies to better understand device to device switching variations (that may result from shape or materials variations), the behavior of devices having perpendicularly magnetized films, magnetic tunnel junction structures, and a large area scanned probe ferromagnetic resonance (FMR) measurement system.

Technical Strategy

The technical strategy is to develop the metrology and perform the fundamental measurements to characterize and understand the effects of spin-polarized currents in spin-based magnetic nanostructures. Particular attention will be paid to measuring the intrinsic scaling laws associated with device switching times in both all-metallic and magnetic tunnel junction MRAM structures. A clear understanding of the role that thermal contributions play in determining the critical current densities and switching mechanisms will be essential for future scaling of these devices. Additional measurements will investigate the ef-

fects of shaped switching pulses and developing metrologies to measure the ferromagnetic resonance (FMR) response of individual nanoscale MRAM elements and how that response can be used to predict its switching characteristics. These measurements will directly address of the role of patterning techniques and anisotropy variations in determining the switching distribution of MRAM elements. These metrologies will provide a basis for scaling of MRAM devices below the 65 nm node. Our technical work will also focus on evaluating the potential of emerging nanoscale spintronic devices for replacing/augmenting CMOS in the deep nanometer regime.

DELIVERABLES:

- Develop broadband (20 GHz) wafer-level metrologies to predict magnetic noise contributions to completed MTJ sensors and MRAM devices. (Paper published: Appl. Phys. Lett. 94 (1) 012506, 2009.)

- Development of high speed spin-RAM devices utilizing perpendicularly magnetized materials: Develop in-house deposition techniques for growing Co/Ni and Co/Pd multilayered materials having perpendicularly magnetized anisotropies and measure high speed switching characteristics. FY 09, Q1

- Compare high frequency ferromagnetic resonance measurements of individual spin-RAM elements with their high speed switching characteristics to determine underlying mechanisms determining switching current distributions. FY 09, Q3

Accomplishments

■ *High-Speed, Current-Induced Switching for MRAM Devices:* In collaboration with Hitachi Global Storage Technologies (HGST) and Freescale Semiconductor we have demonstrated that sub-nanosecond (290 ps) switching of nanoscale MRAM devices is possible via the spin transfer effect. To date this is the shortest switching time that has been reported in the literature. The inverse switching time (*i.e.*, the switching frequency) at room temperature is linearly proportional to the current applied to the device. This finding is expected from theoretical considerations and indicates that the measured room-temperature switching threshold is strongly affected by thermal fluctuations in the nanoscale devices. By extrapolating the measured switching current to zero applied pulse width, the theoretical value of the intrinsic device critical current can be determined. However, this theoretical method of determining the intrinsic switching thresholds (i.e., those related to materials properties and device size) from stochastic, thermally activated switching events had not been previously experimentally verified. By comparing the thresholds for current driven switching at room temperature and 4 K for a range of applied field values, we have been able to verify the extrapolation methods used to infer the intrinsic switching current, identify thermal contributions to the switching threshold, and determine the materials/device parameters that are responsible for setting the intrinsic switching threshold. These measurements will allow for improved device design and reliability for future MRAM at the 65 nm node and beyond.

■ *Damping in Magnetic Nanostructures:* One of the critical parameters in determining the threshold switching current in magnetic devices is the magnetic damping parameter; the larger the damping in the system, the larger the current required to switch the device. While material dependent damping parameters have been routinely measured in macro/microscopic devices, very little is known about how damping is affected when device sizes are decreased to the nanometer length scale. As device dimensions are decreased, the surfaces of the devices become increasingly important. This is particularly the case for damping in magnetic nanostructures. Nanomagnetic devices will typically have oxidation of the ferromagnetic materials on at least some of their sides, and ferromagnetic oxides are well known sources of damping. Recently some researchers have shown indirect evidence that the magnetic damping in magnetic nanostructures can be increased by more than a factor of ten relative to that of macroscopic devices. We have recently developed the metrology capabilities to directly measure the magnetic damping in a variety of magnetic systems over a wide range of device sizes. Our new optical method of measuring damping on arrays of devices has shown that, at room temperature, oxidation has a negligible effect and that shape variations in nanoscale devices increase the apparent damping by only about a factor of two. We have also developed a new method to electrically measure the damping parameter in single devices having dimensions below 100 nm. These measurements, while still

being perfected, corroborate those from large arrays, and provide an experimental method for separating broadening effects due to ensemble measurements from intrinsic device variations in damping.

■ *Noise and Current Induced Switching in Magnetic Tunnel Junction Devices:* Currently, typical spin transfer based MRAM structures are based on all-metallic structures. These structures have resistances on the order of 5 ohms to 10 ohms and are poorly impedance matched to standard semiconductor circuitry. While this impedance mismatch will become less severe as device dimensions are decreased, it will likely be necessary to implement magnetic tunnel junction (MTJ) devices. However, in general, there is also an increase in noise, particularly at low frequency, when incorporating tunnel junctions into device structures, which can degrade device performance and read-out fidelity. Low-frequency noise is associated with defects and atomic scale variations in the barrier. We have successfully measured and characterized this excess noise in high-quality aluminum oxide magnetic tunnel junctions with dimensions on the order of several micrometers and used Lorentz transmission electron microscopy (TEM) imaging to investigate the correlation between electronic noise and the structural properties of the barrier. More recently we have upgraded the TEM instrumentation and fabricated devices so that the magnetic devices can now be imaged with Lorentz microscopy under active bias. This allows us to directly image the magnetic fluctuations in a device while simultaneously measuring its electrical characteristics. Through these simultaneous measurements we can discriminate between intrinsic magnetic fluctuations in the MTJ devices and those associated with electrical defects in the barriers.

■ *Nanoscale Generation of Spin Waves for Communication Architectures:* At present, spintronic devices are being considered as potential replacements for future generation CMOS devices. The basic advantage of spintronic devices is that they provide the potential to perform both communication and computation through spin instead of charge, and so may be able to perform these operations with comparatively low power dissipation. Several proposed communication and computation architectures are based on the local generation and subsequent propagation of spin waves, Fig. 1. Previously, we have shown that nanoscale magnetic devices are able to generate coherent, frequency-tunable, gigahertz frequency spin waves. However, the currents required to generate them were relatively high and their propagation away from their source was only theoretical. We have performed the metrology to show directly that in the correct geometry the spin waves can coherently propagate more than 0.5 μm away from their point of generation, putting fairly lenient geometrical constraints on potential device considerations, and demonstrating an additional channel for device coupling and interaction.

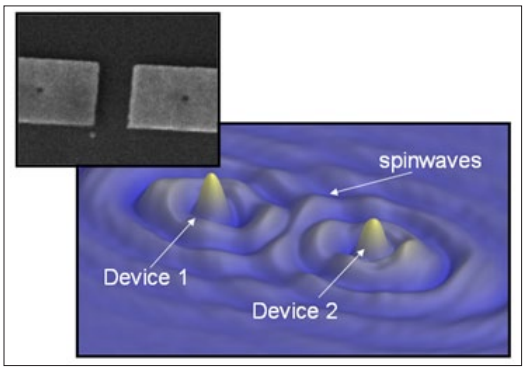

Figure 1. Micromagnetic simulation showing coherent spinwave radition between two local spin transfer oscillators. Inset: SEM image of the fabricated devices.

■ *Size Dependence of Spin Transfer Switching Currents:* In all-metallic spin-RAM devices, single domain modeling (assuming that the magnetization of the device moves as a single vector entity) generally predicts that intrinsic switching current density should be constant with increasing device size. To test this basic prediction we systematically measured the intrinsic switching current density in devices having critical dimensions ranging from 40 nm to 200 nm. From these high-speed pulsed switching experiments we found that the intrinsic switching current densities were size dependent and 50 %–100 % higher than predicted by a single-domain model. On the other hand, the data are in good agreement with detailed micromagnetic simulations, which suggest that reversal on the devices occurs through micromagnetic pathways rather than through completely coherent rotation of the magnetization. Although quasi-static field induced switching measurements suggest that the devices behave as a single domain "macro-spin," this work has shown that this assumption is not valid in the case of high-speed current induced switching.

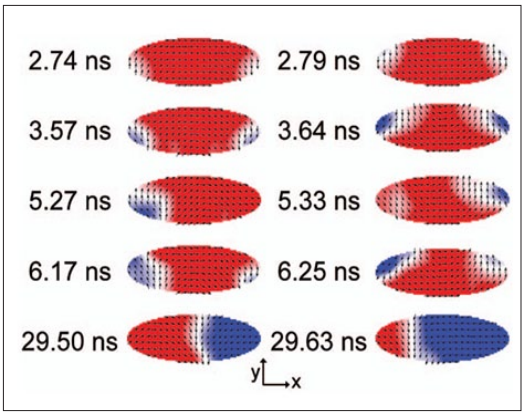

Figure 2. Micromagnetic simulation snapshots showing the reversal process in a 60 x 175 nm^2 ellipse. The colors represent the average component of the magnetization along the x-directions (red-positive, blue negative).

Collaborations

IBM: MRAM device imaging and thermal induced noise in tunnel-junction based MRAM devices. Freescale Semiconductor: MRAM device imaging and incorporating magnetic tunnel junctions into MRAM devices.

Hitachi Global Storage Technologies: high-speed switching in all-metallic MRAM devices.

Seagate Technologies: phase-locking mechanisms in spintronic microwave oscillator arrays.

U. S. Army Research Laboratory: high frequency impedance measurements.

Future Opportunities

Nanoscale spintronic devices also provide an opportunity for the development of dense non-volatile memory elements as well as new spin-enabled nanoscale microwave devices, such as microwave sources and mixers for timing, communications, and spectral analysis applications. In addition, they also provide one potential avenue towards replacing/augmenting conventional CMOS devices in the deep nanometer regime. As such, we expect spintronic devices to have a great impact on the semiconductor industry, particularly as device dimensions shrink into the nanoscale. The goal of this project is to provide the fundamental metrology and measurements to enable the development of this wide range of devices and applications.

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Magneto-resistance and spin transport in non-traditional tunnel devices

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Goals

The goal of the project is to explore non-traditional methods for creating high-transparency tunnel junctions, optimize spin transport through these junctions, and test fundamental limits of the tunneling process in the thin barrier limit.

Customer Needs

Since the introduction of giant magneto-resistive (GMR) hard drive read heads in 2000, spin transport devices have been a part of the technological mainstream. These devices produce a substantial difference in the device resistance due to the remnant magnetic field from a bit stream on the hard drive platter. As the read head is scanned over the platter surface, the pattern of high and low resistances produced by the GMR device maps directly to the information stored on the hard drive. These CIP-GMR (current in plane) read heads fueled an ambitious increase in hard drive information density over several years, but ultimately pushed beyond limits of CIP-GMR feasibility. Consequently, tunneling magneto-resistance (TMR) based read heads were introduced in 2005 to enable new generations of increased density hard drives. Similar to the GMR-based hard drives, TMR read heads exhibit a change in resistance corresponding to the remnant field of the bit stream on the hard drive platter. TMR-based devices use a metal-insulator-metal tunnel junction interface that results in relatively high resistances and resistance-area (RA) products (the mathematical product of the resistance and cross sectional area). As a result, as the hard drive industry moves to higher density generations, the corresponding reduction in the TMR head size acts to increase the resistance and decrease the effective bandwidth. These technical limitations have resulted in dim prospects for extensive reliance on TMR read heads and a reinvestment in a modified current perpendicular to the plane (CPP) GMR-type read head. While the TMR read heads exhibit RA products that are undesirably large, the CPP GMR heads currently have undesirably small RA products. An ideal middle ground for future hard drive read heads would come from *a layer structure with an intermediate RA product that still exhibits good magnetic field sensitivity with high bandwidths and low power dissipation.*

These fundamental challenges facing the hard drive industry as bit sizes push below 100 nm has fueled development of massively parallel magnetic storage systems in the form of magnetic random access memory (MRAM). These systems utilize massive arrays of TMR devices, using the high or low resistance state to directly store information. The "write" process in contemporary MRAM utilizes a separate "write" line that produces a local magnetic field to change the TMR device from the high to low resistance state. For MRAM to achieve massive market penetration the bit density has to be increased and the device cost decreased, most likely accomplished by elimination of this separate write line element. The "write" operation would be accomplished by spin transfer torque (STT) mechanisms already demonstrated in the research setting, but outside the feasibility envelope for commercial devices. Successful integration of the STT write relies on improved spin transport through tunnel junctions and *improved fundamental understanding of spin dissipation*.

Magneto-resistive hard drive read heads and the bourgeoning MRAM industry are both spintronic devices, where information is stored, processed, or transferred using electron spin rather than charge. As the semiconductor industry moves "beyond CMOS," successful discovery and implementation of spin processing and data transmission systems rely on yet to be developed systems for spin transport and accumulation. As the most effective means of injecting spin yet discovered, *tunnel junctions figure to be prominent players in spin information processing, demanding spin metrology systems and exquisite understanding of spin transport mechanisms.*

Technical Strategy

High transparency (low electrical resistance) tunnel junctions that preserve (or improve) spin polarization and enable spin-based information technology are of intense technological interest. As tunnel junctions reach the lower limits of barrier thickness (atomic sizes), both practical

limitations related to uniformity of deposition and long standing reliance on the WKB (Wentzel, Kramers and Brillouin) approximations of tunneling pose new challenges. Rather than pursue conventional approaches to increasing tunnel junction transparency through uniform deposition of a thinner barrier, we are utilizing a unique process approach where a robust and reproducible tunnel barrier (typically 1.5 nm thick) is deposited and then irradiated with ions. The irradiation process relies on the deposition of the ion's neutralization energy (as much as 52 keV per ion), thinning a nanometer-sized area of the base tunnel junction to a tunnel junction only Angstroms thick whose conductance dominates the electrical performance of the whole device. Using this approach, a single layer structure can be tuned to a user-selected conductance value spanning many orders of magnitude by adjusting the irradiation parameters. Using this irradiation process as an intermediate step in magnetic tunnel junction (MTJ) fabrication provides a test bed for optimizing the spin transport and understanding the role of spin scattering in the limit of ultra-thin tunnel barriers. At present, our research is establishing the benefits and limitations of the irradiation-based processing approach and the impacts on magnetic tunnel junction performance. Future work will focus on optimizing spin injection and

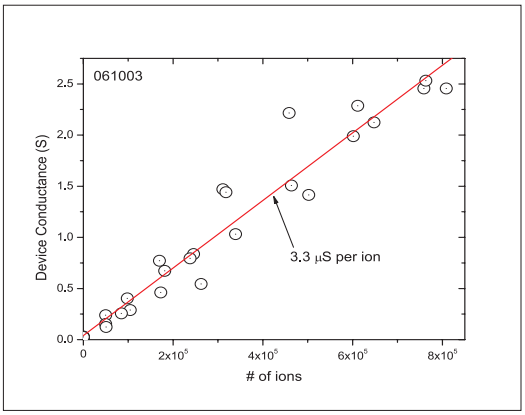

Figure 1. Ion-based tunnel barrier modification can adjust the electrical conductance of magnetic tunnel junction over a range spanning several orders of magnitude, providing an economical means of exploring the properties of tunnel barriers in the extreme limit of thin barriers.

accumulation through tunnel barriers and establishing cornerstones for absolute spin polarization measurements and broader spin metrology.

DELIVERABLES:

- Measure tunability of conductance via a range of different charge states – the increase in the tunnel junction conductance introduced by each ion is a discrete increment, and varying the charge state allows finer or coarser adjustment of the final device conductance. 1Q 2009
- Build new generation of oxygen plasma chamber – the tunability of the ion process, as well as the base tunnel junction reliability sensitively depends on the oxidation process. In the work to date, the oxygen plasma chamber processing has been the limiting factor on ultimate device performance. 3Q 2009
- Measure the TMR of devices modified with different charge states – prior measurements suggest that the magnetic properties of the MTJs should be insensitive to the charge state in the irradiation, and this is a direct test. 3Q 2009
- Eliminate "negative resistance" in test devices – a geometrical artifact manifesting in a negative resistance offset limits the measurement accuracy; methods for eliminating this artifact will be tested. 4Q 2009

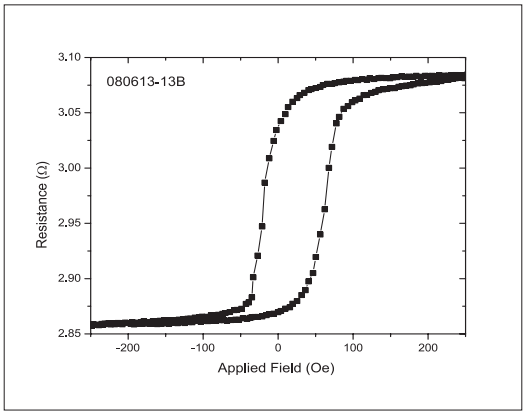

Figure 2. Magneto-resistance plot from a magnetic tunnel junction device whose resistance has been lowered with ion irradiation demonstrating that the ion process is capable of producing usable sensor devices.

Accomplishments

■ *Selectable resistance x area product spanning four orders of magnitude from a single process recipe* – An economical method for producing variable transparency tunnel junctions from a single tunnel barrier recipe is demonstrated in Fig. 1. The data in the figure correspond to a set of MTJ devices with a ≈ 1.0 nm tunnel barrier sandwiched between adjacent cobalt layers. Similar data has been taken for tunnel barriers at thicknesses ranging from 0.9 nm to 1.7 nm and for a range of different barrier stoichiometries. The compilation of these data shows that for a

single charge state, the conductance increases less for tunnel barriers with higher starting RA products. Different combinations of materials deposited, different thicknesses, magnetic behaviors, and exchange biases have been explored to establish the universal applicability of the process technique. Current voltage measurements and temperature dependence both indicate that the devices remain tunnel junctions after the irradiation (rather than metallic point contacts) and retain the high quality of the initial barrier. Accumulated data suggests that the reproducibility of the irradiation process is limited by the tunnel barrier preparation, rather than the ion adjustment, motivating the deployment of an improved plasma oxidation chamber (see deliverables).

■ *Magneto-resistance in conduction channels produced by ion irradiation measured* – The value of selectable RA product tunnel junctions is dramatically increased if they are useful as magnetic sensors. The data in Fig. 2 are taken on a device whose resistance is a factor of three lower than the base tunnel junction resistance but which still exhibits robust magneto-resistance. Exploration of the magneto-resistance for varying barrier properties indicates that for some tunnel barriers, the irradiation produces conductance channels that preserve spin polarization. Preservation of spin polarization appears to be related to the barrier material stoichiometry and

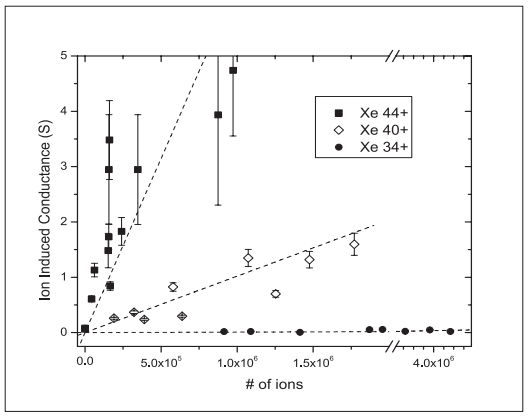

Figure 3. Different charge states result in different rates of tunnel junction conductance change. The lowest charge state is increasing the conductance, but much more slowly than the higher two charge states.

preparation methods. A detailed future study is expected to revisit this topic once the improved oxygen plasma chamber is operational.

■ *Tunability of conductance channels by variation of ion charge state measured* – While all the results demonstrated utilize highly charged ions, the role of the charge state provides an additional degree of freedom, and therefore additional control. Since the barrier reduction process relies on the ion's neutralization energy much more than on kinetic energy, the rate of change of the tunnel junction conductance depends strongly on the ion's charge state, as is shown in Fig. 3. Each of the three charge state shown have a robust and positive slope, but the values of the slopes depends exponentially on the charge state. The value of the slope is also synonymous with the increase in conductance contributed by each ion. For the range of charge states studied, the conductance added per ion spans a range of more than three orders of magnitude, from 1.5 nS/ion to 5 μS/ion. This range provides a great deal of control in selecting a final device resistance and provides important clues for understanding the fundamental processes of the barrier reduction and transport physics.

Collaborations

The work described here has benefited from interactions with many other NIST personnel, including N. Zimmerman, E. Tiesinga, J. Gillaspy, J. Tan, M. Stiles, J. Read, and W. Egelhoff.

An active and ongoing collaboration also exists with Prof. C. Sosolik of the Clemson University Department of Physics and Astronomy.

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BioElectronics Metrology

Technical Contacts:
D. R. Reyes
J. J. Kasianowicz
M. Gaitan

Goals

There is rapidly growing interest in the application of microelectronics and integrated circuit-based fabrication methods to manipulate and monitor biological processes. This emerging field of bioelectronics will require new competencies in the NIST laboratories to support metrology and standardization. Our goal is to develop an internal competency in this field and to establish links with industrial partners in order to position NIST to coordinate the development of a bioelectronics metrology roadmap. Towards this end, we are developing a versatile bioelectronic platform with integrated electronic and microfluidic components that will enable a broad range of quantitative cellular assays, ultimately at the single-cell level. We will characterize the performance of the platform and then use it to study single-cell response to various toxins. These measurement methods will also facilitate fundamental understanding of the behavior of heterogeneous cell populations and cellular interactions, and will enhance NIST's capabilities to address emerging measurement needs for the medical and pharmaceutical industries. This effort will result in new metrology tools and test methods to support growing commercial industries that use high throughput methods for determining drug efficacy and toxicity.

Customer Needs

There is rapidly growing interest in the application of microelectronics and integrated circuit-based fabrication methods to manipulate and monitor biological processes. This emerging field of bioelectronics will require new competencies in the NIST laboratories to support metrology and standardization. Our goal is to develop an internal competency in this field and to establish links with industrial partners in order to position NIST to coordinate the development of a bioelectronics metrology roadmap. Towards this end, we are developing a versatile bioelectronic platform with integrated electronic and microfluidic components that will enable a broad range of quantitative cellular assays, ultimately at the single-cell level. We will characterize the performance of the platform and then use it to study single-cell response to various toxins. These measurement methods will also facilitate fundamental understanding of the behavior of heterogeneous cell populations and cellular interactions, and will enhance NIST's capabilities to address emerging measurement needs for the medical and pharmaceutical industries. This effort will result in new metrology tools and test methods to support growing commercial industries that use high throughput methods for determining drug efficacy and toxicity.

Technical Strategy

Recent scientific reports describe the ability to stimulate electronically and probe single cell activity and to transport, sort, and position single cells. These capabilities have resulted in significant advances in biological sciences and medicine. An excellent example is patch clamp technology that has revolutionized the field of electrophysiology. Advances in microfabrication methods have recently led to the development of patch clamp arrays and other automated on-chip techniques; however, the widespread adoption of more complex integrated systems for biologically relevant measurements continues to face technological hurdles. These include complicated materials integration issues (maintaining a biocompatible environment for cells within the in-vitro measurement systems, developing stable and drift-free electrodes for accurate measurements, in varied buffer solutions, etc.), the difficulty of accurately determining the electrical/electromagnetic response of integrated electronic/MEMS/fluidic systems, and issues related to reproducible fabrication of integrated devices. By addressing these critical measurement infrastructure needs, NIST will accelerate the development of powerful new bioelectronic platforms and techniques.

Our technical approach is to integrate microelectronic, MEMS, and microfluidic systems with cells in order to achieve a new level of control over the electronic/biological interfaces under study. We will develop methods to adhere and grow cells in defined patterns in a biological hybrid in-vitro environment that incorporates microelectronic circuits, both electrochemical and RF, to stimulate and sense cell activity. Microchannel networks will be used to transport the biological specimens to exact locations and to deliver precise amounts of chemicals or drugs to the local cellular environment. These techniques will allow us to apply

precise electrical, electromagnetic, and chemical stimulation to the cells and to measure their metabolic, electrical, and physiological responses. We focused our initial research efforts on the study of retinal (neuronal) cells, and currently, we are working with other mammalian cells such as fibroblasts (NIH-3T3), epithelial cells, and sperm cells.

DELIVERABLES:

- Design and fabricate indium-tin oxide (ITO) electrodes for morphogen gradient studies with dielectrophoretic (DEP) manipulation of cell location. 4Q 2009
- Develop electronic measurement tools and devices for use in microfluidic devices to manipulate, induce and assess changes at the cellular level. 1Q 2010
- Develop monolithic microfluidic devices with integrated microwave transmission lines and carry out measurements required to demonstrate one or more of these: on-chip cell lysis, standing temperature wave generation, or Beer's law attenuation. 3Q 2010
- DEP electrodes. 2Q 2010

Accomplishments

We developed a method to monitor NIH-3T3 fibroblast cell growth on gold electrodes using impedance spectroscopy. In this measurement technique, individual cells are represented as resistive and capacitive elements, which increase the impedance of the system as the number of cells increase. The two-electrode system was fabricated using photolithographic techniques and is comprised of thin-film gold electrodes with an underlying TiW adhesion layer. The system was then passivated with an oxide layer, which was etched through to define and expose the electrode active areas. Fibroblast cells (NIH-3T3) were able to grow directly onto the gold surface, and as they adhered and multiplied, the impedance of the system increased. Cells preferentially grew on the bare gold surface and not on the oxide. However, the oxide surface can be rendered biocompatible with the use of polyelectrolyte multilayers (PEMs), leading to successful measurements of cell growth with impedance spectroscopy (Fig. 1). Thus, the fabricated cell confluence detector demonstrates the ability to monitor cell adhesion and growth with impedance measurements. Future work will focus on the use of this system to monitor cytotoxic effects, of a variety of chemicals, using impedance spectroscopy to detect cell detachment from the surface.

We designed and fabricated a microchip, which enables us to study the metrology problems associated with pH determination within planar microfluidic networks, e.g. Lab-on-a-Chip (LOC) systems. The work was motivated by the realization that LOC systems might enjoy more widespread commercialization if reliable and accurate electronic chemical sensors are more closely integrated with the microfluidic networks. The chip comprised is 1) of an ion-sensitive field-effect transistor (ISFET) fabricated on a silicon substrate, 2) an on-chip Ag/AgCl quasi-reference electrode (RE), and 3) a microfluidic network molded in the transparent elastomer, poly(dimethylsiloxane) (PDMS) (Fig. 2). Thus, both ion-sensitive field-effect transistor (ISFET)-based and fluorescence intensity (FI)-based pH measurements were conducted simultaneously with the chip. Since two independent pH measurements are used on the same device, the mH+ chip can be used to quantitate the accuracy and precision of microfluidic pH determinations. The utility of the chip was demonstrated with comparisons of the dynamic range and flow rate dependence of the ISFET-based and FI-based pH measurements. Additionally, ISFET-based measurements clearly resolved step changes in pH as small as 0.26 pH unit in flowing solution. Sample plugs of less than 100 microliters were needed for the measurements.

A method for fabricating Ag/AgCl planar microelectrodes for microfluidic applications is presented. Micro-reference electrodes enable accurate potentiometric measurements with min-

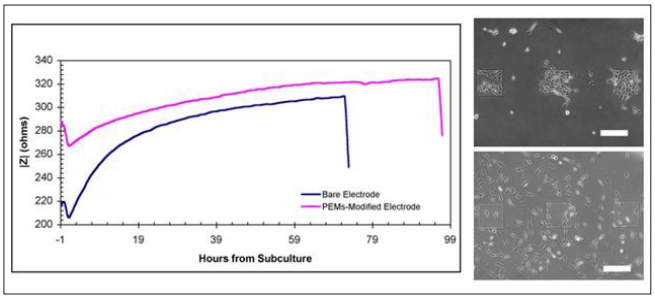

Figure 1. Magnitude of impedance of NIH-3T3 fibroblast cell growth on unmodified (blue line) and EMs-modified devices (red line) at 1000 Hz. The sharp decrease in impedance observed in both curves denote the detachment of NIH-3T3 fibroblast cells from the electrode surface after trypsin addition. (Right panel) NIH-3T3 fibroblast cells growing on unmodified gold electrodes (top) and PEMs-modified electrodes (bottom).

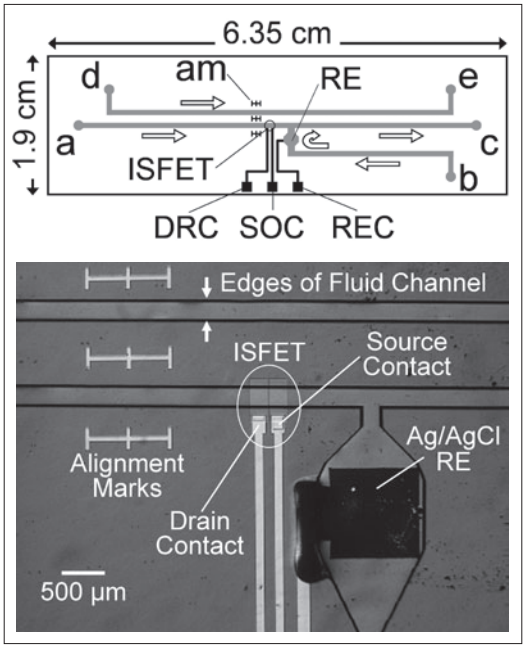

Figure 2. Schematic of mH+ layout. Overall chip dimensions are as indicated; however, other features are not shown to scale. The gray lines indicate flow channels molded into PDMS, 280 µm wide by 50 µm high. Arrows indicate the direction of fluid flow. a) test solution inlet, b) reference solution inlet, c) main outlet, d) blank inlet, e) blank outlet, am) alignment mark, RE) on-chip Ag/AgCl quasi-reference electrode, REC) reference electrode contact, DRC) electrical contact to ISFET drain, SOC) electrical contact to ISFET source. (Bottom panel) Photograph of sensing region of the mH+ device, scale as indicated. The ISFET is visible near the center of the figure, while the Ag/AgCl quasi-reference electrode appears in the lower right portion of the figure. Alignment marks and electrical contacts to the ISFET and reference electrode are made of gold.

iaturized chemical sensors, but such electrodes often exhibit very limited lifetimes. Our goal is to construct Ag/AgCl microelectrodes reliably with improved potential stability that are compatible with surface mounted microfluidic channels. Electrodes with geometric surface areas greater than or equal to 100 square micrometers were fabricated individually and in an array format by electroplating silver, greater than one micrometer thickness, onto photolithographically patterned thin-film metal electrodes (Fig. 3, left panel). The surface of the electroplated silver was chemically oxidized to silver chloride to form Ag/AgCl microreference electrodes. Characterization results showed that Ag/AgCl microelectrodes produced by this fabrication method exhibit increased stability compared with many devices previously reported. Electrochemical impedance spectroscopy allowed device specific parameters to be extracted from an equivalent circuit model, and these parameters were used to describe the performance of the microelectrodes in a microfluidic channel. Thus, stable Ag/AgCl microelectrodes, fabricated with a combination of photolithographic techniques and electroplating, were demonstrated to have utility for electrochemical analysis within microfluidic systems.

Rapid temperature cycling of fluids is essential for increasing the throughput of chemical and biochemical processes and chemical synthesis such as polymerase chain reaction (PCR). In micro total analysis systems (µTAS), temperature cycling is typically implemented by external heating blocks or by integrated microresistive heating elements (microreactors). Our new approach for temperature cycling of microfluidic systems is based on delivering microwave heating energy using a microwave transmission line. A microwave coplanar waveguide is integrated with a surface mounted elastomeric microfluidic channel (Fig. 3, right panel). This approach will have application to microwave assisted chemistries, which have recently been shown (in macro-scale devices) to have several advantages over conventional resistive heating approaches. These advantages include the ability to deliver heat directly to the fluid (and not to the surrounding medium), requiring lower temperatures to implement a chemical reaction and exhibition of more uniform heating profiles. Recently, we have demonstrated, in a different microchip format, the use of microwave heating for the amplification of human DNA

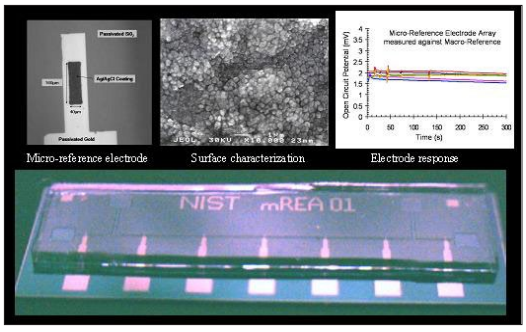

Figure 3. Photographs (left panel) of the NIST micro reference electrode array (mREA) and close-up photo of an Ag/AgCl planar microelectrode, surface, and test. The right panel is a drawing of a fluidic microwave heating assembly showing a gold coplanar transmission line patterned on glass with a poly(dimethylsiloxane) microchannel bonded over it.

(PCR). We are currently working towards the integration of other processes, such as cell lysis and DNA extraction, into a microfluidic system.

We have integrated electrodes within microfluidic devices to carry out a.c. dielectrophoresis. In this trapping technique, electric fields polarize cells inducing electrostatic forces, which trap the cells against the electrode edges. We have been able to trap cells suspended from bulk cultures within microchannels when flowed past integrated, energized electrodes. We have observed that more than 85 % of cells passing the electrodes were trapped. On the other hand, when electrodes were deactivated, about 70 % of the cells were subsequently detached by solution flow. Deposition of PEMs on the electrodes renders an adhesion layer to further cell attachment. Trapping experiments carried out after PEMs were deposited over the electrodes showed that all immobilized cells remained adherent after the electrodes were deactivated. We have been using a.c. dielectrophoresis to array cells within a microfluidic channel perpendicular to flow.

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System Design and Test Metrology Program

Lead counts of several thousand per chip and test frequencies in the microwave regime challenge current test methodologies. The addition of new functions to provide system on-chip solution poses additional testing challenges. The overall task is to develop test methodologies to address these new requirements.

Accurate at-speed test methodology of digital integrated circuits is a critical requirement. Traditional methods utilizing integrated circuit (IC) contact probing technology requires large contact pads incompatible with current IC designs. The development of alternative probing approaches through non-contact and intermittent probing techniques appear very promising. However, to implement these techniques, solving the at-speed test calibration issues is crucial. With the challenges facing designers and the rising costs of development, it is essential to develop accurate testing strategies.

Temperature Sensor Metrology And BIST

Technical Contacts:
M. Y. Afridi
J. Geist

"For this technology (microhotplate-based gas-sensor) to be successful, temperature control is of the highest importance."

Charles J. Taylor

Goals

The purpose of this project is to develop metrology needed for microhotplate temperature sensors that are compatible with standard CMOS technologies and also provide an interface for on-chip built-in self test (BIST) for applications requiring microhotplate integrity check and self calibration. Polysilicon or aluminum layers which are readily available in standard CMOS technologies are not suitable for long-term reliable temperature measurements due to drift in Temperature Coefficient of Resistance (TCR) value at high temperatures (250 - 400 ºC). On the other hand, platinum thin film temperature sensors, which are not available in standard CMOS technologies, exhibit excellent stability over a wide temperature range, -200 to 650 ºC. There is a need to develop new post-processing steps to integrate platinum based temperature sensors into a standard CMOS microhotplate to measure microhotplate temperature, to demonstrate that the resulting temperature sensors are sufficiently stable to be accurately calibrated, and to adapt them to BIST.

Customer Needs

The customer will be any organization that requires accurate microhotplate temperatures above 250 ºC. For instance, accurate microhotplate temperature measurements are crucial for the discrimination and quantification of gas species by low-cost, microhotplate-based, metal-oxide gas sensors. The fabrication and calibration methods developed as a result of this work will be essential for the realization of many homeland security and military objectives.

Professor Charles J. Taylor of Pomona College said:

"Molecular chemisorption and chemical reactions taking place on the gas-sensor surface change the electrical properties of the sensing film, thus providing an opportunity to identify an analyte and to determine its concentration. Since chemisorption and surface reactions are temperature dependent, it is possible to tune sensor selectivity and sensitivity by controlling operating temperature. Furthermore, using temperature-programmed sensing, it is possible to identify analytes based on matching data acquired at multiple temperatures to "molecular fingerprints". Without good temperature control, the matches may be ambiguous and the identity of the analyte may be lost. In addition, any studies performed where temperature is a variable in the experiment such as the deposition of materials by chemical vapor deposition onto the microhotplates, would be more difficult to reproduce without adequate temperature control."

Technical Strategy

To achieve the project goals, CMOS compatible post processing techniques will be developed to integrate different platinum based temperature sensors including resistive and platinum-rhodium thermocouples into the microhotplate structures. Also microhotplate BIST and calibration procedures will be developed and tested.

1. A series of standard CMOS microhotplates with integrated platinum temperature sensors will be developed and tested. The Microhotplate design will be compatible with BIST operation. The micro-hotplates will be fabricated in 1.5 μm CMOS technology through the MOSIS-AMI foundry service, post-processed in the NIST Nano-Fabrication facility, and calibrated and characterized in the EEEL SED Gas Sensor Characterization laboratory

DELIVERABLES:

- CMOS microhotplate test structures with integrated platinum-based temperature sensors. 4Q 2008

2. To develop and test BIST procedures for microhotplate integrity test and temperature calibrations.

DELIVERABLES:

- A report describing BIST performance and calibrations results for the microhotplate temperature sensors. 2Q 2009

3. An enhanced microhotplate characterization laboratory will be setup and configured to test and calibrate microhotplate temperature sensors and to measure BIST performance.

DELIVERABLES:

- A well equipped and automated laboratory setup for microhotplate characterization. 4Q 2009

4. Design analog and digital circuits to integrate control, measure, and BIST functionality for the microhotplate platform.

DELIVERABLES:

- Integrated microhotplate test structures with on-chip digital and analog electronics to control, measure, and perform BIST functionality test. 4Q 2010

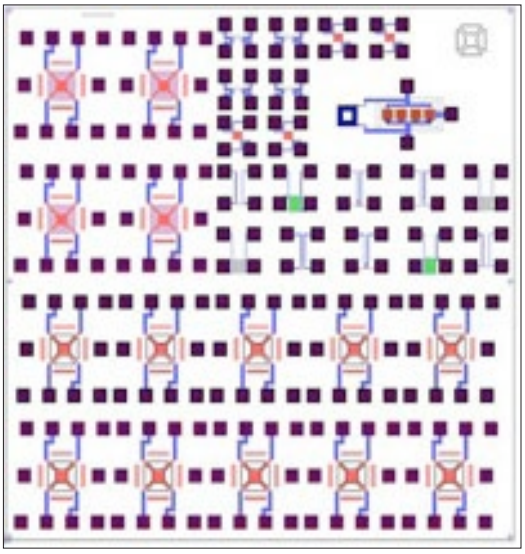

Figure 1. Layout of test structures for testing complementary approaches to microhotplate temperature sensor Built-In Self Test (BIST).

Accomplishments

■ A test chip was designed and submitted to be fabricated in a standard 1.5 micron CMOS technology. The chip includes complementary temperature sensor designs to be evaluated for their performance, stability, and BIST functionality.

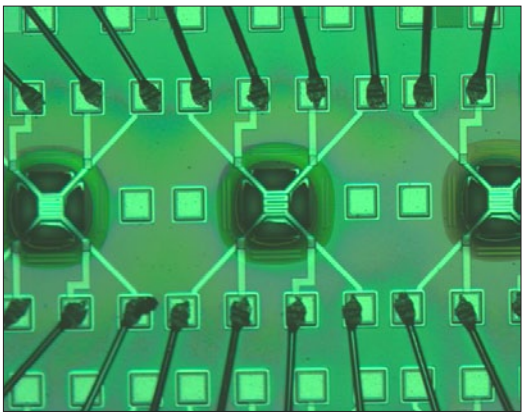

Figure 2. A micrograph of a wire-bonded chip showing different serpentine platinum resistive temperature sensors over microhotplate structures.

■ CMOS microhotplate test structures chips were fabricated, post-processed, and tested for design integrity. The microhotplates were further post processed to integrate different serpentine design patterns to produce platinum resistive temperature sensors.

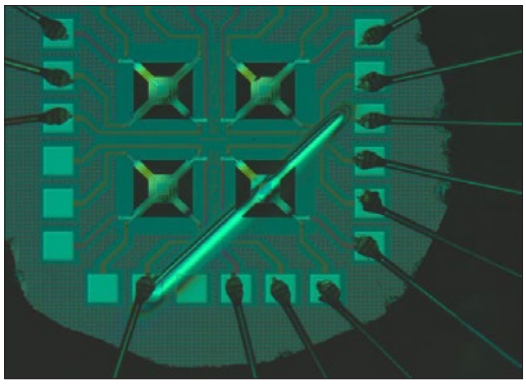

Figure 3. A micrograph of a platinum/rhodium-base thermocouple chip.

Publications

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At-Speed Test of Digital Integrated Circuits

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P. Hale

"As electronic devices shrink into the nano-meter size scales and integrated circuits operate at multi-GHz clock rates, probing their internal characteristics is becoming both more critical and far more difficult than ever before."

Travis M. Eiles, Ph.D.
Intel Corp.

Goals

Develop and demonstrate metrology for the at-speed test of digital integrated circuits. The program will resolve the essential metrology issues of at-speed digital integrated circuit test. It will apply its results to characterizing and calibrating high-impedance probes and developing broadband scanning probe microscopes (SPMs) capable of precisely positioning field probes above the surface of the integrated circuit.

Customer Needs

In the device debug and characterization world, a key challenge is the development of diagnostic tools, particularly for timing information. The 2007 ITRS Metrology section points out that "Metrology was the first semiconductor technology area to work routinely in the area of nanoelectronics. This is because a variation in features size one tenth of the nominal dimension often results in significant changes in device properties." The roadmap continues "As device dimensions shrink, the challenge for physical metrology will be to keep pace with inline electrical testing that provides critical electrical performance data." Interconnects continue to be an important aspect of the increasing density and smaller sizes of ICs. The 2007 roadmap continues "Interconnects, including all of the IC structures necessary to connect from silicon to the boards and boxes of the outside world, have become a potential performance roadblock for the continuation of the semiconductor industry on the Moore's Law curve."

With the increasing reduction in feature (and defect) sizes well below optical wavelengths, rapidly increasing failure analysis throughput times, reduction in failure analysis efficiency, and approaching practical physical limits to other physical techniques (pica, laser probes), the industry is reaching a strategic inflection point for the semiconductor business where the criticality of design for test and test enabled diagnostics and yield learning becomes paramount (2007 ITRS Test and Test Equipment Section, page 5-6). Detecting systemic defects is one of the difficult challenges. Electrical test-based diagnostics and learning is becoming increasingly more important. Parametric related feedback is needed for: (1) device and interconnect parameters; and (2) design-process interactions. To keep pace, improvements and breakthroughs in existing tools/techniques is necessary. In-chamber (SEM) and atomic-force-microscope probing at the nanoscale are required to characterize minimum-sized transistors (4 probe points) and SRAM cells (5 or more points) at first contact level are required for circuit probing. The socket and wafer probe are also serious bandwidth bottlenecks for multi-gigahertz testing and additional R&D is needed in these areas. For key challenges the research and development is urgently required to bring to the market cost-effective probe technologies directed at trends in product offerings and the testing environment. One of the challenges is that the traditional probe technologies do not have the necessary electrical bandwidth for higher frequency devices. At the top end are RF devices, requiring up to 40 GHz.

The critical topics in 2007 ITRS Metrology section are: the microscopy; critical dimension (CD) and overlay; film thickness and profile; materials and contamination analysis; dopant profile; in-situ sensors and cluster stations for process control; reference materials; correlation of physical and electrical measurements; and packaging. We are focusing our metrology methods on development of tools for materials characterization, control of interfacial layers, dopant positions, defects, and atomic concentrations relative to device dimensions. We are developing alternative scanning probing approaches that use high-impedance probes, non-contact probes, atomic-force and scanning tunneling microscopes that respond to either electric or magnetic fields near transmission lines in the circuits. However, while the uncalibrated field measurements performed by these probing systems are suitable for field mapping, they are a far cry from the precise measurements of voltages and currents required for electrical design.

Solving the critical at-speed test calibration issues will add enormous value to the probing systems currently being used or developed for high-performance digital integrated circuits. Developing characterization and calibration methods for high-impedance probes, whether of the conventional type or mounted on atomic-force

microscopes, will help speed the development and implementation of these new measurement tools, and so create a new paradigm for the at-speed test of high-speed digital integrated circuits.

Technical Strategy

We will develop calibration artifacts with precisely known high-frequency voltages and circuits suitable for characterizing and calibrating high-impedance probes and samplers of all types. We will focus on fundamental calibration issues: transforming the response of the probes to the electric and magnetic fields above the integrated circuit into accurate voltages and currents inside the circuit. Figure 1 shows a result of the high-speed metrology we have developed, an on-chip waveform measurement to 200 GHz.

We will first apply the characterization and calibration procedures to conventional high-impedance probes. To facilitate the development and test of electric and magnetic probes with nanoscale resolution, we have constructed a universal SPM test bed for these probes. We are applying our characterization procedures to miniature SPM probes suspended on custom cantilevers designed for high frequency measurements on the nanoscale. Finally, we plan to tie our metrology back to fully characterized electro-optic sampling measurements.

After calibration and correction, the measurement has an improved fidelity and is traceable to fundamental physical principles. Traceability for frequency response is provided to 110 GHz in coaxial transmission media and beyond on wafer through the NIST electro-optic sampling system. The 2007 ITRS roadmap points to the following three key test and measurement drivers:

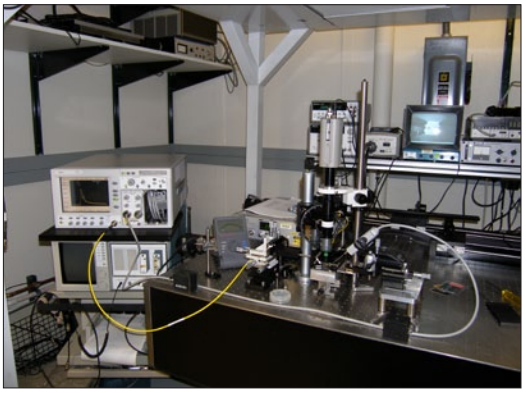

Figure 1. Three on-chip waveform measurements performed with our electro-optic sampling system.

- Increasing device interface bandwidth (# of signals and data rates)
- Increasing device integration (SoC, SiP, MCP, 3D packaging)
- Integration of emerging and non-digital CMOS technologies Our calibration strategy is independent of the particular signals being measured and is applicable to digital, RF/microwave, and mixed signal systems, enabling the single platform measurement solutions called for in the first two of these three key drivers identified in the 2007 ITRS roadmap.

DELIVERABLES:

- Set up system and calculate known calibration waveforms with different impedance terminations. 4Q 2008
- Develop calibration structures and procedures for broadband atomic force microscope 4Q 2009

Accomplishments

- We have demonstrated a novel frequency-domain method for measuring time-domain delay of dispersive calibration artifacts for differential delay. This frequency-domain approach can also account for pulse shape and source and load impedance effects. We have also demonstrated a method to propagate uncertainty in the NIST Timebase Calibration Software through to various pulse parameters and have demonstrated differential delay calibrations of a dispersive calibration artifact with < 1 ps standard uncertainty.
- We have developed, fabricated, and tested a noninvasive AFM scanning probe for measuring local microwave power.
- We have developed a method of characterizing and calibrating conventional high-impedance probes for low-invasive waveform measurements.
- We have applied our high-impedance-probe characterization method to a probe mounted on an atomic-force microscope.
- We have constructed an SPM universal test bed.
- We have demonstrated a calibrated measurement of an on-wafer pulsed waveform up to 200 GHz using electro-optic sampling.

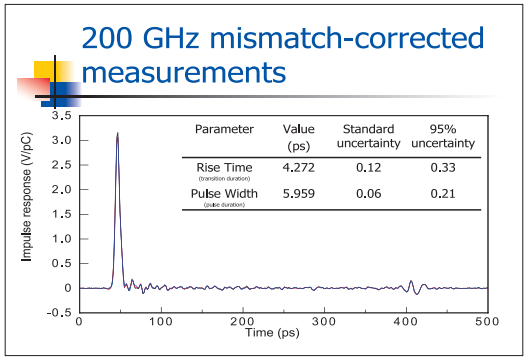

Figure 2. Measurement system used to verify the functionality of our photoconductive switches.

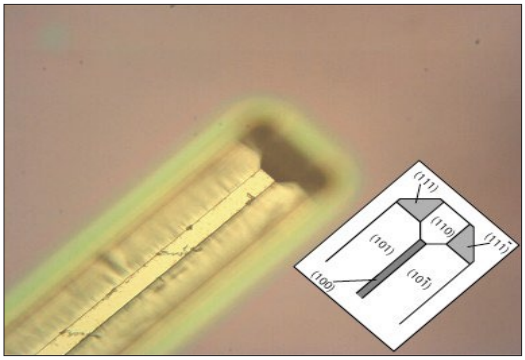

Figure 3. The Fiber-optic trench with integrated 45-degree mirror.

■ We have developed a procedure for testing high-impedance probes directly on our electrooptic sampling system. This system has a calibrated bandwidth of 200 GHz.

■ We have demonstrated a method for correcting oscilloscope time-base jitter, drift, and distortion.

■ We have fabricated fast photoconductive switches and demonstrated a rise time of better than 5 ps, largely exceeding our goal of constructing generator chips useable to 50 GHz. We will use these to construct a portable and calibrateable on-chip pulse source for characterizing high-impedance probes at the micrometer and nanometer length scales, Fig. 2.

■ We developed the fabrication process for creating the MEMS chips with integrated 45-degree mirrors and trenches for fiber alignment, Fig. 3.

■ We assembled the fiber optic interferometer for the measurement of the deflection of the cantilevers including the thermal feedback control.

■ We built a magneto-optic Kerr effect setup for imaging of current distributions in microwave circuits.

■ We modified a commercial AFM for measurement of mechanical resonances of micro/nano oscillators.

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Thermal Measurements and Packaging Reliability

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B. Grummel
N. Yang

Goals

Our goal is to provide the semiconductor industry with information, guidance, and tools necessary to characterize and model the behavior of features and interfaces in packaging and on-chip that are thermally stressed. Advanced temperature measurement methods are developed and transferred to industry to meet the need to characterize semiconductor device and package temperature with increased temporal and spatial resolution. Electro-thermal models and modeling methodologies are also developed and transferred to industry to meet the increased need to model the interaction of electrical and thermal behavior of the device and package.

Overcoming thermal limitations has recently become a major issue in CMOS-based microelectronic circuits because: (1) power levels in CPUs have reached the same levels as in power devices; (2) power density nonuniformities are leading to hot spots in microprocessors as well as power ICs; (3) new materials with different thermal properties are being introduced; (4) many new and future technologies (e.g., SOI, 3-D integration) tend to isolate power dissipating elements thermally; and (5) shrinking dimensions and increasing frequency of ICs are causing significant power dissipation in the interconnects. To address these issues, reliable methods for measuring and modeling the temperature distribution in ICs and power devices are required.

A broad range of temperature measurement techniques are investigated by this project and several unique temperature measurement system requirements have been identified and demonstrated by NIST. High speed transient thermal imaging methods are being developed for measuring localized heating effects at the semiconductor chip surface. This enables the measurement of transient heating events such as burst operation of IC Functional Unit Blocks (FUBs) and enables the measurement of transient current constriction failure events in RF and high power devices. This thermal imaging methodology can serve as a basis for measurement standards. Additionally, methods are being developed to evaluate the heat transfer across package layer interfaces using high-speed temperature sensitive parameter (TSP) measurements. This is important for in situ measurement of heat transfer performance degradation after various levels of thermal stress such as power cycling, thermal cycling and thermal shock.

Customer Needs

The trend in electronics is toward components of higher density and smaller size using less expensive materials. Materials used in packaging and interconnects are many and display a variety of thermal responses that are not always compatible. This makes interconnect lines and package interfaces particularly vulnerable to thermomechanical fatigue failures. This project seeks to offer support through modeling and verification of the thermal performance of devices and packages and the development of new thermal measurement methods to meet the need of the semiconductor industry.

Temperature measurements for microelectronic devices are more important today than they ever have been. It always has been true that extreme temperature places limits on the operating range of nearly all devices, but today, increasing power dissipation and power densities threaten to create temperatures that block continued progress according to “Moore’s Law.” Clearly, new and innovative methods for cooling chips and packages must be found along with new materials and circuit designs, and architectures for decreasing the power dissipation and operating temperature. Equally as clear, we must have accurate and well-understood methods for measuring the temperature of devices to aid in the development of these new techniques and materials.

The need to measure operating temperature of a semiconductor device can be divided into the following four broad categories: (1) predicting reliability or operating life of device, (2) measuring material/device thermal properties in situ, (3) confirming or determining the operating limits or thermal performance of a device, and (4) validating thermal models for device, chip, and system performance. Thermal measurements on small, <10 μm, structures are needed due to the high density of current and future interconnect and packaging designs. Heat transfer informa-

tion at interfaces, such as those seen at solder/intermetallic interfaces and Direct Bonded Copper (DBC) isolation layer is needed for modeling of future package designs.

Measurement of localized and transient heating is also becoming increasingly important in high performance ICs as it is becoming prohibitive to remove the heat that would be dissipated if the entire IC was operated continuously at the full power density level. System techniques that dynamically operate all or part of the chip at reduced power, such as dynamic voltage scaling or clock gating, require experimental evaluation of the rapid transient heating and thermal diffusion from locally heated FUBs.

The 2008 ITRS Design Challenge, Crosscutting Challenges #4, p. 17 states that: "Issues include…thermal impact on device off-currents and interconnect resistivities, and substrate coupling. A basic DT challenge is to improve characterization, modeling, analysis… at all levels of design."

The 2008 ITRS Design Challenge, Crosscutting Challenges #5-(3), p. 17 states that: "In general, automatic insertion of robustness into the design will become a priority as systems become too large to be functionally tested at manufacturing exit."

As the power density of semiconductor devices continues to rise, modeling the interaction of electrical and thermal behavior of the device and package also increases in importance.

The 2008 ITRS Table AP1, for Assembly and Packaging, p. 46 states that: "High current density packages… must be addressed through materials changes together with thermal/mechanical reliability modeling".

Modeling transient heating effects has also become much more important in predicting the thermal cycling effect on reliability and in understanding the impact of dynamic power dissipation within devices.

The 2008 ITRS Design Challenge, Crosscutting Challenges #2-(2), p. 16 states that: "Increasing power densities worsen thermal impact on reliability and performance…"

NIST first introduced the concept of dynamic electro-thermal semiconductor models and package thermal network component models in the early 1990s to address this need and this methodology has been used extensively by industry to model the behavior of a variety of semiconductor devices and packages.

The 2008 ITRS Table AP1, for Assembly and Packaging, p. 45 states that: "Coordinated design tools and simulators to address chip, package, and substrate co-design (need) integrated analysis tools for transient thermal analysis and integrated thermal mechanical analysis."

The 2008 ITRS Modeling and Simulation, p. 55 states that: "Concerning the Modeling and Simulation of Difficult Challenges, the most important changes in 2008 have been the new items … 'Thermal modeling for 3D ICs and assessment of modeling tools capable of supporting 3D designs.' … added to the short-term challenges 'Thermal-mechanical-electrical modeling for interconnections and packaging.' "

The 2008 ITRS Interconnect Table INTC1, for Reliability, p. 39 states that: "Improved failure detection techniques, testing methodologies, modeling, and identification of potentially new failure mechanisms will be required."

Technical Strategy

1. NIST has developed a method to enhance commercial IR thermal microscopes enabling much higher speed transient thermal imaging. This system enables validation of electro-thermal device models needed for electrical and thermal system design.

DELIVERABLES:

- Manufacture new test fixture plates to accommodate various IC and power device packages in order to provide electrical isolation from the system attached hotplate. These fixtures allow the use of an additional thermocouple that can be read by an external temperature controller. 2Q 2009

2. Performance evaluation of the NIST-developed high-speed transient thermal imaging system is required to characterize both the IR microscope's transient detector temporal resolution and spatial resolution (including the use of different lenses) to provide accurate high-speed thermal transient mapping measurements for a wide range of semiconductor power device and package module materials.

DELIVERABLES :

- Determine calibration curves parameters of the transient thermal imaging system for different emissivity samples by performing measurements on a matrix of samples including different surface materials and surface textures. Perform spatial scans to determine spatial resolution of transient detectors and lenses. Investigate other IR lenses and or transient detector systems options to enable higher spatial resolution for NIST high speed transient thermal imaging system. 4Q 2009

3. Transient thermal measurement technique standards are strongly needed for the semiconductor electronics industry. Based on NIST-developed transient thermal calibration test structures (1 μs temporal resolution), micro-hotplate structures may be developed to verify temporal resolution and accuracy of the NIST-developed high-speed transient thermal imaging system in order to provide calibration tools that can be used by the semiconductor electronics industry.

DELIVERABLES:

- Develop and apply improved MEMS-based micro-hotplate structures to verify temporal resolution and accuracy of the NIST high-speed transient thermal imaging system, including fabrication and post process transient micro hotplate structures with integrated thermometers. 4Q 2009
- Identify and apply suitable hotplate surface coatings to control emissivity and limit transparency while also minimizing the coating thickness. 4Q 2009
- Calibrate internal micro-hotplate thermometers using a computer-controlled external heat source. Generate thermal microscope calibration curve using the micro-hotplate internal heater and thermometer controlled by the high speed transient thermal microscope calibration routine. 4Q 2009
- Apply the calibrated micro-hotplate device to determine the response of the transient thermal imaging system to sub 10 μs heating pulses. 4Q 2009

4. NIST-developed thermal measurement tools include the high-speed transient thermal imaging system, high-speed temperature sensitive parameter system, and thermal cycling stress system. These systems are essential to establish electro-thermal performance needed for optimal device design. Thus these thermal measurements are required to address critical technology challenges.

DELIVERABLES:

- Characterize current uniformity of pulsed power devices delivering a 20 MW /cm^2 pulse discharge for 1 ms, using the NIST high-speed transient thermal imaging system. Determine thermal gradients within IC test structures with through-chip contacts during function block heating. 4Q 2009
- Perform kilowatt-level power cycling stress experiments with dynamic thermal resistance monitoring to address critical technology challenges. For example: die voiding for multi-shot pulse power thyristors, high temperature packages, and through chip contacts die attach voiding, high temperature package die attach voiding. 4Q 2009

5. Evaluation of the dynamic electro-thermal behavior is required to establish critical design parameters for semiconductor packages. NIST has been developing dynamic electro-thermal models of semiconductor packages to provide a better understanding of the interaction of the electrical system with the thermal management system for semiconductor devices and modules. These dynamic electro-thermal models are validated using NIST acquired experimental data.

DELIVERABLES:

- Develop thermal network component model for multi-chip power device modules including lateral thermal coupling between die at the DBC and baseplate levels and an integrated high-heat-flux liquid cooled heatsink. 3Q 2009
- Perform steady-state infrared thermal imaging, transient infrared thermal measurements, and transient temperature sensitive parameter measurements to validate multi-chip power device package models for a wide range of power heating. 4Q 2009
- Develop electro-thermal models for the ultra high electrical and thermal efficiency modules for electric vehicle propulsion inverters cooled with high temperature engine coolant. 4Q 2009
- Develop unique high temperature semiconductor package assembly process and metrology to evaluate cooling and reliability performance of these advanced high temperature packages. 4Q 2009

Accomplishments

■ Development of the new high-speed (1 μs) transient thermal imaging system using the InfraScope II system was completed. The acquisition and data analysis capabilities of this system have been extended to allow the system to use the same thermal imaging procedure to determine emissivity calibration curves for different materials and surface textures. The new InfraScope II system hardware was purchased and adapted for the NIST high-speed transient thermal imaging method. The new system provides much faster acquisition performance than the previous CompuTherm III system.

■ As low-degradation rate SiC PiN (power diode made with p-type to intrinsic to n-type semiconductor junctions) diodes are beginning to emerge, the NIST transient thermal imaging

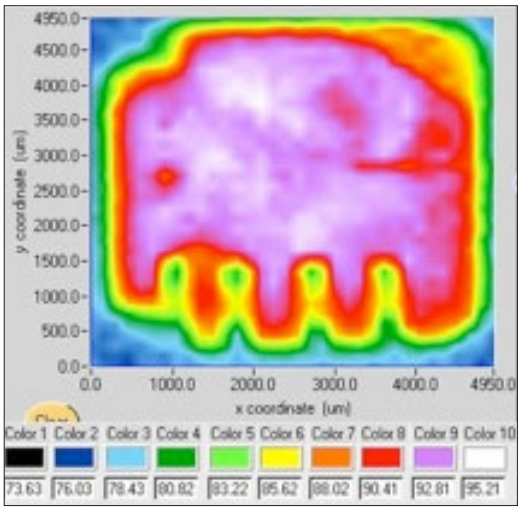

Figure 1a

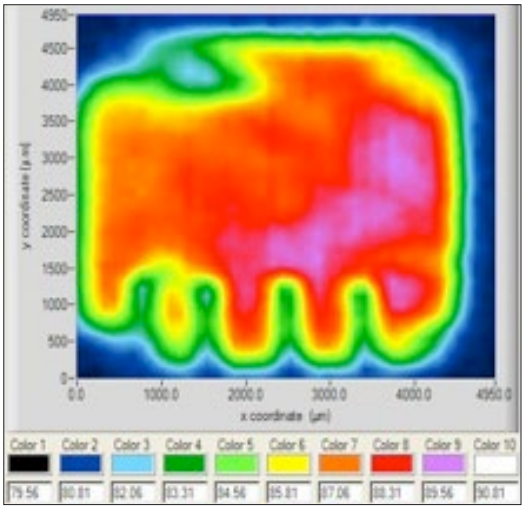

Figure 1b

Figures 1a and 1b. SiC diode relative temperature uniformity map comparison between the previous modified CompuTherm III system (left) and the new modified InfraScope II system results (right). The previous system image was generated using a 34 x 34 matrix of samples, while the new system image was generated with a 46 x 46 matrix during a preliminary measurement made to verify that the performance of the new system replicates the same functionality as the previous one. The new system has much faster measurement speed and thus can produce a higher resolution image in the same amount of time.

system is being used to determine the current uniformity after various levels of stress up to several thousand hours of operation. Figures 1a and 1b are current uniformity images of a SiC 10 kV, 20 A PiN diode obtained from thermal movies for a fast high current pulse. These images are after operation at full rated current for 4000 hours in Figure 1a and after 6000 hours for Figure 1b. The temperature map shown in Fig. 1a demonstrates good current uniformity at 4000 hours while Figure 1b demonstrates some degradation in the upper left hand corner at 6000 hours.

NIST has evaluated the current uniformity degradation of numerous SiC PiN diode samples from 2005 through 2009, providing essential information resulting in the development of "degradation free" SiC power device technology. The long-term degradation process has been extended to measure SiC JBS diodes that emerged after the SiC PiN diodes with better high-power, high-frequency electrical characteristics.

■ NIST had previously developed an "in situ" method to measure the high-speed heating response of Insulated Gate Bipolar Transistors (IGBTs) packaged in high power modules. The method uses the gate-source voltage, Vgs, at a constant, relatively low current and at a high anode-cathode voltage as the temperature sensitive parameter (TSP). This TSP method is used to validate and extract short-time constant thermal parameters for an electro-thermal simulation model of the IGBT (including the details of the package module). The high-speed TSP method was applied to compare heating response measurements with the thermal models for a commercial high power IGBT half-bridge module, a commercial six-pack IGBT module, and a prototype NSF Center for Power Electronic

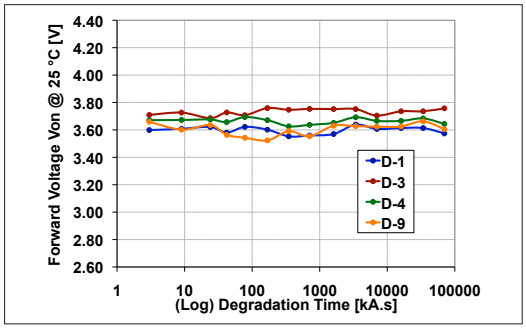

Figure 2. Long degradation performance of different silicon carbide (SiC) junction barrier Schottky (JBS) diodes (10 kV, 5A rated). The diodes have been operated at full current to monitor any changes in forward voltage (Von). The value of the Von voltage has maintained a uniform magnitude for more than 4000 continuous hours of degradation monitoring.

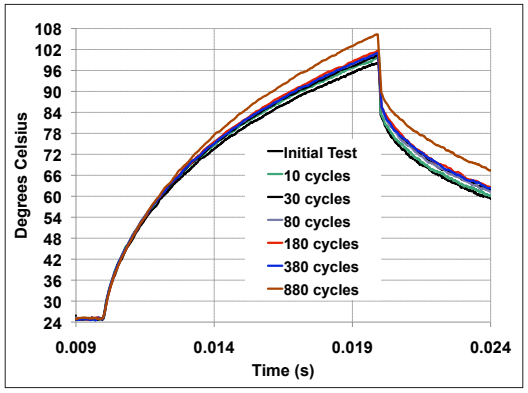

Figure 3. Electrical performance of a co-pack silicon carbide (SiC) MOSFET (10 kV, 5A rated) included in a co-pack package after thermal cycling. Each cycle takes about 30 minutes to complete and continuously changes the temperature of the package between 25 °C and 200 °C. The MOSFET's electrical performance is monitored after various cycling periods using a temperature-sensitive parameter (TSP) test where a 10 ms, 900 W power pulse (200 V @ 4.5 A) is applied to verify any changes in the gate to source voltage (Vgs) magnitude. The device is showing changes in electrical performance after reaching almost 900 continuous cycles.

Systems Module. Electro-thermal simulations of a full three-phase silicon IGBT inverter have been successfully performed and compared with measured results of the power converter temperature monitors. NIST recently performed temperature-dependent measurements for power semiconductor devices that will be used in the DOE Freedom Car project to obtain their parameters and make electro-thermal simulations that are needed for the design of power converters and other circuits in the electric vehicles. The thermal network component model methodology is being applied to generate a model of the power module that will be used and TSP will be used to validate the model against measurements performed using the NIST systems.

■ The NIST high power rapid thermal cycling/shock test systems were completed and they have been used to monitor the changes in electrical behavior on a silicon carbide co-pack module developed by the DARPA HPE program. The package is being subjected to different incremental intervals of cycles that constantly change between 25 °C to 200 °C to thermally (and mechanically) stress the package. Then the NIST high-speed TSP and thermal imaging systems are being used to monitor thermal performance degradation.

■ NIST has developed an advanced packaging design to further expand the capabilities of SiC for use in a greater range of temperatures and environmental conditions. The packaging has been modeled to verify mechanical stability for reliability at temperatures of 300 °C in multiple environments with decreased thermal resistance compared to competing alternatives. The packaging design is being extended to increase the thermal cycling strength with reduced stresses at elevated temperatures while increasing the thermal efficiency of the package. Packaging prototypes have been subjected to thermal resilience testing with success and additional thermal cycling testing along with TSP testing will soon be conducted on additional prototypes as they become available.

Collaborations

University of Maryland CALCE Electronic Products and Systems Center: Patrick McCluskey

Virginia Tech: Jason Lai

University of Central Florida: Z. John Shen

American Competitiveness Institute (ACI), Navy ManTech Center: Barry Thaler

General Electric R&D: Ravisekhar Raju.

Powerex: Scott Leslie

Quantum Focus Instruments Corporation:

Cree Inc.

Recent Publications

J. M. Ortiz-Rodríguez, M. Hernández-Mora, T. Duong, S. G. Leslie, and A. R. Hefner, *"Thermal Network Component Models for 10 kV SiC Power Module Packages,"* in the Proceedings of the 2008 IEEE Power Electronics Specialists Conference (PESC), June 15-19, 2008, Island of Rhodes, Greece.

T. H. Duong, J. M. Ortiz-Rodriguez, R. N. Raju, and A. R. Hefner, *"Electro-thermal Simulation of a 100 A, 10 kV Half-Bridge SiC MOSFET/JBS Power Module,"* in the Proceedings of the 2008 IEEE Power Electronics Specialists Conference (PESC), June 15-19, 2008, Island of Rhodes, Greece.

N. Barbosa III and A. J. Slifka, *"Spatially- and Temporally-Resolved Thermal Imaging of Cyclically Heated Interconnects by Use of Scanning Thermal Microscopy (SThM),"* submitted to Microscopy Research and Technique.

A. R. Hefner and S. Beermann-Curtin, *"Status of the DARPA WBST High Power Electronics Program in SiC Device Development and Technology Transition,"* Proceedings of the Government Microcircuit Applications and Critical Technology Conference (GOMACTech) 2007, March 19-22, 2007, Lake Buena Vista, FL, pp. 185-188.

M. Hernández-Mora, A. Akuffo, C. E. Hood, J. M. Ortiz-Rodríguez, and A. Hefner, *"Experimental Evaluation of SiC PiN Diode Forward Bias Degradation and Long Term Stability,"* 2007 IEEE Power Electronics Specialists Conference (PESC), 17-21 June, 2007, Orlando, FL, pp. 61-65.

A.R. Hefner, R. Sei-Hyung, H. Brett, D.W. Berning, C. E. Hood, J. M. Ortiz-Rodriguez, A. Rivera-Lopez, T. Duong, A. Akuffo, M. Hernández-Mora, *"Recent Advances in High-Voltage, High-Frequency Silicon-Carbide Power Device,"* Proceedings of the 2006 IEEE Industry Applications Society (IAS) Annual Meeting, October 8-12, 2006, Tampa, FL, pp. 330-337.

R. R. Keller, R. H. Geiss, N. Barbosa III, A. J. Slifka, and D. T. Read, *"Strain-Induced Grain Growth during Rapid Thermal Cycling of Aluminum Interconnects,"* Paper presented at the 2006 TMS Annual Meeting, April 2006.

Manufacturing Support Program

Cross-cutting all manufacturing disciplines is the need for supporting information technology and processing capabilities. The transition to 300 mm fabs, single-wafer lots, and the extensive use of foundries has made efficient information handling and automation indispensable to the production process. Information technology touches nearly every aspect of semiconductor production and distribution, including process control, tool to tool interconnect, automated material handling and tracking, reticle management, and information interchange across the supply chain. NIST is working with the International Semiconductor Industry Initiative (ISMI, a subsidiary of SEMATECH) to provide and maintain an on-line engineering statistical handbook to support process control, and is working with industry on standards required to support information flow across the "engineering chain," and to provide standards for secure electronic diagnostic data and for coherent time synchronization on the factory floor.

Product Authentication Information Management

Technical Contacts:
Y. Li-Baboud
E. Simmon
Y. Obeng
A. Griesser

Goals

The project's objective is to realize interoperable and secure exchange of information through participation in standards development and research of information models for capturing the necessary information for authentication of electronics and electronic components throughout its product lifecycle.

Customer Needs

Distinguishing the genuine article from counterfeit is increasingly challenging, and accurate product authentication will require efficient access to information. Central to this objective is the management of the information needed for product authentication. It is imperative to have integrated information flow throughout the product life cycle, from conception to disposal, such that relevant data would be securely yet readily available to the necessary parties from manufacturers to end-users to customs and other law enforcement officers. In order for information management to be an effective tool for product authentication, international government entities and global supply chain stakeholders must ensure accessibility and traceability of pertinent product identity information.

Technical Strategy

A solution to the counterfeiting problem will require a layered approach to provide prevention, detection, and mitigation while maintaining a viable tradeoff between cost and risk. The project will work with industry to determine challenges and priorities in addressing counterfeit issues. Through discussions with industry and government stakeholders, the project will gather information on the current landscape, threats, challenges, priorities and potential solutions in addressing counterfeit electronic products. The overall information integration strategy necessary for developing collaborative anti-counterfeiting countermeasures is shown in Figure 1.

DELIVERABLES:

- Hold a government-industry workshop to determine the current landscape, threats, challenges and priorities in addressing counterfeit electronic products in the supply chain. 2Q 2009
- Draft a white paper on findings and analysis from workshop and discussions with industry stakeholders. 3Q 2009

The project will continue to participate in industry standards activities, including SEMI Anti-Counterfeiting TF to develop a common architecture for product authentication through authentication service providers. The project will also participate in the electronics industry anti-counterfeiting efforts, including IPC. Other industry standards will also be of interest in order to leverage lessons learned and ensure interoperability of product authentication information in the global supply chain as shown in Figure 1. As a starting point, Figure 2 depicts a data model for product authentication was developed for the SEMI Anti-Counterfeiting working group.

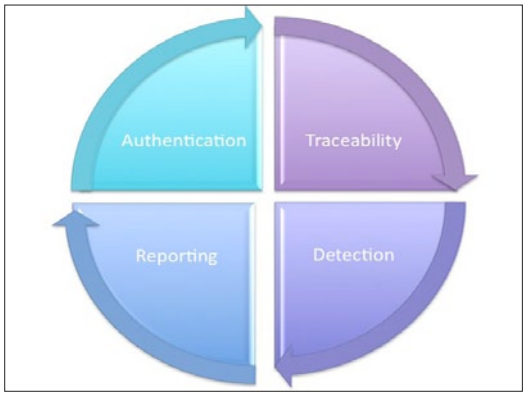

Figure 1. Managing diverse types of information strengthens product identification.

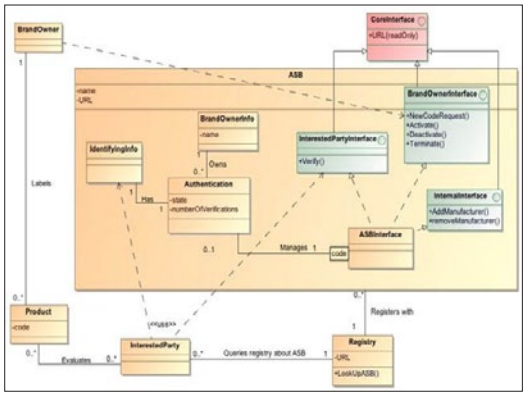

Figure 2. Data model for information exchange between Authentication Service Bodies and stakeholders.

Another thrust is to bring interoperability among disparate information sources on product identity. Information models by developing a concrete understanding of the counterfeiting problem, product authentication requirements,

and other information needs based on input from industry and government stakeholders. The project will strive to develop and propose an integrated information flow throughout the product life cycle, from conception to disposal, such that relevant data would be securely yet readily available to the necessary parties from manufacturers to end-users to customs and other law enforcement officers.

DELIVERABLES:

- Research feasibility of using federated identity management for product authentication. 3Q 2009

Accomplishments

Co-hosted NIST-SEMI Product Authentication Information Management Workshop, February 17-18, 2009, in Gaithersburg, MD.

Participated in the SEMI T20 *Specification for System Architecture on Product Authentication of Semiconductor and Related Products development.*

Presentations and Publications

E. Simmon. *"Secure Authentication Codes"*, SEMICON West, July 2008.

Y. Li-Baboud. *"Product Lifecycle Identity Management,"* Symposium on Prevention, Detection and Mitigation of Counterfeit Electronic Components, September 2008.

Y. Obeng, *"SEMI ACTF Activities,"* NIST-SEMI Product Authentication Information Management Workshop, February 2009.

E. Simmon, *"Counterfeit Avoidance Management: An IPC Perspective,"* NIST-SEMI Product Authentication Information Management Workshop, February 2009.

Next Generation Factory Data Quality

Technical Contacts: J. Amelot C. Vasseur
Y. Li

Goals

The project's objective is to facilitate the development of standards and guidelines to achieve reliable data quality for supporting present and Next-Generation Factory (NGF) data quality needs. The project aims to educate the industry about technology integration and related issues on meeting industry requirement as well as developing prototype and test bed environments for research data quality issues such as time synchronization and data time-stamping.

Customer Needs

The industry NGF goals include 50 percent reduction in cycle time, along with 30 percent reduction in cost of manufacturing. However, increasing wafer sizes, decreasing critical dimensions, and new material introduction all challenge higher initial yield, lower manufacturing costs, and time to market demands. Among the key issues driving the challenges are monitoring and maintaining surface uniformity, decreasing process tolerance windows, as well as increasing process and equipment complexity.

Advancing next-generation semiconductor manufacturing will require data to be collected and analyzed in real-time from a rising confluence of data streams, due to narrowing tolerance windows, new material introduction, and novel processing techniques. Some of the pertinent sources include process equipment and their operational subsystems, in-line metrology, and factory environmental conditions. The retrieved data is vital for designing new processes, maintaining optimal equipment and processing capabilities, controlling the equipment, providing information for rapid yield learning, and expediting handoff of process technology for volume production.

As 300 mm factories mature, the fabrication facilities continue to face difficult challenges in managing the increasing factory complexity, which has resulted in an:

"Explosive growth of data collection/analysis requirements driven by process and modeling needs." *2008 ITRS Update, Factory Integration, p. 42.*

Managing the data proliferation will be critical in realizing the anticipated benefits of greater data accessibility. Extrapolating intelligent correlations from volumes of data in a timely manner requires a common, efficient method of merging the data.

"Increased requirements for high mix factories. Examples are complex process control as frequent recipe creation and changes at process tools and frequent quality control due to small lot sizes." *2008 ITRS Updaate, Factory Integration p. 42*

The quality of the data, including contextual data, impacts the ability to make optimal automated processing quality control decisions in real-time. One aspect of data quality is the ability to acquire accurate time stamps for effectively diagnosing problems and determining other types of cause-effect relationships for Advanced Process Control (APC) applications, especially in the realm of Fault Detection Classification (FDC) and Virtual Metrology (VM).

The Equipment Data Acquisition (EDA) interface where data collection rates can increase to 10,000 data points per second, one millisecond time stamp accuracy is required. An inaccurate time stamp potentially renders the data invalid for many data mining and other analysis applications, yet there continues to be a wide variation in time stamping accuracies among semiconductor manufacturing systems. A robust infrastructure to support accurate time stamps will provide the means to better exploit the increased data availability in next generation semiconductor manufacturing. Such an infrastructure will require an efficient clock synchronization architecture for maintaining time on all related clocks within the process and metrology tools as well as in the manufacturing site.

Technical Strategy

Through participation in the SEMI Data Quality Task force, this project will continue to support standards development to ensure factory equipment and equipment components can reliably and consistently provide quality data and metadata.

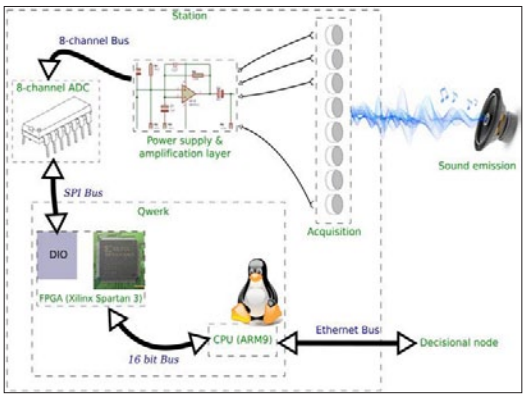

Figure 1. Integration architecture of sensor board and embedded system, where analog acoustic data is time-stamped at the FPGA and packaged for analysis at the control node.

The initial focus area included the exploration of data time-stamping, data acquisition and data fusion through an embedded sensor and control system, as shown in Figure 1, to pinpoint the key issues and challenges impacting data quality for a generic embedded sensor and control system. The research will examine the flow of sensor data as it is processed using analog-to-digital conversion, FPGA, and an embedded processor (Figure 2) to determine the key data bottlenecks and various methods to ensure the quality of the data is maintained throughout the system in order to make accurate and intelligent decisions. The findings would provide insights in how to integrate embedded sensor technologies to provide tested potential solutions for meeting next-generation data quality requirements. Additionally, a distributed sensor and control network enables NIST to research system optimization for effective data collection, sensor data fusion, and real-time control. In parallel to the technical developments, a survey report based on industry feedback for next-generation factory requirements is also provided to detail research opportunities for meeting NGF requirements related to data quality.

DELIVERABLES:

- Develop a sensor network and control test bed to research improvements on generic embedded systems for improving data time-stamping, acquisition, and fusion. 2Q 2009

Accurate time stamping requires a reliable and accurate clock synchronization methodology. Research on practical application and performance testing of the synchronization protocols would determine the impact of various computing factors (e.g., CPU usage, network traffic, constraints of sensors and embedded systems, etc.) on distributed clock synchronization performance

The second focus area is establishing a distributed clock synchronization test bed. The Engineering Research Center at the University of Michigan has been collaborating with NIST in conducting studies on the accuracies achievable with software-based time synchronization protocols in industrial networks. To fully understand the impact of data quality on automated decision-making, a distributed sensor and control environment is being developed along with an evolving factory simulation system. The work will have practical benefits in ensuring the potential solutions and new industry standards are feasible and effective in achieving accurate clock synchronization and data time stamping.

The test bed will provide a research environment to explore mainstream time synchronization protocols and methods to optimize accuracy and cost tradeoffs. The synchronization protocols to be explored include IEEE 1588, Precision Clock Synchronization Protocol for Networked Measurement and Control Systems, and NTP, Network Time Protocol.

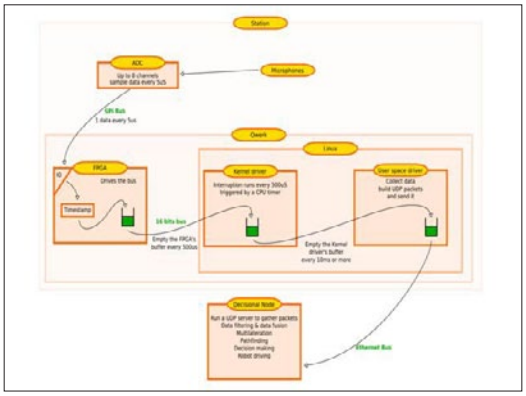

Figure 2. Data flow of sensor data acquisition including the sampling frequencies and processing latencies throughout the system.

DELIVERABLES:

- Develop a research report on establishing a 1588 test bed with initial clock synchronization performance results through experimentation of various integration architectures. 4Q 2009

Conformance to industry standards would enable more effective interoperability among factory automation systems. To enable a method to evaluate and provide guidance on improving conformance to current and future implementa-

tions, the project is also working with ISMI on the development of a prototype metadata quality assessment tool, where one of the objectives is for assessing conformance to SEMI equipment metadata standards and ISMI guidelines. The tool development was suggested by ISMI.

DELIVERABLES:

- Design and develop a prototype metadata quality assessment tool based on SEMI standards and ISMI guidelines. 4Q 2009

Accomplishments

■ Established a sensor network testbed to study data quality issues and recommended practices relevant to timing in embedded sensor systems.

■ Developed EDA Factory Data Collection Simulation software for testing and developing recommend practices for network performance data quality aspects.

■ "Using Network Time Protocol (NTP): Introduction and Recommended Practices" was published as an ISMI Technical Report in February 2006, and updated in May 2008.

■ SEMI E148 Specification for the Definition of Time Synchronization Method and Format.

■ "Time Synchronization in Manufacturing Networks" at the Network Performance Workshop, University of Michigan, April 2006.

Collaborations

Harvey Wohlwend, Gino Crispieri, Lance Rist, International SEMATECH Manufacturing Initiative.

James Moyne Engineering Research Center, University of Michigan Ann Arbor.

Alan Weber, Alan Weber and Associates.

Ecole Supérieure d'Informatique et Applications de Lorraine Nancy, France.

Presentations and Publications

Y. Li-Baboud, A.Weber, P. McGuire, J. Amelot, and J. Le Guen. *"Assessment of Industry Research Priorities for Intelligent Sensors and Control"*, AEC/APC Symposium, October 4-8, 2008.

Y. Li-Baboud, X. Zhu, D. Anand, S. Hussaini, and J. Moyne. *"Semiconductor Manufacturing Equipment Data Acquisition Simulation for Timing Performance Analysis,"* Proceedings of IEEE International Symposium on Precision Clock Synchronization for Measurement, Control and Communication 2008, September 24-26, 2008.

Y. Li, *"Using NTP: Introduction and Recommended Practices,"* ISMI Technology Transfer, May 2008.

V. Anandarajah, N. Kalappa, S. Hussaini, R. Sangole, J. Baboud, Y. Li, and J. Moyne. *"Precise Time Synchronization in Semiconductor Manufacturing,"* Proceedings of the IEEE International Symposium on Precision Clock Synchronization for Measurement Control and Communication, October 1-3, 2007, Vienna, Austria.

N. Kalappa, V. Anandarajah, J. Baboud, Y. Li, and J. Moyne. *"Fab-Wide Network Time Synchronization – Simulation and Analysis,"* AEC/APC Symposium, September 15-20, 2007, Indian Wells, CA.

Securing E-Manufacturing

Technical Contacts:
Y. Li
K. Brady

Goals

The project strives to employ the latest web services security technologies for mitigating increasing security risks of potential Internet-based application systems. As a proof of concept, the project aims to design a security framework enabling efficient authentication and access control to critical resources.

Customer Needs

Optimizing factory and process capabilities and efficiency will require resources to be shared among disparate partners in the engineering chain. The ability to share critical resources among disparate partners has become a priority in the International Technology Roadmap for Semiconductors (ITRS):

"Cyber security continues to remain a high priority from the factory operations perspective" 2007 ITRS , Factory Integration, p. 16.

With the convenience and economic advantages of the distributed global network necessary to realize e-Manufacturing comes the security challenges of the digital world. As data becomes readily accessible from remote locations, the semiconductor industry is facing greater obstacles in protecting its data in order to ensure their intellectual property (IP) will not be compromised. Compromised data can result in lost profits and in a period where counterfeiters of electronic components are increasingly prevalent, allow access to information to which they are not authorized.

"Ensuring IP protection is critical to overall financial success in an environment where there is a significant amount of operations-level overlap." 2007 ITRS, Factory Integration, p. 17.

In addition to protecting data, the semiconductor factory must also be vigilant to protect its networked systems from viruses and similar threats, which can lead to additional equipment downtime. Security has been a significant issue in a variety of industries, particularly in healthcare and finance where date privacy is inherent to the industry; the semiconductor industry can potentially leverage the need to ensure privacy and apply similar solutions toward equipment data for protection of IP. Additionally, the web services community has been striving to resolve security issues by developing technologies to expedite integration and management of security.

Technical Strategy

Based on the needs and priorities of industry, we will be expanding upon the security framework developed for e-Diagnostics to protect data exchange within the factory and to secure equipment from both internal and external threats. Companies have expressed the need for methods to manage security risks, but not at the expense of productivity. Therefore simplicity of use and security are the key objectives of this project.

The web services community has been striving to resolve security issues by developing technologies to expedite integration and management of security. The eXtensible Markup Language (XML) security suite provides a standard paradigm to manage access control in order to restrict who may and may not control the equipment remotely, encryption and signatures in order to protect the data and ensure against malicious attackers, and key management to ensure the encryption used is safe. These features work with web services transport systems such as Simple Object Access Protocol (SOAP) to further ensure the safety of the data passed in transit. Leveraging the available standards in an effective manner can serve as a potential line of defense. However, employing XML-based standards alone is not sufficient in implementing a secure framework. Security must be managed through careful interaction with factory systems, databases and networks, as well as the users accessing the factory systems.

DELIVERABLES:

- Development of an authentication and access control framework. 4Q 2009

Robust identity management, authentication, and access control of legitimate users must be in place. The system should be readily managed to accommodate dynamic security policies. Simplifying security management is a key practice in avoiding security loopholes. Therefore, in facing the proliferation of security threats and system vulnerabilities, the industry can benefit by leveraging mainstream security tools to pro-

vide a robust line of defense against potentially costly threats to intellectual property and the continuous operation of factory systems.

DELIVERABLES:

- Survey of existing and upcoming technologies for managing authorization and access control. 3Q 2009

Lastly, the security of the system will need to be analyzed and verified. Due to the rapidly evolving nature of security attacks, it is imperative to ensure systems are not only secure against current threats, but also mitigate potential risks in the future. The project will examine the latest types of attacks on identity management and access control and design methods to evaluate the ability of a system to mitigate such risks. The result of the project is intended to provide guidance to current industry activities and a prototype to demonstrate a security framework for managing security at various levels of factory systems from the equipment to enterprise-level systems.

DELIVERABLES:

- Design and prototype a framework for automated assessment of security risks. 4Q 2009

As appropriate, the survey also provides an opportunity for providing insights and guidance from similar industry efforts in supply chain and equipment communication standards to facilitate existing standards developments.

ACCOMPLISHMENTS

E-Diagnostics Security Framework Software.

Engineering Chain Management in the Semiconductor Industry

Technical Contacts:
J. Messina
K. Brady
E. Simmon

Goals

This project will investigate and document key issues related to electronic data exchange, supply chain communication, and other automation standardization needs confronting the semiconductor industry. The objective of this project is to facilitate the evolution of an integrated semiconductor "Engineering Chain" which provides each partner with the data needed to make business decisions in a timely manner.

Customer Needs

Increasing technological requirements have led the semiconductor industry to seek further means of cost savings by improving factory productivity, streamlining business models, and accelerating their supply chain. The growing complexity of product development and manufacturing models in parallel with shrinking product lifecycles further exacerbates the challenges the industry faces. Maximizing interoperability among automation systems in the factory and data exchange throughout the entire manufacturing chain (see Figure 1) will become a greater issue for realizing the semiconductor industry's requirements to reduce time, inventory, and therefore costs.

"Lack of robust and fully featured and integrated software systems to manage the complexity of factory and equipment control is also adding to our challenges." International Technology Roadmap for Semiconductors (ITRS) 2007 Factory Integration, p.1.

A growing area of concern for the semiconductor industry is the growing trend towards legislation that seeks to minimize the environmental impact of manufacturing. This can range from legislation that bans the use of hazardous substances, to mandating tracking of resources (energy and water), to mandating the use of energy efficient designs. An example of this new trend is the European Union's Restriction of Hazardous Substances (RoHS) in electronics directive that seeks to reduce or eliminate six substances known to be hazardous to humans and the environment. RoHS alone will result in a massive shift in the availability of parts as some components are removed from the marketplace while others are redesigned completely to remove the banned substances. For most of these pieces of environmental legislation, companies will only be able to prove compliance through the exchange of extensive amounts of product and manufacturing data. This can only be achieved through the development of new standards that span the entire supply chain.

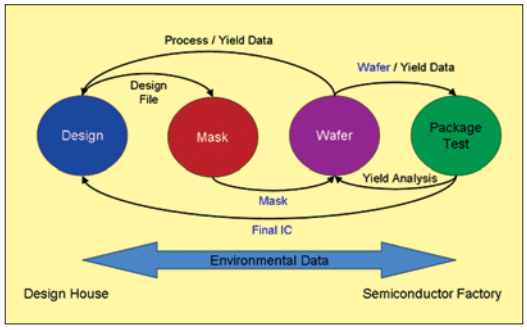

Figure 1. Engineering Chain: Semiconductor Data Exchange Needs Engineering Chain: Semiconductor Data Exchange Needs.

Determining the physical/chemical, environmental, and toxicological properties of chemicals and materials as well as any reaction by-products is essential to protecting human health and the environment as well as minimizing business impacts after processes are developed and introduced into high volume manufacturing.2007 ITRS ESH, p. 1.

Finally, the semiconductor industry is also seeking to control costs and improve semiconductor yields through the development of advanced Factory Information and Control Systems (FICS). Next generation FICS are expected to be able to collect information from equipment that will enable intelligent automated decision-making concerning factory resources. (This will require data quality assurance). Materials will be processed and dispatched to equipment in a way to minimize production-equipment idle time thus maximizing factory output. In addition, FICS will allow factories to be more reconfigurable as needed even to the point of being able to modifying wafer processes on a wafer-by-wafer basis. This is even more important with factories expected to use even fewer total wafers with the expected transition to 450mm. Developing these FICS will require a greater level of interoperability and data exchange within the semiconductor factory.

Technical Strategy

To help the industry achieve their goal of effective partnerships within an Engineering Chain, this project will engage in industry efforts that would benefit from NIST's neutrality, multi-industry expertise, and broad and detailed knowledge of the Information Technology (IT) standards development process.

DELIVERABLES:

- Chair the Information Management Systems (IMS) TWG of the 2009 iNEMI Roadmap. 4Q 2009

Attendance at workshops, conferences, and standards meetings held by key organizations in the semiconductor community such as International SEMATECH (ISMT), Semiconductor Equipment Materials International (SEMI), and RosettaNet provides opportunities to assess current areas of IT standards development. As the industry moves towards utilization of mainstream computing technologies including eXtensible Markup Language (XML) and Simple Object Access Protocol (SOAP), the project provides guidance in leveraging existing best practices from other industries and promoting collaborations among industry partners for mutual benefit. The investigation also includes an informal survey of semiconductor supply chain partners including designers, chip manufacturers, and equipment suppliers to gauge their existing practices, requirements and priorities. Site visits will provide an opportunity for key industry figures to share their vision of how IT standards would expedite advancement of new technologies and business models.

DELIVERABLES:

- Work with SEMI to identify standards needs for developing areas such as environmental compliance, anti-counterfeiting activities, and data quality. 4Q 2009

As appropriate, the survey also provides an opportunity for providing insights and guidance from similar industry efforts in supply chain and equipment communication standards to facilitate existing standards developments. In response to industry needs, the survey will validate internal NIST IT projects against the semiconductor industry's requirements. One potential project is the Infrastructure for Integrated Electronics Design and Manufacturing (IIEDM). IIEDM has facilitated neutral XML-based standards development for the electronic exchange of technical and business data in the electronic components supply chain. Similarities in challenges and technologies utilized may provide an opportunity for future collaborations. In addition, experience with standards development in various industries positions NIST to provide impartial cross-industry benchmarks for IT exchange strategies.

DELIVERABLES:

- Work with industry to create suitable data exchange standards designed to assist industry in complying with all the forthcoming environmental legislation being passed around the world. 4Q 2009

Accomplishments

■ Developed and built a free software tool called "Scriba". The Scriba tool was created to be the new reference implementation for the IPC 1752 version 2.0 Material Declaration standard.

■ Organized and hosted the NIST Product Authentication Information Management Workshop February 17-18th, 2009.

■ In conjunction with IPC Corp., NIST developed the IPC 1752 material declaration standard that supports the exchange of RoHS environmental legislation through the engineering chain.

■ Created a tutorial on how to improve the semiconductor standards development process through the use of XML and UML. This tutorial has been taught as a class at both NIST and various SEMI standards workshops.

■ Assessed the current and future direction of IT use in semiconductor and mask manufacturing. Site visits conducted at four IC manufacturers, one design house, and one photomask supplier. Diagnostic Data Acquisition (DDA), XML, Process Control System (PCS), and Equipment Engineering Capabilities (EEC) are possible areas where NIST can play a future role. Leveraging use of mainstream technologies appears to be widely accepted. Data acquisition standards, including issues of data modeling, speed, bandwidth, quality and integrity, have become critical in advancing e-manufacturing efforts. Follow-up discussions with members of SEMI and ISMT indicated interest in enlisting NIST expertise and contacts to leverage best practices from other industries on specific issues such

as XML-based standards development for manufacturing, timing and synchronization of equipment data, as well as data security issues.

Collaborations

Alan Weber, Alan Weber & Associates.

ITRS Factory Integration Technical Working Group.

SEMI.

SEMATECH.

IPC.

Publications

E. D. Simmon, J. V. Messina, *"Harmonizing Environmental Data Exchange Standards: Lessons Learned from the electronics Industry"*, The Eighth International Conference on EcoBalance, The Eighth International Conference on EcoBalance, Tokyo, Japan, 12/10/2008 to 12/12/2008.

E. D. Simmon, J. V. Messina, M. L. Aronoff, M. Cox, *"Environmental Trends Affecting Electronics Manufacturing"* Fab Engineering and Operations, No. 4, (01-Aug-2008).

J. V. Messina , E. Simmon, E., K. Brady, *"Information Management for Environmental Concerns and Regulatory Requirements"* FEO Magazine, Feb 2008.

K. Botsford, J. V. Messina, E. Simmon, *"North American Environmental Compliance Attitudes Towards Electronics,"* Jun 04-06, 2007, Singapore, Singapore.

E. Simmon, *"RoHS Harmonization ? Progress Toward a Single Global Standard?,"* Advanced Forum on Achieving and Maintaining Global RoHS Compliance, Jun 11-12, 2007, San Francisco, California.

NIST/SEMATECH e-Handbook of Statistical Methods

Technical Contacts:
W. F. Guthrie
A. Heckert
J. J. Filliben

Goals

The goal of the NIST/SEMATECH e-Handbook of Statistical Methods project is to produce an online resource to help scientists and engineers incorporate statistical methods into their work more efficiently. Electronic publication and a practical, example-driven format were chosen to make the e-Handbook readily accessible to its target audiences in industry, including the semiconductor industry in particular.

Customer Needs

Semiconductor manufacturing requires extraordinary discipline in process control. For example, a typical integrated circuit manufacturing process involves several hundred steps. These steps may include as many as thirty lithographic levels, which require extremely precise alignment with respect to one another. Tight process control is essential to produce a functional circuit. SEMATECH has recognized the importance of statistical process control in semiconductor manufacturing and has developed and maintained expertise in this field since its inception in 1988. Two of the more difficult issues impeding routine implementation of these techniques, however, include educating the users and making the tools easy to use.

Technical Strategy

NIST and SEMATECH formed a collaboration under the umbrella Cooperative Research and Development Agreement (CRADA), combining the general expertise in engineering statistics at NIST with the semiconductor manufacturing expertise resident at SEMATECH (Fig. 1).

Figure 1. NIST Engineering Statistics Internet Handbook team (left to right, Alan Heckert, Mark Reeder, Will Guthrie, and Carroll Croarkin) reviewing a page from the chapter on product reliability.

DELIVERABLES:

- Update and maintain the e-Handbook on-line. 4Q 2009
- Begin development of a new chapter on evaluation of measurement uncertainty. 4Q 2009
- Add example computations carried out using the open-source statistics software R. 4Q 2009

Accomplishments

Since release of the final version, work has focused on publicizing the e-Handbook, responding to user feedback, and developing a compact disk version for off-line use (Fig. 2). The web version of the e-Handbook averaged over 800000 hits per month during the last 12 months and over 9500 e-Handbook compact disks were distributed to industrial, government, and academic users all over the world while the e-Handbook was supported in CD format. Publicity on the e-Handbook has appeared in Science, Quality Digest, Micro-Magazine.com, States News Service, National

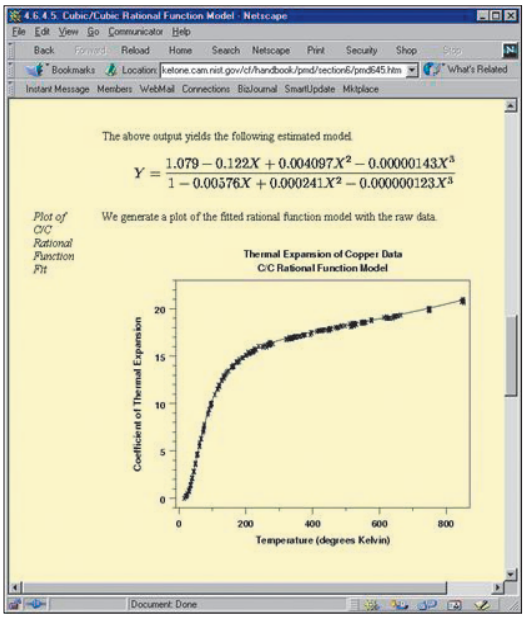

Figure 2. Handbook page from a new case study added to the process modeling chapter this year.

The online engineering statistics handbook is very useful and I make reference to it often in my position as an R&D engineer at a medical device company.

Josh Molho, Ph.D.
Pelikan Technologies

"I reviewed the e-Handbook on the net and I am very impressed with the content, organization and consolidation of the statistical methods."

Jack Lewis
Microchip Technology Inc

Science Digital Library Report for Math, Engineering, and Technology, and American Statistician.

Collaborations

International SEMATECH, Paul Tobias, Jack Prins, Chelli Zey; project planning, organization, writing and editing. Motorola, Pat Spagon; project planning, organization, and writing.

AMD, Barry Hembree; project planning, organization, writing and editing.

Publications

NIST/SEMATECH e-Handbook of Statistical Methods, M. Carroll Croarkin and Paul Tobias, editors, http://www.nist.gov/stat.handbook/.

Abbreviations and Acronyms

A.C.	alternating current
ADR	adiabatic demagnetization refrigerator
AEM	analytical electron microscopy
AES	auger-electron spectroscopy
AFM	atomic force microscope
ALMWG	Analytical Laboratory Managers Working Group (ISMT)
AMAG	Advanced Metrology Advisory Group (ISMT)
ANSI	American National Standards Institute
ARXPS	angle resolved X-ray photoelectron spectroscopy
ASPE	American Society of Professional Engineers
ATP	Advanced Technology Program (NIST)
BCB	benzocyclobutene
BESOI	bond and etch-back silicon-on-insulator
BGA	ball-grid array
BIPM	Bureau International des Poids et Mésures
BIST	built-in self-test
BST	barium strontium titanate
C-AFM	calibrated atomic force microscope (NIST)
C-V	capacitance-voltage
CAD	computer-aided design
CCD	charge-coupled device
CD	critical dimension
CMOS	complementary metal oxide semiconductor
CMP	chem-mechanical polishing
CNT	carbon nanotubes
CPU	central processing unit
CRADA	Cooperative Research and Development Agreement
CRDS	cavity ring-down spectroscopy
CSP	chip-scale package
CTCMS	Center for Theoretical and Computational Materials Science (NIST)
CVD	chemical vapor deposition
D.C.	direct current
DFT	design-for-test
DMA	differential mobility analyzer
DRAM	dynamic random-access memory
DSP	digital signal processing
DUV	deep ultraviolet
EBSD	electron backscatter diffraction
EELS	electron energy loss spectroscopy
EDC	embedded decoupling capacitance
EDS	energy-dispersive spectroscopy
EMC	electromagnetic compatibility

Abbreviations and Acronyms (cont'd)

EMI	electromagnetic interference
EPMA	electron probe microanalysis
EUV	extreme ultraviolet
FIFEM	field ion field emission microscope
FIM	field ion microscope
FWHM	full-width half-maximum
GIXR/SE	grazing incidence X-ray reflection/spectrascopic ellipsometry
GIXPS	grazing incidence X-ray photoelectron spectroscopy
GMR	giant magneto-resistive
HRTEM	high resolution transmission electron microscope
HSQ	current-voltage
IC	integrated circuit
IGBT	insulated-gate bipolar transistor
IETS	Inelastic Electron Tunneling Spectroscopy
IPC	Association Connecting Electronics Industries
ISMT	International SEMATECH
ISO	International Organization for Standardization
ITRS	International Technology Roadmap for Semiconductors
LEED	low-energy electron diffraction
LER	line-edge roughness
LFPG	low frost-point generator
LOCOS	local oxidation of silicon
LPP	laser-produced plasma
LPRT	light-pipe radiation thermometer
MBE	molecular beam epitaxy
MEMS	micro-electro-mechanical systems
MFC	mass flow controller
MMIC	millimeter and microwave integrated circuits
MOS	metal-oxide-semiconductor
MOSFET	metal-oxide-semiconductor field-effect transistor
MPU	microprocessor unit
MUX	multiplex
NCMS	National Center for Manufacturing Sciences
NDP	neutron depth profiling
NGL	next generation lithography
NEMI	National Electronics Manufacturing Initiative
NIST	National Institute of Standards and Technology
NSMP	National Semiconductor Metrology Program
NLO	non-linear optical
NSOM	nearfield scanning optical microscopy
OMAG	Overlay Metrology Advisory Group (ISMT)
PED	Precision Engineering Division (NIST)

PLIF	planar laser-induced fluorescence
PMI	phase-measuring interferometer
PTB	Physikalisch-Technische Bundesanstalt
PZT	lead zirconium titanate
QM	quantum mechanics
RAM	random-access memory
RCWA	rigorous coupled wave analysis
RGA	residual gas analyzer
RLGC	distributed resistance, inductance, conductance, and capacitance
RTA	rapid thermal annealing
RTD	resonant tunneling diodes
RTP	rapid thermal processing
SAM	self assembled monolayer
SANS	small-angle neutron scattering
SBIR	Small Business Innovative Research
SCM	scanning capacitance microscope
SEM	scanning electron microscope
SHG	second harmonic generation
SIA	Semiconductor Industry Association
SIMOX	separation by implantation of oxygen
SIMS	secondary-ion mass spectrometry
SoC	system-on-a-chip
SOI	silicon on insulator
SPM	scanning probe microscope
SRC	Semiconductor Research Corporation
SRM®	Standard Reference Material
SSHG	surface second-harmonic generation
SSIS	surface-scanning inspection system
STM	scanning tunneling microscope
SURF III	Synchrotron Ultraviolet Radiation Facility III
TCAD	technology computer-aided design
TCR	temperature coefficient resistance
TDDB	time-dependent dielectric breakdown
TDR	time-domain reflectometry
TEM	transmission electron microscope
TFTC	thin-film thermocouple
TOF	time-of-flight
TMAH	tetramethyl ammonium hydroxide
UHV	ultra-high vacuum
UV	ultraviolet
WMS	wavelength modulation spectroscopy
VUV	vacuum ultraviolet
XPS	X-ray photoelectron spectroscopy
XRR	X-ray reflectometry

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