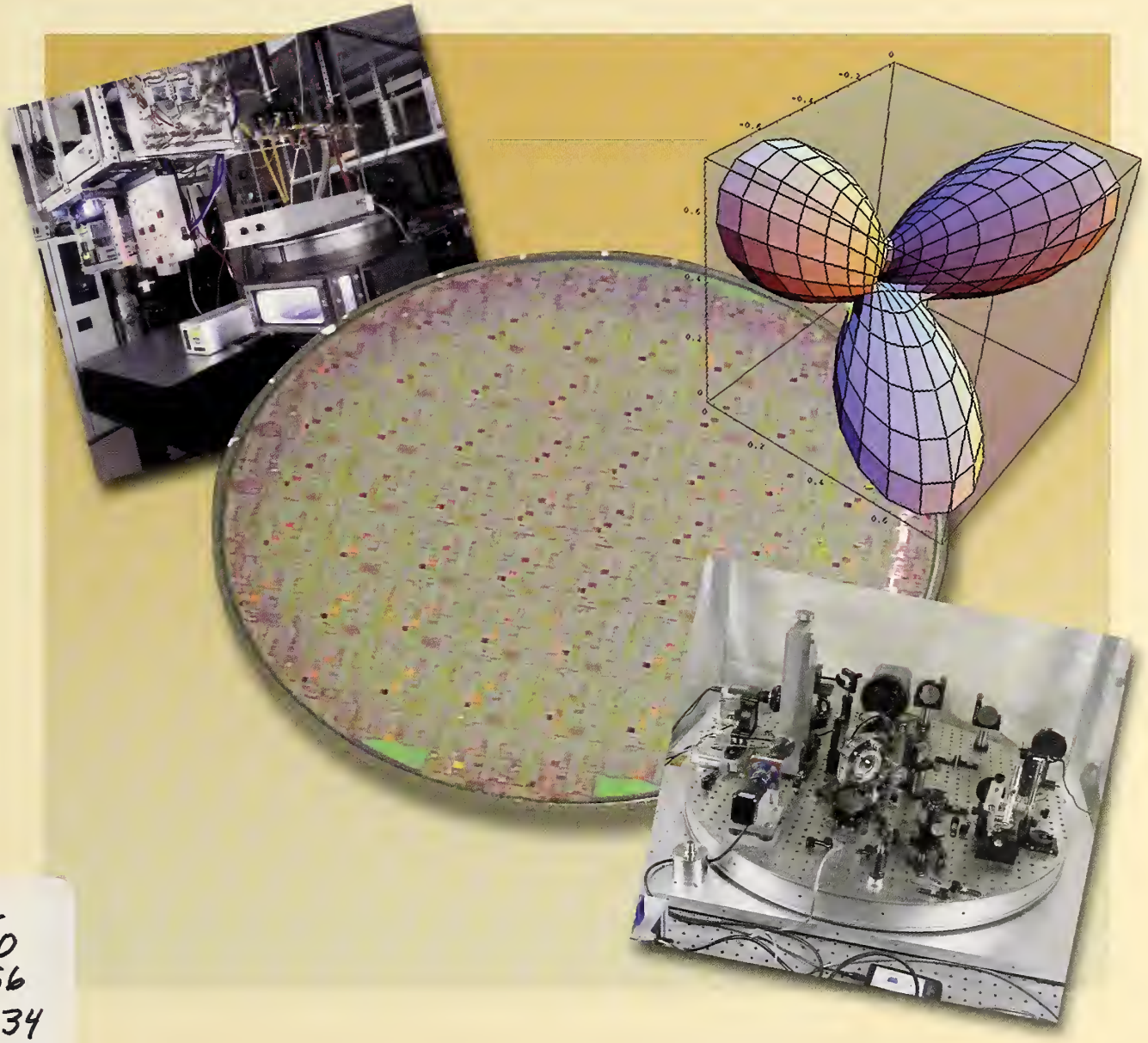
TRONICS AND ELECTRICAL
NEERING LABORATORY

National Institute of
Standards and Techr
Technology Administra
U.S. Department of
Commerce

NISTIR 6934
January 2003

FFICE OF MICROELECTRONICS PROGRAMS

PROGRAMS, ACTIVITIES, AND ACCOMPLISHMENTS



The Electronics and Electrical Engineering Laboratory (EEEL)

One of NIST's seven measurement and standards laboratories, EEEL conducts research, provides measurement services, and helps set standards in support of the fundamental electronic technologies of semiconductors, magnetics, and superconductors; information and communications technologies, such as fiber optics, photonics, microwaves, electronic displays, electronics manufacturing supply chain collaboration; forensics and security measurement instrumentation; fundamental and practical physical standards and measurement services for electrical quantities; maintaining the quality and integrity of electrical power systems; and the development of nanoscale and microelectromechanical devices. EEEL provides support to law enforcement, corrections, and criminal justice agencies, including homeland security.

EEEL consists of six programmatic divisions and two matrix-managed offices:

Electricity Division

Semiconductor Electronics Division

Radio-Frequency Technology Division

Electromagnetic Technology Division

Optoelectronics Division

Magnetic Technology Division

Office of Microelectronic Programs

Office of Law Enforcement Standards

This publication describes the technical programs of the Office of Microelectronics Programs. Similar documents describing the other Divisions and Offices are available. Contact NIST/EEEL, 100 Bureau Drive, MS 8100, Gaithersburg, MD 20899-8100, telephone 301-975-2220, http://www.eeel.nist.gov. These publications are updated biennially.

Cover caption: The Office of Microelectronics Programs administers and assists laboratory management in a NIST-wide effort to meet the highest priority measurement needs of the semiconductor manufacturing industry and its supporting infrastructure. The National Semiconductor Metrology Program (NSMP) is a funding mechanism supporting many of those metrology projects. Research efforts include scaling issues associated with plasmas used for manufacturing of 300 mm wafers, and the experimental measurement of the birefringence of CaF_2 and other materials used for deep UV light (these materials were thought to be non-birefringent until NIST measurements and later modeling determined that under UV they do posses birefringence), the Twyman-Green VUV interferometer was used to make the measurements.

Electronics and Electrical Engineering Laboratory

Office of Microelectronics Programs

Programs, Activities, and Accomplishments

NISTIR 6934

January 2003

U.S. DEPARTMENT OF COMMERCE
Donald L. Evans, Secretary

Technology Administration
Phillip J. Bond, Under Secretary of Commerce for Technology

National Institute of Standards and Technology
Arden L. Bement, Jr., Director

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Reference: References made to the International Technology Roadmap for Semiconductors (ITRS) apply to the 2001 edition. The ITRS is available from the Semiconductor Industry Association (SIA), 181 Metro Drive, Suite 450, San Jose, CA 95110, phone: (408) 436-6600; fax: (408) 436-6646, or at http://public.itrs.net. In the near future, 2002 update material will be available at this website.

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Welcome and Introduction

Welcome

The microelectronics industry supplies vital components to the electronics industry and to the U.S. economy, enabling rapid improvements in productivity and in new high technology growth industries such as electronic commerce and biotechnology. The National Institute of Standards and Technology, NIST, works with industry to develop and apply technology, measurements and standards, and applies substantial efforts on behalf of the semiconductor industry and its infrastructure. This report describes the many projects being conducted at NIST that constitute that effort.

Historical Perspective

NIST's predecessor, the National Bureau of Standards (NBS), began work in the mid-1950s to meet the measurement needs of the infant semiconductor industry. While this was initially focused on transistor applications in other government agencies, in the early 1960s the Bureau sought industry guidance from the American Society for Testing and Materials (ASTM) and the (U.S.) Electronic Industries Association (EIA). ASTM's top priority was the accurate measurement of silicon resistivity. NBS scientists developed a practical non-destructive method ten times more precise than previous destructive methods. The method is the basis for five industrial standards and for resistivity standard reference materials widely used to calibrate the industry's measurement instruments. The second project, recommended by a panel of EIA experts, addressed the "second breakdown" failure mechanism of transistors. The results of this project have been widely applied, including solving a problem in main engine control responsible for delaying the launch of a space shuttle.

From these beginnings, by 1980 the Bureau's semiconductor metrology program had grown to employ a staff of sixty with a $6 million budget, mostly from a variety of other government agencies. Congressional funding in that year gave NBS the internal means to maintain its semiconductor metrology work. Meeting industrial needs remained the most important guide for managing the program.

Industrial Metrology Needs

By the late 1980's, NBS (now NIST) recognized that the semiconductor industry was applying a much wider range of science and engineering technology than the existing NIST program was designed to support. The necessary expertise existed at NIST, but in other parts of the organization. In 1991, NIST established the Office of Microelectronics Programs (OMP) to coordinate and fund metrological research and development across the agency, and to provide the industry with easy single point access to NIST's widespread projects. Roadmaps developed by the (U.S.) Semiconductor Industry Association (SIA) have independently identified the broad technological coverage and growing industrial needs for NIST's semiconductor metrology developments. As the available funding and the scope of the activities grew, the collective name became the National Semiconductor Metrology Program (NSMP), operated by the OMP.

The NSMP has stimulated a greater interest in semiconductor metrology, motivating most of NIST's laboratories to launch additional projects of their own and to cost-share OMP-funded projects. The projects described in this book represent this broader portfolio of microelectronics projects. Most, but not all, of the projects described are partially funded by the NSMP, which provided a $12.5 million budget in fiscal year 2002.

Fostering NIST's Relationships with the Industry

NIST's relationships with the SIA, International SEMATECH, and the Semiconductor Research Corporation (SRC) are also coordinated through the OMP. Staff from OMP represents NIST on the SIA committees that develop the International Technology Roadmap for Semiconductors (ITRS) as well as on numerous SRC Technical Advisory Boards. OMP and other NIST staff are also active in the semiconductor standards development work of the ASTM, the Deutsches Institut für Normung (DIN), the EIA, the International Organization for Standardization (ISO), and Semiconductor Equipment and Materials International (SEMI).

Office of Microelectronics Programs

The **Office of Microelectronics Programs** provides coordination of silicon semiconductor manufacturing metrology activities across NIST to maximize the impact of this critical industry on the health of the U.S. economy. The Office, with a permanent staff of three, is located in Gaithersburg, Maryland, and is one of the two Offices in the Electronics and Electrical Engineering Laboratory at NIST.

Many of the projects managed by the Office are cooperative activities across several of NIST's Operating Units. Thus the projects are able to leverage the best expertise available for the specific task across NIST, regardless of organizational structure. Our projects are also aligned by research Program Areas: Lithography Metrology, Critical Dimension and Overlay Metrology, Thin Film and Shallow Junction Metrology, Interconnect and Packaging Metrology, Wafer Characterization and Process Metrology, Modeling and Design Metrology, Test Metrology, and Manufacturing Support.

Additional activities of the Office which insure timely response to industry need to include:

- Extensive interactions with industry consortia, such as the Semiconductor Research Corporation (SRC) and International SEMATECH (ISMT).
- Participation in the roadmapping activities commissioned by the Semiconductor Industry Association and administered by International SEMATECH.
- Standards bodies activities related to the semiconductor industry including the Semiconductor Equipment and Materials International (SEMI) standards program, American Society of Testing of Materials (ASTM) in the US, and Deutsches Institut für Normung (DIN) in Germany.

For additional information about the Office of Microelectronics Programs, please visit our website http://www.eeel.nist.gov/omp/.

Stephen Knight, Director

Vision

The Office of Microelectronics Programs will be recognized as an outstanding organization managing and coordinating projects key to meeting the metrology needs of the semiconductor manufacturing industry.

Values

The Office of Microelectronics Programs values relevance and focus of its projects in solving crucial metrology issues facing the semiconductor manufacturing industry. The Office values the technical excellence and the dedication of the scientists, engineers, and technicians participating in the National Semiconductor Metrology Program.

Mission

The mission of the Office of Microelectronics Programs is to manage the National Semiconductor Metrology Program (NSMP), a NIST-wide effort designed to meet the highest priority measurement needs of the semiconductor manufacturing industry and its supporting infrastructure industries as expressed by the International Technology Roadmap for Semiconductors and other authoritative industry sources.

Goals

The Office of Microelectronics Programs will:

- Diligently identify critical metrology gaps confronting the semiconductor manufacturing industry, and implement robust projects to confront those needs;
- Insure expeditious technology transfer of NSMP results to the industry; and
- Assist the NIST technical body in interfacing efficiently with key elements of the semiconductor manufacturing industry and its research and development community.

Funding

The National Semiconductor Metrology Program (NSMP) was established in 1994 with a strong focus on mainstream silicon CMOS technology and an ultimate funding goal of $25M. Current funding from NSMP is $12.5M, augmented with additional funding from all sources of $11.8M, supporting a broad portfolio of semiconductor metrology projects conducted in all of the Laboratory Units of the Measurements and Standards Laboratories of NIST:

- Electronics and Electrical Engineering Laboratory (810)
- Manufacturing Engineering Laboratory (820)
- Chemical Sciences and Technology Laboratory (830)
- Physics Laboratory (840)
- Materials Sciences and Engineering Laboratory (850)
- Building and Fire Research Laboratory (860)
- Information Technology Laboratory (890)

Chart 1 shows the disposition of NSMP Funding and Other Sources Funding by Laboratory, and Chart 2 shows the disposition of NSMP Funding and Other Sources Funding by Program. Other Sources Funding includes Laboratory STRS, Advanced Technology Program Intramural, Competence, and Other Agency.

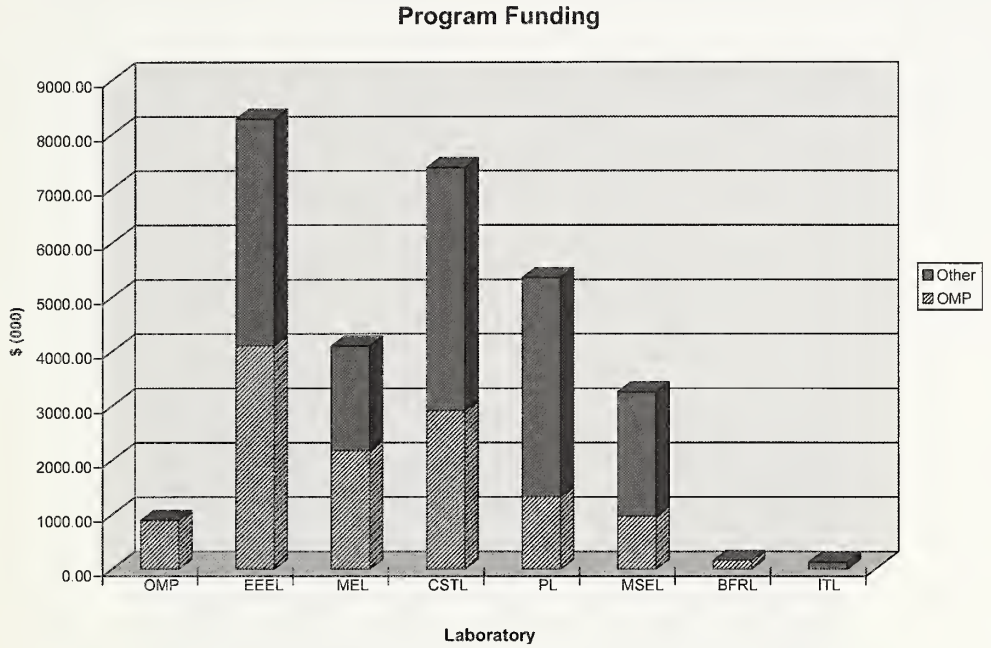

CHART 1

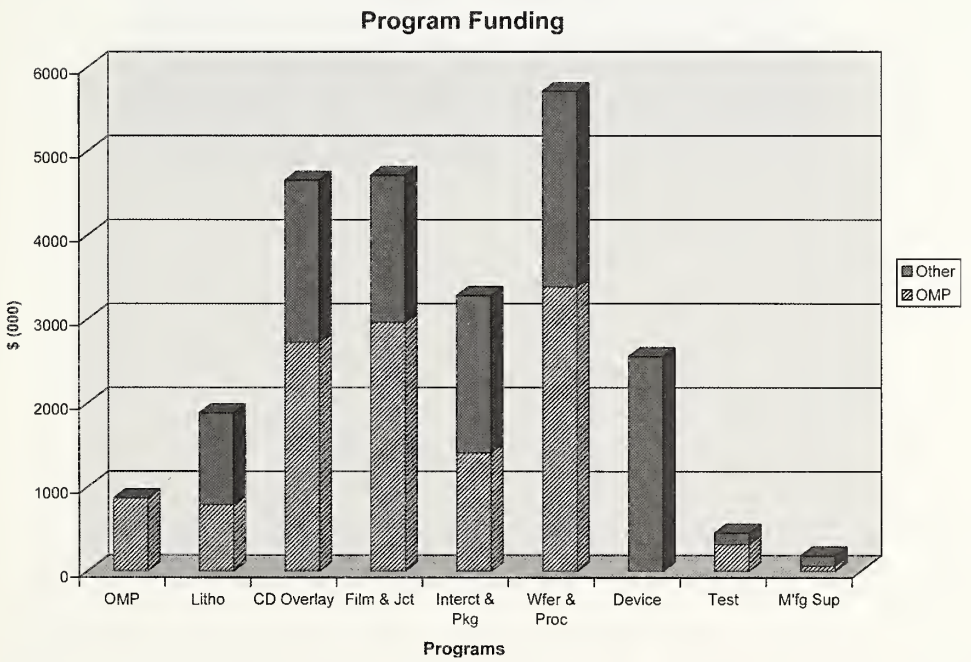

CHART 2

Office of Microelectronics Programs Organization

KNIGHT, Stephen (Director) stephen.knight@nist.gov
(301) 975-2871

BUCKLEY, Michele L. (Secretary) michele.buckley@nist.gov
(301) 975-4400

MARTINEZ DE PINILLOS, Joaquin V. (Senior Scientist) jack.martinez@nist.gov
(301) 975-8125

SCACE, Robert I. (Guest Researcher/Contractor) robert.scace@nist.gov
(301) 975-5198

Back Row: Stephen Knight, Robert Scace, Joaquin Martinez de Pinillos
Seated: Michele Buckley

Lithography Metrology Program

Advances in lithography have largely driven the spectacular productivity improvements of the integrated circuit industry, a steady quadrupling of active components per chip every three years over the past several decades. This continual scaling down of transistor dimensions has allowed more and more components on a chip, lowered the power consumption per transistor, and increased the speed of the circuitry. The shrinking of device dimensions has been accomplished by shortening the wavelength of the radiation used by the lithography exposure tools. The industry at this point has moved into the deep ultraviolet (DUV) spectrum. Currently, exposure tools operating at 193 nm are being introduced, and exposure tools operating at 157 nm are in development. Looking beyond the deep ultraviolet, extreme ultraviolet radiation (EUV) at 13 nm is being investigated, and demonstration tools are being designed and assembled. The overall goal of this task is to support these developments in DUV and EUV. The areas of emphasis are lens materials, laser calorimetry, radiation detector sensitivity and damage, EUV lens metrology, and metrology for the development of advanced phoresist materials. The current projects are:

- Metrology Supporting Deep Ultraviolet Lithography
- Metrology Supporting Extreme Ultraviolet Lithography
- Polymer Photoresist Fundamentals for Next-Generation Lithography

Critical Dimension and Overlay Metrology Program

The principal productivity driver for the semiconductor manufacturing industry has been the ability to shrink linear dimensions. A key element of lithography is the ability to create reproducible undistorted images, both for masks and the images projected by these masks onto semiconductor structures. Lithography as a whole, fabricating the masks, printing and developing the images, and measuring the results, currently constitutes ≈35 % of wafer processing costs. The overall task of the Critical Dimension and Overlay Program is to assist the industry in providing the necessary metrology support for current and future generations of lithography technology. These goals include advances in modeling, the provision of next generation critical dimension and overlay artifacts, and comparisons of different critical dimension and overlay measurement techniques.

Currently, resolution improvements have outpaced overlay and critical dimension measurement improvements. To maintain cost effectiveness significant advances must be made. The current projects are:

- Atom-Based Dimensional Metrology
- Scanning Electron Microscope-Based Dimensional Metrology
- Optical-Based Dimensional Metrology
- Scanning Probe Microscope-Based Dimensional Metrology
- Electrical-Based Dimensional Metrology
- X-Ray and Neutron Small Angle Scattering-Based Dimensional Metrology
- Model-Based Linewidth Metrology

Thin Film and Shallow Junction Metrology Program

The dimensions of the active transistor areas are approaching the spacing between dopant atoms, the stochastic regime, complicating both modeling and doping gradient measurements. Thin dielectric and conducting films are approaching monolayer thicknesses.

As device dimensions continue to shrink, junctions and critical film thicknesses approach the realm of several atoms thick, challenging gradient, thickness and roughness metrology as well as electrical and reliability characteristics. The gate dielectric, traditionally SiO_2, will soon no longer be viable. This Program's overall task is to provide suitable metrology and reference materials for thin dielectrics and conducting barrier films, including electrical characterization, gradient, thickness and roughness metrology and overall reliability metrology. The current projects are:

- Two- and Three-Dimensional Profiling
- Boron and Nitrogen Thin Film and Implant Standards Using Neutron Depth Profiling
- Gate Dielectric Metrology
- Chemical Metrology of Materials and Particle Contamination
- Thin Film X-ray Metrology for Microelectronics
- Second Harmonic Generation from the Silicon-Silicon Dioxide Interface

Interconnect and Packaging Metrology Program

Advances in interconnect and packaging technologies have introduced rapid successions of new materials and processes. Environmental pressures are leading to the reduction and eventual elimination of lead in solder used for attaching chips to packages and packages to circuit boards. The overall task of this program is to provide critical metrology and methodology for mechanical, chemical, metallurgical, electrical, thermal, and reliability evaluations of interconnect (IC) and packaging technologies.

The function of packaging is to connect the integrated circuit to the system or subsystem platform, such as a circuit board, and to protect the integrated circuit from the environment. The increasing number of inputs and outputs (I/O) on circuits with vastly larger scale of integration is forcing ever smaller I/O pitches, the use of flip chip bonding, and the use of intermediary platforms called interposers. The integration of sensors and actuators onto integrated circuits through MEMS technology and the increasing use of low cost integrated circuits in harsh environments is increasing the complexity of the packaging task. Environmental concerns are forcing the need for development of reliable lead-free solder and other low environmental impact packaging materials.

System reliability requirements demand modeling, testing methods, and failure analysis of the integrated circuits before and after packaging. Metrology is a significant component of reliability evaluation. The current projects are:

- Superconformal Deposition of Copper and Advanced Interconnect Materials
- Porous Thin Films Metrology for Low-k Dielectrics
- Tomography with Scanning Transmission Electron Microscope Images
- Wire Bonding to Cu/Low-k Semiconductor Devices
- Solders and Solderability Measurements for Microelectronics
- Interconnect Materials and Reliability Metrology
- Thermal Measurements and Packaging Reliability
- Advanced IC Interconnects – Process Metrology and Models
- Dielectric Metrology Supporting Integrated Passive Device Technology

Wafer Characterization and Process Metrology Program

Device scaling has been the primary means by which the semiconductor industry has achieved unprecedented gains in productivity and performance quantified by Moore's Law. Until recently only modest changes in the materials used have been made. The industry was able to rely almost exclusively on the three most abundant elements on Earth – silicon, oxygen, and aluminum.

Recently, however, copper has been introduced for interconnect conductivity, replacing aluminum alloys. A variety of low-dielectric constant materials is being introduced to reduce parasitic capacitance, replacing silicon dioxide. As dimensions continue to shrink, the traditional silicon dioxide gate dielectric thickness has been reduced to the point where tunneling eurrent has become significant and is compromising the performance of the transistors. This is requiring the introduction of higher dielectric constant materials. Initially the addition of nitrogen to the gate material is sufficient, but in the near future more exotic materials such as transition metal oxides, silicates, and aluminates will be required. As dimensions are reduced, gate depletion effects and dopant diffusion through the gate dielectric are limiting transistor performance. With the replacement of the traditional silicon dioxide/polysilicon gate stack processes with materials capable of supporting ever shrinking geometries, the task of the industry becomes more difficult. The overall task represented by the projects below is the development of analytical teehniques with unparalleled spatial resolution, accuracy, robustness and ease of use.

Shrinking dimensions of transistors and increases in the wafer diameter from 200 mm to 300 mm are placing more stringent requirements on wafer flatness, thickness and warp, and on ion and particle contamination.

Accurate metrology of process gases is essential for reproducible manufacture of semiconductor products. Critical physical parameters need to be measured on a wide variety of reactive and nonreactive process gases, allowing the accurate calibration of flow meters and residual gas analyzers. Water contamination at extremely low levels in process gases presents serious manufacturing difficulties. Accurate calibration of water vapor at extremely low vapor pressures is required.

Accurate metrology of process gases is essential for reproducible manufacture of semiconductor products and a wide variety of metrology issues emerge in plasma, chemical vapor, and rapid thermal processing steps used in semiconductor manufacture.

Detection and accurate sizing of particle contamination continues to challenge semiconductor manufacturing.

- Wafer and Chuck Flatness Metrology
- Modeling, Measurements, and Standards for Wafer Surface Inspection
- High-Resolution Microcalorimeter X-Ray Spectrometer for Chemical Analysis
- Thermophysical Property Data for Modeling CVD Processes and for the Calibration of Mass Flow Controllers
- Temperature Measurements and Standards for Rapid Thermal Processing
- Low Concentration Humidity Standards
- Plasma Process Metrology
- Measurements for Vacuum Process Control

Test Metrology Program

Lead counts of several thousand per chip and test frequencies in the microwave regime challenge current test methodologies. The overall task is to develop test methodologies to address these new requirements.

Accurate at-speed test methodology of digital integrated circuits is a critical requirement. Traditional methods utilizing IC contact probing technology require large contact pads incompatible with current IC designs. The development of alternative probing approaches through non-contact and intermittent probing techniques appears very promising. However, to implement these techniques, solving the at-speed test calibration issues is crucial. With the challenges facing designers and the rising costs of development, it is crucial to develop accurate testing strategies. The current projects are:

- Metrology for System-on-a-Chip (SOC)
- Non-Linear Device Characterization
- At-Speed Test of Digital Integrated Circuits
- Jitter and Propagation Delay

Manufacturing Support

Certain disciplines such as statistical process control are generic to all aspects of manufacturing. These disciplines are equally applicable to the manufacture of the materials and the manufacturing equipment as well as the manufacturing of the integrated circuits, their packaging and testing. NIST has one project jointly with ISMT in this category; the creation of an engineering statistical handbook on the internet. The current projects are:

- NIST/SEMATECH Engineering Statistics Internet Handbook
- Supply Chain Communication and Automation Needs Assessment of the Semiconductor Industry

Technical Contacts

Project Title	Technical Contacts	Phone Number	Email Address
Lithography Metrology Program			
Metrology Supporting Deep Ultraviolet Lithography	J. Burnett M. Dowell R. Gupta	(301) 975-2679 (303) 497-7455 (301) 975-2325	john.burnett@nist.gov mdowell@boulder.nist.gov rejeev.gupta@nist.gov
Metrology Supporting Extreme Ultraviolet Lithography	T. Lucatorto C. Tarrio U. Griessman	(301) 975-3734 (301) 975-3737 (301) 975-4929	thomas.lucatorto@nist.gov charles.tarrio@nist.gov ulfg@nist.gov
Polymer Photoresist Fundamentals for Next-Generation Lithography	E. Lin C. Soles W. Wu	(301) 975-6743 (301) 975-8087 (301) 975-6839	eric.lin@nist.gov christopher.soles@nist.gov wen-li.wu@nist.gov
Critical Dimension and Overlay Metrology Program			
Atom-Based Dimensional Metrology	R. Silver	(301) 975-5609	richard.silver@nist.gov
Scanning Electron Microscope-Based Dimensional Metrology	A. Vladar M. Postek	(301) 975-2399 (301) 975-2299	andras.vladar@nist.gov michael.postek@nist.gov
Optical-Based Dimensional Metrology	J. Potzick R. Silver T. Doiron	(301) 975-3481 (301) 975-5609 (301) 975-3472	james.potzick@nist.gov richard.silver@nist.gov theodore.doiron@nist.gov
Scanning Probe Microscope-Based Dimensional Metrology	T. Vorburger J. Dagata R. Dixson M. Postek	(301) 975-3493 (301) 975-3597 (301) 975-4399 (301) 975-2299	thedore.vorburger@nist.gov john.dagata@nist.gov ronald.dixson@nist.gov michael.postek@nist.gov
Electrical-Based Dimensional Metrology	M. Cresswell	(301) 975-2072	michael.cresswell@nist.gov
X-Ray and Neutron Small Angle Scattering-Based Dimensional Metrology	R. Jones E. Lin W. Wu	(301) 975-4624 (301) 975-6743 (301) 975-6839	ronald.jones@nist.gov eric.lin@nist.gov wen-li.wu@nist.gov
Model-Based Linewidth Metrology	J. Villarrubia A.E. Valadar M. Postek	(301) 975-3958 (301) 975-2399 (301) 975-2299	john.villarrubia@nist.gov andras.valadar@nist.gov michael.postek@nist.gov
Thin Film and Shallow Junction Metrology Program			
Two- and Three-Dimensional Profiling	J. Kopanski J. Marchiando D. Simons G. Gillen	(301) 975-2089 (301) 975-2088 (301) 975-3903 (301) 975-2190	joseph.kopanski@nist.gov jay.marchiando@nist.gov david.simons@nist.gov greg.gillen@nist.gov
Boron and Nitrogen Thin Film and Implant Standards Using Neutron Depth Profiling	G.P. Lamaze H. Chen-Mayer	(301) 975-6202 (301) 975-3782	george.Lamaze@nist.gov heather.chen-mayer@nist.gov
Gate Dielectric Metrology	E. Vogel J. Suehle J. Ehrstein C. Richter E. Steel N.V. Nguyn	(301) 975-4723 (301) 975-2247 (301) 975-2060 (301) 975-2082 (301) 975-3902 (301) 975-2044	eric.vogel@nist.gov john.suehle@nist.gov james.erhstein@nist.gov curt.richter@nist.gov eric.steel@nist.gov nnguyen@nist.gov
Chemical Metrology of Materials and Particle Contamination	C.J. Powell E. Steel	(301) 975-2534 (301) 975-3902	cedric.powell@nist.gov eric.steel@nist.gov

Project Title	Technical Contacts	Phone Number	Email Address
Thin Film X-ray Metrology for Microelectronics	R. Matyi	(301) 975-4272	richard.matyi@nist.gov
Interconnect and Packaging Metrology Program			
Superconformal Deposition of Copper and Advanced Interconnect Materials	T. Moffat D. Josell	(301) 975-2143 (301) 975-5788	thomas.muffat@nist.gov daniel.josell@nist.gov
Porous Thin Films Metrology for Low-k Dielectrics	B. Bauer W. Wu	(301) 975-6849 (301) 975-6839	barry.bauer@nist.gov wen-li.wu@nist.gov
Tomography with Scanning Transmission Electron Microscope Images	Z. Levine	(301) 975-5453	zachary.levine@nist.gov
Wire Bonding to Cu/Low-k Semiconductor Devices	G. Harman C. Johnson	(301) 975-2097 (301) 975-6409	george.harman@nist.gov christian.johnson@nist.gov
Solders and Solderability Measurements for Microelectronics	F. Gayle C. Handwerker M. Williams	(301) 975-2659 (301) 975-6158 (301) 975-6170	frank.gayle@nist.gov carol.handwerker@nist.gov maureen.williams@nist.gov
Interconnect Materials and Reliability Metrology	D. Read R. Keller M. Gaitan	(303) 497-3853 (303) 497-7651 (301) 975-2070	read@boulder.nist.gov keller@boulder.nist.gov michael.gaitan@nist.gov
Thermal Measurements and Packaging Reliability	A. Slifka E. Drexler D. Blackburn	(303) 497-3744 (303) 497-5350 (301) 975-2068	slifka@boulder.nist.gov drexler@boulder.nist.gov david.blackburn@nist.gov
Advanced IC Interconnects – Process Metrology and Models	J.E. Maslar R. Davis D.R. Burgess	(301) 975-4182 (301) 975-2739 (301) 975-2614	james.maslar@nist.gov ronald.davis@nist.gov donald.burgess@nist.gov
Dielectric Metrology Supporting Integrated Passive Device Technology	J. Obrzut	(301) 975-6845	jan.obrzut@nist.gov
Wafer Characterization and Process Metrology Program			
Wafer and Chuck Flatness Metrology	U. Griesmann	(301) 975-4929	ulf.griesmann@nist.gov
Modeling, Measurements, and Standards for Wafer Surface Inspection	T. Germer G. Mulholland M. Winchester	(301) 975-2876 (301) 975-6695 (301) 975-3886	thomas.germer@nist.gov george.mulholland@nist.gov michael.winchester@nist.gov
High-Resolution Microcalorimeter X-Ray Spectrometer for Chemical Analysis	K. Irwin S. Nam G. Hilton	(303) 497-5911 (303) 497-3148 (303) 497-5679	irwin@boulder.nist.gov names@boulder.nist.gov hiltong@boulder.nist.gov
Thermophysical Property Data for Modeling CVD Processes and for the Calibration of Mass Flow Controllers	J.J. Hurly M. Moldover	(301) 975-2476 (301) 975-2459	john.hurly@nist.gov michael.moldover@nist.gov
Temperature Measurements and Standards for Rapid Thermal Processing	K. Kreider D. P. DeWitt	(301) 975-2619 (301) 975-4199	kenneth.kreider@nist.gov david.dewitt@nist.gov
Low Concentration of Humidity Standards	J. Hodges G. Scace	(301) 975-2605 (301) 975-2626	joseph.hodges@nist.gov gregory.scace@nist.gov
Plasma Process Metrology	M. Sobolewski K. Steffens E. Benck	(301) 975-2980 (301) 975-2656 (301) 975-3697	mark.sobolewski@nist.gov kristen.steffens@nist.gov eric.benck@nist.gov
Measurements for Vacuum Process Control	R.F. Berg A. Lee	(301) 975-2466 (301) 975-2857	robert.berg@nist.gov albert.lee@nist.gov

Project Title	Technical Contacts	Phone Number	Email Address
Test Metrology Program			
Metrology for System-on-a-Chip (SOC)	B. Michelet A. Hefner	(301) 975-8777 (301) 975-2071	robert.michelet@nist.gov hefner@nist.gov
Non-Linear Device Characterization	D. DeGroot	(303) 497-7212	degroot@boulder.nist.gov
At-Speed Test of Digital Integrated Circuits	D. Williams J. Moreland J. Kopanski P. Kabos	(303) 497-3138 (303) 497-3641 (301) 975-2089 (303) 497-3997	dylan@boulder.nist.gov moreland@boulder.nist.gov joseph.kopanski@nist.gov kabos@nist.gov
Jitter and Propagation Delay Measurement	N. Paulter D. Larson D. Bergman	(301) 975-2405 (301) 975-2437 (301) 975-4464	npaulter@nist.gov larson@nist.gov dbergman@nist.gov
Manufacturing Support			
NIST/SEMATECH Engineering Statistics Internet Handbook	W. Guthrie A. Heckert	(301) 975-2854 (301) 975-2899	william.guthrie@nist.gov alan.heckert@nist.gov
Supply Chain Communication and Automation Needs Assessment of the Semiconductor Industry	Ya-Shian Li B. Goldstein	(301) 975-5319 (301) 975-2304	yashian@nist.gov barbara.goldstein@nist.gov

Note: Project Lead is highlighted in gray.

Division/Office Publication Editor:	Michele L. Buckley
Publication Coordinator:	Gaylen R. Rinaudot
Printing Coordinators:	Warren Overman Verna M. Moore
Document Production:	Technology & Management Services, Inc. Gaithersburg, Maryland

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For additional information contact:
Telephone: (301) 975-4400
Facsimile: (301) 975-6513
On the Web: http://www.eeel.nist.gov/omp/