National Institute of
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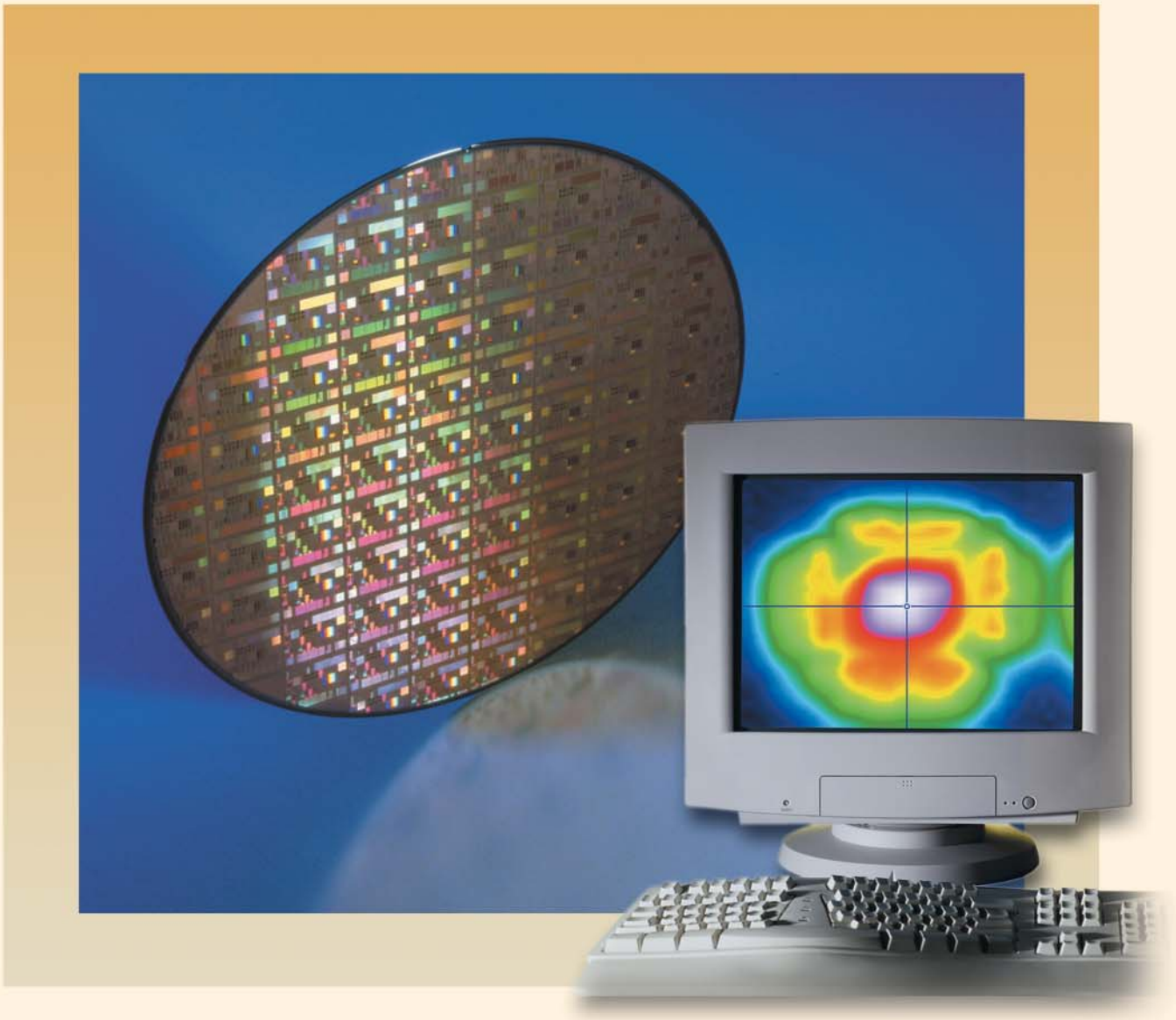
January 2003

Electronics and Electrical Engineering Laboratory

Semiconductor Electronics Division

Programs, Activities, and Accomplishments



The Electronics and Electrical Engineering Laboratory (EEEL)

One of NIST's seven measurement and standards laboratories, EEEL conducts research, provides measurement services, and helps set standards in support of the fundamental electronic technologies of semiconductors, magnetics, and superconductors; information and communications technologies, such as fiber optics, photonics, microwaves, electronic displays, electronics manufacturing supply chain collaboration; forensics and security measurement instrumentation; fundamental and practical physical standards and measurement services for electrical quantities; maintaining the quality and integrity of electrical power systems; and the development of nanoscale and microelectromechanical devices. EEEL provides support to law enforcement, corrections, and criminal justice agencies, including homeland security.

EEEL consists of six programmatic divisions and two matrix-managed offices:

Electricity Division

Semiconductor Electronics Division

Radio-Frequency Technology Division

Electromagnetic Technology Division

Optoelectronics Division

Magnetic Technology Division

Office of Microelectronic Programs

Office of Law Enforcement Standards

This publication describes the technical programs of the Semiconductor Electronics Division. Similar documents describing the other Divisions and Offices are available. Contact NIST/EEEL, 100 Bureau Drive, MS 8100, Gaithersburg, MD 20899-8100, telephone 301-975-2220, http://www.eeel.nist.gov. These publications are updated biennially.

Cover caption: (front to back) a thermal image of a MEMS-based hotplate during a transient event and an IBM 200 mm EDRAM Wafer (photo by Tom Way, courtesy of International Business Machines Corporation. Unauthorized use not permitted.).

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U.S. DEPARTMENT OF COMMERCE
Donald L. Evans, Secretary

Technology Administration
Phillip J. Bond, Under Secretary of Commerce for Technology

National Institute of Standards and Technology
Arden L. Bement, Jr., Director

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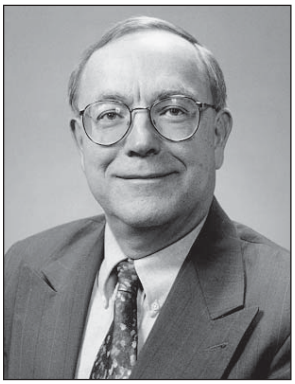


David G. Seiler,
Division Chief

"The Semiconductor Electronics Division has played a key role in the phenomenal growth of the semiconductor industry and in helping U.S. companies maintain leadership in the development and manufacture of silicon and compound semiconductors. NIST continues to provide the state-of-the-art measurement capabilities and standards necessary to support industry's ongoing efforts to push physical and chemical limits in the production of new devices and processes."

NRC Panel Report, An Assessment of the National Institute of Standards and Technology Measurement and Standards Laboratories: Fiscal Year 2001

Welcome

The Semiconductor Electronics Division (SED) provides leadership in developing the semiconductor measurement infrastructure essential to improving U.S. economic competitiveness. It provides necessary measurements, physical standards, and supporting data and technology; associated generic technology; and fundamental research results to industry, government, and academia. The primary mission of the Division is to provide the measurement infrastructure to U.S. industry for mainstream silicon CMOS (complementary metal-oxide semiconductor) technology. The Division's programs also respond to industry measurement needs related to MicroElectroMechanical Systems (MEMS), power electronics, and compound semiconductors.

The Division has extensive interactions with individual companies, industry organizations, and professional societies; these activities enable the development of a research agenda responsive to the needs of industry. Active participation in industry roadmapping, such as the Semiconductor Industry Association's International Technology Roadmap for Semiconductors, and standards activities, such as committee work for the American Society for Testing and Materials, is practiced by the Division to prioritize and establish programs with the highest potential impact. The Division widely disseminates the results of its research, especially in the areas of standardized test methods and Standard Reference Materials (SRMs), through a variety of channels: publications, software, conferences and workshops, and participation in standards organizations and consortia. NIST also actively seeks industrial, academic, and non-profit research partners to work collaboratively on projects of mutual benefit.

The Division, with a staff of about 70 including full-time and part-time employees as well as guest researchers, is based in Gaithersburg, Maryland. The Division is one of six divisions within the Electronics and Electrical Engineering Laboratory at NIST. The Division's technical activities are organized into four groups: the Materials Technology Group, the Advanced Microelectronics Technology Group, the Device Technology Group, and the IC Technology Group. The Division assists industry by providing tools such as SRMs, test chips, standard reference data, and software that support the needed measurement infrastructure. Division personnel visit industrial sites, host a variety of visitors, and make available tutorial material on an as-needed basis. We also are active in conference and workshop activities that directly benefit the industry. The Division receives and is responsive to hundreds of special requests for assistance from industry each year.

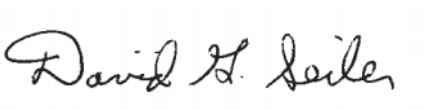
A broad array of activities that serve the semiconductor industry is currently underway in the Division. The staff of the SED addresses projects ranging from materials qualification to test structures for integrated circuits. Some of these projects are supported by the NIST National Semiconductor Metrology Program (NSMP), which is managed by the Electronics and Electrical Engineering Laboratory's Office of Microelectronic Programs. For more information on the NSMP, go to www.eeel.nist.gov/omp.

The Division, in cooperation with the National Research Council (NRC), offers awards for post-doctoral research for U.S. citizens in a variety of fields related to the semiconductor electronics industry. For additional details, including field descriptions and qualification guidelines, please see page 34.

The technical programs, activities, and accomplishments described here for each Division project clearly demonstrate the impact of the SED's leadership and effective service as it continues to respond to the needs of industry and to contribute to the scientific and engineering communities.

Please take an opportunity to visit our Division Web site at www.eeel.nist.gov/812/. In addition to providing further details on our Division and up-to-date project information, our Web site has interactive tutorials on the Hall effect (www.eeel.nist.gov/812/hall.html) and MEMS standard test structures based on e-standards (www.eeel.nist.gov/812/test-structures/).

Thank you for your interest in our Division! I welcome your comments and suggestions. Feel free to e-mail me at david.seiler@nist.gov.



David G. Seiler
Division Chief

Semiconductor Electronics Division Staff

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On the Web: www.eeel.nist.gov/812/

"The nature of the vision's purpose is not only to achieve a meaningful strategic or company goal, but also to build a dedicated community"

Jay A. Conger, The Brave New World of Leadership Training, IEEE Eng. Mgmt. Review (1996)

Mission

The **Semiconductor Electronics Division** provides leadership in developing the semiconductor measurement infrastructure essential to improving U.S. economic competitiveness by providing necessary measurements, physical standards, and supporting data and technology; associated generic technology; and fundamental research results to industry, government, and academia. The primary focus is on mainstream silicon CMOS (complementary metal-oxide semiconductor) technology. The Division's programs also respond to industry measurement needs related to MicroElectroMechanical systems (MEMS), power electronics, and compound semiconductors.

Vision

The **Semiconductor Electronics Division** is recognized as a dynamic world-class resource for semiconductor measurements, data, models, and standards focused on enhancing U.S. technological competitiveness in the world market.

Values

The **Semiconductor Electronics Division** values its commitment to identify and to meet crucial measurement technology needs. The Division values its collaboration with all segments of the semiconductor community. It strives for integrity, excellence, objectivity, responsiveness, and creativity, while maximizing and utilizing the potential of its employees.

The Division mission, vision, values, and goals were developed by a strategic planning process facilitated by a professional consultant. This process involved extensive workforce involvement, the Division leadership, and numerous meetings and informal discussions.

Goals

The Division will:

- Aggressively pursue and achieve select metrology needs as identified in the International Technology Roadmap for Semiconductors for mainstream silicon.
- Develop new and improved process-monitoring tools, methodologies, and data for the more efficient manufacture of silicon and compound-semiconductor devices.
- Develop cooperative, multidisciplinary projects within the Division and synergistic external collaborative efforts to better meet the critical needs of the semiconductor industry.
- Support novel research that has high potential for providing breakthroughs in materials, process, devices, and measurement technologies for the semiconductor industry.

Semiconductors: Backbone of the Electronic/Digital Revolution

"This year the semiconductor industry will manufacture about 60 million transistors for every man, woman and child on earth. By 2008, chipmakers will be producing 1 billion transistors or more per year. Transistors improve our lives in countless ways—they make cars safer and more fuel-efficient, they enable personal communication devices, they promote medical breakthroughs and they improve the quality of education."

- Building Blocks for Innovation, Semiconductor Industry Association (SIA) Annual Report 2002, p. 17

For the past 20 years, the personal computer reigned supreme as the driver of semiconductor industry growth. But new leadership is emerging. The communications revolution, perhaps the defining social and economic transition of our time, is fueled by the ever smaller, ever cheaper, ever faster invention of the chip industry. The explosive demands of the wireless, broadband Internet and optical networking industries have crowned the communications chip as the dominant end market for semiconductors.

- Information technology (IT) continues to be the primary driver of the U.S. economy, and U.S. semiconductor companies are leading the charge. American chipmakers now supply nearly half of the world's chips.
- U.S. chipmakers add more value to the national economy than any other industry.
- For 50 years, the semiconductor industry has provided the bricks and mortar that built the modern world. The exciting expansion in semiconductor applications means our job has only just begun and that our industry's greatest growth lies ahead.
- Personal communications devices will become so functional as to be indispensable, cars will be safer and more fuel-efficient, the quality of education will improve, chips implanted in our bodies will tell our doctor we're sick before we register symptoms. Eventually silicon and biology will converge, and the biocomputer will seem no more novel than today's laptop. As *Forbes ASAP* Editor Michael Malone has noted, "the microprocessor is the defining invention of the electronic age, the inventor of inventions."

- adapted from the Semiconductor Industry Association (SIA) 2001 Annual Report, pp. 2-5.

Semiconductors, transistors, and their applications represent one of the greatest scientific and technological breakthroughs of the twentieth century. Consider their far reaching influence on our society in general and our daily lives. Can you imagine life without them? Semiconductors are pervasive in the microelectronic components used in computers, entertainment equipment, automotive electronics, medical instrumentation, telecommunications, space technology, television, radio, cell phones, and many other information technologies. Every hospital, school, factory, car, airplane, office, bank, and household contains transistors, microprocessors, and other semiconductor devices.

These breakthroughs are possible because of the miniaturization of the transistor dimensions, which allows the construction of compact systems with tremendous computing power and memory. Miniaturization, in turn, is possible because of the perfection of fabrication techniques that allow the "integration" of circuits and thus the production of chips containing millions of elements per square centimeter. The foundation stone of this complex technology is silicon. Meeting the demands for these large-scale, complex, integrated circuits (ICs) continues to require technological advances in materials, processing, circuit design, characterization, testing, and standards.

"No other human invention is the equal of the semiconductor device - if only because no other invention has been adopted so quickly and pervasively as the integrated circuit. Since the invention of the planar process forty years ago, billions of transistors are now in use beneath, around and above the earth. The microprocessor is the defining invention of the electronic age, the inventor of inventions from the personal computer to the internet."

The Silicon Century, Semiconductor Industry Association (SIA) Annual Report and Directory 2000

"Private sector and government collaboration is essential to our continued progress. For example, the National Institute of Standards and Technology is developing standards for measuring the ever-shrinking line widths that characterize semiconductor products. Industry alone cannot develop these new standards—government must oversee the process."

Building Blocks for Innovation, Semiconductor Industry Association (SIA) Annual Report 2002, p. 20.

The semiconductor electronics industry is outstripping the measurement capability needed for maintaining and improving U.S. international competitiveness. Important factors affected include product performance, price, quality, compatibility, and time to market. The Division provides the measurement capability needed to support the efforts of U.S. industry to improve its competitiveness. In order to support this effort, the Division also engages in technology development and fundamental research, and makes the findings available to industry.

The Division focuses the largest part of its resources on the development and delivery of measurement capability for two principal reasons: measurement capability has a very high impact on U.S. industry because it helps manufacturers address many of the challenges they face in realizing competitive products in the marketplace, and NIST is the official lead U.S. Government agency for measurements.

The Division focuses on developing measurement capability that is beyond the reach of the broad range of individual companies. Companies seek NIST's help for several reasons:

- The companies need NIST's special technical capability for measurement development.
- The companies need NIST's acknowledged impartiality for diagnosing a measurement problem affecting the industry broadly or for achieving adoption of a solution across the industry.
- The companies cannot develop the measurement capability needed by the industry broadly because they cannot individually capture the returns of the cost of development.
- Industry's quality standards require that key measurements be traceable to the national measurement reference standards that NIST maintains. This is a requirement of growing importance in export markets.

The Division continues to interact and collaborate with a wide variety of companies, consortia [such as International Semiconductor Manufacturing Technology (ISMT), Semiconductor Equipment and Materials International (SEMI), and the Semiconductor Research Corporation (SRC)], academia, and other government labs to accomplish its mission. Specific details are given in the project sheets that follow. Work in the Division results in extensive outputs or deliverables that cover knowledge and improvements in physical understanding, test methods and measurements, Standard Reference Materials (SRMs), Standard Reference Data (SRD) sets, standards, test structures and test chips, software, measurement accuracy and traceability, publications and reports, patents and Cooperative Research and Development Agreements (CRADAs), round robins, data and models, talks and short courses, company visits, conferences and workshops, consortia participation, and various activities and leadership roles on committees and working groups.

Division staff serve the semiconductor community in leadership roles on standards committees such as American Society for Testing and Materials (ASTM) and Electronic Industries Alliance (EIA) / Joint Electron Device Engineering Council (JEDEC), societies such as IEEE, ECS, and APS, and on numerous semiconductor conferences/workshops. Many test methods and standards have been developed and written over the years by NIST staff for ASTM and EIA/JEDEC, including ones for resistivity, oxygen in silicon, thin dielectrics, electromigration, and device characterization. Staff serve on various Technical Working Groups to help put together the International Technology Roadmap for Semiconductors (ITRS). These groups are Process Integration, Devices, and Structures; Assembly and Packaging; Lithography; Interconnect; and Front End Processes. The ITRS provides targets for equipment, material, and software suppliers; provides targets for researchers; and serves as a common reference for the semiconductor industry.

The Division also has impacted the semiconductor community by producing a number of SRMs. To date, over 2,500 SRMs have been sold and distributed for resistivity, oxygen in silicon, and optical thickness by ellipsometry. Hundreds of companies throughout the world have purchased these SRMs to maintain and improve their measurement capability.

Semiconductor Electronics Division Organization

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2044 NGUYEN, Nhan V.
2082 RICHTER, Curt A.
2065 RICKS, Donnie R.

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2071 HEFNER, Allen R., Jr.
4709 JOSHI, Yogendra K. (GR)
2056 LAI, Jih-Sheng (GR)
2056 MANTOOTH, Homer (GR)
8776 McNUTT, Ty R. (GR)
2056 NOAMAN, Bassam
5967 REICHL, John V. (GR)
8751 TIGLI, Onur (GR)

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2056 ETINA, Natalya (S)
5484 GEIST, Jon (GR)
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4710 JAHN, Andreas (GR)
2049 MARSHALL, Janet C. (PT)
6367 MIJARES, Geraldine I.
2045 MORGAN, Nicole (PD)
6347 POLK, Brian (PD)
5466 REYES-HERNANDEZ, Darwin (PD)
4710 SWOPE, Bretton M. (S)
2056 WEI, Xiaojin (GR)

Legend:

AO = Administrative Officer
FA = Focus Area
FH = Faculty Hire
FL = Focus Area Leader
FM = Facility Manager
GL = Group Leader
GR = Guest Researcher
PD = Post-Doctoral Appointment
PL = Project Leader
PT = Part Time
S = Student

Telephone numbers are: (301) 975-XXXX (the four digit extension as indicated)

Metrology for Systems-on-a-Chip (FA)

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2236 ELLENWOOD, Colleen E.
2071 HEFNER, Allen R., Jr.
8751 TIGLI, Onur (GR)
2239 ZAGHLOUL, Mona E. (FH)

Wire Bonding to Cu/Low-κ Semiconductor Devices (FA)

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IC Technology Group (812.04)

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2052 WILKES, Jane M., Secretary

Electrical Test Structure Metrology

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5026 ALLEN, Richard A.
4446 GHOSHTAGORE, Rho (GR)
8193 MURABITO, Christine E. (S)
5623 OWEN, James C.
2234 SCHAFFT, Harry A. (GR)
2182 YARIMBIYIK, Emre

Microfabrication Process Facility

2699 HAJDAJ, Russell (FM)
2096 JOHNSON, Eric S.

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PD = Post-Doctoral Appointment
PL = Project Leader
PT = Part Time
S = Student

Telephone numbers are:
(301) 975-XXXX (the four digit extension as indicated)

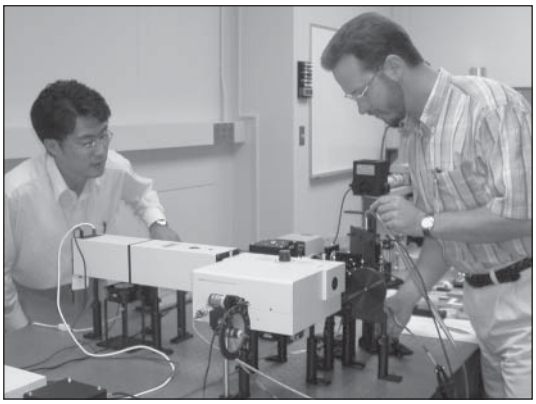
Scanning-Probe Microscope Metrology

Technical Contact:
Joseph J. Kopanski

Staff-Years (FY 2002):
3.5 professionals
5 guest researchers

Goals

Develop advanced scanning-probe and conventional electrical metrology techniques, models, and artifacts that are essential to improving semiconductor materials, processes, device performance, and reliability for the silicon and compound semiconductor industries. A current specific goal is to provide the technology computer-aided design (TCAD) community with quantitative two-dimensional dopant profiles to calibrate and enhance the predictivity of simulators.



Gyoung-Ho Buh (left) and Glen Birdwell (right) loading a sample onto the stage of the modulation/ surface photovoltage spectroscopy system.

Customer Needs

The Semiconductor Industry Association's (SIA's) International Technology Roadmap for Semiconductors (ITRS) identifies 2-D and 3-D carrier profiling as a key enabling technology for the development of next-generation integrated circuits. In 2003, it is desired to know 2-D carrier profiles with spatial resolution of 5 nm and with a precision (in concentration) of ±5 %; these demands increase to less than 1 nm and ±2 % by 2015. The Scanning Capacitance Microscope (SCM) has emerged as the leading contender to provide 2-D carrier profiles.

While SCMs are commercially available, techniques to interpret SCM images accurately have lagged. Much work remains to be done to develop 3-D physical models of scanning capacitance microscopy and techniques to use these models to extract quantitative carrier profiles from SCM images of differential capacitance. Likewise, the measurement methodology for quantitative scanning capacitance microscopy is still evolving. The need for, and form of, reference materials for scanning capacitance microscopy has yet to be defined.

Other scanning probe microscopy (SPM) based techniques for semiconductor metrology suffer similar problems; microscopes have been invented, but standard measurement and interpretation techniques are not available.

Technical Strategy

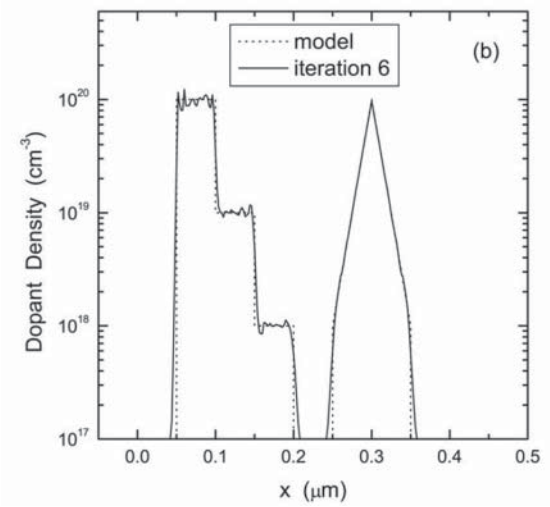
The Scanning-Probe Microscope Metrology Project is developing tools that are intended to enable scanning capacitance microscopes to function as two-dimensional dopant profiling tools. This work is divided into three tasks. Task 1 is development of SCM measurement methodologies. Best measurement practices are being determined via collaborative projects with industrial users and research into the physics of the silicon surface preparation. Task 2 is development of theoretical models of the SCM. The focus of our modeling effort has been to develop 2-D and 3-D finite-element solutions of Poisson's equation for the SCM geometry. Task 3 is interpretation of SCM data and technology transfer. Our expertise with interpreting SCM images is being transferred to industry through our software program *FASTC2D*. The program features an easy to use interface, rapid profile extraction, and operation in a Windows environment.

DELIVERABLES: By 2003, demonstrate optimized 3-D calculations of the SCM signal across dopant gradients and junctions.

Currently, the spatial resolution of 2-D dopant profiles measured with the SCM is limited by the tip size and by the data interpretation techniques. One way to overcome the tip size limitation may be to bevel the sample on a cross section, producing magnification both in depth and laterally. We have begun to investigate SCM measurements on beveled samples. While it is straightforward to produce a beveled cross section, carrier redistribution may raise new interpretation issues.

The version of *FASTC2D* currently available utilizes a calibration curve, determined from a database of pre-calculated solutions, which can very rapidly determine a 2-D carrier profile from an SCM image. When used in conjunction with Secondary Ion Mass Spectrometry (SIMS) measurements or a reference sample, relatively accurate profiles can be obtained. We have produced a series of "known good samples," which are intended to be used with *FASTC2D* in a tutorial teaching best measurement and data interpretation procedures.

DELIVERABLES: By 2004. improve spatial resolution of SCM measured dopant profiles by developing techniques to produce precisely beveled samples and techniques for their interpretation.



SCM regression solution matched to theoretical dopant profile. Regression solutions provided enhanced spatial resolution and accuracy over calibration curve methods.

A physically accurate 3-D model and determination of the dopant profile by an inverse solution are required to meet industrial needs for 2-D dopant profiling to the end of the ITRS. We have previously developed a quasi-3-D model of the SCM that predicts the essential behavior of the SCM measurement. However, for the required dopant profiling performance goals, a more rigorous approach is necessary. Towards this end, the finite element method has been employed to solve Poisson's Equation for the SCM geometry in three dimensions. Accuracy requirements may also force the consideration of quantum mechanical effects, necessitating the solution of the coupled Poisson and Schrödinger Equations. We are developing improved 3-D Poisson solvers using the LaGriT grid management toolbox in collaboration with Los Alamos National Laboratories.

An inverse solution of the SCM requires repeated solutions of the forward problem; i.e., calculation of the SCM signal from candidate carrier profiles. The candidate carrier profile is adjusted until a carrier profile is found that yields a calculated SCM signal that agrees with the measured SCM signal. Project staff have developed a regression procedure to do this with a 2-D solver. The final level of refinement is to use the full 3-D model as the basis of inverse solutions of the SCM. However, the volume of data to be processed and the time required for calculation make this intractable for routine profile extraction. Practical application requires finding shortcuts that will achieve the 3-D result without having to complete the entire round of 3-D simulations.

DELIVERABLES: By 2005, have available for distribution to users a computationally efficient method of determining carrier profiles from inverse solutions of scanning capacitance microscopy based on 3-D models.

The project is also actively investigating other SPM based characterization techniques. We plan to extend the SCM carrier profiling capacity to SiC and III-V semiconductors. Intermittent-contact scanning capacitance microscopy is sensitive to variations in the dielectric constant of thin films and can detect metal layers buried beneath insulating films. Optical pumping of scanning probe microscopes promises to allow determination of carrier recombination and generation lifetimes with unprecedented spatial resolution.

Accomplishments

■ *Progress in development of SCM 3-D regression solutions.* Developed a methodology for calculating the SCM signal by using the oxide-capacitance distribution to specify a natural boundary condition along the probed surface of the semiconductor sample, so that only the semiconductor substrate region needs to be discretized. This approach may lead to a dramatic increase in the speed of which 3-D solutions can be obtained.

■ *Developed techniques to optically pump scanning probe microscopes.* Dr. Gyoung-Ho Buh, guest researcher from the University of Seoul, Korea, has developed techniques to precisely optically pump scanning probe microscopes. The technique encompasses a GUI interface written in Visual C++ to precisely control a laser, lock-in amplifier, and digital oscilloscope to measure optically induced capacitance transients. Publications and a patent application are pending.

■ *Implemented advanced MOS models in FASTC2D.* Implemented new routines to calculate the SCM capacitance-voltage curve database using Fermi-Dirac statistics and either a classical or quantum mechanical model. This is the first implementation of a quantum mechanical correction to the C-V response for SCM data interpretation. Since SCM usually uses a very thin oxide, this is an important extension to previous practice.

■ *Developed software to simulate the dopant profile exposed on a beveled cross section.* The

BASSAR (for Bevel and Section Simulation and Reconstruction) software can (1) simulate 2-D profiles from input model parameters, (2) predict profiles that would be exposed at specified cross sectioning and bevel angles, and (3) recover the normal profile from an input profile measured on a beveled cross section.

■ *SPICE Simulation of SCM Capacitance Sensor.* Chi Tran, guest researcher from the University of California, Berkley, and Dr. Buh conducted SPICE simulations of an RCA style capacitance sensor confirming several previously unverified assumptions about the behavior of the SCM. A paper will be submitted to USJ-2003.

■ *Improved optical characterization facility.* Dr. Glen Birdwell has extended our photoreflectance capability from a room temperature only measurement, which covered a spectral range of 0.62 eV to 1.8 eV, to a continuously variable temperature system capable of measurements from 15 K to 300 K over a spectral range of 0.5 eV to 3.75 eV. In addition, further upgrades of the optics throughout the system now allow for surface photovoltage measurements from 0.5 eV to 5.6 eV. With these extended capabilities, we are able to investigate a large number of elemental and compound semiconductors. Investigations of antimony-based compounds and devices, transition metal silicides, and III-nitrides are currently in progress.

■ *Updated resistivity mapping system.* The rebuilt and updated system uses a Keithley source/measure unit (instead of an analog current source and voltmeter) and is controlled by Testpoint (instead of a DOS-based language). A switch matrix to enable simultaneous 2-pt and 4-pt measurements has been procured. A prototype process to produce the contact array and implement resistivity mapping of GaN substrates with 40 micrometer spatial resolution has also been developed.

FY Outputs

Collaborations

■ Agere Systems, Jack Hergenrother, Quantitative SCM of vertical replacement-gate transistors (Joseph J. Kopanski)

■ Air Force Research Laboratory, Materials and Manufacturing Directorate, WPAFB, Joe VanNostrand, MBE transferred to WPAFB, DARPA proposal submitted, samples exchanged (Thomas J. Shaffner)

■ ARL, Paul Amirtharaj, Guest Researcher, Optical characterization metrologies and OA funding strategy (Thomas J. Shaffner)

■ ARL, Paul Amirtharaj, optical characterization by surface photovoltage techniques (A. Glen Birdwell)

■ ATMI, Danbury, CT, George Brandes and Ed Hutchins, DARPA funded collaboration on III-nitride materials (Thomas J. Shaffner)

■ Atolytics Inc., Paul Weiss, State College, PA, Development of ac microwave scanning tunneling microscope, Dept. of Commerce SBIR (Joseph J. Kopanski)

■ Dynamic Research Corporation, SCM of actively biased SOI MOSFETs (Joseph J. Kopanski)

■ Freiberger, M/A-COM, Osemi, AXT, Picogiga, Emcore, Epitronics, IQE, Hall Round-Robin participants (W. Robert Thurber and Thomas J. Shaffner)

■ Imago Scientific Instruments Corporation, Madison, WI, Tom Kelly, Evaluation of position sensitive atom probe (Thomas J. Shaffner)

■ Manufacturing Instrumentation Consultant Company, Massood Tabib-Azar, Cleveland, OH, Co-axial AFM probes for near-field microwave and electrical measurements (Joseph J. Kopanski)

■ NIST ATP Evaluation Board (Thomas J. Shaffner)

■ NIST Division 814, Dick Harris, MBE transferred to Boulder (Thomas J. Shaffner)

■ NIST Division 815, Norman Sanford, Wide bandgap nitride materials metrology (A. Glen Birdwell and Thomas J. Shaffner)

■ NIST Division 836, Jim Maslar, Raman spectroscopy of wide bandgap nitride materials (Thomas J. Shaffner and A. Glen Birdwell)

■ NIST Division 852, Larry Robins, Optical metrology of wide bandgap nitride materials (Thomas J. Shaffner and A. Glen Birdwell)

■ NIST Division 855, Albert Davydov, Leo Bendersky, TEM of wide bandgap nitride materials (Thomas J. Shaffner and A. Glen Birdwell)

■ NIST Division 860, Harold Marshall, Strategy for OA funding (Thomas J. Shaffner)

■ NIST Division 841, Dan Pierce, Hall effect and resistivity measurements on GaAs (W. Robert Thurber)

- NIST Division 855, Albert Davydov and Leo Bendersky, Characterization of GaN defects and contacts (Joseph J. Kopanski)

- NIST Division 855, Albert Davydov, Hall effect and resistivity measurements on GaN (W. Robert Thurber)

- North Carolina State University, John Muth, Surface photovoltage analysis of III-nitride materials (A. Glen Birdwell)

- NRL, Brian Bennett, Analysis of InGaSb samples by surface photovoltage and photoreflectance (A. Glen Birdwell)

- Semiconductor Characterization Instruments, Inc., Fred Pollak, PR/SPV characterization and technique development (Thomas J. Shaffner and A. Glen Birdwell)

- TriQuint Semiconductor, Dallas, TX, Paul Saunier and Ed Beam, DARPA proposal submitted in joint collaboration and exchange of III-V and GaN samples (Thomas J. Shaffner and A. Glen Birdwell)

- University of Missouri-Rolla, Matt O'Keefe, and Wright State University, David Look, DARPA proposal submitted to in joint collaboration with NIST and WPAFB. Proposed work covered electron microscopy and electrical characterization of III-nitride and novel chalcopyrite materials (Thomas J. Shaffner)

- University of North Texas, Chris Littler/Terry Golden, Collaboration of GaAsSb by modulation spectroscopy metrology (A. Glen Birdwell)

- University of North Texas, Denton, TX, Chris Littler, Collaboration on III-V modulation spectroscopy metrology (Thomas J. Shaffner)

Recent Publications

J.J. Kopanski, "Capacitive Probe Microscopy," Encyclopedia of Imaging Science and Technology, pp. 16-31 (15-JAN-2002).

Advanced MOS Device Reliability and Characterization

Goals

To provide electrical and reliability measurement techniques, data, physical models, and fundamental understanding for ultra-thin silicon dioxide and alternate gate dielectrics in future Metal Oxide Semiconductor (MOS) devices. To increase the understanding of the relationship between the gate dielectric material/interface properties and device electrical and reliability measurements.

John Suehle loading a test wafer on a wafer prober for long-term dielectric testing.

Customer Needs

The Semiconductor Industry Association's (SIA's) International Technology Roadmap for Semiconductors indicates that the equivalent thickness of the gate dielectric will need to be 1.0 nm to 1.5 nm by 2004. Due to increased power consumption, intrinsic device reliability, and circuit instabilities associated with SiO_2 of this thickness, a high-permittivity gate dielectric (e.g., Si_3N_4, HfSixOy, ZrO_2) with low leakage current and at least equivalent capacitance, performance, and reliability will be required. The physics of failure and traditional reliability testing techniques must be re-examined for ultra-thin gate oxides that exhibit excessive tunneling currents and soft breakdown. Electrical characterization of MOS capacitors and Field Effect Transistors (FETs) have historically been used to determine device and gate dielectric properties such as insulator thickness, defect densities, mobility, substrate doping, bandgap, and reliability. Electrical and reliability characterization methodologies need to be developed and enhanced to address issues associated with both ultra-thin SiO_2 and alternate dielectrics including large leakage currents, quantum effects, and thickness dependent properties. As compared to SiO_2, very little is known about the physical or electrical properties of high dielectric constant gate dielectrics in MOS devices. The use of these films in Complementary Metal Oxide Semiconductor (CMOS) technology requires a fundamental understanding of the relationship between the gate dielectric material/interface and device electrical and reliability measurements.

Technical Strategy

The strategy of this effort will be to obtain or fabricate both device samples and blanket films, to perform reliability and electrical characterization of the devices, and to collaborate with other researchers to perform analytical characterization. Many issues such as tunnel/leakage current and spatially dependent properties associated with metal oxide and silicate dielectrics are also present in ultra-thin oxide and oxide-nitride stacked dielectrics. Therefore, many of the characterization schemes will first be developed on the simpler ultra-thin oxide and oxide-nitride dielectrics and then applied to the metal oxide and silicate dielectrics.

There are two main focus areas for this project. The first focus area investigates the physics of failure and the reliability testing techniques for ultra-thin SiO_2 and high dielectric constant gate dielectrics. The physical mechanism responsible for "soft" or "quasi" breakdown modes in ultra-thin SiO_2 and high-κ films and its implications for device reliability will be investigated as a function of test conditions and temperature. Long-term time-dependent-dielectric breakdown (TDDB) tests will be conducted on SiO_2 films and high-κ dielectrics with equivalent oxide thickness (EOT) as thin as 1.5 nm at electric fields close to operating conditions. These tests will be used to determine the thermal and electrical acceleration parameters of device breakdown.

DELIVERABLES: By 2003, studies of the long-term wear-out and breakdown of advanced high-κ dielectrics.

Experiments will be conducted to investigate the differences of gate oxide breakdown and wear-out due to high oxide field and hot-carrier injection. This study will provide insight into the physical

Technical Contact:
John S. Suehle

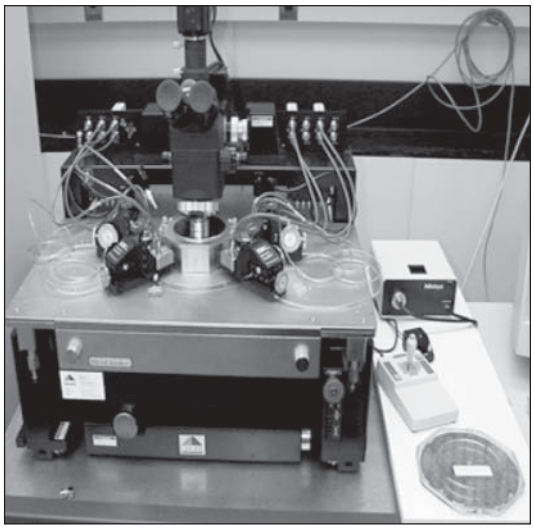
Staff-Years (FY 2002):
2 professionals
1 technician
3 guest researchers

mechanism of ultra-thin and high-κ gate oxide wear-out and breakdown.

DELIVERABLES: By 2003, experimental results of charge stability and trapping in HfO_2 films including defect generation rates due to constant voltage stress.

The understanding generated in this research will be used to continue generating standard measurements through a NIST-coordinated collaboration between EIA-JEDEC (Electronic Industries Association Joint Electron Device Engineering Council) and the ASTM (American Society for Testing and Materials). Studies on the reliability of high dielectric constant dielectrics also will be performed.

DELIVERABLES: By 2004, a new JEDEC standard, including guidelines for performing capacitance-voltage (CV), conductance-voltage (GV), and charge pumping measurements on ultra-thin SiO_2 and high-κ films for extracting parameters such as EOT, Interface State Density (D_{it}), V_{FB}, etc.



A low-noise (fA), high-temperature (300 °C) probe station is used to electrically characterize devices.

The second focus area investigates electrical measurement techniques, procedures, and analysis associated with devices having thin oxide and alternate gate dielectrics. The electrical measurement techniques that we are investigating include capacitance-conductance characterization, dielectric tunnel and leakage current characterization, and defect density measurements such as charge pumping and conductance. Furthermore, standard properties and mechanisms/correlations for these dielectrics, including defect centers, dielectric constant, defect generation rates, and leakage/tunnel current, will be characterized.

DELIVERABLES: By 2003, experimental studies on the effect of annealing and aluminum concentration on the charge trapping characteristics of HfO_2 gate dielectrics.

High-κ gate dielectric films will be obtained from key industrial and university groups. Electrical characterization methodologies will be developed to address various issues associated with these films, including large leakage currents, quantum effects, thickness dependent properties, large trap densities, transient (non-steady state) behavior, unknown physical properties, and the lack of physical models.

Examples of measurement problems that are being addressed include modifying and verifying electrical defect density measurement techniques, including conductance-frequency, capacitance-voltage, and charge-pumping.

Accomplishments

■ *New JEDEC document including noise-based test procedures for TDDB standard of sub-2 nm films.* The document includes new test methodologies for detecting soft or noisy breakdown events in ultra-thin gate dielectrics and is expected to be effective in detecting breakdown in films as thin as 1.5 nm. It has been approved by the JEDEC JC-14.2 Committee and is undergoing final ballot by the JEDEC Council. A round-robin experiment is currently being planned to investigate the effectiveness of the test procedure.

■ *Negative bias temperature instability studied for deep sub-micro p-MOS devices under pulsed bias stress.* Bias Temperature Instability (BTI) has become a serious reliability problem in deep sub-micron p-MOSFETs as device dimensions are continually scaled down. The ΔVth of negative bias temperature instability (NBTI) was observed to be significantly reduced for pulsed bias repetition frequencies greater than 10 kHz, implying an important role of hole trapping and detrapping. However, ΔVth of positive bias temperature instability (PBTI) was almost independent of frequency. The ΔVth did not show significant channel length dependency. These results suggested that there are different mechanisms for ΔVth of NBTI and NBTI, and the reliability specifications of NBTI could possibly be relaxed under certain pulsed operation conditions.

■ *A study was performed to investigate defect generation in ultra-thin silicon dioxide films over large fluence ranges.* The defect generation rate (P_g) during constant voltage stress was investigated

by using short-time voltage pulses over a large fluence range. It was found that P_g is not constant as a function of injected charge, and the voltage acceleration of P_g in the linear defect generation regime is similar to that of the reciprocal of Q_{BD}. The change of carrier capture cross (σ) during defect generation was speculated as one of the reasons responsible for the change of P_g value. However, from this preliminary report, we have determined that the change of P_g cannot be explained by the change of σ.

■ *A Visual Basic MOS simulation code was developed based on first-order approximations for the quantum mechanical (QM) effects.* The code, which permits us to evaluate experimental and simulation parameters on CV characteristics quickly, was developed. Comparisons with full Schroedinger-Poisson solvers (UTQuant) showed good agreement over a large range of experimental conditions (t_{ox} = 1.0 nm to 2.0 nm, Nsub = 10^{15} cm^{-3} to 10^{18} cm^{-3}). The results show that a model based on the modification of the total semiconductor charge can be used to simulate QM CV characteristics of polysilicon-gated MOS devices.

The effects of a distribution of interface states with energy on the CV characteristics can be simulated. Further work on the impact of bulk insulator defects (slow states), EOT extraction, etc. can now begin. The code is currently being used in collaboration with J. Kopanski in *FASTC2D* applications.

CV-software was completed which permits simulation of the frequency dependent interface state capacitance. The software was transferred to, and is being used by, International SEMATECH.

■ *A joint collaboration between NIST and the Jet Propulsion Laboratory (JPL) investigated what effect ionizing radiation experienced in deep space missions will have on the reliability of ultra-thin gate dielectrics.* It has been previously reported that heavy ion bombardment can cause radiation-induced soft breakdown (RSB) in ultra-thin gate dielectrics. Constant voltage TDDB distributions were obtained for both un-irradiated and irradiated 3.0 nm and 3.2 nm thick SiO_2 films subjected to ^{60}Co gamma irradiation and heavy ions of 823 MeV ^{129}Xe (Linear Energy Transfer, LET = 59 MeV cm^2/mg). The gamma irradiation had no effect on oxide lifetime. Under heavy ion irradiation, lifetime degradation was observed for devices with zero gate voltage applied, suggesting that even powered down circuits may be at risk for long-term missions in ionizing radiation environments. The reduction of oxide lifetime under constant-voltage stress conditions was a strong function of the heavy ion fluence.

FY Outputs

Collaborations

- Advanced Micro Devices, Ultra thin oxide reliability (John S. Suehle)
- Agere Technologies, Ultra-thin gate oxide reliability (John S. Suehle)
- Analog Devices, Limerick, Ireland, Ultra-thin gate oxide reliability (John S. Suehle)
- The George Washington University, Microhotplate-based chemical sensors (John S. Suehle)
- Motorola, Ultra-thin gate oxide reliability (John S. Suehle)
- N.C. State University (oxynitrides, nitrides, ultra-thin SiO_2), Alternative gate dielectrics (Eric M. Vogel)
- National Semiconductor, Ultra-thin gate oxide reliability (John S. Suehle)
- NIST Division 836, Microhotplate-based sensor arrays (John S. Suehle and Michael Gaitan)
- NIST Divisions 836, 837, 838, Dr. Roger van Zee et al., Molecular Electronics Competence Project (Curt A. Richter and John S. Suehle)
- NIST Divisions 836, 837, 838, Roger Van Zee, et al., Spectroscopic ellipsometry of molecular electronics (Nhan V. Nguyen, Curt A. Richter, and John S. Suehle)
- Penn State University, Ultra-thin gate oxide reliability (John S. Suehle)
- Sharp Microelectronics, Dr. John Conley, Characterization of Hafnium-oxide dielectric films (James R. Ehrstein and John S. Suehle)
- Texas Instruments, Electrical and reliability characterization of ultra thin gate oxides (John S. Suehle and Curt A. Richter)
- Texas Instruments, Ultra-thin gate oxide reliability (John S. Suehle)
- The Pennsylvania State University, Molecular electronics (Curt A. Richter and John S. Suehle)
- University of Delaware, Alternative dielectrics (John S. Suehle)

- University of Maryland, College Park, Micro-hotplate-based chemical sensors (John S. Suehle)

- University of Maryland, College Park, Ultra-thin gate oxide reliability (John S. Suehle)

- University of Maryland, Gate dielectric reliability (Eric M. Vogel)

- University of Minnesota, Alternate Gate Dielectrics (Eric M. Vogel)

Standards Committee Participation

- JEDEC JC14.2 Committee on Wafer-Level Reliability, Dielectric Working Group, Chairman (John S. Suehle)

Recent Publications

J.F. Conley, J.S. Suehle, A.H. Johnston, B. Wang, T. Miyahara, E.M. Vogel, J.B. Bernstein, "Heavy Ion Induced Soft Breakdown of Thin Gate Oxides," IEEE Trans. on Nuclear Science, Vol. 48, No. 6, pp. 1913-1916, (01-DEC-2001).

C.A. Richter, J.S. Suehle, M.D. Edelstein, O. Kirillov, R.D. van Zee, "Molecular Electronic Test Structures," Bulletin of the American Physical Society, Vol. 47, No. 1, pp. 285-285, (01-MAR-2002).

J.S. Suehle, "Ultra-Thin Gate Oxide Reliability: Physical Models, Statistics, and Characterization," IEEE Trans. on Electron Dev., Vol. 49, No. 6, pp. 958-971, (01-JUN-2002).

J.S. Suehle, B. Wang, J.F. Conley, E.M. Vogel, P. Roitman, C.E. Weintraub, A.H. Johnston, J.B. Bernstein, "Observation of Latent Reliability Degradation in Ultra-Thin Oxides after Heavy-Ion Irradiation," Applied Physics Letters, Vol. 80, No. 7, pp. 1282-1284, (18-FEB-2002).

E.M. Vogel, D. Heh, J.B. Bernstein, "Interaction Between Low-energy Electrons and Defects Created By Hot Holes in Ultra-Thin Silicon Dioxide," Applied Physics Letters, Vol. 80, No. 18, pp. 3343-3345, (06-MAY-2002).

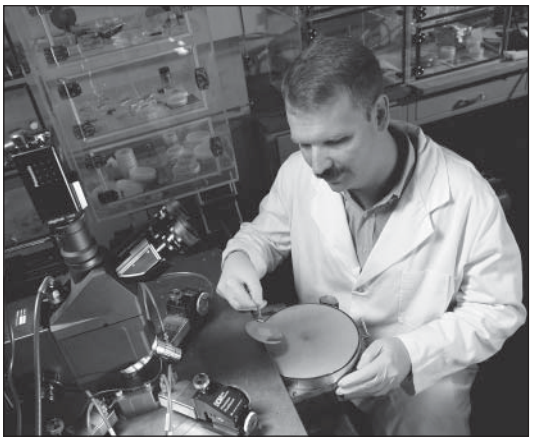
E.M. Vogel, M.D. Edelstein, J.S. Suehle, "Reliability of Ultra-Thin Silicon Dioxide Under Substrate Hot-Electronic, Substrate Hot-Hole, and Tunneling Stress," Microelectronics Engineering, pp. 1-11, (01-NOV-2001).

C.E. Weintraub, E.M. Vogel, J.R. Hauser, N. Yang, V. Misra, J.J. Wortman, J.J. Ganem, P. Masson, "Study of Low-Frequency Charge Pumping on Thin Stacked Dielectrics," IEEE Transactions on Electron Devices, Vol. 48, No. 12, pp. 2754-2762, (01-DEC-2001).

Nanoelectronic Device Metrology

Goals

The overall goal of the Nanoelectronic Device Metrology (NEDM) Project is to develop the metrology that will help enable new nanotechnologies (such as molecular electronics and Si-based quantum devices) to supplement and/or supplant conventional Complementary Metal Oxide Semiconductor (CMOS) devices. This involves determining the critical metrology needs for these exploratory technologies. One specific goal is to develop test structures and methods to measure reliably the electrical properties of small ensembles of molecules. A second targeted goal is to develop the precise metrology and characterization methods required for the systematic characterization of Si-based nanoelectronic devices.



Curt Richter loads a molecular electronic sample for electrical characterization. Copyright Robert Rathe

Customer Needs

The CMOS FET (Field Effect Transistor), which is the current basis of ULSI (Ultra-Large-Scale Integration) circuits, is beginning to show fundamental limits associated with the laws of quantum mechanics and the limitations of fabrication techniques. The Semiconductor Industry Association's (SIA's) International Technology Roadmap for Semiconductors (ITRS) shows no known solutions by 2005 for a variety of technological requirements including gate dielectric, gate leakage, and junction depth. Therefore, it is expected that entirely new device structures and computational paradigms will be required to augment and/or replace standard planar CMOS devices. Two post-CMOS technologies that show promise to extend traditional scaling laws for increased computational performance beyond the limits of conventional CMOS are molecular electronics and Si-based quantum electronic devices.

Molecular electronics (ME) is a field that many predict will have important technological impacts on the computational and communication systems of the future. In ME systems, molecules perform the functions of electronic components. Research and development for silicon-based nanoelectronics (e.g., wrap-around FETs, Si-based RTDs [resonant tunneling diodes], silicon quantum dots) for the post-CMOS era are currently of interest due to their inherent compatibility with CMOS technology.

The NEDM Project is concerned with fundamental research related to possible future devices that will replace or augment standard CMOS technology. In order to ensure that our research is technically relevant, we plan to align ourselves with research described by the Microelectronics Advanced Research Corporation (MARCO), alluded to in the SIA's Roadmap and other similar semiconductor industry organizations and documents.

The industry for these emerging nanoelectronic devices will require reference data, standards, precision measurement protocols, and standardized test structures and associated measurement protocols to develop into a viable commercial technology. The ultimate objective of this project is to provide the measurement infrastructure to aid this development. Through strong ties with industry leaders and cutting-edge researchers, we are accelerating the pace of our program and focusing our research on the most relevant technologies.

Technical Strategy

The NEDM Project investigates and is developing metrology for two specific areas of nanotechnology: molecular electronics and Si-based quantum electronics.

In ME, our major objectives are:

- A NIST standard suite of molecular test structures.
- Fundamental understanding of charge transport through molecules and molecular ensembles.

We plan to develop robust molecular test structures and use them to measure the electrical properties of molecules. Specifically, we are developing test-structures based upon nanofabrication and NEMS (Nano-Electro-Mechanical Systems)

Technical Contact:
Curt A. Richter

Staff-Years (FY 2002):
3.5 professionals
0.5 technician
2 guest researchers

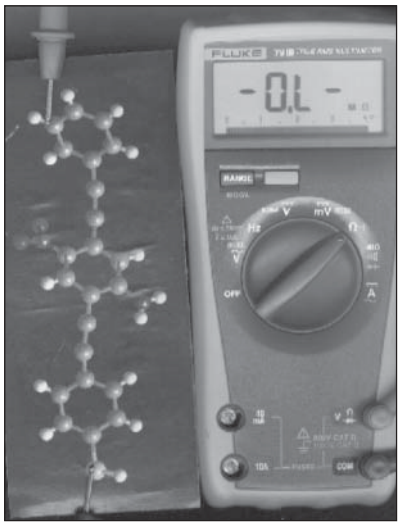
"…there is no particular reason why Moore's law should continue to hold: it is a law of human ingenuity, not of nature. At some point, Moore's law will break down. The question is when?"

Seth Lloyd, d'Arbeloff Laboratory for Information Systems and Technology, Massachusetts Institute of Technology

"If individual molecules can be made to process information, they could be the answer to the computer industry's prayers."

P. Ball, Consultant Editor, Nature, vol. 406, 13 July, 2000, pp. 118-120

processing techniques for assessing the electrical properties and reliability of moletronic molecules. (One example, the "nano-Bucket," is illustrated on page 12.) Molecules will be incorporated into the test structures via self-assembly to form high-quality SAMs (self-assembled monolayers). In addition to the complexity of the nanofabrication of test structures, the challenges associated with measuring the electrical properties (such as current-voltage and capacitance-voltage as functions of temperature and applied fields) of these small molecular ensembles are daunting. The measured electrical properties will be correlated with systematic characterization studies by a variety of advanced analytical probes and the results used in the validation of predictive theoretical models.



Electrically measuring molecules: the concept.

The new Si-nanotechnology effort will focus on physical and electrical metrology of the basic building blocks of silicon quantum electronic devices (e.g., quantum layers, wires, and dots of silicon surrounded by silicon dioxide). By identifying and addressing the critical metrology issues associated with these basic building blocks, the basis of metrology for future Si-based ULSI nanotechnology will be defined.

A major goal is to fabricate single quantum dots and wires with controllable size. These will be used to establish the relationship between the key fabrication conditions, physical properties (such as the geometry of the quantum-dot and the tunneling barrier), and final electrical properties of these floating silicon devices (i.e., metal-oxide-silicon-oxide-silicon [MOSOS] devices). Production of MOSOS capacitor structures is an intermediate step en route to this end goal. This research will provide the information necessary to help identify and address the necessary electrical and physical characterization methodologies.

Developing the metrology for "beyond-CMOS" nanoelectronic devices is a challenging and multidisciplinary task; therefore, it is important to be teamed with strong collaborators. The ME staff is part of a NIST Competence Project with the Chemical Science and Technology Laboratory (CSTL). CSTL provides the bulk of the molecules we will use, provides insights into SAM formation, performs precise structural characterization, and performs advanced quantum chemistry theoretical analysis. In addition, the ME team is working with various companies, universities, and government laboratories (e.g., Hewlett-Packard (HP), Yale University, University of North Texas, Naval Research Labs). The quantum Si device team is working closely with NIST's Electricity Division to study Si-based single-electron tunneling devices.

DELIVERABLES: By 2003, characterize and optimize preferred molecular electronic test structure (METS). NIST Special Publication and/or manuscript prepared and submitted.

DELIVERABLES: By 2003, correlation of the physical properties of self-assembled quantum dots with the processing parameters used to form them. Manuscript prepared and submitted.

DELIVERABLES: By 2005, complete a documented NIST standard suite of molecular electronic test structures.

DELIVERABLES: By 2005, quantum-dot memory field effect transistors (QD FETs): Experimental correlation of the final performance and electrical properties of QD FETs with the physical properties obtained from precise physical characterization. Manuscript prepared and submitted.

Accomplishments

■ *Establishing Infrastructure for the Nanoelectronic Device Metrology Project.* In FY 2002, the Nanoelectronic Device Metrology Project was established. Extensive plans were developed and funding was acquired for this project. There are three areas of infrastructure that have been improved: personnel, equipment, and funding. In addition to the joint CSTL/EEEL Molecular Electronics Competence (started FY01) and funding from the National Nanotechnology Initiative (started mid-year FY01), the NEDM Project is part of two recently funded ATP Intramural Awards (for 2002), "The Missing Plateau: Confined Silicon Devices for ULSI Nanotechnology," (EEEL/MSEL) and "Model-Guided Screening of Electrically-Active Molecules for Nanoelectronics" (CSTL/EEEL).

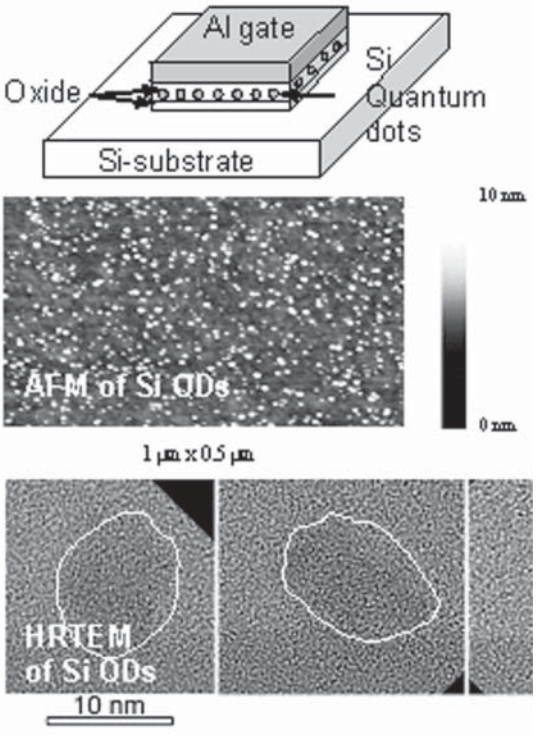
■ *Personnel.* Since Sep. 2001, four full-time researchers have joined the NEDM Project. Oleg A. Kirillov (a recent graduate of Rochester Institute of Technology's [RIT's] process engineering program) was hired as a processing engineer. Dr. Jin-Wan Park (Seoul National University) and Dr. Jin-Ping Han (Yale University) joined the NEDM Project as guest researchers and are concentrating their efforts on the Si-Based Quantum Devices Task. Dr. Christina Hacker (U. Wisconsin at Madison) most recently joined the NEDM Project as a post-doctoral candidate through the NRC Research Associate Program. Dr. Hacker is investigating hybrid Si/molecular technologies.

■ *Nanoelectronic Equipment Infrastructure.* A substantial portion of the first year was spent in vastly improving our nanoelectronic equipment infrastructure. A new backside mask aligner and an oil-free metal deposition system have been installed. The installation process is underway for a plasma deposition and etching system. This new equipment combined with our growing expertise and the existing capabilities (including electron-beam lithography) in the Microfabrication Process Facility, give us fabrication capabilities near the forefront of nanoelectronic research.

■ *Development of nano-Bucket Fabrication Processes.* Individual nano-Bucket devices have been fabricated. Key processing steps (that combine NEMS techniques with planar integrated circuit processing methods) have been developed for the nano-Bucket. The critical steps are suspension of thin Si membranes, electron-beam lithography to define the nanopore, base metal deposition, self assembly of a molecular monolayer, and deposition of metal on top of the molecules without destroying or electrically shorting through them.

■ *Prototypical Multiple-Quantum-Dot-Island Floating Body Devices.* Processing parameters have been established to reproducibly control the size distribution, concentration, and shape of silicon quantum dots formed using LPCVD (Low Pressure Chemical Vapor Deposition). Two methodologies for forming silicon quantum dots have been explored. The first is by direct deposition of polycrystalline quantum dots using LPCVD at short deposition times. The second is by deposition of thin amorphous silicon layers using LPCVD followed by annealing. Quantum-dot island floating body capacitors and transistors will be made by using these quantum dot formation techniques. A simple two-level capacitor mask set and a four-level mask set to fabricate field-oxide isolated, polysilicon gated, field effect transistors (FETs) have been designed and purchased. Working polysilicon gated capacitors (without the floating quantum dots) have been fabricated with gate oxide thicknesses of approximately 5 nm, and processes have been developed to form gate oxides with thicknesses of approximately 2 nm.

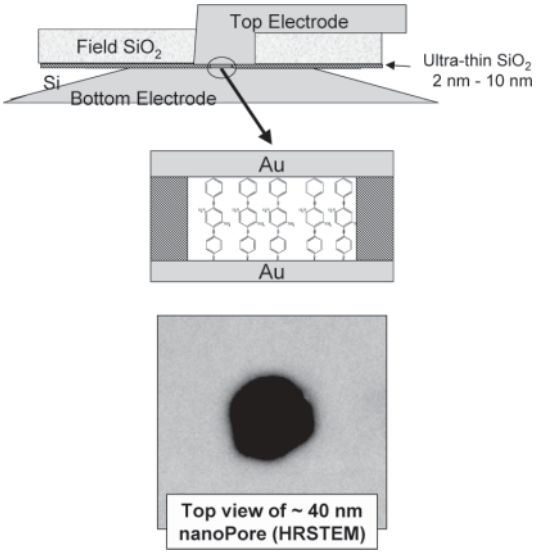
■ *Alternate Molecular Electronic Test Structures.* Initial assessment of the capabilities of alternate molecular electronic test structures (based upon cross bars) have been made. Cross-bar structures based upon shadow masks have been fabricated from a variety of metal systems (Au-Au, Al/AlOx-Al, Al-Pt) and electrically characterized by current-voltage and capacitance-voltage measurements. A working demonstration of "molecular doorbells," a prototype flip-chip test structure, has also been implemented. Fabrication processes were developed for these flip-chip structures and an apparatus was set up to apply a controllable, constant force to the flexible top layer to bring the top metal down to contact the base. Experimentally, the system was characterized without molecules (when the metals short). A monolayer of octadecanethiol was self assembled onto Au lines on a mica top electrode and electrically measured. The initial results — that the Au lines do not short — are promising.



Quantum dot floating island capacitor.

■ *Molecular Electronic Test Structure (METS) Assessment Methodology.* An effective test protocol was developed for METS to ensure that electrical results can be attributed to the molecules and are not an artifact of the test structure itself. Current-voltage curves were obtained for devices with no molecules and for devices containing long-chain alkane-thiols (such as octadecanethiol). These two limits, a conducting short and an insulating film in the nanopore, respectively, characterize the METSs and allow the properties of conducting molecules of interest to be measured reliably. In addition to applying this methodology to the METSs being fabricated in the NEDM Project, we apply these techniques to investigate METSs of other researchers. For example, we have characterized Si_3N_4-based nanopore devices in a collaboration with Yale University (M. A. Reed).

■ *Electrical Characterization of Molecules.* We developed an initial suite of electrical test procedures for molecular devices. In collaboration with HP Laboratories, we were the first researchers to independently confirm electrical current-voltage characteristics of moletronic devices supplied by HP. Also, we made the world's first ever capacitance-voltage characterizations of self-assembled molecules by using these structures from HP.



Schematic of the NIST "nano-Bucket" molecular test structure.

FY Outputs

Collaborations

■ Hewlett-Packard, R. Stanley Williams, Interface properties of molecular electronic test structures (Curt A. Richter)

■ Naval Research Laboratories, Ranganathan N. Shashidhar, Molecular test structure assessment (Curt A. Richter)

■ NIST Division 837, Dr. L. Richter, Optical characterization of semiconductor interfaces (Curt A. Richter)

■ NIST Division 837, John Henry Scott, high-resolution TEM studies of molecular test structures (Curt A. Richter)

■ NIST Divisions 836, 837, 838, Dr. Roger van Zee et al., Molecular Electronics Competence Project (Curt A. Richter and John S. Suehle)

■ NIST Divisions 836, 837, 838, Roger Van Zee, et al., Spectroscopic ellipsometry of molecular electronics (Nhan V. Nguyen, Curt A. Richter, and John S. Suehle)

■ The Pennsylvania State University, Molecular electronics (Curt A. Richter and John S. Suehle)

■ U. Texas at Austin, Prof. Jack Lee, Optical properties of ZrO_2 and HfO_2 for use as high-κ gate dielectrics (Curt A. Richter and Nhan V. Nguyen)

■ University of Maryland, L. Sita (Chemistry) and M. Faker (Physics), Single molecule test structure via electromigration (Curt A. Richter)

■ University of North Texas, Fast molecular electronic test structures (Curt A. Richter)

■ University of Wisconsin, Madison, Molecular monolayers on Si (Curt A. Richter)

■ Yale University, Prof. M. A. Reed, Robust molecular electronic test structures (Curt A. Richter)

External Recognition

Elevated to IEEE Senior Member status (Curt A. Richter)

Recent Publications

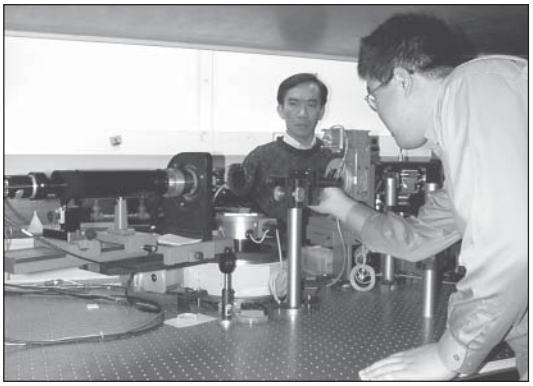
Y.J. Cho, N.V. Nguyen, C.A. Richter, J.R. Ehrstein, B.H. Lee, J.C. Lee, "Spectroscopic Ellipsometry Characterization of High-κ Dielectric HfO_2 Thin Films and the High-Temperature Annealing on Their Optical Properties," Applied Physics Letters, Vol. 80, No. 7, pp. 1249-1251, (18-FEB-2002).

C.A. Richter, J.S. Suehle, M.D. Edelstein, O. Kirillov, R.D. van Zee, "Molecular Electronic Test Structures," Bulletin of the American Physical Society, Vol. 47, No. 1, pp. 285-285, (01-MAR-2002).

Thin-Film Process Metrology

Goals

Develop new and improved electrical and optical measurements, models, data, and reference materials to enable better and more accurate measurements of select, critical, thin-film parameters for silicon Complementary Metal Oxide Semiconductor (CMOS) technology. Major focus is placed on requirements for oxynitrides, and metal-oxide and metal-silicate films and stacks for advanced gate dielectrics detailed in the International Technology Roadmap for Semiconductors (ITRS).



Nhan Van Nguyen (left) and Yong Cho (right) aligning a sample on a custom-built high-accuracy spectroscopic ellipsometer.

Customer Needs

The evolving decrease of the gate dielectric film thickness to an oxide-equivalent value of 1 nm is identified as a critical front-end technology issue in the Semiconductor Industry Association's (SIA's) ITRS. For effective gate dielectric thicknesses below ~2.0 nm, SiO_2 is being replaced, initially by oxynitrides or oxide/nitride stacks, and then by either metal-oxides or metal-silicates. Process control tolerance needs for dielectric thickness are projected to be ±4 % (3 σ), which translates to less than 0.1 nm for 2 nm films. Requirements for process control measurements are a factor of ten smaller.

Spectroscopic ellipsometry (SE) is expected to continue as the preferred measurement for process monitoring of future gate dielectric films. Industry metrology needs not only improved methods to determine film thickness accurately, but also (1) techniques to determine the structure of the individual films and the interfaces between them; (2) understanding of the relationship between physical, electrical, and optical determinations of film properties; and (3) mechanisms, such as reference materials, for traceability of measurements to NIST to support film metrology.

In order for SE to meet process control requirements of film thickness and unambiguously determine film composition and morphology, the optical properties of these advanced dielectric film systems must be characterized and understood.

Technical Strategy

This project focuses on the issues of (1) developing and providing the basis for traceability to NIST for film thickness measurements; (2) identifying structural models and developing preferred optical index dispersion functions or data for improved ellipsometric analysis of future-generation gate dielectric film systems; and (3) correlating optical, electrical, and physical measurements of thickness, composition, and interface structure.

Establish and Transfer Basis of Accuracy for Thin Dielectric Films

Industry requirements for future thin dielectric film optical measurements and calibration standards were identified at a recent NIST-sponsored workshop. Core ellipsometry measurement capability is being expanded and strengthened to meet these requirements. An investigation has been started into cleaning and recontamination issues for film calibration standards to determine whether a workshop-expressed goal of 0.015 nm long-term reproducibility of reference artifact values is obtainable. Procedures are being developed to enable traceability of instrument accuracy to NIST for suppliers of secondary thin-film reference materials without requiring volume production of NIST Standard Reference Materials (SRMs).

DELIVERABLES: By 2003, develop and evaluate prototype procedures that will enable traceability to NIST for 1st level commercial suppliers of reference materials for oxide films down to 2 nm.

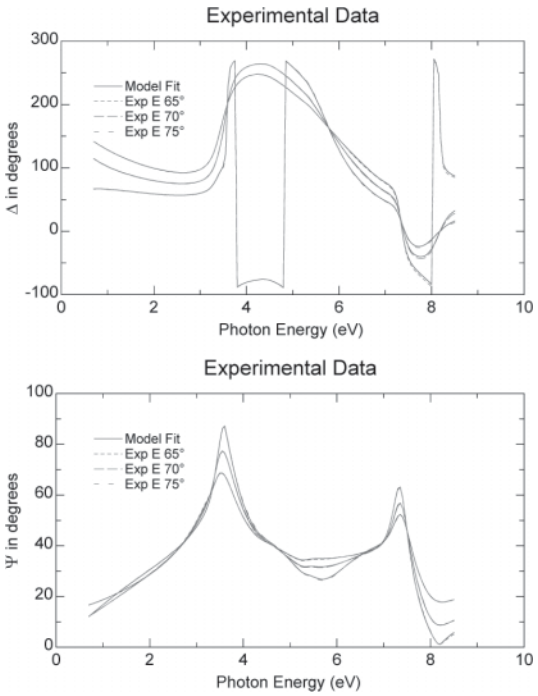
Structural and Optical Models for Ellipsometry

A custom-built, high-accuracy spectroscopic ellipsometer with a spectral range of 1.5 eV to 6 eV is being used for this task, and project staff are working with International SEMATECH, integrated circuit (IC) industry companies, and SRC university staff to obtain and optically characterize advanced oxynitrides, oxide/nitride stacks, and metal oxide and silicate films such as zirconium oxide and hafnium silicate. Characterization will be extended to 8.5 eV to include important optical

Technical Contact:
James R. Ehrstein

Staff-Years (FY 2002):
3.1 professionals
0.5 technician
1.2 guest researchers

index structure of these films beyond their bandgaps. This work is directed at determining preferred structural models, spectroscopic index of refraction values, or preferred optical dispersion functions for each of these film systems, and, where possible, the variability of these parameters due to differences in film fabrication processes. Analysis is done with software developed by NIST for spectroscopic ellipsometry; this software allows maximum flexibility for the addition of the latest published or custom-developed optical response models as appropriate for each material system investigated.



An illustration of the complexity of data resulting from multiple angle spectroscopic ellipsometry measurements for the case of a hafnium silicate film. The challenge is to develop and verify optical models capable of faithfully fitting all data simultaneously to obtain maximal information about the film.

DELIVERABLES: By 2003, determine the optical and structural properties of some technologically relevant high-κ thin films by vacuum ultra-violet spectroscopic ellipsometry and other characterization techniques and establish their relations with growth conditions.

Relation Between Optical, Electrical, and Physical Measurements of Thickness

Through collaborations with International SEMATECH, IC industry companies, and SRC university staff, as well as with key researchers in other parts of NIST, project staff are leading and participating in a number of multimethod comparison studies of various ultra-thin gate dielectric films. These multimethod studies utilize techniques such as X-ray and neutron reflectivity, High-Resolution Transmission Electron Microscopy (HRTEM), Electron Energy Loss Spectrometry (EELS), angle-resolved X-ray Photoelectron Spectroscopy (XPS), Secondary Ion Mass Spectrometry (SIMS), Capacitance-Voltage (C-V) and Current-Voltage (I-V) analysis, as well as spectroscopic ellipsometry and reflectivity. The results of these multimethod studies improve the general understanding of state-of-the-art (SOA) measurement capability for very thin films and also allow project staff to assess the results of various optical models being applied to the analysis of these films with respect to interface layers and structural composition, morphology, and uniformity. SOA C-V and I-V measurement capability for gate films has been established in the project. Advanced 1-D analysis software from commercial and university sources has been established and benchmarked to determine the effect of model and algorithm sophistication on oxide film thickness values calculated from C-V and I-V data. An extension to 2-D modeling is planned.

DELIVERABLES: By 2003, integrate preferred advanced electrical analysis software and structural analyses of high-κ dielectrics to improve agreement between electrical and ellipsometric thickness scales.

DELIVERABLES: By 2004, determine the optical properties of silicon ultra-thin films and evaluate their structural changes such as strains in the films and relate with film thickness and growth conditions.

DELIVERABLES: By 2004, determine the optical properties of amorphous silicon ultra-thin films and their polycrystallizations under high temperature annealing for the quantum dot device preparations.

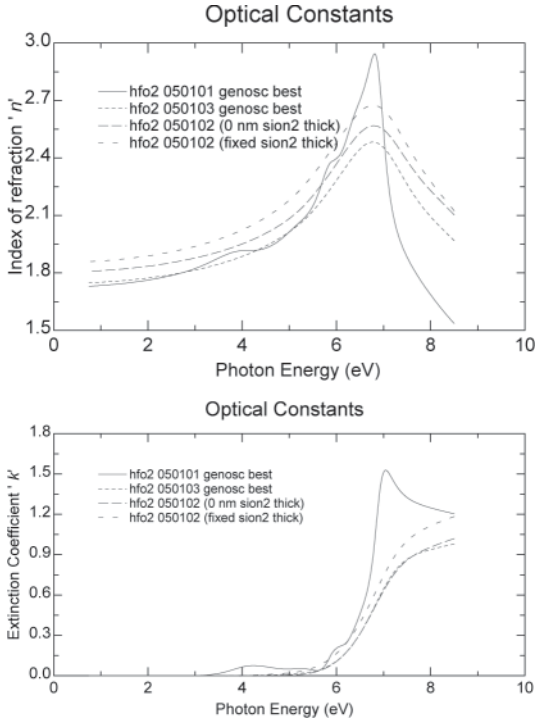
Accomplishments

■ *Extensive testing of upgrades of master single-wavelength ellipsometer that was originally developed for certifying oxide thickness SRMs.* Recent upgrades, many reported last year, are intended to enable attainment of improved short-term and long-term precision necessary to meet industry needs for thin dielectric measurement traceability. Testing has focused on determining the multi-day stability of data taken under continuous acquisition as a measure of core system performance. Measurements of a 10 nm silicon dioxide film over a 3 ½ day period showed slow variation that was equivalent to 0.015 nm of film growth, while measurements of a 2 nm native oxide film over 5 days showed total variation of apparent film thickness of only 0.05 nm. These latter results are well within system performance goals relative to the ITRS traceability needs. Since such tests incorporate possible

changes in actual film thickness, in addition to drift in system component performance, additional tests focused on the effects of temperature and humidity changes on measurement stability. Forced changes of humidity in the near vicinity of the sample were shown to cause meaningful changes in the apparent film thickness, although the changes in relative humidity that were induced are likely only to occur naturally as seasonal changes in the present lab environment. Separately, sudden changes on the order of 1 °C are seen to occur occasionally in the vicinity of the sample and correlate with data changes that imply film thickness changes. However, such temperature changes are not reflected in the ambient relative humidity, and the interaction mechanism is not yet understood.

■ *Primary data acquisition has been completed for comparison of optical, electrical, and physical measurements of thickness on a set of 2 nm silicon dioxide wafers.* The wafer set was originally obtained from NC State University (NCSU) under an International SEMATECH/ NIST/NCSU CRADA. The set included 20 unpatterned SiO_2 wafers that were measured by spectroscopic ellipsometry at NCSU starting with a few hours of completion of growth, and two wafers that were patterned with arrays on capacitors in four different areas. Capacitance-voltage (C-V) measurements were completed for subsets of each size capacitor array in the "sweet spot" (within 25 mm of center) of both of these wafers; additional C-V measurements were taken on arrays of capacitors in an outer region of each wafer which was targeted for HRTEM thickness measurements. Ellipsometry measurements had shown thickness consistency wafer to wafer and uniformity on each wafer all to fall within about 0.16 nm with an overall average just over 2 nm. Capacitance measurements showed thickness variations to be less than 2 % for all spots measured on both wafers and resulted in thicknesses of 2.1 nm using an advanced quantum mechanical (QM) code written by Eric Vogel. This was supported using a QM code from IBM; however, a QM code from NCSU gave thicknesses of 2.3 nm for the same data. HRTEM interpretation of oxide thickness was influenced by interface roughness and was 2.4 nm to 2.6 nm for one of the wafers and 2.2 nm to 2.4 nm for the other wafer. Determination of uncertainty statements for each of these measurements and retesting of optical thickness on a different ellipsometer will be done in order to complete this study for publication.

■ *Spectroscopic ellipsometry of high-κ dielectric films has emphasized the additional information obtainable from vacuum ultraviolet (VUV) ellipsometry.* Following very encouraging preliminary measurements of a number of sets of high-κ films made during FY 2001 at a manufacturer of VUV ellipsometers, NIST purchased its own VUV ellipsometer during FY 2002. The instrument has been used to investigate a large number of sample sets of metal-oxides, aluminates, and silicates that are actively being studied as possible gate dielectric materials of the future. NIST's interest is to develop and verify best models and techniques for extracting the maximum amount of reliable information (including layer structure, component film thicknesses, indices of refraction, and band-gaps). This information and the underlying techniques are very important if ellipsometry is to continue to be used as the primary process monitor should any of these materials become the choice to replace silicon dioxide. The generalized Tauc-Lorentz oscillator model, developed last year at NIST, continues to be quite effective for modeling most of the data sets acquired. Results of analysis show that the material index of refraction depends on both thickness and thermal processing variations above the bandgap, but that there are differences of the



Optical index components, n & k, as determined from VUV ellipsometry for a family of HfO_2 films, illustrating that the optical index can depend strongly on processing variations among samples and is indicative of structure or composition differences among the films.

"Rudolph Technologies Inc. believes there is a significant need for … a sub-40Å oxide … NIST traceable reference material."

Dr. David Leet, Director, Strategic Planning and Advanced Applications, Rudolph Technologies, Inc.

index below the bandgap for various samples of the same nominal composition.

FY Outputs

Collaborations

- AMD Inc., Robert Clark-Phelps, Characterization of High-κ gate dielectric materials (James R. Ehrstein)
- Genus Inc. Dr. Tom Seidel, Characterization of hafnium-oxide and aluminum-oxide nanolaminates (James R. Ehrstein)
- IBM, E. P. Gusev, Extraction of thickness, nitrogen content of SiON films using VUV and infrared ellipsometry (James R. Ehrstein and Curt A. Richter)
- International SEMATECH, Alain Diebold, Gate Oxide Metrology Task FEP Z001 (Eric M. Vogel, James R. Ehrstein, and Nhan V. Nguyen)
- Jet Process Corporation, Takashi Tamagawa, Properties of jet vapor deposition high-κ gate dielectrics (Curt A. Richter and Nhan V. Nguyen)
- Korean Research Institute of Standards and Science (KRISSO), Spectroscopic ellipsometry of SiO_2 films (Yong J. Cho and Nhan V. Nguyen)
- National Physical Lab, (NPL) Teddington, Middlesex, England, Dr. Martin Seah, Ellipsometric thickness of thin SiO_2 films-International Multimethod comparison (Nhan V. Nguyen and Deane Chandler-Horowitz)
- NC State Univ. Prof Greg Parsons, Characterization of yttrium based high-κ gate dielectrics (James R. Ehrstein)
- NIST Division 811, N. Zimmerman, Optical characterization of Si_3N_4 films (Nhan V. Nguyen)
- NIST Division 837, T. Jach, Thickness metrology of SiO_2 films (Nhan V. Nguyen)
- NIST Divisions 836, 837, 838, Roger Van Zee, et al., Spectroscopic ellipsometry of molecular electronics (Nhan V. Nguyen, Curt A. Richter, and John S. Suehle)
- Physikalisch-Technische Bundesanstalt (PTB), Berlin, Germany, Spectroscopic ellipsometry measurements of SiO_2 films (Nhan V. Nguyen)
- Prof. John N. Kidder, Jr., Materials Science and Engineering, University of Maryland, Use of spectroscopic ellipsometry modeling software (SE Studio) and growth of high-κ dielectric thin films (Nhan V. Nguyen)
- Prof. Robert W. Collins, Pennsylvania State University, Instrumentation of rotating compensator ellipsometers and modeling and data analysis (Nhan V. Nguyen)
- Rudolph Technologies, Don Pelcher, Evaluation of experimental procedure for comparative ellipsometric thickness measurements of 3 nm silicon dioxide films (James R. Ehrstein)
- Sharp Microelectronics, Dr. John Conley, Characterization of hafnium-oxide dielectric films (John S. Suehle and Nhan Nguyen)
- Solid State Measurements, Bob Hillard, Combined electrical and optical characterization for extraction of film thicknesses in dielectric stacks (James R. Ehrstein and Curt A. Richter)
- Stanford Univ., Dr. Paul McIntyre, Characterization of HfO_2 and ZrO_2 ALCVD and UV-O_2 dielectric films (James R. Ehrstein)
- Texas Instruments, D. Mercer and L. Columbo, Process metrology for hafnium silicates and oxynitrides (James R. Ehrstein)
- U. Texas at Austin, Prof. Jack Lee, Optical properties of ZrO_2 and HfO_2 for use as high-κ gate dielectrics (Curt A. Richter and Nhan V. Nguyen)
- UCLA, Prof. Jane Chang, Characterization of ZrO_2 dielectric films (R. Mayti, Physics, C. Bouldin, MSEL, and J.H. Scott, CSTL) (Nhan V. Nguyen and James R. Ehrstein)
- Univ. Minnesota, Prof. Steve Campbell, Characterization of HfO_2 dielectric films and silicon nitride interface layers (James R. Ehrstein)
- VLSI Standards Inc., Jerry Prochazka, Traceability to NIST and NVLAP accreditation for SiO_2 film thickness reference materials (James R. Ehrstein)
- Yale University, Prof. T. P. Ma, Optical properties of jet vapor deposition high-κ gate dielectrics (Nhan V. Nguyen and Jin Yong Kim)

External Recognition

■ ASTM Award for "outstanding service and active participation" by the ASTM International Committee F-1 on Electronics at the committee's Jun. 2002, Salt Lake City, meeting (James R. Ehrstein)

Recent Publications

Y.J. Cho, N.V. Nguyen, C.A. Richter, J.R. Ehrstein, B.H. Lee, J.C. Lee, "Spectroscopic Ellipsometry Characterization of High-κ Dielectric HfO_2 Thin Films and the High-Temperature Annealing on Their Optical Properties," Applied Physics Letters, Vol. 80, No. 7, pp. 1249-1251, (18-FEB-2002).

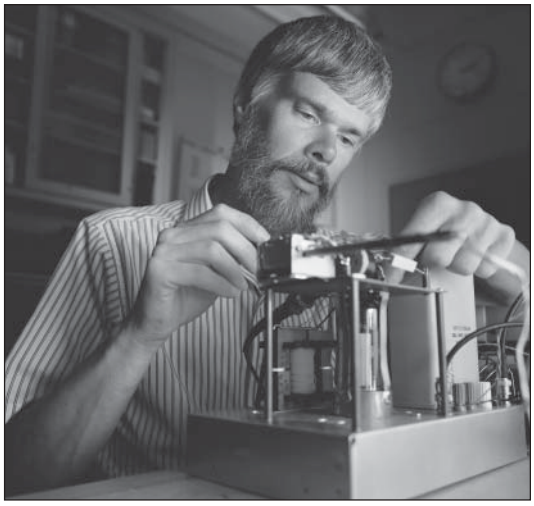
Power Semiconductor Device and Thermal Metrology

Technical Contact:
David L. Blackburn

Staff-Years (FY 2002):
2.5 professionals
6 guest researchers

Goals

The goals of the project are to (1) develop electrical and thermal measurement methods and equipment in support of the development and application of advanced power semiconductor devices and (2) develop advanced thermal measurements for characterizing integrated circuits (ICs), devices, and materials.



David Berning measuring silicon carbide diodes using NIST-developed, specialized equipment, not commercially available. Copyright Robert Rathe

Customer Needs

There are significant technical requirements for more efficient, higher voltage power semiconductor devices. The application needs range from more efficient power supplies for computers and consumer appliances, to electric automobile power converters, to more efficient long distance high voltage power transmission. Rapid technical advances are occurring in the development of new power semiconductor materials and designs to address these needs. With the introduction of these new materials and designs come new requirements for characterizing the performance and reliability of the fabricated devices.

The most exciting, and potentially revolutionary, development in this area is the rapid progress in the development of wide-band-gap semiconductor materials for power semiconductor devices. Wide-band-gap semiconductors offer the potential for higher voltage, higher speed, higher temperature, and overall more efficient power system operation. The two materials of most interest are SiC and GaN. GaN is of interest primarily for very high frequency power devices as well as optical sources, whereas SiC, because the material is further along the development curve, is of interest for high voltage devices used in power conditioning and control systems. The current research effort in the power device effort is focused on SiC. Measurement techniques and systems are being developed to characterize the high voltage switching, safe operation, and thermal characteristics for prototype SiC devices. Also, measurements of the overall performance of devices are being done as part of a DARPA sponsored Wide-Band-Gap Semiconductor program.

While overcoming thermal limitations and barriers has always been at the forefront of power semiconductor technology, this has only come to the fore recently in CMOS-based microelectronic circuits. The major issues include (1) power levels in CPUs are approaching, and in some cases exceeding, those in discrete power devices; (2) power density nonuniformities are leading to hot spots in microprocessors as well as power ICs; (3) new materials are being rapidly introduced that require thorough characterization (for instance, the thermal properties of low-κ interconnect dielectrics); (4) many new and future technologies (e.g., SOI, 3-D integration) tend to thermally isolate power dissipating elements; (5) the ever-shrinking dimensions but increasing frequency of operation of an IC are causing a significant amount of power dissipation in the interconnects; and (6) noncontinuum heat transfer is becoming more important as sizes shrink. In order to address issues like these, reliable methods for measuring the temperature distribution of ICs are required.

Technical Strategy

The strategy is to support the measurement infrastructure of the semiconductor industry by developing and evaluating measurement methods and techniques where suitable ones do not exist for characterizing critical electrical and thermal properties of devices and circuits. This includes methods for extracting device model parameters for system-level simulation. For power devices, the thrusts are on electrical, thermal, and safe operating limits characterization, and for ICs the emphasis is on thermal characterization.

Semiconductor Power Device Metrology

There are four tasks currently underway on power devices. The first three below are for prototype SiC devices, and the fourth is a packaging oriented task applicable to either Si or SiC devices.

Metrology for mapping SiC power bipolar device degradation

Although significant progress has been made in improving the quality of the SiC starting material and the fabricated devices, a major concern for bipolar structures is an observed degradation in the electrical characteristics over time. The degradation is thought to occur from latent defects caused by dislocations that grow and reduce carrier lifetime as the device is operated. The defects should cause current nonuniformities to occur in the device which may be detectable by making very high speed transient thermal images of an operating device.

DELIVERABLES: By 2003, demonstrate high speed thermal image conduction uniformity measurements with SiC power diodes and perform conduction uniformity measurements before and after stress conditions and begin to correlate results with light emission (with NRL).

DELIVERABLES: By 2004, perform degradation measurements on SiC power bipolar transistors as they emerge from the DARPA WBG power device program.

Metrology for nondestructive switching failure

Power devices undergo their greatest electrothermal stress under switching conditions. There are a number of known catastrophic failure mechanisms that occur as a device is switched off with an inductive load. NIST has developed a nondestructive system to test for the failure limits under inductive switching and has done extensive research on Si device failure limits and will extend that work to include SiC power devices.

DELIVERABLES: By 2003, perform unclamped inductive switching measurements for SiC BJTs, MOSFETs, and IGBTs produced by DARPA WBG program.

DELIVERABLES: By 2004, complete analysis of SiC failure mechanisms and compare to those observed in Si devices.

Circuit simulator models for SiC power switching devices.

Parameter extraction is a critical component in developing and using device models in circuit and system simulations. For new devices, not only must new models be developed, but methods must be modified and new ones developed for extracting the parameters for the models.

DELIVERABLES: By 2003, complete development of SiC power MOSFET model and complete development of IMPACT extraction tools for SiC power device model parameter extraction.

DELIVERABLES: By 2003, perform parameter extraction for SiC MOSFETs produced by DARPA WBG program and validate simulations. Publish results.

DELIVERABLES: By 2004, begin to develop SiC power BJT and IGBT model in cooperation with NSF GOLAI program.

Develop thermal metrology for power semiconductor package and cooling system.

The cooling systems for power electronic devices and modules are often quite sophisticated and complex. In evaluating the efficiency and effectiveness of cooling systems, it is critical to be able to measure the temperature of a packaged chip accurately during actual operation. This means that temperature measurement methods are needed that use a chip electrical parameter as the thermometer. Also, validated electro-thermal device models are needed to speed the system design.

DELIVERABLES: By 2003, develop test system and procedures for thermal characterization of Integrated Power Electronic Module (IPEM) and develop electro-thermal model and validation for IPEM.

DELIVERABLES: By 2004, complete development of validation metrology for simulation of thermal management systems for high power inverter and publish results.

Thermal Metrology for Microelectronics Devices and Circuits

There are two tasks associated with thermal measurements for microelectronics. The first is related to measuring the temperature of interconnect structures and measuring the thermal properties of new interconnect dielectrics. The other is the continuing development of a very high speed infrared thermal imaging system.

Advanced interconnect system thermal characterization and metrology

New, low dielectric constant (low-κ) materials are required as circuits operate at higher frequencies to reduce cross-talk and parasitic losses between interconnect lines. These materials also, typically, have a lower thermal conductivity than traditional SiO_2. This, coupled with the increased power dissipation occurring in interconnects, means that characterizing the thermal properties of the new low-κ dielectrics is critical.

"These new silicon carbide devices are powerful additions to our line of surface mount Schottky diodes … We expect their combination of efficiency and high voltage to be particularly valuable in cardioverter defibrillator applications, military aircraft and high voltage telecommunication switching equipment."

Manuel Lynch, Vice President of Business Development, Microsemi Corp.

DELIVERABLES: By 2003, complete modeling of buried interconnect system thermal performance and develop and fabricate test structures for interconnect thermal metrology.

DELIVERABLES: By 2003, demonstrate temperature measurements of buried interconnect lines.

DELIVERABLES: By 2003, begin characterizing thermal properties of candidate low-κ dielectrics.

High-speed thermal image microscopy for on-chip temperature

A limitation of commercially available infrared thermal imaging systems is their inability to make high speed transients measurements. NIST has modified a commercial IR system to be able to make such high speed temperature maps of a device surface with a better than 1 μs time resolution. This task is exploring what physically affects the time and spatial resolution of infrared temperature measurements and developing the requirements for calibrating the high speed measurements.

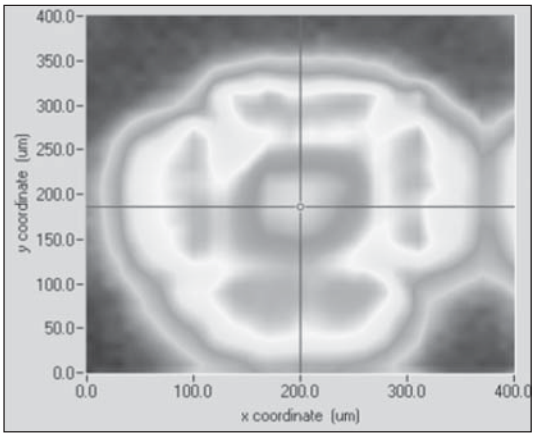
DELIVERABLES: By 2003, develop procedure for coating chips with thin high emissivity paint and characterize the performance for high speed IR thermal metrology; develop transient thermal IR metrology calibration test chip using micro hotplates and demonstrate temporal and spatial calibration procedure.

DELIVERABLES: By 2003, apply transient IR test system to develop gas sensor temperature BIST (with SoC project) and for high-resolution conduction uniformity and avalanche uniformity (with SiC work above).

Accomplishments

■ *Extended capabilities of IMPACT parameter extraction software.* The capabilities of the parameter extraction software, *IMPACT*, were extended to include MOSFETS (in addition to IGBTs) and three polytypes of SiC material (in addition to Si). This was done in collaboration with a University of Puerto Rico, Mayaguez, SURF (Summer Undergraduate Research Fellow) student and an NSF GOALI program student from the University of Arkansas.

■ *High voltage curve tracer and reverse recovery systems.* The development of a 10 kV curve tracer for both 2 and 3 terminal devices was completed. Safety protection and an interlock system have been designed. When the safety system has been installed, the curve tracer will be operational to 10 kV level. Also began development of a new high voltage reverse recovery test system with 5 kV, 20 A capability. These systems are critical components in the SiC power semiconductor device metrology tasks.



Thermal image of a MEMS-based hotplate during a transient event.

■ *Chip temperature measurements for power multichip modules.* A test system to be used in the development of the measurements and models was transferred to the University of Puerto Rico at Mayaguez early in the year for further development there. The NIST/UPRM collaboration was selected by the UPRM Industry Assistantship Program's Industry Advisory Committee as the top project of the year. As a result of this success, the NIST/UPRM project has been expanded, and two additional graduate students from UPRM were added to the program. Software was written for high speed electrical measurement of the temperature of IGBT modules using the threshold voltage. This was done by a UPRM student on a summer internship at NIST. The system is successfully measuring high speed temperature waveforms of the chip surface within a high power IGBT module. Further enhancement, performance characterization, and application of the system will be done in FY03.

■ *High speed transient infrared thermal imaging system.* The high-speed transient imaging capability has been found to be very useful in optimizing a micromachined hot-plate structure used in the development of a gas sensing System on a chip (SoC). Coincidently, the hot-plate is one of the structures being used to develop a calibration methodology for the high speed imager. Measurements made using a calibrated electrical structure on the hotplate show very good agreement with the transient infrared results. As a result of the successful demonstration of the microhotplate as a calibration device, additional measurements are planned to investigate the spatial and temporal resolution limits of the system. Enhancements to software have been completed that enable better control of measurement system parameters and enhance efficiency of measurement. The calibration device was com-

pleted and verified with an accuracy of better than 2 °C. To extend the calibration to higher speed transients, the electrical circuit was improved to measure the hot plate transient temperature electrically. Further electrical measurements made using a high resolution voltmeter demonstrated up to a 1 μs temporal resolution.

FY Outputs

Collaborations

- Avanti Inc., Parameter extraction for IGBT library component models (Allen R. Hefner)
- Avanti Inc./University of Arkansas, SiC power device modeling (Allen R. Hefner)
- Avanti Inc./UPRM, Characterization and modeling of electronic packages for thermal model library component models (Allen R. Hefner)
- CREE, SiC diodes (David W. Berning)
- NIST Division 811 (Nick Paulter), under ATP project to develop low-impedance transmission line characterization (David W. Berning)
- NIST Division 811, Development of low-characteristic impedance time domain reflectometry (Allen R. Hefner)
- NIST Division 811, Metrology for System-on-a-Chip (SoC) design reuse (Allen R. Hefner)
- NIST Division 812, Thin-Film Process Metrology Project/Advanced MOS Device Reliability and Characterization Project, Benchmarks for quantum-mechanical device simulation (Allen R. Hefner)
- NIST/CREE, Development of SiC MPS-diode electro-thermal model (Allen R. Hefner)
- Participants for DARPA contact (including NRL, ARL, Virginia Tech, CREE, University of Arkansas, Rockwell, etc.), Wide bandgap power device program (David W. Berning)
- Rockwell Science Center/NIST, Development of SiC transistor models (Allen R. Hefner)
- University of Maryland, Metrology for multi-technology System-on-a-Chip (SoC) (Allen R. Hefner)
- University of Maryland, Quantum mechanical effects in 2-D semiconductor devices simulators (Allen R. Hefner)
- Virginia Polytechnic Institute and State University, Package interconnect electrical characterization (Allen R. Hefner)
- Virginia Polytechnic Institute and State University, SiC power device utilization (Allen R. Hefner)
- Virginia Tech, SiC diodes (David W. Berning)

Standards Committee Participation

- EIA/International SEMATECH Compact Model Council, member (Allen R. Hefner)

External Recognition

- Elected IEEE Fellow "for contributions to the theory and modeling of power semiconductor devices" (Allen R. Hefner)

Recent Publications

M.Y. Afridi, D.W. Berning, A.R. Hefner, J.S. Suehle, M.E. Zaghloul, E.F. Kelley, Z. Parrilla, C.H. Ellenwood, "Transient Heating Study of Microhotplates by Using a High-Speed Thermal Imaging System," SEMI-THERM Proceedings 2002, IEEE SEMI-THERM SYMPOSIUM, Mar 12-14, 2002, San Jose, California, pp. 92-98, (01-MAR-2002).

M.Y. Afridi, J.S. Suehle, M.E. Zaghloul, D.W. Berning, A.R. Hefner, S. Semancik, R.E. Cavicchi, "A Monolithic Implementation of Interface Circuitry for CMOS Compatible Gas-Sensor System," Proceedings of the ISCAS, IEEE International Symposium on Circuits and Systems, May 26-29, 2002, Scottsdale, Arizona, Vol. 2, pp. 732-735, (01-JUL-2002).

A.R. Hefner, D.W. Berning, T.R. McNutt, A. Mantooth, J. Lai, R. Singh, "Characterization and Modeling of Silicon-Carbide Power Devices," ISDRS, pp. 568-571, (01-DEC-2001).

J.S. Lai, X. Huang, H. Yu, A.R. Hefner, D.W. Berning, R. Singh, "High Current SiC JBS Diode Characterization for Hard- and Soft-switching Applications," Conference record of the IEEE Industry Applications Society Meeting, IEEE Industry Applications Society Meeting, Sep 30, 2001 to Oct 04, 2001, Chicago, Illinois, pp. 384-390, (01-OCT-2001).

T.R. McNutt, A.R. Hefner, A. Mantooth, J.L. Duliere, D.W. Berning, R. Singh, "Parameter Extraction Sequence for Silicon Carbide Schottky, Merged PiN Schottky, and PiN Power Diode Models," Proceedings of the 2002 Power Electronics Specialist Conference, 2002 Power Electronics Specialist Conference, Queensland, Australia, pp. 1269-1276, (01-AUG-2002).

MicroElectroMechanical Systems

Technical Contact:
Michael Gaitan

Staff-Years (FY 2002):
2.5 professionals
6 guest researchers

Goals

The MicroElectroMechanical Systems (MEMS) Project has two research thrusts: (1) develop and provide domestic industry with MEMS test structures, test methods, measurement standards, and standard manufacturing practices; and (2) develop new MEMS-based Micro-Metrology Tools and integrated measurement systems that improve measurements or create new innovation in measurement science.

Geraldine Mijares using a confocal fluorescence imaging microscope to characterize microfluidic systems prepared with microelectrodes. Copyright Robert Rathe

Customer Needs

Measurements and Standards for MEMS

MEMS is a rapidly growing technology with a forecasted annual growth rate that exceeds that of the semiconductor electronics industry as a whole. Manufacturers of MEMS products, such as acceleration sensors for automotive air bags and deformable mirror displays for video projection, are producing these devices in Integrated Circuit (IC) manufacturing lines. This integration of mixed technologies is part of the semiconductor industry's revolution towards "system-on-a-chip." System-on-a-chip links the functionality of the IC (an information processor) with information gathering (sensing the environment) and actuation (acting on decisions). New test structures, test methods, and standards are required for device characterization.

In support for the need of measurement standards for MEMS, the project is working with ASTM Task Group E08.05.03 on "Structural Films for MEMS and Electronic Applications." This task group has undertaken sponsorship of a series of round robin experiments for the testing of residual stress and elastic modulus. MEMS test structures used in these experiments are designed and then fabricated on a test chip that is passed among participating laboratories. The measurement of film stress and elastic modulus is important to the fabrication of MEMS devices. Participation in the ASTM Task Group gives NIST a leadership role in the development of measurement standards for the industry.

MEMS test structures also have applications to measuring the mechanical properties of thin films in ICs, a need identified in the International Technology Roadmap for Semiconductors. As IC devices continue to shrink, thermo-mechanical stress in the thin films that interconnect them is an ever-increasing reliability concern. Current state-of-the-art IC technology uses five or more interconnect layers with aspect ratios (height/width) that can exceed 1.8. Despite the increasing number of interconnect layers in IC technology, existing stress determination and modeling studies have been limited to single level metallization, with few exceptions. This is due, in large part, to the lack of experimental techniques for measuring strain in narrow line width (less than 10 mm) and multilayer structures.

MEMS-based IC test structures allow, for the first time, the measurement of stress in multilayer structures in fully fabricated ICs. These measurements can be used to characterize the mechanical strain in these multilayer films. Results can then be used to verify finite element models of the stress in the films and to correlate mechanical stress data with reliability testing. MEMS-based test structures being developed in this project offer new ways to characterize the mechanical stress in multilayer films.

Micro-Metrology Tools

Miniaturization technologies developed by the semiconductor industry such as thin-film deposition and growth, photolithography, etching, and micro-machining are increasingly being used to make MEMS and NEMS (NanoElectroMechanical Systems) structures that are mechanical in nature. This technology can be thought of as an enabling technology; one that enables you to develop new measurement tools that can measure the physical world more precisely. The MEMS Project works collaboratively with many other projects in NIST to apply microfabrication and nanofabrication tech-

nologies to develop new measurement tools. These tools are used to increase the accuracy of measurements or to develop new measurement methods.

Technical Strategy

Measurements and Standards

The MEMS technical community, composed of companies, universities, and government laboratories, has developed many types of test structures to characterize the fabrication process and device performance. What is lacking is standardized test methods and standard reference materials. The MEMS Project plays an active role in the new ASTM Task Group E08.05.03, metrology for thin-film electromechanical properties of MEMS-based IC technologies.

DELIVERABLES: By 2003, develop a standard test method for measurement of elastic modulus in MEMS devices.

IC Interconnect Characterization

Micro-machining techniques, test structures, and test methods are being developed to characterize the stress, elastic modulus, and adhesion properties in IC interconnects. These test structures are fabricated in the standard IC process on fully fabricated ICs. Fixed-fixed beam and cantilever test structures with interconnect layers are micromachined in the fully processed IC. Measurements of deflection of buckled beams give information on the stress in each interconnect layer. Measurements of mechanical resonance give information on the elastic modulus of the films. These test structures can also be integrated with micro heating elements for accelerated testing.

DELIVERABLES: By 2003, compare measurements of elastic modulus made by mechanical resonance measurements to traditional stress-strain measurements.

Micro-Metrology Tools

In FY 2002, the MEMS Project began a new research program entitled "Single Molecule Manipulation and Measurement" that is funded by the NIST Director's Competence Building Program. This work is in collaboration with the Biotechnology Division, the Analytical Chemistry Division, the Optical Technology Division, the Magnetic Technology Division, the Center for Advanced Research in Biology (CARB), and the Joint Institute for Laboratory Astrophysics (JILA). The goal of this effort is to develop a nanofabricated fluidic-based system that can electronically control the movement of single molecules of DNA and RNA and incorporate "workstations" that support electronic and optical measurements of the structure of these molecules.

DELIVERABLES: By 2003, develop a nanofluidic switch that is capable of changing the solution in the channel at a rate of 10 ms or faster.

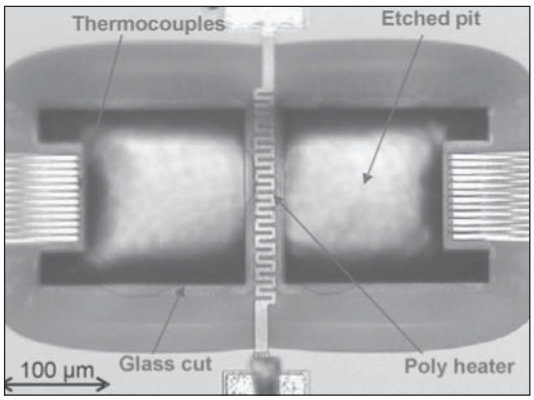
DELIVERABLES: By 2004, develop a nanometer-scale solid state pore that mimics the functionality of the biological-based nanopore structure.

DELIVERABLES: By 2005, develop a platform that integrates nanometer-scale fluidic restrictions, fluidic networks, switches, and workstations that support the electronic and optical control and measurement of single molecules of DNA and RNA.

Accomplishments

- *Cantilever test structures and an analysis to extract the elastic modulus from the measurement of their mechanical resonance were developed.* These test structures are from IC thin films in fully fabricated Complementary Metal-Oxide Semiconductor (CMOS) ICs. A test chip containing the new cantilever test structure designs was fabricated on a commercial CMOS foundry through the MOSIS service. The test structures are silicon micro-machined as a post process in order to release them mechanically. These test structures complement the doubly clamped beam test structures that have been developed and used to measure the strain in CMOS films. The combination of data from strain measurements and elastic modulus measurements will enable the measurement of thin-film stress.

- *Three ASTM test methods have been completed and are now in consideration for adoption by the ASTM.* The test methods are based on the NIST Internal Report published in the previous year. A test chip has also been designed and fabricated for the round robin experiment to determine the precision and bias of the test methods. The round robin experiment is planned to be completed in the next year. The test chips contain designs for fixed-fixed beam test structures, cantilever test structures, bow-tie test structures, T test structures, and Guckle rings. In addition to this, an online version of the users' guide for the experiment has been prepared that includes data entry and calculation programs for the measurements.



Optical micrograph of a micromachined CMOS convective accelerometer. This device works on a principle that is completely different from the traditional "proof mass" MEMS accelerometers; it works on the principal that hot air rises. This invention was awarded a U.S. patent, number 6,171,880.

■ *NIST was awarded a patent on the invention of a new type of accelerometer*. The convective accelerometer, as it is named in the patent, operates on the principle that hot air rises. This device differs from the traditional MEMS-based accelerometers in that its operation is not based on a solid proof mass. The device consists of microheating elements and thermocouple sensors separated by a gap and placed in differential configurations. Thermocouple sensors measure the temperature difference between the two sides of the microheater caused by the effect of acceleration on free convection in the surrounding gas. The devices show a small error in linearity of <0.5 % under tilt conditions from -90 ° to 90 °, and <1.6 % under acceleration from 0 g to 8 g. The sensitivity of the devices is a linear function of heater power (temperature). A sensitivity of 20 µV/g to 30 µV/g was measured for operating power between 35 mW and 45 mW. This invention is a spin-off of research on Micromachined Passive Microwave Components in CMOS Technology that was sponsored by the U.S. Navy.

FY Outputs

Collaborations

■ ASTM Task Group E08.05.03, Structural films for MEMS and electronic applications (Janet C. Marshall)

■ NIST Division 836, Microhotplate-based sensor arrays (John S. Suehle and Michael Gaitan)

■ NIST Division 839, Bill MacCrehan, Micro-electro-chemical cells (Geraldine Mijares)

■ University of Maryland/Georgia Tech, Measuring and modeling bonding temperature rise (George G. Harman, Michael Gaitan)

Standards Committee Participation

■ ASTM Task Group E08.05.03, assumed the role of Task Group Chair for the ASTM E08.05.03 Task Group Meeting on 11/6/01 and performed the duties of the Task Group Chair for the meetings on 5/7/02 (Janet C. Marshall)

External Recognition

■ Received Department of Commerce Silver Medal Award, October 2002 (Michael Gaitan)

Recent Publications

M.D. Gaitan, "Overview on CMOS MEMS Fabrication Techniques and Applications," Proceedings of 2001 IMAPS, 2001 IMAPS, Oct 09-11, 2001, Baltimore, Maryland, pp. 1-6, (01-NOV-2001).

S. Shuman, M.D. Gaitan, Y.K. Joshi, G.G. Harman, "Wire Bond Temperature Sensor," Proceedings of 2001 IMAPS, 2001 IMAPS, Oct 09-11, 2001, Baltimore, Maryland, pp. 344-349, (01-NOV-2001).

Electrical Test Structure Metrology

Goals

Develop test-structure-based electrical metrology methods and related reference materials with emphasis on linewidth and overlay metrology-tool calibration; contribute to standards organizations supporting the development of metrology standards for the semiconductor tool industry; target the specific near-term goal of fabricating a quantity of reference-features with nominal critical dimensions (CDs) in the range 70 nm to 100 nm having CD uniformities of 1 nanometer per micrometer by Jun. 2003.

Christine Murabito using a hot plate to do a post-exposure bake during the photo-lithography process.

Customer Needs

The Semiconductor Industry Association's (SIA's) International Technology Roadmap for Semiconductors (ITRS) states that it is critically important to have suitable reference materials for lithography support available when on-wafer measurements are made as a new technology generation in integrated circuit (IC) manufacturing is introduced, and particularly during development of advanced materials and process tools. Each generation of ICs is characterized by the transistor gate length whose control to specifications during IC fabrication is a primary determinant of manufacturing success. The SIA projects the decrease of gate linewidths used in state-of-the-art IC manufacturing from present levels of up to 250 nm to below 70 nm within several years. Scanning electron microscopes (SEMs) and other systems used for traditional linewidth metrology exhibit measurement uncertainties exceeding ITRS-specified tolerances for these applications. It is widely believed that these uncertainties can be at least partially managed through the use of reference materials with linewidths traceable to nanometer-level uncertainties. Until now, such reference materials have been unavailable because the technology needed for their fabrication and certification has not been available.

It is also widely believed that the usefulness of SEM metrology for monitoring wafers in advanced development and production may become inadequate at some future IC generation. Thus, there exists a need for new methodology to meet future metrology requirements.

Technical Strategy

The technology that the project staff have developed for fabricating linewidth and overlay reference materials is known as the Single-Crystal CD Reference-Material implementation. Patterning with lattice-plane selective etches of the kind used in silicon micro-machining provides reference features with quasi-atomically planar sidewalls over local length segments of the reference feature, typically extending to several micrometers. This unique attribute is highly desirable for the intended applications, particularly if the quasi-atomically planar sidewall smoothness can be further extended to reference-feature segment lengths of up to 10 micrometers. Essential elements of the technology implementation include starting silicon wafers having a (110) orientation; alignment of the reference features to specific lattice vectors; and lithographic patterning with lattice-plane selective etches of the kind used in silicon micro-machining.

The traceability path for dimensional certification is provided by High-Resolution Transmission Electron Microscopy (HRTEM) imaging. This method provides nanometer-level accuracy, but is sample-destructive and thus is impractical on a 100 % basis. The project's traceability strategy has thus featured the sub-nanometer repeatability of electrical CD metrology as a secondary reference means. Low-cost, whole-wafer electrical measurements are effectively calibrated with a limited number of HRTEM lattice-plane image counts made on a selection of reference features that are replicated on other chips on the same wafer. Typical reference features are several-hundred lattice planes wide. A technique of making lattice-plane image counts, by automated analysis of HRTEM phase-contrast images, was developed in order to minimize the uncertainties of the linewidths of the standards due to lattice-plane counting.

Technical Contact:
Michael W. Cresswell

Staff-Years (FY 2002):
3 professionals
1 technician
1 guest researcher

"The three way partnership between International SEMATECH, VLSI Standards, and NIST is driving towards creating a CD standard which is critically needed as the industry goes below 65 nm."

Hal Bogardus, International SEMATECH

An important metric of the progress and success of the project is the level of uncertainty attributed to the product CD reference features. The units that were delivered to International SEMATECH (ISMT) last year, per contractual arrangements, typically exhibited 14 nm uncertainty. This level is considered by the industry to be four to five times higher than what is desired for the road-map out years. Therefore, the main target of the project during the current year is reducing uncertainty to 4 nm or better.

Our recent results have indicated that a significant portion of the uncertainty in the certified linewidth of the finished product is attributable to variations, which are typically up to tens of nanometers, in the physical linewidth of the features over segment lengths of typically ten micrometers. Since electrical CD metrology effectively extracts the average width of a reference feature, it is insensitive to these physical CD variations. Consequently, it can contribute commensurate uncertainties of local linewidths of the finished product. The current year's effort has therefore focused on reducing the macroscopic variations of the physical CDs of the reference features by refinements to the starting-material specifications and to the wafer-fabrication process.

The technical strategy has to be responsive to industry's requirement for reference materials to have the physical properties of standard 200 mm wafers. Since 200 mm (110) starting material is virtually unobtainable at an acceptable cost, this project's technical strategy has been to dice each 150 mm (110) wafer after lithography and to mount the separate chips in micro-machined standard 200 mm wafers to accommodate the test chips. The result is that finished units are rendered metrology-tool-compatible at an acceptable cost. The entire fabrication and certification process is planned to be transferred to a commercial standards vendor.

However, some leading semiconductor manufacturers are now requesting single full-wafer implementations at the 200 mm and 300 mm diameter levels. Accordingly, the current year's effort has also addressed this issue.

In the current year, project researchers have set up a chip-level reference-material patterning facility at the ISMT facility in Austin. One leading motivation for this effort was the ready availability of SEM imaging facilities having a capability to inspect the high volume of reference-material chips being generated by processing variations. The latter are directed at reducing single-feature CD variation to below the several-nanometer level. In addition, qualified operating staff were also made generously available. ISMT has been contributing 20 to 40 hours of SEM machine time per week, with operators. In addition, the project has access to a state-of-the-art dual-beam focused ion beam (FIB) inspection tool and operator staff for necessary cross section measurements on an as-needed basis.

Richard Allen and Michael Cresswell discuss SEM measurements of prototype reference materials with Laurie, an International SEMATECH staff member, in Austin, Texas.

A second motivation for setting up the reference-material patterning facility at the ISMT facility in Austin was essential proximity to the Advanced Technology Development Facility (ATDF), which is being operated by a NIST assignee from the Manufacturing Engineering Laboratory in ISMT's clean room. Our current year's CD-variation control effort has depended exclusively on this one-of-a-kind world-class installation and the unique skills of the NIST assignee. As stated previously, the atomic force microscope (AFM) facility is intended also to serve as an alternative transfer-calibration tool.

The lithography for the wafers that have been used during the current year to facilitate our uncertainty-reduction experiments was conducted at the Microelectronics Development Sandia Laboratory at Sandia National Laboratories and at the Scottish Micro-Electronics Centre of the University of Edinburgh. These activities were funded by ISMT, but the technical direction was provided by project staff at NIST.

The member companies of the project's major client, ISMT, insist that transfer of the Single-Crystal CD Reference-Material (SCCDRM) technology to a commercial standards manufacturing and marketing company organization be an integral part of the project. Therefore, ISMT and NIST have agreed

that VLSI Standards, Inc., of San Jose, California, be invited to contribute to the new phase of the project that is described below. One immediate outcome has been that we have honored a request to incorporate scatterometry targets in the next design iteration.

DELIVERABLES: By 2003, design improved Single-Crystal Silicon-on-Insulator and bulk CD reference materials, procure photomasks and starting materials, and deliver to ISMT and its contractor for CD reference-material fabrication. Include scatterometry target grids in the layout.

DELIVERABLES: By 2003, develop patterning processes capable of replicating reference features in bulk and Silicon-on-Insulator (SOI) with line-edge roughness below 5 nanometers extending up to 10 micrometer feature lengths. Patterning processes are to include procedures for removing particles and precipitates having low-single nanometer dimensions that are typically produced by the patterning-process chemistry. In addition, develop decontamination procedures for removing organic side-wall residues that are not detectable by electron-beam imaging but adversely affect AFM transfer metrology.

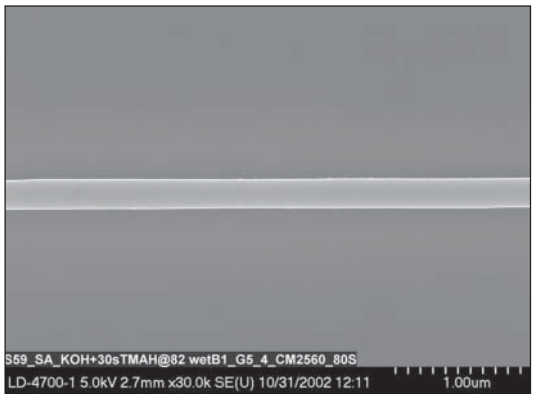
DELIVERABLES: By 2003, evaluate new vertical etch-stop implementations to enhance reference-feature straightness, edge roughness, and side-wall quality. In particular, design, fabricate, and evaluate buried boron profiles. Also, replicate reference features in high-resistivity epitaxial silicon device layers grown on highly-doped boron substrates. Include evaluation of stencil-mask based sub-tenth micro-meter lithography techniques being sponsored by ISMT and respond to requests by member companies to develop a single full 200 mm wafer implementation.

DELIVERABLES: By 2004, fabricate and calibrate scatterometry targets using the single-crystal reference-material implementation. Invite industry partners to evaluate performance benefits produced by alternative starting-material etch stops. Fabricate a selection of reference materials having features replicated in metal and polysilicon with built-in rulers provided by HRTEM illumination.

Accomplishments

■ *A selection of SIMOX (Separation by Implantation of Oxygen) and bulk (110) 150 mm wafers was procured, pre-processed, and delivered to Sandia National Laboratories for lithography on behalf of client ISMT. NIST project staff also designed a new reference-feature layout and procured the 5X mask that was used for this Sandia operation.* The lot-split processing was specified by this project and featured pre-patterning by reactive-ion etching for reference-feature dimensional uniformity and plasma etching of the SIMOX-wafer buried oxides to investigate control of substrate contamination during SEM inspection. The Sandia work was funded by ISMT. The finished wafers were delivered to NIST for dicing prior to being taken to ISMT for completion of processing at the chip level.

■ *A collection of 75 mm (110) wafers was procured, re-flatted at NIST to meet orientation requirements, and, after implant pre-processing, delivered to the Scottish Microelectronics Centre (SMC) at the University of Edinburgh for silicon-nitride hard-mask deposition and patterning by g-line stepper to our specifications.* The lot-split processing was specified by this project and featured SOI as well as p^+np and n^+p buried junctions to isolate the patterned layers electrically. This work was also funded by ISMT. A subset of wafers was patterned collaboratively at the SMC by NIST, SMC, and ISMT staff before being returned to NIST for dicing and then to ISMT for pattern-transfer from the hard mask.



This image of a S59-SA-G5-4 feature, patterned by hybrid KOH/TMAH etching, was taken prior to cleaning. It is estimated to be uniform to within less than 3 nm over 4 micrometers.

■ *A facility for patterning individual reference-feature chips was set up and operated at ISMT. Processes, including cleaning protocols, for silicon pattern-transfer and nitride hard-mask removal at the chip level were established and documented.* Chemical variables that were optimized for pattern-transfer include TMAH-etch immersion time and temperature for the various available substrate boron-doping levels. The variables that were optimized for nitride hard-mask stripping include immersion-time and phosphoric-acid temperature and concentration. Comparisons between straight TMAH and hybrid TMAH/KOH etching processes were also investigated and reported.

■ *Protocols for SEM imaging and evaluation of large quantities of reference features by ISMT operators were established and implemented.* The problem addressed was screening and inspecting thousands of top-down reference-feature images

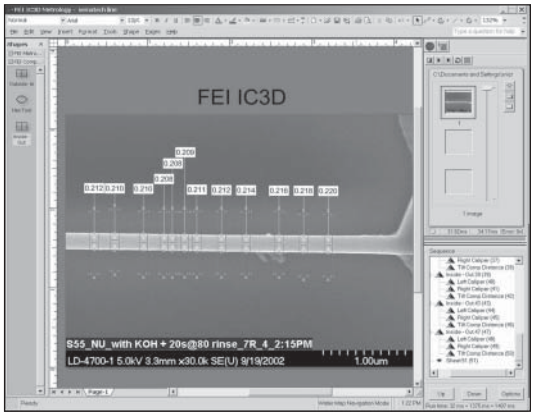
"I would like to thank you and NIST for your pioneering work on silicon pocket wafer technology. We have now incorporated this technology in one of our products. We also regard very highly your work on the single crystal linewidth standard. We see this as the first and only attempt by anyone in the world to produce a linewidth standard traceable to the fundamental units of measure, in the sub-100 nm range, for use in the semiconductor industry.

This work is of technical and economic importance to the semiconductor industry, because the ability to correctly size ever smaller lateral dimensions on silicon substrates is key to the manufacturing yield of silicon chips.

We look forward to a continuing technical relationship between VLSI Standards and NIST."

Marco Tortonese, Ph.D., Engineering Manager, VLSI Standards, Inc.

for fabrication-process development purposes and for selecting reference features for AFM and HRTEM imaging, both of which are very costly and time-consuming operations. In order to maintain the inspection budget below $20K per month, a hybrid optical/SEM inspection process was implemented and interfaced with a database that has been designed by project staff. In addition, image-analysis software was purchased and modified to allow off-line, large-sample, CD extraction from high-density SEM images of single features. This result was facilitated through collaboration with Hitachi Instruments, FEI, Inc., Image-Pro Company, Leeds Instrument Company, and SEM image-analysis specialists at NIST/MEL and ISMT.



This image, as analyzed by FEI Inc., indicates a 4 nm CD range over 2 μm of feature length.

■ *Chip-patterning processes to reduce line-edge roughness developed and demonstrated.* The accomplishments listed above were applied to the identification of a hybrid TMAH/KOH etching process that reduces average line-edge roughness from last year's 17 nm to typically 6 nm on SOI material. This is a very important result because it is a prerequisite for the reduction in final-product uncertainty to levels consistent with requirements of the 70 nm node. Key contributions to achieving this result were made by the staff of the Failure-Analysis Laboratory and numerous other professional staffers at ISMT in Austin.

■ *The project's selected technology-transfer partner, VLSI Standards, Inc., of San Jose, California, has formally agreed to support the project by making its 150 mm wafer clean room, which is equipped with an i-line stepper, available for performing the lithography for the project's next generation of SCCDRMs.* The collaborative agreement, which was recently concluded, provides for project staff at NIST to design the reference features which will include a novel set of scatterometry targets. The NIST project team has also written the starting-material specifications, scheduled the pre-processing ion implants, and taken responsibility for the technical management of the next phase of the three-way collaborative project phase. ISMT will provide the chip-level processing facilities and the AFM transfer-calibration measurements, and will fund the HRTEM microscopy.

FY Outputs

Collaborations

■ International SEMATECH member companies (AMD, Compaq, Conexant, Hewlett Packard, IBM, Intel, Lucent Technologies, Motorola, Texas Instruments, Hyundai, Infineon Technologies, Philips, STMicroelectronics, TSMC), Development of single-crystal critical dimension reference materials (Michael W. Cresswell and Richard A. Allen)

■ International SEMATECH, Development of single-crystal critical dimension reference materials (Michael W. Cresswell and Richard A. Allen)

■ NIST Division 821, Bill Penzes, Development of electrically calibratable stage micrometer (Richard A. Allen)

■ Photronics, Development of optical/electrical hybrid critical dimension measurement for photomasks (Richard A. Allen and Michael W. Cresswell)

■ Sandia National Laboratories Microelectronics Development Laboratory, Sandia National Laboratories Compound Semiconductor Research Laboratory, Sandia National Laboratories Integrated Materials Research Laboratory, NIST ITL, MSEL, MEL, and International SEMATECH on Fabrication and certification of reference materials for linewidth and overlay metrology (Michael W. Cresswell, Loren W. Linholm, and Richard A. Allen)

■ Sandia National Labs, NIST Divisions 898, 855, and 821, University of Central Florida, and International SEMATECH, Reference artifacts for critical dimension measurements (Michael W. Cresswell, Loren W. Linholm, and Richard A. Allen)

■ University of Edinburgh, U.K., and International SEMATECH, Process development for single-crystal critical dimension reference materials (Michael W. Cresswell, Loren W. Linholm, and Richard A. Allen)

- VLSI Standards, Development of single-crystal critical dimension and overlay reference materials (Michael W. Cresswell and Richard A. Allen)

- VLSI Standards, Inc., and ISMT, Development of commercial architecture and distribution plan for single-crystal CD reference materials (Michael W. Cresswell and Richard A. Allen)

- VTT Finland and George Washington University, Develop non-contact test structures and methods (Richard A. Allen, Michael W. Cresswell, and Loren W. Linholm)

- VTT Finland, Design and fabrication of capacitance sensors based on co-fired ceramic technology (Michael W. Cresswell)

Standards Committee Participation

- Electrical Test Structures Task Force, Co-Chair (Richard A. Allen)

- SEMI International Standards Microlithography Committee, member (Richard A. Allen)

External Recognition

- Senior Member, IEEE, elected Jun. 2002 (Richard A. Allen)

Recent Publications

M.W. Cresswell, J.E. Bonevich, R.A. Allen, N.M. Guillaume, L.A. Giannuzzi, S.C. Everist, C.E. Murabito, P.J. Shea, L.W. Linholm, "Electrical Linewidth Test Structures Patterned in (100) Silicon-on-Insulator for Use as CD Standards," IEEE Transactions on Semiconductor Manufacturing, Vol. 14, No. 4, pp. 356-364, (01-NOV-2001).

R.A. Allen, M.W. Cresswell, C.E. Murabito, W.F. Guthrie, L.W. Linholm, C.H. Ellenwood, E.H. Bogardus, "Test Structures for Referencing Electronics Linewidth Measurements to Silicon Lattice Parameters Using HRTEM," Proceedings of the 2002 ICMTS, IEEE 2002 International Conference on Microelectronic Test Structures, Apr 09-11, 2002, Cork, Ireland, pp. 13-18, (08-APR-2002).

B.A. am Ende, M.W. Cresswell, R.A. Allen, T.J. Headley, W.F. Guthrie, L.W. Linholm, E.H. Bogardus, C.E. Murabito, "Measurement of the Linewidth of Electrical Test-Structure Reference Features By Automated Phase-Contrast Image Analysis," Proceedings of the 2002 ICMTS, IEEE 2002 International Conference on Microelectronic Test Structures, Cork, Ireland, Vol. 15, pp. 1-5, (01-APR-2002).

M.W. Cresswell, E.H. Bogardus, J.V. Martinez de Pinillos, M.H. Bennett, R.A. Allen, W.F. Guthrie, C.E. Murabito, B.A. am Ende, L.W. Linholm, "CD Reference Materials for Sub-Tenth Micrometer Applications," Proceedings of the SPIE, SPIE's 27th Annual International Symposium and Education Program on Microlithography, Mar 03-08, 2002, Santa Clara, California, Vol. 4689, pp. 116-127, (01-JUN-2002).

N.M. Guillaume, M. Lahti, M.W. Cresswell, R.A. Allen, L.W. Linholm, M.E. Zaghloul, "Non-contact Electrical Critical Dimensions Metrology Sensor for Chrome Photomasks," SPIE, 21st Annual BACUS Symposium on Photomask Technology, Oct 02-05, 2001, Monterey, California, Vol. 4562, (30-NOV-2001).

R. Schlaf, Y. Emirov, J.A. Bieber, A. Sikder, J. Kohlscheen, D.A. Walters, M.R. Islam, B. Metha, Z.F. Ren, T.L. Shofner, B.B. Rossi, M.W. Cresswell, "Using Carbon Nanotube Cantilevers in Scanning Probe Metrology," Proceedings of the SPIE, SPIE's 27th Annual International Symposium and Education Program on Microlithography, Mar 03-08, 2002, Santa Clara, California, p. 53, (01-JUN-2002).

Major Facilities / Laboratories

Microfabrication Process Facility

See next page for facility description

Contacts: Russell Hajdaj, 301-975-2699
Eric S. Johnson, 301-975-2096

Materials Characterization Labs

High-Resolution Optical:

Spectroscopic Ellipsometry, High-Resolution Fourier Transform Infrared Spectroscopy, Photoluminescence, Raman Scattering, Photoreflectance, and other Modulation Spectroscopies

Electrical:

Resistivity, Spreading Resistance, Lifetime, Hall Effect, Deep-Level Transient Spectroscopy, Deep-Level Optical Spectroscopy, Charge-Pumping Measurements, Capacitance-Voltage (high frequency & quasi-static), Surface Photovoltage, AC Impedance Analysis, Scanning Capacitance/Atomic Force Microscopy

X-Ray:

Double-Crystal Rocking Curve, Laue Orientation Facility

Device and Test Structure Characterization Labs

Electrical and Thermal Package Evaluation
Power Device Model Extraction and Validation
Packaging, Assembly, and Bonding Evaluation
Package Interconnect
Scanning-Electron Microscope
Scanning-Probe Microscope
Automatic Wafer-Level Measurement
Gate Dielectric Integrity
MEMS Electrical, Mechanical, Optical, and Microwave

Computer-Aided Design Labs

Test Structure Layout and Design
Integrated Circuit Layout, Design, and Simulation
Finite Element Thermal Analysis Tools and Computational Fluid Simulations
System, Device, Process, Interconnect, and Virtual Fabrications Simulations

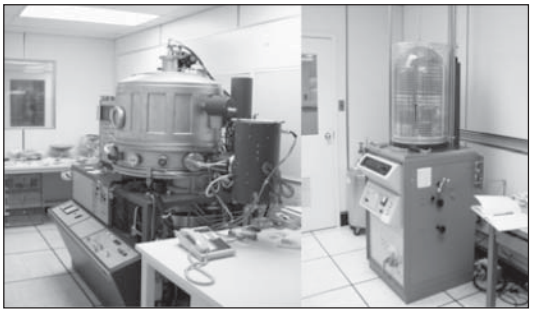
Microfabrication Process Facility

Description

As integrated circuit (IC) sizes increase to more than 1 cm^2 and feature sizes within the circuits decrease to less than 1 μm, critical demands are placed on the measurement capability required to control and monitor IC fabrication successfully. To meet the demand, NIST researchers are developing state-of-the-art measurement procedures for microelectronics manufacturing.

The Microfabrication Process Facility provides a quality physical environment for a variety of research projects in semiconductor microelectronics as well as in other areas of physics, chemistry, and materials research. The laboratory facilities are used for projects addressing many areas of semiconductor materials and processes, including process control and metrology, materials characterization, and the use of IC materials and processes for novel applications.

The laboratory complex, approximately half of which is composed of Class 1000 cleanroom space, occupies about 2900 square meters. Within the cleanroom, work areas are maintained at Class 100 or better. The facility is designed so the work areas can be modified easily to accommodate the frequent equipment and other changes required by research.



Metallization: sputter and evaporation.

Objective

Current objectives are to develop and fabricate structures and devices to fulfill the needs of metrology projects within SED and NIST. These structures include MEMS-based devices, microelectronic devices, and other specialized devices.

Capabilities

The facility has a complete capability for IC fabrication. Principal processing and analytical equipment is listed below.

Diffusion, Oxidation, and Annealing

Six furnace tubes for up to 75 mm diameter wafers and five tubes for up to 100 mm diameter wafers.

Mask Alignment

The Karl Suss Mask Aligner model MA/BA6, a new tool for the facility, is capable of sub-micron resolution (< 0.75 μm) and also has the ability to expose the backside of a substrate, which can be aligned to the front side features. The tool also is designed to be upgraded to a wafer-to-wafer bond aligner.

Plasma Etching and Deposition

The NIST Microfabrication Process Facility has recently procured a plasma etching and deposition system, the Unaxis 790. The system is capable of etching Si, SiO_2, Silicon Nitride, and polyamides. Low temperature (< 300 °C) film depositions of SiO_2 and silicon nitride can also be accomplished using Plasma Enhanced Chemical Vapor Deposition.

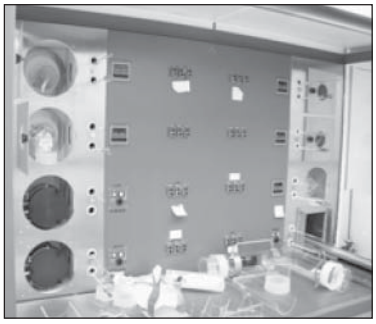
Unaxis 790 plasma etching and deposition system. [Property of Unaxis Semiconductors, reprinted with permission]

Photolithography

Research mask aligner (proximity and contact) for wafers up to 100 mm in diameter and irregularly shaped samples and 10 × direct-step-on wafer system for 75 mm diameter wafers. Photoresist spin coating and developing and related chemical processing, including oxygen plasma stripping. E-beam writing and scanning electron microscope examination for nano-features on 75 mm diameter wafers.

Film Deposition

Low-pressure chemical vapor deposition systems for depositing silicon nitride, polysilicon, and low-temperature silicon dioxide. Radio frequency and dc vacuum sputtering of metals and dielectrics.



Film deposition and diffusion furnaces.

Etching

Wet and dry etching processes. Plasma barrel etching of nitride films and wet chemical etching of silicon for micromachining. Xenon Difluoride silicon etch process.

Wet chemical processing.

Analytical Measurements

Thin-film reflectometry and other thickness measurements, optical microscopy, and grooving and staining. Detak 6M Profilometer providing step height measurements and thin film stress analysis software.

Post Processing Equipment

DISCO HI-Tech America Inc. 8" wafer dicing saw and SEM cross section sample prep equipment.

Applications

Small quantities of specialized semiconductor test specimens, experimental samples, prototype devices, and processed materials can be produced. The processes and processing equipment can be monitored during operation to study the process chemistry and physics. The effects of variations in operating conditions and process gases and chemical purities can be investigated. Research is performed under well-controlled conditions.

A research-oriented facility, the laboratory is not designed to produce large-scale ICs or similar complex structures. Rather, the laboratory emphasizes breadth and flexibility to support a wide variety of projects.

Automatic 8" wafer dicing saw.

Currently, research projects address many aspects of microelectronic processing steps and materials as well as silicon micro-machining. Examples include: metal-oxide-semiconductor measurements; metal-semiconductor-specific contact resistivity; uniformity of resistivity, ion-implanted dopant density, surface potential, and interface state density; characterization of deposited insulating films on silicon carbide; ionization and activation of ion-implanted species in semiconductors as a function of annealing temperature; electrical techniques for dopant profiling and leakage current measurements; and processing effects on silicon-on-insulator materials. A simple Complementary Metal-Oxide Semiconductor (CMOS) process has been established. Recent work has also begun in the field of molecular electronics.

Availability

Facility staff welcome collaborative research projects consistent with the research goals of the NIST semiconductor program. Work is performed in cooperation with the technical staff of the laboratory.

The most productive arrangements begin with the development of a research plan with specific goals. The commitment of knowledgeable researchers to work closely with NIST staff and the provision of

equipment and other needed resources are required. Because hazardous materials are present, laboratory staff must supervise all research activities.

Tasks

- Design and develop optical thermometer (bi-material cantilever w/optical coupling for measurement).
- Fabricate Multi-Junction Thermal Converter (MJTC) in collaboration with Electricity Division.
- Fabricate structures for thermal conduction of silicon dioxide round robin.
- Investigate over-etching phenomena that occurs in Si at the (111) - (001) plane junction with anisotropic etchants.
- Publish MJTC fabrication procedure and process data as a NIST Special Publication.
- Develop and organize equipment and processes for molecular electronics.

Recent Process Equipment Additions

- SEM with E-Beam Writing Capability
- 8" Wafer Dicing Saw
- Karl Suss Mask Aligner MA6/BA6
- Plasma Etching, RIE, and Plasma-Enhanced Chemical Vapor Deposition utilizing two Unaxis 790s.

National Research Council (NRC) Post-Doctoral Opportunities

The Semiconductor Electronics Division at the National Institute of Standards and Technology (NIST), in cooperation with the National Research Center (NRC), offers awards for post-doctoral research for American citizens in the fields described below. The Division conducts research in semiconductor materials, processing, devices, and integrated circuits to provide, through both experimental and theoretical work, the necessary basis for understanding measurement-related requirements in semiconductor technology.

NIST affords great freedom and an opportunity for both interdisciplinary research and research in well-defined disciplines. These technical activities of NIST are conducted in its laboratories, which are based in Gaithersburg, a large complex in a Maryland suburb of metropolitan Washington, DC. Applications for NIST Research Associateships are evaluated by the panels only during February. To be eligible for review in February, completed application materials must be postmarked no later than Feb. 1, 2003. This time will also be approximately the same in 2004.

Molecular Electronics: Electrical Metrology

In Molecular Electronics — a field that many predict will have important technological impacts on the computational and communication systems of the future - molecules perform the functions of electronic components. We are developing methods to reliably and reproducibly measure the electrical properties of small ensembles of molecules in order to investigate molecular conduction mechanisms. Specifically, we are developing test-structures based on nanofabrication and MicroElectroMechanical Systems processing techniques for assessing the electrical properties and reliability of moletronic molecules. In addition to the complexity of the nanofabrication of test structures, the challenges associated with measuring the electrical properties (such as current-voltage and capacitance-voltage as functions of temperature and applied fields) of these small molecular ensembles are daunting. The measured electrical properties will be correlated to systematic characterization studies by a variety of probes and the results used in the validation of predictive models. This task is part of a cross-disciplinary, interlaboratory effort at NIST, with an overall role of developing the measurement science that will enable molecular electronics to blossom into a viable industry.

Contact: Curt A. Richter, 301-975-2082, or John S. Suehle, 301-975-2247

Scanning Probe Metrology

We are developing scanning probe microscopes to characterize and manipulate the physical and electrical properties of electronic devices, semiconductors, and related materials at the nanometer resolution scale. Projects should be aimed at impacting silicon technology 5-10 years in the future or at characterization problems unique to compound semiconductors, molecular electronic devices, or quantum devices. We recently developed scanning capacitance microscopy as a tool for measuring the two-dimensional dopant profile across a silicon p-n junction. We are particularly interested in projects to develop techniques to measure material properties in three dimensions and that have spatial resolution below 1 nm. Our interests extend to other scanning probe techniques, including variable scanning tunneling microscopy in UHV, surface photovoltage microscopy, and other optically pumped scanning probes.

Contact: Joseph J. Kopanski, 301-975-2089, or David G. Seiler, 301-975-2054

Electrical Overlay- and CD-Metrology Development for Characterization of Advanced Lithography Instruments

Projected CD and overlay control-tolerances for new generations of ICs are reducing metrology uncertainty down to the several-nanometer region. However, the development of CD and overlay metrology is not keeping pace with lithographic resolution capabilities of advanced imaging systems. In addition, preferred processing options such as chemical/mechanical polishing tend to render existing overlay metrology less effective for key process steps. The IC Technology Group seeks individuals interested in conducting further research in (1) novel electrical overlay-sensing instruments and techniques; (2) the design and optimization reference materials for scatterometry metrology; (3) noncontact electrical CD-measurement and extraction methodologies; and (4) design, fabrication, and

certification of CD standards in the range of 0.05 μm to 0.10 μm. We also encourage applicants with research experience in noncontact/nonintrusive electrical CD extraction and multimode overlay-sensor development, including MEMS-based overlay and CD reference-material implementations.

Contact: Michael W. Cresswell, 301-975-2072

Novel Test Structures for Characterizing the Performance of Advanced Multilevel Interconnection Systems

As the complexity of advanced integrated circuits continues to increase, new materials (copper, low-κ dielectrics) need to be thoroughly evaluated in order to produce highly reliable, low-resistance on-chip wiring. Extensions of traditional wiring technologies are no longer practical. The IC Technology Group seeks individuals interested in developing electrical test structures, measurement methods, and analysis models needed to evaluate copper-based, multilevel interconnection systems. Of particular importance are methods to measure interconnect and barrier film thickness, dimensional control, by filling, interfacial contact resistance, planarity, defect density/yield, dishing, stress effects, median-time-to-failure, and high-frequency performance. Emphasis is placed on developing thoroughly evaluated structures for use with high-measurement speed, low-frequency electrical test techniques.

Contact: Michael W. Cresswell, 301-975-2072

Electrical and Optical Characterization of Semiconductors and Devices

Research focuses on understanding the electronic, optical, and magneto-optical behavior of semiconductor materials and devices. Areas of interest include the role of impurities and native defects in bulk crystals, and novel and useful properties induced by quantum confinement in reduced dimensional structures (heterostructures, quantum wells, superlattices, and quantum wires and dots). A broad range of optical techniques is available for reflection, transmission and absorption, and modulation spectroscopy; photoluminescence and photoluminescence excitation; Raman and resonant-Raman scattering; and spectroscopic ellipsometry and surface photovoltage. A wide variety of electrical and magnetotransport techniques are also utilized to characterize the electronic properties. Emphasis is placed on understanding fundamentals and technologically relevant properties as well as developing accurate measurement techniques.

Contact: David G. Seiler, 301-975-2054

Physics of Semiconductor Devices

Device-modeling and theoretical-device physics research are in progress to interpret measurements of model parameters in microelectronic device simulators. One goal of this work is predictive computer simulation of devices with high carrier and doping concentrations. For example, topics include high-concentration effects, carrier lifetimes, carrier mobilities, and radiation effects that affect the operation and performance of semiconductor devices. The approach in this work involves the careful examination, extension, and experimental verification of the theoretical basis used in device models for silicon, gallium-aluminum-arsenide, and other compound semiconductor devices. Collaborations are in progress to include these improved physical models in device simulations and then to verify, validate, and benchmark these enhancements. We plan to extend the above calculations to include magnetic semiconductors (spintronics), such as manganese-doped gallium arsenide.

Contact: Herbert S. Bennett, 301-975-2079

Microelectronic Package Characterization

Research focuses on the thermal properties of microelectronic packages and interconnects. Our objectives are to improve methods for characterizing these properties for advanced packages and modules; improve measurement methods and techniques; and verify "compact" electrical and thermal models for packages and modules, and parameter extraction techniques for the models. We have fully equipped thermal characterization laboratories including an infrared thermal imager with μs temporal and 20 μm spatial resolution, and several computer workstations with a compliment of thermal and electrical modeling and analysis software.

Contact: David L. Blackburn, 301-975-2068

Quantum Devices for ULSI Circuits

The complementary-metal-oxide-semiconductor (CMOS) field-effect-transistor is showing fundamental limits associated with the laws of quantum mechanics and the limitations of fabrication tech-

niques. This is driving research on innovative solutions to augment or replace CMOS technologies. Quantum devices, such as quantum dots, resonant tunneling devices, and single-electron transistors, deliberately exploit quantum and size effects. We are interested in fundamental research in all aspects of quantum devices, particularly those that are compatible with Si technologies. Our interests include, but are not limited to, fabrication, simulation, and characterization of device structures and constituent materials/processes. Our primary expectation is to be able to identify and address critical metrology issues for this emerging technology of silicon-based quantum devices. In support of this research, we have a cleanroom with a variety of fabrication equipment including furnaces, evaporators, and optical and electron-beam lithography. We have numerous device, electrical, and physical simulation software available including the NanoElectronic Modeling program, NEMO; and the molecular simulation program, CeriusII/CASTEP. We have a wide range of electrical characterization equipment that allows device characterization at temperatures ranging from approximately 1 K to 700 K. This includes ultra-low noise probe stations, cryostats, semiconductor parameter analyzers for current-voltage measurements, ac capacitance-conductance-inductance measurements, specialized setups for Hall and magnetotransport measurements, and a variety of additional electronics. We also have numerous supporting analytical measurement techniques available including spectroscopic ellipsometry, atomic force microscopy, and scanning capacitance microscopy.

Contact: Eric M. Vogel, 301-975-4723, David L. Blackburn, 301-975-2068, or Curt A. Richter, 301-975-2082

Modeling Advanced Semiconductor Devices for Circuit Simulation

Accurate circuit simulator models for advanced semiconductor devices are required for effective computer-aided design of electronic circuits and systems. However, the semiconductor device models provided in most commercial circuit simulators (e.g., simulation program with integrated circuit emphasis) are based on microelectronic devices, and they do not adequately describe the dynamic behavior of advanced semiconductor devices. Therefore, research focuses on the following: (1) physics-based models - for advanced semiconductor devices such as power and compound semiconductor devices (these models are implemented into available circuit and system simulation programs); (2) parameter extraction algorithms — for obtaining model parameters from terminal electrical measurements; and (3) characterization procedures — for verifying the models' ability to simulate the behavior of the devices within application circuits. NIST also works closely with commercial software vendors to make the new models available to circuit design engineers and has established the NIST/IEEE Working Group on Model Validation to develop comprehensive procedures for evaluating the performance of circuit simulator models. (For more information, see ray.eeel.nist.gov/modval.html.)

Contact: Allen R. Hefner, Jr., 301-975-2071

MicroElectroMechanical Systems

The MicroElectroMechanical Systems (MEMS) Project focuses on the development of new MEMS-based sensors and actuators for measurement applications. It functions in a multidisciplinary environment with collaborations in the NIST laboratories in chemistry, materials science, physics, biotechnology, and building and fire research. Current activities in the project include thermal-based elements, mechanically resonant structures, microwave elements, and microfluidic systems. The project is also developing MEMS test structures, test methods, and standards to characterize device properties for device performance and reliability testing. These MEMS-based test structures are being utilized to characterize thin-film properties in mainline semiconductor fabrication processes. We are interested in post-doctoral applications not only from individuals who have specialized in MEMS research but also from individuals of other science disciplines who wish to learn microfabrication methods and apply their expertise for new measurement applications.

Contact: Michael Gaitan, 301-975-2070

Microfluidic Systems

Our work focuses on developing integrated circuit-based microreactors and other active elements and embedding them in plastic-based microfluidic systems. This technology will allow researchers to harness heat for monitoring and controlling chemical reactions in microfluidic systems that provide active control of processes in picoliter volumes. The microreactors are fabricated using a silicon integrated circuit (IC) process followed by post process bulk and surface micromachining steps. The ICs are embedded in the plastic and/or polymeric-

based substrates that contain a network of microchannels. Fabrication methodology is fully compatible with the monolithic integration of digital and analog circuits. We believe that integration is the key issue for advancement of the Microanalytical Laboratory of the future, and it is the basis of the "drop-in functionality" for microfluidic integration. Because of the multidisciplinary nature of this work, we are interested in post-doctoral candidates in engineering, chemistry, materials science, and physics. Research would focus on the development of new fabrication methodologies, design and fabrication of new thermal-fluidic systems, and device modeling and characterization.

Contact: Michael Gaitan, 301-975-2070

Reliability of Integrated Circuit Dielectric Films

Aggressive scaling of gate oxide thickness used in silicon integrated circuits necessitates the understanding of the physical mechanisms responsible for dielectric degradation and breakdown. We are particularly concerned with the reliability of ultra-thin gate oxides that are in the direct tunneling regime during circuit operation. Research focuses on (1) identifying parameters to determine the physics of time-dependent dielectric breakdown of ultra-thin dielectric films in the tunneling regime; (2) determining the effectiveness of highly accelerated stress tests to predict long-term reliability of thin dielectric films; (3) relating analytical characterization of oxide bulk and interfaces to electrical behavior; (4) identifying and controlling fabrication process parameters that affect intrinsic and extrinsic failure modes; and (5) characterizing and evaluating alternate dielectrics for use as substitutes for silicon oxide in advanced circuit technologies.

Contact: John S. Suehle, 301-975-2247

Physical and Electrical Properties of Advanced Gate Dielectric Films

It is increasingly difficult to characterize ultra-thin gate dielectric films (typically 0.1 nm to 3.0 nm) used in MOS devices as technology drives them ever thinner. We are developing electrical test methods (using conventional techniques such as I-V and C-V, as well as low-temperature magnetotransport techniques) to measure the physical properties (e.g., film thickness and permittivity) of alternate gate dielectric materials such as high-κ metal oxides as well as ultra-thin SiO_2. Electrical results are compared with those of optical and other measurement methods, and fundamental physical models are developed to be effective for more than one measurement technique. Because the interface between the dielectric film and the silicon substrate is critical to understanding these measurements, we are developing techniques to characterize buried interfaces (i.e., interface roughness) and are determining how the interface and physical properties affect device performance and reliability.

Contact: Eric M. Vogel, 301-975-4723, or Curt A. Richter, 301-975-2082

Measurement Traceability for Thin Dielectric Films

The development and fabrication of ultra-thin, increasingly sophisticated gate dielectrics is a key technology for integrated circuits at the 0.10 micrometer feature size and beyond. With the use of single-wavelength and spectroscopic ellipsometry, thin dielectric films are characterized for use in the calibration of instruments to monitor and control gate dielectric fabrication. Research involves the development of physical standards and supporting methodologies that will provide traceability to NIST for advanced gate dielectrics. Input from various physical, optical, and electrical techniques is needed to improve our knowledge of the structure and composition of advanced dielectrics and their interfaces for correct interpretation of ellipsometric measurements. Research will focus on relating the analyses of XTEM, surface second harmonic generation, scanning probe methods, X-ray reflectance, and various electrical techniques to improve our understanding of the structure of thin dielectric films, which would strengthen and extend NIST's capability for providing thin dielectric measurement traceability.

Contact: Curt A. Richter, 301-975-2082, or Nhan V. Nguyen, 301-975-2044

2003 International Conference on Characterization and Metrology for ULSI Technology, Mar. 24–28, 2003, Austin, TX

"The Semiconductor Electronics Division has initiated and organized a series of excellent meetings, the International Conferences on Characterization and Metrology for Ultralarge-Scale Integration (ULSI) Technology ….

Hard-bound proceedings of these conferences have been published by the American Institute of Physics and are regarded as the ultimate reference books on the latest developments in semiconductor metrology and as thorough reviews of state-of-the-art methods."

NRC Panel Report, An Assessment of the National Institute of Standards and Technology Measurement and Standards Laboratories: Fiscal Year 2000

The 2003 International Conference on Characterization and Metrology for ULSI Technology will be held Mar. 24-28, 2003, at the J.J. Pickle Research Campus, University of Austin, Austin, Texas, USA. The conference is the fourth in a series, all of which were coordinated under the under the leadership of the Semiconductor Electronics Division, NIST. Additional sponsors include the American Physical Society, the American Vacuum Society, the Electrochemical Society, International Semiconductor Manufacturing Technology, the Materials Research Society, the National Science Foundation, Semiconductor Equipment and Materials International, the Semiconductor Research Corporation, and the University of Texas at Austin.

This conference will bring together scientists and engineers interested in all aspects of the technology and characterization techniques for silicon device research, development, manufacturing, and diagnostics: chemical and physical, electrical, optical, *in situ*, and real-time control and monitoring. The conference is dedicated to summarizing major issues and giving critical reviews of important semiconductor techniques that are needed by the semiconductor industry. The International Technology Roadmap for Semiconductors (ITRS) will be reviewed as a benchmark for all characterization and metrology needs. Revisions of the ITRS will be discussed, along with the Metrology Roadmap.

Bob Helms, Keynote Speaker, President and CEO of International SEMATECH

The conference provides a forum to present and discuss critical issues, problems and limits, evolving requirements and analysis needs, future directions, and key measurement principles, capabilities, applications, and limitations. The conference will comprise formal invited presentation sessions by high-level industry leaders, led by Bob Helms, President and CEO of International SEMATECH (pictured), and poster sessions for contributed papers. The poster papers will cover new developments in characterization/metrology technology. Also, for the first time in the series, the 2003 conference will offer five short courses, all to be held on Mar. 24th from 1:00 pm – 5:00 pm and all at a fee to be determined. The courses and instructors are:

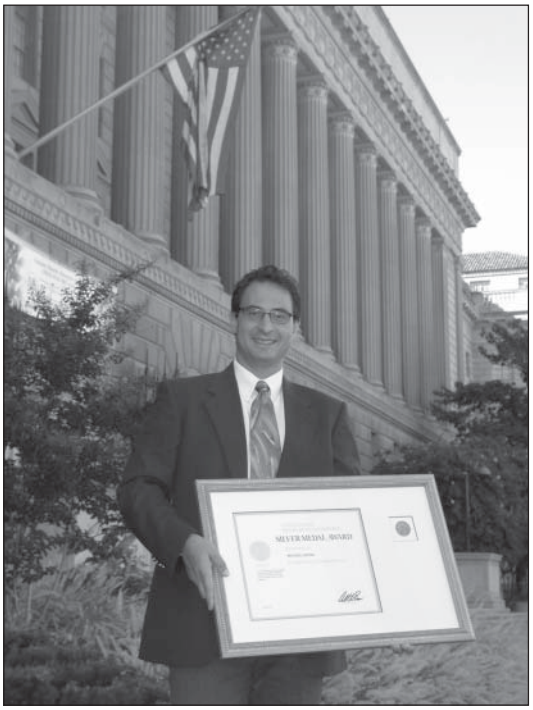
- Electrical Metrology for ULSI Process Control: R.G. Mazur and G.A. Gruber, Solid State Measurements, Inc.
- Full Wafer Defect Detection, Review, and Characterization: C.R. Brundle, formerly of Applied Materials, Inc.
- High Resolution X-ray Reflection and Diffraction Methods for ULSI Materials Characterization: R. Matyi, National Institute of Standards and Technology
- Surface Analysis Characterization of High-κ Gate Dielectrics: R. Hockett, Charles Evans and Associates
- Variable Angle Spectroscopic Ellipsometry for Semiconductor Applications: T. Tiwald, J.A. Woollam Co., Inc.

Additional details regarding the upcoming conference, including details on registration, accommodations, and other program information, are available on the conference Web site at: www.eeel.nist.gov/812/conference.

The proceedings for the previous three conferences in this series were published as hardcover volumes by The American Institute of Physics, New York and are available for purchase at: proceedings.aip.org/proceedings/confproceed/550.jsp. The most recent proceedings, *Characterization and Metrology for ULSI Technology: 2000*, was published in Feb. 2001.

Gaitan Receives DoC Silver Medal Award

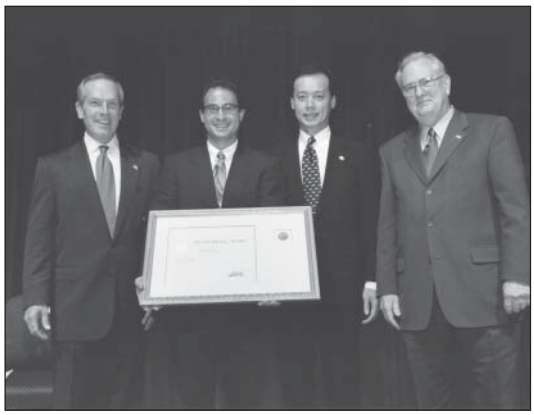
Michael Gaitan, Leader of the MicroElectroMechanical Systems (MEMS) Project in the Semiconductor Electronics Division, was awarded a 2002 Department of Commerce (DoC) Silver Medal and cited "for his championing of MEMS research at NIST and world-wide, particularly his pioneering efforts on CMOS compatible MEMS."



Gaitan holds his Silver Medal Award by the Herbert C. Hoover Building, Washington, D.C.

Gaitan was nominated for spearheading the development of new measurement capabilities for the MEMS industry and the development of novel MEMS technologies that have been incorporated by industry into military and commercial products. His work has allowed NIST to develop MEMS-based metrology programs, which have resulted in the first MEMS-based test structures to measure mechanical strain in integrated circuit (IC) interconnects in fully processed ICs.

Gaitan's work at NIST has been cited on the front page of *EE Times*, cited on the cover of *IEEE Devices and Circuits Magazine*, and highlighted in a half-page article in the *New York Times*. He has 68 publications, 13 first author publications, and 365 citations, which ranks him in the top 5 % of NIST employees. Gaitan has been awarded seven patents and has one additional patent pending. He has authored 2 of the 61 actively licensed patents for all NIST employees. Gaitan received the DoC Bronze Medal in 1993 for his work in making "MEMS technology available to designers of Integrated Circuits."



Gaitan is presented the Silver Medal Award. (from left to right) Donald Evans, DoC Secretary; Michael Gaitan, NIST; Benjamin Wu, Deputy Under Secretary of Commerce for Technology; and Arden Bement, NIST Director.

Michael Gaitan received his Ph.D., MSEE, and BSEE in 1988, 1982, and 1980, respectively, from the University of Maryland, College Park. He was awarded the University of Maryland/National Bureau of Standards (NBS) Graduate Research Fellowship from 1980 to 1982. Following this, he began employment at NBS, now called the National Institute of Standards and Technology (NIST). From 1980 to 1988, he developed measurement methods and models for silicon dioxide-silicon interface traps. In 1988, he began work on microfabrication and integration of thermo-electro-mechanical elements in standard IC fabrication and application specific integrated circuit (ASIC) technologies. He is now the Leader of the MEMS Project in the Semiconductor Electronics Division. The primary goal of his work is to develop MEMS-based test structures, test methods, and measurement standards for the MEMS and IC industries. Gaitan is a senior member of the IEEE and is serving as treasurer of the International Electron Devices Meeting (IEDM).

The DoC Silver Medal Award is the second highest honorary award granted by the Secretary of Commerce. A Silver Medal is defined as exceptional performance characterized by noteworthy or superlative contributions which have a direct and lasting impact within the Department.

Division Teamwork Team Receives DoC Bronze Medal Award

The Division Teamwork Team, composed of Monica Edelstein (Team Chair), Sherri Gorman, Joseph Kopanski, Loren Linholm, Christine Murabito, Lori Guariglia, and Curt Richter, received a 2002 Department of Commerce (DoC) Bronze Medal "for their outstanding contributions in improving teamwork, cooperation, and communications within the SED."

Teamwork Team Photo.

A Bronze Medal is the highest honorary award granted by an operating unit or Secretarial Officer or equivalent. A Bronze Medal is defined as superior performance characterized by outstanding or significant contributions which have increased the efficiency and effectiveness of the operating unit.

Background

Confronted with direct feedback about Division communications and teamwork from the 2000 NIST-wide employee survey, a team was formed in the Division to tackle these issues, which were also prevalent throughout NIST. After confronting and identifying critical issues, the team quickly recommended the hiring of professional consultants and eagerly began its work with the support and encouragement of Division management. A Division "needs assessment" survey was designed and conducted to identify the communications and teamwork issues more clearly in response to the NIST-wide surveys.

Over the past year, there has been a noticeable increase in the professional and support staff communications, cooperation, and interpersonal interaction within the Division. This can be directly attributed to the formation and hard work of the Teamwork Team. Prior friction and negative tones between people have substantially diminished, and there is a distinct improvement in efficiency and morale throughout the Division. There is general recognition of these positive outcomes, and the expectation is that the substantial progress made already will continue.

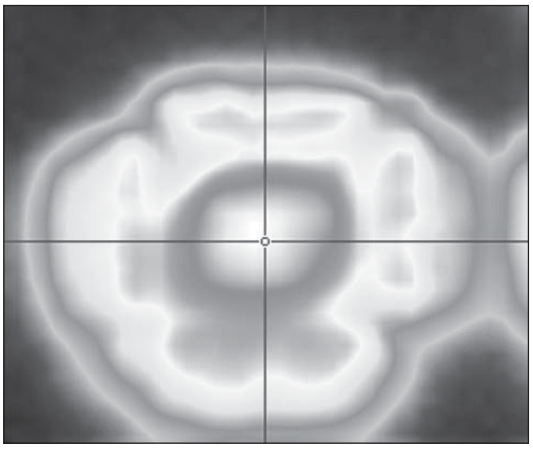
The Teamwork Team is a cross-discipline internal team comprised of Division professional, technical, and administrative staff chaired by Monica Edelstein. Since the fall of 2000, this team has tirelessly executed its mission: to help management drive changes and improvements in Division-wide communications. Working with external consultants, Dailey & O'Brien, Inc., the team has become the internal consultant to the Division management. The team recommended, orchestrated, and executed learning events for all staff; focused on individual and team efforts to improve communications; helped conduct and improve Division meetings; collected data on what is working and not working about Division communications and advised management on specific action steps; promoted new team behaviors to encourage staff to speak directly with management, not the grapevine, about issues that need to be addressed in the Division; recommended developing a frequently asked for (Web-based) "users' guide" to administrative policies and procedures (NIST and Division) that address the source of much miscommunication and frustration for staff; and acted as a "model" to staff for positive, professional behavior.

Results to date have been impressive. When surveyed in Jun. 2001, 82 % of Division respondents (69 % of the Division) acknowledged they had seen improvement in communications within the Division. Also, 95 % of respondents indicated they were hopeful that teamwork is improving within the Division. Ninety-two (92) percent saw improvement in the work environment. And finally, 92 % of the surveyed staff saw progress toward a more cooperative workplace over the next 12 months.

Integrated Circuit Gas Sensing System Technology Valuable for Homeland Security

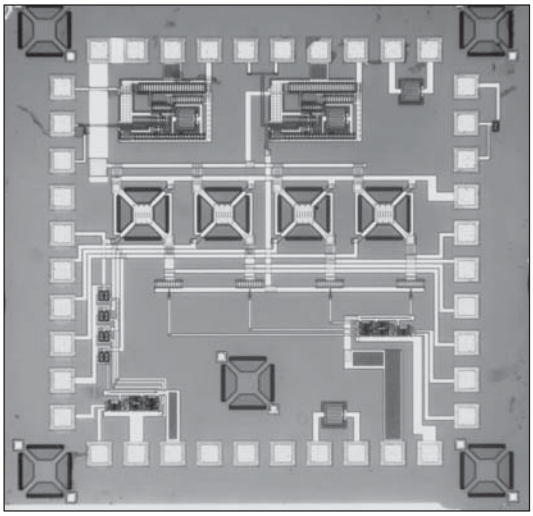
Today, portable devices for detecting toxic airborne chemicals are largely limited to specialized equipment designed for use by the military or by first responders to chemical spills. In the event of an attack involving toxic chemical agents — such as the recent use of sarin gas in a Tokyo subway station — such portable detectors typically would not arrive on the scene until after victims already had been harmed by the gas.

NIST is currently conducting research on a class of microsensors that have the potential to serve as a cost-effective early warning system for the presence of toxic gases. This same basic technological approach also may be applicable to detection of vapors from explosive materials. The NIST integrated smart gas sensing technology uses an array of microhotplates with metal oxide sensing films. The microhotplate gas sensors are incorporated into an integrated circuit device that can be fabricated with a standard CMOS process, enabling the devices to be produced inexpensively with built-in digital and analog electronic processing circuits.



Temperature contour map of a microhotplate structure.

A key advantage of this technology is that an array of microhotplates with various types of films can be programmed to cycle through specific temperatures resulting in a signature for specific chemicals that can be matched up against a library to identify both the type and concentration of the gas in the ambient air. Furthermore, the integration of the sensors onto the same semiconductor substrate as the electronic circuitry improves the signal to noise ratio substantially and enables the inclusion of self-calibration circuits.



NIST chemical sensor semiconductor circuit with four microheaters.

Because the performance of the microhotplate gas sensor is dependent upon rapid heating and cooling of the microhotplate sensing surface, thermal analysis of the structure is essential. The small size and fast heating speed of these micromachined devices previously made it difficult to measure dynamic temperature distribution, so a new NIST-developed high-speed transient thermal imaging system is used to make a unique "thermal contour" movie. NIST researchers found that the thermal imaging system can be used to optimize the design of microhotplates, which consist of a heater, a metal thermometer/heat distribution plate, and electrical contacts, all separated by insulating layers.

With funding from the Defense Threat Reduction Agency, NIST researchers have demonstrated that simulants of sulfur-mustard compounds and nerve agents (sarin, VX, etc.) can be detected at or significantly below the l-part-per-million level in laboratory testing. Preliminary testing at the Army's Edgewood Arsenal has confirmed that this sensitivity is feasible with actual chemical warfare agents. Further research is under way to demonstrate that the presence of each agent will produce unique temperature-dependent response signatures.

SPS Intern Contributes to Division Research

"This week the research got fun and interesting! In fact, the hafnium data that I have been analyzing turned out to have some interesting features in the dielectric functions for the samples. These features, or the lack thereof, describe whether the material is amorphous or crystallized. So, now my job is to make connections between what types of samples (how they are grown, annealed, etc.) have these features and develop a working theory as to why or when the hafnium becomes crystallized."

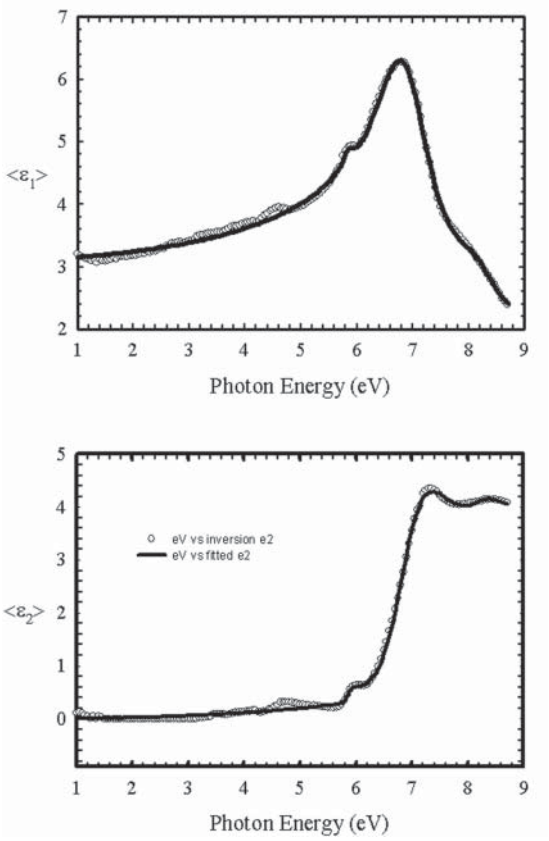
excerpt from Eva Wilcox's June 26, 2002, on-line SPS journal, www.spsnational.org/programs/wilcoxjournal.htm

The Semiconductor Electronics Division (SED) welcomed its first Society of Physics Students (SPS) intern during the summer of 2002 when Eva Wilcox joined the Division's Advanced Microelectronics Technology Group for her internship.

The SPS, which operates within the American Institute of Physics (AIP), is a professional association designed for students. In the words of Gary White, the Director of the SPS, "SPS internships are designed to create broad-based learning opportunities for undergraduate physics majors. Students were placed in organizations and agencies, which utilize the energy and diversity of aspiring students and contribute to their professional development through meaningful assignments, both relevant to the institution's programs and in the advancement of physics or allied sciences."

(From left to right) Eva Wilcox, SPS Intern; Eva's father; Nhan Van Nguyen, NIST; Eva's mother; Eric Vogel, NIST; and David Seiler, NIST.

While in the SED, Wilcox worked with Nhan V. Nguyen in the Thin Film Process Metrology Project. Eva was with the project only for two months, but she demonstrated her quick learning skills and her outstanding ability to work independently. The project involves a study of the instrument stability and the data analyses of a set of technologically important high-κ dielectric thin films using spectroscopic ellipsometry. For instance, Eva was able to determine the dielectric function of thin HfO_2 films and model it with a theoretical dispersion (see figure). During her stay, she was able to work independently both in the laboratories and when doing data modeling as soon as we provided some frame work. In addition, she was able to assess the results of her experimental analyses critically and make sound observations and conclusions of the research results. At the end of the two month internship, she was able to put together an excellent report, and she professionally presented the work to our group and her colleagues at the SPS. Part of her work is currently being integrated in the project's other experiments for a scientific publication.



The dielectric function for high-κ dielectric thin HfO_2 films determined experimentally (open circles) and modeled with a theoretical dispersion (solid line) by Eva Wilcox using the Semiconductor Electronics Division's new Vacuum Ultraviolet Spectroscopic Ellipsometer.

Eva Wilcox graduated in physics teaching from Brigham Young University, Provo, Utah. For the past four years in school she researched in the area of neutron detection at school for her Honors thesis requirement and worked at NIST each summer through the Summer Undergraduate Research Fellowship (SURF) program.

Transfer of Equipment to the University of Puerto Rico at Mayaguez Strengthens Power Electronics Research

A recent collaborative effort with the University of Puerto Rico at Mayaguez (UPRM) led to the development and delivery of new measurement systems that are benefiting the power electronics industry through involvement with the Center for Power Electronics Systems (CPES), a National Science Foundation Engineering Research Center. The collaboration was initiated by Dr. Allen Hefner of the Semiconductor Electronics Division (SED), Prof. Miguel Velez of the UPRM Electrical Engineering Dept., Prof. Jorge Gonzalez of the UPRM Mechanical Engineering Dept., and Jason Lai of the Virginia Polytechnic Institute and State University (VPISU) Electrical Engineering Dept. The collaboration involves the development of electro-thermal simulation models and thermal metrology for high power electronic systems. In 1993, Dr. Hefner pioneered the electro-thermal simulation methodology used in commercial system simulation programs. CPES's interest is in applying the methodology to high power electronic systems.

Jose J. Rodriguez and Allen Hefner at the UPRM.

Zharadeen Parrilla Rodriguez and Jose J. Rodriguez, two UPRM students, spent the summer of 2001 with the SED. Jose developed analog-hardware-description-language models for electrothermal behavior of multi-chip power modules and cooling systems. Zharadeen developed the measurement system to calibrate and validate the developed models. The measurement system was transferred to the UPRM in the fall of 2001. Jose used this NIST work as the basis for his MS power electronics research, and Zharadeen was awarded funding to continue her research at CPES using this equipment. At the annual UPRM Industry Affiliations Program (IAP) conference in Apr. 2002, Jose and Zharadeen's project was voted "Best Project of the Year" by a committee of participating industrial companies, including IBM, Raytheon, Kodak, MITRE, and others, underscoring the significance of the NIST collaboration.

Allen Hefner (NIST), Jason Lai (VPISU), Philip Krein (Univ. of Illinois at Urbana), and Miguel Velez (UPRM) at the UPRM.

Over the summer of 2002, two new UPRM students, Jose M. Ortiz-Rodriguez and Madelaine Hernandez-Mora, continued the collaborative research with the SED. Ortiz-Rodriguez extended the high-power module electro-thermal model to include the new planar packaging technology of the CPES integrated power electronic module (IPEM). Hernandez-Mora, David Berning (SED), and Colleen Ellenwood (SED) developed a high-speed chip temperature measurement system using the temperature sensitive parameter method. The developed models are being used by John Reichl, a Masters Degree student from Virginia Tech., to simulate the electro-thermal performance of high-power inverter systems.

The UPRM and VPISU are two of five universities in the CPES consortium. The CPES Mission is to improve competitiveness of the U.S. power electronics industry by developing integrated systems that use intelligent power electronic modules. These modules are used for industrial motor drives, electric vehicles, and other high power electronic systems. The developed electro-thermal models enable simultaneous simulation of electrical and thermal performance of high-power electronic systems.

Educational Outreach by Division Staff

Dear Dave the Scientist,

Thank you for coming to our classroom. I enjoyed you sharing science with us. I liked when you showed us how air can travel through many things like space, and that cold things can squeeze oxygen or I would say air!

I liked when you showed us that electricity can travel through many things and can pop balloons, that are blown 'up'. Also that tops can come in many shapes and also many sizes!

I have done many things in science like sounds, transportation, and many things but the most important thing is that you CAME!!
THANK YOU!!

Your friend,
S.K.

Letter from S.K., student, Whetstone Elementary School, Gaithersburg, Maryland

The National Institute of Standards and Technology takes an active role in promoting science and technology education throughout the Gaithersburg, Md., community.

Michael Gaitan explains his MEMS work by relating it to common end-products for the NIST 'Take Our Daughters and Sons to Work' Day.

Michael Gaitan with his students from the NIST 'Take Our Daughters and Sons to Work' Day.

David Seiler performs science experiments for a local elementary school.

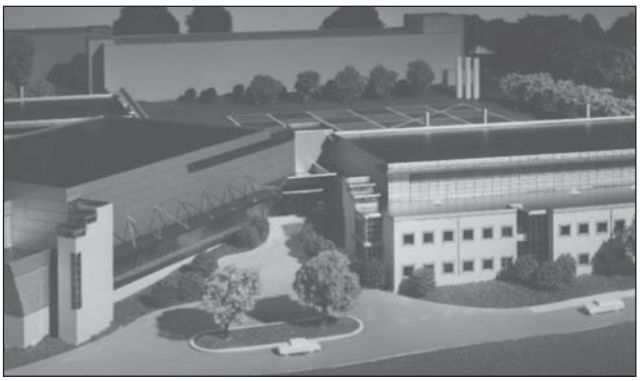
Drawing of "Dave the Scientist" Seiler from C.C., student, Whetstone Elementary, Gaithersburg, MD.

Richard Allen and a group of students prepare to package diced chips after removing them from the tape during the NIST Centennial Open House.

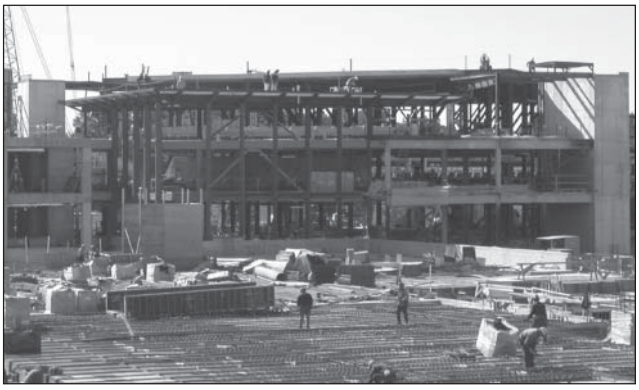
Students prepare for their next experiment during the NIST Centennial Open House.

Future NIST Cleanroom Facility on Track for Spring 2003 Completion

The Advanced Measurement Laboratory (AML) Cleanroom occupies 8,520 square meters of the new AML, which is currently under construction in NIST, Gaithersburg, Maryland. The above-ground Cleanroom has a NC-55 acoustical design and will be a Class 100 facility (3.5 or fewer particles per liter), upgradeable to Class 10. Construction for the facility is on schedule and should be completed in the spring of 2003.



AML model showing the main entrance between the Cleanroom (left) and Instrument East Wings (right).



Construction of the AML Cleanroom, late Oct. 2001.

Construction of the AML Cleanroom, late Oct. 2002.

"The AML is the world-class facility that will provide the United States with global leadership in measurements and standards, and set the foundation for technological advances well into the 21st century … What will come from within these walls will enhance U.S. industrial competitiveness, foster economic growth and improve the quality of life for all Americans."

William Dailey, former Commerce Secretary

NIST's Gaithersburg, Maryland Campus and Surrounding Area

NIST MISSION -
To develop and promote measurement, standards, and technology to enhance productivity, facilitate trade, and improve the quality of life.

NIST VISION -
To be the global leader in measurement and enabling technology, delivering outstanding value to the nation.

"Washington is located in a region that is rich in historic lore and natural beauty. From the bustling sounds of a Chesapeake Bay harbor to the utter stillness of a Blue Ridge mountaintop, from the small, old tobacco farms of southern Maryland to the grand estates of Virginia's hunt country, you will find a richness of scenery and history."

"Welcome to Washington" brochure, National Park Service, U.S. Department of the Interior

About NIST

The National Institute of Standards and Technology (NIST) is an agency of the U.S. Department of Commerce's Technology Administration. NIST was established in 1901 by Congress "to assist industry in the development of technology ... needed to improve product quality, to modernize manufacturing processes, to ensure product reliability ... and to facilitate rapid commercialization ... of products based on new scientific discoveries."

Location

Located approximately 40 km Northwest of Washington, D.C., on a 234-hectare campus, NIST Gaithersburg offers the advantages of being in close proximity to government offices, while maintaining the seclusion of a rural setting. The site is beautifully landscaped and features mature trees and ponds, as well as a herd of white-tailed deer and gaggles of Canada geese. Walking paths and picnic areas provide easy and pleasant access for outdoor repasts, biking, walking, and jogging. The campus also is easily accessible, with a shuttle service to a nearby metro (subway) station and is in close proximity to three major airports.

NIST's 11-story Administration Building.

Staff

NIST's staff is comprised of about 3,300 scientists, engineers, technicians, business specialists, and administrative personnel. About 1,500 visiting researchers complement the staff. In addition, NIST partners with 2,000 manufacturing specialists and staff at affiliated centers around the country.

Some Nearby Attractions

Landmarks

Bureau of Engraving and Printing
Capitol Building
Ford's Theater
Franklin Delano Roosevelt Memorial
I.R.S. Building
J. Edgar Hoover F.B.I. Building
Jefferson Memorial
Library of Congress
Lincoln Memorial
National Archives
Supreme Court
Union Station
Vietnam Veterans Memorial
Washington Monument
White House

The NIST Gaithersburg campus is home to many different types of wildlife.

Museums and Other Attractions

Capital Children's Museum
Corcoran Gallery
Kennedy Center
MCI Center
National Geographic Society
National Sports Gallery
National Theater
Smithsonian Institute
United States Holocaust Memorial Museum
Washington D.C. Convention Center

Outdoor Attractions

Antietam National Battlefield Site
C&O Canal National Historical Park
Clara Barton National Historic Site
Eisenhower National Historic Site
Fort McHenry
Fort Washington
Gettysburg National Military Park
Glen Echo Park
Great Falls Park
Greenbelt Park
Mount Vernon
Oxon Hill Farm
Prince William Forest Park
Rock Creek Park
Shenandoah National Park
Wolf Trap Farm Park for the Performing Arts

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