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Silicon Microelectronics Programs At the National Institute of Standards and Technology

Programs, Activities and Accomplishments

JULY 2002

Edited by

Stephen Knight Joaquin V. Martinez de Pinillos and Michele Buckley



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Cover Picture Caption

Silicon Microelectronics Programs at the National Institute of Standards and Technology is a NISTwide effort to meet the highest priority measurement needs of the semiconductor industry and its supporting infrastructure. Research efforts include development of standard test structures for interconnect reliability evaluation; fundamental measurements of ionization cross sections of gas species used in plasma processing of integrated circuits; development of advanced at-speed test techniques for gigahertz integrated circuits; and development of precise measurement techniques for characterizing aspheric lenses for Extreme Ultraviolet Lithography.

Silicon Microelectronics Programs at the National Institute of Standards and Technology

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NISTIR 6884 July 2002

U.S. DEPARTMENT OF COMMERCE Donald L. Evans, Secretary

Technology Administration Phillip J. Bond, Under Secretary of Commerce for Technology

National Institute of Standards and Technology Arden L. Bement, Jr., Director



Disclaimer: Certain commercial equipment and/or software are identified in this report to adequately describe the experimental procedure. Such identification does not imply recommendation or endorsement by the National Institute of Standards and Technology, nor does it imply that the equipment and/or software identified is necessarily the best available for the purpose.

References: References made to the *International Technology Roadmap for Semiconductors* (ITRS) apply to the most recent edition, dated 1999. This document is available from the Semiconductor Industry Association (SIA), 181 Metro Drive, Suite 450, San Jose, CA 95110, phone: (408) 436-6600; fax: (408) 436-6646.

Appendices: The reader will notice that there are acronyms and abbreviations throughout this document that are not spelled out due to space limitations. To enable the reader to learn more about these acronyms and abbreviations, we have included an acronyms/abbreviations list is in an appendix at the end of this report. We have also included a list of the National Semiconductor Metrology Program (NSMP) projects, which demonstrates the synergism resulting from this matrix-managed program.

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Jacob Sand Barrier

Welcome and Introduction

Welcome

The microelectronics industry supplies vital components to the electronics industry and to the U.S. economy, enabling rapid improvements in productivity and in new high technology growth industries such as electronic commerce and biotechnology. To achieve its goal of strenghting the U.S. economy, the National Institute of Standards and Technology, NIST, works with industry to develop and apply technology, measurements and standards. NIST has substantial efforts on behalf of the semiconductor industry and its infrastructure; this report describes the many projects being conducted at NIST that constitute that effort.

Historical Perspective

NIST's predecessor, the National Bureau of Standards (NBS), began work in the mid-1950's to meet the measurement needs of the infant semiconductor industry. While this effort was initially focused on transistor applications in other government agencies, in the early 1960's the Bureau sought industry guidance from the American Society for Testing and Materials (ASTM) and the (U.S.) Electronic Industries Association (EIA). To address ASTM's top priority of accurate was the accurate measurement of silicon resistivity, NBS scientists developed a practical non-destructive method ten times more precise than previous destructive methods. This method is now the basis for five industrial standards and for resistivity standard reference materials widely used to calibrate the industry's measurement instruments. The second project, recommended by a panel of EIA experts, addressed the "second breakdown" failure mechanism of transistors. The results of this project have been widely applied, including solving a problem in main engine control responsible for delaying the launch of a space shuttle.

From these beginnings, by 1980 the semiconductor metrology program had grown to employ a staff of sixty with a \$6 million budget, mostly from a variety of other government agencies. Congressional funding in that year gave NBS the internal means to maintain its semiconductor metrology work. Meeting industrial needs remained the most important guide for managing the program.

Industrial Metrology Needs

By the late 1980's, NBS (now NIST) recognized that the semiconductor industry was applying a much wider range of science and engineering technology than the existing NIST program was designed to cover. The necessary expertise existed at NIST, but in other parts of the organization. In 1991, NIST established the Office of Microelectronics Programs (OMP) to coordinate and fund metrological research and development across the agency, and to provide the industry with easy single point access to NIST's widespread projects. Roadmaps developed by the (U.S.) Semiconductor Industry Association (SIA) have independently identified the broad technological coverage and growing industrial needs for NIST's semiconductor metrology developments. As the available funding and the scope of the activities grew, the collective name became the National Semiconductor Metrology Program (NSMP), operated by the OMP.

The NSMP has stimulated a greater interest in semiconductor metrology, motivating most of NIST's laboratories to launch additional projects of their own and to cost-share OMP-funded projects. The projects described in this book represent this broader portfolio of microelectronics projects. Most, but not all, of the projects described are partially funded by the NSMP, which provided a \$12 million budget in fiscal year 2002.

Fostering NIST's Relationships with the Industry

NIST's relationships with the SIA, International SEMATECH, and the Semiconductor Research Corporation (SRC) are also coordinated through the OMP. Staff from OMP represent NIST on the SIA committees that develop the International Technology Roadmap for Semiconductors (ITRS) as well as on numerous SRC Technical Advisory Boards. OMP staff are also active in the semiconductor standards development work of the ASTM, the Deutsches Institut für Normung (DIN), the EIA, the International Organization for Standardization (ISO), and Semiconductor Equipment and Materials International (SEMI).

Learn More about Semiconductor Metrology at NIST

This publication provides summaries of NIST's metrology projects for the silicon semiconductor industry and their suppliers of materials and manufacturing equipment. Each project responds to one or more metrology requirements identified by the industry in sources such as the ITRS. NIST is committed to listening to the needs of industry, working with industry representatives to establish priorities, and responding where resources permit with effective measurement technology and services. For further information, please contact NIST as follows:

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Lithography

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Advances in lithography have largely driven the spectacular productivity improvements of the integrated circuit industry, a steady quadrupling of active components per chip every three years over the past several decades. This continual scaling down of transistor dimensions has allowed more and more components on a chip, lowered the power consumption per transistor, and increased the speed of the circuitry. The shrinking of device dimensions has been accomplished by shortening the wavelength of the radiation used by the lithography exposure tools. The industry at this point has moved into the deep ultraviolet (DUV) spectrum. Currently, exposure tools operating at 193 nm are being introduced, and exposure tools operating at 157 nm are in development. Looking beyond the deep ultraviolet, extreme ultraviolet radiation (EUV) at 13 nm is being investigated, and demonstration tools are being designed and assembled. The overall goal of this task is to support these developments in DUV and EUV. The areas of emphasis are lens materials, laser calorimetry, radiation detector sensitivity and damage, EUV lens metrology, and metrology for the development of advanced phoresist materials. Technical Contacts: J. H. Burnett M. Dowell R. Gupta

"It's an excellent service NIST has performed for the entire industry. The kind of thing NIST is there for – to identify issues before the train wreck takes place." Mordechai Rothschild, Massachusetts

Institute of Technology's Lincoln Laboratory

Metrology Supporting Deep Ultraviolet Lithography

Goals

Develop solutions to key metrology issues confronting the semiconductor lithography industry. These include development of measurement methods and standards for characterizing deep ultraviolet (DUV) laser sources, detectors, and materials. One focus is on delivering highaccuracy measurements of UV detector parameters and materials properties of immediate need by the industry. There is ongoing activity in the following areas: standards development, calibration services, characterization of optical materials, sources, and detectors, in addition to advising customers on in-house measurements.

Customer Needs

Increasing information technology requirements have yielded a strong demand for faster logic circuits and higher-density memory chips. This demand has led to the introduction of DUV laserbased lithographic tools for semiconductor manufacturing. These tools, which employ KrF (248 nm) and ArF (193 nm) excimer lasers, have led to an increased demand for accurate measurements at DUV laser wavelengths. Next generation tools employing F_2 (157 nm) excimer lasers, projected for insertion into production lines by 2005, require even higher accuracy measurements. To support these efforts, the National Institute of Standards and Technology (NIST), with International SEMATECH support, has initiated a DUV metrology program focusing on the characterization of DUV optical materials, sources, and detectors.

The potential solutions for lithographic systems are discussed in the 2001 International Technology Roadmap for Semiconductors on page 14 of the Lithography Section, and in Figure 34 on page 15. "Optical lithography is the mainstream approach through the 90 nm node,---." The emphasis is on 193 nm and 157 nm light source systems.

Technical Strategy

1. Beginning with the first edition of the National Technology Roadmap for Semiconductors (NTRS) in 1992, the semiconductor industry has made an organized, concentrated effort to reduce the feature sizes of integrated circuits. As a result, there has been a continual shift towards shorter exposure wavelengths in the optical lithography process. Because of their inherent characteristics, deep ultraviolet (DUV) lasers, specifically KrF (248 nm) and ArF (193 nm), and more recently F_2 (157 nm) excimer lasers are the preferred sources for high-resolution lithography at this time. To meet the laser metrology needs of the optical lithography community, we have developed primary standards and associated measurement systems at 193 and 248 nm, and are in the process of developing standards at 157 nm.



Excimer laser calorimeter for 157 nm measurements.

DELIVERABLES: Develop a 157 nm excimer laser primary standard and calibration service to provide support for the next generation of optical lithography. 1Q 2003

2. In addition to existing DUV laser measurement services, there is increasing demand for laser dose measurements, *i.e.*, energy density, where the detector samples a fraction of the total laser beam. Accurate laser dose measurements are important because small area detectors are widely used to monitor laser pulse energy density at the wafer plane of a lithographic tool. Accurate measurements of laser dose are especially crucial to the development of new resist materials, since lower dose requirements lead to greater wafer throughput and also extend the lifetime of an exposure tool's optical components as well.

DELIVERABLES: Reduce overall calibration uncertainty to a level of 1 %. 4Q 2002



Dose meter calibration system. The energy meter acts as a monitor to record pulse-to-pulse laser energy fluctuations.

3. High-accuracy measurements of the index properties of UV materials are a requirement for the design of DUV lithography systems. To meet this demand NIST has developed methods to make measurements of the DUV refractive index, as well as its wavelength, temperature, and stress dependencies to the high accuracy needed. Index variations and birefringence have become a limiting factor in the development of the optics for lithography systems, especially at 157 nm. To address this problem we have developed unique VUV polarimetry and Twyman-Green interferometer systems to measure 157 nm index variation in lens materials due both to external stress and grown-in defects.

DELIVERABLES: Develop capability of completely characterizing index inhomogeneities of DUV materials near 157 nm at the sub ppm level. 4Q 2002

4. In the course of our measurements we discovered that in addition to index variations and birefringence due to material defects and external stress, there are also index variations and birefringence intrinsic to the material. The commonly-accepted assumption that the cubic symmetry of the crystals used would ensure the isotropy of the optical properties, in fact breaks down due to the finite value of the photon momentum q. This previously-neglected effect on ultraviolet optics has a $1/\lambda^2$ wavelength dependence, and is negligible at visible wavelengths, where the index homogeneity and birefringence are measured. However, at 157 nm the effect is large (~ten times the 157 nm birefringence specification), and this has serious implications on 157 nm lithography system design and performance. This intrinsic birefringence must be accurately characterized for all materials considered for optics in 157 nm systems, including the mixed crystals $Ca_{1-x}Sr_xF_2$ we are co-developing that have the potential of having negligible intrinsic birefringence.

DELIVERABLES: Complete measuring intrinsic birefringence of UV materials, including mixed crystals. 4Q 2002

5. We are developing a new method for measuring the refractive index of transmissive samples to a high accuracy of $\approx 0.000 \%1$ in the DUV and VUV using a VUV FT spectrometer. This technique will allow measurements down to 135 nm using synchrotron radiation as a continuum source. This method will also be extended to measure the index and the thermal coefficient of the refractive index for liquids in the UV/VUV spectral range.

DELIVERABLES: Measurements of refractive index in the VUV using an interferometric technique in conjunction with SURF III. 1Q 2003

6. Our efforts for complete characterization of the optical properties of materials involve measuring the transmittance, reflectance, surface and bulk scatter, and surface and bulk absorption. This characterization is done on one of the beamlines at the NIST Synchrotron Ultraviolet Radiation Facility (SURF) which is devoted to material and detector characterization in the wavelength range 120 nm to 320 nm. We have used this facility to characterize various samples of calcium fluoride where the transmittance and reflectance was measured with an uncertainty of better than 1 %.

SURF III acts as the primary standard for both sources and detectors in the DUV and VUV spectral region.

DELIVERABLES: Achieve a 0.1 % standard uncertainty of UV irradiance from 3 nm to 400 nm, and enable accurate, direct radiance and irradiance comparisons with new as well as existing source transfer standards. 2Q 2003

7. Monochromatized radiation from SURF III along with a cryogenic radiometer is used to provide absolute detector-based radiometric calibrations in the spectral range from 125 nm to 320 nm with a standard uncertainty of better than 1%. This facility has also been used to study the degradation in diodes induced by exposure to UV radiation. A wide variety of diodes (Si diodes, nitrided Si diodes, PtSi, GaN, GaP, GaAsP, and diamond) were characterized for spectral responsivity and uniformity mapping, and the degradation in these diodes at 130 nm was also measured.

A new facility for characterizing the degradation of diodes to excimer radiation at 157 has been completed. This facility allows the measurement of the spectral responsivity of the devices in the spectral range from 130 nm to 500 nm along with the measurement of the reflectivity of the diodes as the devices are irradiated by the excimer radiation. This allows identification of potentially stable diodes for UV irradiance measurements. Some preliminary results regarding stability of pyroelectric detectors under excimer radiation have also been obtained. The facility can also be used to characterize other types of detectors such as photochromic films.

DELIVERABLES: Characterize the stability of a variety of semiconductor diodes and pyroelectric detectors to excimer radiation at 157 nm. 2Q 2003

8. We plan to use the synchrotron radiation in conjunction with a cryogenic radiometer to measure the transmittance, reflectance, surface and bulk losses, which would lead to a complete optical characterization of the transmissive samples. Capability will also be developed to make polarization dependent measurements in the spectral range from 125 nm to 320 nm.

DELIVERABLES: Build a state of the art facility for an accurate and complete characterization of the optical properties of transmissive materials. 4Q 2002

Accomplishments

Established capability to accurately perform absolute responsivity calibrations of laser dose meters at the laser wavelength of 193 nm. Additional excimer laser wavelengths will be added to this service in the near future. The dose measurements are performed using a beamsplitterbased calibration system in which a spatially uniform beam from an argon-fluoride excimer laser is generated using a special beam homogenizer. The beam propagation properties, including uniformity or homogeneity, are fully characterized with a state-of-the-art beam profile measurement system based on a pyroelectric camera array. This uniform beam then is used to irradiate a NIST-calibrated aperture placed immediately in front of the test detector.

• We determined the damage thresholds and lifetimes of several materials using 157 nm and 193 nm excimer lasers and a beam profile technique similar to ISO 11254-2. We made these measurements to select an appropriate absorbing material for use in our primary standard laser calorimeter for 157 nm excimer laser power measurements. The materials we tested were nickel-plated sapphire, chemically-vapordeposited silicon carbide (CVD SiC), nickelplated copper, and polished copper. Applied pulse energy densities (or dose) ranged from 80 to 840 mJ/cm². We determined the applied dose from a series of laser beam profile measurements. Silicon carbide had the highest damage threshold: 730 mJ/cm² per pulse. For this reason, and for its high thermal and electrical conductivities, we have chosen silicon carbide as the absorber material for the 157 nm calorimeter. ŀ



Damage threshold measurements. Beam profiles were recorded and characterized at 22 planes along the propagation axis using a CCD camera and quantum converter. Three energy density distributions at innerand outer-most positions, together with their dimensions, are shown. The dimensions are based on the calculation of the second moments according to ISO 11146.

Using a unique UV polarimetry system we developed, we made the first measurements of an intrinsic birefringence in CaF₂, BaF₂, and SrF₂. These values turned out to be over ten times the 157 nm lithography birefringence target value, and have forced all 157 nm system designs to be substantially redesigned. We developed the complete theory of the effect, now fully accepted, and analyzed its angular dependence. From this, we first suggested a compensation approach based on combining lenses of different crystal axis orientations. All 157 nm system designs now utilize this correction approach. We also showed that since the intrinsic birefringence of CaF₂ has the opposite sign to that of an BaF₂ and SrF₂, then mixed crystals, e.g., Ca_{1-x}Ba_xF₂ or $Ca_{1-x}Sr_xF_2$, can in principle be made which have zero intrinsic birefringence at 157 nm. We are working with crystal growers to explore this approach.



Measured (symbols) and calculated (curves) intrinsic birefringence of CaF₂ and BaF₂. The figure shows the opposite sign of the effect for the two materials and the $\approx 1/\lambda^2$ dependence. The value for CaF₂ at 157.63 nm is 11.2×10^{-7} .

The stability of semiconductor diodes under irradiation from an excimer laser operating at 157 nm has been evaluated. We have built a facility at SURF III that allows simultaneous exposure of photodiodes to excimer radiation and synchrotron radiation. Measurements of the spectral responsivity can be made in the spectral range from 130 nm to 320 nm with a standard uncertainty of less than 1 %. The intense, pulsed laser radiation was used to expose the photodiodes for varying amounts of accumulated irradiation whereas the low intensity, continuously-tunable cw radiation from the synchrotron source was used to characterize the photodiodes. The changes in the spectral responsivity of different kinds of diodes such as UV silicon, GaP, GaAsP, PtSi, diamond, and GaN were measured for a large range of total accumulated dose from an F₂ excimer laser operating at 157 nm. Differing amounts of changes were seen in different diodes depending on the total excimer irradiation dose and they showed different spectral changes in the responsivity as well. This yields important information about the mechanism responsible for the degradation of photodiodes.



Photodetector damage experiment for 157 nm radiation.

We have also characterized pyroelectric detectors which are commonly used for highpower laser application. In the vacuum UV to near UV range, pyroelectric detectors are commercially available because of important applications in areas like semiconductor photolithography. Instead of calibrating these detectors using high-power radiation, we performed measurements with low-power UV radiation at beamline 4 of the SURF III. To accommodate the pulse detection nature of the pyroelectric detectors, we installed a 10 Hertz tuning fork chopper at beamline 4 and lock-in amplifiers were used for detector signal processing. Several commercial pyroelectric detectors were tested at our facility. We found that in most cases, the manufacturersupplied amplifiers were too noisy for our light intensity on the order of one microwatt. Subsequently, a low-noise amplifier was constructed and installed near the detection head. In addition, for several high reflectance pyroelectric detectors, we also measured the reflectance of the pyroelectric element to check the internal quantum efficiency of the detector.

We have constructed and characterized a probe that is suitable for accurate measurements of irradiance in the vacuum ultraviolet spectral range. Many industrial applications such as UV curing, photolithography, or semiconductor chip fabrication require accurate measurement of the irradiance and will benefit from having such a stable, accurate UV probe. The probe was characterized at various wavelengths ranging from 157 nm to 325 nm, encompassing many of the important industrial application wavelengths. The principle of measurement of the irradiance is based on scanning the probe in a light field and measuring the spectral responsivity on a grid with regular spacing. Measurement of the spectral responsivity in the center of the probe along with

the integrated total responsivity yields the spectral irradiance. This method can alternatively be used to calculate aperture areas as well by measuring the ratio of the total responsivity and the responsivity in the center.



Measurement of the areal responsivitity of a UV probe at 157 nm.

Collaborations

International SEMATECH, Richard Harbison; optical characterization of 157 nm lens materials.

MIT Lincoln Laboratory, Mordechai Rothschild; DUV detector damage, immersion optical fluid measurements.

Recent Publications

M.L. Dowel, R.D. Jones, H. Laabs, C.L. Cromer, and R. Morton, "New developments in excimer laser metrology at 157 nm." Metrology, Inspection, and Process Control for Microlithography XVI, *in press*.

H. Laabs, R. Jones, C. Cromer, M. Dowell, V. Liberman, "Damage Testing of Partial Reflectors for 157 nm Laser Calorimeters," Annual Symposium on Optical Materials for High Powered Lasers, *in press*.

M. Dowell, "Pulsed-laser Metrology at NIST," Optics and Photonics News (February 2001) 28.

M. Dowell, "The Power of Light: Choosing the Right Detector is key to accurate beam power measurements," OE Magazine (January 2001) 56. M. L. Dowell, C. L. Cromer, R. D. Jones, D. A. Keenan, and T. R. Scott, "New Developments in Deep Ultraviolet Laser Metrology for Photolithography," Characterization and Metrology for ULS1 Technology: 2000, D. G. Seiler, A. C. Diebold, T. J. Shaffner, R. McDonald, W. M. Bullis, P. J. Smith, and E. M. Secula, Eds. (AIP, New York, 2001), pp. 391-394.

M. L. Dowell, C. L. Cromer, R. D. Jones, D. A. Keenan, and T. R. Scott, "New Developments in Deep Ultraviolet Laser Metrology for Photolithography," Society of Manufacturing Engineers Technical Note Paper MS00-236 (2000).

P-S. Shaw, T. C. Larason, R. Gupta, S. W. Brown, R. E. Vest, and K. R. Lykke, "The New DUV Spectral Responsivity Scale Based on Cryogenic Radiometry at SURF III," Review of Scientific Instruments, **72**, 2242 (2001).

J. H. Burnett, Z. H. Levine, E. L. Shirley, "Intrinsic birefringence in calcium fluoride and barium fluoride," Phys. Rev. B 64, 241102 (2001).

T.A. Germer, R. Gupta, L. Hanssen, and E. Shirley, "Optical Properties of Materials," Optics and Photonics News 12, 38, (2001).

P.-S. Shaw, R. Gupta, T.A. Germer, U. Arp, T. Lucatorto, and K.R. Lykke, "Characterization of materials using an ultraviolet radiometric beamline at SURF III," Metrologia **37**, 551 (2000).

J. H. Burnett, Z. H. Levine, and E. L. Shirley, "The trouble with calcium fluoride," OE Magazine (March 2002).

J. H. Burnett, R. Gupta, and U. Griesmann, "Absolute refractive indices and thermal coefficients of CaF₂, SrF₂, BaF₂, and LiF near 157 nm," Applied Optics **41**, 2508 (2002).

Metrology Supporting EUV Lithography

Goals

Provide leading-edge metrology for the development and characterization of optical components and detectors used in Extreme Ultraviolet Lithography (EUVL). (EUVL utilizes radiation at 13.4 nm.)

Customer Needs

As the features and design rules of the components used in semiconductor chips continue to shrink, we approach the limit at which the diffraction of the DUV presently used for state-ofthe-art lithography will prevent further reduction of the dimensions. Thus, within the next few years, the industry will need to identify a suitable "next generation lithography" (NGL) beyond the current DUV-based tools. The leading contender for the NGL is EUVL. In this country its development is being intensely pursued by the EUV-Limited Liability Corporation (EUV-LLC). An alpha-tool called the ETS (Engineering Test Stand) is now in operation at the EUV-LLC's Sandia National Laboratory Facility.

High resolution imaging with EUV radiation was not possible until the development of multilayer EUV mirrors in the mid 80s. This development has spawned the relatively new field of EUV optics and its associated set of new metrological challenges. Among these are: 1) precise EUV reflectivity maps; 2) EUV dosimetry; 3) EUV damage characterization; and 4) nanometer level optical figure measurement.

Technical Strategy

1. Precise EUV reflectivity maps.

The present NIST/DARPA EUV Reflectometry Facility is located on a multipurpose beamline on the NIST Synchrotron Ultraviolet Radiation Facility (SURF III) storage ring. The beamline can provide a monochromatic beam of EUV or soft x-ray radiation in the 3 nm to 40 nm (400 eV to 30 eV) spectral range. Although primarily designed to serve the EUVL community by providing accurate measurements of multilayer mirror reflectivities, this beamline with its associated sample chamber has been used for many other types of measurements since the beamline's commissioning in early 1993. Among the other measurements performed recently are grating efficiencies, photocathode conversion efficiencies, phosphor conversion efficiencies, film dosimetry, and determination of EUV optical constants though angle dependent reflectance measurements.

Presently the NIST/DARPA facility is the only one in the US large enough to measure optics larger than 200 mm in diameter. An example was a set of six C1 mirrors within their deposition fixture, which was measured this spring and compared to measurements at the Advanced Light Source at Berkeley (See figure 1.) We have also participated in a round-robin intercomparision with four other international standard laboratories, demonstrating an uncertainty in the measurement of absolute reflectivity of less than 0.2%.

DELIVERABLES: Full reflectivity map of EUV mirrors up to 40 cm in diameter and 45 kg mass on an as needed basis for the EUVL community.



Figure 1. C-1 Mirror from the ETS of the EUV-LLC. Only two of the six sectors are shown. The laser-plasma source is positioned on the central axis.

2. EUV Dosimetry

NIST is the primary national source for the radiometric calibration of detectors from the infrared to the soft x-ray regions of the spectrum. Until recently all NIST-characterized EUV photodetectors were calibrated on the SURF storage ring, which is essentially a cw source. In the last year we have designed and built a pulsed EUV source based on the source being used in the ETS to calibrate the EUV wafer-plane do-simeters to be used in EUVL. A schematic of the pulsed radiometric facility is shown in figure 2.

Technical Contact: Tom Lucatorto Charles Tarrio Ulf Griesmann

"NIST is uniquely capable of serving the EUVL community in critical areas. For example, NIST was the first metrology laboratory to anticipate the need to perform metrology on very large optics and now has the only reflectometer in the U.S. capable of measuring the large optics to be used in production EUV steppers and large astronomical telescopes."

Eberhard Spiller, inventor of the multilayer EUV mirror, Lawrence Livermore National Laboratory.



Figure 2. Schematic of Pulsed Radiometric Facility

Two major concerns arise when using solid state photodiodes for detection of short pulse length radiation. First, while the average power may be quite modest, the peak power can be quite high. For example, a 10 Hz laser with an average power of 10 mW has a peak power of 100 kW for a 10 ns pulse. Photodiode saturation may seriously affect the linearity of EUVL dosimeters, even at fairly low average power levels. We have measured the limit of the linear operating range for an EUV sensitive Si photodiode using (532 nm radiation as a proxy for 13.4 nm); the absorption characteristics in Si are nearly identical. We have found that Si photodiodes are linear detectors at incident pulse energies of 15 nJ or less in a 10 ns pulse. This corresponds to a peak power of about 1.5 W. A second concern in pulsed radiometry is the equivalence of the quantum efficiency (detected electrons per incident photon) under pulsed and cw conditions. All absolute calibration sources in the EUV are effectively cw sources, but EUVL sources are all pulsed. We have demonstrated that the quantum efficiency measured under cw conditions is the same as the quantum efficiency with 10 ns pulses incident to within an uncertainty of 10%. More accurate measurements are currently in progress.

DELIVERABLES: (1) Commission pulsed radiometric facility 2Q 2002 (2) Provide EUV-LLC with calibrated photodiodes 4Q 2002.

3. EUV Damage Characterization

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The energetic (91 eV) EUV photons impinging on the mirrors in the vacuum environment of the stepper induce various reactions that can damage the multilayer coatings. Some of the reactions can be attributed to EUV-excited water vapor and EUV-dissociated hydrocarbons. (Both a small amount of residual water and hydrocarbon vapors are present in the stepper environment.) In fact, lifetime tests show that the expected lifetime under present conditions is far short of the year duration needed for economic operation.

Several mitigation schemes have been proposed, including cap layers and gas assisted cleaning. To test the efficacy of these schemes, our group is constructing an exposure chamber on SURF III that will provide carefully measured long term exposures to test samples under various environmental conditions.

DELIVERABLES: (1) Commission exposure chamber on SURF III 1Q 2002(2) Provide service to EUVL community of carefully measured doses on test mirrors in controlled environments.

4. Nanometer Optical Figure Measurement

The approach to measurement of optical figure is to use phase measuring interferometry (PMI). Commercially available phase measuring interferometers can be extremely repeatable; an array of techniques, including some developed in this program, are now available for separation of part errors from the signature of the instrument - at least for some classes of surface. Such approaches have shown that they can provide measurement uncertainties of the order of 1 nm and near flats. For the measurement of aspheric optics (i.e., systematic deviations from a base sphere), such as those needed for NGL, there are some basic limitations to the potential of the commercially available PMIs. Concepts for a system combining a PMI with high precision slideways have been developed and implemented (in collaboration with an industrial vendor) in a new measurement capability, known as the NIST X-ray Optics Calibration InterferometeR (XCALIBIR). The goal is 0.25 nm rms uncertainty in measurement of aspheric optics up to 300 mm with focal lengths up to 2 m. XCALIBIR is designed to have the flexibility to measure flat, spherical, and aspheric optics. The interferometer was installed at NIST in the fourth quarter of FY99; a calibration service is being developed based on this capability.

A critical part of the uncertainty evaluation of an ultra-precision interferometric measurement is a ray-trace evaluation of the test. The uncertainty in the radius of curvature of spherical optics in the test limits the accuracy of the models. XCALIBIR is being used to provide state-of-theart radius of curvature measurements to address this problem. Lithography at EUV wavelengths also leads to challenging tolerances for the photomask. The mask is the optical element containing the desired wafer pattern; lithography is accomplished by projecting the image of the pattern onto the resist-coated wafer with a several-fold reduction in magnification. Current EUVL designs call for a mask blank flatness of 50 nm. Proposed substrate materials are transparent in the visible and have nearly opposing parallel faces, which makes surface flatness difficult with traditional phase measuring interferometry. A modern version of the Ritchey-Common test based on commercial phase measuring interferometry has been developed at NIST to measure the flatness of photomask blanks. XCALIBIR can be used in a mode with reduced coherence length to measure flatness of parallel windows. Fig. 3 shows the result of a measurement of a photomask.



Figure 3. Photomask blank flatness measured with the Ritchey-Common test

DELIVERABLES: Establish capability for EUV photomask blank flatness measurement on XCALIBIR (3Q 2002).

Collaborations

EUV-LLC at Sandia National Laboratory, Leonard Klebanoff, Environmental Team Leader.

EUV-LLC at Lawrence Livermore National Laboratory, Eberhard Spiller, Don Sweeney, Saša Bajt, and Regina Soufli, EUV mirror fabrication team.

Recent Publications

"Facility for Extreme Ultraviolet reflectometry of Lithographic Optics," C. Tarrio, S. Gratham, and T.B. Lucatorto, submitted to Metrologia.

"Towards High Accuracy Reflectometry for EUV Lithography," C. Tarrio, S. Gratham, M.B. Squires, and T.B. Lucatorto, submitted to Applied Optics.

"Extreme Ultraviolet Metrology at SURF III," C. Tarrio, R. E. Vest, S. Grantham, and T. B. Lucatorto, *Synchrotron Radiation News14*, pp. 21-31 (2001).

"Upgrades to the NIST/DARPA EUV Reflectometry Facility," C. Tarrio, T. B. Lucatorto, U. Arp, S. Grantham, and L. Deng, Proc. SPIE vol. 4506, *Soft X-ray and EUV imaging systems II* pp.32 -39 (2001).

"Absolute Extreme Ultraviolet Metrology," C. Tarrio, R. E. Vest, and S. Grantham, Proc. SPIE vol. 4450, *Harnessing light: Optical science and metrology at NIST*, pp 94-107 (June 2001).

"Advanced Optics Characterization," A. Davies, C. Tarrio, and C. J. Evans, *Optics and Photonics News*, February, 2001, pp. 34-37.

"Uncertainties in Interferometric Measurements of Radius of Curvature," Schmitz, T., Davies, A., and Evans, C., to appear in Proc. SPIE 4451 (2001)

"Interferometric Testing of Photomask Substrate Flatness," Evans C. J., Parks R. E, Shao L-Z., Schmitz T., and Davies A. Proc SPIE Vol 4344, in press.

"Interferometric ,etrology of Substrates for VLSI," Evans C. J., Davies A., Schmitz T., Parks R. E, and Shao L-Z., Proc of 2nd EUSPEN International Conference, Turin, May 2001, pp. 388-92.

Technical Contacts: E. K. Lin C. L. Soles W. L. Wu

"Sub-100 nm lithography poses significant challenges. In particular, the resist thickness is decreasing to 100 nm and below – this is a critical regime where interfaces cannot be ignored... [NIST researchers], as recognized experts in reflectivity techniques and in using these to probe thin films are uniquely positioned to apply these high resolution capabilities to help us probe fundamental questions that we need to answer."

Dr. Marie Angelopoulos, IBM T.J. Watson Research

Polymer Photoresist Fundamentals for Next-Generation Lithography

Goals

In this project, we are developing an integrated program involving fundamental studies of photoresist materials to be correlated with resist performance metrics that will have a broad industrial impact in next-generation photolithography. We work closely with industrial collaborators to develop and apply high spatial resolution and chemically specific measurements to understand varying material properties and process kinetics at nanometer scales and to provide high quality data needed in advanced modeling programs. The understanding developed in this program will provide a detailed foundation for the rational design of materials and processing strategies for the fabrication of sub-100 nm structures. The unique measurement methods we apply include x-ray and neutron reflectivity (XR, NR), small angle neutron scattering (SANS), incoherent neutron scattering (INS), near-edge x-ray absorption fine structure (NEXAFS), atomic force microscopy (AFM), and combinatorial methods. Our efforts focus on the fundamentals of polymeric materials and processes that control the resolution of the photolithography process including: (1) the physical properties of and polymer chain conformation within sub-100 nm structures, (2) the spatial segregation and distribution of photoresist components, (3) the transport and kinetics of photoresist components and the deprotection reaction interface over nanometer distances, (4) the material sources of line-edge roughness (LER), a measure of the ultimate resolution of the lithographic process, and (5) the polymer physics of the developer solution and the dissolution process. These data are needed to meet the future lithographic requirements of sub-100 nm imaging layers and critical dimensions.

Customer Needs

Photolithography remains the driving and enabling technology in the semiconductor industry to fabricate integrated circuits with ever decreasing feature sizes. Today, current fabrication facilities use chemically-amplified (CA) photoresists, complex and highly tuned formulations of a polymer film loaded with photoacid generators (PAGs) and other additives. Upon exposure of the photoresist film through a mask, the PAG releases acidic protons. A post-exposure bake is then applied and the acid protons diffuse and catalyze a deprotection reaction on the polymer that alters its solubility in an aqueous base developer solution. These reaction, diffusion, and development processes must be understood and controlled at the nanometer length scale to effectively fabricate integrated circuits.

There are significant challenges in extending this technology to fabricate the smaller feature sizes (sub-100 nm) needed to continue performance increases in integrated circuits. First, new radiation sources with shorter wavelengths (193 nm and 157 nm) require photoresist films nearing 100 nm thick to ensure optical transparency and uniform illumination. In these ultrathin films, two-dimensional confinement can induce deviations in several key materials parameters such as the macromolecular chain conformation, glass transition temperature, viscosity, or transport properties. Furthermore, the required resolution for a sub-100 nm feature will be on the order of 2 nm, approaching the macromolecular dimensions of the photoresist polymers. It is not yet clear how deviations due to confinement will affect the ultimate resolution in these ultra-thin photoresist films. Additionally, the material sources of feature resolution (line-edge and sidewall roughness) and profile control need to be identified and understood to ensure the success of needed patterning technologies.

Computer simulations of the lithographic process are widely used within the semiconductor industry to plan and optimize processing variables to produce integrated circuits. Complex processing steps provide a significant challenge to simulator developers to successfully predict photoresist behavior with smaller features and tighter error budgets. High-resolution data of material, transport, and reaction kinetics on nanometer length scales are needed to benchmark these numerical simulations for future processes. We are developing measurements with sufficient spatial resolution to aid in these efforts.

Technical Strategy

1. In this project, we use model photoresist materials to validate the new measurement methods. Model 248 nm photoresist materials are used to address several important fundamental questions including the thermal properties of ultrathin films as a function of film thickness and substrate type, the conformation of polymer chains confined in ultrathin films, the surface concentration of PAGs, the diffusion and the reaction kinetics of the deprotection reaction, and the physics of the development process. We also are exploring the application of combinatorial methods as a tool to rapidly determine important lithographic parameters and to identify material factors impacting feature resolution. These results provide a strong basis for understanding the material property changes that may affect the development of lithography for sub-100 nm structures using thin photoresist imaging layers.

DELIVERABLES: Measure the atomic leveldynamics of photoresist polymer thin films that impact processing variables such as postexposure bake temperature and time. 2Q 2002

DELIVERABLES: Measure the three-dimensional conformation of polymer chains confined in thin films. Determine length scale at which deviations from bulk conformation become important. Compare experimental results with detailed molecular dynamics simulations. 2Q 2002

DELIVERABLES: Measure the spatial profile of the deprotection reaction front with nanometer resolution. Determine dependence on postexposure bake temperature and time. 3Q 2002

DELIVERABLES: Measure the surface concentration of the PAG component in photoresist thin films. 3Q 2002

DELIVERABLES: Develop combinatorial methods to quantify rapidly material factors that affect resolution control. 4Q 2002

Accomplishments

Incoherent neutron scattering was used to measure the atomic-level dynamics of model photoresist polymer thin films for the first time. The local, atomic-level, dynamics of the photoresist polymer directly affect transport processes essential to modern photoresists, such as the diffusion of photogenerated acids and other small molecules within the polymer matrix. To date, changes in the local dynamics of polymer thin films have been inferred from changes in macroscopic quantities such as the apparent glass transition temperature, Tg, as a function of film thickness and substrate interaction energies. Direct measurements of the segmental motions of polymer chains confined to ultrathin films provide a molecular picture of observed changes in these macroscopic quantities and insight into differences in photoresist transport processes in ultrathin films. By utilizing different polymers and polymer/substrate combinations, we obtain

crucial insight into the dynamical effects of polymer thin film confinement.

The three-dimensional structure of polymers confined to ultrathin films was measured for the first time using small angle neutron scattering (SANS). In ultrathin photoresist films and sub-100 nm structures, polymer chain conformations may affect key material parameters germane to photoresist processing, such as film quality, thermal stability, line-edge roughness, and both dissolution and etch rates. We performed SANS measurements on polystyrene films that are confined on silicon wafers with the thickness as thin as 110 Å, less than 70 % of the radius of gyration, Rg, of the constituent polymer. The conformation perpendicular to the surface is probed by rotating the incident neutron beam to an angle of 35 ° with respect to the silicon wafers, thereby tilting the scattering vector out of the plane of the film. The results confirm that within the plane of the film the Rg is Gaussian and bulk-like, while perpendicular to the film the Rg is significantly reduced. The chain conformation normal to the surface is measurably distorted even at thickness greater than the bulk diameter (2Rg). Molecular dynamics simulations were performed to provide detailed insight into the conformation of confined polymer chains and to compare with the scattering data.

The deprotection reaction front profile was measured with nanometer resolution using both x-ray and neutron reflectometry on a bilayer structure prepared with a specially labeled (deuterated) protected polymer. The upper layer of the structure is loaded with the PAG. Upon exposure and baking, the acid diffuses into the lower layer and catalyzes the deprotection reaction. The protecting group is deuterated and is volatile upon reaction. Thus, contrast to neutrons results from the reaction allowing for observation of the reaction front. By comparing the reaction front to the developed film profile, we obtain important insight into both the spatial extent of the reaction and the development process itself. These data are the first available with this spatial resolution and are critically needed for the development of process control over nanometer length scales. We find that the reaction front broadens with time while the surface roughness of the developed structure remains relatively sharp. Additionally, we find that a broader reaction front results in changes in the compositional profile upon development in an aqueous base.

NEXAFS measurements were used to measure the surface concentration of PAG components and the surface reaction kinetics in model photoresist polymers as a function of common processing conditions. A significant advantage of the NEXAFS measurement is the capability of separating interfacial and bulk signals within the same sample and experiment. NEXAFS measurements of interfacial chemistry are possible because of the limited escape depth of produced secondary electrons. By separately observing the electron and fluorescence yield, the chemistry at the surface (2 nm) and bulk (200 nm) may be determined. Different chemistries may be observed by examining the near-edge x-ray spectra of light elements such as carbon, oxygen, fluorine, and nitrogen. In this way, changes in the surface chemistry relative to the bulk film can be investigated as a function of lithographic processing steps such as exposure and heating. We have found that fluorinated PAG molecules preferentially segregate to the film surface. The relative amount of segregation is dependent upon the specific polymer.

Combinatorial methods have been applied to determine rapidly the deprotection temperature of blends of the protected and deprotected model polymers and to quantify the activation energy of the deprotection reaction. Samples were prepared on gradients in temperature and postexposure bake time. Using a modified highthroughput combinatorial analysis technique, the relationship between composition and deprotection temperature of a model photoresist blend The temperature gradient was established. method provides a quick, reproducible, and surprisingly accurate method of deprotection determination over a wide range of compositions. FTIR and x-ray reflectivity measurements were used to establish the correlation between deprotection and the observed color change evident in the combinatorial experiment.

Collaborations

Polymers Division, NIST – Ronald L. Jones, Joseph L. Lenhart, Vivek M. Prabhu, Francis W. Starr, Patricia M. McGuiggan, David Vanderhart.

IBM T. J. Watson Research Center – Dario L. Goldfarb, Qinghuang Lin, Marie Angelopoulos.

DARPA – Advanced Lithography Program, Contract N66001-00-C-8803.

Ceramics Division, NIST – Danieł A. Fischer, Sharadha Sambasivan

Brewer Science, Inc. – Douglas Guererro, Yubao Wang, Rama Puligadda

University of Texas at Austin – Brian C. Trinque, Sean D. Burns, C. Grant Willson

Center for Neutron Research, NIST - Charles J. Glinka, Sushil K. Satija

Recent Publications

Lin, E. K., Soles, C. L., Goldfarb, D. L., Trinque, B. C., Burns, S. D., Jones, R. L., Lenhart, J. L., Angelopoulos, M., Wilson, C.G., Satija, S. K., and Wu, W. L., "Measurement of the Spatial Evolution of the Deprotection Reaction Front With Nanometer Resolution Using Neutron Reflectometry," Proc. SPIE, 4690, (2002).

Jones, R. L., Starr, F. W., Soles, C. L., Lin, E. K., Lenhart, J. L., Wu, W. L., Goldfarb, D. L., Angelopoulos, M., "Chain Conformation in Ultrathin Polymer Resists," Proc. SPIE, 4689, (2002).

Lenhart, J. L., Jones, R. L., Lin, E. K., Soles, C. L., Wu,W. L, Goldfarb, D. L., and Angelopoulos, M., "A Combinatorial Methodology to Discovering the Material Factors Controlling Resist Line Edge Roughness, Shape, and Critical Dimension," J. Vac. Sci. Tech. B, in print (2002).

Soles, C. L., Lin, E. K., Lenhart, J. L., Jones, R. L., Wu, W. L., Goldfarb, D. L., and Angelopoulos, M., "Thin Film Confinement Effects on the Thermal Properties of Model Photoresist Polymers," J. Vac. Sci. Tech. B., **19**, 2690 (2001).

Goldfarb, D. G., Angelopoulos, M., Lin, E. K., Jones, R. L., Soles, C. L., Lenhart, J. L., and Wu, W.L., "Confinement Effects on the Spatial Extent of the Reaction Front in Ultrathin Chemically Amplified Photoresists," J. Vac. Sci. Tech. B., **19**, 2699 (2001).

Goldfarb, D. L., Lin, Q. H., Angelopoulos, M., Soles, C. L., Lin, E.K., and Wu, W. L., "Characterization of Thin and Ultrathin Polymer and Resist Films," Proc. SPIE, 4345, 335 (2001).

Critical Dimension and Overlay Metrology Program

The principal productivity driver for the semiconductor manufacturing industry has been the ability to shrink linear dimensions. A key element of lithography is the ability to create reproducible undistorted images, both for masks and the images projected by these masks onto semiconductor structures. Lithography as a whole, fabricating the masks, printing and developing the images, and measuring the results, currently constitutes ≈ 35 % of wafer processing costs. The overall task of the Critical Dimension and Overlay Program is to assist the industry in providing the necessary metrology support for current and future generations of lithography technology. These goals include advances in modeling, the provision of next generation critical dimension and overlay artifacts, and comparisons of different critical dimension and overlay measurement techniques.

Currently, resolution improvements have outpaced overlay and critical dimension measurement improvements. To maintain cost effectiveness significant advances must be made.

Technical Contact: R. Silver "There are many people who do use the NIST (photomask) linewidth standard and will continue to do so and expect NIST to continue to provide leadership in this area. That is one of the main reasons that we are always pleased to see a metrology paper submitted by NIST to the Photomask symposium each year."

Grenon Consulting and Chairman of BACCUS

Brian Grenon

Atom-Based Dimensional Metrology

Goals

Provide technological leadership to semiconductor and equipment manufacturers and other government agencies by developing the methods, tools, and artifacts needed to apply leading edge, high-resolution atom-based dimensional measurement methods to meet the metrology needs of semiconductor microlithography. One specific goal is to provide the customer with the techniques and standards needed to make traceable dimensional measurements on wafers with nanometer accuracy. We are developing threedimensional structures of controlled geometry whose dimensions can be measured and traced directly to the intrinsic crystal lattice. These samples are intended to be dimensionally stable to allow transfer to other measurement tools which can measure the artifacts with dimensions known on the nanometer scale.



Figure 1. The atomic resolution image above was measured with a 20 picometer resolution interferometer system mounted on the UHV STM.

Customer Needs

NIST responds to U.S. industry needs for developing length intensive measurement capabilities and calibration standards in the nanometer scale regime. The new class of scanned probes have unparalleled resolution and offer the most promise for meeting these future needs of the microelectronics industry. One important application of the high-resolution SPM methods is in the development of linewidth standards whose dimensions can be measured and traced through the crystal lattice from which they are made. In addition, these high-resolution tools can be coupled directly to a new NIST-designed picometer resolution interferometer.



Figure 2. This recent result utilizes the atomically flat surfaces as a substrate for nanomanufacturing. The features CDs are 10 nm and the entire lateral field of view is 250 nm.

The work funded in this project is for the development of atom-based linewidth standards to assist in the calibration of linewidth metrology tools and the development of unique interferometry capabilities which can be used in conjunction with accurately measured tips to measure feature critical dimensions. This effort is intended to enable the accurate counting of atom spacings across a feature in a controlled environment and to subsequently transfer that artifact to other measuring instruments as a structure with atomically known dimensions. As critical dimensions continue to shrink, the detailed atomic structure, such as edge roughness or sidewall undercut, of the features to be measured represents a larger portion of the measurement uncertainty. Furthermore, particularly with SEMs, the instrument response and the uncertainty in the edge location within an intensity pattern becomes significant issue due to the increased sensitivity to detailed elements of the edge detection model. The complexity of these models and large computer resources required for each individual computation make the idea of having samples of known geometry and width essential. This project is intended to develop samples of known geometry and atomic surface structure which will yield measurements resulting in a specific number of atoms across the line feature or between features. These samples will be measured in the UHV

environment and then stabilized and subsequently transferred to other instruments.

There are three primary applications of this type of artifact after it has been atomically counted. The first method is the direct calibration in an SEM for a product wafer whose geometry and material is near to the structure of the atomically counted sample. The second method utilizes an AFM to calibrate the SEMs with the AFM acting as an SEM matching tool. In this method, the AFM is calibrated with an atomically measured sample of the same geometry as the product wafer to be measured by the SEMs. This sample only needs to have similar geometry to the product wafer but does require similarity in materials due to the insensitivity of an AFM to materials variations. An AFM that has been calibrated for a particular geometry by an atomic artifact can then transfer that calibration to a product wafer of similar geometry and any material such as photoresist, resulting in a calibrated product wafer which can then be transferred to calibrate an SEM.

The third method uses the number of atoms between features to determine the feature spacing. This method can be used to make magnification and pitch calibration standards based on the intrinsic crystal lattice.

These methods of atom counting and highresolution interferometry, as outlined in this project description, are non-destructive and are intended to yield samples which can be measured by various instruments such as an SEM and subsequently re-measured atomically. This is a unique and important element of this work since there are no other known methods that allow this kind of atomic dimensional measurement without being destructive. In addition, this new method opens up the possibilities of basing the measurement metric on the intrinsic crystal lattice.

Technical Strategy

The technical work is focused into four thrust areas.

1. The development of methods to prepare photolithographically patterned three-dimensional structures in semiconductor materials. These structures must be prepared in such materials as to allow the atomic surface reconstruction of those features such that the atomic order is commensurate with the underlying crystal lattice. This involves either using conventional photolithography methods for sample production or using the STM itself to fabricate very small nanometer scale features as shown in figure 2.

DELIVERABLES: Write features in silicon with critical dimensions as small as 10 nm. Improve the fabrication robustness to enable the regular processing of features this size. 2Q 2002.

DELIVERABLES: Work with SEMATECH for the development of improved methods for preparation of photolithographically patterned three-dimensional double-etched structures in silicon. These structures must be prepared in such materials as to allow the measurements of those features in silicon. 4Q 2002.

2. The development of techniques for the preparation of SPM tips with reproducible geometries and the direct characterization of the SPM tip geometry and dimensions on the atomic scale. These well characterized tip probes can then be used to measure the samples with photolithographically defined and canonically ordered surfaces on the sub-nanometer length scale. We are developing the SPM tip etching, field evaporation, and cleaning procedures which reliably yield stable W tips and produce atomic resolution on Si (7x7) surfaces. These tips are also useful in a collaboration with the SEM project for development as nanotips as SEM field emitters. Our tip preparation methods leave us uniquely qualified in this arena.

DELIVERABLES: Prepare nanotips for use in SEM metrology. Work with the SEM metrology project for the testing of nanotips as SEM field emitters. 1Q 2002.

3. Focus on the development of artifacts that can be atom counted and then measured in a number of different metrology tools such as SEM and AFM. The integrity of the line geometry, such as side wall angle, is crucial to having useful artifacts for linewidth specimens. These edge geometry requirements are not as stringent for the magnification standards since feature symmetry is the most crucial element in these measurements. The work on linewidth artifacts, therefore, is focused on reducing the process temperatures required for atomic reconstructions. We have made wet chemical processing fully operational and are currently working on preparing atomically ordered Si surfaces at significantly reduced temperatures. For sample preparation, we are utilizing the existing in-situ processing apparatus and techniques from the UHV STM and concentrating on the reproducible production of atomically ordered Si surfaces and Si (111) step and terrace structures.

DELIVERABLES: We will design and procure a new set of wafers specifically for atom-based dimensional metrology. This new wafer set will be written by ebeam on silicon (111) wafers. 3Q 2002.



Figure 3. These are atomically flat, chemically prepared surfaces for use in atom-counting and nanomanufacturing.

4. The development of a new interferometer system intended to measure dimensions in the 20 picometer range with high accuracy. The system should also be capable of use on the STM so atomic scale measurements can be made with new levels of accuracy. In addition we are exploring new applications of FIM calibrated tips in conjunction with the interferometry to measure CDs of leading edge, small semiconductor features.

The long term technical objective is the development of *insitu* stabilized, atomically ordered surfaces which can be transferred to other measurement instruments such as scanning electron microscopes, AFMs, or optical metrology tools. These nanometer scale standard artifacts with atomically ordered surfaces will then act as linewidth or magnification calibration samples. These samples will have been measured either by direct atom counting or high-resolution interferometry and atomically measured tips.

Accomplishments

• We have obtained atomically flat surfaces and are now trying to obtain atomic order, routinely to obtain atomic order using the low temperature wet chemical based methods. Although we had a similar effort with GaAs, which was successful, we are currently focused on silicon substrates.

• The ability to prepare atomically sharp tips in W (111) has been demonstrated. The details of this methodology and the new models we have developed for analyzing sharpness have been prepared as a journal article.

• We have prepared two publications which give new insight into the etching process for fabricating atomically flat silicon surfaces. The results, seen in figure 3, yield a new, more comprehensive understanding of the physical processes involved in making atomically flat surfaces in silicon as required for much of the work in this project.

• The first UHV transfer was been demonstrated between the NIST MBE system and the PED UHV STM. The sample was maintained in a UHV environment during the entire event. Further UHV sample manipulation and preparation for transfer to other systems and long term storage will be investigated in the future as required.

We have developed techniques for the preparation of SPM tips with reproducible geometries and the direct characterization of the SPM tip geometry and dimensions on the atomic scale. We are now applying these ideas to FIM tips used in SEM metrology.





• We have attempted our first direct measure of the surface atom spacings based on a traceable interferometer measurement. We have fitted our UHV STM with a high accuracy subangstrom resolution interferometer. We have closed the loop and made our first atomic resolution measurements with full interferometer length basis. The successful completion of this aspect has enabled direct distance determination with simple atomic counting.

DELIVERABLES: Develop methods for the first demonstration of direct interferometer measurements of surface atom spacings with a complete unbroken uncertainty. Complete this link to develop an unbroken traceability chain to the international unit of length. 3Q 2002.

Wafers from the NIST designed metrology reticle set have been evaluated for use in atombased dimensional metrology. The initial evaluation is very promising and all four wafer flows yielded good product wafers. These wafers contain the prototype test structures, including a comprehensive set of critical dimension and line space arrays for general metrology purposes. The double-etched silicon multi-level features are intended to provide long term stable artifacts for calibration with the line arrays being test patterns for atom-based dimensional metrology work.

• We have produced atomically ordered surfaces of GaAs at far reduced temperatures and have worked with patterned GaAs linewidth samples. The GaAs linewidth features have been fabricated and we have successfully prepared As capped samples without damaging the line geometry or integrity in any measurable way. These samples have been processed using the complete atomic surface preparation method, measured in UHV and then allowed to oxidize to create a stable surface for measurement in other tools.

Collaborations:

ISMT, IBM, University of Maryland, Dept. of Physics, University of Purdue, Dept. of Physics.

Recent Publications

P.V.M. Rao, C. Jensen, and R. M. Silver, "A Generic Shape Model for STM Tip Geometry," submitted to Ultramicroscopy, (2001).

R. M. Silver, S. Gonda, C. Jensen, and L. Howard, "A New Tunable Diode Laser Method for a sub-nanometer Resolution Interferometry," to be submitted to Applied Optics, 2001.

J. Fu, H. Zhou, S. Gonda, and R. M. Silver "Wet Chemistry of Si Samples," to be submitted to Applied Physics Letters, in preparation

S. Gonda, H. Zhou, J. Fu and R. M. Silver "A new design and uncertainty consideration of a metrology UHV-STM for direct measurements of atom spacings," SPIE Nanotechnology workshop proceedings, NIST 2001.

H. Zhou, J. Fu, S. Gonda and R. M. Silver, "Processing atomically flat Si surfaces," SPIE Nanotechnology workshop proceedings, NIST 2001. Technical Contacts: A. E. Vladar M.T. Postek

"Scanning Electron Microscopy (SEM) – continues to provide at-line and inline imaging ... and CD measurements. Improvements are needed ... at or beyond the 90 nm generation... Determination of the real 3D shape...will require continuing advances in existing microscopy..."

International Technology Roadmap for Semiconductors, 2001

Scanning Electron Microscope-Based Dimensional Metrology

Goals

To provide the microelectronics industry with highly accurate SEM measurement and modeling methods for shape-sensitive measurements and relevant calibration standards with nanometerlevel resolution. Carry out SEM metrology instrumentation development, including improvements in electron gun, detection, sample stage and vacuum system. Conduct research and development of new metrology techniques using digital imaging and networked measurement tools solutions to key metrology issues confronting the semiconductor lithography industry.

Customer Needs

The scanning electron microscope is used extensively in many types of industry, including the more than \$200 billion semiconductor industry in the manufacture and quality control of semiconductor devices. The International Technology Roadmap for Semiconductors targets SEMs as the metrology tool of choice for use in semiconductor production through at least the year 2005. The industry needs SEM standard artifacts, specifically those related to instrument magnification calibration, performance and the measurement of linewidth. This entails a multidimensional program including: artifact fabrication, understanding the function and signal generation in the SEM, electron beam interaction modeling, developing NIST metrology instruments for the certification of standards, and developing the necessary artifacts and calibration procedures. The manufacturing of present-day integrated circuits requires that certain measurements be made of structures with dimensions of 100 nm or less with a high degree of precision. The accuracy of these measurements is also important, but more so in the development and pilot lines. The measurements of minimum feature sizes known as critical dimensions (CD) are made to ensure proper device operation. The U.S. industry needs high-precision, accurate, shape-sensitive dimension measurement methods and relevant calibration standards. The SEM Metrology Project supports all aspects of this need since scanning electron microscopy is the major microscopic technique used for this sub-micrometer metrology.

Technical Strategy

The Scanning Electron Microscope Metrology Project a multidimensional project. It is being executed through several thrusts fully supported by the semiconductor industry.

1. SEM Magnification Calibration Artifacts: Primary to SEM dimensional metrology is the calibration of the magnification of the instrument. Standard Reference Material (SRM) 2090 is an SEM magnification standard that will function at the low beam voltages used in the semiconductor industry and high beam voltages used in other forms of microscopy. A prototype with 200 nm lines and spaces was fabricated by the Nanofabrication Facility at Cornell University as a proof of concept and was used in a round robin study that clearly demonstrated the need for this standard. Texas Instruments was contracted to supply the first production run of the artifact with 100 nm lines and spaces and delivered over 180 of these artifacts. In order to speed the availability of this artifact to the industry (while the final certification details are being completed) the artifact has been released to the industry as Reference Material (RM) 8090.

DELIVERABLES: Completion of the renewal of the AMRAY metrology SEM-based sample calibration measuring system. Preparation of an assessment of the error budget for the fully functional metrology system. Preparation of customized recipes for various versions of magnification calibration samples. Upon availability of suitable quality samples, quality assessment and delivery of a new batch of RM 8090. Upon availability of suitable quality samples, completion calibration and delivery of a batch of SRM 2090 samples.

2. SEM Performance Measurement Artifact: This effort includes the development of the Reference Material 8091 and evaluation procedures suitable for correctly measuring image sharpness of scanning electron microscopes, especially of those that are used in the semiconductor industry. The performance characteristics of the SEM are particularly important to precise and accurate measurements on the semiconductor processing line. NIST has demonstrated that a critical dimension scanning electron microscope functioning poorly can be 5 nm or more larger than the same instrument functioning optimally. For reliable image sharpness measurements a suitable sample with small features is needed.

3. SEM Linewidth Measurement Artifacts: Artifacts that are characterized and calibrated to the required small levels of uncertainty were and are in the focal point of the IC industry's dimensional metrology needs. Therefore, at NIST, it has been a long-term goal to develop and deliver appropriate samples. For a long time the possibilities were limited by the lack of various technologies available, especially the lack of accurate modeling methods. NIST, through several years of systematic efforts, developed Monte Carlo simulation-based modeling methods that can deliver excellent results. These new methods can deduce the shape of integrated circuit structures from top-down view images through modeling and library-based measurement techniques with few nm accuracy. NIST in several publications demonstrated the possibilities and described power of this measuring approach. Based on the newest results, now it is becoming possible to start to develop the long-awaited relevant linewidth standard for the semiconductor industry. Reference Material 8120 line width samples will be a relevant sample on a 200 mm and 300 mm Si wafer with polySi features with sizes from 1 mm to down to 70 nm. Standard Reference Material 2120 is going to be the calibrated, traceable version for linewidth measurements. This work is being carried out in cooperation with ISMT.

DELIVERABLES: Preparation of an assessment of feasibility of the use of mixed, NIST and external measuring systems for certification of wafer format line width samples. Accomplishment of preliminary measurements on samples made with ISMT current and new "AMAG4L" metrology masks sets. 4Q 2002

Accomplishments

SEM Magnification Calibration Artifacts - Samples for Reference Material 8090 and the certified traceable version, the Standard Reference Material 2090 are being made at two places. We have a new mask designed at International SEMATECH to get samples made by 193 nm UV light lithography. The use of this conventional lithography and a somewhat modified design provides a chance for large amount of good quality samples produced inexpensively. Because of this technology, it is now possible to produce the finest lines with 100 nm width and with 200 nm pitch values. The largest pitch is 1500 µm. There are a large number of 250 nm wide crosses for distortion and other measurements. Also scatterometry patterns with varying

pitches will be available. The features on the conductive Si wafer will be formed from polySi material. These samples will give suitable contrast in any SEM to allow the user to set the magnification of the instrument from the smallest to the highest magnifications.



The new design of the SRM 2090 Magnification calibration Standard Reference Material.

The other contract with the Naval Research Laboratory (NRL) is currently moving faster and already yielded close to acceptable samples. NRL makes samples with a slightly modified original process using e-beam lithography and lift-off technique with a metal stack, which gives good contrast at low and high accelerating voltage. We have a good chance to obtain a larger amount of good samples, and start the evaluation process soon. This version of the samples has the original finest structure with 100 nm wide lines at 200 nm pitch. In the meantime, the renewal of the AMRAY Metrology SEM has been successfully accomplished. A new high-precision stage with sub-nanometer stepping distance is now fully operational. The development of LabView-based new control software has also been completed and the software has been thoroughly tested. This new measuring system offers the same functions in a PC Windows environment as the old expensive and outdated hardware under HP Basic but it also offers greater flexibility for adding new measurements (for example the SRM 484 can be measured with it) and it is up-to-date in every regard.

• SEM Performance Measurements – After comprehensive studies and experiments a plasma-etching Si called "grass" was chosen for

1:5

Reference Material 8091. This sample has 5 nm to 25 nm size structures as illustrated in the figure below. 15 pieces of RM 8091 were delivered to International SEMATECH (ISMT) for the member companies, and 75 additional samples have been delivered to the Office of Standard Reference Materials, NIST. A sharpness standard and evaluation procedure have been developed to monitor (or compare) SEM image quality. A NIST kurtosis method, Spectel Company's userfriendly analysis system called SEM Monitor, and University of Tennessee's SMART algorithm can be used with RM 8091. An effort is underway to produce more of these samples. These samples are now available to the public.



The RM 9081 Sharpness Reference Material.

SEM Linewidth Measurement Artifacts -The development of accurate modeling methods are in progress and have shown excellent results on polySi samples. From a top-down view, using our high-accuracy modeling and fitting methods a cross section of the lines can be determined with few nm uncertainties and discrepancies. The match is so good that this method may be capable of eliminating the costly and destructive cross sectional SEM measurements. The candidate sample for linewidth artifact must be relevant to state-of-the-art IC technologies, should have chips on 200 mm and later 300 mm wafers with all process variation, including a meaningful focus-exposure matrix (FEM). The design and the fabrication of ISMT/NIST mask have been successfully completed. The first 9 good quality wafers arrived at NIST just before the end of June. These wafers are currently at Accent for scatterometry measurements. After CD-SEM measurements at ISMT, cross sectional measurements will be made at NIST. All these measurements will yield an excellent database for a decision on how to proceed with this wafer type linewidth reference sample. It is conceivable that by the end of the year 2001 the Reference Material 8120 line width samples will be available. This work is being carried out in close cooperation with ISMT.

Development of Ultra-High Resolution Nano-tip Electron Gun for CD-SEMs - The source diameter and the brightness of the electron beam are two of the major factors limiting the performance of CD-SEMs in the semiconductor production environment. Thus, alternative solutions to improve performance are being sought as the metrology for sub-100 nm lithography is being pushed to its limit. One possible alternative approach is the application of nano-tips as an electron source replacement. Nano-tips, by comparison to both conventional cold field and to Schottky field emitters, offer a substantial increase in brightness (10 x to 100 x) and a large reduction (5 x to 10 x) in source size. Therefore, in an optimized electron optical column, substitution of a CFE or Schottky source by a nano-tip could be expected to produce:

- Higher beam currents into a spot of given size.
- Better signal-to-noise ratio and resolution.
- Faster scan rate and better charge control.

This work has progressed through:

- New tip preparation and evaluation procedures;

- Preparation of the Hitachi S-6000 CD-SEM. It has been prepared for the installation of the nanotips. This was facilitated through the help of Hitachi Scientific Instruments. The SEM currently works to the original specifications. One sharp tip was successfully tried with good results.

- Fabrication of a nano-tip assembly, which matches in geometry the S-6000 CD-SEM field emitter tip.

While the nano-tip fabrication technology (i.e. sharpening process) is working reliably, the main issue is to properly mount the prepared tip on the hairpin shaped tungsten tip holder. Several approaches were tried and for now, it is more feasible to use the hairpin part of used cathodes. As a back-up solution sharpening of existing tips as also explored. Two new tips were delivered from NIST to Dr. David Joy's research facility (Science and Engineering Research Facility University of Tennessee, Knoxville, TN).

There have been problems with control of the etching process, so our collaborators at University of Tennessee could not make a tip to try in the CD-SEM. In the meantime, a parallel effort at NIST has started in order to diversify the source of extreme sharp tips.

Design and implementation of the SEM Sentinel Measuring System – These tasks were successfully completed. The PC-based computerized measuring system monitors the vital signs of the CD-SEM through a LabView-based set of software.



Schematic of the SEM Sentinel system (left) Resolution improvement with sharp tip (right).

Collaborations

International SEMATECH, Metrology Council.

Naval Research Laboratory; E-beam Lithography.

International Technology Roadmap for Semiconductors; Microscopy and Metrology Sections.

Recent Publications

Damazo, B. N., Jayewardene, E. C., Keery, W. J., Vladár A. E. and Postek, M. T., "Design and Development of a Measurement and Control System for Measuring SEM Magnification Calibration Samples," Proceedings of SPIE 4344, 2002, Santa Clara (In press)

Marinenko, R. B., Steel, E. and Postek, M. T., Microscopy and Microanalysis Standards.

Vladar, A. E., Postek, M. T. and Vane R., "Active Monitoring and Control of Electron Beam–Induced Contamination," Proceedings of SPIE 3444; 2001 Santa Clara; pp. 835-843

Postek, M. T., Vladar, A. E., Larrabee, R. D. and Jones, S. N., "Report of Investigation. Reference Material 8091," SEM Sharpness Standard. OSRM Publication

Damazo, B. N., Vladar, A. E., Ling, A. V., Donmez, M. A., Postek, M. T. and Jayewardene, E. C., "SEM Sentinel-SEM Performance Measurement System," Proceedings of SPIE 3444; 2001 Santa Clara; pp. 773-782

Villarrubia, J. S., Vladar, A. E., Lowney, J. R. and Postek, M. T., "Edge Determination for Polysilicon Lines on Gate Oxide," Proceedings of SPIE 3444; 2001 Santa Clara; pp. 147-156, 2001.

Postek, M. T., Vladar, A. E., Wells, O. C. and Lowney, J. L., "Application of the Low-Loss Scanning Electron Microscope (SEM) Image to Integrated Circuit Technology. Part 1. Applications to Accurate Dimension Measurements," SCANNING; pp. 289-304, 2001.

Wells, O. C, McGlashan–Powell, M., Vladar A. E. Postek, M. T., "Application of the Low–Loss Electron Image to Quality Control During the Manufacture of Integrated Microcircuits. Part 2. Chemically–Mechanically Planarized Samples," SCANNING. 2001.

Vladar, A. E. and Postek, M. T., "Application of Nano-Tips to Production CD-SEMs," NIST/SEMATECH Collaboration LITG 4101 Project – SEMATECH Final Report; pp. 1-17, 2001.

Postek, M. T. and Vladar, A. E., "Critical Dimension Metrology in the Scanning Electron Microscope," Chapter. Handbook of Silicon Semiconductor Metrology (Dr. Alain C. Diebold, Ed. Dekker) ISBN 0-8247-0506-8, 2001. Technical Contact: R. Silver J. Potzick T. Doiron

"The NIST Overlay Metrology project is researching important and relevant measurement techniques in optics and optical modeling. We support their effort and believe they are making useful contributions in overlay methods and standards development." Mark Davidson Spectel Co.

Goals

Provide technological leadership to semiconductor and equipment manufacturers and other government agencies by developing and evaluating the methods, tools, and artifacts needed to apply optical techniques to the metrology needs of semiconductor microlithography. One specific goal is to provide the customer with the techniques and standards needed to make traceable dimensional measurements on photomasks and wafers, where appropriate, at the customer's facility. The industry focus areas of this project are primarily the optical based methods used in overlay metrology, photomask critical dimensional placement metrology.



One of the new advanced target designs from the NIST/ISMT collaboration.

Customer Needs

Tighter tolerances on CD measurements in photomask and wafer production place increasing demands on photomask linewidth accuracy and on overlay tolerances. NIST has a comprehensive program to both support and advance the optical techniques needed to make these overlay and photomask critical dimension measurements.

In addition, improved two-dimensional measurement techniques and standards are needed for measuring and controlling overlay capabilities of steppers and mask-making tools under development. Overlay is listed in Table 96 of the 2001 SIA ITRS as a difficult challenge for both >65 nm and <65 nm processes. Overlay improvements have not kept pace with resolution improvements and will be inadequate for ground rules less than 67 nm. In fact, Table 98b shows that no known solutions for overlay output metrology exist beyond the 67 nm node. As shown in Table 99a, the problems are more acute for CD mask metrology where the industry is currently encountering metrology problems without known manufacturing solutions.

Technical Strategy

There are three main strategic technical components of this project.

1. The NIST's overlay metrology tool, continuous development of the tool, measurement methods to obtain uncertainties comparable to better than the best industry overlay tools, and standards to support and calibrate these tools. The technical strategy for overlay metrology is divided into two segments: a) instrumentation development and overlay metrology methodology and b) design and calibration of standard artifacts. Pattern placement and overlay of the various lithographic levels is monitored with a series of targets, each in a different plane. The overlay offset is then obtained by optical measurements with a determination of the relative target centerlines. Any misalignment in the overlay metrology system will translate into an artificial overlay offset, referred to as tool induced shift (TIS). Additionally, there are residual errors caused by asymmetries in the target edges or covering layers (resist) known as wafer induced shift (WIS). A set of standard artifacts and procedures, under development at NIST, is designed to assist in aligning overlay measurement systems and eliminating TIS. After alignment, the tool must then be calibrated with standard artifacts to yield accurate overlay offsets. The measurement system used in this component is an optical reflection mode instrument, operational in either a bright field or confocal mode, with interferometry on three orthogonal axes also capable of monitoring the stage tilt. Additional hardware capabilities include the options to scan the sample while acquiring data with an on-axis photometer or high resolution image capture with a full field CCD data acquisition system. This latter mode has enabled a detailed study of CCD array performance and characterization. In this work, several CCD acquisition systems are being evaluated and improved edge detection and CCD array calibration procedures are being developed These same methods for two-dimensional CCD array analysis are now being applied to optics

analysis. Additional investigation of CCD measurement problems are focused on the detailed response of typical CCD camera light sensors.

WIS-free standard overlay artifacts have been fabricated in 200 mm wafers. These overlay artifacts are for the calibration of industrial optical overlay tools. The artifacts are being fabricated in single crystal silicon and will provide an array of etched silicon three-dimensional targets with additional targets fabricated using industry standard process levels. These wafers additionally have an extensive set of characterization targets and structures developed in close collaboration with SEMATECH and several leading semiconductor manufacturers.

DELIVERABLES: Update the formal qualification numbers on the overlay microscope, optics, and the *x*-*y* metrology stage. This is largely completed and the final uncertainties need to be tabulated. The current, most difficult challenge is the qualification for calibration of complex overlay target process levels such as contact-to-poly. 2Q 2002.

DELIVERABLES: Use the new metrology reticles from the ISMT collaboration to make leading edge overlay calibration targets/wafers. Work with industry partners to determine designs and which levels are most appropriate for the silicon fabrication phase. Calibrate these overlay standards (both alignment and calibration) for SRM certification, 3Q. 2003.

2. The ultraviolet transmission microscope, calibration of NIST Photomask Linewidth Standard SRM 2059, and the development of calibration methods to obtain photomask linewidth measurement uncertainties adequate to meet industry needs.

The technical strategy for photomask linewidth standards is similarly divided into two segments: (1) instrumentation and model development and (2) design and calibration of standard artifacts. An ultraviolet transmission microscope (Fig. 1) has been constructed to replace the green-light linewidth calibration system. This new instrument uses a unique geometry (a Stewart platform) as the main rigid structure and shows considerable improvement in vibration characteristics over a conventional microscope. Higher image resolution, reduced transmission of UV light through the chrome, and reduced instrument vibration will offer improved linewidth measurement uncertainties.

NIST has supplied a substantial number of photomask linewidth standards worldwide over the past decade. Chrome-on-quartz photomasks with linewidth and pitch features in the range of 0.5 μ m to 30 μ m have been certified on a green light optical calibration system. Linewidth uncertainties have been reduced to 40 nm. The next generation in this line of standards is SRM 2059 (Fig. 2), printed on a standard size 6x6x0.25 inch substrate with calibrated line- and spacewidths ranging from nominally 0.25 μ m to 32 μ m and pitch patterns from 0.5 μ m to 250 μ m.



Figure 1. The NIST Scanning Ultraviolet Microscope.

In response to customers' needs for more accurate photomask feature size measurements, an industry group was formed for the improvement of mask metrology through process modeling. The features on even the highest quality masks exhibit roughness and runout at the chrome edges, compromising the definition of edge and linewidth. Modeling the effects of all of the relevant feature properties in both the mask metrology process and in wafer exposure and development processes, using existing and new software tools, can improve feature size accuracy by establishing the relationship between maskfeature metrology results and the corresponding wafer-feature sizes.

DELIVERABLES: Upgrade ultraviolet source intensity on the UV microscope for SRM 2059 photomask calibrations. 3Q 2002.

DELIVERABLES: Commence circulation of the NIST linewidth standards for the BIPM international comparison. 3Q 2002.

3. The third component is the development of two-dimensional grid calibration standards and associated measurement techniques, including statistical analysis and CCD characterization as used by industry. These individual technical

"Researchers in the NIST Overlay Metrology project are developing measurement techniques aimed directly at improving overlay measurement accuracy and optical characterization. The member companies support their effort and believe they are making useful contributions in overlay metrology and standards development." Beth Russo Motorola and International SEMATECH

strategies for these components are described in more detail below.

We are approaching the problem of twodimensional measurements from a couple of directions. The first, and most immediate step is to develop an artifact standard which can be used to bring all of the two-dimensional based inspection instruments to the same metric. This work has developed a standard grid which will be available as a NIST Standard Reference Material, # 5001, to standardize 2D measurements in the semiconductor industry. The effort has three main parts: development of an industry consensus standard grid, measurements by state-of-theart machines in private industry, and verification of the measurements using NIST capabilities.

Grids for the SRM have been made and final measurements are in process. Each measurement of the grid will have data in each of at least two orientations. Rotating the grid 90° between measurements samples a number of the geometric errors of the machine. The remaining geometric sources of uncertainty are the scale and some components of the linearity of each machine axis travel.

Verification of the grid measurements is being done at NIST. The overall scale of the grid is checked with the NIST linescale interferometer, an instrument that is known to provide the most accurate 1D measurements available in the world. Two sources of uncertainty not captured by these measurements include components of the straightness and effects of the plate bending when fixtured. Work is now focused on methods to characterize both of these effects. These studies provide a complete error budget for SRMs.

To strengthen the foundation of NIST's claims for linewidth measurement traceability and to support the BIPM *Mutual Recognition Arrangement*, NIST has become the pilot laboratory for an international intercomparison of submicrometer linewidth measurements. National metrology institutes in nine countries around the world are participating.

DELIVERABLES: Calculate asymmetric overlay targets images upon successful comparison for modeling results of more standard double etched silicon structures. Publish and present these results at SPIE Microlithography, 2Q 2002.

DELIVERABLES: Continue to develop comprehensive analysis capabilities for centerline and edge detection methods. This includes the implementation of automated positioning and focus mechanisms. 3Q 2002.



SRM 2059 the next generation NIST photomask linewidth standard

Figure 2. The new linewidth photomask standard.

DELIVERABLES: Develop methods for CCD calibration and analysis. Utilize the new microgrid and 8 inch overlay wafers for calibration of optics and the CCD acquisition systems using the new self-calibration methods. Implement more advanced methods for TIS/WIS separation and present at SEMATECH member company forums. 4Q 2002.

DELIVERABLES: Complete the 2-dimensional grid artifact calibrations and measurements. This is a combined industry/NIST effort using our LSI and statistical methods. Deliver the reticles to the SRM office. 4Q 2002.

DELIVERABLES: Complete calibrations of SRM 2059 and the related documentation, and deliver to the Office of Standard Reference Materials for distribution to customers. 4Q 2002.

Accomplishments

SRM 2800 Microscope Magnification Standard is a standard-size microscope slide with calibrated pitch features ranging from 1 μm to 1 cm. It contains a lithographically produced chrome pitch pattern consisting of a single array of parallel lines with calibrated center-to-center spacings. It contains no linewidth structures. This SRM is intended to be used for the calibration of reticles and scales for optical or other microscopes at the user's desired magnification. The SRM may be used in either transmission or reflection mode optical microscopes, SEMs, or SPMs. Calibration is traceable to the meter through NIST Line Scale Interferometer. Fiftysix units have been calibrated and delivered to the NIST Office of Standard Reference Materials.

• NIST is currently commencing calibration for SRM 2059 Photomask Linewidth Standard, intended to enable customers to make traceable measurements of the dimensions of features on integrated circuit photomasks.

New image recognition and quantitative image analysis software has been developed by lead analyst J. Jun of the Precision Engineering Division. This comprehensive software package is based on the Matlab programming language and tool set and allows the evaluation of numerous effects on algorithm performance. The package has been used to quantify feature roughness and asymmetry effects on overlay pattern evaluation used in the feedback and control of lithography stepper tools. It has also been used in the quantification of algorithm robustness for sample-to-noise effects. This code has been used extensively to evaluate correlation and leastsquares.



Figure 3. The potential effects in improved target recognition and analysis are seen in this improved correlation curve and fitting routine.

• Two sets of overlay wafers have now been received from SEMATECH. These will be made available in the very near future as RM 8100 for overlay.

The overlay metrology project is working closely with several companies such as Schlumberger and KLA Tencor to make available recent important research results on optical characterization, CCD data acquisition calibration, and focus and edge detection work. Neil Sullivan of Schlumberger showed strong interest in strengthening the collaboration with the overlay metrology project. NIST development of new correlation methods and image analysis/recognition software has enabled the detailed evaluation of noise, feature roughness, and feature inhomogeneity effects on repeatability and robustness of measurement tool performance, issues of paramount importance in semiconductor overlay metrology. We have performed a detailed, in depth study of CCD data acquisition cameras including the development of CCD mapping methods

The NIST Overlay Metrology project leader has played a significant role in the Overlay Metrology Advisory Group (OMAG) of ISMT. This group is developing a comprehensive set of measurement guidelines, test methods, and tool performance measures to be adopted by the semiconductor manufacturing industry. The group is made up of more than 15 international semiconductor manufacturers. The OMAG has strong interest in adopting several new methods developed in the NIST Overlay Metrology Project. In particular, the recently published methods for evaluating CCD array performance and overall optical system characterization and calibration performance measures have been adopted.

• The OMAG, organized by ISMT has completed the specification document for the evaluation and benchmarking of overlay metrology tools for semiconductor manufacturing. The document will be used for procuring, testing, and matching tools.

• The first set of two-dimensional grid artifacts, is known as SRM 5001, and has been received. These 6-inch wafer artifacts have been measured on a state-of-the-art I-pro metrology system by the photomask manufacturer. This effort, to make available traceable, 6-inch feature placement standards involves a close collaboration between NIST and Photronics. The collaboration employs the industry tool and the traceability of the NIST line scale interferometer with appropriate statistical analysis. The uncertainty budget for grid measurements has been developed and peripheral studies on various items are near completion.

NIST researchers have made comparisons between the E. Marx developed optical scattering code with the Spectel company Metrologia metrology modeling package. Different material systems were compared as well as one overlay feature at different focus positions. New results, based on the full integration of the NIST scattering code and Spectel optical microscope model, show very good agreement. This is an important step in the effort to provide industry the quantitative ability to determine sample-dependent effects on overlay tool performance. Results are to be presented at SPIE Microlithography, 2002.

• Near completion for the clean room enclosure on the overlay metrology tool. This will allow us to work closely with the industry and make SRMs directly transferable to a clean room environment.

• Leadership for the industry group for the improvement of mask metrology through process modeling has been transferred to ISMT.

Collaborations:

ISMT, IBM, IVS Schlumberger, KLA-Tencor, Intel, Motorola, AMD and several other leading manufacturers or tool vendors.

The fourteen members of The Neolithography Consortium.

Recent Publications

2.5

R. Silver, J. Jun, E. Kornegay, "Recent advances in Overlay Metrology," Future Fab, 2001.

J. Potzick, "The problem with submicrometer linewidth standards and a proposed solution," *Proceedings of SPIE 26th International Symposium on Microlithography*, vol. 4344-20 (2001).

R.M. Silver, J. Jun, E. Kornegay, and R. Morton, "Comparison of Edge Detection Methods using a Prototype Overlay Calibration Artifact," Proc. SPIE Microlithography, Feb. 2001. T. Doiron and R. Silver, "Two-dimensional grid Standards," Proc. Measurement Sciences Conf., 2000

S. Fox, E. Kornegay, and R. Silver, "Characterization of Imaging Optics and CCD Cameras for Metrology Applications," *Characterization and Metrology for ULSI Technology*, D. Seiler, et. al., eds, A.I.P. Press, 2000, pp. 378-382.

S. Fox, R. Silver Thesis Advisor, "Focus, Edge Detection, and CCD Camera Characterization for Development of an Optical Overlay Calibration Standard," Graduate Thesis, Univ. of MD, 2000.

J. Potzick, "The Neolithography Consortium--a progress report," *Proceedings of BACUS Symposium on Photomask Technology*, vol. 4186-73 (2000).

J. Potzick, "The Neolithography Consortium," Proceedings of SPIE 25th International Symposium on Microlithography, vol. 3998-54 (2000).

M. Schroeck, and T. Doiron, "Probing of two-dimensional grid patterns by means of camera based image processing," accepted by SPIE for January 2000.

K. Meissner, and T. Wegener, "Robust Regression for Two Dimensional Coordinate Measurements," Proceedings of the International Symposium on Laser Metrology for Precision Measurement and Inspection in Industry, Florianoplis, Brazil, October 13-15, 1999.

R. Silver, T. Doiron, S. Fox, E. Kornegay, M. Takac, and S. Rathjen, Two dimensional Grid Standards, Proceedings of the SPIE, The International Society for Optical Engineering, Metrology, Inspection, and Process Control for Microlithography XIII (1999).
Scanning Probe Microscope-Based Dimensional Metrology

Goals

Improve the measurement uncertainty of criticaldimension measurements in the semiconductor industry through improvements in SPM-based measurements. The International Technology Roadmap for Semiconductors (ITRS) identifies dimensional metrology as a key enabling technology for the development of nextgeneration integrated circuits. For example, the goal in 1999 for critical dimension (CD) measurement precision for isolated lines was ± 2.8 nm; this demand tightens to ± 0.8 nm by 2011. The technical focus of this project, development and implementation of scanned probe microscope instrumentation, is driven by the anticipated industry needs for reduced measurement uncertainty, particularly for existing tools such as the SEM.

Customer Needs

The SEM is the current tool of choice for inspection and metrology of sub-micrometer features in the semiconductor industry. SPMs unique capabilities, which possess may significantly enhance the performance of SEMs in-line critical dimension for (CD)measurements, and are also emerging as CD measurement tools in their own right. A creative strategy, which successfully harnesses the strong points of both techniques in order to reduce the measurement uncertainty of sub-micrometer features, will help NIST meet the expectations of the semiconductor industry expressed in the current ITRS. As is the case with SEMs, the magnification or scale of an SPM must be calibrated in order to perform accurate measurements. Although many SPMs are commercially available, appropriate calibration standards have lagged. In particular, traceable pitch/height standards with sub-micrometer pitch values are not yet available.

Technical Strategy

SPM development is proceeding along two parallel directions: The first direction addresses dimensional metrology of SPM specifically through an in-house research instrument we refer to as the calibrated atomic force microscope (C-AFM). This instrument, with metrology traceable to the wavelength of light for all three axes of motion, is furthering the design and

development of SPM standards as well as providing customers with calibrated dimensional measurements at the nanometer scale. For example, pitch, height, and width measurement capabilities of the C-AFM have been evaluated and validated by internal comparisons. Pitch, ranging up to 20 µm has been measured with standard uncertainties (u_c) as low as ~0.5 nm at sub-micrometer scales and relative standard uncertainties of ≈ 0.1 % at the largest scales. Step height, ranging from a few nanometers up to several hundred nanometers, can be measured with u_c on the order of 0.5 %. The width of near-vertical features, sub-micrometer, as encountered in CD measurements, can be measured with u_c of ~10 nm, due mostly to the finite size of the SPM tip. As part of the project, we have begun to pursue research in the measurement and standardization of line edge roughness.

DELIVERABLES: Draft procedure for calibration of AFM z-scales with Si single atom step heights completed and submitted to ASME and ASTM Standards Committees. 3Q 2002

DELIVERABLES: Report published demonstrating improved uncertainty for linewidth measurements using sharpened tips. 1Q 2003

DELIVERABLES: SRM 2089, a combined pitch and height standard for AFM, released. 2Q 2004

DELIVERABLES: Reports submitted on three remaining international Preliminary Key Comparisons in Nanometrology: step heights, 2D grids, and linewidth. 3Q 2003

DELIVERABLES: Report published demonstrating improved performance of the C-AFM after integration of a new x-y and z stage to increase scan area and reduce motion errors. 1Q 2003

DELIVERABLES: Report published demonstrating traceable measurements of line edge roughness using an AFM. 1Q 2004

The second direction addresses increasingly overlapping demands for dimensional control during fabrication and subsequent calibration of nanometer scale features. For this purpose we employ an SPM-based lithography technique, pioneered at NIST, to produce grating structures with linewidths of 20 nm or below. Latent oxide patterns function as masks for anisotropic wet or Technical Contacts: T.V. Vorburger J. A Dagata R. Dixson M. T. Postek

"VLSI Standards has been working to respond to the Semiconductor Industries needs for a NIST traceable pitch standard to calibrate CD SEMs. I want to thank you for suggesting to our engineers an appropriate methodology. Our staff really enjoy working with you and with many groups at NIST, and I hope that we can collaborate on many projects in the future."

Ian Smith, President VLSI Standards, Inc. dry etching. We are also developing an instrument which integrates both SPM and probe station measurement capabilities whereby we are able to compare SPM-based electrical (capacitance and surface potential) and topographical measurements of active device structures simultaneous with traditional current-voltage (I-V) characteristics measured with a probe station. This allows us to examine local nanoscale variations at exposed and buried interfaces of critical dimensioned features in order to identify processing induced variations which contribute to linewidth uncertainty in dimensional and electrical test structures.

DELIVERABLES: Data analysis of optical and SEM images for a series of six one dimensional calibration prototypes produced by SPM oxidation and anisotropic etching of silicon. Report in preparation. 1Q 2002

DELIVERABLES: Demonstrate the use of submicrometer-pitch, two dimensional grids produced by SPM oxidation and anisotropic etching for controlling the spatial configuration of block co-polymer films. Second phase using large-scale patterned substrates underway. 3Q 2002

DELIVERABLES: Fabricate a two dimensional metal-silicon grid using SPM oxidation and anisotropic etching for characterizing automated SEM grain boundary detection. Proof-of-concept demonstrated, work underway on extending technique to large-scale patterned substrates. 4Q 2002

DELIVERABLES: Demonstrate a combined maskless optical and SPM lithography system for prototyping sub-100-nm pitch calibration scales integrated onto 1 cm square chips. 1Q 2003

DELIVERABLES: Demonstrate large-scale replication of sub-100 nm pitch one and two D features using SPM lithography, anisotropic etching, and nanoimprint lithography techniques. 3Q 2003

DELIVERABLES: Fabricate functional microfluidic arrays with nanoscale features using combined maskless optical, SPM, and nanoimprint lithographies. 1Q 2003

Accomplishments

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The C-AFM thrust involves collaboration with industrial users and academic researchers in AFM metrology, as well as interaction with researchers in national measurement institutes in other nations. During 2001 we completed traceable pitch measurements for a metrology supplier to the semiconductor industry and issued a report. This was the fourth such test we have performed for customers in microelectronics related industries. We reported an expanded uncertainty (k=2) of approximately 0.16 %, limited by sample uniformity.

We are participating in a series of international Preliminary Key Comparisons in nanometrology coordinated by the CIPM (Comité International des Poids et Mesures) CCL (Coordinating Committee for Length). Successful participation in these Comparisons will facilitate international recognition of NIST-traceable measurements of dimensional quantities important to the semiconductor industry. Comparisons of 1D pitch, 2D pitch, step height, and linewidth measurements are being carried out. For the 1D pitch comparison, gratings having nominal pitches of 300 nm and 700 nm were measured using the C-AFM. This Comparison has now been completed by all participants and published and NIST's measurement service for pitch is now listed in Appendix B of the Mutual Recognition Arrangement (MRA) between national measurement institutes (NMIs) under which the NMIs recognize each other's measurement capability, thus helping to eliminate technical barriers to trade. Appendix B establishes the technical underpinning of the MRA by showing the technical bases for mutual recognition.

We are currently measuring specimens for a Preliminary Key Comparison for Step Height. For this work we have completed the installation of a new x, y stage and have tested its displacement range, angular motion errors, and out-of-plane motion. With 100 µm range in both the x and y directions, typical angular motion error of ~0.5 µR, and out-of-plane motion of a few nanometers over the entire x,y scan range, the new motion stage has significantly improved performance over the previous one. Figure 1 shows one of three sets of angular motion errors measured using an autocollimator. Figure 2 shows elements of the C-AFM as it was being reassembled and aligned. Preliminary measurements with the reassembled C-AFM of a 20 nm step height show good agreement with previous measurements of this step taken with both the C-AFM and other instruments.



Figure 1. Autocollimator data for the new C-AFM motion stage showing rotation error around the x-axis. Maps for both fast-x scan with stepping in y and fast-y scan with stepping in x are overlayed here.



Figure 2. Photo of C-AFM during reassembly. A) x,y, motion stage, B) metrology plate, C) interferometer beam splitters, D) sample platform mounted on zmotion stage. The AFM sensor is not shown.

Another effort involves the study of single atomic Si steps as fundamental height standards in the sub-nanometer regime. During 2001 we completed research on the subject by publishing the results of our independent traceable measurements of these steps as well as the results of a laboratory comparison by industrial colleagues testing the reproducibility of measurements on the steps and their potential usefulness as a calibration standard. This year we plan to submit a procedure for AFM z-calibration using the single atom steps to the ASTM Subcommittee 42.14 on STM/AFM and the ASME B46 Committee on the Classification and Designation of Surface Qualities.

• We also began work on measurement and development of physical standards for line edge roughness (LER), a potential showstopper in the *ITRS*. With colleagues at IBM Almaden Research Center, we organized a special meeting of researchers to discuss the key issues in LER metrology and set directions for future research.

Ronald Dixson is currently on detail as NIST's first Guest Scientist at International Sematech. He is working with Sematech researcher Marylyn Bennett on calibration and statistical process control techniques to establish Sematech's critical dimension AFM as a reference measurement system (RMS) with close traceability to the SI unit of length. The RMS-AFM will be used for measurements of pitch, height, and CD. A joint publication of NIST and International Sematech on this work is cited below.

In the integrated SPM probe-station thrust, we have completed construction and testing of the combined instrument. Test structures consisting of silicon FETs realized on silicon-oninsulator substrates are being used as a starting point for patterning nanodevices and performing in-situ correlation of the dimensional and electrical properties of these confined regions. SPM lithography has been used interactively with electrical mapping to create successively smaller active gate regions for detailed studies of local device scaling. This capability allows us to examine local nanoscale variations at exposed and buried interfaces of critical dimensioned features in order to identify processing induced which contribute to variations linewidth uncertainty.

We have also demonstrated large-scale (100 μ m × 100 μ m) patterning and anisotropic etching of sub-50 nm linewidth SPM oxide features on 110-oriented silicon substrates, as shown in Figures 3 and 4. A series of six 1-D pitch calibration prototypes were produced and analyzed using calibration optical and SEM instruments at NIST. The absolute placement accuracy of the oxide patterns was determined, allowing an instrument error map to be constructed. Error correction will reduce placement errors to well below 0.1 % over the 100 μ m scan range of the SPM, limited by thermal gradients caused by an on-board CCD camera. A new series of prototypes will be

produced to demonstrate placement accuracy in the sub-10 nm range. 2-D grid structures have also been fabricated using these methods.

(a) SEM accessible scale



(b) optically accessible scale



Figure 3. (a) SEM accessible scale of a 1-D pitch calibration prototype produced by SPM oxidation and anisotropic etching of a silicon substrate. (b) Optically accessible scale with 8 μ m pitch.

(a) measured pitch/nominal pitch



(b) SEM image of 100-nm pitch features



Figure 4. (a) Calibrated pitch measurements from SEM and optical analysis demonstrating 3-4 nm absolute pattern placement accuracy for etched SPM oxide features patterned on a silicon substrate.

Collaborations

Department of Mechanical Engineering, University of North Carolina, Charlotte

Physikalisch Technische Bundesanstalt, Braunschweig, Germany

IBM Almaden Research Center, San Jose, CA

Department of Computer Science, University of North Carolina, Chapel Hill NC

School of Mechatronic Engineering, Harbin Institute of Technology, Harbin, China

General Electric Corporate Research and Development, Niskayuna NY 12309

Departments of Physics and Engineering, University of Akron, Akron OH

National Institute of Advanced Industrial Science and Technology, Tsukuba Japan

National Microelectronics Center of Spain, Barcelona Spain

Center for Measurement Standards, Industrial Technology Research Institute, Hsinchu Taiwan

Department of Physics, National Tsing-hua University, Hsinchu, Taiwan

Recent Publications

R. Dixson, N.G. Orji, J. Fu, V. Tsai, E.D. Williams, R. Kacker, T. Vorburger, H. Edwards, D. Cook, P. West, and R. Nyffenegger, "Silicon single atom steps as AFM height standards," Proc. SPIE, 4344, 157, 2001.

R. Köning, R. Dixson, J. Fu, and T.V. Vorburger, "The Role of periodic interferometer errors in the calibration of capacitance displacement sensors for nanometrology applications," Meas. Sci. and Technol., **12**, 2002, 2001.

T.V. Vorburger, R.H. Allen, B. Damazo, J. Fu, D. Monk, M. Osti, J. Pellegrino, R. Rhorer, R. Russell, R. Silver, R. Sriram, K. Stouffer, D.A. Swyt, E.C. Teague, T. Wheatley, and D. Wilmering, "Nanomanufacturing of atom-based dimensional standards, a final report of the National Advanced Manufacturing Testbed," NISTIR 6850 (NIST, Gaithersburg, MD, 2002).

R. Dixson, A. Guerry, M. Bennett, T. Vorburger, and M. Postek, "Toward traceability for at line dimensional metrology," Proc. SPIE, **4689**, 2002 (in press).

F.S.S. Chien, W-f. Hsieh, S. Gwo, A.E. Vladar, and J.A. Dagata, "Silicon nanostructures fabricated by scanning probe oxidation and tetra-methyl ammonium hydroxide etching," J. Appl. Phys., to appear June 2002.

F.S.S. Chien, J.A. Dagata, W-f. Hsieh, and S. Gwo, "Nanomachining of Si with Si3N4 masks patterned by scanning probe microscopy," 5th Conference of Nanoengineering and Microsystem Technology, ITRI, Hsinchu, Taiwan, November 2001.

J.A. Dagata, "Electric force microscopy with a single carbon nanotube tip," Proc. SPIE, **4344**, 58, 2001.

Electrical-Based Dimensional Metrology

Goals

Apply test-structure-based electrical and other sub-tenth-micrometer metrology methods to the development of reference materials primarily for CD and overlay applications. Contribute to standards organizations supporting the development of metrology standards for the semiconductor tool industry.



Figure 1. Christine Murabito using hot plate to do a post-exposure bake during the photo-lithography process.

Customer Needs

The Metrology Section, page 24, of the 2001 ITRS states it is critically important to have suitable reference materials available when a measurement is first applied to a technology generation, especially during early materials and process tool development. Each type of reference material has its own set of difficult challenges involving different combinations of the challenges described above. Each generation of ICs is characterized by the transistor gate length whose control to specifications during IC fabrication is a primary determinant of manufacturing success. The SIA projects the decrease of gate linewidths used in state-of-the-art IC manufacturing from present levels of up to 250 nm to below 70 nm within several years. Scanning electron microscopes (SEMs) and other systems used for traditional linewidth metrology exhibit measurement uncertainties exceeding ITRS-specified tolerances for these applications. It is widely believed that these uncertainties can be at least partially managed through the use of reference materials with linewidths traceable to

nanometer-level uncertainties. Until now, such reference materials have been unavailable because the technology needed for their fabrication and certification has not been available. It is also widely believed that the usefulness of SEM metrology for monitoring wafers in advanced development and production will become inadequate at some future IC generation. Thus, there exists a need for new reference materials to meet future metrology requirements.

Technical Strategy

The technical strategy that the project staff has developed for fabricating linewidth and overlay reference materials is known as the Single-Crystal CD (critical dimension) Reference-Material implementation. Patterning with latticeplane selective etches of the kind used in silicon micro-machining provides reference features with atomically planar sidewalls. Essential elements of the technology are the starting silicon wafers having either a (110) or a (100) orientation; the reference features, which must be aligned to specific lattice vectors; and the lithographic patterning with lattice-plane selective etches of the kind used in silicon micromachining. C. Murabito is shown processing some wafers in Fig.1.

The traceability path for dimensional certification is provided by High-Resolution Transmission Electron Microscopy (HRTEM) imaging. An example of this can be seen in Fig. 2. This method provides nanometer-level accuracy, but is sample-destructive and extremely costly to implement. This project's unique traceability strategy thus currently features the sub-nanometer repeatability of electrical CD metrology as a secondary reference means. Work has been initiated into the application of other methods such as Atomic Force Microscopy (AFM) and Scanning Electron Microscopy (SEM), which may offer special advantages in some cases. For traceability-path purposes, the present strategy remains the calibration of low-cost, whole-wafer electrical measurements with a limited selection of HRTEM lattice-plane image counts. Reference features having of the order of tenth micrometer linewidths are typically several-hundred lattice planes wide. HRTEM lattice-plane image counts, achieved by automated analysis of phasecontrast images, were developed in order to minimize the uncertainties of the linewidths of the standards.

Technical Contact: Michael W. Cresswell

"This work is of technical and economic importance to the semiconductor industry, because the ability to correctly size ever smaller lateral dimensions on silicon substrates is key to the manufacturing yield of silicon chips." Pat J. Brady, Ph.D. President VLSI Standards, Inc. The technical strategy has to be responsive to industry's requirement for reference materials to have the physical properties of standard 200 mm wafers. This project's technical strategy has been to dice each 150 mm wafer and mount the separate chips in micro-machined standard 200 mm wafers to accommodate the test chips. The result is that finished units are user-friendly at an acceptable cost. The entire fabrication and certification process has been transferred to a commercial standards vendor. These chip-carrier wafers are being supplied to, and widely used by, industry clients.



Figure 2. Low magnification transmission-electron micrograph of the complete cross-section of a feature, having a measured ECD of 73 nm.

Recently, project researchers have delivered prototype CD reference materials for calibrating linewidth metrology instruments used in manufacturing semiconductor devices to International SEMATECH (ISMT) for evaluation by member The work was the result of companies. collaborations with ISMT, VLSI Technology Inc., and Sandia National Laboratories as well as collaborations with the Information Technology Laboratory's (ITL's) Statistical Engineering Division and Mathematical, and Computational Division. the Manufacturing Sciences Engineering Laboratory's (MEL's) Precision Engineering Division, and the Materials Science and Engineering Laboratory's (MSEL's) Division, and Scottish Metallurgy the Microelectronics Centre of the University of Edinburgh to fabricate, test, and evaluate this new class of reference materials directed at meeting ITRS goals. The technical approach that was implemented for this delivery was to incorporate the reference features into electrical test structures, thus enabling the determination of

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their electrical linewidth. A selection of 36 test structures was incorporated into the test chip that was patterned in the device layer of (110) siliconon-insulator (SOI) wafers based on wellestablished silicon micro-machining technology that produced feature sidewalls having nearatomic planarity. Primary calibration of the CD of the test-structures on all the test chips was accomplished by means of high cost, low speed HRTEM imaging and lattice-plane counting at a limited number of sites on the wafer. HRTEM provides nanometer-level accuracy, but is sample-destructive besides being too costly to implement on all reference features. The samples delivered to ISMT were calibrated via a statistical correlation with a high-precision electrical CD (ECD) measurement.

DELIVERABLES: Evaluate enhanced fabrication techniques for SCCDRMs to reduce uncertainty of the nominal CDs. Target 50-nm CDs with less than 7-nm uncertainty. Q3 2002

DELIVERABLES: Complete electrical measurements on Single-Crystal Silicon-on-Insulator and Bulk Reference Materials, obtain CD measurements from HRTEM images, and produce transfer calibration data. Q2 2002

DELIVERABLES: Deliver up to 15 improved Single-Crystal Silicon-on-Insulator and/or bulk Reference Materials to ISMT mounted in 200-mm chip carriers supplied by ISMT contractor. Transfer improved fabrication and calibration technology to commercial standards supplier. Q1 2003

Accomplishments

For the first time, CD-reference features have been designed, built, and tested on bulk (110) wafers using junction isolation to isolate the test feature from the bulk wafer. Samples with measured linewidths below 180 nm were evaluated with no adverse leakages from feature to bulk observed. Junction isolated reference materials offer lower initial material costs, simplicity in processing, and possible lower calibration uncertainties.

Based on a NIST patent entitled "Test Chip Reference-Artifact Carrier," a silicon-valley company has completed the development of 200 mm and 300 mm chip-carrier wafers that were developed by the project last year and has transferred the product to its marketing operation for product distribution.

National Institute of Standards and Technology



Figure 3. Data relating ECD to physical linewidth with calibration function.

Semiconductor Electronics Division (SED) researchers have delivered prototype CD reference materials, RM-8110, for calibrating linewidth metrology instruments used in manufacturing semiconductor devices to ISMT for evaluation by member companies. An example of the calibration curve between ECD and HRTEM is shown in Fig. 3. Finished CD reference materials were mounted in 200 mm pocket wafers. These materials respond to a need identified by the SIA ITRS that states that it is critically important to have suitable reference materials to support the development of advanced lithography tools and processes.



Figure 4. A TEM image cross section of another feature on the same wafer.

• The uncertainty attributed to the physical CD values of the reference features that were delivered to ISMT members last year was typically 13 nm. An apparent time dependence of the electrical CD of the as-patterned reference features is believed to be responsible for most of this uncertainty. However, project staff have now demonstrated that a forming-gas annealing treatment just prior to electrical CD extraction appears to

prevent the referenced time dependence and thus has the potential for reducing the uncertainty levels.

A second generation of CD and scatterometry reference materials has been designed at NIST and lithographically patterned by sub-contractor teams at the University of Edinburgh and Sandia National Laboratories to NIST's specifications. The more advanced properties of these reference materials include provisions to suppress reference-feature and local-substrate charging under SEM inspection and further uncertainty reduction by reference-feature pre-patterning with the use of reactive ion etching. The pattern-transfer processes have now been transferred to ISMT. An early example of the success of this new laboratory collaboration with ISMT staff is shown in the SEM image of a 58-nm line in Fig. 4. A TEM image cross section of another feature on the same wafer is shown in Fig. 5.



Figure 5. 58-nm vertical-sidewall reference feature replicated on a p-type (110) bulk substrate is an early example of the success of the new collaboration with ISMT staff.

A decontamination process using oxygen plasma was developed for cleaning CD reference features mounted in 200 mm chip-carrier wafers. The procedure successfully removed hydrocarbon contamination that is often deposited when the material is inspected by an SEM. A 35minute oxygen plasma etch removed the bulges, removed the associated rectangular carbon stain on the surrounding substrate surface, and decreased the size of the circular defects on a test structure reference segment and surrounding area that are sometimes created by beam-focusing. This hydrocarbon contamination cleaning process was applied to a reference feature on a chip supplied to an ISMT company that had been contaminated by a SEM.

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Collaborations

The IC Technology Group, in collaboration with the National Research Center of Finland (VTT) and the George Washington University, has demonstrated the feasibility of a novel noncontact capacitive-sensor metrology tool developed for chrome photomasks. The sensor is intended for use as an independent metrology tool for mask makers and mask users. The linewidth metrology sensor, developed using a Low Temperature Co-Fired Ceramic (LTCC) technology, is based on non-contact microcapacitance measurements of features located on chrome-on-glass reticles. Initial results indicate that the non-contact capacitive sensor is capable of extracting chrome-feature linewidths in the range of 0.4 μ m to 0.5 μ m.

In collaboration with the Precision Engineering Division (PED), the SED is developing stage micrometers, with the goal of providing them to industry as NIST SRMs. Stage micrometers are used extensively for calibration of optical microscopes; however, unless they have been individually calibrated by NIST, currently a slow and expensive process, they do not provide a traceable calibration. By combining fast and inexpensive electrical test structure metrology with NIST-traceable measurements on PED's Linescale Interferometer, NIST will be able to make calibrated stage micrometers widely available at a reasonable cost. The initial designs are completed and test samples are expected early in FY 2002.

In collaboration with ITL's Mathematical and Computational Sciences Division, an initial machine-counting procedure for improving the determination of the number of lattice planes as determined from HRTEM images was developed. The overall emphasis is to reduce the analysis time and to improve the overall linewidth uncertainty.

ISMT and ISMT member companies (AMD, Compaq, Conexant, Hewlett-Packard, IBM, Intel, Lucent Technologies, Motorola, Texas Instruments, Hyundai, Infineon Technologies, Philips, STMicroelectronics, TSMC), April 30, 2001 delivery of prototype CD reference materials, to meet ISMT MDL (Michael W. Cresswell and Richard A. Allen).

ISMT, Sandia National Laboratories, and NIST have collaborated on the optimization of silicon patterning and nitride stripping processes for the SIMOX and bulk implementations of the

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SCCDRM application. (Michael W. Cresswell and Richard A. Allen).

Precision Engineering Division, Bill Penzes, development of electrically calibratable stage micrometer (Richard A. Allen).

Process Measurements Division, Michael Carrier, made plots and reviewed new chip (Colleen H. Ellenwood).

 Scientific Computing Division, Hai Tang, assistance with ANSYS model of single crystal CD reference material project (Colleen H. Ellenwood).

Simplex Solutions, Inc., LSI Logic, and Chartered Semiconductor, procedures and algorithms for CD extraction from test features having conformal coatings (Michael W. Cresswell).

• Scottish Microelectronics Centre of the University of Edinburgh, in the development of a hybrid RIE and lattice-plane selective etch process for the patterning of silicon reference features and a hybrid RIE-hot-phosphoric immerse for nitride stripping (Michael W. Cresswell, Loren W. Linholm, and Richard A. Allen).

 VLSI Standards, Inc., and ISMT, development of commercial architecture and distribution plan for single-crystal CD reference materials (Michael W. Cresswell and Richard A. Allen).

• Texas Instruments, Dallas, and ISMT on comparison of AFM and electrical CD measurements maded on a selection of SCCDRM features. (Richard A. Allen and Michael W. Cresswell).

Standards Committee Participation

 SEMI International Standards Electrical Metrology Test Structures Task Force, Co-Chair (SEMI Doc 2860 balloted, winter 2000) (Richard A. Allen)

 SEMI International Standards Microlithography Committee, member (Richard A. Allen)

Recent Publications

R.A. Allen, T.J., Headley, S.C. Everist, R.N. Ghoshtagore, M.W. Cresswell, and L.W. Linholm, "High-Resolution Transmission Electron Microscopy Calibration of Critical Dimension Reference Materials," IEEE Transaction on Semiconductor Manufacturing, vol. 14, no. 1, pp. 26-31, 2001.

M.W. Cresswell, and R. A. Allen, "Electrical CD Metrology and Related Reference Materials, in Handbook of Silicon Semiconductors Metrology," A. C. Diebold, Ed. (Marcel Dekker, Inc., New York - Basel, 2001), pp. 377-409. M.W. Cresswell, N. Arora, R.A. Allen, C.E. Murabito, C.A. Richter, A. Gupta, L.W. Linholm, D. Pachura, and P. Bendix,, "Test Chip for Electrical Linewidth of Copper-Interconnection Features and Related Parameters," Proceedings of the 2001 IEEE International Conference on Microelectronic Test Structures, Kobe, Japan, March 19-22, 2001, vol. 14, pp. 183-188.

N. Guillaume, J. Kiihamaki, J. Karttunen, and H. Kattelus, "Use of Electrical Test Structures to Characterize Trench Profiles Etched on SOI Wafers," Proc. IEEE 2001 Int. Conference on Microelectronic Test Structures, vol. 14, March 2001, pp. 159-164.

W.B. Penzes, R.A. Allen, M.W. Cresswell, L.W. Linholm, and E.C. Teague, "A New Method to Measure the Distance Between Graduation Lines on Graduate Scales," IEEE Transactions on Instrumentation and Measurement, vol. 49, no. 6, December 2000, pp. 1285-1288. Cresswell, M.W., Allen, R.A., Guillaume, N.M., Murabito, C.E., andLinholm, L.W., Electrical Linewidth Test Structures Patterned in (100) Silicon-on-Insulator for Use as CD Standards, IEEE Transactions on Semiconductor Manufacturing, Vol. 14, No. 4, pp. 356-364 (November 2001).

Allen, R.A., Cresswell, M.W., Murabito, C.E., Guthrie, W.F., Linholm, L.W., Ellenwood, C.H., and Bogardus, E.H., Test Structures for Referencing Electronics Linewidth Measurements to Silicon Lattice Parameters Using HRTEM, Proceedings of the 2002 ICMTS, Cork, Ireland, pp. 13-18 (April 2002).

am Ende, B.A., Cresswell, M.W., Allen, R.A., Headley, T.J., Guthrie, W.F., Linholm, L.W., Bogardus, E.H., and Murabito, C.E., Measurement of the Linewidth of Electrical Test-Structure Reference Features by Automated Phase-Contrast Image Analysis, Proceedings of the 2002 ICMTS, Cork, Ireland, pp. 1-6 (April 2002). Technical Contacts: Ronald L. Jones Eric K. Lin Wen-li Wu

"The SANS method is a new technique to measure lithographic patterns, capitalizing on the unique capability of the NIST Center for Neutron Research. It complements existing Scanning Electron Microscopy and Atomic Force Microscopy methods and could serve as a calibration standard, particularly as we further scale semiconductor devices."

Qinghuang Lin TA to Director of Silicon Technology IBM T. J. Watson Research Center

X-Ray and Neutron Small Angle Scattering-Based Dimensional Metrology

Goals

Develop methods of pattern characterization using small angle scattering of x-ray and neutrons on structures produced by current and nextgeneration lithographic patterning. Quantities of interest include critical dimension, sidewall angle, and statistical deviations across large areas. Of particular focus is delivering an absolute determination of parameters contributing to line edge roughness, such as fluctuations in critical dimension over large areas and correlations in these fluctuations along a sidewall. The development of these techniques will provide a new characterization technique for standard reference materials, supporting existing techniques such as CD-SEM, AFM, and light-based scatterometry.

Customer Needs

The drive to reduce feature sizes to the sub-100nm regime imposed by the ISMT Roadmap continues to challenge traditional metrology techniques for pattern characterization. As pattern sizes decrease, existing techniques such as CD-SEM face significant technical hurdles in imaging quantities such as Line Edge Roughness (LER). Emerging metrologies based on techniques such as atomic force microscopy are still being evaluated, providing a lack of clear definition in suitable metrology for standardized measurements of both organic and inorganic structures. To address these issues, NIST is evaluating the potential application of both x-ray and neutron scattering as metrology tools in both fundamental photoresist research and in the production of standards for industrially relevant metrologies such as CD-SEM.

Technical Strategy

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1. The implementation of 157 nm wavelength exposure tools and resists expected by 2005 will further restrict the critical dimension (CD) budget, requiring control of CD to within 10 nanometers. Current methods of critical dimension measurement are not believed to possess this level of precision, however significant investments in CD-SEM metrology suggest its continued use as the prevalent metrology tool. We are developing scattering based methods capable of angstrom level precision in critical dimension evaluation over large arrays of periodic structures. These techniques offer the possibility of calibration of industrial methods and evaluation of their limits. Using patterned photoresists with large arrays of equivalently spaced lines, we have provided the first measurements of pattern quality. Patterns can be produced within a fabrication line without substantial alteration in processing parameters. As an example, the required square centimeter spot size allows patterns to be produced as part of a standard dose matrix. Samples from both IBM Yorktown Heights and Shipley, Inc. have been measured using SANS at varying angles of incidence. Below, SEM images show a series of samples provided by Shipley in which the photoresist formulation is varied but each pattern is generated under optimal focus conditions.



SEM micrographs of photoresist grating patterns produced under optimal conditions. Shown are three different photoresist formulations.

We have performed initial tests of the technique on commercial photoresists and demonstrated nanometer level precision in average critical dimension. The non-destructive nature of the neutron scattering measurement allows direct comparison of identical samples to other metrology techniques, and similar measurements are planned using SEM and AFM based techniques.

DELIVERABLES: Provide measurements of critical dimension in a commercial photoresist pattern with SANS. 3Q 2002

2. Characterization of pattern quality includes shape factors indicating the slope of the line edge and curvature. Using the above protocol for scattering, measurements taken at a series of angles of incidence allow the reconstruction of the line shape in a manner similar to microscopic tomography. We have performed an initial set of tests using multiple angles on a test grating and determined an ability to measure sidewall angle to within 3°. Ongoing analysis and technique refinement will provide additional shape factors, allowing determination of more complex shape information such as sidewall curvature. In addition, patterns of varying dimension, including arrays of contact holes, are subject to similar analyses.

DELIVERABLES: Provide measurements of line shape in terms of simple trapezoidal model for photoresist grating patterns. 3Q 2002

DELIVERABLES: Provide measurements of sidewall curvature. 1Q 2003

3. Fluctuations in critical dimension result from both mask related issues, such as overlay or defects, and factors related to the image development within the photoresist, such as acid Fluctuations in CD are observed diffusion. through spreading of the Bragg diffraction peaks, requiring a precise determination of resolution smearing effects. Initial measurements have demonstrated the SANS measurements to be limited in this capacity by a poor resolution in wavelength. To test the limits of feasibility with current SANS technology, samples were measured on a neutron perfect crystal diffractometer (PCD) that provides the same data as the SANS but at substantially better resolution. Additionally, ongoing studies with small angle x-ray. scattering (SAXS) are probing the possibility of measurements without substantial resolution smearing effects. SAXS measurements provide the additional possibility of measurement within industrial fabrication facilities.



Schematic of NCNR Perfect Crystal Diffractometer

DELIVERABLES: Determine relative contribution of critical dimension fluctuation to Bragg peak width in SANS CD measurement. 3Q 2002

DELIVERABLES: Provide first transmission measurements of photoresist gratings using SAXS. 4Q 2002

4. While there is little direct connection of Line Edge Roughness (LER) to gate electrical performance, the routine specification of LER in CD budgets requires high precision metrology for both quality control by vendors as well as quality assessment by customers. The definition of LER itself is yet to be determined. Currently, metrologies such as CD-SEM, a top down technique, measure qualitatively different quantities compared to that of light scatterometry and AFM. Our approach is to provide metrology of sidewall roughness, where sidewall roughness is defined by deviations from the average sidewall plane on length scales smaller than the CD. These measurements can then be connected to varying definitions of LER through cross measurement of samples with, for instance, CD-SEM. In the case of photoresists, we are employing AFM to provide the appropriate wavevector range, or frequency spectrum, over which correlations exist. This data is being used to develop the appropriate neutron and x-ray optical configurations for sidewall roughness characterization. It is our goal, however, to produce techniques applicable to a wide range of roughness types and size scales with minimal technique modification.

DELIVERABLES: Provide relevant wavevector range for sidewall roughness scattering measurements. 3Q 2002

DELIVERABLES: Develop metrology of sidewall roughness based on small angle scattering. 2Q 2003

Accomplishments

We provided the first measurements of critical dimension using small angle neutron scattering. Using a series of commercial photoresists imaged with parallel line masks, 1dimensional Bragg diffraction patterns characteristic of uniformly spaced gratings were analyzed to provide the pattern CD with precision on the order of 10 nanometers. In contrast to light based techniques, where analyses is exclusively performed on the zeroth-order Bragg peak, the use of sub-nanometer wavelengths produces more than six orders of diffraction for line width determination. A linear fit of peak position provides critical dimensions consistent with vendor estimates. The measurements are performed on the unaltered photoresist, free of the need for labeling or intrusive sample preparation techniques. Data are obtained under vacuum, however ambient air studies produced identical



Wavevector, q, of peak position as a function of peak order. Solid line is a linear fit.

values. We note that increased precision is possible as linewidths decrease below 100 nm, allowing more flexibility in technique optimization. Maximum critical dimensions achievable with current SANS technology are ca. 190 nm in line width. The true minimum linewidth is not currently known, however features of sizes less than 10 nm are routinely obtainable. The applicability of SANS for several future nodes of the ISMT Roadmap is therefore assured.



SANS intensity data across range of wavevectors for three different photoresists at optimal exposure conditions. Small changes in patterns produce significant changes in Bragg intensities and position.

■ We have provided the first measurements of sidewall angle. Measurements of a single test pattern have been provided with varying degrees of incidence angle, allowing the reconstruction of the line form from multiple data sets. Data from a set of gratings provided by IBM-Yorktown Heights was measured for several samples imaged under varying conditions of focus. Changes in focus provide changes in line quality without changes in critical dimension.

Comparison of various samples demonstrate the dramatic changes in SANS data from small changes in line shape. Using a simple model of

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Photoresist grating measured by SANS at two different angles of incidence: 0° (open circles) and 15° (closed circles). A simplified model fit of a trapezoidal form is shown with a solid line, fitted to the 0° data.

the line shape as a trapezoid, the sidewall angle is obtained through fitting of the data at multiple angles. Due to the relatively large aspect ratio of the features, projected data changes rapidly with rotation angle, allowing a precision of $< 3^{\circ}$ in sidewall slope using the current simplified model. Ongoing efforts include the development of more complex models incorporating non-linear deviations of sidewall shape. In addition, these studies will be continued on patterns of varying shapes, including contact holes and patterns with corners to estimate changes in pattern shape due to line shrinkage and corner rounding.



Comparison of measurements from first two Bragg peaks of the same sample using two neutron based techniques, SANS and PCD.

• Using the PCD diffractometer at the NCNR, we have determined an upper limit of Bragg peak smearing due to CD fluctuation that is significantly lower than smearing from instrumental resolution effects in the SANS measurement. Results from PCD measurements demonstrate that pattern size fluctuations are still smaller than the resolution provided by the PCD measurement, where the resolution is nearly twice the resolving power of SANS. While the two measurements provide the same estimate of critical dimension, which is dependent only on peak position, the smearing of Bragg peaks due to wavelength resolution issues suggests the lack of capable metrology in this area by SANS. Ongoing investigations using small angle x-ray scattering, where resolving power is an order of magnitude better than the PCD, will provide an additional option in this area.



Fourier transform of AFM image of model photoresist line edge morphology.

• The relevant wavevector range for sidewall roughness has been identified as a range of 0.3 nm⁻¹ to 1.0 nm⁻¹ using AFM. Morphological images collected from a series of model photoresist line edges confirm that this range varies slowly with processing parameters, and this range serves to guide the development of a suitable metrology of sidewall roughness based on scattering methods. The identified wavevector range is significantly higher than those probed in the critical dimension studies, requiring the use of different neutron optics, however the range is well within technical limits of current SANS technology.

Collaborations

NIST Center for Neutron Research, Charles Glinka, John Barker; SANS and USANS measurements.

IBM Yorktown Heights, Dario Goldfarb, Marie Angelopolous, Contributions to Line Edge Roughness.

Shipley, Inc., Patrick Boulton, George Barclay, Photoresist patterning.

Recent Publications

E. K. Lin, R. L. Jones, W. Wu, J. G. Barker, P. J. Boulton, and G. G. Barclay, "Structural Characterization of Deep Sub-Micron Lithographic Structures Using Small Angle Neutron Scattering," Submitted to Proc. SPIE(2002).

E. K. Lin, W. Wu, Q. Lin, and M. Angelopolous, "Feature-Shape and Line-Edge Roughness Measurement of Deep Sub-Micron Lithographic Structures Using Small-Angle Neutron Scattering," Proc. SPIE **4344**, 414 (2001).

W. Wu, E. K. Lin, Q. Lin, and M. Angelopolous, "Small Angle Neutron Scattering Measurements of Nanoscale Lithographic Features," J. Appl. Phys. 88, 7298 (2000).

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Technical Contacts: John Villarrubia András Vladár

"[The] theoretical work on the behavior of the probe-sample interaction has had a profound influence on our ability to quantitatively analyze probe microscope images."

—Joseph Griffith, Bell Labs, Lucent Technologies

"The modeling work ... for electrical CD, AFM, and CDSEM is of value to us ... The current crisis in CD offset uncertainty may be partially answered by this work."

-Anonymous industry feedback to NIST.

Model-Based Linewidth Metrology

Goals

The goal of this project is to address the metrology needs of industry, particularly the U.S. semiconductor industry, for linewidth metrology with uncertainties of a few nanometers.

Customer Needs

"Lithography metrology continues to be challenged by rapid advancement of patterning technology. Critical dimension measurement capability does not meet precision requirements which comprehend measurement variation from individual tool reproducibility and tool to tool matching...CD measurement must be extended to line shape determination." International Technology Roadmap for Semiconductors, Metrology Section, p. 7 (2001).

Due to the changing aspect ratios of IC features, besides the traditional lateral feature size, e.g. linewidth measurement, full three-dimensional shape measurements are gaining importance and should be available inline. Development of new metrology methods that use and take the full advantage of advanced digital image processing and analysis techniques and networked measurement tools will be needed to meet the requirements of near future IC technologies. International Technology Roadmap for Semiconductors, Metrology Section, p. 6 (2001).

"...the exponential rise in value of each nanometer, as nominal gate dimensions shrink, can be estimated... Under these assumptions, the value of CD control for the 180 nm generation of microprocessors exceeds \$10 per nanometer." C.P. Ausschnitt and M. E. Lagus, IBM Advanced Semiconductor Technology Center, Proc. SPIE Vol. 3332, p. 212 (1998).

A feature's width is one of its fundamental dimensional characteristics. Width measurement is important in a number of industries including the semiconductor electronics industry, which had more than \$200 billion in worldwide sales in 2000.¹ As a measure of its importance in that industry, consider that the term "critical dimension" or "CD" is used there nearly interchangeably with "linewidth," and semiconductor device generations are known according to the characteristic width of the features, as in "the 130 nm generation."

Existing linewidth standards are optical photomask standards, the minimum linewidth of which is $0.25 \,\mu\text{m}$ with a combined expanded uncertainty of $\approx 10 \,\text{nm}$ (coverage factor 2). To support present and future semiconductor technologies, industry needs to measure gate widths with total uncertainties, as identified by International SEMATECH, of less than 10 nm and with measurement repeatabilities of 1 nm or better. Neither NIST nor any other national laboratory presently offers a wafer linewidth measurement service or SRM with this level of accuracy.

A line's width must generally be determined from its image. However, the image is not an exact replica of the line. The scanning electron microscope (SEM), scanning probe microscope (SPM), and optical microscope all have image artifacts that are important at the relevant size scales. Physical linewidth determination therefore requires modeling of the probe/sample interaction in order to correct image artifacts and identify edge locations. Barriers to accurate linewidth determination include inadequate confidence in existing models, the complexity and consequent expense of using some models, inadequately quantified methods divergence, and ignorance of best measurement practices.

Technical Strategy

1. The scope of the model-based linewidth metrology project includes the development and improvement of computational models to simulate the artifacts introduced by measuring instruments, inversion of these models (to the extent possible) to deduce the sample geometry that produced a measured image, validation of models by appropriate experiments, development and testing of measurement processes that provide the necessary inputs for model-based deduction of sample width and shape, estimation of uncertainties for the measurement process, assistance to industry linewidth measurement by communication of best practices, and laying of the necessary research groundwork for a future linewidth and/or line shape Standard Reference Material.

NIST is uniquely positioned to execute such a project. NIST is a center of expertise in the instrument models to be tested, with optical,

¹ Semiconductor Industry Association press release, Feb. 5, 2001.



Fig. 1. The SEM image may be calculated for a given edge geometry by using a Monte Carlo algorithm that follows a number of representative electron trajectories.

SEM Monte Carlo, and SPM tip and sample reconstruction models all having been developed at NIST. Also, because NIST's standards function necessitates concern for accuracy, the NIST measurement tools are among the best characterized anywhere. For example, transmission optical measurements can be made here with the same instrument used to calibrate standard reference materials, and scale calibrations can be assisted by the NIST linescale interferometer.

We have been developing a model-based library method of determining line width and line shape from top-down SEM images. The top-down measurement configuration is the one employed by industry CD-SEMs. Edge locations tell us the line's width (the "CD" desired by industry). However, lines with different sidewall geometries appear to have different widths when measured using algorithms that are standard today on CD-SEMs. That is, sidewall variation masquerades as width variation. Accordingly, our method is a model-based algorithm that explicitly accounts for the physics of the interaction of the electron beam with the sample and the effect of sidewall geometry.

The method works like this: A set of parameters for describing edge geometry is chosen. These parameters might be, for example, sidewall angle and corner radius. For a given set of parameter values, the expected image is calculated using a Monte Carlo algorithm that simulates electron trajectories (Fig. 1). This calculation is repeated for other choices of edge parameters at discrete intervals representative of the range of shapes that one is likely to encounter in a measurement. The resulting actual shape / calculated image pairs form a library, or database. To determine



Fig. 2. Concept of metrology using a model-based library. The measured left and right edges are compared to a library of images calculated for a range of possible edge shapes. The shape of the unknown structure that gave rise to the measured image is assigned to be the line shape corresponding to the image that most closely matches the measured one.

the shape of an unknown sample, its measured image is compared to computed images in the database to find the closest match. The corresponding line shape is assigned to the unknown (Fig. 2). In practice there may be more than two parameters, and the library may be interpolated.

In 2001 and early 2002 this new method produced encouraging results for data taken with our laboratory SEM. In the rest of 2002 we will be attempting to implement and validate the method on an industrial CD-SEM. The method has not yet been validated on such instruments, which differ from our laboratory instrument in depth of focus and extraction fields.

Results of this comparison may indicate the need for some changes in the instrument model to accommodate the CD-SEM's differences. Once these changes are implemented, the code will be installed at International SEMATECH.

DELIVERABLES: Stand-alone software to perform off-line model-based shape-sensitive linewidth analysis will be installed at International SEMATECH. 4Q 2002

Such stand-alone software may help interested industrial laboratories to assess the usefulness of this method in an industrial environment. In the long run, however, if the method proves to be useful the most effective transfer mechanism will be to have this method of data analysis become incorporated into the CD-SEM instrument itself by instrument vendors. To that end, the initial



Fig. 3. Design of new linewidth test pattern. The design contains both nested lines and isolated lines with nominal widths varying from 100 nm to 1 μ m. The side-by-side arrangement permits lines of all sizes to be cross-sectioned with the same cut or cleave. Scale patterns above and below the linewidth patterns are measurable with the NIST linescale interferometer to provide a traceable scale.

NIST role will be to publicize to vendors and their potential customers the performance, both strengths and weaknesses, of this method.

DELIVERABLES: Results of a model-based shape-sensitive linewidth measurement system using data from an industrial CD-SEM will be compared to independent measurements of line width and shape. The performance will be assessed and reported. 4Q 2002

Accomplishments

• A new linewidth test pattern (Fig. 3) was designed and fabricated in collaboration with International SEMATECH.

We developed and implemented a number of improvements in the model-based library method for analyzing SEM data and embodied them in software. Improvements include the ability to perform the required non-linear least squares matching of measured results to library results for an arbitrary number of line scans, each containing an arbitrary number of line features in a single fitting operation, separate treatment of instrument parameters (brightness, contrast, and beam size), and the ability to pin parameters that are independently known.

We employed the new analysis method to obtain linewidth and line shape information from top-down SEM images acquired with our laboratory SEM. We compared these results to crosssectional images of the same lines (Fig. 4).

The repeatability of the new method was compared to that of one of the commonly used algorithms employed in industry CD-SEMs. The two methods were used to analyze the same data set. The new method was more than a factor of three better.

• We reported results from our previous year's study to ISMT directly (in the form of a project report that is accessible to member companies via the web). We reported them to the semiconductor metrology community and public generally via oral presentation at the SPIE Micrometrology Symposium and publication in the symposium proceedings.

Collaborations

International SEMATECH, Michael Bishop and Applied Materials, John Swyers; CD-SEM data acquisition.

International SEMATECH, Benjamin Bunday and Michael Bishop; linewidth test pattern sample fabrication.



Fig. 4. Left: Cross section (continuous red line) deduced by model-based method from a top-view image overlaid on a cross-sectional SEM image of the same line. Edge assignments from the cross section image are shown in blue, but are difficult to distinguish at this scale. For this reason the edge areas (inside the yellow boxes) are expanded in the graph on the right. The width difference of 1.4 nm and edge angle differences of 0.1° and 0.2° are within the uncertainty, shown in red, due to line edge roughness. (Figure from Villarrubia et al., *Proc. SPIE* **4689**, 2002, in press.)

Recent Publications

"Scanning electron microscope analog of scatterometry," J. S. Villarrubia, A. E. Vladár, J. R. Lowney, and M. T. Postek, *Proc. SPIE* **4689**, (2002), in press.

"Trial Shape Sensitive Linewidth Measurement System," J. S. Villarrubia, final report to International SEMATECH, December 2001, available at member company web site.

"Shape-Sensitive Linewidth Measurement with the SEM using a Model-Based Library," J. S. Villarrubia, A. E. Vladár, J. R. Lowney and M. T. Postek, SCANNING **23**(2), pp. 90-91 (2001).

"Edge Determination for Polysilicon Lines on Gate Oxide," J. S. Villarrubia, A. E. Vladár, J. R. Lowney and M. T. Postek, Proc. SPIE **4344**, pp. 147-156, (2001)

Thin Film and Shallow Junction Metrology Program

The dimensions of the active transistor areas are approaching the spacing between dopant atoms, the stochastic regime, complicating both modeling and doping gradient measurements. Thin dielectric and conducting films are approaching monolayer thicknesses.

As device dimensions continue to shrink, junctions and critical film thicknesses approach the realm of several atoms thick, challenging gradient, thickness and roughness metrology as well as electrical and reliability characteristics. The gate dielectric, traditionally SiO_2 , will soon no longer be viable. The overall task is to provide suitable metrology and reference materials for thin dielectrics and conducting barrier films, including electrical characterization, gradient, thickness and roughness metrology and overall reliability metrology.

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Two- and Three-Dimensional Dopant Profiling

Goals

To provide industry with the metrology infrastructure needed to measure two- and threedimensional dopant/carrier profiles in the ultrashallow junction regime. The project is divided into two thrusts (SIMS and SCM):

1) Improve the capabilities for compositional depth-profiling by defining optimum procedures for ultra-high depth resolution by Secondary Ion Mass Spectrometry (SIMS), developing depth-profiling reference materials needed by U.S. industry, and improving the uncertainty of implant dose measurements by SIMS.

2) Provide measurement methodologies, theoretical models, and data interpretation software necessary to make the Scanning Capacitance Microscope (SCM) a useful two-dimensional dopant-profiling tool.

Customer Needs

Since source/drain dopant profiles are a critical factor determining the performance of a transistor, dopant profiling has always been needed by the silicon integrated circuit industry. One-dimensional dopant profiles from SIMS or electrical techniques remain an important process control tool. As transistors are scaled to ever-smaller dimensions, the variation of dopant profiles in two- and three-dimensions also begin to influence device operation. Two- and three-dimensional dopant profiles are now needed to validate models of the processes used to produce ultra-shallow junctions and for accurate device simulations.

SIMS is most likely to provide the solution to precision requirements for 1-D dopant concentration measurements. These goals can be achieved by careful control of SIMS depth-profiling conditions and by developing and making available implant reference materials for common dopant elements. Scanning Capacitance Microscopy (SCM) has emerged as a leading contender to provide two-dimensional carrier profiles. Relatively accurate 2-D profiles of the dopant concentration can be obtained when SCM images are combined with SIMS measurements.

Metrology needs for Doping Technology are discussed in the 2001 International Technology Roadmap for Semiconductors on pages 6 and 16 of the Metrology Section. The ITRS requirements are for at-line 2-D dopant profile concentration measurements improving from a spatial resolution of 5 nm and precision of 4 % in 2002 to 1 nm and 2 % by 2016. Complete specifications are given for the short term in Table 100a on page 14 and for the long term in Table 100b on page 15 of the Metrology section. Three-dimensional dopant profiling is identified as one of five difficult challenges < 65 nm beyond 2007, in Table 96 on page 3. Requirements for reference materials and the NIST role are discussed on pp. 23-24, with a specific reference to dopant profiling. Additional discussion about dopant profile fabrication and measurement needs can be found in the Front End Processes and Modeling and Simulation sections.

Technical Strategy

1. Secondary ion mass spectrometry (SIMS) has demonstrated the capability to meet the ITRS dopant profiling requirements for B, As, and P. However, the detailed analytical protocols required to achieve these goals have not been completely specified. We are working in a collaboration with Agere Systems to investigate the parameters that must be controlled to make highly repeatable dose measurements of As and P implants in Si with magnetic sector SIMS instruments.

DELIVERABLES: Develop experimental protocols for high repeatability analysis of As and P implants in silicon. 1Q 2002

2. Shrinking semiconductor device dimensions require increased depth resolution for depth profiling analysis. Typically, the highest depth resolution is achieved by using ultra-low energy primary ion bombardment. However, this capability is not available on most commercial SIMS instruments. In instruments where low energy analysis is available, slow sample erosion rates can result in prohibitively long analysis times. We are exploring an alternate approach that involves using a high energy, focused ion beam to rapidly mill a beveled cross-section in the sample under examination. The "altered layer" produced by the high energy milling beam can be removed by ultra low energy inert gas sputtering in an instrument designed for preparing transmission electron microscopy sections. The cross section prepared in this fashion is then analyzed using high resolution imaging Auger and SIMS analysis.

DELIVERABLES: Develop new 2D image depth

Technical Contact: Greg Gillen (SIMS) David Simons (SIMS) Joseph Kopanski (SCM) Jay Marchiando (SCM)

"SIMS is still a

recognized champion in dopant characterization. However, profiling of active dopant components is a must for good work on dopant characterization today. A progress in "conventional" 2D dopant characterization techniques such as scanning capacitance microscopy (SCM) and scanning spreading resistance microscopy (SSRM) took many by surprise. SCM and SSRM on beveled cross sections promise ITRS desired nanometer and beyond spatial resolution for 2D dopant profiling. Significant progress (has been) made in SCM and SSRM data interpretation."

Vladimir Ukraintsev, Texas Instruments profiling technique for high depth resolution SIMS and Auger depth profiling. 2Q 2002

3. There is considerable recent interest in the use of copper in integrated circuits due to its low resistivity and good electron migration resistance characteristics. With these properties, copper is a good candidate to substitute for aluminum as the interconnection material in the next generation of integrated circuits. However, SIMS depthprofiling of metallic films induces surface topography, which can result in a significant loss of depth resolution. This loss of depth resolution can limit our ability to characterize copper diffusion through metal barrier films and can also make quantification of impurities and intentional additives in copper film problematic. Possible methods to reduce sample roughness include using a very low energy primary ion beam at a glancing angle, rotating the sample stage during depth profiling or using a polyatomic primary ion beam. We are exploring each of these methods in order to determine optimal experimental conditions for depth profiling of metal films.



Atomic force microscope image of sputter-induced topography in a Cr/Ni metal film after SIMS analysis with a 7.5 keV O₂⁺ primary ion beam.

DELIVERABLES: Evaluate methods for reduction of sputter-induced topography in Cu (and other metal films). 3Q 2002

4. Cluster primary ion beam SIMS offers several advantages for the analysis of semiconductor materials. Compared to conventional SIMS analysis using monoatomic primary ions, cluster bombardment SIMS offers improvements in depth resolution; higher sputter rates, and increased sensitivity for some elemental species. Also, greater sensitivity for organic species may greatly increase our ability to detect organic contamination on silicon surfaces. We are exploring various applications of this technique and attempting to develop new, low cost cluster ion beam sources to promote more widespread use of the technique.

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Computer simulation of subsurface damage created by a 25 keV Ga⁺ ion compared to a cluster projectile. Target is a photoresist.

DELIVERABLES: Continue development of cluster SIMS technique for depth profiling of semiconductors. 4Q 2002

5. Development of ion implanted reference materials for the semiconductor industry has been given a high priority by the International SEMATECH Analytical Lab Managers Working group. Previous ion implant NIST standards include B in silicon (SRM 2137) and As in silicon (SRM 2134), which was released in FY 2000. Current efforts are focused on development of a P ion implant standard in silicon.

DELIVERABLES: Development of ion implant reference materials. 4Q 2002

The SCM group is developing tools that are intended to enable scanning capacitance microscopes to function as two-dimensional dopant profiling tools. This work is divided into three tasks: Task 1 is to develop SCM measurement methodologies. Best measurement practices are being determined via collaborative projects with industrial users and research into the physics of the silicon surface preparation. Task 2 is to develop theoretical models of the SCM. The focus of our modeling effort has been to develop 2-D and 3-D finite-element solutions of Poisson's equation for the SCM geometry. Task 3 is interpretation of SCM data and technology transfer. Our expertise with interpreting SCM images is being transferred to industry through our software program FASTC2D. The program features an easy to use interface, rapid profile extraction, and operation in a Windows environment.

The version of *FASTC2D* currently available utilizes a calibration curve, determined from a database of pre-calculated solutions, which can very rapidly determine a 2-D carrier profile from an SCM image. When used in conjunction with SIMS measurements or a reference sample, relatively accurate profiles can be obtained.

6. We are also developing an additional tool for technology transfer: a new generation of test

structures consisting of fully processed and partially processed transistors. These will eventually be produced in sufficient numbers so that every *FASTC2D* user can get a set. A roundrobin set of measurements based on these structures and using an easy to implement measurement procedure, is planned, with devices to be distributed through the SEMATECH 2-D dopant profiling working group.



Prototype known test sample for SCM. Extended length transistor-like devices for easy cross sectioning, containing structures both with and without p-n junctions.

DELIVERABLES: Develop and characterize "known good sample" for distribution with FASTC2D code. 4Q 2002

7. To meet industrial needs for 2-D dopant profiling to the end of the ITRS, requires a physically accurate 3-D model and determination of dopant profile by an inverse solution. We have previously developed a quasi-3-D model of the SCM that predicts the essential behavior of the SCM measurement. However, for the required dopant profiling performance goals, a more rigorous approach is necessary. Towards this end, the finite-element method has been employed to solve Poisson's Equation for the SCM geometry in three dimensions. Accuracy requirements may also force the consideration of quantum mechanical effects, necessitating the solution of the coupled Poisson and Schrödinger Equations. We are developing improved 3-D Poisson solvers using the LaGriT grid management toolbox in collaboration with Los Alamos National Laboratories.

DELIVERABLES: Demonstrate optimized 3-D calculations of the SCM signal across dopant gradients and junctions. 4Q 2003

8. An inverse solution of the SCM requires repeated solutions of the forward problem, i.e. calculation of the SCM signal from candidate carrier profiles. The candidate dopant profile is adjusted until a carrier profile is found that yields a calculated SCM signal that agrees with the measured SCM signal. Project staff have developed a regression procedure to do this with a 2-D solver. The final level of refinement is to use the full 3-D model as the basis of inverse solutions of the SCM. However, the volume of data to be processed and the time required for calculation makes this intractable for routine profile extraction. Practical application requires finding approximations that will achieve the 3-D result without having to complete extensive 3-D simulations.

DELIVERABLES: Have available for distribution to users a computationally efficient method of determining carrier profiles from inverse solutions of SCM based on 3-D models. 4Q 2004

Accomplishments

High Repeatability SIMS Measurements -We collaborated with Agere Systems to investigate the parameters that must be controlled to make highly repeatable dose measurements of As and P implants in Si with magnetic sector SIMS instruments. With optimized settings, we demonstrated the ability to distinguish As or P implant doses differing by 5 % with an RSD of less than 0.5 % in favorable cases. As the level of required precision for SIMS dopant concentration measurements continues to increase, consideration must also be given to more subtle effects that may affect the measurement. In particular, the behavior of the secondary ion detection system (electron multiplier) may become a significant factor. Typically, the detector settings used in routine analyses are those set by the tool manufacturer. However, these are not always optimal for high precision measurements. We have found that the detection sensitivity for elements such as Si and B can change by a factor of 2 depending on the energy of the detected secondary ion and the settings of the detection system. We have developed a system at NIST that allows for reproducible detector setup and optimization. We hope this may allow us to achieve even higher levels of precision for dopant concentration measurements.

■ TOF SIMS Analysis – Dual-beam TOF SIMS depth profiles were carried out on boron delta-doped structures with layer spacings of 15 nm and 7.5 nm and thin oxide dielectric films. Optimal conditions were determined for each sample type. We have found that the current density of the Ga⁺ analysis beam has a profound effect on the measured depth resolution. Smaller raster sizes and corresponding higher analysis beam current densities produce effects that degrade the depth resolution significantly. This effect places limits on the minimum area that can be analyzed by TOF SIMS and also places limits on the concentration of dopants that can be measured with high depth resolution. Additional studies were conducted on the TOF-SIMS to characterize the effect of residual gas adsorption from the vacuum chamber on the measured secondary ion signals from various metal surfaces. Large time-dependent variations in matrix signals were observed from several metal surfaces.

Metal Depth-Profiling - In a study with Advanced Micro Devices, sample rotation SIMS was used to depth profile copper films with minimal beam-induced topography. Optimal experimental conditions for both Cs⁺ and O₂⁺ depth-profiling were determined. Additional studies were conducted using cluster ion beams to reduced sputter-induced topography. SIMS depth profiles of a Cr/CrO, multilayer structure with CrO₂ monolayers spaced 30 nm apart were analyzed using both Cs^{-} and C_8^{-} primary ions while monitoring negative secondary ions. The C_8 shows a substantial improvement in depth resolution. AFM analysis of the crater bottoms demonstrated the rms roughness was 6 times lower using C₈⁻ bombardment.

Bevel Image Depth Profiling - The NIST magnetic sector SIMS instrument has been modified to create custom ion-milled bevel cross sections in multilayer test structures using 19.5 keV O_2^+ bombardment. The use of an oxygen primary ion beam was found to minimize sputter rate variations between layers and to reduce sputter-induced topography. Subsequent removal of the implanted oxygen and subsurface mixed zone is accomplished using low energy Ar⁺ bombardment. This approach may provide a means to produce depth profiles that have higher depth resolution than is possible using conventional SIMS analysis using higher energy primary ion beams.



SIMS Image of As (purple) and O (green) secondary ion signals from a milled bevel in a multilayer AlGaAs/GaAs test structure (82 nm/layer).

Standard Reference Material Ion Implant Development - Radiochemical neutron activation analysis procedures for the certification of phosphorus implant dose have been refined to the point that a relative standard deviation of 1.3 % was achieved in measurements of 12 samples from an implanted wafer. We now estimate that an expanded relative uncertainty of about 1.7 % can be achieved for the certification of dose for a Standard Reference Material (SRM), and plans are on track to produce an SRM in FY02. Three P-implanted wafers and 2 companion blank wafers have been received. One implanted wafer will be diced into 1 x 1 cm pieces for the SRM's, with the others are to be held in reserve. The blank wafers will be used in the neutron activa-



tion measurements to subtract any phosphorus contribution from the impurity in silicon.

Polyatomic Primary Ion Beam SIMS -Studies of polyatomic primary ion beam sources for high depth resolution SIMS dopant profiling are continuing. Collaborations with international SEMATECH have focused on depth-profiling of novel ZrO_2 films on both magnetic sector and TOF-SIMS instruments. A new polyatomic ion source has been designed and constructed that features an externally removable reaction chamber that will allow for use either as a standard duoplastmatron or as an SF_5^+ source. A special lens system is also being ordered that will allow higher cluster ion currents to be extracted from the source.



SIMS depth profile of ZrO_2 oxide layer (6 nm thickness) with SF_s^+ depth-profiling.

Demonstrated a two-dimensional regression procedure to solve the SCM inverse problem of finding the dopant profile from measured SCM signal. This is the first time that an optimized regression procedure has been used to find the SCM inverse solution based on numerical solution of the Poisson's equation. Second generation (inverse modeling) SCM interpretation techniques are a significant improvement over the first generation (calibration curve) techniques. The technique uses two meshes to achieve conversion in only a few iterations (5 steps of the coarse mesh and 2 steps of the fine mesh for a model problem). Inverse solutions determined by this technique fully include the effects of the local dopant gradient and gradient curvature on the SCM measurement of the dopant profile. The method can handle dopant profiles in like type substrates or in opposite type substrates (i.e., across p-n junctions). The procedures developed for the 2-D model are expected to be useful for the 3-D models that are currently under development.

Development of 3-D models of the SCM in collaboration with Los Alamos National Laboratories by applying their LaGriT (Los Alamos Gridding Toolkit) software package. LaGriT is a library of user callable tools that provide 3-D mesh generation, mesh optimization, and dynamic mesh maintenance for finite element methods. Access to such code will enable more efficient 3-D simulations of the SCM measurement across dopant gradients and p-n junctions.

• Compared the response of SCMs using sensors from four different manufacturers and correlated the double zero crossing in SCM signal sometimes observed at p-n junctions with the magnitude of the sensor high frequency voltage. • Development of scanning microwave microscope - Atolytics, Inc. in State College, PA has started the second year of their SBIR phase II contract to develop a commercial version of their scanning microwave microscope. A prototype instrument has been constructed. Manufacturing Instrumentation Consultant Co of Cleveland, OH has been granted an SBIR phase II contract to develop co-axial shielded scanning probe microscope tips. Tips will be evaluated by NIST.

• Application of SCM to Dopant Profiling of High Bandgap Semiconductors - Summer students Brenda Handy, Howard University and Quan Chau, University of California, Berkley, developed a process to prepare cross-sections of SiC for examination with the SCM. Depletion layers and micropipes in SiC have been imaged with the SCM. Work is underway to apply SCM to other high bandgap semiconductors such as GaN.

Collaborations

Agere Systems, Jack Hergenrother, quantitative SCM of vertical replacement-gate transistors.

Agere Systems, Fred Stevie - Dose repeatability of SIMS measurements.

AMD - Metal film depth-profiling by SIMS.

Atolytics Inc, Paul Weiss – Phase II SBIR to develop a commercial version of their scanning microwave microscope

International SEMATECH, Joe Bennett – Thin oxide depthprofiling by SIMS.

University of Seoul, Korea. Dr. Gyoung Ho Buh is a guest researcher in the SPM project for 2002. He is developing methods to optically pump SPMs for carrier lifetime and mobility measurements.

Los Alamos National Laboratory, Denise George and Andrew Kuprat – Development of next generation 3-D Poisson simulators using the LaGrit grid management toolbox.

Manufacturing Instrumentation Consultant Co – Phase II SBIR to develop co-axial shielded scanning probe microscope tips.

Peabody Scientific - lon source development for SIMS.

University of Queensland, Brisbane, Australia. Prof. Tong Yeow was a guest researcher during the summer of 2001. Dr. Yeow learned to operate the SCM and acquired SCM data of NIST test structures for interpretation using Medici and inverse modeling.

Recent Publications

Kopanski, J.J., "Scanning Capacitance Microscopy" in The Encyclopedia of Imaging Science and Technology, J. P. Hornak, ed., John Wiley & Sons, NY (2002).

Gillen, G., "Cluster Secondary Ion Mass Spectrometry," Applied Surface Science, In press (2002). Fahey, A.J., and Roberson, S.V. "Shallow Depth Profiling with ToF-SIMS and the Effect of Analysis Beam Current Density on Depth Resolution," Submitted to J. Vac. Sci. Technol. (2001).

Chi, P. H., Simons, D.S., McKinley, J.M., Stevie, F.A., and Granger, C.N. "High Precision Measurements of Arsenic Implantation Dose in Silicon by Secondary Ion Mass Spectrometry," in Characterization and Metrology for ULSI Technology 2000, D. G. Seiler et al., eds., A.I.P. Press, pp. 682-686 (2001).

Gillen, G., Roberson, S., Fahey, A., Walker, M., Bennett, J., and Lareau, R.T., "Cluster Primary Ion Beam Secondary Ion Mass Spectrometry for Semiconductor Characterization," in Characterization and Metrology for ULSI Technology, D. G. Seiler et al., eds., A.I.P Press, pp. 687-691 (2001).

McBride, D. E., Kopanski, J. J. and Belzer, B. J., "Gate Oxide Formation Under Mild Conditions for Scanning Capacitance Microscopy," in Characterization and Metrology for ULSI Technology, D. G. Seiler et al., eds., A.I.P Press, pp. 657-661 (2001).

Paul, R. L., and Simons, D. S., "Neutron Activation Analysis for Calibration of Phosphorous Implantation Dose," in Characterization and Metrology for ULSI Technology, D. G. Seiler et al., eds., A.I.P. Press, American Institute of Physics, pp. 677-681 (2001).

Rennex, B. G., Kopanski, J. J., and Marchiando, J. F., "FASTC2D: Software for Extracting 2D Carrier Profiles from Scanning Capacitance Microscopy Images," in Characterization and Metrology for ULSI Technology, D. G. Seiler et al., eds., A.I.P Press, pp. 635-640 (2001). Fuoco, E.R., Gillen, G. M., Wijesundara, B. J., Wallace, B., and Hanley, L., "Surface analysis studies of yield enhancements in secondary ion mass spectrometry by polyatomic projectiles," J Phys. Chem **B** 105(18), 3950-3956 (May 10 2001).

Gillen, G., King, L., Freibaum, B., et al., "Negative cesium sputter ion source for generating cluster primary ion beams for secondary ion mass spectrometry analysis," J. Vac. Sci. Technol. A 19(2), 568-575 (Mar-Apr 2001).

Hobart, K. D., Thompson, P. E., Rommel, S. L., Dillon, T. E., Berger, P. R., Simons, D. S. and Chi, P. H., "p-on-n Si interband tunnel diode grown by molecular beam epitaxy," J. Vac. Sci. Technol. **B 19**(1), 290-293 (Jan-Feb 2001)

Krider K. G., and Gillen, G., "High Temperature Materials for Thin-Film Thermocouples on Silicon Wafers," Thin Solid Films **376**, 32-37 (2000).

Thompson, P. E., Hobart. K. D., Twigg, M. E., Rommel, S. L., Jin, N. P., Rger, R., Lake, R., Seabaugh, A. C., Chi, P. H. and Simons, D. S. "Epitaxial Si-based tunnel diodes," Thin Solid Films **380**(1-2), 145-150 (Dec 22, 2000).

Greenberg, R. R., Lindstrom, R. M., and Simons, D. S., "Instrumental neutron activation analysis for certification of ion-implanted arsenic in silicon," J. Radioanal. Nucl. Chem. 245(1), 57-63 (Jul 2000).

Kopanski, J. J., Marchiando, J. F., and Rennex, B. G., Carrier Concentration "Dependence of the Scanning Capacitance Microscopy Signal in the Vicinity of p-n Junctions," J. Vac. Sci. Technol. B 18(1), 409-413 (Jan/Feb 2000).

Marchiando, J. F., Kopanski, J. J., and Albers, J., "Limitations of the Calibration Curve Method for Determining Dopant Profiles from Scanning Capacitance Microscope Measurements," J. Vac. Sci. Technol. B 18(1), 414-417 (Jan/Feb 2000).

Boron and Nitrogen Thin Film and Implant Standards Using Neutron Depth Profiling

Goals

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Develop boron and nitrogen thin film and implant standards to support the needs of the semiconductor industry. There is ongoing activity in the following areas: stability of primary standards, measurements of charged-particle stopping power (dE/dx) to improve quality of depth data, and providing measurement services to customers.

Customer Needs

For many materials processes, knowledge of the quantity and distribution of the constituent elements is needed. Examples include: uniformity of dopant distributions, lateral and longitudinal boron migration, and nitrogen uniformity in GaN/GaAS bilayers.

The dopant concentration needs are discussed in the 2001 International Technology Roadmap for Semiconductors on page 14 and 15 of the Metrology Section.

Technical Strategy

1. Absolute concentration of dopant materials is an important parameter in semiconductor manufacturing. We have a collection of boron and lithium deposits on silicon wafers that have been characterized by Isotope Dilution Mass Spectrometry. We are in the process of recharacterizing these deposits to determine their stability since their manufacture in 1990. We also plan on obtaining new deposits, which will include nitrogen.

DELIVERABLES: Characterize the stability of evaporated deposits in NIST inventory. 1Q 2003

2. Reduce background and increase sensitivity for boron measurements to permit measurement of levels of about 5×10^{15} atoms/cm³. This is about an order of magnitude below our present capabilities. Recent improvements to the cold source at the NIST reactor have given us increased neutron fluences. More attention must now be paid to reducing boron present on apertures, collimators and detector surfaces.

DELIVERABLES: Establish new lower detection limit of boron for customers of 5×10^{15} at/cm³. 3Q 2003

Schematic Sketch of NDP Experimental Arrangement



Schematic of NDP chamber showing detectors at two angles and neutron flux monitor.

Accomplishments

Review of current stopping power data of alpha particles in silicon has shown discrepancies of up to 5 %. Through a combination of new measurements and calculations, new values of the stopping power of alpha particles in the range of interest for boron measurements have been determined. Using a epitaxially grown silicon sample with four boron spikes at different depths, the depths were first measured with SIMS to determine the depths with high resolution. NDP measurements were then made at multiple angles yielding sets of energy loss versus depth spectra. Modeling this data to account for all sources of energy spreading, i.e., straggling, multiple scattering, geometric effects and detector resolution, new values of the stopping power were obtained that are about 5 % below those calculated by TRIM.

Combining two neutron techniques, neutron depth profiling (NDP) and neutron reflectometry (NR), we have studied a silicon wafer coated with a 200 nm thick boron/phosphorus-doped silicate glass (BPSG) film with a 20-nm SiO2 overcoat. The two techniques enable us to determine the density of both layers and the boron content of each layer as well as the surface of the silicon. Results show that there was no boron diffusion out of the BPSG layer.

Technical Contacts: G.P. Lamaze H.H Chen-Mayer

"The NIST NDP facility is a great resource that is unique, and helps us establish the dopant depth profiles. We have in-house methods that are benchmarked with the NDP depth profiling and this facility is critical for such important measurements." Michael Brooks, AMD, Inc.



Boron depth profile obtained directly from NDP, compared with the SLD profile from model fitting to neutron reflectivity data.

■ N solubility in GaAs is very small; phase separation occurs at high levels of N. Therefore, the N concentration is a crucial parameter for establishing characteristics of devices such as long-wavelength lasers and photodiodes. We have made quantitative nitrogen determination in a GaN/GaAs system to understand the CVD fabrication processes and to cross-calibrate SIMS and X-ray diffraction results. In a series of samples with concentrations varying from 0 to 3 mol % GaN, the NDP measured N content differs as much as 13% from the nominal value.



Nitrogen distribution in GaAs/GaN alloy measured by NDP.

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Collaborations

Corning, Kamal Soni; nitrogen distributions in GaN/GaAs bilayers.

AMD, Tim Hossein; boron distributions in ultra shallow doped silicon.

Tufts Univ., Ron Goldner; lithium distributions in battery components.

Recent Publications

Chen-Mayer, H. H., Lamaze, G. P., Coakley, K. J. and Satija S. K., "Two aspects of thin film analysis: boron profile and scattering length density profile," NIMB, in press.

Coakley, K.J., Chen-Mayer, H.H., Lamaze, G.P., Simons, D.S. and Thompson, P.E., "Calibration of a stopping power model for silicon based on analysis of neutron depth profiling and secondary ion mass spectrometry measurements," NIMB, in press.

Gate Dielectric Metrology

Goals

To develop new and improved electrical and optical measurements, models, data, and reference materials to enable better and more accurate measurements of select, critical, thinfilm parameters for silicon Complementary Metal Oxide Semiconductor (CMOS) technology.



Researchers align sample on custom-built high-accuracy spectroscopic ellipsometer.

To address needs in composition and thickness measurements for thin films and interfaces including high and low k materials from gate dielectrics to polymers. This project develops new methods and standards as well as characterizes the accuracy and reliability of existing methods using analytical electron, X-ray, and laser probes. This year the project has four main components:

 Develop Grazing Incidence X-ray Photoelectron Spectroscopy (GIXPS) for the measurement of silicon oxide and oxynitride films and determining the uncertainty of this method.

Characterize the accuracy of High Resolution Transmission Electron Microscopy (HRTEM) for thickness measurements of ultrathin gate dielectrics.

 Develop Nonlinear Optical (NLO) methods for the characterization of thin film interfaces in polymers and simple oxides.

Apply extended x-ray absorption fine structure (EXAFS) and electron energy loss spectroscopy (EELS) to characterize compositional homogeneity and local-scale structure in ultrathin (< 10 nm) dielectric films.</p>

To provide electrical and reliability measurement techniques, data, physical models, and fundamental understanding for ultra-thin silicon dioxide and alternate gate dielectrics in future MOS devices. To increase the understanding of the relationship between the gate dielectric material/interface properties and device electrical and reliability measurements.



Test wafer being loaded on wafer prober for long-term dielectric testing.

Customer Needs

The evolving decrease of the gate dielectric film thickness to an oxide-equivalent value of 1 nm is identified as a critical front-end technology issue in the ITRS. For effective gate dielectric thicknesses below ≈ 2.0 nm, SiO₂ is being replaced, initially by oxynitrides or oxide/nitride stacks, and then by either metal-oxides or metal-silicates. Process control tolerance needs for dielectric thickness are projected to be ±4 % (3 σ), which translates to less than 0.1 nm for 2 nm films. Requirements for process control measurements are a factor of ten smaller still.

Spectroscopic ellipsometry (SE) is expected to continue as the preferred measurement for process monitoring of future gate dielectric films. Industry metrology needs not only improved methods to determine film thickness accurately, but also (1) techniques to determine the structure of the individual films and the interfaces between them; (2) an improved understanding of the relationship between physical, electrical, and optical determinations of film properties; and (3) mechanisms, such as reference materials, for traceability of measurements to NIST to support film metrology.

In order for SE to meet process control requirements of film thickness and unambiguously determine film composition and morphology, the optical properties of these advanced dielectric Technical Contact: James R. Ehrstein Eric Steel Deborah Kaiser John S. Suehle film systems must be characterized and understood.

The microelectronics industry has a high demand for reliable thin film measurement methods that yield composition and dimension information with known accuracy and precision. The metrology section of the ITRS 1999 metrology section clearly states the needs for "reference materials and standard measurement methodology for new, high k gate and capacitor dielectrics with interface layers, thin films such as interconnect barrier and low k dielectric layers, and other process needs. Optical measurement of gate and capacitor dielectric averages over too large an area and needs to characterize interfacial layers. The same is true for measurement of barrier layers."

As semiconductor processing and devices move to smaller dimensions and new materials, the characterization of the device thin film thickness, composition, and interface quality become ever more critical to device operation and reliability.

The ITRS Roadmap for Semiconductors indicates that the equivalent thickness of the gate dielectric will need to be 1.0 nm to 1.5 nm by 2004. Due to increased power consumption, intrinsic device reliability and circuit instabilities associated with SiO₂ of this thickness, a high permitivity gate dielectric (e.g., Si₃N₄, HfSixOy, ZrO₂) with low leakage current and at least equivalent capacitance, performance, and reliability will be required. The physics of failure and traditional reliability testing techniques must be reexamined for ultra-thin gate oxides that exhibit excessive tunneling currents and soft breakdown. Electrical characterization of Metal Oxide Semiconductor (MOS) capacitors and Field Effect Transistors (FET) has historically been used to determine device and gate dielectric properties such as insulator thickness, defect densities, mobility, substrate doping, bandgap, and reliability. Electrical and reliability characterization methodologies need to be developed and enhanced to address issues associated with both ultra-thin SiO₂ and alternate dielectrics including large leakage currents, quantum effects, and thickness dependent properties. As compared to SiO₂, very little is known about the physical or electrical properties of high dielectric constant gate dielectrics in MOS devices. The use of these films in CMOS technology requires a fundamental understanding of the relationship between the gate dielectric material/interface and device electrical and reliability measurements. "The 2001 ITRS identifies the gate dielectric as being one of the most difficult challenges for future device

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difficult challenges for future device scaling, p. 19 of the Front End Processes Section.

Technical Strategy

This project focuses on the issues of (1) developing and providing the basis for traceability to NIST for film thickness measurements, (2) identifying structural models and developing preferred optical index dispersion functions or data for improved ellipsometric analysis of futuregeneration gate dielectric film systems, and (3) correlating optical, electrical, and physical measurements of thickness, composition, and interface structure.

1. Establish and transfer basis of accuracy for thin dielectric films

Industry requirements for future thin dielectric film optical measurements and calibration standards were identified at a NIST-sponsored workshop in FY 98. Core ellipsometry measurement capability is being expanded and strengthened to meet these requirements. An investigation has been started into cleaning and recontamination issues for film calibration standards to determine whether a workshop-expressed goal of 0.015 nm long-term reproducibility of reference artifact values is obtainable. Procedures are being developed to enable traceability of instrument accuracy to NIST for suppliers of secondary thin-film reference materials without requiring volume production of NIST standard reference materials.

DELIVERABLES: Develop and evaluate prototype procedures that will enable traceability to NIST for 1st Level commercial suppliers of reference materials for oxide films down to 2 nm. 2Q 2003

2. Structural and optical models for ellipsometry

A custom-built, high-accuracy spectroscopic ellipsometer with a spectral range of 1.5 eV to 6 eV is being used for this task, and Project staff are working with SEMATECH, IC industry companies, and SRC university staff to obtain and optically characterize advanced oxynitrides, oxide/nitride stacks, and metal oxide and silicate films such as zirconium oxide and hafnium silicate. Characterization will be extended to 8.5 eV to include important optical index structure of these films beyond their bandgaps. This work is directed at determining preferred structural models, spectroscopic index of refraction values, or preferred optical dispersion functions for each of these film systems, and, where possible, the variability of these parameters due to

differences in film fabrication processes. Analysis is done with software developed by NIST for spectroscopic ellipsometry; this software allows maximum flexibility for addition of the latest published or custom-developed optical response models as appropriate for each material system investigated.

Unannealed TiO₂





Fitting the complex ellipsometry spectra of TiO₂ with the recently developed Generalized Tauc-Lorentz Dispersion functions.

DELIVERABLES: Evaluate ellipsometric structural and optical models to determine suitability for process monitoring and control of advanced gate dielectric materials. 4Q 2002

3. Relation between optical, electrical, and physical measurements of thickness

Through collaborations with SEMATECH, IC industry companies, and SRC university staff, as well as with key researchers in other parts of NIST, Project staff are leading and participating in a number of multimethod comparison studies of various ultra-thin gate dielectric films. These multimethod studies utilize techniques such as Xray and neutron reflectivity, high resolution TEM, EELS, angle-resolved XPS, SIMS, C-V and I-V analysis, as well as spectroscopic ellipsometry and reflectivity. The results of these multimethod studies improve the general understanding of state-of-the-art (SOA) measurement capability for very thin films, and also allow Project staff to assess the results of various optical models being applied to the analysis of these films with respect to interface layers and structural composition, morphology, and uniformity. SOA C-V and I-V measurement capability for gate films has been established in the Project. Advanced 1-D analysis software from commercial and university sources has been established and benchmarked to determine the effect of model and algorithm sophistication on oxide film thickness values calculated from C-V and I-V data; extension to 2-D modeling is planned.

DELIVERABLES: Integrate preferred advanced electrical analysis software and structural analyses of high-k dielectrics to improve agreement between electrical and ellipsometric thickness scales. 1Q 2003

4. Many of the existing and innovative analytical procedures for the analysis of thin films such as x-ray photoelectron spectroscopy (XPS), nonlinear optical spectroscopies (NLO), high resolution (HRTEM) and analytical electron microscopy (AEM) with x-ray and electron energy loss spectroscopies, low voltage scanning electron microscopy x-ray analysis, and Auger spectroscopy must be significantly improved to obtain accurate quantitative composition measurements on films with thicknesses below 10 nm. Our goals are to develop the necessary methods, analytical correction procedures, standard data and materials to determine realistically achievable accuracy levels for analysis of thin films by these techniques. Films for these measurement activities are obtained from industrial sources and fabricated in-house by spin coating metalorganic solutions.

Vibrational spectroscopy is a powerful probe of chemical structure. Unfortunately, IR absorption studies of the development of a mature thin-film interface are impossible. The technique is sensitive to the entire film, and the film signal quickly overwhelms that of the interface structure. Second order nonlinear optical techniques such as second harmonic generation (SHG) and sum frequency generation (SFG) are symmetry forbidden in centrosymmetric media such as bulk Si or SiO₂. Thus they are uniquely interface sensitive. SHG studies of SiO₂ films on Si have demonstrated empirical sensitivity to diverse properties of the interface, including strain, roughness, and midgap interface trap density. It is expected that properties such as interface roughness and midgap trap density will be correlated. We are investigating and developing nonlinear optical

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methods as probes of interfaces in semiconductor thin films.

Grazing incidence XPS allows both depth and chemical information to be attained from very thin (less than 10 nm) films. Using a NIST designed, built, and patented device on the Brookhaven synchrotron we have been developing the necessary instrumentation and data interpretation procedures to characterize SEMATECH silicon oxynitride films.

One of the more common methods of evaluating film thickness and composition is through the use of HRTEM and Analytical TEM, respectively. But the uncertainty of these approaches has only recently been looked at quantitatively. Films of dielectric materials grown on silicon were obtained from SEMATECH and analyzed to determine the accuracy of this HRTEM and AEM approach. Comparisons across many methods were made to determine the relative accuracy and precision of these approaches.



Comparison of Si 2p XPS spectra with angle taken at 1823 eV (top) and 1844 eV (bottom) from the same sample. The changes in the spectra reflect changes in the index of refraction across the Si K edge at 1839 eV.

DELIVERABLES: Develop Grazing Incidence Xray Photoelectron Spectroscopy (GIXPS) for the measurement of silicon oxide and oxynitride films and determine the uncertainty of this method. 3Q 2002

5. GIXPS has been employed successfully as a novel means to analyze the depth, density, and chemical composition of the ultrathin dielectric layers being researched for future semiconductor devices. Serious discrepancies exist among the traditional methods of measuring these layers below 10 nm thickness. An important consideration has therefore been a determination of the accuracy of this new method and its potential sources of error. Discrepancies may also exist because of differences between phenomenological and discrete (i.e. atomic) measurements. We have addressed the first question by studying the dependence of the results obtained from the GIXPS method on the accuracy of the physical parameters required as inputs. We are studying the second question by comparison with scattering measurements by short wavelength probes like x-rays and neutrons.

DELIVERABLES: Characterize the accuracy of High Resolution Transmission Electron Microscopy (HRTEM) for thickness measurements of ultra-thin gate dielectrics. 4Q 2002



Molecular model of a gate stack (top) and one frame from an HRTEM simulation movie (bottom) showing changes in apparent thickness with changing imaging conditions.

6. The ability of HRTEM to measure the thickness of sub 4 nm gate dielectric films is in question, pending a quantitative understanding of the errors and uncertainties in the measurement process. The goal of this work is to quantify the accuracy of HRTEM as a technique for measuring the thickness of such films. Because device performance is very sensitive to the dielectric thickness, semiconductor device manufacturers consider this a critical fabrication parameter and are keenly interested in its accurate measurement. To address this problem, a suite of computer modeling tools was developed to build virtual gate stacks and simulate HRTEM micrographs from these stacks. Using these new tools, several hundred images of amorphous SiO_2 films between Si substrates were calculated, covering a range of imaging conditions and sample parameters. Combining the apparent thickness from the micrograph (measured value), and the known thickness from the model (true value) calculation of the accuracy as a function of the input variables is possible. A quantitative understanding of the errors in HRTEM thickness measurements plays an important role in improving the quality and yield of semiconductor electronic device fabrication.

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Vibrationally resonant SFG spectra illustrating changes in molecular orientation, which correlate with atomic oxygen treatment of the substrate and changes in adhesion

DELIVERABLES: Develop a new technique that enables selective measurement of free and buried polymer interfaces by vibrationally resolved sum frequency generation spectroscopy (VR-SFG). 1Q 2003

7. VR-SFG is generally applicable to optical quality films and is demonstrated here for the buried polystyrene/ dielectric interface. Manipulation of Fresnel coefficients through the choice of film thicknesses allows enhancement of the nonlinear optical signal from the desired interface and cancellation of the signal from other obscuring interfacial sources. Our spectra reveal intuitively and through straightforward analysis that the phenyl group orientation for the buried interface is in the opposite direction of the phenyl groups at the top surface. The molecular ordering at the polymer/dielectric interface changes with changing hydrophobicity of the dielectric surface

and correlates to the adhesive strength of the interface.

DELIVERABLES: Measure crystallinity in ZrO₂ films by EXAFS. 1Q 2003

8. EXAFS is a synchrotron x-ray spectroscopy tool that determines the average short-range (about 0.5 nm) local structural information around an atom that has absorbed an x-ray photon. Since the separate local structure around each atomic type present in a material can be measured, the technique is chemically sensitive. We are investigating the applicability of EXAFS to study crystallization and chemical bonding in gate dielectric films.

The strategy of this effort will be to obtain or fabricate both device samples and blanket films, to perform reliability and electrical characterization of the devices, and to collaborate with other researchers to perform analytical characterization. Many issues such as tunnel/leakage current and spatially dependent properties associated with metal oxide and silicate dielectrics are also present in ultra-thin oxide and oxide-nitride stacked dielectrics. Therefore, many of the characterization schemes will first be developed on the simpler ultra-thin oxide and oxide-nitride dielectrics and then be applied to the metal oxide and silicate dielectrics.

There are two main focus areas for this project. The first focus area investigates the physics of failure and the reliability testing techniques for ultra-thin SiO₂ and high dielectric constant gate dielectrics. The physical mechanism responsible for "soft" or "quasi" breakdown modes in ultra-thin SiO₂ films and its implications for device reliability will be investigated as a function of test conditions and temperature. Long-term time-dependent-dielectric breakdown tests will be conducted on SiO₂ films as thin as 1.5 nm at electric fields close to operating conditions. These tests will be used to determine the thermal and electrical acceleration parameters of device breakdown.

DELIVERABLES: Studies of Negative Bias Temperature Instability (NBTI) in p-channel MOSFETs under DC and pulsed operating conditions. 1Q 2003

9. Experiments will be conducted to investigate Negative Bias Temperature Instability (NBTI) in p-channel MOSFET devices. NBTI has become a serious reliability problem in advanced microelectronic devices with ultra-thin gate dielectrics. **DELIVERABLES:** Experimental results of the electron-hole interaction in SiO₂ and the affect on dielectric breakdown. Studies of oxide degradation using high voltage, short time single pulse stressing. 3Q 2002

10. The understanding generated in this research will be used to continue generating standard measurements through a NIST coordinated collaboration between EIA-JEDEC (Electronic Industries Association Joint Electron Device Engineering Council) and the American Society for Testing and Materials (ASTM). Studies on the reliability of high dielectric constant dielectrics such as oxide-nitride stacks will also be performed.

DELIVERABLES: A new standard constant voltage stress test will be developed for determining Time-Dependent-Dielectric Breakdown (TDDB) acceleration parameters in sub 3 nm thick SiO₂ films. The new test will utilize current or voltage noise as breakdown criteria when films exhibit soft breakdown. Such a test will find application by the semiconductor industry when qualifying new manufacturing processes. 4Q 2002



A low-noise (fA), high temperature (300 °C) probe station is used to electrically characterize devices.

The second focus area is to investigate electrical measurement techniques, procedures and analysis associated with devices having thin oxide and alternate gate dielectrics. The electrical measurement techniques that we are investigating include capacitance-conductance characterization, dielectric tunnel and leakage current characterization and defect density measurements such as charge pumping and conductance. Furtherstandard properties and mechamore, nisms/correlations for these dielectrics including defect centers, dielectric constant, defect generation rates, and leakage/tunnel current will be characterized.

High-k gate dielectric films will be obtained from key industrial and university groups. Electrical characterization methodologies will be developed to address various issues associated with these films, including large leakage currents, quantum effects, thickness dependent properties, large trap densities, transient (non-steady state) behavior, unknown physical properties, and the lack of physical models.

Examples of measurement problems that are being addressed include modifying and verifying electrical defect density measurement techniques, including conductance-frequency, capacitancevoltage, and charge-pumping.

DELIVERABLES: Studies of insulator defects and current transport through high-k dielectrics (e.g. HfO₂) including current noise, and the energy distribution of HfO₂ interface states using conductance. 4Q 2002

Accomplishments

Completed extensive upgrade of Master high accuracy ellipsometer that was originally developed for certifying oxide thickness SRMs; the upgrade is intended to enable attainment of improved short-term and long term precision needed to meet industry needs for thin dielectric measurement traceability. Upgrades included a power/frequency stabilized HeNe laser, large area photodiode, new A/D electronics with higher conversion resolution, improved low noise motor drive for the rotating analyzer, and completely rewritten system control and data acquistion software in a format that enables easier maintenance and upgrade. An autocollimator to monitor stability of sample alignment, a temperature readout in the vicinity of the wafer, and monitoring of laser power were also added to enable identification of possible sources of unacceptable measurement variability. Initial tests showed sample alignment to be stable to better than 0.001 ° over many hours, very good short term (1/2 hour time-frame) sample measurement stability, but full-day precision was inconsistent with only partial correlation of variability with temperature. A matrix of additional thermocouples is being added to a variety of points in the ellipsometer to better the pinpoint measurement sensitivity to temperature of various system components.

• A three-pass sample exchange for singlewavelength (SWE) and spectroscopic ellipsometry (SE) measurement of film thickness was completed by NIST and VLSI Standards Inc. The samples were a set of silicon nitride films of

"NIST-traceable standards are increasingly necessary for the precise calibration of diverse metal film thickness measurement tools." Alexander E. Braun,

Metal Film Thickness Standards Enable NIST-Traceable Calibration, Semiconductor International, June 2001

to larger thicknesses. Single moderate wavelength measurements from both labs were in excellent control and showed good agreement of film thickness values. Relatively large discrepancies resulted from the SE measurements at both laboratories, however. This occurred despite careful planning that included such factors as using optical constants for silicon and silicon-nitride at 632.8 nm that were taken from the spectroscopic data base for these materials. This experiment is being used by NIST to develop an understanding of potential pitfalls in measurement exchange programs that are expected to be used as the basis for future programs to offer film thickness measurement traceability to NIST. In the case of the siliconnitride sample exchange, additional investigation of sources of observed SE discrepancies are ongoing.

Several sets of oxynitride and metaloxide/silicate films were measured by spectroscopic ellipsometry in order to determine preferred structural models and optical dispersions for determining film thickness, dielectric function and the possible existence of interface layers. One of these, a set of HfO2 films, fabricated by physical vapor deposition and annealed at temperatures from 500 °C to 700 °C was measured over the range energy range 1.5 eV to 6.2 eV. The 500 °C annealed specimen was fit well with a single Tauc-Lorentz (T-L) dispersion without need to include any surface roughness. However, the films annealed at 600 °C and 700 °C manifested extra structure above the band gap, which required the use of a second T-L dispersion in each case to fit the data adequately. This secondary structure is attributed to the formation of a polycrystalline phase due to elevated temperature. While all samples showed an extended low energy tail of the dielectric function, the tail was shorter for the two higher annealing temperatures. Comparison of the energy gap values for these films as determined by a fitting parameter identified as Eg in the T-L dispersion and also by the regression models of Tauc and of Balog gave inconsistent results. Thus a robust method for band-gap determination for such films is one of the remaining challenges in their optical characterization.



Difficulty determining Optical Band-gap of High-K Materials due to defect related band tail states.

Developed a generalized dielectric dispersion function, called Generalized Tauc-Lorentz (GTL), to expand capability of analyzing the variety of dielectric-function shapes found from spectroscopic ellipsometry measurements of high-K dielectric films fabricated by a variety of processes. The GTL, which is Kramers-Kronig consistent, generalizes a quadratic exponent found in the Tauc-Lorentz (TL) dispersion, allowing it to have values 1 through 4, and includes one additional fitting parameter, Ep, related to the Urbach tail, that is not found in the TL dispersion. Other common dispersion functions, such as TL, Lorentz, and harmonic oscillator, are all special cases of GTL with m=2. The exponent, m, yields four different shape functions for the values 1 through 4. Initial evaluation of possible benefits of having these four shape functions were done by fitting literature data for a-silicon, Si₃N₄ and SiO. The dielectric function data for these materials were shown to be best described by GTLs with m = 2, 3, and 4, respectively. The GTL with m = 1 was found to have a shape function that is well suited to films that have a very sharp absorption edge.

An extensive comparison of the most advanced Quantum Mechanical CV simulators was extended in a number of aspects. A systematic comparison of QM simulators for p-channel (nsubstrate) devices was performed. The number of 1D simulators in the test ensemble was extended to seven. Quantitative differences in the accumulation capacitance with ultrathin gate dielectric films were up to 20 % -similar to previously reported differences for n-channel devices. Some of the underlying physical and modeling differences leading to these differences were identified, "Rudolph Technologies Inc. believes there is a significant need for ... a sub-4nm oxide ... NIST traceable reference material."

Dr. David Leet, Director, Strategic Planning and Advanced Applications, Rudolph Technologies, Inc. investigated and reported; a complex interplay of a number of factors was found.

A method to extend the comparison to include 2D simulators was also investigated and demonstrated. A model test structure was developed, refined and calibrated for use with Medici, a commercial 2-D simulator, to insure that a quasi-1D device was being simulated. Requests have been received for permission to use figures from this work in manuscripts, presentations and a University MOSFET class.

We performed an analysis of the effects of errors in physical input parameters (e.g., x-ray cross-sections, atomic form factors, electron mean free paths) on the results obtained for films of different thicknesses. This allowed us to identify the sensitivity of the results to certain inputs. We were able to test one of these dependences experimentally on the tunable NIST beamline X-24A at the National Synchrotron Light Source. By performing the same photoemission experiment with x-rays of slightly different energies about the K excitation edge of Si, the physical performance of the same sample was dramatically changed. An extensive analysis showed that the two results for the same sample differed by 16 %, which is a good indicator of the accuracy level of the optical parameters used in the determination.

A suite of computer modeling tools was developed to build virtual gate stacks and simulate HRTEM micrographs from these stacks. Using these new tools, several hundred images of amorphous SiO₂ films between Si substrates were calculated, covering a range of imaging conditions and sample parameters. Combining the apparent thickness from the micrograph (measured value) and the known thickness from the model (true value) allows calculation of the accuracy as a function of the input variables. This revealed that measured thickness depends strongly on defocus and astigmatism. Using the Tcl scripting language, a graphical user interface was written to enhance the tools, improve efficiency, and simplify the database interface needed to manage the large amount of data that was generated.

EXAFS: The instrument at beamline X23A2 at the National Synchrotron Light Source in Brookhaven was configured in grazing incidence mode to measure 5 nm thick ZrO₂ gate dielectric films. Two series of films were measured: atomic layer chemical vapor deposited (ALCVD) films annealed at (825 to 900) °C in air, oxygen,

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nitrogen or vacuum (courtesy of J. Chang, UCLA); and spin-coated films annealed in air at temperatures of (200 to 800) °C (NIST). The degree of crystallinity in the films was estimated from the measured Zr-O-Zr bond angle spread $\Delta\theta^2$ in the EXAFS results. ALCVD films annealed at temperatures comparable to the thermal budget required for device fabrication (825 to 900) °C exhibited the same degree of crystallinity, $\Delta\theta^2 < 1^\circ$, regardless of annealing atmosphere. Crystallinity in the spin-coated films (200 °C) to $\Delta\theta^2 > 6^\circ$ for the as-deposited films (200 °C) to $\Delta\theta^2 = 2.4^\circ$ for films annealed above 600 °C.

Test samples: ZrO₂ thin films with thicknesses ranging from 2.5nm to 10 nm were deposited by spin coating metalorganic zirconium acetate-based solutions onto (100) Si wafers. Processes were developed for depositing zircofilms nium silicate from zirconium acetate/tetraethoxysilane and zirconium nitrate/tetraethoxysilane solutions. Silicate films with thicknesses of 10 nm to 15 nm and SiO_2/ZrO_2 ratios of 1:1 to 4:1 were fabricated; the composition of these films is being measured by EELS.

A systematic study of the uncertainties, sensitivity and limitations of capacitance and conductance measurements for extracting device properties and interface state density of metaloxide-semiconductor (MOS) devices with ultrathin (< 3.0 nm) oxides was completed. Capacitance and conductance characterization of metal-oxide-semiconductor (MOS) devices is used to determine properties such as oxide thickness, substrate doping and interface state density. However, with the advent of ultra-thin oxides, effects such as tunnel current, series resistance and quantum mechanical confinement in the substrate require additional consideration. This work provides a detailed analysis of the impact of these effects on parameter extraction using conductance and capacitance characterization of MOS devices with ultra-thin oxides.

Several extensive experimental investigations of the mechanisms responsible for defect generation and breakdown of thin silicon dioxide were performed. The results confirm that breakdown is directly related to the current passing through the dielectric. This confirms that the trap creation model based on energetic electrons creating damage and the statistical behavior of the number of defects at breakdown correctly describes the reliability of ultra-thin SiO₂ at both constantvoltage tunneling and substrate hot-electron

conditions. Additional studies using substrate hot hole injection showed that holes are extremely effective in creating defects in the dielectric. However, these defects are ineffective in causing dielectric breakdown. These results shed doubt on the anode hole injection model for oxide breakdown. An experiment was also conducted to determine if simultaneous hole and electron injection significantly affected time to breakdown in ultra-thin oxide films. The rate of interface state generation as a function of hole charge injected is observed to be similar even though the ratio of hole current to tunneling current is different by two orders magnitude. The rate of bulk defect generation as a function of hole charge injected is observed to be similar even though the ratio of hole current to tunneling current is different by two orders magnitude. The breakdown susceptibility was not effected by the hole to electron ratio even after SHHs were injected to ≈ 2 C/cm² with two different hole to electron ratios.

• A detailed investigation of the reliability of various SiNxOy/SiO₂ (N/O) found that an N₂O anneal of a N/O stack results in device lifetime orders of magnitude greater than SiO₂ of the same equivalent oxide thickness. The results suggest that this lifetime improvement may be due to a high critical defect density at breakdown, low defect generation rate, and low leakage current of the N₂O-annealed stack. In collaboration with North Carolina State University, measurements and modeling were used to determine the impact of stacked dielectrics on charge-pumping measurements to determine interface and near interface defect densities.

The increased occurrence of soft breakdown in ultra-thin SiO₂ films makes reliability characterization very difficult and necessitates the development of more sophisticated techniques to detect breakdown. The effects of stress interruption on the time-dependent dielectric breakdown (TDDB) life distributions of 2.0 nm oxynitride gate dielectric films were studied. TDDB tests using two different breakdown detection techniques were conducted at several gate voltages. Additional tests were conducted using unipolar and bipolar pulsed bias with pulse repetition frequencies up to 100 kHz to study the effects of pulsed bias on the lifetime of 2 nm films. Our results show that: (1) stress interruption longer than 1 s does not affect the defect generation and TDDB life distributions, (2) both current noise and the increase in low-voltage stress-induced leakage current (SILC) detection techniques

provide similar failure statistics for ultra-thin SiO_2 , (3) TDDB lifetime for ultra-thin gate dielectrics under unipolar biased stress does not substantially depend on pulse repetition frequencies less than 1 MHz, and (4) lifetime under bipolar pulsed bias is significantly improved and exhibits a dependence on pulse repetition frequency.

A joint collaboration between NIST and JPL investigates what effect ionizing radiation experienced in deep space missions will have on the reliability of ultra-thin gate dielectrics. It has been previously reported that heavy ion bombardment can cause radiation-induced soft breakdown (RSB) in ultra-thin gate dielectrics. Heavy ion induced soft and hard breakdown were investigated in thin gate oxides (tox≈ 3.0 nm) as a function of Linear Energy Transfer (LET), fluence, and voltage applied during irradiation. It is found that post-irradiation oxide conduction is well described by a quantum point contact model. This new work showed for the first time that heavy ion irradiation can significantly decrease the long-term reliability of ultra-thin oxide films. In fact, only a few heavy ion hits on a "powered down" device can significantly impact device reliability.

Development and characterization of 2 nm thick oxide reference materials, NC State Univ., KLA-Tencor and International SEMATECH; Measurement traceability experiments for SiO₂ and Si₃N₄ film thickness, VLSI Standards Inc. and Rudolph Technologies Inc.

Studies of optical, electrical and physical measurements and properties of oxynitrides and high-K dielectric films, NIST Divisions 837, 842, 852; Univ. Maryland, Univ. Minnesota, NC State Univ., Univ. Texas-Austin, UCLA, Yale Univ; IBM, Solid State Measurements, Texas Instruments, International SEMATECH.

• Development and transfer of ellipsometer techniques and models for analysis, Penn State University and Univ. Maryland.

 Spectroscopic ellipsometry characterization of low-K SiO₂ thin films, Division 854 and International SEMATECH

• We collaborated on measurements on high quality SiO₂/Si samples by x-ray reflectivity at high momentum transfer at the Advanced Photon Source. The Fourier inversion of the reflectivities yields electron density with depth. Similarly, we have measured the neutron reflectivity from the same samples on a cold neutron beamline at the NIST Reactor. We are in the process of extracting mass densities from the data with depth. These determinations allow us to calibrate the electron densities and mass densities used in layer thickness fits by GIXPS, which may differ greatly in thin films from the quoted values in the literature for bulk compounds. This type of verification has not been readily available.

181 Based on simulated HRTEM micrographs at three different objective lens defocus values and three different specimen tilt angles, their results suggested (surprisingly) that minimum contrast defocus yields more accurate film thickness measurements than Scherzer defocus, and that a 25 mrad specimen tilt was more accurate that no tilt. Also, as expected, eliminating the spherical aberration of the objective lens improves the measurement considerably. Because of their sparse sampling of the parameter space (12 simulations to characterize changes in 6 variables), they were unable to quantify the results or confirm these promising anomalies. By using hundreds of simulations chosen to systematically sample the parameter space, this work seeks to extend their result and quantitatively characterize the error of the measurement as a function of the input variables. Optimum conditions for performing gate dielectric thickness measurements can then be chosen with confidence, and the inevitable effects of experimental variation in the measurement process can be assessed and managed.

■ We have demonstrated the use of a multilayer thin film stack to selectively measure the VR-SFG signal from buried interfaces through the manipulation of Fresnel factors. We expect this technique to be broadly applicable to polymer/polymer and polymer/dielectric interfaces. The study of molecular orientation at buried polymer interfaces and its influence on adhesion has been demonstrated. The influence of molecular orientation on the functional properties of a wide range of transparent media can now be explored.

Collaborations

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Advanced Micro Devices, ultra-thin oxide reliability (John S. Suehle)

- Analog Devices, Limerick, Ireland, ultra-thin gate oxide reliability (John S. Suehle)
- CSTL/Process Measurements Division, microhotplate-based sensor arrays (John S. Suehle and Michael Gaitan)

Division 836, 837, 838, Roger Van Zee, et al., spectroscopic Ellipsometry of molecular electronics (Nhan V. Nguyen, Curt A. Richter, and John S. Suehle)

 Divisions 836, 837, 838, Dr. Roger van Zee et al., Molecular Electronics Competence Project (Curt A. Richter and John S. Suehle)

• Fairchild Semiconductor, ultra-thin gate oxide reliability (John S. Suehle)

 George Washington University, microhotplate-based chemical sensors (John S. Suehle)

• Agere Technologies, ultra-thin gate oxide reliability (John S. Suehle)

 Motorola, ultra-thin gate oxide reliability (John S. Suehle)

 N.C. State University (oxynitrides, nitrides, ultra-thin SiO₂), alternative gate dielectrics (Eric M. Vogel)

 National Semiconductor, ultra-thin gate oxide reliability (John S. Suehle)

 Penn State University, ultra-thin gate oxide reliability (John S. Suehle)

• Texas Instruments, electrical and reliability characterization of ultra-thin gate oxides (John S. Suehle and Curt A. Richter)

• Texas Instruments, ultra-thin gate oxide reliability (John S. Suehle)

• The Pennsylvania State University, Molecular Electronics (Curt A. Richter and John S. Suehle)

University of Delaware, alternative dielectrics (John S. Suehle)

 University of Maryland, College Park, ultrathin gate oxide reliability (John S. Suehle)

 University of Maryland, gate dielectric reliability (Eric M. Vogel)

 University of Minnesota, Alternate Gate Dielectrics, 6/1/01 to present (Eric M. Vogel)

Standards Committee Participation

• ASTM F-1 on Electronics, Membership Secretary and Member of Executive Subcommittee, (James R. Ehrstein)

 ASTM F-1 on Electronics, Subcommittee F1.06 on Silicon Materials and Process Control, Chairman and Ballot Coordinator (James R. Ehrstein)
ASTM F-1 on Electronics, Subcommittee F1.06, Section B on Thin Film Characterization, Section Chair, (James R. Ehrstein)

 ITRS Conference, SEMICON West 2001, San Francisco, CA, July 13-18, 2001 (Barbara J. Belzer)

 JEDEC JC14.2 Committee on Wafer-Level Reliability, Dielectric Working Group, Chairman (John S. Suehle)

Recent Publications

Chism, W., Diebold, A., Canterbury, J., and Richter, C., "Characterization and Production Metrology of Thin Transistor Gate Dielectric Films, Solid State Phenomena," vols. 76-77, 2001 pp. 177-180.

Conley, J. F., Jr., J. S. Suehle, A. H. Johnston, B. Wang, T. Miyahara, E. M. Vogel, and J. B. Bernstein, "Heavy Ion Induced Soft Breakdown of Thin Gate Oxides," *IEEE Trans. Nucl. Sci.* Dec. 2001.

Cresswell, M. W., Arora, N., Allen, R. A., Murabito, C. E., Richter, C. A., Gupta, A., Linholm, L. W., Pachura, D., and Bendix, P., "Test Chip for Electrical Linewidth of Copper-Interconnection Features and Related Parameters," Proceedings of the 2001 IEEE International Conference on Microelectronic Test Structures, Kobe, Japan, March 19-22, 2001, Vol. 14, pp. 183-188.

Diebold, A., Canterbury, J., Chism, W., Richter, C. A., Nguyen, N. V., Ehrstein, J. R., and Weintraub, C., "Characterization and Production Metrology of Gate Dielectric Films: Optical Models for Oxynitrides and High Dielectric Constant Films," Materials Science in Semiconductor Processing, Vol. 4., pp. 3-8, 2001.

Nguyen, N. V., Richter, C. A., Cho, Y. J., Alers, G. B., and Stirling, L. A., "Effects of High Temperature Annealing on the Dielectric Function of Ta_2O_3 Films Observed by Spectroscopic Ellipsometry," Applied Physics Letters, Vol. 77, No. 19, 2000, pp. 1-3.

Richter, C. A., Hefner, A. R., and Vogel, E. M., "A Comparison of Quantum-Mechanical Capacitance-Voltage Simulators," IEEE Electron Device Letters, Vol. 22, No. 1, January 2001, pp. 35-37.

Richter, C. A., Nguyen, N. V., Gusev, E. P., Zabel, T. H., and Alers, G. B., "Optical and Electrical Thickness Measurements of Altemate Gate Dielectrics: a Fundamental Difference," Characterization and Metrology for ULSI Technology: 2000, D. G. Seiler, A. C. Diebold, T. J. Shaffner, R. McDonald, W. M. Bullis, P. J. Smith, and E. M. Secula, Eds. (AIP, New York, 2001), pp. 134-139.

Richter, C., Vogel, E., Hodge, A., and Hefner, A., "Differences Between Quantum-Mechanical Capacitance-Voltage Simulators," SISPAD Technical Digest 2001 (2001 International Conference of Simulation of Semiconductor Processes and Devices), 4 p.

E. Landree, T. Jach, D. Brady, A. Karemcheti, J. Canterbury, W. Chism, and A. C. Diebold, "Characterization of Silicon-Oxynitride Dielectric Thin Films Using Grazing Incidence X-Ray Photoelectron Spectroscopy," *Characterization and Metrology for ULSI Technology: 2000 International Conference*, D. G. Seiler, A. C. Diebold, T. J. Shaffner, R. McDonald, W. M. Bullis, P. J. Smith, and E. M. Secula, Eds., CP550, American Institute of Physics (2001) p. 159-163

"Grazing Incidence X-Ray Photoemission Spectroscopy and the Accuracy of Thickness Measurements of CMOS Gate Dielectrics," Terrence Jach and Eric Landree, Surf. and Inter. Anal. 31, 768 (2001).

J.H. Scott, "Characterization of Dielectric Films by Spectrum-Line Imaging, Second International Conference on Microelectronics and Interfaces, Advanced Emerging Metrology and Nanoscience," Emerging Metrology, 2001, Santa Clara, CA, AVS

D.E. Newbury, "Diagnostics for Assessing Spectral Quality for X-ray Microanalysis in Low Voltage and Variable Pressure Scanning Electron Microscopy," Microsc. Microanal. 7 (Supp 2: proceedings) (2001) 702-703.

Richter, C. A., Hefner, A. R., and Vogel, E. M., "A Comparison of Quantum-Mechanical Capacitance-Voltage Simulators," IEEE Electron Device Letters, Vol. 22, No. I, January 2001, pp. 35-37.

Richter, C., Vogel, E., Hodge, A., and Hefner, A., "Differences Between Quantum-Mechanical Capacitance-Voltage Simulators," SISPAD Technical Digest 2001 (2001 International Conference of Simulation of Semiconductor Processes and Devices), 4 p.

Schuster, C. E., Vangel, M. G., and Schafft, H. A., "Improved Estimation of the Resistivity of Pure Copper Electrical Determination of Thin Copper Film Dimensions," Microelectronics Reliability, vol. 41, pp. 239-252, 2001.

B. Wang, J. S. Suehle, J. F. Conley, Jr., E. M. Vogel, C. E. Weintraub, A. H. Johnston, and J. B. Bernstein, "Latent Reliability Degradation of Ultra-Thin Oxides After Heavy Ion and γ -ray Irradiation," 2001 IEEE Integrated Reliability Workshop, Lake Tahoe, CA, Oct. 15-18, 2001.

Suehle, J. S., B. Wang, J.F. Conley, Jr., E. M. Vogel, P. Roitman, C.E. Weintraub, A. H. Johnston, and J.B. Bernstein, "Observation of Latent Reliability Degradation in Ultra-Thin Oxides After Heavy-Ion Irradiation," *Appl. Phys. Lett.*, vol 80, no. 6, (2002).

Suehle, J. S. "Ultra-Thin Gate Oxide Reliability: Physical Models, Statistics, and Characterization," IEEE Tran. On Elec. Dev., Vol. 29, No. 6, June 2002.

Vogel, E. M., and Misra, V., "MOS Device Characterization, in Handbook of Silicon Semiconductors Metrology," A. C. Diebold, Ed. (Marcel Dekker, Inc., New York - Basel), 2001, pp. 59-95.

Vogel, E. M., Edelstein, M. D., and Suehle, J. S., "Defect Generation and Breakdown of Ultra-Thin Silicon Dioxide Induced by Substrate Hot Hole Injection," Journal of Applied Physics, v. 90, no. 5, September 1, 2001, pp. 2338-2347.

Vogel, E. M., Edelstein, M. D., and Suehle, J. S., "Reliability of Ultra-Thin Silicon Dioxide Under Substrate Hot-Electronic, Substrate Hot-Hole, and Tunneling Stress," Microelectronics Engineering 1 (2001), 11 p. Vogel, E. M., Heh, D.-W., and Bernstein, J. B., "Impact of the Trapping of Anode Hot Holes on Silicon Dioxide Breakdown," submitted IEEE Elec. Dev. Lett.

Vogel, E. M., Richter, C. A., and Rennex, B. G., "A capacitance-voltage model for polysilicon-gated MOS devices including substrate quantization effects based on modification of the total semiconductor charge," submitted Sol.-St. Elecs.

Vogel, E. M., Heh, D., and Bernstein, J. B., "Interaction between low energy electrons and defects created by hot holes in ultra-thin silicon dioxide," Appl. Phys. Lett., vol. 80, p. 3343, 2002. Wang, B., Suehle, J. S., Conley, Jr., J. F., Vogel, E. M., Weintraub, C. E., Johnston, A. H., and Bernstein, J. B., "Latent Reliability Degradation of Ultra-Thin Oxides After Heavy Ion and γ -ray Irradiation," 2001 IEEE Integrated Reliability Workshop, Lake Tahoe, CA, Oct. 15-18, 2001.

Cho, Y.J., Nguyen, N.V., Richter, C.A., Ehrstein, J.R., Lee, B.H., and Lee, J.C., "Spectroscopic Ellipsometry Characterization of High-K Dielectric HfO_2 Thin Films and the High-Temperature Annealing on Their Optical Properties," Applied Physics Letters, Vol. 80, No. 7, 1249-1251 (18-FEB-2002).

Chemical Metrology of Materials & Particle Contamination

Goals

Develop methods, standard materials and data for the characterization of the elemental composition, crystallographic phase, and chemical structure of microelectronic thin films and particle contaminants at nanometer spatial resolution. We develop and test X-ray, FEGSEM, TEM, XPS, Auger, SPM and diffraction methods to characterize the chemical composition and phase of microelectronic components and particle contaminants. Standard materials and data are developed to support these methods and enable improved accuracy and applicability of these methods to microelectronic devices.

Customer Needs

The constant introduction of new materials (SiGe, oxynitride, novel high K, low K, Cu, etc.) and decreasing dimension size in semiconductor fabrication cause increasing demands for new, selective, quantitative, interface and thin film metrology tools. Typically, many of these same measurement tools are applied to identify particle contaminants in the Fabs. There is a critical need to attain better speed and accuracy of chemical information from thin and chemically complex layered materials. The development of faster methods with known accuracy and the development of standards to demonstrate and maintain the quality of chemical analysis methods is critical to the continuous advancement of semiconductor technology.

The challenges and needs are outlined in the metrology section of the 2001 International Technology Roadmap for Semiconductors on page 21. "The rapid introduction of new materials, reduced feature size, new device structures, and low temperature processing continues to challenge materials characterization and contamination analysis. Correlation of appropriate offline characterization methods with each other and with inline physical and electrical methods should be accelerated. Use of characterization methods to provide more accurate information such as layer thickness or elemental concentration will continue. Characterization methods will continue to move toward whole wafer measurement capability and clean room compatibility."

Technical Strategy

1. SiGe thin film compositional standards - After the need for SiGe compositional standards was discussed at the 14th Annual Workshop on SIMS in 2001, NIST contacted fabrication and analytical laboratory facilities to develop a reference material using an interactive approach. The typical time-frame for an NIST SRM is many years to develop, characterize, and bring to market. The need for SiGe standards was seen as an immediate need, because the current calibration method of Rutherford Backscatter is only accurate to 5 to 10% relative and this is insufficient for reliable device production. NIST is collaborating with several semiconductor facilities and analytical laboratories to develop a suite of SiGe compositional standard films. Using an interactive data collection mechanism with collaborators and publishing the data on the web, a faster approach to standard materials production is being developed. This will allow materials to be used and compared even while reference data are being developed.

2. XPS Standard Data – chemical characterization using X-ray Photoelectron Spectroscopy (XPS) depends on fundamental data and an understanding of the physics of the x-ray and photoelectron interactions with semiconductor materials.

Standard Reference Database (SRD) 20 provides identification of unknown spectral lines in user measurements, retrieval of data for selected elements, retrieval of data for selected compounds, and retrieval of data by scientific citation.

SRD 82 provides values of electron effective attenuation lengths and related data for AES and XPS. Values of effective attenuation lengths (EALs) are needed mainly for measurements of thicknesses of overlayer films and to a much lesser extent for measurements of the depths of thin marker layers.

NIST is developing a new database to be used for AES and XPS analyses of materials with complex morphologies. This database will access data from SRD 64 and SRD 71 and, with additional data, will enable comparisons to be made of measured and simulated spectra for particular Technical Contacts: E.B. Steel C.J. Powell

"Researchers in the Microanalysis Research Group continue to drive the commercialization of new x-ray detectors for materials microanalysis. The new silicon drift detectors, whose development is being supported and encouraged by the group, will allow unprecedented highcount x-ray detection. The semiconductor industry eagerly awaits the availability of commercial instrumentation, first for laboratory analysis applications, then eventually for online defect identification and classification." Anne Testoni, KLA-Tencor

specimen morphologies and specified analytical conditions.

DELIVERABLES: Develop new database for interpreting XPS and Auger data from complex morphologies. 2Q 2004

3. New X-ray Technology - Silicon Drift Detectors: A prototype of a silicon drift detector energy dispersive x-ray spectrometer (SDD-EDS) developed by Photon Imaging, Inc. of Los Angeles under a NIST Phase II SBIR grant is being tested on a scanning electron microscope (SEM) at NIST. Conventional silicon (lithium) EDS forms the backbone of x-ray microanalysis systems implemented on more than 25,000 SEMs worldwide. Conventional EDS is limited to a maximum count rate of approximately 25,000 per second and is usually cooled with liquid nitrogen. The new SDD-EDS technology is capable of limiting count rates of 1MHz with 150 eV energy resolution and operates at -70 C, which is achieved with Peltier cooling. The SDD-EDS detection area is also physically large. Individual detector chips are 50 mm², and assemblies of multiple chips are possible. The combination of a large solid angle and a high-count rate are expected to lead to increased efficiency for SEM/Xray microanalysis. The high count rate capability of SDD-EDS will be especially important for elemental mapping, where the number of photons counted per image pixel defines the concentration level that can be detected.

DELIVERABLES: Establish feasibility of live-time elemental mapping of particles. 2Q 2003



Silicon drift x-ray detector (highlighted oval) on conventional SEM.

4. New X-ray Technology - Microcalorimeter-

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EDS: The microanalysis laboratory at NIST Gaithersburg is working as a Beta-test site for the NIST-Boulder μ cal EDS system (discussed elsewhere.) The system has been outfitted with a second-generation Cu-Mo thermometer rather than the first-generation Al-Ag. Immediately after installation of the new thermometer, the NIST Boulder staff obtained 7 eV resolution on Al. The NIST Gaithersburg staff was then instructed on the operation and maintenance of the cryogenic systems and the adjustment of the cryoelectronics, including the SQUID array, that are critical to obtaining optimum performance.

The initial thrust of the research for the application of this high resolution x-ray detector is in the development of fundamental x-ray data including x-ray weights of lines and peak shape and energy While the characteristic x-ray energies shifts. above about 3 keV are reasonably well known, the energy and especially the relative intensity of lower energy x-ray lines in L and M shell x-rays are not well known and causes significant uncertainty and bias when analyzing complex thin film The characteristic peak systems, e.g. W-Si. energy can shift and peak shape can change as a function of chemical bonding allowing the possibility of chemical compound identification and mapping using the microcalorimeter. A feasibility study of a new database for chemical x-ray data is being initiated.

The development of these standard x-ray data systems requires that we first establish a reproducible response function in intensity and energy for the detector.

DELIVERABLES: Define microcalonimeter detector response function and stability. 1Q 2003

5. Characterization of particles: We are developing two areas of metrology for particles – quantitative chemical analysis using electron and x-ray spectroscopies and quantifying morphology through image analysis of electron microscope images.

The quantitative elemental characterization and identification of nanometer and micrometer-sized particles is critical to defect control. In the chemical analysis of particles with electron-beam instruments, the size and shape of the particle often results in large analytical errors associated with x-ray emission and absorption. Over the years, several different researchers have developed correction procedures to minimize the uncertainties associated with particle analysis. Although these correction procedures reduce the effects of particle geometry, elemental concentrations determined from the quantitative analysis of particles by these methods are often accompanied by errors on the order of 10 % to 50 % relative compared to 3 % to 5 % relative errors for the analysis of conventional samples. We are investigating the advantages and disadvantages of low voltage electron beam analysis.



Schematic results of Monte Carlo calculation of electron beam interaction with a two micrometer particle sitting on substrateIn addition to using chemical composition to classify particles, the shape and surface texture of a particle can help to classify or identify it and may also be indicative of its chemical composition or the process through which it was created. Shape and texture are used routinely by humans viewing objects, while many image analysis approaches currently only use a handful of parameters, such as roundness or root mean square roughness. Since the fractal dimension of a boundary or surface seems visually related to its roughness or tortuosity respectively, we are investigating the applicability of these dimensions for the description of the shape and texture of individual grains of particulate matter. These physical objects by their very nature do not have true fractal shapes, but we hope that they do exhibit fractal-like behavior in a limited size range (the "local fractal dimension" or LFD). After investigation of some image processing methods in the literature, we have chosen and refined two, to characterize the LFD of the projected boundary of a particle and the LFD of an averaged brightness profile representing the surface. These measurements require the particle to be segmented from background, a tedious task to perform manually and a problematic one to do automatically. We have developed operatoraided segmenting methods that are designed for the image data sets under study.

DELIVERABLES: Distinguish particle morphology, matrix correction procedure and instrumental effects on the elemental analysis of particles 4Q 2003

Accomplishments

• SiGe thin films on Si were received from . Agere and SiGe single crystal wafer reference samples were procured from Virginia Semiconductor. The single crystal wafer material has been characterized for heterogeneity and is intended to act as NIST's primary reference for the thin film analysis. Monte Carlo analysis of experimental design has been completed to determine appropriate conditions for low voltage electron beam analysis of the thin film samples.

During the past year, a new version of the popular NIST X-Ray Photoelectron Spectroscopy Database (SRD 20) was released, the new NIST Electron Effective-Attenuation-Length Database (SRD 82) was released, and work advanced on a new NIST database for Quantification of Electron Spectroscopic Techniques (QUEST).

• This year we established a beta-site for the application of x-ray microcalorimetry to chemical analysis. To characterize the response function of the x-ray detector a calibration glass was developed that has characterstic x-ray peaks at many energies. This allows the energy scale of calorimeter to be calibrated and checked for consistency, efficiency, linearity, etc.



X-ray spectrum of NIST calibration glass

• We tested the Silicon Drift X-ray Detector at high count rates and determined the current limitations of the detector and processing electronics. The maximum usable count rate is now limited to approximately 200,000 counts/sec by the processing electronics and we are determining means of addressing this limit.

• We tested the accuracy of quantitative correction procedure in the SEM as a function of beam voltage for particle analysis. We determined that for some cases the lower voltage can have significantly improved accuracy, but the relative improvement depends on the material.



Plot of the relative errors for particle analyses vs. electron beam accelerating voltage.

■ We developed a set of model fractal particle images on which we tested the accuracy of different approaches to particle outline fractal dimension and determined the best algorithms for the most accurate fractal dimension determination. After determining the appropriate algorithm we incorporated it into our image processing package (<u>http://www.nist.gov/lispix/</u>) along with our newly developed robust segmentation methods for defining the edges of particles in secondary and backscatter electron images. The reliability and applicability were tested for three large particle image data sets.

Collaborations

Agere, Stevie (now at North Carolina State University), McKinley, SiGe thin film standards

Evans Analytical, Buyuklimanli, SiGe thin film standards

Motorola, Christiansen, SiGe thin film standards

Photon Imaging, Iwanczyk, new x-ray detector technology

Recent Publications

Conny, J.M., and Powell, C.J., "Standard Test Data for Estimating Peak-Parameter Errors in X-Ray Photoelectron Spectroscopy. III. Errors with Different Curve-Fitting Approaches," Surf. Interface Anal., 29, pp. 856-872 (2000).

Joy, D.C., and Newbury, D.E., "Low Voltage Scanning Electron Microscopy," Microsc. Microanal. 7 (Supp 2: proceedings) 762-763, (2001).

Newbury, D.E., "Measures for Spectral Quality in Low-Voltage X-Ray Microanalysis," SCANNING, 22, 345-351, (2000).

Newbury, D.E., "Diagnostics for Assessing Spectral Quality for X-Ray Microanalysis in Low Voltage and Variable Pressure Scanning Electron Microscopy," Microscopy and Microanalysis 7, Supp. 2 Proceedings, 762-763, (2001)

Powell, C.J. and Jablonski, A., "Effects of Elastic-Electron Scattering on Measurements of Silicon Dioxide Film Thicknesses by X-Ray Photoelectron Spectroscopy," J. Elect. Spect. & Related Phenomena, 114-116, 1139-1143, (2001). Powell, C.J. and Jablonski, A., "Evaluation of Electron Inealstic Mean Free Paths for Selected Elements and Compounds," Surf. and Interface Anal., 29, 108-114, (2000).

Powell, C.J., Jablonski, A., Naumkin, A.V., Kraut-Vass, A., Conny, J.M., and Rumble, Jr, J.R., "NIST Data Resources for Surface Analysis by X-Ray Photoelectron Spectroscopy and Auger Electron Spectroscopy," J. Elect. Spectros. and Related Phenomena, 114-116, 1097-1102 (2001).

Powell, C.J., and Jablonski, A., "NIST Electron Effective-Attenuation-Length Database, Version 1.0 (NIST Standard Reference Database 82)," Standard Reference Data Program (2001).

Powell, C.J., and Jablonski, A., "Electron Effective Attenuation Lengths for Applications in Auger-Electron Spectroscopy and X-Ray Photoelectron Spectroscopy," Surface and Interface Analysis, (In Press)

Powell, C.J., Conny, J.M., and Jablonski, A., "Some Issues in Quantitative X-Ray Photoelectron Spectroscopy and Auger-Electron Spectroscopy," Proceedings of Symposium on Stateof-the-Art Application of Surf. & Interface Anal. Meth. to Environ. Mat. Inter. In Honor of J.E. Castle's 65th year. (In Press)

Powell, C.J., and Jablonski, A., "Comparisons of Calculated and Measured Effective Attenuation Lengths for Silicon Dioxide over a Wide Electron Energy Range," Surface Science Letters, 488, L547-L552, (2001).

Powell, C.J., and Jablonski, A., "Influence of Elastic-Electron Scattering on Measurements of Silicon Dioxide Film Thicknesses by X-Ray Photoelectron Spectroscopy," Journal of Vacuum Science and Technology A 19(5), 2604-2611 (2001).

Powell, C.J., and Jablonski, A., "NIST Electron Inelastic-Mean-Free-Path Database, Version 1.1," NIST Standard Reference Database 71, Standard Reference Data Program, (2000).

Powell, C.J. and Jablonski, A., "Measurement of Silicon Dioxide Film Thicknesses by X-Ray Photoelectron Spectroscopy," in <u>Characterization and Metrology for Ultra Large</u> <u>Scale Integration Technology -2000</u> 591-595, (2001).

Scott, J.H., "Characterization of Dielectric Films by Spectrum-Line Imaging," Second International Conference on Microelectronics and Interfaces, Advanced Emerging Metrology and Nanoscience, Emerging Metrology (2001).

Small, J.A. and Bright, D.S., "Comparison of High- and Low-Voltage X-Ray Mapping of an Electronic Device," in <u>Proc.</u> of the International Conference on Characterization and <u>Metrology for Ultra Large Scale Integration Technology</u>, AIP 550, Seiler, D.G., et. al., eds. 596-600, (2001).

Small, J.A. and Michael, J.R., "Phase Identification of Individual Crystaline Particle by Electron Backscatter Diffraction (EBSD)," J. Microscopy, Vol. 201, 1, 59-69, (2001)

Thin Film X-ray Metrology for Microelectronics

Goals

Provide the semiconductor industry with high accuracy X-ray based measurement methods, reference materials, and data for the structural characterization of simple and complex thin film structures.

Customer Needs

Thin film thickness, density and interfacial roughness are critical to the performance of conducting and dielectric layers in semiconductor devices. Sensitive and accurate measurement of such properties are needed in the process development phase as well as in subsequent manufacturing practice. In the process development phase the needs are for structural properties that can be associated with the electrical performance characteristics of subsequently patterned device arrays. In the subsequent manufacturing phase the need is principally to calibrate the responses of on-line measurement tools that do not deliver first-principles based data. These tools have been developed to meet the needs for high measurement throughput and compatibility with the production environment. Such tools have material-dependent calibration requirements that lead end users and tool manufacturers to look for alternatives that are less sensitive to materials properties and process variability.

These needs are most practically addressed by the use of well-characterized reference materials whose structural properties are certified by offline measurements using X-ray reflectivity and diffraction in conjunction with robust analysis and well calibrated angle measurement instrumentation

Technical Strategy

The sub-nanometer wavelengths and relatively weak interaction of X-ray probes make them a nearly ideal means for determining the geometry of the thin film and multilayer structures that underlie modern semiconductor manufacturing. Our approach has been to develop advanced metrological capability in this area including high performance instrumentation and advanced forms of modeling and analysis.

1. We have made these capabilities available for applications to a considerable range of structural problems involving metallic interconnect layers, advanced dielectrics, and diffusion barrier films. By responding to currently urgent problems, principally, but not exclusively, mediated through SEMATECH, it has been possible to develop first-hand knowledge of industrial needs as well as of the level of timely responsiveness needed to provide useful input to these problems.

DELIVERABLES: Quantitative measurements of density, thickness, and roughness in thin film semiconductor materials 4Q 2002

2. Our program develops and applies X-ray methods to reveal the microstructure of thin film and multi-layer structures produced by advanced semiconductor manufacturing. We also generate and certify reference structures for the calibration of in-line production tools. The main components of this work are: (a) the development and application of high-resolution X-ray scattering techniques; (b) the production of reference samples of thin film and multi-layer structures; (c) providing a rapid response to urgent problems identified by SEMATECH. Both the details and the areas of emphasis of our program have evolved on the basis of this experience and guidance received during presentations to various specialized groups within the SEMATECH





A high resolution X-ray reflectometry system (shown schematically above and in the photograph below) was designed and optimized for the routine analysis of complex thin film and multilayer structures that are of interest to the semiconductor industry framework. Finally, we are in contact with commercial developers of X-ray instrumentation in order to facilitate interactions with customers through the documentation of best practices and the characterization of reference materials.

DELIVERABLES: Begin developing a knowledge base on the effects of systematic errors on the analysis of high resolution X-ray reflectometry analyses of semiconductor thin film structures. 3Q 2002

3. In addition to the development of experimental approaches, we recognize that there is need for the development of advanced analytical methods for extracting structural information from high resolution X-ray reflectometry data. We are therefore developing new approaches for interpreting X-ray analyses based on a wavelet analysis approach.

DELIVERABLES: Development of a new wavelet-based modeling approach for the determination of thin film structural parameters from X-ray reflectometry data. 2Q 2002

Accomplishments

• High-k dielectric films – The structural characteristics of several HfO₂ and ZrO₂ high-k thin film structures were determined by high resolution X-ray reflectometry followed by computer fitting of the reflectometry scans. The HfO₂ films were well modeled by a thin SiO₂ interfacial layer, a mixed oxide Hf_xSi_{1-x}O₂ with x = 0.5, the main HfO₂ high-k dielectric layer, and a thin, very rough, low density HfO₂ top surface layer. Examples of X-ray reflectometry curves from HfO₂ layers (nominally 4 nm) following post-deposition rapid thermal annealing are shown to the right.

In contrast, with the HfO_2 layers, the ZrO_2 samples were well described by a simpler structure consisting of an interfacial SiO_2 layer, the principal ZrO_2 layer, and a rough top low density ZrO_2 layer. The densities of both the ZrO_2 and SiO_2 were found to be considerably larger than the assumed bulk values.

■ TiNSi diffusion barriers –We have examined a series of TiNSi/Cu metallization systems by high resolution X-ray reflectometry. X-ray methods are particularly useful for the analysis of complex metal systems, because the X-rays can "see" a thin buried layer that lies beneath a much thicker top layer. Data from these samples are shown on the following page; the rapid oscillations seen in the experimental curves arise from the interference of the phases of the scattered X- rays from the thick Cu and the thin underlying TiNSi. Examination of the model fit of the experimental data shows excellent agreement between the two for an assumed structure consisting of a thin (approximately 1 nm) Si_3N_4 layer at the silicon substrate, TiNSi and Cu layer thicknesses of 2.4 nm and 76 nm, and a top copper oxide layer with a thickness of about 3 nm.

■ Wavelet-based analysis of interfacial roughness – A method for analyzing X-ray reflectivity curves from multilayered structures with interfacial roughness using a wavelet transform approach has been developed. By using this approach, we have been able (1) to extract the contribution of a particular rough interface to a specular reflectivity curve, and (2) to determine the root-mean-square amplitude of the roughness of a particular interface independently of the other interfaces in the multilayered structure from the specular reflectivity data. Analytical proce-



National Institute of Standards and Technology



X-ray reflectometry data from TiNSi/Cu samples. Top: Raw reflectometry data from samples deposited at 340°C as a function of TiNSi thickness (nominal Cu thickness 75 nm). Bottom: Companson of experimental data and model fit for 3 nm TiNSi/ 76 nm Cu sample; inset shows detail at low angles.

dures that allow the interpretation of the wavelet coefficients obtained from specular reflectivity curves have been developed. This approach has been successfully applied to experimental reflectivity curves obtained from Cu/Ta, Ta_2O_5/Ta , and Ta_2O_5/Ta_2N bilayer structures; a typical result is shown.

The Consortium for High-resolution X-ray



This wavelet-based analysis of X-ray reflectivity data from a C/Cr/SiO₂ structure allowed information on roughness at each interface to be obtained from specular data.

Calibration Strategies (CHiXCS) - We are establishing a new industrial consortium (the Consortium for High-resolution X-ray Calibration Strategies) to better address the long term needs of users of high resolution X-ray scattering instrumentation in the semiconductor industry. Specific tasks of this Consortium will include (1) developing specified procedures for instrument and sample alignment, and quantitatively assess the effect of alignment and other systematic errors on the accuracy and precision of highresolution X-ray diffractometry and reflectometry measurements; (2) providing to the members of the Consortium documentation with regard to recommended best practices for performing highresolution X-ray diffractometry and reflectometry measurements, and (3) delivering NIST-traceable prototype calibration samples to each consortium member in a timely manner. In anticipation of the experimental work in support of CHiXCS, we have initiated (i) the construction of a new reflectometer that will permit closure calibration of both the sample and detector circles, and (ii) the re-incorporation of an optical angle interferometer onto an existing high resolution double axis diffractometer.

Recent Publications

Prudnikov, I.R., Matyi, R.J. and Deslattes, R.D., "Wavelet Transform Approach to the Analysis of Specular X-ray Reflectivity Curves," *Journal of Applied Physics*, **90**, 3338 (2001).

Deslattes, R.D. and Matyi, R.J., "Analysis of thin layer structures by X-ray reflectometry," *Handbook of Silicon Semiconductor Metrology* (ed. A.C. Diebold), 789 (2001).

Kelly, T.F.; Gribb, T.T.; Martens, R.L.; Larson, D.J.; Tabat, N.; Matyi, R.J.; and Shaffner, T.J., "Local Electrode Atom Probes: Prospects for 3D Atomic Scale Metrology Applications in the Semiconductor and Data Storage Industries," *Characterization and Metrology for USLI Technology 2000* (AIP Conference Proceedings), 550, 620 (2001).

Bowen, D.K. and Deslattes, R.D., "X-Ray Metrology by Diffraction and Reflectivity," *Characterization and Metrol*ogy for USLI Technology 2000 (AIP Conference Proceedings), 550, 150 (2001).

Second Harmonic Generation from the Silicon-Silicon Dioxide Interface

Goals

To develop a better understanding of optical second harmonic generation at the Si/SiO_2 interface, its sensitivity to roughness and to explore the potential of second harmonic generation for interface metrology.

Customer Needs

Feature sizes in semiconductor integrated circuits have been decreasing relentlessly, resulting in remarkable performance gains. As lateral dimensions shrink, the dimensions of gate dielectrics must decrease proportionally. Surface second harmonic generation (SSHG) is an optical technique that is highly surface/interface selective. SSHG has been empirically shown to be sensitive to roughness at the Si/SiO₂ interface. The goal of this project is to obtain a better understanding of the basic physics that gives rise to this sensitivity to roughness. This will give insight into the morphology of the interface and into the potential for SSHG as a measurement tool. Limitation on how thin the gate oxide can be made presents a potential barrier to further reduction in device size by the semiconductor industry. In future generations of integrated circuits (ICs) the gate oxide thickness will be reduced to the point where monolayer fluctuations at the Si/SiO₂ interface will represent a significant percent fluctuation of the total oxide thickness. Hence the industry is in need of a greater understanding of the morphology of the interface. Additionally, method of making in-situ measurements of the interface would be beneficial. SSHG may have advantages over other methods.

Technical Strategy

The SSHG signal from Si/SiO_2 displays resonant behavior due to both features in the bulk band structure and the interface alone. We are studying how this resonant behavior changes with change in surface preparation. Specifically we are looking at samples with different miscut (and hence differing step edge density), different oxidation and different roughness (as characterized by x-ray scattering).

SSHG is a very weak effect because a layer only a few monolayers thick at the interface contribute. To obtain a measurable signal, without having to subject the samples to high average powers or high-energy pulses, we use 100 femtosecond pulses at a repetition rate of 76 MHz. This allows high peak powers to be obtained with a modest average power. Photon counting is used for signal detection. A tunable Kerr-lensmodelocked laser is used as the primary source. To extend the tuning range, an optical parametric oscillator is also employed.



Experimental setup for second harmonic generation

A key challenge is to calibrate for changes in laser average power and pulse width that occur with tuning. The change in pulse width results in a change in peak power, and hence signal strength. To do this, a second reference arm is included in the experiment. The reference arm is virtually identical to the signal arm, but a quartz sample is used. Quartz generates a strong second harmonic signal, which is largely independent of laser tuning. A cross calibration between the signal and reference arms is obtained by installing a quartz sample in the signal arm and measuring the two signals versus tuning. The resulting calibration curve is used to correct all subsequent data.

Accomplishments

Simultaneous measurements of the rotational anisotropy and photon energy have shown that the resonance position can be modified if only a single sample orientation is used. This can change the interpretation of earlier studies of the resonance behavior. The modification of the resonance is expected due to variations in the interface due to roughness.

Examination of the polarization dependence of the SSHG signal on hydrogen terminated and oxidized samples has provided evidence that the SSHG signal is dominated by the modification of the interface bonds due to the presence of oxygen in the oxide layer. By using polarization of the incident pulses and emitted SSHG signal, it is possible to partially separate surface and bulk contributions. Furthermore, the phase of the surface terms relative to the anisotropic bulk terms can be used, effectively using the latter as a reference. The results show that the surface term changes sign between a hydrogen terminated surface and oxidized surface. This shows that the oxidation dramatically alters the surface contribution.

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Collaborations

University of Colorado: Yongqiang An.

Bell Laboratories/Lucent Technologies: Kenneth Evans-Lutterodt

Recent Publications

Y. An and S.T. Cundiff, "Bulk Contribution to Resonant Second-Harmonic Generation at $Si-SiO_2$ Interfaces," presented at Quant. Electr. Laser Sci conference, Long Beach, QWA30 (May 2002).

Interconnect and Packaging Metrology Program

Advances in interconnect and packaging technologies have introduced rapid successions of new materials and processes. Environmental pressures are leading to the reduction and eventual elimination of lead in solder used for attaching chips to packages and packages to circuit boards. The overall task of this program is to provide critical metrology and methodology for mechanical, chemical, metallurgical, electrical, thermal, and reliability evaluations of interconnect and packaging technologies.

The function of packaging is to connect the integrated circuit to the system or subsystem platform, such as circuit board, and to protect the integrated circuit from the environment. The increasing number of input/output (I/O) on circuits with vastly larger scale of integration is forcing ever smaller I/O pitches, the use of flip chip bonding, and the use of intermediary platforms called interposers. The integration of sensors and actuators onto integrated circuits through MEMS technology and the increasing use of low cost integrated circuits in harsh environments is increasing the complexity of the packaging task. Environmental concerns are forcing the need for development of reliable lead-free solder and other low environmental impact packaging materials.

System reliability requirements demand modeling, testing methods, and failure analysis of the integrated circuits before and after packaging. Metrology is a significant component of reliability evaluation.

Goals

This project is developing solutions to metrology issues confronting integrated circuit manufacturers in the area of interconnect metallization. The main effort involves determining the essential process requirements for superconformal filling of high aspect ratio features. For electrodeposition this includes: determining measurement methods for characterizing electrolytes, quantifying kinetics for industrially relevant copper electrolytes, and direct assessment of the efficacy of electrolytes for trench and via filling. This project also seeks to explore the generality of the superconformal filling mechanism for metallizations other than copper and processes other than electrodeposition.

Customer Needs

Increasing information technology requirements have yielded a strong demand for faster logic circuits and higher-density memory chips. The low electrical resistivity of copper and the ability of electrodeposition to "superconformally" fill high aspect ratio features has made electrodeposited copper the interconnect material of choice. To support these efforts the National Institute of Standards and Technology (NIST) has a program focusing on the role of electrolyte additives on the superconformal filling process. Evaluation of prospective electrolytes will be greatly accelerated by NIST's recent development of a predictive capability for describing the influence of additives on superconformal deposition.

Interconnect metallization issues are discussed in the 2001 International Technology Roadmap for Semiconductors on Interconnect Section, page 11.

Technical Strategy

1. The semiconductor industry has steadily worked to reduce interconnect dimensions, while improving their electrical performance. As a result, metallization has changed from sputtered aluminum(copper) alloys to electrodeposited copper. To meet future industrial needs, we have developed the metrology and fully disclosed electrolytes that permit characterization of the ability of generic electrolytes to fill fine features. We are also developing electrolytes and metrology for deposition of advanced interconnect materials such as silver (the only metal with a higher conductivity than copper) as well as alternative processing schemes such as chemical vapor deposition.

DELIVERABLES: We will publish the composition of an electrolyte for superconformal electrodeposition of silver. 3Q 2002

Our publications explain the mechanism behind the process of superconformal "bottom-to-top" filling. They also detail how it can be fully quantified using only experiments with planar substrates.

DELIVERABLES: We will develop software for modeling superconformal filling of vias. 2Q 2002

Our model for the superconformal filling process has been implemented in computer code. This software, capable of predicting the timedependent filling of trenches and vias can be obtained for free from our website http://www.ctcms.nist.gov/~wd15/superfill/super fill.html



Superconformal electrodeposition of copper in vias. After a \approx 70 s incubation period of conformal deposition, rapid bottom-to-top filling occurs. Formation of an overfill bump is visible toward the end of deposition. Technical Contacts: T.P. Moffat D. Josell

"We are very excited about the capabilities of this tool, and we want to put it to use ASAP!!! Yet another example of NIST innovation helping industrial competitiveness!!!"

Dennis Buss, Vice President, Silicon Technology Development, Texas Instruments

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This simulation details the time-dependent filling of a trench (viewed in cross-section). One observes the initial conformal deposition, bottom-to-top superconformal filling, and final creation of an overfill bump. All these phenomena are also observed industrially.

DELIVERABLES: We will publish an analysis quantifying how the mechanism that results in superconformal filling of fine features also yields bright deposits on planar surfaces. 4Q. 2002

2. Our publications note the link that can exist between electrolytes that provide "bright" deposits and those that yield superconformal filling of fine features.



Superconformal electrodeposition of silver in vias. After a ~40 s incubation period of conformal filling, rapid bottom-to-top filling occurs.

DELIVERABLES: We will quantify the impact of both accumulation and consumption of adsorbed catalyst on superconformal copper electrodeposition. 3Q. 2002

3. We have quantified the impact of the catalyst on the superconformal filling process through electrochemical measurements as well as surface studies.



The accumulation of the selenium catalyst on the surface of the silver electrodeposit is indicated by the increase of the selenium Auger signal with deposition time (X-ray Photoelectron Spectroscopy).



The impact of the catalyst accumulation on the silver metal deposition rate is evident in this comparison of the time-dependent plating current (metal deposition rate) and the coverage of the catalyst on the surface.

DELIVERABLES: We will quantify the effect of iodine catalyst on superconformal chemical vapor depositon of copper. 4Q. 2002

Our publications extend the formalism originally developed for electrodeposition to chemical vapor deposition. The results provide a basis for understanding recently reported experimental studies with iodine catalyzed chemical vapor deposition of superconformal copper.

Accomplishments

• We have quantified the kinetics of catalyst adsorption on the electrodeposit surface and the role that this adsorption plays in the feature filling process.

• We have applied this understanding to copper and silver electrodeposition and to copper chemical vapor deposition.

• We have demonstrated and explained superconformal electrodeposition of silver. The model electrolyte developed contains only one additive. We have established the metrology for determining all kinetic parameters required to model superconformal feature filling from studies of deposition on planar substrates.

Collaborations

D. Wheeler, B. Baker, W.E. Egelhoff, Materials Science and Engineering Laboratory. L. Richter and C. Yang, Chemical Science and Technology Laboratory, NIST.

ISMT, Christian Witt; fabrication of patterned substrates.

Motorola, Bradley Melnik; Fabrication of Patterned Substrates.

Recent Publications

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D. Josell, D. Wheeler and T.P. Moffat, "Superconformal Electrodeposition in Vias," Electrochemical and Solid-State Letters 5(4), C49 (2002).

T. P. Moffat, B. Baker, D. Wheeler, J.E. Bonevich, M. Edelstein, D.R. Kelly, L. Gan, G.R. Stafford, P.J. Chen, W.F. Egelhoff, and D. Josell, "Superconformal Electrodeposition of Silver in Submicron Features," Journal of the Electrochemical Society (in press).

D. Josell, D. Wheeler and T. P. Moffat, "Superconformal Deposition by Surfactant-Catalyzed Chemical Vapor Deposition," Electrochemical and Solid-State Letters 5(3), C44 (2002).

D. Josell, D. Wheeler, W.H. Huber, J.E. Bonevich and T.P. Moffat, "A Simple Equation for Predicting Superconformal Electrodeposition," Journal of the Electrochemical Society 148, (12) C767 (2001).

D. Josell, D. Wheeler and T.P. Moffat, "Superconformal Electrodeposition in Submicron Features," 2001 Proceedings Eighteenth International VLSI Multilevel Interconnect Conference (VMIC), 385-390, Nov. 28-29, 2001, Santa Clara, California (2001).

D. Josell, D. Wheeler and T.P. Moffat, "Catalyst Induced Superconformal Filling: Electrodeposition and Chernical Vapor Deposition," Proceedings of Advanced Metallization Conference 2001, Oct. 9-11, 2001, Montreal, Canada (in press). Technical Contacts: Barry J. Bauer Wen-li Wu

continuously delivered

"NIST has

high quality

experimental

measurements in

characterizing low-k

dielectric materials,

new metrologies to

meet our changing

while also developing

needs. The SANS/SXR

become a key metric in

measurements have

our low-k dielectric

characterization and

have also provided a

means for us to

benchmark other

characterization

techniques. The

recently developed

solvent infusion and

moisture adsorption

capabilities and

meaningful

comparisons of

techniques extend the

previous measurement

further enable ISMT to

characterize and make

candidate porous low-

k materials for inter-

level dielectric (ILD)

applications. We look

forward to continued

fruitful collaboration."

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Jeffrey A. Lee, Ph.D.

International

SEMATECH

screening process, and

materials

porosity

Porous Thin Films Metrology for Low K Dielectric

Goals

In this project, we are developing measurement methods of morphological characteristics in porous thin films for low-k dielectric applications. We work closely with industrial collaborators to develop and apply these methods to measurements of newly developed materials destined for integration in the next generation of integrated circuits. The unique measurement methods we apply include x-ray reflectivity (XR), small angle neutron scattering (SANS), Rutherford backscattering spectroscopy (RBS), and forward recoil elastic spectroscopy (FRES). Our efforts focus on two areas, implementing routine measurements of film thickness, coefficient of thermal expansion (CTE), moisture uptake, film connectivity, pore volume, pore size, and matrix density on films under development, and devising new measurement methods to characterize pore size distribution (PSD), pore connectivity, and matrix homogeneity.

Customer Needs

As integrated circuit (IC) feature sizes continue to shrink, new low-k interlevel dielectric materials are needed to address problems with power consumption, signal propagation delays, and cross talk between interconnects. One avenue to low-k dielectric materials is the introduction of nanometer scale pores into a solid film to lower its effective dielectric constant. However, the pore structure of these low-k dielectric materials strongly affects important material properties other than the dielectric constant such as mechanical strength, moisture uptake, coefficient of thermal expansion, and adhesion to different substrates. The characterization of the pore structure is needed by materials engineers to optimize and to develop future low-k materials and processes. Currently, there is no clear consensus among IC chip manufacturers for the selection of a class of material or a processing method of nanoporous films. Candidates include silica-based films, organic polymers, inorganic spin-on materials, chemical vapor deposited materials, and several others. With the large number of possible materials and processes, there is a strong need for high quality structural data to understand correlations between processing conditions and the resulting physical properties.

Technical Strategy

1. The small sample volume of 1 μ m films and the desire to characterize the film structure on silicon wafers narrows the number of available measurement methods. A novel technique has been developed using a combination of SANS, XR, RBS, and FRES to determine important structural and physical property information about thin porous films less than 1 μ m thick deposited on a 1 mm substrate. These measurements are performed directly on films supported on silicon substrates so that processing effects can be investigated.

The elemental composition of the films is determined by RBS for silicon, carbon, and oxygen and FRES for hydrogen. In both techniques, a beam of high energy ions is directed toward the sample surface. The number of scattered particles is counted as a function of their energy. Fits are performed on the scattered peaks to compute the relative fraction of each element. The atomic composition information is necessary to calculate the relative contrast factors for x-ray and neutrons.

The XR experiments are performed at grazing incident angles on a modified to 20 x-ray diffractometer at the specular condition. With the modified configuration, reflectivity fringes can be observed from films up to 1.2 μ m thick. High-resolution XR is a powerful experimental technique to accurately measure the structure of thin films in the direction normal to the film surface. In particular, the film thickness, film quality (roughness and uniformity) and average film density can be determined with a high degree of precision. The CTE is determined from measurements of the film thickness at different temperatures.

The SANS measurements are performed on the 8 m NG1 line at NIST Center for Neutron Research. Up to 10 films are stacked to increase the SANS signal and the samples are placed in vacuum without any obstructions between the sample and the neutron detector. Scattering measurements were performed under ambient conditions to determine the structural characteristics of the pore structure. Measurements were also made on samples immersed in deuterated toluene, a solvent that readily wets the sample. Changes in the scattered intensity after immersion provides a measure of the percentage of pores that are interconnected and accessible to the film surface. The scattering data are analyzed using a simple random two-phase description of the film, the Debye model.



Three thin film measurements that are combined for complete characterization.

DELIVERABLES: Measure 20 films for pore volume, pore size, and matrix density associated with IMST CRADA. 3Q 2002.

2. Toluene infusion XR was done on films that have been measured in vacuum in a conventional way, and then soaked in toluene for several hours. The wet samples are placed in the XR apparatus along with a container of solvent to saturate the atmosphere and to cause capillary action to fill pores of the film. The XR critical edge where adsorption first begins gives an accurate value of the average electron density and hence, the average mass density which is a combination of the walls and the solvent-filled pores. By comparing the results of the sample in air or vacuum with the toluene results, one can calculate the amount of toluene adsorbed, and hence the volume of open pores. Also, XR oscillations at higher angle provide a measurement of the total film thickness before and after exposure to toluene and gives a measure of the solvent resistance and rigidity of the walls.

The toluene infusion results confirm that the open pores of thin films can be filled by toluene supplied by saturated vapor and that XR can accurately measure the amount adsorbed. If the vapor pressure of the toluene or any other condensable solvent can be controlled at a partial pressure, standard porosimetry techniques may be applied to thin films. Data on the amount of solvent adsorption for a series of pressures could be converted to a PSD through the appropriate thermodynamic analysis.



Schematic of the porosimetry measurement, increased solvent vapor pressure fills increased pore sizes.

DELIVERABLES: Complete design and construction of environmental chamber and controller for x-ray porosimetry. 2Q 2002

3. The SANS technique often takes advantage of the ability to change the neutron contrast of a solvent by mixing deuterium for hydrogen versions of that solvent. This technique can be used for characterization of the porous thin films by filling the pores with various mixtures of toluene h_8 and toluene- d_8 . If the pores are accessible to the solvent and there are homogeneous walls, the wall density can be found. If the wall is heterogeneous, the average wall density could be found with information on the extent of heterogeneity also being possible. If closed pores exist that are inaccessible to solvent, closed pore porosity can be determined.

If both the XR porosimetry and the SANS contrast match techniques prove practical, a combination of the two may be possible. A match solvent mixture at controlled vapor pressures would deposit the match liquid in the pores through capillary action. SANS would provide an additional measure of PSD.



Schematic of the SANS contrast match measurement, closed pores cannot be filled by probe solvent.

DELIVERABLES: Develop measurement methods and equipment for SANS contrast match technique and make measurements on IMST samples. 2Q 2002.

4. While very small pores lower the dielectric constant without significantly sacrificing electrical or physical properties, occasionally very large pores or aggregated matrix material can form that have sizes comparable to the film thickness. Such large "killer" pores can cause a chip to fail catastrophically and can potentially be a major source of chip rejection. Killer pores can be studied by the use of electron microscopy, but such methods cannot be used in a routine manner because the field of vision of such techniques is relatively small and an extensive number of micrographs would be necessary to fully examine films. SANS, however, can sample relatively large areas of a film at once. The major difficulty is to obtain data at low enough scattering angles to reveal this information.

The Bonse-Hart-type, perfect channel-cut crystal diffractometer that came into full operation this year at the NCNR extends the measurement range of the SANS instrumentation at the NCNR by more than one order of magnitude, to over 5000 nm. This overlaps the range of the 30-m pinhole collimation SANS instruments so that together they provide continuous coverage of microstructural features over 4 orders of magnitude (~1 nm to >5000 nm). This new capability will be used to measure the limits of "killer" pore detection.

DELIVERABLES: Obtain samples of thin films with "killer" pores and test SANS and USANS methods of detection. 3Q 2002.

Accomplishments

• A CRADA was completed with International Sematech (IMST) in which 18 thin films have been characterized annulally for film thickness, CTE, moisture uptake, film connectivity, pore volume, pore size, and matrix density by XR, SANS, RBS, and FRES. Quarterly reports were delivered on the results and two trips were made to IMST to discuss the findings.

• A CRADA was completed with Rohm & Haas in which 4 thin films were characterized for film thickness, CTE, moisture uptake, film connectivity, pore volume, pore size, and matrix density by XR, SANS, RBS, and FRES. A trip was made to Rohm & Haas to discuss the findings.

A new measurement method has been implemented that utilizes infusion of toluene into the open pores of a film by placing the film into a controlled atmosphere of saturated toluene vapor. All of the connected open pores become filled with liquid toluene through capillary action. The critical edge measured by XR is used to calculate the total mass density and, hence, the total amount of adsorbed solvent and open pore content. This method allows calculation of the total open pore porosity that can be compared to the total combined open and closed pore porosity that is measured by the previous method that uses a combination of XR, SANS, RBS, and FRES.

A contrast match method was developed to provide an independent SANS measurement of pore volume, pore size, and matrix density as well as pore connectivity, and matrix homogeneity. A new SANS cell was designed and constructed that causes solvent adsorption in the pores of thin films by using saturated solvent vapor. A device was constructed to deliver saturated vapor of mixtures of toluene-h₈ and toluene-d₈ at any preprogrammed ratio. The films in the SANS cell become saturated by the vapor and the pores become filled. Several solvent ratios are used and the SANS results of the saturated films along with SANS of the films in vacuum are used to calculate the exact match composition. The match composition is used to calculate the mass density of the matrix material and closed pores. This matrix density measurement is independent of the method that uses toluene infusion XR. The contrast match method offers improved accuracy of the final measured parameters. The matrix heterogeneity and the closed pore content can also be determined by the contrast match method.

Collaborations

ISMT Jeffrey T. Wetzel, Changming Jin, Jeffrey Lee

Rohm & Haas - Nick Pugliano

Dow Chemical - Brian Landes

Lucent - Shu Yang

Dow Corning - Wei Chen, Eric Moyer

IMEC - Mikhail Baklanov

Sandia National Laboratory - Hongyou Fan, C. J. Brinker

University of Michigan - David Gidley

Recent Publications

Bauer, B.J., Lin, E.K., Lee, H-J., Wang, H. and W, W-l, "Structure and Property Characterization of Low-k Dielectric Porous Thin Films," J. Electronic Materials, 30(4), p. 304 (2001). Wu, W. L; Wallace, W. E.; Lin, E. K.; Lynn, G. W.; Glinka, C. J.; Ryan, E. T., and Ho, H. M., "Properties of Nanoporous Silica Thin Films Determined by High-Resolution X-Ray Reflectivity and Small-Angle Neutron Scattering," Journal of Applied Physics, 87(3):1193-1200 (2000).

Lin, E. K., Lee, H. J., Bauer, B. J., Wang, H., Wu, W. L., and J. T. Wetzel, "Structure and Property Characterization of Low-k Dielectric Porous Thin Films Determined by X-ray Reflectivity and Small-angle Neutron Scattering," in Low Dielectric Constant Materials for IC Applications, edited by P. S. Ho, J. Leu, and W. W. Lee, Springer Publishing, Inc. (2001).

Yang, S., Mirau, P., Pai, C. S., Nalamasu, O., Reichmanis, E., Lin E. K., Lee, H. J., Gidley, D. W., and J. N. Sun, "Molecular Templating of Nanoporous Ultra Low-Dielectric Constant (\approx 1.5) Organosilicates By Tailoring the Microphase Separation of Triblock Copolymers," *Chem. Mat.*, 13, 2762, (2001).

Lee, H. J., Lin, E. K., Wu, W. L., Fanconi, B. F., Liou, H. C., Lan, J. K., Cheng, Y. L., Wang, Y. L., Feng, M. S., and C. G. Chao, "X-ray Reflectivity Measurements of N_2 Plasma Effects on the Density Profile of Hydrogen Silsesquioxane Thin Films," *J. Electochem. Soc*, 148, F195 (2001). Kohdoh, E., Baklanov, M. R., Lin, E. K., Gidley, D. W., and A. Nakashima, "Comparative Study of Pore Size of Low-Dielectric Constant Porous Spin-on-glass Films with Different Ways of Nondestructive Instrumentation," *Japanese Journal of Applied Physics*, 40, L323 (2001).

Bauer, B. J.; Lee H. J.; Hedden, R. C.; Liu, D. W.; and Wu, W. L. "Pore Size Distributions in Low-k Thin Films by X-ray Reflectivity and Small Angle Neutron Scattering," Proceedings of Ultra Low k Workshop (2001).

Lee, H. J., Lin, E. K., Wang, H., Wu, W. L., Chen, W., and T. A. Deis, "Characterization of Porous Low-k Dielectric Thin Films Using X-ray Reflectivity and Small-angle Neutron Scattering," *Proceedings of IITC 2001*, (2001) in press.

Lin, E. K.; Lee, H. J.; Wang, H., and Wu, W. L.,"Structure and Property Characterization of Low-k Dielectric Porous Thin Films Determined by X-ray Reflectivity and Small-Angle Neutron Scattering," Proc. of the 2000 Intl. Conf. on Characterization and Metrology for ULSI Technology (2000).

Lin, E. K.; Wu, W. L.; Jin, C., and Wetzel, J. T., "Structure and Property Characterization of Porous Low-k Dielectric Constant Thin Films Using X-ray Reflectivity and Smallangle Neutron Scattering," Proc. of the Materials Research Society Meeting. (2000).

National Institute of Standards and Technology

Technical Contact: Michael Janezic Dylan Williams Pavel Kabos

"The high frequency measurements performed at NIST complement the SEMATECH DC characterization and provide the effective dielectric constant over a broad frequency range...Since high performance microprocessors have broken the 1 GHz barrier, it is extremely important that new interconnect materials and structures be characterized at high freauency." Robert Haveman

International SEMATECH

Interconnect Dielectric Characterization Using Transmission-Line Measurement

Goals

We develop and disseminate methods to accurately measure the high-frequency dielectric properties of low-k thin films from easy-toperform *insitu* transmission-line measurements. This project brings together the NIST Electromagnetic Properties of Materials Program and the NIST High-speed Microelectronics Program into a collaborative effort with International SEMATECH and manufacturers of low-k materials to develop methods for determining the dielectric properties of low-k thin films.

In this work, MMIC probing techniques are used to measure the capacitance and conductance per unit length of small printed transmission lines in which the materials to be characterized are incorporated. The dielectric constant of the dielectric thin films and the conductivity of the metals used in the lines construction are subsequently derived over broad frequency ranges.

Customer Needs

In order to improve the electrical performance of interconnects, the semiconductor industry is replacing traditional silicon dioxide thin films with lower permittivity (low-k) thin films. Reducing the permittivity of the dielectric separating the interconnects decreases the parasitic capacitive effects. As a result, smaller interconnects that operate at higher frequencies are feasible. Although many candidate low-k thin film materials exist, the permittivity of many of these new materials remains relatively unknown, especially at high frequencies.

The 2001 Semiconductor Industry Association's (SIA) International Technology Roadmap for Semiconductors identifies the development and characterization of low-k dielectrics as a critical component in the drive to increase interconnect performance. On page 9 of the Interconnect Section it states, "*The effective permittivity encountered by signal in the interconnect structure is the most important parameter*..."

Technical Strategy

Our primary goal is to continue to develop and disseminate the measurement methodology based on single transmission line measurements for determining the dielectric



Figure 1 Typical cross-section of a microstrip transmission line incorporating a low-k thin film.

constant of low-k thin films. An important component of this is to provide measurement services to the semiconductor industry to enable them to evaluate the high-frequency electrical performance of new low-k materials.

Another important issue related to interconnect performance is the possible anisotropy of new low-k materials. To address this issue, we have designed coupled, transmission-line test structures that incorporate the low-k thin film. Broadband measurements of these structures, in addition to the single, transmission-line test structures will allow us to calculate the permittivity of the low-k material as a function of the electric field orientation. An added benefit of characterizing the coupled transmission lines is that they will also provide information about the overall electrical behavior of adjacent interconnect lines.

DELIVERABLES: Improve accuracy and extend frequency range of permittivity measurements using single transmission lines. 3Q 2002

In collaboration with International SEMATECH, we are designing a new set of microstrip transmission-line test structures that will enable us to improve the measurement accuracy. In addition to designing new test structures, we have also upgraded our on-wafer network analysis equipment to extend our frequency range to 110 GHz.

DELIVERABLES: Disseminate measurement method to industry. (Ongoing)

Through publications, measurement software and presentations at International SEMATCH Technical Advisory Boards, we are providing the semiconductor industry with the necessary tools to determine the electrical characteristics of low-k thin films.

DELIVERABLES: Provide measurement services to low-k material manufacturers. (Ongoing)

With expertise in on-wafer network analysis and material characterization, we can offer an independent and unbiased measurements service to low-k material manufacturers.

DELIVERABLES: Design and fabricate coupled transmission-line test structures for evaluation of low-k dielectric anisotropy and electrical performance of adjacent interconnect lines. 4Q 2002

In collaboration with International SEMATECH, we are developing a method to measure possible anisotropy of low-k thin films. Although measuring the electrical properties of the thin-films is the primary focus, we will also be able to provide measurements on the electrical behavior of coupled interconnects.

Accomplishments

• Low-k Material Measurements – In collaboration with International SEMATECH, we measured the dielectric constant of various candidate low-k thin films over a frequency range of 50 MHz to 40 GHz using transmission-line test structures. An example of a typical test structure cross-section is shown in Figure 1. We show in Figure 2 dielectric constant results for a few of the different classes of low-k materials we characterized.

Four-port Microwave Probe Station Construction – The High-Speed Microelectronics Project constructed a four-port microwave probe station including automated measurement software. With this probe station and software, we will be able to characterize the properties of coupled interconnect lines, including the dielectric properties of the low-k thin film separating the coupled lines.

Microwave Probe Station Upgrade – We upgraded our microwave probe station and acquired a high-frequency network that will enable us to perform dielectric constant measurements from 50 MHz to 110 GHz. In addition to a larger frequency range, the microwave probe station has an environmental chamber that will allow us to make dielectric constant measurements as a function of temperature and humidity. • Coupled Transmission-Line Test Structures -In collaboration with International SEMATECH, we have designed a set of coupled transmissionline test structures. These structures will enable us to determine the level of anisotropy of low-k thin films as well as provide valuable data on the electrical performance of adjacent interconnect lines.



Figure 2 Dielectric constant measurements of low-k thin films.

Collaborations

International SEMATECH

Dow Chemical

Texas Instruments

Recent Publications

M. D. Janezic, D.F. Williams, V. Blaschke, A. Karamcheti, C. S. Chang, "Permittivity Characterization of Low-k Thin Films from Transmission-line Measurements," (accepted by IEEE Transactions on Microwave Theory and Techniques).

U. Arz, D.F. Williams, D.K. Walker, H. Grabinski, "Accurate Electrical Measurement of Coupled Lines on Lossy Silicon," 9th Topical Conference on Electrical Performance of Electronic Packaging, pp. 181-184, Oct. 23-35, 2000.

D.F. Williams, J. E. Rogers, C.L. Holloway, "Multiconductor Transmission-Line Characterization: Representations, Approximations, and Accuracy," IEEE Transactions on Microwave Theory and Techniques, vol. 47, no. 4, pp. 403-April 1999.

D. F. Williams, M. D. Janezic, A. Ralston, S. List, "Quasi-TEM model for coplanar waveguide on silicon," 1997 EPEP Conference Digest, pp. 225-228, Oct. 27-29, 1997.

M. D. Janezic and D. F. Williams, "Permittivity Characterization from Transmission-Line Measurement," IEEE International Microwave Symposium Digest, vol. 3, pp. 1343-1345, June 10-12, 1997.

Wire Bonding to Cu/Low-k Semiconductor Devices

Goals

The overall objective is to determine the best process method/top coating and support structures for wire bonding to Cu-Low-K chips. A two step gold deposition system is being developed and some thin inorganic films are also being studied as top-coating surfaces to prevent oxidation during bonding.

Customer Needs

The advent of copper metallization semiconductor chips has resulted in a requirement to wirebond interconnect them in a manner similar to that used for 65 billion ICs. The process should be invisible to the current wire bonding machines. However, the copper bond pads oxidize, requiring a protective/bondable coating. When low-modulus low-dielectric materials lie below the pad, a support structure is necessary to prevent damage to the interconnection/dielectric layers. There are many approaches to solving these problems; the NIST program is attempting to optimize and develop new solutions where necessary.

Technical Strategy

1. One approach to protecting the copper is to coat the bond pads with a bondable gold layer. For this approach the first objective is to determine the diffusion coefficients of copper through gold, because Cu can diffuse to the surface and will oxidize, preventing a good bond. Literature values on various gold platings are contradicting and are being measured using deposits on actual damascene-process copper pads. A more classical approach, but also a more difficult process, using SIMS has been proposed. We have developed a two step (immersion + auto-catalytic gold) deposition process over the copper-LoK chips. This will be pursued at NIST. Even without the actual diffusion coefficients, a pragmatic approach is being carried out by heating gold coated samples and doing extensive wire bonding and evaluating with ball shear tests. A subset of this will be to determine the minimum thickness of gold necessary to prevent copper diffusion/oxidation in normal bonding/processing temperatures. At the same time several inorganic coatings for protection are being evaluated. Sandia has applied thin deposited SiO2 coatings on the copper wafers and they were evaluated. Results so far indicate that all of our coatings are nonuniform, but bonding did occur on the better pads. This evaluation is continuing, possibly by depositing a thick, uniform coating and then etching thinner.

2. Another objective is to measure the nanohardness and modulus of the (damascene) copper in order to optimize bonding, [hardness should be minimized (80-100 Knoop)]. This is being accomplished with a series of annealing experiments made with copper chips, and pragmatically verified by actual bonding experiments. Values of measured nanohardness have been dependant on the annealing gas (argon is best) and have been as low as 60 GPa (about 120 unannealed) and the modulus as low as 20 GPa.

Problems have occurred when sawing the bare copper chips in which the saw particles stick to the bare copper. Several approaches to curing this problem have been pursued. Copper damascene process samples have been supplied by International SEMATECH for this effort.

DELIVERABLES: Problems with the two step Au deposition will be solved. Some pad lifting during Au deposition will be studied and an understanding obtained. The desired thickness of gold deposition will be determined, and hardness and modulus studies completed.

Accomplishments

• One paper published, entitled "Wire Bonding To Advanced Copper-Low-K Integrated Circuits, the Metal/Dielectric Stacks, and Materials Considerations," by George G. Harman and Christian E. Johnson, Proc. 2001 IMAPS Symposium, Oct 9-11, 2001, Baltimore, MD, pp. 484-491. This paper won an award as an outstanding paper in the Symposium.

• The two step non-contact deposition process has been developed. However, there is a slight (very thin) deposition over the entire chip and the desired thick one on the Cu. We think that it is due to trace amounts of the first solution left on the entire surface, which catalyzes the second solution, leaving a thin deposit. We are pursuing a simple cleaning step after the first deposition.

Technical Contacts: G. G. Harman C. Johnson

Solders and Solderability Measurements for Microelectronics

Goals

Solders and solderability are increasingly tenuous links in the assembly of microelectronics as a consequence of ever shrinking chip and package dimensions, the broadening use of flip-chip technology, and the movement toward environmentally friendly lead-free solders. To support needs in this area, the goal of this project is to provide data and materials measurements of critical importance to solder interconnect technology for microelectronics assembly.

Customer Needs

The U.S. microelectronics industry has clearly articulated measurement needs for solderability and assembly, especially for Pb-free solders. For example, the urgency for materials data for Pbfree solders has been specified in the 1999 and 2001 ITRS, 2000 NEMI, and 2000 IPC Lead-Free Solder Roadmaps. Pressure from the European Union and the Japanese consumer product market to produce lead-free microelectronics continues to increase. In addition, the lack of understanding and control of current standard solderability measurements has inhibited the development of improved measurements necessary for new solders and for new packaging schemes. These industrial needs are addressed under this NIST project.

Additional needs have been identified through participation in the National Electronics Manufacturing Initiative (NEMI) working group on Pb-free solder alloys. It was learned that significant industrial problems had arisen due to contamination of Pb-free solders by the Pb contained in the protective solder coatings that are used on Cu leads. The protective layer deposited on Cu is usually referred to as a "pretinned" coating and is required to maintain solderability of the component during storage prior to assembly. Pb-free coatings of nearly pure tin tend to grow "whiskers," however, which can cause shorts across leads. Thus the development of Pb-free alloy platings to replace Pb-containing protective layers is considered important, and tests which ascertain the tendency to form whiskers are much needed.

Technical Strategy

We are providing the microelectronics industry with measurement tools and data to address solder interconnect problems. A thermodynamic database has been publicly distributed for modeling lead-free solder systems. We also work closely with industry groups on measurement tools needed for development of lead-free solders for use in harsh environments, and provide guidance for adoption of these solders into assembly processes through work with industrial standards organizations.

We will continue working with the NEMI consortium to establish suitability of particular leadfree solder compositions. In addition, solderability tests will be developed working with the IPC lead-free solder sub-committee. Databases for phase diagrams and thermodynamics critical to solder development and for mechanical properties of solder will be expanded and distributed via the web. In addition, a much-needed guide to interpretation of thermal analysis data will be produced.

It is well known that the use of pure Sn protective deposits has serious problems. Sn whiskers (1 µm diameter and several mm long) can grow from the Sn plate and cause electrical shorts and failure (see figure). Historically Pb was added to Sn plate to prevent whisker growth as well as to lower cost. In the current research program, it was decided to focus this project on Pb-free Snrich deposits with alloying additions that would retard whisker formation. The Sn-Cu system was chosen, as the Sn-Cu-Ag is likely to be the Pbfree bulk solder of choice for industrial application. The basic idea is that the substitution of a different solute for Pb in the Sn-rich deposit will also retard whisker growth. A detailed microstructural comparison of deposits with high and low whiskering tendency is being conducted. Sn grain size, shape, preferred orientation and residual stress will be measured. The dominant mechanism(s) for whisker growth will be determined.

DELIVERABLES: Develop wetting balance test procedure to modify industry standard (IPC/EIA-J STD-002A). 3Q 2002.

Technical Contacts: Frank W. Gayle Carol Handwerker Maureen Williams Christian Johnson

"As a result of NIST's involvement, I feel NEMI has been successful in responsibly leading the effort to understand the implications of leadfree assembly in a way that is benefiting the entire electronics assembly industry."

-- Edwin Bradley, Motorola and National Electronics Manufacturing Initiative **DELIVERABLES:** Perform wetting balance tests for the IPC solderability task group pilot study on Pb-free surface finishes and components. 4Q 2002, IPC solder study).

DELIVERABLES: Add Sb-containing systems to the current thermodynamic database (Sn-Ag-Bi-Cu-Pb) for solders. 3Q 2002.

DELIVERABLES: Develop an easy-to-use interface for phase equilibria software for the calculation of liquidus temperature, lever rule equilibrium and Scheil solidification. 4Q 2002.

DELIVERABLES: Expand pages for phase diagram Metallurgy Division Webbook with emphasis on solder alloys. Add pages for constituent binary and ternary systems containing Sb. 3Q 2002.

DELIVERABLES: Make simple phase equilibria software available for interactive use; make more complex programs available for downloads. 4Q 2002.

DELIVERABLES: Prepare draft Best Practice Guide for Differential Thermal Analysis 4Q 2002.

Accomplishments

NIST has taken a major role working with industry through a NEMI Task Force to identify and move Pb-free solders into practice. NIST co-chairs the NEMI alloy selection group that selected standard alloy compositions for U.S. microelectronics assembly. NIST is also active in the NCMS High Temperature Fatigue Resistant Solder Consortium and, as in the NEMI Task Force, led the alloy selection task group. The NCMS consortium, including Ford, Delphi, Allied Signal, Rockwell, Amkor, Heraeus, Johnson Manufacturing, and Indium Corporation, has identified and thermally cycle tested several Pbfree alloys for applications as high as 160 C. In the past year NIST has been responsible for analyzing microstructure evolution during thermomechanical fatigue.

■ NIST has developed the database necessary to calculate multicomponent phase diagrams essential for Pb-free alloy development. The experimental determination of phase diagrams is a time-consuming, costly task requiring expert interpretation of results. The calculation of phase diagrams significantly reduces the effort required to determine phase evolution in multicomponent systems and can provide quantitative information that is frequently needed in other modeling efforts. During the past year the NIST thermodynamics database for solders was expanded. Of particular importance is the development of a refined thermodynamic description for the Snrich part of the Sn-Ag-Cu system that was critical for alloy selection by the NEMI Lead-Free Task Force.

■ We are also working in collaboration with IPC Standards Committees (most closely with members from Celestica, Lucent, Raytheon, Rockwell, and Shipley-Ronel) to establish reproducible solderability test standards for board assembly. Activities include providing benchmark experiments for the wetting balance tests to predict on-line solderability for a wide range of surface finishes, lead materials, and solder alloys. New NIST research to develop electrochemical solderability tests and an understanding of whisker formation in Sn-based, Pb-free electroplated surface finishes complements the solderability studies.

NIST was also active in the NCMS High Temperature Fatigue Resistant Solder Consorincluding 8 companies in tium, the microelectronics and automotive industries, which completed a four-year project this year to develop Pb-free solders for harsh environment applications, such as automotive and NIST lead the alloy telecommunications. selection task group and took the lead in developing final conclusions and writing the final report, published in August, 2001 on CD-ROM.

Experiments were performed to establish the feasibility of Cu-Sn codeposition. In the case of the Sn-based electrolytes containing copper sulfate, one can assume that the copper deposition reaction proceeds at the diffusion-limited current density. The theoretical alloy composition can then be calculated assuming a Cu(II) diffusion coefficient of 5.0 x 10-6 cm^2/sec , a diffusion layer thickness of 100 µm, and a Sn current efficiency of 80%. As expected, the theoretical alloy composition increased linearly with the Cu(II) electrolyte concentration. It is also clear that the experimental alloy compositions deviate from those expected based on calculations that assume a diffusion limited copper reaction. This is likely due to an error in estimated diffusion layer thickness and indicates that rigorous hydrodynamic control should be implemented in future experiments.

• We have constructed a rotation electrode plating cell to reproducibly deposit Sn and Sn alloy coatings. A variety of substrates will be employed to determine the effect of substrate including amorphous carbon, vapor deposited Cu and electroplated Cu and Sn. Special emphasis is being focused on the characterization of the grain size, surface topography and residual stress. The last is being measured using x-ray 'sine-squared psi' analysis.

• Sources of uncertainty have been established for wetting balance solderability tests, leading to increased repeatability and reproducibility of tests.

• Recent flux studies performed at NIST have led to a change in test procedures for the IPC J-ANSI solderability standard.

Trace copper levels have been identified as contributor to propensity to tin whisker growth in electroplated deposits.

Collaborations

National Center for Manufacturing Sciences; high temperature lead-free fatigue-resistant solder.

IPC; development of solderability test procedures

National Electronics Manufacturing Initiative; Lead-free solders and reliability.

Recent Publications

Boettinger, W.J., Handwerker C. A., Newbury, B., Pan, T.Y., and Nicholson, J.M. "Mechanism of Fillet Lifting in Sn-Bi Alloys," J. Electronic Materials, 31 (2002) 545.

Boettinger, W.J. and U. R. Kattner, "On DTA Curves for the Melting and Freezing of Alloys," Metal. and Matls. Transactions, (2002), in press.

Gayle, F. W., "Fatigue-Resistant, High Temperature Solder," Adv. Mater. Process., **159** (4) 43-44 (2001).

Gayle, F. W., Becka, G., Syed, A., Badgett, J., Whitten, G., Pan, T.-Y., Grusd, A., Bauer, B., Lathrop, R., Slattery, J., Anderson, I., Foley, J., Gickler, A., Napp, D., Mather, J., and Olson, C. "Lead-Free High-temperature Fatigue-resistant Solder," Final Report, NCMS, August 2001 (published as CD-ROM). Gayle, F. W., Becka, G., Syed, A., Badgett, J., Whitten, G., Pan, T.-Y., Grusd, A., Bauer, B., Lathrop, R., Slattery, J., Anderson, I., Foley, J., Gickler, A., Napp, D., Mather, J., and Olson, C., "High Temperature Lead-free Solder for Microelectronics," Proceedings of The 4th Pacific Rim Conf. on Adv. Materials and Processing, Honolulu, HA (2001) in press.

Gayle, F. W., Becka, G., Syed, A., Badgett, J., Whitten, G., Pan, T.-Y., Grusd, A., Bauer, B., Lathrop, R., Slattery, J., Anderson, I., Foley, J., Gickler, A., Napp, D., Mather, J., and Olson, C., "High Temperature Lead-free Solder for Microelectronics," JOM, **53** (6) 17-21 (2001).

Kattner, U. R. and Handwerker, C. A., "Calculation of Phase Equilibria in Candidate Solder Alloys," Z. Metallkd., **92** (7) (2001).

Moon, K. W., Boettinger, W. J., Kattner, U. R., Biancaniello, F. S., and Handwerker, C. A., "Experimental and Thermodynamic Assessment of Sn-Ag-Cu Solder Alloys," J. Electron. Mater., **29** (10) 1122-1136 (2000).

Moon, K. W., Boettinger, W. J., Kattner, U. R., Biancaniello, F. S., and Handwerker, C. A., "The Ternary Eutectic of Sn-Ag-Cu Solder Alloys," Proceedings of 2000 SMTA Conference, Edina, MN, Surface Mount Technology Assoc, 941-944 (2000).

Moon, K. W., Williams, M. E., Johnson, C. E., Stafford, G. R., Handwerker, C. A., and Boettinger, W. J., "The Formation of Whiskers on Electroplated Tin Containing Copper," Proceedings of The 4th Pacific Rim Conf. on Adv. Materials and Processing, Honolulu, HA (2001) pp. 1115-1118.

Moon, K. W., Boettinger, W. J., Kattner, U. R., Handwerker, C. A., and Lee, D. J., "The Effect of Pb Contamination on the Solidification Behavior of Sn-Bi Solders," J. Electron. Mater., **30** 45-52 (2001).

Bath, J., Handwerker, C. and Bradley, E. "NEMI Group Recommends "Standardized Lead-Free Solder Alternative," Circuits Assembly (2000).

Handwerker, C., Noctor, R. and Whitten, G., "Reliability of Lead-Free Solders," published in Lead-Free Solders, Ed. Jennie S. Hwang (2000).

brought unique skills and expertise to both NCMS projects [Lead-Free Solder Project, and Lead-Free High **Temperature Fatique** Resistant Solder Project]. Without the support from NIST, both these projects would have extended over a longer period of time and would have been more costly to the project's industrial partners. In the case of the Lead-Free Program, a critical evaluation of the data would not have been done without NIST's leadership."

"NIST personnel

-- Duane Napp, Program Manager, National Center for Manufacturing Sciences

Interconnect Materials and Reliability Metrology

Goals

The objectives of this project are: (1) to develop experimental techniques to measure the reliability-related properties of thin films, including basic tensile properties, elastic modulus by both static and dynamic means, residual stresses, fatigue, fracture resistance, and electromigration and stress-voiding resistance, in specimens fabricated and sized like materials used in actual commercial devices; (2) to advance the ability to anticipate and meet thin interconnect reliability challenges by relating thin film reliability to microstructure and by developing understanding of the relationships between various modes of thin film failure, for example, electromigration and mechanical fatigue.

Customer Needs

Thin films are an essential component of all advanced electronic devices. Interconnect structures built up on ULSI microchips consist of 7 thin-film layers now, and will soon reach 10 layers (International Technology Roadmap for Semiconductors, 2001, Interconnect, Table 62a). These structures are fabricated using adjacent layers of materials with very different thermal expansion coefficients, using exotic materials such as nanoporous low-k dielectric, and operate at ever higher temperatures. According to the Roadmap (2001), Interconnect, p. 23, "Computer-aided design (CAD) tools will need to incorporate contextual reliability considerations in the design of new products and technologies. It is essential that advances in failure mechanism understanding and modeling, which result from the use of improved test methodologies, be used to provide input data for these new CAD tools. With these data and smart reliability CAD tools, the impact on product reliability of design selections can be evaluated." The National Electronics Manufacturing Initiative (NEMI) Roadmap of December 2000 reports a similar need. A section on pages 227-228 entitled "Key Simulation Prerequisites" states that "Laboratory infrastructure/experimental expertise is essential for both model verification as well as property input evaluations, to have truly effective simulations." A following subsection lists critical simulation areas. Listed first is "Reliability-Mechanics-Physics of Failure (POF), and associated Mechanical Analysis and Design." The message is clear: understanding and modeling of mechanical

performance and potential failure modes in these devices require knowledge of the mechanical behavior of the films. This issue of mechanical modeling is likely to increase in significance with the growing integration of interconnect between the chip and the package, with their disparate material sets.

Because the films are formed by physical vapor deposition, their microstructures, and hence their mechanical properties, are quite different from those of bulk materials of the same chemical composition. While the general principles of conventional mechanical testing are applicable to thin films, conventional test equipment and techniques are not. Because vapor-deposited films are of the order of 1 µm thick, the failure loads are of the order of gram-forces or less, and the specimens cannot be handled directly. So, techniques specific to films on silicon substrates are needed. Developing test methods must eventually become applicable to test structures that can be included in production or development wafers, so that applicability to 'real' materials can be demonstrated. The intent of our goal of testing specimens similar in size to structures on actual production devices is to maximize the relevance of our results.

Technical Strategy

We are developing a variety of measurement techniques to provide material property data on interconnect materials. In testing and exercising these techniques, we develop data that are valuable in themselves, and we also develop our understanding of the relationship between the observed behavior and the microstructure, as influenced by processing conditions specific to the specimen material at hand.

We study individual thin films and multilayer interconnect structures on silicon substrates, both obtained from industry and fabricated by researchers within NIST and elsewhere. Specimens of CMOS structures have been obtained through the MOSIS service run by UCLA. Occasionally, wafers or fabricated specimen geometries are received directly from our counterparts in industry. Some of our techniques require the removal of the silicon substrate beneath the test structure itself, to a depth of up to 50 µm. We have developed dry etching systems that use xenon difluoride to carry out these processes.

Technical Contacts: D. T. Read R. R. Keller M. Gaitan

"A microtensile

methodology, developed at the National Institute for Standards and Technology, has been adopted and applied in Motorola to evaluate material properties of thin films. This methodology is a significant part of the materials technology development at Motorola."

Betity Yeung, David Read, Yifan Guo, Bill Lytle, and Vijay Sarihan (Motorola AISL, Tempe, AZ), "Microtensile Methodology for Mechanical Characterization of Thin Films," manuscript submitted to Semiconductor International.



Test chip produced in the 1.2 μm AMI CMOS process available through the MOSIS service.

Measurement capabilities operating within this project include microtensile testing and d.c. and a.c. electromigration measurements. Resonant structure measurements will soon go on line. We have developed the silicon-frame tensile specimen and the piezo-actuated tensile tester, which operate successfully for specimens 100 µm wide and larger. We have continued to support one such apparatus at NIST and one at Motorola in Tempe. Another, which uses different control software, exists at the University of Colorado at Boulder. Because problems were encountered with specimens narrower than 100 µm, a new technique, called the force-probe tensile test technique, has been developed. The apparatus includes a tensile loading system operable within the scanning electron microscope (SEM). This system has now been used on specimens as small as 2 µm wide. It is anticipated that the magnification of the SEM will allow testing even narrower specimens.

Our measurements involving alternating current stressing of chip-level interconnects are used to explore the relationships between electrical and mechanical reliability. High current density a.c. signals are run at low frequencies through Aland Cu-based electromigration structures in either passivated or unpassivated states. Joule self-heating results in a cyclic strain due to thermal expansion mismatch between the metal lines and their substrates. The associated deformation then leads to severe topographic distortions in the lines, and can eventually cause open circuit failure. We have begun investigating the effects of current density, frequency, crystallographic orientation, and encapsulant material. cantilevers patterned from interconnect materials. The resonant frequency of these is related to the Young's modulus, the density, and the geometry of these cantilevers. These structures can be fabricated simultaneously with free fixed-fixed and fixed-free cantilevers used in a related, static method for measuring through-film average residual strain and strain gradient. With the residual strains, from the static method, and the elastic constant, from the dynamic method, the residual stress and its gradient can be calculated.

DELIVERABLES:

Our results are being disseminated in conference presentations and peer-reviewed articles in archival journals, as well as in presentations and written reports to the organizations that have supplied specimens. Report microtensile tests on sputtered and electrodeposited copper: 2Q 2002.

Construct system for conducting a.c. tests on interconnects *in-situ* within SEM. 4Q 2002.

Conduct round robin experiment and draft ASTM standard method on fixed-fixed beam test structures for measurement of residual stress. 3Q 2002

Complete report that describes resonant frequency test structures designs, measurement results, and comparisons with models. 4Q 2002

Accomplishments

Progress in recent years on measurements of the mechanical behavior of thin films has put us in the position of starting to be able to make various kinds of critical comparisons among our results: results for the same materials in different laboratories; results for similar materials from different sources; and results for the same property by different measurement methods. These comparisons are necessary to reach our goals of providing accurate and believable measurement techniques and an understanding of the results.

In Fiscal Year 2001 we reported the severe effect of specimen geometry on the tensile elongation of pure e-beam deposited aluminum. Changing to a much narrower specimen raised the elongation from around 1 % to over 20 %.

• This result highlights the necessity of standardized geometry in tests used to compare different materials. Several advances in the utilization of our new force-probe technique were made in Fiscal Year 2001. These include successful testing of a polymer, photodefinable polyimide, and of a hard, brittle material, polysilicon.

We are developing resonant measurements for

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Ring-pull specimen of polysilicon made by Sandia National Laboratories, tested using the NIST forceprobe technique

These results demonstrate the wide applicability of the force-probe technique.

• Another milestone reached in Fiscal Year 2001 was the successful testing of a film that had been produced as part of a commercial fabrication process, specifically, metal 2 and metal 1-2 composite specimens of CMOS aluminum contact material. The layout is shown above. The contact material picks up a significant silicon content during the anneal, and so it is not surprising that this material has properties that are significantly different from pure aluminum.

■ This material had very low elongation, and also very low tensile strength. Its elastic stiffness was difficult to measure because the strength was so low, but it appears to be well above that of pure aluminum. The third significant milestone reached in microtensile testing in 2001 was testing at elevated temperature. We tested both the CMOS material and polyimide at temperatures of 100 °C and 150 °C, in addition to room



Microtensile specimen on CMOS chip obtained through the MOSIS process. The slender strip on the right is the test section. It is 10 µm wide by about 200 µm long.

temperature. The specimen wafers were placed on a heating stage in the SEM, and the force probe used to load the specimens was also heated. We are conducting further tests in order to understand the observed behavior. The changes in the measured properties of the CMOS material were subtle, 10 % or less. Larger changes were seen in the polyimide, but the results so far are ambiguous because the specimens were apparently damaged during sputtercoating, which was carried out to make the specimens visible in the SEM.





Results of a microtensile test of sputtered copper film.

Results of a microtensile test of an electrodeposited copper film.

• Recently, we have been working to demonstrate the applicability of these techniques to materials used in the microelectronics industry. Here we show examples of results obtained on two different types of copper films. The strength values are far above the handbook values for pure annealed bulk copper, and the elongations are much lower than the handbook values. The differences between the thin sputtered film and the thick electrodeposited film are generally consistent with trends seen for other thin film materials.

The demonstrated applicability of the forceprobe technique to a variety of specimen materials and temperatures leads us to think that this technique and its complementary specimen geometry may become a standard method for microtensile testing.



Surface morphology produced by a.c. testing. Both slip band offsets and whiskers can be seen.

• Our a.c. tests have produced microstructural features completely different in both quantity and quality from those seen in conventional d.c. electromigration tests. Similar features are produced during mechanical fatigue. High currents in a.c. can also produce whiskers that tend to be longer and narrower than those produced during d.c. testing.

With further investigation, we expect to find conditions where the damage induced by high current density a.c. testing is due solely to fatigue. This method then has the potential for becoming a controlled fatigue testing technique that could be applied to structures with dimensions well below one micrometer. The relationships among failure by d.c. electromigration, failure by a.c. stressing, and the mechanical performance of actual devices are now being



Janet Marshall investigating the measurement of Young's modulus using an optical vibrometer.

studied.

. Because it is sometimes impossible to get films of individual materials with the interconnect stack in a chip that goes through a normal manufacturing process, we are studying measurement methods that use composite laminate specimens that include several materials, such as metal and dielectric. The elastic modulus of the individual films in the laminate is to be determined by differences between the resonant frequencies of beams with different combinations of metal, dielectric, and polysilicon. A model has been developed for a composite cantilever beam. Preliminary measurements indicate that this technique can provide accurate values of the different layers in the interconnect structure, as well as insight into the behavior of the structure as a whole.

We have been collaborating with George



Frequency response of two cantilever resonant test structures: the SiO2 and the SiO2 plus one layer of Polysilicon, and 2 layers of metal interconnect.

Harman on IC bond pad test structures to measure the temperature of the wire bonding process. The bond pad test structures contain an integrated thermocouple that is used to sense the temperature of the bond pad during wire bonding. The thermocouple is composed of an aluminumpolysilicon contact. A test chip containing the bond pad test structures was fabricated and tested. The aluminum-polysilicon thermocouple was determined to have a Seebeck coefficient of 44 μ V/°C using a newly designed test structure. Measurements of the bond pad temperature and a model that is being developed have been reported at an industry conference.

Collaborations

Max-Planck-Institut für Metallforschung, Stuttgart, Germany, Prof. Eduard Arzt, Dr. Cynthia Volkert Intel Corp., Chandler, AZ, Dr. Richard Emery

Motorola, Inc., AISL, Tempe, AZ, Betty Yeung, and MATC, Schaumburg, IL, Dr. Andrew Skipor

Intel, Dr. Tracey Scherban

Recent Publications

Herman, David, Gaitan, Michael, and DeVoe, Don, "MEMS Test Structures for Mechanical Characterization of VLSI Thin Films," Proc. SEM Conference, Portland Oregon, June 4-6 (2001).

Keller, R. R., Mönig, R., Volkert, C. A., Arzt, E., Schwaiger, R., and Kraft, O., "Interconnect Failure due to Cyclic Loading," *Proceedings of the Sixth International Workshop on Stress-Induced Phenomena in Metallizations*, S. P. Baker, M. A. Korhonen, E. Arzt, and P. S. Ho, Eds., American Institute of Physics Conference Proceedings Vol. 612, pp. 119-132, Melville, NY (2002).

LaVan, D.A., Tsuchiya, T., Coles, G., Knauss, W. G., Chasiotis, I., and Read, D. T., "Cross Comparison of Direct Strength Testing Techniques on Polysilicon Films," *Mechanical Properties of Structural Films, ASTM STP 1413*, C. Muhlstein and S. B. Brown, Eds., American Society for Testing and Materials, West Conshohocken, PA, (2001).

Long, G. S., Read, D. T., McColskey, J. D., and Crago, K., "Microstructural and Mechanical Characterization of Electrodeposited Gold Films," *Mechanical Properties of Structural Films, ASTM STP 1413,* C. L. Muhlstein and S. B. Brown, Eds., American Society for Testing and Materials, West Conshohocken, PA, (2001).

Read, D. T., Cheng, Y.-W., and McColskey, J.D., "High Ductility in Small Tensile Specimens of e-Beam-Deposited Aluminum Films," *Scripta Materiala* **45** (2001), pp. 583-589. Read, D. T., Cheng, Y. –W., McColskey, J. D., and Keller, R. R., "Mechanical Behavior of Contact Aluminum Alloy," *MRS Symposium Proceedings* vol. 695, pp. L6.11.1-L6.11.6. (2002).

Read, D. T., Cheng, Y-W., Sutton, M. A., McNeill, S. R., Schrier, H., "Proposed Standardization Effort: Digital-Image Correlation for Mechanical Testing," *Proceedings of the SEM Annual Conference on Experimental and Applied Mechanics*, pp. 365-368, (2001).

Read, D. T., McColskey, J.D., and Cheng, Y.-W., "Microscale Test Technique and Results for Aluminum Thin Films," *Proceedings of the SEM Annual Conference on Experimental and Applied Mechanics*, June, pp. 442-445, (2001).

Shuman, Shivesh, Gaitan, Michael, Joshi, Yogendra, and Harman, George, "Wire Bond Temperature Sensor," IMAPS 2001 Symposium, Baltimore, MD, October 7-11, (2001).

Yeung, B., Read, D. T., Guo, Y., Lytle, W., Sarihan, V., "Microscale test technique and results for aluminum thin films", accepted for International Mechanical Engineering Conference and Exhibition, November, (2001).

Keller, R. R., Mönig, R., Volkert, C. A., Arzt, E., Schwaiger, R., and Kraft, O., "Interconnect Failure due to Cyclic Loading," Sixth International Workshop on Stress-Induced Phenomena in Metallizations, Ithaca, NY, July 25-27, 2001. (INVITED)

Mönig, R., Orso, S., Volkert, C. A., Keller, R. R., and Arzt, E., "AC-Induced Damage in Cu Interconnects," Materials Research Society Spring Meeting, San Francisco, CA, April 1-5, 2002.

Read, D. T., Cheng, Y. –W., McColskey, J. D., and Keller, R. R., "Mechanical Behavior of Contact Aluminum Alloy," Materials Research Society Fall Meeting, Boston, MA, November 26-30, 2001.

Read, D. T., Cheng, Y. -W., and McColskey, J. D., "Microtensile Behavior of a Commercial Photodefinable Polyimide," accepted for *Proceedings of the SEM Annual Conference on Experimental and Applied Mechanics*, (2002).

Thermal Measurements and Packaging Reliability

Goals

The goals of this project are to:

a) Provide the micro-electronics packaging industry with information, guidance, and tools through technology transfer to characterize the behavior of features and interfaces in packaging that are thermally stressed. Information and guidance are provided directly to individual companies and to consortia through collaborations whereby we are provided with specimens, which present a reliability concern to the manufacturer or end-user. The results of the tests are reported to the provider, and are typically reported in the general literature or at technical This system contributes toward meetings. achieving our third and primary goal-providing the industry with the tools to characterize these thermomechanical behaviors. Review and evaluation of the techniques by our industrial collaborators allows us to refine the techniques to make them optimally beneficial to industry and to demonstrate to the industry at large the capabilities of the techniques on actual packages in development, essential for technology transfer.

b) Develop and evaluate methods for measuring temperatures at and within the chip-level for the purposes of determining *insitu* material thermal properties (e.g., thermal properties of interlayer dielectrics), device performance (e.g., SOI devices), and for evaluating the thermal performance of new architectures and technologies (e.g., 3D integration and innovative cooling methods for high performance logic).

Customer Needs

The trend in electronics is toward components of higher density and smaller size using less expensive materials. Materials used in packaging are many and display a variety of thermal responses that are not always compatible. This makes interfaces particularly vulnerable to thermomechanical fatigue failures. The program seeks to offer support and verification of models conducted or sponsored by the microelectronics industry. The technique allows the researcher to observe the substrate throughout the thermal cycling so that one can identify the locations and materials in which deformations are occurring.

The physical size of nearly all electronic devices is decreasing rapidly and, at the same time, their capabilities are increasing dramatically. One move in this direction is the advent of integral passive components and another is the increasingly prevalent use of organic (polymeric) conductors and fillers. These organic materials have a large coefficient of thermal expansion, which can reduce the reliability of electronic packaging systems. We are investigating interfaces between organic materials and between organics and metals to determine the initiation of damage and failure mechanisms in these material systems.

Temperature measurements for microelectronic devices are more important today than they ever have been. It has always been true that extreme temperature places limits on the operating range of nearly all devices, but today, increasing power dissipation and power densities threaten to create temperatures that block continued progress according to 'Moore's Law.' Clearly, new and innovative methods for cooling chips and packages must be found along with new materials and circuit designs, and architectures for decreasing the power dissipation and operating temperature. Equally as clear, we must have accurate and wellunderstood methods for measuring the temperature of devices to aid in the development of these new techniques and materials.

"Packaging cost is a second area that could be an obstacle to realizing the potential of advances in silicon technology. ...the average packaging share of total product cost will double over the next 15 years and, more significantly, the ultimate result will be greatly reduced gross profit margins, limiting investments in R&D and factory capacity." 2000 NEMI Roadmap

The maximum junction temperatures for chip operation are shown in tables 75 a and b of the 2001 ITRS Assembly and Packaging section. The criticality of knowing thermal properties of materials and devices is discussed on page 8 of the Assembly and Packaging section, page 25 of the Metrology section, and page 19 of the Interconnecty section. Validated thermal models are discussed on page 25 of the Metrology section.

Technical Strategy

1. Our established programs in infrared (IR) (thermal) microscopy and electron-beam moiré, and our developing techniques in scanning thermal microscopy and scanning probe moiré, utilizing the AFM (atomic force microscope), have much to offer the microelectronics industry.

Technical Contacts: A.J. Slifka E.S. Drexler D. L. Blackburn A. R. Hefner

"The task of dissipating the heat from integrated circuits while maintaining acceptable junction temperatures has been a significant challenge for semiconductor and system manufacturers." "We continue to push the cooling and mechanical limits of electronic products. Complete thermal and mechanical modeling,

validated with measurements, is needed."

2001 International Technology Roadmap for Semiconductors

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We have been approached by industry with requests for aid as simple as "How high are the temperatures in this MCM (multichip module) during service" to as challenging as "What are the strains in the on-chip tungsten vias under thermal loading." The first was answered using the IR microscope; the second has yet to be answered.

We have just completed our second year of applying thermal conductivity measurements using the IR microscope to the problem of packaging reliability and have engendered great interest from the Advanced Embedded Passives Technology (AEPT) Consortium. As thermal conductivity measurements are one of the most sensitive indicators of metal purity, likewise they are one of the most sensitive indicators of interfacial integrity. A minute decline in interfacial thermal conductivity is the first indication of the microcracks and fissures that may ultimately result in failure.

DELIVERABLES: Quantitative measurements of industrial specimens from AEPT using thermal SPM. 4Q 2002

IR microscope measurements of next-generation embedded resistor specimens from the AEPT consortium using laser heating. 3Q 2002

IR microscope measurements of next-generation embedded resistor specimens from the AEPT consortium using Joule heating. 4Q 2002

2. The electron-beam moiré technique offers a unique capability. Unlike moiré interferometry, it can quantify strain in the different materials at both low temperatures and at high temperatures. It measures thermally-induced strains representative of those experienced by the package in service, rather than residual strains due to processing. In addition, it can quantify the accumulation of plastic strain during thermal cycling, and it is clear from the images in which materials the strains are occurring. The technique is designed to look at strains on a local scale, but is flexible enough to allow comparison of those local strains at multiple locations across the cross section.

A collaboration with the Jet Propulsion Laboratory (JPL) is studying the effect of a microwave process on solder bump reliability. The 3-phase program will look at the differences in strain in solder bumps that have been processed before thermal cycling, after thermal cycling, and a control set that will not be processed.

DELIVERABLES: Electron-beam moiré measurements of the post process JPL specimen

will be made over two thermal cycles followed by analysis and comparison with the strain data from the pre-processed and control specimens. 3Q 2002

3. Work continues with the AEPT on the embedded resistors. The first round of measurements were completed in October, comparing strain in the printed circuit board for four different layouts of the copper interconnects and terminations. A second test vehicle has been sent to NIST for strain measurements for embedded resistors that have different sizes and layouts.

DELIVERABLES: Electron beam moiré measurements of next-generation embedded resistor specimens from the AEPT consortium. 3Q 2002 and 1Q 2003

Present results of first generation embedded resistor from AEPT at ECTC 2002. 4Q 2002

4. Thermal microscopy and electron-beam moiré are complementary techniques, each supplying pieces to the puzzle of how failure occurs. The AEPT Consortium has actively enlisted our help, recognizing the value of each technique, alone and together.

DELIVERABLES: Analyze and report IR microscopy and electron beam moiré data from next generation embedded resistor specimens to members of the AEPT consortium. 1Q and 2Q 2003

5. The reasons for desiring to know the operating temperature of a semiconductor device can be divided into the following four broad categories:

Predict reliability or operating life of device,

 Measure material/device thermal properties in-situ,

• Confirm or determine the operating limits or thermal performance of a device,

• Validate thermal models for chip and device performance,

A broad range of temperature measurement techniques will be investigated. These will include:

• electrical techniques that use temperature sensitive device and material parameters (such as junction voltages, threshold voltages, and resistivity) as thermometers,

• optical techniques such as infrared thermal emission, micro-Raman spectroscopy, and reflectance, and

micro-probes based upon AFM systems.

DELIVERABLES: Complete verification of high speed thermal imager calibration procedure and software performance. 4Q 2002.

Write a critical survey paper of the possible methods for measuring semiconductor device temperature and publish in archival journal. 4Q 2002

Demonstrate applicability of the NIST high-speed infrared imaging system to high performance logic and/or system-on-a-chip devices. 1Q 2003

Establish full range of capabilities for measuring the temperature of microelectronic devices using electrical techniques. 1Q 2003

Accomplishments

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A test program was begun for IBM in Rochester, MN on their BGA (ball grid array) package with the Si chip encased in ceramic. The specimens were received in early February. The combination of alumina and solder columns made specimen preparation very difficult. The first electron-beam moiré test was completed in July, but the results were ambiguous. A second specimen was prepared, tested for seven thermal cycles between -5 °C and 130 °C, and the results analyzed in August. These results show that no shearing of the solder column developed over this temperature range and number of cycles, either at the interface with the circuit board or the alumina (See Figure 1).

We began working with MicroFab Technologies of the Advanced Embedded Passives Technology (AEPT) Consortium on inkjet printing of embedded resistors. Meanwhile, one of the other consortium members learned about our techniques and asked our help in evaluating termination geometries. SAS Circuits provided us with samples with four different geometries. Two of the specimens had interconnects with straight approaches to the termination, but different sized terminations. The other two had indirect approaches, that is, the interconnect had a bend. SAS Circuits was interested in knowing what magnitude of strains was experienced by the package during processing up to 177 °C. Four specimens were prepared and tested in the 4th



Figure 1. Moiré image and corresponding strain map of the IBM BGA specimen after 7 thermal cycles.

quarter of FY01 (see Figure 2). The data showed larger strains in the printed circuit board (PCB) with indirect interconnects to the copper



Figure 2. Moiré images of embedded resistor specimens provided by SAS/Coretec Inc. at 177 °C.

terminations. Cracks developed between the resistor and the laser barrier within the PCB with the indirect interconnects, but the PCB with the direct interconnects had no cracks develop and very little plastic deformation after two thermal cycles.

One issue became clear as the thermal conductivity tests were being conducted for Micro-Fab: we needed improved resolution in order to distinguish what was occurring in the very thin (<10 µm) resistive ink. This need, coupled with the desire for increased resolution for the moiré measurements, led us to the atomic force microscope (AFM). We had an existing AFM outfitted for thermal measurements. Special cantilevers with coated tips that act as thermistors are used. Figure 3 shows a thermal image of an integral resistor specimen using that system. Thermal imaging is possible with the system, but the electronics provided are so noisy that there is no way to repeatably acquire images. Therefore, using that AFM system for thermal measurements is not possible. We acquired another AFM from another vendor, one that does thermal imaging in two different modes. We have prepared samples for thermal AFM measurements, and are beginning those measurements on samples from the AEPT.

Moiré on the scanning probe microscope should follow the same theory as with moiré generated in the scanning electron microscope. The probe tip is looking for height differences, analogous to how the electron beam looks for edges. So if the number of raster lines is approximately equal to the number of lines of the specimen grating in the field of view, moiré fringes will be reproducibly generated. This part of the theory has been validated.

The problem arises when one attempts to calibrate the technique for thermally induced strains. Early on in the process, we recognized that a very stable system was essential and, as a result, our existing AFM system was inadequate. We tested a stable, closed-loop system that also had a wellcontrolled thermal attachment at the manufacturer's applications laboratory and obtained extremely consistent room temperature data $(\pm 0.03 \text{ fringes})$. However, when we attempted to thermally load and unload a gold standard to obtain coefficient of thermal expansion data, the value measured was 3× the handbook value (14.2 $\times 10^{-6}$ /°C), and the loading and unloading slopes were inconsistent. However, the linearity specification cited by the manufacturer could account for this error, as such small displacements are being measured. At the present time, we are collaborating with researchers at the University of Colorado and working with manufacturers of AFMs and the closed-loop piezo systems to determine if an instrument can be developed that will provide the required x-y precision necessary

Isothermal, 22 °C



Figure 3. Thermal SPM image of an industrial integral resistor specimen.

for quantitative displacement measurement using scanning probe moiré.

We have developed and tested software that provides repeatable quantitative analysis of IR microscope data. This enables us to measure interfacial thermal resistance across relevant interfaces in electronic packaging specimens and embedded and integral resistor specimens. A modification to allow Joule heating of resistor specimens for IR microscopy measurement was designed and tested. This yields accelerated degradation of interfaces and also allows analysis of heat flow under extreme conditions as defined by our industrial collaborators. We have developed the mathematics required to analyze IR microscope measurements under Joule heating. Numerous industrial specimens were measured using IR microscopy with Joule heating, one being shown in figure 4. A set of measurements was used to model interfacial thermal resistance as a function of thermal cycling and a paper was written on the subject.



Figure 4. IR microscope image of a Joule-heated integral resistor from MicroFab, Inc.

• For comparison with IR microscopy, a method of generating a comparable temperature difference across a specimen was needed for thermal SPM. A heating apparatus for use with thermal SPM measurements was designed and constructed. Comparative measurements of a single specimen, using both IR microscopy and thermal SPM, showed the potential of the new thermal SPM technique. Members of the AEPT consortium have shown interest in this technique, as it is able to probe features on an appropriate size scale and will be applicable for years to come.

• We have developed a high-speed transient thermal imaging system with less than 5 μ s temporal resolution and less than 20 μ m spatial resolution. Applications investigated include microelectronic devices, MEMS, and advanced semiconductor power devices (SiC). The transient thermal imager can make a movie of the heating of the entire surface (one frame of which is shown in figure 5) as well as simultaneously provide a single point response (as shown in figure 6).

We have determined that the micromachined hotplate (figures 7 and 8) should serve as an excellent vehicle for calibration of the high speed transient thermal imaging system and for determining its temporal resolution more accurately.

Preliminary results demonstrate that the infrared high speed imaging system and the MEMS micro hotplate are in very good agreement on the transient thermal response of the MEMS structure. The hotplate temperature is measured electricacally as a change in resistance of the aluminum spreading plate with temperature. Results of the comparison are shown in figure 9.



Figure 5. Infrared temperature map of MEMS hotplate approximately 50 μ s after heating pulse was applied.



Figure 6. Measured temperature versus time for center point of hotplate indicated by cross-hairs in above transient infrared image.



Figure 7. Photo micrograph of MEMS-based hotplate that can be used to determine the time and spatial resolution of the high-speed thermal imaging system.









Table 1. List of some temperature measurement methods for semiconductor devices.

	Technique	Advantages	Disadvantages
esponse hermal nce test ng the ne tem- given at n Next figure nethods	Optical	 Temperature map possible. Generally non-contacting, minimally invasive. Potentially very good spatial resolution. 	 Chip surface must be visible. Generally expensive and complex. Device cannot be normally packaged.
nethods ges and	Electrical	 No contact, non-invasive (can be done on a packaged device). Generally inexpensive, simple. 	 Generally a non- specific tempera- ture average. Electrical and other interferences.
	Physically Contacting	 Temperature map possible. Excellent spatial resolu- 	 Contact to surface required. Expensive and complex. Device cannot be

Figure 9. Comparison of transient temperature re waveforms measured with the transient "IR" th microscope and the calibrated "electrical" refere structure.

An invited presentation discussing variety of methods used for measuring th perature of semiconductor devices was g THERMES 2002, 'Thermal Challenges in Generation Electronic Systems.' The below shows examples of the generic n that have been used to measure chip-leve peratures.

Tables 1. and 2. list some of the specific m (Table 1) and also some of the advantage disadvantages that each has (Table 2).





TABLE 2. List of some advantages and disadvantages of generic measurement types

normally packaged.

tion.
Collaborations

IBM, Rochester, MN

Arv Sinha, Joe Kuczynski

AEPT Consortium

Dupont, John Felten

MacDermid, Dennis Fritz

Merix, Bob Greenlee

MicroFab, Plano, TX

Virang Shah

SAS Circuits, Littleton, CO

Richard Snogren, Matt Snogren

University of Colorado

Ken Douglass, T. Andrew Winningham

Colorado School of Mines

Ivar Reimanis, Saki Krishnamurthy,

John Berger

George Washington University

Georgia Institute of Technology

University of Maryland

Recent Publications

Drexler, E. S., "Plastic Strain in Thermally Cycled Flip-Chip PBGA Solder Bumps," *IEEE Transactions on Advanced Packaging* 23, 4, pp. 646–651, (2000).

Drexler, E. S., and Winningham, T. A., "Validation of Scanning Probe Moiré Technique Using the CTE of Gold," in *Proceedings of the Society for Experimental Mechanics Annual Conference on Experimental and Applied Mechanics*, June 4–6, 2001, Portland, OR, Society for Experimental Mechanics, Bethel, CT, pp. 387–390 (2001).

Slifka, A. J., Drexler, E. S., "Thermomechanical Effects in Embedded Passive Materials," *Journal of Electronic Materials*, 31, 4, pp.286-291, (2002).

Drexler, E. S., Snogren, R. C., Snogren, M. C., Felten, J. J., and Green, P. A., "Strain Measurements In Thermally Loaded Circuit Boards Containing Embedded Resistors," accepted to the *Proceedings of the Electronic Components Technology Conference.*

Slifka, A. J., Drexler, J. W., "Apparent Mobility of Interfaces in Integral Resistor Material," accepted by *Microscopy and Analysis*, to be published March 2003.

Hefner, A., Berning, D., Blackburn, D., Chapuy, C., and Bouche, S.A "High-Speed Thermal Imaging System for Semiconductor Device Analysis," *Proceedings of the 17th Annual IEEE Semiconductor Thermal Measurement and Management Symposium*, pp. 43-49, 2001.

Afridi, M. Y., et. al, "Transient Thermal Study of Microhotplates by Using High-Speed Thermal Imaging System," *Proceedings of the 18th Annual IEEE Semiconductor Measurement and Management Symposium*, March 2002.

Blackburn, D. L, "Temperature Measurement of Semiconductor Devices," Thermes 2002-Thermal Challenges in Next Generation Electronic Systems, Millpress, Rotterdam Netherlands, 2002, pg. 23.

National Institute of Standards and Technology

Dielectric Metrology Supporting Integrated Passive Device Technology

Technical Contacts: J. Obrzut

"We truly need NIST expertise to take on this metrology work and help guide the participating people in the proper direction."

Tom Newton Director of PWB Standards & Technology IPC Association Connecting Electronics Industries

"Your effort to characterize the dielectric performance of the materials at high frequencies helped us to understand these materials and successfully realize our program objectives." Richard A. Charbonneau, Project Leader of the EDC Consortium, Storage

Technologies.

Goals

Develop techniques for accurate broad-band measurements of permittivity at microwave frequencies and the fundamental framework for identifying the key structural attributes that control the dielectric properties of organic resins filled with ferroelectric ceramics. The development of Integrated Passive Device (IPD) technology for packaging high speed electronics critically depends on measurements of the dielectric permittivity and ability to control the dielectric properties from the material's microstructure.

Customer Needs

Novel dielectric hybrid materials based on organic resins and ferroelectric ceramics with high dielectric constants have been identified by the industry as essential for advancing miniaturization and functional performance of high-speed electronics. The development of advanced dielectric composites requires new metrology and fundamental understanding of the high frequency relaxation mechanism in relation to structural and molecular attributes.

The materials and testing requirements for capacitors, resistors and inductors in Mixed-signal and RF Technology are outlined in the 2001 International Technology Roadmap for Semiconductors, Table 29b, section on Process Integration Devices and Structures. A need for a new high frequency standard test method was identified by the IPC Embedded Passive Device Standard Sub-committee.

Technical Strategy

1. We employed a new broad-band measurement technique to determine the impedance characteristics and the dielectric permittivity of highdielectric constant films at frequencies of 100 MHz to 10 GHz.

DELIVERABLES: Complete the first precision prototype test fixture for high frequency dielectric measurements. Perform the feasibility study of measurement on high–k films that are currently being developed by the electronic materials suppliers. 1Q 2003

2. In partnership with the IPC Standard Test Committee Task Force for Embedded Passive Devices. Design the test protocol and make arrangement with co-sponsoring member companies for a round-robin evaluation of the testing methodology.

DELIVERABLES: Draft a standard test method document for the Institute of Packaging Circuits (IPC). Identify configuration for in-situ on-chip measurements above 10 GHz. 1Q 2003

3. Exploring the relationships between the dielectric properties and structure in polymer resins filled with ferroelectric ceramics. Our effort is focused on the local fast relaxation mechanism that we discovered in dielectric composites.

DELIVERABLES: Identify key materials attributes characterizing high frequency dielectric relaxation in polymers filled with ferroelectric inclusions in relation to molecular structure, polarizability, morphology, and the domain size. 3Q 2003

Accomplishments

We have developed an accurate broadband measurement technique that enables dielectric measurements at microwave frequencies of up to several GHz. The broadband test methods currently in use by the industry are based upon the lumped element approximation. They are limited to frequencies below a few hundred megahertz. Our new technique is based on the observation and theoretical analysis of the fundamental mode propagating at high frequencies in thin film dielectrics terminating a coaxial air-filled transmission line. The 3D vector plot of the electric field of the first fundamental mode, simulated inside a high-k specimen, is shown in Figure 1.



Fig. 1 The vector plot of the electric field, E, of the first fundamental mode inside the film specimen (ε* = 34.6 – j1.6) terminating an AP-7 coaxial line. The arrows indicate the direction and strength of the field E.

In contrast to the lumped element model, the field in the specimen section is not uniform. At a resonant frequency of 8.2 GHz, the magnitude of the electric field, E, shows two maxima localized near the edge of the specimen, while the magnitude field E minimum extends along the specimen diameter. The corresponding plot of H is parallel to the propagation direction. Both E and H fields appear to decay rapidly at the interface between the high-k dielectric and air. Our capability to measure the dielectric relaxation times in the sub-nanosecond regime and the relaxation strength for wide range of dielectric permittivity values will be used to quantify dispersion, alignment, and structure in hybrid materials that exploit nanoscale anisotropy and heterogeneity.

Collaborations

J. Baker, R. Gayer, P. Kabos, B. Riddle, (NIST, Radio Frequency Technology Div.)

J. Dougherty (Penn State Univ.), T. Hubbing (Univ. of Missouri)

J. Lauffer (IBM),D. Murry (Litton), R. Foly (DOD), L. Patch (NCMS),D. McGregor (DuPont), D. Senk (Shipley), R. Sheffield (Nortel), A. Tungare (Motorola)

Recent Publications

R. Popielarz, C.K. Chiang, R. Nozaki and J. Obrzut, "Dielectric properties of polymerferroelectric ceramic composites from 100 MHz to 10 GHz," Macromolecules, 34, pp. 5910 (2001)

J. Obrzut, N. Noda and R. Nozaki, "Broadband metrology for polymer composite films," IEEE Dielectrics and Electrical Insulation Society, 2001 Annual Report, pp. 269 (2001)

N. Noda, and J. Obrzut, "High frequency dielectric relaxation in polymers filled with ferroelectric ceramics," Mat. Res. Soc. Symp. Proc., **628**, pp. EE.3.8.1-6, (2002)

J. Obrzut, N. Noda and R. Nozaki, "Broadband characterization of high-dielectric constant films for power-ground decoupling," IEEE Transactions on Instrumentation and Measurements, August (2002). Device scaling has been the primary means by which the semiconductor industry has achieved unprecedented gains in productivity and performance quantified by Moore's Law. Until recently only modest changes in the materials used have been made. The industry was able to rely almost exclusively on the three most abundant elements on Earth – silicon, oxygen, and aluminum.

Recently, however, copper has been introduced for interconnect conductivity, replacing aluminum alloys. A variety of low-dielectric constant materials are being introduced to reduce parasitic capacitance, replacing silicon dioxide. As dimensions continue to shrink, the traditional silicon dioxide gate dielectric thickness has been reduced to the point where tunneling current has become significant and is compromising the performance of the transistors. This is requiring the introduction of higher dielectric constant materials. Initially the addition of nitrogen to the gate material is sufficient, but in the near future more exotic materials such as transition metal oxides, silicates, and aluminates will be required. As dimensions are reduced, gate depletion effects and dopant diffusion through the gate dielectric are limiting transistor performance. With the replacement of the traditional silicon dioxide/ polysilicon gate stack processes with materials capable of supporting ever shrinking geometries, the task of the industry becomes more difficult. The overall task represented by the projects below reflects the need for analytical techniques with unparalleled spatial resolution, accuracy, robustness and ease of use.

Shrinking dimensions of transistors while simultaneously increasing the wafer diameter from 200 mm to 300 mm is placing more stringent requirements on wafer flatness, thickness and warp, ion and particle contamination.

Accurate metrology of process gases is essential for reproducible manufacture of semiconductor products. Critical physical parameters need to be measured on a wide variety of reactive and non-reactive process gases, allowing the accurate calibration of flow meters and residual gas analyzers. Water contamination at extremely low levels in process gases presents serious manufacturing difficulties. Accurate calibration of water vapor at extremely low vapor pressures is required.

Accurate metrology of process gases is essential for reproducible manufacture of semiconductor products and a wide variety of metrology issues emerge in plasma, chemical vapor, and rapid thermal processing steps used in semiconductor manufacture.

Detection and accurate sizing of particle contamination continues to challenge semiconductor manufacturing.

Wafer and Chuck Flatness Metrology

Goals

Develop measurement support for 300 mm diameter silicon wafers used in lithography applications. This project will provide measurement and infrastructural technology to support the interferometric measurement of thickness variation and surface flatness in the free form or aschucked condition.

Customer Needs

Decreasing linewidths, and the resulting reduced depth of focus, combined with larger wafer diameters for current stepper lithography applications place ever increasing restrictions on flatness measurement and the required measurement uncertainty for thin parallel windows. For example, the International Technology Roadmap for Semiconductors (ITRS) suggests a flatness of less than 90 nm will be required per die site for the 90 nm node (expected by 2005). We are focused on meeting customer requirements for calibrated thickness variation maps of free form wafers and flatness measurements of as-chucked wafers. We are addressing the need for thickness variation maps of 300 mm diameter wafers using the NIST Infrared Interferometer (IR²). There are two reasons for concentrating on wafer thickness variation. First, an independent traceable measurement is required by instrument manufacturers to certify the performance of their instru-Second, thickness variation measurements. ments of silicon wafers can be combined with models of wafer/chuck interactions to determine the flatness of low surface area wafer vacuum chucks, which is typically difficult to measure. The surface flatness of as-chucked wafers will be measured using XCALIBIR, a general-purpose 300 mm aperture interferometer developed at NIST, and will provide verification of industry models of wafer/chuck interactions.

Technical Strategy

 IR^2 is a prototype infrared interferometer built for NIST by Tropel, Inc., based on a NIST patent (5,739,906). The instrument can be configured to operate as a phase shifting Twyman-Green interferometer or to wavelength shift Haidinger fringes. Wafers may be measured either in a diverging wavefront or with a plane wave. The plane, or collimated, wavefront Haidinger fringe measurement technique is the current focus of the project. In this method, the planar infrared wavefront is normally incident on the wafer. A portion of the beam is reflected from the front wafer surface, while the rest passes through the wafer and reflects from the rear surface. The interference of these two wavefronts produces the Haidinger fringes and, by wavelength shifting, allows calculation of the wafer thickness variation. See Figure below. This measurement configuration is limited to double side polished wafers.

Technical Contacts: T. L. Schmitz U. Griesmann

"NIST's contributions this year to our industry have been significant and striking. They will influence decisions by IC companies such as INTEL and others, and have beneficially impacted WFSI."

T. D. Raymond

Wavefront Sciences, Inc., Albuquerque, NM



Schematic for collimated wavefront Haidinger fringe wafer thickness variation measurement.

1. There are two primary limitations to reaching the desired measurement performance using the current configuration of IR². These are the available measurement aperture and the optical imaging system. Using the collimated wavefront measurement technique, the existing measurement aperture is 150 mm. Although this aperture allows measurements to be performed and uncertainty evaluation to proceed, it is not sufficient to reach the end goal of thickness variation measurements of 300 mm diameter wafers. Additionally, it has been experimentally observed that due to large-scale geometric distortions in the free form wafers (e.g., bow or a drum shaped deflection), it is not possible to obtain data over the full measurement aperture. Instead, data dropout occurs because light does not reach the detector from certain portions of the wafer. This is due to: 1) a long path length from the objective lens to zoom lens in the imaging system; 2) non-uniform illumination over the measurement aperture, which subtracts from the available dynamic range of the detector; and 3) an asymmetric design for the objective lens. To address these needs, a Request for Proposal has been completed for a

300 mm aperture collimator and a re-design of IR^2 imaging system has been recommended.

DELIVERABLES: Award contract for collimator manufacture 3Q 2002. Complete upgrade to IR² imaging system performance 4Q 2002.

2. As mentioned in the previous item, free form wafers can exhibit significant geometric distortion. While this is not a significant problem for clamped wafer measurements, provided the wafer is fully flattened, it is an issue for the IR^2 measurements. Initial ray trace simulations have been carried out for a bowed wafer. As expected, for a wafer with uniform thickness, the effect of bow (approximately 20 μ m) on the reported thickness variation is small. However, for wafers that exhibit thickness variation a bias on the order of tens of nm can be introduced.

DELIVERABLES: Complete ray trace simulations to evaluate measurement bias introduced by bowed wafer geometry. 1Q 2003

3. A key component in the evaluation of chucked wafer non-flatness is interactions between the vacuum chuck and wafer. We will be continuing collaboration with Wavefront Sciences, Inc. (WFSI), Albuquerque, NM and potentially one or more lithographic stepper manufacturers to help understand these interactions. WFSI is carrying out numerical analyses of the chuck/wafer interface for various chuck geometries. XCALIBIR, a general purpose 300 mm aperture phase measuring interferometer developed at NIST, and the WFSI optical measurement tool will be used to measure chucked wafer flatness(es). The data can then be used to evaluate the influence of wafer/chuck interactions on the chucked wafer flatness.

DELIVERABLES: Complete flatness measurements of 200 mm and 300 mm diameter chucked wafers to help characterize interactions between vacuum chucks and wafers. 1Q 2003

Accomplishments

A drift test was carried out using a 150 mm aperture collimator that captured data from the central portion of a 200 mm diameter, 750 μ m thick, double side polished wafer. The measured optical path difference (*OPD*) was converted to thickness variation in nm using an assumed, homogeneous silicon index of 3.5. Total thickness variation (*TTV*), which includes both the constant wafer thickness as well as local and/or linear variations in thickness, was not measured here because the piston, or constant, term was considered a setup error and removed during data

analysis. Piston was removed because the OPD between the front surface and back surface reflections varies with changes in the angular orientation between the wafer and collimated source. The result of removing piston is shown schematically in the figure below, where it is seen that the contribution of the gray region to TTV is lost.



Collimator Effect of removing piston, or constant term, from measurement result.



Average of repeatability testing measurements.

The average of 192 phase measurements recorded at 15 minute intervals over a two day period is shown in the figure above. A peak-tovalley (PV) thickness variation of 1663.0 nm and root-mean-square (RMS) value of 414.4 nm were recorded over the measured aperture. Clearly, this wafer geometry is dominated by wedge, or a linear variation in thickness across the wafer face (the wafer is thinner at the top).

The (one sigma) pixel by pixel standard deviation in the 192 measurements is also shown. This result, which was dominated by stray light in the interferometer, suggests repeatability at the 6 nm level for this set of tests. Temperature was also measured; however, no strong correlation between variation in the results and temperature existed due to the high stability of the measurement cavity (i.e., the wafer).



One sigma pixel by pixel standard deviation of repeatability measurements.

A comparison of measurements of a single wafer using two different collimators was completed. The wafer was 200 mm in diameter, 750 µm thick, and double side polished. The two collimators were 150 mm aperture f/3 and 100 mm aperture f/3.3. The average of 25 measurements using the f/3 collimator with both piston and tilt removed follows. The corresponding standard deviation, with a maximum value of 2.7 nm, is also shown.



RMS = 16.9 nm, PV = 85.4 nm Average of 25 f/3 collimator measurements.

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The averaged result using the f/3.3 collimator is given below. The standard deviation map for the f/3.3 measurements was similar to the f/3 tests with a maximum of 3.3 nm. The same features are identified in both the f/3 and f/3.3 measurements, including a high spot to the right of the triangular fiducial and two low spots to the left, and similar RMS and PV values were recorded: 16.9 nm and 85.4 nm for the f/3 result and 16.0

nm and 88.0 nm for the f/3.3 result, respectively. This agreement suggests that the measured thickness variation may not be highly sensitive to the incident wavefront.

Pixel by pixel standard deviation of f/3 collimator







Average of 25 f/3.3 collimator measurements.

The potential impact of phase change on reflection from physical contact of the back side of the wafer with the support mechanism has also been investigated. This could be an area of concern depending on the chuck type, contact area, and camera resolution. Two cases were evaluated: 1) the current wafer holding mechanism for IR² using a small vacuum orifice, an 11 mm diameter o-ring seal surrounds an 8 mm diameter orifice, near the bottom edge of wafer in conjunction with two cylindrical supports; and 2) metallic coatings were applied to a 50 mm diameter wafer directly to simulate intimate contact with a metallic surface and phase maps obtained (in this case, the wafer was supported at the edges). IR² measurements in the local area of the vacuum

orifice were obtained using a 25 mm diameter, f/3 collimator for improved spatial resolution. The following figure shows the average of phase measurements performed at eight different locations on a single double side polished wafer. The effect of phase change on reflection is clearly seen as the circular change in reported thickness variation where the o-ring contacts the wafer.



Effect of phase change on reflection for IR² wafer holding mechanism.

The result for a thickness variation measurement of a 100 mm diameter, 750 μ m thick double side polished wafer follows and shows a PV thickness variation of 204 nm, where the thickness variation is manifested as 'power', or the Zernike a_2^0 term, in the phase map. This large power suggests a gradual thinning radially from the outside edge to the center of the wafer.

Surface reflection measurements of this wafer were performed using a commercial phase measuring interferometer in a Fizeau configuration. A front surface measurement showed a slightly concave shape with an a_2^0 Zernike coefficient of 4.437 waves (at a wavelength of 632.8 nm). A back surface measurement demonstrated a slightly convex shape with an a_2^0 value of 4.372 waves. The sagitta, s, for each surface can be calculated as $s = 2 \cdot a_2^0 \cdot 632.8$ (nm). The larger sag for the front (concave) surface suggests the wafer is thinner in the center, as shown by the IR² result. The sagitta for the front surface measurement was 5615 nm and 5533 nm for the back surface. The difference of these two gives an estimate of the gross thickness variation over the approximate measurement aperture of 30 mm (the smaller aperture was required to obtain reasonable fringe density for the bowed wafer and allow successful phase unwrapping). This difference is 82 nm. If this value is scaled to the

approximately 76 mm aperture for the f/3.3 IR^2 measurements, the result is 208 nm, which agrees with the IR^2 PV value and provides at least a qualitative, if not comprehensive, validation of the IR^2 result.



Thickness variation measurement for 100 mm diameter, 750 µm thick double side polished wafer (piston and tilt removed). Map shows that wafer is thinner in center by approximately 204 nm.

Collaborations

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Wavefront Sciences, Inc, T.D. Raymond; flatness measurements of free form wafers on XCALIBIR.

Virginia Semiconductor, Inc., Stephen Jones; thickness variation measurements of ultra-flat wafers.

Komatsu Silicon America, Paul Langer; 300 mm diameter wafer measurements.

Recent Publications

Schmitz, T.L., "Silicon Wafer Thickness Variation Measurements Using the NIST Infrared Interferometer," submitted to the Journal of Research of the National Institute of Standards and Technology.

Griesmann, U., Schmitz, T.L., Soons, J., Polvani, R., "New Optical Metrology at NIST for Semiconductor Lithography," ASPE Spring Topical Meeting "Progress in Precision," April 17-18, 2002, Raleigh, NC (in press).

Parks, R.E., Shao, L.-Z., Davies, A., Evans, C.J., "Haidinger Interferometer for Silicon Wafer TTV Measurement," Proceedings of SPIE, Vol. 4344, Metrology, Inspection and Process Control for Microlithography XV (2001) 496-505.

Evans, C.J., Davies, A., Schmitz, T.L., Parks, R.E., Shao, L.-Z., "Interferometric metrology of substrates for VLSI," 2nd International Conference of the European Society for Precision Engineering and Nanotechnology – euspen, "Torino Incontra" Congress Centre, Torino, Italy, (2001).

Evans, C.J., Parks, R.E., Shao, L.-Z., Davies, A., "Interferometric Metrology of Photomask Blanks: Approaches Using 633 nm Wavelength Illumination," NISTIR 6701, December, 2000.

Modeling, Measurements, and Standards for Wafer Surface Inspection

Goals

Provide industry with models, measurements, and standards for particles and other defects in order to improve the inspection of wafer surfaces. Develop facilities to accurately measure particle size and to deposit monosize particles on calibration artifacts to reduce the uncertainty in the sizes of particles used by the semiconductor industry to calibrate scanning surface inspection systems (SSIS). Investigate theoretically and experimentally the behavior of light scattering from particles, defects, and roughness on wafer surfaces.

Customer Needs

The Semiconductor Industry Association's (SIA) International Technology Roadmap for Semiconductors identifies the detection and characterization of defects and particles on wafers to be a potentially show-stopping barrier to device miniaturization. The roadmap specifies that by 2005, 43 nm particles must be detectable on bare silicon and nonmetallic films, 56 nm particles on metallic films, and 100 nm particles on wafer backsides, for which no solutions currently exist. While the detection sensitivity for defects must be increased, the ability to characterize defects in terms of size, shape, composition, etc., is critical for yield-learning. Defects must be characterized independent of defect location and topology.

With the need to detect smaller defects, the costs of inspecting wafers are skyrocketing. In order for new advances to be implemented in production environments, improvements in sensitivity must be achieved without suffering a tradeoff in throughput and must be cost-effective. The drive towards *in situ* sensors for production tools requires techniques which can be effectively miniaturized.

In order that wafer manufacturers and the device manufacturers have a common basis for comparing specifications of particle contamination, improved standards for particles are needed. A recent comparison of the measurements of calibration wafers by thirteen different SSISs indicated unacceptably large deviation between the SSIS results and the actual particle sizes. This study involved six particle sizes ranging from 88 nm to 290 nm and included the NIST SRM 1963 and two other sizes measured by NIST. For the two smallest particle sizes, 88 nm and 100.7 nm, the scanners systematically underestimated the size by about 8 %. By 2005, it is anticipated that accurate calibration particles as small as 30 nm will be needed.

By 2005, at the 80 nm node, particle having diameters 43 nm, 56 nm, and 100 nm or larger must be detectable on bare silicon and nonmetallic films, metallic films, and the backsides of wafers, respectively. No known solutions exist at this time. [2001 ITRS, Yield Enhancement, p. 8]



The Goniometric Optical Scatter Instrument is a state-of-the-art laser scattering facility.

Technical Strategy

There are two major strategies to improving the performance of scanning surface inspection systems. One strategy is to develop a fundamental understanding of optical scattering at surfaces so that tool manufacturers can optimize the performance of their instrumentation, in terms of defect detection limits and discrimination capabilities, to characterize the response of instrumentation to different types of defects, and to develop and calibrate particles of well-defined size and material. Recent work by this group has demonstrated that the polarization of light scattered by particulate contaminants, subsurface defects, and microroughness has a unique signature that can **Technical Contacts:** T. A. Germer G. W. Mulholland

"I would like to thank you and NIST for the support that you have provided to VLSI Standards in the sizing of polystyrene latex spheres through the work of Dr. George Mulholland. We are very pleased with the measurements that Dr. Mulholland has performed, and with the level of technical support that the NIST staff has provided to us. This work is of technical and economic importance to the semiconductor industry and to VLSI Standards, because the ability to correctly size ever smaller particulate contaminants on silicion substrates is key to the manufacturing yield of silicon chips. We look forward to a continuing technical relationship between VLSI Standards and NIST."

Marco Tortonese, Ph.D. VLSI Standards, Inc. be used to identify the source of scatter. In particular, it was found that small amounts of roughness do not depolarize scattered light. This finding has enabled the development of instrumentation which can collect light over most of the scattering hemisphere, while being blind to microroughness. That instrumentation, for which a patent has been awarded, should result in a factor of two improvement in minimum detectable defect size.

A second strategy is to provide leadership in the development of low uncertainty calibration particles for use in calibrating surface scanners. A major focus has been development of the differential mobility analysis (DMA) method for accurately sizing monosize polystyrene spheres. This work together with a SSIS round robin has provided evidence that current SSIS measurements have an unacceptably large uncertainty for particle sizes in the 90 nm to 100 nm size range. The technical focus of our future work will be applying the DMA for accurately sizing calibration particle sizes as small as 30 nm and developing methods for generating other types of monosize particles.

Specific project elements are defined below:

1. Polarized Light Scattering Measurements – The Goniometric Optical Scatter Instrument (GOSI) enables accurate measurements of the intensity and polarization of scattered light with a wide dynamic range, high angular accuracy, and multiple incident wavelengths (visible and UV). We measure the light scattering properties of well-characterized samples exhibiting interfacial roughness, deposited particles, subsurface defects, dielectric layers, or patterns. The emphasis is on providing accurate data, which can be used to guide the development of light scattering instruments, and to test theoretical models.

DELIVERABLES: Development, validation, and uncertainty analysis for a light scatteringbased measurement of the 100 nm PSL sphere standard (SRM 1963). 3Q 2002

Demonstrate proof of principle light scattering-based overlay measurement. 3Q 2002

Light scattering measurement of diameter of a 60 nm sphere standard and an associated uncertainty analysis. 3Q 2003

2. Theoretical Light Scattering Calculations - The focus of our theoretical work is on (a) developing models that accurately predict the polarization and intensity of scattered light, and (b) determining what information can be efficiently and accurately extracted from light scattering measurements. Approximate theories are used in conjunction with more complex techniques to gain an understanding of which parameters affect the light scattering process. Particular cases that are being analyzed include (a) scattering by defects and roughness associated with dielectric layers, (b) scattering by particulate contamination on bare and oxidized wafers, and (c) scattering by periodic structures.

DELIVERABLES: Publish, via the world-wideweb, a version of the SCATMECH library of scattering codes which contains a theory for scattering by axially-symmetric particles on surfaces. 1Q 2003



The MHPOSI enables the scattering from individual particles to be analyzed.

3. Instrument Development - A second instrument, the Multidetector Hemispherical Optical Scatter Instrument Polarized (MHPOSI) complements the capabilities of GOSI as a prototype for a production-line light scattering inspection tool. An instrument with twenty-eight fixed detection elements covering the scattering hemisphere, MHPOSI enables a determination of the differential scattering cross section, for individual particles or defects on a wafer surface. This instrument can be configured so that it is blind to interfacial roughness. Together with an understanding of the light scattering functions for different imperfections, MHPOSI has a substantially improved capability for rapidly detecting and identifying defects, particles, and microroughness on wafers.

DELIVERABLES: Perform size distribution measurements using the MHPOSI system. 4Q 2002 4. Size Distribution Measurements – Differential mobility analysis (DMA) has been shown to be capable of making accurate size measurements for the mean particle size for 100 nm monosize polystyrene spheres. There are promising results for the measurement of the size distribution for broader size distributions; however, the results are not quantitative. Work is in progress to quantify the uncertainty in the size distribution measurement and to extend the method to smaller particle sizes.

DELIVERABLES: Development of particle sizing calibration facility and documentation of measurement protocol and data analysis. 3Q 2002

Provide uncertainty estimates for moments of the size distribution for PSL spheres based on DMA measurements. 3Q 2003

5. Aerosol Generation – An aerosol must be formed typically from a liquid spray of a particle suspension before the particles can be sized by the DMA or deposited on a wafer. Work is in progress to use a variety of innovative methods for generating, shaping the size distribution of the aerosol, and depositing the particles. These include the electrospray for generating particle sizes smaller than 60 nm, impactor to remove the large size fraction of the aerosol and to deposit the particles, and an electrostatic chamber for depositing small particle sizes. Work is also in progress to generate copper particles from chemical precursors in a tube furnace.

DELIVERABLES: Publication of manuscript on the use of i.e., electrospray, pneumatic atomization, and spray pyrolysis together with size classification and electrostatic deposition for depositing monosize PSL spheres and copper particles with sizes as small as 40 nm. 1Q 2003

6. Resource on Particle Science – Over the past five years, the particle related work has included projects with SEMATECH and particle suppliers to the semiconductor industry. A number of needs by particle related companies were expressed at the NIST particle workshop including redoing the uncertainty assessments of existing particle SRMs and offering a particle sizing calibration service. Providing support for particle needs critical to the semiconductor industry will continue to be a priority. **DELIVERABLES:** Coordinate round robin to assess the performance of particle deposition systems in collaboration with the semiconductor industry. 2Q 2003



Transmission electron microscope images of 100 nm copper spheres generated by a novel spray pyrolosis method. These particles are being developed to test light scattering theories for scattering by particles on surfaces.

Accomplishments

In January 2001, A NIST-sponsored workshop entitled "Issues Related to SSIS Calibration with Polystyrene Spheres" brought together suppliers of wafers, reference particles, particle sizing and deposition equipment, and wafer inspection instruments this set the stage for developing a more responsive particle program.

• Determined that the electrospray technique can produce an aerosol having characteristics optimal for transferring particles in a liquid suspension onto wafers for particle diameters as small as 25 nm. This significant finding enables improved wafer depositions by reducing the number of contaminant residue particles, the number of doublets, and the amount of residue on the particles.

In collaboration with the University of Maryland, developed a method for generating pure copper spheres with diameters ranging from 100 nm to 200 nm. These spheres, which mimic real-world particles better than polystyrene, were used to validate particle scattering theories in conditions for which models have a higher degree of uncertainty. Measured polarization and intensity of light scattered from the copper spheres and found good agreement with the Bobbert-Vlieger theory for light scattering from a sphere above a surface.

Developed a method, based upon scattering ellipsometry, for quantifying scatter from two sources and demonstrated its use by characterizing the roughness of both interfaces of an SiO₂/silicon system. This finding establishes the validity of the light scattering models for roughness in a dielectric film, which in turn limits the detection sensitivity of SSIS instruments. The method was also used to characterize scattering from steel surfaces, demonstrating capability to distinguish between scattering from surface roughness and material inhomogeneity. The method was further used to study the scatter from an anticonformal polymer film, helping to establish the limits of validity of the scattering theory.

Developed the SCATMECH library of C++ routines for light scattering. Published the SCATMECH library, providing a means for distributing scattering models and polarized light calculations to others. From the time of its public availability in March 2000 to the end of January 2002, 647 copies of the library have been downloaded from the web. In December 2001, Version 3 was released, which contains an accurate theory for the scattering of light by a spherical particle on a surface and theories for scattering from roughness and small defects in dielectric layers.

• Extended the theory of scattering of a sphere on a surface to axially-symmetric non-spherical particles. Demonstrated that the scattering by a metal particle on a surface is extremely sensitive to the shape of the particle in the region where the particle contacts the surface. This unusual sensitivity to shape must be considered when light scattering tools classify particles for material and size.

Collaborations

Department of Chemical Engineering, University of Maryland, Professor Sheryl H. Ehrman, Validation of Scattering Theory Using Novel Monodisperse Particles.

Department of Mechanical Engineering, University of Minnesota, Professor David Pui, Generation and Measurement of Nanosize Particles.

National Metrology Institute of Japan, Dr. Kensei Ehara, Nanoparticle Metrology.

Recent Publications

Thomas A. Germer, "Measurement of Roughness of Two Interfaces of a Dielectric Film by Scattering Ellipsometry," Phys. Rev. Lett. 85 (2), 349–352 (2000). Egon Marx, Thomas A. Germer, Theodore Vorgurger, and Byong C. Park, "Angular Distribution of Light Scattered From a Sinusoidal Grating," Appl. Opt. 39(25), 4473– 4485 (2000).

Thomas A. Germer, Thomas Rinder, and Hendrik Rothe, "Polarized Light Scattering Measurements of Polished and Etched Steel Surfaces," in Scattering and Surface Roughness III, Z.-H. Gu, and A. A. Maradudin, Eds., Proc. SPIE 4100, 148–155 (2000).

Ping-Shine Shaw, Rajeev Gupta, Thomas A. Germer, Uwe Arp, Thomas Lucatorto, and Keith R. Lykke, "Material Characterization using ACR-Based Beamline at SURF III," Metrologia, 37(5), 551–554 (2000).

Thomas A. Germer, "Polarized Light Scattering by Microroughness and Small Defects in Dielectric Layers," J. Opt. Soc. Am. A 18(6), 1279–1288 (2001).

Thomas A. Germer, "Large Angle In-Plane Light Scattering from Rough Surfaces: Comment," Applied Optics 40(31), 5708–5710 (2001).

Jung Hyeun Kim, Thomas A. Germer, George W. Mulholland, and Sheryl Ehrman, "Size-Monodisperse Metal Nanoparticles Via Hydrogen-Free Spray Pyrolysis," Advanced Materials 14(7), 518–521 (2002).

Thomas A. Germer, "Light Scattering from Slightly Non-Spherical Particles on Surfaces," Optics Letters, in press (2002).

Thomas A. Germer, Rajeev Gupta, Leonard M. Hanssen, and Eric L. Shirley, "Optical Properties of Materials," Optics and Photonics News 12(2) 38–42, (2001).

Jung Hyeun Kim, Sheryl H. Ehrman, George W. Mulholland, and Thomas A. Germer, "Polarized Light Scattering from Metallic Particles on Silicon Wafers," in Optical Metrology Roadmap for the Semiconductor, Optical, and Data Storage Industries, A. Duparré and B. Singh, Eds., Proc. SPIE 4449, 281–290 (2001).

G. W. Mulholland and B. Bauer, "Nanometer Calibration Particles: What is Available and What is Needed?" J. Nanoparticle Research 2, 5–15 (2000).

K. Ehara, G.W. Mulholland, and R.C. Hagwood, "Determination of Arbitrary Moments of Aerosol size Distribution from Measurements with a Differential Mobility Analyzer," Aerosol Sci. and Tech., **32**, 434–452 (2000).

George W. Mulholland, Da Ren Chen, and David Y.H. Pui, "Comparison of the Size Distribution of Polystyrene spheres Produced by Pneumatic and Electrospray Nebulization," in *Characterization and Metrology for ULSI Technology: 2000 International Conference*, D. G. Seiler, A. C. Diebold, T. J. Shaffner, R. McDonald, W. M. Bullis, P. J. Smith, and E. M. Secula, eds., Proc. AIP **550**, 322– 326 (AIP, New York, 2001).

Junghyeun Kim, Sheryl H. Ehrman, George W. Mulholland, Eric B. Steel, and Thomas A. Germer, "Method for Making Spherical Pure Metal Micro and Nanoscale Powders by Spray Pyrolysis," Provisional United States Patent, filed January 26, 2001.

Goals

We will develop new generations of x-ray spectroscopy tools to meet the materials analysis needs of the semiconductor manufacturing industry. Energy-Dispersive Spectrometers (EDS) based on microcalorimeters have the ability to detect photons with high energy resolution and near-unity quantum efficiency. Using these tools, a wide range of materials analysis problems can be solved. In semiconductor manufacturing, improved X-ray materials analysis is needed to identify nanoscale contaminant particles on wafers and to analyze very thin layers of materials and minor constituents. Microcalorimeter EDS improves the spectral resolution by one to two orders of magnitude compared to the semiconductor Si-EDS, the existing industry standard. Such improved resolution combined with energy dispersive operation makes possible direct spectral separation of most overlapping peaks often encountered with Si-EDS in complex multi-element systems. The improved resolution of the microcalorimeter EDS also increases the peak-to-background ratio. Peak shape and shift can be studied to reveal chemical state information. Developing arrays of x-ray microcalorimeters will enable the acquisition of high statistics

spectra in reduced time, improving the efficiency and statistical quality of existing materials analysis applications. Further, large-format arrays (up to 1,000 pixels) will make it possible to chemically analyze smaller features and trace constituents, and to track rapidly evolving x-ray spectra for in-process and process-stream monitoring.

The microcalorimeter EDS detector invented at NIST consists of a superconducting thermometer (a superconducting transition-edge sensor (TES)) and an x-ray absorber fabricated on a micromachined Si₃N₄ membrane, and cooled to cryogenic temperatures (0.1 K). When x-rays are absorbed in the detector, the resulting heat pulse in the microcalorimeter is measured by the TES thermometer. The change in the temperature of the thermometer is measured by a superconducting quantum interference device (SQUID) amplifier. The temperature pulse height gives a measurement of the energy of the x-ray photon one to two orders of magnitude more sensitive than Si-EDS. The detector is cooled to 0.1 K by a compact adiabatic demagnetization refrigerator,

which has unique design features that produce nearly 24 hours of continuous operation, and days of hold time for liquid helium.

Customer Needs

Improved x-ray detector technology has been cited by SEMATECH's Analytical Laboratory Managers Working Group (ALMWG, now ALMC) as one of the most important metrology needs for the semiconductor industry. In the International Technology Roadmap for Semiconductors, improved x-ray detector technology is listed as a key capability that addresses analysis requirements for small particles and defects. The transition-edge sensor (TES) microcalorimeter xray detector developed at NIST has been identified as a primary means of realizing these detector advances, which will greatly improve in-line and off-line metrology tools that currently use semiconductor energy-dispersive spectrometers (EDS). At present, these metrology tools fail to provide fast and unambiguous analysis for particles less than approximately 0.1 mm to 0.3 mm in diameter. Improved EDS detectors such as the TES microcalorimeter are necessary to extend the capabilities of existing SEM-based instruments to meet the analytical requirements for future technology generations. To make this technology available to the semiconductor industry and other materials analysis communities. NIST has licensed several patents for commercialization. With commercialization and continued development, microcalorimeter EDS should be able to meet both the near-term and the longer-term requirements of the semiconductor industry for improved particle analysis.

Promising new technology such as high energy resolution X-ray detectors must be rapidly commercialized. Prototype microcalorimeter energy dispersive spectrometers (EDS) and superconducting tunnel junction techniques have X-ray energy resolution capable of separating overlapping peaks and providing chemical information. These advances over traditional EDS and some wavelength dispersive spectrometers can enable particle and defect analysis on SEMs located in the clean room. 2001 International Technology Roadmap for Semiconductors Technical Contacts: K. D. Irwin

- G. C. Hilton
- S. W. Deiker
- S. W. Nam
- C. D. Reintsema
- L. R. Vale

"[T]his type of resolution, very simply, was something that I thought was truly, truly a dramatic advance. And I really would like to encourage the people working on this at NIST and the equipment industry to get this into commercialization as soon as they possibly can."

Mark Melliar-Smith, Former President and Chief Executive Officer of SEMATECH

Technical Strategy

1. The usefulness of single-pixel x-ray microcalorimeter EDS in materials analysis has now been well established in a variety of demonstration experiments. To meet the needs of the semiconductor industry, it is necessary to make microcalorimeter EDS systems more widely available. Introducing this radically new technology requires transferring an entire measurement instrument. In addition to the microcalorimeter, the system requires novel superconducting electronics to instrument the detector, compact adiabatic demagnetization refrigerators to simplify cooling to milliKelvin operating temperatures, and custom room-temperature electronics and software to process the output signals. Our goal is to develop new detector systems, to transfer them to the Chemical Science and Technology Laboratory (CSTL) in NIST Gaithersburg for collaborative use in studying problems of interest to the industry, and to provide support to companies commercializing the technology.



NIST x-ray microcalorimeter system on a scanningelectron microscope. The system was developed in the Electronics and Electrical Engineering Laboratory (EEEL) at NIST, Boulder, and transferred to the Chemical Science and Technology Laboratory (CSTL) at NIST Gaithersburg to be used to study problems of interest to the semiconductor industry.

DELIVERABLES: Provide support for the complete prototype microcalonimeter system recently transferred to CSTL. Collaborate with CSTL on using the microcalorimeter to study problems of interest to the semiconductor industry. 4Q 2002.

DELIVERABLES: Provide technology transfer support to the companies commercializing microcalorimeter technology. 3Q 2002

2. For many semiconductor materials analysis problems, further improvements in energy resolution (beyond that already demonstrated with these detectors) are not as important as an increase in the maximum count rate and collection area. Both the collection area and count rate can be improved by the implementation of multipixel arrays of detectors. Small arrays of several widely spaced pixels can be instrumented with separate readout channels, leading to modest improvement in count rate and collection area, improving the statistics and data acquisition time.

DELIVERABLES: Fabricate, instrument and test a small array of x-ray microcalorimeter detectors to demonstrate the increase in collection area and count rate achievable through arrays. 4Q 2002

3. Eventually, the development of much larger format arrays will be required to meet the materials analysis needs of the semiconductor industry. Arrays of 1,000 closely packed pixels would provide high-energy-resolution EDS with large collection area (> 50 mm²) and high maximum count rates (> 100,000 cps). Novel fabrication techniques will be needed to make large-format, densely packed arrays, and to enable the extraction of electrical leads from the detector array. We are developing surface micromachining approaches to meet this need.

DELIVERABLES: Demonstrate the fabrication of a small, densely packed array of microcalorimeters using surface micromachining techniques. 4Q 2002.

4. The superconducting electronics to read out large-format arrays must also be created. Due to constraints on wiring complexity, the signals from many pixels must be multiplexed at cryogenic temperatures. We are developing multiplexers using superconducting quantum interference devices (SQUIDs) to meet this need. Using SQUID multiplexers it will eventually be possible to instrument a kilopixel array of microcalorimeters with only 32 output channels.

DELIVERABLES: Demonstrate the multiplexing of a small number of x-ray microcalorimeters using SQUID multiplexers. 4Q 2002.

5. Room-temperature digital electronics and software must be developed to drive and provide feedback signals to the SQUID multiplexers, and to acquire data from the multiplexed x-ray microcalorimeters. To meet this need, we have developed custom electronics including a digital signal processor card with an analog-to-digital converter to measure the signal from the superconducting electronics and a digital-to-analog converter to apply the feedback signal, cards to provide the address signals to the multiplexer, preamplifier cards, clock cards, and custom PCI cards to interface to a control computer. We now must develop the firmware and software to drive the SQUID multiplexer.

DELIVERABLES: Develop the firmware and software to drive SQUID multiplexers and acquire data from an array of microcalorimeters. Demonstrate the operation of a SQUID multiplexer chip using our custom digital electronics, and the new firmware and software. 3Q 2002.

Accomplishments

Transferred a complete prototype microcalorimeter EDS system from EEEL in NIST, Boulder to CSTL in NIST, Gaithersburg. The microcalorimeter system has been successfully implemented on a CSTL analytical scanning electron microscope in Gaithersburg. The microcalorimeter will be used initially by CSTL scientists for a program of basic x-ray spectrometry to establish better values of weights of lines of complex Land M- family x-rays in the 200 eV to 3 keV range. This improved spectral database is vital for the next stage in developing a systematic approach to low energy x-ray microanalysis.





Demonstrated a novel SQUID multiplexing circuit designed to multiplex the readout of largeformat arrays of x-ray microcalorimeters. The circuit consists of 32 SQUIDs connected to one output channel. The circuit will allow 32 x-ray microcalorimeters to be read out using only one output channel, making it possible to instrument large arrays. We have tested the circuit and found it to work well.



Photograph of part of a 32-channel SQUID multiplexer chip fabricated at NIST to instrument microcalorimeter EDS arrays.

Fabricated surface-micromachined structures suitable for the development of densely packed arrays of microcalorimeters. These structures consist of a silicon nitride membrane "floating" 2 microns above a solid silicon substrate, and connected to it by small silicon nitride legs. This is in contrast to our usual bulk micromachining technique, in which a silicon nitride membrane is deposited on a silicon wafer, and all silicon below it is removed through the entire thickness of the wafer. If single pixel microcalorimeters were fabricated on a floating membrane, the device would be much more robust than a bulk micromachined structure, since the bulk micromachining weakens the entire silicon wafer. Further, it is possible to route electrical leads below the suspended silicon nitride membrane to connect them to the amplifiers.



A 6x6 array of suspended silicon nitride platforms created using surface micromachining at NIST. Platforms like these will be used to thermally isolate microcalonmeter pixels in a densely packed array. The electrical leads can be routed beneath the platforms.

The NIST microcalorimeter EDS holds the world record for energy resolution for an EDS xray detector of 2.0 eV at 1500 eV, which is over 30 times better than the best high resolution semiconductor-based detectors currently available. This energy resolution was measured using a glass prepared by Dale Newbury of NIST to use as a test standard for EDS.



The Al-K α region of a microcalorimeter EDS spectrum of the multielement NIST K3670 glass. The acquired spectrum is shown as well as a weighted least-squares fit of the Al K α and satellite lines convolved with a Gaussian instrument response, yielding an energy resolution of 2.0 eV \pm 0.1 eV FWHM.

We created a chemical shift map showing the chemical bonding state of Al in a sample containing both Al and Al₂O₃. An aluminum film was deposited on part of a sapphire substrate. A microcalorimeter EDS was used to measure the x-ray spectrum as the electron beam was rastered to form the SEM image. The Al x-ray line position was shifted by a small amount (about 0.2 eV) in the regions containing Al₂O₃ as compared to the regions containing elemental Al. The high energy resolution of the microcalorimeter allowed the shift to be measured, resulting in the false-color image below. The map clearly demonstrates that microcalorimeter EDS can be used to discriminate the chemical bonding state using shifts in the positions of x-ray lines. The result also highlights the need for large-format arrays to increase the data-collection rate. The image shown here was acquired over several hours. Images such as this could be acquired much more quickly and with much sharper position resolution using an array microcalorimeter.





SEM photo (top) of an aluminum film partially covering a sapphire substrate and a false-color map (bottom) of the shift in the mean x-ray energy of the Al K α peak taken using a microcalorimeter EDS system. The shift in energy is due to the chemical bonding of the aluminum with the oxygen. The average energy shift is ~0.2 eV.

In collaboration with researchers at SUNY Albany, we used our microcalorimeter EDS system to analyze ultra-thin TaSiN films used as ion diffusion barriers in sub-0.1 micrometer integrated circuit interconnect structures. In conventional Si-EDS, the overlap of the Si K α and Ta M α , β lines makes it difficult to characterize TaSiN films. The thinnest film analyzed, 3.5 nm, was easily measurable. This result shows that microcalorimeter EDS is an effective tool for the characterization of ultra-thin barrier films used in microelectronics, and highlights it potential for quantitative microanalysis.



Microcalorimeter EDS spectrum ofTaSiN films of different thickness on a silicon substrate. The high energy resolution of the microcalorimeter enables the line separation. Even a 3.5 nm thick film is easily measured.

Collaborations

Chemical Science and Technology Laboratory, NIST, Gaithersburg, Terry Jach, Lance King, Dale Newbury, John Small, and Eric Steel, the development of microcalorimeter EDS systems.

SUNY Albany Institute for Materials, Robert E. Geer, EDS analysis of diffusion barriers.

Recent Publications

Irwin, K.D., "SQUID Multiplexers for Transition-Edge Sensors" (review), Physica C, 368, 203 (2002).

Geer, R.E.; Wu, D.; Wollman, D.A., "High-Resolution Energy-dispersive X-ray Spectroscopic Analysis of Ultrathin lon Diffusion Barriers Using Microcalorimetery," Journ. Appl. Phys., **91**,1099 (2002).

Irwin, K.D., Vale, L.R., Bergren, N.E., Deiker, S., Grossman, E.N., Hilton, G.C., Nam, S.W., Reintsema, C.D., and Rudman, D.A., "Time-Division SQUID Multiplexers," Proc. 9th International Workshop on Low-Temperature Detectors, AIP Conf. Proc. 605, 301 (2002).

Geer, R.E.; Wu, D.; Wollman, D.A., "High-resolution EDS Analysis of Ultra-Thin TaSiN Diffusion Barriers for Cu Metallization Using Microcalorimetry," Proc. IEEE 2001 Int'l Interconnect Tech. Conf., 192-194 (2001).

Nam, S.W.; Wollman, D.A.; Newbury, D.E.; Hilton, G.C.; Irwin, K.D.; Rudman, D.A.; Deiker, S.; Bergren, N.F.; Martinis "Progress Towards Arrays of Microcalorimeter Xray Detectors," J.M., Microscop. & Microanal. 7 (Suppl. 2: Proc.), 1050-1051 (2001).

Deiker, S.; Chervenak, J.; Hilton, G.C.; Irwin, K.D.; Martinis, J.M.; Nam, S.; Wollman, D.A., "Transition Edge Sensor Array Development," IEEE Trans. Appl. Supercond. 11, 469-472 (2001).

Hilton, G.C.; Martinis, J.M.; Irwin, K.D.; Bergren, N.F.; Wollman, D.A.; Huber, M.E.; Nam, S.W., "Microfabricated Transition-Edge X-ray Detectors," IEEE Trans. Appl. Supercond. 11, 739-742 (2001).

Irwin, K.D.; Hilton, G.C.; Martinis, J.M.; Deiker, S.; Bergren, N.F.; Nam, S.W.; Rudman, D.A.; Wollman D.A, "A Mo-Cu Superconducting Transition-Edge Microcalorimeter with 4.5 eV Energy Resolution at 6 keV," Nuclear Instrum. and Methods in Physics Research A 444, 184-187 (2000).

Wollman, D.A.; Nam, S.W.; Newbury, D.E.; Hilton, G.C., Irwin, K.D.; Bergren, N.F.; Deiker, S.; Rudman, D.A.; Martinis,J.M., "Superconducting Transition-Edge-Microcalorimeter X-ray Spectrometer with 2 eV Energy Resolution at 1.5 keV," Nucl. Instrum. and Methods in Phys. Res. A 444, 145-150 (2000).

Wollman, D.A.; Nam, S.W.; Hilton, G.C.; Irwin, K.D.; Bergren, N.F.; Rudman, D.A.; Martinis, J.M.; Newbury, D.E., "Microcalorimeter Energy-Dispersive Spectrometry Using a Low Voltage Scanning Electron Microscope," J. Microscopy 199, 37-44 (2000).

Nam, S.; Wollman, D.A.; Hilton, G.C.; Chervenak, J.; Deiker, S.; Irwin, K.D.; Martinis, J.M., "A Digital Readout Scheme for Arrays of Microcalorimeter X-ray Detectors," Proc. Microscopy and Microanal. 2000, 742-743 (2000).

Wollman, D.A.; Newbury, D.E.; Nam. S.W.; Hilton, G.C.; Irwin, K.D.; Rudman, D.A.; Deiker, S.; Bergren, N.F.;Martinis, J.M., "Microcalorimeter EDS: Benefits and Drawbacks," Proc. Microscopy and Microanal. 2000, 738-739 (2000).

Chervenak, J.A., Grossman, E.N., .Irwin, K.D., Martinis, J.M., Reintsema, C.D., Allen, C.A., Bergman, D.I., Moseley, S.I., Shafer, R., "Performance of multiplexed SQUID readout for Cryogenic Sensor Arrays," Nuclear Instruments and Methods in Physics Research A 444, 107 (2000).

Stahle, C.K., McCammon, D., Irwin, K.D. "Quantum Calorimetry," Physics Today 52, 32 (1999). **Technical** Contacts: John Hurly Michael R. Moldover

"I was pleasantly surprised when I came across your database of thermophysical properties of gases used in the semiconductor industry.

It was virtually, exactly what I was searching for."

Bob Rathfelder

Project Engineer, Parker Hannifin, Central Engineering.

Thermophysical Property Data for Modeling CVD Processes and for the Calibration of Mass Flow Controllers

Goals

NIST will measure the thermophysical properties of the gases used in semiconductor processing. The property data will improve the modeling of chemical vapor deposition (CVD) and the calibration of mass flow controllers (MFCs). As data are acquired, they are promptly being posted as part of an online database at http://properties.nist.gov/semiprop. (Fig. 1.) The gases and the properties to be studied were identified by industry representatives. The gases include process gases, "surrogate" gases used for calibration, and binary mixtures of process and carrier gases. The required properties include: speed-of-sound, heat capacity, density (equation of state), viscosity, and thermal conductivity. Industry representatives have also recommended targets for the accuracy of the data.

Customer Needs

The Modeling and Simulations section of the 2001 International Technology Roadmap for Semiconductors lists "Materials Modeling" as first in a list of "Technology Requirements." The Roadmap states that "Modeling and simu-

lation tools in equipment, process, device, package, patterning, and interconnect are only as good as the input materials parameters. In many cases these parameters are not known. Databases that contain both experimental and, calculated are needed." The Roadmap states that continuing research is needed to obtain experimental data for "transport and thermal constants." This project will generate transport and thermodynamic property data for



Figure 2. Components of a generic mass flow controller (MFC) and the themophysical properties required to model them.

Tungsten Hexafluoride					M.W. [1]	N.B.P. [2]	T.P. [2] 275.0 K	
					P. [3]	T. [3]	V. [3]	
W1.6	ala timbre in manifesta and a sectore a la superiore de la sectore de la sectore de la sectore de la sectore d	anne a thair ann an tha a thair an thair a thai	ร้าง เริ่ามีเรียงเรื่อง เริ่ามีเรียงเรื่อง	4.57 MPa	452.7 K 0.1 m ³ /kmol			
atum to [Gas]	Index Fluid Se	ience Group	Process Mea	asurements Divisio	on NIST Home	SEMI NSMP	1	
T	$C_p^0(T)$	Vapor	B(T)	dB/dT	C(T)	dC/dT	2	17
R	R	MPa	cm ³ ·mol ⁻¹	cm ³ ·mol ⁻¹ ·T ⁻¹	em ⁶ -mol ⁻²	cm ⁶ -mol ⁻³ .T ¹	mWi(m·K)	µPa•ı
Estimated Uncertainty	1%/	1%	Gas densities are calculated to better than 0.1% over the temperature and pressure ranges of the reference.			10%	10%	
Reference	[4]/	[6]	[5]	[5]	[5]	[5]	[5]	[5]
205	11.84	0.19	-2001.6	59512	-4658932	47121716		-
210	12.00	0.34	-1864.5	5441.0	-3653771	36754361		
215	12 16	0.58	-1741 8	4994 1	-2884907	28924191	52	14 1
220		0 95	-1631.6	4600.8	-2291407	22949084	5.4	14 41
225		1.53	-1532 2	4252.9	-1829413	18345717	5.6	14.64
		2.39	-1442.1	3943.9	-1466994	14767456	57	14.88
230	1 11 11 21 11 12						The state is a second of the state of the st	and have been been made and

Figure 1 Sample Web Page from database located at the URL http://properties.nist.gov/semiprop/

the gases used in semiconductor processing. The data will be useful for equipment modeling in CVD processes and the data will also provide a rational basis for the calibration of MFCs used to meter process gases.

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Figure 2 shows the components of a generic MFC and the thermophysical properties required to model their performance. During May, 2000, a workshop entitled "Mass Flow Measurement and Control for the Semiconductor Industry" was organized at NIST by Dr. Robert Berg. At the workshop, representatives of industry identified the gas properties and their allowable uncertainties which are required for accurately modeling MFCs and related equipment. The workshop's list of properties is: heat capacity at constant pressure $C_p(T)$ (±0.1 %), equation of state $\rho(T,p)$ for predicting gas densities (±0.1 %), viscosity $\eta(T)$ (±0.5 %), and thermal conductivity $\kappa(T)$ $(\pm 0.5 \%)$. The workshop urged that values of these properties be made available from a 'standard' source that is accessible to all of the industries associated with semiconductor processing.

Technical Strategy

In the first phase of the work, NIST is measuring the speed of sound u(T, p) in process gases and in the surrogate gases that are often used for calibration. The speed-of-sound data have standard uncertainties of $0.0001 \times u$. The initial results range up to 200 °C and from 25 kPa to 1500 kPa (or to 80 % of the vapor pressure for condensable gases). As an example, Figure 3 shows the phase diagram of trimethyl gallium. Each triangle on Figure 3 indicates values of u(T, p) where a speed-ofsound measurement was made. The speed-ofsound data were used to determine the ideal-gas heat-capacities $C_p^0(T)$ with the targeted uncertainty of $0.001 \times C_p^0$. The pressure and temperature-dependence of u(T, p) were correlated with model two-body and threebody intermolecular potentials. These potentials are used to calculate the virial equation of state $\rho(T, p)$ and to get first estimates of the viscosity $\eta(T)$ and the thermal conductivity $\kappa(T)$. For gases where reliable data exist, we verified that results calculated in this way have uncertainties that are less than $0.001 \times \rho$, $0.1 \times \eta$, and 0.1×k from 200 K to 1000.

In parallel with measuring the speed of sound, NIST is developing novel acoustic techniques to measure the viscosity and thermal conduc-



Figure 3. Phase diagram of trimethyl gallium. The vapor pressure is represented by the curved line which ends at the critical point: $T_c \approx 510$ K and $\rho_c \approx 4.4$ MPa. At each triangle, the speed of sound was measured.

tivity with uncertainties of less than 0.5 % as specified by the Mass Flow Controller Workshop. Throughout the project, the results will be made available to the customers through publications in professional journals, presentations at professional meetings, and via an online data base accessible through the internet at http://properties.nist.gov/semiprop.

DELIVERABLES: Design and fabricate a facility capable of measuring the speed of sound in the hazardous gases utilized in semiconductor processing. Completed 2Q 2000.

1. NIST has already developed techniques to accurately measure the speed of sound in gases and to determine the ideal-gas heat-capacity and the equation of state from the u(T, p) data. NIST used these techniques to determine the thermodynamic properties of alternative refrigerants. Because the alternative refrigerants are inert and non-hazardous by design, modifications are needed to study the reactive, corrosive, and/or toxic gases used in semiconductor processing. These modifications address the issues of safety, sample purity, sample disposal, and materials compatibility.

DELIVERABLES: Develop and optimize novel acoustic techniques for measuring the transport properties of semiconductor process gases. Viscometer designed, fabricated and optimized by 1Q 2002, thermal conductivity device designed by 2Q 2002, fabricated by 4Q 2002, and optimized by 2Q 2003.



Figure 4. Speed of sound in tungsten hexafluoride as a function of pressure along isotherms.

2. Because conventional measurements of the transport properties of dilute, corrosive gases are difficult, we are developing acoustical methods of measurement. As suggested by M. Greenspan, the acoustical viscometer is a double Helmholtz resonator. The viscosity is deduced from the viscous damping of gas oscillating at acoustic frequencies through a tube joining two chambers. A second resonator will be developed to obtain the thermal conductivity from measurements of the thermal losses of similar oscillations.

DELIVERABLES: Design and fabricate a facility capable of safely measuring the transport properties in the hazardous gases utilized in semiconductor processing. Facility installed by 1Q 2002, viscometer installed in facility by 2Q 2002, automation software written and tested by 3Q 2002, design and fabricate hazardous gas viscometer by 3Q 2002, install hazardous gas viscometer by 4Q 2002, design and fabricate hazardous gas thermal conductivity device by 2Q 2003.

3. A second facility to measure the transport properties will have to be fabricated taking into account the same issues of safety, sample purity, sample disposal, and materials compatibility as for the speed-of-sound facility.

DELIVERABLES: Measure the speed of sound in the semiconductor process gases identified by the customer. From the speed-

of-sound measurements determine the idealgas heat-capacity and equation of state for each species. Nitrous oxide by 1Q 2002, Nitric Oxide by 2Q 2002, Octafluoro-cyclobutane by 4Q 2002.

DELIVERABLES: Measure the transport properties in the semiconductor process gases identified by the customer. C_2F_4 by Q3 2002, CF₄ by 4Q 2002, SF₆ by 1Q 2003, NO by Q2 2003, NO₂ by 3Q 2003.

4. Once the two facilities have been fabricated, calibrated and safety assessments performed the actual measurements in the semiconductor process gases identified by the customers will

Table 1. Ranges of speed-of-sound data for process gases.

	Temperature Range (K)	Maximum Pressure (kPa)
Cl	260 - 440	1,500
HBr	230 - 475	1,500
BCl ₃	300 - 460	1,500
WF ₆	290 - 420	300
C_2H_4O	285 - 440	1,000
NF ₃	200 - 425	1,600
Ga(CH ₃) ₃	340 - 420	900
N ₂ O	220 - 460	1,600
NO	200 - 450	1,600

be performed.



made in the Greenspan viscometer from the reference values in several gases.



Figure 6. Monel Greenspan acoustic viscometer for use with corrosive process gases.

DELIVERABLES: Disseminate the resulting measurements to the customer. Update online database by 4Q 2002, publish measurements in Cl₂ by 1Q 2002, publish measurements in Ga(CH₃)₃, C₂H₄O, and NF₃ by 3Q 2002, publish measurements in NO and NO₂ by 1Q 2003.

5. The measurements will be disseminated to the customer through papers in professional journals, talks given at professional meetings, and on an on-line database available via the internet.

Accomplishments

• A facility was built to safely measure the speed of sound in semiconductor process gases. The apparatus was calibrated with argon. The speed of sound was measured in the surrogate gases CF_4 , C_2F_6 and SF_6 .

• Computer programs were developed for correlating speed-of-sound data with model, hard-core Lennard-Jones intermolecular potentials. Programs were developed to calculate second and third virial coefficients and transport properties from the model intermolecular potentials.

• The speed of sound was measured in the process gases Cl_2 , HBr, BCl_3 , WF_6 , $Ga(CH_3)_3$, NF_3 , C_2H_4O , NO, and N_2O throughout the temperature and pressure ranges listed in Table 1. Figure 4 shows a fraction of the results for WF_6 . Typically, the standard uncertainty of the speed of sound was less than 0.01 %. The ideal-gas heat-capacity was determined to within 0.1 % from the zero-pressure intercept of each isotherm. The slope and curvature of each isotherm provided information about each gas's non-ideality from which we developed an equation of state to predict the gas's densities to within 0.1 %. This year we will

complete measurements in C_4H_6 and octa-fluoro-cyclobutane.

• The Greenspan acoustic viscometer was developed to measure the viscosity of process gases. Several viscometer geometries and acoustic models were tested to optimize the viscometer's performance. The performance of the acoustic viscometer was tested by comparing the acoustic results for several gases with reference data from the literature. Figure 5 shows that the data from the acoustic viscometer are within 0.5 % of the from reference values. This year we plan to measure the viscosity in the three surrogate gases CF₄, C₂F₆ and SF₆ as well as a hazardous semiconductor gas to be determined.

• A second generation Greenspan viscometer has been designed and will be assembled this year. The new version is being constructed out of Monel which will allow the study of the corrosive process gases. Figure 6 shows the parts of the new resonator before their final assembly.

• A database available on the internet at the URL <u>http://properties.nist.gov/semiprop/</u> has been developed (Figure 1). This data base is updated regularly to give our customers immediate access to our results.

Recent Publications

Hurly, J. J., "Thermophysical Properties of Gaseous CF_4 and C_2F_6 from Speed-of-Sound Measurements," *International Journal of Thermophysics*, Vol 20, No 2, 455-484, September 1999.

Hurly, J. J., and Moldover, M. R., "Thermophysical Properties of Process Gases," Proceedings of SEMICON West 1999.

Hurly, J. J., "Thermophysical Properties of Gaseous HBr and BCl₃ from Speed-of-Sound Measurements," *International Journal of Thermophysics*, Vol.21, No. 4, 805-829, July 2000.

Hurly, J. J., "Thermophysical Properties of Gaseous Tungsten Hexafluoride From Speed-of-Sound Measurements," *International Journal of Thermophysics*, Vol. 21, No. 1, 185-206, January 2000.

Hurly, J. J., "A Progress Report: Thermophysical Properties of Semiconductor Manufacturing Process Gases," Proceedings of SEMICON West 2000.

Hurly, J. J., "The Thermodynamic Properties of Chlorine From Speed-of-Sound Measurements," Vol. 23, No. 3, 667-695, May 2002.

J. J. Hurly, "Thermophysical Properties of Nitrogen Trifluoride, Ethylene Oxide, and Trimethyl Gallium from Speed-of-Sound Measurements," Vol. 23, No. 2, 455-475, March 2002. M. R. Moldover, K. A. Gillis, J. J. Hurly, J. B. Mehl, and J. Wilhelm, "Chapter 10. Acoustic measurements in gases.", in Modern Acoustical Techniques for the Measurement of Mechanical Properties, edited by Moises Levy and Henry E. Bass, pp 377-427 (Academic Press, San Diego, USA, 2001); also "Chapter 12: Acoustic measurements in gases: Applications to thermodynamic properties, transport properties, and the temperature scale", Vol IV, in Handbook of Elastic Properties of Solids, Fluids, and Gases, edited by M. Levy, H. Bass, and R. Stem, pp 329-370 (Academic Press, San Diego, USA, 2000).

J. Wilhelm, K. A. Gillis, J. B. Mehl, and M. R. Moldover, An improved Greenspan viscometer, Int. J. Thermophysics, Int. J. Thermophysics, Vol 21, pp. 983-997 (2000).

List of Talks/ Presentations

J. J. Hurly: "Progress Report: Thermophysical Properties of Semiconductor Manufacturing Process Gases," delivered to the Gas Distribution Systems Working Group, Sunday July 15, at the SEMICON west 2000 conference in San Francisco, CA.

J. J. Hurly: "Thermophysical Properties of Semiconductor Process Gases," delivered to the European SEMI Technical Gas Committee, September 21, at Oostende Belgium.

J. J. Hurly: "Thermophysical Properties of Semiconductor Process Gases Determined with Acoustic Techniques," delivered at the Fourteenth International Symposium on Thermophysical Properties, June 28, 2000.

Advanced IC Interconnects – Process Metrology and Models

Goals

Develop metrologies and process models that address key issues in development of low dielectric constant films, copper metallization, and diffusion barrier systems in advanced semiconductor manufacturing.

Customer Needs

To achieve higher operating frequencies, future generation devices will use interconnect strategies based on inter-level dielectric films having dielectric properties lower than that of silicon dioxide with copper is, as the interconnection metal itself separated by diffusion barrier material(s) to minimize or eliminate copper diffusion. Lo K films are composed of a number of materials systems most of which are porous. Thickness requirements (<10 nm) for barrier layers in the sub-100 nm nodes implies the use of atomic layer deposition processes. A variety of metrology needs are associated with the use of Low K materials at sub-100 nm features dimensions. Although recent advances in the electrochemical deposition processes currently used for copper deposition are anticipated to meet deposition needs below 100 nm feature sizes, their use requires a copper seed layer to operate effectively. The currently used physical vapor deposition of seed layers is anticipated to not be useful below 100 nm feature sizes where aspect ratios of 10:1 or greater are planned. CVD copper is a leading process candidate for seed layer deposition. The 2001 ITRS identifies the need to develop materials and process modeling and simulation for barrier layer and copper fill, Interconnect Section page 23, Modeling and Simulation Section pages 8,9.

Technical Strategy

This project is evolving from pervious efforts to support development of process models for gas phase formation of particulates in process reactors, particularly during CVD processes. The tools developed during a previous project are being turned toward the interconnect issues we anticipate for future device generations. The following is a review of particle formation modeling and model validation efforts. Technical Strategy – Micro-Contamination Models and Validation

Both experimental and modeling expertise have been developed to address formation issues at the sub-50 nm particle size resulting in 1 and 2 dimensional models combining thermal decomposition chemical models with fluid and particle transport. The current understanding of particle formation and transport in this size range is extremely limited. These particles are primarily gas-phase generated as opposed to the larger particles that may enter the reactor in the process stream or flake off equipment surfaces. A more fundamental understanding of the physics/chemistry of gas-phase generated particles supports improved strategies to attain particle control in this size regime and will underpin the development of the micro-contamination models that are necessary for particle control in thermal CVD reactors.

1. The approach being employed here is to carry out a combined numerical/experimental effort in which particle dynamics are probed optically in a rotating disk CVD reactor in close coordination with the development of several microcontamination models. This type of synergistic multimode approach is optimal for achieving an enhanced understanding of the basic physics and chemistry that underlies the micro-contamination phenomenon. The rotating disk configuration is ideal for this type of study because of its simple and well-defined flow in which particles form in a highly accessible region of the reactor.

An optically-accessible rotating disk CVD reactor has been constructed and installed for detailed experimental investigation of micro-contaminants. This reference reactor can achieve a substrate temperature of up to 1300 K and a rotation rate of 1000 rad/s. Silicon CVD can be performed at the purity levels required for microelectronics fabrication. Raman spectroscopy is utilized for *in situ* temperature measurements in this reactor, while light scattering is employed to observe particle behavior.

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Technical Contacts:

R. W. Davis

J. E. Maslar

D. R. Burgess



Two micro-contamination models are being developed in close conjunction with the experimental effort. These models are based on aerosol dynamics algorithms for particle formation, growth and transport. One model employs a onedimensional formulation valid in the central region of the reactor. This model is operational and, due to the reduction in spatial dimensions, employs a sophisticated kinetics mechanism. A second model still in development is a full twodimensional axisymmetric formulation that will enable the prediction of particle behavior anywhere in the reactor. The 1-D model supports a more complex chemical model than does the axisymmetric model. Both provide valid methods for simulation of copper CVD.

Experimental data are being compared with results from these models in order both to validate them and to help guide the experiments. The figure on the next page shows a typical numerical/experimental comparison involving reactor centerline temperature profiles for two values of the disk rotation rate. The agreement between the two types of profiles is seen to be excellent.

DELIVERABLES: Experimentally-validated microcontamination models for the rotating disk reactor. 1Q 2003

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2. An important aspect of this project is the calculation, estimation, and dissemination of fundamental thermo-chemical and chemical kinetic properties of organometallic compounds.

These compounds are used during manufacturing processes to deposit metals in semiconductor, optical, fuel cell, MEMS, and NEMS devices. The thermo-chemical properties and reaction kinetics of most useful organometallic compounds and related molecular precursors are poorly characterized. This project obtains these properties through three activities involving theoretical estimations and modeling studies. The first data activity, which is in coordination with the Standard Reference Data Program, compiles evaluates currently available thermoand chemical data of organometallic compounds and related precursors. This data will become available through an external NIST website. The second activity supplements available data by using *ab initio* and semi-empirical calculations to develop reaction mechanisms from computed molecular structures, thermodynamic properties and spectroscopic properties of Group III and Group V compounds. The third activity utilizes the experimental and computed thermo-chemical and chemical kinetic data to develop mechanisms for the decomposition of organometallic precursors. These mechanisms are then utilized in reacting flow models of the rotating disk CVD reactor.

DELIVERABLES: Web-based thermochemical and chemical kinetic database for organometallic compounds and related precursors. 3Q 2003

Accomplishments

New Full Axisymmetric Microcontamination Model - Significant progress has been made toward development of a full two-dimensional axisymmetric microcontamination model. This enhanced model will be able to predict particle dynamics throughout the reactor, not just in the central region which the existing onedimensional model is limited to geometrically. An initial test case has been successfully computed for the aerosol dynamics in a rotating disk reactor with an inlet silane concentration of 0.03 % in helium. While this is a very encouraging result, more work will be necessary to reduce the inordinately long computation time of several weeks on a high performance workstation. Improvement of algorithm efficiency will thus be a high priority as this effort continues.

Improvements in NIST Microcontamination Model — The efficiency of the one-dimensional NIST Microcontamination Model has been significantly enhanced. An increase in speed of approximately five has been obtained by utilizing a non-reacting temperature profile until virtually the end of the computation, when it is finally allowed to adjust to the presence of multiple reacting species. It has also been determined that the employment in this one-dimensional model of temperature profiles computed with the new twodimensional axisymmetric code results in improved comparisons with experimental results. This is because these temperature profiles more closely match those found in the actual experimental reactor.



Spatially-Resolved Gas-Phase Temperature Measurements --- Knowledge of the thermal environment in the CVD reactor is critical for investigation of CVD mechanisms. Therefore, rotational Raman spectroscopy was utilized to measure gas-phase temperature profiles in order to validate numerical temperature profiles. The Raman scattering volume was nominally a cylinder 500 µm in length and 250 µm in diameter. Temperatures were determined by comparing a measured Raman spectrum to a calculated spectrum and employing a global search minimization to minimize the sum of the residuals squared. The calculated spectrum was the convolution of the rotational Raman spectrum and the fit of the spectrograph lineshape function, and was obtained using the SANDIA CARS code modified for spontaneous Raman scattering. This global fit to all rotational lines simultaneously is particularly useful to minimize the effects of noise on the spectrum, e.g., KF interference, as well as to account for Raman scattering from excited vibrational states which becomes significant at approximately 1000 K and higher for nitrogen. The measured temperature profiles were in good agreement with numerical temperature profiles.

Spatially-Resolved Gas-Phase Species Concentration Measurements - Knowledge of gas phase species identities and concentrations is important to validate the numerical flow fields and the model silane pyrolysis mechanism. Therefore, gas phase species identities and relative concentrations were measured with vibrational Raman scattering. The signal from the gas phase nucleated particles is intense when silane is present. In addition, signal from hydrogen molecules (another reaction product) is also observed. Finally, it is noted that nitrogen rotational lines are observed. This indicates that temperature measurements will be possible in the presence of particles. This will enable us to determine whether or not the presence of particles affects the temperature profile, an important consideration for model development.

Chemical Properties Calculations - Molecular structure and vibrational frequency data for Group III (Al, Ga, In) and Group V (N,P,As) Hydrides have been compiled. These include the stable molecules (e.g., AlH₃) and radicals (e.g., AlH₂). Ab initio calculations have been over a wide range of theories utilizing different quality basis sets. The ab initio results have been compared to available experimental data in order to determine the minimum level of calculation necessary to give good molecular structures and vibrational frequencies. Although some of this work has already been reported in the literature, no comprehensive set of benchmark calculations for the whole series has been performed. Molecular structure and vibrational frequency data and bond dissociation energies (BDE's) for the Indium Methyl Hydrides InH_x(CH3)_y have been computed at the B3LYP/cc-pVTZ level of theory. The Indium Methyl Hydrides include the stable InH₃. $InH_2(CH_3)$, molecules $InH(CH_3)_2$, In(CH₃)₃, the radicals InH₂, InH(CH₃), In(CH₃)₂, and the closed shell intermediates (with lone pairs) InH, In(CH₃). Transition state calculations for abstraction of H atoms from the Indium Methyl Hydrides (In-H, CH2-H bonds) by H atoms and CH₃ have been computed, as well as a number of other transition state calculations. These transition state structures were then used to determine temperature-dependent rate expressions for the reactions. A simple decomposition mechanism has been constructed based on these data, compared to available experimental data, and is currently being refined. Calculated molecular structure, vibrational frequencies, and

BDE's for the Gallium Methyl Hydrides have also been carried out.

Prototype Database Website — A prototype website (http://h105097.nist.gov/ckmechx/) has been made accessible via the internal NIST web. This site currently contains thermochemical and bibliographic information of silicon hydrides and halocarbons important to semiconductor processes. The plan for this site is to have it provide all data necessary to support chemical mechanisms of significance to the industry. The current version of CKMechX has a number of capabili-Over 4000 enthalpies of formation are ties. available for more than 1000 species with over 4000 bibliographic citations. These data were taken from NIST compilations and evaluations of silicon hydrides, silicon oxy-hydrides, hydrocarbons, fluorinated hydrocarbons, and chlorinated hydrocarbons.

Microcontamination Website — A comprehensive microcontamination website (<u>http://www.cstl.nist.gov/div836/836.02/cvd/topp</u> age.html) has been established in order to disseminate the numerical and experimental results obtained from this investigation. Data is available on all aspects of this project, and reprints of relevant publications are downloadable.

Collaborations

University of Maryland, Sheryl Ehrman; numerical modeling of microcontaminant formation and transport.

Recent Publications

R. W. Davis, E. F. Moore, J. E. Maslar, D. R. Burgess, D. M. Kremer, and S. H. Ehrman, "A Numerical/Experimental Investigation of Microcontamination in a Rotating Disk Chemical Vapor Deposition Reactor," Characterization and Metrology for ULSI Technology: 2000 International Conference, ed. D. G. Seiler, A. C. Diebold, T. J. Shaffner, R. McDonald, W. M. Bullis, P. J. Smith and E. M. Secula, CP550, The American Institute of Physics, pp. 292-296 (2001).

J. E. Maslar and W. S. Hurst, "Non-Intrusive Optical Measurements of Gas and Surface Temperatures in Hostile Environments Using Raman Spectroscopy," NISTIR 6572.

J. E. Maslar, W. S. Hurst, D. M. Kremer, and S. H. Ehrman, "In Situ Gas Phase Optical Measurements of Silane Decomposition in a Thermal Chemical Vapor Deposition Reactor," in Fundamental Gas-Phase and Surface Chemistry of Vapor Deposition / Process Control, Diagnostics and Modeling in Semiconductor Manufacturing, ed. M. D. Allendorf, M. T. Swihart, and M. Meyyappan, The Electrochemical Society Proceedings Series, p. 168 (2001).

Temperature Measurements and Standards for Rapid Thermal Processing

Goals

The goal is to develop the technologies required to enable the measurement of Rapid Thermal Processing (RTP) wafer absolute temperatures with uncertainties of 2 °C at 1000 °C as prescribed in the International Semiconductor Technology Roadmap (ISTR).

Our project, initiated in FY97, has approached this goal with four objectives: (1) to improve calibration wafer technology to a 1 °C standard uncertainty by demonstrating the use of thin-film thermocouples (TFTCs) in conjunction with wire thermocouples (TCs) on test wafers in RTP tools; (2) to develop methods for in-tool radiation thermometer (RT) calibration, which relate TFTC wafer temperatures to indicated radiance temperatures; (3) to develop and validate models to account for wafer emissivity and the effects of chamber reflected-irradiation on temperatures determined from model-corrected RTs that are calibrated against blackbodies; and (4) to collaborate with the semiconductor industry in implementing new methods for reliable and traceable temperature measurements.

Customer Needs

The measurement needs of the semiconductor manufacturing industry have been stated in the ISTR. The requirement is for measurement and control of RTP tools to ± 2 °C at 1000 °C during processing with calibrations traceable to the International Temperature Scale of 1990 (ITS-90). Current industry measurement capabilities are ± 6 °C and major producers have voiced concerns to International SEMATECH (ISMT).

Our customers are the device manufacturers and the suppliers of thermal processing equipment and temperature measurement instrumentation. This community forms our project's Common Interest Group (20 companies meeting annually at NIST since 1997). They serve as a bridge between research and practice, provide advice on shaping objectives, and generate opportunities for technology transfer. ISMT has established a joint effort at UT-Austin, with NIST and several instrument suppliers, to develop a facility to evaluate and validate accuracy claims of commercial thermometry systems. *The 2001-ITRS states "Near-term solutions will impose severe* restraints on..., and post-processing thermal budgets." Front End Processes Section p. 19.



NIST TFTC test wafer in the ISMT-UT test bed being developed to qualify commercial contact and radiation thermometry instrumentation, and establish uncertainties in their traceability to the ITS-90.

Technical Strategy

Our strategy is to address three core elements of our research that will enable the semiconductor industry to meet the road map requirement: (a) fabrication of test wafers with improved thin-film technology for use by our industrial collaborators to demonstrate in-tool calibration of RTs traceable to the ITS-90; (b) experimentation on the NIST test bed and thermal modeling to determine the effects of wafer emissivity on in-tool calibration of lightpipe radiation thermometers (LPRTs); and (c) calibration and characterization of LPRTs.

The present scope of the TFTC technology work includes designing, fabricating, and testing thinfilm thermocouple calibration wafers for use in industrial RTP tools, defining the effect of various wafer and film emissivities on the temperature measurement, and establishing the uncertainty of the temperature measurements using the NIST calibration wafer.

We are using the NIST Test Bed to perform intercomparisons between the TFTCs and LPRTs. The goals are (a) to demonstrate calibration procedures for and establish uncertainties of the LPRTs against the TFTCs, and (b) to establish uncertainties for model-corrected LPRTs caliTechnical Contact: K.G. Kreider D.P. DeWitt

"The NIST light pipe calibration services and the thin-film thermocouple test wafer provide essential benchmarking for accuracy and traceability to the (ITS-90) in this new test facility for the semiconductor industry in meeting the ITRS requirement."

Prof. K.S. Ball, Univ. of Texas at Austin, April 26, 2002. brated against blackbodies. Experimental studies are being designed for these conditions: a range of wafer and film emissivities, variable separation distance between wafer and LPRT, and variable chamber wall reflectance. These studies require concurrent efforts to develop and validate radiation heat transfer models to estimate wafer effective emissivities that are essential for establishing uncertainty limits for LPRTs in our test bed, and in production tools.

DELIVERABLES: Quantification of emissivity effects on calibration wafers with model to correct LPRT calibrations in situ. 2Q 2002

We are using industrial RTP test beds to establish the usefulness of the NIST calibration wafer in the semiconductor processing industry and to define the benefits of using the NIST calibration wafer under various industrial conditions.

A cooperative project with ISMT and the University of Texas at Austin (UT-Austin) uses their RTP test bed, which has very high uniformity in wafer temperatures and can be used to confirm the uncertainties and repeatability of the NIST calibration wafer. Their test bed also is used to compare the NIST wafer with commercial thermocouple test wafers and industrial lightpipe radiation thermometers.

DELIVERABLES: NIST TFTC calibration wafers for ISMT test bed and joint report with UT-Austin on LPRT calibrations. 3Q 2002

A cooperative project with Vortek industries is permitting us to investigate the use of the NIST calibration wafer in a cutting edge RTP tool that has the fastest ramp rates in the industry. This tool has cold blackbody walls and extremely high heat flux gradients and is not suitable for commercial thermocouple temperature measurements. The NIST thin-film thermocouple calibration wafer has demonstrated unique capabilities in this pulse anneal system.

DELIVERABLES: NIST TFTC calibration wafers for pulse anneal RTP and joint report with Vortek on LPRT calibrations. 4Q 2002

We are collaborating with EMCORE, a semiconductor device fabricator, to establish methodologies for making model-corrected radiation thermometry measurements during a deposition process. The goal of the collaboration is to demonstrate a mix of technologies suitable for EMCORE to establish traceability to the ITS-90 with known uncertainties. The work involves detailed characterization of radiation thermometers and commercial blackbodies, measurement of reflectance standards, and application of thermal radiation effective-emissivity models previously developed by our project team. One aim of the work is to demonstrate the reduction in temperature uncertainty that is possible using a calibrated radiation thermometer in place of the contact sensor (thermocouple) to establish linkage to the ITS-90.

DELIVERABLES: Demonstration of improvements in temperature measurement uncertainty that can be achieved using well characterized blackbodies and calibrated radiation thermometers with appropriate thermal models of tool chambers. 3Q 2002

Common Interest Group (CIG) meetings have been held annually since 1997 for the purposes of assessing and planning project research directions. We are attempting to schedule this year's meeting during the 10th International Conference on Advanced Thermal Processing of Semiconductors (Sept. 25-27, 2002, Vancouver) Two major themes are being proposed: reports by our industrial collaborators on test wafer demonstration experiments, and discussions on proposals for establishing emissivity-standard-wafers. We will review the plan with members of the CIG at the May 2002 meeting of the ElectroChemcial Society and recruit participants to make presentations.

DELIVERABLES: Meet with members of CIG at the May 2002 meeting of the ElectroChemical Society and establish concrete plans for 2003 and 2004 activities. 2Q 2002

Accomplishments

Emissivity Effects

We investigated the effect of different silicon wafer emissivities and the effect of low emissivity films on RTP wafer temperature measurements using LPRTs. These tests were performed in the NIST RTP Test Bed. We used a NIST TFTC calibration wafer to calibrate the LPRTs in situ. The measurements of LPRTs viewing Au and Pt thin-film spots in the center of the wafer were compared to LPRT radiance temperature readings that viewed bare Si/SiO₂. We found differences of up to 36 °C at 900 °C in the LPRT measurements due to the low emissivity films. A model of the water temperature measurement was presented to provide an insight into the effects of wafer emissivity on LPRT measurements in RTP tools.

Thermal Model

A thermal model of the wafer and cold shield enclosure has been developed and employed to predict the effects of NIST Test Bed chamber features on LPRT measurements. The thermal response of the wafer was predicted for different thin-film spot, wafer emissivity, and shield reflectivity. The thin-film spot resulted in a temperature rise at the center of the wafer and its magnitude is strongly dependent on the shield reflectivity and less dependent on the wafer emissivity. The effects of the lightpipe sensor on the temperature distribution of the wafer were also investigated. Due to its low reflectivity compared with the cold shield, the lightpipe sensor caused a temperature decrease at its viewing area, which is a strong function of the shield reflectivity.

ISMT Wafer Evaluation

We have redesigned the calibration wafer for ISMT after the preliminary results have been released by UT-Austin on the test results of the first two wafers. Two designs are in progress. The first new design for a double pattern was fabricated and tested at NIST and sent to ISMT. They reported the results of the testing at the RTP 2001 International Symposium. The NIST wafer with 9 operating thermocouples (6 thin film TCs and 3 wire TCs) showed that the uniformity of their wafer heating was within 2.5 °C. The second new design is for a sandwich wafer which will have Sensarray thermocouples in submerged grooves as well as 12 NIST TFTCs and 4 NIST wire TCs. This complex wafer is a collaborative effort of NIST, ISMT, UT-Austin, Carl Suess, and Sensarray. The thin films on the sandwich wafer will be deposited in the Fabrication Technology Division thin film facility.

VORTEK Wafer Evaluation

• Five wafers were delivered to Vortek and four have been tested. We redesigned our calibration wafer because of the extremely high heat transfer fluxes in the Vortek chamber. The new design was developed using the excellent Vortek capabilities of mapping the temperature of the wafer. We have improved the thin film pattern to minimize thermal distortion caused by the thin films. Significant improvement was measured after the first design change and further improvements were made with the third wafer. The fourth wafer was tested on July 5-7 in Vortek's new spike anneal RTP tool. This instrumented wafer compares the thin-film thermocouple outputs to two of Vortek's radiometers. The plan includes a comparison to calibrated radiometers (0.95 and $1.45\mu m$) in the near future.





Photograph (upper) of visual comparison between a lightpipe with imperfections (top) and a quality lightpipe (bottom). Photograph (lower) of calibrating a lightpipe in water cooled jacket and viewing sodium heat pipe blackbody at 900 °C.

Lightpipe Characterization

Our objective was to investigate improved procedures for characterization and calibration of sapphire lightpipes using uniform blackbody sources. We evaluated spectral, spatial, and temporal characterizations of LPRTs to obtain critical information on effective wavelength and field of view, as well as stability information required for making accurate temperature measurements and uncertainty assessments. We reported guidelines for making qualitative and quantitative inspections of the sapphire lightpipes. Proper inspections of the lightpipes can assist the user in identifying lightpipes that will have poor performance before using them in RTP tools. We also compared "cold" calibrations done in less than 5 s and "hot" calibrations taking about 30 min and discovered that the difference between "cold" and "hot" calibrations can be as much as 2.5 °C in some situations. We offered

caution for utilizing information received in factory calibration reports. A comparison of three vendors showed that the differences between the factory calibration and the NIST calibration were as much as 7.6 °C. We disseminated a list of recommendations for the lightpipe user to assist them in performing more useful characterizations and accurate calibrations.

Thermal Modeling with Non-Smooth Wafers

A Monte-Carlo based, radiation thermal model was developed to simulate wafer-chamber radiative process and to predict the wafer effective emissivity required to perform accurate, model-corrected radiometric temperature measurements. The wafer-chamber arrangement is comprised of a silicon wafer, a guard ring, a cold reflective shield, and a guard tube. A trueeffective emissivity considering the limited numerical aperture of the light pipe was defined. The calculation showed that the true effective emissivity could be different from the hemispherical effective emissivity and is the appropriate parameter for correcting light-pipe radiation thermometer readings. The wafer reflectance behavior was represented by combinations of specular and diffuse components. The reflectance behavior from rough wafer surfaces is more complicated. For such situations, the bidirectional distribution function (BRDF) is more appropriate as it describes the detailed angular distribution of the reflected energy. Based upon earlier BRDF measurements on representative wafers, different types of BRDFs are being implemented in the Monte-Carlo model code. In the next-generation model under development using actual BRDFs, we expect the roles of guard tube and guard ring specular surfaces to be more prominent. These surfaces have notable effects on LPRTs located near the wafer center, but will cause markedly different radial distributions of the true effective emissivity. The results of the model will be important for improving our understanding of NIST Test Bed TFTC-LPRT intercomparison as well as for correcting multi-point temperature measurements across the wafer radius.

Recent Publications

K. G. Kreider and G. J. Gillen, "High Temperature materials for thin-film thermocouples on silicon wafers," accepted for publication in *Thin Solid Films*, July 7, 2000.

K.G. Kreider, D.P. DeWitt, C.W. Meyer, and V.P. Scheuerman, "Calibration of Light-Pipe Radiation Thermometers in an RTP Tool at 1000 °C with an uncertainty of 2 °C," *Eighth International Conference on Advanced Thermal Processing of Semiconductors - RTP'00*, pp 64-70, September 2000, Gaithersburg, MD.

B.K. Tsai, C.W. Meyer, F.J. Lovas, "Calibration and Characterization of Light-Pipe Radiation Thermometers for the NIST RTP Test Bed," *Eighth International Conference on Advanced Thermal Processing of Semiconductors - RTP'00*, pp 83-93, September 2000, Gaithersburg, MD.

Y.H. Zhou, Y.J. Shen, and Z.M. Zhang (University of Florida), B.K. Tsai and D.P. DeWitt, "Effect of Directional Properties on the Radiometric Temperature Measurement in Rapid Thermal Processing," *Eighth International Conference* on Advanced Thermal Processing of Semiconductors -*RTP'00*, pp 94-103, September, 2000, Gaithersburg, MD.

Y.H. Zhou, Shen, Y.J., Zhang, Z.M., Tsai, B.K., and DeWitt, D.P., "Monte Carlo Simulation for Radiometric Temperature Measurement in Rapid Thermal Processing," to be published in *The 2000 International Mechanical Engineering Congress* & *Exposition*, Orlando, FL, November 4-7, 2000.

B.K Tsai, and D.P. DeWitt, "Methods used at NIST to Characterize and Calibrate Lightpipe Radiation Thermometers," TEMPMEKO 2001, *The Eighth Symposium on Temperature and Thermal Measurements in Science and Industry*, Berlin, Germany, June 19-21, 2001.

C.W. Meyer, "Effects of Extraneous Radiation on the Performance of Light Pipe Radiation Thermometers," TEMPMEKO 2001, *The Eighth Symposium on Temperature and Thermal Measurements in Science and Industry*, Berlin, Germany, June 19-21, 2001.

K.G. Kreider, D.W. Allen, D.H. Chen, D.P. DeWitt, C.W. Meyer, and B.K. Tsai, "Effects of Wafer Emissivity on Light Pipe Radiometry in RTP Tools," *Ninth International Conference on Advanced Thermal Processing of Semiconductors - RTP'00*, pp 163-168, September 2001, Anchorage, AK.

Y.H. Zhou, and Z.M. Zhang, (University of Florida, Gainesville, FL), D.P. DeWitt and B.K. Tsai, "Effects of Radiative Property of Surfaces on Radiometric Temperature Measurement," *Ninth International Conference on Advanced Thermal Processing of Semiconductors - RTP'00*, pp 179-188, September 2001, Anchorage, AK.

Low Concentration Humidity Standards

Goals

The primary objective is to establish quantitative standards enabling the accurate measurement of trace quantities of water vapor ($< 10^{13}$ molecules cm⁻³). This effort supports the development and application of commercial humidity sensors used for gas purity measurements, and inline monitoring and process control – functions that are relevant to minimizing wafer misprocessing.

Customer Needs

As discussed in the 2001 International Technology Roadmap for Semiconductors (ITRS) in the chapter entitled Metrology, the evolution of sensor-based metrology for integrated manufacturing requires the development of in-situ sensors enabling in-time measurements. In Table 96 entitled Metrology Difficult Challenges, the need for robust and accurate sensor technology and impurity detection in starting materials is highlighted. Of the known impurities in processing gases, water vapor is one of the most ubiquitous and difficult to eliminate. Thus its measurement and control is often critical to various semiconductor-related processes.

Although a variety of high sensitivity sensors of water vapor are available, most do not directly measure water in the gas phase. Rather they typically respond to moisture-induced changes in bulk or surface properties associated with the adsorption of water vapor. Consequently, a rigorous first-principles determination of sensor response is often precluded, thus compromising accuracy. Moreover, since many such devices exhibit drift and poor reproducibility, frequent recalibration is required. Interpretation of these measurements is also complicated by complex physical interactions of water vapor with technical surfaces in transfer lines, in reaction chambers and in sensor housings.

Technical Strategy

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The development of accurate and robust water vapor sensors requires well-characterized reference standards against which such devices can be evaluated. This should include a primary method of measurement for water vapor concentration and a complementary method yielding highprecision and stable sources of water vapor. By providing access and traceability to the unique capabilities at NIST discussed below, instrument manufacturers and sensor users can assess the overall performance and accuracy of their measurements.

Our strategy is to establish complementary capabilities in high-precision generation and measurement of water vapor. To address these respective needs, we have



Figure 1. NIST Low Frost-Point Humidity Generator Accomplishments

developed a thermodynamically based humidity source and high-sensitivity optical absorption measurement methods discussed below. The thermodynamic humidity source, known as the Low Frost-Point Generator (LFPG), serves as the project cornerstone and is capable of delivering 3 mmol to 3 nmol of water vapor per mole of dry gas. Here the water vapor concentration in a gas stream is precisely controlled by active regulation of the saturator temperature and pressure. As such, the LFPG is ideally suited for testing the performance of various sensing and humidity generation technologies. To date, it is has been used to characterize water vapor measurement and generation systems at the research and development stage as well as commercial devices.



Figure 2: Steady state response of saturator control thermometers in NIST Low Frost-Point Humidity Generator.

Technical Contacts: J.T. Hodges G.E. Scace

"The LFPG is the 'Gold' standard for moisture generation and after the round robin experiments it is possible for the industry to talk about moisture measurements that can be compared to the standard."

Suhas Ketkar, Air Products and Chemicals 1. A common technology used by the semiconductor industry for delivering controlled quantities of water vapor is based upon the controlled permeation of water vapor through a material, followed by mixing and dilution with a dry gas of known flow rate. During FY 2002 we will establish a calibration service for water permeation tubes, comparing permeation tubes to the LFPG using a commercial water vapor sensor as a nulling device. This calibration service will constitute an efficient and low-cost mechanism for the dissemination of NIST trace humidity standards.

DELIVERABLES: Commission permeation tube calibration service. 3Q 2002

2. To complement our established capability in precision generation of trace humidity levels, we are developing absolute techniques based upon the absorption of visible and near-infrared laser radiation. Water vapor has an absorption spectrum comprising thousands of distinct rovibronic absorption transitions in this spectral region. Thus, the concentration of water vapor can be readily determined in terms of measurements of sample absorbance and independently determined absorption line strengths. Recent advances in source and detector technology, and new spectroscopic techniques that extend the sensitivity of laser absorption measurements now enable the precise sensing of water vapor at concentrations below 10¹⁰ molecules cm⁻³. To account for line broadening effects, and mitigate interference effects associated with absorption by other species the most precise absorption measurements require that individual transitions be spectrally resolved. This demands a technique having a frequency resolution much smaller than the characteristic widths of the absorption transitions, and requires that the frequency intervals in the measured spectrum be accurately determined. By combining high spectral resolution with high precision absorbance measurements, the water vapor concentration can be found independently of the composition of the carrier gas. Of the optical absorption methods, cavity ring-down spectroscopy (CRDS) is expected to be the most suitable for a primary method. CRDS is a cavityenhanced optical absorption technique that has high sensitivity, fast response, and probes a compact well-defined volume. It is important to emphasize that under certain conditions, CRDS can exhibit exceptional spectral resolution, enabling detailed measurements of absorption line shape. To this end, we are developing a refined version of CRDS called frequency-stabilized

single-mode cavity ring-down spectroscopy (FSSM-CRDS). Here, the ring-down cavity is actively length stabilized, the probe laser is frequency locked to the ring-down cavity, and the frequency axis of the spectra is based upon the longitudinal mode spacing of the ring-down cavity. See Figure 3 below.



Figure 3: Frequency-stabilized CRDS system.

To achieve the high performance promised by FSSM-CRDS, we will complete our ongoing development of a cw diode laser frequency locked to the length-stabilized ring-down cavity. We will measure the output of a permeation tube moisture generator (in the range 10 nmol/mol to 100 nmol/mol and directly traceable to the LFPG) using this FSSM-CRDS system, and thereby determine the line strengths of the absorption transitions in terms of the LFPG output.

DELIVERABLES: Demonstrate FSSM-CRDS as primary method of measurement for low concentration humidity standards. 3Q 2002.

Accomplishments

We completed a detailed uncertainty analysis of the LFPG, accounting for measurement uncertainties, and uncertainties in the relevant thermodynamic properties of ice, water vapor and N₂. In summary, the LFPG saturator has a temperature stability of better than \pm 2.5 mK (see Fig. 1) giving a relative precision of better than \pm 0.05 % and an expanded uncertainty (k=2) in the generated water vapor concentration of less than 0.8% (see Fig. 4). The uncertainty of the LFPG frostpoint temperature is less than 0.014 °C.



Figure 4: Expanded uncertainty (k=2) of the LFPG output H₂O mole fraction as a function of saturator temperature.

The LFPG uncertainty analysis discussed above was based on the uncertainties in temperature and pressure within the LFPG saturator, ice vapor pressure and the enhancement factor for mixtures of water vapor and air. However, this analysis neglected background effects associated with the transient adsorption and desorption of water vapor from internal surfaces in the flow manifold located downstream of the LFPG. For the lowest range considered, such processes may effect significantly the water vapor concentration in the sample gas delivered by the LFPG to test instrumentation. In collaboration with Air Products Inc., we quantified the magnitude of this water vapor background using atmospheric pressure ionization mass spectrometry (APIMS). Results shown in Fig. 5, indicate that background contribution to H₂O from system components downstream of the LFPG was less than 0.2 nmol/mol. These measurements also demonstrated that linearity deviations of the LFPG output H₂O mole fraction are less than 0.1 nmol/mol.



Figure 5: APIMS measurement of LFPG background H2O concentration showing decay to steady state level.

We developed a quantitative method for comparing the outputs of permeation tube moisture generators (PTMG) to that of the LFPG. This technique is capable of resolving fractional differences of approximately 1 %, for PTMGs covering the mole fraction range 10 to 100 nmol/mol. An intercomparison of PTMG devices from several customers was completed. and results comparing two representative PTMGs to the LFPG are summarized in Fig. 6. Uncertainties in flow metering and background water vapor present in the carrier gas were identified as limiting effects. The measurement technique used for this work forms the basis for the upcoming permeation-tube calibration service.





• We measured trace levels of water vapor generated by the LFPG using a prototype diode laser hygrometer (DLH). This hygrometer, which was based upon wavelength modulation spectroscopy, had a linearity better than 1 % over the water vapor mole fraction range 3 nmol/mol to 2 μ mol/mol and yielded a sensitivity of better than 0.5 nmol/mol when tested against the LFPG. These experiments and subsequent tests on a beta system were critical to the development of a similar DLH that is now commercially available.

We have successfully fabricated and tested a length-stabilized CRDS system, based on a continuous wave diode laser. The system is optimized for high-precision measurements of trace water vapor concentration. A CRDS spectrum of atmospheric H₂O is shown in Fig. 7, corresponding to a mole fraction of approximately 6 μmol/mol and concentration of 2x10¹³ molecules cm⁻³. Other results indicate that the integrated CRDS spectra scale linearly with H₂O concentration and support the expectation that nmol/mol level sensitivities and high-precision line shape measurements will be realizable with the fully developed FSSM-CRDS system. Recently, a detection limit of better than 10 nmol/mol of H_2O in N_2 has been demonstrated, using the relatively weak absorption lines near 935 nm.



Figure 7: CRDS spectrum of pressure-broadened H_2O rovibronic transition at 10687.36 cm⁻¹, corresponding to an absorbing wavelength of 935.7 nm. The open circles are the measured losses, and the solid line is a Voigt fit to the measured profile.

Collaborations

Air Products and Chemicals Inc., Seksan Dheandhanoo; APIMS measurements of trace moisture and characterization of semiconductor gas purity.

NIST Optoelectronics Division, Kris A. Bertness; CRDS measurements of H_2O in III-V compound process gases.

Dow Chemical, Linh Le and J.D. Tate; CRDS measurements for process gas control RH Systems, Robert Hardy; Characterization of low range chilled-mirror hygrometers.

Southwest Sciences lnc, Chris Hovde.; Development of wavelength modulation laser hygrometer for trace H_2O sensing.

Recent Publications

J.T. Hodges, J.P. Looney and R.D. van Zee, "Response of a ring-down cavity to an arbitrary excitation," J. Chem. Phys., **105**, 10278-10288, 1996.

G.E. Scace, P.H. Huang, J.T. Hodges, D.A. Olson and J.R. Whetstone, "The new NIST low frost-point humidity generator," National Conference of Standards Laboratories, Proceedings of the 1997 Workshop and Symposium, 2, 657-673, July 27-31, 1997, Atlanta, GA.

G.E. Scace, D.C. Hovde, J.T. Hodges, P.H. Huang, J.A. Silver and J.R. Whetstone, "Performance of a precision low frostpoint humidity generator," 3rd International Symposium on Humidity and Moisture, sponsored by the National Physical Laboratory, Teddington, England, April 6-8, 1998.

G.E. Scace, D.C. Hovde, J.T. Hodges, P.H. Huang, J.A. Silver and J.R. Whetstone, "The NIST Low Frost-Point Humidity Generator: A New Standard for Trace Humidity Measurement," Workshop on Gas Distribution Systems, Semicon West 98, San Francisco, CA, July 12, 1998.

J.T. Hodges, J.P. Looney and R.D. van Zee, "Single mode cavity ring-down spectroscopy with pulsed lasers," 1998 International Symposium on Molecular Spectroscopy, June 15-19, 1998, Columbus, OH.

R. D. van Zee, J. P. Looney, and J. T. Hodges, "Measuring pressure with cavity ring-down spectroscopy," in *Advanced Sensors and Monitors for Process Industrial Environment*, W. A. de Groot, ed., SPIE Proc. **3535** (1998).

J.P. Looney, J.T. Hodges and R.D. van Zee, "Quantitative absorption measurements using cavity-ringdown spectroscopy with pulsed lasers," Chapter 7, in *Cavity-Ringdown Spectroscopy-A New Technique for Trace Absorption Measurements*, ed. K.W. Busch, American Chemical Society Symposium Series No. 720, 1999.

R. D. van Zee, J. T. Hodges and J. P. Looney, "Pulsed, single-mode cavity ring-down spectroscopy," Appl. Opt., 38, 3951-3960, 1999.

D.C. Hovde, J.T. Hodges, G.E. Scace, J.A Silver, "Wavelength-modulation laser hygrometer for ultrasensitive detection of water vapor in semiconductor gases," Appl. Opt., 40, 829-839, 2001.

G.E. Scace, and J.T. Hodges, "Uncertainty of the NIST low frost-point humidity generator," Proceedings of the 8th International Symposium on Temperature and Thermal Measurements in Industry and Science, June 19-21, 2001, Berlin, Germany.

P.H. Huang, G.E. Scace, and J. T. Hodges, "Measuring technique for quantifying performance of dilution-based trace moisture generators," Proceedings of the 8th International Symposium on Temperature and Thermal Measurements in Industry and Science, June 19-21, 2001, Berlin, Germany.

Plasma Process Metrology

Goals

To provide advanced measurement techniques, data, and models needed to characterize plasma etching and deposition processes important to the semiconductor industry, enabling continued progress in model-based reactor design, process development, and process control.

Customer Needs

To fabricate future generations of devices, the semiconductor industry requires improvements in plasma etching and deposition processes. Plasma processes and equipment face increasingly stringent requirements due to the need to maintain high device vields at decreasing feature sizes, the introduction of new dielectric materials. and the constant pressure to keep production efficiency high. To meet these challenges, the International Technology Roadmap for Semiconductors (ITRS) identifies a need for better predictive system modeling. To obtain more reliable predictions of the chemical, physical, and electrical properties of processing plasmas, further progress in model development and validation is required. ITRS also identifies a need improvements for in intelligent process monitoring and control, which require the development of robust and reliable sensors that are compatible with manufacturing equipment.

Technical Strategy

Our multifaceted program provides numerous outputs to assist our customers, including advanced measurement methods, high-quality experimental and fundamental data, and reliable, well-tested models of plasma behavior.



One of the inductive, high-density plasma reactors used in our experimental studies.

1. We develop and evaluate a variety of *measurement techniques* that provide industry and academia with methods to characterize the chemical, physical, and electrical properties of plasmas. The techniques we develop include improved laboratory diagnostic measurements for use in research and development, as well as more robust, non-perturbing measurements for use in process monitoring and control in manufacturing applications.

We are currently developing a new optical diagnostic technique, sub-millimeter wave spectroscopy, to measure the density and temperature of important chemical species in plasmas. To optimize the sensitivity and spatial resolution of the sub-mm technique we are investigating several different sources and detectors, including an IR laser photo-mixer and a room temperature microbolometer.

DELIVERABLES: Develop sub-mm wave spectroscopy for use as a plasma diagnostic. Implement and evaluate improved sources and detectors, including IR laser photo-mixer and room temperature microbolometer. 4Q 2002

2. We are also extending the planar laserinduced fluorescence (PLIF) technique to provide two-dimensional maps of the temperature of reactive species in etching plasmas, as well as their density.

DELIVERABLES: Develop diagnostic technique to measure two-dimensional images of temperature in fluorocarbon plasmas using PLIF of the CF radical. 3Q 2002

3. Electrical measurement techniques for use in process monitoring and control applications are also under development. These techniques rely on measurement of the radio-frequency current and voltage applied to plasma reactors. The rf measurements are compatible with commercial reactors and they contain valuable information about the flux and energy of the ions that bombard wafers during processing. Values for the total ion flux and ion energies are obtained by analyzing the current and voltage signals using electrical models of plasma sheaths.

DELIVERABLES: Methods for monitoring total ion flux and ion energies using rf current and voltage measurements, validated in inductively coupled plasma reactors. 3Q 2002

Technical Contacts:

- M. Sobolewski
- K. Steffens
- J. Olthoff
- Y. Wang
- E. Benck

"NIST is one of the leaders in plasma processing related research in the US. They have capability to thoroughly understand plasma behavior using a variety of diagnostics tools."

Peter Ventzek Motorola

"The NIST plasma process metrology group has helped us to understand the fundamental physical and chemical processes that are important to electronics materials and semiconductor processing industries." Bing Ji,

Air Products and Chemicale, Inc. **DELIVERABLES:** Validation of rf-based ion flux and ion energy measurement techniques in dualfrequency, capacitively coupled plasma reactors. 1Q 2004

4. In addition to measurement techniques, we also provide *data* necessary for gaining an understanding of complex plasma properties and for testing and validating plasma models. The data help semiconductor manufacturers and plasma equipment manufacturers to better understand and control existing processes and tools and help them to develop new ones. The experimental data we provide are measured under well-defined conditions in highly-characterized standard plasma reactors.

Recently, dual-frequency, capacitively coupled reactors have become popular for state-of-the-art dielectric etching processes, but there is relatively little experimental data available for such plasmas. To address this lack of data, we are in the process of converting our capacitivelycoupled reactors to operate in dual-frequency mode. Electrical and optical measurements will be performed to characterize the dual-frequency plasmas, provide understanding of their operation, and validate models of their behavior.

DELIVERABLES: Electrical and optical data in dual-frequency capacitively coupled plasma reactors needed to validate models and increase understanding. 3Q 2003

We also assess, evaluate, and measure 5. fundamental that describe important data collision processes in reactive plasmas. Recommended values for fundamental data provided by NIST greatly assist plasma modelers throughout industry and academia to improve the accuracy of their simulations.

DELIVERABLES: Database of recommended values of electron interaction cross-sections for commonly used plasma processing gases. 4Q 2002

6. Finally, we are engaged in the development and validation of plasma *models*. Such efforts concentrate on modeling of plasma sheaths, the thin regions at the boundary of the plasma. Sheaths play a dominant role in determining discharge electrical properties and the properties of the highly energetic ions that are necessary for plasma etching. More accurate sheath models are needed to better predict and optimize discharge electrical characteristics and ion kinetic energies. Sheath models are also used to develop new types of process monitoring techniques based on radio-frequency electrical measurements.

1.34

DELIVERABLES: Accurate, validated models of plasma sheaths that can predict plasma electrical properties and ion energies in inductively coupled plasmas 4Q 2002.

DELIVERABLES: Validated models of plasma sheaths for dual-frequency capacitively coupled plasmas 4Q 2003.

Accomplishments

This year we performed a rigorous test of the ability of models to predict ion kinetic energies in high-density plasmas. Energetic ions play a crucial role in plasma etching and other plasma processes. Ions exiting the plasma are accelerated to high energies by strong, radio-frequency electric fields in plasma sheaths, thin regions located at the boundaries of plasmas. The complicated ion dynamics in plasma sheaths are usually modeled using simplifying assumptions that have never been sufficiently validated. Our tests, performed in CF₄ discharges, showed that ion energy distributions predicted by simple, commonly-used, analytical sheath models did not agree with measurements. A more sophisticated model, however, did accurately predict the behavior of measured ion energy distributions and their dependence on frequency, sheath voltage, ion current density, and ion mass. The model, developed at NIST in previous years, can be adapted for use in commercial plasma simulations, and also serves as the basis for new methods for in situ monitoring of ion energies at wafers during plasma processing.



Ion energy distributions in a high-density CF_4 plasma: measurements (top) and model predictions (bottom).

For the first time, sub-millimeter wave absorption spectroscopy is being developed as a plasma diagnostic to identify and monitor species in etching plasmas. Sub-mm wave spectroscopy
can monitor the crucial chemical species in a plasma and provide the necessary feedback for understanding plasma processing. Initial measurements have concentrated on the use of a backwards wave oscillator (BWO) as the sub-mm wave source. This source is relatively compact and could easily be used in an industrial setting. In addition, a new sub-mm wave source (IR laser photomixer) and detector (room temperature microbolometer) were tested. Spectra from a variety of species have been identified in both capacitively and inductively coupled plasma reactors, including feed gases (CHF₃, CF₃I), etching radicals (CF2, CF, O3), etching byproducts (CO, CO⁺, COF₂, SiO, SiF₂, SiF) and contaminants (H₂O, CN, HCN). In one study of fluorocarbon etching plasmas. sub-mm measurements were compared with etching rates of blanket coated wafers and FTIR measurements of downstream effluents. The spectral resolution of the sub-mm diagnostic is so high that it can also be used to determine the translational temperature of plasma species through the Doppler broadening of absorption line shapes. Gas temperatures are important input parameters to many plasma models since they are necessary to relate the measured gas pressure to the actual particle density in the chamber.



Sub-millimeter wave absorption spectrum of CHF₃ in a high-density, inductively coupled plasma.

Also this year we have extended our capabilities for monitoring spatially-resolved radical densities in fluorocarbon plasmas using 2-D planar laser-induced fluorescence (PLIF) imaging. With the implementation of a tunable wavelength laser, we are now able to obtain PLIF images of the CF radical, in addition to CF₂. Both CF and CF₂ are important precursors for the formation of the fluorocarbon polymer layer which provides selectivity during oxide etching

and is the basis for plasma deposition of lowdielectric-constant fluorocarbon films. Currently, measurements of spatially-resolved CF density have been made in CF4, CF4/O2 and C4F8 plasmas, investigating the effects of pressure and power, and the presence of oxygen feedgas and silicon wafers. The comparison between CF and our additional results on CF₂ gives insight into the different roles played by the two radicals, providing guidance for selection of precursor and processing conditions. PLIF images of the two radicals also provide a useful data set for quantitative validation of 2-D plasma simulations.



PLIF images of CF₂ (top) and CF (bottom) density in a capacitively coupled discharge in 200 mTorr of CF₄, with a Si wafer on the lower electrode.

• One of our capacitively coupled cells has been recently modified to allow operation as a dual frequency system. Dual frequency plasma reactors are becoming of increasing importance to the semiconductor industry, particularly in oxide etching. A new time-resolved optical emission diagnostic based on an intensified CCD camera has been established. Optical emissions due to the main powered electrode are time averaged and subtracted from the images to show the time-resolved perturbations to the plasma from the bias electrode.

• Absolute, mass-resolved ion fluxes and densities of selected radicals were simultaneously measured in the presence of a silicon wafer in capacitively coupled plasmas generated in processing gases including C_4F_8 and SF_6 . The results indicate that the wafer significantly influences the ion and radical composition in each gas as evidence of the complex chemistries present in the etching plasmas. These results are useful to validate and refine reactor modeling

codes used in the development of plasma processing methods.

■ NIST-recommended data were derived for electron interactions with C_4F_8 , a gas with many industrial applications. The review was published in the Journal of Chemical and Physical Reference data. These data were used by industry to improve deep silicon etch processes.

• Measurements and modeling of collisioninduced decomposition rates of SF_6^- have been completed in collaboration with researchers at the College of William and Mary.

Electron drift velocities and effective ionization coefficients were measured and analyzed for C_2F_4 . C_2F_4 is a dominant fragment formed in highly dissociated C₄F₈ etching plasmas. These data were required as input parameters for newly developed process models C_4F_8 etching describing processes. The determination of these previously unavailable data enabled the development of a more accurate chemical code describing the primary reactions in C₄F₈ discharges.

• Fundamental data were distributed to plasma modelers throughout industry and academia via the web-based NIST "Electron Interactions with Plasma Processing Gases" database (http://eeel.nist.gov/811/refdata/). This web site has experienced thousands of hits in FY 2001 and tens of thousands of hits throughout its history.



Recommended electron cross section data for SF₆ (shown here) and numerous other plasma processing gases are available on the web at http://eeel.nist.gov/811/refdata/.

Recent Publications

M. A. Sobolewski, Y. Wang, and A. Goyette, "Measurements and modeling of ion energy distributions in high-density, radio-frequency biased CF₄ discharges," Journal of Applied Physics 91, 6303-6314 (2002). M. A. Sobolewski, "Measuring the ion current in high-density plasmas using radio-frequency current and voltage measurements," Journal of Applied Physics **90**, 2660-2671 (2001).

R. Champion, I. Dyakov, B. Peko, and Y. Wang, "Collisional decomposition of SF_6 ," J. Chem. Phys. **115**, 1765 (2001).

K. L. Steffens and M. A. Sobolewski, "Investigation and control of spatial characteristics of chamber-cleaning plasmas," in AIP Conference Proceedings **550**, *Proceedings* of the 2000 International Conference on Characterization and Metrology for ULSI Technology, 233-237 (2001).

A. N. Goyette, Y. Wang, and J. K. Olthoff, "Comparison of the identities, fluxes, and energies of ions formed in high density fluorocarbon discharges," in AIP Conference Proceedings **550**, *Proceedings of the 2000 International Conference on Characterization and Metrology for ULSI Technology*, 238-242 (2001).

M. A. Sobolewski, "Monitoring ion current and ion energy during plasma processing using radio-frequency current and voltage measurements," in AIP Conference Proceedings **550**, *Proceedings of the 2000 International Conference on Characterization and Metrology for ULSI Technology*, 263-267 (2001).

E. C. Benck and K. Etamadi, "Fiber optic based optical tomography sensor for monitoring plasma uniformity," in AIP Conference Proceedings **550**, *Proceedings of the 2000 International Conference on Characterization and Metrology for ULSI Technology*, 268-272 (2001).

A. N. Goyette, Y. Wang, and J. K. Olthoff, "lon compositions and energies in inductively coupled plasmas containing SF₆," J. Vac. Sci. Technol. A **19**, 1294 (2001).

A. N. Goyette, J. de Urquijo, Y. Wang, L.G. Christophorou, and J.K. Olthoff, "Electron transport, ionization, and attachment coefficients in C_2F_4 and C_2F_4/Ar mixtures," J. Chem. Phys. 114, 8932 (2001).

L. G. Christophorou and J. K. Olthoff, "Electron Attachment Cross Sections and Negative Ion States of SF₆," International Journal of Mass Spectrometry **205**, 27-41 (2001).

L. G. Christophorou and J. K. Olthoff, "Interactions of Low-Energy Electrons with $c-C_4F_8$," Journal of Physical and Chemical Reference Data **30**, 449-473 (2001).

L. G. Christophorou and J. K. Olthoff, "Interactions of Low-Energy Electrons with CF_3l ," Journal of Physical and Chemical Reference Data **29**, 553-569 (2000).

Y. Wang, M. Misakian, A. N. Goyette, and J. K. Olthoff, "Ion fluxes and energies in inductively coupled radio-frequency discharges containing CHF₃," J. Appl. Phys. **88**, 5612-5617 (2000).

M. A. Sobolewski, "Sheath model for radio-frequency-biased, high density plasmas valid for all ω/ω_i ," Phys. Rev. E, 62, 8540-8553 (2000).

Measurements for Vacuum Process Control

Goals

Develop primary flow standards in the flow range from 10^{-7} to 10^{-3} mol/s and transfer this flow measurement capability to the US semiconductor industry. (10^{-6} mol/s is 1.3 standard cubic centimeters per minute.)

Support semiconductor process-control efforts by developing a real-time, quantitative, *insitu* approach for measuring process gas composition.

Customer Needs

Many industrial processes require the accurate metering of mass flow rate over the range from 10^{-7} to 10^{-3} mol/s. Most prominent are the manufacturers of semiconductor devices, who use thermal mass flow controllers (MFCs) to control a wide variety of toxic, flammable, and corrosive gases. Participants at a recent industry workshop at NIST expected future requirements for flow measurement accuracies to be better than 1 %, and they identified the need for national flow transfer standards with uncertainties of 0.1 %. New primary flow standards and improved flow measurement techniques must be developed to meet these needs.

The increasing volume and complexity of vacuum processing in the semiconductor industry requires improved real-time process monitoring and control of process gases, reaction products, and gaseous contaminants. RGAs are the most promising candidates for this task, and are already used in a variety of vacuum processes, but their often-unpredictable performance has limited these applications. Realizing their potential requires a better understanding of the factors limiting their performance, particularly when operating with reactive process gases, and the development of *in situ* calibration techniques to compensate for instrument drifts in process applications.

Measurement of gas flow is crucial for the control of the stoichiometry in plasma etching. The Critical Dimension reduction efforts discussed in the 2001 International Technology Roadmap for Semiconductors imply improvements in MFCs. "Improvements will be required in the otch chemistries..."; "...development of multi-step etch processes...may translate into the need to change gas chemistries in the same etch module..."

Technical Strategy

The flow measurements are based on a diverse series of primary standards. The first was a constant-volume (pressure rate-of-rise) primary standard that we developed to measure flows up to 10^{-3} mol/s with uncertainties of about 0.1 %. It has been replaced by a constant-pressure (variable volume) standard that can operate at pressures from 0.5 to 5 atmospheres with an uncertainty of about 0.05 %. The third primary standard is gravimetric; flow measurements made by a transfer standard are integrated and compared to the weight change of a gas bottle.

Transfer standards allow the primary flow standards at NIST to be compared to flow meters at other locations. Although a flow meter manufacturer typically constructs its own primary standard, comparisons with NIST allow the manufacturer to demonstrate proficiency and, if necessary, provide traceability to NIST. For this purpose, we have developed a series of very stable transfer standards based on laminar flow through a thermostatted duct. The first generation used a stainless steel, helical duct of rectangular crosssection. It was used to perform on-site proficiency tests of industrial flow standards at more than ten fabrication facilities and MFC manufacturers. The second generation transfer standard uses quartz capillaries with a circular crosssection, which are available commercially for gas chromatography. It has been used in five comparisons.

Technical Contact: Robert F. Berg A. Lee

I wish you success in obtaining increased funding to continue your superb work, which I regard as essential to the future success of all American companies making flow control instruments for the semiconductor industry worldwide." T. Maginnis, Unit Instruments, Kinetics Fluid Systems



Left: A transfer standard flow impedance formed from 19 parallel quartz capillaries. Right: Tightly coiling the flow impedance tacted the contrifugal corrections used in the transfer standard's hydrodynamic model.

NIST vacuum (partial-pressure) standards have been used to examine the performance characteristics of commercial residual gas analyzers (RGAs), the most flexible instruments available for *in situ* monitoring of process gas composition. These studies found that the performance of RGAs depends not only on instrument design, but also on instrument operating parameters. In particular, these parameters can significantly affect electron and ion space charge within the RGA, which in turn can change performance characteristics by orders of magnitude. For most RGAs the performance can be optimized by proper adjustment of instrument operating parameters, guided by *in situ* calibration results. Within the past year, the RGA studies have been extended to the new closed-ion-source (CIS) instruments.

1. The performance of RGAs is also significantly affected by the gases being measured, which is a critical issue for the reactive gases used in many semiconductor processes. We have explored these problems in a collaboration with the University of Maryland on the use of RGAs to control a tungsten CVD process in a commercial tool. This experiment involves the measurement of two highly reactive gases, WF_6 and HF, as well as H₂. The objectives are threefold: To test in situ RGA-calibration procedures in a process tool, to examine the quantitative behavior of RGAs operating under process conditions, and to examine the feasibility of using RGAs for process control.

DELIVERABLES: Develop and characterize a primary flow meter based on constant-pressure operation. 4Q 2002

2. This flowmeter uses optical interferometry to measure and control the displacement of a piston of known cross-section. Controlling the piston's rate of displacement maintains a constant pressure in the gas accumulation volume.

DELIVERABLES: Develop and characterize an improved transfer standard for gas flow. 4Q 2002

3. The second-generation transfer standard is based on laminar flow through a quartz capillary impedance. It operates at higher flow rates with a smaller slip correction and much smaller centrifugal effects than the first-generation transfer.

DELIVERABLES: In collaboration with the University of Maryland, demonstrate real-time process control in a CVD process tool. 4Q 2002

Accomplishments

Residual gas analysis, combined with *in situ* calibration, was demonstrated to control deposited tungsten thickness to better than ~1 % de-

spite intentionally introduced systematic and random process variations in temperature and process gas flow.

• We built and tested a gravimetric primary standard for low flow rates of gases. Its measurement principle (weighing) is very different from that of the constant-pressure flow meter already in use (pressure-volume-temperature). In combination, the two primary standards provide a powerful verification of the flow measurement accuracy. Comparisons of the two primary standards show agreement to within 0.1 %.

• A new transfer standard for low flow rates of gases was built and tested. The use of quartz capillary flow impedances avoids problems with the interior roughness of stainless steel capillaries, and it allows the use of an accurate analytical model for centrifugal effects. Tests show that temperature-induced errors of the transfer standard are less than 0.01 % per Kelvin; which is negligible. Preliminary tests on helium and argon show agreement with nitrogen to within the uncertainty of the published viscosity values of these gases.

• Temperature and frequency locking electronics for a real-time optical diagnostic system were fabricated.

The majority of a gas handling and metering system to handle wet hydrogen fluoride also was constructed. Hydrogen fluoride is the principal species of interest in the CVD tool at the University of Maryland (UMD).

• At UMD, several improvements to the CVD process tool were completed in preparation for installation of an optical diagnostic system. These improvements allow operation at higher yield rates more typical of industrial processes. The relevant gas concentrations have increased, thereby increasing measurement sensitivity and reducing measurement error. Previously, low conversions caused layer thickness measurement errors that were typically 10 %. The recent improvements decreased this to about 1 %.

• An acoustic-based technique to measure species ratio was successfully tested at UMD. It is expected to provide complementary measurements for the optical approach under development at NIST.

• We used the second-generation transfer standard to make two international comparisons of gas flow. The first, with the National Metrology Institute of Japan, was made at NIST. The second, with the Istituto di Metrologia "Gustavo Colonnetti," was made in Torino, Italy.

Recent Publications

R.F. Berg and S.A. Tison, "Laminar flow of four gases through a helical rectangular duct," *AIChE Journal* 47, 263 (2001).

R.F. Berg, D.S. Green, and G.E. Mattingly, "Mass flow research and standards: NIST workshop results," *Future Fab International*, edition 10 (2001).

R.F. Berg, D.S. Green, and G.E. Mattingly, "Workshop on mass flow measurement and control for the semiconductor industry," *NIST Special Publication 400-101* (2001).

J.T. Herron and D.S. Green, "Chemical Kinetics Database and Predictive Schemes for Humid Air Plasma Chemistry. Part II. Neutral Reactions," *Plasma Chemistry & Plasma Processing* 21, 459 (2001).

Test Metrology Program

Lead counts of several thousand per chip and test frequencies in the microwave regime challenge current test methodologies. The overall task is to develop test methodologies to address these new requirements.

Accurate at-speed test methodology of digital integrated circuits is a critical requirement. Traditional methods utilizing IC contact probing technology requires large contact pads incompatible with current IC designs. The development of alternative probing approaches through non-contact and intermittent probing techniques appear very promising. However, to implement these techniques, solving the at-speed test calibration issues is crucial. With the challenges facing designers and the rising costs of development, it is crucial to develop accurate testing strategies.

Metrology for System-on-a-Chip (SoC)

Goals

Develop solutions to key metrology issues confronting the semiconductor SoC industry. These include development of measurement methods and standards for characterizing non-digital Virtual Components (ND-VCs), a critical class of building blocks from which SoCs are developed. One focus is on delivering standards to facilitate the incorporation of MEMS based VCs into SoCs. The project activities include: multitechnology hardware description language (HDL) model development, VC interface standards, synthesis and scaling standards for ND-VCs compatible with digital methodologies, testing standards and verification standards. General purpose MEMS based integrated gas-sensing VCs will be used as a test bed to demonstrate the viability of these standards. In addition, the demonstration of general purpose gas-sensing VC methodologies will be used to facilitate the adoption of Multiple Circuit Technologies (MT-VCs) into new Homeland Security and Industrial applications.

Customer Needs

The driving force in today's semiconductor industry is the need to maintain a rate of improvement of 2x every two years in highperformance components. Historically, these improvements have relied exclusively on advances made in semiconductor miniaturization technology. The 1999 International Technology Roadmap for Semiconductors (ITRS) suggests that, "innovation in the techniques used in circuit and system design will be essential to maintain the historical trends in performance improvements." Achievement of this advancement in circuit and system design techniques is increasingly becoming dependent on integrating multiple circuit technologies (MT) into a single chip referred to as System-on-a-Chip (SoC). The design challenges for SoC-MT devices will be overcome with the use of platform-based design approaches that emphasize design reuse, i.e. the development of ND-VCs that can be used as cost-effective building blocks for SoC-MT devices.

The challenges for SoC-MT devices are discussed in the 2001 International Technology Roadmap for Semiconductors in the Design, System Drivers and Test and Test Equipment sections.

Technical Strategy

1. The key to developing successful ND-VCs for SoC-MT devices it to make the ND-VCs, for all practical purposes, look like digital VCs. The first step in this multi-step process is to develop the ability to make the ND-VC devices via a CMOS compatible process. To demonstrate this capability we have chosen a MEMs hotplate based VC, including operational amplifiers and decoders to process the data.

DELIVERABLES: Build and evaluate a ND-VC consisting of a small array of micro hotplates, sensors, operational amplifiers, and decoders. 2Q 2002

2. The second step in making the ND-VC look like a digital VC is to build a digital interface shell around the ND-VC. Since the ND-VC needs to interface to the digital circuitry of the system, this shell will add no additional cost to the system and having digital circuitry on as many of the interfaces as possible will greatly simplify the definition of the ND-VC's IO. To facilitate this approach we will develop methodologies and standards for adding digital shells to ND-VCs and demonstrate them on the ND-VC above.

DELIVERABLES: Develop methodologies and standards for designing digital interface shells for ND-VCs and demonstrate their viability via our micro hotplate gas sensor technology. 4Q 2003

3. The predominant design approach used by industry for SoC devices is top-down design. This requires that high-level HDL models exist for the VCs that are candidates for use in any particular system of interest. Compared to those for digital VCs, the methodology and standards for developing high-level models for ND-VCs is at best poorly developed. To address this need, high-level models are being developed for ND-VCs using Analog and Digital Hardware Description Languages, and methodologies are being developed to validate the models.

DELIVERABLES: Develop methodologies and standards for developing high-level models for ND-VCs and demonstrate their viability via our micro hotplate gas sensor technology. 4Q 2003

4. After the high-level simulation of the system in the top-down design process is successfully completed, the next step is to synthesize the individual VCs. Compared to those for digital VCs, the methodology and standards for ND-VC Technical Contacts: R. W. Michelet A. R. Hefner, Jr. synthesis is at best poorly developed. To address the need for synthesizing ND-VCs, we are developing standards and metrologies for a non-digital synthesis like process that is compatible with digital synthesis. This process is based upon libraries of existing designs and the device design equations.

DELIVERABLES: Develop methodologies and standards for an equivalent ND-VC synthesis approach and demonstrate its viability via our micro hotplate gas sensor technology. 2Q 2004

5. Scaling digital circuitry is a key capability used by digital designers to reduce the costs of their designs. Since most systems that would use ND-VCs will be predominately digital, it is important that there be an equivalent scaling capability for the ND-VCs. To address the need for scaling ND-VCs, we are developing for metrologies for non-digital scaling processes.

DELIVERABLES: Develop methodologies and standards for an equivalent ND-VC scaling approach and demonstrate its viability via our micro hotplate gas sensor technology. 2Q 2005

6. The testability of ND-VCs represents another significant challenge since standards and methodologies for non-digital circuits do not exist. The most promising approach to address testability is to use Built-In-Self-Test (BIST) techniques. To facilitate this approach we will develop methodologies and standards for adding BIST to ND-VCs and interface them via the digital shell.

DELIVERABLES: Develop methodologies and standards for assessing the testability of ND-VC devices and demonstrate their viability via our micro hotplate gas sensor technology. 2Q 2005

Accomplishments

A monolithic micro-gas-sensor system was designed and fabricated in a standard CMOS process. The gas-sensor system incorporated an array of four micro hotplate-based gas-sensing structures. The system utilized a thin film of tin oxide (SuO_2) as a sensing material. The interface circuitry on the chip has digital decoders to select each element of the sensing array and an operational amplifier to monitor the change in conductance of the film. The chip is post-processed to create micro hotplates using bulk micromachining techniques. Detection of gas concentrations in the 100 parts-per-billion range was achieved. This represents a factor of 100 improvement in sensitivity compared to existing MEMS-based micro-hotplate gas sensors.



Figure 1. Micrograph of gas-sensor system to be used as demonstration vehicle.

Recent Publications

M. Y. Afridi, J. S. Suehle, M. E. Zaghloul, D. W. Berning, A. R. Hefner, S. Semancik, R. E. Cavicchi, "A Monolithic Implementation of Interface Circuitry for CMOS Compatible Gas-Sensor System." ISCAS-2002

Nonlinear Device Characterization

Goals

Develop and support general methods of characterizing the large-signal responses of nonlinear devices, components, and circuits; refine and transfer these methods through interactions with industrial research and development laboratories.



Dr. Kate Remley performs large-signal measurements of an RF power amplifier using the Nonlinear Network Measurement System.

Customer Needs

Radio-Frequency measurements are applied extensively in the deployment of commercial wireless communication systems. They are crucial to all stages of system development, from device modeling, to circuit design and system performance characterization. NIST's RF and microwave measurement support recently expanded to address the critical need for accurate large-signal measurements of nonlinear electrical devices and networks, and to support industrial standards development.

Technical Strategy

The Nonlinear Device Characterization (NDC) Project is verifying measurement-based descriptions of devices, circuits, and systems that contain nonlienar elements. The RF transistor amplifier is a key nonlinear component with which engineers are currently contending. Industrial experts estimate that the RF power amplifier accounts for 60-70% of the base station costs and 20-30% of the total wireless link cost. Traditional microwave circuit design has relied on the ability to cascade circuit elements through simple linear operations and transformations, but engineers lose the ability to predict circuit performance across operating environments, or states, when their circuits include a nonlinear element. Presently, there is a critical need for fundamental RF measurement techniques to develop and validate nonlinear device and circuit models. Contributions in this area will significantly improve design-cycle efficiency and trade between manufacturers, and will eventually facilitate improvements in communications through the full incorporation of nonlinear models at the system design level.

The NDC Project recently acquired and established a new measurement facility known as the Nonlinear Measurement Network System (NNMS). This experimental system provides the most general approach to measuring large-signal responses. It is a stimulus-response network analyzer that supplies periodic signals, then acquires broadband incident and reflection waveforms at the device under test. The NIST facility will be used as a reference system in measurement and model comparisons. The project team is developing accurate calibration and measurement techniques for the NNMS, including validation of the Nose-to-Nose calibration technique, the only practical and available method of measuring the phase relations of components in signals with 50 GHz bandwidths. The project team is now refining the statement of measurement uncertainty in the Nose-to-Nose method and will apply it to the NNMS measurements.

The NNMS is first being applied to canonical circuits to compare general measurements with predictions made by circuit simulators and new behavioral models. The project team has applied these techniques to identify stable verification circuits that will be used in NIST-sponsored inter-laboratory comparisons. Second, the measurements system is being applied to develop and verify artificial neural network (ANN) models for nonlinear circuits being developed in cooperation with the University of Colorado. NNMS data will be used to train ANN models, to verify circuit operation and model predictions, and to validate circuit optimization approaches.

The NDC Project has also started to examine the link between nonlinear circuit descriptions and system performance simulations. Members of the Technical Contact: Don DeGroot

"Agilent Lightwave Division would like to encourage NIST's continued work to develop the nose-tonose characterization, so that the technology can become more widely available."

Dennis Derickson, Agilent technologies, Inc. NDC Project have assembled a measurement system to characterize the performance of wideband and broad-band communication links.

Plans are underway with the University of Colorado to establish a Research Center for Nonlinear Electronics in Wireless at Radio Frequencies (newRF). This Center, funded by industrial members, will support graduate research projects. Graduate research assistants and CU faculty will work with NIST staff on newRF projects. The Center will increase the effectiveness of the NIST facilities while developing a new class of technical professionals who have the skills required by industry.

Accomplishments

• Expanded numerical simulations of the Nose-to-Nose calibrations as the basis for an uncertainty statement on the NNMS phase alignment. There are no other methods of identifying the error terms due to the internal sampling electronics used by the Nose-to-Nose equipment. The simulator-based sensitivity study gives us the basis for a first-level uncertainty bound.

Adapted Multiline TRL Calibration for NNMS and included in commercial software, with Agilent collaborators. All users of current and future NNMS-like instruments will have access to this NIST reference calibration in their daily measurements.

Added modulated signal capabilities to the NIST NNMS. Demonstrated modulated signal measurements on example RF amplifier. Conducted multiple modulation calibrations to study instrument repeatability. NIST can now use the NNMS to characterize circuits using two-tone and multi-tone signals, and then compare these to commonly used figures of merit.

Designed interlaboratory measurement comparison for nonlinear network analyzer users. Designed and fabricated prototype verification circuits. Formulated initial comparison method and measures. Performed initial comparisons between NIST and Belgian research labs. Users of NNMS and related nonlinear network analyzers will gain assurance in their ability to identify nonlinear input-output transfer functions or extract model parameters.

Developed nonlinear models for verification devices. Developed and applied conventional compact diode models. Developed frequencydomain behavioral modeling strategy with the University of Colorado. Developed time-domain behavioral model with guest researcher from K. U. Leuven, Belgium. The interlaboratory comparison of nonlinear network analyzers requires models since we do not have a generalized nonlinear parameter to compare. The models can accurately represent the nonlinear transfer functions of the verification circuits over the statespace that they are characterized, allowing participants to find the differences between their measurements and our model predictions.

• Developed first-generation metrics for comparing data from nonlinear circuit characterizations. These tools can easily summarize the differences found in multidimensional data sets common to nonlinear network analysis. The metrics will be used immediately in the NISTsponsored measurement comparison.

Developed generalized approach to measurement-based frequency-domain models of nonlinear circuits. Demonstrated ANN models to define and obtain large-signal scattering functions. This approach is proving useful in improving the efficiency of nonlinear circuit design and optimization. It is currently the only definition of large-signal scattering functions that does not assume some level of linearization.

• Concluded second phase of a Passive Intermodulation measurement comparison. Participants determined how well their measurements compared to ensemble averages for characterizations of a verification device with ultra-low passive intermodulation response.

■ In collaboration with Professor K. C. Gupta of the University of Colorado at Boulder, applied artificial neural networks (ANNs) to improve the modeling of on-wafer open-short-load-thru (OSLT) standards and coaxial line-reflect-match (LRM) calibrations used for calibrating vector network analyzers. The new methods will be used in *Time-domain Network Analyzer* (DNACal) and new NNMS software.

Discovered nonlinear error mechanism in the Nose-to Nose calibration. Through an innovative combination of large-signal and small-signal analyses, showed how nonlinear junction capacitance in the sampler circuit induces an error that had been ignored in the initial Nose-to-Nose analysis.

Initiated NIST's Nonlinear Network Measurement System (NNMS) and conducted NIST's first large-signal nonlinear device verification experiments. Agilent Technologies delivered the NNMS instrument in fulfillment of a custom

equipment contract and extensive collaborative research effort with NIST.

Collaborations

Agilent Technologies, Inc., Network Measurement and Description Group. To develop measurement uncertainty statement for NNMS and NNMS-like instruments.

University of Colorado, Electrical and Computer Engineering Department. To develop new measurement-based behavioral models of nonlinear RF circuits and devices.

NIST ITL Statistical Engineering Division and EEEL Electromagnetic Technology Division. To develop standard nonlinearity, then use it to verify NNMS calibrations and modeling approaches; to extend nonlinear circuit models to system characterization.

Free University of Brussels, Belgium. To determine general nonlinear modeling descriptors for modulated signal responses.

K.U. Leuven, Belgium. To develop models for measurement comparison verification devices, and to study instrument repeatability.

Recent Publications

K. A. Remley, D. C. DeGroot, J. A. Jargon, and K. C. Gupta, "A method to compare vector nonlinear network analyzers," 2001 IEEE MTT-S Internat. Microwave Symp. Dig., pp. 1667-1670, May 21-24, 2001.

K. A. Remley, D. F. Williams, D. C. DeGroot, J. Verspecht, and J. Kerley, "Effects of nonlinear diode junction capacitance on the nose-to-nose calibration," IEEE Microwave Wireless Comp. Lett., vol. 11, no. 5, pp. 196-198, 2001.

J. A. Jargon and K. C. Gupta, "Artificial neural network modeling for improved coaxial line-reflect-match calibrations," Internat. J. RF Microwave Computer-Aided Eng., vol. 11, no. 1, pp. 33-37, Jan., 2001.

D. F. Williams and K. A. Remley, "Analytic sampling-circuit model," IEEE Trans. Microwave Theory Techn., vol. 49, no. 6, pp. 1013-1019, 2001.

J. A. Jargon, "Measurement Comparison of a Low-Intermodulation Termination for the U.S. Wireless Industry," NIST Technical Note 1521, Jul. 2001. J. A. Jargon and K. C. Gupta, "Artificial neural network modeling for improved on-wafer line-reflect-match calibrations," 31st European Microwave Conf. Dig., Sep., 2001.

J. A. Jargon, P. Kirby, K. C. Gupta, L. Dunleavy, and T. Weller, "Modeling Load Variations with Artificial Neural Networks to Improve On-Wafer OSLT Calibrations," 56th ARFTG Conf. Dig., pp. 76-88, Boulder, CO, Nov. 2000.

J. A. Jargon, K. C. Gupta, and D. C. DeGroot, "Artificial neural network modeling for improved on-wafer OSLT calibration standards," Int. J. RF Microwave Computer-Aided Engin., vol. 10, no. 5, pp. 319-328, Sep., 2000

L. Rouault, B. Verbaere, D. DeGroot, D. LeGolvan, and R. Marks, "Measurements and models of a power amplifier suitable for 802.16.1," IEEE 802.16.1 p-00, Sep. 13, 2000

P. D. Hale, T. S. Clement, K. S. Coakley, C. M. Wang, D. C. DeGroot, and A. P. Verdoni, "Estimating the magnitude and phase response of a 50 GHz sampling oscilloscope using the "Nose-to-Nose" method," 55th ARFTG Conf. Dig., pp. 35-42, June 13, 2000

D. C. DeGroot, P. D. Hale, M. Vanden Bossche, F. Verbeyst, and J. Verspecht, "Analysis of interconnection networks and mismatch in the Nose-to-Nose calibration," 55th ARFTG Conf. Dig., pp. 116-121, June 16, 2000

K. A. Remley, D. F. Williams, and D. C. DeGroot, "Realistic sampling-circuit model for a Nose-to-Nose simulation," 2000 IEEE MTT-S Int. Microwave Symp. Dig., June 11-16, 2000

J. A. Jargon and D. C. DeGroot, "NIST unveils status of PIM testing," Microwaves & RF, pp. 78-81, Jan., 2000

D. F. Williams, K. A. Remley, "Nose-To-Nose Response Of A 20 GHz Sampling Circuit; Proc., 54th Auto. RF Tech. Group Conf., 2-3 Dec. 1999, Atlanta, Ga, pp. 64-70; December 1999.

D. C. DeGroot, K. L. Reed, And J. A. Jargon, "Equivalent Circuit Models For Coaxial Oslt Standards," 54th ARFTG Conf. Dig., pp. 103-115, Dec. 3-4, 1999

J. A. Jargon, D. C. DeGroot, "Comparison Of Passive Intermodulation Measurements For The U. S. Wireless Industry;" NIST TN 1515; October 1999

J. A. Jargon, D. C. DeGroot, K. L.; Reed, NIST Passive Intermodulation Measurement Comparison For Wireless Base-Station Equipment;" Dig., Auto. RF Tech. Group Conf. 3-4 December 1998, Rohnert Park, Ca, pp. 128-139; December 1998

At-Speed Test of Digital Integrated Circuits

Technical Contacts: D.F. Williams J. Moreland P. Kabos J. Kopanski

"As electronic devices shrink into the nanometer size scales and integrated circuits operate at multi-GHz clock rates, probing their internal characteristics is becoming both more critical and far more difficult than ever before."

Travis M. Eiles, Ph.D. Intel Corp.

Goals

Develop and demonstrate metrology for the atspeed test of digital integrated circuits. The program will resolve the essential metrology issues of at-speed digital integrated circuit test. It will apply its results to characterizing and calibrating high-impedance probes, develop atomic force microscopes (AFMs) capable of precisely positioning field probes above the surface of the integrated circuit, and push the current on-chip sampling technologies now being explored by the industry.

Customer Needs

The semiconductor industry needs accurate metrology for the at-speed test of digital integrated circuits. Traditional IC contact probing technology requires large contact pads incompatible with the operation and economic constraints of modern IC designs. Alternative probing approaches use high-impedance probes, noncontact probes, atomic-force microscopes, electron beams, optical beams, or on-chip samplers that respond to either electric or magnetic fields near transmission lines in the circuits. However, while the uncalibrated field measurements performed by these probing systems are suitable for field mapping, they are a far cry from the precise measurements of voltages and currents required for electrical design.

Solving the critical at-speed test calibration issues will add enormous value to the probing systems currently being used or developed for high-performance digital integrated circuits. Developing characterization and calibration methods for high-impedance probes, whether of the conventional type or mounted on atomicforce microscopes, will help speed the development and implementation of these new measurement tools, and so create a new paradigm for the at-speed test of high-speed digital integrated circuits.

The need for noninvasive waveform measurements in silicon integrated circuits is discussed in the Test and Test Equipment section, pages 1-5, 2001 International Technology Roadmap for Semiconductors.



Test of a commercial high-impedance probe.

Technical Strategy

1. We will develop calibration artifacts with precisely known high-frequency voltages and circuits suitable for characterizing and calibrating high-impedance probes and samplers of all types. We will focus on fundamental calibration issues: transforming the response of the probes to the electric and magnetic fields above the integrated circuit into accurate voltages and currents inside the circuit.

DELIVERABLES: Demonstrate calibration method for commercial contacting highimpedance probes, and show concrete improvement in measurement results. 2Q 2002

2. We will first apply the characterization and calibration procedures to conventional highimpedance probes, and then to miniature AFM probes suspended on custom cantilevers designed for high frequency measurements. We will follow up with a round robin, and will use the results to help other groups to characterize their measurement approaches. We will also investigate the application of the calibration artifacts to the onchip samplers now being pursued by a number of large semiconductor manufactures, including Intel, Motorola, and IBM.

DELIVERABLES: Apply method to custom noncontacting probes for AFM test station. 4Q 2002.

DELIVERABLES: Develop and calibrate nnncontacting AFM waveform measurement system. 4Q 2003.

Accomplishments

We have designed and tested a prototype sinusoidal waveform standard.

• We have constructed a high-speed electrooptic sampling system.

• We have developed, fabricated and tested a noninvasive AFM scanning probe for measuring local microwave power.

• We have developed a method of characterizing and calibrating conventional high-impedance probes for low-invasive waveform measurements.

• We have applied our high-impedance-probe characterization method to a probe mounted on an atomic-force microscope.

Recent Publications

D.F. Williams and D.K. Walker, "0.1-10 GHz CMOS Voltage Standard," IEEE Workshop on Signal Propagation on Interconnects, Titisee-Neustadt, Germany, May 19-21, 1999.

U. Arz, D.F. Williams, D.K. Walker, J.E. Rogers, M. Rudack, D. Treytnar, and H. Grabinski, "Characterization of Asymmetric Coupled CMOS Lines," 2000 International Microwave Symposium Digest, June 11-16, 2000.

A. Jander, J. Moreland, and P. Kabos, "Dielectric Micromachined Calorimeter Probe for High Resolution Microwave Power Measurements Based on Ferromagnetic Resonance," 15th IEEE Int. Conf. on MicroElectroMechanical Systems, Jan. 20-24, 2002, Las Vegas, Nevada.

D.F. Williams, P.D. Hale, T.S. Clement, and J.M. Morgan "Mismatch Corrections for Electro-optic Sampling Systems," 56th ARFTG Conference Digest, Nov. 30-Dec. 1, 2000.

U. Arz, D.F. Williams, D.K. Walker, and H. Grabinski, "Asymmetric Coupled CMOS Lines: An Experimental Study," IEEE Trans. Microwave Theory and Tech.

D. F. Williams, B.K. Alpert, U. Arz, and H. Grabinski, "Causal Characteristic Impedance of Planar Transmission Lines," IEEE Trans. on Microwave Theory and Tech., Dec. 2000.

A. Jander, J. Moreland, and P. Kabos, "Micromechanical Detectors for Local Field Measurements Based on Ferromagnetic Resonance," Journal of Applied Physics, pp. 7086-7090, June 2001.



A high-frequency AFM probe for making waveform measurements.



A 1 mm long dielectric bimaterial cantilever AFM probe fabricated at NIST for noninvasively measuring local microwave power.

Jitter and Propagation Delay Measurement

Technical Contacts: N.G. Paulter D.R. Larson D.I. Bergman

"Accurate

characterization of the jitter on a signal, as well as a system's ability to tolerate jitter are critical... for the designer and manufacturer of communication systems and components."

Brian Scott, Agilent Technologies

Goals

To develop methods for accurately measuring timing jitter in high bit rate (> 10 GB/s) telecommunication systems and develop systems and protocols for measuring and computing propagation delay through active circuits. This includes the development of artifact standards, data analysis procedures extraction and and algorithms, and measurement systems, each where necessary. Existing measurement methods will be examined to determine consistency amongst them, measurement limitations, and range of applicability. Measurement services will be developed for the measurement of different types of jitter and for propagation delay.

Customer Needs

Jitter is a limiting factor in the performance of high-frequency/high-speed telecommunications and computer systems. In a telecommunications system, where a series of clock-recovery circuits is typically used, jitter degrades data recovery performance. Jitter measurements on telecommunications components and equipment are needed to assure compatibility between manufacturers and to identify sources of jitter. For microprocessor chips, the jitter in the on-chip phase-lock-loop circuit is used by the manufacturer to sort the microprocessor for clock speed usage. Large errors in the measurement of clock jitter represent manufacturing yield loss. Furthermore, for some high-speed computers, the frequency of the microprocessor clock is a multiple of the system clock frequency, and jitter degrades the timing tolerance of the circuit. The data storage industry is also concerned with jitter in recovery of data from the source media.

The calibration of jitter measurement equipment to an uncertainty of a few picoseconds is a difficult problem. Several types of jitter measurements that are important are: transition-totransition jitter, jitter relative to a fixed clock, jitter spectrum, and data dependent jitter. These measurements are important for determining the source of jitter and component compatibility. To test components accurately, jitter generation is important. Industry has reported to NIST that they get inconsistent results from jitter measurements using different techniques and would welcome a neutral party to evaluate the limits of the many measurement methods. The importance of jitter measurement capability is described in the 2001 International Technology Roadmap for Semiconductors on several pages. In particular, on page 11, it states, "The jitter generated by the transmitter is the key parameter to guarantee transmitter quality. Currently, jitter measurement capability on ATE is in its infancy – there is no instrument available that simultaneously satisfies the noise floor, analog bandwidth, and test time requirements for high performance interfaces."

Propagation Delay - Propagation delay in active circuits is defined as the difference between the occurrence of some event on an output signal relative to that of the input signal. The measurement of this type of delay is not straightforward because the characteristics of the input signal affect both the characteristics of the output signal and the time the output signal exits the circuit. Automated test equipment (ATE) from different manufacturers produce different input signals, and this results in different delays for a given circuit. Furthermore, the ATE results may not emulate actual delays because the ATE signal and/or electrical environment may not represent accurately what is expected by the circuit.

The ability to reproducibly measure propagation delay is an issue. This will require interaction with industry to develop an accepted reference signal and, perhaps, impedance environment. Furthermore, accurate (picosecond) delay measurements will require traceability over the delay ranges (several microseconds) required by industry. Measurement protocols will also have to be established.

Technical Strategy

To develop a precision differential delay system that will be used to measure jitter and propagation delay in electronic circuits and systems. The hardware for providing differential delays to 1 µsec will be designed and developed, and the temperature sensitivity and repeatability of the differential delay settings will be measured. In addition, methods for accurately (uncertainties \pm 1 ps) calibrating the discrete differential delays will be developed. A continuously variable differential delay from 0 ns to 1 ns and methods for accurately calibrating the delay transfer function and its temperature sensitivity will also be developed.



Eye diagram for jitter measurements.

DELIVERABLES: Develop the general design of the precision differential delay system. 2Q 2002

DELIVERABLES: Design and build the medium differential delay (1 ns to 16 ns) subsystem. 1Q 2003

DELIVERABLES: Design and build the coarse differential delay (> 10 ns) and fine differential delay (< 2 ns) subsystems. 2Q 2003

DELIVERABLES: Design calibration methods for and calibrate the precision differential delay system. 4Q 2003

Accomplishments

New project.

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Manufacturing Support

Certain disciplines such as statistical process control are generic to all aspects of manufacturing. These disciplines are equally applicable to the manufacture of the materials and the manufacturing equipment as well as the manufacturing of the integrated circuits, their packaging and testing. NIST has one project jointly with ISMT in this category; the creation of an engineering statistical handbook on the internet.

NIST/SEMATECH Engineering Statistics Internet Handbook

Goals

The goal of the NIST/SEMATECH Engineering Statistics Internet Handbook project is to produce an online resource to help scientists and engineers incorporate statistical methods into their work more efficiently. An online publication and a practical, example-driven format were chosen to make the Handbook readily accessible to its target audiences in industry, including the semiconductor manufacturing industry in particular.

Customer Needs

Semiconductor manufacturing requires extraordinary discipline in process control. For example, a typical integrated circuit manufacturing process involves several hundred steps. These steps may include as many as thirty lithographic levels, which require extremely precise alignment with respect to one another. Tight process control is essential to produce a functional circuit. SEMATECH has recognized the importance of statistical process control in semiconductor manufacturing and has developed and maintained expertise in this field since its inception in 1988. Two of the more difficult issues impeding routine implementation of these techniques, however, include educating the users and making the tools easy to use.

Technical Strategy

NIST and SEMATECH formed a collaboration under the umbrella Cooperative Research and Development Agreement (CRADA), combining the general expertise in engineering statistics at NIST with the semiconductor manufacturing expertise resident at SEMATECH.

DELIVERABLES: Release of the final version the Handbook. 2Q 2002

Accomplishments

Since the beta release of the Handbook, efforts have focused on responding to feedback from users, developing, implementing and testing additional case studies, chapter editing and addressing accessibility issues. User feedback has been very positive and constructive and has helped us prepare for the release of the final version of the Handbook.



NIST Engineering Statistics Internet Handbook team (left to right, Alan Heckert, Mark Reeder, Will Guthrie, and Carroll Croarkin) reviewing a page from the chapter on product reliability

Collaborations

International SEMATECH, Paul Tobias, Jack Prins, Chelli Zey; project planning, organization, writing and editing.

AMD, Barry Hembree; project planning, organization, and writing.

Motorola, Pat Spagon; project planning, organization, and writing.

Recent Publications

NIST / SEMATECH Engineering Statistics Internet Handbook M. Carroll Croarkin and Paul Tobias, editors, http://www.nist.gov/stat.handbook/.



Page from a new case study recently added to the process modeling chapter of the Handbook. Technical Contacts: W.F. Guthrie A. Heckert J.J. Filliben

"I am thoroughly enjoying your Engineering Statistics Handbook. Thanks so much for adding real value to the information available on the Internet!!!"

Paul Zaremba, Systems Engineer, Aailent Technoloaies Technical Contacts: B. Goldstein Y. Li

Supply Chain Communication and Automation Needs Assessment in the Semiconductor Industry

Goals

This project will investigate and document key issues related to electronic data exchange, supply chain communication, and other automation standardization needs confronting the semiconductor industry. Emphasis will be placed on determining how to further advance electronic design automation (EDA) and e-manufacturing in the industry as well as an appropriate NIST role in facilitating development of standards for the electronic exchange of intellectual property (IP), virtual components and other technical data among supply chain partners.

Customer Needs

Increasing technological requirements has led the semiconductor industry to seek further means of cost savings by improving factory productivity, streamlining business models, and accelerating their supply chain. The growing complexity of product development and manufacturing models in parallel with shrinking product lifecycles further exacerbate the challenges the industry faces. Maximizing interoperability among automation systems in the factory and throughout the supply chain will become a greater issue for realizing the semiconductor industry's hopes to reduce time, inventory, and therefore costs.

Integration of FICS [Factory Information Control System] applications with business-level software systems provides accurate factory floor data for supply management, and improved product tracking. Potential solutions will require the standardization of technologies that enable this level of integration. 2001 International Technology Roadmap for Semiconductors, Factory Integration (ITRS), p. 17

The semiconductor design industry is migrating towards the reuse and commerce of designs that can be custom assembled and configured with other "off the shelf" design elements in order to leverage existing low-level component designs from intellectual property (IP) vendors. According to the 2001 ITRS, design complexity has been growing exponentially due to the increasing density and number of transistors to meet performance goals. IP reuse allows companies to place greater focus on designing more complex systems while minimizing support and time to market. Standard formats for IP specifications

1572

and tool interfaces for the design of a System-ona-Chip (SoC) would reduce time to market by eliminating the need for translations. Security mechanisms must also be incorporated to protect IP during transfers.

Other information exchange gaps in design houses include standard data formats for timing and power to expedite timing closure, reduce design iterations and promote interoperability among best of breed software tools.

Cost of design is the greatest threat to continuation of the semiconductor roadmap. 2001 ITRS, Design, p. 1

The 2001 ITRS further describes upcoming challenges confronting factory integration. The difficulties lie in managing complexity and optimizing factory production while insuring flexibility, extendibility, and scalability of new technologies, equipments, and standards to prolong factory equipment life. Development of data exchange and interface standards to reduce integration time and complexity has become a necessity for rapid, cost-effective implementation of material handling, e-diagnostics, and advanced process control (APC).

The trend towards large global, geographically distributed partnerships to incorporate the diversity of expertise provides further testimony to the need for electronic data interchange standards. A consensus on exchange formats and a need to support complex conversations and various transport mechanisms among the multiple levels of factory and business-to-business (B2B) communications is paramount to advancing semiconductor technologies in a cost-effective manner.

Technical Strategy

Attendance in workshops, conferences, and standards meetings held by key figures in the semiconductor community such International SEMATECH (ISMT), Semiconductor Equipment Materials International (SEMI) and RosettaNet provides opportunities to assess current areas of IT standards development. As the industry moves towards utilization of mainstream computing technologies including eXtensible Markup Language (XML) and Simple Object Access Protocol (SOAP), the project also provides guidance in leveraging existing best practices from other industries and to promote collaborations among industry partners for mutual benefit.

The investigation also includes an informal survey of semiconductor supply chain partners including designers, chip manufacturers, and equipment suppliers to gauge their existing practices, requirements and priorities. Site visits will provide an opportunity for key industry figures to share their vision of how IT standards would expedite advancement of new technologies and business models.

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DELIVERABLES: White paper evaluating semiconductor industry's IT standards needs and priorities as well as an assessment of potential solutions to the current challenges based upon cross-industry solutions facing similar issues. 4Q 2002

As appropriate, the survey also provides an opportunity for providing insights and guidance from similar industry efforts in supply chain and equipment communication standards to facilitate existing standards developments.

In response to industry needs, the survey will validate internal NIST IT projects against the semiconductor industry's requirements. One potential project is the Infrastructure for Integrated Electronics Design and Manufacturing (IIEDM). IIEDM has facilitated neutral XMLbased standards development in the electronic exchange of technical and business data in the electronic components supply chain. Similarities in challenges and technologies utilized may manifest an opportunity for future collaborations. In addition, experience with standards development in various industries affords NIST with a foundation to provide the impartial cross-industry benchmarks for IT exchange strategies.

DELIVERABLES: Define potential NIST roles in providing technical assistance to facilitate current IT standards development in the semiconductor industry. 4Q 2002

Accomplishments

Discussed IT standards issues facing ASICs designers with representatives from BAE. Standardizing timing and power calculations formats were among the most critical priorities. Standard library formats, such as Open Library Architecture (OLA) by Silicon Integration Initiatives (Si2), are being implemented in the EDA arena.

Surveyed current standards development activities in semiconductor manufacturing and potential NIST roles in various task forces by attending SEMI Standards Meetings March 17-22, 2002. Diagnostic Data Acquisition (DDA), XML, Process Control System (PCS), and Equipment Engineering Capabilities (EEC) are possible areas where NIST can play a future role. Leveraging use of mainstream technologies appears to be widely accepted. Data acquisition standards, including issues of data modeling, speed, bandwidth, quality and integrity, have become critical in advancing e-manufacturing efforts. Follow-up discussions with members of SEMI and ISMT indicated interest in enlisting NIST expertise and contacts to leverage best practices from other industries on specific issues such as XML-based standards development for manufacturing, timing and synchronization of equipment data, as well as data security issues.

Began assessment of IT standards needs in developing APC systems by attending the 3rd Annual European Advanced Equipment Control (AEC)/Advanced Process Control (APC) Conference. Proven benefits of AEC/APC have led to industry acceptance as a requirement for further technological and business advancements in semiconductor manufacturing. To realize the vision of seamless integration among APC components, interface standards would become a necessity. Ensuring interchangeability requires standardization of data formats and fundamental features, while interoperability requires standard interfaces among equipments, remote diagnostic mechanisms. and manufacturing equipment systems.

Discussed current key issues and potential NIST roles with Alan Weber, and began initial phase of drafting the white paper on IT standards needs in the semiconductor industry.

Meetings have also been arranged with Agere, IBM, and Dominion/Micron to gauge their viewpoints and future directions in meeting the impending challenges.

Collaborations

Alan Weber and Associates, Alan Weber; process control system standards needs and potential solutions.

SEMI XML, Diagnostic Data Acquisition Task Forces

Abbreviations and Acronyms

AC	alternating current
ADR	adiabatic demagnetization refrigerator
AEM	analytical electron microscopy
AES	Auger-electron spectroscopy
AFM	atomic force microscope
ALMWG	Analytical Laboratory Managers Working Group (ISMT)
AMAG	Advanced Metrology Advisory Group (ISMT)
ANSI	American National Standards Institute
ARXPS	angle resolved x-ray photoelectron spectroscopy
ASPE	American Society of Professional Engineers
ATP	Advanced Technology Program (NIST)
BCB	benzocyclobutene
BESOI	bond and etch-back silicon-on-insulator
BGA	ball-grid array
BIPM	Bureau International des Poids et Mésures
BIST	built-in self-test
BST	barium strontium titanate
C-AFM	calibrated atomic force microscope (NIST)
C-V	capacitance-voltage
CAD	computer-aided design
CCD	charge-coupled device
CD	critical dimension
CMOS	complementary metal oxide semiconductor
CMP	chem-mechanical polishing
CRADA	Cooperative Research and Development Agreement
CRDS	cavity ring-down spectroscopy
CSP	chip-scale package
CTCMS	Center for Theoretical and Computational Materials Science (NIST)
CVD	chemical vapor deposition
DC	direct current
DFT	design-for-test
DMA	differential mobility analyzer
DRAM	dynamic random-access memory
DSP	digital signal processing
DUV	deep ultraviolet
EBSD	electron backscatter diffraction

EELS	electron energy loss spectroscopy
EDC	embedded decoupling capacitance
EDS	energy-dispersive spectroscopy
EMC	electromagnetic compatibility
EMI	electromagnetic interference
EPMA	electron probe microanalysis
EUV	extreme ultraviolet
FIFEM	field ion field emission microscope
FIM	field ion microscope
FWHM	full-width half-maximum
GIXR/SE	grazing incidence x-ray reflection/spectrascopic ellipsometry
GIXPS	grazing incidence x-ray photoelectron spectroscopy
HRTEM	high resolution transmission electron microscope
HSQ	hydrogen silsesquoxane
I-V	current-voltage
IGBT	insulated-gate bipolar transistor
IPC	Association Connecting Electronics Industries
ISMT	International SEMATECH
ISO	International Organization for Standardization
ITRS	International Technology Roadmap for Semiconductors
LEED	low-energy electron diffraction
LER	line-edge roughness
LFPG	low frost-point generator
LOCOS	LOCal oxidation of silicon
LPP	laser-produced plasma
LPRT	light-pipe radiation thermometer
MBE	molecular beam epitaxy
MEMS	micro-electro-mechanical systems
MFC	mass flow controller
MMIC	millimeter and microwave integrated circuits
MOS	metal-oxide-semiconductor
MOSFET	metal-oxide-semiconductor field-effect transistor
MUX	multiplex
NCMS	National Center for Manufacturing Sciences
NDP	neutron depth profiling
NGL	next generation lithography
NEMI	National Electronics Manufacturing Initiative

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NIST	National Institute of Standards and Technology
NLO	non-linear optical
NSOM	nearfield scanning optical microscopy
OMAG	Overlay Metrology Advisory Group (ISMT)
PED	Precision Engineering Division (NIST)
PLIF	planar laser-induced fluorescence
PMI	phase-measuring interferometer
PTB	Physikalisch-Technische Bundesanstalt
PZT	lead zirconium titanate
QM	quantum mechanics
RAM	Random-access memory
RGA	residual gas analyzer
RTA	rapid thermal annealing
RTP	rapid thermal processing
SANS	small-angle neutron scattering
SBIR	Small Business Innovative Research
SCM	scanning capacitance microscope
SEM	scanning electron microscope
SHG	second harmonic generation
SIA	Semiconductor Industry Association
SIMOX	separation by implantation of oxygen
SIMS	secondary-ion mass spectrometry
SoC	system-on-chip
SOI	silicon on insulator
SPM	scanning probe microscope
SRC	Semiconductor Research Corporation
SRM [®]	Standard Reference Material
SSHG	surface second-harmonic generation
SSIS	surface-scanning inspection system
SURF III	Synchrotron Ultraviolet Radiation Facility III
TCAD	technology computer-aided design
TDDB	time-dependent dielectric breakdown
TDR	time-domain reflectometry
TEM	transmission electron microscope
TFTC	thin-film thermocouple
TOF	time-of-flight
TMAH	tetramethyl ammonium hydroxide

UHV	ultra-high vacuum
UV	ultraviolet
WMS	wavelength modulation spectroscopy
VUV	vacuum ultraviolet
XPS	x-ray photoelectron spectroscopy

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