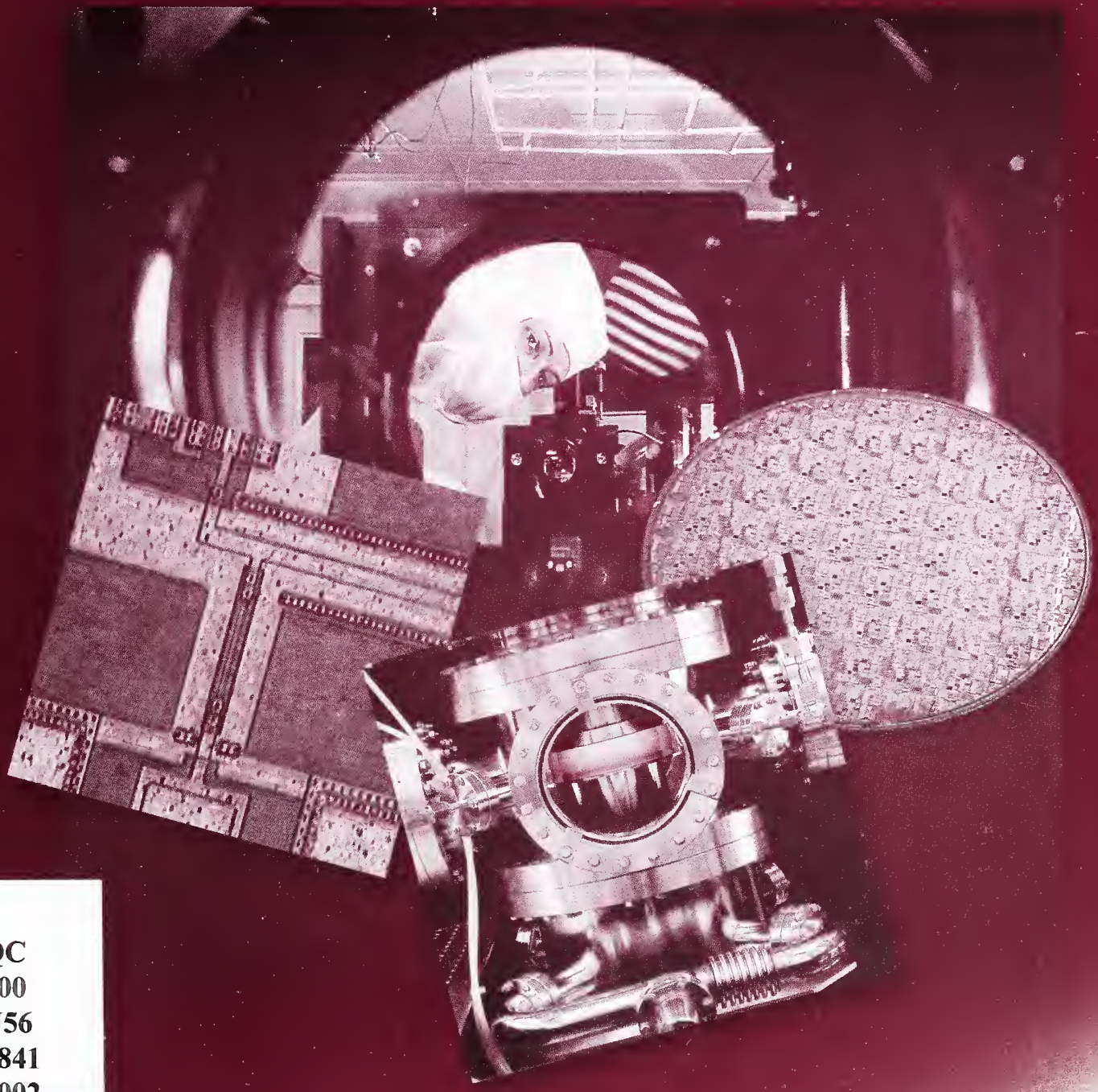
National Institute of Standards and Technology
Technology Administration
U.S. Department of Commerce

NISTIR 6841
January 2002

d Electrical Engineering Laboratory

Office of Microelectronics Programs

Programs, Activities, and Accomplishments



The Electronics and Electrical Engineering Laboratory

Through its technical laboratory research programs, the Electronics and Electrical Engineering Laboratory (EEEL) supports the U.S. electronics industry, its suppliers, and its customers by providing measurement technology needed to maintain and improve their competitive position. EEEL also provides support to the Federal government as needed to improve efficiency in technical operations, and cooperates with academia in the development and use of measurement methods and scientific data.

EEEL consists of six programmatic divisions and two matrix-managed offices:

Electricity Division

Semiconductor Electronics Division

Radio-Frequency Technology Division

Electromagnetic Technology Division

Optoelectronics Division

Magnetic Technology Division

Office of Microelectronics Programs

Office of Law Enforcement Standards

This document describes the technical programs of the Office of Microelectronics Programs. Similar documents describing the other Divisions and Offices are available. Contact NIST/EEEL, 100 Bureau Drive, MS 8100, Gaithersburg, MD 20899-8100, Telephone: (301) 975-2220, On the Web: http://www.eeel.nist.gov

Cover Caption: The National Semiconductor Metrology Program (NSMP) is a NIST-wide effort to meet the highest priority measurement needs of the semiconductor manufacturing industry and its supporting infrastructure. Research efforts include development of precise measurement techniques for characterizing aspheric lenses for Extreme Ultraviolet Lithography; development of standard test structures for interconnect reliability evaluation; development of advanced at-speed test techniques for gigahertz integrated circuits; and fundamental measurements of ionization cross sections of gas species used in plasma processing of integrated circuits.

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U.S. DEPARTMENT OF COMMERCE
Donald L. Evans, Secretary

Technology Administration
Phillip J. Bond, Under Secretary of Commerce for Technology

National Institute of Standards and Technology
Arden L. Bement, Jr., Director

Disclaimer: Certain commercial equipment and/or software are identified in this report to adequately describe the experimental procedure. Such identification does not imply recommendation or endorsement by the National Institute of Standards and Technology, nor does it imply that the equipment and/or software identified is necessarily the best available for the purpose.

References: References made to the International Technology Roadmap for Semiconductors (ITRS) apply to the edition, dated 1999, available at the time of writing this document. The most recent edition, November 2001, has some changes. It is available from the Semiconductor Industry Association (SIA), 181 Metro Drive, Suite 450, San Jose, CA 95110, phone: (408) 436-6600, fax: (408) 436-6646.

Contents

Welcome

The **Office of Microelectronics Programs** provides coordination of silicon semiconductor manufacturing metrology activities across NIST to maximize the impact of this critical industry on the health of the U.S. economy. The Office, with a permanent staff of three, is located in Gaithersburg, Maryland, and is one of the two Offices in the Electronics and Electrical Engineering Laboratory at NIST.

Many of the projects managed by the Office are cooperative activities across several Operating Units. Thus the projects are able to leverage the best expertise available for the specific task across NIST, regardless of organizational structure. Our projects are also aligned by research TASK area: Lithography Metrology, Critical Dimension and Overlay Metrology, Thin Film and Shallow Junction Metrology, and Device Modeling, Design and Test Metrology.

Additional activities of the Office which insure timely response to industry need include:

Extensive interactions with industry consortia, such as the Semiconductor Research Corporation (SRC) and International SEMATECH (ISMT).

Participation in the road mapping activities commissioned by the Semiconductor Industry Association and administered by International SEMATECH.

Standards bodies activities related to the semiconductor industry including the Semiconductor Equipment and Materials International (SEMI) standards program, American Society of Testing and Materials (ASTM) in the U.S., and Deutsches Institut fur Normung (DIN) in Germany.

For additional information about the Office of Microelectronics Programs, please visit our website http://www.eeel.nist.gov/omp/.

Stephen Knight, Director

Vision

The Office of Microelectronics Programs will be recognized as an outstanding organization managing and coordinating projects key to meeting the metrology needs of the semiconductor manufacturing industry.

Values

The Office of Microelectronics Programs values relevance and focus of its projects in solving crucial metrology issues facing the semiconductor manufacturing industry. The Office values the technical excellence and the dedication of the scientists, engineers, and technicians participating in the National Semiconductor Metrology Program.

Mission

The mission of the Office of Microelectronics Programs is to manage the National Semiconductor Metrology Program (NSMP), a NIST-wide effort designed to meet the highest priority measurement needs of the semiconductor manufacturing industry and its supporting infrastructure industries as expressed by the International Technology Roadmap for Semiconductors and other authoritative industry sources.

Goals

The Office of Microelectronics Programs will:

Diligently identify critical metrology gaps confronting the semiconductor manufacturing industry, and implement robust projects to confront those needs;

Insure expeditious technology transfer of NSMP results to the industry; and

Assist the NIST technical body in interfacing efficiently with key elements of the semiconductor manufacturing industry and its research and development community.

National Semiconductor Metrology Program

The NSMP was established in 1994 with a strong focus on mainstream silicon CMOS technology and an ultimate funding goal of $25M. Current funding from NSMP is $12M, with additional funding from the laboratories of $14M, supporting a broad portfolio of semiconductor metrology development projects conducted in six of the Operating Units of the Measurements and Standards Laboratories of NIST:

Electronics and Electrical Engineering Laboratory (EEEL)

Manufacturing Engineering Laboratory (MEL)

Chemical sciences and Technology Laboratory (CSTL)

Physics Laboratory (PL)

Materials Science and Engineering Laboratory (MSEL)

Building and Fire Research Laboratory (BFRL)

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FRONT ROW: BARBARA BELZER AND MICHELE BUCKLEY.

Lithography Metrology Program

Advances in lithography have largely driven the spectacular productivity improvements of the integrated circuit industry, a steady quadrupling of active components per chip every three years over the past several decades. This continual scaling down of transistor dimensions has allowed more and more components on a chip, lowered the power consumption per transistor, and increased the speed of the circuitry. The shrinking of device dimensions has been accomplished by shortening the wavelength of the radiation used by the lithography exposure tools. The industry at this point has moved into the deep ultraviolet (DUV) spectrum. Currently, exposure tools operating at 193 nm are being introduced, and exposure tools operating at 157 nm are in development. Looking beyond the deep ultraviolet, extreme ultraviolet radiation (EUV) at 13 nm is being investigated, and demonstration tools are being designed and assembled. The overall goal of this task is to support these developments in DUV and EUV. The areas of emphasis are lens materials, laser calorimetry, radiation detector sensitivity and damage, EUV lens metrology, and metrology for the development of advanced photoresist materials.

Metrology Supporting Deep Ultraviolet Lithography

Technical Contacts:
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M. Dowell
R. Gupta

Staff-Years (FY 2001):
7 professional
2 guest researcher

Funding Sources:
STRS (85 %)
Other Agency (15 %)

Goals

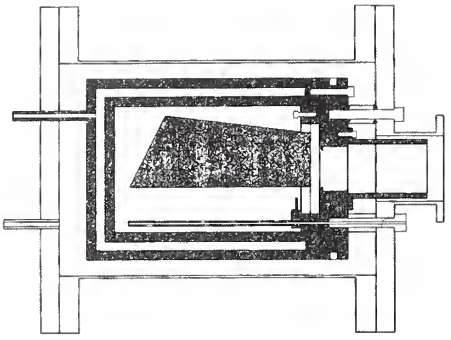
Develop solutions to key metrology issues confronting the semiconductor lithography industry. These include development of measurement methods and standards for characterizing deep ultraviolet (DUV) laser sources, detectors, and materials. One focus is on delivering high-accuracy measurements of UV detector parameters and materials properties of immediate need by the industry. There is ongoing activity in the following areas: standards development, calibration services, characterization of optical materials, sources, and detectors, in addition to advising customers on in-house measurements.

Customer Needs

Increasing information technology requirements have yielded a strong demand for faster logic circuits and higher-density memory chips. This demand has led to the introduction of DUV laser-based lithographic tools for semiconductor manufacturing. These tools, which employ KrF (248 nm) and ArF (193 nm) excimer lasers, have led to an increased demand for accurate measurements at DUV laser wavelengths. Next generation tools employing F_2 (157 nm) excimer lasers, projected for insertion into production lines by 2005, require even higher accuracy measurements. To support these efforts, the National Institute of Standards and Technology (NIST), with ISMT support, has initiated a DUV metrology program focusing on the characterization of DUV optical materials, sources, and detectors.

Technical Strategy

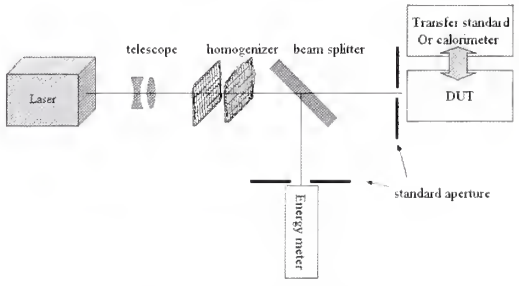
Beginning with the first edition of the National Technology Roadmap for Semiconductors (NTRS) in 1992, the semiconductor industry has made an organized, concentrated effort to reduce the feature sizes of integrated circuits. As a result, there has been a continual shift towards shorter exposure wavelengths in the optical lithography process. Because of their inherent characteristics, deep ultraviolet (DUV) lasers, specifically KrF and ArF, and more recently F_2 excimer lasers, are the preferred sources for high-resolution lithography at this time. To meet the laser metrology needs of the optical lithography community, we have developed primary standards and associated measurement systems at 193 and 248 nm, and in the process of developing standards for 157 nm measurements.



EXCIMER LASER CALORIMETER FOR 157 NM MEASUREMENTS.

DELIVERABLES: Develop a 157 nm excimer laser primary standard and calibration service to provide support for the next generation of optical lithography.

In addition to existing DUV laser measurement services, there is increasing demand for laser dose, *i.e.*, energy density, measurements, where the detector samples a fraction of the total laser beam. Accurate laser dose measurements are important because small area detectors are widely used to monitor laser pulse energy density at the wafer plane of a lithographic tool. Accurate measurements of laser dose are especially crucial to the development of new mask resist materials, since lower dose requirements lead to greater wafer throughput and also extend the lifetime of an exposure tool's optical components.



DOSE METER CALIBRATION SYSTEM. THE ENERGY METER ACTS AS A MONITOR TO RECORD PULSE-TO-PULSE LASER ENERGY FLUCTUATIONS.

DELIVERABLES: Establish a dose measurement service for 193 nm excimer lasers.

High-accuracy measurements of the index properties of UV materials is a requirement for the design of DUV lithography systems. To meet

this demand NIST has developed methods to make measurements of the DUV refractive index, as well as its wavelength, temperature, and stress dependencies to the high accuracy needed. Index variations and birefringence have become a limiting factor in the development of the optics for lithography systems, especially at 157 nm. To address this problem we have developed unique VUV polarimetry and Twyman-Green interferometer systems to measure 157 nm index variation in lens materials due both to external stress and grown-in defects.

DELIVERABLES: By the end of 2002, have the capability of completely characterizing index inhomogeneities of DUV materials near 157 nm at the sub ppm level.

In the course of our measurements we discovered that in addition to index variations and birefringence due to material defects and external stress, there are also index variations and birefringence *intrinsic* to the material. The commonly-accepted assumption that the cubic symmetry of the crystals used would ensure the isotropy of the optical properties, in fact breaks down due to the finite value of the photon momentum q. This previously-neglected effect on ultraviolet optics has a $1/\lambda^2$ wavelength dependence, and is negligible at visible wavelengths, where the index homogeneity and birefringence are measured. However, at 157 nm the effect is large (ten times the 157 nm birefringence specification), and this has serious implications on 157 nm lithography system design and performance. This intrinsic birefringence must be accurately characterized for all materials considered for optics in 157 nm systems, including the mixed crystals $Ca_{1-x}Ba_xF_2$ we are co-developing that have the potential of having negligible intrinsic birefringence.

DELIVERABLES: By the end of 2002, have completely characterized the intrinsic birefringence of UV materials, including mixed crystals.

We are developing a new method for measuring the refractive index of transmissive samples to a high accuracy 0.1 ppm inthe DUV and VUV using a VUV FT spectrometer. This method is directed to measurements down to 135 nm using synchrotron radiation as a continuum source.

DELIVERABLES: Measurements of refractive index in the VUV using an interferometric technique in conjunction with SURF III.

Our efforts for complete characterization of the optical properties of materials involve measuring the transmittance, reflectance, surface and bulk scatter, and surface and bulk absorption. This characterization is done on one of the beamlines at the NIST Synchrotron Ultraviolet Radiation Facility (SURF) which is devoted to material and detector characterization in the wavelength range 120 nm to 320 nm. We have used this facility to characterize various samples of calcium fluoride where the transmittance and reflectance was measured with an uncertainty of better than 1 %.

SURF III acts as the primary standard for both sources and detectors in the DUV and VUV spectral region. Efforts are underway to use this facility to achieve a 0.1 % standard uncertainty of UV irradiance from 3 nm to 400 nm, and will enable accurate, direct radiance, and irradiance comparisons with new as well as existing source transfer standards.

Monochromatized radiation from SURF III along with a cryogenic radiometer is used to provide absolute detector-based radiometric calibrations in the spectral range from 125 nm to 320 nm with a standard uncertainty of better than 1 %. This facility has also been used to study the degradation in diodes induced by exposure to UV radiation. A wide variety of diodes (Si diodes from Hamamatsu, nitrided Si diodes from IRD, PtSi, GaN, GaP, GaAsP, and diamond) were characterized for spectral responsivity and uniformity mapping, and the degradation in these diodes at 130 nm was also measured.

A new facility for characterizing the degradation of diodes to excimer radiation at 157 nm has been completed. This facility allows the measurement of the spectral responsivity of the devices in the spectral range from 130 nm to 500 nm along with the measurement of the reflectivity of the diodes as the devices are irradiated by the excimer radiation. This allows identification of potentially stable diodes for UV irradiance measurements. The facility can also be used to characterize other types of detectors such as photochromic films.

DELIVERABLES: Characterize the stability of a variety of semiconductor diodes to excimer radiation at 157 nm.

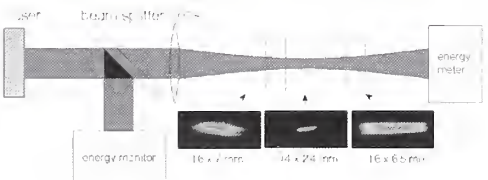
We plan to use the synchrotron radiation in conjunction with a cryogenic radiometer to measure the transmittance, reflectance, surface and bulk losses, which would lead to a complete optical characterization of the transmissive samples. Capability will also be developed to make polarization dependent measurements in the spectral range from 125 nm to 320 nm.

DELIVERABLES: By end of 2002, build a state of the art facility for an accurate and complete characterization of the optical properties of transmissive materials.

Accomplishments

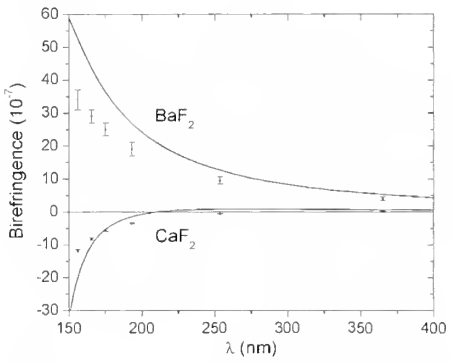
- Established capability to accurately perform absolute responsivity calibrations of laser dose meters at the laser wavelength of 193 nanometers. Additional excimer laser wavelengths will be added to this service in the near future. The dose measurements are performed using a beam-splitter-based calibration system in which a spatially uniform beam from an argon-fluoride excimer laser is generated using a special beam homogenizer. The beam propagation properties, including uniformity or homogeneity, are fully characterized with a state-of-the-art beam profile measurement system based on a pyroelectric camera array. This uniform beam then is used to irradiate a NIST-calibrated aperture placed immediately in front of the test detector.

- We determined the damage thresholds and lifetimes of several materials using 157 and 193 nm excimer lasers and a beam profile technique similar to ISO 11254-2. We made these measurements to select an appropriate absorbing material for use in our primary standard laser calorimeter for 157 nm excimer laser power measurements. The materials we tested were nickel-plated sapphire, chemically-vapor-deposited silicon carbide (CVD SiC), nickel-plated copper, and polished copper. Applied pulse energy densities (or dose) ranged from 80 to 840 mJ/cm^2. We determined the applied dose from a series of laser beam profile measurements. Silicon carbide had the highest damage threshold: 730 mJ/cm^2 per pulse. For this reason, and for its high thermal and electrical conductivities, we have chosen silicon carbide as the absorber material for the 157 nm calorimeter.



DAMAGE THRESHOLD MEASUREMENTS. BEAM PROFILES WERE RECORDED AND CHARACTERIZED AT 22 PLANES ALONG THE PROPAGATION AXIS USING A CCD CAMERA AND QUANTUM CONVERTER. THREE ENERGY DENSITY DISTRIBUTIONS AT INNER- AND OUTER-MOST POSITIONS, TOGETHER WITH THEIR DIMENSIONS, ARE SHOWN. THE DIMENSIONS ARE BASED ON THE CALCULATION OF THE SECOND MOMENTS ACCORDING TO ISO 11146.

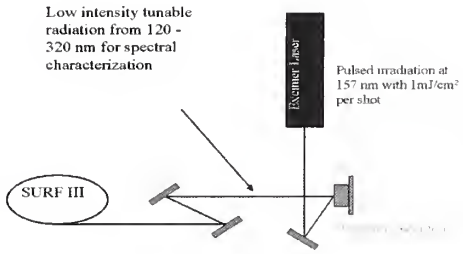
- Using a unique UV polarimetry system we developed, we made the first measurements of an intrinsic birefringence in CaF_2 and BaF_2. These values turned out to be over ten times the 157 nm lithography birefringence target value, and have forced all 157 nm system designs to be substantially redesigned. We developed the complete theory of the effect, now fully accepted, and analyzed its angular dependence. From this we first suggested a compensation approach based on combining lenses of different crystal axis orientations. All 157 nm system designs now utilize this correction approach. We also showed that since the intrinsic birefringence of CaF_2 and BaF_2 have opposite sign, then a mixed crystal $Ca_{1-x}Ba_xF_2$ can in principle be made which has zero intrinsic birefringence at 157 nm. We are working with crystal growers to explore this approach



MEASURED (SYMBOLS) AND CALCULATED (CURVES) INTRINSIC BIREFRINGENCE OF CaF_2 AND BaF_2. THE FIGURE SHOWS THE OPPOSITE SIGN OF THE EFFECT FOR THE TWO MATERIALS AND THE $\approx 1/\lambda^2$ DEPENDENCE. THE VALUE FOR CaF_2 AT 157.63 NM IS 11.2×10^{-6}.

- The stability of semiconductor diodes under irradiation from an excimer laser operating at 157 nm has been evaluated. We have built a facility at SURF III that allows simultaneous exposure of photodiodes to excimer radiation and synchrotron radiation. Measurements of the spectral responsivity can be made in the spectral range from 130 nm to 320 nm with a standard uncertainty of less than 1 %. The intense, pulsed laser radiation was used to expose the photodiodes for varying amounts of accumulated irradiation whereas the low intensity, continuously tunable cw radiation from the synchrotron source was used to characterize the photodiodes. The changes in the spectral responsivity of different kinds of diodes such as UV silicon, GaP, GaAsP, PtSi, diamond, and GaN were measured for a large range of total accumulated dose from an F_2 excimer laser operating at 157 nm. Differing amounts of changes were seen in different diodes depending on the total excimer irradiation dose and they showed different spectral changes in the respon-

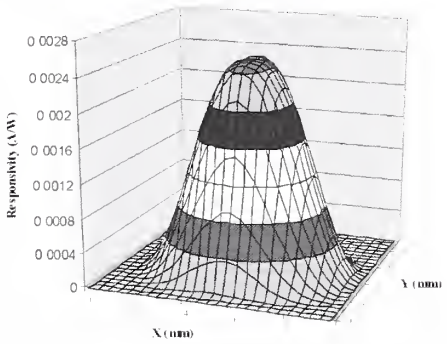
sivity as well. This yields important information about the mechanism responsible for the degradation of photodiodes.



DETECTOR RESPONSIVITY TEST METHOD

■ We have also characterized pyroelectric detectors which are commonly used for high-power laser application. In the vacuum UV to near UV range, pyroelectric detectors are commercially available because of important applications in areas like semiconductor photolithography. Instead of calibrating these detectors using high-power radiation, we performed measurements with low-power UV radiation at beamline 4 of the SURF III. To accommodate the pulse detection nature of the pyroelectric detectors, we installed a 10 Hertz tuning fork chopper at beamline 4 and lock-in amplifiers were used for detector signal processing. Several commercial pyroelectric detectors were tested at our facility. We found that in most cases, the manufacturer-supplied amplifiers were too noisy for our light intensity on the order of one microwatt. Subsequently, a low-noise amplifier was constructed and installed near the detection head. In addition, for several high reflectance pyroelectric detectors, we also measured the reflectance of the pyroelectric element to check the internal quantum efficiency of the detector.

■ We have constructed and characterized a probe that is suitable for accurate measurements of irradiance in the vacuum ultraviolet spectral range. Many industrial applications such as UV curing, photolithography, or semiconductor chip fabrication require accurate measurement of the irradiance and will benefit from having such a stable, accurate UV probe. The probe was characterized at various wavelengths ranging from 157 nm to 325 nm, encompassing many of the important industrial application wavelengths. The principle of measurement of the irradiance is based on scanning the probe in a light field and measuring the spectral responsivity on a grid with regular spacing. Measurement of the spectral responsivity in the center of the probe along with the integrated total responsivity yields the spectral irradiance. This method can alternatively be used to calculate aperture areas as well by measuring the ratio of the total responsivity and the responsivity in the center.



DETECTOR RESPONSIVITY MAP

Recent Publications

Holger Laabs, Richard Jones, Chris Cromer, Marla Dowell, Vlad Liberman, "Damage Testing of Partial Reflectors for 157 nm Laser Calorimeters," Annual Symposium on Optical Materials for High Powered Lasers, *in* press.

Marla Dowell, "Pulsed-laser Metrology at NIST," Optics and Photonics News (February 2001) 28.

Marla Dowell, "The Power of Light: Choosing the Right Detector is Key to Accurate Beam Power Measurements," OE Magazine (January 2001) 56.

M. L. Dowell, C. L. Cromer, R. D. Jones, D. A. Keenan, and T. R. Scott, "New Developments in Deep Ultraviolet Laser Metrology for Photolithography," Characterization and Metrology for ULSI Technology: 2000, D. G. Seiler, A. C. Diebold, T. J. Shaffner, R. McDonald, W. M. Bullis, P. J. Smith, and E. M. Secula, Eds. (AIP, New York, 2001), pp. 391-394.

M. L. Dowell, C. L. Cromer, R. D. Jones, D. A. Keenan, and T. R. Scott, "New Developments in Deep Ultraviolet Laser Metrology for Photolithography," Society of Manufacturing Engineers Technical Note Paper MS00-236 (2000).

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T.A. Germer, Rajeev Gupta, Leonard Hanssen, and Eric Shirley, "Optical Properties of Materials," Optics and Photonics News, **12,** 38, (2001).

P.-S. Shaw, R. Gupta, T.A. Germer, U. Arp, T. Lucatorto, and K.R. Lykke, "Characterization of materials using an ultraviolet radiometric beamline at SURF III," Metrologia, **37,** 551 (2000).

Metrology Supporting EUV Lithography

Technical Contact:
Tom Lucatorto
Ulf Griesmann
Staff-Years (FY 2001):
4.5 professional

Funding Sources:
STRS (86 %)
ATP (14 %)

Goals

Provide leading-edge metrology for the development and characterization of optical components and detectors used in Extreme Ultraviolet Lithography (EUVL). (EUVL utilizes radiation at 13.4 nm.)

Customer Needs

As the features and design rules of the components used in semiconductor chips continue to shrink, we approach the limit at which the diffraction of the DUV presently used for state-of-the-art lithography will prevent further reduction of the dimensions. Thus, within the next few years, the industry will need to identify a suitable "next generation lithography" (NGL) beyond the current DUV-based tools. A leading contender for the NGL is EUVL, development of which is being intensely pursued by US companies through the EUV-Limited Liability Corporation (LLC) consortium.

High resolution imaging with EUV radiation was not possible until the development of multilayer EUV mirrors in the mid 80s. This development has spawned the relatively new field of EUV optics and its associated set of new metrological challenges. Among these are: 1) precise EUV reflectivity maps; 2) EUV dosimetry; and 3) nanometer level optical figure measurement.

Technical Strategy

1. Precise EUV Reflectivity Maps

The present NIST/DARPA EUV Reflectometry Facility is located on a multipurpose beamline on the NIST Synchrotron Ultraviolet Radiation Facility (SURF III) storage ring. The beamline can provide a monochromatic beam of EUV or soft x-ray radiation in the 3 nm to 40 nm (400 eV to 30 eV) spectral range. Although dedicated to serving the EUV optics community by providing accurate measurements of multilayer mirror reflectivities, this beamline with its associated sample chamber has been used for many other types of measurements since the beamline's commissioning in early 1993. Among the other measurements performed recently are grating efficiencies, photocathode conversion efficiencies, phosphor conversion efficiencies, film dosimetry, and determination of EUV optical constants through angle dependent reflectance measurements.

The last year has been spent in commissioning a new, very large sample chamber that can generate a reflectivity map of the entire surface of a large optic (up to 35 cm in diameter and 40 kg in mass) such as those used by the EUV-LLC in their Engineering Test Stand (ETS) which began operation last April. In fact, presently the NIST/DARPA facility is the only one in the world large enough to measure the intact C-I mirror (the first condenser mirror in the ETS stepper), a function we performed this spring. (See figure 1.)

DELIVERABLES: 1. Full uncertainty analysis for reflectivity measurements. 2. Intercomparison on EUV mirror test pieces with PTB (Germany), ASET Laboratory (Japan), and ALS Storage Ring Facility (Lawrence Berkeley Laboratory).

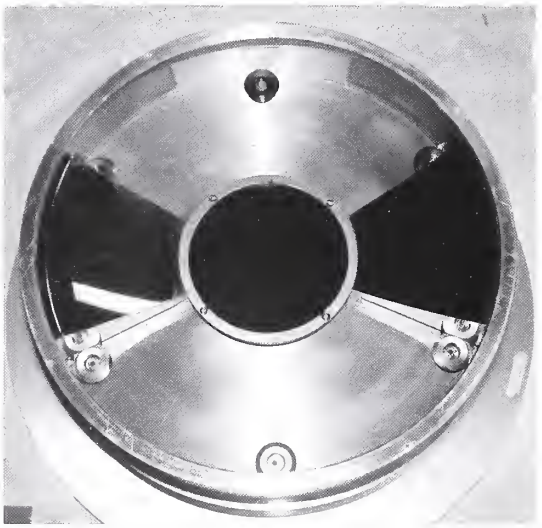

FIGURE 1. C-1 MIRROR FROM THE ETS OF THE EUV-LLC. ONLY TWO OF THE SIX SECTORS ARE SHOWN. THE LASER-PLASMA SOURCE IS POSITIONED ON THE CENTRAL AXIS.

2. EUV Dosimetry

NIST is the primary national source for the radiometric calibration of detectors from the infrared to the soft x-ray regions of the spectrum. Until recently all NIST-characterized EUV photodetectors were calibrated on the SURF storage ring, which is essentially a cw source. In the last year we have designed and built a pulsed EUV source based on the source being used in the ETS to calibrate the EUV wafer-plane dosimeters to be used in EUVL. A schematic of the pulsed radiometric facility is shown in figure 2.

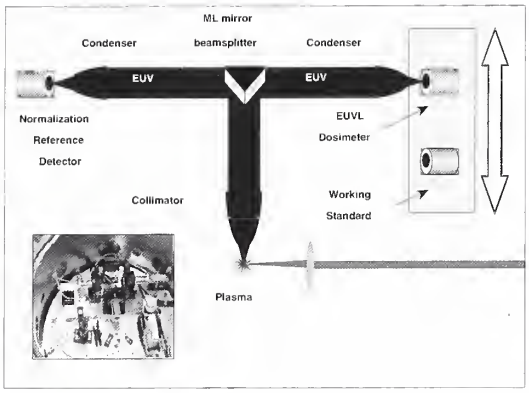

FIGURE 2. SCHEMATIC OF PULSED RADIOMETRIC FACILITY.

DELIVERABLES: 1. Commission pulsed radiometric facility. 2. Provide EUV-LLC with calibrated photodiodes.

3. Nanometer Optical Figure Measurement

The approach to measurement of optical figure is to use phase measuring interferometry (PMI). Commercially available phase measuring interferometers can be extremely repeatable; an array of techniques, including some developed in this program, are now available for separation of part errors from the signature of the instrument – at least for some classes of surface. Such approaches have shown that they can provide measurement uncertainties of the order of I nm and near flats. For the measurement of aspheric optics (i.e., systematic deviations from a base sphere), such as those needed for NGL, there are some basic limitations to the potential of the commercially available PMIs. Concepts for a system combining a PMI with high precision slideways have been developed and implemented (in collaboration with an industrial vendor) in a new measurement capability, known as the NIST X-ray Optics Calibration InterferometeR (XCALIBIR). The goal is 0.25 nm rms uncertainty in measurement of aspheric optics up to 300 mm with focal lengths up to 2 m. XCALIBIR is designed to have the flexibility to measure flat, spherical, and aspheric optics. The interferometer was installed at NIST in the fourth quarter of FY99; a calibration service is being developed based on this capability.

A critical part of the uncertainty evaluation of an ultra-precision interferometric measurement is a ray-trace evaluation of the test. The uncertainty in the radius of curvature of spherical optics in the test limits the accuracy of the models. XCALIBIR is being used to provide state-of-the-art radius of curvature measurements to address this problem.

Lithography at EUV wavelengths also leads to challenging tolerances for the photomask. The mask is the optical element containing the desired wafer pattern; lithography is accomplished by projecting the image of the pattern onto the resist-coated wafer with a several-fold reduction in magnification. Current EUVL designs call for a mask blank flatness of 50 nm. Proposed substrate materials are transparent in the visible and have nearly opposing parallel faces, which makes surface flatness difficult with traditional phase measuring interferometry. A modern version of the Ritchey-Common test based on commercial phase measuring interferometry has been developed at NIST to measure the flatness of photomask blanks. XCALIBIR can be used in a mode with reduced coherence length to measure flatness of parallel windows. Fig. 3 shows the result of a measurement of a photomask.

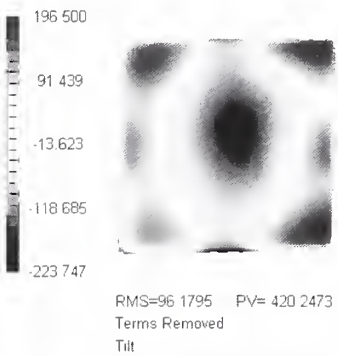

FIGURE 3. PHOTOMASK BLANK FLATNESS MEASURED WITH THE RITCHEY-COMMON TEST.

DELIVERABLES: 1. Complete commissioning of XCALIBIR and establish sub-nm flat test capability for 300 mm flats. 2. Evaluate short coherence length interferometry with XCALIBIR for photo mask blank flatness measurements.

FY Outputs & Outcomes

- Commissioning and comprehensive characterization of the NIST/DARPA large reflectometer.
- Measurement of the C-1 replica for the EUV-LLC ETS instrument.
- Participation in EUV reflectivity intercomparision to assure accuracy of reflectivity measurements standards.
- Initial testing of pulsed radiometry facility for EUV dosimetry.

- Radius of curvature measurements for a nominally 25 mm radius polished Zerodur sphere have been completed on XCALIBIR.

- Photomask blank flatness measurements completed with the Ritchey-Common test.

Recent Publications

C. Tarrio, T. B. Lucatorto, U. Arp, S. Grantham, and L. Deng, "Upgrades to the NIST/DARPA EUV Reflectometry Facility," to appear in Proc. SPIE vol. 4506, *Soft X-ray and EUV imaging systems II.*

C. Tarrio, R. E. Vest, and S. Grantham, "Absolute extreme ultraviolet metrology," Proc. SPIE vol. 4450, *Harnessing light: Optical science and metrology at NIST*, pp. 94-107.

A. Davies, C. Tarrio, and C. J. Evans, "Advanced optics characterization," *Optics and Photonics News*, February, 2001, pp. 34-37.

C. Tarrio, R. E. Vest, S. Grantham, and T. B. Lucatorto, "Extreme Ultraviolet Metrology at SURF III," to appear in *Synchrotron Radiation News.*

Schmitz, T., Davies, A., and Evans, C., "Uncertainties in interferometric measurements of radius of curvature," to appear in Proc. SPIE 4451 (2001).

Evans C. J., Parks R. E, Shao L-Z., Schmitz T., and Davies A. "Interferometric Testing of Photomask Substrate Flatness," Proc SPIE Vol 4344, in press.

Evans C. J., Davies A., Schmitz T., Parks R. E, and Shao L-Z., "Interferometric metrology of Substrates for VLSI," Proc of 2nd EUSPEN International Conference, Turin, May 2001, pp. 388-92.

Lithographic Polymers

Goals

In this project, we are developing an integrated program of fundamental studies of photoresist materials that are correlated with resist performance metrics that will have a broad industrial impact on next-generation photolithography. We work closely with industrial collaborators to develop and apply high spatial resolution and chemically specific measurements to understand varying material properties and process kinetics at nanometer scales and to provide high quality data needed in advanced modeling programs. The unique measurement methods we apply include x-ray and neutron reflectivity (XR, NR), small angle neutron scattering (SANS), incoherent neutron scattering (IENS), near-edge x-ray absorption fine structure (NEXAFS), and combinatorial methods. Our efforts focus on the fundamentals of polymer materials and processes that control the resolution of the photolithography including: (1) the physical properties and polymer chain conformation within sub-100 nm structures, (2) the spatial segregation and distribution of photoresist components, (3) the transport and kinetics of photoresist components and the deprotection reaction interface over nanometer distances, and (4) the structural characterization of lithographically prepared structures. These data are needed to meet the future lithographic requirements of sub-100 nm imaging layers and critical dimensions.

Customer Needs

Photolithography remains the driving and enabling technology in the semiconductor industry to fabricate integrated circuits with ever decreasing feature sizes. Today, most fabrication facilities use chemically-amplified (CA) photoresists, complex and highly tuned formulations of a polymer film loaded with photoacid generators (PAGs) and other additives. Upon exposure of the photoresist film through a mask, the PAG releases acidic protons. A post-exposure bake is then applied and the acid protons diffuse and catalyze a deprotection reaction on the polymer that alters its solubility in an aqueous base developer solution. These reactive and diffusive processes must be understood and controlled at the nanometer length scale to effectively fabricate integrated circuits.

There are significant challenges in extending this technology to fabricate the smaller feature sizes (sub-100 nm) needed to continue performance increases in integrated circuits. First, new radiation sources with shorter wavelengths (193 nm and 157 nm) require photoresist films nearing 100 nm thick to ensure optical transparency and uniform illumination. In these ultrathin films, two-dimensional confinement can induce deviations in several key materials parameters such as the macromolecular conformation, glass transition, viscosity, or transport properties. Furthermore, the required resolution for a sub-100 nm feature will be on the order of 2 nm, approaching the macromolecular dimensions of the photoresist polymers. It is not yet clear how deviations due to confinement will affect the ultimate resolution in these ultra-thin photoresist films. Additionally, the material sources of feature resolution (line-edge and sidewall roughness) and profile control need to be identified and understood to ensure the success of needed patterning technologies.

Computer simulations of the lithographic process are widely used within the semiconductor industry to plan and optimize processing variables to produce integrated circuits. Complex processing steps provide a significant challenge to simulator developers to successfully predict photoresist behavior with smaller features and tighter error budgets. High-resolution data of material, transport, and reaction kinetics on nanometer length scales are needed to benchmark these numerical simulations for future processes. We are developing measurements with sufficient spatial resolution to aid in these efforts.

Technical Strategy

In this project, we use model materials to validate the new measurement methods and fully formulated, patterned materials for structural characterization. Model 248 nm materials are used to address several important fundamental questions including the thermal properties of ultrathin films as a function of film thickness and substrate type, the conformation of polymer chains confined in ultrathin films, the surface concentration of PAGs, the diffusion and the reaction kinetics of the deprotection reaction. We also apply combinatorial methods as a tool to rapidly determine important lithographic parameters and to identify material factors impacting feature resolution. These results provide a strong basis for understanding the material property changes that may affect the development of lithography for sub-100 nm structures using thin photoresist imaging layers.

Technical Contacts:
Eric K. Lin
Christopher L. Soles
Wen-li Wu

Staff-Years (FY 2001):
4.5 professional

Funding Sources:
STRS (60 %)
Other Agency (40 %)

DELIVERABLES: Measure the atomic level-dynamics of photoresist polymer thin films that impact processing variables.

DELIVERABLES: Measure the three-dimensional conformation of polymer chains confined in thin films. Determine length scale at which deviations from bulk conformation become important.

DELIVERABLES: Measure the spatial profile of the deprotection reaction front with angstrom resolution.

DELIVERABLES: Measure the surface concentration of the PAG component in photoresist thin films.

DELIVERABLES: Develop combinatorial methods to quantify rapidly material factors that affect resolution control.

Accomplishments

- Incoherent neutron scattering was used to measure the atomic-level dynamics of model photoresist polymer thin films for the first time. The local, atomic-level, dynamics of the photoresist polymer directly affect transport processes essential to modern photoresists, such as the diffusion of photogenerated acids and other small molecules within the polymer matrix. To date, changes in the local dynamics of polymer thin films have been inferred from changes in macroscopic quantities such as the apparent glass transition temperature, Tg, as a function of film thickness and substrate interaction energies. Direct measurements of the segmental motions of polymer chains confined to ultrathin films provide a molecular picture of observed changes in these macroscopic quantities and insight into differences in photoresist transport processes in ultrathin films. By utilizing different polymers and polymer/substrate combinations, we obtain crucial insight into the dynamical effects of polymer thin film confinement.

- The three-dimensional structure of polymers confined to ultrathin films was measured for the first time using small angle neutron scattering (SANS). In ultrathin photoresist films and sub-100 nm structures, polymer chain conformations may affect key material parameters germane to photoresist processing, such as film quality, thermal stability, line-edge roughness, and both dissolution and etch rates. We performed SANS measurements on polystyrene films that are confined on Si wafers with the thickness as thin as 110 Å, less than 70 % of the radius of gyration, Rg, of the constituent polymer. The conformation perpendicular to the surface is probed by rotating the incident neutron beam to an angle of 35 ° with respect to the Si wafers, thereby tilting the scattering vector out of the plane of the film. The results confirm that within the plane of the film the Rg is Gaussian and bulk-like, while perpendicular to the film the Rg is non-Gaussian and significantly reduced. The chain conformation normal to the surface is distorted even at thickness greater than the bulk diameter (2Rg). Efforts are underway to quantitatively describe the deviations from Gaussian behavior orthogonal to the film as a function of film thickness.

- The deprotection reaction front profile was measured *in-situ* with angstrom resolution using neutron reflectivity from a bilayer structure prepared with a specially labeled (deuterated) protected polymer. The upper layer of the structure is loaded with the PAG. Upon exposure and baking, the acid diffuses into the lower layer and catalyzes the deprotection reaction. The protecting group is deuterated and is volatile upon reaction. Thus, contrast to neutrons results from the reaction allowing for observation of the reaction front. By comparing the reaction front *in-situ* to the developed film profile, we obtain important insight into both the spatial extent of the reaction and the development process itself. These data are the first available with this spatial resolution and are critically needed for the development of process control over nanometer length scales.

- NEXAFS measurements were used to measure the surface concentration of PAG components in model photoresist polymers as a function of common processing conditions. A significant advantage of the NEXAFS measurement is the capability of separating interfacial and bulk signals within the same sample and experiment. NEXAFS measurements of interfacial chemistry are possible because of the limited penetration depth of produced secondary electrons. By separately observing the electron and fluorescence yield, the chemistry at the surface (2 nm) and bulk (200 nm) may be determined. Different chemistries may be observed by examining the near-edge x-ray spectra of light elements such as carbon, oxygen, fluorine, and nitrogen. In this way, changes in the surface chemistry relative to the bulk film can be investigated as a function of lithographic processing steps such as exposure and heating. We have found that PAG segregation is depleted from the surface of films of the deprotected polymer, but enhanced at the surface from films of the protected polymer.

■ Combinatorial methods have been applied to determine rapidly the deprotection temperature of blends of the protected and deprotected model polymers and to quantify the activation energy of the deprotection reaction. Samples were prepared on gradients in temperature and post-exposure bake time. Using a modified high-throughput combinatorial analysis technique, the relationship between composition and deprotection temperature of a model photoresist blend was established. The temperature gradient method provides a quick, reproducible, and surprisingly accurate method of deprotection determination over a wide range of compositions. FTIR was used to establish the correlation between deprotection and the observed color change evident in the combinatorial experiment.

FY Outputs & Outcomes

■ Incoherent neutron scattering was used to measure the atomic-level dynamics of model photoresist polymer thin films for the first time. By utilizing different polymers and polymer/substrate combinations, we obtain crucial insight into the dynamical effects of polymer thin film confinement.

■ The three-dimensional structure of polymers confined to ultrathin films was measured for the first time using small angle neutron scattering (SANS). The results confirm that within the plane of the film the Rg is Gaussian and bulk-like, while perpendicular to the film the Rg is non-Gaussian and significantly reduced. The chain conformation normal to the surface is distorted even at thickness greater than the bulk diameter (2Rg).

■ The reaction front profile was measured *in-situ* with angstrom resolution using neutron reflectivity from a bilayer structure prepared with a specially labeled (deuterated) protected polymer. These data are the first available with this spatial resolution and are critically needed for the development of process control over nanometer length scales.

■ NEXAFS measurements were used to measure the surface concentration of PAG components in model photoresist polymers as a function of common processing conditions. We have found that PAG segregation is depleted from the surface of films of the deprotected polymer, but enhanced at the surface from films of the protected polymer.

■ Combinatorial methods have been applied to determine rapidly the deprotection temperature of blends of the protected and deprotected model polymers and to quantify the activation energy of the deprotection reaction.

Collaborations and Support

■ IBM T. J. Watson Research Center – Dario Goldfarb, Marie Angelopoulos.

■ DARPA – Advanced Lithography

■ Dr. Daniel A. Fischer – MSEL, Ceramics Division

Recent Publications

C. L. Soles, E. K. Lin, J. L. Lenhart, R. L. Jones, W. L. Wu, D. L. Goldfarb, and M. Angelopoulos, "Thin Film Confinement Effects on the Thermal Properties of Model Photoresist Polymers," J. Vac. Sci. Tech. B., accepted (2001).

J. L. Lenhart, R. L. Jones, E. K. Lin, C. L. Soles, W. L. Wu, D. L. Goldfarb, and M. Angelopoulos, "A Combinatorial Methodology to Discovering the Material Factors Controlling Resist Line Edge Roughness, Shape, and Critical Dimension," J. Vac. Sci. Tech. B, accepted (2001)

D. L. Goldfarb, M. Angelopoulos, E. K. Lin, R. L. Jones, C. L. Soles, J. L. Lenhart, and W. L. Wu, "Confinement Effects on the Spatial Extent of the Reaction Front in Ultrathin Chemically Amplified Photoresists," J. Vac. Sci. Tech. B., accepted (2001).

E. K. Lin, W. L. Wu, Q. H. Lin, and M. Angelopoulos, "Feature-shape and Line-edge Roughness Measurement of Deep Sub-micron Lithographic Structures Using Small Angle Neutron Scattering," SPIE Proceedings 26th International Symposium on Microlithography, (2001) in press.

D. L. Goldfarb, Q. H. Lin, M. Angelopoulos, C. L. Soles, E. K. Lin, and W. L. Wu, "Characterization of Thin and Ultrathin Polymer and Resist Films," SPIE Proceedings 26th International Symposium on Microlithography, (2001) in press.

W. L. Wu, E. K. Lin, Q. H. Lin, and M. Angelopoulos, "Small Angle Neutron Scattering Measurements of Nanoscale Lithographic Features," J. Appl. Phys. 88, 7298 (2000).

Critical Dimension and Overlay Metrology Program

The principal productivity driver for the semiconductor manufacturing industry has been the ability to shrink linear dimensions. A key element of lithography is the ability to create reproducible undistorted images, both for masks and the images projected by these masks onto semiconductor structures. Lithography as a whole, fabricating the masks, printing and developing the images, and measuring the results, currently constitutes 0.35 % of wafer processing costs. The overall task of the Critical Dimension and Overlay Program is to assist the industry in providing the necessary metrology support for current and future generations of lithography technology. These goals include advances in modeling, the provision of next generation critical dimension and overlay artifacts, and comparisons of different critical dimension and overlay measurement techniques.

Currently, resolution improvements have outpaced overlay and critical dimension measurement improvements. To maintain cost effectiveness significant advances must be made.

Atom-Based Dimensional Metrology

Goals

Provide technological leadership to semiconductor and equipment manufacturers and other government agencies by developing the methods, tools, and artifacts needed to apply leading edge, high-resolution atom-based dimensional measurement methods to meet the metrology needs of semiconductor microlithography. One specific goal is to provide the customer with the techniques and standards needed to make traceable dimensional measurements on wafers with nanometer accuracy. We are developing three-dimensional structures of controlled geometry whose dimensions can be measured and traced directly to the intrinsic crystal lattice. These samples are intended to be dimensionally stable to allow transfer to other measurement tools which can measure the artifacts with dimensions known on the nanometer scale.

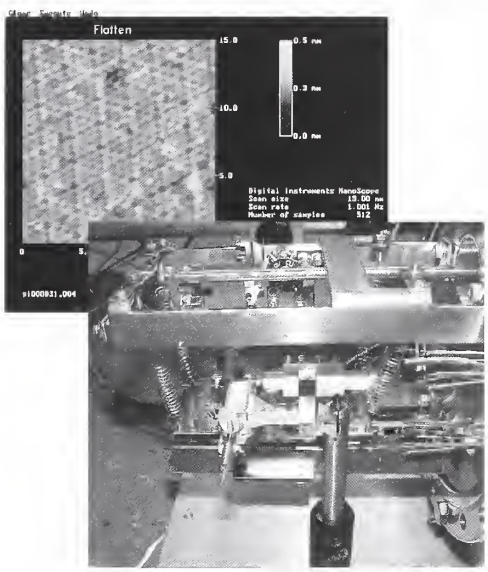

FIGURE 1. THE ATOMIC RESOLUTION IMAGE ABOVE WAS MEASURED WITH A 20 PICOMETER RESOLUTION INTERFEROMETER SYSTEM MOUNTED ON THE UHV STM.

Customer Needs

NIST is responsible to U.S. industry for developing length intensive measurement capabilities and calibration standards in the nanometer scale regime. The new class of scanned probes have unparalleled resolution and offer the most promise for meeting these future needs of the microelectronics industry. One important application of the high-resolution SPM methods is in the development of linewidth standards whose dimensions can be measured and traced through the crystal lattice from which they are made. In addition, these high-resolution tools can be coupled directly to a new NIST-designed picometer resolution interferometer.

FIGURE 2. THIS RECENT RESULT UTILIZES THE ATOMICALLY FLAT SURFACES AS A SUBSTRATE FOR NANOMANUFACTURING. THE FEATURES CDS ARE 10 NM AND THE ENTIRE LATERAL FIELD OF VIEW IS 250 NM.

The work funded in this project is for the development of atom-based linewidth standards to assist in the calibration of linewidth metrology tools and the development of unique interferometry capabilities which can be used in conjunction with accurately measured tips to measure feature critical dimensions. This effort is intended to enable the accurate counting of atom spacings across a feature in a controlled environment and to subsequently transfer that artifact to other measuring instruments as a structure with atomically known dimensions. As critical dimensions continue to shrink, the detailed atomic structure, such as edge roughness or sidewall undercut, of the features to be measured occupies a larger portion of the measurement uncertainty. Furthermore, particularly with SEMs, the instrument response and the uncertainty in the edge location within an intensity pattern becomes a significant issue due to the increased sensitivity to detailed elements of the edge detection model. The complexity of these models and large computer resources required for each individual computation make the idea of having samples of known geometry and width essential. This project is intended to develop samples of known geometry and atomic surface structure which will yield measurements resulting in a specific number of atoms across the line feature or between features. These samples will be measured in the UHV environment and

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R. Silver

Staff-Years (FY 2001):
2.0 professional
1.5 guest researcher
1 student

Funding Sources:
STRS (100 %)

then stabilized and subsequently transferred to other instruments.

There are three primary applications of this type of artifact after it has been atomically counted. The first method is the direct calibration in an SEM for a product wafer whose geometry and material is near to the structure of the atomically counted sample. The second method, utilizes an AFM to calibrate the SEMs with the AFM acting as an SEM matching tool. In this method, the AFM is calibrated with an atomically measured sample of the desired geometry as the product wafer to be measured by the SEMs. This sample only needs to have similar geometry to the product wafer but does require similarity in materials due to the insensitivity of an AFM to materials variations. The AFM which has been calibrated for a particular geometry by an atomic artifact can then transfer that calibration to a product wafer of similar geometry and any material such as photo resist, resulting in a calibrated product wafer which can then be transferred to calibrate an SEM.

The third method uses the number of atoms between features to determine the feature spacing. This method can be used to make magnification and pitch calibration standards based on the intrinsic crystal lattice.

These methods of atom counting and high-resolution interferometry, as outlined in this project description, are non-destructive and are intended to yield samples which can be measured by various instruments such as an SEM and subsequently re-measured atomically. This is a unique and important element of this work since there are no other known methods which allow this kind of atomic dimensional measurement without being destructive. In addition this new method opens up the possibilities of basing the measurement metric on the intrinsic crystal lattice.

Technical Strategy

The technical work is focused into four thrust areas. The first area is the development of methods to prepare photolithographically patterned three-dimensional structures in semiconductor materials. These structures must be prepared in such materials as to allow the atomic surface reconstruction of those features such that the atomic order is commensurate with the underlying crystal lattice. This involves either using conventional photolithography methods for sample production or using the STM itself to fabricate very small nanometer scale features as shown in figure 2.

DELIVERABLES: Write features in silicon with critical dimensions as small as 10 nm. Improve the fabrication robustness to enable the regular processing of features this size.

The second thrust is the development of techniques for the preparation of SPM tips with reproducible geometries and the direct characterization of the SPM tip geometry and dimensions on the atomic scale. These well characterized tip probes can then be used to measure the samples with photolithographically defined and canonically ordered surfaces on the sub-nanometer length scale. We are developing the SPM tip etching, field evaporation, and cleaning procedures which reliably yield stable W tips and produce atomic resolution on Si (7x7) surfaces. These tips are also useful in a collaboration with the SEM project for development of nanotips as SEM field emitters. Our tip preparation methods leave us uniquely qualified in this arena.

The third thrust area in the atom-based metrology effort is focusing on developing artifacts which can be atom counted and then measured in a number of different metrology tools such as SEM and AFM. The integrity of the line geometry, such as side wall angle, is crucial to having useful artifacts for linewidth specimens. These edge geometry requirements are not as stringent for the magnification standards since feature symmetry is the most crucial element in these measurements. The work on linewidth artifacts, therefore, is focused on reducing the process temperatures required for atomic reconstructions. We have made wet chemical processing fully operational and are currently working on preparing atomically ordered Si surfaces at significantly reduced temperatures. For sample preparation, we are utilizing the existing in-situ processing apparatus and techniques from the UHV STM and concentrating on the reproducible production of atomically ordered Si surfaces and Si (111) step and terrace structures.

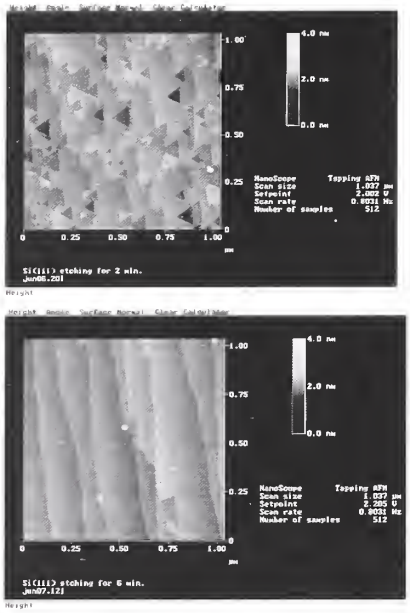

FIGURE 3. THESE ARE ATOMICALLY FLAT, CHEMICALLY PREPARED SURFACES FOR USE IN ATOM-COUNTING AND NANOMANUFACTURING.

The fourth thrust area is the development of a new interferometer system. This system is intended to measure in the 20 picometer resolution range with accuracy in the same range. The system should also be capable of use on the STM so atomic scale measurements can be made with new levels of accuracy. In addition we are exploring new applications of FIM calibrated tips in conjunction with the interferometry to measure CDs of leading edge, small semiconductor features.

DELIVERABLES: Prepare nanotips for use in SEM metrology. Work with the SEM metrology project for the testing of nanotips as SEM field emitters.

The long term technical objective is the development of in-situ stabilized, atomically ordered surfaces which can be transferred to other measurement instruments such as scanning electron microscopes, AFMs, or optical metrology tools. These nanometer scale standard artifacts with atomically ordered surfaces will then act as linewidth or magnification calibration samples. These samples will have been measured either by direct atom counting or high-resolution interferometry and atomically measured tips.

Accomplishments

- We have obtained atomically flat surfaces and are now trying to obtain atomic order, routinely using the low temperature wet chemical based methods. Although, we had a similar effort with

GaAs, which was successful, we are currently focused on silicon substrates

DELIVERABLES: We will design and procure a new set of wafers specifically for atom-based dimensional metrology. This new wafer set will be written by ebeam on silicon (111) wafers.

- The ability to prepare atomically sharp tips in W (111) has been demonstrated and the details of this methodology along with the new models we have developed for analyzing sharpness have been prepared as a journal article.

- We have prepared two publications which give new insight into the etching process for fabricating atomically flat silicon surfaces. The results, seen in figure 3, yield a new, more comprehensive understanding of the physical processes involved in making atomically flat surfaces in silicon as required for much of the work in this project.

- The first UHV transfer was demonstrated between the NIST MBE system and the PED UHV STM. The sample was maintained in a UHV environment during the entire event. Further UHV sample manipulation and preparation for transfer to other systems and long-term storage will be investigated in the future as required.

DELIVERABLES: Work with International SEMATECH for the development of improved methods for preparation of photolithographically patterned three-dimensional double-etched structures in silicon. These structures must be prepared in such materials as to allow the measurements of those features in silicon.

- We have developed techniques for the preparation of SPM tips with reproducible geometries and the direct characterization of the SPM tip geometry and dimensions on the atomic scale. We are now applying these ideas to FIM tips used in SEM metrology.

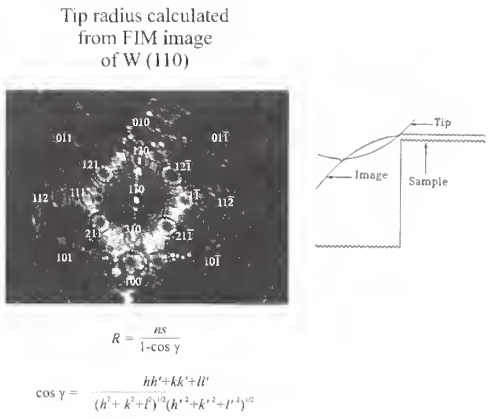

FIGURE 4. AN FIM IMAGE SHOWING THE ATOMIC ORDER IN A W TIP IS SHOWN. THE SCHEMATIC ON THE RIGHT SHOWS THE METHOD OF ATOM COUNTING OR HIGH RESOLUTION TIP-BASED INTERFEROMETRY.

■ We have attempted our first direct measure of the surface atom spacings based on a traceable interferometer measurement. We have fitted our UHV STM with a high accuracy sub-angstrom resolution interferometer. We have closed the loop and made our first atomic resolution measurements with full interferometer length basis. The successful completion of this aspect has enabled direct distance determination with simple atomic counting.

DELIVERABLES: Develop methods for the first demonstration of direct interferometer measurements of surface atom spacings with a complete unbroken uncertainty. Complete this link to develop an unbroken traceability chain to the international unit of length.

■ Wafers from the NIST designed metrology reticle set have been evaluated for use in atom-based dimensional metrology. The initial evaluation is very promising and all four wafer flows yielded good product wafers. These wafers contain the prototype test structures, including a comprehensive set of critical dimension and line space arrays for general metrology purposes. The double-etched silicon multi-level features are intended to provide long term stable artifacts for calibration with the line arrays being test patterns for atom-based dimensional metrology work.

■ We have produced atomically ordered surfaces of GaAs at far reduced temperatures and have worked with patterned GaAs linewidth samples. The GaAs linewidth features have been fabricated and we have successfully prepared As capped samples without damaging the line geometry or integrity in any measurable way. These samples have been processed using the complete atomic surface preparation method, measured in UHV and then allowed to oxidize to create a stable surface for measurement in other tools.

Collaborations:

■ ISMT, IBM, University of Maryland, Dept. of Physics, University of Purdue, Dept. of Physics.

Recent Publications

P.V.M. Rao, C. Jensen, and R. M. Silver, "A Generic Shape Model for STM Tip Geometry," submitted to Ultramicroscopy, (2001).

R. M. Silver, S. Gonda, C. Jensen, and L. Howard, "A New Tunable Diode Laser Method for a Sub-nanometer Resolution Interferometry," to be submitted to Applied Optics, 2001.

J. Fu, H. Zhou, S. Gonda, and R. M. Silver "Wet Chemistry of Si Samples," to be submitted to Applied Physics Letters, in preparation.

Satoshi Gonda, Hui Zhou, Joseph Fu and Richard M. Silver "A new design and uncertainty consideration of a metrology UHV-STM for direct measurements of atom spacings," SPIE Nanotechnology workshop proceedings, NIST 2001.

Hui Zhou, Joseph Fu, S. Gonda and Richard M. Silver, "Processing atomically flat Si surfaces," SPIE Nanotechnology workshop proceedings, NIST 2001.

Scanning Electron Microscope Metrology

Goals

To provide the microelectronics industry with highly accurate SEM measurement and modeling methods for shape-sensitive measurements and relevant calibration standards with nanometer-level resolution. Carry out SEM metrology instrumentation development, including improvements in electron gun, detection, sample stage and vacuum system. Conduct research and development of new metrology techniques using digital imaging and networked measurement tools.

Customer Needs

The scanning electron microscope is used extensively in many types of industry, including the more than $200 billion semiconductor industry in the manufacture and quality control of semiconductor devices. The International Technology Roadmap for Semiconductors targets SEMs as the metrology tool of choice for use in semiconductor production up through at least the year 2005. The industry needs SEM standard artifacts, specifically those related to instrument magnification calibration, performance and the measurement of linewidth. This entails a multidimensional program including: artifact fabrication, understanding the function and signal generation in the SEM, electron beam interaction modeling, developing NIST metrology instruments for the certification of standards, and developing the necessary artifacts and calibration procedures. The manufacturing of present-day integrated circuits requires that certain measurements be made of close to 100 nm structures composing the device with a high degree of precision. The accuracy of these measurements is also important, but more so in the development and pilot lines. The measurements of minimum feature sizes known as critical dimensions (CD) are made to ensure proper device operation. The U.S. industry needs high-precision, accurate, shape-sensitive dimension measurement methods and relevant calibration standards. The SEM Metrology Project supports all aspects of this need since scanning electron microscopy is the major microscopic technique used for this sub-micrometer metrology.

Technical Strategy

The Scanning Electron Microscope Metrology Project a multidimensional project. It is being executed through several thrusts fully supported by the semiconductor industry. SEM Magnification Calibration Artifacts: Primary to SEM dimensional metrology is the calibration of the magnification of the instrument. Standard Reference Material (SRM) 2090 is an SEM magnification standard that will function at the low beam voltages used in the semiconductor industry, high beam voltages used in other forms of microscopy. A prototype with 200 nanometer lines and spaces was fabricated by the Nanofabrication Facility at Cornell University as a proof of concept and was used in a round robin study that clearly demonstrated the need for this standard. Texas Instruments was contracted to supply the first production run of the artifact with 100 nanometer lines and spaces and delivered over 180 of these artifacts. In order to speed the availability of this artifact to the industry (while the final certification details are being completed) the artifact has been released to the industry as Reference Material (RM) 8090.

DELIVERABLES: Completion of the renewal of the AMRAY metrology SEM-based sample calibration measuring system. Preparation of an assessment of the error budget for the fully functional metrology system. Preparation of customized recipes for various versions of magnification calibration samples. Upon availability of suitable quality samples, quality assessment and delivery of a new batch of RM 8090. Upon availability of suitable quality samples, completion calibration and delivery of a batch of SRM 2090 samples.

SEM Performance Measurement Artifact: This effort includes the development of the Reference Material 8091 and evaluation procedures suitable for correctly measuring image sharpness of scanning electron microscopes, especially of those that are used in the semiconductor industry. The performance characteristics of the SEM are particularly important to precise and accurate measurements on the semiconductor processing line. NIST has demonstrated that a critical dimension scanning electron microscope functioning poorly can measure the dimensions 5 nm or more larger than the same instrument functioning optimally. For reliable image sharpness measurements a suitable sample with small features is needed.

SEM Linewidth Measurement Artifacts: Artifacts that are characterized and calibrated to the required small levels of uncertainty were and are in the focal point of the IC industry's dimensional metrology needs. Therefore, at NIST, it has been a mission in long existence to develop and deliver

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M. T. Postek

Staff-Years (FY 2001):
2.2 professional
0.5 contractor
1 student

Funding Sources:
STRS (74 %)
Other Agency (26 %)

appropriate samples. For a long time the possibilities were limited by the lack of various technologies available, especially the development of accurate modeling methods were required. NIST though several years of systematic efforts, developed Monte Carlo simulation-based modeling methods that can deliver excellent results. These new methods can deduce the shape of integrated circuit structures from top–down view images through modeling and library–based measurement techniques with few a nm accuracy. NIST in several publications demonstrated the possibilities and described power of this measuring approach. Based on the newest results, now it is becoming possible to start to develop the long–awaited relevant linewidth standard for the semiconductor industry. Reference Material 8120 line width samples will be a relevant sample on a 200 mm Si wafer with polySi features with sizes from 1 mm to down to 140 nm. Standard Reference Material 2120 is going to be the calibrated, traceable version for line width measurements. This work is being carried out in cooperation with ISMT.

DELIVERABLES: Preparation of an assessment of feasibility of the use of mixed, NIST and external measuring systems for certification of wafer format line width samples. Accomplishment of preliminary measurements on samples made with ISMT current and new "AMAG4L" metrology masks sets.

Accomplishments

- **SEM Magnification Calibration Artifacts** – Samples for Reference Material 8090 and the certified traceable version, the Standard Reference Material 2090 are being made at two places. We have a contract with Maxim Corp. to get samples made by UV light lithography. The use of this conventional lithography and a somewhat modified design gives a chance for large amount of good quality samples inexpensively. Because of the limitations of this technology, it is impossible to produce the finest lines with 100 nm width and with 200 nm pitch values. Instead 200 nm wide lines with 400 nm pitch will be available. The features on the conductive Si wafer will be formed from polySi material. These samples will give suitable contrast in any SEM to allow the user to set the magnification of the instrument from the smallest to the highest magnifications. The other contract with the Naval Research Laboratory (NRL) is currently moving faster and already yielded close to acceptable samples. NRL makes samples with a slightly modified original process: e-beam lithography and lift-off technique with a metal stack, which gives good contrast at low and high accelerating voltage. We have a good chance to obtain a larger amount of good samples, and start the evaluation process soon. This version of the samples has the original finest structure with 100 nm wide lines at 200 nm pitch. In the meantime, the renewal of the AMRAY Metrology SEM has been successfully accomplished. A new high-precision stage with sub-nanometer stepping distance is now fully operational. The development of a LabView–based new control software has also been completed and the software has been thoroughly tested. This new measuring system offers the same functions in a PC Windows environment as the old expensive and outdated hardware under HP Basic but it also offers greater flexibility for adding new measurements (for example the SRM 484 can be measured with it) and it is up-to-date in every regard.

- **SEM Performance Measurements** – After comprehensive studies and experiments a plasma-etching Si called "grass" was chosen as a reference material 8091. This sample has 5-25 nm size structures as it is illustrated on the Figure here. 15 pieces of RM 8091 were delivered to International SEMATECH (ISMT) for the member companies, and 75 additional samples have been delivered soon to the Office of Standard Reference Materials, NIST. A sharpness standard and evaluation procedure have been developed to monitor (or compare) SEM image quality. A NIST kurtosis method, Spectel Company's user-friendly analysis system called SEM Monitor, and University of Tennessee's SMART algorithm can be used with RM 8091. An effort is underway to produce more of these samples. These samples are now available to the public.

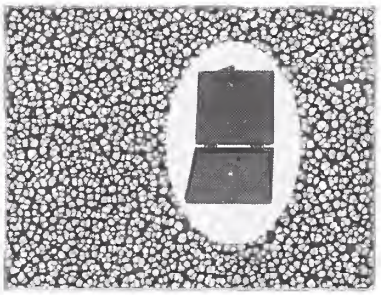

FIGURE 5. THE RM 8091 SHARPNESS REFERENCE MATERIAL

- **SEM Linewidth Measurement Artifacts** – The development of accurate modeling methods are in progress and showed excellent results on polySi samples. From a top-down view, through

our high-accuracy modeling and fitting methods; a cross section of the lines can be deduced with few nm uncertainties and discrepancies. The match is so good that this method looks to be capable of eliminating the costly and destructive cross sectional SEM measurements. The candidate sample for linewidth artifact must be relevant to state-of-the-art IC technologies, should have chips on 200 mm, later 300 mm wafers with all process variation, including a meaningful focus-exposure matrix (FEM). The design and the fabrication of ISMT/NIST mask have been successfully completed. The first 9 good quality wafers arrived at NIST just before the end of June. These wafers are currently at Accent for scatterometry measurements. After CD SEM measurements at ISMT cross sectional measurements will be made at NIST. All these measurements will yield an excellent database for a decision on how to proceed with this wafer type linewidth reference sample. It is conceivable that by the end of the year 2001 the Reference Material 8120 line width samples will be available. This work is being carried out in close cooperation with ISMT.

■ **Development of Ultra-High Resolution Nano-tip Electron Gun for CD SEMs** – The source diameter and the brightness of the electron beam are two of the major factors limiting the performance of CD SEMs in the semiconductor production environment. Thus, alternative solutions to improve performance are being sought as the metrology for sub-100 nm lithography is being pushed to its limit. One possible alternative approach is the application of nano-tips as an electron source replacement. Nano-tips, by comparison to both conventional cold field and to Schottky field emitters, offer a substantial increase in brightness (10 x to 100 x) and a large reduction (5 x to 10 x) in source size. In an optimized electron optical column therefore substitution of a CFE or Schottky source by a nano-tip could be expected to produce:

- Higher beam currents into a spot of given size.

- Better signal-to-noise ratio and resolution.

- Faster scan rate and better charge control.

This work progressed in:

- Preparation of the Hitachi S-6000 CD SEM. It has been prepared for the installation of the nano-tips. This was facilitated through the help of Hitachi Scientific Instruments. The SEM currently works to the original specifications. One sharp tip was successfully tried with good results.

- Fabrication of a nano-tip assembly, which matches in geometry the S-6000 CD SEM field emitter tip.

While the nano-tip fabrication technology (i.e. sharpening process) is working reliably, the main issue is to properly mount the prepared tip on the hairpin shaped tungsten tip holder. Several approaches were tried and for now, it is more feasible to use the hairpin part of used cathodes. As a back-up solution sharpening of existing tips was also carried out. Two new tips were delivered form NIST to Dr. David Joy's research facility (Science and Engineering Research Facility University of Tennessee, Knoxville, TN).

There have been problems with the control the etching process, so our collaborators at University of Tennessee could not make a tip to try in the CD SEM. In the meantime, a parallel effort at NIST has started in order to diversify the source of extreme sharp tips.

- Design and implementation of the SEM Sentinel Measuring System – These tasks were successfully completed. The PC-based computerized measuring system monitors the vital signs of the CD-SEM through a LabView-based set of software.

For the nano-top project, the following system components are monitored: 1) vacuum system along the column, 2) wafer handling system, and 3) diagnostic signals along the column. The system works well according to its specification.

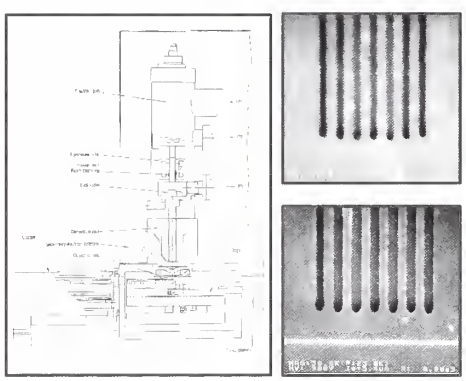

FIGURE 6. SCHEMATIC OF THE SEM SENTINEL SYSTEM (LEFT) RESOLUTION IMPROVEMENT WITH SHARP TIP (RIGHT)

DELIVERABLES: Final Report on nano-tips to ISMT.

Recent Publications

Vladar, A. E., Postek, M. T., Zhang, N–F, Larrabee R. D. and Jones, S. N., Reference Material 8091: New Scanning Electron Microscope Sharpness Standard. Proceedings of SPIE 3444; 2001 Santa Clara; pp. 827-834.

Marinenko, R. B., Steel, E. and Postek, M. T., Microscopy and Microanalysis Standards. (In press).

Vladar, A. E., Postek, M. T. and Vane R., Active Monitoring and Control of Electron Beam–Induced Contamination. Proceedings of SPIE 3444; 2001 Santa Clara; pp. 835-843.

Postek, M. T., Vladar, A. E., Larrabee, R. D. and Jones, S. N., Report of Investigation. Reference Material 8091 SEM Sharpness Standard. OSRM Publication.

Damazo, B. N., Vladar, A. E., Ling, A. V., Donmez, M. A., Postek, M. T. and Jayewardene, E. C., SEM Sentinel– SEM Performance Measurement System. Proceedings of SPIE 3444; 2001 Santa Clara; pp. 773-782.

Villarrubia, J. S., Vladar, A. E., Lowney, J. R. and Postek, M. T., Edge Determination for Polysilicon Lines on Gate Oxide. Proceedings of SPIE 3444; 2001 Santa Clara; pp. 147-156

Postek, M. T., Vladar, A. E., Wells, O. C. and Lowney, J. L., Application of the Low–Loss Scanning Electron Microscope (SEM) Image to Integrated Circuit Technology. Part 1. Applications to Accurate Dimension Measurements. SCANNING; pp. 289-304.

Wells, O. C, McGlashan–Powell, M., Vladar A. E. Postek, M. T., Application of the Low–Loss Electron Image to Quality Control During the Manufacture of Integrated Microcircuits. Part 2. Chemically–Mechanically Planarized Samples. SCANNING (in press).

Vladar, A. E. and Postek, M. T., Application of Nano–Tips to Production CD–SEMs. NIST/SEMATECH Collaboration LITG 4101 Project – SEMATECH Final Report; pp. 1-17.

Postek, M. T. and Vladar, A. E., Critical Dimension Metrology in the Scanning Electron Microscope. Chapter. Handbook of Silicon Semiconductor Metrology (Dr. Alain C. Diebold, Ed. Dekker) ISBN 0-8247-0506-8.

Optical-Based Dimensional Metrology

Goals

Provide technological leadership to semiconductor and equipment manufacturers and other government agencies by developing and evaluating the methods, tools, and artifacts needed to apply optical techniques to the metrology needs of semiconductor microlithography. One specific goal is to provide the customer with the techniques and standards needed to make traceable dimensional measurements on photomasks and wafers, where appropriate, at his or her facility. The industry focus areas of this project are primarily the optical based methods used in overlay metrology and photomask critical dimension metrology as well as the need for high-accuracy two-dimensional placement metrology.

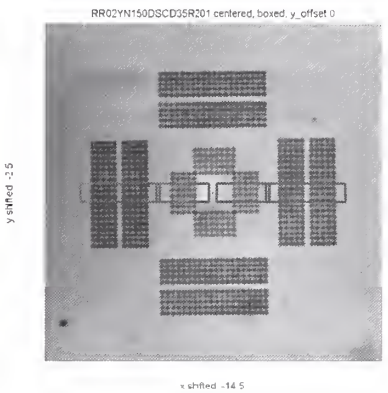

FIGURE 1. ONE OF THE NEW ADVANCED TARGET DESIGNS FROM THE NIST/ISMT COLLABORATION.

Customer Needs

Tighter tolerances on CD measurements in photomask and wafer production place increasing demands on photomask linewidth accuracy and on overlay tolerances. NIST has a comprehensive program to both support and advance the optical techniques needed to make these overlay and photomask critical dimension measurements.

In addition, improved two-dimensional measurement techniques and standards are needed for measuring and controlling overlay capabilities of steppers and mask-making tools under development. Overlay is listed in Table 38, page 145 of the 1999 SIA ITRS as a difficult challenge for both >100 nm and <100 nm processes, and states that overlay improvements have not kept pace with resolution improvements and will be inadequate for ground rules less than 100 nm. Also overlay over large field sizes will continue to be a major concern for sub-130 nm lithography. It also shows, in Table 41, pages 150-151, that two-point placement accuracy is and will be a critical issue for rules at 165 nm and less.

Technical Strategy

There are three main strategic technical components of this project. The first is the NIST overlay metrology tool, continuous development of the tool, measurement methods to obtain uncertainties comparable or better than the best industry overlay tools, and standards to support and calibrate these tools. The second component is the ultraviolet transmission microscope, calibration of NIST Photomask Linewidth Standard SRM 2059, and the development of calibration methods to obtain photomask linewidth measurement uncertainties adequate to meet industry needs. The third component is the development of two-dimensional grid calibration standards and associated measurement techniques, including statistical analysis and CCD characterization as used by industry. These individual technical strategies for these components are described in more detail next.

The technical strategy for overlay metrology is divided into two segments: 1) instrumentation development and overlay metrology methodology and 2) design and calibration of standard artifacts. Pattern placement and overlay of the various lithographic levels is monitored with a series of targets, each in a different plane. The overlay offset is then obtained by optical measurements with a determination of the relative target centerlines. Any misalignment in the overlay metrology system will translate into an artificial overlay offset, referred to as *tool induced shift* (TIS). Additionally, there are residual errors caused by asymmetries in the target edges or covering layers (resist) known as *wafer induced shift* (WIS). A set of standard artifacts and procedures, under development at NIST, is designed to assist in aligning overlay measurement systems and eliminating TIS. After alignment, the tool must then be calibrated with standard artifacts to yield accurate overlay offsets.

The measurement system used in this component is an optical reflection mode instrument, operational in either a bright field or confocal mode, with interferometry on three orthogonal axes also capable of monitoring the stage tilt. Additional hardware capabilities include the options to scan the sample while acquiring data with an on-axis photometer or high resolution

Technical Contact:
R. Silver
J. Potzick
T. Doiron

Staff-Years (FY 2001):
3.8 professional
2 contractor
1 student

Funding Sources:
STRS (94 %)
SRM (6 %)

image capture with a full field CCD data acquisition system. This latter mode has enabled a detailed study of CCD array performance and characterization. In this work, several CCD acquisition systems are being evaluated and improved edge detection and CCD

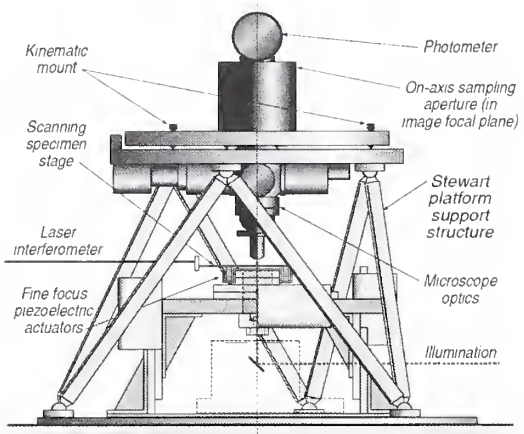

FIGURE 2. THE NIST SCANNING ULTRAVIOLET MICROSCOPE

array calibration procedures are being developed These same methods for 2-dimensional CCD array analysis are now being applied to optics analysis. Additional investigation of CCD measurement problems are focused on the detailed response of typical CCD camera light sensors.

DELIVERABLES: Update the formal qualification numbers on the overlay microscope, optics, and the *x-y* metrology stage. This is largely completed and the final uncertainties need to be tabulated. The current, most difficult challenge is the qualification for calibration of complex overlay target process levels such as contact-to-poly.

DELIVERABLES: Use the new metrology reticles from the ISMT collaboration to make leading edge overlay calibration targets/wafers. Work with Industry partners to determine designs and which levels are most appropriate for the silicon fabrication phase. Calibrate these overlay standards (both alignment and calibration) for SRM certification, 2003.

WIS-free standard overlay artifacts have been fabricated in 200 mm wafers. These overlay artifacts are for the calibration of industrial optical overlay tools. The artifacts are being fabricated in single crystal silicon and will provide an array of etched silicon three-dimensional targets with additional targets fabricated using industry standard process levels. These wafers additionally have an extensive set of characterization targets and structures developed in close collaboration with ISMT and several leading semiconductor manufacturers.

The technical strategy for photomask linewidth standards is similarly divided into two segments: (1) instrumentation and model development and (2) design and calibration of standard artifacts. An ultraviolet transmission microscope (Fig. 2) has been constructed to replace the green-light linewidth calibration system. This new instrument uses a unique geometry (a Stewart platform) as the main rigid structure and shows considerable improvement in vibration characteristics over a conventional microscope. Higher image resolution, reduced transmission of UV light through the chrome, and reduced instrument vibration will offer improved linewidth measurement uncertainties.

NIST has supplied a substantial number of photomask linewidth standards worldwide over the past decade. Chrome-on-quartz photomasks with linewidth and pitch features in the range of 0.5 µm to 30 µm have been certified on a green light optical calibration system. Linewidth uncertainties have been reduced to 40 nm. The next generation in this line of standards is SRM 2059 (Fig. 3), printed on a standard size 15.24 cm x 15.24 cm x 0.635 cm (6x6x0.25 inch standard mask) substrate with calibrated line- and spacewidths ranging from nominally 0.25 µm to 32 µm and pitch patterns from 0.5 µm to 250 µm.

In response to customers' needs for more accurate photomask feature size measurements, an industry group was formed for the improvement of mask metrology through process modeling. The features on even the highest quality masks exhibit roughness and runout at the chrome edges, compromising the definition of edge and linewidth. Modeling the effects of all of the relevant feature properties in both the mask metrology process and in wafer exposure and development processes, using existing and new software tools, can improve feature size accuracy by establishing the relationship between mask-feature metrology results and the corresponding wafer-feature sizes.

DELIVERABLES: Identify and invite appropriate companies to participate in the Neolithography task force, and have the first meeting.

DELIVERABLES: Commence circulation of the NIST linewidth standards for the BIPM international comparison.

We are approaching the problem of two-dimensional measurements from a couple of

directions. The first, and most immediate, is to develop an artifact standard which can be used to bring all of the two-dimensional based inspection instruments to the same metric. This work has developed a standard grid which will be available as a NIST Standard Reference Material, # 5001, to standardize 2D measurements in the semiconductor industry. The effort has three main parts: development of an industry consensus standard grid, measurements by state-of-the-art machines in private industry, and verification of the measurements using NIST capabilities.

Grids for the SRM have been made and final measurements are in process. Each measurement of the grid will have data in each of at least two orientations. Rotating the grid 90° between measurements samples a number of the geometric errors of the machine. The remaining geometric sources of uncertainty are the scale and some components of the linearity of each machine axis travel.

Verification of the grid measurements is being made at NIST. The overall scale of the grid is checked with the NIST linescale interferometer, an instrument that is known to provide the most accurate 1D measurements available in the world. Two sources of uncertainty not captured by these measurements include components of the straightness and effects of the plate bending when fixtured. Work is now focused on methods to characterize both of these effects. These studies provide a complete error budget for SRMs.

To strengthen the foundation of NIST's claims for linewidth measurement traceability and to support the BIPM *Mutual Recognition Arrangement*, NIST has become the pilot laboratory for an international intercomparison of submicrometer linewidth measurements. National metrology institutes in nine countries around the world are participating.

DELIVERABLES: Calculate asymmetric overlay targets images upon successful comparison for modeling results of more standard double etched silicon structures. Publish and present these results at SPIE Microlithography, 2002.

DELIVERABLES: Continue to develop comprehensive analysis capabilities for centerline and edge detection methods. This includes the implementation of automated positioning and focus mechanisms.

DELIVERABLES: Develop methods for CCD calibration and analysis. Utilize the new microgrid and 8 inch overlay wafers for calibration of optics and the CCD acquisition systems using the new self-calibration methods. Implement more advanced methods for TIS/WIS separation and present at SEMATECH member company forums.

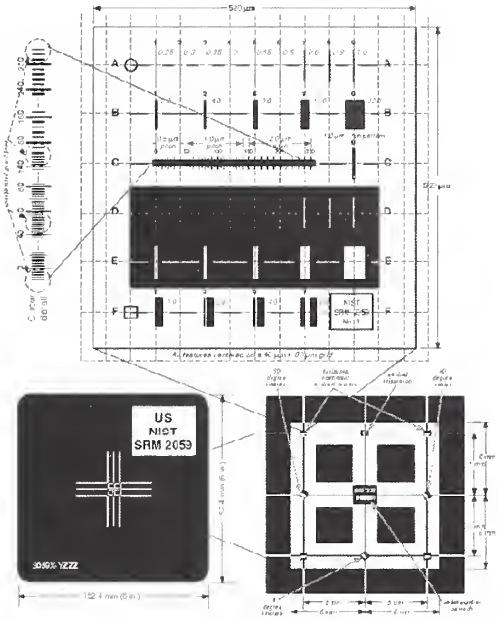

FIGURE 3. THE NEW LINEWIDTH PHOTOMASK STANDARD.

DELIVERABLES: Complete the 2-dimensional grid artifact calibrations and measurements. This is a combined industry/NIST effort using our LSI and statistical methods. Deliver the reticles to the SRM office.

DELIVERABLES: Complete calibrations of SRM 2059 and the related documentation, and deliver to the Office of Standard Reference Materials for distribution to customers.

Accomplishments

■ *SRM 2800 Microscope Magnification Standard* is a standard-size microscope slide with calibrated pitch features ranging from 1 µm to 1 cm. It contains a lithographically produced chrome pitch pattern consisting of a single array of parallel lines with calibrated center-to-center spacings. It contains no linewidth structures. This SRM is intended to be used for the calibration of reticles and scales for optical or other microscopes at the user's desired magnification. The SRM may be used in either transmission or reflection mode optical microscopes, SEMs, or SPMs. Calibration is traceable to the meter through NIST Line Scale Interferometer. Fifty-six units have been calibrated and delivered to the NIST Office of Standard Reference Materials.

- NIST is currently commencing calibration for *SRM 2059 Photomask Linewidth Standard*, intended to enable customers to make traceable measurements of the dimensions of features on integrated circuit photomasks.

- New image recognition and quantitative image analysis software has been developed by lead analyst J. Jun of Precision Engineers Division (PED). This comprehensive software package is based on the Matlab programming language and tool set and allows the evaluation of numerous effects on algorithm performance. The package has been used to quantify feature roughness and asymmetry effects on overlay pattern evaluation used in the feedback and control of lithography stepper tools. It has also been used in the quantification of algorithm robustness for sample-to-noise effects. This code has been used extensively to evaluate correlation and least-squares. A typical result is shown in Figure 4.

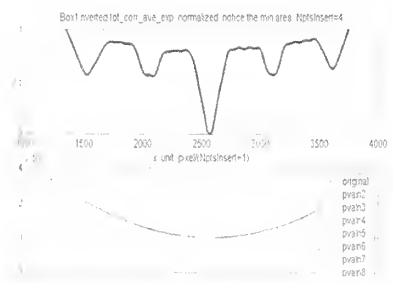

FIGURE 4. THE POTENTIAL EFFECTS IN IMPROVED TARGET RECOGNITION AND ANALYSIS ARE SEEN IN THIS IMPROVED CORRELATION CURVE AND FITTING ROUTINE.

- Two sets of overlay wafers have now been received from ISMT. These will be made available in the very near future as RM 8100 for overlay.

- The overlay metrology project is working closely with several companies such as Schlumberger and KLA Tencor to make available recent important research results on optical characterization, CCD data acquisition calibration, and focus and edge detection work. Schlumberger has shown strong interest in strengthening the collaboration with the overlay metrology project. NIST development of new correlation methods and image analysis/recognition software has enabled the detailed evaluation of noise, feature roughness, and feature inhomogeneity effects on repeatability and robustness of measurement tool performance, issues of paramount importance in semiconductor overlay metrology. We have performed a detailed, in depth study of CCD data acquisition cameras including the development of CCD mapping methods.

- The NIST Overlay Metrology project leader has played a significant role in the Overlay Metrology Advisory Group (OMAG) of ISMT. This group is developing a comprehensive set of measurement guidelines, test methods, and tool performance measures to be adopted by the semiconductor manufacturing industry. The group is made up of more than 15 international semiconductor manufacturers. The OMAG has strong interest in adopting several new methods developed in the NIST Overlay Metrology Project. In particular, the recently published methods for evaluating CCD array performance and overall optical system characterization and calibration performance measures have been adopted.

- The Overlay Metrology Group (OMAG) organized by ISMT has completed the specification document for the evaluation and benchmarking of overlay metrology tools for semiconductor manufacturing. The document will be used for procuring, testing, and matching tools.

- The first set of two-dimensional grid artifacts, is known as SRM 5001, and has been received . These 6-inch masks sets have been measured on a state-of-the-art I-pro metrology system by the photomask manufacturer. This effort, to make available traceable, 6-inch standard mask feature placement standards, involves a close collaboration between NIST and Photronics. The collaboration employs the industry tool and the traceability of the NIST line scale interferometer with appropriate statistical analysis. The uncertainty budget for grid measurements has been developed and peripheral studies on various items are near completion.

- NIST researchers have made comparisons between the E. Marx developed optical scattering code with the Spectel company Metrologia metrology modeling package. Different material systems were compared as well as one overlay feature at different focus positions. New results, based on the full integration of the NIST scattering code and Spectel optical microscope model, show very good agreement. This is an important step in the effort to provide industry the quantitative ability to determine sample-dependent effects on overlay tool performance. Results are to be presented at SPIE Microlithography, 2002.

- Near completion for the clean room enclosure on the overlay metrology tool. This will allow us to work closely with the industry and make SRMs directly transferable to a clean room environment.

- Leadership for the industry group for the improvement of mask metrology through process modeling has been transferred to ISMT.

Collaborations:

- ISMT, IBM, IVS Schlumberger, KLA-Tencor, Intel, Motorola, AMD and several other leading manufacturers or tool vendors.

- The fourteen members of The Neolithography Consortium.

Recent Publications

"Recent advances in Overlay Metrology," R. Silver, J. Jun, E. Kornegay, Future Fab, 2001.

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Meissner K., and Wegener, T., Robust Regression for Two Dimensional Coordinate Measurements, Proceedings of the International Symposium on Laser Metrology for Precision Measurement and Inspection in Industry, Florianoplis, Brazil, October 13-15, 1999.

R. Silver, T. Doiron, S. Fox, E. Kornegay, M. Takac, and S. Rathjen, Two-Dimensional Grid Standards, Proceedings of the SPIE, The International Society for Optical Engineering, Metrology, Inspection, and Process Control for Microlithography XIII (1999).

Scanning Probe Microscope-Based Dimensional Metrology

Technical Contact:
T.V. Vorburger
J.A. Dagata
R. Dixson
M.T. Postek

Staff-Years (FY 2001):
3.1 professionals
.4 Technician

Funding Sources:
STRS (88 %)
ATP (12 %)

Goals

Improve the measurement uncertainty of critical-dimension measurements in the semiconductor industry through improvements in SPM-based measurements. The International Technology Roadmap for Semiconductors identifies dimensional metrology as a key enabling technology for the development of next-generation integrated circuits. For example, the goal in 1999 for critical dimension (CD) measurement precision for isolated lines was ± 2.8 nm; this demand tightens to ± 0.8 nm by 2011. The technical focus of this project, development and implementation of scanned probe microscope instrumentation, is driven by the anticipated industry needs for reduced measurement uncertainty, particularly for existing tools such as the SEM.

Customer Needs

The SEM is the current tool of choice for inspection and metrology of sub-micrometer features in the semiconductor industry. SPMs possess unique capabilities that may significantly enhance the performance of SEMs for in-line critical dimension (CD) measurements, and are also emerging as CD measurement tools in their own right. A creative strategy, which successfully harnesses the strong points of both techniques in order to reduce the measurement uncertainty of sub-micrometer features, will help NIST meet the expectations of the semiconductor industry expressed in the current Roadmap. As is the case with SEMs, the magnification or scale of an SPM must be calibrated in order to perform accurate measurements. Although many SPMs are commercially available, appropriate calibration standards have lagged. In particular, traceable pitch/height standards with sub-micrometer pitch values are not yet available.

Technical Strategy

SPM development is proceeding along two parallel directions: The first direction addresses dimensional metrology of SPM specifically through an in-house research instrument we refer to as the calibrated atomic force microscope (C-AFM). This instrument, with metrology traceable to the wavelength of light on all three axes, is furthering the design and development of SPM standards as well as providing customers with calibrated dimensional measurements at the nanometer scale. For example, pitch, height, and width measurement capabilities of the C-AFM have been evaluated and validated by internal comparisons. Pitch, ranging up to 20 μm has been measured with standard uncertainties (1σ), as low as ≈0.5 nm at sub-micrometer scales and relative standard uncertainties of ≈0.1 % at the largest scales. Step height, ranging from a few nanometers up to several hundred nanometers, can be measured with standard uncertainties (1σ) of ≈0.1 %. The width of sub-micrometer, near-vertical features, as encountered in CD measurements, can be measured to an uncertainty (1σ) of ≈10 nm, due mostly to the finite size of the SPM tip. As part of project, we have begun to pursue research in the measurement and standardization of line edge roughness.

DELIVERABLES: By 2002, draft procedure completed for calibration of AFM z-scales with Si single atom step heights and submitted to ASME and ASTM Standards Committees.

DELIVERABLES: By 2003, report published demonstrating improved uncertainty for linewidth measurements using sharpened tips.

DELIVERABLES: By 2004, SRM 2089, a combined pitch and height standard for AFM, released.

DELIVERABLES: By 2003, reports submitted on three remaining BIPM-coordinated international Preliminary Key Comparisons in Nanometrology, step heights, 2D grids, and linewidth.

DELIVERABLES: By 2002: report published demonstrating improved performance of the C-AFM after integration of a new x-y and z stage to increase scan area and reduce motion errors.

DELIVERABLES: By 2004, report published demonstrating traceable measurements of line edge roughness using an AFM.

The second direction addresses increasingly overlapping demands for dimensional control during fabrication and subsequent calibration of nanometer scale features. For this purpose we employ an SPM-based lithography technique, pioneered at NIST, to produce grating structures with linewidths of 20 nm or below. Latent oxide patterns function as masks for anisotropic wet or dry etching. We are also developing an instrument which integrates both SPM and probe station measurement capabilities whereby we are able to compare SPM-based electrical

(capacitance and surface potential) and topographical measurements of active device structures simultaneous with traditional current-voltage (I-V) characteristics measured with a probe station. This allows us to examine local nanoscale variations at exposed and buried interfaces of critical dimensioned features in order to identify processing induced variations which contribute to linewidth uncertainty in dimensional and electrical test structures.

DELIVERABLES: Data analysis of optical and SEM images for a series of six 1-dimensional calibration prototypes produced by SPM oxidation and anisotropic etching of silicon.

DELIVERABLES: Demonstrate the use of submicrometer-pitch, 2-dimensional grids produced by SPM oxidation and anisotropic etching for controlling the spatial configuration of block co-polymer films.

DELIVERABLES: Fabricate a 2-dimensional metal-silicon grid using SPM oxidation and anisotropic etching for characterizing automated SEM grain boundary detection.

DELIVERABLES: Demonstrate a combined maskless optical and SPM lithography system for prototyping sub-100-nm pitch calibration scales integrated onto 1-cm square chips.

DELIVERABLES: Demonstrate large-scale replication of sub-100-nm pitch 1- and 2-D features using SPM lithography, anisotropic etching, and nanomprint lithography techniques.

DELIVERABLES: Fabricate functional microfluidic arrays with nanoscale features using combined maskless optical, SPM, and nanoimprint lithographies.

Accomplishments

■ The C-AFM thrust involves collaboration with industrial users and academic researchers in AFM metrology, as well as interaction with researchers in NIST's sister institutions in other nations. During FY2001 we completed traceable pitch measurements for a metrology supplier to the semiconductor industry and a issued a report. This was the fourth such test we have performed for customers in microelectronics related industries. We reported an expanded uncertainty (k=2) of approximately 0.16 %, limited by sample uniformity.

■ We are participating in a series of international Preliminary Key Comparisons in nanometrology coordinated by the BIPM (Bureau International des Poids et Mesures) CCL (Coordinating Committee for Length). Comparisons of 1D pitch, 2D pitch, step height, and linewidth measurements are being carried out. For the 1D pitch comparison, gratings having nominal pitches of 300 nm and 700 nm were measured using the C-AFM. This comparison has been completed and the pilot laboratory in Switzerland has submitted the final report to the Coordinating Committee for Length.

■ Another effort involves the study of single atomic steps as fundamental height standards in the sub-nanometer regime. Various researchers have studied silicon samples, fabricated in UHV with single atomic steps on the surfaces, and observed the preservation of the step structure after native oxidation. We have performed C-AFM measurements on such samples under a variety of measurement conditions. The theoretical value of the step height, based upon the measured lattice constant of bulk silicon, is about 313.56 pm. The C-AFM measured value is 304 pm ± 8 pm (k=2), a difference of 10 pm. Using the lattice value, the C-AFM result, and a LEED (low energy electron diffraction) result obtained by researchers at the University of Maryland, and in consultation with the NIST statisticians, we developed a recommended value for the step height of 312 pm ± 12 pm (k=2). Figure 1 shows the various results.

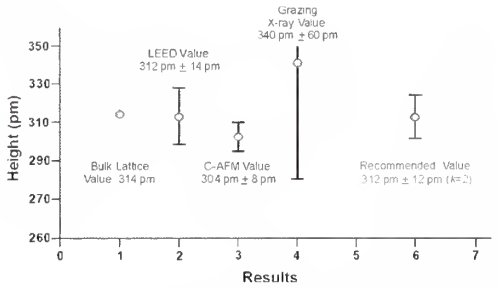


FIG. 1: ESTIMATE FOR THE SINGLE ATOM STEP HEIGHT OF SI(111) OBTAINED FROM SI BULK LATTICE GEOMETRY AND THREE EXPERIMENTAL RESULTS ALONG WITH THE RECOMMENDED VALUE OF 312 PM ± 12 PM. THE GRAZING X-RAY VALUE WAS NOT INCLUDED IN THE CALCULATION OF THE RECOMMENDED VALUE BECAUSE OF ITS RELATIVELY LARGE UNCERTAINTY.

■ We also distributed a set of silicon step samples, prepared by E. Williams, et al. at the University of Maryland, to four industrial collaborators, and completed analysis of the data received from the participants. All of the analysis was performed at NIST using the NIST algorithm for step height calculations, which is insensitive to tilt and curvature of the surface, an issue at the high magnifications required to perform subnanometer height measurements. Figure 2 shows a typical measured image obtained during

the study. A key observation following from the study is that specimens of this type, which can now be procured commercially or fabricated using published methods, can be used as z-axis calibration standards for atomic force microscopes in the sub-nanometer regime with an expanded relative uncertainty of about 6 %. These results were presented at the 2001 SPIE Microlithography Meeting and recently published. During 2002, the procedure will be proposed for standardization by national committees.

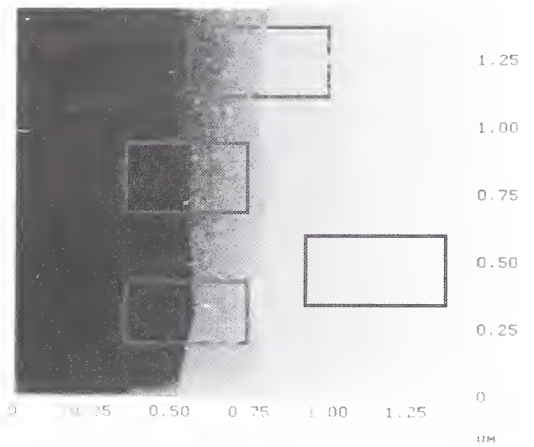


FIG. 2. TOPOGRAPHIC IMAGE OF THE SI(111) SURFACE OBTAINED WITH AFM AND SHOWING FOUR SINGLE ATOM STEPS. THE RECTANGLES INDICATE TYPICAL SUBAREAS SELECTED FOR STEP HEIGHT CALCUALTIONS. THE FIELD OF VIEW IS APPROXIMATELY 1.4 MM X 1.4 MM.

■ The C-AFM is currently being upgraded with an x,y translation stage having longer range and smaller motion errors than the previous stage and with a new sensor that combines low noise with low Abbe offset. Testing of the angular motion errors is underway.

■ Support by the NIST Office of Standard Reference Materials has enabled us to design prototypes of SRM 2089, a calibrated pitch/height specimen. Evaluation of the first set of prototypes has been completed.

■ Ronald Dixson became the first NIST assignee to International Sematech (ISMT) beginning on October 1, 2001. Ron will be concentrating on the development of an AFM there for measuring critical dimensions with close traceability to the SI unit of length. He has successfully handed off his expertise on the many aspects of the C-AFM operation to a team of three people newly assigned to the project through meetings and with a thorough document describing the procedures.

■ In the integrated SPM probe-station thrust, we have completed construction and testing of the combined instrument. Test structures consisting of silicon FETs realized on silicon-on-insulator substrates are being used as a starting point for patterning nanodevices and performing in-situ correlation of the dimensional and electrical properties of these confined regions. An example is shown in Figure 3. SPM lithography has been used interactively with electrical mapping to create successively smaller active gate regions for detailed studies of local device scaling. This capability allows us to examine local nanoscale variations at exposed and buried interfaces of critical dimensioned features in order to identify processing induced variations which contribute to linewidth certainty.

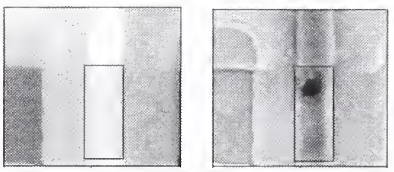


FIG. 3: SPM TOPOGRAPHICAL (LEFT) AND SURFACE POTENTIAL (RIGHT) IMAGE MAPS OF THE 2 µM X 0.5 µM X 7 NM GATE REGION OF A SOI TUNNEL TRANSISTOR, SHOWN WITH AN OUTLINE IN THE FIGURES. P^{++}-SI SOURCE AND DRAIN ARE THE BRIGHT AREAS ABOVE AND BELOW THE GATE, WHICH IS ALSO P^{++}-SI. THE DEVICE FUNCTIONS BY BACKGATING VIA THE SUBSTRATE. ALTHOUGH THE TOPOGRAPHY OF THE GATE STRUCTURE IS HIGHLY UNIFORM, LOCOS THINNING OF THE GATE REGION LEADS TO PARTIALLY DEPLETED DEFECT REGIONS NEAR THE SOURCE AND DRAIN.

■ We have also demonstrated large-scale (100 µm × 100 µm) patterning of 35 nm linewidth SPM oxide features on 110-oriented silicon substrates, as shown in Figure 4. These patterns can be developed by potassium hydroxide or trimethyl ammonium hydroxide etching to form densely packed gratings that can be several hundred nanometers in height. Processing control during the lithographic patterning and etching steps to routinely produce calibration-grating structures is now being optimized and SEM inspection of these structures is anticipated shortly.

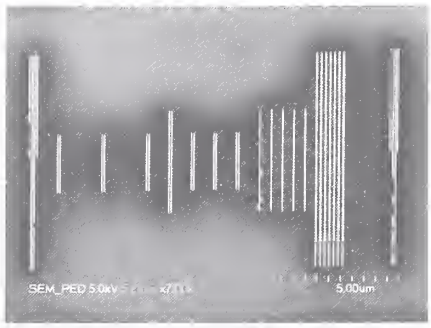


FIG. 4. SEM MICROGRAPH OF AN ANISOTROPICALLY ETCHED SPM OXIDE CALIBRATION PROTOTYPE PRODUCED ON A SI(110) SUBSTRATE. THE TWO OUTER BARS CONSIST OF LINES WITH 100 NM NOMINAL PITCH.

Recent Publications

R. Dixson, N. G. Orji, J. Fu, V. Tsai, E. D. Williams, R. Kacker, T. Vorburger, H. Edwards, D. Cook, P. West, and R. Nyffenegger, "Silicon single atom steps as AFM height standards," *Proc. SPIE* 4344 p. 157 (2001).

R. Köning, "The Role of Periodic Inerferometer Errors in the Calibration of Capacitance Displacement Sensors for Nanometrology Applications," Meas. Sci. and Technol. (in press).

T.V. Vorburger, R.H. Allen, B. Damazo, J. Fu, D. Monk, M. Osti, J. Pellegrino, R. Rhorer, R. Russell, R. Silver, R. Sriram, K. Stouffer, D.A. Swyt, E.C. Teague, T. Wheatley, D. Wilmering, "Nanomanufacturing of Atom-based Dimensional Standards, a Final Report of the National Advanced Manufacturing Testbed" (in review).

F. S. S. Chien, J. A. Dagata, W-f. Hsieh, and S. Gwo, "Nanomachining of Si with Si3N4 masks patterned by scanning probe microscopy," *5th Conference of Nanoengineering and Microsystem Technology*, ITRI, Hsinchu Taiwan, November 2001.

J. A. Dagata, "Electric force microscopy with a single carbon nanotube tip," ***Proc. SPIE*** 4344, p. 58 (2001).

J. A. Dagata, F. Perez-Murano, G. Abadal, K. Morimoto, T. Inoue, J. Itoh, and H. Yokoyama, "Predictive model for scanned probe oxidation kinetics," *Appl. Phys. Lett.* **76**: 2710 (2000).

K. Morimoto, F. Perez-Murano, and J. A. Dagata, "Density variations in scanned probe oxidation," *Appl. Surf. Sci.* 158: 205 (2000) .

K. Matsumoto, Y. Gotoh, T. Maeda, J. A. Dagata, and J. S. Harris, "Room-temperature single-electron memory made by pulse-mode atomic force microscopy nano oxidation process on atomically flat alumina substrate," *Appl. Phys. Lett.* 76: 239 (2000).

Linewidth and Overlay Standards for Nanometer Metrology

Technical Contact:
Michael W. Cresswell

Staff-Years (FY 2001):
3 professionals
1 technician
1 guest researcher
1 student

Funding Sources:
STRS (100 %)

Goals

Develop test-structure-based electrical metrology methods and related reference materials with primary emphasis on linewidth metrology and calibration and overlay; contribute to standards organizations supporting the development of metrology standards for the semiconductor tool industry.

CHRISTINE MURABITO USING HOT PLATE TO DO A POST-EXPOSURE BAKE DURING THE PHOTO-LITHOGRAPHY PROCESS.

Customer Needs

The Semiconductor Industry Association's (SIA) International Technology Roadmap for Semiconductors (ITRS) states that it is critically important to have suitable reference materials for lithography support available when on-wafer measurements are made as a new technology generation in integrated circuit (IC) manufacturing is introduced, and particularly during development of advanced materials and process tools. Each generation of ICs is characterized by the transistor gate length whose control to specifications during IC fabrication is a primary determinant of manufacturing success. The SIA projects the decrease of gate linewidths used in state-of-the-art IC manufacturing from present levels of up to 250 nm to below 70 nm within several years. Scanning electron microscopes (SEMs) and other systems used for traditional linewidth metrology exhibit measurement uncertainties exceeding ITRS-specified tolerances for these applications. It is widely believed that these uncertainties can be at least partially managed through the use of reference materials with linewidths traceable to nanometer-level uncertainties. Until now, such reference materials have been unavailable because the technology needed for their fabrication and certification has not been available. It is also widely believed that the usefulness of SEM metrology for monitoring wafers in advanced development and production will become inadequate at some future IC generation. Thus, there exists a need for new methodology to meet future metrology requirements.

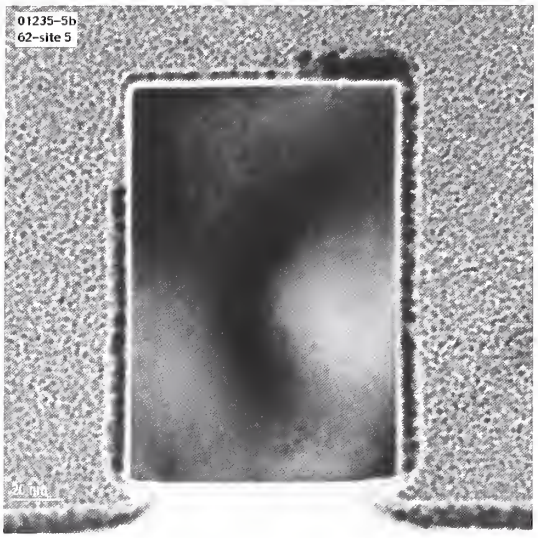
Technical Strategy

The technical strategy that the project staff have developed for fabricating linewidth and overlay reference materials is known as the Single-Crystal CD (critical dimension) Reference-Material implementation. Patterning with lattice-plane selective etches of the kind used in silicon micro-machining provides reference features with atomically planar sidewalls. Essential elements of the technology are the starting silicon wafers having a (110) orientation; the reference features, which must be aligned to specific lattice vectors; and the lithographic patterning with lattice-plane selective etches of the kind used in silicon micro-machining.

The traceability path for dimensional certification is provided by High-Resolution Transmission Electron Microscopy (HRTEM) imaging. This method provides nanometer-level accuracy, but is sample-destructive and prohibitively costly to implement. This project's unique traceability strategy thus features the sub-nanometer repeatability of electrical CD metrology as a secondary reference means. Low-cost, whole-wafer electrical measurements are effectively calibrated with a few local HRTEM lattice-plane image counts. Typical reference features are several-hundred lattice planes wide. HRTEM lattice-plane image counts, achieved by automated analysis of phase-contrast images, were developed in order to minimize the uncertainties of the linewidths of the standards.

The technical strategy has to be responsive to industry's requirement for reference materials to have the physical properties of standard 200 mm wafers. This project's technical strategy has been to dice each 150 mm wafer and mount the separate chips in micro-machined standard 200 mm wafers to accommodate the test chips. The result is that finished units are user-friendly at an

acceptable cost. The entire fabrication and certification process is planned to be transferred to a commercial standards vendor.



LOW MAGNIFICATION TRANSMISSION-ELECTRON MICROGRAPH OF THE COMPLETE CROSS-SECTION OF A FEATURE, HAVING A MEASURED ECD OF 73 NM.

In the past year, project researchers have delivered prototype CD reference materials for calibrating linewidth metrology instruments used in manufacturing semiconductor devices to International SEMATECH (ISMT) for evaluation by member companies. The work was the result of collaborations with ISMT, VLSI Technology Inc., and Sandia National Laboratories as well as collaborations with the NIST Information Technology Laboratory's (ITL's) Statistical Engineering Division and Mathematical and Computational Sciences Division, the NIST Manfacturing Engineering Laboratory's (MEL's) Precision Engineering Division, and the NIST Materials Science and Engineering Laboratory's (MSEL's) Metallurgy Division to fabricate, test, and evaluate this new class of reference artifacts to meet the ITRS goals. The technical approach was to design the reference features into electrical test structures, thus enabling the determination of their electrical linewidth. A selection of (36) test structures was incorporated into the test chip that was patterned in the device layer of (110) silicon-on-insulator (SOI) wafers based on well-established silicon micro-machining technology that produced feature sidewalls having near-atomic planarity. Primary calibration of the CD of the test-structures on all the test chips was accomplished by means of high cost, low speed HRTEM imaging and lattice-plane counting at a limited number of sites on the wafer. HRTEM provides nanometer-level accuracy, but is sample-destructive and prohibitively costly to implement on all reference features. The samples delivered to ISMT were calibrated via a statistical correlation with their high-precision electrical CD (ECD) measurement.

DELIVERABLES: Design improved Single-Crystal Silicon-on-Insulator and bulk Reference Materials, procure photomasks, and deliver to ISMT contractors for sample fabrication.

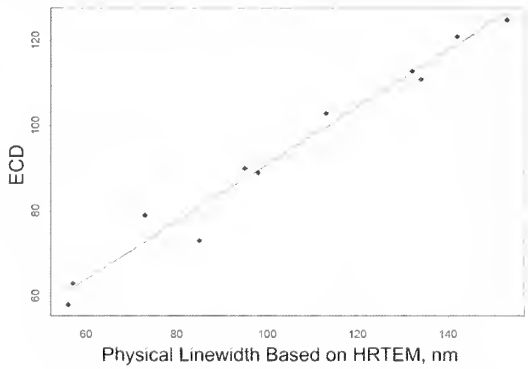
DELIVERABLES: Complete electrical measurements on Single-Crystal Silicon-on-Insulator and bulk Reference Materials, obtain HRTEM measurements, and produce transfer calibration data.

DELIVERABLES: Deliver up to 15 improved Single-Crystal Silicon-on-Insulator and/or bulk Reference Materials to ISMT mounted in carriers supplied by ISMT contractor.

Accomplishments

- For the first time, CD-reference features have been designed, built, and tested on bulk (110) wafers using junction isolation to isolate the test feature from the bulk wafer. Samples with measured linewidths below 180 nm were evaluated with no adverse leakages from feature to bulk observed. Junction isolated reference materials offer lower initial material costs, simplicity in processing, and possible lower calibration uncertainties.

- Based on a NIST patent entitled "Test Chip Reference-Artifact Carrier," a commercial standards supplier has completed work on the development of pocket wafers and has transferred the carrier wafers process to their manufacturing group for product development.



DATA RELATING ECD TO PHYSICAL LINEWIDTH WITH CALIBRATION FUNCTION.

- We have delivered prototype CD reference materials, RM-8110, for calibrating linewidth metrology instruments used in manufacturing semiconductor devices to ISMT for evaluation by

member companies. Finished CD reference materials were mounted in 200 mm pocket wafers. These materials respond to a need identified by the SIA ITRS that states that it is critically important to have suitable reference materials to support the development of advanced lithography tools and processes.

- The IC Technology Group, in collaboration with the National Research Center of Finland (VTT) and the George Washington University, has demonstrated the feasibility of a novel non-contact capacitive-sensor metrology tool developed for chrome photomasks. The sensor is intended for use as an independent metrology tool for mask makers and mask users. The linewidth metrology sensor, developed using a Low Temperature Co-Fired Ceramic (LTCC) technology, is based on non-contact micro-capacitance measurements of features located on chrome-on-glass reticles. Initial results indicate that the non-contact capacitive sensor is capable of extracting chrome-feature linewidths in the range of 0.4 µm to 0.5 µm.

- In collaboration with the Precision Engineering Division (PED), the Semiconductor Electronics Division is developing stage micrometers, with the goal of providing them to industry as NIST SRMs. Stage micrometers are used extensively for calibration of optical microscopes; however, unless they have been individually calibrated by NIST, currently a slow and expensive process, they do not provide a traceable calibration. By combining fast and inexpensive electrical test structure metrology with NIST-traceable measurements on PED's Linescale Interferometer, NIST will be able to make calibrated stage micrometers widely available at a reasonable cost. The initial designs are completed and test samples are expected early in FY 2002.

- In collaboration with ITL's Mathematical and Computational Sciences Division, an initial machine-counting procedure for improving the determination of the number of lattice planes as determined from HRTEM images was developed. The overall emphasis is to reduce the analysis time and to improve the overall linewidth uncertainty.

- A decontamination process using oxygen plasma was developed for cleaning CD reference materials mounted in 200 mm carrier wafers. The procedure successfully removed the contamination bulges caused by hydrocarbon contamination when the material is inspected by a SEM. A 35-minute oxygen plasma etch removed the bulges, removed the rectangular cloud, and decreased the size of the circular defects on a test structure reference segment and surrounding area. This hydrocarbon contamination cleaning process was applied on a reference segment with a specified exact width on a chip supplied to an ISMT company that had been contaminated by a SEM.

FY Outputs

Collaborations

- ISMT and ISMT member companies (AMD, Compaq, Conexant, Hewlett-Packard, IBM, Intel, Lucent Technologies, Motorola, Texas Instruments, Hyundai, Infineon Technologies, Philips, STMicroelectronics, TSMC), April 30, 2001 delivery of prototype CD reference materials, to meet ISMT MDL (Michael W. Cresswell and Richard A. Allen)

- ISMT, development of single-crystal CD reference materials (Michael W. Cresswell and Richard A. Allen)

- Photronics, development of optical/electrical hybrid critical dimension measurement for photomasks (Richard A. Allen and Michael W. Cresswell)

- Polymers, Sharon Kennedy, consultation to discuss design tools available for a simple geometry project (Colleen H. Ellenwood)

- Precision Engineering Division, Bill Penzes, collaboration on test structure NIST40 design (Colleen H. Ellenwood and Michael W. Cresswell)

- Precision Engineering Division, Bill Penzes, development of electrically calibratable stage micrometer (Richard A. Allen)

- Process Measurements Division, Michael Carrier, consultation regarding how L-Edit works and some advanced ideas to gain efficiency (Colleen H. Ellenwood)

- Process Measurements Division, Michael Carrier, made plots and reviewed new chip (Colleen H. Ellenwood)

- Process Measurements Division, Michael Carrier, reviewed chip designed by M. Carrier (Colleen H. Ellenwood)

- Sandia National Laboratories Microelectronics Development Laboratory, Sandia National Laboratories Compound Semiconductor Research Laboratory, Sandia National Laboratories Inte-

grated Materials Research Laboratory, NIST ITL, MSEL, MEL, and ISMT on fabrication and certification of reference materials for linewidth and overlay metrology (Michael W. Cresswell, Loren W. Linholm, and Richard A. Allen)

- Sandia National Labs, Statistical Engineering Division, Metallurgy Division, University of Central Florida, and Precision Engineering Division, ISMT reference artifacts for CD measurements (Michael W. Cresswell, Loren W. Linholm, and Richard A. Allen)

- Scientific Computing Division, Hai Tang, assistance with ANSYS model of single crystal CD reference material project (Colleen H. Ellenwood)

- Simplex Solutions, Inc., LSI Logic, and Chartered Semiconductor, procedures and algorithms for CD extraction from test features having conformal coatings (Michael W. Cresswell)

- University of Edinburgh, U.K., and ISMT, process development for single-crystal CD reference materials (Michael W. Cresswell, Loren W. Linholm, and Richard A. Allen)

- VLSI Standards, development of single-crystal CD and overlay reference materials (Michael W. Cresswell and Richard A. Allen)

- VLSI Standards, Inc., and ISMT, development of commercial architecture and distribution plan for single-crystal CD reference materials (Michael W. Cresswell and Richard A. Allen)

Standards Committee Participation

- SEMI International Standards Electrical Metrology Test Structures Task Force, Co-Chair (SEMI Doc 2860 balloted, winter 2000) (Richard A. Allen)

- SEMI International Standards Microlithography Committee, member (Richard A. Allen)

External Recognition

- Certificate of Appreciation for SEMI standards leadership activities (Richard A. Allen)

- Elected IEEE Fellow (Michael W. Cresswell)

Recent Publications

Allen, R. A., Headley, T. J., Everist, S. C., Ghoshtagore, R. N., Cresswell, M. W., and Linholm, L. W., High-Resolution Transmission Electron Microscopy Calibration of Critical Dimension Reference Materials, IEEE Transaction on Semiconductor Manufacturing, vol. 14, no. 1, pp. 26-31, 2001.

Cresswell, M. W., and Allen, R. A., Electrical CD Metrology and Related Reference Materials, in Handbook of Silicon Semiconductors Metrology, A. C. Diebold, Ed. (Marcel Dekker, Inc., New York - Basel, 2001), pp. 377-409.

Cresswell, M. W., Arora, N., Allen, R. A., Murabito, C. E., Richter, C. A., Gupta, A., Linholm, L. W., Pachura, D., and Bendix, P., Test Chip for Electrical Linewidth of Copper-Interconnection Features and Related Parameters, Proceedings of the 2001 IEEE International Conference on Microelectronic Test Structures, Kobe, Japan, March 19-22, 2001, vol. 14, pp. 183-188.

Guillaume, N., Kiihamaki, J., Karttunen, J., and Kattelus, H., Use of Electrical Test Structures to Characterize Trench Profiles Etched on SOI Wafers, Proc. IEEE 2001 Int. Conference on Microelectronic Test Structures, vol. 14., March 2001, pp. 159-164.

Penzes, W. B., Allen, R. A., Cresswell, M. W., Linholm, L. W., and Teague, E. C., A New Method to Measure the Distance Between Graduation Lines on Graduate Scales, IEEE Transactions on Instrumentation and Measurement, vol. 49, no. 6, December 2000, pp. 1285-1288.

Model-Based Linewidth Metrology

Technical Contact:
John Villarrubia

Staff-Years (FY 2001):
1.5 professional

Funding Sources:
STRS (74 %)
Other Agency (26 %)

Goals

The goal of this project is to address the metrology needs of industry, particularly the U.S. semiconductor industry, for linewidth metrology with uncertainties of a few nanometers.

Customer Needs

"Physical metrology is challenged by the advancement of lithography capabilities and is not meeting required improvement for precision and reproducibility. Mask and wafer CD metrology tool resolution, accuracy, tool- to-tool matching, and reproducibility all require significant advancement if they are to meet the accelerating timing of the industry needs. Additionally, metrologists must learn how to effectively extract three-dimensional data from CD and overlay measurements to provide the maximum level of process control." International Technology Roadmap for Semiconductors, p. 300 (1999).

"CD measurements must account for sidewall shape." International Technology Roadmap for Semiconductors, Table 81, "Metrology Difficult Challenges," p. 297 (1999).

"Under these assumptions, the value of CD control for the 180 nm generation of microprocessors exceeds $10 per nanometer." C.P. Ausschnitt and M. E. Lagus, IBM Advanced Semiconductor Technology Center, Proc. SPIE Vol. 3332, p. 212 (1998).

A feature's width is one of its fundamental dimensional characteristics. Width measurement is important in a number of industries including the semiconductor electronics industry, which had more than $200 billion in worldwide sales in 2000.[1] As a measure of its importance in that industry, consider that the term "critical dimension" or "CD" is used there nearly interchangeably with "linewidth," and semiconductor device generations are known according to the characteristic width of the features, as in "the 130 nm generation."

It is part of NIST's mission to provide standard reference materials and/or calibration services to meet the needs of U.S. industry. Presently, our only linewidth standards are optical photo-mask standards, the minimum linewidth of which is 0.5 µm with a combined expanded uncertainty of ≈37 nm (coverage factor 2). To support present and future semiconductor technologies, industry needs to measure sub-micrometer lines with total uncertainties, as identified by International SEMATECH, of better than 10 nm and with measurement repeatabilities better than 2 nm. The magnetic recording and photographic industries have gap width and grain size measurement requirements at approximately the same scale. Neither NIST nor other national laboratories presently offer a linewidth measurement service or SRM with this level of accuracy.

A line's width must generally be determined from its image. However, the image is not an exact replica of the line. The scanning electron microscope (SEM), scanning probe microscope (SPM), and optical microscope all have image artifacts that are important at the relevant size scales. Physical linewidth determination therefore requires modeling of the probe/sample interaction in order to correct image artifacts and identify edge locations. Barriers to accurate linewidth determination include inadequate confidence in existing models, the complexity and consequent expense of using some models, inadequately quantified methods of divergence, and ignorance of best measurement practices.

Technical Strategy

The scope of the model-based linewidth metrology project includes the development and improvement of computational models to simulate the artifacts introduced by measuring instruments, inversion of these models (to the extent possible) to deduce the sample geometry that produced a measured image, validation of models by appropriate experiments, development and testing of measurement processes that provide the necessary inputs for model-based deduction of sample width and shape, estimation of uncertainties for the measurement process, assistance to industry linewidth measurement by communication of best practices, and laying of the necessary research groundwork for a future linewidth and/or line shape Standard Reference Material.

NIST is uniquely positioned to execute such a project. NIST is a center of expertise in the instrument models to be tested, with the optical,

[1] Semiconductor Industry Association press release, Feb. 5, 2001.

SEM Monte Carlo, and SPM tip and sample

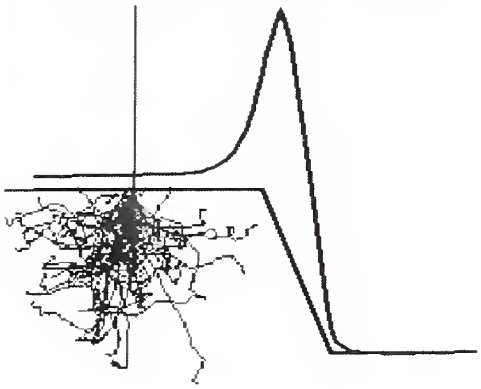


FIG. 1. THE SEM IMAGE MAY BE CALCULATED FOR A GIVEN EDGE GEOMETRY BY USING A MONTE CARLO ALGORITHM THAT FOLLOWS A NUMBER OF REPRESENTATIVE ELECTRON TRAJECTORIES.

reconstruction models all having been developed at NIST. Also, because NIST's standards function necessitates concern for accuracy, the NIST measurement tools are among the best characterized anywhere. For example, transmission optical measurements can be made here with the same instrument used to calibrate SRMs, and scale calibrations can be assisted by the NIST linescale interferometer.

We have been developing a model-based library method of determining line width and line shape from top-down SEM images. The top-down measurement configuration is the one employed by industry CD-SEMs. Edge locations tell us the line's width (the "CD" desired by industry). However, lines with different sidewall geometries appear to have different widths when measured using algorithms that are standard today on CD-SEMs. That is, sidewall variation masquerades as width variation. Accordingly, our method is a model-based algorithm that explicitly accounts for the physics of the interaction of the electron beam with the sample and the effect of sidewall geometry.

The method works like this: A set of parameters with which to describe edge geometry, for example sidewall angle and corner radius, are chosen. For a given set of values of these parameters, the expected image is calculated using a Monte Carlo algorithm that simulates electron trajectories (Fig. 1). This calculation is repeated for other choices of edge parameters at discrete intervals representative of the range of shapes that one is likely to encounter in a measurement. The resulting actual shape / calculated image pairs form a library, or database. To determine the shape of an unknown sample, its measured image is compared to computed images in the database to find the closest match. The corresponding line shape is assigned to the unknown (Fig. 2). In practice, only individual edge shapes (not entire line shapes as shown in the figure) need be modeled, there may be more than two parameters, and the library may be interpolated.

In fiscal year 2001 this new method produced encouraging results for data taken with our laboratory SEM. In the first part of fiscal 2002, we will be reporting on these results.

DELIVERABLES: Final report to International SEMATECH on development and testing of the shape-sensitive linewidth metrology system.

DELIVERABLES: Report results of development and testing of shape-sensitive linewidth metrology system at SPIE Metrology, Inspection, and Process Control Conference.

In the rest of fiscal year 2002 we will be attempting to implement and validate the method on an industrial CD-SEM. The method has not yet been validated on such instruments, which differ from our laboratory instrument in depth of focus and extraction fields.

DELIVERABLES: Results of model-based shape-sensitive linewidth measurement system using data from an industrial CD-SEM will be compared to independent measurements of line width and shape.

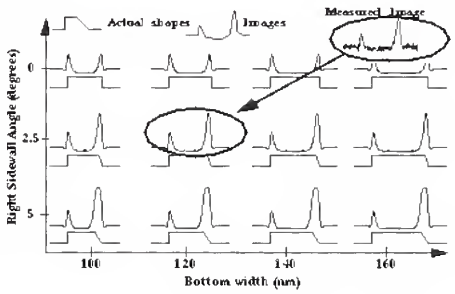


FIG. 2. CONCEPT OF METROLOGY USING A MODEL-BASED LIBRARY. THE MEASURED IMAGE IS COMPARED TO A LIBRARY OF IMAGES CALCULATED FOR A RANGE OF POSSIBLE LINE SHAPES USING A PHYSICS-BASED MODEL OF THE MEASURING INSTRUMENT. THE SHAPE OF THE UNKNOWN STRUCTURE THAT GAVE RISE TO THE MEASURED IMAGE IS ASSIGNED TO BE THE LINE SHAPE CORRESPONDING TO THE IMAGE THAT MOST CLOSELY MATCHES THE MEASURED ONE.

Results of this comparison may indicate the need for some changes in the instrument model to accommodate the CD-SEM's differences. Once these changes are implemented, the code may (if they so desire) be installed at International SEMATECH.

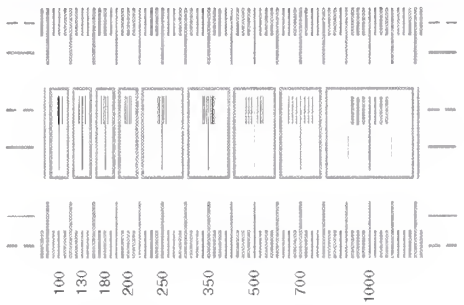


FIG. 3. DESIGN OF NEW LINEWIDTH TEST PATTERN. THE DESIGN CONTAINS BOTH NESTED LINES AND ISOLATED LINES WITH NOMINAL WIDTHS VARYING FROM 100 NM TO 1 μM. THE SIDE-BY-SIDE ARRANGEMENT PERMITS LINES OF ALL SIZES TO BE CROSS SECTIONED WITH THE SAME CUT OR CLEAVE. SCALE PATTERNS ABOVE AND BELOW THE LINEWIDTH PATTERNS ARE MEASURABLE WITH THE NIST LINESCALE INTERFEROMETER TO PROVIDE A TRACEABILITY PATH.

DELIVERABLES: Stand-alone software to perform off-line model-based shape-sensitive linewidth analysis will be installed at International SEMATECH.

Such stand-alone software may help interested industrial laboratories to assess the usefulness of this method in an industrial environment. In the long run, however, if the method proves to be useful the most effective transfer mechanism will be to have this method of data analysis become incorporated into the CD-SEM instrument itself by instrument vendors. To that end, the initial NIST role will be to publicize to vendors and their potential customers the performance, both strengths and weaknesses, of this method.

DELIVERABLES: The performance of model-based shape-sensitive linewidth method using data from an industrial CD-SEM will be assessed and reported.

Accomplishments

- We reported results from our previous year's study to ISMT directly (in the form of a project report that is accessible to member companies via the web). We reported these results, to the semiconductor metrology community and public generally via oral presentation at the SPIE Micrometrology Symposium and publication in the symposium proceedings. These were results from a precursor of the present model-based library technique applied to polycrystalline silicon lines.

- We developed and implemented a number of improvements in the model-based library method for analyzing SEM data and embodied them in software. Improvements include the ability to perform the required non-linear least squares matching of measured results to library results for an arbitrary number of line scans, each containing an arbitrary number of line features in a single fitting operation, separate treatment of instrument parameters (brightness, contrast, and beam size), and the ability to pin parameters that are independently known.

- In collaboration with International SEMATECH, we designed and fabricated a new linewidth test pattern (Fig. 3).

- We employed the new analysis method to obtain linewidth and line shape information from top-down SEM images acquired with our laboratory SEM. We compared these results to cross-sectional images of the same lines (Fig. 4).

- The repeatability of the new method was compared to that of one of the standard algorithms employed in industry CD-SEMs. The two methods were used to analyze the same data set. The new method was more than a factor of three better.

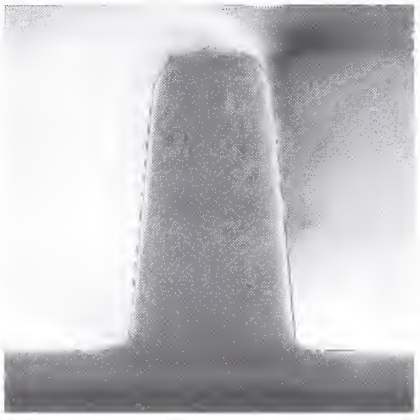


FIG. 4. CROSS SECTION (CONTINUOUS LINE) DEDUCED BY MODEL-BASED METHOD OVERLAID ON CROSS-SECTIONAL SEM IMAGE OF A NOMINALLY 200 NM WIDE LINE. AGREEMENT FOR THE UPPER CORNER RADII IS POOR. HOWEVER, SIDEWALL ANGLES ARE WITHIN A FEW TENTHS OF A DEGREE OF AGREEMENT, AND WIDTHS AT HALF THE LINE HEIGHT AGREE TO BETTER THAN THE UNCERTAINTY ASSOCIATED WITH THE CROSS SECTION IMAGE.

Recent Publications

"Nanoindentation of Polymers: An Overview," Mark R. VanLandingham, John S. Villarrubia, William F. Guthrie, Greg F. Meyers, in Macromol. Symp. 167: "Recent Advances in Scanning Probe Microscopy of Polymers," V. V. Tsukruk and N. D. Spencer, eds., pp. 15-44 (2001).

"Shape-Sensitive Linewidth Measurement with the SEM Using a Model-Based Library," J. S. Villarrubia, A. E. Vladár, J. R. Lowney and M. T. Postek, SCANNING **23**(2), pp. 90-91 (2001).

"Linewidth Intercomparison on a PolySilicon Sample," International SEMATECH member company web site.

"Edge Determination for Polysilicon Lines on Gate Oxide," J. S. Villarrubia, A. E. Vladár, J. R. Lowney and M. T. Postek, Proc. SPIE **4344**, pp. 147-156, (2001).

Thin Film and Shallow Junction Metrology Program

The dimensions of the active transistor areas are approaching the spacing between dopant atoms, the stochastic regime, complicating both modeling and doping gradient measurements. Thin dielectric and conducting films are approaching monolayer thicknesses.

As device dimensions continue to shrink, junctions and critical film thickness approach the realm of several atoms thick, challenging gradient, thickness and roughness metrology as well as electrical and reliability characteristics. The gate dielectric, traditionally SiO_2, is no longer viable for the most advanced structures. Nitrided SiO_2 of various forms is being introduced widely, and more complex dielectric structures incorporating metals such as hafnium, zirconium and aluminum are being explored. The overall task is to provide suitable metrology and reference materials for thin dielectrics and conducting barrier films, including electrical characterization, gradient, thickness and roughness metrology , and overall reliability metrology.

Two- and Three-Dimensional Dopant Profiling

Goals

To provide industry with the metrology infrastructure needed to measure two- and three-dimensional dopant/carrier profiles in the ultra-shallow junction regime. The project is divided into two thrusts (SIMS and SCM):

1) Improve the capabilities for compositional depth-profiling by defining optimum procedures for ultra-high depth resolution by Secondary Ion Mass Spectrometry (SIMS), develop depth-profiling reference materials needed by U.S. industry, and decrease the uncertainty of implant dose measurements by SIMS.

2) Provide measurement methodologies, theoretical models, and data interpretation software necessary to make the Scanning Capacitance Microscope (SCM) a useful two-dimensional dopant-profiling tool.

Customer Needs

The 1999 SIA ITRS discusses the need for improved SIMS capabilities and development of two- and three-dimensional profiling techniques for measurements of ultrashallow dopant profiles and offline doping process control. Under Front End Processes, the need for thin-film reference materials is delineated, and, under Metrology, the increasing precision requirements for dopant concentration measurements are indicated. The ITRS specifies requirements for at-line dopant profile concentration measurements improving from a spatial resolution of 2 nm and precision of 4 % in 2002 to 0.6 nm and 2 % by 2015. These values are to be accomplished with "low systematic error."

SIMS is most likely to provide the solution to precision requirements for dopant concentration measurements. These goals can be achieved by careful control of SIMS depth-profiling conditions and by developing and making available implant reference materials for common dopant elements. Scanning Capacitance Microscopy (SCM) has emerged as a leading contender to provide 2-D carrier profiles. Relatively accurate two-dimensional profiles of the dopant concentration can be obtained when SCM images are combined with SIMS measurements.

Technical Strategy

DELIVERABLES: Develop experimental protocols for high repeatability analysis of As and P implants in silicon.

Secondary ion mass spectrometry (SIMS) has demonstrated the capability to meet the ITRS dopant profiling requirements for B, As, and P. However, the detailed analytical protocols required to achieve these goals have not been completely specified. We are working in a collaboration with Agere Systems to investigate the parameters that must be controlled to make highly repeatable dose measurements of As and P implants in Si with magnetic sector SIMS instruments.

DELIVERABLES: Evaluate Time-of- Flight (TOF) SIMS for ultrashallow depth-profiling of boron delta doped structures and thin oxide films.

TOF-SIMS depth-profiling is potentially a useful approach for dopant profiling that combines both high spatial and depth resolution. TOF-SIMS depth profiles are performed with two temporally interlaced ion beams. One beam is used for analysis (i.e., generating ions to be accepted into the mass spectrometer) and the other beam is used to remove material (often referred to as the "sputter beam"). This method of depth-profiling is often referred to as "dual-beam depth-profiling." We have conducted a systematic investigation of the instrumental conditions that affect depth resolution in dual beam TOF-SIMS depth-profiling and applied these procedures to the analysis of thin oxide films and delta doped structures.

DELIVERABLES: Evaluate methods for reduction of sputter-induced topography in Cu (and other metal films).

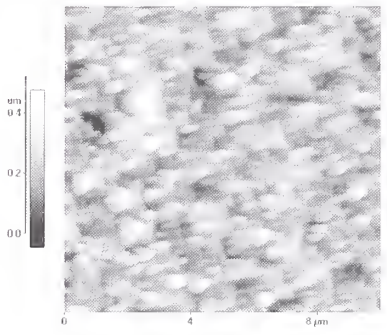
There is considerable recent interest in the use of copper in integrated circuits due to its low resistivity and good electron migration resistance characteristics. With these properties, copper is a good candidate to substitute for aluminum as the interconnection material in the next generation of integrated circuits. However, SIMS depth-profiling of metallic films induces surface topography, which can result in a significant loss of depth resolution. This loss of depth resolution can limit our ability to characterize copper diffusion through metal barrier films and can also make quantification of impurities and intentional additives in copper film problematic. Possible

Technical Contact:
Greg Gillen (SIMS)
David Simons (SIMS)
Joseph Kopanski (SCM)
Jay Marchiando (SCM)

Staff-Years (FY 2001):
5.5 professional

Funding Sources:
STRS (100 %)

methods to reduce sample roughness include using a very low energy primary ion beam at a glancing angle, rotating the sample stage during depth-profiling or using a polyatomic primary ion beam. We are exploring each of these methods in order to determine optimal experimental conditions for depth-profiling of metal films.



ATOMIC FORCE MICROSCOPE IMAGE OF SPUTTER-INDUCED TOPOGRAPHY IN A CR/NI METAL FILM AFTER SIMS ANALYSIS WITH A 7.5 KEV O_2^+ PRIMARY ION BEAM.

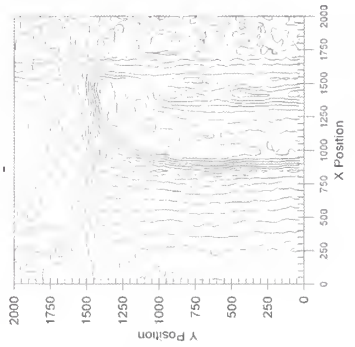
DELIVERABLES: Continue development of cluster SIMS technique for depth-profiling of semiconductors.

Cluster primary ion beam SIMS offers several advantages for the analysis of semiconductor materials. Compared to conventional SIMS analysis using monoatomic primary ions, cluster bombardment SIMS offers improvements in depth resolution, higher sputter rates and increased sensitivity for some elemental species. Also, greater sensitivity for organic species may greatly increase our ability to detect organic contamination on silicon surfaces. We are exploring various applications of this technique and attempting to develop new, low cost cluster ion beam sources to promote more widespread use of the technique.

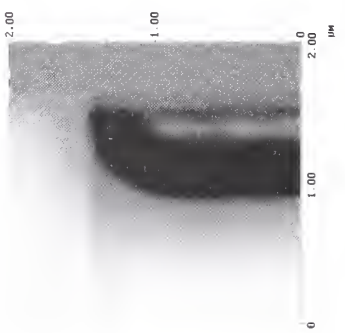
DELIVERABLES: Development of ion implant reference materials.

Development of ion implanted reference materials for the semiconductor industry has been given a high priority by the International SEMATECH Analytical Lab Managers Working group. Previous ion implant NIST standards include B in silicon (SRM 2137) and As in silicon (SRM 2134) which was released in FY 2000. Current efforts are focused on development of a P ion implant standard in silicon.

The SCM group is developing tools that are intended to enable scanning capacitance microscopes to function as two-dimensional dopant profiling tools. This work is divided into three tasks: Task 1 is to develop SCM measurement methodologies. Best measurement practices are being determined via collaborative projects with industrial users and research into the physics of the silicon surface preparation. Task 2 is to develop theoretical models of the SCM. The focus of our modeling effort has been to develop 2-D and 3-D finite-element solutions of Poisson's equation for the SCM geometry. Task 3 is interpretation of SCM data and technology transfer. Our expertise with interpreting SCM images is being transferred to industry through our software program *FASTC2D*. The program features an easy to use interface, rapid profile extraction, and operation in a Windows environment.



SCM image of a p+/n junction.



Dopant contours extracted with *FASTC2D* .

DELIVERABLES: By 2002, develop and characterize "known good sample" for distribution with ***FASTC2D*** code.

The version of *FASTC2D* currently available utilizes a calibration curve, determined from a

database of pre-calculated solutions, which can very rapidly determine a 2-D carrier profile from an SCM image. When used in conjunction with SIMS measurements or a reference sample, relatively accurate profiles can be obtained. We are also developing an additional tool for technology transfer: a new generation of test structures consisting of fully processed and partially processed transistors. These will eventually be produced in sufficient numbers so that every *FASTC2D* user can get a set. A round-robin set of measurements based on these structures and using an easy to implement measurement procedure, is planned, with devices to be distributed through the SEMATECH 2-D dopant profiling working group.

DELIVERABLES: By 2003, demonstrate optimized 3-D calculations of the SCM signal across dopant gradients and junctions.

To meet industrial needs for 2-D dopant profiling to the end of the ITRS, requires a physically accurate 3-D model and determination of dopant profile by an inverse solution. We have previously developed a quasi-3-D model of the SCM that predicts the essential behavior of the SCM measurement. However, for the required dopant profiling performance goals, a more rigorous approach is necessary. Towards this end, the finite element method has been employed to solve Poisson's Equation for the SCM geometry in three-dimensions. Accuracy requirements may also force the consideration of quantum mechanical effects, necessitating the solution of the coupled Poisson and Schrödinger Equations. We are developing improved 3-D Poisson solvers using the LaGriT grid management toolbox in collaboration with Los Alamos National Laboratories.

DELIVERABLES: By 2004, have available for distribution to users a computationally efficient method of determining carrier profiles from inverse solutions of SCM based on 3-D models.

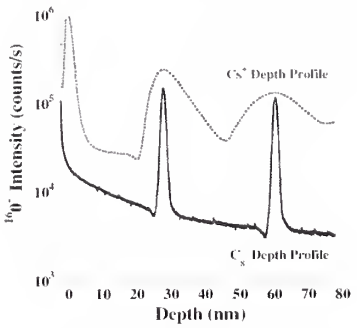
An inverse solution of the SCM requires repeated solutions of the forward problem, i.e. calculation of the SCM signal from candidate carrier profiles. The candidate carrier profile is adjusted until a carrier profile is found that yields a calculated SCM signal that agrees with the measured SCM signal. Project staff have developed a regression procedure to do this with a 2-D solver. The final level of refinement is to use the full 3-D model as the basis of inverse solutions of the SCM. However, the volume of data to be processed and the time required for calculation makes this intractable for routine profile extraction. Practical application requires finding shortcuts that will achieve the 3-D result without having to complete the entire round of 3-D simulations.

Accomplishments

■ **High Repeatability SIMS Measurements** - In the third quarter of FY 2001 we collaborated with Agere Systems to investigate the parameters that must be controlled to make highly repeatable dose measurements of As and P implants in Si with magnetic sector SIMS instruments. With optimized settings, we demonstrated the ability to distinguish As or P implant doses differing by 5 % with an RSD of less than 0.5 % in favorable cases. As the level of required precision for SIMS dopant concentration measurements continues to increase, consideration must also be given to more subtle effects that may affect the measurement. In particular, the behavior of the secondary ion detection system (electron multiplier) may become a significant factor. Typically, the detector settings used in routine analyses are those set by the tool manufacturer. However, these are not always optimal for high precision measurements. We have found that the detection sensitivity for elements such as Si and B can change by a factor of 2 depending on the energy of the detected secondary ion and the settings of the detection system. We have developed a system at NIST that allows for reproducible detector setup and optimization. We hope this may allow us to achieve even higher levels of precision for dopant concentration measurements.

■ **TOF SIMS Analysis** – Dual-beam TOF SIMS depth profiles were carried out on boron delta-doped structures with layer spacings of 15 nm and 7.5 nm and thin oxide dielectric films. Optimal conditions were determined for each sample type. We have found that the current density of the Ga^+ analysis beam has a profound effect on the measured depth resolution. Smaller raster sizes and corresponding higher analysis beam current densities produce effects that degrade the depth resolution significantly. This effect places limits on the minimum area that can be analyzed by TOF SIMS and also places limits on the concentration of dopants that can be measured with high depth resolution. Additional studies were conducted on the TOF-SIMS to characterize the effect of residual gas adsorption from the vacuum chamber on the measured secondary ion signals from various metal surfaces. Large time-dependent variations in matrix signals were observed from several metal surfaces. We hope to use this information for optimizing the TOF-SIMS for high precision analysis of surface contamination and surface metals.

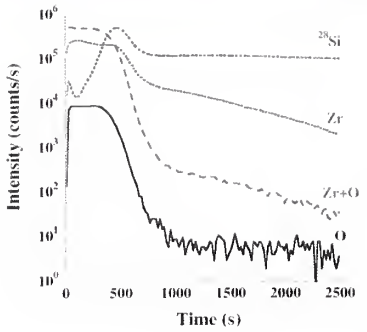
■ Metal Depth-Profiling - In a study with Advanced Micro Devices, sample rotation SIMS depth-profiling were determined. Additional studies were conducted using cluster ion beams to reduced sputter-induced topography. SIMS depth profiles of a Cr/CrO_2 multilayer structure with CrO_2 monolayers spaced 30 nm apart were analyzed using both Cs^+ and C_8^- primary ions while monitoring negative secondary ions. The C_8^- shows a substantial improvement in depth resolution. AFM analysis of the crater bottoms demonstrated the rms roughness was 6 times lower using C_8^- bombardment.



SIMS depth profile of Cr/CrO_2 multilayer sample demonstrating improvement in depth resolution resulting from a reduction in beam-induced topography.

■ **Standard Reference Material Ion Implant Development** - Radiochemical neutron activation analysis procedures for the certification of phosphorus implant dose have been refined to the point that a relative standard deviation of 1.3 % was achieved in measurements of 12 samples from an implanted wafer. We now estimate that an expanded relative uncertainty of about 3 % can be achieved for the certification of dose of a Standard Reference Material, and plans are on track to produce an SRM in FY02.

■ **Polyatomic Primary Ion Beam SIMS** - Studies of polyatomic primary ion beam sources for high depth resolution SIMS dopant profiling are continuing. Collaborations with international SEMATECH have focused on depth-profiling of novel ZrO_2 films on both magnetic sector and TOF-SIMS instruments. A new polyatomic ion source has been designed and constructed that features an externally removable reaction chamber that will allow for use either as a standard duoplastmatron or as an SF_5^+ source.



SIMS DEPTH PROFILE OF ZrO_2 OXIDE LAYER (6 NM THICKNESS) WITH SF_5^+ DEPTH-PROFILING.

■ **Demonstrated a two-dimensional regression procedure** to solve the SCM inverse problem of finding the dopant profile from measured SCM signal. This is the first time that an optimized regression procedure has been used to find the SCM inverse solution based on numerical solution of the Poisson's equation. Second generation (inverse modeling) SCM interpretation techniques are a significant improvement over the first generation (calibration curve) techniques. The technique uses two meshes to achieve conversion in only a few iterations (5 steps of the coarse mesh and 2 steps of the fine mesh for a model problem). Inverse solutions determined by this technique fully include the effects of the local dopant gradient and gradient curvature on the SCM measurement of the dopant profile. The method can handle dopant profiles in like type substrates or in opposite type substrates (i.e., across p-n junctions). The procedures developed for the 2-D model are expected to be useful for the 3-D models that are currently under development.

■ **Development of 3-D models of the SCM** in collaboration with Los Alamos National Laboratories by applying their LaGriT (Los Alamos Gridding Toolkit) software package. LaGriT is a library of user callable tools that provide 3-D mesh generation, mesh optimization, and dynamic mesh maintenance for finite element methods. Access to such code will enable more efficient 3-D simulations of the SCM measurement across dopant gradients and p-n junctions.

■ **Compared the response of SCMs** using sensors from four different manufacturers and correlated the double zero crossing in SCM signal sometimes observed at p-n junctions with the magnitude of the sensor high frequency voltage. Publication submitted.

■ **Development of scanning microwave microscope** - Atolytics, Inc. in State College,

PA, has started the second year of their SBIR phase II contract to develop a commercial version of their scanning microwave microscope. A prototype instrument has been constructed. Manufacturing Instrumentation Consultant Co of Cleveland, OH, has been granted an SBIR phase II contract to develop co-axial shielded scanning probe microscope tips. Tips will be evaluated by NIST.

■ **Application of SCM to Dopant Profiling of High Bandgap Semiconductors** - Summer students Brenda Handy, Howard University and Quan Chau, University of California, Berkley, developed a process to prepare cross-sections of SiC for examination with the SCM. Depletion layers and micropipes in SiC have been imaged with the SCM. Work is underway to apply SCM to other high bandgap semiconductors such as GaN.

FY Outputs

■ New analytical procedures for SIMS were developed that allow dose repeatability measurements of 0.5% or better.

■ Identified and characterized artifacts that may be a limiting factor for TOF SIMS depth-profiling of ultrashallow implants.

■ New approaches were developed for depth-profiling of metal films while minimizing sample topography.

■ The Annual Workshop on SIMS was held recently in Phoenix, AZ. A special session was organized on the standards and measurement needs of the semiconductor industry. A critical need for Si/Ge reference materials was highlighted. The development of such reference materials will be pursued in FY 2002.

Collaborations

Agere Systems, Jack Hergenrother, quantitative SCM of vertical replacement-gate transistors.

Agere Systems, Fred Stevie – Dose repeatability of SIMS measurements.

AMD – Metal film depth-profiling by SIMS.

Atolytics Inc, Paul Weiss – Phase II SBIR to develop a commercial version of their scanning microwave microscope

Howard University, Gary Harris – Application of SCM to high bandgap semiconductors.

International SEMATECH, Joe Bennett – Thin oxide depth-profiling by SIMS.

Los Alamos National Laboratory, Denise George and Charles Snell – Development of next generation 3-D Poisson simulators using the LaGrit grid management toolbox.

Manufacturing Instrumentation Consultant Co – Phase II SBIR to develop co-axial shielded scanning probe microscope tips.

Peabody Scientific – Ion source development for SIMS.

University of Queensland, Brisbane, Australia. Prof. Tong Yeow was a guest research during the summer of 2000. Dr. Yeow learned to operate the SCM and acquired SCM data of NIST test structures for interpretation using Medici and inverse modeling.

External Recognition

Dept. of Commerce Bronze Metal Award, recognized as having greatly accelerated development of SCM as a practical measurement tool, November 29, 2000 (Joseph J. Kopanski, Jay F. Marchiando, and Brian G. Rennex).

Senior Member IEEE, March 31, 2000 (Joseph J. Kopanski)

Invited Review Article, J. J. Kopanski, Scanning Capacitance Microscopy, to be published in The Encyclopedia of Imaging Science and Technology, John Wiley & Sons, (New York, 2002).

CSTL Technical Achievement Award for Certification of Ion-Implanted Arsenic-in-Silicon SRM 2134 (David Simons, Robert Greenberg, and Richard Lindstrom).

Recent Publications

A. J. Fahey and S. V. Roberson, "Shallow Depth Profiling with ToF-SIMS and the Effect of Analysis Beam Current Density on Depth Resolution," Submitted to J. Vac. Sci. Technol. (2001).

P. H. Chi, D. S. Simons, J. M. McKinley, F. A. Stevie, and C. N. Granger, "High Precision Measurements of Arsenic Implantation Dose in Silicon by Secondary Ion Mass Spectrometry," in *Characterization and Metrology for ULSI Technology 2000*, D. G. Seiler *et al.*, eds., A.I.P. Press, pp. 682-686 (2001).

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D. E. McBride, J. J. Kopanski, and B. J. Belzer, "Gate Oxide Formation Under Mild Conditions for Scanning Capacitance Microscopy," in *Characterization and Metrology for ULSI Technology*, D. G. Seiler *et al.*, eds., A.I.P Press, pp. 657-661 (2001).

R. L. Paul and D. S. Simons, "Neutron Activation Analysis for Calibration of Phosphorous Implantation Dose," in *Characterization and Metrology for ULSI Technology*, D. G. Seiler *et al.*, eds., A.I.P. Press, American Institute of Physics, pp. 677-681 (2001).

B. G. Rennex, J. J. Kopanski, and J. F. Marchiando, "*FASTC2D*: Software for Extracting 2D Carrier Profiles from Scanning Capacitance Microscopy Images," in *Characterization and Metrology for ULSI Technology*, D. G. Seiler *et al.*, eds., A.I.P Press, pp. 635-640 (2001).

E.R. Fuoco, G. Gillen, M. B. J. Wijesundara, B. Wallace, and L. Hanley, "Surface analysis studies of yield enhancements in secondary ion mass spectrometry by polyatomic projectiles," J Phys. Chem **B 105**(18), 3950-3956 (May 10 2001).

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K. D. Hobart, P. E. Thompson, S. L. Rommel, T. E. Dillon, P. R. Berger, D. S. Simons, and P. H. Chi, "p-on-n Si interband tunnel diode grown by molecular beam epitaxy," J. Vac. Sci. Technol. B **19**(1), 290-293 (Jan-Feb 2001).

K. G. Krider and G. Gillen, "High Temperature Materials for Thin-Film Thermocouples on Silicon Wafers," Thin Solid Films **376**, 32-37 (2000).

P. E. Thompson, K. D. Hobart, M. E. Twigg, S. L. Rommel, N. Jin, P. R. Rger, R. Lake, A. C. Seabaugh, P. H. Chi, and D. S. Simons, "Epitaxial Si-based tunnel diodes," Thin Solid Films **380**(1-2), 145-150 (Dec 22, 2000).

R. R. Greenberg, R. M. Lindstrom, and D. S. Simons, "Instrumental neutron activation analysis for certification of ion-implanted arsenic in silicon," J. Radioanal. Nucl. Chem. **245**(1), 57-63 (Jul 2000) .

J. J. Kopanski, J. F. Marchiando, and B. G. Rennex, Carrier Concentration Dependence of the Scanning Capacitance Microscopy Signal in the Vicinity of p-n Junctions, *J. Vac. Sci. Technol. B* 18(1), 409-413 (Jan/Feb 2000).

J. F. Marchiando, J. J. Kopanski, and J. Albers, Limitations of the Calibration Curve Method for Determining Dopant Profiles from Scanning Capacitance Microscope Measurements, *J. Vac. Sci. Technol. B* 18(1), 414-417 (Jan/Feb 2000).

Recent Talks

J. Kopanski, "Scanning Capacitance Microscopy for Measuring Device Carrier Profiles Beyond the 100 nm Generation", 2000 International Microprocesses and Nanotechnology Conference (MNC 2000), The Univ. of Tokyo, JAPAN, July 11-13, 2000. (INVITED).

D. Simons, "Secondary Ion Mass Spectrometry in Semiconductor Metrology," Pacific Northwest National Laboratory, Richland, WA, October 17, 2000. (INVITED)

G. Gillen, "Surface Analysis with Energetic Cluster Ion Beams," PITTCON, New Orleans, LA, March 5, 2001.

G. Gillen, "SIMS Depth Profiling with Cluster Primary Ion Beams," Surface Analysis 2001Meeting, Orlando, FL, March 12-14, 2001.

G. Gillen , "Secondary Ion Mass Spectrometry Using Cluster Ion Beams," National Security Agency and University of Maryland, April 4, 2001. (INVITED)

J. Kopanski, "Comparison of Experimental and Theoretical Scanning Capacitance Microscope Signals and Their Impact on the Accuracy of Determined Two-Dimensional Carrier Profiles," Sixth International Workshop on the Fabrication, Characterization and Modeling of Ultra Shallow Doping Profiles in Semiconductors," Napa, CA, April 22-26, 2001.

D. Simons, "Reference Materials for SIMS - What we have now and what we need," 14th Annual SIMS Workshop, Scottsdale, AZ, May 14, 2001.

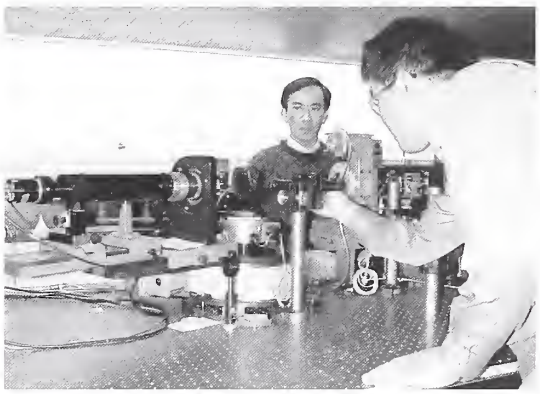
A. Fahey and G. Gillen, "Characterization of Electron Multiplier Post Acceleration using Pulse Height Distributions," 14th Annual SIMS Workshop, Scottsdale, AZ, May 14, 2001.

P. Chi, "Roughness Reduction on Depth Profiling of Cu Films with Sample Rotation," 14th Annual SIMS Workshop, Scottsdale, AZ, May 14, 2001.

Gate Dielectric Metrology

Goals

To develop new and improved electrical and optical measurements, models, data, and reference materials to enable better and more accurate measurements of select, critical, thin-film parameters for silicon Complementary Metal Oxide Semiconductor (CMOS) technology. Major focus is placed on requirements for oxynitrides, and metal-oxide and metal-silicate films and stacks for advanced gate dielectrics detailed in the 1999 International Technical Roadmap for Semiconductors (ITRS).



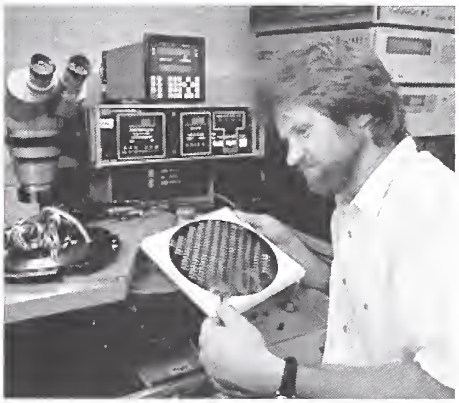
RESEARCHERS ALIGN SAMPLE ON CUSTOM-BUILT HIGH-ACCURACY SPECTROSCOPIC ELLIPSOMETER.

To address needs in composition and thickness measurements for thin films and interfaces including high and low k materials from gate dielectrics to polymers. This project develops new methods and standards as well as characterizes the accuracy and reliability of existing methods using analytical electron, X-ray, and laser probes. This year the project has four main components:

Develop Grazing Incidence X-ray Photoelectron Spectroscopy (GIXPS) for the measurement of silicon oxide and oxynitride films and determine the uncertainty of this method.

- Characterize the accuracy of High Resolution Transmission Electron Microscopy (HRTEM) for thickness measurements of ultra-thin gate dielectrics.
- Develop Nonlinear Optical (NLO) methods for the characterization of thin film interfaces in polymers and simple oxides.
- Apply extended x-ray absorption fine structure (EXAFS) and electron energy loss spectroscopy (EELS) to characterize compositional homogeneity and local-scale structure in ultrathin (< 10 nm) dielectric films.

To provide electrical and reliability measurement techniques, data, physical models, and fundamental understanding for ultra-thin silicon dioxide and alternate gate dielectrics in future MOS devices. To increase the understanding of the relationship between the gate dielectric material/interface properties and device electrical and reliability measurements.



TEST WAFER BEING LOADED ON WAFER PROBER FOR LONG-TERM DIELECTRIC TESTING.

Customer Needs

The evolving decrease of the gate dielectric film thickness to an oxide-equivalent value of 1 nm is identified as a critical front-end technology issue in the ITRS. For effective gate dielectric thicknesses below 2.0 nm, SiO_2 is being replaced, initially by oxynitrides or oxide/nitride stacks, and then by either metal-oxides or metal-silicates. Process control tolerance needs for dielectric thickness are projected to be ±4 % (3 s), which translates to less than 0.1 nm for 2 nm films. Requirements for process control measurements are a factor of ten smaller still.

Spectroscopic ellipsometry (SE) is expected to continue as the preferred measurement for process monitoring of future gate dielectric films. Industry metrology needs not only improved methods to determine film thickness accurately, but also (1) techniques to determine the structure of the individual films and the interfaces between them; (2) an improved understanding of the relationship between physical, electrical, and optical determinations of film properties; and (3) mechanisms, such as reference materials, for traceability of measurements to NIST to support film metrology.

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Staff-Years (FY 2001):
9.3 professionals
2.3 technicians
5 guest researchers

Funding Sources:
STRS (96 %)
Other Agency (4 %)

In order for SE to meet process control requirements of film thickness and unambiguously determine film composition and morphology, the optical properties of these advanced dielectric film systems must be characterized and understood.

The microelectronics industry has a high demand for reliable thin film measurement methods that yield composition and dimension information with known accuracy and precision. The metrology section of the ITRS 1999 metrology section clearly states the needs for "reference materials and standard measurement methodology for new, high k gate and capacitor dielectrics with interface layers, thin films such as interconnect barrier and low k dielectric layers, and other process needs. Optical measurement of gate and capacitor dielectric averages over too large an area and needs to characterize interfacial layers. The same is true for measurement of barrier layers."

As semiconductor processing and devices move to smaller dimensions and new materials, the characterization of the device thin film thickness, composition, and interface quality become ever more critical to device operation and reliability.

The Roadmap for Semiconductors indicates that the equivalent thickness of the gate dielectric will need to be 1.0 nm to 1.5 nm by 2004. Due to increased power consumption, intrinsic device reliability and circuit instabilities associated with SiO_2 of this thickness, a high permitivity gate dielectric (e.g., Si_3N_4, $HfSi_xO_y$, ZrO_2) with low leakage current and at least equivalent capacitance, performance, and reliability will be required. The physics of failure and traditional reliability testing techniques must be reexamined for ultra-thin gate oxides that exhibit excessive tunneling currents and soft breakdown. Electrical characterization of Metal Oxide Semiconductor (MOS) capacitors and Field Effect Transistors (FET) has historically been used to determine device and gate dielectric properties such as insulator thickness, defect densities, mobility, substrate doping, bandgap, and reliability. Electrical and reliability characterization methodologies need to be developed and enhanced to address issues associated with both ultra-thin SiO_2 and alternate dielectrics including large leakage currents, quantum effects, and thickness dependent properties. As compared to SiO_2, very little is known about the physical or electrical properties of high dielectric constant gate dielectrics in MOS devices. The use of these films in CMOS technology requires a fundamental understanding of the relationship between the gate dielectric material/interface and device electrical and reliability measurements.

Technical Strategy

This project focuses on the issues of (1) developing and providing the basis for traceability to NIST for film thickness measurements, (2) identifying structural models and developing preferred optical index dispersion functions or data for improved ellipsometric analysis of future-generation gate dielectric film systems, and (3) correlating optical, electrical, and physical measurements of thickness, composition, and interface structure.

Establish and transfer basis of accuracy for thin dielectric films

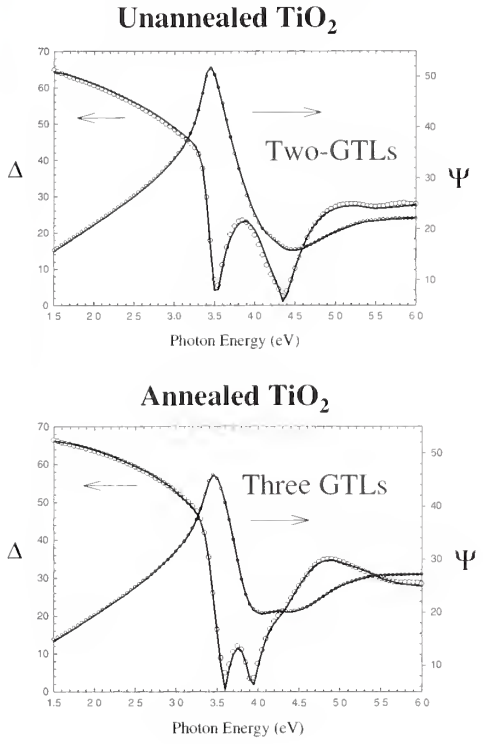
Industry requirements for future thin dielectric film optical measurements and calibration standards were identified at a NIST-sponsored workshop in FY 98. Core ellipsometry measurement capability is being expanded and strengthened to meet these requirements. An investigation has been started into cleaning and recontamination issues for film calibration standards to determine whether a workshop-expressed goal of 0.015 nm long-term reproducibility of reference artifact values is obtainable. Procedures are being developed to enable traceability of instrument accuracy to NIST for suppliers of secondary thin-film reference materials without requiring volume production of NIST standard reference materials.

DELIVERABLES: Develop and evaluate prototype procedures that will enable traceability to NIST for 1st Level commercial suppliers of reference materials for oxide films down to 2 nm.

Structural and optical models for ellipsometry

A custom-built, high-accuracy spectroscopic ellipsometer with a spectral range of 1.5 eV - 6 eV is being used for this task, and Project staff are working with ISMT, IC industry companies, and SRC university staff to obtain and optically characterize advanced oxynitrides, oxide/nitride stacks, and metal oxide and silicate films such as zirconium oxide and hafnium silicate. Characterization will be extended to 8.5 eV to include important optical index structure of these films beyond their bandgaps. This work is directed at determining preferred structural models, spectroscopic index of refraction values, or preferred optical dispersion functions for each of these film systems, and, where possible, the variability of these parameters due to differences in film fabrication processes. Analysis is done with software developed by NIST for spectroscopic ellipsometry; this software allows maximum

flexibility for addition of the latest published or custom-developed optical response models as appropriate for each material system investigated.



FITTING THE COMPLEX ELLIPSOMETRY SPECTRA OF TiO_2 WITH THE RECENTLY DEVELOPED GENERALIZED TAUC-LORENTZ DISPERSION FUNCTIONS.

DELIVERABLES: Evaluate ellipsometric structural and optical models to determine suitability for process monitoring and control of advanced gate dielectric materials.

Relation between optical, electrical, and physical measurements of thickness

Through collaborations with ISMT, IC industry companies, and SRC university staff, as well as with key researchers in other parts of NIST, Project staff are leading and participating in a number of multimethod comparison studies of various ultra-thin gate dielectric films. These multimethod studies utilize techniques such as X-ray and neutron reflectivity, high resolution TEM, EELS, angle-resolved XPS, SIMS, C-V and I-V analysis, as well as spectroscopic ellipsometry and reflectivity. The results of these multimethod studies improve the general understanding of state-of-the-art (SOA) measurement capability for very thin films, and also allow Project staff to assess the results of various optical models being applied to the analysis of these films with respect to interface layers and structural composition, morphology, and uniformity. SOA C-V and I-V measurement capability for gate films has been established in the Project. Advanced 1-D analysis software from commercial and university sources has been established and benchmarked to determine the effect of model and algorithm sophistication on oxide film thickness values calculated from C-V and I-V data; extension to 2-D modeling is planned.

DELIVERABLES: Integrate preferred advanced electrical analysis software and structural analyses of high-k dielectrics to improve agreement between electrical and ellipsometric thickness scales.

Many of the existing and innovative analytical procedures for the analysis of thin films such as x-ray photoelectron spectroscopy (XPS), non-linear optical spectroscopies (NLO), high resolution (HRTEM) and analytical electron microscopy (AEM) with x-ray and electron energy loss spectroscopies, low voltage scanning electron microscopy x-ray analysis, and Auger spectroscopy must be significantly improved to obtain accurate quantitative composition measurements on films with thicknesses below 10 nm. Our goals are to develop the necessary methods, analytical correction procedures, standard data and materials to determine realistically achievable accuracy levels for analysis of thin films by these techniques. Films for these measurement activities are obtained from industrial sources and fabricated in-house by spin coating metalorganic solutions.

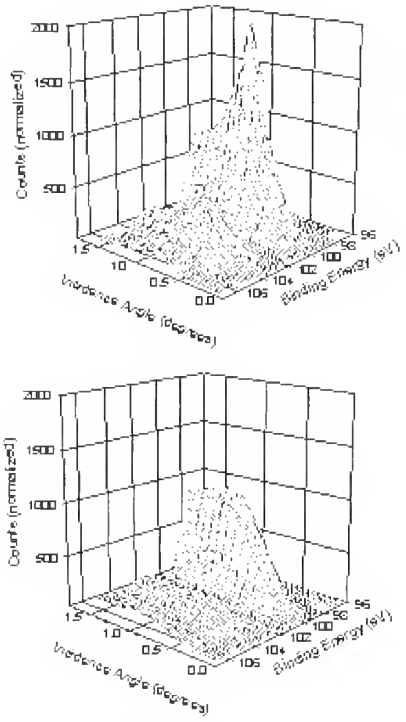
Vibrational spectroscopy is a powerful probe of chemical structure. Unfortunately, IR absorption studies of the development of a mature thin-film interface are impossible. The technique is sensitive to the *entire* film, and the film signal quickly overwhelms that of the interface structure. Second order nonlinear optical techniques such as second harmonic generation (SHG) and sum frequency generation (SFG) are symmetry forbidden in centrosymmetric media such as bulk Si or SiO_2. Thus they are uniquely interface sensitive. SHG studies of SiO_2 films on Si have demonstrated empirical sensitivity to diverse properties of the interface, including strain, roughness, and midgap interface trap density. It is expected that properties such as interface roughness and midgap trap density will be correlated. We are investigating and developing nonlinear optical methods as probes of interfaces in semiconductor thin films.

Grazing incidence XPS allows both depth and chemical information to be attained from very thin (less than 10 nm) films. Using a NIST designed, built, and patented device on the Brookhaven synchrotron we have been

developing the necessary instrumentation and data interpretation procedures to characterize ISMT silicon oxynitride films.

One of the more common methods of evaluating film thickness and composition is through the use of HRTEM and Analytical TEM, respectively. But the uncertainty of these approaches has only recently been looked at quantitatively. Films of dielectric materials grown on silicon were obtained from ISMT and analyzed to determine the accuracy of this HRTEM and AEM approach. Comparisons across many methods were made to determine the relative accuracy and precision of these approaches.

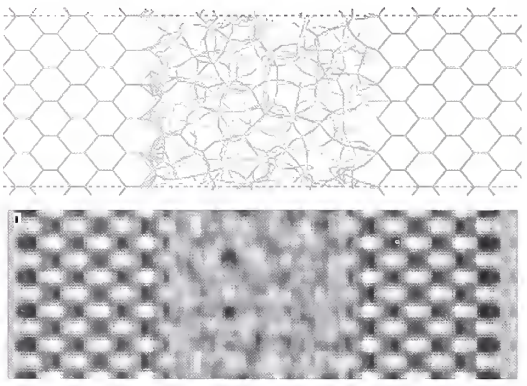
DELIVERABLES: Develop Grazing Incidence X-ray Photoelectron Spectroscopy (GIXPS) for the measurement of silicon oxide and oxynitride films and determine the uncertainty of this method.



Comparison of Si 2p XPS spectra with angle taken at 1823 eV (top) and 1844 eV (bottom) from the same sample. The changes in the spectra reflect changes in the index of refraction across the Si K edge at 1839 eV.

GIXPS has been employed successfully as a novel means to analyze the depth, density, and chemical composition of the ultrathin dielectric layers being researched for future semiconductor devices. Serious discrepancies exist among the traditional methods of measuring these layers below 10 nm thickness. An important consideration has therefore been a determination of the accuracy of this new method and its potential sources of error. Discrepancies may also exist because of differences between phenomenological and discrete (i.e., atomic) measurements. We have addressed the first question by studying the dependence of the results obtained from the GIXPS method on the accuracy of the physical parameters required as inputs. We are studying the second question by comparison with scattering measurements by short wavelength probes like x-rays and neutrons.

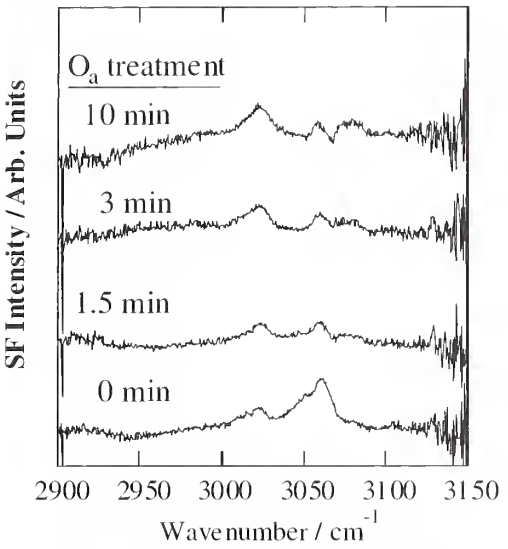
DELIVERABLES: Characterize the accuracy of High Resolution Transmission Electron Microscopy (HRTEM) for thickness measurements of ultra-thin gate dielectrics



MOLECULAR MODEL OF A GATE STACK (TOP) AND ONE FRAME FROM AN HRTEM SIMULATION MOVIE (BOTTOM) SHOWING CHANGES IN APPARENT THICKNESS WITH CHANGING IMAGING CONDITIONS.

The ability of HRTEM to measure the thickness of sub-4 nm gate dielectric films is in question, pending a quantitative understanding of the errors and uncertainties in the measurement process. The goal of this work is to quantify the accuracy of HRTEM as a technique for measuring the thickness of such films. Because device performance is very sensitive to the dielectric thickness, semiconductor device manufacturers consider this a critical fabrication parameter and are keenly interested in its accurate measurement. To address this problem, a suite of computer modeling tools was developed to build virtual gate stacks and simulate HRTEM micrographs from these stacks. Using these new tools, several hundred images of amorphous SiO_2 films between Si substrates were calculated, covering a range of imaging conditions and sample parameters. Combining the apparent thickness from the micrograph (measured value) and the known thickness from the model (true value) calculation of the accuracy as a function of the input variables is possible. A quantitative under-

standing of the errors in HRTEM thickness measurements plays an important role in improving the quality and yield of semiconductor electronic device fabrication.



VIBRATIONALLY RESONANT SFG SPECTRA ILLUSTRATING CHANGES IN MOLECULAR ORIENTATION, WHICH CORRELATE WITH ATOMIC OXYGEN TREATMENT OF THE SUBSTRATE AND CHANGES IN ADHESION

DELIVERABLES: Develop a new technique that enables selective measurement of free and buried polymer interfaces by vibrationally resolved sum frequency generation spectroscopy (VR-SFG).

VR-SFG is generally applicable to optical quality films and is demonstrated here for the buried polystyrene/ dielectric interface. Manipulation of Fresnel coefficients through the choice of film thicknesses allows enhancement of the nonlinear optical signal from the desired interface and cancellation of the signal from other obscuring interfacial sources. Our spectra reveal intuitively and through straightforward analysis that the phenyl group orientation for the buried interface is in the opposite direction of the phenyl groups at the top surface. The molecular ordering at the polymer/dielectric interface changes with changing hydrophobicity of the dielectric surface and correlates to the adhesive strength of the interface.

DELIVERABLES: Measure crystallinity in ZrO_2 films by EXAFS

EXAFS is a synchrotron x-ray spectroscopy tool that determines the average short-range (about 0.5 nm) local structural information around an atom that has absorbed an x-ray photon. Since the separate local structure around each atomic type present in a material can be measured, the technique is chemically sensitive. We are investigating the applicability of EXAFS to study crystallization and chemical bonding in gate dielectric films.

The strategy of this effort will be to obtain or fabricate both device samples and blanket films, to perform reliability and electrical characterization of the devices, and to collaborate with other researchers to perform analytical characterization. Many issues such as tunnel/leakage current and spatially dependent properties associated with metal oxide and silicate dielectrics are also present in ultra-thin oxide and oxide-nitride stacked dielectrics. Therefore, many of the characterization schemes will first be developed on the simpler ultra-thin oxide and oxide-nitride dielectrics and then be applied to the metal oxide and silicate dielectrics.

There are two main focus areas for this project. The first focus area investigates the physics of failure and the reliability testing techniques for ultra-thin SiO_2 and high dielectric constant gate dielectrics. The physical mechanism responsible for "soft" or "quasi" breakdown modes in ultra-thin SiO_2 films and its implications for device reliability will be investigated as a function of test conditions and temperature. Long-term time-dependent-dielectric breakdown tests will be conducted on SiO_2 films as thin as 1.5 nm at electric fields close to operating conditions. These tests will be used to determine the thermal and electrical acceleration parameters of device breakdown.

DELIVERABLES: Studies of the long-term drift and stability of post-soft conduction in ultra-thin SiO_2 films including voltage and temperature acceleration parameters.

Experiments will be conducted to investigate the differences of gate oxide breakdown and wear-out due to high oxide field and hot-carrier injection. This study will provide insight into the physical mechanism of ultra-thin gate oxide wear-out and breakdown.

DELIVERABLES: Experimental results of the electron-hole interaction in SiO_2 and the affect on dielectric breakdown. Studies of oxide degradation using high voltage, short time single pulse stressing.

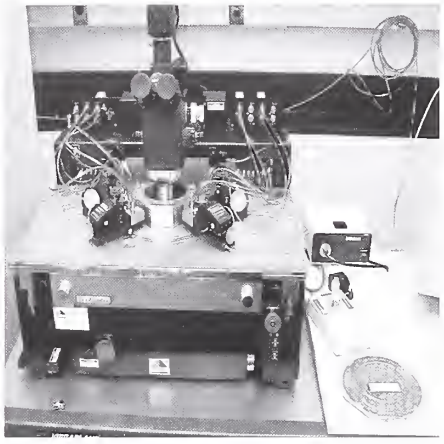
The understanding generated in this research will be used to continue generating standard measurements through a NIST coordinated collaboration between EIA-JEDEC (Electronic Industries Association Joint Electron Device Engineering Council) and the American Society for Testing and Materials (ASTM). Studies on the reliability of high dielectric constant

"NIST-traceable standards are increasingly necessary for the precise calibration of diverse metal film thickness measurement tools."

Alexander E. Braun, Metal Film Thickness Standards Enable NIST-Traceable Calibration, Semiconductor International, June 2001

dielectrics such as oxide-nitride stacks will also be performed.

DELIVERABLES: A new standard constant voltage stress test will be developed for determining Time-Dependent-Dielectric Breakdown (TDDB) acceleration parameters in sub 3 nm thick SiO_2 films. The new test will utilize current or voltage noise as breakdown criteria when films exhibit soft breakdown. Such a test will find application by the semiconductor industry when qualifying new manufacturing processes.



A LOW-NOISE (FA), HIGH TEMPERATURE (300 °C) PROBE STATION IS USED TO ELECTRICALLY CHARACTERIZE DEVICES.

The second focus area is to investigate electrical measurement techniques, procedures and analysis associated with devices having thin oxide and alternate gate dielectrics. The electrical measurement techniques that we are investigating include capacitance-conductance characterization, dielectric tunnel and leakage current characterization and defect density measurements such as charge pumping and conductance. Furthermore, standard properties and mechanisms/correlations for these dielectrics including defect centers, dielectric constant, defect generation rates, and leakage/tunnel current will be characterized

DELIVERABLES:. A Visual Basic-based application that simulates capacitance-voltage and long-channel drain current including insulator defects, quantum mechanical and polysilicon depletion effects.

High-k gate dielectric films will be obtained from key industrial and university groups. Electrical characterization methodologies will be developed to address various issues associated with these films, including large leakage currents, quantum effects, thickness dependent properties, large trap densities, transient (non-steady state) behavior, unknown physical properties, and the lack of physical models.

Examples of measurement problems that are being addressed include modifying and verifying electrical defect density measurement techniques, including conductance-frequency, capacitance-voltage, and charge-pumping.

DELIVERABLES: Studies of insulator defects and current transport through high-k dielectrics (e.g., HfO_2) including current noise, and the energy distribution of HfO_2 interface states using conductance.

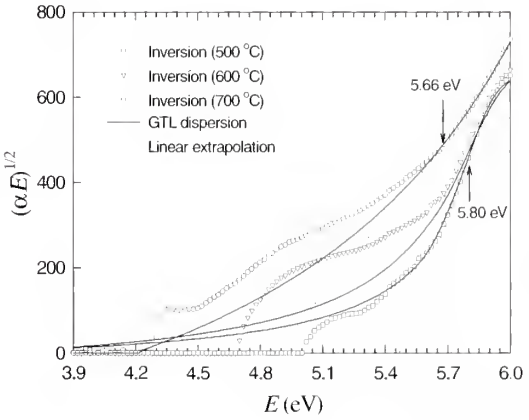
Accomplishments

- Completed extensive upgrade of Master high accuracy ellipsometer that was originally developed for certifying oxide thickness SRMs; the upgrade is intended to enable attainment of improved short-term and long term precision needed to meet industry needs for thin dielectric measurement traceability. Upgrades included a power/frequency stabilized HeNe laser, large area photodiode, new A/D electronics with higher conversion resolution, improved low noise motor drive for the rotating analyzer, and completely rewritten system control and data acquistion software in a format that enables easier maintenance and upgrade. An autocollimator to monitor stability of sample alignment, a temperature readout in the vicinity of the wafer, and monitoring of laser power were also added to enable identification of possible sources of unacceptable measurement variability. Initial tests showed sample alignment to be stable to better than 0.001deg over many hours, very good short term (1/2 hour time-frame) sample measurement stability, but full-day precision was inconsistent with only partial correlation of variability with temperature. A matrix of additional thermocouples is being added to a variety of points in the ellipsometer to better pinpoint measurement sensitivity to the temperature of various system components.

- A three-pass sample exchange for single-wavelength (SWE) and spectroscopic ellipsometry (SE) measurement of film thickness was completed by NIST and VLSI Standards Inc. The samples were a set of silicon nitride films of moderate to larger thicknesses. Single wavelength measurements from both labs were in excellent control and showed good agreement of film thickness values. Relatively large discrepancies resulted from the SE measurements at both laboratories, however. This occurred despite careful planning that included such factors as using optical constants for silicon and silicon-nitride at 632.8 nm that were taken from the spectroscopic data base for these materials.

This experiment is being used by NIST to develop an understanding of potential pitfalls in measurement exchange programs that are expected to be used expected to expected to be used as the basis for future programs to offer film thickness measurement traceability to NIST. In the case of the silicon-nitride sample exchange, additional investigation of sources of observed SE discrepancies are ongoing.

■ Several sets of oxynitride and metal-oxide/silicate films were measured by spectroscopic ellipsometry in order to determine preferred structural models and optical dispersions for determining film thickness, dielectric function and the possible existence of interface layers. One of these, a set of HfO_2 films, fabricated by physical vapor deposition and annealed at temperatures from 500 °C to 700 °C was measured over the range energy range 1.5 to 6.2eV. The 500 °C annealed specimen was fit well with a single Tauc-Lorentz (T-L) dispersion without need to include any surface roughness. However, the films annealed at 600 °C and 700 °C manifested extra structure above the band gap, which required the use of



DIFFICULTY DETERMINING OPTICAL BAND-GAP OF HIGH-K MATERIALS DUE TO DEFECT RELATED BAND TAIL STATES.

a second T-L dispersion in each case to fit the data adequately. This secondary structure is attributed to the formation of a polycrystalline phase due to elevated temperature. While all samples showed an extended low energy tail of the dielectric function, the tail was shorter for the two higher annealing temperatures. Comparison of the energy gap values for these films as determined by a fitting parameter identified as Eg in the T-L dispersion and also by the regression models of Tauc and of Balog gave inconsistent results. Thus a robust method for band-gap determination for such films is one of the remaining challenges in their optical characterization.

■ Developed a generalized dielectric dispersion function, called Generalized Tauc-Lorentz (GTL), to expand capability of analyzing the variety of dielectric-function shapes found from spectroscopic ellipsometry measurements of high-K dielectric films fabricated by a variety of processes. The GTL, which is Kramers-Kronig consistent, generalizes a quadratic exponent found in the Tauc-Lorentz (TL) dispersion, allowing it to have values 1 through 4, and includes one additional fitting parameter, Ep, related to the Urbach tail, that is not found in the TL dispersion. Other common dispersion functions, such as TL, Lorentz, and harmonic oscillator, are all special cases of GTL with m=2. The exponent, m, yields four different shape functions for the values 1 through 4. Initial evaluation of possible benefits of having these four shape functions were done by fitting literature data for a-silicon, Si_3N_4 and SiO. The dielectric function data for these materials were shown to be best described by GTLs with m = 2, 3, and 4, respectively. The GTL with m = 1 was found to have a shape function that is well suited to films that have a very sharp absorption edge.

■ An extensive comparison of the most advanced Quantum Mechanical CV simulators was extended in a number of aspects. A systematic comparison of QM simulators for p-channel (n-substrate) devices was performed. The number of 1D simulators in the test ensemble was extended to seven. Quantitative differences in the accumulation capacitance with ultrathin gate dielectric films were up to 20 % -similar to previously reported differences for n-channel devices. Some of the underlying physical and modeling differences leading to these differences were identified, investigated and reported; a complex interplay of a number of factors was found.

■ A method to extend the comparison to include 2D simulators was also investigated and demonstrated. A model test structure was developed, refined and calibrated for use with Medici, a commercial 2-D simulator, to insure that a quasi- 1D device was being simulated. Requests have been received for permission to use figures from this work in manuscripts, presentations and a University MOSFET class.

■ We performed an analysis of the effects of errors in physical input parameters (e.g., x-ray cross-sections, atomic form factors, electron mean free paths) on the results obtained for films

"Rudolph Technologies Inc. believes there is a significant need for ... a sub-4 nm oxide ... NIST traceable reference material."

Dr. David Leet, Director, Strategic Planning and Advanced Applications, Rudolph Technologies, Inc.

of different thicknesses. This allowed us to identify the sensitivity of the results to certain inputs. We were able to test one of these dependences experimentally on the tunable NIST beamline X-24A at the National Synchrotron Light Source. By performing the same photoemission experiment with x-rays of slightly different energies about the K excitation edge of Si, the physical performance of the same sample was dramatically changed. An extensive analysis showed that the two results for the same sample differed by 16 %, which is a good indicator of the accuracy level of the optical parameters used in the determination.

■ A suite of computer modeling tools was developed to build virtual gate stacks and simulate HRTEM micrographs from these stacks. Using these new tools, several hundred images of amorphous SiO_2 films between Si substrates were calculated, covering a range of imaging conditions and sample parameters. Combining the apparent thickness from the micrograph (measured value) and the known thickness from the model (true value) allows calculation of the accuracy as a function of the input variables. This revealed that measured thickness depends strongly on defocus and astigmatism. Using the Tcl scripting language, a graphical user interface was written to enhance the tools, improve efficiency, and simplify the database interface needed to manage the large amount of data that was generated.

■ EXAFS: The instrument at beamline X23A2 at the National Synchrotron Light Source in Brookhaven was configured in grazing incidence mode to measure 5 nm thick ZrO_2 gate dielectric films. Two series of films were measured: atomic layer chemical vapor deposited (ALCVD) films annealed at 825-900 °C in air, oxygen, nitrogen or vacuum (courtesy of J. Chang, UCLA); and spin-coated films annealed in air at temperatures of 200–800 °C (NIST). The degree of crystallinity in the films was estimated from the measured Zr-O-Zr bond angle spread $\Delta\theta^2$ in the EXAFS results. ALCVD films annealed at temperatures comparable to the thermal budget required for device fabrication (825-900 °C) exhibited the same degree of crystallinity, $\Delta\theta^2 <$ 1°, regardless of annealing atmosphere. Crystallinity in the spin-coated films decreased from $\Delta\theta^2 >$ 6° for the as-deposited films (200 °C) to $\Delta\theta^2 =$ 2-4° for films annealed above 600 °C.

■ Test samples: ZrO_2 thin films with thicknesses ranging from 2.5nm to 10 nm were deposited by spin coating metalorganic zirconium acetate-based solutions onto (100) Si wafers. Processes were developed for depositing zirconium silicate films from zirconium acetate/tetraethoxysilane and zirconium nitrate/tetraethoxysilane solutions. Silicate films with thicknesses of 10-15 nm and SiO_2/ZrO_2 ratios of 1:1 to 4:1 were fabricated; the composition of these films is being measured by EELS.

■ A systematic study of the uncertainties, sensitivity and limitations of capacitance and conductance measurements for extracting device properties and interface state density of metal-oxide-semiconductor (MOS) devices with ultra-thin (< 3.0 nm) oxides was completed. Capacitance and conductance characterization of metal-oxide-semiconductor (MOS) devices is used to determine properties such as oxide thickness, substrate doping and interface state density. However, with the advent of ultra-thin oxides, effects such as tunnel current, series resistance and quantum mechanical confinement in the substrate require additional consideration. This work provides a detailed analysis of the impact of these effects on parameter extraction using conductance and capacitance characterization of MOS devices with ultra-thin oxides.

■ Several extensive experimental investigations of the mechanisms responsible for defect generation and breakdown of thin silicon dioxide were performed. The results confirm that breakdown is directly related to the current passing through the dielectric. This confirms that the trap creation model based on energetic electrons creating damage and the statistical behavior of the number of defects at breakdown correctly describes the reliability of ultra-thin SiO_2 at both constant-voltage tunneling and substrate hot-electron conditions. Additional studies using substrate hot hole injection showed that holes are extremely effective in creating defects in the dielectric. However, these defects are ineffective in causing dielectric breakdown. These results shed doubt on the anode hole injection model for oxide breakdown.

■ A detailed investigation of the reliability of various $SiNxOy/SiO_2$ (N/O) found that an N_2O anneal of a N/O stack results in device lifetime orders of magnitude greater than SiO_2 of the same equivalent oxide thickness. The results suggest that this lifetime improvement may be due to a high critical defect density at breakdown, low defect generation rate, and low leakage current of the N_2O-annealed stack. In collabora-

tion with North Carolina State University, measurements and modeling were used to determine the impact of stacked dielectrics on charge-pumping measurements to determine interface and near interface defect densities.

■ A study was performed to investigate soft breakdown in ultra-thin silicon dioxide films and to investigate the temperature dependence of time-dependent dielectric breakdown. A more dramatic temperature dependence of wear-out was observed and raises serious reliability concerns. Thinner oxides and larger areas exhibited softer breakdown that requires the use of noise as the breakdown criteria. However, both hard breakdown and noise detection exhibited the same thermal activation. These tests provide critically important field acceleration parameters and thermal activation energies that are required for reliability extrapolation of ultra-thin oxides. Furthermore, the use of noise as a breakdown criterion was validated.

■ The increased occurrence of soft breakdown in ultra-thin SiO_2 films makes reliability characterization very difficult and necessitates the development of more sophisticated techniques to detect breakdown. The effects of stress interruption on the time-dependent dielectric breakdown (TDDB) life distributions of 2.0 nm oxynitride gate dielectric films were studied. TDDB tests using two different breakdown detection techniques were conducted at several gate voltages. Additional tests were conducted using unipolar and bipolar pulsed bias with pulse repetition frequencies up to 100 kHz to study the effects of pulsed bias on the lifetime of 2 nm films. Our results show that: (1) stress interruption longer than 1 s does not affect the defect generation and TDDB life distributions, (2) both current noise and the increase in low-voltage stress-induced leakage current (SILC) detection techniques provide similar failure statistics for ultra-thin SiO_2, (3) TDDB lifetime for ultra-thin gate dielectrics under unipolar biased stress does not substantially depend on pulse repetition frequencies less than 1 MHz, and (4) lifetime under bipolar pulsed bias is significantly improved and exhibits a dependence on pulse repetition frequency.

■ A joint collaboration between NIST and JPL investigates what effect ionizing radiation experienced in deep space missions will have on the reliability of ultra-thin gate dielectrics. It has been previously reported that heavy ion bombardment can cause radiation-induced soft breakdown (RSB) in ultra-thin gate dielectrics. Heavy ion induced soft and hard breakdown were investigated in thin gate oxides (tox≈ 3.0 nm) as a function of Linear Energy Transfer (LET), fluence, and voltage applied during irradiation. It is found that post-irradiation oxide conduction is well described by a quantum point contact model. This new work provides information about the physical nature of the soft breakdown path induced during irradiation and provides insight into the structure of the breakdown path in ultra-thin oxides induced under voltage stress.

FY Outputs

Collaborations

■ Development and characterization of 2 nm thick oxide reference materials, NC State Univ., KLA-Tencor and International SEMATECH; Measurement traceability experiments for SiO_2 and Si_3N_4 film thickness, VLSI Standards Inc. and Rudolph Technologies Inc.

■ Studies of optical, electrical and physical measurements and properties of oxynitrides and high-K dielectric films, NIST Divisions 837, 842, 852; Univ. Maryland, Univ. Minnesota, NC State Univ., Univ. Texas-Austin, UCLA, Yale Univ; IBM, Solid State Measurements, Texas Instruments, International SEMATECH.

■ Development and transfer of ellipsometer techniques and models for analysis, Penn State University and Univ. Maryland.

■ Spectroscopic ellipsometry characterization of low-K SiO_2 thin films, Division 854 and International SEMATECH.

■ We collaborated on measurements on high quality SiO2/Si samples by x-ray reflectivity at high momentum transfer at the Advanced Photon Source. The Fourier inversion of the reflectivities yields electron density with depth. Similarly, we have measured the neutron reflectivity from the same samples on a cold neutron beamline at the NIST Reactor. We are in the process of extracting mass densities from the data with depth. These determinations allow us to calibrate the electron densities and mass densities used in layer thickness fits by GIXPS, which may differ greatly in thin films from the quoted values in the literature for bulk compounds. This type of verification has not been readily available.

■ Based on simulated HRTEM micrographs at three different objective lens defocus values and three different specimen tilt angles, their results suggested (surprisingly) that minimum contrast

defocus yields more accurate film thickness measurements than Scherzer defocus, and that a 25 mrad specimen tilt was more accurate that no tilt. Also, as expected, eliminating the spherical aberration of the objective lens improves the measurement considerably. Because of their sparse sampling of the parameter space (12 simulations to characterize changes in 6 variables), they were unable to quantify the results or confirm these promising anomalies. By using hundreds of simulations chosen to systematically sample the parameter space, this work seeks to extend their result and quantitatively characterize the error of the measurement as a function of the input variables. Optimum conditions for performing gate dielectric thickness measurements can then be chosen with confidence, and the inevitable effects of experimental variation in the measurement process can be assessed and managed.

- We have demonstrated the use of a multilayer thin film stack to selectively measure the VR-SFG signal from buried interfaces through the manipulation of Fresnel factors. We expect this technique to be broadly applicable to polymer/polymer and polymer/dielectric interfaces. The study of molecular orientation at buried polymer interfaces and it influence on adhesion has been demonstrated. The influence of molecular orientation on the functional properties of a wide range of transparent media can now be explored.

- Advanced Micro Devices, ultra-thin oxide reliability (John S. Suehle)

- Analog Devices, Limerick, Ireland, ultra-thin gate oxide reliability (John S. Suehle)

- CSTL/Process Measurements Division, microhotplate-based sensor arrays (John S. Suehle and Michael Gaitan)

- Division 836, 837, 838, Roger Van Zee, et al., spectroscopic Ellipsometry of molecular electronics (Nhan V. Nguyen, Curt A. Richter, and John S. Suehle)

- Divisions 836, 837, 838, Dr. Roger van Zee et al., Molecular Electronics Competence Project (Curt A. Richter and John S. Suehle)

- Fairchild Semiconductor, ultra-thin gate oxide reliability (John S. Suehle)

- George Washington University, microhotplate-based chemical sensors (John S. Suehle)

- Lucent Technologies, ultra-thin gate oxide reliability (John S. Suehle)

- Motorola, ultra-thin gate oxide reliability (John S. Suehle)

- N.C. State University (oxynitrides, nitrides, ultra-thin SiO_2), alternative gate dielectrics (Eric M. Vogel)

- National Semiconductor, ultra-thin gate oxide reliability (John S. Suehle)

- Penn State University, ultra-thin gate oxide reliability (John S. Suehle)

- Texas Instruments, electrical and reliability characterization of ultra-thin gate oxides (John S. Suehle and Curt A. Richter)

- Texas Instruments, ultra-thin gate oxide reliability (John S. Suehle)

- The Pennsylvania State University, Molecular Electronics (Curt A. Richter and John S. Suehle)

- University of Delaware, alternative dielectrics (John S. Suehle)

- University of Maryland, College Park, microhotplate-based chemical sensors (John S. Suehle)

- University of Maryland, College Park, ultra-thin gate oxide reliability (John S. Suehle)

- University of Maryland, gate dielectric reliability (Eric M. Vogel)

- University of Minnesota, Alternate Gate Dielectrics, 6/1/01 to present (Eric M. Vogel)

Standards Committee Participation

- ASTM F-1 on Electronics, Membership Secretary and Member of Executive Subcommittee, (James R. Ehrstein)

- ASTM F-1 on Electronics, Subcommittee F1.06 on Silicon Materials and Process Control, Chairman and Ballot Coordinator (James R. Ehrstein)

- ASTM F-1 on Electronics, Subcommittee F1.06, Section B on Thin Film Characterization, Section Chair, (James R. Ehrstein)

- ITRS Conference, SEMICON West 2001, San Francisco, CA, July 13-18, 2001 (Barbara J. Belzer)

- JEDEC JC14.2 Committee on Wafer-Level Reliability, Dielectric Working Group, Chairman (John S. Suehle)

External Recognition

- Service Award from Lehighton Electronics, Inc., in recognition of his commitment and outstanding work in developing and providing NIST standard reference materials for resistivity measurement (James R. Ehrstein)

Recent Publications

Chism, W., Diebold, A., Canterbury, J., and Richter, C., Characterization and Production Metrology of Thin Transistor Gate Dielectric Films, Solid State Phenomena, vols. 76-77, pp. 177-180.

Cresswell, M. W., Arora, N., Allen, R. A., Murabito, C. E., Richter, C. A., Gupta, A., Linholm, L. W., Pachura, D., and Bendix, P., "Test Chip for Electrical Linewidth of Copper-Interconnection Features and Related Parameters, Proceedings of the 2001 IEEE International Conference on Microelectronic Test Structures," Kobe, Japan, March 19-22, 2001, Vol. 14, pp. 183-188.

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Nguyen, N. V., Richter, C. A., Cho, Y. J., Alers, G. B., and Stirling, L. A., Effects of High Temperature Annealing on the Dielectric Function of Ta_2O_5 Films Observed by Spectroscopic Ellipsometry, Applied Physics Letters, Vol. 77, No. 19, pp. 1-3.

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Thin Film Metrology Using X-rays

Technical Contact:
Richard J. Matyi

Staff-Years (FY 2001):
1 professional

Funding Sources:
STRS (70 %)
Other Agency (30 %)

Goals

To provide the semiconductor industry with high accuracy X-ray based measurement methods, reference materials, and data for the structural characterization of simple and complex thin film structures

Customer Needs

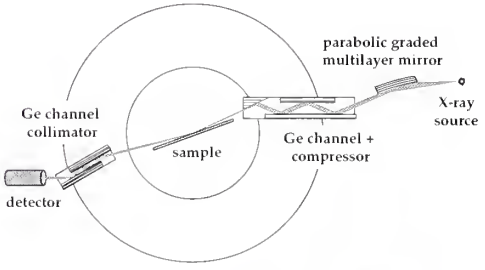
Thin film thickness, density and interfacial roughness are critical to the performance of conducting and dielectric layers in semiconductor devices. Sensitive and accurate measurement of such properties are needed in the process deveopment phase as well as in subsequent manfacturing practice. In the process development phase the needs are for structural properties that can be associated with the electrical performance characteristics of subsequently patterned device arrays. In the subsequent manufacturing phase the need is principally to calibrate the responses of on-line measurement tools that do not deliver first-principles based data. These tools have been developed to meet the needs for high measurement throughput and compatibility with the production environment. Such tools have material-dependent calibration requirements that lead end users and tool manufacturers to look for alternatives that are less sensitive to materials properties and process variability.

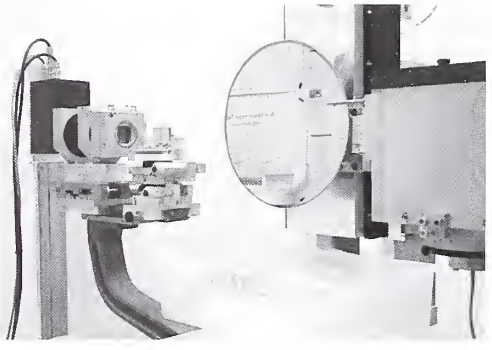
These needs are most practically addressed by the use of well-characterized reference materials whose structural properties are certified by off-line measurements using X-ray reflectivity and diffraction in conjunction with robust analysis and well-calibrated angle measurement instrumentation.

Technical Strategy

The sub-nanometer wavelengths and relatively weak interaction of X-ray probes make them a nearly ideal means for determining the geometry of the thin film and multilayer structures that underlie modern semiconductor manufacturing. Our approach has been to develop advanced metrological capability in this area including high performance instrumentation and advanced forms of modeling and analysis. We have made these capabilities available for applications to a considerable range of structural problems involving metallic interconnect layers, advanced dielectrics, and diffusion barrier films. By responding to currently urgent problems, principally, but not exclusively, mediated through ISMT, it has been possible to develop first-hand knowledge of industrial needs as well as of the level of timely responsiveness needed to provide useful input to these problems.

Our program develops and applies X-ray methods to reveal the microstructure of thin film and multi-layer structures produced by advanced semiconductor manufacturing. We also generate and certify reference structures for the calibration of in-line production tools. The main components of this work are the following: (1) Development and application of high-resolution X-ray diffraction techniques; (2) Advanced application of modeling methods to describe specular and diffuse scattering; (3) Production of reference samples of thin film and multi-layer structures; (4) Rapid response to urgent problems identified by ISMT. Both the details and the areas of emphasis of our program have evolved on the basis of this experience and guidance received during presentations to various specialized groups within the ISMT framework. Finally, we are in contact with commercial developers of X-ray instrumentation in order to facilitate interactions with customers through the



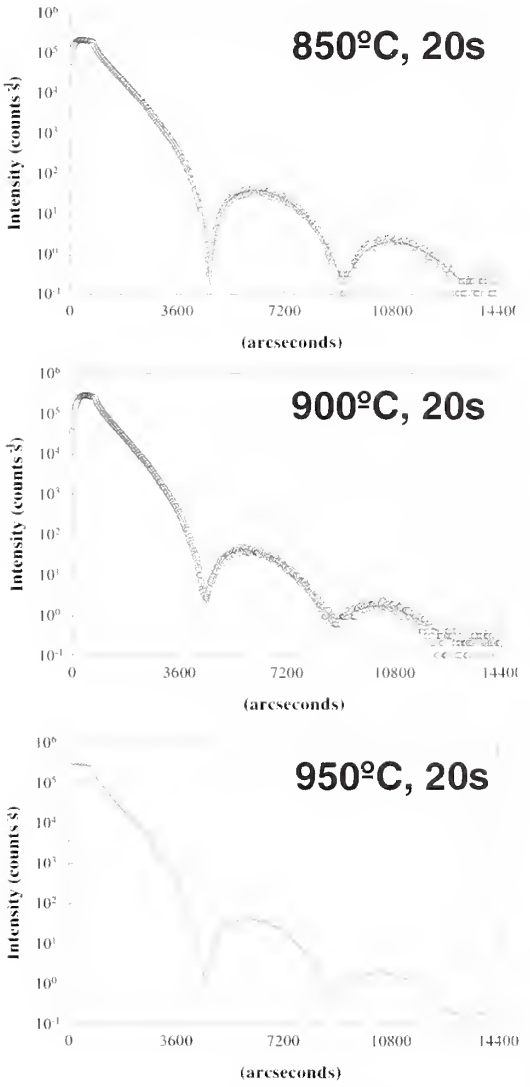


A HIGH RESOLUTION X-RAY REFLECTOMETRY SYSTEM WAS DESIGNED AND OPTIMIZED FOR THE ROUTINE ANALYSIS OF COMPLEX THIN FILM AND MULTILAYER STRUCTURES THAT ARE OF INTEREST TO THE SEMICONDUCTOR INDUSTRY

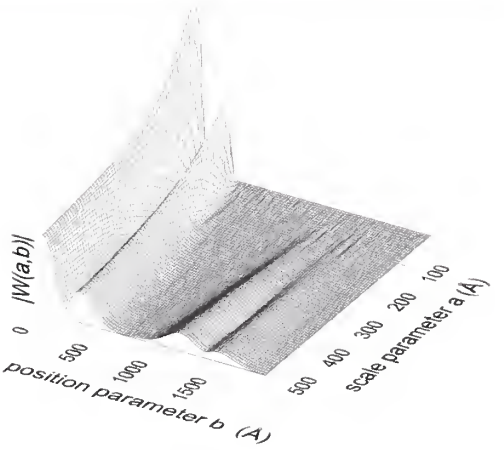
documentation of best practices and characterization of reference materials.

Accomplishments

■ High-*k* dielectric films – The structural characteristics of several HfO_2 and ZrO_2 high-*k* thin film structures were determined by high resolution X-ray reflectometry followed by computer fitting of the reflectometry scans. The HfO_2 films were well modeled by a thin SiO_2 interfacial layer, a mixed oxide $Hf_xSi_{1-x}O_2$ with $x = 0.5$, the main HfO_2 high-*k* dielectric layer, and a thin, very rough, low density HfO_2 top surface layer. The ZrO_2 layers were well described by a simpler structure consisting of an interfacial SiO_2 layer, the principal ZrO_2 layer, and a rough top low density ZrO_2 layer. The densities of both the ZrO_2 and SiO_2 were found to be considerably larger than the assumed bulk values.



A COMPARISON OF EXPERIMENTAL AND FITTED X-RAY REFLECTOMETRY CURVES FOR THIN (APPROX. 4 NM) HfO_2 FILMS AFTER RAPID THERMAL ANNEALING



THIS WAVELET-BASED ANALYSIS OF AN X-RAY REFLECTIVITY CURVE FROM A Cu/Ta/SiO_2 STRUCTURE PERMITTED INFORMATION ON ROUGHNESS AT EACH INTERFACE TO BE OBTAINED FROM SPECULAR (NOT DIFFUSE) SCATTERING DATA.

■ Wavelet-based analysis of interfacial roughness – A method for analyzing X-ray reflectivity curves from multilayered structures with interfacial roughness using a wavelet transform approach has been developed. By using this approach, we have been able (1) to extract the contribution of a particular rough interface to a specular reflectivity curve, and (2) to determine the root-mean-square amplitude of the roughness of a particular interface independently of the other interfaces in the multilayered structure from the specular reflectivity data. Analytical procedures that allow the interpretation of the wavelet coefficients obtained from specular reflectivity curves have been developed. This approach has been successfully applied to experimental reflectivity curves obtained from Cu/Ta, Ta_2O_5/Ta, and Ta_2O_5/Ta_2N bilayer structures

■ The Consortium for High-resolution X-ray Calibration Strategies (CHiXCS) – We are establishing a new industrial consortium (the Consortium for High-resolution X-ray Calibration Strategies) to better address the long term needs of users of high resolution X-ray scattering instrumentation in the semiconductor industry. Specific tasks of this Consortium will included (1) developing specified procedures for instrument and sample alignment, and quantitatively assess the effect of alignment and other systematic errors on the accuracy and precision of high-resolution X-ray diffractometry and reflectometry measurements; (2) providing to the members of the Consortium documentation regard recom-

mended best practices for performing high-resolution X-ray diffractometry and reflectometry measurements, and (3) delivering a NIST-traceable prototype calibration sample to each consortium member in a timely manner. In anticipation of the experimental work in support of CHiXCS, we have initiated (*i*) the construction of a new reflectometer that will permit closure calibration of both the sample and detector circles, and (*ii*) the re-incorporation of an optical angle interferometer onto an existing high resolution double axis diffractometer.

FY Outputs & Outcomes:

- Quantitative measurements of density, thickness, and roughness in thin film semiconductor materials.
- A knowledge base on the effects of systematic errors on the analysis of high resolution X-ray reflectometry analyses of semiconductor thin film structures.
- New wavelet-based approach for the determination of thin film structural parameters from X-ray reflectometry data.

Recent Publications

Prudnikov, I.R.; Matyi, R.J. and Deslattes, R.D., "Wavelet Transform Approach to the Analysis of Specular X-ray Reflectivity Curves," *Journal of Applied Physics*, **90**, 3338 (2001).

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Interconnect and Packaging Metrology Program

Advances in interconnect and packaging technologies have introduced rapid successions of new materials and processes. Environmental pressures are leading to the reduction and eventual elimination of lead in solder used for attaching chips to packages and packages to circuit boards. The overall task of this program is to provide critical metrology and methodology for mechanical, chemical, metallurgical, electrical, thermal, and reliability evaluations of interconnect and packaging technologies.

The function of packaging is to connect the integrated circuit to the system or subsystem platform, such as circuit board, and to protect the integrated circuit from the environment. The increasing number of input/output (I/O) on circuits with vastly larger scale of integration is forcing ever smaller I/O pitches, the use of flip chip bonding, and the use of intermediary platforms called interposers. The integration of sensors and actuators onto integrated circuits through MEMS technology and the increasing use of low cost integrated circuits in harsh environments is increasing the complexity of the packaging task. Environmental concerns are forcing the need for development of reliable lead-free solder and other low environmental impact packaging materials.

System reliability requirements demand modeling, testing methods, and failure analysis of the integrated circuits before and after packaging. Metrology is a significant component of reliability evaluation.

Measurements and Modeling of Electrodeposited Cu for ULSI

Technical Contact:
T.P. Moffat
D. Josell
G.R. Stafford

Staff-Years (FY 2001):
3 professional
1 post doc
1 guest researcher

Funding Sources:
STRS (85 %)
Other Agency (15 %)

Goals

The introduction of copper metallization and low dielectric constant materials into chip manufacture represent the most difficult interconnect challenges of modern microelectronics. Current state-of-the-art chips have interconnects, or on-chip "wiring," as narrow as 180 nm with aspect (height:width) ratios as great as five to one. The filling of such trenches with copper can currently be accomplished by electrodeposition, but roadmaps for the semiconductor industry state needs for trenches as narrow as 50 nm with a 10:1 aspect ratio. Researchers at NIST are providing the fundamental understanding required to achieve these goals. Models of the mechanism behind superfilling during copper electrodeposition and associated computational and measurement tools developed at NIST are addressing the needs of the microelectronics community and are already in use by industry.

Customer Needs

The semiconductor industry has recently shifted from the use of aluminum for interconnects, or on-chip "wiring," in integrated circuits to copper because of its lower electrical resistivity and higher electromigration resistance. Electrodeposition has been found to be the best means to deposit copper into the narrow, deep trenches used for circuitry, because "superconformal" deposition that fills very narrow trenches without porosity is possible.

An electrolytic copper linewidth of 180 nm is now the state of technology in IC fabrication. Extension to the narrower and deeper lines needed in the next generation of IC requires industrial development of new electrolytes and deposition schemes. Development of plating baths able to deposit in trenches with aspect ratios as high as 10:1 is limited by the need to do time-consuming, resource-intensive evaluations with actual nano-structures. Such experiments require microstructural characterization by FIB, SEM and TEM on an individual basis. The NIST efforts address metrology needed for superconformal deposition that minimizes this time-consuming experimental work.

Technical Strategy

The mechanism responsible for superconformal electrodeposition of copper in high aspect ratio features has been determined. Simulations from a model based on this mechanism have been shown to predict results of electrodeposition filling experiments in trenches as small as 90 nm wide and 450 nm deep. No fitting parameters are required to model this behavior. This work has built upon two recent Metallurgy Division discoveries. First, an electrolyte was developed that yields superconformal electrodeposition of copper. Second, voltage cycling induced hysteresis of copper deposition rate on flat copper specimens was shown to be indicative of the ability of an electrolyte to yield superconformal deposition. Superconformal deposition was shown to occur only when both an inhibiting additive and an accelerating additive are present in the electrolyte.

Kinetic parameters for particular electrolytes are obtained from the cyclic voltammetry described above. These kinetic parameters describe the rate at which the accelerating additive accumulates on the copper surface, displacing the inhibiting additive that retards local copper deposition. They also quantify the impact this accumulation has on the local copper deposition rate. The Curvature Enhanced Accelerator Coverage (CEAC) model of superconformal electrodeposition uses these parameters to predict filling of features. Most importantly, this model recognizes changes of local coverage of accelerator on the interface both by accumulation from the electrolyte and by changes of the local area upon which the accelerator has adsorbed. Accumulation of accelerator at the bottom of superfilling trenches is dominated by the latter, geometrical effect. Accelerator coverage on the bottoms of fine features thus increases as the surface area decreases during copper deposition. This, in turn, accelerates copper deposition there. The positive feedback cycle results in filling of the trench from the bottom upward, i.e., superconformal deposition. The finer the feature, the more important area change can be – it requires an appropriately designed electrolyte composition and appropriate deposition conditions to take full advantage of this effect.

Accomplishments

This research has resulted in accomplishments and impacts of consequence to the microelectronics industry. These are as follows:

- Explained the significance for superconformal deposition of hysteretic behavior in cyclic

current-voltage studies of deposition on flat copper substrates in an electrolyte.

- Shown how the hysteretic behavior can be modeled to extract kinetic parameters describing the rate and impact of additive accumulation on the copper/electrolyte interface.

- Developed the Curvature Enhanced Accelerator Coverage (CEAC) model that explains how accumulation of accelerator is impacted by changing area at the bottoms of fine features and how this effect causes superconformal deposition.

- Developed computer codes to predict superfilling of fine features using only the results of cyclic voltammetry studies with flat copper substrates. The most complete of these codes describes diffusion of the cupric ion and accelerator through the electrolyte, interface kinetics affecting transfer onto the copper/electrolyte interface, motion of the interface, and the impact of interfacial area change on accelerator concentration and local copper deposition rate (through the CEAC model).

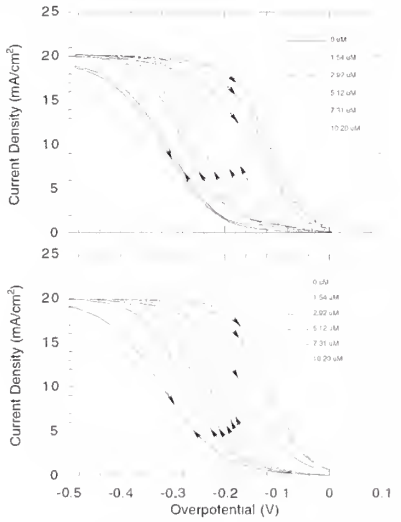

FIGURE 1. (TOP) EXPERIMENTAL CURRENT-VOLTAGE CURVES FOR COPPER DEPOSITION ON A FLAT COPPER SUBSTRATE IN ELECTROLYTES CONTAINING A DEPOSITION INHIBITING ADDITIVE PLUS VARYING AMOUNTS OF AN ACCELERATING ADDITIVE. NOTE THE HYSTERESIS AND THE SATURATION AT HIGH CONCENTRATIONS. (BOTTOM) FIT OF ACCELERATOR ACCUMULATION USED TO EXTRACT KINETIC PARAMETERS FOR THE CURVATURE ENHANCED ACCELERATOR COVERAGE (CEAC) MODEL OF SUPERFILL.

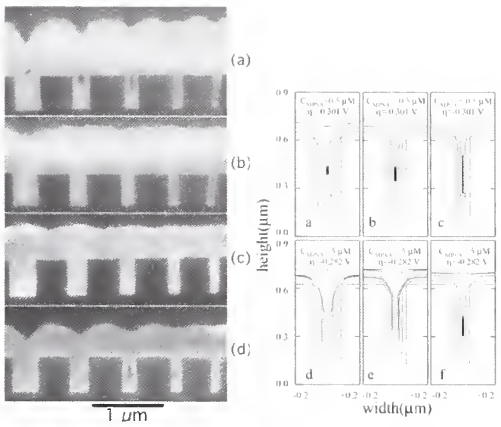

FIGURE 2 (LEFT SIDE) SUPERFILL RESULTS FOR ACCELERATOR CONCENTRATIONS OF 0, 0.5, 5 AND 40 μMOL/L (TOP TO BOTTOM). A WINDOW FOR SUPERFILL EXISTS AROUND 5 μMOL/L CONCENTRATION. (RIGHT SIDE) PREDICTIONS OF THE NEWEST COMPUTER CODE FOR THE THREE FINEST FEATURES AT 0.5 AND 5 μMOL/L (TOP AND BOTTOM). INCLUSION OF DIFFUSIONAL EFFECTS RESULTS IN VOIDS INDICATING FAILURE TO FILL. SIMPLIFICATIONS IN THE FIRST NIST MODEL OF SUPERFILL RESULTED IN SEAMS IN FEATURES THAT FAILED TO FILL.

FY Outputs & Outcomes

This information has been conveyed to U.S. industry, Academia and other National Laboratories through (8) presentations given in professional society meetings attended by industry representatives from electrolyte suppliers, analytical tool, plating tool and chip manufacturing industries. These presentations described:

- The one-to-one correlation between current-voltage hysteresis and efficacy of an electrolyte for superconformal deposition.

- The Curvature Enhanced Accelerator Coverage (CEAC) model of the mechanism behind superconformal electrodeposition.

- Comparison of experimental fill results with predictions of the computational codes based on the CEAC model.

This work has also been disseminated through:

- Refereed journal publications (3) showing the predictive power of the CEAC model by comparison of experimental filling results with two of the computational codes based on the model. These publications are already being cited in the literature by industry and academia.

- Invited talks (2) at leading electrolyte and tool manufacturers.

- Industry initiated collaboration with (1) major chip manufacturer.
- Mailing of publications to industrial and academic researchers in the field of copper electrodeposition (~50).

Recent Publications

D. Josell, D. Wheeler, W.H. Huber and T.P. Moffat, "Superconformal Electrodeposition in Submicron Features," Phys. Rev. Lett. 87, 016102 (2001).

T.P. Moffat, D. Wheeler, W.H. Huber, and D. Josell, "Superconformal Electrodeposition of Copper," Electrochem. and Solid-State Lett., 4, (4) C26 (2001).

T.P. Moffat, J.E. Bonevich, W.H. Huber, A. Stanishevsky, D.R. Kelley, G.R. Stafford, and D. Josell, "Superconformal Electrodeposition of Copper in 500-90 nm Features," J. Electrochem. Soc. 147, 4524-4535 (2000).

Stafford, G., Moffat, T., Jovic, V., Kelley, D., Bonevich, J., Josell, D., Vaudin, M., Armstrong, N., Huber, W., and Stanishevsky, A., "Cu Electrodeposition for On-chip Interconnections," Characterization and Metrology for ULSI Technology: 2000, D. G. Seiler, A. C. Diebold, T. J. Shaffner, R. McDonald, W. M. Bullis, P. J. Smith, and E. M. Secula, Eds. (AIP, New York, 2001), pp. 439-443.

Porous Thin Films Metrology for Low K Dielectrics

Goals

In this project, we are developing measurement methods of morphological characteristics in porous thin films for low-k dielectric applications. We work closely with industrial collaborators to develop and apply these methods to measurements of newly developed materials destined for integration in the next generation of integrated circuits. The unique measurement methods we apply include x-ray reflectivity (XR), small angle neutron scattering (SANS), Rutherford backscattering spectroscopy (RBS), and forward recoil elastic spectroscopy (FRES). Our efforts focus on two areas, implementing routine measurements of film thickness, coefficient of thermal expansion (CTE), moisture uptake, film connectivity, pore volume, pore size, and matrix density on films under development, and devising new measurement methods to characterize pore size distribution (PSD), pore connectivity, and matrix homogeneity.

Customer Needs

As integrated circuit (IC) feature sizes continue to shrink, new low-k interlayer dielectric materials are needed to address problems with power consumption, signal propagation delays, and cross talk between interconnects. One avenue to low-k dielectric materials is the introduction of nanometer scale pores into a solid film to lower its effective dielectric constant. However, the pore structure of these low-k dielectric materials strongly affects important material properties other than the dielectric constant such as mechanical strength, moisture uptake, coefficient of thermal expansion, and adhesion to different substrates. The characterization of the pore structure is needed by materials engineers to help optimize and develop future low-k materials and processes. Currently, there is no clear consensus among IC chip manufacturers for the selection of a class of material or a processing method of nanoporous films. Candidates include silica-based films, organic polymers, inorganic spin-on materials, chemical vapor deposited materials, and several others. With the large number of possible materials and processes, there is a strong need for high quality structural data to help understand correlations between processing conditions and the resulting physical properties.

Technical Strategy

The small sample volume of 1 μm films and the desire to characterize the film structure on silicon wafers narrows the number of available measurement methods. A novel technique has been developed using a combination of SANS, XR, RBS, and FRES to determine important structural and physical property information about thin porous films less than 1 μm thick deposited on a 1 mm substrate. These measurements are performed directly on films supported on silicon substrates so that processing effects can be investigated.

The elemental composition of the films is determined by RBS for silicon, carbon, and oxygen and FRES for hydrogen. In both techniques, a beam of high-energy ions is directed toward the sample surface. The number of scattered particles is counted as a function of their energy. Fits are performed on the scattered peaks to compute the relative fraction of each element. The atomic composition information is necessary to calculate the relative contrast factors for x-rays or neutrons.

The XR experiments are performed at grazing incident angles on a modified θ–2θ x-ray diffractometer at the specular condition. The x-ray source is a fine focus copper x-ray tube with a wavelength of 1.54 Å. The incident beam is conditioned with a four-bounce germanium monochrometer. Before the detector, the reflected beam is further conditioned with a three-bounce germanium channel cut crystal. With this configuration, reflectivity fringes can be observed from films up to 1.2 μm thick.

High-resolution XR is a powerful experimental technique to accurately measure the structure of thin films in the direction normal to the film surface. In particular, the film thickness, film quality (roughness and uniformity) and average film density can be determined with a high degree of precision. The CTE is determined from measurements of the film thickness at different temperatures.

The SANS measurements are performed on the 8 m NG1 line at NIST Center for Neutron Research. Up to 10 films are stacked to increase the SANS signal and the samples are placed in vacuum without any obstructions between the sample and the neutron detector. Scattering measurements were performed under ambient conditions to determine the structural characteristics of the pore structure.

Technical Contacts:
Barry J. Bauer
Wen-li Wu

Staff-Years (FY 2001):
3.8 professional

Funding Sources:
STRS (68 %)
Other Agency (32 %)

Measurements were also made on samples immersed in deuterated toluene, a solvent that readily wets the sample. Changes in the scattered intensity after immersion provides a measure of the percentage of pores that are interconnected and accessible to the film surface. The scattering data are analyzed using a simple random two-phase description of the film, the Debye model.

Toluene infusion XR was done on films that have been measured in vacuum in a conventional way, and then soaked in toluene for several hours. The wet samples are placed in the XR apparatus along with a container of solvent to saturate the atmosphere and to cause capillary action to fill pores of the film. The XR critical edge where adsorption first begins gives an accurate value of the average electron density and hence, the average mass density which is a combination of the walls and the pores. By comparing the results of the sample in air or vacuum with the toluene results, one can calculate the amount of toluene adsorbed, and hence the volume of open pores. Also, XR oscillations at higher angle provide a measurement of the total film thickness before and after exposure to toluene and gives a measure of the solvent resistance and rigidity of the walls.

The toluene infusion results confirm that the open pores of thin films can be filled by toluene supplied by saturated vapor and that XR can accurately measure the amount adsorbed. If the vapor pressure of the toluene or any other condensable solvent can be controlled at a partial pressure, standard porosimetry techniques may be applied to thin films. Data on the amount of solvent adsorption for a series of pressures could be converted to a PSD through the appropriate thermodynamic analysis.

The SANS technique often takes advantage of the ability to change the neutron contrast of a solvent by mixing deuterium for hydrogen versions of that solvent. This technique can be used for characterization of the porous thin films by filling the pores with various mixtures of toluene-h_8 and toluene-d_8. If the pores are accessible to the solvent and there are homogeneous walls, the wall density can be found. If the wall is heterogeneous, the average wall density could be found with information on the extent of heterogeneity also being possible. If closed pores exist that are inaccessible to solvent, closed pore porosity can be determined.

If both the XR porosimetry and the SANS contrast match techniques prove practical, a combination of the two may be possible. A match solvent mixture at controlled vapor pressures would deposit the match liquid in the pores through capillary action. SANS from the resultant films would provide an additional measure of PSD

DELIVERABLES: Measure 20 films for pore volume, pore size, and matrix density associated with IMST CRADA.

DELIVERABLES: Measure 10 films for pore volume, pore size, and matrix density for collaboration with Dow Chemical.

DELIVERABLES: Develop measurement methods and equipment for SANS contrast match technique and make measurements on ISMT samples.

Accomplishments

- A CRADA was completed with International Sematech (ISMT) in which 18 thin films were characterized for film thickness, CTE, moisture uptake, film connectivity, pore volume, pore size, and matrix density by XR, SANS, RBS, and FRES. Quarterly reports were delivered on the results and two trips were made to IMST to discuss the findings.

- A CRADA was completed with Rohm & Haas in which 4 thin films were characterized for film thickness, CTE, moisture uptake, film connectivity, pore volume, pore size, and matrix density by XR, SANS, RBS, and FRES. A trip was made to Rohm & Haas to discuss the findings.

- A new measurement method has been implemented that utilizes infusion of toluene into the open pores of a film by placing the film into a controlled atmosphere of saturated toluene vapor. All of the connected open pores become filled with liquid toluene through capillary action. The critical edge measured by XR is used to calculate the total mass density and, hence, the total amount of adsorbed solvent and open pore content. This method allows calculation of the total open pore porosity that can be compared to the total combined open and closed pore porosity that is measured by the previous method that uses a combination of XR, SANS, RBS, and FRES.

- A contrast match method was developed to provide an independent SANS measurement of pore volume, pore size, and matrix density as well as pore connectivity, and matrix homogeneity. A new SANS cell was designed and constructed that causes solvent adsorption in the pores of thin films by using saturated solvent vapor. A device was constructed to deliver saturated vapor of mixtures of toluene-h_8 and

toluene-d_8 at any preprogrammed ratio. The films in the SANS cell become saturated by the vapor and the pores become filled. Several solvent ratios are used and the SANS results of the saturated films along with SANS of the films in vacuum are used to calculate the exact match composition. The match composition is used to calculate the mass density of the matrix material and closed pores. This matrix density measurement is independent of the method that uses toluene infusion XR. The contrast match method offers improved accuracy of the final measured parameters. The matrix heterogeneity and the closed pore content can also be determined by the contrast match method.

FY Outputs & Outcomes

- Two CRADAs were established with ISMT and Rohm & Haas. A total of 22 thin films were characterized for film thickness, CTE, moisture uptake, film connectivity, pore volume, pore size, and matrix density by XR, SANS, RBS, and FRES. Four quarterly reports were delivered on the results and two trips were made to IMST to discuss the findings and a trip was made to Rohm & Haas.

- Five papers have been published in archival journals, four in proceedings on the techniques developed at NIST. A book chapter has been written and is in press. Four presentations have been given at Industrial locations and two invited talks have been given at National Meetings.

Collaborations and Support

- ISMT Jeffrey T. Wetzel, Changming Jin, Jeffrey Lee
- Rohm & Haas – Nick Pugliano
- Dow Corning – Brian Landes
- Lucent - Shu Yang
- Dow Corning - Wei Chen, Eric Moyer
- IMEC - Mikhail Baklanov
- Sandia National Laboratory - Hongyou Fan, C. J. Brinker
- University of Michigan - David Gidley

Recent Publications

Bauer, B.J., Lin, E.K., Lee, H. Wang, H. and Wu, W., "Structure and Property Characterization of Low-k Dielectric Porous Thin Films," J. Electronic Materials, 30(4), pp. 304 (2001).

Wu, W. L.; Wallace, W. E.; Lin, E. K.; Lynn, G. W.; Glinka, C. J.; Ryan, E. T., and Ho, H. M., "Properties of Nanoporous Silica Thin Films Determined by High-Resolution X-Ray Reflectivity and Small-Angle Neutron Scattering," Journal of Applied Physics, 87(3):1193-1200 (2000).

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Lee, H. J., Lin, E. K., Wu, W. L., Fanconi, B. F., Liou, H. C., Lan, J. K., Cheng, Y. L., Wang, Y. L., Feng, M. S., and C. G. Chao, "X-ray Reflectivity Measurements of N_2 Plasma Effects on the Density Profile of Hydrogen Silsesquioxane Thin Films," *J. Electochem. Soc*,*148*, F195 (2001).

Kohdoh, E., Baklanov, M. R., Lin, E. K., Gidley, D. W., and A. Nakashima, "Comparative Study of Pore Size of Low-Dielectric Constant Porous Spin-on-glass Films with Different Ways of Nondestructive Instrumentation," *Japanese Journal of Applied Physics*, *40*, L323 (2001).

Bauer, B. J.; Lee H. J.; Hedden, R. C.; Liu, D. W.; and Wu, W. L. "Pore Size Distributions in Low-k Thin Films by X-ray Reflectivity and Small Angle Neutron Scattering," Proceedings of Ultra Low k Workshop (2001).

Lee, H. J., Lin, E. K., Wang, H., Wu, W. L., Chen, W., and T. A. Deis, "Characterization of Porous Low-k Dielectric Thin Films Using X-ray Reflectivity and Small-angle Neutron Scattering," *Proceedings of IITC 2001*, (2001) in press.

Lin, E.K., Lee, H. J., Wang, H., and Wu, W. L., "Structure and Property Characterization of Low-k Dielectric Porous Thin Films Determined by X-ray Reflectivity and Small-Angle Neutron Scattering," Proc. of the 2000 Intl. Conf. on Characterization and Metrology for ULSI Technology (2000).

Lin, E. K., Wu, W. L., Jin, C., and Wetzel, J. T., "Structure and Property Characterization of Porous Low-k Dielectric Constant Thin Films Using X-ray Reflectivity and Small-angle Neutron Scattering," Proc. of the Materials Research Society Meeting. (2000).

Interconnect Dielectric Characterization Using Transmission-Line Measurement

Technical Contact:
Michael Janezic
Dylan Williams

Staff-Years (FY 2001):
0.25 professional

Funding Sources:
STRS (70 %)
Other (30 %)

Goals

We develop and disseminate methods to accurately measure the high-frequency dielectric properties of low-k thin films from easy-to-perform in-situ transmission-line measurements. This project brings together the NIST Electromagnetic Properties of Materials Program and the NIST High-speed Microelectronics Program into a collaborative effort with International SEMATECH and manufacturers of low-k materials to develop methods for determining the dielectric properties of low-k thin films.

In this work, MMIC probing techniques are used to measure the capacitance and conductance per unit length of small printed transmission lines in which the materials to be characterized are incorporated. The dielectric constant of the dielectric thin films and the conductivity of the metals used in the lines construction are subsequently derived over broad frequency ranges.

Customer Needs

In order to improve the electrical performance of interconnects, the semiconductor industry is replacing traditional silicon dioxide thin films with lower permittivity (low-k) thin films. Reducing the permittivity of the dielectric separating the interconnects decreases the parasitic capacitive effects. As a result, smaller interconnects that operate at higher frequencies are feasible. Although many candidate low-k thin film materials exist, the permittivity of many of these new materials remains relatively unknown, especially at high frequencies.

The 1999 Semiconductor Industry Association's (SIA) International Technology Roadmap for Semiconductors identifies the development and characterization of low-k dielectrics as a critical component in the drive to increase processor performance. In the Critical Interconnect Measurement Needs Summary on page 309, it states, "Design of interconnect structures requires measurement of the high frequency dielectric constant of low-k materials."

Technical Strategy

Our primary goal is to continue to develop and disseminate the measurement methodology based on single transmission line measurements for determining the dielectric constant of low-k thin films. An important component of this is to provide measurement services to the semi-

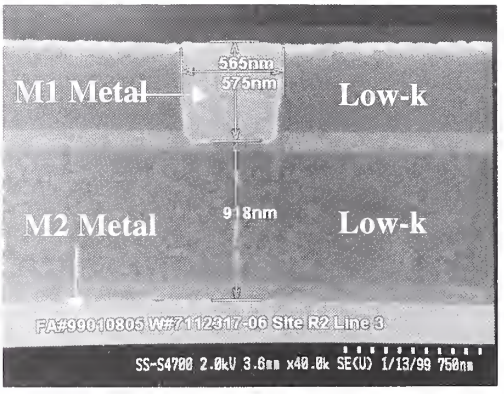


FIGURE 1 TYPICAL CROSS-SECTION OF A MICROSTRIP TRANSMISSION LINE INCORPORATING A LOW-K THIN FILM.

conductor industry to enable them to evaluate the high-frequency electrical performance of new low-k materials.

Another important issue related to interconnect performance is the possible anisotropy of new low-k materials. To address this issue, we have designed coupled, transmission-line test structures that incorporate the low-k thin film. Broadband measurements of these structures, in addition to the single, transmission-line test structures will allow us to calculate the permittivity of the low-k material as a function of the electric field orientation. An added benefit of characterizing the coupled transmission lines is that they will also provide information about the overall electrical behavior of adjacent interconnect lines.

DELIVERABLES: Improve accuracy and extend frequency range of permittivity measurements using single transmission lines.

In collaboration with International SEMATECH, we are designing a new set of microstrip transmission-line test structures that will enable us to improve the measurement accuracy. In addition to designing new test structures, we have also upgraded our on-wafer network analysis equipment to extend our frequency range to 110 GHz.

DELIVERABLES: Disseminate measurement method to industry.

Through publications, measurement software and presentations at International SEMATCH

Technical Advisory Boards, we are providing the semiconductor industry the necessary tools to determine the electrical characteristics of low-k thin films.

DELIVERABLES: Provide measurement services to low-k material manufacturers.

With expertise in on-wafer network analysis and material characterization, we can offer and independent and unbiased measurements services to low-k material manufacturers.

DELIVERABLES: Design and fabricate coupled transmission-line test structures for evaluation of low-k dielectric anisotropy and electrical performance of adjacent interconnect lines.

In collaboration with International SEMATECH, we are developing a method to measure possible anisotropy of low-k thin films. Although measuring the electrical properties of the thin-films is the primary focus, we will also be able to provide measurements on the electrical behavior of coupled interconnects.

Accomplishments

- Low-k Material Measurements – In collaboration with International SEMATECH, we measured the dielectric constant of various candidate low-k thin films over a frequency range of 50 MHz to 40 GHz using transmission-line test structures. An example of a typical test structure cross-section is shown in Figure 1. We show in Figure 2 dielectric constant results for a few of the different classes of low-k materials we characterized.

- Four-port Microwave Probe Station Construction – The High-Speed Microelectronics Project constructed a four-port microwave probe station including automated measurement software. With this probe station and software, we will be able to characterize the properties of coupled interconnect lines, including the dielectric properties of the low-k thin film separating the coupled lines.

- Microwave Probe Station Upgrade – We upgraded our microwave probe station and acquired a high-frequency network that will enable us to perform dielectric constant measurements from 50 MHz to 110 GHz. In addition to a larger frequency range, the microwave probe station has an environmental chamber that will allow us to make dielectric constant measurements as a function of temperature and humidity.

- Coupled Tranmission-Line Test Structures – In collaboration with International SEMATECH, we have designed a set of coupled transmission-line test structures. These structures will enable us to determine the level of anisotropy of low-k thin films as well as provide valuable data on the electrical performance of adjacent interconnect lines.

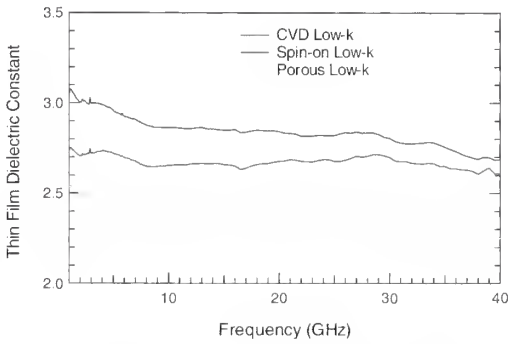


FIGURE 2 DIELECTRIC CONSTANT MEASUREMENTS OF LOW-K THIN FILMS.

FY Outputs & Outcomes

- Low-k Dielectric Constant Measurement Service – Using NIST-designed transmission-line test structures fabricated at International SEMATECH, we characterized the dielectric constant of low-k thin films from 50 MHz to 40 GHz for low-k material manufacturers.

- Publication of Low-k Measurement Method – In an effort to disseminate the low-k dielectric constant measurement method to the semiconductor industry, we authored a paper outlining the measurement technique. The paper has been accepted for publication in the IEEE Transactions on Microwave Theory and Techniques and will be published in 2002.

- International SEMATECH Collaboration- We continued working very closely with International SEMATECH in the area of low-k dielectric characterization. In concert with low-k material manufacturers, they continued to fabricate test structures to NIST for high-frequency dielectric characterization of low-k thin films.

Recent Publications

M. D. Janezic, D.F. Williams, V. Blaschke, A. Karamcheti, C. S. Chang, "Permittivity Characterization of Low-k Thin Films from Transmission-line Measurements" (accepted by IEEE Transactions on Microwave Theory and Techniques).

U. Arz, D.F. Williams, D.K. Walker, H. Grabinski, "Accurate Electrical Measurement of Coupled Lines on Lossy Silicon,"

9th Topical Conference on Electrical Performance of Electronic Packaging, pp. 181-184, Oct. 23-35, 2000.

D.F. Williams, J. E. Rogers, C.L. Holloway, "Multiconductor Transmission-Line Characterization: Representations, Approximations, and Accuracy," IEEE Transactions on Microwave Theory and Techniques, vol. 47, no. 4, pp. 403-April 1999.

D. F. Williams, M. D. Janezic, A. Ralston, S. List, "Quasi-TEM model for coplanar waveguide on silicon," 1997 EPEP Conference Digest, pp. 225-228, Oct. 27-29, 1997.

M. D. Janezic and D. F. Williams, "Permittivity Characterization from Transmission-Line Measurement," IEEE International Microwave Symposium Digest, vol. 3, pp. 1343-1345, June 10-12, 1997.

Wire Bonding to Cu/Low-k Semiconductor Devices

Goals

To develop the best, most economical, practical bonding surface(s)/sub-surface support structures and techniques for wire bonding to advanced semiconductor devices with copper metallization and to resolve metallurgical diffusion issues that relate to these surfaces and structures.

Customer Needs

The U.S. semiconductor industry needs to broadly implement copper intraconnections on the chip to maintain our competitive world position. Wire bonding is the dominant method of interconnecting the chip to the package. The work in this program is being developed in collaboration with ISMT. Through its consortial interactions, ISMT is uniquely able to provide the appropriate material samples (wafers, etc.) for the experimental work. In addition, NIST is able to supply new types of plating materials for evaluating the deposition processes and measurement techniques used therein.

"George Harman is the author of *Wire Bonding in Microelectronics* and an internationally acclaimed expert in the area of wire bonding and packaging of semiconductor chips. His current work with in collaboration with ISMT on the leading edge technology of wire bonding to advanced copper/Lo-K chips and measurements of temperature during wirebonding is critically important to advancing the industry." Michelle Rasco and Rod Auger, ISMT.

Technical Strategy

The highest priority is to determine the optimum (bondable/protective) metal surface to place on top of the copper pad. Gold plating, electro/electro-less is considered the best (a two step deposition system is being developed), but diffusion of the base copper can limit its usefulness. The literature has contradictions as to diffusion coefficients, and they can vary, depending upon the impurities in both the copper and the gold. Measurements will be made on samples similar to those used in the industry. Other top metal (inorganic) surfaces will also be evaluated. As appropriate, such evaluations will be made using Auger and other measurement techniques available at NIST. Verification will be carried out by wire bonding bondability experiments. A new approach is also being pursued in which copper pads are protected with a thin (50 Å) layer of inorganic material (patent applied for). ISMT is cooperating by supplying Cu LoK wafers with specially prepared copper surfaces for bonding experiments.

Accomplishments

- A paper entitled Wire Bonding To Advanced Copper-Low-K Integrated Circuits, the Metal/Dielectric Stacks, and Materials Considerations was given (and published) at the 2001 IMAPS Symposium and won an award as an outstanding paper. Also a paper at the same Conference entitled: A Wire Bond Temperature Sensor was given and published.

- A two-step gold-on-copper deposition system was developed and testing has begun.

FY Outputs & Outcomes

- G.G. Harman, and C.E. Johnson, "Wire Bonding to Advanced Copper-Low-K Integrated Circuits, the Metal/Dielectric Stacks, and Materials Considerations," International Microelectronics Symposium (IMAPS), October 9-12, 2001.

Technical Contact:
G. Harman
D. Kelley
C. Johnson

Staff-Years (FY 2001):
2 professional
1 Technician

Funding Sources:
STRS (100 %)

Solders and Solderability Measurements for Microelectronics

Technical Contact:
Frank W. Gayle, MSEL

Staff-Years (FY 2001):
2 professionals
1.2 guest researchers

Funding Sources:
STRS (100 %)

"As a result of NIST's involvement, I feel NEMI has been successful in responsibly leading the effort to understand the implications of lead-free assembly in a way that is benefiting the entire electronics assembly industry."

-- Edwin Bradley, Motorola and National Electronics Manufacturing Initiative

"NIST personnel brought unique skills and expertise to both NCMS projects [Lead-Free Solder Project, and Lead-Free High Temperature Fatigue Resistant Solder Project]. Without the support from NIST, both these projects would have extended over a longer period of time and would have been more costly to the project's industrial partners. In the case of the Lead-Free Program, a critical evaluation of the data would not have been done without NIST's leadership."

-- Duane Napp, Program Manager, National Center for Manufacturing Sciences

Goals

Solders and solderability are increasingly tenuous links in the assembly of microelectronics as a consequence of ever shrinking chip and package dimensions and the movement toward environmentally friendly lead-free solders. As a result, the goal of this project is to provide data and materials measurements of critical importance to solder interconnect technology for microelectronics assembly.

Customer Needs

The U.S. microelectronics industry has clearly articulated the measurement needs for Pb-free solders and for solderability and assembly. For example, the urgency for materials data for Pb-free solders has been specified in the 1997 IPC, 1999 ITRS, 2000 NEMI, and 2000 IPC Lead-Free Solder Roadmaps. The pressure from the Japanese consumer product market and from the European Union to produce lead-free microelectronics continues to increase. In addition, the lack of understanding and control of current standard solderability measurements has inhibited the development of improved measurements necessary for new solders and for new packaging schemes. These industrial needs are addressed under this NIST project.

Technical Strategy

We are providing the microelectronics industry with measurement tools and data to address solder interconnect problems. A thermodynamic database has been publicly distributed for modeling lead-free solder systems. We also work closely with industry groups on measurement tools needed for development of lead-free solders for use in harsh environments, and provide guidance for adoption of these solders into assembly processes through work with industrial standards organizations.

We will continue working with the NEMI consortium to establish suitability of particular lead-free solder compositions. In addition, solderability tests will be developed working with the IPC lead-free solder sub-committee. Databases for phase diagrams and thermodynamics critical to solder development and for mechanical properties of solder will be expanded and distributed via the web. In addition, a much needed guide to interpretation of thermal analysis data will be produced.

DELIVERABLES: Develop wetting balance test procedure to modify industry standard (IPC/EIA-J STD-002A). March 2002.

DELIVERABLES: Perform wetting balance tests for the IPC solderability task group pilot study on Pb-free surface finishes and components. (FY02 IPC solder study).

DELIVERABLES: Add Sb-containing systems to the current thermodynamic database (Sn-Ag-Bi-Cu-Pb) for solders. March 2002.

DELIVERABLES: Develop an easy-to-use interface for phase equilibria software for the calculation of liquidus temperature, lever rule equilibrium and Scheil solidification. June 2002.

DELIVERABLES: Expand pages for phase diagram Metallurgy Division Webbook with emphasis on solder alloys. Add pages for constituent binary and ternary systems containing Sb. June 2002.

DELIVERABLES: Make simple phase equilibria software available for interactive use; make more complex programs available for downloads. Sept. 2002.

DELIVERABLES: Prepare draft Best Practice Guide for Differential Thermal Analysis Sept. 2002.

Accomplishments

- NIST has taken a major role working with industry through a NEMI Task Force to identify and move Pb-free solders into practice. NIST co-chairs the NEMI alloy selection group which selected standard alloy compositions for U.S. microelectronics assembly. NIST is also active in the NCMS High Temperature Fatigue Resistant Solder Consortium and, as in the NEMI Task Force, led the alloy selection task group. The NCMS consortium, including Ford, Delphi, Allied Signal, Rockwell, Amkor, Heraeus, Johnson Manufacturing, and Indium Corporation, has identified and thermally cycle tested several Pb-free alloys for applications as high as 160 C. In the past year NIST has been responsible for analyzing microstructure evolution during thermomechanical fatigue.

- NIST has developed the database necessary to calculate multicomponent phase diagrams essential for Pb-free alloy development. The experimental determination of phase diagrams is a time-consuming, costly task requiring expert

interpretation of results. The calculation of phase diagrams significantly reduces the effort required to determine phase evolution in multicomponent systems and can provide quantitative information that is frequently needed in other modeling efforts. During the past year the NIST thermodynamics database for solders was expanded. Of particular importance is the development of a refined thermodynamic description for the Sn-rich part of the Sn-Ag-Cu system that was critical for alloy selection by the NEMI Lead-Free Task Force.

- We are also working in collaboration with IPC Standards Committees (most closely with members from Celestica, Lucent, Raytheon, Rockwell, and Shipley-Ronel) to establish reproducible solderability test standards for board assembly. Activities include providing benchmark experiments for the wetting balance tests to predict on-line solderability for a wide range of surface finishes, lead materials, and solder alloys. New NIST research to develop electrochemical solderability tests and an understanding of whisker formation in Sn-based, Pb-free electroplated surface finishes complements the solderability studies.

- NIST was also active in the NCMS High Temperature Fatigue Resistant Solder Consortium, including eight companies in the microelectronics and automotive industries, which completed a four-year project this year to develop Pb-free solders for harsh environment applications, such as automotive and telecommunications. NIST lead the alloy selection task group and took the lead in developing final conclusions and writing the final report, published in August 2001 on CD-ROM.

FY Outputs & Outcomes

- Sources of uncertainty have been established for wetting balance solderability tests, leading to increased repeatability and reproducibility of tests.

- Recent flux studies performed at NIST have led to a change in test procedures for the IPC J-ANSI solderability standard.

- Presentation voted one of the 5 best papers out of 58 presented at the TMS 2001 Annual Meeting, Symposium on "Recent Progress in Pb-Free Solders and Soldering Technologies."

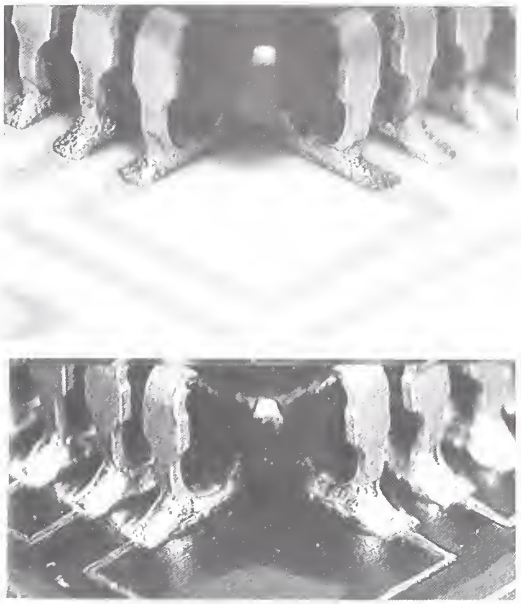


FIGURE 1. PLASTIC LEADED CHIP CARRIERS ON CERAMIC AND POLYMERIC SUBSTRATES ASSEMBLED WITH PB-FREE SOLDERS AND SURFACE FINISHES.

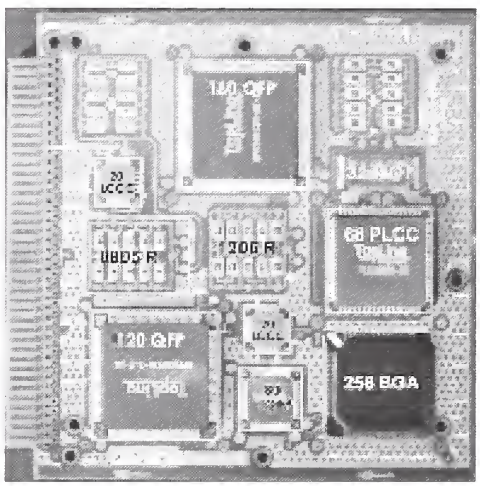


FIGURE 2. RELIABILITY TEST VEHICLE USED TO TEST MANUFACTURABILITY AND THERMAL FATIGUE RESISTANCE OF A VARIETY OF SURFACE MOUNT COMPONENTS ON PRINTED CIRCUIT BOARDS.

Recent Publications

Gayle, F. W., Fatigue-Resistant, High Temperature Solder, Adv. Mater. Process., **159** (4) 43-44 (2001).

Gayle, F. W., Becka, G., Syed, A., Badgett, J., Whitten, G., Pan, T.-Y., Grusd, A., Bauer, B., Lathrop, R., Slattery, J., Anderson, I., Foley, J., Gickler, A., Napp, D., Mather, J., and Olson, C., Lead-free High-temperature Fatigue-resistant Solder, final report, NCMS, August 2001 (published as CD-ROM).

Gayle, F. W., Becka, G., Syed, A., Badgett, J., Whitten, G., Pan, T.-Y., Grusd, A., Bauer, B., Lathrop, R., Slattery, J., Anderson, I., Foley, J., Gickler, A., Napp, D., Mather, J., and Olson, C., High Temperature Lead-free Solder for Microelectronics, Proceedings of The 4th Pacific Rim Conf. on Adv. Materials and Processing, Honolulu, HA (2001) in press.

Gayle, F. W., Becka, G., Syed, A., Badgett, J., Whitten, G., Pan, T.-Y., Grusd, A., Bauer, B., Lathrop, R., Slattery, J., Anderson, I., Foley, J., Gickler, A., Napp, D., Mather, J., and Olson, C., High Temperature Lead-free Solder for Microelectronics, JOM, **53** (6) 17-21 (2001).

Kattner, U. R. and Handwerker, C. A., Calculation of Phase Equilibria in Candidate Solder Alloys, Z. Metallkd., **92** (7) (2001).

Moon, K. W., Boettinger, W. J., Kattner, U. R., Biancaniello, F. S., and Handwerker, C. A., Experimental and Thermodynamic Assessment of Sn-Ag-Cu Solder Alloys, J. Electron. Mater., **29** (10) 1122-1136 (2000).

Moon, K. W., Boettinger, W. J., Kattner, U. R., Biancaniello, F. S., and Handwerker, C. A., The Ternary Eutectic of Sn-Ag-Cu Solder Alloys, Proceedings of 2000 SMTA Conference, Edina, MN, Surface Mount Technology Assoc, 941-944 (2000).

Moon, K. W., Williams, M. E., Johnson, C. E., Stafford, G. R., Handwerker, C. A., and Boettinger, W. J., The Formation of Whiskers on Electroplated Tin Containing Copper, Proceedings of The 4th Pacific Rim Conf. on Adv. Materials and Processing, Honolulu, HA (2001) in press.

Moon, K. W., Boettinger, W. J., Kattner, U. R., Handwerker, C. A., and Lee, D. J., The Effect of Pb Contamination on the Solidification Behavior of Sn-Bi Solders,î J. Electron. Mater., **30** 45-52 (2001).

J. Bath, C. Handwerker, and E. Bradley, "NEMI Group Recommends 'Standardized' Lead-Free Solder Alternative," Circuits Assembly (2000).

C. Handwerker, R. Noctor, and G. Whitten, "Reliability of Lead-Free Solders," published in Lead-Free Solders, Ed. Jennie S. Hwang (2000).

Interconnect Materials and Reliability Metrology

Technical Contact:
David T. Read
Michael Gaitan

Staff-Years (FY 2001):
3.2 professional
2 student

Funding Sources:
STRS (100 %)

Goals

The objectives of this project are: (1) to develop experimental techniques to measure the reliability-related properties of thin films, including basic tensile properties, elastic modulus by both static and dynamic means, residual stresses, fatigue, fracture resistance, and electromigration and stress-voiding resistance, in specimens fabricated and sized like materials used in actual commercial devices; (2) to advance the ability to anticipate and meet thin interconnect reliability challenges by relating thin film reliability to microstructure and by developing understanding of the relationships between various modes of thin film failure, for example, electromigration and mechanical fatigue.

Customer Needs

Thin films are an essential component of all advanced electronic devices. Interconnect structures built up on ULSI microchips consist of 7 thin-film layers now, and will soon reach 9 layers (*International Technology Roadmap for Semiconductors, 2000 Update*, Interconnect, Table 46a). These structures are fabricated using adjacent layers of materials with very different thermal expansion coefficients, exotic materials such as nanoporous low-k dielectric, and operate at ever higher temperatures. According to the *Roadmap (1999)*, "Computer-aided design (CAD) tools will need to incorporate contextual reliability considerations in the design of new products and technologies. It is essential that advances in failure mechanism understanding and modeling, which result from the use of improved test methodologies, be used to provide input data for these new CAD tools. With these data and smart reliability CAD tools, the impact on product reliability of design selections can be evaluated." The National Electronics Manufacturing Initiative (NEMI) Roadmap of December 2000 reports a similar need. A section on pages 227-228 entitled "Key Simulation Prerequisites" states that "Laboratory infrastructure/experimental expertise is essential for both model verification as well as property input evaluations, to have truly effective simulations." A following subsection lists critical simulation areas. Listed first is "Reliability-Mechanics-Physics of Failure (POF), and associated Mechanical Analysis and Design." The message is clear: understanding and modeling of mechanical performance and potential failure modes in these devices require knowledge of the mechanical behavior of the films. This issue of mechanical modeling is likely to increase in significance with the growing integration of interconnect between the chip and the package, with their disparate material sets.

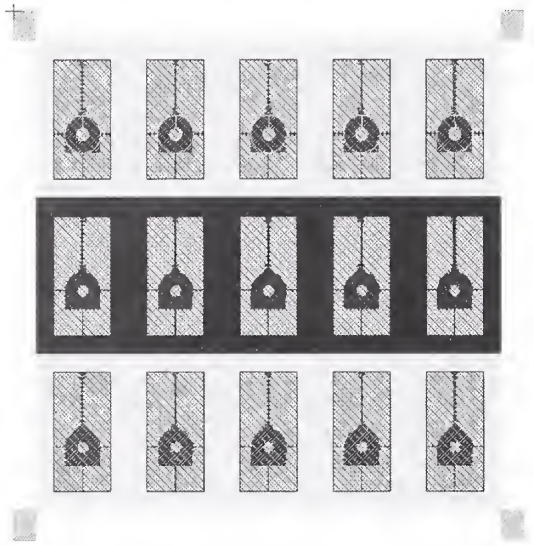
Because the films are formed by physical vapor deposition, their microstructures, and hence their mechanical properties, are quite different from those of bulk materials of the same chemical composition. While the general principles of conventional mechanical testing are applicable to thin films, conventional test equipment and techniques are not. Because vapor-deposited films are of the order of 1 μm thick, the failure loads are of the order of gram-forces or less, and the specimens cannot be handled directly. So, techniques specific to films on silicon substrates are needed. Developing test methods must eventually become applicable to test structures that can be included in production or development wafers, so that applicability to 'real' materials can be demonstrated. The intent of our goal of testing specimens similar in size to structures on actual production devices is to maximize the relevance of our results.

Technical Strategy

We are developing a variety of measurement techniques to provide material property data on interconnect materials. In testing and exercising these techniques, we develop data that are valuable in themselves, and we also develop our understanding of the relationship between the observed behavior and the microstructure, as influenced by processing conditions specific to the specimen material at hand.

We study individual thin films and multilayer interconnect structures on silicon substrates, both obtained from industry and fabricated by researchers within NIST and elsewhere. Specimens of CMOS structures have been obtained through the MOSIS service run by UCLA. Occasionally, wafers or fabricated specimen geometries are received directly from our counterparts in industry. Some of our techniques require the removal of the silicon substrate beneath the test structure itself, to a depth of up to 50 μm. We have developed dry etching systems that use xenon difluoride to carry out these processes.

Measurement capabilities operating within this project include microtensile testing and DC and AC electromigration measurements. Resonant structure measurements will soon go on line. We have developed the silicon-frame tensile



TEST CHIP PRODUCED IN THE 1.2 MM AMI CMOS PROCESS AVAILABLE THROUGH THE MOSIS SERVICE.

specimen and the piezo-actuated tensile tester, which operate successfully for specimens 100 μm wide and larger. We have continued to support one such apparatus at NIST and one at Motorola in Tempe. Another, which uses a different control software, exists at the University of Colorado at Boulder. Because problems were encountered with specimens narrower than 100 μm, a new technique, called the force-probe tensile test technique, has been developed. The apparatus includes a tensile loading system operable within the scanning electron microscope (SEM). This system has now been used on specimens as small as 2 μm wide. It is anticipated that the magnification of the SEM will allow testing even narrower specimens.

Our measurements on AC electromigration are intended to develop better understand the processes of stress- voiding and the effects of electromigration in actual circuits. To date we are exploring the low-frequency domain, typically 100 Hz.

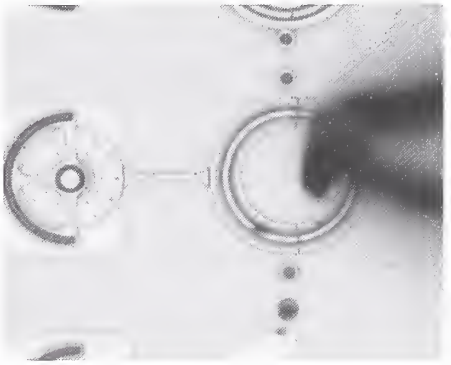
We are developing resonant measurements for cantilevers patterned from interconnect materials. The resonant frequency of these is related to the Young's modulus, the density, and the geometry of these cantilevers. These structures can be fabricated simultaneously with free fixed-fixed and fixed-free cantilevers used in a related, static method for measuring through-film average residual strain and strain gradient. With the residual strains, from the static method, and the elastic constant, from the dynamic method, the residual stress and its gradient can be calculated.

DELIVERABLES: Our results are being disseminated in conference presentations and peer-reviewed articles in archival journals, as well as in presentations and written reports to the organizations that have supplied specimens.

Accomplishments

- Progress in recent years on measurements of the mechanical behavior of thin films has put us in the position of starting to be able to make various kinds of critical comparisons among our results: results for the same materials in different laboratories; results for similar materials from different sources; and results for the same property by different measurement methods. These comparisons are necessary to reach our goals of providing accurate and believable measurement techniques and an understanding of the results.

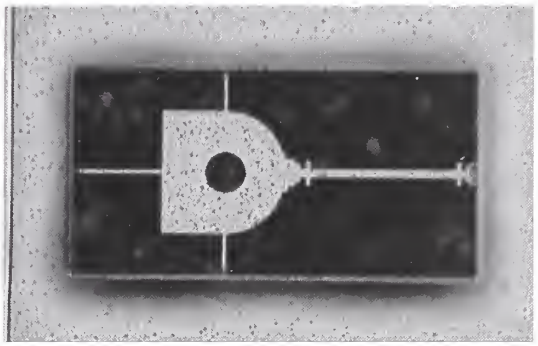
- In fiscal 2001 we reported the severe effect of specimen geometry on the tensile elongation of pure e-beam deposited aluminum. Changing to a much narrower specimen raised the elongation from around 1 % to over 20 %. This result highlights the necessity of standardized geometry in tests used to compare different materials. Several advances in the utilization of our new force-probe technique were made in fiscal 2001 but have not yet been reported publicly. These include successful testing of a polymer, photodefinable polyimide, and of a hard, brittle material, polysilicon. These results demonstrate the wide applicability of the force-probe technique.



RING-PULL SPECIMEN OF POLYSILICON MADE BY SANDIA NATIONAL LABORATORIES TESTED USING THE NIST FORCE-PROBE TECHNIQUE.

- Another milestone reached in fiscal 2001 was the successful testing of a film that had been produced as part of commercial fabrication process, specifically, metal 2 and metal 1-2 composite specimens of CMOS aluminum contact material.

The layout is shown above. The contact material picks up a significant silicon content during the anneal, and so it is not surprising that this material has properties that are significantly different from pure aluminum.

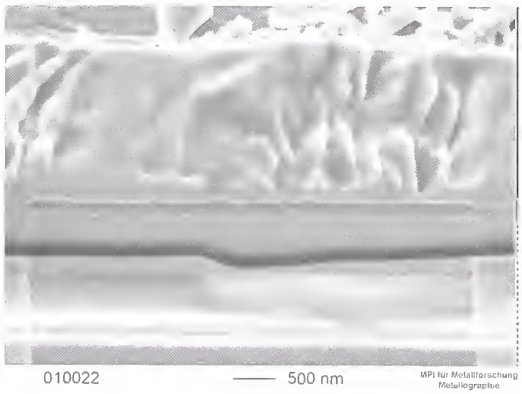


MICROTENSILE SPECIMEN ON CMOS CHIP OBTAINED THROUGH THE MOSIS PROCESS. THE SLENDER STRIP ON THE RIGHT IS THE TEST SECTION. IT IS 10 MM WIDE BY ABOUT 200 MM LONG.

■ This material had very low elongation, and also very low tensile strength. Its elastic stiffness was difficult to measure because the strength was so low, but it appears to be well above that of pure aluminum. The third significant milestone reached in microtensile testing in 2001 was testing at elevated temperature. We tested both the CMOS material and polyimide at temperatures of 100 and 150 C, in addition to room temperature. The specimen wafers were placed on a heating stage in the SEM, and the force probe used to load the specimens was also heated. We are conducting further tests in order to understand the observed behavior. The changes in the measured properties of the CMOS material were subtle, 10 % or less. Larger changes were seen in the polyimide, but its the results so far are ambiguous because the specimens were apparently damaged during sputter-coating, which was carried out to make the specimens visible in the SEM.

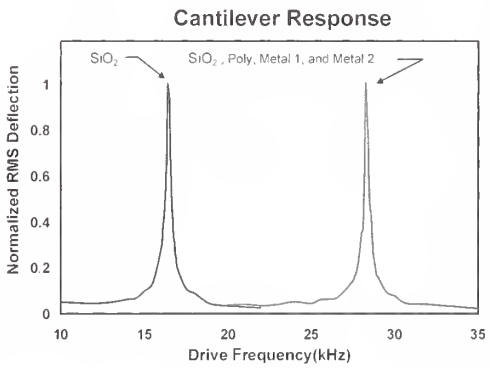
■ The demonstrated applicability of the force-probe technique to a variety of specimen materials and temperatures leads us to think that this technique and its complementary specimen geometry may become a standard method for microtensile testing.

■ Our measurements of AC electromigration have produced microstructural features completely different in both quantity and quality from those seen in conventional DC electromigration testing. Similar features are produced during mechanical fatigue. High-currents at AC also produce whiskers, although they are longer and more slender than those produced during DC electromigration tests. The relationship among failure by DC electromigration, failure by AC electromigration, and the performance of actual devices is now being studied.



SURFACE MORPHOLOGY PRODUCED BY AC ELECTROMIGRATION MEASUREMENTS.

■ Because it is sometimes impossible to get films of individual materials with the interconnect stack in a chip that goes through a normal manufacturing process, we are studying measurement methods that use composite laminate specimens that include several materials, such as metal and dielectric. The elastic modulus of the individual films in the laminate is to be determined by differences between the resonant frequencies of beams with different combinations of metal, dielectric, and polysilicon. A model has been developed for a composite cantilever beam. Preliminary measurements indicate that this technique can provide accurate values of the different layers in the interconnect structure, as well as insight into the behavior of the structure as a whole.



FREQUENCY RESPONSE OF TWO CANTILEVER TEST STRUCTURES.

■ We have been collaborating with George Harman on IC bond pad test structures to meas-

ure the temperature of the wire bonding process. The bond pad test structures contain an integrated thermocouple that is used to sense the temperature of the bond pad during wire bonding. The thermocouple is composed of an aluminum-polysilicon contact. A test chip containing the bond pad test structures was fabricated and tested. The aluminum-polysilicon thermocouple was determined to have a Seebeck coefficient of 44 ΦV/°C using a newly designed test structure. Measurements of the bond pad temperature and a model that is being developed have been reported at an industry conference.

Recent Publications

Yeung, B., Read, D. T., Guo, Y., Lytle, W., Sarihan, V., "Microscale test technique and results for aluminum thin films," accepted for International Mechanical Engineering Conference and Exhibition, November. 2001.

Read, D. T., Cheng, Y-W., Sutton, M. A., McNeill, S. R., Schrier, H., "Proposed Standardization Effort: Digital-Image Correlation for Mechanical Testing," *Proceedings of the SEM Annual Conference on Experimental and Applied Mechanics*, June 2001, pp. 365-368.

Read, D. T., McColskey, J.D., and Cheng, Y.-W., "Microscale Test Technique and Results for Aluminum Thin Films," *Proceedings of the SEM Annual Conference on Experimental and Applied Mechanics*, June 2001, pp. 442-445.

LaVan, D.A., Tsuchiya, T., Coles, G., Knauss, W. G., Chasiotis, I., and Read, D. T., "Cross Comparison of Direct Strength Testing Techniques on Polysilicon Films," *Mechanical Properties of Structural Films, ASTM STP 1413*, C. Muhlstein and S. B. Brown, Eds., American Society for Testing and Materials, West Conshohocken, PA, 2001.

Read, D. T., Cheng, Y.-W., and McColskey, J.D., "High Ductility in Small Tensile Specimens of e-Beam-Deposited Aluminum Films," *Scripta Materiala* **45** (2001), pp. 583-589.

Long, G. S., Read, D. T., McColskey, J. D., and Crago, K., "Microstructural and Mechanical Characterization of Electrodeposited Gold Films," *Mechanical Properties of Structural Films, ASTM STP 1413*, C. L. Muhlstein and S. B. Brown, Eds., American Society for Testing and Materials, West Conshohocken, PA, 2001.

Herman, David, Gaitan, Michael, and DeVoe, Don, "MEMS Test Structures for Mechanical Characterization of VLSI Thin Films," Proc. SEM Conference, Portland Oregon, June 4-6 ,2001.

Shuman, Shivesh, Gaitan, Michael, Joshi, Yogendra, and Harman, George, "Wire Bond Temperature Sensor," IMAPS 2001 Symposium, Baltimore, MD, October 7-11, 2001.

Volkert, C.A. , Keller, R. R., Mönig, R., Arzt, E., and O. Kraft, O., "Fatigue as a Failure Mechanism in Interconnects," submitted to *Applied Physics Letters*.

Keller, R.R., Mönig, R., Volkert, C. A., Arzt, E., Schwaiger, R., and Kraft, O., "Interconnect Failure due to Cyclic Loading," submitted to American Institute of Physics Conference Proceedings: Sixth International Workshop on Stress-Induced Phenomena in Metallizations.

Packaging Reliability

Goals

The goal of this project is to provide the microelectronics packaging industry with information, guidance, and tools through technology transfer to characterize the behavior of features and interfaces in packaging that are thermally stressed. Information and guidance are provided directly to individual companies and to consortia through collaborations whereby we are provided with specimens, which present a reliability concern to the manufacturer or end-user. The results of the tests are reported to the provider, and are typically reported in the general literature or at technical meetings. This system contributes toward achieving our third and primary goal—providing the industry with the tools to characterize these thermomechanical behaviors. Review and evaluation of the techniques by our industrial collaborators allows us to refine the techniques to make them optimally beneficial to industry and to demonstrate to the industry at large the capabilities of the techniques on actual packages in development, essential for technology transfer.

Customer Needs

The challenges faced by the microelectronics industry are multi-fold as they continuously strive to make products that are lighter, faster, and more efficient, while maintaining their profit margin. Addressing one aspect can present multiple secondary problems, as with Cu interconnects requiring a barrier to prevent contamination of the Si die. New materials and previously used materials at smaller size scales will have unfamiliar behaviors in service, and may or may not be compatible. The industry typically tests for reliability using thermal cycle, pressure cook, and thermal shock tests. These tests indicate when there is unacceptable response, a 10–20% increase in resistance, but they cannot determine how or where failures occur. It is an inefficient use of resources to reengineer a package without understanding the failure mechanisms of the existing layout, and modeling cannot answer these questions without reliable input data. As companies endeavor to gain the competitive edge, they become more willing to do the groundwork to obtain insight into failure mechanisms. Data that reflect actual materials behavior and interactions are needed both at the design stage and at the qualification stage.

Technical Strategy

Our established programs in infrared (IR) (thermal) microscopy and electron-beam moiré, and our developing techniques in scanning thermal microscopy and scanning probe moiré, each utilizing the AFM (atomic force microscope), have much to offer the microelectronics industry. We have been approached by industry with requests for aid as simple as "How high are the temperatures in this MCM (multichip module) during service" to as challenging as "What are the strains in the on-chip tungsten vias under thermal loading". The first was answered using the IR microscope; the second has yet to be answered.

We have just completed our second year of applying thermal conductivity measurements using the IR microscope to the problem of packaging reliability and have engendered great interest from the Advanced Embedded Passives Technology (AEPT) Consortium. As thermal conductivity measurements are one of the most sensitive indicators of metal purity, likewise they are one of the most sensitive indicators of interfacial integrity. A minute decline in interfacial thermal conductivity is the first indication of the microcracks and fissures that may ultimately result in failure.

The electron-beam moiré technique offers a unique capability. Unlike moiré interferometry, it can quantify strain in the different materials at both low temperatures and at high temperatures. It measures thermally-induced strains representative of those experienced by the package in service, rather than residual strains due to processing. In addition, it can quantify the accumulation of plastic strain during thermal cycling, and it is clear from the images in which materials the strains are occurring. The technique is designed to look at strains on a local scale, but is flexible enough to allow comparison of those local strains at multiple locations across the cross section.

Thermal microscopy and electron-beam moiré are complementary techniques, each supplying pieces to the puzzle of how failure occurs. The AEPT Consortium has actively enlisted our help, recognizing the value of each technique, alone and together.

DELIVERABLES: Quantitative measurements of thermal conductivity of homogeneous material using scanned-probe microscopy (SPM)

DELIVERABLES: Quantitative measurements of industrial specimens using thermal SPM

Technical Contact:
Elizabeth Drexler
Andrew Slifka

Staff-Years (FY 2001):
1.5 professional

Funding Sources:
OMP STRS (70 %)
Other Agency (30 %)

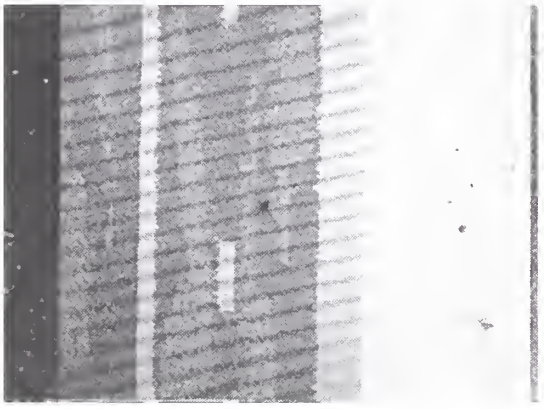
DELIVERABLES: IR microscope measurements of next-generation embedded resistor specimens from the AEPT consortium

DELIVERABLES: Electron beam moiré measurements of next-generation embedded resistor specimens from the AEPT consortium

DELIVERABLES: Transfer of IR microscopy and electron beam moiré measurement technologies to members of the AEPT consortium

Accomplishments

■ A test program was begun for IBM in Rochester, MN on their BGA (ball grid array) package with the Si chip incased in ceramic. The specimens were received in early February. The combination of alumina and solder columns made specimen preparation very difficult. The first electron-beam moiré test was completed in July, but the results were ambiguous. A second specimen was prepared, tested for seven thermal cycles between –5 °C and 130 °C, and the results analyzed in August. These results show that no shearing of the solder column developed over this temperature range and number of cycles, either at the interface with the circuit board or the alumina (See Figure 1).



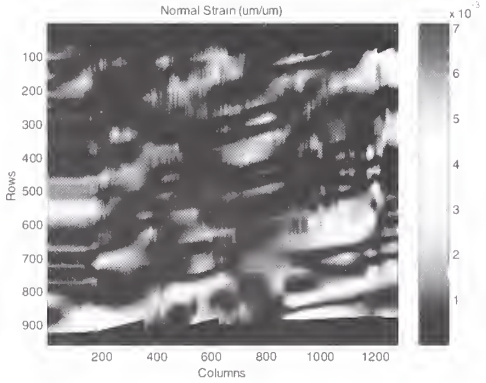


FIGURE 1. MOIRÉ IMAGE AND CORRESPONDING STRAIN MAP OF THE IBM BGA SPECIMEN AFTER 7 THERMAL CYCLES.

■ In the early part of FY 01 we tested integral resisitor material from Polymore in the next phase of our work on interfaces in integral and embedded passive components. Seventy-two thermal cycles were completed between –55 and 125 °C with no damage detected by electron-beam moiré and only slight damage detected by interfacial thermal conductivity measurements. IR microscopy detected a change in interfacial thermal resistance at the interface between the resistor material and the printed wiring board, which turned out to be due to diffusion of metals through the polymeric materials. Electron probe microanalysis confirmed this. Analysis of this specimen is continuing. In mid-February we were approached by MicroFab Technologies, a member of the Advanced Embedded Passives Technology (AEPT) Consortium. They use an inkjet process to dispense resistive ink for producing embedded resistors. There were some issues concerning the adhesion of intrinsically conductive polymer (ICP) to the copper traces and they felt that electron-beam moiré and thermal conductivity tests would offer some insight. Tests on the first set of samples were completed in April and the preliminary results were reported at the quarterly meeting of the AEPT Consortium. At that time we learned that the focus of the program had changed slightly; now MicroFab would use their process to reverse-trim resistors by adding minute amounts of resistive ink to obtain the required resistance value. For the initial stages of development, they wanted interfacial thermal conductivity data to determine the quality of the interface. By late fall of 2001, they expect to have a product ready for qualification testing and, at that time, they would want data from both thermal microscopy and electron-beam moiré to help in understanding the materials' behavior.

■ Meanwhile, one of the other consortium members learned about our techniques and asked our help in evaluating termination geometries. SAS Circuits provided us with samples with four different geometries. Two of the specimens had interconnects with straight approaches to the termination, but different sized terminations. The other two had indirect approaches, that is, the interconnect had a bend. SAS Circuits was interested in knowing what magnitude of strains was experienced by the package during processing up to 177 °C. Four specimens were prepared and tested in the 4th quarter of FY01 (see Figure 2). The data will be reduced, analyzed, com-

pared, and presented to the quarterly meeting of the AEPT Consortium in October.

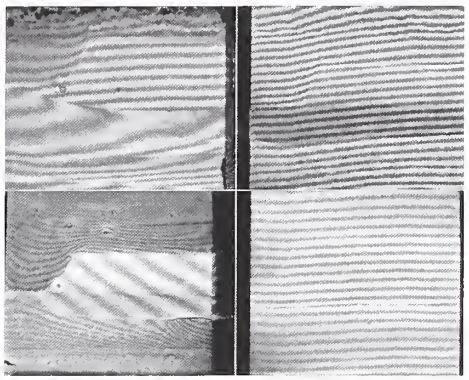


FIG 2. MOIRÉ IMAGES OF EMBEDDED RESISTOR SPECIMENS PROVIDED BY SAS/CORETEC INC. AT 177 °C.

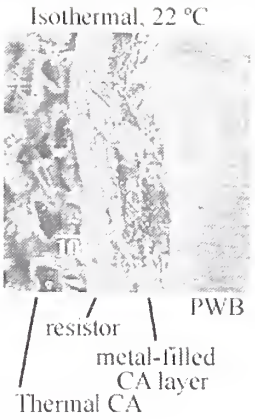


FIG 3. THERMAL SPM IMAGE OF AN INDUSTRIAL INTEGRAL RESISTOR SPECIMEN.

■ One issue became clear as the thermal conductivity tests were being conducted for MicroFab, we needed improved resolution in order to distinguish what was occurring in the very thin (<10 μm) resistive ink. This need, coupled with the desire for increased resolution for the moiré measurements, led us to the atomic force microscope (AFM). We had an existing AFM outfitted for thermal measurements. Special cantilevers with coated tips that act as thermistors are used. Figure 3 shows a thermal image of an integral resistor specimen using that system. Thermal imaging is possible with the system, but the electronics provided are so noisy that there is no way to repeatably acquire images. Therefore, using that AFM system for thermal measurements is not possible. Moiré on the scanning probe microscope should follow the same theory as with moiré generated in the scanning electron microscope. The probe tip is looking for height differences, analogous to how the electron beam looks for edges. So if the number of raster lines is approximately equal to the number of lines of the specimen grating in the field of view, moiré fringes will be reproducibly generated. This part of the theory has been validated.

■ The problem arises when one attempts to calibrate the technique for thermally-induced strains. Early on in the process, we recognized that a very stable system was essential and, as a result, our existing AFM system was inadequate. We tested a stable, closed-loop system that also had a well-controlled thermal attachment at the manufacturer's applications laboratory and obtained extremely consistent room temperature data (±0.03 fringes). However, when we attempted to thermally load and unload a gold standard to obtain coefficient of thermal expansion data, the value measured was 3× the handbook value (14.2×10^{-6}/°C), and the loading and unloading slopes were inconsistent. Work continues with researchers at the University of Colorado to try to determine the source of the error. Several factors have been ruled out, but the solution is still undetermined.

■ We have developed and tested software that provides repeatable quantitative analysis of IR microscope data. This enables us to measure interfacial thermal resistance across relevant interfaces in electronic packaging specimens and embedded and integral resistor specimens. A modification to allow joule heating of resistor specimens for IR microscopy measurement was designed and tested. This yields accelerated degradation of interfaces and also allows analysis of heat flow under extreme conditions as defined by our industrial collaborators. We have developed the mathematics required to analyze IR microscope measurements under joule heating. Numerous industrial specimens were measured using IR microscopy with joule heating, one being shown in figure 4. A set of measurements was used to model interfacial thermal resistance

FIGURE 4. IR MICROSCOPE IMAGE OF A JOULE-HEATED INTEGRAL RESISTOR FROM MICROFAB, INC.

as a function of thermal cycling and a paper was written on the subject.

- For comparison with IR microscopy, a method of generating a comparable temperature difference across a specimen was needed for thermal SPM. A heating apparatus for use with thermal SPM measurements was designed and constructed. Comparative measurements of a single specimen, using both IR microscopy and thermal SPM, showed the potential of the new thermal SPM technique. Members of the AEPT consortium have shown interest in this technique, as it is able to probe features on an appropriate size scale and will be applicable for years to come.

FY Outputs & Outcomes

Collaborators:

- IBM, Rochester, MN
- Arv Sinha, Joe Kuczynski
- AEPT Consortium
- Dupont, John Felten
- MacDermid, Dennis Fritz
- Merix, Bob Greenlee
- MicroFab, Plano, TX
- Virang Shah
- SAS Circuits, Littleton, CO
- Richard Snogren, Matt Snogren
- University of Colorado
- Ken Douglass, T. Andrew Winningham
- Colorado School of Mines
- Ivar Reimanis, Saki Krishnamurthy,
- John Berger

Invited Talks:

- HP, Ft. Collins, CO, January 26, 2001
- ASNT Spring Conference, Denver, CO, March 27, 2001
- University of Denver, Denver, CO, April 18, 2001

Recent Publications:

Drexler, E. S., "Plastic Strain in Thermally Cycled Flip-Chip PBGA Solder Bumps," *IEEE Transactions on Advanced Packaging* **23**, 4, pp. 646–651, (2000).

Drexler, E.S., and Winningham, T.A., "Validation of Scanning Probe Moiré Technique Using the CTE of Gold," in *Proceedings of the Society for Experimental Mechanics Annual Conference on Experimental and Applied Mechanics*, June 4–6, 2001, Portland, OR, Society for Experimental Mechanics, Bethel, CT, pp. 387–390 (2001).

Slifka, A.J., Drexler, E.S., "Thermomechanical Effects in Embedded Passive Materials," submitted to *Journal of Electronic Materials*.

Wafer Characterization and Process Metrology Program

Device scaling has been the primary means by which the semiconductor industry has achieved unprecedented gains in productivity and performance quantified by Moore's Law. Until recently only modest changes in the materials used have been made. The industry was able to rely almost exclusively on the three most abundant elements on Earth – silicon, oxygen, and aluminum.

Recently, however, copper has been introduced for interconnect conductivity, replacing aluminum alloys. A variety of low-dielectric constant materials are being introduced to reduce parasitic capacitance, replacing silicon dioxide. As dimensions continue to shrink, the traditional silicon dioxide gate dielectric thickness has been reduced to the point where tunneling current has become significant and is compromising the performance of the transistors. This is requiring the introduction of higher dielectric constant materials. Initially the addition of nitrogen to the gate material is sufficient, but in the near future more exotic materials such as transition metal oxides, silicates, and aluminates will be required. As dimensions are reduced, gate depletion effects and dopant diffusion through the gate dielectric are limiting transistor performance. With the replacement of the traditional silicon dioxide/ polysilicon gate stack processes with materials capable of supporting ever shrinking geometries, the task of the industry becomes more difficult. The overall task represented by the projects below reflects the need for analytical techniques with unparalleled spatial resolution, accuracy, robustness and ease of use.

Shrinking dimensions of transistors while simultaneously increasing the wafer diameter from 200 mm to 300 mm is placing more stringent requirements on wafer flatness, thickness and warp, ion and particle contamination.

Accurate metrology of process gases is essential for reproducible manufacture of semiconductor products. Critical physical parameters need to be measured on a wide variety of reactive and non-reactive process gases, allowing the accurate calibration of flow meters and residual gas analyzers. Water contamination at extremely low levels in process gases presents serious manufacturing difficulties. Accurate calibration of water vapor at extremely low vapor pressures is required.

Accurate metrology of process gases is essential for reproducible manufacture of semiconductor products and a wide variety of metrology issues emerge in plasma, chemical vapor, and rapid thermal processing steps used in semiconductor manufacture.

Detection and accurate sizing of particle contamination continues to challenge semiconductor manufacturing.

Wafer and Chuck Flatness Metrology

Technical Contact:
Tony L. Schmitz

Staff-Years (FY 2001):
0.9 professional
0.2 contractor

Funding Sources:
STRS (100 %)

Goals

This project will provide measurement and infrastructural technology to support the measurement of flat wafer surfaces, either in the free-form or as chucked states. Specific goals are to provide interferometric measurements of as-chucked 300 mm wafer flatness and to develop and demonstrate infrared interferometric measurements of wafer thickness, thickness variation, and bow.

Customer Needs

Limited lithographic depth of focus budgets for finer features, combined with larger silicon wafers, pose new challenges for flatness and flatness metrology. Conventional vacuum chucks introduce additional distortions to the thickness variations in the wafer itself. These combined effects may reduce the process latitude.

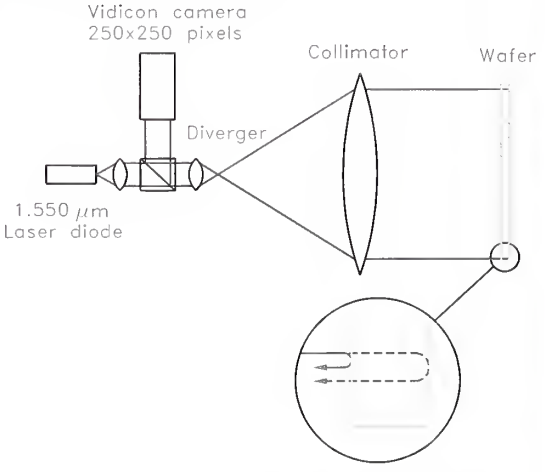
Capacitance based tools are widely used today for wafer geometry measurements, but have some limitations. Optical techniques are being developed in a number of organizations, but initial intercomparisons show significant measurement divergence. At a recent NIST hosted workshop (I/30/01), instrument developers and wafer manufacturers both expressed the need for calibration artifacts calibrated optical flats as references for the instrument makers and reference wafers with mapped thickness variations for the instrument users. The optical metrology tools developed in this project will provide traceable measurements for 300 mm wafers at uncertainties compatible with all lithographies envisioned in the NTRS. Once that measurement capability is in place, the mechanism for providing industry with artifacts will be selected.

Technical Strategy

The primary goal in this project is to develop full aperture interferometric methods to evaluate important wafer characteristics such as flatness, thickness, thickness variation, and bow.

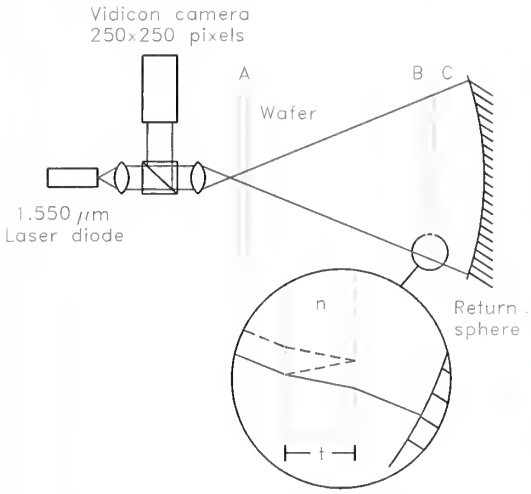
The main tool applied to the measurement of as-chucked wafer flatness will be a 300 mm aperture, multi-purpose interferometer designed to be capable of measurements of flats, spherical and aspheric optics. The NIST X-ray Optics CALIBration InterferometeR (XCALIBIR) has a target uncertainty for the measurement of flats of 0.25 nm. The instrument was installed at NIST in 3Q99 in a specially designed environment. XCALIBIR will be available for measurement of as-chucked wafer flatness, over both full- and sub-apertures.

As-chucked wafer flatness depends both on the chuck and on thickness variations in the wafer. A second major tool to be applied in this project is the NIST InfraRed InterferometeR (IR^2), a prototype infrared interferometer built for NIST by Tropel, Inc., based on a NIST patent. The instrument can now be configured to operate as a phase shifting Twyman-Green interferometer or to wavelength shift Haidinger fringes. Wafers may be measured either in a diverging wavefront or with a plane wave. The plane wavefront Haidinger fringe measurement technique is the current focus of the project. In this method, the planar infrared wavefront is normally incident on the wafer. A portion of the beam is reflected from the front wafer surface, while the rest passes through the wafer and reflects from the rear surface. The interference of these two wavefronts produces the Haidinger fringes and, by wavelength shifting, allows calculation of the wafer thickness variation.

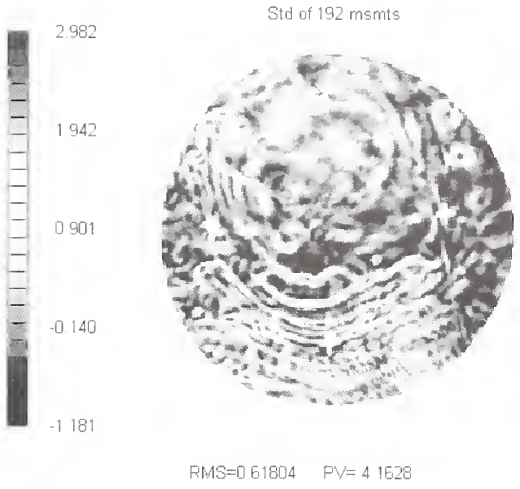


SCHEMATIC FOR COLLIMATED WAVEFRONT HAIDINGER FRINGE WAFER THICKNESS VARIATION MEASUREMENT.

Other setups of the interferometer allow measurement of wafer thickness and bow, as well as thickness variation. Using a spherical wavefront, the wafer geometry can be determined by a series of three measurements: one near the beam focus to calculated center thickness (A) and two with the wafer fully illuminated (B and C), one for each side of the wafer, to find thickness variation and bow.



SCHEMATIC FOR SPHERICAL WAVEFRONT HAIDINGER FRINGE WAFER THICKNESS, THICKNESS VARIATION, AND BOW DETERMINATION. PROCEDURE IS SEQUENCE OF THREE MEASUREMENTS DENOTED A, B, AND C.



PIXEL-BY-PIXEL STANDARD DEVIATION IN THICKNESS VARIATION FOR MEASUREMENTS SPANNING TWO DAYS (UNITS IN NM). NON-REPEATABILITY IS DOMINATED BY STRAY LIGHT IN INTERFEROMETER.

DELIVERABLES: Measure pixel-by-pixel thickness variation for wafers up to 300 mm in diameter using IR^2. Evaluate uncertainty.

DELIVERABLES: Measure flatness of as-chucked wafers in XCALIBIR. Report flatness information with estimated uncertainty.

Accomplishments

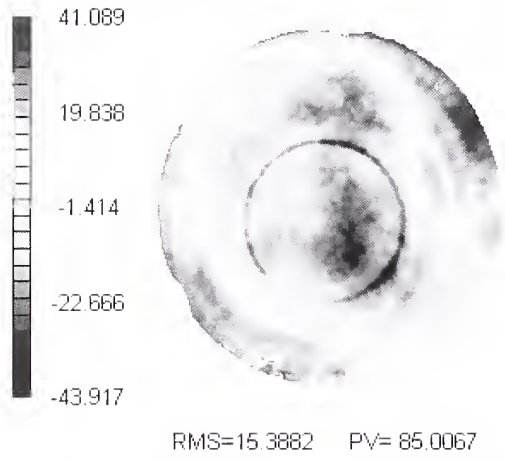
- Measurements were performed to evaluate the pixel-by-pixel measurement repeatability (over the central 150 mm aperture of a 200 mm diameter wafer) for the collimated wavefront Haidinger fringe technique. Phase maps were obtained at 15 min intervals over two days. The repeatability, equal to the maximum value of the pixel-by-pixel standard deviation, was 4 nm.

THICKNESS VARIATION FOR CENTRAL 150 MM OF 200 MM WAFER (UNITS IN NM). DATA DROPOUT IS DUE TO FIDUCIALS USED TO IDENTIFY WAFER POSITION.

- The potential impact of phase change on reflection from physical contact of the back side of the wafer with the support mechanism was investigated. This could be an area of concern for thickness variation measurements of chucked wafers using IR^2 depending on the chuck type and contact area. Two cases were evaluated: 1) current wafer holding mechanism using small vacuum orifice near bottom edge of wafer (12 mm o-ring seal); and 2) metallic coatings were applied to the wafer directly (to simulated intimate contact with a metal surface) and phase maps obtained.

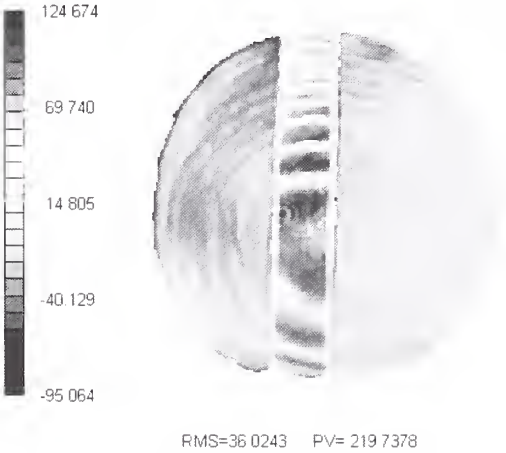
CURRENT WAFER HOLDING MECHANISM (VIEWED FROM THE WAFER BACK SIDE). THE SMALL VACUUM ORIFICE IS SEEN AT THE LOWER EDGE OF THE 200 MM WAFER. BEYOND THE WAFER IS AN F/6 300 MM COLLIMATOR.

The phase change on reflection due to contact between the wafer and o-ring for the current holding method was measured using an f/3 25 mm aperture collimator to increase resolution. The recorded phase maps showed a clear change in the local thickness variation. Additionally, measurements and modeling were completed to evaluate possible local distortion of the wafer geometry due to the vacuum orifice (i.e., bow in the wafer inside the orifice). Recorded local bow (e.g., 0.5 µm for 740 µm thick wafer) matched well with analytic calculations.



PHASE MAP SHOWING EFFECTS OF PHASE CHANGE ON REFLECTION DUE TO WAFER CONTACT WITH RUBBER O-RING (UNITS IN NM).

As noted, the effect of wafer contact with a metallic surface was approximated by a sputter coating a thin gold strip onto a 51.5 mm wafer. Measurements showed a clear change in thickness in the area of the coated strip.



DIFFERENCE MAP BETWEEN MEASUREMENTS OF WAFER WITH/WITHOUT GOLD STRIP APPLIED (UNITS IN NM). PHASE CHANGE ON REFLECTION EFFECTS ARE APPARENT.

- Potential uncertainty contributors were identified. These include: diode wavelength calibration, phase measuring algorithm, camera/wafer coordinate systems, imaging system distortion, stray light, holding technique (phase change on reflection), wavefront effects, diffraction, alignment/focus sensitivity, and resolution/spatial frequency effects. The evaluation of the relative magnitudes is not complete.

- A meeting was held at NIST on January 30, 2001, to address current needs of wafer manufacturers and users, as well as instrument makers. Participants included representatives from: Bay Tech Group, Metrology Perspectives, Komatsu Electronics Metals, Tropel, ADE Phase Shift, Wavefront Sciences, NIST, Komatsu Silicon America, KLA-Tencor Corp., VLSI Standards, MEMC Electronic Materials, Lehighton Electronics, and Northrop Grumman. Several views were expressed at the meeting. A general consensus was reached that NIST would measure 300 mm low-doped silicon wafers, provide a pixel-by-pixel uncertainty statement for the measurement, and make the wafer/measurement information available to the public.

- Continued development of new polishing process models including those using the NIST patented Rapidly Renewable Lap and applications to chemo-mechanical polishing of tungsten.

FY Outputs & Outcomes

- Obtain hardware (collimator/flat) to allow 300 mm aperture measurements. The current available aperture of IR^2 is 150 mm (f/3 system).

- Quantify combined standard uncertainty for collimated wavefront Haidinger fringe thickness variation measurement technique. This step will include comparisons with other measurement techniques to help identify systematic error sources.

- Obtain suitable vacuum chuck(s) to allow measurements of as-chucked wafers on XCALIBIR.

Recent Publications

Evans, C., Davies, A., Schmitz, T., Parks, R., Shao, L.-Z., "Interferometric metrology of substrates for VLSI," 2nd International Conference of the European Society for Precision Engineering and Nanotechnology – euspen, "Torino Incontra" Congress Centre, Torino, Italy, May 27-31, 2001.

Evans, C., Parks R., Shao L-Z., Schmitz T., and Davies A., "Interferometric Testing of Photomask Blank Flatness," Proceedings of the 2001 SPIE Annual Meeting, Vol. 4344, in press.

Paul, E., "A Model of Chemical Mechanical Polishing," Proc. Mater. Res. Soc. 613, E1.4, 2000.

Paul, E., "A Model of Chemical Mechanical Polishing," Semiconductor Online, 27 March 2001, htpp://www.SemiconductorOnline.com/read/sp20010422/421794.

Paul, E., "A Model of Chemical Mechanical Polishing," J. Electrochem. Soc., 148, G355, 2001.

Paul, E., "Application of a CMP Model to Tungsten CMP," J. Electrochem. Soc., 148, G359, 2001.

Paul, E., "Modeling the Effects of Polishing Pressure and Speed on CMP Rates," accepted for the Proceedings Symposium M, Spring 2001 Meeting Materials Research Society.

Paul, E., "A Model of Chemical Mechanical Polishing Part II: Polishing Pressure and Speed," submitted to J. Electrochem. Soc.

Thermophysical Property Data for Modeling CVD Processes and for the Calibration of Mass Flow Controllers

Technical Contact:
John Hurly
Michael R. Moldover

Staff-Years (FY 2001):
1.5 professional

Funding Sources:
STRS (100 %)

Goals

NIST will measure the thermophysical properties of the gases used in semiconductor processing. The property data will improve the modeling of chemical vapor deposition (CVD) and the calibration of mass flow controllers (MFCs). As data are acquired, they are being posted on the internet at http://properties.nist.gov/semiprop. (Fig. 1.) The gases and the properties to be studied were identified by industry representatives. The gases include process gases, "surrogate" gases used for calibration, and binary mixtures of process and carrier gases. The required properties include: speed-of-sound, heat capacity, density (equation of state), viscosity, and thermal conductivity. Industry representatives have also recommended targets for the accuracy of the data.

Customer Needs

The *National Technology Roadmap for Semiconductors* identifies "Equipment Modeling" as first in a list of "Technology Requirements" and states that "the drivers for equipment modeling are *equipment design, process control*, . . . " The *Roadmap* indicates that continuing research is needed to obtain experimental data for "transport and thermal constants." This project will generate transport and thermodynamic property data for the gases used in semiconductor processing. The data will be useful for equipment modeling in CVD processes and the data will also provide a rational basis for the calibration of MFCs used to meter process gases.

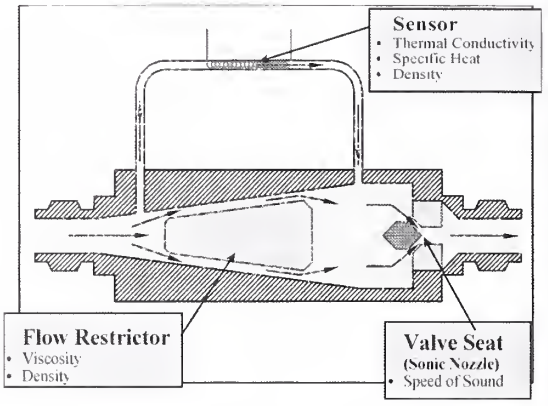


FIGURE 2. COMPONENTS OF A GENERIC MASS FLOW CONTROLLER (MFC) AND THE THEMOPHYSICAL PROPERTIES REQUIRED TO MODEL THEM. COMPONENTS.

Figure 2 shows the components of a generic MFC and the thermophysical properties required to model their performance. During May, 2000,

Tungsten Hexafluoride

WF_6

M.W. [1]	N.B.P. [2]	T.P. [2]
297.84	290.25 K	275.0 K
P_c [3]	T_c [3]	V_c [3]
4.57 MPa	452.7 K	0.1 m^3/kmol

Return to [Gas Index | Fluid Science Group | Process Measurements Division | NIST Home | SEMI | NSMP]

T K	$\frac{C_P^0(T)}{R}$	Vapor Pressure MPa	$B(T)$ $cm^3 \cdot mol^{-1}$	dB/dT $cm^3 \cdot mol^{-1} \cdot T^{-1}$	$C(T)$ $cm^6 \cdot mol^{-2}$	dC/dT $cm^6 \cdot mol^{-2} \cdot T^{-1}$	λ mW/(m·K)	η μPa·s
Estimated Uncertainty	1%/	1%	Gas densities are calculated to better than 0 1% over the temperature and pressure ranges of the reference.				10%	10%
Reference	[4]/	[6]	[5]	[5]	[5]	[5]	[5]	[5]
205	11.84	0.19	-2001.6	5951.2	-4658932	47121716	-	-
210	12.00	0.34	-1864.5	5441.0	-3653771	36754361	-	-
215	12.16	0.58	-1741.8	4994.1	-2884907	28924191	5.2	14.17
220		0.95	-1631.6	4600.8	-2291407	22949084	5.4	14.41
225		1.53	-1532.2	4252.9	-1829413	18345717	5.6	14.64
230		2.39	-1442.1	3943.9	-1466994	14767456	5.7	14.88
235		3.62	-1360.3	3668.3	-1180656	11962851	5.9	15.11

FIGURE 1 SAMPLE WEB PAGE FROM DATABASE LOCATED AT THE URL HTTP://PROPERTIES.NIST.GOV/SEMIPROP/

a workshop entitled "Mass Flow Measurement and Control for the Semiconductor Industry" was organized at NIST by Dr. Robert Berg. At the workshop, representatives of industry identified the properties and their allowable uncertainties for accurately modeling MFCs and related equipment. The workshop's list of properties is: heat capacity at constant pressure $C_p(T)$ (±0.1 %), equation of state $\rho(T,p)$ for predicting gas densities (±0.1 %), viscosity $\eta(T)$ (±0.5 %), and thermal conductivity $\kappa(T)$ (±0.5 %). The workshop urged that values of these properties be made available from a 'standard' source that is accessible to all of the industries associated with semiconductor processing.

Technical Strategy

In the first phase of the work, NIST is measuring the speed of sound $u(T, p)$ in process gases and in the surrogate gases that are often used for calibration. The speed-of-sound data have standard uncertainties of $0.0001 \times u$. The initial results range up to 200 °C and from 25 kPa to 1500 kPa (or to 80 % of the vapor pressure for condensable gases). As an example, Figure 3 shows the phase diagram of trimethyl gallium. Each triangle on Figure 3 indicates values of (T, p) where a speed-of-sound measurement was made. The speed-of-sound data were used to determine the ideal-gas heat-capacities $C_p^0(T)$ and achieved the targeted uncertainty of $0.001 \times C_p^0$. The pressure and temperature-dependence of $u(T, p)$ were correlated with model two-body and three-body intermolecular potentials. These potentials are used to calculate the viral equation of state $\rho(T, p)$ and to get first estimates of the viscosity $\eta(T)$ and the thermal conductivity $\kappa(T)$. For gases where reliable data exist, we verified that results calculated in this way have errors that are less than $0.001 \times \rho$, $0.1 \times \eta$, and $0.1 \times \kappa$ from 200 K to 1000 K at pressures up to 1.5 MPa or 80 % of the vapor pressure.

In parallel with measuring the speed of sound, NIST is developing novel acoustic techniques to measure the viscosity and thermal conductivity with uncertainties of less than 0.5 %. Throughout the project, the results will be made available to the customers through publications in professional journals, presentations at professional meetings, and via a data base accessible through the internet at http://properties.nist.gov/semiprop.

DELIVERABLES: Design and fabricate a facility capable of measuring the speed of sound in the hazardous gases utilized in semiconductor processing.

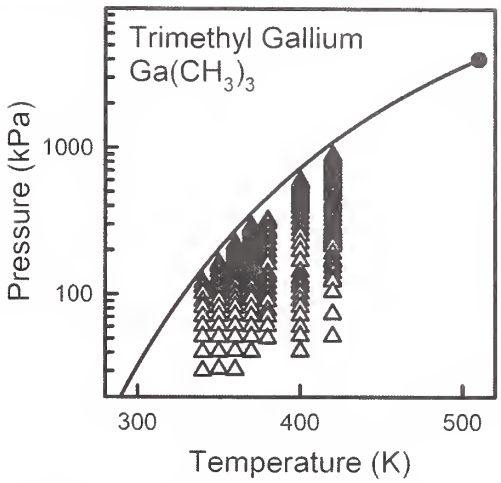


FIGURE 3. PHASE DIAGRAM OF TRIMETHYL GALLIUM. THE VAPOR PRESSURE IS REPRESENTED BY THE CURVED LINE WHICH ENDS AT THE CRITICAL POINT: $T_c \approx$ 510 K AND $P_c \approx$ 4.4 MPA. AT EACH TRIANGLE, THE SPEED OF SOUND WAS MEASURED.

NIST has already developed techniques to accurately measure the speed of sound in a gases and to determine the ideal-gas heat-capacity and the equation of state from the $u(T, p)$ data. NIST used these techniques to determine the thermodynamic properties of alternative refrigerants. Because the alternative refrigerants are inert and non-hazardous by design, modifications are needed to study the reactive, corrosive, and/or toxic gases used in semiconductor processing. These modifications address the issues of safety, sample purity, sample disposal, and materials compatibility.

DELIVERABLES: Develop and optimize novel acoustic techniques for measuring the transport properties of semiconductor process gases.

Because conventional measurements of the transport properties of dilute, corrosive gases are difficult, we are developing acoustical methods of measurement As suggested by M. Greenspan, the acoustical viscometer is a double Helmholtz resonator. The viscosity is deduced from the viscous damping of gas oscillating at acoustic frequencies through a tube joining two chambers. A second resonator will be developed to obtain the thermal conductivity from measurements of the thermal losses of similar oscillations.

DELIVERABLES: Design and fabricate a facility capable of measuring the transport properties in the hazardous gases utilized in semiconductor processing.

A second facility to measure the transport properties will have to be fabricated taking into account the same issues of safety, sample purity, sample disposal, and materials compatibility as

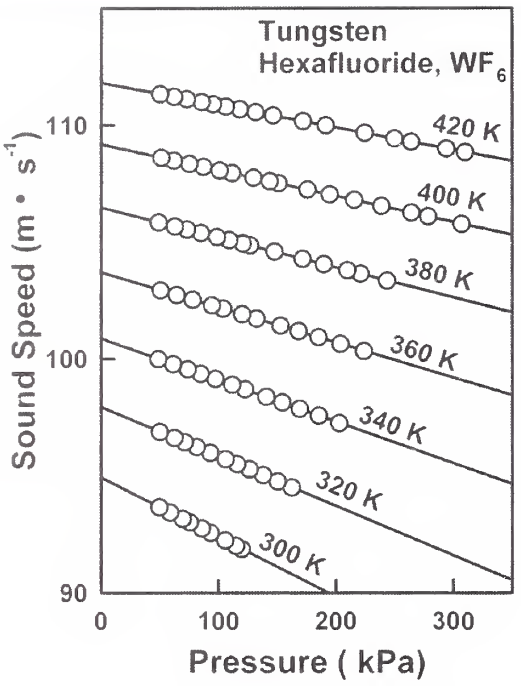


FIGURE 4. SPEED OF SOUND IN TUNGSTEN HEXAFLUORIDE AS A FUNCTION OF PRESSURE ALONG ISOTHERMS.

DELIVERABLES: Measure the speed of sound in the semiconductor process gases identified by the customer. From the speed-of-sound measurements determine the ideal-gas heat-capacity and equation of state for each species.

DELIVERABLES: Measure the transport properties in the semiconductor process gases identified by the customer.

Once the two facilities have been fabricated, calibrated and safety assessments performed the actual measurements in the semiconductor process gases identified by the customers will be performed.

DELIVERABLES: Disseminate the resulting measurements to the customer.

The measurements will be disseminated to the customer through papers in professional journals, talks given at professional meetings, and on a on-line database available via the internet.

Accomplishments

■ A facility was built to safely measure the speed of sound in semiconductor process gases. The apparatus was calibrated with argon. The speed of sound was measured in the surrogate gases CF_4, C_2F_6 and SF_6.

■ Computer programs were developed for correlating speed-of-sound data with model, hard-core Lennard-Jones intermolecular potentials. Programs were developed to calculate second and third virial coefficients and transport properties from the model intermolecular potentials.

■ The speed of sound was measured in the process gases Cl_2, HBr, BCl_3, WF_6, $Ga(CH_3)_3$, NF_3 and C_2H_4O throughout the temperature and pressure ranges listed in Table 1. Figure 4 shows a fraction of the results for WF_6. Typically, the standard uncertainty of the speed of sound was less than 0.01 %. The ideal-gas heat-capacity was determined to within 0.1 % from the zero-pressure intercept of each isotherm. The slope and curvature of each isotherm provided information about each gas's non-ideality from which we developed an equation of state to predict the gas's densities to within 0.1 %.

Table 1. Ranges of speed-of-sound data for process gases.

	Temperature Range (K)	Maximum Pressure (kPa)
Cl_2	260 ! 440	1,500
HBr	230 ! 475	1,500
BCl_3	300 ! 460	1,500
WF_6	290 ! 420	300
C_2H_4O	285 ! 440	1,000
NF_3	200 ! 425	1,600
$Ga(CH_3)_3$	340 ! 420	900

■ The Greenspan acoustic viscometer was developed to measure the viscosity of process gases. Several viscometer geometries and acoustic models were tested to optimize the viscometer's performance. The performance of the

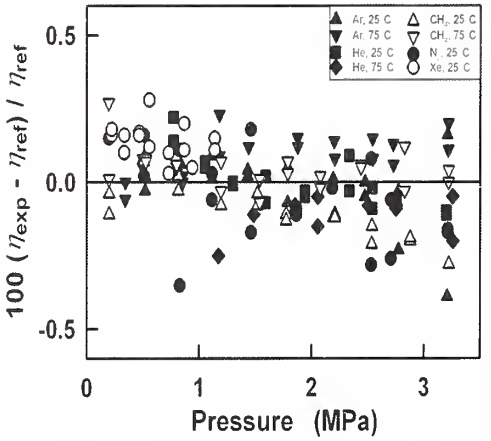


FIGURE 5. PERCENT DEVIATION OF VISCOSITY MEASUREMENTS MADE IN THE GREENSPAN VISCOMETER FROM THE REFERENCE VALUES IN SEVERAL GASES.

acoustic viscometer was tested by comparing the acoustic results for several gases with reference data from the literature. Figure 5 shows that the data from the acoustic viscometer are within 0.5 % of the reference values.

- A second generation Greenspan viscometer has been designed. The new version is being constructed out of Monel which will allow the study of the corrosive process gases. Figure 6 shows the parts of the new resonator before their final assembly.

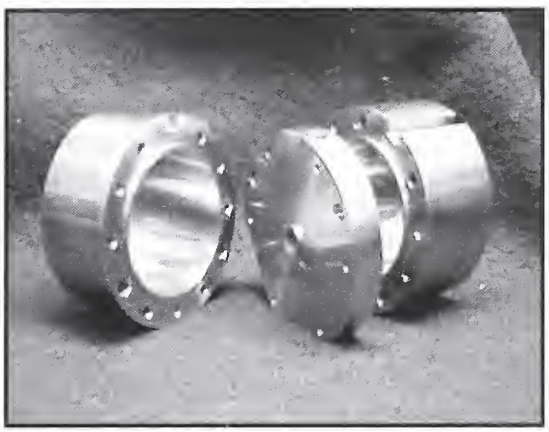


FIGURE 6. MONEL GREENSPAN ACOUSTIC VISCOMETER FOR USE WITH CORROSIVE PROCESS GASES.

- A data base available on the internet at the URL http://properties.nist.gov/semiprop/ has been developed (Figure 1). This data base is updated regularly to give our customers immediate access to our results.

FY Outputs & Outcomes

- We have completed the measurements of the speed of sound of three surrogate gases (CF_4, C_2F_6 and SF_6) and seven semiconductor process gases (Cl_2, HBr, BCl_3, WF_6, $Ga(CH_3)_3$, NF_3 and C_2H_4O). The speed-of-sound data were analyzed to provide the ideal-gas heat-capacity to better than 0.1 % and equation of state for each species able to predict gas densities to better than 0.1 %.

- The Greenspan viscometer has been developed and shown to measure the viscosity of reference gases with errors less than 0.5 %. A Monel version is being fabricated and installed in a hazardous gases facility to allow the study of semiconductor process gases.

- The results of this research have been disseminated by six publications in professional journals and three talks at professional meetings. An on-line data base of the results is available on the internet at http://properties.nist.gov/semiprop/

- John Hurly, (a member of our group) is the Technical Editor of the Gases and Facilities Standards Committee of SEMI (Semiconductor Equipment and Materials International). This year, the committee gave Hurly an award for his "outstanding contributions" to the committee's work.

Recent Publications

J. J. Hurly, "Thermophysical Properties of Gaseous CF_4 and C_2F_6 from Speed-of-Sound Measurements" *International Journal of Thermophysics*, Vol **20**, No 2, 455-484, September 1999.

J. J. Hurly and M. R. Moldover, "Thermophysical Properties of Process Gases," Proceedings of SEMICONwest 1999.

J. J. Hurly, "Thermophysical Properties of Gaseous HBr and BCl_3 from Speed-of-Sound Measurements," *International Journal of Thermophysics* Vol. 21, No. 4, 805-829, July 2000.

J. J. Hurly, "Thermophysical Properties of Gaseous Tungsten Hexafluoride from Speed-of-Sound Measurements," *International Journal of Thermophysics*, Vol. 21, No. 1, 185-206, January 2000.

J. J. Hurly, "A Progress Report: Thermophysical Properties of Semiconductor Manufacturing Process Gases," Proceedings of SEMICONwest 2000.

J. J. Hurly, "The Thermodynamic Properties of Chlorine from speed-of-sound measurements," *International Journal of Thermophysics*, in press.

List of Talks/ Presentations:

J. J. Hurly: "Progress Report: Thermophysical Properties of Semiconductor Manufacturing Process Gases," delivered to the Gas Distribution Systems Working Group, Sunday July 15, at the SEMICON West 2000 conference in San Francisco, CA.

J. J. Hurly: "Thermophysical Properties of Semiconductor Process Gases," delivered to the European SEMI Technical Gas Committee, September 21, 2000, at Oostende Belgium.

J. J. Hurly: "Thermophysical Properties of Semiconductor Process Gases Determined with Acoustic Techniques," delivered at the Fourteenth International Symposium on Thermophysical Properties, June 28, 2000.

Low Concentration Humidity Standards

Technical Contact:
Joseph T. Hodges

Staff-Years (FY 2001):
1.5 professionals

Funding Sources:
STRS (75 %)
Other Agency (25 %)

Goals

The primary objective is to establish quantitative standards enabling the accurate measurement of trace quantities of water vapor (< 10^{13} molecules cm^{-3}). This effort supports the development and application of commercial humidity sensors used for gas purity measurements, and inline monitoring and process control – functions that are relevant to minimizing wafer misprocessing.

Customer Needs

As discussed in the 1997 National Technology Roadmap for Semiconductors in the chapter entitled Metrology, the evolution of sensor-based metrology for integrated manufacturing requires the development of in-situ sensors enabling in-time measurements. In Table 60 entitled Metrology Difficult Challenges, the need for robust and accurate sensor technology and impurity detection in starting materials is highlighted. Of the known impurities in processing gases, water vapor is one of the most ubiquitous and difficult to eliminate. Thus its measurement and control is often critical to various semiconductor-related processes.

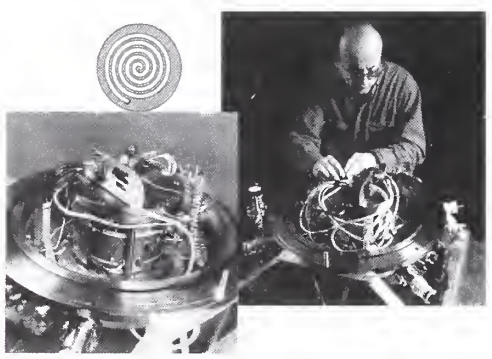


Figure 1. Low Frost Point Humidity Generator.

Although a variety of high sensitivity sensors of water vapor are available, most do not directly measure water in the gas phase. Rather they typically respond to moisture-induced changes in bulk or surface properties associated with the adsorption of water vapor. Consequently, a rigorous first-principles determination of sensor response is often precluded, thus compromising accuracy. Moreover, since many such devices exhibit drift and poor reproducibility, frequent recalibration is required. Interpretation of these measurements is also complicated by complex physical interactions of water vapor with technical surfaces in transfer lines, in reaction chambers and in sensor housings.

The development of accurate and robust water vapor sensors requires well-characterized reference standards against which such devices can be evaluated. This should include a primary method of measurement for water vapor concentration and a complementary method yielding high-precision and stable sources of water vapor. By providing access and traceability to the unique capabilities at NIST discussed below, instrument manufacturers and sensor users can assess the overall performance and accuracy of their measurements

Technical Strategy

Our strategy is to establish complementary capabilities in high-precision generation and measurement of water vapor. Accordingly we have developed a thermodynamically based humidity source capable of delivering 3 mmol to 3 nmol of water vapor per mole of dry gas. This unique system, known as the Low Frost-Point Generator (LFPG), Figure 1, serves as the project cornerstone. Here the water vapor concentration in a gas stream is precisely controlled by active regulation of the saturator temperature and pressure, Figure 2. As such, the LFPG is ideally suited as a platform for testing the performance of various sensing and humidity generation technologies. To date, it is has been used to characterize systems at the research and development stage as well as commercial devices.

To complement our established capability in precision generation of trace humidity levels, we are developing absolute techniques based upon the absorption of optical or near-infrared laser radiation. Water vapor has an absorption spectrum comprising thousands of distinct rovibronic absorption transitions in the visible and near-infrared spectral regions. Thus, the concentration of water vapor can be readily determined in terms of measurements of sample absorbance and independently determined absorption line strengths. Recent advances in source and detector technology, and new spectroscopic techniques that extend the sensitivity of laser absorption measurements now enable the precise sensing of water vapor at concentrations below 10^{10} molecules cm^{-3}. In one such approach, we measured nmol/mol levels of water vapor generated by the LFPG using a prototype diode laser hygrometer (DLH). This hygrometer, which was based upon wavelength modulation spectroscopy, had a linearity better than 1 % over the water vapor mole fraction

range 3 nmol/mol to 2 µmol/mol and yielded a sensitivity of better than 0.5 nmol/mol when tested against the LFPG. These experiments were critical to the development of a similar DLH that is now commercially available.

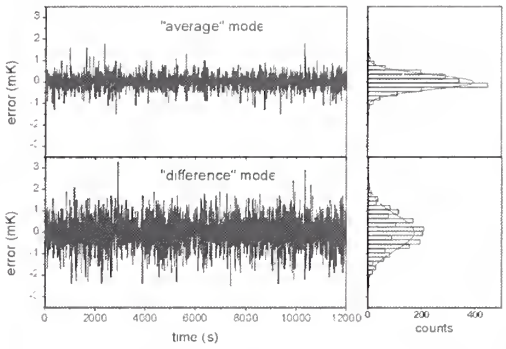


FIGURE 2: STEADY STATE RESPONSE OF SATURATOR CONTROL THERMOMETERS IN NIST LOW FROST-POINT HUMIDITY GENERATOR.

To account for line broadening effects, the most precise absorption measurements require that individual transitions be spectrally resolved. This demands a technique having a frequency resolution much smaller than the characteristic widths of the absorption transitions, and requires that the frequency intervals in the measured spectrum be accurately determined. By combining high spectral resolution with high precision absorbance measurements, the water vapor concentration can be found independently of the composition of the carrier gas. Of the optical absorption methods, cavity ring-down spectroscopy (CRDS) is expected to be the most suitable for a primary method, Figure 3. CRDS is a cavity-enhanced optical absorption technique that has high sensitivity, fast response, and probes a compact well-defined volume. It is important to emphasize that under certain conditions, CRDS can exhibit exceptional spectral resolution, enabling detailed measurements of absorption line shape. To this end, we are developing a refined version of CRDS called frequency-stabilized single-mode cavity ring-down spectroscopy (FSSM-CRDS). Here, the ring-down cavity is actively length stabilized, the probe laser is frequency locked to the ring-down cavity, and the frequency axis of the spectra is based upon the longitudinal mode spacing of the ring-down cavity. See Figure 4.

DELIVERABLES: Commission permeation tube calibration service.

A common technology used by the semiconductor industry for delivering controlled quantities of water vapor is based upon the controlled permeation of water vapor through a material, followed by mixing and dilution with a dry gas of known flow rate. In FY 2002 we will establish a calibration service for water permeation tubes, comparing permeation tubes to the LFPG using a commercial water vapor sensor as a nulling device

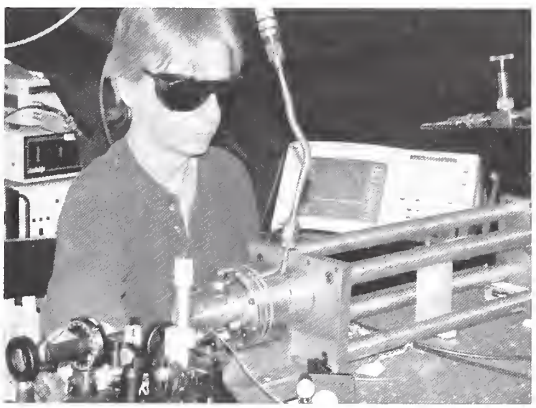


FIGURE 3: FREQUENCY-STABILIZED CRDS SYSTEM.

DELIVERABLES: Investigate background water vapor effects on the output of the LFPG.

The LFPG uncertainty analysis performed in FY2001 is based on the uncertainties in temperature and pressure within the LFPG saturator, ice vapor pressure and the enhancement factor for mixtures of water vapor and air. However, this analysis neglects background effects associated with the transient adsorption and desorption of water vapor from internal surfaces in the flow manifold located downstream of the LFPG. For the lowest range considered, such processes may significantly affect the water vapor concentration in the sample gas delivered by the LFPG to test instrumentation. In collaboration with Air Products Inc., we will quantify the magnitude of this water vapor background using atmospheric pressure ionization mass spectrometry (APIMS).

DELIVERABLES: By 2002, demonstrate FSSM-CRDS as primary method of measurement for low concentration humidity standards.

To achieve the high performance promised by FSSM-CRDS, we will complete our ongoing development of a cw diode laser frequency locked to the length-stabilized ring-down cavity. We will measure the output of a permeation tube moisture generator (in the range 10 nmol/mol to 100 nmol/mol and directly traceable to the LFPG) using this FSSM-CRDS system, and thereby determine the line strengths of the absorption transitions in terms of the LFPG output.

Accomplishments

■ We completed a detailed uncertainty analysis of the LFPG, accounting for measurement uncertainties, and uncertainties in the relevant thermodynamic properties of ice, water vapor and N_2. In summary, the LFPG saturator has a temperature stability of better than ± 2.5 mK (see Fig. 2) giving a relative precision of better than ± 0.05 % and an expanded uncertainty (k=2) in the generated water vapor concentration of less than 0.8% (see Fig. 4). The uncertainty of the LFPG frost-point temperature is less than 0.014 °C.

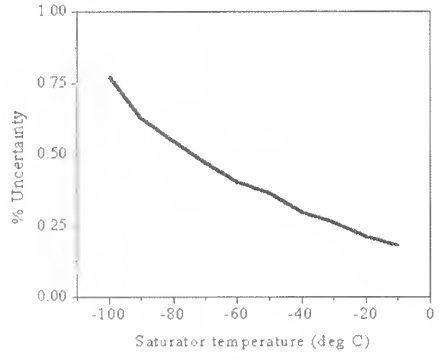


FIGURE 4: EXPANDED UNCERTAINTY (K=2) OF THE LFPG OUTPUT H_2O MOLE FRACTION AS A FUNCTION OF SATURATOR TEMPERATURE.

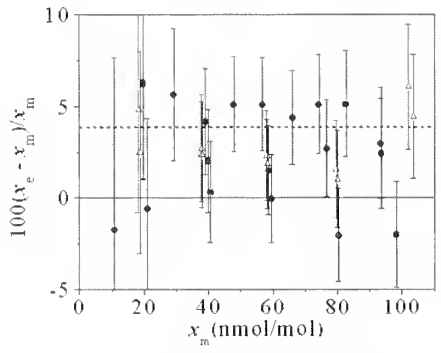


FIGURE 5: COMPARISON OF RESULTS FOR PTMG *A* (CIRCLES) AND PTMG *B* (TRIANGLES). THE DASHED CURVES REPRESENT THE RESPECTIVE AVERAGE PERCENT DIFFERENCES BETWEEN THE PTMG AND THE LFPG

■ We developed a quantitative method for comparing the outputs of permeation tube moisture generators (PTMG) to that of the LFPG. This technique is capable of resolving fractional differences of approximately 1 %, for PTMGs covering the mole fraction range 10 to 100 nmol/mol. An intercomparison of PTMG devices from several customers was completed, and results comparing two representative PTMGs to the LFPG are summarized in Fig. 5. Uncertainties in flow metering and background water vapor present in the carrier gas were identified as limiting effects. The measurement technique used for this work forms the basis for the upcoming permeation-tube calibration service.

■ We have successfully fabricated and tested a length-stabilized CRDS system, based on a continuous wave diode laser. The system is optimized for high-precision measurements of trace water vapor concentration. A CRDS spectrum of atmospheric H_2O is shown in Fig. 6, corresponding to a mole fraction of approximately 6 µmol/mol and concentration of $2x10^{13}$ molecules cm^{-3}. Other results indicate that the integrated CRDS spectra scale linearly with H_2O concentration and support the expectation that nmol/mol level sensitivities and high-precision line shape measurements will be realizable with the fully developed FSSM-CRDS system.

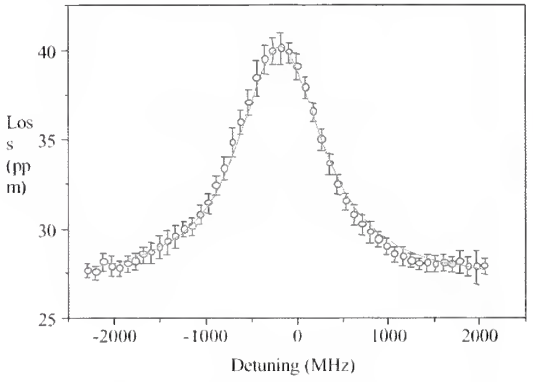


FIGURE 6: CRDS SPECTRUM OF PRESSURE-BROADENED H_2O ROVIBRONIC TRANSITION AT 10687.36 CM^{-1}, CORRESPONDING TO AN ABSORBING WAVELENGTH OF 935.7 NM. THE OPEN CIRCLES ARE THE MEASURED LOSSES, AND THE SOLID LINE IS A VOIGT FIT TO THE MEASURED PROFILE.

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J.T. Hodges, J.P. Looney and R.D. van Zee, "Response of a ring-down cavity to an arbitrary excitation," J. Chem. Phys., **105**, 10278-10288,1996.

G.E. Scace, P.H. Huang, J.T. Hodges, D.A. Olson and J.R. Whetstone, "The new NIST low frost-point humidity generator, "National generator Conference of Standards Laboratories, Proceedings of the 1997 Workshop and Symposium, 2, 657-673, July 27-31, 1997, Atlanta, GA.

G.E. Scace, D.C. Hovde, J.T. Hodges, P.H. Huang, J.A. Silver and J.R. Whetstone, "Performance of a precision low frost-point humidity generator," 3rd International Symposium on Humidity and Moisture, sponsored by the National Physical Laboratory, Teddington, England, April 6-8, 1998.

G.E. Scace, D.C. Hovde, J.T. Hodges, P.H. Huang, J.A. Silver and J.R. Whetstone, "The NIST Low Frost-Point Humidity Generator: A New Standard for Trace Humidity Measurement," Workshop on Gas Distribution Systems, Semicon West 98, San Francisco, CA, July 12, 1998.

J.T. Hodges, J.P. Looney and R.D. van Zee, "Single mode cavity ring-down spectroscopy with pulsed lasers," 1998 International Symposium on Molecular Spectroscopy, June 15- 19, 1998, Columbus, OH.

R. D. van Zee, J. P. Looney, and J. T. Hodges, "Measuring pressure with cavity ring-down spectroscopy," in *Advanced Sensors and Monitors for Process Industrial Environment*, W. A. de Groot, ed., SPIE Proc. **3535** (1998).

J.P. Looney, J.T. Hodges and R.D. van Zee, "Quantitative absorption measurements using cavity-ringdown spectroscopy with pulsed lasers," Chapter 7, in *Cavity-Ringdown Spectroscopy-A New Technique for Trace Absorption Measurements*, ed. K.W. Busch, American Chemical Society Symposium Series No. 720, 1999.

R. D. van Zee, J. T. Hodges and J. P. Looney, "Pulsed, single-mode cavity ring-down spectroscopy," Appl. Opt, **38**, 3951-3960, 1999.

D.C. Hovde, J.T. Hodges, G.E. Scace, J.A Silver, "Wavelength-modulation laser hygrometer for ultrasensitive detection of water vapor in semiconductor gasses," Appl. Opt, **40**, 829-839, 2001.

G.E. Scace, and J.T. Hodges, "Uncertainty of the NIST low frost-point humidity generator," Proceedings of the 8th International Symposium on Temperature and Thermal Measurements in Industry and Science, June 19-21, 2001, Berlin, Germany.

P.H. Huang, G.E. Scace, and J. T. Hodges, "Measuring technique for quantifying performance of dilution-based trace moisture generators," Proceedings of the 8th International Symposium on Temperature and Thermal Measurements in Industry and Science, June 19-21, 2001, Berlin, Germany.

Development of Quantitative Measurements for Vacuum Process Control

Technical Contact:
Robert F. Berg

Staff-Years (FY 2001):
2 professional

Funding Sources:
STRS (100 %)

Goals

Develop primary flow standards in the flow range from 10^{-7} to 10^{-3} mol/s and transfer this flow measurement capability to the US semiconductor industry. (10^{-6} mol/s is 1.3 standard cubic centimeters per minute.)

Support semiconductor process-control efforts by developing a real-time, quantitative, *in-situ* approach for measuring process gas composition.

Customer Needs

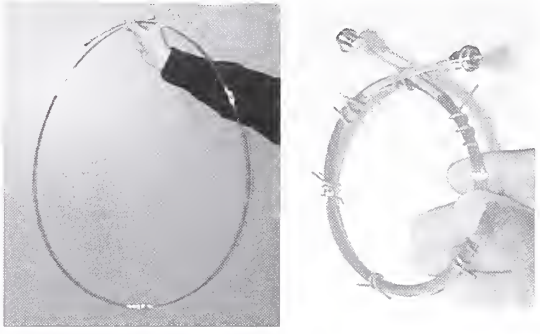
Many industrial processes require the accurate metering of mass flow rate over the range from 10^{-7} to 10^{-3} mol/s. Most prominent are the manufacturers of semiconductor devices, who use thermal mass flow controllers (MFCs) to control a wide variety of toxic, flammable, and corrosive gases. Participants at a recent industry workshop at NIST expected future requirements for flow measurement accuracies to be better than 1 %, and they identified the need for national flow transfer standards with uncertainties of 0.1 %. New primary flow standards and improved flow measurement techniques must be developed to meet these needs.

The increasing volume and complexity of vacuum processing in the semiconductor industry requires improved real-time process monitoring and control of process gases, reaction products, and gaseous contaminants. RGAs are the most promising candidates for this task, and are already used in a variety of vacuum processes, but their often unpredictable performance has limited these applications. Realizing their potential requires a better understanding of the factors limiting their performance, particularly when operating with reactive process gases, and the development of *in situ* calibration techniques to compensate for instrument drifts in process applications.

Technical Strategy

The flow measurements are based on a diverse series of primary standards. The first was a constant-volume (pressure rate-of-rise) primary standard that we developed to measure flows up to 10^{-3} mol/s with uncertainties of about 0.1 %. It has been replaced by a constant-pressure (variable volume) standard that can operate at pressures from 0.5 to 5 atmospheres with an uncertainty of about 0.05 %. The third primary standard is gravimetric; flow measurements made by a transfer standard are integrated and compared to the weight change of a gas bottle.

Transfer standards allow the primary flow standards at NIST to be compared to flow meters at other locations. Although a flow meter manufacturer typically constructs its own primary standard, comparisons with NIST allow the manufacturer to demonstrate proficiency and, if necessary, provide traceability to NIST. For this purpose, we have developed a series of very stable transfer standards based on laminar flow through a thermostatted duct. The first generation used a stainless steel, helical duct of rectangular cross-section. It was used to perform on-site proficiency tests of industrial flow standards at more than ten fabrication facilities and MFC manufacturers. The second generation transfer standard uses quartz capillaries with a circular cross-section, which are available commercially for gas chromatography. It has been used in five comparisons.



LEFT: A TRANSFER STANDARD FLOW IMPEDANCE FORMED FROM 19 PARALLEL QUARTZ CAPILLARIES. RIGHT: TIGHTLY COILING THE FLOW IMPEDANCE TESTED THE CENTRIFUGAL CORRECTIONS USED IN THE TRANSFER STANDARD'S HYDRODYNAMIC MODEL.

NIST vacuum (partial-pressure) standards have been used to examine the performance characteristics of commercial residual gas analyzers (RGAs), the most flexible instruments available for *in situ* monitoring of process gas composition. These studies found that the performance of RGAs depends not only on instrument design, but also on instrument operating parameters. In particular, these parameters can significantly affect electron and ion space charge within the RGA, which in turn can change performance

characteristics by orders of magnitude. For most RGAs the performance can be optimized by proper adjustment of instrument operating parameters, guided by *in situ* calibration results. Within the past year the RGA studies have been extended to the new closed-ion-source (CIS) instruments.

The performance of RGAs is also significantly affected by the gases being measured, which is a critical issue for the reactive gases used in many semiconductor processes. We have explored these problems in a collaboration with the University of Maryland on the use of RGAs to control a tungsten deposition process in a commercial tool. This experiment involves the measurement of two highly reactive gases, WF_6 and HF. The objectives are threefold: To test *in situ* RGA-calibration procedures in a process tool, to examine the quantitative behavior of RGAs operating under process conditions, and to examine the feasibility of using RGAs for process control.

DELIVERABLES: Develop and characterize a primary flow meter based on constant-pressure operation.

This flowmeter uses optical interferometry to measure and control the displacement of a piston of known cross-section. Controlling the piston's rate of displacement maintains a constant pressure in the gas accumulation volume.

DELIVERABLES: Develop and characterize an improved transfer standard for gas flow.

The second-generation transfer standard is based on laminar flow through a quartz capillary impedance. It operates at higher flow rates with a smaller slip correction and much smaller centrifugal effects than the first-generation transfer standard.

DELIVERABLES: Develop a real-time optical diagnostic system for measurement of chemical vapor deposition (CVD) product gases.

Cavity-ring-down spectroscopy is a feasible approach. An optical cavity or cell and a gas handling/metering system were constructed. A compact, small-footprint diode-laser-based system is being developed, based on existing technology for humidity measurement.

DELIVERABLES: In collaboration with the University of Maryland, demonstrate real-time process control in a CVD process tool.

Residual gas analysis, combined with *in-situ* calibration, was demonstrated to control wafer thickness to better than ± 2 % despite intentionally introduced systematic and random process variations in temperature and process gas flow.

Accomplishments

- We built and tested a gravimetric primary standard for low flow rates of gases. Its measurement principle (weighing) is very different from that of the constant-pressure flow meter already in use (pressure-volume-temperature). In combination, the two primary standards provide a powerful verification of the flow measurement accuracy. Comparisons of the two primary standards show agreement to within 0.1 %.

- A new transfer standard for low flow rates of gases was built and tested. The use of quartz capillary flow impedances avoids problems with the interior roughness of stainless steel capillaries, and it allows the use of an accurate analytical model for centrifugal effects. Tests show that temperature-induced errors of the transfer standard are less than 0.01 % per kelvin; which is negligible. Preliminary tests on helium and argon show agreement with nitrogen to within the uncertainty of the published viscosity values of these gases.

- Temperature and frequency locking electronics for a real-time optical diagnostic system were fabricated.

- The majority of a gas handling and metering system to handle wet hydrogen fluoride also was constructed. Hydrogen fluoride is the principal species of interest in the CVD tool at the University of Maryland (UMD).

- At UMD, several improvements to the CVD process tool were completed in preparation for installation of an optical diagnostic system. These improvements allow operation at higher yield rates more typical of industrial processes. The relevant gas concentrations have increased, thereby increasing measurement sensitivity and reducing measurement error. Previously, low conversions caused layer thickness measurement errors that were typically 10 %. The recent improvements decreased this to less than 2 %.

- An acoustic-based technique to measure species ratio was successfully tested at UMD. It is expected to provide complementary measurements for the optical approach under development at NIST.

FY Outputs & Outcomes

- Flow comparisons — We used the second-generation transfer standard to make two interna-

tional comparisons of gas flow. The first, with the National Metrology Institute of Japan, was made at NIST. The second, with the Istituto di Metrologia "Gustavo Colonnetti," was made in Torino, Italy.

Recent Publications

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R.F. Berg, D.S. Green, and G.E. Mattingly, "Workshop on mass flow measurment and control for the semiconductor industry," *NIST Special Publication 400-101* (2001).

J.T. Herron and D.S. Green, "Chemical Kinetics Database and Predictive Schemes for Humid Air Plasma Chemistry. Part II. Neutral Reactions," *Plasma Chemistry & Plasma Processing* **21**, 459 (2001).

Models and Data for Chemical Vapor Deposition

Technical Contact:
R. W. Davis

Staff-Years (FY 2001):
2 professional
1 student

Funding Sources:
STRS (100 %)

Goals

Acquire an improved understanding of the physics/chemistry of gas-phase generated microcontaminants in thermal chemical vapor deposition (CVD) reactors. Develop a predictive capability for this phenomenon that can be utilized to guide process parameter selection and develop microcontamination standards. The development of experimentally-validated numerical models for microcontaminant formation, growth and transport in rotating disk CVD reactors is a specific goal of this project.

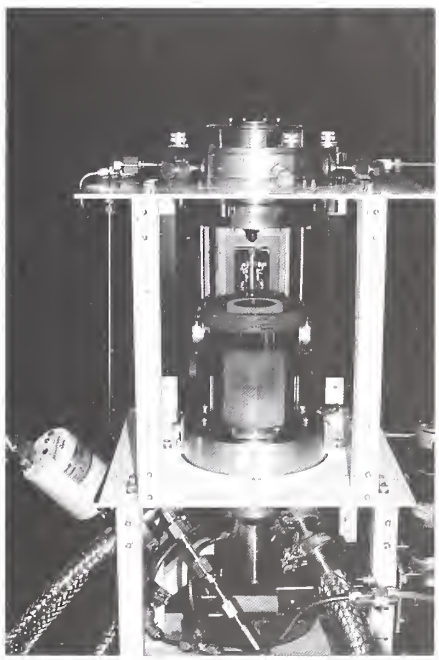
Customer Needs

The Semiconductor Industry Association's (SIA) 1999 International Technology Roadmap for Semiconductors identifies the need for a more fundamental understanding of reactor contaminant formation and transport. It also calls for the development and experimental validation of advanced chemistry/contamination models for defect-free equipment. These needs are being driven by the relentless decrease in feature size. As feature size decreases, the allowable particle contaminant size also decreases. Upon attainment of the 100 nm technology node in 2005, the allowable particle size will only be 50 nm. The current understanding of particles in this size range is extremely limited. These particles are primarily gas-phase generated as opposed to the larger particles that may enter the reactor in the process stream or flake off equipment surfaces. Thus, there is a critical need for the type of research effort being carried out by this project. It will be very difficult to attain particle control in this size regime without the more fundamental understanding of the physics/chemistry of gas-phase generated particles being sought here. This enhanced understanding will underpin the development of the microcontamination models that are necessary for particle control in thermal CVD reactors.

Technical Strategy

The approach being employed here is to carry out a combined numerical/experimental effort in which particle dynamics are probed optically in a rotating disk CVD reactor in close coordination with the development of several microcontamination models. This type of synergistic multimode approach is optimal for achieving an enhanced understanding of the basic physics and chemistry that underlies the microcontamination phenomenon. The rotating disk configuration is ideal for this type of study because of its simple and well-defined flow in which particles form in a highly accessible region of the reactor.

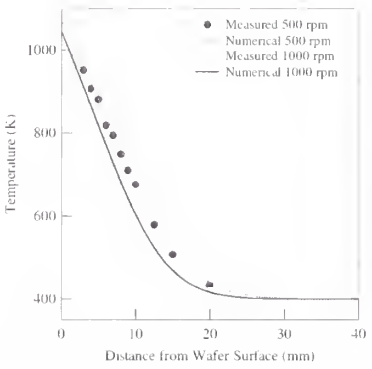
An optically-accessible rotating disk CVD reactor has been constructed and installed for detailed experimental investigation of microcontaminants. This reference reactor can achieve a substrate temperature of up to 1300 K and a rotation rate of 1000 rpm. Silicon CVD can be performed at the purity levels required for microelectronics fabrication. Raman spectroscopy is utilized for *in situ* temperature measurements in this reactor, while light scattering is employed to observe particle behavior.



REFERENCE ROTATING DISK CVD REACTOR.

Two microcontamination models are being developed in close conjunction with the experimental effort. These models are based on aerosol dynamics algorithms for particle formation, growth and transport. One model employs a one-dimensioal formulation valid in the central region of the reactor. This model is operational and, due to the reduction in spatial dimensions, employs a sophisticated kinetics mechanism. A second model still in development is a full two-dimensional axisymmetric

formulation that will enable the prediction of particle behavior anywhere in the reactor. Experimental data are being compared with results from these models in order both to validate them and to help guide the experiments. The figure below shows a typical numerical/experimental comparison involving reactor centerline temperature profiles for two values of the disk rotation rate. The agreement between the two types of profiles is seen to be excellent.



NUMERICAL/EXPERIMENTAL REACTOR CENTERLINE TEMPERATURE COMPARISONS UTILIZING FULL AXISYMMETRIC SIMULATION.

DELIVERABLES: Experimentally-validated microcontamination models for the rotating disk reactor.

An important aspect of this project is the calculation, estimation, and dissemination of fundamental thermochemical and chemical kinetic properties of organometallic compounds. These compounds are used during manufacturing processes to deposit metals in semiconductor, optical, fuel cell, MEMS, and NEMS devices. The thermochemical properties and reaction kinetics of most useful organometallic compounds and related molecular precursors are poorly characterized. This project obtains these properties through three activities involving theoretical estimations and modeling studies. The first data activity, which is in coordination with the Standard Reference Data Program, compiles and evaluates currently available thermochemical data of organometallic compounds and related precursors. These data will become available through an external NIST website. The second activity supplements available data by using *ab initio* and semi-empirical calculations to develop reaction mechanisms from computed molecular structures, thermodynamic properties and spectroscopic properties of Group III and Group V compounds. The third activity utilizes the experimental and computed thermochemical and chemical kinetic data to develop mechanisms for the decomposition of organometallic precursors. These mechanisms are then utilized in reacting flow models of the rotating disk CVD reactor.

DELIVERABLES: Web-based thermochemical and chemical kinetic database for organometallic compounds and related precursors.

Accomplishments

■ New Full Axisymmetric Microcontamination Model — Significant progress has been made toward development of a full two-dimensional axisymmetric microcontamination model. This enhanced model will be able to predict particle dynamics throughout the reactor, not just in the central region which the existing one-dimensional model is limited to geometrically. An initial test case has been successfully computed for the aerosol dynamics in a rotating disk reactor with an inlet silane concentration of 0.03 % in helium. While this is a very encouraging result, more work will be necessary to reduce the inordinately long computation time of several weeks on a high performance workstation. Improvement of algorithm efficiency will thus be a high priority as this effort continues.

■ Improvements in NIST Microcontamination Model — The efficiency of the one-dimensional NIST Microcontamination Model has been significantly enhanced. An increase in speed of approximately five has been obtained by utilizing a nonreacting temperature profile until virtually the end of the computation, when it is finally allowed to adjust to the presence of multiple reacting species. It has also been determined that the employment in this one-dimensional model of temperature profiles computed with the new two-dimensional axisymmetric code results in improved comparisons with experimental results. This is because these temperature profiles more closely match those found in the actual experimental reactor.

■ Spatially-Resolved Gas-Phase Temperature Measurements — Knowledge of the thermal environment in the CVD reactor is critical for investigation of CVD mechanisms. Therefore, rotational Raman spectroscopy was utilized to measure gas-phase temperature profiles in order to validate numerical temperature profiles. The Raman scattering volume was nominally a cylinder 500 μm in length and 250 μm in diameter. Temperatures were determined by comparing a measured Raman spectrum to a calculated spec-

trum and employing a global search minimization to minimize the sum of the residuals squared. The calculated spectrum was the convolution of the rotational Raman spectrum and the fit of the spectrograph lineshape function, and was obtained using the SANDIA CARS code modified for spontaneous Raman scattering. This global fit to all rotational lines simultaneously is particularly useful to minimize the effects of noise on the spectrum, e.g., RF interference, as well as to account for Raman scattering from excited vibrational states which becomes significant at ca. 1000 K and higher for nitrogen. The measured temperature profiles were in good agreement with numerical temperature profiles.

■ Spatially-Resolved Gas-Phase Species Concentration Measurements — Knowledge of gas phase species identities and concentrations is important to validate the numerical flow fields and the model silane pyrolysis mechanism. Therefore, gas phase species identities and relative concentrations were measured with vibrational Raman scattering. The signal from the gas phase nucleated particles is intense when silane is present. In addition, signal from hydrogen molecules (another reaction product) is also observed. Finally, it is noted that nitrogen rotational lines are observed. This indicates that temperature measurements will be possible in the presence of particles. This will enable us to determine whether or not the presence of particles affects the temperature profile, an important consideration for model development.

■ Chemical Properties Calculations — Molecular structure and vibrational frequency data for Group III (Al, Ga, In) and Group V (N,P,As) Hydrides have been compiled. These include the stable molecules (*e.g.*, AlH_3) and radicals (*e.g.*, AlH_2). *Ab initio* calculations have been over a wide range of theories utilizing different quality basis sets. The *ab initio* results have been compared to available experimental data in order to determine the minimum level of calculation necessary to give good molecular structures and vibrational frequencies. Although some of this work has already been reported in the literature, no comprehensive set of benchmark calculations for the whole series has been performed. Molecular structure and vibrational frequency data and bond dissociation energies (BDE's) for the Indium Methyl Hydrides $InH_x(CH3)_y$ have been computed at the B3LYP/cc-pVTZ level of theory. The Indium Methyl Hydrides include the stable molecules InH_3, $InH_2(CH_3)$, $InH(CH_3)_2$, $In(CH_3)_3$, the radicals InH_2, $InH(CH_3)$, $In(CH_3)_2$, and the closed shell intermediates (with lone pairs) InH, $In(CH_3)$. Transition state calculations for abstraction of H atoms from the Indium Methyl Hydrides (In-H, CH_2-H bonds) by H atoms and CH_3 have been computed, as well as a number of other transition state calculations. These transition state structures were then used to determine temperature-dependent rate expressions for the reactions. A simple decomposition mechanism has been constructed based on these data, compared to available experimental data, and is currently being refined. Calculated molecular structure, vibrational frequencies, and BDE's for the Gallium Methyl Hydrides have also been carried out.

FY Outputs & Outcomes

■ Prototype Database Website — A prototype website (http://h105097.nist.gov/ckmechx/) has been made accessible via the internal NIST web. This site currently contains thermochemical and bibliographic information of silicon hydrides and halocarbons important to semiconductor processes. The plan for this site is to have it provide all data necessary to support chemical mechanisms of significance to the industry. The current version of CKMechX has a number of capabilities. Over 4000 enthalpies of formation are available for more than 1000 species with over 4000 bibliographic citations. These data were taken from NIST compilations and evaluations of silicon hydrides, silicon oxy-hydrides, hydrocarbons, fluorinated hydrocarbons, and chlorinated hydrocarbons.

■ Microcontamination Website — A comprehensive microcontamination website (http://www.cstl.nist.gov/div836/836.02/cvd/toppage.html) has been established in order to disseminate the numerical and experimental results obtained from this investigation. Data is available on all aspects of this project, and reprints of relevant publications are downloadable.

Recent Publications

R. W. Davis, E. F. Moore, J. E. Maslar, D. R. Burgess, D. M. Kremer, and S. H. Ehrman, "A numerical/experimental investigation of microcontamination in a rotating disk chemical vapor deposition reactor," Characterization and Metrology for ULSI Technology: 2000 International Conference, ed. D. G. Seiler, A. C. Diebold, T. J. Shaffner, R. McDonald, W. M. Bullis, P. J. Smith and E. M. Secula, CP550, The American Institute of Physics, pp. 292-296 (2001).

J. E. Maslar and W. S. Hurst, "Non-Intrusive Optical Measurements of Gas and Surface Temperatures in Hostile Environments Using Raman Spectroscopy," NISTIR 6572 (in press).

J. E. Maslar, W. S. Hurst, D. M. Kremer, and S. H. Ehrman, "In Situ Gas Phase Optical Measurements of Silane Decomposition in a Thermal Chemical Vapor Deposition Reactor," Proceedings of the Spring 2001 Electrochemical Society Meeting, Washington, D.C. (in press).

Temperature Measurements and Standards for Rapid Thermal Processing

Goals

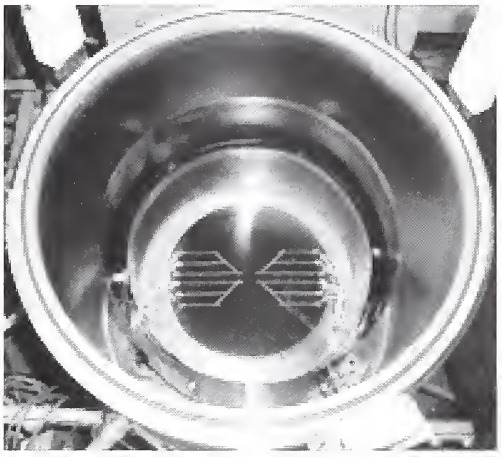
The goal is to develop the technologies required to enable the measurement of Rapid Thermal Processing (RTP) wafer absolute temperatures with uncertainties of 2 °C at 1000 °C as prescribed in the International Semiconductor Technology Roadmap.

Our project, initiated in FY97, has approached this goal with four objectives: (1) To improve calibration wafer technology to a I °C standard uncertainty by demonstrating the use of thin-film thermocouples (TFTCs) in conjunction with wire thermocouples (TCs) on test wafers in RTP tools; (2) To develop methods for in-tool radiation thermometer (RT) calibration, which relate TFTC wafer temperatures to indicated radiance temperatures; (3) To develop and validate models to account for wafer emissivity and the effects of chamber reflected-irradiation on temperatures determined from model-corrected RTs that are calibrated against blackbodies; and (4) To collaborate with the semiconductor industry in implementing new methods for reliable and traceable temperature measurements.

Customer Needs

The measurement needs of the semiconductor manufacturing industry have been stated in the International Semiconductor Technology Roadmap. The requirement is for measurement and control of RTP tools to ± 2 °C at 1000 °C during processing with calibrations traceable to the International Temperature Scale of 1990 (ITS-90). Current industry measurement capabilities are ± 6 °C or three times the uncertainty goal, and major producers have voiced concerns to International SEMATECH (ISMT).

Our customers are the device manufacturers and the suppliers of thermal processing equipment and temperature measurement instrumentation. This community forms our project's Common Interest Group (20 companies meeting annually at NIST since 1997). They serve as a bridge between research and practice, provide advice on shaping objectives, and generate opportunities for technology transfer. The semiconductor manufacturing community is also represented by ISMT, which has set the roadmap requirement for the year 2000. In an earlier planning meeting for demonstrations of the NIST technology, ISMT stated: "Based upon the progress at NIST, it appears that the ISTR roadmap requirements are within reach " [B. Van Eck, ISMT, November 5, 1999].



NIST TFTC TEST WAFER IN THE ISMT-UT TEST BED BEING DEVELOPED TO QUALIFY COMMERCIAL CONTACT AND RADIATION THERMOMETRY INSTRUMENTATION, AND ESTABLISH UNCERTAINTIES IN THEIR TRACEABILITY TO THE ITS-90.

Technical Strategy

Our strategy is to address three core elements of our research that will enable the semiconductor industry to meet the road map requirement: (a) fabrication of test wafers with improved thin-film technology for use by our industrial collaborators to demonstrate in-tool calibration of RTs traceable to the ITS-90; (b) experimentation on the NIST test bed and thermal modeling to determine the effects of wafer emissivity on in-tool calibration of lightpipe radiation thermometers (LPRTs); and (c) calibration and characterization of LPRTs.

The present scope of the TFTC technology work includes designing, fabricating, and testing thin-film thermocouple calibration wafers for use in industrial RTP tools, defining the effect of various wafer and film emissivities on the temperature measurement, and establishing the uncertainty of the temperature measurements using the NIST calibration wafer.

We are using the NIST Test Bed to perform inter-comparisons between the TFTCs and LPRTs. The aims are (a) to demonstrate calibration procedures for and establish uncertainties of the LPRTs against the TFTCs, and (b) to establish

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Staff-Years (FY 2001):
3 professionals
0.25 technician

Funding Sources:
STRS (100 %)

uncertainties for model-corrected LPRTs calibrated against blackbodies. Experimental studies are being designed for these conditions: a range of wafer and film emissivities, variable separation distance between wafer and LPRT, and variable chamber wall reflectance. These studies require concurrent efforts to develop and validate radiation heat transfer models to estimate wafer effective emissivities that are essential for establishing uncertainty limits for LPRTs in our test bed, and in production tools.

DELIVERABLES: Quantification of emissivity effects on calibration wafers with model to correct LPRT calibrations in situ.

We are using industrial RTP test beds to establish the usefulness of the NIST calibration wafer in the semiconductor processing industry and to define the benefits of using the NIST calibration wafer under various industrial conditions.

A cooperative project with ISMT and the University of Texas at Austin (UT-Austin) uses their RTP test bed, which has very high uniformity in wafer temperatures and can be used to confirm the uncertainties and repeatability of the NIST calibration wafer. Their test bed also is used to compare the NIST wafer with commercial thermocouple test wafers and industrial lightpipe radiation thermometers.

DELIVERABLES: NIST TFTC calibration wafers for ISMT test bed and joint report with UT-Austin on LPRT calibrations.

A cooperative project with Vortek industries is permitting us to investigate the use of the NIST calibration wafer in a cutting edge RTP tool that has the fastest ramp rates in the industry. This tool has cold blackbody walls and extremely high heat flux gradients and is not suitable for commercial thermocouple temperature measurements. The NIST thin-film thermocouple calibration wafer has demonstrated unique capabilities in this pulse anneal system.

DELIVERABLES: NIST TFTC calibration wafers for pulse anneal RTP and joint report with Vortek on LPRT calibrations.

We are collaborating with EMCORE, a semiconductor device fabricator, to establish methodologies for making model-corrected radiation thermometry measurements during a deposition process. The goal of the collaboration is to demonstrate a mix of technologies suitable for EMCORE to establish traceability to the ITS-90 with known uncertainties. The work involves detailed characterization of radiation thermometers and commercial blackbodies, measurement of reflectance standards, and application of thermal radiation effective-emissivity models previously developed by our project team. One aim of the work is to demonstrate the reduction in temperature uncertainty that is possible using a calibrated radiation thermometer in place of the contact sensor (thermocouple) to establish linkage to the ITS-90.

DELIVERABLES: Demonstration of improvements in temperature measurement uncertainty that can be achieved using well characterized blackbodies and properly calibrated radiation thermometers with appropriate thermal models of tool chambers.

This year's Common Interest Group (CIG) meeting scheduled as a satellite event to the 9th International Conference on Advanced Thermal Processing of Semiconductors (Sept. 24-28, 2001, Anchorage, AK) was cancelled because of the national emergency. This meeting was to feature two major themes: reports by our industrial collaborators on test wafer demonstration experiments, and discussions on proposals to establishing emissivity-standard-wafers. The purpose for the latter theme was to identify requirements and design a research plan. The topic of emissivity standard-wafers has been discussed annually since 1997. With the development of a new high temperature emissometer having a world-class accuracy of 0.5%, the means to perform the prerequisite reference-grade measurements will be available to our project by the start of FY03. Our plan is to convene the CIG at the May 2002 meeting of the ElectroChemcial Society to deal with the themes.

Accomplishments

Emissivity Effects

- We investigated the effect of different silicon wafer emissivities and the effect of low emissivity films on RTP wafer temperature measurements using LPRTs. These tests were performed in the NIST RTP Test Bed. We used a NIST TFTC calibration wafer to calibrate the LPRTs *in situ*. The measurements of LPRTs viewing Au and Pt thin-film spots in the center of the wafer were compared to LPRT radiance temperature readings that viewed bare Si/SiO_2. We found differences of up to 36 °C at 900 °C in the LPRT measurements due to the low emissivity films. A model of the wafer temperature measurement was presented to provide an insight into the effects of wafer emissivity on LPRT measurements in RTP tools.

Thermal Model

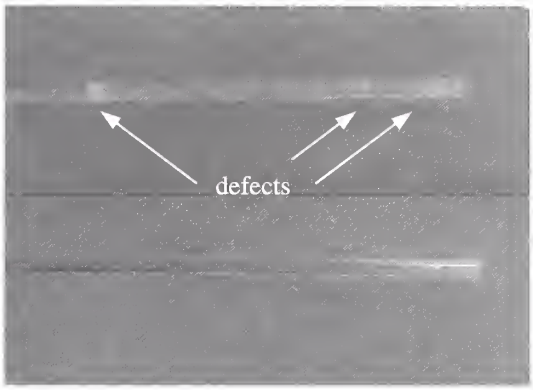
■ A thermal model of the wafer and cold shield enclosure has been developed and employed to predict the effects of NIST Test Bed chamber features on LPRT measurements. The thermal response of the wafer was predicted for different thin-film spot, wafer emissivity, and shield reflectivity. The thin-film spot resulted in a temperature rise at the center of the wafer and its magnitude is strongly dependent on the shield reflectivity and less dependent on the wafer emissivity. The effects of the lightpipe sensor on the temperature distribution of the wafer were also investigated. Due to its low reflectivity compared with the cold shield, the lightpipe sensor caused a temperature decrease at its viewing area, which is a strong function of the shield reflectivity.

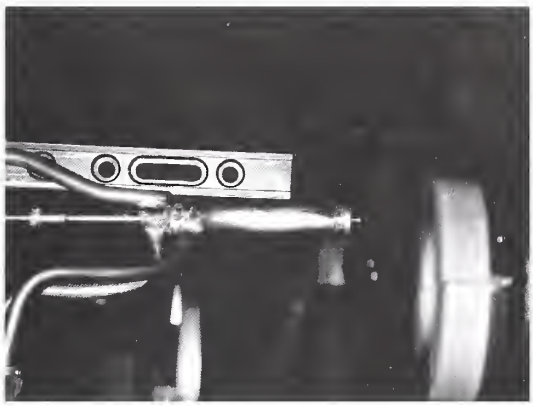
ISMT Wafer Evaluation

■ We have redesigned the calibration wafer for ISMT after the preliminary results have been released by UT-Austin on the test results of the first two wafers. Two designs are in progress. The first new design for a double pattern was fabricated and tested at NIST and sent to ISMT. They reported the results of the testing at the RTP 2001 International Symposium. The NIST wafer with 9 operating thermocouples (6 thin film TCs and 3 wire TCs) showed that the uniformity of their wafer heating was within 2.5 °C. The second new design is for a sandwich wafer which will have Sensarray thermocouples in submerged grooves as well as 12 NIST TFTCs and 4 NIST wire TCs. This complex wafer is a collaborative effort of NIST, ISMT, UT-Austin, Carl Suess, and Sensarray. The thin films on the sandwich wafer will be deposited in the Fabrication Technology Division thin film facility.

VORTEK Wafer Evaluation

■ Five wafers were delivered to Vortek and four have been tested. We redesigned our calibration wafer because of the extremely high heat transfer fluxes in the Vortek chamber. The new design was developed using the excellent Vortek capabilities of mapping the temperature of the wafer. We have improved the thin film pattern to minimize thermal distortion caused by the thin films. Significant improvement was measured after the first design change and further improvements were made with the third wafer. The fourth wafer was tested on July 5-7 in Vortek's new spike anneal RTP tool. This instrumented wafer compares the thin-film thermocouple outputs to two of Vortek's radiometers. The plan includes a comparison to calibrated radiometers (0.95 μm and 1.45 μm) in the near future.





PHOTOGRAPH (UPPER) OF VISUAL COMPARISON BETWEEN A LIGHTPIPE WITH IMPERFECTIONS (TOP) AND A QUALITY LIGHTPIPE (BOTTOM). PHOTOGRAPH (LOWER) OF CALIBRATING A LIGHTPIPE IN WATER COOLED JACKET AND VIEWING SODIUM HEAT PIPE BLACKBODY AT 900 °C.

Lightpipe Characterization

■ Our objective was to investigate improved procedures for characterization and calibration of sapphire lightpipes using uniform blackbody sources. We evaluated spectral, spatial, and temporal characterizations of LPRTs to obtain critical information on effective wavelength and field of view, as well as stability information required for making accurate temperature measurements and uncertainty assessments. We reported guidelines for making qualitative and quantitative inspections of the sapphire lightpipes. Proper inspections of the lightpipes can assist the user in identifying lightpipes that will have poor performance before using them in RTP tools. We also compared "cold" calibrations done in less than 5 s and "hot" calibrations taking about 30 min and discovered that the difference between "cold" and "hot" calibrations can be as

much as 2.5 °C in some situations. We offered caution for utilizing information received in factory calibration reports. A comparison of three vendors showed that the differences between the factory calibration and the NIST calibration were as much as 7.6 °C. We disseminated a list of recommendations for the lightpipe user to assist them in performing more useful characterizations and accurate calibrations.

Thermal Modeling with Non-Smooth Wafers

■ A Monte-Carlo based, radiation thermal model was developed to simulate wafer-chamber radiative process and to predict the wafer effective emissivity required to perform accurate, model-corrected radiometric temperature measurements. The wafer-chamber arrangement is comprised of a silicon wafer, a guard ring, a cold reflective shield, and a guard tube. A true-effective emissivity considering the limited numerical aperture of the light pipe was defined. The calculation showed that the true effective emissivity could be different from the hemispherical effective emissivity and is the appropriate parameter for correcting light-pipe radiation thermometer readings. The wafer reflectance behavior was represented by combinations of specular and diffuse components. The reflectance behavior from rough wafer surfaces is more complicated. For such situations, the bi-directional distribution function (BRDF) is more appropriate as it describes the detailed angular distribution of the reflected energy. Based upon earlier BRDF measurements on representative wafers, different types of BRDFs are being implemented in the Monte-Carlo model code. In the next-generation model under development using actual BRDFs, we expect the roles of guard tube and guard ring specular surfaces to be more prominent. These surfaces have notable effects on LPRTs located near the wafer center, but will cause markedly different radial distributions of the true effective emissivity. The results of the model will be important for improving our understanding of NIST Test Bed TFTC-LPRT intercomparison as well as for correcting multi-point temperature measurements across the wafer radius.

Recent Publications

K. G. Kreider and G. J. Gillen, High Temperature materials for thin-film thermocouples on silicon wafers, accepted for publication in *Thin Solid Films*, July 7, 2000.

K.G. Kreider, D.P. DeWitt, C.W. Meyer, and V.P. Scheuerman, "Calibration of Light-Pipe Radiation Thermometers in an RTP Tool at 1000 °C with an uncertainty of 2 °C," *Eighth International Conference on Advanced Thermal Processing of Semiconductors - RTP'00*, pp 64-70, September 2000, Gaithersburg, MD.

B.K. Tsai, C.W. Meyer, F.J. Lovas, "Calibration and Characterization of Light-Pipe Radiation Thermometers for the NIST RTP Test Bed," *Eighth International Conference on Advanced Thermal Processing of Semiconductors - RTP'00*, pp 83-93, September 2000, Gaithersburg, MD.

Y.H. Zhou, Y.J. Shen, and Z.M. Zhang (University of Florida), B.K. Tsai and D.P. DeWitt, "Effect of Directional Properties on the Radiometric Temperature Measurement in Rapid Thermal Processing," *Eighth International Conference on Advanced Thermal Processing of Semiconductors - RTP'00*, pp 94-103, September, 2000, Gaithersburg, MD.

Y.H. Zhou, Shen, Y.J., Zhang, Z.M., Tsai, B.K., and DeWitt, D.P., "Monte Carlo Simulation for Radiometric Temperature Measurement in Rapid Thermal Processing," to be published in *The 2000 International Mechanical Engineering Congress & Exposition,* Orlando, FL, November 4-7, 2000.

B.K Tsai, and D.P. DeWitt, "Methods used at NIST to Characterize and Calibrate Lightpipe Radiation Thermometers," TEMPMEKO 2001, *The Eighth Symposium on Temperature and Thermal Measurements in Science and Industry*, Berlin, Germany, June 19-21, 2001.

C.W. Meyer, "Effects of Extraneous Radiation on the Performance of Light Pipe Radiation Thermometers," TEMPMEKO 2001, *The Eighth Symposium on Temperature and Thermal Measurements in Science and Industry*, Berlin, Germany, June 19-21, 2001.

K.G. Kreider, D.W. Allen, D.H. Chen, D.P. DeWitt, C.W. Meyer, and B.K. Tsai, "Effects of Wafer Emissivity on Light Pipe Radiometry in RTP Tools," *Ninth International Conference on Advanced Thermal Processing of Semiconductors - RTP'00*, pp 163-168, September 2001, Anchorage, AK.

Y.H. Zhou, and Z.M. Zhang, (University of Florida, Gainesville, FL), D.P. DeWitt and B.K. Tsai, "Effects of Radiative Property of Surfaces on Radiometric Temperature Measurement," *Ninth International Conference on Advanced Thermal Processing of Semiconductors - RTP'00*, pp 179-188, September 2001, Anchorage, AK.

Plasma Process Metrology

Goals

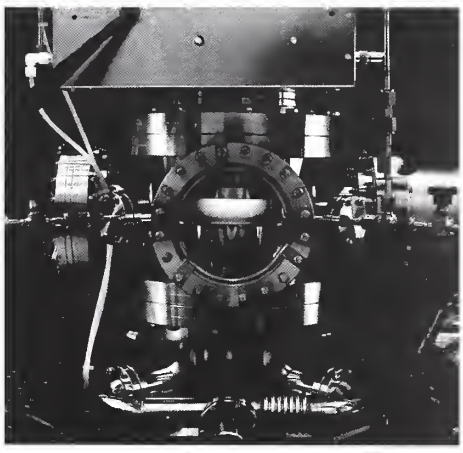
To provide advanced measurement techniques, data, and models needed to characterize plasma etching and deposition processes important to the semiconductor industry, enabling continued progress in model-based reactor design, process development, and process control.

Customer Needs

To fabricate future generations of devices, the semiconductor industry requires improvements in plasma etching and deposition processes. Plasma processes and equipment face increasingly stringent requirements due to the need to maintain high device yields at decreasing feature sizes, the introduction of new dielectric materials, and the constant pressure to keep production efficiency high. To meet these challenges, the International Technology Roadmap for Semiconductors (ITRS-99) identifies a need for better predictive system modeling. To obtain more reliable predictions of the chemical, physical, and electrical properties of processing plasmas, further progress in model development and validation is required. ITRS-99 also identifies a need for improvements in intelligent process monitoring and control, which require the development of robust and reliable sensors that are compatible with manufacturing equipment.

Technical Strategy

Our multifaceted program provides numerous outputs to assist our customers, including advanced measurement methods, high-quality experimental and fundamental data, and reliable, well-tested models of plasma behavior.



ONE OF THE INDUCTIVE, HIGH-DENSITY PLASMA REACTORS USED IN OUR EXPERIMENTAL STUDIES.

First, we develop and evaluate a variety of *measurement techniques* that provide industry and academia with methods to characterize the chemical, physical, and electrical properties of plasmas. The techniques we develop include improved laboratory diagnostic measurements for use in research and development, as well as more robust, non-perturbing measurements for use in process monitoring and control in manufacturing applications.

DELIVERABLES: Improved laboratory diagnostic measurement techniques.

DELIVERABLES: Robust, non-perturbing measurement techniques for process monitoring and control.

Second, we provide *data* necessary for gaining an understanding of complex plasma properties and for testing and validating plasma models. The data help semiconductor manufacturers and plasma equipment manufacturers to better understand and control existing processes and tools and help them to develop new ones. The experimental data we provide are measured under well-defined conditions in highly-characterized standard plasma reactors. We also assess, evaluate, and measure fundamental data that describe important collision processes in reactive plasmas. Recommended values for fundamental data provided by NIST greatly assist plasma modelers throughout industry and academia to improve the accuracy of their simulations.

DELIVERABLES: High-quality experimental data needed to validate plasma models and increase understanding of plasma processes.

DELIVERABLES: Recommended values of fundamental data for use in plasma simulations.

Finally, we are also engaged in the development and validation of plasma *models*. Such efforts concentrate on modeling of plasma sheaths, the thin regions at the boundary of the plasma. Sheaths play a dominant role in determining discharge electrical properties and the properties of the highly energetic ions that are necessary for plasma etching. More accurate sheath models are needed to better predict and optimize discharge electrical characteristics and ion kinetic energies. Sheath models are also used to develop new types of process monitoring techniques based on radio-frequency electrical measurements.

DELIVERABLES: Accurate, validated models of plasma sheaths that can predict plasma electrical properties and ion energies.

Technical Contact:
M. Sobolewski
K. Steffens
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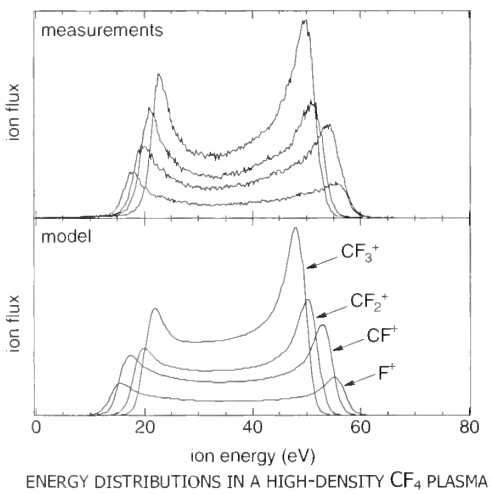
Y. Wang
L. Christophorou
A. Goyette
E. Benck

Staff-Years (FY 2001):
5 professionals
.25 students

Funding Sources:
STRS (90 %)
ATP (10 %)

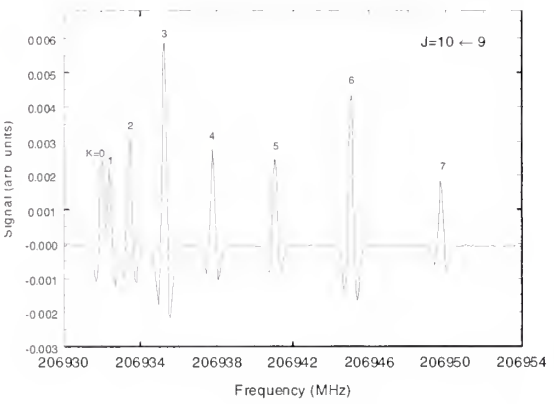
Accomplishments

■ This year we performed a rigorous test of the ability of models to predict ion kinetic energies in high-density plasmas. Energetic ions play a crucial role in plasma etching and other plasma processes. Ions exiting the plasma are accelerated to high energies by strong, radio-frequency electric fields in plasma sheaths, thin regions located at the boundaries of plasmas. The complicated ion dynamics in plasma sheaths are usually modeled using simplifying assumptions that have never been sufficiently validated. Our tests, performed in CF_4 discharges, showed that ion energy distributions predicted by simple, commonly-used, analytical sheath models did not agree with measurements. A more sophisticated model, however, did accurately predict the behavior of measured ion energy distributions and their dependence on frequency, sheath voltage, ion current density, and ion mass. The model, developed at NIST in previous years, can be adapted for use in commercial plasma simulations, and also serves as the basis for new methods for *in situ* monitoring of ion energies at wafers during plasma processing.



ION ENERGY DISTRIBUTIONS IN A HIGH-DENSITY CF_4 PLASMA: MEASUREMENTS (TOP) AND MODEL PREDICTIONS (BOTTOM).

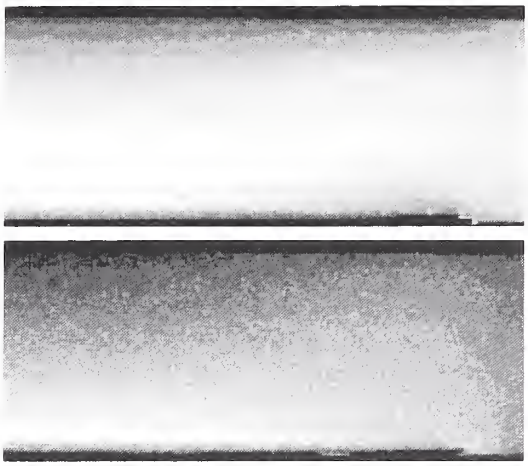
■ For the first time, sub-millimeter wave absorption spectroscopy has been applied to etching type plasmas for the identification and monitoring of plasma species. Sub-mm wave spectroscopy can monitor the crucial chemical species in a plasma and provide the necessary feedback for understanding plasma processing. Initial measurements have concentrated on the use of a backwards wave oscillator (BWO) as the sub-mm wave source. This source is relatively compact and could easily be utilized in an industrial setting. Spectra from ten molecular species have been identified in an inductively coupled plasma reactor, including feed gases (CHF_3, CF_3I), etching radicals (CF_2, CF), etching byproducts (CO, COF_2, SiO, SiF_2, SiF) and contaminants (H_2O). The diagnostic has been used to measure the dissociation of CHF_3 in the plasma and the relative dependence of various plasma species on plasma conditions. Spectral resolution of the BWO is so high that it can also be used to measure the translational temperature of the different plasma species through the Doppler broadening of the absorption line shapes. Gas temperatures are important input parameters to many plasma models since they are necessary to relate the measured gas pressure to the actual particle density in the chamber.



SUB-MILLIMETER WAVE ABSORPTION SPECTRUM OF CHF_3 IN A HIGH-DENSITY, INDUCTIVELY COUPLED PLASMA.

■ Also this year we have extended our capabilities for monitoring spatially-resolved radical densities in fluorocarbon plasmas using 2-D planar laser-induced fluorescence (PLIF) imaging. With the implementation of a tunable wavelength laser, we are now able to obtain PLIF images of the CF radical, in addition to CF_2. Both CF and CF_2 are important precursors for the formation of the fluorocarbon polymer layer which provides selectivity during oxide etching and is the basis for plasma deposition of low-dielectric-constant fluorocarbon films. Currently, measurements of spatially-resolved CF density have been made in CF_4, CF_4/O_2 and C_4F_8 plasmas, investigating the effects of pressure and power, and the presence of oxygen feedgas and silicon wafers. The comparison between CF and our additional results on CF_2 gives insight into the different roles played by the two radicals, providing guidance for selection of precursor and processing conditions. PLIF images of the two radicals also provide a useful data set for

quantitative validation of 2-D plasma simulations.



PLIF IMAGES OF CF_2 (TOP) AND CF (BOTTOM) DENSITY IN A CAPACITIVELY COUPLED DISCHARGE IN 200 MTORR OF CF_4, WITH A SI WAFER ON THE LOWER ELECTRODE.

- One of our capacitively coupled cells has been recently modified to allow operation as a dual frequency system. Dual frequency plasma reactors are becoming of increasing importance to the semiconductor industry, particularly in oxide etching. A new time-resolved optical emission diagnostic based on an intensified CCD camera has been established. Optical emissions due to the main powered electrode are time averaged and subtracted from the images to show the time-resolved perturbations to the plasma from the bias electrode.

- Evaluation of a fiber optic based optical tomography sensor has been completed. Using the sensor we were able to detect plasma nonuniformities in a high-density, inductively coupled plasma reactor. We obtained plasma density maps of excited Ar and C_2 in Ar/CF_4 and Ar/CHF_3 discharges. Unfortunately, the tomography images were subject to systematic uncertainties related to slight variations in the mounting of the optical components. A variety of algorithms were developed to compensate for these variations and improve the quality of the tomography images. However, attaining the 0.1% accuracy required for use on commercial etching reactors is not possible with the existing sensor, which uses monolithic lens arrays. A sensor with individually adjustable optical fibers would be required.

- Absolute, mass-resolved ion fluxes and densities of selected radicals were simultaneously measured in the presence of a silicon wafer in capacitively coupled plasmas generated in processing gases including C_4F_8 and SF_6. The results indicate that the wafer significantly influences the ion and radical composition in each gas as evidence of the complex chemistries present in the etching plasmas. These results are useful to validate and refine reactor modeling codes used in the development of plasma processing methods.

- NIST-recommended data were derived for electron interactions with C_4F_8, a gas with many industrial applications. The review was published in the Journal of Chemical and Physical Reference data. These data were used by industry to improve deep silicon etch processes.

- Measurements and modeling of collision-induced decomposition rates of SF_6^- have been completed in collaboration with researchers at the College of William and Mary.

- We also successfully organized and conducted the Ninth International Symposium on Gaseous Dielectrics in Ellicott City, Maryland.

- Electron drift velocities and effective ionization coefficients were measured and analyzed for C_2F_4. C_2F_4 is a dominant fragment formed in highly dissociated C_4F_8 etching plasmas. These data were required as input parameters for newly developed process models describing C_4F_8 etching processes. The determination of these previously unavailable data enabled the development of a more accurate chemical code describing the primary reactions in C_4F_8 discharges.

FY Outputs & Outcomes

Measurement techniques, data, and models provided by NIST continue to assist our customers in industry to improve their plasma modeling and characterization efforts. Examples from this fiscal year include:

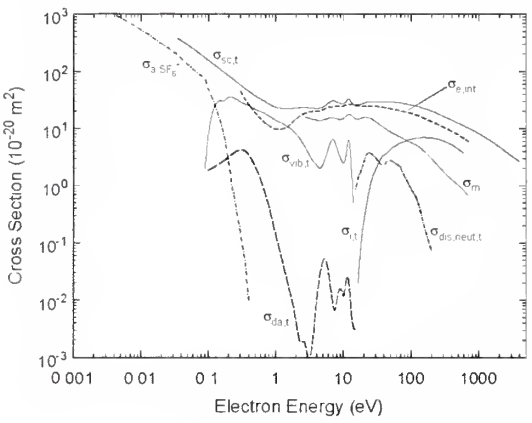
- Mass-resolved ion fluxes and ion energy distributions measured in high density SF_6 plasmas used by Motorola for modeling deep trench etching processes.

- Use of NIST-developed electrical analysis techniques by Novellus to improve tool-to-tool reproducibility.

- A collaboration with Watlow, Inc., to evaluate new methods for wafer temperature measurements in plasma reactors.

- The web-based NIST "Electron Interactions with Plasma Processing Gases" database

(http://eeel.nist.gov/811/refdata/) that distributes fundamental data to plasma modelers throughout industry and academia. This web site has experienced thousands of hits in FY 2001 and tens of thousands of hits throughout its history.



RECOMMENDED ELECTRON CROSS SECTION DATA FOR SF_6 (SHOWN HERE) AND NUMEROUS OTHER PLASMA PROCESSING GASES ARE AVAILABLE ON THE WEB AT HTTP://EEEL.NIST.GOV/811/REFDATA/.

Recent Publications

M. A. Sobolewski, "Measuring the ion current in high-density plasmas using radio-frequency current and voltage measurements," J App. Phys. **90**, 2660-2671 (2001).

R. Champion, I. Dyakov, B. Peko, and Y. Wang, "Collisional decomposition of SF_6^-," J. Chem. Phys. **115**, 1765 (2001).

K. L. Steffens and M. A. Sobolewski, "Investigation and control of spatial characteristics of chamber-cleaning plasmas," in AIP Conference Proceedings **550**, *Proceedings of the 2000 International Conference on Characterization and Metrology for ULSI Technology*, 233-237 (2001).

A. N. Goyette, Y. Wang, and J. K. Olthoff, "Comparison of the identities, fluxes, and energies of ions formed in high density fluorocarbon discharges," in AIP Conference Proceedings **550**, *Proceedings of the 2000 International Conference on Characterization and Metrology for ULSI Technology*, 238-242 (2001).

M. A. Sobolewski, "Monitoring ion current and ion energy during plasma processing using radio-frequency current and voltage measurements," in AIP Conference Proceedings **550**, *Proceedings of the 2000 International Conference on Characterization and Metrology for ULSI Technology*, 263-267 (2001).

E. C. Benck and K. Etamadi, "Fiber optic based optical tomography sensor for monitoring plasma uniformity," in AIP Conference Proceedings **550**, *Proceedings of the 2000 International Conference on Characterization and Metrology for ULSI Technology*, 268-272 (2001).

A. N. Goyette, Y. Wang, and J. K. Olthoff, "Ion compositions and energies in inductively coupled plasmas containing SF_6," J. Vac. Sci. Technol. A **19**, 1294 (2001).

A. N. Goyette, J. de Urquijo, Y. Wang, L.G. Christophorou, and J.K. Olthoff, "Electron transport, ionization, and attachment coefficients in C_2F_4 and C_2F_4/Ar mixtures," J. Chem. Phys. **114**, 8932 (2001).

L. G. Christophorou and J. K. Olthoff, "Electron Attachment Cross Sections and Negative Ion States of SF_6," International Journal of Mass Spectrometry **205**, 27-41 (2001).

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L. G. Christophorou and J. K. Olthoff, "Interactions of Low-Energy Electrons with c-C_4F_8," Journal of Physical and Chemical Reference Data **30**, 449-473 (2001).

Y. Wang, M. Misakian, A. N. Goyette, and J. K. Olthoff, "Ion fluxes and energies in inductively coupled radio-frequency discharges containing CHF_3," J. Appl. Phys. **88**, 5612-5617 (2000).

M. A. Sobolewski, "Sheath model for radio-frequency-biased, high density plasmas valid for all ω/ω_i," Phys. Rev. E **62**, 8540-8553 (2000).

Phase Identification from sub 200 nm particles by electron backscatter diffraction (EBSD)

Technical Contact:
Eric Steel
John Small

Staff-Years (FY 2001):
0.5 professional

Funding Sources:
STRS (100 %)

Goals

To develop methods to improve the quality of electron backscatter diffraction patterns from particles less than 200 nm in size and improve identification of contamination particles in semiconductor processing.

Customer Needs

One of the major sources of failure for microelectronics devices is particulate contamination during processing. Identifying the particle allows source identification, control, and increased productivity. EBSD is a new approach for identifying crystalline particles, but has limitations that make it difficult to use for this application. This research is aimed at overcoming some of these limitations.

Technical Strategy

We are investigating methods for particle identification in the scanning electron microscope based on electron backscatter diffraction from particles in the 100 nm and above size range. We suspect that the poor pattern quality from submicrometer particles is the result of electron scattering from areas other than the particle of interest. In the case of the very small particles many of the incident electrons exit the particle volume without diffracting and enter the substrate. This not only decreases the intensity of the diffraction signal but also increases the average noise in the EBSD pattern, reducing the signal-to-noise ratio in the pattern to an unacceptably low level.

To test this hypothesis and improve the EBSD pattern quality for submicrometer particles a sample holder was constructed that enables particle mounting on a thin, electron transparent, substrate. The thin substrate should dramatically reduce the noise contribution from electrons that scatter into the substrate and thus improve pattern quality from very small particles.

DELIVERABLES: Develop approaches for applying EBSD to sub 200 nm particles and determine fundamental sources of signal and noise in EBSD as applied to small particles.

Accomplishments

- Using Al_2O_3 test particles, the quality of EBSD patterns from particles mounted on the thin substrates were shown to be clearly superior to the pattern from the same types of particles mounted on bulk substrates and have a high enough signal-to-noise ratio to conduct a phase identification analysis of the particle and identify it as hexagonal Al_2O_3. Future plans include investigating other thin-film compositions and low accelerating voltages to extend the application of EBSD phase identification to particles less than 100 nm in size.

FY Outputs & Outcomes

We have demonstrated the use of EBSD to identify sub 200 nm particles. To do this, a thin substrate method was developed. An understanding of the relative strengths of sources of signal and noise in EBSD patterns of small particles was developed.

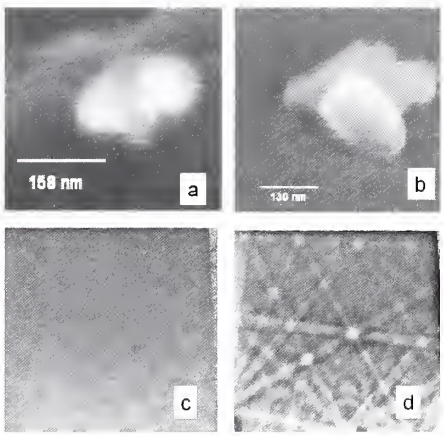

FIGURE C IS THE EBSD PATTERN FROM A 160 NM AL2O3 PARTICLE MOUNTED ON A BULK CARBON SUBSTRATE (FIGURE A). FIGURE D IS THE EBSD PATTERN FROM A 150 NM AL2O3 PARTICLE MOUNTED ON A 20 NM CARBON THIN-FILM (FIGURE B).

Recent Publications

J.A. Small, J.R. Michael, "Phase identification of individual crystalline particles by electron backscatter diffraction (EBSD)," J. of Microscopy, Vol. 201, Pt. 1, Jan 2001, pp. 59-69.

J. Small, J. Michael, Electron Backscatter Diffraction (EBSD) of Sub 500 NM Particles, Proceedings of the Microscopy and Microanalysis Meeting, Published in M&M V. 7 Suppl. 2, 2001 p. 378.

High Resolution Microcalorimeter X-ray Spectrometer for Chemical Analysis

Technical Contact:
Sae Woo Nam
Gene Hilton
Kent Irwin
David Wollman
David Rudman

Staff-Years (FY 2001):
5 professional
1 contractor
1 student

Funding Sources:
STRS (50 %)
Other Agency (50 %)

Goals

To develop the ability to detect photons with high-energy resolution and near-unity quantum efficiency that will enable new generations of spectroscopic tools to be created. Using these tools, improved energy-dispersive X-ray spectroscopy can be performed to solve a wide range of problems in materials analysis, with a particular focus on the semiconductor manufacturing industry. In semiconductor manufacturing, improved X-ray materials analysis is needed to identify small contaminant particles on wafers and to analyze very thin layers of materials.

Customer Needs

Improved x-ray detector technology has been cited by ISMT's Analytical Laboratory Managers Working Group (ALMWG, now ALMC) as one of the most important metrology needs for the semiconductor industry. In the Metrology Roadmap section of the 1997 National Technology Roadmap for Semiconductors (NTRS), improved x-ray detector technology is listed as a key capability that addresses analysis requirements for small particles and defects. The transition-edge sensor (TES) microcalorimeter x-ray detector developed at NIST has been identified as a primary means of realizing these detector advances, which will greatly improve in-line and off-line metrology tools that currently use semiconductor energy-dispersive spectrometers (EDS). At present, these metrology tools fail to provide fast and unambiguous analysis for particles less than approximately 0.1 μm to 0.3 μm in diameter. Improved EDS detectors such as the TES microcalorimeter are necessary to extend the capabilities of existing SEM-based instruments to meet the analytical requirements for future technology generations. To make this technology available to the semiconductor industry and other materials analysis communities, NIST has licensed several patents to two U.S. companies, EDAX and NORAN, for commercialization. With commercialization and continued development, microcalorimeter EDS should be able to meet both the near-term and the longer-term requirements of the semiconductor industry for improved particle analysis.

Promising new technology such as high energy resolution X-ray detectors must be rapidly commercialized. ***1999 International Technology Roadmap for Semiconductors***

Technical Strategy

Introducing a radically new technology such as cryogenic microcalorimeters to a large community requires creating and demonstrating an entire measurement instrument, not just the detector. In addition to developing revolutionary x-ray detectors, we have developed superconducting electronics to read the detectors, compact adiabatic demagnetization refrigerators to simplify cooling the detectors to milliKelvin operating temperatures, and room-temperature electronics to process the output signals. Our goal is to develop new detector systems and to apply those systems to problems of interest to our customers.

DELIVERABLES: Provide the Chemical Science and Technology Laboratory (CSTL) of NIST with a complete prototype system for collaborative use in studying problems of interest to our customers.

DELIVERABLES: Provide techology transfer support to the NIST licensees commercializing this technology.

In the area of X-ray spectroscopy, the performance target depends on the application. For many semiconductor materials analysis problems, further improvements in energy resolution (beyond that already demonstrated with these detectors) are not as important as an increase in the maximum count rate and collection area. This can be achieved by the creation of multipixel arrays of detectors. In addition to the fabrication difficulties in making such arrays, the cold- and room temperature electronics to read out the arrays must also be created. The current approach to the electronics is to develop a superconducting quantum interference device (SQUID) multiplexer (MUX) circuit to read the array, and room-temperature digital signal processing (DSP) to process the MUX signals.

We are developing a small array of microcalorimeter detectors for X-ray analysis to be read out using SQUID MUX and DSP circuitry. The application of X-ray detectors to materials-analysis problems represents a test bed for this technology. With a focus towards the semiconductor manufacturing industry, problems in characterization of small particles and very

thin layers of material are very important. The ability of the detector to differentiate overlapping X-ray lines at low energies enables analysis of previously inaccessible systems.

DELIVERABLES: Fabricate, instrument and test a small array of x-ray microcalorimeter detectors to demonstrate the increase in collection area and count rate achievable through arrays.

For some materials-analysis applications improvements in the energy resolution at relatively high X-ray energies (6000 eV) are still needed. In addition, large-format, densely packed arrays of detectors are required for imaging. Novel fabrication techniques will need to be developed to make densely packed arrays, and SQUID MUX and DSP circuitry will be required to read out the arrays.

DELIVERABLES: Develop improved bulk and/or surface micromachining techniques to allow fabrication of dense packed arrays of detectors.

Accomplishments

■ The schematic in Fig. 1 shows a microcalorimeter energy-dispersive spectrometer (EDS) X-ray detector system inserted into a scanning electron microscope to allow chemical microanalysis of materials.

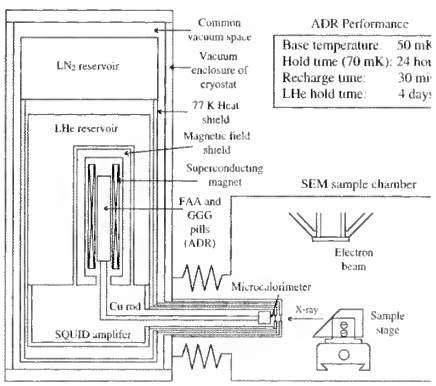

FIG. 1: SCHEMATIC OF A MICROCALORIMETER ENERGY-DISPERSIVE SPECTROMETER (EDS) X-RAY DETECTOR SYSTEM INSERTED INTO A SCANNING ELECTRON MICROSCOPE.

■ The microcalorimeter detector uses a Mo/Cu superconducting/normal-metal bilayer to create a superconducting transition-edge sensor (TES). The use of Mo/Cu has allowed whole-wafer photolithographic processing to fabricate large numbers of detectors. The TES and appropriate X-ray absorber are fabricated on a Si_3N_4 micromachined membrane to produce the required thermal isolation. The device operates using a current bias and extreme negative electrothermal feedback, so that it self-regulates in temperature. Absorbed X rays produce heat pulses in the device, which are read out as pulses of reduced bias current by a first-stage, single-SQUID amplifier located adjacent to the detector to minimize inductance. The output of the first-stage SQUID is read out via a unique 100-SQUID amplifier invented and fabricated by the Project specifically to allow direct coupling of the signal to room-temperature electronics. The detector is cooled to below 100 mK by a compact adiabatic demagnetization refrigerator, which has unique design features that produce nearly 24 hs of continuous operation, and days of hold time for liquid helium.

■ This system holds the world record for energy resolution for an EDS detector of 2.0 eV at 1500 eV, which is over 30 times better than the best high resolution semiconductor-based detectors currently available as can be seen in Fig. 2. This figure compares an X-ray spectrum obtained with this system to that from a semiconductor EDS, clearly demonstrating the remarkable improvement in resolution. The specimen was a glass prepared by Dale Newbury of NIST to use as a test standard for EDS. We have used the system to identify sub-micrometer particles of

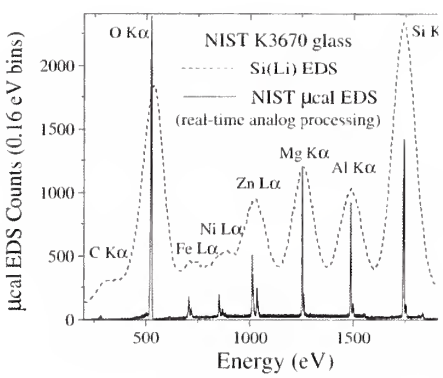

FIG. 2: COMPARISON OF RESOLUTIONS OF NIST MICRO-CALORIMETER EDS TO STANDARD SEMICONDUCTOR EDS.

materials such as W on Si substrates, an identification problem that is impossible with standard EDS detectors and of great importance to the semiconductor industry. It has also demonstrated energy shifts in the EDS X-ray spectra of materials such as Al, Fe, and Ti, depending on their chemical bonding state, thus allowing differentiation between a particle of Al and Al_2O_3, for example.

■ In collaboration with researchers at Lucent Technologies in Orlando, Florida, we compared the trace Cu detection ability of microcalorimeter-based X-ray analysis with that of other industrial analytical techniques (see Fig. 3), including conventional semiconductor EDS, Auger Elec-

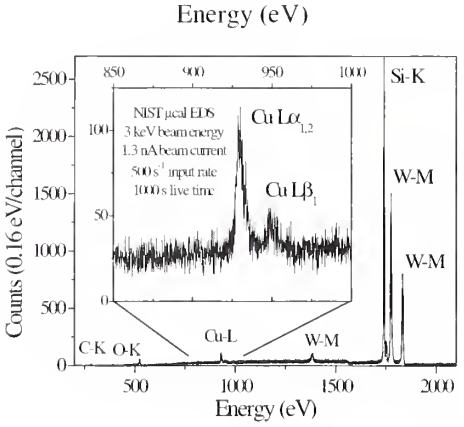

FIG. 3. A MICROCALORIMETER EDS SPECTRUM OF 0.7 % BY WEIGHT CU/AL ALLOY THIN FILM (FROM LUCENT TECHNOLOGIES) DEMONSTRATING THE SENSITIVITY OF MICROCALORIMETER EDS FOR TRACE CU ANALYSIS IN THE SEMICONDUCTOR INDUSTRY.

tron Spectrometry, and Secondary Ion Mass Spectrometry (SIMS). Although only SIMS is capable of trace Cu analysis down to the ≈ 0.02 % atomic level, microcalorimeter EDS fared very well in comparison with the other non-destructive analytical techniques.

■ More advanced applications of this technology to materials-analysis problems requires coupling the spectrometer to state-of-the-art analytical tools. The spectrometer used in the above research has been relocated to CSTL in Gaithersburg. Installation will be completed once a new detector is available, and the system will be used to continue microanalytical work on problems of interest to the semiconductor and other materials-intensive industries.

FY Outputs & Outcomes

■ "Particle Calorimeter with Normal Metal Base Layer," patent issued June 1997.

■ "Mechanical Support for a Two Pill Adiabatic Demagnetization Refrigerator," patent issued August 1999.

■ "Superconducting Transition-Edge Sensor," patent issued March 1999.

■ "Microcalorimeter X-ray Detectors with X-ray Lens," patent issued March 1999.

■ "Superconducting Transition-Edge Sensor with Weak Links," patent application filed November 1998.

■ "The Use of Superconductor-Insulator-Normal (SIN) Tunnel Junctions in Superconducting Quantum Interference Device (SQUID) Multiplexers," disclosure submitted April 2000.

Recent Publications:

Geer, R.E.; Wu, D.; Wollman, D.A., "High-resolution EDS Analysis of Ultra-Thin TaSiN Diffusion Barriers for Cu Metallization Using Microcalorimetry," Proc. IEEE 2001 Int'l Interconnect Tech. Conf., 192-194 (2001).

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Irwin, K.D.; Hilton, G.C.; Martinis, J.M.; Deiker, S.; Bergren, N.F.; Nam, S.W.; Rudman, D.A.; Wollman D.A, "A Mo-Cu Superconducting Transition-Edge Microcalorimeter with 4.5 eV Energy Resolution at 6 keV," Nuclear Instrum. and Methods in Physics Research A 444, 184-187 (2000).

Wollman, D.A.; Nam, S.W.; Newbury, D.E.; Hilton, G.C., Irwin, K.D.; Bergren, N.F.; Deiker, S.; Rudman, D.A.; Martinis,J.M., "Superconducting Transition-Edge-Microcalorimeter X-ray Spectrometer with 2 eV Energy Resolution at 1.5 keV," Nucl. Instrum. and Methods in Phys. Res. A 444, 145-150 (2000).

Calculation of Tc in a Normal-Superconductor Bilayer Using the Microscopic-Based Usadel Theory, Martinis, J.M.; Hilton, G.C.; Irwin, K.D.; Wollman, D.A., Nucl. Instrum. and Methods in Phys. Res. A 444, 23-27 (2000).

Wollman, D.A.; Nam, S.W.; Hilton, G.C.; Irwin, K.D.; Bergren, N.F.; Rudman, D.A.; Martinis, J.M.; Newbury, D.E., "Microcalorimeter Energy-Dispersive Spectrometry Using a Low Voltage Scanning Electron Microscope," J. Microscopy 199, 37-44 (2000).

Nam, S.; Wollman, D.A.; Hilton, G.C.; Chervenak, J.; Deiker, S.; Irwin, K.D.; Martinis, J.M., "A Digital Readout Scheme for Arrays of Microcalorimeter X-ray Detectors," Proc. Microscopy and Microanal. 2000, 742-743 (2000).

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J. A. Chervenak, K. D. Irwin, E. N. Grossman, J. M. Martinis, C. D. Reintsema, M. E. Huber, "Superconducting Multiplexer for Arrays of Transition Edge Sensors," Appl. Phys. Lett. 74, 4043 (1999).

C. K. Stahle, D. McCammon, K. D. Irwin, "Quantum Calorimetry," Physics Today 52, 32 (1999).

Modeling, Measurements, and Standards for Wafer Surface Inspection

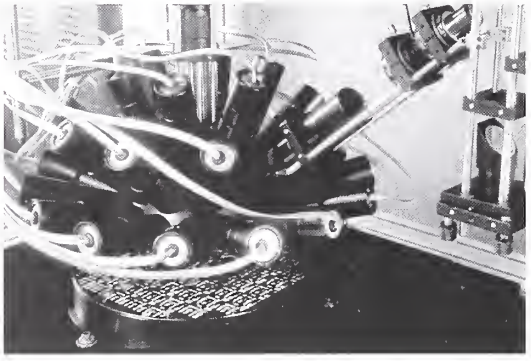
Technical Contact:
Thomas A. Germer
George W. Mulholland

Staff-Years (FY 2001):
1.6 professional
0.25 technician
1.0 guest researcher

Funding Sources:
STRS (99 %)
Other Agency(1 %)

Goals

Provide industry with models, measurements, and standards for particles and other defects in order to improve the inspection of wafer surfaces. Develop facilities to accurately measure particle size and to deposit monosize particles on calibration artifacts to reduce the uncertainty in the sizes of particles used by the semiconductor industry to calibrate scanning surface inspection systems (SSIS). Investigate theoretically and experimentally the behavior of light scattering from particles, defects, and roughness on wafer surfaces.



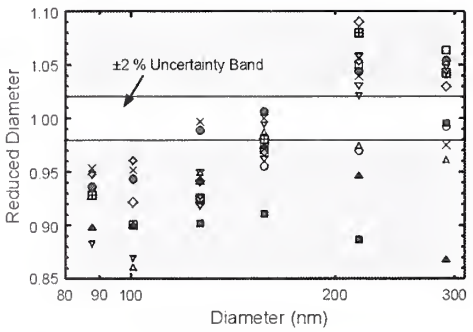
THE MULTIDETECTOR HEMISPHERICAL POLARIZED OPTICAL SCATTER INSTRUMENT WAS DESIGNED TO DEMONSTRATE HOW POLARIZED LIGHT SCATTER METHODS COULD BE USED TO IMPROVE DEFECT CLASSIFICATION ON WAFER SURFACES.

Customer Needs

The Semiconductor Industry Association's (SIA) International Technology Roadmap for Semiconductors identifies the detection and characterization of defects and particles on wafers to be a potentially show-stopping barrier to device miniaturization. The roadmap specifies that by 2005, 30 nm particles must be detectable on bare silicon and nonmetallic films, 39 nm particles on metallic films, and 100 nm particles on wafer backsides, for which no solutions currently exist. While the detection sensitivity for defects must be increased, the ability to characterize defects in terms of size, shape, composition, etc., is critical for yield-learning. Defects must be characterized independent of defect location and topology.

With the need to detect smaller defects, the costs of inspecting wafers are skyrocketing. In order for new advances to be implemented in production environments, improvements in sensitivity must be achieved without suffering a tradeoff in throughput and must be cost-effective. The drive towards in-situ sensors for production tools requires techniques which can be effectively miniaturized.

In order that wafer manufacturers and device manufacturers have a common basis for comparing specifications of particle contamination, improved standards for particles are needed. A recent comparison of the measurements of calibration wafers by thirteen different SSISs indicated unacceptably large deviation between the SSIS results and the actual particle sizes. This study involved six particle sizes ranging from 88 nm to 290 nm and included the NIST SRM 1963 and two other sizes measured by NIST. For the two smallest particle sizes, 88 nm and 100.7 nm, the scanners systematically underestimated the size by about 8 %. By 2005, it is anticipated that accurate calibration particles as small as 30 nm will be needed.



RESULTS FROM A ROUND ROBIN SHOW DISAGREEMENTS BETWEEN DIFFERENT USERS' MEASUREMENTS OF SIX SIZES OF POLYSTYRENE SPHERES ON BARE SILICON WAFERS. THE DATA FOR TWO OF THE SIZES LIE OUTSIDE THE UNCERTAINTY FOR THE PARTICLES.

Technical Strategy

There are two major strategies to improving the performance of scanning surface inspection systems. One strategy is to develop a fundamental understanding of optical scattering at surfaces so that tool manufacturers can optimize the performance of their instrumentation, in terms of defect detection limits and discrimination capabilities, to characterize the response of instrumentation to different types of defects, and to develop and calibrate particles of well-defined size and material. Recent work by this group has demonstrated that the polarization of light scattered by particulate contaminants, subsurface

defects, and microroughness has a unique signature that can be used to identify the source of scatter. In particular, it was found that small amounts of roughness do not depolarize scattered light. This finding has enabled the development of instrumentation which can collect light over most of the scattering hemisphere, while being blind to microroughness. That instrumentation, for which a patent has been awarded and for which a major manufacturer of wafer inspection systems has licensed, should result in a factor of two improvement in minimum detectable defect size.

A second strategy is to provide leadership in the development of low uncertainty calibration particles for use in calibrating surface scanners. A major focus has been development of the differential mobility analysis (DMA) method for accurately sizing monosize polystyrene spheres. This work together with a SSIS round robin has provided evidence that current SSIS measurements have an unacceptably large uncertainty for particle sizes in the 90 nm to 100 nm size range. The technical focus of our future work will be applying the DMA for accurately sizing calibration particle sizes as small as 30 nm, developing methods for generating other types of monosize particles, and the evaluation of light scattering techniques for calibrating these particles on wafer surfaces.

Specific project elements are defined below:

Theoretical Light Scattering Calculations – The focus of our theoretical work is on (a) developing models that accurately predict the polarization of scattered light, and (b) determining what information can be efficiently and accurately extracted from light scattering measurements. Approximate theories are used in conjunction with more complex finite element time-domain and discrete-dipole approximation techniques to gain an understanding of which parameters affect the light scattering process. Particular cases that are being analyzed include (a) scattering by defects and roughness associated with dielectric layers, (b) scattering by particulate contamination on bare wafers, and (c) scattering by high aspect ratio vias.

DELIVERABLES: Publish and distribute via SCATMECH software library theoretical models for light scattering from particles, roughness, and defects on wafers.

Polarized Light Scattering Measurements – The Goniometric Optical Scatter Instrument (GOSI) enables accurate measurements of the intensity and polarization of scattered light with a wide dynamic range, high angular accuracy, and multiple incident wavelengths (visible and UV). We measure the light scattering properties of well-characterized samples exhibiting interfacial roughness, deposited particles, subsurface defects, dielectric layers, or patterns. The emphasis is on providing accurate data, which can be used to guide the development of light scattering instruments, and to test theoretical models.

DELIVERABLES: Validate theoretical models with model measurements.

DELIVERABLES: Develop capability of measuring mean size of particles deposited on silicon wafers.

Instrument Development – A second instrument, the Multidetector Hemispherical Polarized Optical Scatter Instrument (MHPOSI) complements the capabilities of GOSI as a prototype for a production-line light scattering inspection tool. An instrument with twenty-eight fixed detection elements covering the scattering hemisphere, MHPOSI enables a determination of the differential scattering cross section, for individual particles or defects on a wafer surface. This instrument can be configured so that it is blind to interfacial roughness. Together with an understanding of the light scattering functions for different imperfections, MHPOSI has a substantially improved capability for rapidly detecting and identifying defects, particles, and microroughness on wafers.

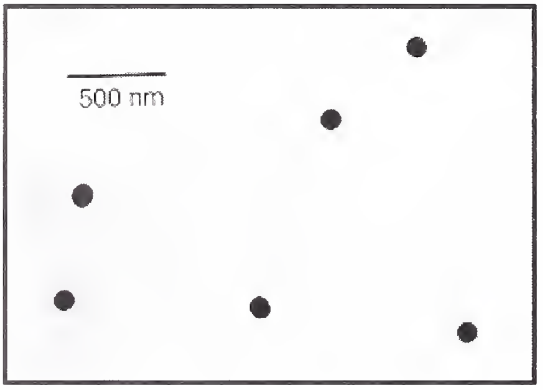
DELIVERABLES: Develop capability to measure size distribution of spherical particles deposited on silicon wafers.

Overlay Metrology by Scattering Ellipsometry Scatterometry has become a popular method for measuring critical dimension (CD) and performing overlay metrology. The addition of polarization information may allow the method, which is usually restricted to one dimension, to be applied to two dimensions. Work performed by this program has shown that roughness of multiple interfaces can be measured simultaneously by light scattering ellipsometry. One application of this technique is the metrology of overlay, whereby small height structures can be measured in two dimensions. This program is evaluating the effectiveness of this method for measuring two dimensional overlay.

DELIVERABLES: Demonstrate measurement of two-dimensional overlay of low-profile features by light scattering ellipsometry.

Size Distribution Measurements - Differential mobility analysis (DMA) has been shown to be capable of making accurate size measurements for the mean particle size for 100 nm monosize polystyrene spheres. There are promising results for the measurement of the size distribution for broader size distributions; however, the results are not quantitative. Work is in progress to quantify the uncertainty in the size distribution measurement and to extend the method to smaller particle sizes.

DELIVERABLES: Develop method for inferring the size distribution parameters of an asymmetric Gaussian by a moment analysis of DMA data.



TRANSMISSION ELECTRON MICROSCOPE IMAGE OF 96 NM COPPER SPHERES GENERATED BY SPRAY PYROLOSIS OF A COPPER PRECURSOR SOLUTION AND SIZE-CLASSIFIED BY A DMA.

Aerosol Generation – An aerosol must be formed typically from a liquid spray of a particle suspension before the particles can be size by the DMA or deposited on a wafer. Work is in progress to use a variety of innovative methods for generating, shaping the size distribution of the aerosol, and depositing the particles. These include the electrospray for generating particle sizes smaller than 60 nm, impactor to remove the large size fraction of the aerosol and to deposit the particles, and an electrostatic chamber for depositing small particle sizes. Work is also in progress to generate copper particles from chemical precursors in a tube furnace.

DELIVERABLES: Demonstrate capability to generate 30 nm polystyrene spheres without agglomerates using electrospray

DELIVERABLES: Develop methods for generating and depositing monosize, spherical copper particles.

Resource on Particle Science – Over the past five years, the particle related work has included projects with SEMATECH and particle suppliers to the semiconductor industry. A number of needs by particle related companies were expressed at the NIST particle workshop including redoing the uncertainty assessments of existing particle SRMs and offering a particle sizing calibration service. Providing support for particle needs critical to the semiconductor industry will continue to be a priority.

DELIVERABLES: Establish a trial phase calibration service for the measurement of peak particle size.

Accomplishments

- Developed a method, based upon scattering ellipsometry, for quantifying scatter from two sources and demonstrated its use by characterizing the roughness of both interfaces of an SiO_2/silicon system. This finding establishes the validity of the light scattering models for roughness in a dielectric film, which in turn limits the detection sensitivity of SSIS instruments. The method was also used to characterize scattering from steel surfaces, demonstrating capability to distinguish between scattering from surface roughness and material inhomogeneity. The method was further used to study the scatter from an anticonformal polymer film, helping to establish the limits of validity of the scattering theory.

- In collaboration with the University of Maryland, developed a method for generating pure copper spheres with diameters ranging from 100 nm to 200 nm. These spheres, which mimic real-world particles better than polystyrene, will be used to validate the particle scattering theory in conditions for which models have a higher degree of uncertainty. Also, developed a method for depositing colloidal gold spheres onto silicon wafers, using a liquid phase process. Measured polarization of light scattered from 100 nm, 150 nm, and 200 nm gold spheres on silicon wafers, and found good agreement between the Bobbert-Vlieger theory for light scattering from a sphere above a surface.

- SCATMECH: Polarized Light Scattering C++ Class Library — Published the SCATMECH library, providing a means for distributing scattering models and polarized light calculations to others. The library provides a common interface for accessing a variety of different scattering models, allowing users to tailor their use of the library to their own light scattering application, whether it be an imaging, polarized, or integrated scatter measurement. From the time of its public availability in March 2000 to the end of July 2001, 393 copies of the library have been downloaded from the web.

Version 2, released in March 2001, adds theories for scattering from dielectric films, while Version 3, due to be released during Fall 2001 will include an exact theory for scattering by a sphere above a surface.

■ Optical Scattering from Metallic Spheres — The scattering of metallic spheres, especially those made of noble metals at wavelengths near their plasmon resonance, provide a challenging and rigorous test for any light scattering theory. During FY2001, monodisperse copper spheres with specific sizes ranging in size from 96 nm to 198 nm, produced using a novel method developed at NIST, were deposited onto silicon wafers. The intensity and polarization of laser light diffusely scattered by these particles were measured using a variety of optical geometries. Theoretical calculations, based upon a theory by Bobbert and Vlieger for scattering by spheres above a substrate, were compared to the data. Implementation of the theory had to be extensively modified in order to ensure robust and accurate convergence of the theory. Comparison of the model with the data yielded excellent results. The implementation of the theory is being made publicly available in the SCATMECH library, a set of scattering codes available from the NIST website. The code can be considered a benchmark by which approximate methods can be compared.

■ A NIST-sponsored workshop entitled "Issues Related to SSIS Calibration with Polystyrene Spheres" brought together suppliers of wafers, reference particles, particle sizing and deposition equipment, and wafer inspection instruments set the stage for developing a more responsive particle program.

■ Determined that the electrospray technique can produce an aerosol having characteristics optimal for transferring particles in a liquid suspension onto wafers for particle diameters as small as 25 nm. This significant finding enables improved wafer depositions by reducing the number of contaminant residue particles, the number of doublets, and the amount of residue on the particles.

FY Outputs & Outcomes

■ Developed robust software implementation of the Bobbert-Vlieger theory for light scattering by a sphere on a surface, validated that theory under challenging conditions, published the results in a conference proceeding, and made the software available publicly on the web.

■ Version 2 of the SCATMECH library of scattering codes was released. This new version includes codes which predict the scattering by roughness and defects in dielectric films. Accurate models for scattering from various interfaces of films are necessary for the testing of designs for post chemical mechanical polishing (CMP) inspection systems.

■ Organized workshop with industrial colleagues entitled "Issues Related to SSIS Calibration with Polystyrene spheres," presented key action items at SEMI Meeting in La Jolla, and changed project focus to address these items.

■ Improved DMA measurement method by developing software for automation of data acquisition/analysis and implemented non-linear fitting algorithm for determining peak size. The improved analysis method has been used for sizing a set of particles from one customer with resulting reduced analysis time and improved consistency of the analysis.

■ Developed the capability to generate and deposit monosize, spherical copper particles. Copper particles of size 100 nm, 150 nm, and 200 nm were deposited and the light scattering by the particles was characterized as a function of angle and polarization state. The excellent agreement with theory suggests that such depositions could be used as calibration artifacts for mimicking real-world conducting type particle contaminants.

Recent Publications

G. W. Mulholland and B. Bauer, "Nanometer Calibration Particles: What is Available and What is Needed?" J. Nanoparticle Research **2**, 5–15 (2000).

K. Ehara, G.W. Mulholland, and R.C. Hagwood, "Determination of Arbitrary Moments of Aerosol size Distribtion from measurements with a Differential Mobility Analyzer," Aerosol Sci. and Tech., **32**, 434–452 (2000).

Thomas A. Germer, "Measurement of Roughness of Two Interfaces of a Dielectric Film by Scattering Ellipsometry," Phys. Rev. Lett. **85**, 349–352 (2000).

Egon Marx, Thomas A. Germer, Theodore Vorgurger, and Byong C. Park, "Angular Distribution of Light Scattered From a Sinusoidal Grating," Appl. Opt. **39**, 4473–4485 (2000).

Thomas A. Germer and Clara C. Asmail, "Microroughness-blind optical scattering instrument," United States Patent 6,034,776, granted March 7, 2000.

Thomas A. Germer, Thomas Rinder, and Hendrik Rothe, "Polarized light scattering measurements of polished and etched steel surfaces," in *Scattering and Surface Roughness III*, Z.-H. Gu, and A. A. Maradudin, Eds., Proc. SPIE **4100**, 148–155 (2000).

Thomas A. Germer, "Characterizing Interfacial Roughness by Light Scattering Ellipsometry," in *Characterization and Metrology for ULSI Technology: 2000 International Conference*, D. G. Seiler, A. C. Diebold, T. J. Shaffner, R. McDonald, W. M. Bullis, P. J. Smith, and E. M. Secula, eds., Proc. AIP **550**, 186–190 (AIP, New York, 2001).

George W. Mulholland, Da Ren Chen, and David Y.H. Pui, "Comparison of the Size Distribution of Polystyrene spheres Produced by Pneumatic and Electrospray Nebulization," in *Characterization and Metrology for ULSI Technology: 2000 International Conference*, D. G. Seiler, A. C. Diebold, T. J. Shaffner, R. McDonald, W. M. Bullis, P. J. Smith, and E. M. Secula, eds., Proc. AIP **550**, 322–326 (AIP, New York, 2001).

Thomas A. Germer, "Polarized light scattering by microroughness and small defects in dielectric layers," J. Opt. Soc. Am. A **18**, 1279–1288 (2001).

Thomas A. Germer, "Comment on 'Large angle in-plane light scattering from rough surfaces,'" Appl. Opt. **31**, 5708–5710 (2001).

Jung Hyeun Kim, Sheryl H. Ehrman, George W. Mulholland, and Thomas A. Germer, "Polarized light scattering from metallic particles on silicon wafers," in *Optical Metrology Roadmap for the Semiconductor, Optical, and Data Storage Industries*, A. Duparré and B. Singh, Eds., Proc. SPIE **4449**, submitted (2001).

Junghyeun Kim, Sheryl H. Ehrman, George W. Mulholland, Eric B. Steel, and Thomas A. Germer, "Method for making spherical pure metal micro and nanoscale powders by spray pyrolysis," Provisional United States Patent, filed January 26, 2001.

Thomas A. Germer, "SCATMECH: Polarized Light Scattering C++ Class Library," online software and document published at http://physics.nist.gov/scatmech. Version 1 online in March 2000, Version 2 online in March 2001, and Version 3 scheduled to be online in December 2001.

Device Modeling, Design, and Test Metrology Program

Device scaling to atomic dimensions and single chip integration exceeding a billion active components requires new concepts in modeling of devices, processes, circuit performance, and thermal management.

The industry needs efficient and reliable simulation methods as device structures continue to evolve rapidly, requiring the addition of quantum mechanical effects. Benchmarking of simulation tools that include quantum mechanical effects is a critical need of the industry.

Rapid changes in packaging, including its integration with chip interconnect is placing new demands in thermal management. Modeling of heat flow is another critical need of the industry.

Lead counts of several thousand per chip and test frequencies in the microwave regime challenge current test methodologies. The overall task is to develop test methodologies to address these new requirements.

Accurate at-speed test methodology of digital integrated circuits is a critical requirement. Traditional methods utilizing IC contact probing technology requires large contact pads incompatible with current IC designs. The development of alternative probing approaches through non-contact and intermittent probing techniques appear very promising. However, to implement these techniques, solving the at-speed test calibration issues is crucial. With the challenges facing designers and the rising costs of development, it is crucial to develop accurate testing strategies.

Metrology for Simulation and Computer-Aided Design

Technical Contact:
Allen R. Hefner, Jr.

Staff-Years (FY 2001):
2.5 professionals
4 guest researchers

Funding Sources:
STRS (100 %)

Goals

The goal of the Project is to facilitate the efficient and reliable application of semiconductor computer-aided design (CAD) tools and System-on-a-Chip (SoC) design methodologies by providing leadership for the development of an industry infrastructure for establishing model accuracy, developing methods for simulator model validation and benchmarking, developing metrology necessary for providing model data and model parameter extraction sequences, and developing metrology infrastructure required for a block-based design paradigm.

Customer Needs

Efficient and reliable simulation methods are becoming more important as device structures and packages rapidly evolve. In addition, higher speed and higher power devices increase the importance of including the effects of packages in system performance simulation. However, advanced device electrical and thermal characterization procedures and validation of models used in computer-aided design tools have not kept pace with the application of the new device types and processes.

Several device technologies have evolved to an extent that conventional modeling and simulation capabilities are not suitable. For example, as Complementary Metal-Oxide Semiconductor (CMOS) devices are scaled to atomic dimensions, simulators must include quantum mechanical (QM) physics. The SRC/NIST/NSF Workshop on Nanoscale Transistors: Technology, Physics, and Simulation (Feb. 1999) identified QM device simulation as an area required for device simulator progress. In addition, the device types used for power and microwave applications can no longer be represented by conventional device models provided in circuit and system simulation programs.

The driving force in today's semiconductor industry is the need to maintain a rate of improvement of 2x every two years in high-performance components. Currently, these improvements rely exclusively on advances made in semiconductor miniaturization technology. The 1999 ITRS (International Technology Roadmap for Semiconductors) suggests that, "innovation in the techniques used in circuit and system design will be essential to maintain the historical trends in performance improvement." Achievement of this advancement in circuit and system design techniques is increasingly becoming dependent on integrating multiple silicon technologies into an SoC. Design challenges for SoC are overcome with the use of block-based design approaches that emphasize design reuse that include Built-In Self Test (BIST) functions and accommodate Design-For-Test (DFT).

Technical Strategy

NIST addresses these needs by developing the theoretical foundations, standards, model validation procedures, and associated experimental techniques for the measurement of device system block electrical and thermal characteristics, and package electrical and thermal characteristics. NIST is developing, with industry, accepted procedures for validating device models for circuit simulation. NIST is developing procedures for characterizing the thermal and electrical performance of micro-electronic packages that are compatible and useful for CAD of boards and systems.

Device and Process Simulation Benchmarking

Accurate models and benchmarking procedures are becoming more important for device and process simulators. Current tasks include development of mobility, band gap, and intrinsic carrier concentration models for accurate simulation of compound semiconductor devices, and benchmarking of semiconductor device simulation tools that include QM effects, including MEDICI, UTQuant, NCSU code, and NEMO.

DELIVERABLES: Complete benchmarking of QM effects in 2-D device simulator for MOSFET (Metal-Oxide Semiconductor Field Effect Transistor) with ultra-thin gate oxide.

Package Thermal Metrology and Models

Accurate and timely simulation of system thermal performance requires new temperature measurement methods, new simulation methodologies, and validation procedures. Current tasks include the NIST electro-thermal network simulation methodology, including thermal network component models for semiconductor packages and heatsinks, and the development of methodologies to validate the performance and accuracy of compact package thermal models.

Compact Device Electrical Models

Only recently has there been a significant effort in developing an infrastructure for validating the performance of compact models. An example of this activity is the NIST/IEEE Model Validation Working Group, founded in 1994 and now having over 200 members from 100 different technical organizations. For more information see ray.eeel.nist.gov/modval.html.

Metrology for Multi-Technology SoC System Blocks

The emergence of the block-based design paradigm that emphasizes design reuse imposes various metrology and standardization challenges. The NIST research provides the metrology infrastructure required to facilitate the emergence of effective SoC design methodologies for multi-technology systems. Current tasks included: (1) development of test structures for multi-technology process monitoring; (2) development of measurement infrastructure to calibrate multi-technology BIST functions for system sub-blocks; (3) development of metrology to validate behavioral models for the multi-technology system blocks; and (4) development of benchmarking procedures for system block, simulation-based Analog Hardware Description Language design.

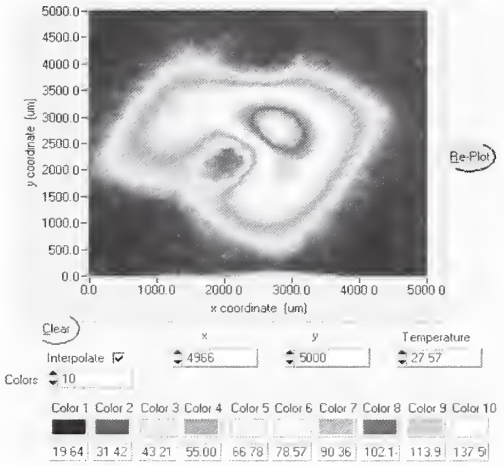
DELIVERABLES: Complete development of test bench on a chip metrology necessary for multi-technology SoC, block-based design, and develop test structures for monitoring multi-technology SoC processes.

Accomplishments

■ Developed SoC test-bench. The test-bench provides the capability of testing multiple device types on a single chip. The system studies the interactions between biosensors, voltage controlled oscillators, and analog to digital converters. The system also studies the effects of post process HF etching on SoC devices. Angela Hodge presented an invited paper discussing this testbench at a special session of the IEEE International Symposium on Circuits and Systems. The purpose of this symposium was to uncover the latest advances in SoC research, bio-sensors, and related systems.

■ Benchmarking 2-D QM simulator, Medici, led to uncovering weaknesses in the simulator. This discovery resulted in Avanti Corporation's decision to improve the model for its most recent release of the software.

■ Developed High-Speed Semiconductor Device Transient Thermal Imaging System. The system provides the capability to measure the transient temperature distributions on the surface of a silicon chip with 10 ns temporal, 15 μm spatial resolution. The system uses computer-control software with a graphical user interface for controlling the translation stages, digitizing oscilloscope, and device test fixture temperature controller. The system also required the development of algorithms for calibrating and extracting the transient temperature waveform from an infrared microscope signal.



SEMICONDUCTOR DEVICE TRANSIENT THERMAL IMAGING SYSTEM CAPTURES FORMATION OF DYNAMIC HOT SPOT.

FY Outputs

Collaborations

■ Avanti Inc., characterization of electronic packages for thermal model library component models (Allen R. Hefner)

■ DELPHI/Virginia Polytechnic Institute and State University, electronic interconnect characterization for vehicle auxiliary motor drive interconnects (Allen R. Hefner)

■ Electricity Division, Jim St. Pierre, collaborating on defining research goals for metrology and benchmarking related to SoC (Angela M. Hodge)

■ Electricity Division, metrology for SoC design reuse (Allen R. Hefner)

■ Electricity Division, metrology and standardization for the use of Virtual Components (VCs) in SoC devices, January 2001 - ongoing (Angela M. Hodge)

■ Semiconductor Electronics Division, Scanning-Probe Microscope Metrology Project, implant simulation and device simulation (Allen R. Hefner)

- Semiconductor Electronics Division, Thin-Film Process Metrology Project/Gate Dielectric and Interconnect Reliability Project, benchmarks for QM device simulation (Allen R. Hefner)

- Aventi, implementation of new device physics into Medici device simulator (Allen R. Hefner)

- University of Maryland, 2-D QM simulator analysis, September 1, 2000-September 30, 2001 (Allen R. Hefner, Angela M. Hodge, and Curt A. Richter)

- University of Maryland, BIST for SoC, September 1, 2000-September 30, 2001 (Angela M. Hodge)

- University of Maryland, metrology for multi-technology SoC (Allen R. Hefner)

- University of Maryland, Professor Neil Goldsman, collaborating on benchmarking QM simulators for semiconductor devices (Angela M. Hodge)

- University of Maryland, Professor Robert Newcomb, collaborating on defining research goals and objectives for NIST/SED initiative on SoC (Angela M. Hodge)

- University of Maryland, QM effects in 2-D semiconductor device simulators (Allen R. Hefner)

- Virginia Polytechnic Institute and State University, package interconnect electrical characterization (Allen R. Hefner)

Standards Committee Participation

- EIA/SEMATECH Compact Model Council (Allen R. Hefner)

- IEEE Electron Devices Society, Standards Technical Committee, Chairman (Allen R. Hefner)

Recent Publications

Hefner, A., Berning, D., Blackburn, D., Chapuy, C., and Bouche, S., A High-Speed Thermal Imaging System for Semiconductor Device Analysis, proceedings of the Seventeenth Annual IEEE Semiconductor Thermal Measurement and Management Symposium, pp. 43-49, 2001.

Hodge, A., Newcomb, R., and Hefner, A., Use of the Oscillation Based Built-in Self-test Method for Smart Sensor Devices, Conference Proceedings - 2001 IEEE International Symposium on Circuits and Systems, vol. 2, pp. 281-284, 2001.

Richter, C. A., Hefner, A. R., and Vogel, E. M., A Comparison of Quantum-Mechanical Capacitance-Voltage Simulators, IEEE Electron Device Letters, vol. 22, no. 1, January 2001, pp. 35-37.

Richter, C., Vogel, E., Hodge, A., and Hefner, A., Differences Between Quantum-Mechanical Capacitance-Voltage Simulators, SISPAD Technical Digest 2001 (2001 International Conference of Simulation of Semiconductor Processes and Devices), 4 p.

At-Speed Test of Digital Integrated Circuits

Goals

Develop and demonstrate metrology for the at-speed test of digital integrated circuits. The program will resolve the essential metrology issues of at-speed digital integrated circuit test. It will apply its results to characterizing and calibrating high-impedance probes, develop atomic force microscopes (AFMs) capable of precisely positioning field probes above the surface of the integrated circuit, and push the current on-chip sampling technologies now being explored by the industry..

Customer Needs

The semiconductor industry needs accurate metrology for the at-speed test of digital integrated circuits ("Grand Challenges", page 11, 1997 National Technology Roadmap for Semiconductors). Traditional IC contact probing technology requires large contact pads incompatible with the operation and economic constraints of modern IC designs. Alternative probing approaches use high-impedance probes, non-contact probes, atomic-force microscopes, electron beams, optical beams, or on-chip samplers that respond to either electric or magnetic fields near transmission lines in the circuits. However, while the uncalibrated field measurements performed by these probing systems are suitable for field mapping, they are a far cry from the precise measurements of voltages and currents required for electrical design.

Solving the critical at-speed test calibration issues will add enormous value to the probing systems currently being used or developed for high-performance digital integrated circuits. Developing characterization and calibration methods for high-impedance probes, whether of the conventional type or mounted on atomic-force microscopes, will help speed the development and implementation of these new measurement tools, and so create a new paradigm for the at-speed test of high-speed digital integrated circuits.

Technical Strategy

We will develop calibration artifacts with precisely known high-frequency voltages and circuits suitable for characterizing and calibrating high-impedance probes and samplers of all types. We will focus on fundamental calibration issues: transforming the response of the probes to the electric and magnetic fields above the integrated circuit into accurate voltages and currents inside the circuit.

We will first apply the characterization and calibration procedures to conventional high-impedance probes, and then to miniature AFM probes suspended on custom cantilevers designed for high frequency measurements. We may also explore electron-beam approaches being developed at NIST. We will follow up with a round robin, and will use the results to help other groups to characterize their measurement approaches. We will also investigate the application of the calibration artifacts to the on-chip samplers now being pursued by a number of large semi-conductor manufactures, including Intel, Motorola, and IBM.

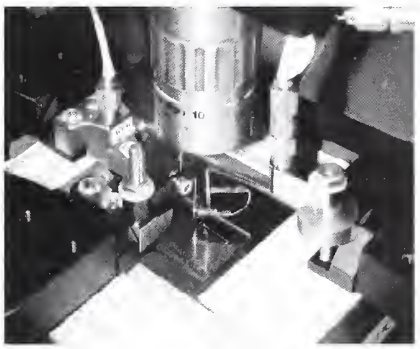


FIGURE 1. TEST OF A COMMERCIAL HIGH-IMPEDANCE PROBE

DELIVERABLES: By Oct 2002, demonstrate calibration method for high-impedance probes, show concrete improvement in measurement results. Design custom noncontacting probes for AFM test station.

DELIVERABLES: By Oct 2003, develop and calibrate noncontacting AFM waveform measurement system.

Accomplishments

- Designed and tested a prototype sinusoidal waveform standard.
- Constructed a high-speed electro-optic sampling system.
- Developed, fabricated and tested a noninvasive AFM scanning probe for measuring local microwave power.
- Developed a method of characterizing conventional high-impedance probes.

Technical Contacts:
Dylan Williams
John Moreland
Joseph Kopanski

Staff-Years (FY 2001):
0.15 professionals

Funding Sources:
STRS (100 %)

- Applied our high-impedance-probe characterization method to a probe mounted on an atomic-force microscope.

FY Outputs & Outcomes

- We will develop on-wafer waveform standards, metrology for characterizing probing systems, and develop AFM probing systems. We will disseminate our methods through industry presentations, and conference and journal publications.

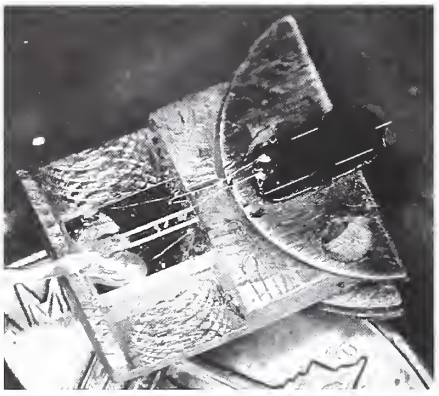


FIG. 1. A HIGH-FREQUENCY AFM PROBE FOR MAKING WAVEFORM MEASUREMENTS.

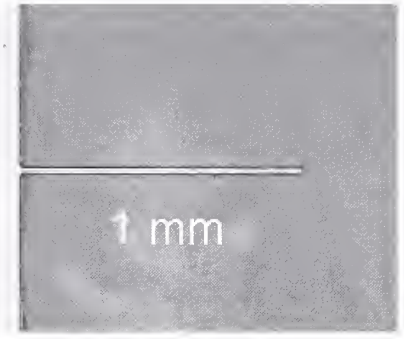


FIG. 2 A 1 MM LONG DIELECTRIC BIMATERIAL CANTILEVER AFM PROBE FABRICATED AT NIST FOR NONINVASIVELY MEASURING LOCAL MICROWAVE POWER.

Recent Publications

D. P. Pappas, C. S. Arnold, G. Shalev, C. Eunice, D. Stevenson, S. Voran, M. E. Read, E. M. Gormley, J. Cash, K. Marr, and J. J. Ryan, "Second Harmonic Magneto-Resistive Imaging to Authenticate and Recover Data from Magnetic Storage Media," Conf. on Law Enforcement Technology, Proc. SPIE, in press.

D.F. Williams and D.K. Walker, "0.1-10 GHz CMOS Voltage Standard," IEEE Workshop on Signal Propagation on Interconnects, Titisee-Neustadt, Germany, May 19-21, 1999.

U. Arz, D.F. Williams, D.K. Walker, J.E. Rogers, M. Rudack, D. Treytnar, and H. Grabinski, "Characterization of Asymmetric Coupled CMOS Lines," 2000 International Microwave Symposium Digest, June 11-16, 2000.

Albrecht Jander, John Moreland, and Pavel Kabos, "Dielectric micromachined calorimeter probe for high resolution microwave power measurements based on ferromagnetic resonance," 15th IEEE Int. Conf. on MicroElectroMechanical Systems, Jan. 20-24, 2002, Las Vegas, Nevada.

D.F. Williams, P.D. Hale, T.S. Clement, and J.M. Morgan "Mismatch corrections for electro-optic sampling systems," 56th ARFTG Conference Digest, Nov. 30-Dec. 1, 2000.

U. Arz, D.F. Williams, D.K. Walker, and H. Grabinski, "Asymmetric Coupled CMOS Lines: An Experimental Study," IEEE Trans. Microwave Theory and Tech.

D. F. Williams, B.K. Alpert, U. Arz, and H. Grabinski, "Causal characteristic impedance of planar transmission lines," IEEE Trans. on Microwave Theory and Tech., Dec. 2000.

Albrecht Jander, John Moreland, and Pavel Kabos, "Micromechanical Detectors for Local Field Measurements Based on Ferromagnetic Resonance," Journal of Applied Physics, pp. 7086-7090, June 2001.

Appendix A – Technical Contacts

Technical Contact Information

Project Title	Page Number	Technical Contacts	Phone Number
Metrology Supporting DeepUltraviolet Lithography	2	J. Burnett M. Dowell R. Gupta T. R. Scott	(301) 975-2679 (303) 497-7455 (301) 975-2325 (303) 497-3651
Metrology Supporting ExtremeUltraviolet Lithography	6	T. Lucatorto U. Griessman	(301) 975-3734 (301) 975-4929
Lithographic Polymers	9	E. Lin C. Soles J. Lenhart R. Jones W. Wu	(301) 975-6743 (301) 975-8087 (301) 975-4769 (301) 975-4624 (301) 975-6839
Atom-Based Dimensional Metrology	13	R. Silver	(301) 975-5609
Scanning Electron Microscope-Based Dimensional Metrology	17	A. Vladar M. Postek	(301) 975-2399 (301) 975-2299
Optical-Based Dimensional Metrology	21	J. Potzick R. Silver T. Doiron	(301) 975-3481 (301) 975-5609 (301) 975-3472
Scanning Probe Microscope-Based Dimensional Metrology	26	R. Dixson J. Dagata M. Postek T. Vorburger	(301) 975-4399 (301) 975-3597 (301) 975-2299 (301) 975-3493
Linewidth & Overlay Standards for Nanometer Metrology	30	M. Cresswell	(301) 975-2072
Model-Based Linewidth Metrology	34	J. Villarrubia A. E. Valadar M. Postek	(301) 975-3958 (301) 975-2399 (301) 975-2299
Two- and Three-Dimensional Dopant Profiling	39	J. Kopanski J. Marchiando D. Simons G. Gillen	(301) 975-2089 (301) 975-2088 (301) 975-3903 (301) 975-2190
Gate Dielectric Metrology	45	E. Vogel J. Suehle J. Ehrstein C. Richter D. Kaiser E. Steel N. V. Nguven	(301) 975-4723 (301) 975-2247 (301) 975-2060 (301) 975-2082 (301) 975-6759 (301) 975-3900 (301) 975-2044
Thin Film Metrology Using X-Rays	56	R. Matyi	(301) 975-4272
Measurements and Modeling of Electrodeposited Cu for ULSI	60	G. Stafford T. Moffat D. Josell L. Richter	(301) 975-6412 (301) 975-2143 (301) 975-5788 (301) 975-4152
Porous Thin Films Metrology for Low-k Dielectrics	63	B. Bauer C. Soles W. Wu	(301) 975-6849 (301) 975-8087 (301) 975-6839
Interconnect Dielectric Characterization Using Transmission-Line Measurement	66	M. Janezic D. Williams	(303) 497-3656 (303) 497-3138

Project Title	Page Number	Technical Contacts	Phone Number
Wire Bonding to Cu/Low-k Semiconductor Devices	69	G. Harman D. Kelley C. Johnson	(301) 975-2097 (301) 975-6410 (301) 975-6409
Solders and Solderability Measurements for Microelectronics	70	F. Gayle W. Boettinger C. Handwerker U. Kattner M. Williams	(301) 975-2659 (301) 975-6160 (301) 975-6158 (301) 975-6044 (301) 975-6170
Interconnect Materials and Reliability Metrology	73	D. Read R. Keller M. Gaitan	(303) 497-3853 (303) 497-7651 (301) 975-2070
Packaging Reliability	77	E. Drexler A. Slifka	(303) 497-5350 (303) 497-3744
Wafer and Chuck Flatness Metrology	82	T. Schmitz	(301) 975-8346
Thermophysical Property Data for Modeling CVD Processes and Calibration of Mass Flow Controllers	86	J. J. Hurly K. A. Gillis M. R. Moldover	(301) 975-2476 (301) 975-2468 (301) 975-2459
Low Concentration Humidity Standards	90	J. Hodges G. Scace	(301) 975-2605 (301) 975-2626
Development of Quantitative Measurements for Vacuum Process Control	94	J. P. Looney R. F. Berg D. S. Green (Univ. of Maryland)	(301) 975-4525 (301) 975-2466 (301) 975-4869
Models and Data for Chemical Vapor Deposition	97	R. Davis D. R. Burgess, Jr. J. E. Maslar E. F. Moore S. H. Ehrman (Univ. of Maryland)	(301) 975-2739 (301) 975-2614 (301) 975-4182 (301) 975-2582
Temperature Measurements and Standards for Rapid Thermal Processing	101	K. Kreider C. W. Meyer V. P. Scheuerman W. C. Ausherman D. P. DeWitt B. K. Tsai	(301) 975-2619 (301) 975-4825 (301) 975-4755 (301) 975-4810 (301) 975-4199 (301) 975-2347
Plasma Process Metrology	105	M. Sobolewski K. Steffens J. Olthoff Y. Wang L. Christophorou A. Goyette E. Benck	(301) 975-2980 (301) 975-2656 (301) 975-2431 (301) 975-4278 (301) 975-2432 (301) 975-2502 (301) 975-3697
Phase Identification from sub 200 nm Particles by Electron Backscatter Diffraction (EBSD)	109	John A. Small	(301) 975-3900

Project Title	Page Number	Technical Contacts	Phone Number
High-Resolution Microcalorimeter X-Ray Spectrometer for Chemical Analysis	110	D. Rudman D. Wollman S. Nam G. Hilton K. Irwin J. Martinis	(303) 497-5081 (303) 497-7457 (303) 497-3148 (303) 497-5679 (303) 497-5911 (303) 497-3597
Modeling, Measurements, and Standards for Wafer Inspection	114	T. Germer G. Mulholland	(301) 975-2876 (301) 975-6695
Metrology for Simulated and Computer Aided Design	120	A. Hodge-Miller	(301) 975-2071
At-Speed Test of Digital Integrated Circuits	123	D. Williams J. Moreland J. Kopanski	(303) 497-3138 (303) 497-3641 (301) 975-2089

Appendix B – Abbreviations and Acronyms

AC	alternating current
ADR	adiabatic demagnetization refrigerator
AEM	analytical electron microscopy
AES	Auger-electron spectroscopy
AFM	atomic force microscope
ALMWG	Analytical Laboratory Managers Working Group (ISMT)
AMAG	Advanced Metrology Advisory Group (ISMT)
ANSI	American National Standards Institute
ARXPS	angle resolved x-ray photoelectron spectroscopy
ASPE	American Society of Professional Engineers
ATP	Advanced Technology Program (NIST)
BCB	benzocyclobutene
BESOI	bond and etch-back silicon-on-insulator
BGA	ball-grid array
BIPM	Bureau International des Poids et Mésures
BIST	built-in self-test
BST	barium strontium titanate
C-AFM	calibrated atomic force microscope (NIST)
C-V	capacitance-voltage
CAD	computer-aided design
CCD	charge-coupled device
CD	critical dimension
CMOS	complementary metal oxide semiconductor
CMP	chem-mechanical polishing
CRADA	Cooperative Research and Development Agreement
CRDS	cavity ring-down spectroscopy
CSP	chip-scale package
CTCMS	Center for Theoretical and Computational Materials Science (NIST)
CVD	chemical vapor deposition
DC	direct current
DFT	design-for-test
DMA	differential mobility analyzer
DRAM	dynamic random-access memory
DSP	digital signal processing
DUV	deep ultraviolet
DUT	device under test
EBSD	electron backscatter diffraction
EELS	electron energy loss spectroscopy
EDC	embedded decoupling capacitance
EDS	energy-dispersive spectroscopy
EMC	electromagnetic compatibility
EMI	electromagnetic interference
EPMA	electron probe microanalysis
EUV	extreme ultraviolet
EUVL	extreme ultraviolet lithography
FIFEM	field ion field emission microscope
FIM	field ion microscope
FWHM	full-width half-maximum
GIXR/SE	grazing incidence x-ray reflection/spectrascopic ellipsometry
GIXPS	grazing incidence x-ray photoelectron spectroscopy
HRTEM	high resolution transmission electron microscope
HSQ	hydrogen silsesquoxane
I-V	current-voltage

IGBT	insulated-gate bipolar transistor
IPC	Association Connecting Electronics Industries
ISMT	International SEMATECH
ISO	International Organization for Standardization
ITRS	International Technology Roadmap for Semiconductors
LEED	low-energy electron diffraction
LER	line-edge roughness
LFPG	low frost-point generator
LOCOS	LOCal oxidation of silicon
LPP	laser-produced plasma
LPRT	light-pipe radiation thermometer
MBE	molecular beam epitaxy
MEMS	micro-electro-mechanical systems
MFC	mass flow controller
MMIC	millimeter and microwave integrated circuits
MOS	metal-oxide-semiconductor
MOSFET	metal-oxide-semiconductor field-effect transistor
MUX	multiplex
NCMS	National Center for Manufacturing Sciences
NDP	neutron depth profiling
NGL	next generation lithography
NEMI	National Electronics Manufacturing Initiative
NIST	National Institute of Standards and Technology
NLO	non-linear optical
NSOM	nearfield scanning optical microscopy
OMAG	Overlay Metrology Advisory Group (ISMT)
PED	Precision Engineering Division (NIST)
PLIF	planar laser-induced fluorescence
PMI	phase-measuring interferometer
PTB	Physikalisch-Technische Bundesanstalt
PZT	lead zirconium titanate
QM	quantum mechanics
RAM	Random-access memory
RGA	residual gas analyzer
RTA	rapid thermal annealing
RTP	rapid thermal processing
SANS	small-angle neutron scattering
SBIR	Small Business Innovative Research
SCM	scanning capacitance microscope
SEM	scanning electron microscope
SHG	second harmonic generation
SIA	Semiconductor Industry Association
SIMOX	separation by implantation of oxygen
SIMS	secondary-ion mass spectrometry
SoC	system-on-chip
SOI	silicon on insulator
SPM	scanning probe microscope
SRC	Semiconductor Research Corporation
SRM®	Standard Reference Material
SSHG	surface second-harmonic generation
SSIS	surface-scanning inspection system
SURF III	Synchrotron Ultraviolet Radiation Facility III
TCAD	technology computer-aided design
TDDB	time-dependent dielectric breakdown
TDR	time-domain reflectometry
TEM	transmission electron microscope

TFTC	thin-film thermocouple
TOF	time-of-flight
TMAH	tetramethyl ammonium hydroxide
UHV	ultra-high vacuum
UV	ultraviolet
WMS	wavelength modulation spectroscopy
VUV	vacuum ultraviolet
XPS	x-ray photoelectron spectroscopy

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