d Electrical Engineering Laboratory

National Institute of Standards and Technology
Technology Administration
U.S. Department of Commerce

NISTIR 6833
January 2002

# Semiconductor Electronics Division

## Programs, Activities, and Accomplishments

# The Electronics and Electrical Engineering Laboratory

Through its technical laboratory research programs, the Electronics and Electrical Engineering Laboratory (EEEL) supports the U.S. electronics industry, its suppliers, and its customers by providing measurement technology needed to maintain and improve their competitive position. EEEL also provides support to the federal government as needed to improve efficiency in technical operations, and cooperates with academia in the development and use of measurement methods and scientific data.

EEEL consists of six programmatic divisions and two matrix-managed offices:

Electricity Division

Semiconductor Electronics Division

Radio-Frequency Technology Division

Electromagnetic Technology Division

Optoelectronics Division

Magnetic Technology Division

Office of Microelectronic Programs

Office of Law Enforcement Standards

This document describes the technical programs of the Semiconductor Electronics Division. Similar documents describing the other Divisions and Offices are available. Contact NIST/EEEL, 100 Bureau Drive, MS 8100, Gaithersburg, MD 20899-8100, Telephone: (301) 975-2220, On the Web: www.eeel.nist.gov

**Cover caption: (front to back) Effective isotropic radiated MEMS-based microwave power sensor, test wafer from International SEMATECH (provided by Gennadi Bersuker), and a standard consumer laptop computer.**

## Electronics and Electrical Engineering Laboratory

# Semiconductor Electronics Division

## Programs, Activities, and Accomplishments

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**U.S. DEPARTMENT OF COMMERCE**
Donald L. Evans, Secretary

**Technology Administration**
Phillip J. Bond, Under Secretary for Technology

**National Institute of Standards and Technology**
Arden L. Bement, Jr., Director

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# Contents

# Welcome

David G. Seiler,
Division Chief

***"Through its involvement with industry, mainstream roadmapping activities, and associated working groups, the Semiconductor Electronics Division has successfully identified the needs of the semiconductor industry to which the unique capabilities of NIST can be applied most effectively."***

*From the NRC Panel Report, An Assessment of the National Institute of Standards and Technology Measurement and Standards Laboratories: Fiscal Year 2000*

The Semiconductor Electronics Division (SED) provides leadership in developing the semiconductor measurement infrastructure essential to improving U.S. economic competitiveness. It provides necessary measurements, physical standards, and supporting data and technology; associated generic technology; and fundamental research results to industry, government, and academia. The primary mission of the Division is to provide the measurement infrastructure to U.S. industry for mainstream silicon CMOS (complementary metal-oxide semiconductor) technology. The Division's programs also respond to industry measurement needs related to MicroElectroMechanical Systems (MEMS), power electronics, and compound semiconductors.

The Division has extensive interactions with individual companies, industry organizations, and professional societies; these activities enable the development of a research agenda responsive to the needs of industry. Active participation in industry roadmapping, such as the Semiconductor Industry Association's International Technology Roadmap for Semiconductors, and standards activities, such as committee work for the American Society for Testing and Materials, also is practiced by the Division to prioritize and establish programs with the highest potential impact. The Division widely disseminates the results of its research, especially in the areas of standardized test methods and SRMs, through a variety of channels - publications, software, conferences and workshops, and participation in standards organizations and consortia. NIST also actively seeks industrial, academic, and non-profit research partners to work collaboratively on projects of mutual benefit.

The Division, with a staff of about 65 (including full-time and part-time employees as well as guest researchers), is based in Gaithersburg, Maryland. The Division is one of six divisions within the Electronics and Electrical Engineering Laboratory at NIST. The Division's technical activities are organized into four groups: the Materials Technology Group, the Advanced Microelectronics Technology Group, the Device Technology Group, and the IC Technology Group. The Division assists industry by providing tools such as standard reference materials (SRMs), test chips, standard reference data, and software that support the needed measurement infrastructure. Division personnel visit industrial sites, host a variety of visitors, and make available tutorial material on an as-needed basis. We also are active in conference and workshop activities that directly benefit the industry. The Division receives and is responsive to hundreds of special requests for assistance from industry each year.

A broad array of activities that serve the semiconductor industry is currently underway in the Division. The staff of the SED addresses projects ranging from materials qualification to test structures for integrated circuits. Some of these projects are supported by the NIST National Semiconductor Metrology Program (NSMP), which is managed by the Electronics and Electrical Engineering Laboratory's Office of Microelectronic Programs. For more information on the NSMP, go to www.eeel.nist.gov/omp.

The Division, in cooperation with the National Research Council (NRC), offers awards for post-doctoral research for U.S. citizens in a variety of fields related to the semiconductor electronics industry. For additional details, including field descriptions and qualification guidelines, please see page 31.

The technical programs, activities, and accomplishments described here for each Division project clearly demonstrate the impact of SED's leadership and effective service as it continues to respond to the needs of industry and to contribute to the scientific and engineering communities.

Please take an opportunity to visit our Division Web site at www.eeel.nist.gov/812/. In addition to providing additional details on our Division and up-to-date project information, our Web site has interactive tutorials on the Hall effect (www.eeel.nist.gov/812/hall.html) and MEMS standard test structures based on e-standards (www.eeel.nist.gov/812/test-structures/). The Hall effect site was recommended as a "Hot Pick" in the July 21, 2000, issue of *Science* Magazine.

Thank you for your interest in our Division! I welcome your comments and suggestions. Feel free to e-mail me at david.seiler@nist.gov.

David G. Seiler
Division Chief

**Semiconductor Electronics Division Staff**

For additional information, contact

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Division/Office Facsimile: 301-975-6021
On the Web: www.eeel.nist.gov/812/

# Mission

The **Semiconductor Electronics Division** provides leadership in developing the semiconductor measurement infrastructure essential to improving U.S. economic competitiveness by providing necessary measurements, physical standards, and supporting data and technology; associated generic technology; and fundamental research results to industry, government, and academia. The primary focus is on mainstream silicon CMOS (complementary metal-oxide semiconductor) technology. The Division's programs also respond to industry measurement needs related to MicroElectroMechanical systems (MEMS), power electronics, and compound semiconductors.

***"The nature of the vision's purpose is not only to achieve a meaningful strategic or company goal, but also to build a dedicated community"***

*Jay A. Conger, The Brave New World of Leadership Training, IEEE Eng. Mgmt. Review (1996)*

# Vision

The **Semiconductor Electronics Division** is recognized as a dynamic world-class resource for semiconductor measurements, data, models, and standards focused on enhancing U.S. technological competitiveness in the world market.

# Values

The **Semiconductor Electronics Division** values its commitment to identify and to meet crucial measurement technology needs. The Division values its collaboration with all segments of the semiconductor community. It strives for integrity, excellence, objectivity, responsiveness, and creativity, while maximizing and utilizing the potential of its employees.

***The Division mission, vision, values, and goals were developed by a strategic planning process facilitated by a professional consultant. This process involved extensive workforce involvement, the Division leadership, and numerous meetings and informal discussions.***

# Goals

The Division will:

- Aggressively pursue and achieve select metrology needs as identified in the International Technology Roadmap for Semiconductors for mainstream silicon.
- Develop new and improved process-monitoring tools, methodologies, and data for the more efficient manufacture of silicon and compound-semiconductor devices.
- Develop cooperative, multidisciplinary projects within the Division and synergistic external collaborative efforts to better meet the critical needs of the semiconductor industry.
- Support novel research that has high potential for providing breakthroughs in materials, process, devices, and measurement technologies for the semiconductor industry.

# Semiconductors: Backbone of the Electronic/Digital Revolution

"This year, the semiconductor industry will produce about 20 million transistors for every man, woman and child on earth. By 2008, we will be producing 1 billion transistors or more per person per year. Those transistors improve our lives in countless ways - they make cars safer and more fuel-efficient, they enable personal communication devices, they promote medical breakthroughs, and they improve the quality of education. Chips have become the foundation upon which the world's progress is built. So even as we honor semiconductors as an invention, a prodigy of engineering prowess, we overlook this even greater miracle: that it is the culmination of forces stretching back a thousand generations into pre-history. That's what gives it its power in our imaginations; what makes it a kind of talisman, a magical object of almost supernatural powers. A tiny sliver of glass that brings the world into a vast conversation, heals the sick, sees to the edge of the universe, imagines worlds never seen. Even in our jaded age, the chip can still command awe."

*- The Silicon Century, Semiconductor Industry Association (SIA) Annual Report and Directory 2000*

Semiconductors, transistors, and their applications represent one of the greatest scientific and technological breakthroughs of the twentieth century. Consider their far reaching influence on our society in general and our daily lives. Can you imagine life without them? Semiconductors are pervasive in the microelectronic components used in computers, entertainment equipment, automotive electronics, medical instrumentation, telecommunications, space technology, television, radio, cell phones, and many other information technologies. Every hospital, school, factory, car, airplane, office, bank, and household contains transistors, microprocessors, and other semiconductor devices.

These breakthroughs are possible because of the miniaturization of the transistor dimensions, which allows the construction of compact systems with tremendous computing power and memory. Miniaturization, in turn, is possible because of the perfection of fabrication techniques that allow the "integration" of circuits and thus the production of chips containing millions of elements per square centimeter. The foundation stone of this complex technology is silicon. Meeting the demands for these large-scale, complex, integrated circuits (ICs) continues to require technological advances in materials, processing, circuit design, characterization, testing, and standards.

The semiconductor electronics industry is outstripping the measurement capability needed for maintaining and improving U.S. international competitiveness. Important factors affected include product performance, price, quality, compatibility, and time to market. The Division provides the measurement capability needed to support the efforts of U.S. industry to improve its competitiveness. In order to support this effort, the Division also engages in technology development and fundamental research, and makes the findings available to industry.

The Division focuses the largest part of its resources on the development and delivery of measurement capability for two principal reasons: measurement capability has a very high impact on U.S. industry (because it helps manufacturers address many of the challenges they face in realizing competitive products in the marketplace), and NIST is the official lead U.S. Government agency for measurements.

The Division focuses on developing measurement capability that is beyond the reach of the broad range of individual companies. Companies seek NIST's help for several reasons:

- The companies need NIST's special technical capability for measurement development.
- The companies need NIST's acknowledged impartiality for diagnosing a measurement problem affecting the industry broadly or for achieving adoption of a solution across the industry.
- The companies cannot develop the measurement capability needed by the industry broadly because they cannot individually capture the returns of the cost of development.
- Industry's quality standards require that key measurements be traceable to the national measurement reference standards that NIST maintains. This is a requirement of growing importance in export markets.

***"No other human invention is the equal of the semiconductor device - if only because no other invention has been adopted so quickly and pervasively as the integrated circuit. Since the invention of the planar process forty years ago, billions of transistors are now in use beneath, around and above the earth. The microprocessor is the defining invention of the electronic age, the inventor of inventions from the personal computer to the internet."***

*The Silicon Century, Semiconductor Industry Association (SIA) Annual Report and Directory 2000*

***"Sometime toward the end of 2000 or the beginning of 2001, sales to the communications sector will exceed those of the PC sector, marking the end of perhaps 20 years of domination of the PC sector dominating semiconductor chips ... In the Internet Era, it's no longer microprocessors and memory that are the primary semiconductor components - it's DSP Digital Signal Processing plus analog."***

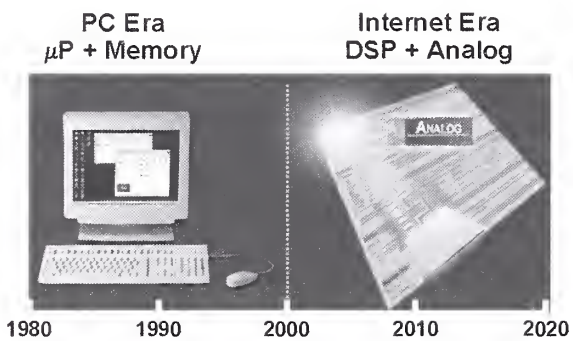
*Dennis Buss, Vice-President of Mixed-Signal Technology, Texas Instruments, at the 2000 International Conference on Characterization and Metrology for ULSI Technology*

The Division continues to interact/collaborate with a wide variety of companies, consortia [such as International Semiconductor Manufacturing Technology (ISMT), Semiconductor Equipment and Materials International (SEMI), and the Semiconductor Research Corporation (SRC)], academia, and other government labs to accomplish its mission. Specific details are given in the project sheets that follow. Work in the Division results in extensive outputs or deliverables that cover knowledge/improvements in physical understanding, test methods/measurements, Standard Reference Materials (SRMs), Standard Reference Data (SRD) sets, standards, test structures/test chips, software, measurement accuracy/traceability, publications/reports, patents/Cooperative Research and Development Agreements (CRADAs), round robins, data and models, talks/short courses, company visits, conferences/workshops, consortia participation, and various activities and leadership roles on committees and working groups.

Division staff serve the semiconductor community in leadership roles on standards committees such as American Society for Testing and Materials (ASTM) and Electronic Industries Alliance (EIA) / Joint Electron Device Engineering Council (JEDEC), societies such as IEEE, ECS, and APS, and on numerous semiconductor conferences/workshops. Many test methods and standards have been developed and written over the years by NIST staff for ASTM and EIA/JEDEC, including ones for resistivity, oxygen in silicon, thin dielectrics, electromigration, and device characterization. Staff serve on various Technical Working Groups to help put together the International Technology Roadmap for Semiconductors (ITRS). These groups are Process Integration, Devices, and Structures; Assembly and Packaging; Lithography; Interconnect; and Front End Processes. The ITRS provides targets for equipment, material, and software suppliers; provides targets for researchers; and serves as a common reference for the semiconductor industry.

The Division also has impacted the semiconductor community by producing a number of SRMs. To date, over 2,500 SRMs have been sold and distributed for resistivity, oxygen in silicon, and optical thickness by ellipsometry. Hundreds of companies throughout the world have purchased these SRMs to maintain and improve their measurement capability.

According to Dennis Buss, Vice-President of Mixed-Signal Technology, Texas Instruments, the semiconductor industry is moving from an era dominated by PC sales to one heavily dominated by communications. As the industry progresses along this new avenue, the leadership in measurement infrastructure that this Division provides continues to be important.




**The Internet Era. [Used with permission from Dennis Buss' talk "Technology in the Internet Era," presented at the 2000 International Conference on Characterization and Metrology for ULSI Technology]**

# Semiconductor Electronics Division Organization

## Division Office (812.00)

2054 SEILER, David G., Chief
2068 BLACKBURN, David L., Deputy
2054 PRINTZ, Lori A., Secretary
4514 COOK, Sharon W., AO
5633 MURPHY, Joan, Admin. Assistant (PT)
2079 BENNETT, Herbert S., NIST Fellow
2097 HARMAN, George G., NIST Fellow
2050 SECULA, Erik M.

## Materials Technology Group (812.01)

8009 SHAFFNER, Thomas J. (GL)
2053 HUFF, Barbara, Secretary

### Scanning-Probe Microscope Metrology

2089 KOPANSKI, Joseph J. (PL)
3241 BIRDWELL, A. Glen (PD)
8755 BUH, Gyoung-Ho (GR)
2088 MARCHIANDO, Jay F.
2108 RENNEX, Brian G. (PT)
2067 THURBER, W. Robert

### Theoretical Solid-State Physics for Semiconductors

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## Advanced Microelectronics Technology Group (812.02)

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2053 HUFF, Barbara, Secretary
2052 WILKES, Jane M., Secretary

### Advanced MOS Device Reliability and Characterization

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2053 BAYNE, Anthony (GR)
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8687 HEH, Da-Wei (GR)
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### Nanoelectronic Device Metrology

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2053 GNADE, Bruce (GR)
2087 KIRILLOV, Oleg
2053 PARK, Jin-Won (GR)
2247 SUEHLE, John S.
4723 VOGEL, Eric M.

### Thin-Film Process Metrology

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2084 CHANDLER-HOROWITZ, Deane
8747 CHO, Yong J. (GR)
2044 NGUYEN, Nhan V.
2082 RICHTER, Curt A.
2065 RICKS, Donnie R.

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2056 GORMAN, Sherri D., Secretary

### Metrology for Simulation and Computer-Aided Design

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2075 ALBERS, John (detailed to ATP)
2069 BERNING, David W.
2068 BLACKBURN, David L.
2242 BUCK, Laurence M.
8777 HODGE-MILLER, Angela
4709 JOSHI, Yogendra K. (GR)
2056 LAI, Jih-Sheng (GR)
2056 MANTOOTH, Homer (GR)
8776 McNUTT, Ty R. (GR)
5967 REICHL, John V. (GR)
8751 TIGLI, Onur (GR)

### MicroElectroMechanical Systems

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4710 BARNOY, Ishai (GR)
5484 GEIST, Jon (GR)
4739 HERMAN, David L. (GR)
2049 MARSHALL, Janet C. (PT)
6367 MIJARES, Geraldine I.
4796 SUMAN, Shivesh K. (GR)
2056 WEI, Xiaojin (GR)
2239 ZAGHLOUL, Mona E. (FH)

### Assembly and Packaging

2097 HARMAN, George G.

**Legend:**

AO = Administrative Officer
ATP = Advanced Technology Program
FH = Faculty Hire
FM = Facility Manager
GL = Group Leader
GR = Guest Researcher
PD = PostDoctoral Appointment
PL = Project Leader
PT = Part Time
S = Student
TS = Technology Services

Telephone numbers are: (301) 975-XXXX, (the four digit extension as indicated)

## IC Technology Group (812.04)

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2052 WILKES, Jane M., Secretary

### Linewidth and Overlay Standards for Nanometer Metrology

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5026 ALLEN, Richard A.
2236 ELLENWOOD, Colleen E.
4446 GHOSHTAGORE, Rho (GR)
2182 GUILLAUME, Nadine (GR)
8193 MURABITO, Christine E. (S)
5623 OWEN, James C.

### Microfabrication Process Facility

2699 HAJDAJ, Russell (FM)
2096 JOHNSON, Eric S.

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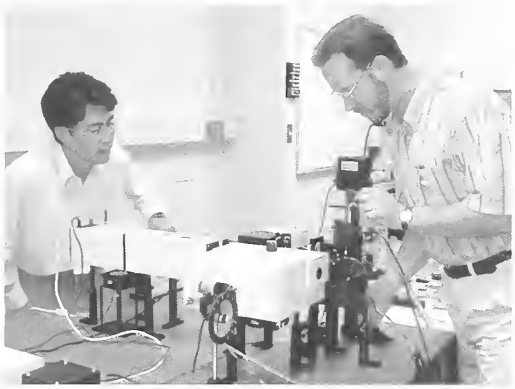
# Scanning-Probe Microscope Metrology

## Goals

Develop advanced scanning-probe and conventional electrical metrology techniques, models, and artifacts that are essential to improving semiconductor materials, processes, device performance, and reliability for the silicon and compound semiconductor industries. A current specific goal is to provide the technology computer-aided design (TCAD) community with quantitative two-dimensional dopant profiles to calibrate and enhance the predictivity of simulators.



**Gyoung-Ho Buh (left) and Glen Birdwell (right) loading a sample onto the stage of the modulation/surface photovoltage spectroscopy system.**

## Customer Needs

The Semiconductor Industry Association's (SIA's) International Technology Roadmap for Semiconductors (ITRS) identifies 2-D and 3-D carrier profiling as a key enabling technology for the development of next-generation integrated circuits. In 2002, it is desired to know 2-D carrier profiles with spatial resolution of 5 nm and with a precision (in concentration) of ±5 %; these demands increase to less than 1 nm and ±2 % by 2015. The Scanning Capacitance Microscope (SCM) has emerged as the leading contender to provide 2-D carrier profiles.

While SCMs are commercially available, techniques to interpret accurately SCM images have lagged. Much work remains to be done to develop 3-D physical models of scanning capacitance microscopy and techniques to use these models to extract quantitative carrier profiles from SCM images of differential capacitance. Likewise, the measurement methodology for quantitative scanning capacitance microscopy is still evolving. The need for, and form of, reference materials for scanning capacitance microscopy has yet to be defined. Other scanning probe microscopy (SPM) based techniques for semiconductor metrology suffer similar problems - microscopes have been invented, but standard measurement and interpretation techniques are not available.

## Technical Strategy

The Scanning-Probe Microscope Metrology Project is developing tools that are intended to enable scanning capacitance microscopes to function as two-dimensional dopant profiling tools. This work is divided into three tasks. Task 1 is to develop SCM measurement methodologies. Best measurement practices are being determined via collaborative projects with industrial users and research into the physics of the silicon surface preparation. Task 2 is to develop theoretical models of the SCM. The focus of our modeling effort has been to develop 2-D and 3-D finite-element solutions of Poisson's equation for the SCM geometry. Task 3 is interpretation of SCM data and technology transfer. Our expertise with interpreting SCM images is being transferred to industry through our software program *FASTC2D*. The program features an easy to use interface, rapid profile extraction, and operation in a Windows environment.

**DELIVERABLES:** By 2002, develop and characterize "known good sample" for distribution with *FASTC2D* code.

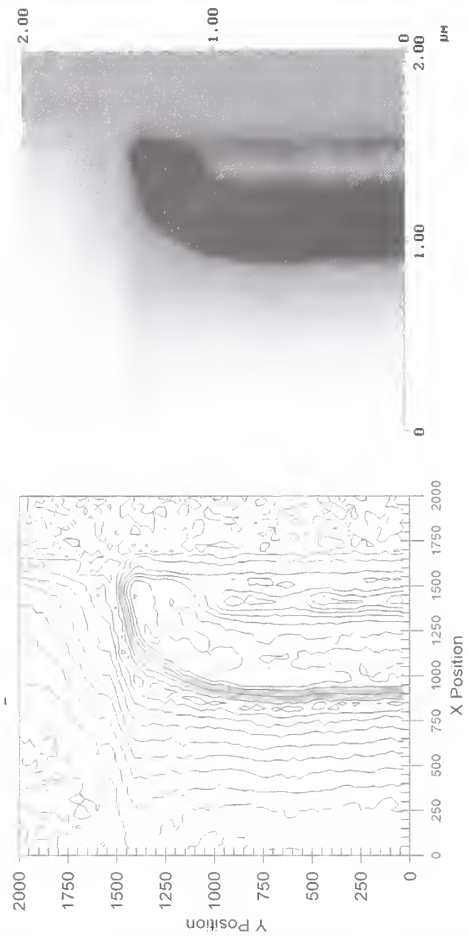
The version of *FASTC2D* currently available utilizes a calibration curve, determined from a database of pre-calculated solutions, which can very rapidly determine a 2-D carrier profile from an SCM image. When used in conjunction with SIMS measurements or a reference sample, relatively accurate profiles can be obtained. We are also developing an additional tool for technology transfer: a new generation of test structures consisting of fully processed and partially processed transistors. They will eventually be produced in sufficient numbers so that every *FASTC2D* user can get a set. A round-robin set of measurements based on these structures is planned, with devices to be distributed through the International SEMATECH 2-D dopant profiling working group.

**DELIVERABLES:** By 2003, demonstrate optimized 3-D calculations of the SCM signal across dopant gradients and junctions.

**Technical Contact:**
Joseph J. Kopanski

**Staff-Years (FY 2001):**
4 professionals
6 guest researchers

**Funding Sources:**
NIST (100%)




**SCM image of a p+/n junction (top). Dopant contours extracted with *FASTC2D* (bottom).**

A physically accurate 3-D model and determination of the dopant profile by an inverse solution are required to meet industrial needs for 2-D dopant profiling to the end of the ITRS. We have previously developed a quasi-3-D model of the SCM that predicts the essential behavior of the SCM measurement. However, for the required dopant profiling performance goals, a more rigorous approach is necessary. Towards this end, the finite element method has been employed to solve Poisson's Equation for the SCM geometry in three-dimensions. Accuracy requirements may also force the consideration of quantum mechanical effects, necessitating the solution of the coupled Poisson and Schrödinger Equations. We are developing improved 3-D Poisson solvers using the LaGriT grid management toolbox in collaboration with Los Alamos National Laboratories.

**DELIVERABLES:** By 2004, have available for distribution to users a computationally efficient method of determining carrier profiles from inverse solutions of scanning capacitance microscopy based on 3-D models.

An inverse solution of the SCM requires repeated solutions of the forward problem; i.e., calculation of the SCM signal from candidate carrier profiles. The candidate carrier profile is adjusted until a carrier profile is found that yields a calculated SCM signal that agrees with the measured SCM signal. Project staff have developed a regression procedure to do this with a 2-D solver. The final level of refinement is to use the full 3-D model as the basis of inverse solutions of the SCM. However, the volume of data to be processed and the time required for calculation makes this intractable for routine profile extraction. Practical application requires finding shortcuts that will achieve the 3-D result without having to complete the entire round of 3-D simulations.

The project is also actively investigating other SPM based characterization techniques. We plan to extend the SCM carrier profiling capacity to SiC and III-V semiconductors. Intermittent-contact scanning capacitance microscopy is sensitive to variations in the dielectric constant of thin films and can detect metal layers buried beneath insulating films. Optically-pumped scanning capacitance microscopy is sensitive to variations in carrier lifetime. The scanning microwave microscope (SMWM) is of interest because it can provide both the real and imaginary parts of impedance at frequencies from dc to 50 GHz. Our plan is for research into SPM characterization techniques other than scanning capacitance microscopy to be a majority of the project's effort by the end of FY 2004.

## Accomplishments

- *Demonstrated a 2-D regression procedure to solve the SCM inverse problem of finding the dopant profile from the measured SCM signal.* This is the first time that an optimized regression procedure has been used to find the SCM inverse solution based on numerical solution of the Poisson's equation. Second generation (inverse modeling) SCM interpretation techniques are a significant improvement over the first generation (calibration curve) techniques. The technique uniquely uses two meshes to achieve conversion in only a few iterations (five steps of the coarse mesh and two steps of the fine mesh for a model problem). Inverse solutions determined by this technique fully include the effects of the local

dopant gradient and gradient curvature on the SCM measurement of the dopant profile. The method can handle dopant profiles in like-type substrates or in opposite-type substrates (i.e., across p-n junctions). The procedures developed for the 2-D model are expected to be useful for the 3-D models that are currently under development.

- Development of 3-D models of SCM in collaboration with Los Alamos National Laboratories by applying their LaGriT (Los Alamos Gridding Toolkit) software package. LaGriT is a library of user callable tools that provide 3-D mesh generation, mesh optimization, and dynamic mesh maintenance for finite element methods. Access to such code will enable more efficient 3-D simulations of the SCM measurement across dopant gradients and p-n junctions.

- *Compared the response of SCMs using sensors from four different manufacturers and correlated the double zero crossing in SCM signal sometimes observed at p-n junctions with the magnitude of the sensor high frequency voltage.* Publication submitted.

- *Development of scanning microwave microscope.* Atolytics, Inc. in State College, PA, has started the second year of their SBIR phase II contract to develop a commercial version of their SMWM. A prototype instrument has been constructed. Manufacturing Instrumentation Consultant Co. of Cleveland, OH, has been granted an SBIR phase II contract to develop co-axial shielded scanning probe microscope tips. These tips will be evaluated by NIST.

- *Application of Scanning Capacitance Microscopy to Dopant Profiling of High Bandgap Semiconductors.* Summer students Brenda Handy, Howard University, and Quan Chau, University of California, Berkley, developed a process to prepare cross sections of SiC for examination with the SCM. Depletion layers and micropipes in SiC have been imaged with the SCM. Work is underway to apply scanning capacitance microscopy to other high bandgap semiconductors such as GaN.

- *Post-doc Glen Birdwell and Guest Researcher Gyoung-Ho Buh joined the project late in FY 2000.* They will begin looking at ways to optically pump scanning probe microscopes and examine the information that can be obtained with these techniques.

## FY Outputs

### Collaborations

- Agere Systems, Jack Hergenrother, quantitative SCM of vertical replacement-gate transistors, June 2001 to current (Joseph J. Kopanski)

- Dynamic Research Corporation, scanning capacitance microscopy of actively biased SOI MOSFETs, November 2000 to current (Joseph J. Kopanski)

- Howard University, Gary Harris, application of scanning capacitance microscopy to high bandgap semiconductors (Joseph J. Kopanski)

- Los Alamos National Laboratory, Charles Snell, UT-MARLOWE Software (Jay F. Marchiando)

- Los Alamos National Laboratory, Denise George and Andrew Kuprat, LaGrit software (Jay F. Marchiando)

- NIST, gate oxide formation under mild conditions for scanning capacitance microscopy (Barbara J. Belzer and Joseph J. Kopanski)

- University of Queensland, Brisbane, Australia; Prof. Tong Yeow was a guest researcher during the summer of 2001. Prof. Yeow learned to operate the SCM and acquired SCM data of NIST test structures for interpretation using Medici and inverse modeling (Tong Yeow)

### Recognition

- Bronze Medal Award, recognized as having greatly accelerated development of the SCM as a practical measurement tool, November 29, 2000 (Joseph J. Kopanski, Jay F. Marchiando, and Brian G. Rennex)

- Senior Member IEEE, March 31, 2001 (Joseph J. Kopanski)

## Recent Publications

McBride, D. E., Kopanski, J. J., Gate Oxide Formation under Mild Conditions for Scanning Capacitance Microscopy, Characterization and Metrology for ULSI Technology: 2000, D. G. Seiler, A. C. Diebold, T. J. Shaffner, R. McDonald, W. M. Bullis, P. J. Smith, and E. M. Secula, Eds. (AIP, New York, 2001), pp. 657-661.

Rennex, B., Kopanski, J., and Marchiando, J., FASTC2D: Software for Extracting 2D Carrier Profiles from Scanning Capacitance Microscopy Images, Characterization and Metrology for ULSI Technology: 2000, D. G. Seiler, A. C. Diebold, T. J. Shaffner, R. McDonald, W. M. Bullis, P. J. Smith, and E. M. Secula, Eds. (AIP, New York, 2001), pp. 635-640.

# Advanced MOS Device Reliability and Characterization

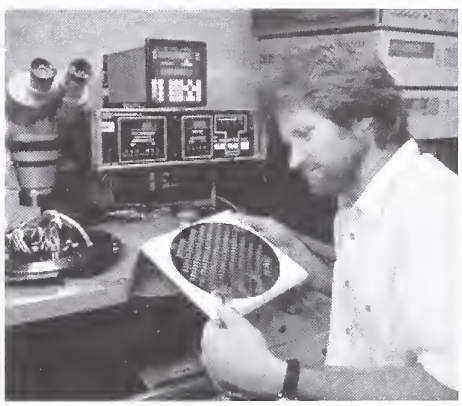
**Technical Contact:**
John S. Suehle

**Staff-Years (FY 2001):**
2 professionals
1 technician
7 guest researchers

**Funding Sources:**
NIST (98%)
Other (2%)

## Goals

To provide electrical and reliability measurement techniques, data, physical models, and fundamental understanding for ultra-thin silicon dioxide and alternate gate dielectrics in future Metal Oxide Semiconductor (MOS) devices. To increase the understanding of the relationship between the gate dielectric material/interface properties and device electrical and reliability measurements.



**John Suehle loading a test wafer on a wafer prober for long-term dielectric testing.**

## Customer Needs

The Semiconductor Industry Association's (SIA's) International Technology Roadmap for Semiconductors indicates that the equivalent thickness of the gate dielectric will need to be 1.0 nm to 1.5 nm by 2004. Due to increased power consumption, intrinsic device reliability, and circuit instabilities associated with $SiO_2$ of this thickness, a high-permitivity gate dielectric (e.g., $Si_3N_4$, $HfSi_xO_y$, $ZrO_2$) with low leakage current and at least equivalent capacitance, performance, and reliability will be required. The physics of failure and traditional reliability testing techniques must be re-examined for ultra-thin gate oxides that exhibit excessive tunneling currents and soft breakdown. Electrical characterization of MOS capacitors and Field Effect Transistors (FETs) has historically been used to determine device and gate dielectric properties such as insulator thickness, defect densities, mobility, substrate doping, bandgap, and reliability. Electrical and reliability characterization methodologies need to be developed and enhanced to address issues associated with both ultra-thin $SiO_2$ and alternate dielectrics including large leakage currents, quantum effects, and thickness dependent properties. As compared to $SiO_2$, very little is known about the physical or electrical properties of high dielectric constant gate dielectrics in MOS devices. The use of these films in Complementary Metal Oxide Semiconductor (CMOS) technology requires a fundamental understanding of the relationship between the gate dielectric material/interface and device electrical and reliability measurements.

## Technical Strategy

The strategy of this effort is to obtain or fabricate both device samples and blanket films, to perform reliability and electrical characterization of the devices, and to collaborate with other researchers to perform analytical characterization. Many issues such as tunnel/leakage current and spatially dependent properties associated with metal oxide and silicate dielectrics are also present in ultra-thin oxide and oxide-nitride stacked dielectrics. Therefore, many of the characterization schemes are first developed on the simpler ultra-thin oxide and oxide-nitride dielectrics and then applied to the metal oxide and silicate dielectrics.

There are two main focus areas for this project. The first focus area investigates the physics of failure and the reliability testing techniques for ultra-thin $SiO_2$ and high dielectric constant gate dielectrics. The physical mechanism responsible for "soft" or "quasi" breakdown modes in ultra-thin $SiO_2$ films and its implications for device reliability will be investigated as a function of test conditions and temperature. Long-term time-dependent-dielectric breakdown (TDDB) tests will be conducted on $SiO_2$ films as thin as 1.5 nm at electric fields close to operating conditions. These tests will be used to determine the thermal and electrical acceleration parameters of device breakdown.

**DELIVERABLES:** By 2002, studies of the long-term drift and stability of post-soft conduction in ultra-thin $SiO_2$ films including voltage and temperature acceleration parameters.

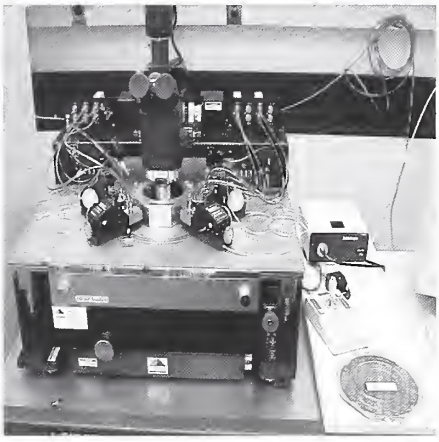
This project is conducting experiments to investigate the differences of gate oxide breakdown and wear-out due to high oxide field and hot-carrier injection. This study will provide insight

into the physical mechanism of ultra-thin gate oxide wear-out and breakdown.

**DELIVERABLES:** By 2002, experimental results of the electron-hole interaction in $SiO_2$ and the effect on dielectric breakdown. Studies of oxide degradation using high voltage, short-time single pulse stressing.

The understanding generated in this research is being used to continue generating standard measurements through a NIST-coordinated collaboration between EIA-JEDEC (Electronic Industries Association Joint Electron Device Engineering Council) and the ASTM (American Society for Testing and Materials). Studies on the reliability of high dielectric constant dielectrics such as oxide-nitride stacks are also being performed.

**DELIVERABLES:** By 2003, a new standard constant-voltage stress test will be developed for determining TDDB acceleration parameters in sub 3 nm thick $SiO_2$ films. The new test will utilize current or voltage noise as breakdown criteria when films exhibit soft breakdown. Such a test will find application by the semiconductor industry when qualifying new manufacturing processes.



**A low-noise (fA), high-temperature (300 °C) probe station is used to electrically characterize devices.**

The second focus area is to investigate electrical measurement techniques, procedures, and analysis associated with devices having thin oxide and alternate gate dielectrics. The electrical measurement techniques that we are investigating include capacitance-conductance characterization, dielectric tunnel and leakage current characterization, and defect density measurements such as charge pumping and conductance. Furthermore, standard properties and mechanisms/correlations for these dielectrics, including defect centers, dielectric constant, defect generation rates, and leakage/tunnel current are being characterized.

**DELIVERABLES:** By 2003, a Visual Basic based application that simulates capacitance-voltage and long-channel drain current, including insulator defects, quantum mechanical considerations, and polysilicon depletion effects, will be developed.

Using high-κ gate dielectric films obtained from key industrial and university groups, electrical characterization methodologies are being developed to address various issues associated with these films, including large leakage currents, quantum effects, thickness dependent properties, large trap densities, transient (non-steady state) behavior, unknown physical properties, and the lack of physical models.

Examples of measurement problems that are being addressed include modifying and verifying electrical defect density measurement techniques, including conductance-frequency, capacitance-voltage, and charge-pumping.

**DELIVERABLES:** By 2003, studies of insulator defects and current transport through high-κ dielectrics (e.g., $HfO_2$) including current noise and the energy distribution of $HfO_2$ interface states using conductance.

## Accomplishments

■ *A systematic study of the uncertainties, sensitivity, and limitations of capacitance and conductance measurements for extracting device properties and interface state density of MOS devices with ultra-thin (< 3.0 nm) oxides was completed.* Capacitance and conductance characterization of MOS devices is used to determine properties such as oxide thickness, substrate doping, and interface state density. However, with the advent of ultra-thin oxides, effects such as tunnel current, series resistance, and quantum mechanical confinement in the substrate require additional consideration. This work provides a detailed analysis of the impact of these effects on parameter extraction using conductance and capacitance characterization of MOS devices with ultra-thin oxides.

■ *Several extensive experimental investigations of the mechanisms responsible for defect generation and breakdown of thin silicon dioxide were performed.* The results confirm that breakdown is directly related to the current passing through the dielectric. This confirms that the trap creation model based on energetic electrons creating damage and the statistical behavior of the number of defects at breakdown correctly

describes the reliability of ultra-thin $SiO_2$ at both constant-voltage tunneling and substrate hot-electron conditions. Additional studies using substrate hot hole injection showed that holes are extremely effective in creating defects in the dielectric. However, these defects are ineffective in causing dielectric breakdown. These results cast doubt on the anode hole injection model for oxide breakdown.

- *A detailed investigation of the reliability of various $SiN_xO_y/SiO_2$ (N/O) found that an $N_2O$ anneal of an N/O stack results in device lifetime orders of magnitude greater than $SiO_2$ of the same equivalent oxide thickness.* The results suggest that this lifetime improvement may be due to a high critical defect density at breakdown, low defect generation rate, and low leakage current of the $N_2O$-annealed stack. In collaboration with North Carolina State University, measurements and modeling were used to determine the impact of stacked dielectrics on charge-pumping measurements to determine interface and near interface defect densities.

- *A study was performed to investigate soft breakdown in ultra-thin silicon dioxide films and to investigate the temperature dependence of TDDB.* A more dramatic temperature dependence of wear-out was observed and raises serious reliability concerns. Thinner oxides and larger areas exhibited softer breakdown that requires the use of noise as the breakdown criteria. However, both hard breakdown and noise detection exhibited the same thermal activation. These tests provide critically important field acceleration parameters and thermal activation energies that are required for reliability extrapolation of ultra-thin oxides. Furthermore, the use of noise as a breakdown criterion was validated.

- *The increased occurrence of soft breakdown in ultra-thin $SiO_2$ films makes reliability characterization very difficult and necessitates the development of more sophisticated techniques to detect breakdown.* The effects of stress interruption on the TDDB life distributions of 2.0 nm oxynitride gate dielectric films were studied. TDDB tests using two different breakdown detection techniques were conducted at several gate voltages. Additional tests were conducted using unipolar and bipolar pulsed bias with pulse repetition frequencies up to 100 kHz to study the effects of pulsed bias on the lifetime of 2 nm films. Our results show that (1) stress interruption longer than 1 s does not affect the defect generation and TDDB life distributions, (2) both current noise and the increase in low-voltage stress-induced leakage current (SILC) detection techniques provide similar failure statistics for ultra-thin $SiO_2$, (3) TDDB lifetime for ultra-thin gate dielectrics under unipolar biased stress does not substantially depend on pulse repetition frequencies less than 1 MHz, and (4) lifetime under bipolar pulsed bias is significantly improved and exhibits a dependence on pulse repetition frequency.

- *A joint collaboration between NIST and JPL investigates what effect ionizing radiation experienced in deep space missions will have on the reliability of ultra-thin gate dielectrics.* It has been previously reported that heavy ion bombardment can cause radiation-induced soft breakdown (RSB) in ultra-thin gate dielectrics. Heavy ion-induced soft and hard breakdown were investigated in thin gate oxides ($t_{ox}$ ~3.0 nm) as a function of Linear Energy Transfer (LET), fluence, and voltage applied during irradiation. It was found that post-irradiation oxide conduction is well described by a quantum point contact model. This new work provides information about the physical nature of the soft breakdown path induced during irradiation and provides insight into the structure of the breakdown path in ultra-thin oxides induced under voltage stress.

## FY Outputs

### Collaborations

- Advanced Micro Devices, ultra-thin oxide reliability (John S. Suehle)
- Analog Devices, Limerick, Ireland, ultra-thin gate oxide reliability (John S. Suehle)
- CSTL/Process Measurements Division, microhotplate-based sensor arrays (John S. Suehle and Michael Gaitan)
- Divisions 836, 837, 838, Roger Van Zee et al., spectroscopic ellipsometry of molecular electronics (Nhan V. Nguyen, Curt A. Richter, and John S. Suehle)
- Divisions 836, 837, 838, Dr. Roger van Zee et al., Molecular Electronics Competence Project (Curt A. Richter and John S. Suehle)
- Fairchild Semiconductor, ultra-thin gate oxide reliability (John S. Suehle)
- George Washington University, microhotplate-based chemical sensors (John S. Suehle)
- Lucent Technologies, ultra-thin gate oxide reliability (John S. Suehle)

- Motorola, ultra-thin gate oxide reliability (John S. Suehle)
- N.C. State University (oxynitrides, nitrides, ultra-thin $SiO_2$), alternative gate dielectrics (Eric M. Vogel)
- National Semiconductor, ultra-thin gate oxide reliability (John S. Suehle)
- Penn State University, ultra-thin gate oxide reliability (John S. Suehle)
- Texas Instruments, electrical and reliability characterization of ultra-thin gate oxides (John S. Suehle and Curt A. Richter)
- Texas Instruments, ultra-thin gate oxide reliability (John S. Suehle)
- The Pennsylvania State University, molecular electronics (Curt A. Richter and John S. Suehle)
- University of Delaware, alternative dielectrics (John S. Suehle)
- University of Maryland, College Park, microhotplate-based chemical sensors (John S. Suehle)
- University of Maryland, College Park, ultra-thin gate oxide reliability (John S. Suehle)
- University of Maryland, gate dielectric reliability (Eric M. Vogel)
- University of Minnesota, alternate gate dielectrics (Eric M. Vogel)

### Standards Committee Participation

- JEDEC JC14.2 Committee on Wafer-Level Reliability, Dielectric Working Group, Chairman (John S. Suehle)

## Recent Publications


Richter, C. A., Hefner, A. R., and Vogel, E. M., A Comparison of Quantum-Mechanical Capacitance-Voltage Simulators, IEEE Electron Device Letters, vol. 22, no. 1, January 2001, pp. 35-37.

Richter, C., Vogel, E., Hodge, A., and Hefner, A., Differences Between Quantum-Mechanical Capacitance-Voltage Simulators, SISPAD Technical Digest 2001 (2001 International Conference of Simulation of Semiconductor Processes and Devices), 4 p.

Schafft, H., Head, L., Lechner, J., Gill, J., and Sullivan, T., Deep Censoring Method for Early Reliability Assessment, 2000 IRW (Integrated Reliability Workshop) Final Report, pp. 1-8, IEEE Catalog Number 00TH8515.

Schuster, C. E., Vangel, M. G., and Schafft, H. A., Improved Estimation of the Resistivity of Pure Copper Electrical Determination of Thin Copper Film Dimensions, Microelectronics Reliability, vol. 41, pp. 239-252, 2001.

Vogel, E. M., and Misra, V., MOS Device Characterization, in Handbook of Silicon Semiconductors Metrology, A. C. Diebold, Ed. (Marcel Dekker, Inc., New York - Basel, 2001), pp. 59-95.

Vogel, E. M., Edelstein, M. D., and Suehle, J. S., Defect Generation and Breakdown of Ultra-Thin Silicon Dioxide Induced by Substrate Hot Hole Injection, Journal of Applied Physics, vol. 90, no. 5, Sept. 1, 2001, pp. 2338-2347.

Vogel, E. M., Edelstein, M. D., and Suehle, J. S., Reliability of Ultra-Thin Silicon Dioxide Under Substrate Hot-Electronic, Substrate Hot-Hole, and Tunneling Stress, Microelectronics Engineering 59 (2001), pp. 73-83.

von Hagen, J., Antonin, G., Fazekas, J., Head, L., and Schafft, H., New SWEAT Method for Fast, Accurate, and Stable Electromigration Testing on Wafer Level, 2000 IRW (Integrated Reliability Workshop) Final Report, pp. 85-89, IEEE Catalog Number 00TH8515.

Wang, B., Suehle, J. S., Vogel, E. M., and Bernstein, J. B., The Effect of Stress Interruption and Pulsed Biased Stress on Ultra-Thin Gate Dielectric Reliability, 2000 IEEE International Integrated Reliability Workshop Final Report, Lake Tahoe, CA, Oct. 23-25, 2000, pp. 74-79.

Wang, B., Suehle, J. S., Vogel, E. M., and Bernstein, J. B., Time Dependent Breakdown of Ultra-Thin Gate Dielectrics Under Pulsed Biased Stress, IEEE Elec. Dev. Lett, vol. 22, no. 5, pp. 224-226, 2001.

# Nanoelectronic Device Metrology

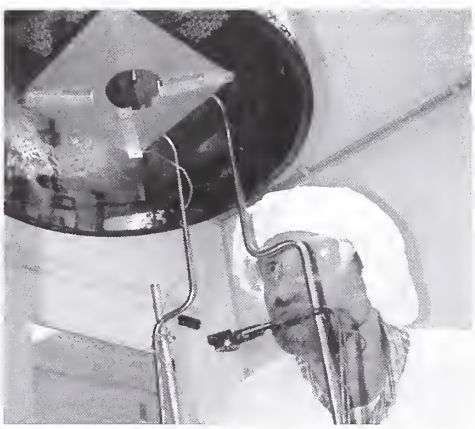
**Technical Contact:**
Curt A. Richter

**Staff-Years (FY 2002):**
2.5 professionals
1 technician
1 guest researcher

**Funding Sources:**
NIST (100%)

## Goals

The overall goal of the Nanoelectronic Device Metrology (NEDM) Project is to develop the metrology that will help enable new nanotechnologies (such as molecular electronics and Si-based quantum devices) to supplement and/or supplant conventional Complementary Metal Oxide Semiconductor (CMOS) devices. This involves determining the critical metrology needs for these exploratory technologies. One specific goal is to develop test structures and methods to measure reliably the electrical properties of small ensembles of molecules. A second targeted goal is to develop the precise metrology and characterization methods required for the systematic characterization of Si-based nanoelectronic devices.



**John Suehle loading a sample for metallization on cryogenic chuck.**

## Customer Needs

The CMOS FET (Field Effect Transistor), which is the current basis of ULSI (Ultralarge-Scale Integration) circuits, is beginning to show fundamental limits associated with the laws of quantum mechanics and the limitations of fabrication techniques. By 2005, the Semiconductor Industry Association's (SIA's) 1999 International Technology Roadmap for Semiconductors (ITRS) shows no known solutions for a variety of technological requirements including gate dielectric, gate leakage, and junction depth. Therefore, it is expected that entirely new device structures and computational paradigms will be required to augment and/or replace standard planar CMOS devices. Two post-CMOS technologies that show promise to extend traditional scaling laws for increased computational performance beyond the limits of conventional CMOS are molecular electronics and Si-based quantum electronic devices.

Molecular electronics (ME) is a field that many predict will have important technological impacts on the computational and communication systems of the future. In ME systems, molecules perform the functions of electronic components. This task is one component of a major NIST Competence Building Project that is funded by the NIST Program Office and was started in FY 2001. The Molecular Electronics Competence is a cross disciplinary, inter-laboratory effort at NIST (EEEL and CSTL - the Chemical Sciences and Technology Laboratory) with an overall objective to develop the measurement science that will enable molecular electronics to blossom into a viable industry.

Research and development for silicon-based nanoelectronics (e.g., wrap-around FETs, Si-based RTDs [resonant tunneling diodes], silicon quantum dots) for the post-CMOS era is currently of interest due to its inherent compatibility with CMOS technology.

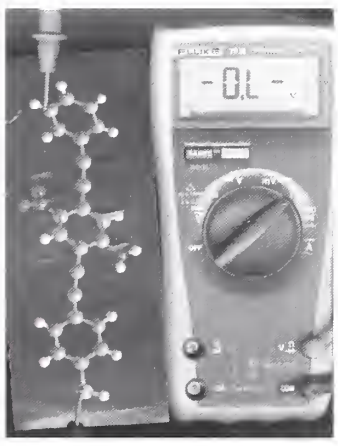
The NEDM Project is concerned with fundamental research related to possible future devices that will replace or augment standard CMOS technology. In order to ensure that our research is technically relevant, we plan to align ourselves with research described by the Microelectronics Advanced Research Corporation (MARCO), alluded to in SIA's Roadmap and other similar semiconductor industry organizations and documents.

The industry for these emerging nanoelectronic devices will require reference data, standards, precision measurement protocols, and standardized test structures and associated measurement protocols to develop into a viable commercial technology. The ultimate objective of the project, of course, is to provide the measurement infrastructure to aid this development. Through strong ties with industry leaders and cutting-edge researchers, we are accelerating the pace of our program and focusing our research on the most relevant technologies.

## Technical Strategy

The Nanoelectronic Device Metrology Project, which is newly established in FY 2002, will investigate and develop metrology for two specific areas of nanotechnology: molecular electronics and Si-based quantum electronics.

ME is a field that many predict will have a revolutionary impact on future computational systems. These predictions arise because the majority of molecules are intrinsically small and thus already at the size-scale that future CMOS is driving towards. Furthermore, modern synthetic chemistry techniques allow atomic control over a wide variety of molecular structures allowing ME systems to be flexible. Our objectives are to develop methods to reliably and reproducibly measure the electrical properties of small ensembles of molecules in order to investigate molecular conduction mechanisms. We plan to develop robust molecular test structures and use them to measure the electrical properties of molecules. Specifically, we are developing test-structures based upon nanofabrication and NEMS (Nano-Electro-Mechanical Systems) processing techniques for assessing the electrical properties and reliability of moletronic molecules. (One example, the "nano-Bucket," is illustrated in the last figure.) Molecules will be incorporated into the test structures via self-assembly to form high-quality SAMs (self-assembled monolayers). In addition to the complexity of the nanofabrication of test structures, the challenges associated with measuring the electrical properties (such as current-voltage and capacitance-voltage as functions of temperature and applied fields) of these small molecular ensembles are daunting. The measured electrical properties will be correlated with systematic characterization studies by a variety of advanced analytical probes and the results used in the validation of predictive theoretical models.



**Electrically measuring molecules, the concept.**

The major scientific objectives and goals of the ME task are:

- A NIST standard suite of molecular test structures.
- Fundamental understanding of charge transport through molecules and molecular ensembles.

The new Si-nanotechnology task will focus on physical and electrical metrology of the basic building blocks of silicon quantum electronic devices (e.g., quantum layers, wires, and dots of silicon surrounded by silicon dioxide). By identifying and addressing the critical metrology issues associated with these basic building blocks, the basis of metrology for future Si-based ULSI nanotechnology will be defined.

A major goal is to fabricate single quantum dots and wires with controllable size. These will be used to establish the relationship between the key fabrication conditions, physical properties (such as the geometry of the quantum-dot and the tunneling barrier), and final electrical properties of these floating silicon devices (i.e., metal-oxide-silicon-oxide-silicon [MOSOS] devices). Production of MOSOS capacitor structures is an intermediate step en route to this end goal. This research will provide the information necessary to help identify and address the necessary electrical and physical characterization methodologies.

Developing the metrology for "beyond-CMOS" nanoelectronic devices is a challenging and multidisciplinary task; therefore, it is important to be teamed with strong collaborators. The ME staff is part of a NIST Competence Project with CSTL. CSTL provides the bulk of the molecules we will use, provides insights into SAM formation, performs precise structural characterization, and performs advanced quantum chemistry theoretical analysis. In addition, the ME task is working with various companies, universities, and government laboratories (e.g., Hewlett-Packard (HP), Yale University, University of North Texas, Naval Research Labs). The quantum Si device task is working closely with NIST's Electricity Division to study Si-based single-electron tunneling devices.

***"...there is no particular reason why Moore's law should continue to hold: it is a law of human ingenuity, not of nature. At some point, Moore's law will break down. The question is when?"***

*Seth Lloyd, d'Arbeloff Laboratory for Information Systems and Technology, Massachusetts Institute of Technology*

## Accomplishments

■ *Establishing the Nanoelectronic Device Metrology Project.* In FY 2001, the NIST ME Competence was established. Extensive plans were developed and funding was acquired for this effort. Plans were also established for the Si-based quantum electronics task.

■ *Infrastructural Development.* A substantial portion of the first year was spent in developing a molecular electronics infrastructure. This included the specification and procurement of a

***"If individual molecules can be made to process information, they could be the answer to the computer industry's prayers."***

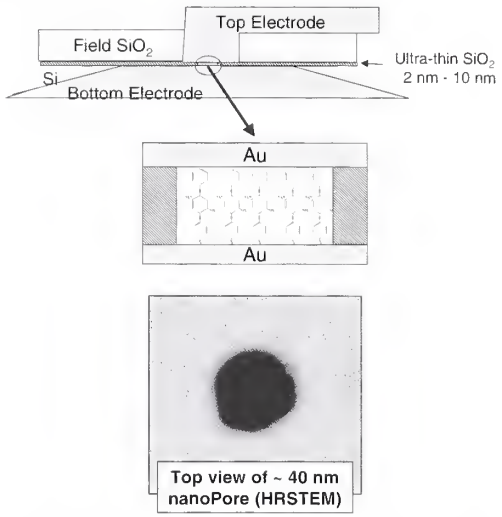
*P. Ball, Consultant Editor, Nature, vol. 406, 13 July, 2000, pp. 118-120*

new backside mask aligner, a new metal deposition system, as well as the expected early FY 2002 purchase of a plasma deposition and etching system. By combining this new equipment with the existing capabilities, including electron-beam (e-beam) writing, in the Microfabrication Process Facility, our fabrication capabilities will be at the forefront of ME research.

- *Development of nano-Bucket Fabrication Processes.* A specific device structure has been identified for the NIST "nano-Bucket" test structure, and a detailed process flow has been designed. Key processing steps (that combine NEMS techniques with planar integrated circuit processing methods) have been developed for the nano-Bucket. For example, suspended membranes have been fabricated with a variety of film thicknesses and areas from low-stress silicon nitride/silicon dioxide stacks, and ultra-thin silicon dioxide films with molecular length-scale thicknesses have been thermally grown and optically characterized. A variety of photolithographic masks that define various levels of the nano-Bucket test structure has been designed and manufactured. The metal/molecule interfaces are critical, and a custom-designed $LN_2$ chuck for controlled low-temperature thermal evaporation of metals has been fabricated and installed in a filament evaporation system in order to determine optimal methods for metal deposition. A collaboration with Yale University (M. A. Reed) is underway to extend their existing nanopore technology and develop nanopore characterization methods based upon their nanopores. In addition, alternative planar test structures (such as cross-bar devices) have also been designed and are in the initial stages of development.

- *Electrical Measurements.* We developed an initial suite of electrical test procedures for molecular devices. In collaboration with HP Laboratories, we were the first researchers to independently confirm electrical current-voltage characteristics of moletronic devices supplied by HP. Also, we made the world's first ever capacitance-voltage characterizations of self-assembled molecules by using these structures from HP.

- *Spectroscopic Measurements.* It is postulated that the structure of the molecular monolayers and the molecule-metal interface play a pivotal role in through-molecule charge transport in moletronic devices. Spectroscopic ellipsometry and other optical spectroscopies (in collaboration with CSTL) have been used to investigate the structure of a compound that is a molecular conductor and a molecular switch.




**Schematic of the NIST "nano-Bucket" molecular test structure.**

- *Development of Collaborations.* To accelerate and enhance our program, we have established collaborative research efforts with leading research teams. The Quantum System Research Group at the HP Laboratories provided us with moletronic systems test structures developed at HP. These allowed us to develop and perfect test procedures, as well as make the first-ever capacitance-voltage measurement on a moletronic system. Another profitable collaboration has been with the Defense Advanced Research Projects Agency (DARPA) funded Nanocell Molecular Computer Collaboratory of Rice University (J. M. Tour), Pennsylvania State University (P. S. Weiss and D. L. Allara), and Yale University (M. A. Reed). Members of this consortium synthesized and gave us the switching and conductive molecules used in the spectroscopic experiments; these will be used in upcoming test-structure measurements. This team also has provided us with nanometer-sized test structures used to screen moletronic systems. These will be used in upcoming electronic property tests. Bruce Gnade (University of North Texas and part of the Naval Research Lab's molecular electronics team) is a strong collaborator and sometimes guest researcher. We are currently exploring collaborative opportunities with other leading laboratories as well.

# Thin-Film Process Metrology

## Goals

Develop new and improved electrical and optical measurements, models, data, and reference materials to enable better and more accurate measurements of select, critical, thin-film parameters for silicon Complementary Metal Oxide Semiconductor (CMOS) technology. Major focus is placed on requirements for oxynitrides, and metal-oxide and metal-silicate films and stacks for advanced gate dielectrics detailed in the 1999 International Technical Roadmap for Semiconductors (ITRS).

**Nhan Van Nguyen (left) and Yong Cho (right) aligning sample on custom-built high-accuracy spectroscopic ellipsometer.**

## Customer Needs

The evolving decrease of the gate dielectric film thickness to an oxide-equivalent value of 1 nm is identified as a critical front-end technology issue in the Semiconductor Industry Association's (SIA's) International Technology Roadmap for Semiconductors (ITRS). For effective gate dielectric thicknesses below ~2.0 nm, $SiO_2$ is being replaced, initially by oxynitrides or oxide/nitride stacks, and then by either metal-oxides or metal-silicates. Process control tolerance needs for dielectric thickness are projected to be ± 4 % (3 σ), which translates to less than 0.1 nm for 2 nm films. Requirements for process control measurements are a factor of ten smaller still.

Spectroscopic ellipsometry (SE) is expected to continue as the preferred measurement for process monitoring of future gate dielectric films. Industry metrology needs not only improved methods to determine film thickness accurately, but also (1) techniques to determine the structure of the individual films and the interfaces between them; (2) understanding of the relationship between physical, electrical, and optical determinations of film properties; and (3) mechanisms, such as reference materials, for traceability of measurements to NIST to support film metrology.

In order for SE to meet process control requirements of film thickness and unambiguously determine film composition and morphology, the optical properties of these advanced dielectric film systems must be characterized and understood.

## Technical Strategy

This project focuses on the issues of (1) developing and providing the basis for traceability to NIST for film thickness measurements, (2) identifying structural models and developing preferred optical index dispersion functions or data for improved ellipsometric analysis of future-generation gate dielectric film systems, and (3) correlating optical, electrical, and physical measurements of thickness, composition, and interface structure.

### Establish and Transfer Basis of Accuracy for Thin Dielectric Films

Industry requirements for future thin dielectric film optical measurements and calibration standards were identified at a NIST-sponsored workshop in FY 1998. Core ellipsometry measurement capability is being expanded and strengthened to meet these requirements. An investigation has been started into cleaning and recontamination issues for film calibration standards to determine whether a workshop-expressed goal of 0.015 nm long-term reproducibility of reference artifact values is obtainable. Procedures are being developed to enable traceability of instrument accuracy to NIST for suppliers of secondary thin-film reference materials without requiring volume production of NIST standard reference materials.

**DELIVERABLES:** By 2003, develop and evaluate prototype procedures that will enable traceability to NIST for 1st level commercial suppliers of reference materials for oxide films down to 2 nm.

### Structural and Optical Models for Ellipsometry

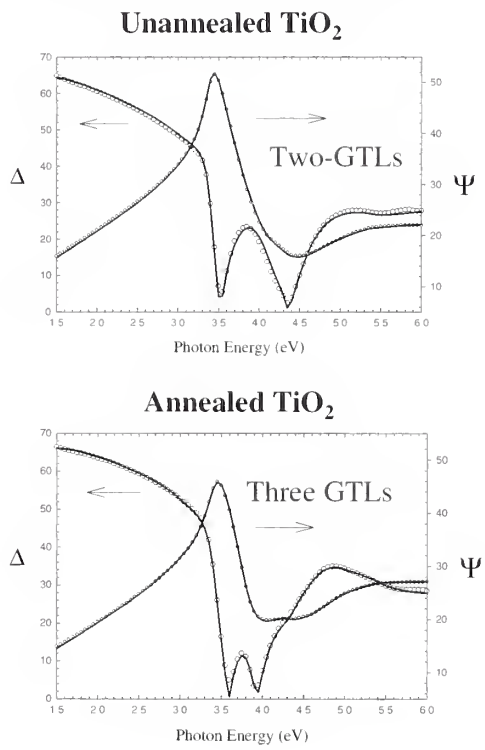
A custom-built, high-accuracy spectroscopic ellipsometer with a spectral range of 1.5 eV to 6 eV is being used for this task, and project staff are working with International SEMATECH, IC industry companies, and SRC university staff to

**Technical Contact:**
James R. Ehrstein

**Staff-Years (FY 2001):**
4 professionals
1.7 technicians
3 guest researchers

**Funding Sources:**
NIST (93%)
Other (7%)

obtain and optically characterize advanced oxynitrides, oxide/nitride stacks, and metal oxide and silicate films such as zirconium oxide and hafnium silicate. Characterization will be extended to 8.5 eV to include important optical index structure of these films beyond their bandgaps. This work is directed at determining preferred structural models, spectroscopic index of refraction values, or preferred optical dispersion functions for each of these film systems, and, where possible, the variability of these parameters due to differences in film fabrication processes. Analysis is done with software developed by NIST for spectroscopic ellipsometry; this software allows maximum flexibility for the addition of the latest published or custom-developed optical response models as appropriate for each material system investigated.




**Fitting the complex ellipsometry spectra of $TiO_2$ with the recently NIST-developed Generalized Tauc-Lorentz Dispersion functions.**

**DELIVERABLES:** By 2002, evaluation of advantages of extended UV ellipsometry for analysis of high-κ and stacked dielectric films.

### Relation Between Optical, Electrical, and Physical Measurements of Thickness

Through collaborations with International SEMATECH, IC industry companies, and SRC university staff, as well as with key researchers in other parts of NIST, project staff are leading and participating in a number of multimethod comparison studies of various ultra-thin gate dielectric films. These multimethod studies utilize techniques such as X-ray and neutron reflectivity, High-Resolution Transmission Electron Microscopy (HRTEM), Electron Energy Loss Spectrometry (EELS), angle-resolved X-ray Photoelectron Spectroscopy (XPS), Secondary Ion Mass Spectrometry (SIMS), Capacitance-Voltage (C-V) and Current-Voltage (I-V) analysis, as well as spectroscopic ellipsometry and reflectivity. The results of these multimethod studies improve the general understanding of state-of-the-art (SOA) measurement capability for very thin films and also allow project staff to assess the results of various optical models being applied to the analysis of these films with respect to interface layers and structural composition, morphology, and uniformity. SOA C-V and I-V measurement capability for gate films has been established in the project. Advanced 1-D analysis software from commercial and university sources has been established and benchmarked to determine the effect of model and algorithm sophistication on oxide film thickness values calculated from C-V and I-V data. An extension to 2-D modeling is planned.

**DELIVERABLES:** By 2003, integrate preferred advanced electrical analysis software and structural analyses of high-κ dielectrics to improve agreement between electrical and ellipsometric thickness scales.

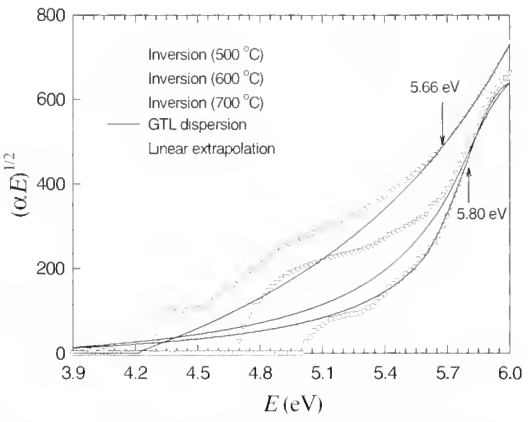
## Accomplishments

■ *Completed extensive upgrade of master high-accuracy ellipsometer that was originally developed for certifying oxide thickness SRMs.* The upgrade is intended to enable attainment of improved short-term and long-term precision necessary to meet industry needs for thin dielectric measurement traceability. Upgrades included a power/frequency stabilized HeNe laser, large area photodiode, new A/D electronics with higher conversion resolution, improved low noise motor drive for the rotating analyzer, and completely rewritten system control and data acquistion software in a format that enables easier maintenance and upgrade. An autocollimator to monitor the stability of a sample alignment, a temperature readout in the vicinity of the wafer, and monitoring of laser power were also added to enable identification of possible sources of unacceptable measurement variability. Initial tests showed sample alignment to be stable to better than 0.001 ° over many

hours, very good short term (1/2 hour timeframe) sample measurement stability. However, full-day precision was inconsistent with only partial correlation of variability with temperature. A matrix of additional thermocouples is being added to a variety of points in the ellipsometer to better pinpoint measurement sensitivity to the temperature of various system components.

■ *A three-pass sample exchange for single-wavelength (SWE) and SE measurement of film thickness was completed by NIST and VLSI Standards Inc.* The samples were a set of silicon nitride films of moderate-to-larger thicknesses. SWE measurements from both laboratories were in excellent control and showed good agreement of film thickness values. Relatively large discrepancies resulted from the SE measurements at both laboratories, however. This occurred despite careful planning that included such factors as using optical constants for silicon and silicon-nitride at 632.8 nm that were taken from the spectroscopic database for these materials. This experiment is being used by NIST to develop an understanding of potential pitfalls in measurement exchange programs that are expected to be used as the basis for future programs to offer film thickness measurement traceability to NIST. In the case of the silicon-nitride sample exchange, additional investigation of sources of observed SE discrepancies is ongoing.

■ *Several sets of oxynitride and metal-oxide/silicate films were measured by SE in order to determine preferred structural models and optical dispersions for determining film thickness, dielectric function, and the possible existence of interface layers.* One of these, a set of $HfO_2$ films, fabricated by physical vapor deposition and annealed at temperatures from 500 °C to 700 °C, was measured over the energy range 1.5 eV to 6.2 eV. The 500 °C annealed specimen was fit well with a single Tauc-Lorentz (T-L) dispersion without need to include any surface roughness. However, the films annealed at 600 °C and 700 °C manifested extra structure above the band gap, which required the use of a second T-L dispersion in each case to fit the data adequately. This secondary structure is attributed to the formation of a polycrystalline phase due to elevated temperature. While all samples showed an extended low energy tail of the dielectric function, the tail was shorter for the two higher annealing temperatures. Comparison of the energy gap values for these films, as determined by a fitting parameter identified as Eg in the T-L dispersion and also by the regression models of Tauc and of Balog, gave inconsistent results. Thus, a robust method for band-gap determination for such films is one of the remaining challenges in their optical characterization.




**Difficulty determining optical band-gap of high-κ materials due to defect-related band tail states.**

■ *Developed a generalized dielectric dispersion function, called Generalized Tauc-Lorentz (GTL), to expand capability of analyzing the variety of dielectric-function shapes found from SE measurements of high-κ dielectric films fabricated by a variety of processes.* The GTL, which is Kramers-Kronig consistent, generalizes a quadratic exponent found in the T-L dispersion, allowing it to have values 1 through 4. The GTL also includes one additional fitting parameter, Ep, related to the Urbach tail, that is not found in the T-L dispersion. Other common dispersion functions, such as T-L, Lorentz, and harmonic oscillator, are all special cases of GTL with m = 2. The exponent, m, yields four different shape functions for the values 1 through 4. Initial evaluation of possible benefits of having these four shape functions was done by fitting literature data for a-silicon, $Si_3N_4$, and SiO. The dielectric function data for these materials were shown to be best described by GTLs with m = 2, 3, and 4, respectively. The GTL with m = 1 was found to have a shape function that is well suited to films that have a very sharp absorption edge.

■ *An extensive comparison of the most advanced Quantum Mechanical (QM) C-V simulators was extended in a number of aspects.* A systematic comparison of QM simulators for p-channel (n-substrate) devices was performed. The number of 1-D simulators in the test ensemble was extended to seven. Quantitative differences in the accumulation capacitance with ultra-thin

***"Rudolph Technologies Inc. believes there is a significant need for ... a sub-40Å oxide ... NIST traceable reference material."***

*Dr. David Leet, Director, Strategic Planning and Advanced Applications, Rudolph Technologies, Inc.*

gate dielectric films were up to 20 % - similar to previously reported differences for n-channel devices. Some of the underlying physical and modeling differences leading to these differences were identified, investigated, and reported. A complex interplay of a number of factors was found.

*A method to extend the comparison to include 2-D simulators also was investigated and demonstrated.* A model test structure was developed, refined, and calibrated for use with Medici, a commercial 2-D simulator, to ensure that a quasi-1-D device was being simulated. Requests have been received for permission to use figures from this work in manuscripts, presentations, and a University MOSFET (Metal-Oxide Semiconductor Field Effect Transistor) class.

## FY Outputs

### Collaborations

- N.C. State Univ., KLA-Tencor, and International SEMATECH, development and characterization of 2 nm thick oxide reference materials; and VLSI Standards Inc. and Rudolph Technologies Inc., measurement traceability experiments for $SiO_2$ and $Si_3N_4$ film thickness.
- NIST Divisions 837, 842, and 852; Univ. Maryland, Univ. Minnesota, NC State Univ., Univ. Texas-Austin, UCLA, and Yale Univ; and IBM, Solid State Measurements, Texas Instruments, and International SEMATECH, studies of optical, electrical, and physical measurements and properties of oxynitrides and high-$\kappa$ dielectric films.
- Penn State Univ. and Univ. Maryland, development and transfer of ellipsometer techniques and models for analysis.
- NIST Division 854 and International SEMATECH, spectroscopic ellipsometry characterization of low-$\kappa$ $SiO_2$ thin films.
- NIST Divisions 836, 837, and 838, Dr. Roger van Zee et al., Molecular Electronics Competence Project; and Penn State Univ., Yale Univ., Naval Research Laboratory, and Hewlett Packard, materials and test structures for molecular electronics.

### Standards Committee Participation

- ASTM F-1 on Electronics, Membership Secretary and Member of Executive Subcommittee (James R. Ehrstein)
- ASTM F-1 on Electronics, Subcommittee F1.06 on Silicon Materials and Process Control, Chairman and Ballot Coordinator (James R. Ehrstein)
- ASTM F-1 on Electronics, Subcommittee F1.06, Section B on Thin Film Characterization, Section Chair (James R. Ehrstein)

### External Recognition

- Service Award from Lehighton Electronics, Inc., in recognition of commitment and outstanding work in developing and providing NIST standard reference materials for resistivity measurement (James R. Ehrstein)

## Recent Publications


Chism, W., Diebold, A., Canterbury, J., and Richter, C., Characterization and Production Metrology of Thin Transistor Gate Dielectric Films, Solid State Phenomena, vols. 76-77, pp. 177-180., 2001.

Cresswell, M. W., Arora, N., Allen, R. A., Murabito, C. E., Richter, C. A., Gupta, A., Linholm, L. W., Pachura, D., and Bendix, P., Test Chip for Electrical Linewidth of Copper-Interconnection Features and Related Parameters, Proceedings of the 2001 IEEE International Conference on Microelectronic Test Structures, Kobe, Japan, Mar. 19-22, 2001, vol. 14, pp. 183-188.

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Nguyen, N. V., Richter, C. A., Cho, Y. J., Alers, G. B., and Stirling, L. A., Effects of High Temperature Annealing on the Dielectric Function of $Ta_2O_5$ Films Observed by Spectroscopic Ellipsometry, Applied Physics Letters, vol. 77, no. 19, pp. 1-3, 2001.

Richter, C. A., Hefner, A. R., and Vogel, E. M., A Comparison of Quantum-Mechanical Capacitance-Voltage Simulators, IEEE Electron Device Letters, vol. 22, no. 1, January 2001, pp. 35-37.

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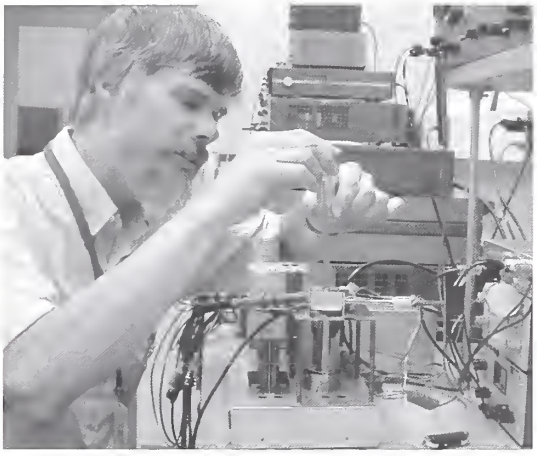
Richter, C., Vogel, E., Hodge, A., and Hefner, A., Differences Between Quantum-Mechanical Capacitance-Voltage Simulators, SISPAD Technical Digest 2001 (2001 International Conference of Simulation of Semiconductor Processes and Devices), 4 p.

# Metrology for Simulation and Computer-Aided Design

## Goals

The goal of the project is to facilitate the efficient and reliable application of semiconductor computer-aided design (CAD) tools and System-on-a-Chip (SoC) design methodologies by providing leadership for the development of an industry infrastructure for establishing model accuracy, developing methods for simulator model validation and benchmarking, developing metrology necessary for providing model data and model parameter extraction sequences, and developing metrology infrastructure required for a block-based design paradigm.



**David Berning measuring silicon carbide diodes using NIST-developed, specialized equipment, not commercially available.**

## Customer Needs

Efficient and reliable simulation methods are becoming more important as device structures and packages rapidly evolve. In addition, higher speed and higher power devices increase the importance of including the effects of packages in system performance simulation. However, advanced device electrical and thermal characterization procedures and validation of models used in computer-aided design tools have not kept pace with the application of the new device types and processes.

Several device technologies have evolved to an extent that conventional modeling and simulation capabilities are not suitable. For example, as Complementary Metal-Oxide Semiconductor (CMOS) devices are scaled to atomic dimensions, simulators must include quantum mechanical (QM) physics. The SRC/NIST/NSF Workshop on Nanoscale Transistors: Technology, Physics, and Simulation (Feb. 1999) identified QM device simulation as an area required for device simulator progress. In addition, the device types used for power and microwave applications can no longer be represented by conventional device models provided in circuit and system simulation programs.

The driving force in today's semiconductor industry is the need to maintain a rate of improvement of 2x every two years in high-performance components. Currently, these improvements rely exclusively on advances made in semiconductor miniaturization technology. The 1999 ITRS (International Technology Roadmap for Semiconductors) suggests that, "innovation in the techniques used in circuit and system design will be essential to maintain the historical trends in performance improvement." Achievement of this advancement in circuit and system design techniques is increasingly becoming dependent on integrating multiple silicon technologies into an SoC. Design challenges for SoC are overcome with the use of block-based design approaches that emphasize design reuse that include Built-In Self Test (BIST) functions and accommodate Design-For-Test (DFT).

## Technical Strategy

NIST addresses these needs by developing the theoretical foundations, standards, model validation procedures, and associated experimental techniques for the measurement of device system block electrical and thermal characteristics, and package electrical and thermal characteristics. NIST is developing, with industry, accepted procedures for validating device models for circuit simulation. NIST is developing procedures for characterizing the thermal and electrical performance of micro-electronic packages that are compatible and useful for CAD of boards and systems.

### Device and Process Simulation Benchmarking

Accurate models and benchmarking procedures are becoming more important for device and process simulators. Current tasks include development of mobility, band gap, and intrinsic carrier concentration models for accurate simulation of compound semiconductor devices, and benchmarking of semiconductor device simula-

**Technical Contact:**
Allen R. Hefner, Jr.

**Staff-Years (FY 2001):**
3 professionals
9 guest researchers

**Funding Sources:**
NIST (100%)

tion tools that include QM effects, including MEDICI, UTQuant, NCSU code, and NEMO.

**DELIVERABLES:** By 2002, complete benchmarking of QM effects in 2-D device simulator for MOSFET (Metal-Oxide Semiconductor Field Effect Transistor) with ultra-thin gate oxide.

***"These new silicon carbide devices are powerful additions to our line of surface mount Schottky diodes ... We expect their combination of efficiency and high voltage to be particularly valuable in cardioverter defibrillator applications, military aircraft and high voltage telecommunication switching equipment."***

*Manuel Lynch, Vice President of Business Development, Microsemi Corp.*

### Compact Package Electrical Interconnect Models

Interconnect structures are becoming a dominant factor in limiting the performance of modern computer, communication, and power systems. The Time-Domain Reflectometry (TDR) technique is being applied to characterize various multi-chip module and discrete packages interconnect systems.

**DELIVERABLES:** By 2002, publish document describing a TDR test system with low source impedance (10 Ω), and characterize low-impedance interconnects used in microprocessor voltage regulator modules, advanced memory busses, and power electronic systems.

### Package Thermal Metrology and Models

Accurate and timely simulation of system thermal performance requires new temperature measurement methods, new simulation methodologies, and validation procedures. Current tasks include the NIST electro-thermal network simulation methodology, including thermal network component models for semiconductor packages and heatsinks, and the development of methodologies to validate the performance and accuracy of compact package thermal models.

### Compact Device Electrical Models

Only recently has there been a significant effort in developing an infrastructure for validating the performance of compact models. An example of this activity is the NIST/IEEE Model Validation Working Group, founded in 1994 and now having over 200 members from 100 different technical organizations. For more information see ray.eeel.nist.gov/modval.html.

**DELIVERABLES:** By 2003, develop test system and models for SiC three terminal device.

### Metrology for Multi-Technology SoC System Blocks

The emergence of the block-based design paradigm that emphasizes design reuse imposes various metrology and standardization challenges. The NIST research provides the metrology infrastructure required to facilitate the emergence of effective SoC design methodologies for multi-technology systems. Current tasks include (1) development of test structures for multi-technology process monitoring, (2) development of measurement infrastructure to calibrate multi-technology BIST functions for system sub-blocks; (3) development of metrology to validate behavioral models for the multi-technology system blocks, and (4) development of benchmarking procedures for system block, simulation-based Analog Hardware Description Language design.

**DELIVERABLES:** By 2004, complete development of test bench on a chip metrology necessary for multi-technology SoC, block-based design, and develop test structures for monitoring multi-technology SoC processes.

## Accomplishments

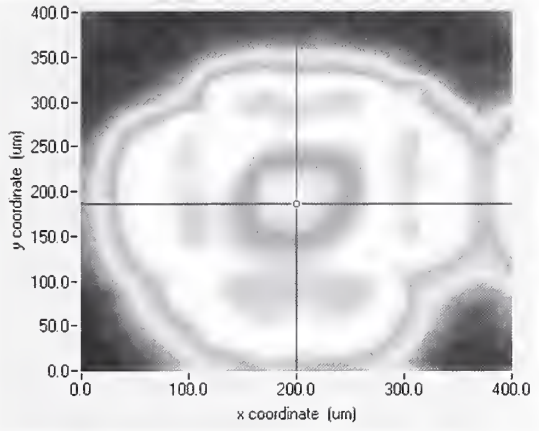
■ *NIST provided state-of-the-art measurement capability to aid in the development of SiC (Silicon Carbide) Schottky power diodes.* Through collaboration with CREE, Inc. (Durham, NC), prototype SiC diodes of various designs made by researchers at CREE were put through a variety of tests to measure their voltage and current characteristics, switching speed, and temperature parameters by NIST researchers Hefner and Berning. The combination of the voltage and speed capability of these diodes required the development and construction of specialized equipment not commercially available. Meanwhile, under a collaborative effort between NIST, CREE, and Virginia Tech University, these prototype diodes also were evaluated for energy savings and EMI emissions in switching power-supply circuits. As a result of this developmental and measurement effort, CREE and Microsemi Corp. (Irvine, CA) have formed an alliance to make and market a SiC diode line. Microsemi announced the commercial availability of a series of SiC diodes on Sept. 27, 2001.

■ *Developed SoC test-bench.* The test-bench provides the capability of testing multiple device types on a single chip. The system studies the interactions between biosensors, voltage controlled oscillators, and analog to digital converters. The system also studies the effects of post process HF etching on SoC devices. Angela Hodge presented an invited paper discussing this testbench at a special session of the IEEE International Symposium on Circuits and Systems. The purpose of this symposium was to uncover

the latest advances in SoC research, bio-sensors, and related systems.

- *Benchmarking 2-D QM simulator, Medici, led to uncovering weaknesses in the simulator.* This discovery resulted in Avanti Corporation's decision to improve the model for its most recent release of the software.

- *Completed calibration procedure and validated the accuracy for the high-speed semiconductor device transient thermal imaging system.* This system provides the capability to measure the transient temperature distributions with 10 ns temporal and 15 µm spatial resolution. The system required the development of algorithms for calibrating and extracting the transient temperature waveform from an infrared microscope signal.




**Thermal image of a MEMS-based hotplate during a transient event.**

## FY Outputs

### Collaborations

- Analogy/POWERX/NIST, development of high power IGBT module library component models (Allen R. Hefner)

- Avanti Inc., characterization of electronic packages for thermal model library component models (Allen R. Hefner)

- Avanti Inc., parameter extraction for IGBT library component models (Allen R. Hefner)

- Avanti Inc./University of Arkansas, SiC power diode model cam library (Allen R. Hefner)

- CREE, SiC diodes (David W. Berning)

- CREE/NIST, development of SiC MPS-diode electro-thermal model (Allen R. Hefner)

- DELPHI/Virginia Polytechnic Institute and State University, electronic interconnect characterization for vehicle auxiliary motor drive interconnects (Allen R. Hefner)

- Division 811 (Nick Paulter), under ATP project to develop low-impedance transmission line characterization (David W. Berning)

- Division 811, development of low-characteristic impedance time domain reflectometry (Allen R. Hefner)

- Division 811, Jim St. Pierre, collaborating on defining research goals for metrology and benchmarking related to SoC (Angela M. Hodge)

- Division 811, metrology for SoC design reuse (Allen R. Hefner)

- Division 811, metrology and standardization for the use of Virtual Components (VCs) in SoC devices, January 2001 - ongoing (Angela M. Hodge)

- Division 812, Scanning-Probe Microscope Metrology Project, implant simulation and device simulation (Allen R. Hefner)

- Division 812, Thin-Film Process Metrology Project/Gate Dielectric and Interconnect Reliability Project, benchmarks for QM device simulation (Allen R. Hefner)

- General Electric CRD/NIST, development of IGBT module models and parameter extraction tools (Allen R. Hefner)

- Harris Semiconductor, development of component models for Harris IGBTs (Allen R. Hefner)

- Rockwell Science Center/NIST, development of SiC transistor models (Allen R. Hefner)

- TMA, implementation of new device physics into Medici device simulator (Allen R. Hefner)

- University of Maryland, 2-D QM simulator analysis, Sept. 1, 2000 - Sept. 30, 2001 (Allen R. Hefner, Angela M. Hodge, and Curt A. Richter)

- University of Maryland, BIST for SoC, Sept. 1, 2000 - Sept. 30, 2001 (Angela M. Hodge)

- University of Maryland, metrology for multi-technology SoC (Allen R. Hefner)

- University of Maryland, Professor Neil Goldsman, collaborating on benchmarking QM simulators for semiconductor devices (Angela M. Hodge)

- University of Maryland, Professor Robert Newcomb, collaborating on defining research goals and objectives for NIST/SED initiative on SoC (Angela M. Hodge)

- University of Maryland, QM effects in 2-D semiconductor device simulators (Allen R. Hefner)

- Virginia Polytechnic Institute and State University, package interconnect electrical characterization (Allen R. Hefner)

- Virginia Polytechnic Institute and State University, SiC power device utilization (Allen R. Hefner)

- Virginia Polytechnic Institute, SiC diodes (David W. Berning)

### Standards Committee Participation

- EIA/SEMATECH Compact Model Council (Allen R. Hefner)

- IEEE Electron Devices Society, Standards Technical Committee, Chairman (Allen R. Hefner)

## Recent Publications


Bayne, S. B., Portnoy, W. M., Rohwein, G. J., and Hefner, A. R., MOS-Gated Thyristors (MCTs) for Repetitive High Power Switching, IEEE Transactions on Power Electronics, vol. 16, January 2001, pp. 125-131.

Berning, D. W. and Hefner, A. R., IGBT Model Validation for Soft-Switching Applications, IEEE Transactions on Industry Applications, vol. 37, no. 2., March/April 2001, pp. 650-660.

Hefner, A. R., Singh, R., Lai, J-S., Berning, D. W., Bouche, S., and Chapuy, C., SiC Power Diodes Provide Breakthrough Performance for a Wide Range of Applications, IEEE Transactions on Power Electronics, vol. 16, no. 2, March 2001, pp. 273-280.

Hefner, A., Berning, D., Blackburn, D., Chapuy, C., and Bouche, S., A High-Speed Thermal Imaging System for Semiconductor Device Analysis, proceedings of the Seventeenth Annual IEEE Semiconductor Thermal Measurement and Management Symposium, pp. 43-49, 2001.

Hefner, A., Jr., Berning, D., Lai, J. S., Liu, C., and Singh, R., Silicon Carbide Merged PiN Schottky Diode Switching Characteristics and Evaluation for Power Supply Applications, in conf. record IEEE Industry Applications Society Meeting, October 2000, pp. 2948-2954.

Hodge, A., Newcomb, R., and Hefner, A., Use of the Oscillation Based Built-in Self-test Method for Smart Sensor Devices, Conference Proceedings - 2001 IEEE International Symposium on Circuits and Systems, vol. 2, pp. 281-284, 2001.

Huang, X., Yu, H., Lai, J., Hefner, A. R., and Berning, D. W., Characterization of Paralleled Super Junction MOSFET Devices under Hard- and Soft-Switching Conditions, Proceedings of the Power Electronics Specialist Conference, June 2001, pp. 2145-2150.

Lai, J. S., Song, B. M., Zhou, R., Nguyen, H., Hefner, A., Berning, D., and Shen, C., Characterization and Utilization of a New Class of Low On-Resistance MOS-Gated Power Device, IEEE Transactions on Industry Applications, September 2001, 7 p.

McNutt, T., Hefner, A., Montooth, A., Duliere, J., Berning, D., and Singh, R., Silicon Carbide PiN and Merged PiN Schottky Power Diode Models Implemented in the Saber Circuit Simulator, Proceedings of the Power Electronics Specialist Conference, June 2001, pp. 2103-2108.

Richter, C. A., Hefner, A. R., and Vogel, E. M., A Comparison of Quantum-Mechanical Capacitance-Voltage Simulators, IEEE Electron Device Letters, vol. 22, no. 1, January 2001, pp. 35-37.

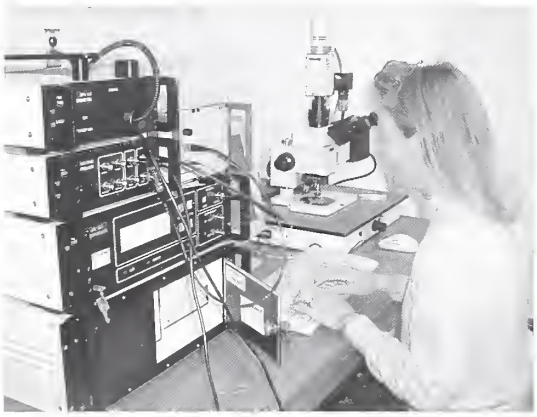
Richter, C., Vogel, E., Hodge, A., and Hefner, A., Differences Between Quantum-Mechanical Capacitance-Voltage Simulators, SISPAD Technical Digest 2001 (2001 International Conference of Simulation of Semiconductor Processes and Devices), 4 p.

Singh, R., Hefner, A., Berning, D., and Palmer, J., High Temperature Characteristics of 5 kV, 20 A 4H-SiC PiN Rectifiers, Proceedings of 2001 International Symposium on Power Semiconductor Devices and ICs, Jun. 4-7, 2001, Osaka, Japan, pp. 45-48.

# MicroElectroMechanical Systems

## Goals

The MicroElectroMechanical Systems (MEMS) Project has two research thrusts: (1) develop and provide domestic industry with MEMS test structures, test methods, measurement standards, and standard manufacturing practices; and (2) develop new MEMS based Micro-Metrology Tools and integrated measurement systems that improve measurements or create new innovation in measurement science.



**Janet Marshall investigating the measurement of Young's modulus using an optical vibrometer.**

## Customer Needs

### Measurements and Standards for MEMS

MEMS is a rapidly growing technology with a forecasted annual growth rate that exceeds that of the semiconductor electronics industry as a whole. Manufacturers of MEMS products, such as acceleration sensors for automotive air bags and deformable mirror displays for video projection, are producing these devices in Integrated Circuit (IC) manufacturing lines. This integration of mixed technologies is part of the semiconductor industry's revolution towards "system-on-a-chip." System-on-a-chip links the functionality of the IC (an information processor) with information gathering (sensing the environment) and actuation (acting on decisions). New test structures, test methods, and standards are required for device characterization.

In support for the need of measurement standards for MEMS, the project is working with ASTM Task Group E08.05.03 on "Structural Films for MEMS and Electronic Applications." This task group has undertaken sponsorship of a series of round robin experiments for the testing of residual stress and elastic modulus. MEMS test structures used in these experiments are designed and then fabricated on a test chip that is passed among participating laboratories. The measurement of film stress and elastic modulus is important to the fabrication of MEMS devices. Participation in the ASTM Task Group gives NIST a leadership role in the development of measurement standards for the industry.

MEMS test structures also have applications in measuring the mechanical properties of thin films in ICs, a need identified in the International Technology Roadmap for Semiconductors. As IC devices continue to shrink, thermo-mechanical stress in the thin films that interconnect them is an ever-increasing reliability concern. Current state-of-the-art IC technology uses five or more interconnect layers with aspect ratios (height/width) that can exceed 1.8. Despite the increasing number of interconnect layers in IC technology, existing stress determination and modeling studies have been limited to single level metallization, with few exceptions. This is due, in large part, to the lack of experimental techniques for measuring strain in narrow line width (less than 10 mm) and multilayer structures.

MEMS-based IC test structures allow, for the first time, the measurement of stress in multilayer structures in fully fabricated ICs. These measurements can be used to characterize the mechanical strain in these multilayer films. Results can then be used to verify finite element models of the stress in the films and to correlate mechanical stress data with reliability testing. MEMS-based test structures being developed in this project offer new ways to characterize the mechanical stress in multilayer films.

### Micro-Metrology Tools

Miniaturization technologies developed by the semiconductor industry such as thin-film deposition and growth, photolithography, etching, and micro machining are increasingly being used to make MEMS and NEMS (NanoElectroMechanical Systems) structures that are mechanical in nature. This technology can be thought of as an enabling technology; one that enables you to develop new measurement tools that can measure the physical world more precisely. The MEMS Project works collaboratively with many other projects in NIST to apply microfabrication and nanofabrication technologies to develop new

**Technical Contact:**
Michael Gaitan

**Staff-Years (FY 2001):**
2.5 professionals
6 guest researchers

**Funding Sources:**
NIST (100%)

***"... The MEMS through MOSIS foundry service [facilitated by the MEMS Project] paved the road for the establishment of the MUMPS and iMEMS foundry services."***

*Richard S. Payne, former Director of Manufacturing for Analog Devices Micromachined Products Division*

measurement tools. These tools are used to increase the accuracy of measurements or to develop new measurement methods.

## Technical Strategy

### Measurements and Standards

The MEMS technical community, composed of companies, universities, and government laboratories, has developed many types of test structures to characterize the fabrication process and device performance. What is lacking is standardized test methods and standard reference materials. The MEMS Project plays an active role in the new ASTM Task Group E08.05.03, metrology for thin-film electromechanical properties of MEMS-based IC technologies.

**DELIVERABLES:** By 2002, develop a standard test method for measurement of residual stress in MEMS devices.

**DELIVERABLES:** By 2003, develop a standard test method for measurement of elastic modulus in MEMS devices.

### IC Interconnect Characterization

Micro-machining techniques, test structures, and test methods are being developed to characterize the stress, elastic modulus, and adhesion properties in IC interconnects. These test structures are fabricated in the standard IC process on fully fabricated ICs. Fixed-fixed beam and cantilever test structures with interconnect layers are micromachined in the fully processed IC. Measurements of deflection of buckled beams give information on the stress in each interconnect layer. Measurements of mechanical resonance give information on the elastic modulus of the films. These test structures can also be integrated with micro heating elements for accelerated testing.

**DELIVERABLES:** By 2002, compare measurements of elastic modulus made by mechanical resonance measurements to traditional stress-strain measurements.

### Micro-Metrology Tools

In FY 2002, the MEMS Project begins a new research program entitled "Single Molecule Manipulation and Measurement" that is funded by the NIST Director's Competence Building Program. This work is in collaboration with the Biotechnology Division, the Analytical Chemistry Division, the Optical Technology Division, the Magnetic Technology Division, CARB, and JILA. The goal of this effort is to develop a nanofabricated fluidic-based system that can electronically control the movement of single molecules of DNA and RNA and incorporate "workstations" that support electronic and optical measurements of the structure of these molecules.

**DELIVERABLES:** By 2002, develop a micrometer-scale pore that facilitates the formation of a biological-based nanopore structure and demonstrate measurements for electrical characterization of single-stranded DNA.

**DELIVERABLES:** By 2003, develop a nanofluidic switch that is capable of changing the solution in the channel at a rate of 10 miliseconds or faster.

**DELIVERABLES:** By 2004, develop a nanometer-scale solid state pore that mimics the functionality of the biological-based nanopore structure.

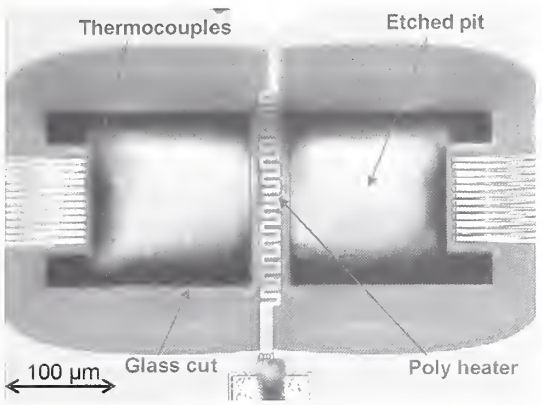
**DELIVERABLES:** By 2005, develop a platform that integrates nanometer-scale fluidic restrictions, fluidic networks, switches, and workstations that support the electronic and optical control and measurement of single molecules of DNA and RNA.

## Accomplishments

■ *Cantilever test structures and an analysis to extract the elastic modulus from the measurement of their mechanical resonance were developed.* These test structures are from IC thin films in fully fabricated Complementary Metal-Oxide Semiconductor (CMOS) ICs. A test chip containing the new cantilever test structure designs was fabricated on a commercial CMOS foundry through the MOSIS service. The test structures are silicon micro-machined as a post process in order to mechanically release them. These test structures compliment the doubly clamped beam test structures that have been developed and used to measure the strain in CMOS films. The combination of data from strain measurements and elastic modulus measurements will enable the measurement of thin-film stress.

■ *A NIST Internal Report (NISTIR) was published entitled "MEMS Length and Strain Measurements Using an Optical Interferometer" that addresses dimensional measurements of MEMS test structures.* The first round-robin experiment was completed for the ASTM Task Group formed on MEMS. The experiment explored the precision and bias associated with the residual stress test structures in a round-robin experiment for residual stress. Results of the round robin, which had 11 other organizations involved, showed that methods for accurate dimensional measurements were critically needed. These results led to the effort to publish the NISTIR and

to the initiation of work to develop two standard test methods for dimensional measurements.




**Optical micrograph of a micromachined CMOS convective accelerometer. This device works on a principle that is completely different from the traditional "proof mass" MEMS accelerometers; it works on the principal that hot air rises. This invention was awarded a U.S. patent, number 6,171,880.**

■ *NIST was awarded a patent on the invention of a new type of accelerometer. The convective accelerometer, as it is named in the patent, operates on the principle that hot air rises.* This device differs from the traditional MEMS-based accelerometers in that its operation is not based on a solid proof mass. The device consists of microheating elements and thermocouple sensors separated by a gap and placed in differential configurations. Thermocouple sensors measure the temperature difference between the two sides of the microheater caused by the effect of acceleration on free convection in the surrounding gas. The devices show a small error in linearity of <0.5 % under tilt conditions from -90 ° to 90 °, and <1.6 % under acceleration from 0 g to 8 g. The sensitivity of the devices is a linear function of heater power (temperature). A sensitivity of 20 µV/g to 30 µV/g was measured for operating power between 35 mW and 45 mW. This invention is a spin-off of research on Micromachined Passive Microwave Components in CMOS Technology that was sponsored by the U.S. Navy.

## FY Outputs

### Collaborations

■ ASTM Task Group E08.05.03, metrology for thin-film electromechanical properties for MEMS and IC technologies (Janet C. Marshall and Michael Gaitan)

■ ASTM Task Group E08.05.03, structural films for MEMS and electronic applications (Janet C. Marshall)

■ CSTL Analytical Chemistry Division, microfluidic integration (Michael Gaitan)

■ CSTL Biotechnology Division, fabrication methods for synthetic nanopores (Michael Gaitan)

■ MOSIS, USC, Marina del Rey, CA, standard manufacturing practices for MEMS (Michael Gaitan)

■ Optical ETC, Inc., Huntsville, Alabama, thermal flat panel displays (Michael Gaitan)

■ PL Optical Technology Division, single molecule probes (Michael Gaitan)

■ University of Maryland, measuring and modeling bonding temperature rise (George G. Harman and Michael Gaitan)

### Standards Committee Participation

■ ASTM Task Group E08.05.03, wrote NISTIR 6779 entitled "MEMS Length and Strain Measurements Using an Optical Interferometer." The purpose of the NISTIR is to provide the technical basis for three new MEMS ASTM standard test methods (Janet C. Marshall)

■ ASTM Task Group E08.05.03, wrote a first draft of an ASTM test method currently entitled "Standard Test Method for Residual Strain Measurements of Thin, Reflecting Films Using an Optical Interferometer" (Janet C. Marshall)

■ ASTM Task Group E08.05.03, wrote a first draft of an ASTM test method currently entitled "Standard Test Method for Strain Gradient Measurements of Thin, Reflecting Films Using an Optical Interferometer" (Janet C. Marshall)

■ International MEMS Standardization Forum, member (Michael Gaitan)

### External Recognition

■ The "Scout Report for Science and Engineering Award," which selects the "Best of the Web," chose the MEMS Test Structure Web Pages on Oct. 25, 2000 (Janet C. Marshall)

## Recent Publications

Barker, S., Ross, D., Tarlov, M., Gaitan, M., and Locascio, L., Control of Flow Direction in Microfluidic Devices with Polyelectrolyte Multilayers, Anal. Chem. 72 (24), 5925-5929, 2000.

***"Janet Marshall and others in the MEMS program at NIST are an integral part of the core group of the ASTM standardization effort. Through their involvement, NIST plays a crucial role in the development of standards and shapes the future of the MEMS industry in the United States."***

*Chris Muhlstein, ASTM Committee*

Gaitan, M., MEMS Standardization, Proceedings of the 6th International Micromachine Symposium, Tokyo, Japan, Nov. 9-10, 2000, 7 p.

Herman, D., Gaitan, M., and DeVoe, D., MEMS Test Structures for Mechanical Characterization of VLSI Thin Films, Proc. SEM Conference, Portland, Oregon, Jun. 4-6, 2001, 5 p.

Johnson, T. J., Ross, D., Gaitan, M., and Locascio, L. E., Laser Modification of Preformed Polymer Microchannels: Application to Reduce Band Broadening around Turns Subject to Electrokinetic Flow, Anal. Chem. 73 (15), 3656 - 3661, 2001.

Marshall, J. C., MEMS Length and Strain Measurements Using an Optical Interferometer, NISTIR 6779, 81 p., 2001.

Marshall, J. C., New Optomechanical Technique for Measuring Layer Thickness in MEMS Processes, Journal of Microelectromechanical Systems, vol. 10, no. 1, March 2001, pp. 153-157.

Rasmussen, A., Gaitan, M., Locascio, L., and Zaghloul, M., Fabrication Techniques to Realize CMOS-compatible Microfluidic Microchannels, JMEMS, 10: (2) 286-297, June 2001.

Ross, D., Gaitan, M., and Locascio, L. E., Temperature Measurement in Microfluidic Systems Using a Temperature-Dependent Fluorescent Dye, Anal. Chem. 73 (11) 2509-2515, 2001.

# Linewidth and Overlay Standards for Nanometer Metrology

## Goals

Develop test-structure-based electrical metrology methods and related reference materials with primary emphasis on linewidth metrology and calibration and overlay; contribute to standards organizations supporting the development of metrology standards for the semiconductor tool industry.

**Christine Murabito using a hot plate to do a post-exposure bake during the photo-lithography process.**

## Customer Needs

The Semiconductor Industry Association's (SIA's) International Technology Roadmap for Semiconductors (ITRS) states that it is critically important to have suitable reference materials for lithography support available when on-wafer measurements are made as a new technology generation in integrated circuit (IC) manufacturing is introduced, and particularly during development of advanced materials and process tools. Each generation of ICs is characterized by the transistor gate length whose control to specifications during IC fabrication is a primary determinant of manufacturing success. The SIA projects the decrease of gate linewidths used in state-of-the-art IC manufacturing from present levels of up to 250 nm to below 70 nm within several years. Scanning electron microscopes (SEMs) and other systems used for traditional linewidth metrology exhibit measurement uncertainties exceeding ITRS-specified tolerances for these applications. It is widely believed that these uncertainties can be at least partially managed through the use of reference materials with linewidths traceable to nanometer-level uncertainties. Until now, such reference materials have been unavailable because the technology needed for their fabrication and certification has not been available. It is also widely believed that the usefulness of SEM metrology for monitoring wafers in advanced development and production will become inadequate at some future IC generation. Thus, there exists a need for new methodology to meet future metrology requirements.

## Technical Strategy

The technical strategy that the project staff have developed for fabricating linewidth and overlay reference materials is known as the Single-Crystal CD (critical dimension) Reference-Material implementation. Patterning with lattice-plane selective etches of the kind used in silicon micro-machining provides reference features with atomically planar sidewalls. Essential elements of the technology are the starting silicon wafers having a (110) orientation; the reference features, which must be aligned to specific lattice vectors; and the lithographic patterning with lattice-plane selective etches of the kind used in silicon micro-machining.

The traceability path for dimensional certification is provided by High-Resolution Transmission Electron Microscopy (HRTEM) imaging. This method provides nanometer-level accuracy, but is sample-destructive and prohibitively costly to implement. This project's unique traceability strategy thus features the sub-nanometer repeatability of electrical CD metrology as a secondary reference means. Low-cost, whole-wafer electrical measurements are effectively calibrated with a few local HRTEM lattice-plane image counts. Typical reference features are several-hundred lattice planes wide. HRTEM lattice-plane image counts, achieved by automated analysis of phase-contrast images, were developed in order to minimize the uncertainties of the linewidths of the standards.

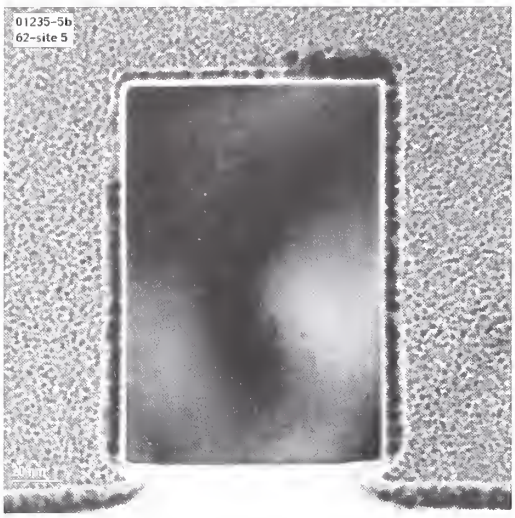
The technical strategy has to be responsive to industry's requirement for reference materials to have the physical properties of standard 200 mm wafers. This project's technical strategy has been to dice each 150 mm wafer and mount the separate chips in micro-machined standard 200 mm wafers to accommodate the test chips. The result is that finished units are user-friendly at an

**Technical Contact:**
Michael W. Cresswell

**Staff-Years (FY 2001):**
3 professionals
1 technician
1 guest researcher
1 student

**Funding Sources:**
NIST (100%)

acceptable cost. The entire fabrication and certification process is planned to be transferred to a commercial standards vendor.




**Low magnification transmission-electron micrograph of the complete cross-section of a feature, having a measured electrical critical dimension of 73 nm.**

In the past year, project researchers have delivered prototype CD reference materials for calibrating linewidth metrology instruments used in manufacturing semiconductor devices to International SEMATECH (ISMT) for evaluation by member companies. The work was the result of collaborations with ISMT, VLSI Technology Inc., and Sandia National Laboratories as well as collaborations with the Information Technology Laboratory's (ITL's) Statistical Engineering Division and Mathematical and Computational Sciences Division, the Manfacturing Engineering Laboratory's (MEL's) Precision Engineering Division, and the Materials Science and Engineering Laboratory's (MSEL's) Metallurgy Division to fabricate, test, and evaluate this new class of reference artifacts to meet the ITRS goals. The technical approach was to design the reference features into electrical test structures, thus enabling the determination of their electrical linewidth. A selection of (36) test structures was incorporated into the test chip that was patterned in the device layer of (110) silicon-on-insulator (SOI) wafers based on well-established silicon micro-machining technology that produced feature sidewalls having near-atomic planarity. Primary calibration of the CD of the test-structures on all the test chips was accomplished by means of high cost, low speed HRTEM imaging and lattice-plane counting at a limited number of sites on the wafer. HRTEM provides nanometer-level accuracy, but is sample-destructive and prohibitively costly to implement on all reference features. The samples delivered to ISMT were calibrated via a statistical correlation with their high-precision electrical CD (ECD) measurement.

**DELIVERABLES:** By 2002, design improved Single-Crystal Silicon-on-Insulator and bulk Reference Materials, procure photomasks, and deliver to ISMT contractors for CD reference material fabrication.

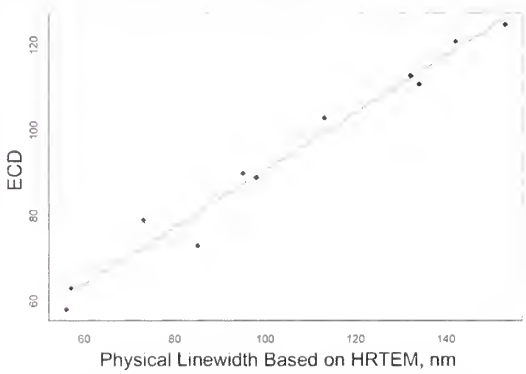
**DELIVERABLES:** By 2002, complete electrical measurements on Single-Crystal Silicon-on-Insulator and bulk Reference Materials, obtain HRTEM measurements, and produce transfer calibration data.

**DELIVERABLES:** By 2002, deliver up to 15 improved Single-Crystal Silicon-on-Insulator and/or bulk Reference Materials to ISMT mounted in carriers supplied by ISMT contractor.

## Accomplishments

■ *For the first time, CD-reference features have been designed, built, and tested on bulk (110) wafers using junction isolation to isolate the test feature from the bulk wafer.* Samples with measured linewidths below 180 nm were evaluated with no adverse leakages from feature to bulk observed. Junction isolated reference materials offer lower initial material costs, simplicity in processing, and possible lower calibration uncertainties.

■ *Based on a NIST patent entitled "Test Chip Reference-Artifact Carrier," a commercial standards supplier has completed work on the development of pocket wafers and has transferred the carrier wafers process to its manufacturing group for product development.*




**Data relating electrical critical dimension (ECD) to physical linewidth with calibration function.**

■ *SED researchers have delivered prototype CD reference materials, RM-8110, for calibrating linewidth metrology instruments used in*

*manufacturing semiconductor devices to ISMT for evaluation by member companies.* Finished CD reference materials were mounted in 200 mm pocket wafers. These materials respond to a need identified by the SIA's ITRS that states that it is critically important to have suitable reference materials to support the development of advanced lithography tools and processes.

- *The IC Technology Group, in collaboration with the National Research Center of Finland (VTT) and the George Washington University, has demonstrated the feasibility of a novel non-contact capacitive-sensor metrology tool developed for chrome photomasks.* The sensor is intended for use as an independent metrology tool for mask makers and mask users. The linewidth metrology sensor, developed using a Low Temperature Co-Fired Ceramic (LTCC) technology, is based on non-contact micro-capacitance measurements of features located on chrome-on-glass reticles. Initial results indicate that the non-contact capacitive sensor is capable of extracting chrome-feature linewidths in the range of 0.4 µm to 0.5 µm.

- *In collaboration with the Precision Engineering Division (PED), the Semiconductor Electronics Division is developing stage micrometers, with the goal of providing them to industry as NIST SRMs.* Stage micrometers are used extensively for calibration of optical microscopes; however, unless they have been individually calibrated by NIST, currently a slow and expensive process, they do not provide a traceable calibration. By combining fast and inexpensive electrical test structure metrology with NIST-traceable measurements on PED's Line-scale Interferometer, NIST will be able to make calibrated stage micrometers widely available at a reasonable cost. The initial designs are completed and test samples are expected early in FY 2002.

- *In collaboration with ITL's Mathematical and Computational Sciences Division, an initial machine-counting procedure for improving the determination of the number of lattice planes as determined from HRTEM images was developed.* The overall emphasis is to reduce the analysis time and to improve the overall linewidth uncertainty.

- *A decontamination process using oxygen plasma was developed for cleaning CD reference materials mounted in 200 mm carrier wafers.* The procedure successfully removed the contamination bulges caused by hydrocarbon contamination when the material is inspected by a SEM. A 35-minute oxygen plasma etch removed the bulges, removed the rectangular cloud, and decreased the size of the circular defects on a test structure reference segment and surrounding area. This hydrocarbon contamination cleaning process was applied on a reference segment with a specified exact width on a chip supplied to an ISMT company that had been contaminated by a SEM.

## FY Outputs

### Collaborations

- ISMT and ISMT member companies (AMD, Compaq, Conexant, Hewlett-Packard, IBM, Intel, Lucent Technologies, Motorola, Texas Instruments, Hyundai, Infineon Technologies, Philips, STMicroelectronics, TSMC), Apr. 30, 2001, delivery of prototype CD reference materials, to meet ISMT MDL (Michael W. Cresswell and Richard A. Allen)

- ISMT, development of single-crystal CD reference materials (Michael W. Cresswell and Richard A. Allen)

- Photronics, development of optical/electrical hybrid critical dimension measurement for photomasks (Richard A. Allen and Michael W. Cresswell)

- Polymers, Sharon Kennedy, consultation to discuss design tools available for a simple geometry project (Colleen H. Ellenwood)

- Precision Engineering Division, Bill Penzes, collaboration on test structure NIST40 design (Colleen H. Ellenwood and Michael W. Cresswell)

- Precision Engineering Division, Bill Penzes, development of electrically calibratable stage micrometer (Richard A. Allen)

- Process Measurements Division, Michael Carrier, consultation regarding how L-Edit works and some advanced ideas to gain efficiency (Colleen H. Ellenwood)

- Process Measurements Division, Michael Carrier, made plots and reviewed new chip (Colleen H. Ellenwood)

- Process Measurements Division, Michael Carrier, reviewed chip designed by M. Carrier (Colleen H. Ellenwood)

- Sandia National Laboratories Microelectronics Development Laboratory, Sandia National Laboratories Compound Semiconductor Research

Laboratory, Sandia National Laboratories Integrated Materials Research Laboratory, NIST ITL, MSEL, MEL, and ISMT, fabrication and certification of reference materials for linewidth and overlay metrology (Michael W. Cresswell, Loren W. Linholm, and Richard A. Allen)

- Sandia National Labs; NIST's Statistical Engineering Division, Metallurgy Division, and Precision Engineering Division; and the University of Central Florida, ISMT reference artifacts for CD measurements (Michael W. Cresswell, Loren W. Linholm, and Richard A. Allen)

- Scientific Computing Division, Hai Tang, assistance with ANSYS model of single crystal CD reference material project (Colleen H. Ellenwood)

- Simplex Solutions, Inc., LSI Logic, and Chartered Semiconductor, procedures and algorithms for CD extraction from test features having conformal coatings (Michael W. Cresswell)

- University of Edinburgh, U.K., and ISMT, process development for single-crystal CD reference materials (Michael W. Cresswell, Loren W. Linholm, and Richard A. Allen)

- VLSI Standards, Inc., development of single-crystal CD and overlay reference materials (Michael W. Cresswell and Richard A. Allen)

- VLSI Standards, Inc. and ISMT, development of commercial architecture and distribution plan for single-crystal CD reference materials (Michael W. Cresswell and Richard A. Allen)

### Standards Committee Participation

- SEMI International Standards Electrical Metrology Test Structures Task Force, Co-Chair (SEMI Doc 2860 balloted, winter 2000) (Richard A. Allen)

- SEMI International Standards Microlithography Committee, member (Richard A. Allen)

### External Recognition

- Certificate of Appreciation for SEMI standards leadership activities (Richard A. Allen)

- Elected IEEE Fellow (Michael W. Cresswell)

## Recent Publications


Allen, R. A., Headley, T. J., Everist, S. C., Ghoshtagore, R. N., Cresswell, M. W., and Linholm, L. W., High-Resolution Transmission Electron Microscopy Calibration of Critical Dimension Reference Materials, IEEE Transaction on Semiconductor Manufacturing, vol. 14, no. 1, pp. 26-31, 2001.

Cresswell, M. W., and Allen, R. A., Electrical CD Metrology and Related Reference Materials, in Handbook of Silicon Semiconductors Metrology, A. C. Diebold, Ed. (Marcel Dekker, Inc., New York - Basel, 2001), pp. 377-409.

Cresswell, M. W., Arora, N., Allen, R. A., Murabito, C. E., Richter, C. A., Gupta, A., Linholm, L. W., Pachura, D., and Bendix, P., Test Chip for Electrical Linewidth of Copper-Interconnection Features and Related Parameters, Proceedings of the 2001 IEEE International Conference on Microelectronic Test Structures, Kobe, Japan, Mar. 19-22, 2001, vol. 14, pp. 183-188.

Guillaume, N., Kiihamaki, J., Karttunen, J., and Kattelus, H., Use of Electrical Test Structures to Characterize Trench Profiles Etched on SOI Wafers, Proc. IEEE 2001 Int. Conference on Microelectronic Test Structures, vol. 14., March 2001, pp. 159-164.

Penzes, W. B., Allen, R. A., Cresswell, M. W., Linholm, L. W., and Teague, E. C., A New Method to Measure the Distance Between Graduation Lines on Graduate Scales, IEEE Transactions on Instrumentation and Measurement, vol. 49, no. 6, December 2000, pp. 1285-1288.

# Major Facilities / Laboratories

## Microfabrication Process Facility

*See next page for facility description*

Contacts: Russell Hajdaj, 301-975-2699
Eric S. Johnson, 301-975-2096

## Materials Characterization Labs

High-Resolution Optical:

Spectroscopic Ellipsometry, High-Resolution Fourier Transform Infrared Spectroscopy, Photoluminescence, Raman Scattering, Photoreflectance, and other Modulation Spectroscopies

Electrical:

Resistivity, Spreading Resistance, Lifetime, Hall Effect, Deep-Level Transient Spectroscopy, Deep-Level Optical Spectroscopy, Charge-Pumping Measurements, Capacitance-Voltage (high frequency & quasi-static), Surface Photovoltage, AC Impedance Analysis, Scanning Capacitance/Atomic Force Microscopy

X-Ray:

Double-Crystal Rocking Curve, Laue Orientation Facility

## Device and Test Structure Characterization Labs

Electrical and Thermal Package Evaluation
Power Device Model Extraction and Validation
Packaging, Assembly, and Bonding Evaluation
Package Interconnect
Scanning-Electron Microscope
Scanning-Probe Microscope
Automatic Wafer-Level Measurement
Gate Dielectric Integrity
MEMS Electrical, Mechanical, Optical, and Microwave

## Computer-Aided Design Labs

Test Structure Layout and Design
Integrated Circuit Layout, Design, and Simulation
Finite Element Thermal Analysis Tools and Computational Fluid Simulations
System, Device, Process, Interconnect, and Virtual Fabrications Simulations

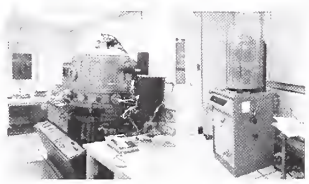
# Microfabrication Process Facility

## Description

As integrated circuit (IC) sizes increase to more than 1 $cm^2$ and feature sizes within the circuits decrease to less than 1 µm, critical demands are placed on the measurement capability required to control and monitor IC fabrication successfully. To meet the demand, NIST researchers are developing state-of-the-art measurement procedures for microelectronics manufacturing.

The Microfabrication Process Facility provides a quality physical environment for a variety of research projects in semiconductor microelectronics as well as in other areas of physics, chemistry, and materials research. The laboratory facilities are used for projects addressing many areas of semiconductor materials and processes, including process control and metrology, materials characterization, and the use of IC materials and processes for novel applications.

The laboratory complex occupies about 2871 square meters, approximately half of which is composed of Class 1000 cleanroom space. Within the cleanroom, work areas are maintained at Class 100 or better. The facility is designed so the work areas can be modified easily to accommodate the frequent equipment and other changes required by research.



**Metallization: sputter and evaporation.**

## Objective

Current objectives are to develop and fabricate structures and devices to fulfill the needs of metrology projects within SED and NIST. These structures include MEMS-based devices, microelectronic devices, and other specialized devices.

## Capabilities

The facility has a complete capability for IC fabrication. Principal processing and analytical equipment is listed below.

### Diffusion, Oxidation, and Annealing

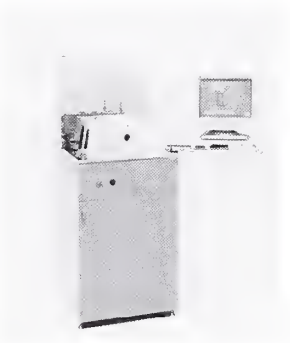
Six furnace tubes for up to 75 mm diameter wafers and five tubes for up to 100 mm diameter wafers.

### Mask Alignment

The newest addition to the Microfabrication Process Facility is a Karl Suss Mask Aligner model MA/BA6. This new tool is capable of submicron resolution (< 0.75 µm) and also has the ability to expose the backside of a substrate, which can be aligned to the front side features. The tool also is designed to be upgraded to a wafer-to-wafer bond aligner.

### Plasma Etching and Deposition

The NIST Microfabrication Process Facility is currently procuring a plasma etching and deposition system. The system we are pursuing is a Unaxis 790. The system will be capable of etching Si, $SiO_2$, Silicon Nitride, and polyamides. Low temperature (< 300 °C) film depositions of $SiO_2$ and silicon nitride can also be accomplished using Plasma Enhanced Chemical Vapor Deposition.



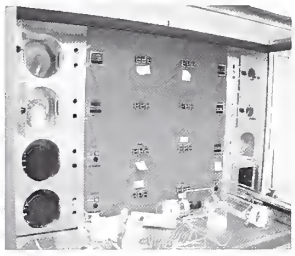
**Unaxis 790 plasma etching and deposition system. [Property of Unaxis Semiconductors, reprinted with permission]**

### Photolithography

Research mask aligner (proximity and contact) for wafers up to 100 mm in diameter and irregularly shaped samples and 10 × direct-step-on wafer system for 75 mm diameter wafers. Photoresist spin coating and developing and related chemical processing, including oxygen plasma stripping. E-beam writing and scanning electron microscope examination for nano-features on 75 mm diameter wafers.

### Film Deposition

Low-pressure chemical vapor deposition systems for depositing silicon nitride, polysilicon, and low-temperature silicon dioxide. Radio frequency and dc vacuum sputtering of metals and dielectrics.



**Film deposition and diffusion furnaces.**

### Etching

Wet and dry etching processes. Plasma barrel etching of nitride films and wet chemical etching of silicon for micromachining. Xenon Difluoride silicon etch process.

**Wet chemical processing.**

### Analytical Measurements

Thin-film reflectometry and other thickness measurements, optical microscopy, and grooving and staining.

### In-Situ Metrology

In-situ, real-time, multiple wavelength ellipsometry to measure optical constants of silicon and other chemical vapor deposition materials such as silicon dioxide, polysilicon, and silicon nitride.

### Post Processing Equipment

DISCO HI-Tech America Inc. 8" wafer dicing saw and SEM cross-section sample prep equipment.

## Applications

Small quantities of specialized semiconductor test specimens, experimental samples, prototype devices, and processed materials can be produced. The processes and processing equipment can be monitored during operation to study the process chemistry and physics. The effects of variations in operating conditions and process gases and chemical purities can be investigated. Research is performed under well-controlled conditions.

A research-oriented facility, the laboratory is not designed to produce large-scale ICs or similar complex structures. Rather, the laboratory emphasizes breadth and flexibility to support a wide variety of projects.

**Automatic 8" wafer dicing saw.**

Currently, research projects address many aspects of microelectronic processing steps and materials as well as silicon micro-machining. Examples include: metal-oxide-semiconductor measurements; metal-semiconductor-specific contact resistivity; uniformity of resistivity, ion-implanted dopant density, surface potential, and interface state density; characterization of deposited insulating films on silicon carbide; ionization and activation of ion-implanted species in semiconductors as a function of annealing temperature; electrical techniques for dopant profiling and leakage current measurements; and processing effects on silicon-on-insulator materials. A simple Complementary Metal-Oxide Semiconductor (CMOS) process has been established. Recent work has also begun in the field of molecular electronics.

## Availability

Facility staff welcome collaborative research projects consistent with the research goals of the NIST semiconductor program. Work is performed in cooperation with the technical staff of the laboratory.

The most productive arrangements begin with the development of a research plan with specific goals. The commitment of knowledgeable re-

searchers to work closely with NIST staff and the provision of equipment and other needed resources are required. Because hazardous materials are present, laboratory staff must supervise all research activities.

## Tasks

- Design and develop optical thermometer (bi-material cantilever w/optical coupling for measurement).
- Fabricate Multi-Junction Thermal Converter (MJTC) in collaboration with Electricity Division.
- Fabricate structures for thermal conduction of silicon dioxide round robin.
- Investigate over-etching phenomena that occurs in Si at the (111) - (001) plane junction with anisotropic etchants.
- Publish MJTC fabrication procedure and process data as a NIST Special Publication.
- Develop and organize equipment and processes for molecular electronics.

## Recent Process Equipment Additions

- SEM with E-Beam Writing Capability
- 8" Wafer Dicing Saw
- Karl Suss Mask Aligner MA6
- Plasma Etching and Plasma-Enhanced Chemical Vapor Deposition

# National Research Council (NRC) Postdoctoral Opportunities

The Semiconductor Electronics Division at the National Institute of Standards and Technology (NIST), in cooperation with the National Research Center (NRC), offers awards for postdoctoral research for American citizens in the fields described below. The Division conducts research in semiconductor materials, processing, devices, and integrated circuits to provide, through both experimental and theoretical work, the necessary basis for understanding measurement-related requirements in semiconductor technology.

NIST affords great freedom and an opportunity for both interdisciplinary research and research in well-defined disciplines. These technical activities of NIST are conducted in its laboratories, which are based in Gaithersburg, a large complex in a Maryland suburb of metropolitan Washington, DC. Applications for NIST Research Associateships are evaluated by the panels only during February. To be eligible for review in February, completed application materials must be postmarked no later than Jan. 15, 2002. This time will also be approximately the same in 2003.

## Molecular Electronics: Electrical Metrology

In Molecular Electronics - a field that many predict will have important technological impacts on the computational and communication systems of the future - molecules perform the functions of electronic components. We are developing methods to reliably and reproducibly measure the electrical properties of small ensembles of molecules in order to investigate molecular conduction mechanisms. Specifically, we are developing test-structures based on nanofabrication and MicroElectroMechanical Systems processing techniques for assessing the electrical properties and reliability of moletronic molecules. In addition to the complexity of the nanofabrication of test structures, the challenges associated with measuring the electrical properties (such as current-voltage and capacitance-voltage as functions of temperature and applied fields) of these small molecular ensembles are daunting. The measured electrical properties will be correlated to systematic characterization studies by a variety of probes and the results used in the validation of predictive models. This task is part of a cross-disciplinary, interlaboratory effort at NIST, with an overall role of developing the measurement science that will enable molecular electronics to blossom into a viable industry.

Contact: Curt A. Richter, 301-975-2082, or John S. Suehle, 301-975-2247

## Scanning Probe Metrology

We are developing scanning probe microscopes to characterize and manipulate the physical and electrical properties of electronic devices, semiconductors, and related materials at the nanometer resolution scale. Projects should be aimed at impacting silicon technology five years in the future or at characterization problems unique to compound semiconductors, molecular electronic devices, or quantum devices. We recently developed scanning capacitance microscopy as a tool for measuring the two-dimensional dopant profile across a silicon p-n junction. We are particularly interested in projects to develop techniques to measure material properties in three dimensions and that have spatial resolution below 1 nm. Our interests extend to other scanning probe techniques, including scanning spreading resistance, scanning Kelvin probe microscopy, surface photovoltage microscopy and other optically pumped scanning probes, and scanning microwave microscopy.

Contact: Joseph J. Kopanski, 301-975-2089, or David G. Seiler, 301-975-2054

## Electrical Overlay- and CD-Metrology Development for Characterization of Advanced Lithography Systems

Projected CD and overlay control-tolerances for new generations of ICs are reducing metrology uncertainty down to the several-nanometer region. However, the development of CD and overlay metrology is not keeping pace with lithographic resolution capabilities of advanced imaging systems. In addition, preferred processing options such as chemical/mechanical polishing tend to render existing overlay metrology less effective for key process steps. The IC Technology Group seeks individuals interested in conducting further research in (1) novel electrical overlay-sensing instruments and techniques, (2) the design and optimization of electrically characterized structures to improve scatterometry

metrology, and (3) contact electrical CD-measurement and extraction methodologies. We also encourage applicants with research experience in noncontact/nonintrusive electrical CD extraction and multimode overlay-sensor development, including overlay and CD-target and test-structure designs.

Contact: Michael W. Cresswell, 301-975-2072

## Novel Test Structures for Characterizing the Performance of Advanced Multilevel Interconnection Systems

As the complexity of advanced integrated circuits continues to increase, new materials (copper, low-κ dielectrics) need to be thoroughly evaluated in order to produce highly reliable, low-resistance on-chip wiring. Extensions of traditional wiring technologies are no longer practical. The IC Technology Group seeks individuals interested in developing electrical test structures, measurement methods, and analysis models needed to evaluate copper-based, multilevel interconnection systems. Of particular importance are methods to measure interconnect and barrier film thickness, dimensional control, by filling, interfacial contact resistance, planarity, defect density/yield, dishing, stress effects, median-time-to-failure, and high-frequency performance. Emphasis is placed on developing thoroughly evaluated structures for use with high-measurement speed, low-frequency electrical test techniques.

Contact: Michael W. Cresswell, 301-975-2072

## Electrical and Optical Characterization of Semiconductors and Devices

Research focuses on understanding the electronic, optical, and magneto-optical behavior of semiconductor materials and devices. Areas of interest include the role of impurities and native defects in bulk crystals, and novel and useful properties induced by quantum confinement in reduced dimensional structures (heterostructures, quantum wells, superlattices, and quantum wires and dots). A broad range of optical techniques is available for reflection, transmission and absorption, and modulation spectroscopy; photoluminescence and photoluminescence excitation; Raman and resonant-Raman scattering; and spectroscopic ellipsometry and surface photovoltage. A wide variety of electrical and magnetotransport techniques are also utilized to characterize the electronic properties. Emphasis is placed on understanding fundamentals and technologically relevant properties as well as developing accurate measurement techniques.

Contact: David G. Seiler, 301-975-2054

## Physics of Semiconductor Devices

Device-modeling and theoretical-device physics research are in progress to interpret measurements of model parameters in microelectronic device simulators. One goal of this work is predictive computer simulation of devices with high carrier and doping concentrations. For example, topics include high-concentration effects, carrier lifetimes, carrier mobilities, and radiation effects that affect the operation and performance of semiconductor devices. The approach in this work involves the careful examination, extension, and experimental verification of the theoretical basis used in device models for silicon, gallium-aluminum-arsenide, and other compound semiconductor devices. Collaborations are in progress to include these improved physical models in device simulations and then to verify, validate, and benchmark these enhancements. We plan to extend the above calculations to include magnetic semiconductors (spintronics), such as manganese-doped gallium arsenide.

Contact: Herbert S. Bennett, 301-975-2079

## Microelectronic Package Characterization

Research focuses on the thermal properties of microelectronic packages and interconnects. Our objectives are to improve methods for characterizing these properties for advanced packages and modules; improve measurement methods and techniques; and verify "compact" electrical and thermal models for packages and modules, and parameter extraction techniques for the models. We have fully equipped thermal characterization laboratories including an infrared thermal imager with μs temporal and 20 μm spatial resolution, and several computer workstations with a compliment of thermal and electrical modeling and analysis software.

Contact: David L. Blackburn, 301-975-2068

## Quantum Devices for ULSI Circuits

The complementary-metal-oxide-semiconductor (CMOS) field-effect-transistor is showing fundamental limits associated with the laws of

quantum mechanics and the limitations of fabrication techniques. This is driving research on innovative solutions to augment or replace CMOS technologies. Quantum devices, such as quantum dots, resonant tunneling devices, and single-electron transistors, deliberately exploit quantum and size effects. We are interested in fundamental research in all aspects of quantum devices, particularly those that are compatible with Si technologies. Our interests include, but are not limited to, fabrication, simulation, and characterization of device structures and constituent materials/processes. Our primary expectation is to be able to identify and address critical metrology issues for this emerging technology of silicon-based quantum devices. In support of this research, we have a cleanroom with a variety of fabrication equipment including furnaces, evaporators, and optical and electron-beam lithography. We have numerous device, electrical, and physical simulation software available including the NanoElectronic Modeling program, NEMO; and the molecular simulation program, CeriusII/CASTEP. We have a wide range of electrical characterization equipment that allows device characterization at temperatures ranging from approximately 1 K to 700 K. This includes ultra-low noise probe stations, cryostats, semiconductor parameter analyzers for current-voltage measurements, ac capacitance-conductance-inductance measurements, specialized setups for Hall and magnetotransport measurements, and a variety of additional electronics. We also have numerous supporting analytical measurement techniques available including spectroscopic ellipsometry, atomic force microscopy, and scanning capacitance microscopy.

Contact: Eric M. Vogel, 301-975-4723, David L. Blackburn, 301-975-2068, or Curt A. Richter, 301-975-2082

## Modeling Advanced Semiconductor Devices for Circuit Simulation

Accurate circuit simulator models for advanced semiconductor devices are required for effective computer-aided design of electronic circuits and systems. However, the semiconductor device models provided in most commercial circuit simulators (e.g., simulation program with integrated circuit emphasis) are based on microelectronic devices, and they do not adequately describe the dynamic behavior of advanced semiconductor devices. Therefore, research focuses on the following: (1) physics-based models - for advanced semiconductor devices such as power and compound semiconductor devices (these models are implemented into available circuit and system simulation programs); (2) parameter extraction algorithms - for obtaining model parameters from terminal electrical measurements; and (3) characterization procedures - for verifying the models' ability to simulate the behavior of the devices within application circuits. NIST also works closely with commercial software vendors to make the new models available to circuit design engineers and has established the NIST/IEEE Working Group on Model Validation to develop comprehensive procedures for evaluating the performance of circuit simulator models. (For more information, see ray.eeel.nist.gov/modval.html.)

Contact: Allen R. Hefner, Jr., 301-975-2071

## MicroElectroMechanical Systems

The MicroElectroMechanical Systems (MEMS) Project focuses on the development of new MEMS-based sensors and actuators for measurement applications. It functions in a multidisciplinary environment with collaborations in the NIST laboratories in chemistry, materials science, physics, biotechnology, and building and fire research. Current activities in the project include thermal-based elements, mechanically resonant structures, microwave elements, and microfluidic systems. The project is also developing MEMS test structures, test methods, and standards to characterize device properties for device performance and reliability testing. These MEMS-based test structures are being utilized to characterize thin-film properties in mainline semiconductor fabrication processes. We are interested in postdoctoral applications not only from individuals who have specialized in MEMS research but also from individuals of other science disciplines who wish to learn microfabrication methods and apply their expertise for new measurement applications.

Contact: Michael Gaitan, 301-975-2070

## Microfluidic Systems

Our work focuses on developing integrated circuit-based microreactors and other active elements and embedding them in plastic-based microfluidic systems. This technology will allow researchers to harness heat for monitoring and controlling chemical reactions in microfluidic systems that provide active control of processes in picoliter volumes. The microreactors are fabricated using a silicon integrated circuit (IC)

process followed by post process bulk and surface micromachining steps. The ICs are embedded in the plastic and/or polymeric-based substrates that contain a network of microchannels. Fabrication methodology is fully compatible with the monolithic integration of digital and analog circuits. We believe that integration is the key issue for advancement of the Microanalytical Laboratory of the future, and it is the basis of the "drop-in functionality" for microfluidic integration. Because of the multidisciplinary nature of this work, we are interested in postdoctoral candidates in engineering, chemistry, materials science, and physics. Research would focus on the development of new fabrication methodologies, design and fabrication of new thermal-fluidic systems, and device modeling and characterization.

Contact: Michael Gaitan, 301-975-2070

## Reliability of Integrated Circuit Dielectric Films

Aggressive scaling of gate oxide thickness used in silicon integrated circuits necessitates the understanding of the physical mechanisms responsible for dielectric degradation and breakdown. We are particularly concerned with the reliability of ultra-thin gate oxides that are in the direct tunneling regime during circuit operation. Research focuses on (1) identifying parameters to determine the physics of time-dependent dielectric breakdown of ultra-thin dielectric films in the tunneling regime; (2) determining the effectiveness of highly accelerated stress tests to predict long-term reliability of thin dielectric films; (3) relating analytical characterization of oxide bulk and interfaces to electrical behavior; (4) identifying and controlling fabrication process parameters that affect intrinsic and extrinsic failure modes; and (5) characterizing and evaluating alternate dielectrics for use as substitutes for silicon oxide in advanced circuit technologies.

Contact: John S. Suehle, 301-975-2247

## Physical and Electrical Properties of Advanced Gate Dielectric Films

It is increasingly difficult to characterize ultra-thin gate dielectric films (typically 0.1 nm to 3.0 nm) used in MOS devices as technology drives them ever thinner. We are developing electrical test methods (using conventional techniques such as I-V and C-V, as well as low-temperature magnetotransport techniques) to measure the physical properties (e.g., film thickness and permittivity) of alternate gate dielectric materials such as high-$\kappa$ metal oxides as well as ultra-thin $SiO_2$. Electrical results are compared with those of optical and other measurement methods, and fundamental physical models are developed to be effective for more than one measurement technique. Because the interface between the dielectric film and the silicon substrate is critical to understanding these measurements, we are developing techniques to characterize buried interfaces (i.e., interface roughness) and are determining how the interface and physical properties affect device performance and reliability.

Contact: Eric M. Vogel, 301-975-4723, or Curt A. Richter, 301-975-2082

## Measurement Traceability for Thin Dielectric Films

The development and fabrication of ultra-thin, increasingly sophisticated gate dielectrics is a key technology for integrated circuits at the 0.10 micrometer feature size and beyond. With the use of single-wavelength and spectroscopic ellipsometry, thin dielectric films are characterized for use in the calibration of instruments to monitor and control gate dielectric fabrication. Research involves the development of physical standards and supporting methodologies that will provide traceability to NIST for advanced gate dielectrics. Input from various physical, optical, and electrical techniques is needed to improve our knowledge of the structure and composition of advanced dielectrics and their interfaces for correct interpretation of ellipsometric measurements. Research will focus on relating the analyses of XTEM, surface second harmonic generation, scanning probe methods, X-ray reflectance, and various electrical techniques to improve our understanding of the structure of thin dielectric films, which would strengthen and extend NIST's capability for providing thin dielectric measurement traceability.

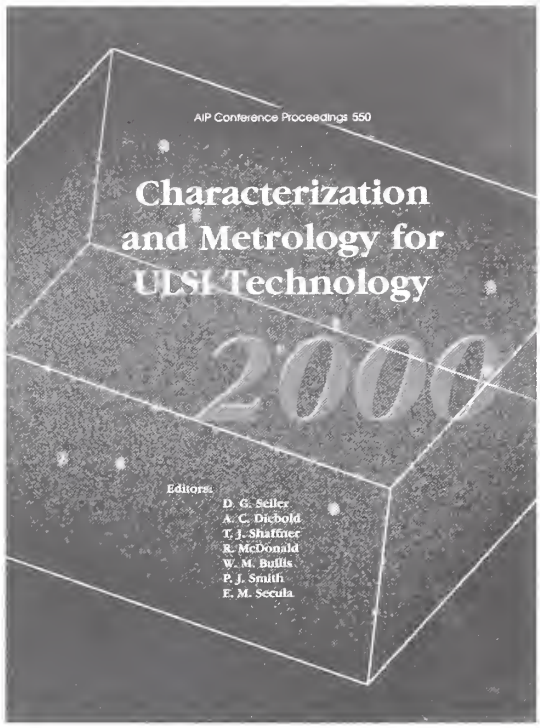
Contact: Curt A. Richter, 301-975-2082, or Nhan V. Nguyen, 301-975-2044

# Book, *Characterization and Metrology for ULSI Technology: 2000* (AIP Conference Proceedings 550), Published in February 2001

*Characterization and Metrology for ULSI Technology: 2000*, containing the proceedings for the June 2000 International Conference on Characterization and Metrology for ULSI Technology, was published in February 2001. The book was compiled by seven editors, led by the Semiconductor Electronics Division's David G. Seiler.

The book addresses the increasingly difficult challenges faced by the worldwide semiconductor community as it moves into the manufacturing of chips with feature sizes less than 100 nm. Some of the challenges are materials-related, such as transistors with high-κ dielectrics and on-chip interconnects made from copper and low-κ dielectrics. The magnitude of these challenges demands special attention from those in the metrology and analytical measurements community. New paradigms must be found for working together. Adequate research and development for new metrology are greatly needed.

Characterization and metrology are key enablers for developing semiconductor process technology and in improving manufacturing. Metrology enables tool improvement, ramping in pilot lines and factory start-ups, and improvement of yield in mature factories. It can reduce the cost of manufacturing and the time-to-market for new products through better characterization of process tools and processes. The metrology community must accelerate cooperative research, development, and prototyping in order to meet ITRS (International Technology Roadmap for Semiconductors) timelines. The book summarizes major issues and gives critical reviews of important measurement techniques that are crucial to continue the advances in semiconductor technology. It covers major aspects of process technology and most characterization techniques for silicon research, including process development, manufacturing, and diagnostics.




***Characterization and Metrology for ULSI Technology: 2000* was published in February 2001 by the American Institute of Physics.**

The editors feel that this book of collected papers provides a concise and effective portrayal of industry characterization needs and some of the problems that must be addressed by industry, academia, and government. Hopefully, it also will provide a basis for stimulating practical perspectives and new metrology ideas for enhancing research and development. The book, published by the American Institute of Physics (AIP) includes about 700 pages of invited and poster papers as well as a key-word searchable CD-ROM. To order, please contact AIP at 1-800-SPRINGER or orders@springer-ny.com.

***"The Semiconductor Electronics Division has initiated and organized a series of excellent meetings, the International Conferences on Characterization and Metrology for Ultralarge-Scale Integration (ULSI) Technology ... Hard-bound proceedings of these conferences have been published by the American Institute of Physics and are regarded as the ultimate reference books on the latest developments in semiconductor metrology and as thorough reviews of state-of-the-art methods."***

*From the NRC Panel Report, An Assessment of the National Institute of Standards and Technology Measurement and Standards Laboratories: Fiscal Year 2000*

# First MEMS Standard Test Structures in the U.S. to be Based on E-Standards

***"The NIST MEMS e-standards Web page has given us a benchmark for MEMS gradient strain and residual strain calculations allowing us to seek anomalies and improvements more efficiently than our previously established methods."***

*Oliver J. Myers, Mechanical Engineer, Electronic Systems and Sensors Sector, Northrop Grumman Corporation*

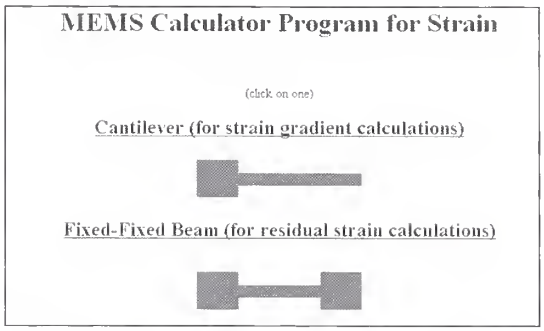
It is anticipated that the first MEMS standard test methods used worldwide will be based on research and measurement analyses currently displayed in the form of e-standards authored by Janet C. Marshall of the Semiconductor Electronics Division (SED). These on-line calculations can be performed on the SED Web site (www.eeel.nist.gov/812/test-structures/), the first implementation of e-standards for this technical community.

The anticipation that the e-standards will evolve into the first MEMS standard test methods is fueled by discussions of the international MEMS/MST/Micromachine Standards Forum attended by Michael Gaitan, Leader of the MEMS Project in the SED. Such international standards are expected to facilitate international commerce in MEMS technologies.

Started as an on-line calculator used to facilitate communication amongst the members of the ASTM E08.05.03 Task Group on Structural Films for MEMS and Electronic Applications, the series of on-line calculations is evolving into a tool of much higher impact on the MEMS industry. The process of achieving this desired impact can be divided into two parts. The first part includes outcomes that have already been achieved. They are (1) draft test procedures for in-plane lengths, residual strain, and strain gradient; (2) the on-line MEMS Calculator Program on aforementioned Web site based on the draft test procedures; (3) a National Institute of Standards and Technology Internal Report (NISTIR 6779), published in August 2001, which presents and derives all the equations used in the analyses; and (4) three draft ASTM Standard Test Methods.

The second part includes outcomes that will be achieved in the foreseeable future. They include a MEMS Instructional Test Chip that will be used in the ASTM Task Group E08.05.03 round robin experiment currently scheduled for the spring of 2002 and a User's Guide for the MEMS Instructional Test Chip.

Therefore, the complete package of MEMS Introductory E-Standard Material will include (1) the design file for the MEMS Instructional Test Chip, (2) the User's Guide for the MEMS Instructional Test Chip, (3) NISTIR 6779, (4) the three ASTM Standard Test Methods, and (5) the on-line MEMS Calculator Program, based on NISTIR 6779.




**Screen capture from the MEMS Calculator Program, the introductory page of the e-standards Web site, located at www.eeel.nist.gov/812/test-structures/.**

Given this wealth of information to be available on the NIST Web site, universities and industry can obtain the design file and submit it for fabrication, and students or employees can learn the standard procedures for measuring in-plane lengths, residual strain, and strain gradient. This will be considered a first step in the learning process when entering the MEMS field.

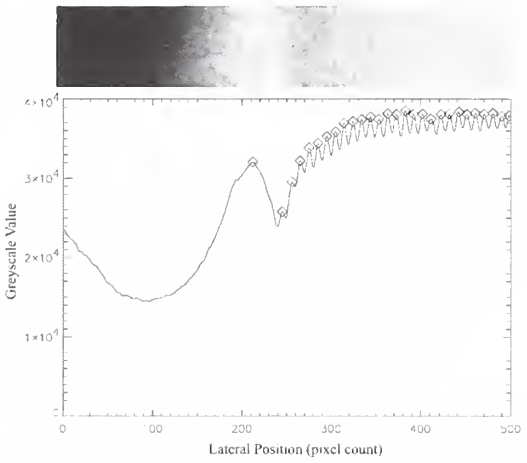
Janet Marshall fields questions from industry and universities almost daily regarding the features and uses of the on-line calculations. She anticipates that providing the e-standards on the easily accessible NIST SED Web site will enable open communication amongst her colleagues in the MEMS industry since everyone will have immediate access to identical standards. In the first MEMS ASTM Round Robin Experiment in the spring of 1999, significant length and strain variations were found when independent laboratories measured the same devices. For example, for a designed 196 µm long fixed-fixed beam, the measured in-plane lengths among the laboratories ranged from 190 µm to 224.6 µm. Also, the reported deflection values (from which the residual strain is calculated) of one fixed-fixed beam ranged from 0.24 µm deflected down to 0.8 µm deflected up. Two laboratories considered this structure as being flat. Similar discrepancies also existed in the measurements done on cantilevers from which the strain gradient is calculated. With the use of these test methods, it is expected that the variations in the community measurements will be significantly tightened.

# Single-Crystal Critical Dimension Reference Materials Delivered by SED Researchers to International SEMATECH

Semiconductor Electronics Division (SED) researchers have delivered prototype single-crystal critical dimension (CD) reference materials for calibrating linewidth metrology instruments used in manufacturing semiconductor devices to International SEMATECH (ISMT) for evaluation by member companies. The work was the result of collaborations with ISMT, VLSI Technology Inc., and Sandia National Laboratories as well as collaborations with ITL's Statistical Engineering Division and Mathematical and Computational Sciences Division, MEL's Precision Engineering Division, and MSEL's Metallurgy Division. The goal is to fabricate, test, and evaluate this new class of reference artifacts to meet the International Technology Roadmap for Semiconductors (ITRS) goals. The Semiconductor Industry Association's (SIA's) ITRS states that it is critically important to have suitable reference materials for lithography support available for the development of advanced materials and process tools as well as on-wafer measurements for integrated circuit (IC) manufacturing. The ITRS projects the decrease of gate linewidths used in state-of-the-art IC manufacturing from present levels of approximately 250 nm to below 70 nm within several years. Until now, such reference materials have been unavailable because of the lack of a technology needed for their fabrication and certification.

**Richard Allen aligning probe card to silicon substrate under test.**

In order to be compatible with users' metrology instruments, test chips containing the reference features were mounted in a "reference-material carrier" wafer also developed by SED staff. This carrier consists of a blank 200 mm silicon wafer with a recessed area etched in the center with dimensions appropriate to accommodate the chip. Fifteen carrier wafers, each containing a chip with a reference feature having a CD in a range from 80 nm to 140 nm, were delivered to ISMT for evaluation by its member companies.




**HRTEM image showing the planes of atoms (top) and a graph showing the automated extraction of the lattice plane count (bottom).**

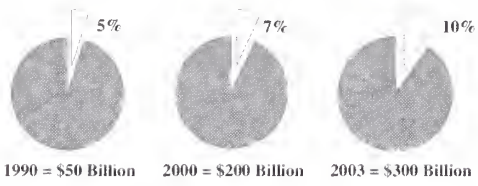
The technical approach was to design the reference features into electrical test structures, thus enabling the determination of their electrical linewidth. A selection of (36) test structures was incorporated into the test chip that was patterned in the device layer of (110) silicon-on-insulator (SOI) wafers based on well-established silicon micro-machining technology that produced feature sidewalls having near-atomic planarity. Primary calibration of the CD of the test-structures on all the test chips was accomplished by means of high cost, low speed High Resolution Transmission Electron Microscopy (HRTEM) imaging and lattice-plane counting at a limited number of sites on the wafer. HRTEM provides nanometer-level accuracy, but is sample-destructive and prohibitively costly to implement on all reference features. The samples delivered to ISMT were calibrated via a statistical correlation with their high-precision electrical CD measurements.

# SED Active in Advocating Support of Compound Semiconductor Roadmap

***A technology "roadmap" is an industrial consensus with inputs from the research community and, if appropriate, inputs from governments. A technology roadmap is often an effective technique to (1) reduce uncertainties in investments, (2) use changes among competing technologies as opportunities, (3) increase the probability for more robust economic performance, (4) guide critical research, (5) assist in setting priorities for resource allocations, and (6) accelerate the rates of both technology development and deployment.***

You should be interested in technology roadmaps for compound semiconductors, SED researcher and NIST Fellow Herbert Bennett stated in his most recent talk, "Why You Should Be Interested in Technology Roadmaps for Compound Semiconductors." While roadmaps for silicon CMOS have been highly successful in the semiconductor industry for two decades, the compound semiconductor industry has generally overlooked the benefits of such roadmaps or compilations of industrial-based consensuses. Bennett declares that you (meaning industry, government, and academia) should be interested in technology roadmaps for compound semiconductors because you (1) will lose less money to competing technologies and (2) will make more money by enabling new technologies (e.g., advanced analog-to-digital converters for very high data rate wireless communications systems, and optical interconnects for scaled CMOS).

**Compound Semiconductors:**
**An Increasingly Larger Slice of a Rapidly Expanding Pie**




*Compound Semiconductor Shipments*
*All Other Semiconductor Shipments*
Dollar amounts are for total semiconductor shipments

**Adapted with permission from the Editor of *Compound Semiconductor* Magazine and Chairwoman of the C-S-Manufacturing Exposition.**

The history of the silicon CMOS roadmaps reveals the potential benefits to be had in the inclusion of compound semiconductor guidelines and goals. For example, the silicon CMOS roadmaps have allowed companies to freely discuss information on technology barriers that they once considered proprietary information. Companies have since discovered that much of their information is actually not proprietary and may be shared with other companies for a globally more competitive industry.

Compound semiconductors enable new technologies and markets such as cell phones and base stations for such phones, CDs and now DVDs, very high data rate communications systems with low bit error rates, and automotive radars. The benefits of compound semiconductors include (1) higher operating frequencies, (2) greater linearity in circuit performance, (3) lower noise in devices, (4) more efficient detection of light, and (5) efficient solid state sources of light such as lasers and light emitting diodes. Benefit (5) is unique to direct bandgap compound semiconductors.

In a move to address this industry void, Dr. Bennett has actively participated in the National Electronics Manufacturing Initiative (NEMI) during the past fiscal year, which has resulted in the writing of several portions of the NEMI Technology Roadmaps for 2000. Through its roadmaps, NEMI charts future opportunities and challenges for the electronics manufacturing industry. These widely utilized roadmaps help OEMs, EMS providers, and suppliers prioritize R&D and technology deployment investments; influence the focus of university-based research; and provide guidance for government investment in emerging technologies. [from www.nemi.org]

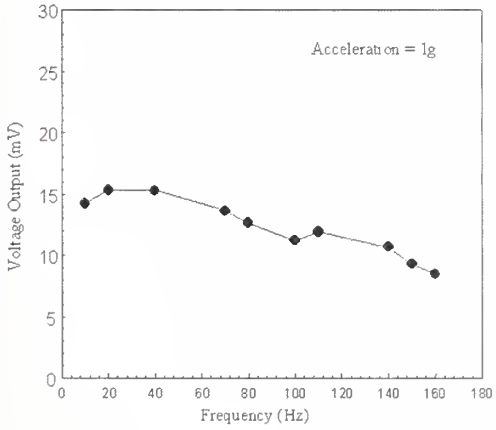
A portion of this material, as well as some additional material on mixed signal processing, modeling and simulation, and optical interconnects will likely appear in the 2002 update of the highly regarded International Technology Roadmap for Semiconductors (ITRS). The goal of this effort, according to Allan Alan, an Intel Corp. official who works with International SEMATECH, is "to develop perspectives for the future of compound semiconductors within integrated circuits and begin tracking their relevance in multi-chip modules." [from *New Technology Week*, King Communications Group, Inc., Washington, D.C., Sept. 17, 2001]

Bennett hopes that these steps toward roadmapping the compound semiconductor industry will help invoke a cultural change in the way companies relate to one another, similar to the change caused by the silicon CMOS roadmaps. The primary goals are to make smarter investments, to increase productivity, to convert technological changes to opportunities, and to use capital and resources more effectively; that is, to make more money and to lose less money.

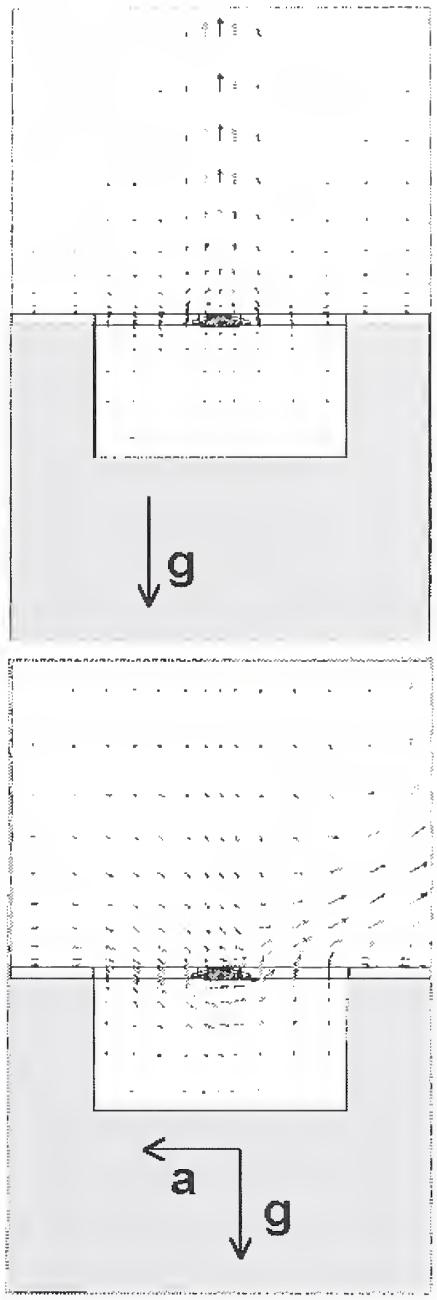
# Patent Issued for Method of Manufacture of Convective Accelerometers Generates Interest in Industry

MEMSIC, a MEMS (micro-electro-mechanical systems) IC (integrated circuit) company in Andover, Massachusetts, which offers advanced technologies that can monolithically integrate micro-electro-mechanical structures with standard CMOS mixed signal circuitry on a single silicon chip, has a keen interest in developing a commercial product based on a patent issued by Michael Gaitan of the Semiconductor Electronics Division's MEMS Project. The patent, entitled "Method of Manufacture of Convective Accelerometers," was issued on Jan. 9, 2001. The invention provides an improved method of making convector accelerometers and tilt sensors using complementary metal-oxide semiconductor (CMOS) technology.

With this patent (number 6,171,880), a method is provided for the manufacture of a convective accelerometer and tilt sensor device using CMOS techniques. An IC chip is produced which includes a silicon substrate having an IC pattern thereon including a heater element located centrally of the substrate and at least first and second thermocouple elements located on the substrate on opposite sides of the heater element. Thereafter, portions of the substrate surrounding and beneath the heater and thermocouple elements are etched away to suspend the element on the substrate and thus to thermally isolate the elements from the substrate. The substrate is etched up to the cold thermocouple junction of the thermocouple elements so the cold junction remains on the substrate.




**Graph of voltage output from thermocouples as a function of frequency.**




**Simulation of airflow for still conditions (top) and acceleration (bottom).**

***"But in the quest for cheaper accelerometers, Dr. Gaitan's lab ... is taking a different approach ... using standard chip-making technology."***

*"What's Next: Motion Sensors to Let Everyday Appliances Do More," The New York Times, April 26, 2001*

# Harman Receives 2001 Total Excellence in Electronics Manufacturing (TEEM) Award

George G. Harman of the Semiconductor Electronics Division was presented the 2001 TEEM Award for Total Excellence in Electronics Manufacturing on Nov. 12, 2001. The award, presented on behalf of the Society of Manufacturing Engineers (SME), was given to Harman at a special ceremony during the SME fall meeting and FABTECH International in Chicago, IL. Harman was honored for "his outstanding 40-year career as a lecturer, author, editor, visiting scientist, and teacher of microelectronics assembly and packaging technology." [SME press release, Aug. 1, 2001]

This prestigious award, now in its tenth year, recognizes one outstanding member of the electronics manufacturing community. As Sam Budhram, 2001 EM/SME chairperson, stated, Harman's nomination was accepted by the Society because of "his spirit, leadership and innovation in connection with his years of service to the electronics manufacturing community, and his enthusiastic stewardship of world-class quality and visionary insight."

**George G. Harman, NIST Fellow, the Semiconductor Electronics Division, NIST**

Harman is an internationally acclaimed expert in the area of wirebonding and packaging of semiconductor chips. He is a NIST Fellow and a former president of the International Microelectronics and Packaging Society (IMAPS). He is considered the world's foremost authority on wire bonding. Harman presents numerous seminars and short courses on wire bonding, packaging reliability, and acoustic emission testing in electronics. His book, *Wire Bonding in Microelectronics*, second edition (McGraw Hill, 1997), is considered to be the "bible" in terms of wirebonding information. He is a Fellow of the IEEE and IMAPS and has received numerous domestic and foreign awards and recognition.

Harman is currently working, with a patent pending, on the development of materials for wire bond interconnections to semiconductor-chip structures.

Past TEEM awardees include Koichi Nishimura, chairman, president, Solectron Corp.; Mauro Walker, retired sr. vice president, Motorola Corp.; Dr. Michael J. Kelly, professor, California State University; Dr. Rao Tummala, director, Georgia Institute of Technology, Dr. Arati Prabhakar, former director, NIST; Dr. Craig Barrett, president, Intel Corp.; Paul Allaire, chairman and CEO, Xerox Corp.; John Young, retired president and CEO, Hewlett-Packard Corp.; and Robert Galvin, former chairman and CEO, Motorola Corp.

# Shaffner Receives EEEL Outstanding Authorship Award

In February 2001, Thomas J. Shaffner of the Semiconductor Electronics Division was presented the EEEL Outstanding Authorship Award for the paper, "Semiconductor Characterization and Analytical Technology," an all-inclusive manuscript that outlines the many analytical characterization tools available for practical applications in the semiconductor industry. The intended audience is the practicing semiconductor wafer-fab engineer, whose primary focus is on manufacturing yield enhancement and process development. This paper was published in the *Proceedings of the IEEE*, vol. 88, Issue no. 9, Sept. 2000, pages 1416-1437.

Thomas J. Shaffner is the Materials Technology Group Leader in the Semiconductor Electronics Division of the Electronics and Electrical Engineering Laboratory. Emphasis of this group is on experimental and theoretical research related to semiconductor materials, structures, and measurement technology essential to growth of the silicon and compound semiconductor industries.

**Thomas J. Shaffner accepting the EEEL Outstanding Authorship Award from EEEL Laboratory Director William Anderson.**

Dr. Shaffner received his Ph.D. degree in physics from Vanderbilt University and a B.S. in physics from North Carolina State University. He has since been active in research involving semiconductor and polymeric materials in industrial, academic, and government laboratories over the past 30 years. Prior to joining NIST in 1998, he managed advanced lithography and materials characterization programs within the Corporate Research Laboratories of Texas Instruments in Dallas. Before this, he worked for six years in surface chemistry and microscopy programs in the Fiber Surface Research Laboratories of E.I. Du Pont de Nemours. During this period, he extended these studies at the University of Manchester (U.K.) during a sabbatical leave as a research associate.

Dr. Shaffner has over 60 publications in solid state science that appear in refereed journals, books, magazines, and symposium proceedings, and over 100 invited presentations in the United States, Canada, Singapore, and Japan. He helped organize five international conferences on materials characterization and device processing through The Electrochemical Society (ECS) and recently co-authored the second edition of *Semiconductor Measurements and Instrumentation*, published by McGraw-Hill. He is a short course instructor for Arizona State University, the Society for Photo-Optical Instrumentation Engineering (SPIE), and the American Physical Society (APS), and he has served on advisory boards for the National Science Foundation, the National Academy of Sciences, ECS, APS, the University of North Texas, and the NIST series of conferences: Characterization and Metrology for ULSI Technology. He also served on the Board on Assessment of NIST Programs for seven years and was an editor of the "Semiconductor Science and Technology" journal. He is active on program committees at ECS, APS, and International SEMATECH, and in addition, he is a member of the Materials Research Society, the American Vacuum Society, SPIE, the American Crystallographic Association, and the American Association for the Advancement of Science.

***"The utility of semiconductor characterization techniques continues to be measured by industry requirements for smaller device geometry, atomically smooth surfaces and interfaces, and increased material purity. Those techniques that specialize in the microspot and structural analysis of microcircuits are reviewed in this paper, with examples of applications to manufacturing and process development. Brief tutorials, case studies, and comparisons show how the strengths and weaknesses of each should be understood before selecting those methods most suitable for the problem at hand."***

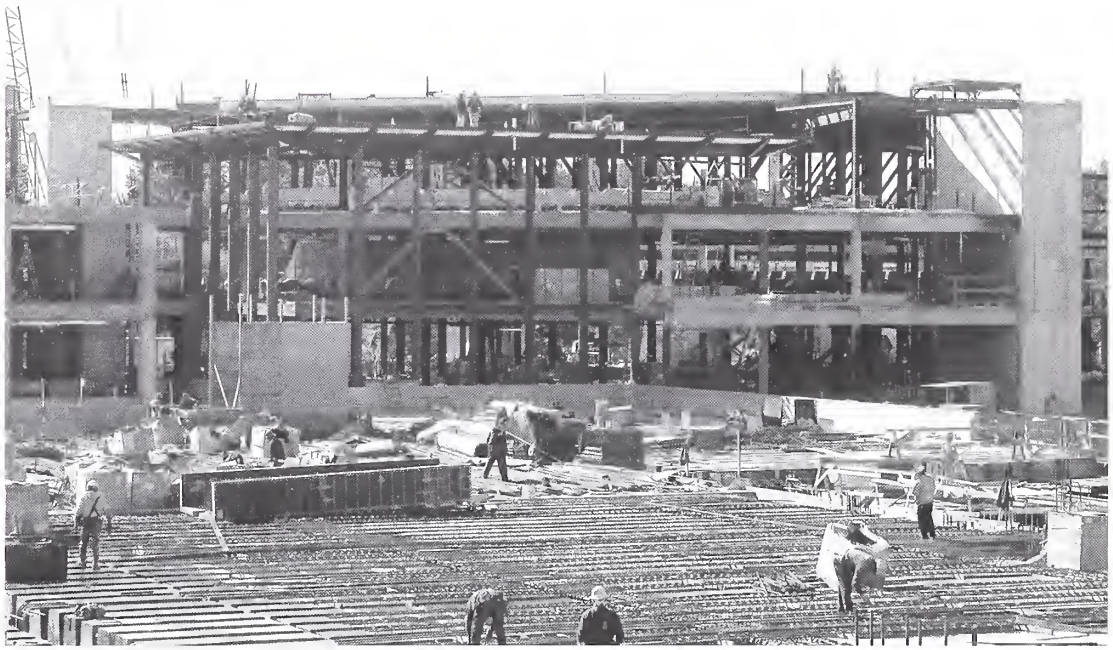
*Abstract, "Semiconductor Characterization and Analytical Technology," by Thomas J. Shaffner, Proceedings of the IEEE, vol. 88, no. 9, September 2000*

# Future NIST Cleanroom Facility on Track for Spring 2003 Completion

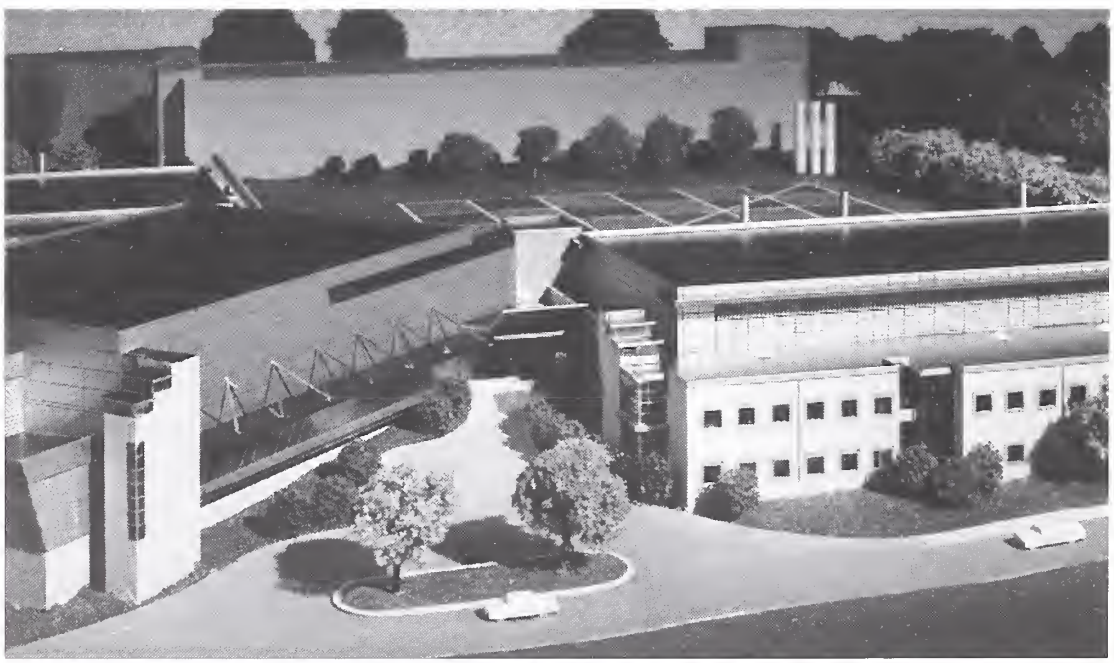
***"The AML is the world-class facility that will provide the United States with global leadership in measurements and standards, and set the foundation for technological advances well into the 21st century ... What will come from within these walls will enhance U.S. industrial competitiveness, foster economic growth and improve the quality of life for all Americans."***

*William Dailey, former Commerce Secretary*

The Advanced Measurement Laboratory (AML) Cleanroom occupies 8,520 square meters of the new AML, which is currently under construction in NIST, Gaithersburg, Maryland. The above-ground Cleanroom has a NC-55 acoustical design and will be a Class 100 facility (3.5 or fewer particles per liter), upgradeable to Class 10. Construction for the facility is on schedule and should be completed in the spring of 2003.



**Construction of the Advanced Measurement Laboratory Cleanroom as seen in late October 2001.**



**AML model showing the main entrance between the Cleanroom (left) and Instrument East Wings (right).**

# NIST's Gaithersburg Campus and Surrounding Area

## About NIST

The National Institute of Standards and Technology (NIST) is an agency of the U.S. Department of Commerce's Technology Administration. NIST was established in 1901 by Congress "to assist industry in the development of technology ... needed to improve product quality, to modernize manufacturing processes, to ensure product reliability ... and to facilitate rapid commercialization ... of products based on new scientific discoveries."

## Location

Located approximately 40 km Northwest of Washington, D.C., on a 234-hectare campus, NIST Gaithersburg offers the advantages of being in close proximity to government offices, while maintaining the seclusion of a rural setting. The site is beautifully landscaped and features mature trees and ponds, as well as a herd of white-tailed deer and gaggles of Canada geese. Walking paths and picnic areas provide easy and pleasant access for outdoor repasts, biking, walking, and jogging. The campus also is easily accessible, with a shuttle service to a nearby metro (subway) station and is in close proximity to three major airports.

**NIST's 11-story Administration Building.**

## Staff

NIST's staff is comprised of about 3,300 scientists, engineers, technicians, business specialists, and administrative personnel. About 1,500 visiting researchers complement the staff. In addition, NIST partners with 2,000 manufacturing specialists and staff at affiliated centers around the country.

## Some Nearby Attractions

### Landmarks

Bureau of Engraving and Printing
Capitol Building
Ford's Theater
Franklin Delano Roosevelt Memorial
I.R.S. Building
J. Edgar Hoover F.B.I. Building
Jefferson Memorial
Library of Congress
Lincoln Memorial
National Archives
Supreme Court
Union Station
Vietnam Veterans Memorial
Washington Monument
White House

**The NIST Gaithersburg campus is home to many different types of wildlife.**

### Museums and Other Attractions

Capital Children's Museum
Corcoran Gallery
Kennedy Center
MCI Center
National Geographic Society
National Sports Gallery
National Theater
Smithsonian Institute
United States Holocaust Memorial Museum
Washington D.C. Convention Center

### Outdoor Attractions

Antietam National Battlefield Site
C&O Canal National Historical Park
Clara Barton National Historic Site
Eisenhower National Historic Site
Fort McHenry
Fort Washington
Gettysburg National Military Park
Glen Echo Park
Great Falls Park
Greenbelt Park
Mount Vernon
Oxon Hill Farm
Prince William Forest Park
Rock Creek Park
Shenandoah National Park
Wolf Trap Farm Park for the Performing Arts

***NIST MISSION -***

***To develop and promote measurement, standards, and technology to enhance productivity, facilitate trade, and improve the quality of life.***

***NIST VISION -***

***To be the global leader in measurement and enabling technology, delivering outstanding value to the nation.***

***"Washington is located in a region that is rich in historic lore and natural beauty. From the bustling sounds of a Chesapeake Bay harbor to the utter stillness of a Blue Ridge mountaintop, from the small, old tobacco farms of southern Maryland to the grand estates of Virginia's hunt country, you will find a richness of scenery and history."***

*"Welcome to Washington" brochure, National Park Service, U.S. Department of the Interior*

January 2002

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