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Silicon Microelectronics Programs at the National Institute of Standards and Technology

Programs, Activities, and Accomplishments

April 2001

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National Institute of Standards and Technology
Technology Administration, U.S. Department of Commerce

Cover Picture Captions:

Picture 1.

Silicon and Oxygen are the most abundant elements on the surface of the earth. When combined chemically, they form quartz – in the fine form, sand.

Picture 2.

Purified single crystal silicon is the underlying material supporting the silicon integrated circuit industry, a major technology driver in today's modern economies (photo of silicon ingot courtesy of MEMC).

Picture 3.

Silicon integrated circuits – active transistor switches and amplifiers, passive components, and many layers of dense interconnecting wiring are formed by complex processing on silicon wafers (photo of silicon integrated circuit wafer courtesy of Austria Mikro System International AG).

Picture 4 and 5.

Metrology is critical to the successful processing of silicon into integrated circuits. Two examples are: Picture 4, the image of a critical dimensional artifact obtained with a calibrated atomic force microscope (CAFM); and Picture 5, an X-ray tomograph of a wiring interconnect. Both projects are progressing at NIST and are among those described in this document.

Office of Microlectronics Programs

Programs, Activities, and Accomplishments

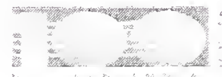
NISTIR 6731

April 2001

U.S. DEPARTMENT OF COMMERCE
Donald L. Evans, Secretary

Technology Administration
Karen H. Brown, Acting Under Secretary for Technology

National Institute of Standards and Technology
Karen H. Brown, Acting Director



Disclaimer: Certain commercial equipment and/or software are identified in this report to adequately describe the experimental procedure. Such identification does not imply recommendation or endorsement by the National Institute of Standards and Technology, nor does it imply that the equipment and/or software identified is necessarily the best available for the purpose.

References: References made the *International Technology Roadmap for Semiconductors* (ITRS) apply to the most recent edition, dated 1999. This document is available from the Semiconductor Industry Association (SIA), 181 Metro Drive, Suite 450, San Jose, CA 95110, phone: (408) 436-6600; fax: (408) 436-6646.

Appendices: The reader will notice that there are acronyms and abbreviations throughout this document that are not spelled out due to space limitations. To enable the reader to learn more about these acronyms and abbreviations, we have included an appendix toward the back including an acronyms/abbreviations list. We have also included a list of the NISMP projects, which demonstrates the synergism resulting through this matrix-managed program.

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I. Welcome and Introduction

Welcome

The microelectronics industry supplies vital components to the electronics industry and to the U.S. economy, enabling rapid improvements in productivity and in new high technology growth industries such as electronic commerce and biotechnology. The National Institute of Standards and Technology, NIST, in fulfilling its mission of strengthening the U.S. economy, works with industry to develop and apply technology, measurements and standards; and applies substantial efforts on behalf of the semiconductor industry and its infrastructure. This report describes the many projects being conducted at NIST that constitute that effort.

Historical Perspective

NIST's predecessor, the National Bureau of Standards (NBS), began work in the mid-1950's to meet the measurement needs of the infant semiconductor industry. While this was initially focused on transistor applications in other government agencies, in the early 1960's the Bureau sought industry guidance from the American Society for Testing and Materials (ASTM) and the (U.S.) Electronic Industries Association (EIA). ASTM's top priority was the accurate measurement of silicon resistivity. NBS scientists developed a practical non-destructive method ten times more precise than previous destructive methods. The method is the basis for five industrial standards and for resistivity standard reference materials widely used to calibrate the industry's measurement instruments. The second project, recommended by a panel of EIA experts, addressed the "second breakdown" failure mechanism of transistors. The results of this project have been widely applied, including solving a problem in main engine control responsible for delaying the launch of a space shuttle.

From these beginnings, by 1980 the semiconductor metrology program had grown to employ a staff of sixty with a $6 million budget, mostly from a variety of other government agencies. Congressional funding in that year gave NBS the internal means to maintain its semiconductor metrology work. Meeting industrial needs remained the most important guide for managing the program.

Industrial Metrology Needs

By the late 1980's, NBS (now NIST) recognized that the semiconductor industry was applying a much wider range of science and engineering technology than the existing NIST program was designed to cover. The necessary expertise existed at NIST, but in other parts of the organization. In 1991, NIST established the Office of Microelectronics Programs (OMP) to coordinate and fund metrological research and development across the agency, and to provide the industry with easy single point access to NIST's widespread projects. Roadmaps developed by the (U.S.) Semiconductor Industry Association (SIA) have independently identified the broad technological coverage and growing industrial needs for NIST's semiconductor metrology developments. As the available funding and the scope of the activities grew, the collective name became the National Semiconductor Metrology Program (NSMP), operated by the OMP.

The NSMP has stimulated a greater interest in semiconductor metrology, motivating most of NIST's laboratories to launch additional projects of their own and to cost-share OMP-funded projects. The projects described in this book represent this broader portfolio of microelectronics projects. Most, but not all, of the projects described are partially funded by the NSMP, which provided a $12 million budget in fiscal year 2001.

Fostering NIST's Relationships with the Industry

NIST's relationships with the SIA, International SEMATECH, and the Semiconductor Research Corporation (SRC) are also coordinated through the OMP. Staff from OMP represent NIST on the SIA committees that develop the International Technology Roadmap for Semiconductors (ITRS) as well as on numerous SRC Technical Advisory Boards. OMP staff are also active in the semiconductor standards development work of the ASTM, the Deutsches Institut für Normung (DIN), the EIA, the International

Organization for Standardization (ISO), and Semiconductor Equipment and Materials International (SEMI).

Learn More about Semiconductor Metrology at NIST

This publication provides summaries of NIST's metrology projects for the silicon semiconductor industry and their suppliers of materials and manufacturing equipment. Each project responds to one or more metrology requirements identified by the industry in sources such as the ITRS. NIST is committed to listening to the needs of industry, working with industry representatives to establish priorities, and responding where resources permit with effective measurement technology and services. For further information, please contact NIST as follows:

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Front Row: Barbara Belzer and Michele Buckley

A. Lithography Metrology Program

Advances in lithography have largely driven the spectacular productivity improvements of the integrated circuit industry, a steady quadrupling of active components per chip every three years over the past several decades. This continual scaling down of transistor dimensions has allowed more and more components on a chip, lowered the power consumption per transistor, and increased the speed of the circuitry. The shrinking of device dimensions has been accomplished by shortening the wavelength of the radiation used by the lithography exposure tools. The industry at this point has moved into the deep ultraviolet (DUV) spectrum. Currently, exposure tools operating at 193 nm are being introduced, and exposure tools operating at 157 nm are in development. Looking beyond the deep ultraviolet, extreme ultraviolet radiation (EUV) at 13 nm is being investigated, and demonstration tools are being designed and assembled. The overall goal of this task is to support these developments in DUV and EUV. The areas of emphasis are lens materials, laser calorimetry, radiation detector sensitivity and damage, EUV lens metrology, and metrology for the development of advanced photoresist materials.

Metrology Supporting Deep Ultraviolet Lithography

Technical Contacts:

*J. **Burnett**, M. Dowell, R. Gupta, T. Scott, T. Lucatorto*

Objective:

Develop solutions to key metrology issues confronting the semiconductor lithography industry. These include development of measurement methods and standards for characterizing deep ultraviolet (DUV) laser sources, detectors, and materials. One focus is on delivering high-accuracy measurements of UV detector parameters and materials properties of immediate need by the industry. There is ongoing activity in the following areas: standards development, calibration services, characterization of optical materials, sources, and detectors, in addition to advising customers on in-house measurements.

Customer Needs:

Increasing information technology requirements have yielded a strong demand for faster logic circuits and higher-density memory chips. This demand has lead to the introduction of DUV laser-based lithographic tools for semiconductor manufacturing. These tools, which employ KrF (248 nm) and ArF (193 nm) excimer lasers, have led to an increased demand for accurate measurements at DUV laser wavelengths. Next generation tools employing F_2 (157 nm) excimer lasers are projected for insertion into production lines in 2003. To support these efforts, the National Institute of Standards and Technology (NIST), with ISMT support, has initiated a DUV metrology program focusing on the characterization of DUV optical materials, sources, and detectors.

Accurate measurement methods and standards for characterizing DUV laser sources, detectors, and optical materials are critical in a number of photolithography applications. Project members work closely with industry to develop standards, new technology, and appropriate measurement techniques for DUV wavelength measurements. These efforts include development work in the following areas: characterization measurements of optical materials, standards development, detector studies, calibration services, and advising customers on in-house measurements. In particular, accurate DUV measurements of optical materials properties, such as the index of refraction, dispersion, temperature dependence, and stress dependence, are critical to the design of DUV photolithography projection systems.

Technical Strategy:

Beginning with the first edition of the National Technology Roadmap for Semiconductors (NTRS) in 1992, the semiconductor industry has made an organized, concentrated effort to reduce the feature sizes of integrated circuits. As a result, there has been a continual shift towards shorter exposure wavelengths in the optical lithography process. Because of their inherent characteristics, deep ultraviolet (DUV) lasers, specifically KrF (248 nm) and ArF (193 nm), and more recently F_2 (157 nm) excimer lasers, are the preferred sources for high-resolution lithography at this time. To meet the laser metrology needs of the optical lithography community, NIST has developed primary standards and associated measurement systems at 193 nm and 248 nm, and is in the process of developing standards for 157 nm measurements.

Milestone: By 2002, develop a 157 nm excimer laser primary standard and calibration service to provide support for the next generation of optical lithography.

In addition to existing DUV laser measurement services, there is increasing demand for laser dose, i.e., energy density measurements, where the

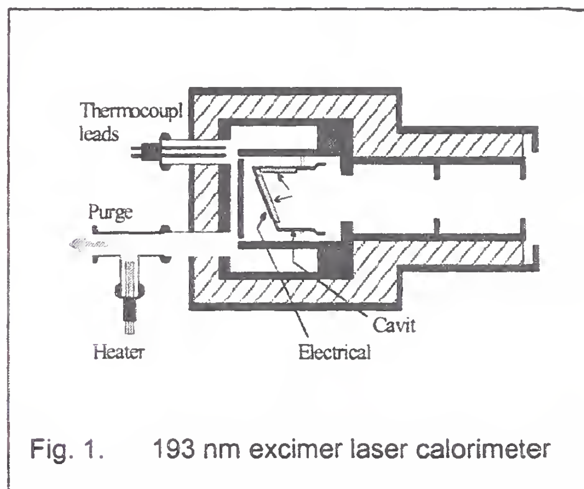


Fig. 1. 193 nm excimer laser calorimeter

detector samples a fraction of the total laser beam. Accurate laser dose measurements are important because small area detectors are widely used to

monitor laser pulse energy density at the wafer plane of a lithographic tool. Accurate measurements of laser dose are especially crucial to the development of new mask resist materials, since lower dose requirements lead to greater wafer throughput and also extend the lifetime of an exposure tool's optical components as well.

Milestone: By 2001, develop the capability at NIST of calibration services for energy density (dose) meters at 248 nm and 193 nm.

High-accuracy measurements of the index properties of UV materials is a requirement for the design of DUV lithography systems. To meet this demand NIST has developed methods to make measurements of the DUV refractive index, as well as its wavelength, temperature, and stress dependencies to the high accuracy needed. Index variations have become a limiting factor in the development of the optics for lithography systems, escpecially at 157 nm. To address this problem we have developed unique VUV polarimetry and Twyman-Green interferometer systems to measure 157 nm index variation in lens materials due both to external stress and grown-in defects.

Milestone: By 2002, have capability of completely characterizing index inhomogeneities of DUV materials near 157 nm at the sub ppm level.

There is an urgent need in the industry for evaluation of stability of VUV detectors to be used for transfer standards or for other applications in various manufacturing processes. Using synchrotron radiation in conjunction with an excimer laser, we measure the stability of these detectors over a wide range in wavelength. We also intend to extend the characterization of photodetectors at 157 nm to include evaluation of the stability of photodiodes as a function of the intensity of the irradiation excimer pulse. This will provide important information regarding non-linear effects in the response towards excimer radiation. We also plan to characterize pyroelectric detectors using synchrotron radiation and measure the stability of such detectors towards excimer radiation.

Milestone: By 2002, complete characterization of semiconductor and pyro-electric detectors in the wavelength range from 120 nm to 400 nm.

Accomplishments:

- **193 nm excimer laser power and energy meter calibration services.** With partial support from ISMT, completed development of a new DUV primary standard calorimeter for measurement of 193 nm excimer laser pulse energy. Established a new service to calibrate customer power and energy meters for 193 nm excimer lasers with an expanded uertainty of ≈ 1 %.

Significance: Standards traceable to SI units for DUV excimer laser pulse energy are important for medical applications such as excimer laser eye surgery, and for the semiconductor industry for accurate process control in computer chip manufacturing.

- **Characterization measurements of excimer laser sources.** We have developed beam homogenization technique that can achieve spatial beam uniformities of 1.5 % or less. In addition, beam characterization measurements have been performed that include: spatial correlation measurements, and measurements of ISO definitions of beam and plateau uniformity.

Significance: Laser beam characterization measurements are critical in photolithography since resolution requirements dictate beam uniformities of 3 % or less.

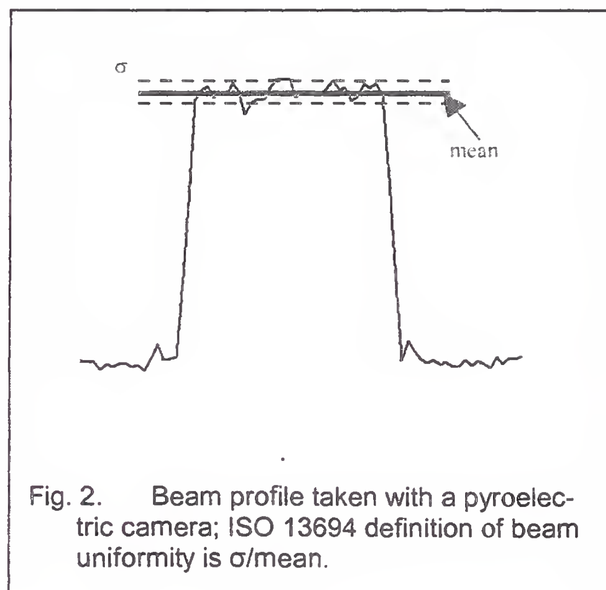


Fig. 2. Beam profile taken with a pyroelectric camera; ISO 13694 definition of beam uniformity is σ/mean.

- **Detector damage testing and characterization at 157 nm.** We have evaluated the stability of

semiconductor diodes under irradiation from an excimer laser operating at 157 nm. A new facility at SURF III has been built that allows simultaneous exposure of photodiodes to excimer radiation and synchrotron radiation. Measurements of the spectral responsivity can be made in the spectral range from 120 nm to 320 nm with a relative standard uncertainty of 0.5 %. The intense, pulsed laser radiation was used to expose the photodiodes for varying amounts of accumulated irradiation whereas the low intensity, continuously-tunable cw radiation from the synchrotron source was used to characterize the photodiodes. The changes in the spectral responsivity of different kinds of diodes such as UV silicon, GaP, GaAsP, PtSi, diamond, and GaN were measured for a large range of total accumulated dose from an F_2 excimer laser operating at 157 nm. Differing amounts of changes were seen in different diodes depending on the total excimer irradiation dose and they showed different spectral changes in the responsivity as well.

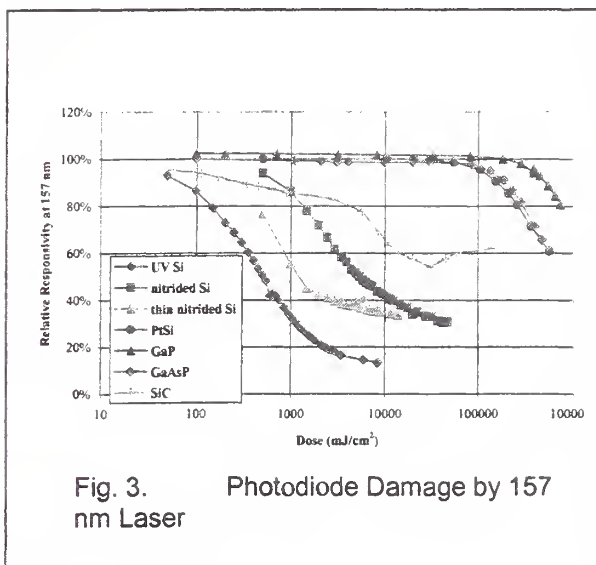


Fig. 3. Photodiode Damage by 157 nm Laser

Significance: Yields important information about the mechanism responsible for the degradation of photodiodes and also for the suitability of use of various kinds of detectors for different industrial applications.

- **Development of VUV transfer standards**. We have also constructed and characterized a probe that is suitable for accurate measurements of irradiance in the vacuum ultraviolet spectral range. The probe consists of a PtSi detector behind a precision 5 mm aperture. The probe was characterized at various wavelengths ranging from 157 nm to 325 nm, encompassing many of the important industrial application wavelengths. The principle of measurement of the irradiance is based on scanning the probe in a light field and measuring the spectral responsivity on a grid with regular spacing. Measurement of the spectral responsivity in the center of the probe along with the integrated total responsivity yields the spectral irradiance. This method can alternatively be used to calculate aperture areas as well by measuring the ratio of the total responsivity and the responsivity in the center.

Significance: Many industrial applications such as UV curing, photolithography, or semiconductor chip fabrication require accurate measurement of the irradiance and would benefit from having such a stable, accurate UV probe.

- **Characterization of optical materials at 157 nm.** We have made the first measurements of the absolute index of refraction, its dispersion, and its temperature dependence near 157 nm for all the principal materials that are currently being considered for use in 157 nm photolithography systems. Using unique UV polarimetry and Twyman-Green interferometer systems we developed, we made the first measurements of the 157 nm stress-optical coefficients and their dispersions of UV materials.

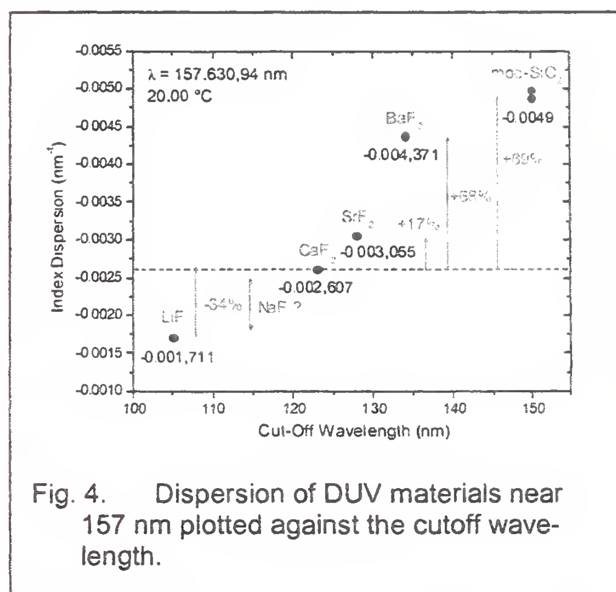


Fig. 4. Dispersion of DUV materials near 157 nm plotted against the cutoff wavelength.

Significance: The index measurements first demonstrated that by combining calcium fluoride and barium fluoride elements, lens systems can be made achromatic over the 157nm excimer laser band width, thus allowing all-refractive system designs. As a result of these measurements, this all-refractive approach is now being pursued as an option by several of the major lithography optics companies. The birefringence measurements are being used by the lithography optics designers to determine the effect of grown-in stress on the index properties of lens materials and to model the effect of externally applied stress, e.g., lens mounts and gravity, on the optical system performance.

- **DUV excimer laser transmittance of optical materials.** Developed a measurement system for the transmittance of optical materials (e.g., fused silica and calcium fluoride) using a 193 nm excimer laser. Measurements are performed in a nitrogen gas environment with an expanded uncertainty of < 1 %, and are available to customers as a special test. (Collaboration with NIST Division 844 and MIT Lincoln Laboratory).

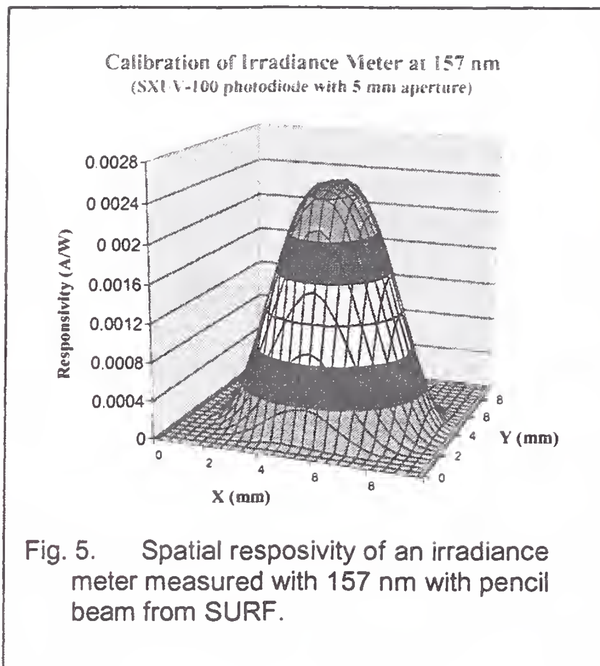


Fig. 5. Spatial resposivity of an irradiance meter measured with 157 nm with pencil beam from SURF.

Significance: Applications for 193 nm excimer lasers require accurate transmittance measurements of system components to assure performance and to meet design tolerances. Industry measurements of transmittance using both excimer lasers and traditional spectrophotometers show considerable disagreements (~ 5 %)

Collaborations:

Corning, Inc. (John Burnett)
International Radiation Detectors (Rajeev Gupta and Marla Dowell)
Molectron Detector (Marla Dowell)
MIT Lincoln Laboratory (John Burnett, Marla Dowell, and Rajeev Gupta)

External Recognition

Invited Talk: "Index Properties of 157 nm Materials", ISMT 157 nm Technical Data Review, San Diego, 15 November 2000. (John Burnett)

Invited Talk: "From Eyeballs to Microchips: Laser Metrology at NIST", Colorado Science Convention, Denver, CO, September 29, 2000. (Marla Dowell)

Invited Talk: "DUV Laser Metrology at NIST", 1999 Optical Properties of Materials NIST-Industry Consortium Workshop, Gaithersburg, MD, December 6, 1999. (Marla Dowell)

Invited Talk: "Detector and Material Characterization Using Synchrotron Radiation", International Symposium on 157 nm Lithography, May 1999, Dana Point, CA. (Rajeev Gupta)

Award: Department of Commerce Silver Medal. (John Burnett and Rajeev Gupta)

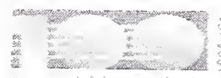
Award: Judson C. French Award. (Marla Dowell, Rod Leonhardt, David Livigni, and Chris Cromer)

Publications

"Pulsed-laser Metrology at NIST" Marla Dowell, Optics and Photonics News (February 2001) 28.

"The Power of Light: Choosing the Right Detector is key to accurate beam power measurements" Marla Dowell, OE Magazine (January 2001) 56.

"New Developments in Deep Ultraviolet Laser Metrology for Photolithography" M. L. Dowell, C. L. Cromer, R. D. Jones, D. A. Keenan, and T. R. Scott, Characterization and Metrology for ULSI Technology: 2000, D. G. Seiler, A. C. Diebold, T. J. Shaffner, R. McDonald, W. M. Bullis, P. J.



Smith, and E. M. Secula, Eds. (AIP, New York, 2001), pp. 391-394.

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Characterization of materials using an ultraviolet radiometric beamline at SURF III, P.-S. Shaw, R. Gupta, T.A. Germer, U. Arp, T. Lucatorto, and K.R. Lykke, Metrologia, **37**, 551 (2000)

"The New DUV Spectral Responsivity Scale Based on Cryogenic Radiometry at SURF III", Ping-Shine Shaw, Thomas C. Larason, Rajeev Gupta, Steven W. Brown, Robert E. Vest, and Keith R. Lykke, submitted to Review of Scientific Instruments.

"Improved Near-Infrared Spectral Responsivity Scale", Ping-Shine Shaw, Thomas C. Larason, Rajeev Gupta, Steven W. Brown, and Keith R. Lykke, to be published in J. Res. Natl. Inst. Stand. Technol.

"Material and Detector Characterization for DUV and VUV Lithography", Rajeev Gupta, Lambda Physik Highlights, **56**, 6 (2000)

"The New UV Radiometry Facility at SURF", P.S. Shaw, K.R. Lykke, R. Gupta, U. Arp, and T.B. Lucatorto, SRI99: Eleventh US National Conference, AIP Conference Proceedings **521**, 81 (1999).

"Detector and Material Characterization for Lithography in the VUV Spectral Range", Rajeev Gupta, John Burnett, and Vladimir Liebermann, Future Fab International, July 2000.

Metrology Supporting Extreme Ultraviolet Lithography

Technical Contacts:
T. Lucatorto, A. Davies

Objective:
Provide leading-edge metrology for the development and characterization of optical components and detectors used in extreme ultraviolet lithography (EUVL).

Customer Needs
As the features and design rules of the components used in semiconductor chips continue to shrink, we approach the limit at which the diffraction of the DUV used for the lithography will prevent further reduction of the dimensions. Thus, within the next few years, the industry will need to identify a suitable "new generation lithography" (NGL) beyond the current DUV-based tools. A leading contender for the NGL is EUVL. In this country its development is being intensely pursued by the EUV-Limited Liability Corporation (EUV-LLC).

High resolution imaging with EUV radiation was not possible until the development of multilayer EUV mirrors in the early 80s. This development has spawned the relatively new field of EUV optics and its associated set of new metrological challenges. Among these are the following: 1) nanometer level optical figure measurement; 2) precise EUV reflectivity maps; 3) EUV dosimetry; and 4) EUV multilayer endurance testing.

Technical Strategy:

1) **Nanometer level optical figure measurement.**

The approach to measurement of optical figure is to use phase measuring interferometry (PMI). Commercially available phase measuring interferometers (PMIs) can be extremely repeatable; an array of techniques, including some developed in this program, are now available for separation of part errors from the signature of the instrument - at least for some classes of surface. Such approaches have shown that they can provide measurement uncertainties of the order of 1 nm for flats and near flats.

For the measurement of aspheric optics (i.e., systematic deviations from a base sphere), such as those needed for EUVL, there are some basic limitations to the potential of the commercially available PMIs. Concepts for a system combining a PMI with high precision slideways have been developed and implemented (in collaboration with an industrial vendor) in a new measurement capability, known as the NIST X-ray Optics Calibration Interferometer (XCALIBIR). The goal is 0.25 nm rms uncertainty in measurement of aspheric optics up to 300 mm diameter with focal lengths up to 2 meters. XCALIBIR designed to have the flexibility to measure flats, spherical, and aspheric optics was installed at NIST in the fourth quarter of FY99; a calibration service will be developed based on this capability.

A critical part of the uncertainty evaluation of an ultra-precision interferometric measurement is a ray-trace evaluation of the test. The uncertainty in the radius of curvature of spherical optics in the test, limits the accuracy of the models. Currently NIST offers no measurement service for radii. XCALIBIR is being used to provide state-of-the-art radius of curvature measurements to address this problem.

Lithography at EUV wavelengths also leads to challenging tolerances for the photomask. The mask is the optical element containing the desired wafer pattern; lithography is accomplished by

Fig. 1. XCALIBIR

projecting the image of the pattern onto the resist-coated wafer with a several-fold reduction in magnification. Current EUVL designs call for a mask blank flatness of 50 nm. Proposed substrate materials are transparent in the visible and nearly opposing parallel forces, which makes surface flatness metrology difficult with traditional phase measuring interferometry. We are developing non-traditional flatness measurements such as the Ritchey-Common test for these substrates. XCALIBIR can also be used in a reduced coherence mode to measure flatness of parallel windows. Lastly, we are developing a coronograph-like variation of PMI for detecting localized defects on these substrates.

2) Precise EUV reflectivity maps.

The present EUV Reflectometry Facility is a multipurpose beamline covering the 3 nm to 40 nm (400 eV to 30 eV) spectral range. Although dedicated to serving the EUV optics community by providing accurate measurements of multilayer mirror reflectivities, this facility has been used for many other types of measurements since its commissioning in early 1993. Among the other measurements performed recently are grating efficiencies, photocathode conversion efficiencies, phosphor conversion efficiencies, film dosimetry, and determination of EUV optical constants though angle-dependent reflectance measurements.

The EUV reflectometry beamline consists of a grazing incidence, varied line space grating monochromator and a recently installed sample chamber able to accept samples up to 40 cm in diameter and 40 kg in mass. The sample chamber is shown in Fig. 2. It has six axes of sample motion and two axes of detector motion. This, coupled with the large size, will allow us to make full reflectivity maps of the surfaces of all the optics currently planned for EUVL stepper systems, as well as mirrors for EUV telescopes.

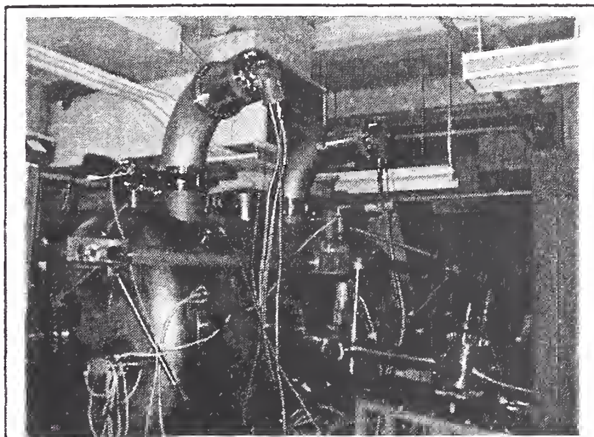


Fig. 2: New sample chamber for reflectometry measurements.

The monochromator consists of collection optics, two varied-line-spaced gratings, and a scanning mirror. SURF III is an ideal source for absolute reflectance measurements. Although not a high-brightness source relative to third-generation storage rings, the small radius allows us to collect a large solid angle, and therefore we still have a dynamic range of five orders of magnitude. Moreover, SURF III is capable of operating at different electron-beam energies from 180 MeV to 400 MeV, allowing us to tune the peak output energy to our particular measurements, thus reducing uncertainties due to multiple-order and scattered light. This allows us to cover wavelengths from 3 nm to 40 nm, virtually the entire range at which normal-incidence multilayers reflect.

Figure 3 shows the reflectance-vs-position of a 20 cm multilayer mirror. This mirror is more than twice the diameter of the largest mirror we had measured six months ago.

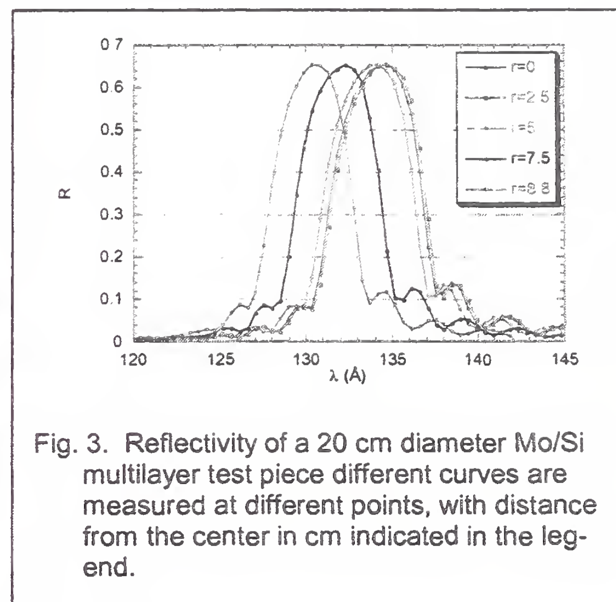


Fig. 3. Reflectivity of a 20 cm diameter Mo/Si multilayer test piece different curves are measured at different points, with distance from the center in cm indicated in the legend.

3) EUV dosimetry.

NIST is the primary source for the radiometric calibration of detectors from the infrared to the soft x-ray regions of the spectrum. Presently, we have a

special project funded by the OMP for the calibration of DUV detectors. (See "Deep Ultraviolet Lithography for Semiconductor Photolithography.") NIST is presently expanding its capabilities to include the special requirements for the calibration of detectors of pulsed EUV radiation.

This year we have constructed a laser-produced-plasma (LPP) source similar to the one used for EUVL. It consists of a Nd:YAG laser that is focussed onto Kr that has been introduced into the vacuum through a pulsed valve. Depending on conditions, the Kr either forms clusters of a few million atoms or droplets a few μm in diameter. These are of solid density, thereby giving the high conversion efficiency of solids without the debris problems. We have also obtained prototype detectors to be used at the wafer plane of an EUVL stepper to monitor intensity and uniformity of the illumination of the wafer. Using our existing EUV facility at SURF III and various short-pulse systems in the visible, we are in the process of developing a method to make the necessary pulsed-EUV calibrations in our LPP system.

Accomplishments:

1. XCALIBIR is in the final commissioning phase.
2. We have developed radii of curvature measurements on XCALIBIR and demonstrated measurement reproducibility at the 10 nm^2 level when measuring a nominal 25 mm radius-of-curvature artifact. We have identified a previously unknown sensitivity of the measurement to wavefront characteristics of the PMI that leads to systematic effects on the order of fractions of a micrometer.
3. We have developed a methodology for arriving at an unbiased estimate of the root-mean-square surface departure from an optical test and the associated uncertainty.
4. The Ritchey-Common test configuration for flatness measurements of photomask blanks has been demonstrated.
5. The new Reflectometer has been delivered and commissioned. We have begun measurements on larger samples than ever before.
6. We have built a laser-produced-plasma light source and are in the final stages of performing measurements of pulsed EUV dosimeters provided by EUVL researchers.

Future Plans:

1) Nanometer level optical figure measurement.

The first self-calibration test will be carried out on XCALIBIR by fourth quarter FY01. This test will determine the figure errors on three 300 mm optical flats.

NIST will carry out figure measurements on EUV lithography mask blanks through a collaboration with Schott. The blanks will be measured in the Ritchey-Common configuration and with XCALIBIR using a short coherence length source. A coronograph-like interferometric test will be explored for identifying localized defects on these substrates.

2) Precise EUV reflectivity maps.

We are expecting the EUV-LLC to send us at least two large, curved optics, the C1 optic from the Engineering Test Stand and the MET1 optic from the MicroExposure Tool. Ours is the only facility in the US capable of measuring these pieces. Successful demonstration of our capabilities will likely lead to the LLC sending us more samples.

3) EUV dosimetry.

We expect to complete our pulsed EUV calibration of the EUVL dosimeter. Our successful completion of this project will likely lead to the LLC sending us later prototypes.

3) Multilayer mirror endurance testing

One of the outstanding problems in commercialization of EUVL is damage to the multilayer coatings of some of the optical elements. Mirrors must last for months between servicing, however, two factors lead to damage to the coatings after the equivalent of a few minutes in a commercial system. First, the system cannot be baked, therefore there is a high concentration of water vapor present; second the photoresist outgases, leading to a significant amount of hydrocarbon in the system. The first leads to oxidation of the top Si layer, the second to cracking of carbon on the surface.

A few mechanisms have been proposed for the mitigation of contamination. We intend to investi-

gate the microscopic causes of this contamination in order to better predict the results of mitigation methods.

Collaborations:

The optical figure metrology is done in collaboration with SVG-Tinsley and Schott.

The reflectometry and pulsed dosimetry are being done in collaboration with the Extreme Ultraviolet Limited Liability Corporation.

Publications:

C. J. Evans, A. Davies, R. E. Parks, and L-Z. Shao, "Interferometric Metrology of Photomask Blanks: Approaches Using 633 nm Wavelength," NISTIR 6701 (2000).

C. J. Evans, R. E. Parks, L-Z. Shao, T. Schmitz, and A. Davies, "Interferometric Testing of Photomask Blank Flatness," conference proceeding, SPIE conference on Microlithography, February (2001).

A Davies and M. Levenson, "Estimating the RMS of a Wavefront and Its Uncertainty," submitted to Applied Optics for publication.

"Extreme-ultraviolet radiation transmission and diffraction measurements of freestanding transmission gratings," D. R. McMullin, D. L. Judge, C. Tarrio, and R. E. Vest, to be submitted to Review of Scientific Instruments.

Presentations:

"New reflectometer chamber at the NIST/DARPA EUV Reflectometry Facility," C. Tarrio, L. Deng, S. Grantham, U. Arp, and T. B. Lucatorto, to be presented at 3-Beam Lithography Conference, Washington, May, 2001

"Extreme-ultraviolet metrology at NIST," C. Tarrio, R. E. Vest, and S. Grantham, invited talk to be presented at SPIE, San Diego, July 2001

"Upgraded measurement chamber at the NIST/DARPA EUV Reflectometry Facility," C. Tarrio, L. Deng, S. Grantham, U. Arp, and T. B. Lucatorto, invited talk to be presented at SPIE, San Diego, July 2001.

Lithographic Polymers

Technical Contacts:

***Eric K. Lin**, Christopher L. Soles, Wen-li Wu*

" Lithography continues to be the key enabler and driver for semiconductor industry. The growth of the industry has been the direct result of improved lithographic resolution ------the key elements of the lithography infrastructure include; ---resist materials ----metrology equipment for critical dimension (CD) and overlay control" **the ITRS, 1999 edition, p. 143**.

Objective:

To develop metrology for CD and roughness characterization at the 100 nm technology node and beyond. To identify and quantify material attributes dictating line-edge roughness (LER) in chemically amplified photoresists.

Customer Needs:

Photolithography remains the prevalent technology to fabricate the smaller feature sizes needed in next generation integrated circuits. The development of advanced lithographic materials and processes requires new metrology and fundamental scientific understanding at length scales approaching the characteristic size of an individual polymer molecule.

Technical Strategy:

We apply high-resolution measurement methods such as neutron reflectivity, x-ray reflectivity, and small angle neutron scattering both to understand fundamental materials and transport issues and to characterize LER and CD in thin film polymer photoresists. We are working closely with our collaborators at IBM to apply high-resolution metrology to address the most pressing issues in the development of new photoresists. Our efforts are focused in three general areas, the physical properties of sub-100 nm polymer films, the transport of polymer chains and small molecule components over nanometer distances, and the structural characterization of lithographically prepared structures.

Accomplishments:

We have developed the use of small angle neutron scattering (SANS) as a new metrology tool for the CD and LER characterizations of 130 nm lithographic features. Unlike current microscopy-based techniques, SANS has the advantages of measuring the structure directly on a silicon wafer (silicon is transparent to neutrons), becoming less technically demanding as feature sizes decrease, and making measurements non-destructively. We have demonstrated nanometer precision in the average width of a line and a methodology to extract the average roughness or resolution of line structures.

In the area of polymer thin film physics, we have performed x-ray reflectivity measurements to

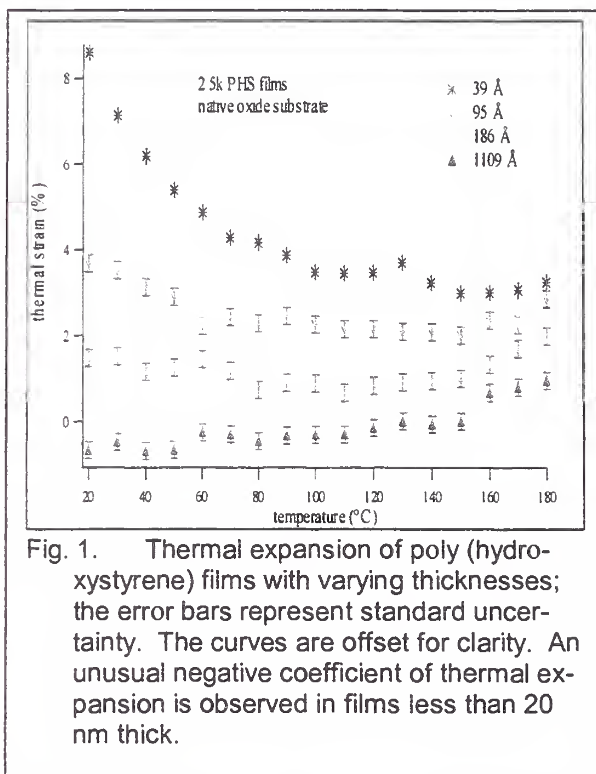


Fig. 1. Thermal expansion of poly (hydroxystyrene) films with varying thicknesses; the error bars represent standard uncertainty. The curves are offset for clarity. An unusual negative coefficient of thermal expansion is observed in films less than 20 nm thick.

determine the thermal stability of a model thin film polymer photoresist material, poly(hydroxystyrene) (PHS) (Fig. 1). We found that PHS polymer films exhibit an unusual negative thermal expansion behavior when the film thickness is less than 20 nm. Additionally, the magnitude of the thermal expansion above the glass transition temperature is suppressed as the film becomes thinner. This behavior has important implications in the stability and processing windows of thin polymer photoresist films. We

are now exploring the origins of this thermal expansion behavior as a function of polymer molecular mass and polymer-substrate interaction energy.

Future Plans:

To determine the feasibility of applying the SANS based metrology for characterizing LER in terms of both the sidewall roughness and the top surface roughness. We are developing an integrated program to correlate fundamental material and transport issues with CD and LER control. Our ability to measure the feature size and resolution of the final structure precisely and quickly will be analyzed using fundamental material information obtained from our high-resolution measurements.

Collaborations:

Qinghuang Lin, Marie Angelopoulos (IBM, T. J. Watson Research Center)

External Recognition:

Lin, E. K. Soles, C. L., Wu, W. L., Lin, Q. H., and M. Angelopoulos, "Neutron Reflectivity Measurements for the Interfacial Characterization of Polymer Thin Film Photoresists," 12th SPE Photopolymer Conference, 2000, in press.

Publications:

Wu, W.-L.; Lin, E. K.; Lin, Q., and Angelopoulos, M.,"Small Angle Neutron Scattering Measurements of Nanoscale Lithographic Features.", J. Appl. Phys. 88(12). (2000).

Wu, W. L.; Lin, E. K.; Lin, Q., and Angelopoulos, M., "Small-Angle Neutron Scattering Measurements for the Characterization of Lithographically Prepared Structures", Proc. of the 2000 Intl. Conf. on Characterization and Metrology for ULSI Technology, AIP Conference Proceedings 550, p. 357-360. (2001).

Soles, C. L., Lin, E. K., Wu, W. L., Lin, Q. H., and Angelopoulos, M., "Confinement Induced Deviation in Ultra-thin Photoresist Films," Proc. 12th SPE Photopolymer Conference, 2000, in press.

B. Critical Dimension and Overlay Metrology Program

The principal productivity driver for the semiconductor manufacturing industry has been the ability to shrink linear dimensions. A key element of lithography is the ability to create reproducible undistorted images, both for masks and the images projected by these masks onto semiconductor structures. Lithography as a whole, fabricating the masks, printing and developing the images, and measuring the results, currently constitutes ~35% of wafer processing costs. The overall task of the Critical Dimension and Overlay Program is to assist the industry in providing the necessary metrology support for current and future generations of lithography technology. These goals include advances in modeling, the provision of next generation critical dimension and overlay artifacts, and comparisons of different critical dimension and overlay measurement techniques.

Currently, resolution improvements have outpaced overlay and critical dimension measurement improvements. To maintain cost effectiveness significant advances must be made.

Atom-Based Dimensional Metrology

Technical Contacts:
R.M. Silver

Objective:
To develop three dimensional structures of controlled geometry whose dimensions can be measured and traced directly to the intrinsic crystal lattice. These samples are intended to be dimensionally stable to allow transfer to other measurement tools which can measure the artifacts with dimensions known on the nanometer scale

Customer Needs:
NIST is responsible to U.S. industry for developing length intensive measurement capabilities and calibration standards in the nanometer scale regime. The new class of scanned probes have unparalleled resolution and offer the most promise for meeting these future needs of the microelectronics industry. One important application of the high resolution SPM methods is in the development of linewidth standards whose dimensions can be measured and traced through the crystal lattice from which they are made.

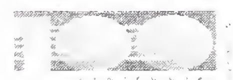
The work funded in this project is for the development of atom-based linewidth standards to assist in the calibration of linewidth metrology tools. This effort is intended to enable the accurate counting of atom spacings across a feature in a controlled environment and to subsequently transfer that artifact to other measuring instruments as a structure with atomically known dimensions. As critical dimensions continue to shrink, the detailed atomic structure, such as edge roughness or sidewall undercut, of the features to be measured occupies a larger portion of the measurement uncertainty. Furthermore, particularly with SEMs, the instrument response and the uncertainty in the edge location within an intensity pattern becomes a significant issue due to the increased sensitivity to detailed elements of the edge detection model. The complexity of these models and large computer resources required for each individual computation make the idea of having samples of known geometry and width essential. This project is intended to develop samples of known geometry and atomic surface structure which will yield measurements resulting in a specific number of atoms across the line feature or between features. These samples will be measured in the UHV environment and then stabilized and subsequently transferred to other instruments.

There are three primary applications of this type of artifact after it has been atomically counted. The first method is the direct calibration in an SEM for a product wafer whose geometry and material is near to the structure of the atomically counted sample. This method provides a direct calibration of an SEM although it is important to keep in mind that this calibration is valid only for the specific materials and geometries of the atomically counted sample. When using this method one perhaps cannot obtain a complete instrument calibration directly. However, when used in combination with Monte Carlo simulation models, it may be possible to calibrate the SEM over the entire range of desired parameters with a traceable calibration

The second method, utilizes an AFM to calibrate the SEMs with the AFM acting as an SEM matching tool. In this method, the AFM is calibrated with an atomically measured sample of the desired geometry as the product wafer to be measured by the SEMs. This sample only needs to have similar geometry to the product wafer but does require similarity in materials due to the insensitivity of an AFM to materials variations. The AFM which has been calibrated for a particular geometry by an atomic artifact can then transfer that calibration to a product wafer of similar geometry and any material such as photo resist, resulting in a calibrated product wafer which can then be transferred to calibrate an SEM. With this technique the AFM is used exclusively in an SEM matching/calibration mode. In addition, this approach removes the need for AFM tip calibration as long as the tip is not damaged during the measurement process.

The third method uses the number of atoms between features to determine the feature spacing. This method can be used to make magnification and pitch calibration standards based on the intrinsic crystal lattice.

These methods of atom counting as outlined in this report are non-destructive and are intended to yield samples which can be measured by various instruments such as an SEM and subsequently re-measured atomically. This is a unique and



important element of this work since there are no other known methods which allow this kind of atomic dimensional measurement **without being destructive**. In addition this new method opens up the possibilities of basing the measurement metric on the intrinsic crystal lattice rather than an external yard stick such as an interferometer or CCD calibration.

Technical Strategy:

The technical work is focused into four thrust areas. The first area is the development of methods to prepare photolithographically patterned three-dimensional structures in semiconductor materials. These structures must be prepared in such materials as to allow the atomic surface reconstruction of those features such that the atomic order is commensurate with the underlying crystal lattice.

The second thrust is the development of techniques for the preparation of SPM tips with reproducible geometries and the direct characterization of the SPM tip geometry and dimensions on the atomic scale. These well characterized tip probes can then be used to measure the samples with photolithographically defined and canonically ordered surfaces on the sub-nanometer length scale.

The third thrust is to develop PtIr and W tips for systematic measurements on atomically ordered silicon and GaAs surfaces. We are developing the SPM tip etching, field evaporation, and cleaning procedures which reliably yield stable W tips and produce atomic resolution on Si (7x7) surfaces. The primary tools for direct tip characterization are the FIFEM for 1 to 100 nm radii tips, and SEM analysis for larger tip features

In parallel the fourth thrust we continuously make a determination of the SPM performance in these dimensional measurements and improve the hardware through better vibration isolation, electrical noise reduction, etc. The last component of the work is to develop the methodology to enable the transfer of atom-counted samples to other measurement tools such as scanning electron microscopes or atomic force microscopes.

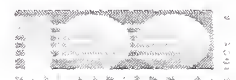
The atom-based metrology effort is focusing on developing artifacts which can be atom counted and then measured in a number of different metrology tools such as SEM and AFM. The integrity of the line geometry, such as side wall angle, is crucial to having useful artifacts for linewidth specimens. These edge geometry requirements are not as stringent for the magnification standards since feature symmetry is the most crucial element in these measurements. The work on linewidth artifacts, therefore, is focused on reducing the process temperatures required for atomic reconstructions. We have made wet chemical processing fully operational and are currently working on preparing atomically ordered Si surfaces at significantly reduced temperatures. For sample preparation, we are utilizing the existing in-situ processing apparatus and techniques from the UHV STM and concentrating on the reproducible production of atomically ordered Si surfaces and Si (111) step and terrace structures.

We have obtained atomically flat surfaces and are now trying to get atomic order using the low temperature wet chemical based methods. We have a similar effort going on with GaAs which will be very useful for AFM and optical CD calibration. We have produced atomically ordered surfaces of GaAs at far reduced temperatures and will begin work shortly with patterned GaAs linewidth samples. We have designed and procured a reticle to have the desired GaAs linewidth features fabricated. The new reticle has been received and we have begun processing new patterned linewidth specimens.

The long term technical objective is the development of in-situ stabilized, atomically ordered surfaces which can be transferred to other measurement instruments such as scanning electron microscopes, AFMs, or optical metrology tools. These nanometer scale standard artifacts with atomically ordered surfaces will then act as linewidth or magnification calibration samples.

Accomplishments:

Wafers from the NIST designed metrology reticle set have arrived. The initial evaluation is very promising and all four wafer flows yielded good product wafers. These wafers contain the prototype test structures for overlay standards as well as a comprehensive set of critical dimension and line space arrays for general metrology purposes. The silicon-etched silicon multi level features are intended to provide long term stable artifacts for calibration and the line arrays are test patterns for atom-based dimensional metrology work.



We have attempted our first direct measure of the surface atom spacings based on a traceable interferometer measurement. We have fitted our UHV STM with a high accuracy sub-angstrom resolution interferometer. We have closed the loop and made our first atomic resolution measurements with full interferometer length basis. The successful completion of this aspect has enabled direct distance determination with simple atomic counting. We are in effect verifying the intrinsic ruler accuracy.

New image recognition and quantitative image analysis software has been developed by lead analyst J. Jun of PED. This comprehensive software package is based on the Matlab programming language and tool set and allows the evaluation of numerous effects on algorithm performance. This package has been used to quantify feature spacings and dimensions using our new high resolution interferometer system. The package has also been used in the quantification of algorithm robustness for signal to noise effects. This code has been used extensively to evaluate and compare several cross-correlation methods.

The GaAs photomask has been received for the new GaAs atom counted linewidth specimen. The actual reticle design is that from quadrant 1 of the silicon ISMT mask set repeated multiple times. We are now making several small GaAs wafers with this mask which should yield enough die to perform a thorough set of experiments to verify the process and demonstrate the method.

We have produced atomically ordered surfaces of GaAs at far reduced temperatures and are now working with patterned GaAs linewidth samples. The new GaAs linewidth features have been fabricated and we have successfully prepared As capped samples without damaging the line geometry or integrity in any measurable way. These samples have been processed using the complete atomic surface preparation method, measured in UHV and then allowed to oxidize to create a stable surface for measurement in other tools. The samples have now been measured in other tools and the work is now focused on a quantitative evaluation of the samples.

The ability to prepare atomically sharp tips in W (111) has been demonstrated and the details of this methodology along with the new models we have developed for analyzing sharpness are currently being prepared as a journal article.

The first demonstration transfer has been attempted between the NIST MBE system and the PED UHV STM with minor difficulties which have been addressed. The sample was maintained in a UHV environment during the entire event.

Future Plans:

The ability to prepare atomically sharp tips in W (111) has been demonstrated and the details of this methodology along with the new models we have developed for analyzing sharpness are currently being prepared as a journal article. FY 2001

The first transfer has been demonstrated between the NIST MBE system and the PED UHV STM with minor difficulties which have been addressed. The sample was maintained in a UHV environment during the entire event. Further UHV sample manipulation and preparation for transfer to other systems and long term storage will now be investigated. FY 2002

Develop improved methods for preparation of photolithographically patterned three-dimensional structures in silicon. These structures must be prepared in such materials as to allow the atomic surface reconstruction of those features such that the atomic order is commensurate with the underlying crystal lattice. FY 2001.

We have developed techniques for the preparation of SPM tips with reproducible geometries and the direct characterization of the SPM tip geometry and dimensions on the atomic scale. We are now applying these ideas to FIM tips used in SEM metrology. FY 2001

Develop methods for the first demonstration of direct interferometer measurements of surface atom spacings with a complete unbroken uncertainty. Complete this link to develop an unbroken traceability chain to the international unit of length. FY 2002

Collaborations:

ISMT, IBM, University of Maryland, Dept. of Physics

External Recognition:

R. M. Silver et al, presentation for the "Best in Length" series hosted by the NIST director, R. Kammer.

Abstract submitted to ASPE, R.M. Silver and S. Gonda, "A Tunable Diode Laser used for Sub—nanometer Resolution Interferometry on an STM".

Publications:

P.V.M. Rao, C. Jensen, and R. M. Silver, "A Generic Shape Model for STM Tip Geometry", to be submitted to Ultramicroscopy, (2001).

R. M. Silver, S. Gonda, C. Jensen, and L. Howard, "A New Tunable Diode Laser Method for sub—nanometer Resolution Interferometry", to be submitted to Applied Optics, 2001.

Scanning Electron Microscope-Based Dimensional Metrology

Technical Contacts:

A.E. Vladar and M.T. Postek

"Scanning Electron Microscopy (SEM) –continues to provide at-line and inline imaging ... and CD measurements... Improvements are needed ... at or beyond the 100 nm generation. Determination of 3D sidewall shape...will require continuing advances in existing microscopy." ITRS, 1999

Objective:

To provide the microelectronics industry with highly accurate SEM measurement and modeling methods for shape-sensitive measurements and relevant calibration standards with nm-level resolution. Carry out SEM metrology instrumentation development, including improvements in electron gun, detection, sample stage and vacuum system. Conduct research and development of new metrology techniques using digital imaging and networked measurement tools.

Customer Needs:

The scanning electron microscope is used extensively in many types of industry, including the more than 200 billion dollar semiconductor industry, in the manufacture and quality control of semiconductor devices. The International Technology Roadmap for Semiconductors targets SEMs as the metrology tool of choice for use in semiconductor production up through at least the year 2005. The industry needs SEM standard artifacts, specifically those related to instrument magnification calibration, performance and the measurement of linewidth. This entails a multidimensional program including: artifact fabrication, understanding the function and signal generation in the SEM, electron beam interaction modeling, developing NIST metrology instruments for the certification of standards, and developing the necessary artifacts and calibration procedures.

The manufacturing of present-day integrated circuits requires that certain measurements be made of close to 100 nm structures composing the device with a high degree of precision. The accuracy of these measurements is also important, but more so in process development and pilot lines. The measurements of minimum feature sizes known as critical dimensions (CD) are made to ensure proper device operation. The U.S. industry needs high-precision, accurate, shape-sensitive dimension measurement methods and relevant calibration standards. The SEM Metrology Project supports all aspects of this need since scanning electron microscopy is the major microscopic technique used for this sub-micrometer metrology.

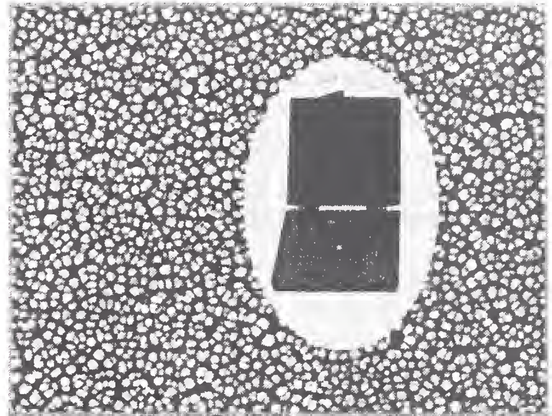


Fig. 1. The new RM 8091 Sharpness Reference Material

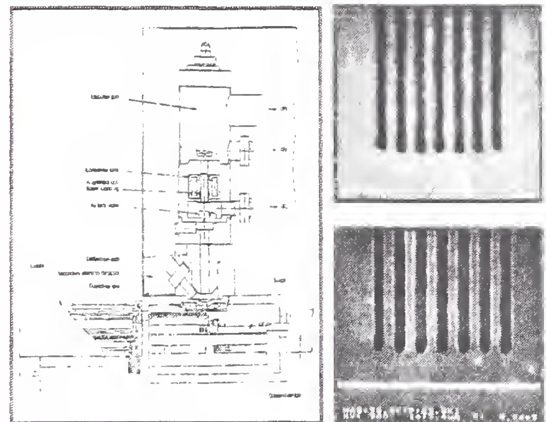


Fig. 2. Schematic drawing of the SEM Sentinel system (left) Resolution improvement with sharp tip (right)

Technical Strategy:

The Scanning Electron Microscope Metrology Project is a multidimensional project. It is being executed through several thrusts fully supported by the semiconductor industry through the interaction with ISMT.

SEM Magnification Calibration Artifacts: Primary to SEM dimensional metrology is the

calibration of the magnification of the instrument. Standard Reference Material (SRM) 2090 is an SEM magnification standard that will function at the low beam voltages used in the semiconductor industry and high beam voltages used in other forms of microscopy. A prototype with 200 nanometer lines and spaces was fabricated by the Nanofabrication Facility at Cornell University as a proof of concept and was used in a round robin study that clearly demonstrated the need for this standard. Texas Instruments was contracted to supply the first production run of the artifact with 100 nanometer lines and spaces and delivered over 180 of these artifacts. In order to speed the availability of this artifact to the industry (while the final certification details are being completed) the artifact has been released to the industry as Reference Material (RM) 8090.

SEM Performance Measurement Artifact: This effort includes the development of the Reference Material (RM) 8091 and evaluation procedures suitable for correctly measuring image sharpness of scanning electron microscopes, especially of those that are used in the semiconductor industry. The performance characteristics of the SEM are particularly important to precise and accurate measurements on the semiconductor processing line. NIST has demonstrated that a critical dimension scanning electron microscope functioning poorly can measure the dimensions 5 nm or more larger than the same instrument functioning optimally. For reliable image sharpness measurements a suitable sample with small features is needed.

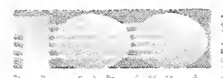
SEM Linewidth Measurement Artifacts: Artifacts that are characterized and calibrated to the required small levels of uncertainty were and are in the focal point of the IC industry's dimensional metrology needs. Therefore, at NIST, it has been a mission in long existence to develop and deliver appropriate samples. For a long time the possibilities were limited by the lack of various technologies available, especially the development of accurate modeling methods were required. NIST though several years of systematic efforts, developed Monte Carlo simulation-based modeling methods that can deliver excellent results. These new methods can deduce the shape of integrated circuit structures from top–down view images through modeling and library–based measurement techniques with few nm accuracy. NIST in several publications demonstrated the possibilities and described the power of this measuring approach. Based on the newest results, now it is becoming possible to start to develop the long–awaited relevant linewidth standard for the semiconductor industry. Reference Material 8120 linewidth samples will be a relevant sample on a 200 mm Si wafer with polySi features with sizes from 1 µm to down to 140 nm. Standard Reference Material 2120 is going to be the calibrated, traceable version for linewidth measurements. This work is being carried out in cooperation with ISMT.

Accomplishments:

SEM Magnification Calibration Artifacts: Samples for Reference Material 8090 and the certified traceable version, the Standard Reference Material 2090 are being made with UV light lithography through a contract with Maxim Corp. The use of conventional lithography and a somewhat modified design gives a chance for large amount of good quality samples. Because of the limitations of the technology, it is not possible to produce the finest lines with 100 nm width and with 200 nm pitch values of the original prototype. Instead 200 nm wide lines with 400 nm pitch will be available. The features on the conductive Silicon wafer will be formed from polySilicon material. These samples will give suitable contrast in any SEM to allow the user to set the magnification of the instrument from the smallest to the highest magnifications.

SEM Performance Measurements: After comprehensive studies and experiments a plasma-etching silicon called "grass" was chosen as a RM 8091. This sample has 5-25 nm size structures as it is illustrated in Fig. 1. 15 pieces of prototype RM 8091 were delivered to ISMT for testing and evaluation by the member companies, and 75 additional samples will be delivered soon to the Office of Standard Reference Materials (OSRM). RM 8091 and the evaluation procedure have been developed to monitor (or compare) SEM image quality. The NIST kurtosis method, Spectel Company's analysis system called SEM Monitor, and University of Tennessee's SMART algorithm can be used with RM 8091. An effort is underway to produce more of these samples in full wafer-sized format.

SEM Linewidth Measurement Artifacts: The development of accurate modeling methods are in



progress. The design of ISMT/NIST mask has been completed; the fabrication of the mask is being done. The first good quality wafers are expected to be made before the end of June 2001. It is conceivable that by the end of the year 2001 the Reference Material 8120 linewidth samples will be available for industrial evaluation. This work is being carried out in close cooperation with ISMT.

Future Plans:

- Issuance of RM 8090 and SRM 2090 magnification calibration artifacts.
- Issuance of RM 8120 linewidth Reference Material as a 200 mm Si wafer. Carrying out the development work, including thorough modeling and preliminary measurements needed for the certified traceable version, the Standard Reference Material 2120.
- Completion of the development of the ultra-high resolution nano-tip electron gun for the ISMT CD SEMs project.
- Proposal development and initiation of a feasibility study of overlay metrology done with SEMs.

Collaborations:

ISMT, Austin, TX

Publications:

Vladar, A. E., Postek, M. T., Zhang, N–F, Larrabee R. D. and Jones, S. N., Reference Material 8091: New Scanning Electron Microscope Sharpness Standard. Proceedings of SPIE 3444; 2001 Santa Clara (in press).

Vladar, A. E., Postek, M. T. and Vane R., Active Monitoring and Control of Electron Beam–Induced Contamination. Proceedings of SPIE 3444; 2001 Santa Clara (in press).

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Optical-Based Dimensional Metrology

Technical Contacts:

R. Silver, J. Potzick, and T. Doiron

Objective:

Provide technological leadership to semiconductor and equipment manufacturers and other government agencies by developing and evaluating the methods, tools, and artifacts needed to apply optical techniques to the metrology needs of semiconductor microlithography. One specific goal is to provide the customer with the techniques and standards needed to make traceable dimensional measurements, where appropriate, at his or her facility. The industry focus areas of this project are primarily the optical based methods used in overlay metrology and photomask critical dimension metrology as well as needs for high-accuracy two-dimensional placement metrology.

Customer Needs:

Tighter tolerances on CD measurements in photomask and wafer production place increasing demands on photomask linewidth accuracy and on overlay tolerances. NIST has a comprehensive program to both support and advance the optical techniques needed to make these overlay and pohotomask critical dimension measurements.

In addition, improved two-dimensional measurement techniques and standards are needed for measuring and controlling overlay capabilities of steppers and mask-making tools under development. Overlay is listed in Table 38, page 145 of the 1999 sia ITRS as a difficult challenge for both >100 nm and <100 nm processes, and states that overlay improvements have not kept pace with resolution improvements and will be inadequate for ground rules less than 100 nm. Also overlay over large field sizes will continue to be a major concern for sub-130 nm lithography. It also shows, in Table 41, pages 150-151, that two-point placement accuracy is and will be a critical issue for rules at 165 nm and less.

Technical Strategy:

There are three main strategic technical components of this project. The first is the continuous development of the NIST overlay metrology tool, measurement methods to obtain uncertainties comparable or better than the best industry overlay tools, and standards to support and calibrate these tools. The second component is the ultra violet transmission microscope, calibration of SRMs 2059 and 2800, and the development of calibration methods to obtain measurement uncertainties adequate to meet industry needs. The third component is the development of two-dimensional grid calibration standards and associated measurement techniques, including statistical analysis and CCD characterization as used by industry. These individual technical strategies for these components are described in more detail next.

The technical strategy for overlay metrology is divided into two segments: 1) instrumentation development and overlay metrology methodology

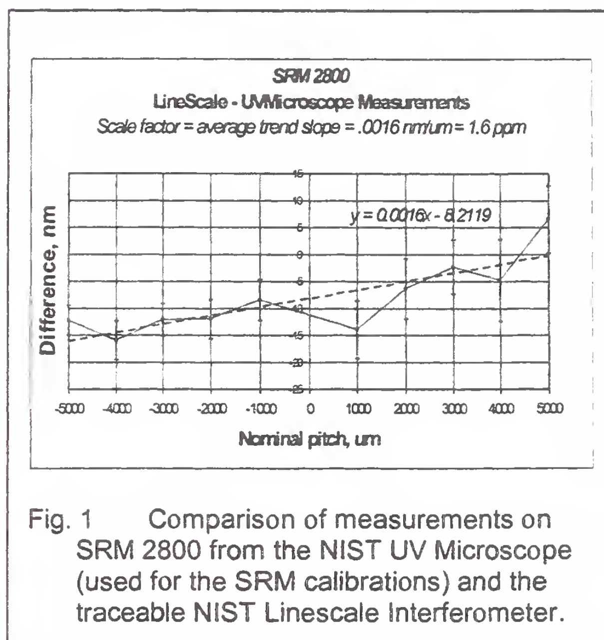


Fig. 1 Comparison of measurements on SRM 2800 from the NIST UV Microscope (used for the SRM calibrations) and the traceable NIST Linescale Interferometer.

and 2) design and calibration of standard artifacts. Pattern placement and overlay of the various lithographic levels is monitored with a series of targets, each in a different plane. The overlay offset is then obtained by optical measurements with a determination of the relative target centerlines. Any misalignment in the overlay metrology system will translate into an artificial overlay offset, referred to as *tool induced shift* (TIS). Additionally, there are residual errors caused by asymmetries in the target edges or covering layers (resist) known as *wafer induced shift* (WIS). A set of standard artifacts and procedures, under development at NIST, is designed to assist in aligning overlay measurement systems and eliminating TIS.

After alignment, the tool must then be calibrated with standard artifacts to yield accurate overlay offsets.

The measurement system used in this component is an optical reflection mode instrument, operational in either a bright field or confocal mode, with interferometry on three orthogonal axes also capable of monitoring the stage tilt. Additional hardware capabilities include the options to scan the sample while acquiring data with an on-axis photometer or high resolution image capture with a full field CCD data acquisition system. This latter mode has enabled a detailed study of CCD array performance and characterization. In this work, several CCD acquisition systems are being evaluated and improved edge detection and CCD array calibration procedures are being developed These same methods for 2-dimensional CCD array analysis are now being applied to optics analysis. Additional investigation of CCD measurement problems are focused on the detailed response of typical CCD camera light sensors.

WIS-free standard overlay artifacts have been fabricated in 200 mm wafers. These overlay artifacts are for the calibration of industrial optical overlay tools. The artifacts are being fabricated in single crystal silicon and will provide an array of etched silicon three-dimensional targets with additional targets fabricated using industry standard process levels. These wafers additionally have an extensive set of characterization targets and structures developed in close collaboration with SEMATECH and several leading semiconductor manufacturers.

The technical strategy for photomask linewidth standards is similarly divided into two segments: (1) instrumentation and model development and (2) design and calibration of standard artifacts. An ultraviolet transmission microscope has been constructed which replaced the green light linewidth calibration system. This new instrument uses a unique geometry (a Stewart platform) as the main rigid structure and shows considerable improvement in vibration characteristics over a conventional microscope. Higher image resolution, reduced transmission of UV light through the chrome, and reduced instrument vibration will offer improved linewidth measurement uncertainties.

NIST has supplied a substantial number of photomask linewidth standards worldwide over the past decade. Chrome-on-quartz photomasks with linewidth and pitch artifacts in the range of 0.5 µm to 30 µm have been certified on a green light optical calibration system. Linewidth uncertainties have been reduced to 40 nm.

SRM 2800 Microscope Magnification Standard is a standard size microscope slide with calibrated pitch features ranging from 1 µm to 1 cm. It contains a lithographically produced chrome pitch pattern consisting of a single array of parallel lines with calibrated spacings. It contains no linewidth structures. This SRM is intended to be used for the calibration of reticles for optical or other microscopes at the user's desired magnification. The SRM may be used in either transmission or reflection mode optical microscopes, SEMs, or SPMs. Calibration is traceable to the meter through NIST Line Scale Interferometer. NIST is also currently instituting a new calibration for SRM 2059, a current specifications photomask linewidth standard artifact. *SRM 2059 Photomask Linewidth Standard* and *SRM 2800 Microscope Magnification Standard* are intended to enable customers to make traceable measurements of the dimensions of features on integrated circuit photomasks and of the magnification of optical, electron, and scanning probe microscopes.

In response to customers' needs for more accurate photomask feature size measurements, an industry group was formed for the improvement of mask metrology through process modeling. The features on even the highest quality masks exhibit roughness and runout at the chrome edges, compromising the definition of edge and linewidth. Modeling the effects of all of the relevant feature properties in both the mask metrology process and in wafer exposure and development processes, using existing and new software tools, can improve feature size accuracy by establishing the relationship between mask-feature metrology results and the corresponding wafer-feature sizes.

We are approaching the problem of two-dimensional measurements from a number of directions. The first, and most immediate, is to develop an artifact standard which can be used to bring all of the two-dimensional based inspection instruments to the same metric. This work will

develop a standard grid which will be sold as a NIST Standard Reference Material, # 5001, to standardize 2D measurements in the semiconductor industry. The effort has three main parts: development of an industry consensus standard grid, measurements by state-of-the-art machines in private industry, and verification of the measurements using NIST capabilities.

A prototype grid has been made and measurements completed. Each measurement of the grid will have data in each of at least two orientations. Rotating the grid 90° between measurements samples a number of the geometric errors of the machine. The remaining geometric sources of uncertainty are the scale and some components of the linearity of each machine axis travel.

Verification of the grid measurements will be made at NIST. The overall scale of the grid will be checked with the NIST linescale interferometer, an instrument that is known to provide the most accurate 1D measurements available in the world. Two sources of uncertainty not captured by these measurements include components of the straightness and effects of the plate bending when fixtured. We have begun work on methods to characterize both of these effects. These studies provide a complete error budget for SRMs in the near future.

To strengthen the foundation of NIST's claims for linewidth measurement traceability and to support the BIPM *Mutual Recognition Arrangement*, NIST has become the pilot laboratory for an international intercomparison of submicrometer linewidth measurements. National metrology institutes in nine countries around the world are participating.

Accomplishments:

New image recognition and quantitative image analysis software has been developed by lead analyst J. Jun of PED. This comprehensive software package is based on the Matlab programming language and tool set and allows the evaluation of numerous effects on algorithm performance. The package has been used to quantify feature roughness and asymmetry effects on overlay pattern evaluation used in the feedback and control of lithography stepper tools. It has also been used in the quantification of algorithm robustness for sample-to-noise effects. This code has been used extensively to evaluate and compare several cross-correlation, self-correlation and new least-squares correlation methods these are proving to be the most robust edge detection and feature centerline determination methods.

The overlay metrology project is establishing a CRADA with Schlumberger to improve ties and make available recent important research results on optical characterization, CCD data acquisition calibration, and focus and edge detection work. Neil Sullivan of Schlumberger showed strong interest in strengthening the collaboration with the overlay metrology project. NIST development of new correlation methods and image analysis/recognition software has enabled the detailed evaluation of noise, feature roughness, and feature inhomogeneity effects on repeatability and robustness of measurement tool performance, issues of paramount importance in semiconductor overlay metrology. We have performed a detailed, in depth study of CCD data acquisition cameras. In this work, several CCD acquisition systems were compared and results demonstrate the significant performance differences and error sets. This work was presented and published at the NIST 2000 ULSI International conference.

- The NIST Overlay Metrology project leader has played a significant role in the Overlay Metrology Advisory Group (OMAG) of ISMT. This group is developing a comprehensive set of measurement guidelines, test methods, and tool performance measures to be adopted by the semiconductor manufacturing industry. The group, made up of more than 15 international semiconductor manufacturers represents leading optical metrology users and tool manufacturers. The OMAG has strong interest in adopting several new methods developed in the NIST Overlay Metrology Project. In particular, the recently published methods for evaluating CCD array performance and overall optical system characterization and calibration performance measures will be adopted to provide quantitative tool evaluations. NIST is also assisting in the development of definitions and categorization for tool errors and performance measures.

NIST was represented in the Overlay Metrology Advisory Group (OMAG) in Austin Texas. This group has completed a specifications document for the evaluation and benchmarking of overlay metrology tools for semiconductor manufacturing.. This international advisory group is composed of

all of the international semiconductor manufacturing ISMT member companies as well as tool manufacturers. The document is expected to be widely used for procuring, testing, and matching overlay metrology tools. R. Silver authored several sections which include the adoption of test methods recently developed by the overlay metrology project at NIST.

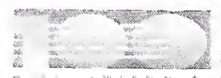
The first set of two-dimensional grid artifacts, to be known as SRM 5001, have been received. These 6-inch have been measured on a state-of-the-art I-pro metrology system by the photomask manufacturer. This effort, to make available traceable, 6-inch feature placement standards, involves a close collaboration between NIST and Photronics. The collaboration employs the industry tool and the traceability of the NIST line scale interferometer with appropriate statistical analysis. The initial comparisons and work leading to this point indicate we will make available the most accurate, traceable feature placement standards in the world. Preliminary uncertainty budget for grid measurements has been developed and peripheral studies on various items have been, or are currently being made.

The 6-inch grid standard prototype has been measured at PTB in a comparative test on the international unit of length. The round robin and PTB measurements have been used in the designs for the new grid artifacts. The new set of have been received and will become available as SRM 5000 in the near future. These grid artifacts have both the 5 mm pitch 6-inch grids as well as the 100 micrometer microgrids. Round robin measurements on the 6-inch photomask grid proved successful. The measurements show that we are able to make available a standard artifact which meets industry need based on the outlined methodology. We have also completed a set of measurements with the microgrid which proved very useful in two-dimensional calibrations and characterization of optical tools. These microgrids present on each 6-inch photomask are designed to assist in system alignment and calibration for both high accuracy x-y tools and overlay metrology tools.

Wafers from the NIST designed metrology reticle set have arrived. The comprehensive set of initial measurements is very promising and all four wafer flows yielded good product wafers. These wafers contain the prototype test structures for SRM 5000, the overlay standards as well as a comprehensive set of critical dimension and line space arrays for general metrology purposes. The silicon-etched silicon multi-level features are intended to provide long term stable artifacts for calibration and the line arrays are test patterns for optical system and CCD mapping and calibration. These results were presented to the semiconductor manufacturing community and the response was very favorable. Close collaboration on the development of these standards with ISMT and the current measurements conducted at NIST have also been compared to ISMT industrial tool measurements successfully.

NIST researchers have made comparisons between the E. Marx developed optical scattering code with the Spectel company Metrologia metrology modeling package. Different material systems were compared as well as one overlay feature at different focus positions. Although more work needs to be done, this result demonstrated the full integration of the NIST scattering code and Spectel optical microscope model. These outputs were compared with the independent scattering calculations performed by Mark Davidson of Spectel. Reasonable agreement was seen in the through focus simulation comparisons. This is an important step in the effort to provide industry the quantitative ability to determine sample-dependent effects on overlay tool performance as well as obtaining accuracy on non-ideal targets.

More than half of the seventy SRM 2800 samples have been calibrated to date. The traceability path has been established through a sophisticated comparison with the NIST Linescale Interferometer. This required development, with the help of the NIST Statistical Engineering Division, of a novel method for calculating the uncertainty of the slope of a regression line taking into account the uncertainty in the data points. The complex index of refraction of the chrome features on SRM 2059 photomasks, as it varies from substrate to antireflecting top surface, has been measured, and a library of modeled microscope images of lines and spaces of varying width is being generated. Leadership of the industry group for the improvement of mask metrology through process modeling has been transferred to ISMT.



Future Plans:

Complete the formal qualification process of the overlay microscope optics and the x-y metrology stage. This is largely completed and the final uncertainties on the CCD array scale factors need to be finalized. The more difficult challenge is the qualification of the calibration for more difficult to measure overlay target process levels such as contact-to-poly.

Continue to develop comprehensive modeling capabilities for centerline and edge detection methods and modeling techniques for edge analysis and pitch determination, in the reflection mode for overlay measurements.

Develop additional methods for CCD calibration and analysis. Utilize the new microgrid and 8 inch overlay wafers for calibration of optics and the CCD acquisition systems using the new self-calibration methods. Utilize these methods with the new CCD stepping calibration stage system.

Complete the 2-dimensional grid artifact calibration measurement sequence with applications of the self-calibration algorithms. This is a combined industry/NIST effort using our LSI and statistical methods.

Design and procure the new metrology reticles for the over all ISMT collaboration. Work with Industry partners to determine designs and which levels are most appropriate for the silicon fabrication phase. Calibrate these overlay standards (both alignment and calibration) for SRM certification.

Identify and invite appropriate companies to participate in the Neolithography task force, and have the first meeting.

Commence circulation of the NIST linewidth standards for the BIPM international comparison.

Complete calibrations of SRM 2800 and the related documentation, and deliver to the Office of Standard Reference Materials for distribution to customers. Commence calibration of SRM 2059.

Collaborations:

ISMT, IBM, IVS Schlumberger, KLA-Tencor, Intel, Motorola, AMD and several other leading manufacturers or tool vendors.

The fourteen members of The Neolithography Consortium.

Semiconductor Equipment and Materials Manufacturers International

External Recognition:

R. Silver was a program committee member and a session chair for the SPIE Microlithography Conference for the past 2 years.

R. Silver is currently the Co-chair for the SPIE Microlithography Conference for February, 2002.

R. Silver is currently an active OMAG member within ISMT. This group is focused on Overlay metrology needs for the international manufacturing community.

R.. Silver was invited to present the NIST reticle design set for the overlay wafers and a comprehensive overview of our overlay project to ISMT member companies in CA, February 2001.

IBM and Photronics have taken an active role in the measurement process and completion of the two-dimensional grid standards. This is a unique collaboration of industry partners and NIST semiconductor research efforts.

R. M. Silver, ISMT presentation on Overlay Metrology at the October 1999 ISMT Metrology Workshop, Austin TX.

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Scanning Probe Microscope-Based Dimensional Metrology

Technical Contacts:

R. Dixson, J. A Dagata, M. T. Postek, T.V. Vorburger

The ITRS identifies dimensional metrology as a key enabling technology for the development of next-generation integrated circuits. For example, the goal in 1999 for critical dimension (CD) measurement precision for isolated lines was ± 2.8 nm; this demand tightens to ± 0.8 nm by 2011.

Objective:

Improve the measurement uncertainty of critical-dimension measurements in the semiconductor industry through improvements in SPM-based measurements. The technical focus of this project, development and implementation of scanned probe microscope instrumentation, is driven by the anticipated industry needs for reduced measurement uncertainty, particularly for existing tools such as the SEM.

Customer Needs:

The SEM is the current tool of choice for inspection and metrology of sub-micrometer features in the semiconductor industry. SPMs possess unique capabilities that may significantly enhance the performance of SEMs for in-line critical dimension (CD) measurements, and are also emerging as CD measurement tools in their own right. A creative strategy which successfully harnesses the strong points of both techniques in order to reduce the measurement uncertainty of sub-micrometer features while minimizing their limitations will help NIST meet the expectations of the semiconductor industry expressed in the current Roadmap. As is the case with SEMs, the magnification or scale of an SPM must be calibrated in order to perform accurate measurements. Although many SPMs are commercially available, appropriate calibration standards have lagged. In particular, traceable standards for sub-micrometer lateral calibration are not yet available.

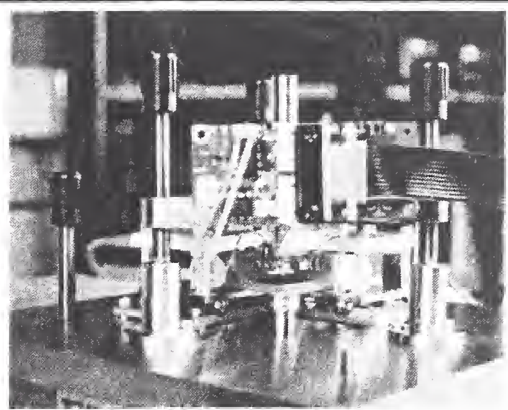

Fig. 1. Photograph of the C-AFM – a dimensional metrology SPM constructed as part of the second thrust of the project.

Technical Strategy:

SPM development is proceeding along two parallel directions: The first direction addresses dimensional metrology of SPM specifically through an in-house research instrument we refer to as the calibrated atomic force microscope (C-AFM). A photograph of the instrument is shown in Figure 1. This instrument, with metrology traceable to the wavelength of light on all three axes, is furthering the design and development of SPM standards as well as providing customers with calibrated dimensional measurements at the nanometer scale. For example, pitch, height, and width measurement capabilities of the C-AFM have been evaluated and validated by internal comparisons. Pitch, ranging up to 20 µm has been measured using an edge-to-edge measurement method, with standard uncertainties (1σ), as low as ≈0.5 nm at sub-micrometer scales and relative standard uncertanties of ≈0.1 % at the largest scales. For measurement of periodic samples, especially holographic gratings, frequency domain analysis of the data may allow for further reduction in uncertainty. Step height, ranging from a few nanometers up to several hundred nanometers, can be measured with standard uncertainties (1σ) of ≈0.1 %. As with pitch measurements, the uncertainty of step height measurements is often increased by variations of the sample. The width of sub-micrometer, near-vertical features, as encountered in CD measurements, can be measured to an uncertainty (1σ) of ≈10 nm, due mostly to the finite size of the SPM tip.

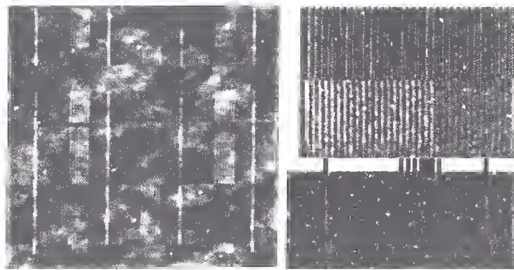

Fig. 2. Latent SPM oxide grating patterns on a silicon substrate. Examples illustrate 100 nm pitch

The second direction addresses increasingly overlapping demands for dimensional control during fabrication and subsequent calibration of nanometer scale features. For this purpose we employ an SPM-based lithography technique, pioneered at NIST, to produce grating structures with linewidths of 20 nm or below. An example of a latent oxide pattern on a silicon substrate is shown in Figure 2. Latent oxide patterns function as masks for anisotropic wet or dry etching. We are also developing an instrument which integrates both SPM and probe station measurement capabilities whereby we are able to compare SPM-based electrical (capacitance and surface potential) and topographical measurements of active device structures simultaneous with traditional current-voltage (I-V) characteristics measured with a probe station. This allows us to examine local nanoscale variations at exposed and buried interfaces of critical dimensioned features in order to identify processing induced variations which contribute to linewidth uncertainty in dimensional and electrical test structures.

Accomplishments:

The C-AFM thrust involves collaboration with industrial users and academic researchers in AFM metrology, as well as interaction with researchers in NIST's sister institutions in other nations. During FY98-99 the first pitch and step height measurements for an external customer were completed. Expanded uncertainties (k=2) of 0.5 % and 1 % were reported for these measurements, limited by sample uniformity. We are participating in a series of international measurement comparisons being sponsored by the BIPM (Bureau International des Poids et Mesures). Comparisons of 1D pitch, 2D pitch, step height, and linewidth measurements are being carried out. Gratings having nominal pitches of 300 nm and 700 nm were measured using the C-AFM with relative standard uncertainties of about 1×10^{-3}. Support by the NIST Office of Standard Reference Materials is allowing us to design prototypes of SRM 2089, with test samples fabricated at the Naval Research Laboratory. This is shown in Figure 3. Evaluation of these samples is currently underway and an initial release of SRM 2089 is expected by FY02. We are also working toward the development of linewidth standards. During FY99, we completed C-AFM linewidth measurements on the NIST linewidth correlation sample. The C-AFM achieved an expanded uncertainty (k=2) of 11 nm for this measurement, in agreement with the SEM and electrical resistance values. During FY00 we performed preliminary measurements on one of the new ISMT/AMAG (Advanced Metrology Advisory Group) samples. We plan to continue these measurements using high resolution probes during FY01.

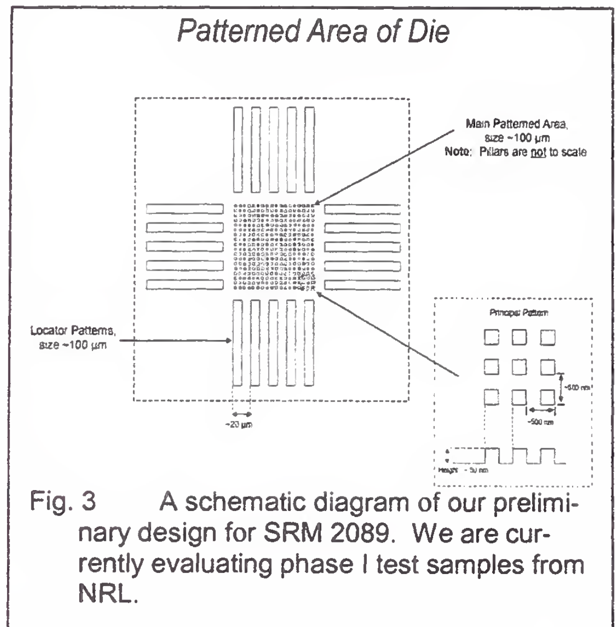

Fig. 3 A schematic diagram of our preliminary design for SRM 2089. We are currently evaluating phase I test samples from NRL.

Another important effort involves the study of single atomic steps as fundamental height standards in the sub-nanometer regime. Various researchers have studied silicon samples, fabricated in UHV with single atomic steps on the surfaces, and observed the preservation of the step structure after native oxidation. We have performed C-AFM measurements on such samples under a variety of measurement conditions. The theoretical value of the step height, based upon the

measured lattice constants of bulk silicon, is about 0.314 nm. The C-AFM measured value is 0.304 nm ± 0.008 nm (k=2), a difference of 0.010 nm. Using the lattice value, the C-AFM result, and a LEED (low energy electron diffraction) result obtained by researchers at the University of Maryland, and in consultation with the NIST statisticians, we developed an accepted value for the step height of 0.312 nm ± 0.012 nm (k=2). We also distributed a set of silicon step samples, prepared by Williams, et al. at the University of Maryland, to four industrial collaborators, and completed analysis of the data received from the participants. All of the analysis was performed at NIST using the NIST algorithm for step height calculations, which is insensitive to tilt and curvature of the surface, an issue at the high magnifications required to perform subnanometer height measurements. A key observation following from the study is that specimens of this type, which can now be procured commercially or fabricated using published methods, can be used as z-axis calibration standards for atomic force microscopes in the sub-nanometer regime with an expanded relative uncertainty of about 6 %. These results were presented in a talk at the 2001 SPIE Microlithography Meeting.

In the integrated SPM probe-station thrust, we have completed construction and testing of the combined instrument. Test structures consisting of silicon FETs realized on silicon-on-insulator substrates are being used as a starting point for patterning nanodevices and performing in-situ correlation of the dimensional and electrical properties of these confined regions. An example is shown in Figure 4. SPM lithography has been used interactively with electrical mapping to create successively smaller active gate regions for detailed studies of local device scaling. This capability allows us to examine local nanoscale variations at exposed and buried interfaces of critical dimensioned features in order to identify processing induced variations which contribute to linewidth uncertainty.

We have also demonstrated large-scale (100 μm × 100 μm) patterning of 35 nm linewidth SPM oxide features on 110-oriented silicon substrates. These patterns can be developed by potassium hydroxide or trimethyl ammonium hydroxide etching to form densely packed gratings which can be several hundred nanometers in height. Processing control during the lithographic patterning and etching steps to routinely produce calibration-grating structures is now being optimized and SEM inspection of these structures is anticipated shortly.

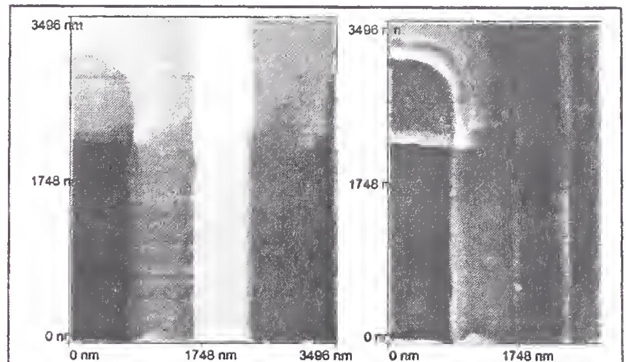

Fig. 4: SPM topographical (left) and surface potential (right) image maps of the 2 μm x 0.5 μm x 7 nm gate region of a SOI tunnel transistor, shown with an outline in the figures. p^{++}-Si source and drain are the bright areas above and below the gate, which is also p^{++}-Si. The device functions by back-gating via the substrate. Although the topography of the gate structure is highly uniform, LOCOS thinning of the gate region leads to partially depleted defect regions near the source and drain.

Future Plans:

In the C-AFM thrust, the major goals are: (1) By 2002, release SRM 2089, a combined pitch and height standard for AFM. (2) By 2002, complete participation in four BIPM-sponsored international measurement comparisons. (3) During 2001, complete integration of a new x-y and z stage into the C-AFM to increase scan area and reduce motion errors. (4) During 2001, improve system performance of C-AFM controller.

In the SPM probe-station thrust, the major goals are: (1) By 2002, fabricate and characterize functional sub 100 nm quantum devices on silicon-on-insulator substrates. (2) By 2001, demonstrate in-house capability to prepare and characterize large-scale calibration gratings with 50 nm to 100 nm pitch. (3) By 2002, initiate efforts employing two NIST standard reference materials, SRM 2090 and SRM 2091, which are currently under development as SEM magnification and sharpness standards, to assess the potential of algorithms for

overlaying SEM and SPM datasets for constructing a reduced uncertainty composite image of calibration features.

Collaborations:

(JAD) Electrotechnical Laboratory, Tsukuba Japan.
(JAD) National Center Microelectronics, Autonomous University of Barcelona, Barcelona Spain.
(RD & TV) University of Maryland, College Park
(RD & TV) University of North Carolina, Charlotte

External Recognition:

(JAD) Science and Technology Agency of Japan research fellowship at the Electrotechnical Laboratory, Tsukuba, Japan, July –October 2000.

Publications:

R. Dixson, N. G. Orji, J. Fu, V. Tsai, E. D. Williams, R. Kacker, T. Vorburger, H. Edwards, D. Cook, P. West, and R. Nyffenegger, "Silicon single atom steps as AFM height standards", *Proc. SPIE* **4344** (2001), to be published.

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Electrical-Based Dimensional Metrology

Technical Contacts:
Michael W. Cresswell

"The Photomask industry as well as the Semiconductor industry have a problem meeting the technical road map using optical systems to measure IC patterns. As the time line moves forward we get closer to a point that our current measurement systems will not be able to satisfy the requirements. This is why the project of electronic measurement has appeal to Photronics. We would like to continue supporting this project and hopefully as the electronic measurement tools become viable NIST has a traceable standard. Thanks for your continuation of this standard." **Dave Owens, Photronics Laboratories.**

Objective:
Develop test-structure-based electrical metrology methods and related reference materials with primary emphasis on linewidth metrology and calibration. Develop infrastructure needed for manufacture and distribution by industry partner. Extend implementation to overlay, scatterometry, and pitch reference materials.

Customer Needs:
The semiconductor industry association's (SIA) International Technology Roadmap for Semiconductors (ITRS) states that it is critically important to have suitable reference materials for lithography support available when on-wafer measurements are made as a new technology generation in integrated circuit (IC) manufacturing is introduced, and particularly during development of advanced materials and process tools. The transistor gate length whose control to specifications during IC fabrication is a primary determinant of manufacturing success, characterizes each generation of ICs. The ITRS projects the decrease of gate linewidth used in state-of-the-art IC manufacturing from present levels of up to 250 nm to below 90 nm within several years. Scanning electron microscopes (SEM) and other systems used for traditional linewidth metrology exhibit measurement uncertainties exceeding ITRS-specified tolerances for these applications. It is widely believed that these uncertainties can be at least partially managed through the use of reference materials with linewidth traceable to nanometer-level uncertainties. Until now, such reference materials have been unavailable because the technology needed for their fabrication and certification has not been available. It is also widely believed that the usefulness of SEM metrology for monitoring wafers in advanced development and production will become inadequate at some future IC generation. Thus, there exists a need for new methodology to meet future metrology requirements.

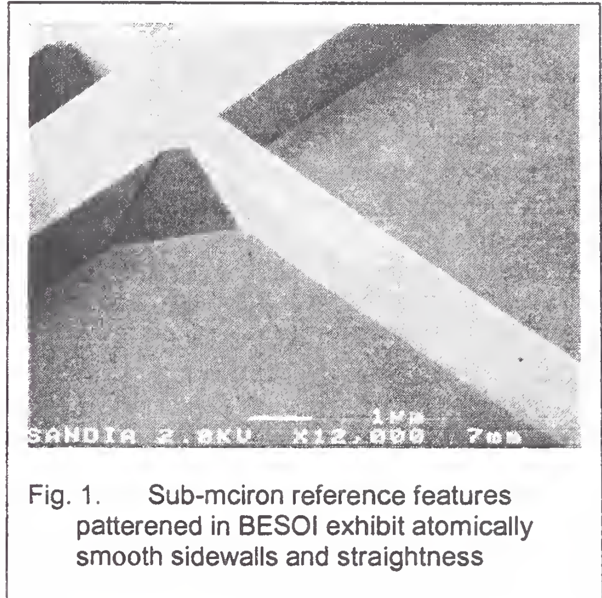

Fig. 1. Sub-mciron reference features patterened in BESOI exhibit atomically smooth sidewalls and straightness

Technical Strategy:

The Project staff has developed a procedure for fabricating linewidth and overlay reference materials. Patterning with lattice-plane selective etches of the kind used in silicon micromachining provides reference features with atomically planar sidewalls. Selection of bond and etch-back silicon-on-insulator (BESOI) starting material with (110) surface orientation that is thermo-mechanically bonded to a (100) handle wafer provides reference-feature-sidewall verticality with a built-in etch-stop facility. Similar results are generated with the use of Separation by Implantation of Oxygen (SIMOX) starting material. However, a bulk non-silicon-on-insulator (SOI) implementation would offer major cost advantages.

The traceability path for dimensional certification is provided by High Resolution Transmission Electron Microscopy (HRTEM) imaging. This method provides nanometer-level accuracy, but is sample-destructive and costly to implement. Our traceability strategy features the sub-nanometer

repeatability of electrical CD metrology as a secondary reference means. Whole-wafer electrical measurements are effectively calibrated with a few local HRTEM lattice-plane image counts. Typical reference features are several-thousand lattice planes wide. HRTEM lattice-plane image counts, require 3000 bpi digitization and specialized, proven image-analysis software. These are achieved by high-density digitization and numerical differentiation of the photographic record. Both Sandia National Laboratories and Los Alamos National Laboratory have collaborated in the development of this procedure.

The technical strategy has to be responsive to industry's requirement for reference materials to have the physical properties of standard 200 mm and 300-mm wafers. We dice each 150 mm wafer and mount the separate chips in micromachined standard 200 mm wafers to accommodate the test chips. The resulting finished units are user-friendly at an acceptable cost. The entire fabrication, assembly, and certification process is being transferred to a commercial standards vendor.

We also use this strategy for a class of overlay reference materials known as tool-induced shift extractors. The special requirement here is the replication of feature sets with different heights from the same photo-lithographic reticle. We have devised a way of doing this with a selection of standard CMOS fabrication steps. Linewidth reference materials must satisfy edge-definition sufficient to render width certification as meaningful. The fabrication and certification approach complies with this requirement. We have devised a method for fabricating the reference materials with suitable geometries and a method of certifying their widths at an acceptable cost. The next milestone is to perform electrical measurements and HRTEM on the same features and, through their correlation, to establish low-cost electrical linewidth metrology as a secondary reference means for the SOI implementation. The certification of tool-induced shift extractors will be expedited by the use of (110) handle wafers and (100) surface wafers, the inverse of that employed for the linewidth reference materials. This approach allows the use of HRTEM images of lattice planes to determine the pitches of line pairs.

On-reticle linewidth metrology is approached by extracting linewidths of control features electrically from test pads located outside the pellicle and therefore accessible to both the user and the supplier. These serve as a built-in reference for the calibration of the optical microscopes used by both parties. In this application, the < 2 nm repeatability and robustness of electrical metrology may have an advantage.

Accomplishments:

High-resolution transmission electron microscopy has revealed (111) lattice fringes spanning the entire width of a NIST [112] mono-crystalline linewidth reference feature patterned on (110) BESOI material. A preliminary lattice-plane count of the HRTEM image was made by inspection of a photographic print obtained by an optical microscope. Use of a drum scanner has demonstrated that the lattice-plane count can be fully automated. The width of the feature was determined to be 583 nm, with a combined standard uncertainty (coverage factor k = 2) of 2.5 nm. Standard 200 mm wafers were micromachined to serve as reference-material test-chip carriers. The fabrication process features three-step lithography and etching with thermal oxide and low-temperature nitride hard masking. A technique for mounting the reference-material test chips in the carriers was developed. Samples of the carriers were delivered to, and used by, all major semiconductor manufacturers.

In collaboration with Photronics Laboratories, Inc., we developed and fabricated electrical linewidth-control features for inspection of photo-mask reticles used in integrated-circuit manufacture. The design allows probe-card access to electrical test pads advantageously located outside the pellicle while uniquely providing for electrical testing of the process-replicated linewidth-control features at the wafer level. Tests are in progress.

A process for fabricating microstructures for calibrating optical-overlay metrology tools used in the manufacture of integrated circuits was developed. It features a unique combination of process steps extracted from CMOS processing, SOI, and silicon micromachining unit-processes. These structures have all the properties, such as atomically-planar feature side-walls, geometrical symmetry, material uniformity, and provisions for traceability, that are necessary for monitoring the fabrication of emerging generations of sub-tenth

micrometer integrated circuits. A unique fabrication process in which different layers of the microstructure are imaged at the same time from a single reticle enhances built-in overlay-vector traceability.

A new generation of Single-Crystal SOI Reference-Material test chips fabricated on BESOI starting material and having feature linewidths less than 200 nm was delivered to a consortium of 11 integrated-circuit manufacturers for evaluation. The distribution was accompanied by NIST electrical-linewidth measurements for the respective features. The consortium members returned their own measurements. The consortium's measurements track this Project's measurements, in most cases, to within less than 25 nm.

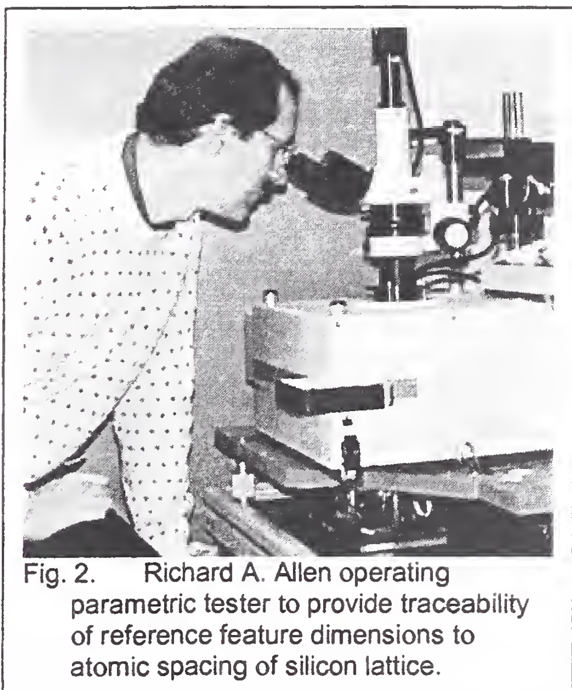

Fig. 2. Richard A. Allen operating parametric tester to provide traceability of reference feature dimensions to atomic spacing of silicon lattice.

The effective electrical linewidths of single-crystal linewidth reference features replicated on (100) BESOI substrates were modulated by dc biasing the handle wafer with respect to the cross-bridge resistor in which the reference feature was embedded. Both the sheet resistance and the electrical linewidths of the reference features closely tracked the predictions of theoretical models.

The use of off-lattice alignment of reference features to enable their replication with linewidths as narrow as 90 nm with a 0.5 μm lithography projection aligner was demonstrated. The results of this activity may enable the narrower features to be routinely replicated using an all-optical standard fabrication process.

A new test structure and CD measurement-processing algorithm for extracting dimensional information from copper-damascene interconnect features has been developed. The work was done in collaboration with a consortium of silicon-valley companies, including LSI Logic, Incorporated.

A bulk starting material implementation of single-crystal CD reference materials has been successfully demonstrated.

Future Plans:

During 2001, we plan to fabricate and certify Single-Crystal SOI Reference-Materials with linewidths traceable to silicon lattice counts with an uncertainty goal of less than 5 nm. Our 2002 goals are to demonstrate the fabrication and certification of overlay reference materials with uncertainties below the 5 nm level and extend the technology to pitch reference materials. By 2003, we will demonstrate electrical CD metrology as a means of providing on-reticle CD calibration.

Collaborations:

ISMT member companies (AMD, Compaq, Conexant, Hewlett-Packard, IBM, Intel, Lucent Technologies, Motorola, Texas Instruments, Hyundai, Infineon Technologies, Philips, STMicroelectronics, TSMC), development of single-crystal critical dimension reference materials (Michael W. Cresswell and Richard A. Allen)
ISMT, development of single-crystal critical dimension reference materials (Michael W. Cresswell and Richard A. Allen)

Solecon Laboratories, evaluating SOI substrates for reference materials (Michael W. Cresswell)

NIST Division 812, Performed focused ion beam (FIB) cut of silicon lines (Richard A. Allen and Wen F. Tseng)

Photronics Laboratories, development of optical/electrical hybrid critical dimension measurement for photomasks (Richard A. Allen and Michael W. Cresswell)

Sandia National Laboratories Microelectronics Development Laboratory, Sandia National Laboratories Compound Semiconductor Research

Laboratory, Sandia National Laboratories Integrated Materials Research Laboratory, Los Alamos National Laboratory, NIST Statistical Engineering, Precision Engineering Divisions, and ISMT, fabrication and certification of reference materials for linewidth and overlay metrology (Michael W. Cresswell, Loren W. Linholm, and Richard A. Allen)

Sandia National Laboratories, Statistical Engineering Division, Metallurgy Division, University of Central Florida, and Precision Engineering Division, ISMT, reference artifacts for critical dimension measurements (Michael W. Cresswell, Loren W. Linholm, and Richard A. Allen)

Scientific Computing Division, Hai Tang, assistance with ANSYS model of single crystal CD reference material project (Colleen H. Ellenwood)

Simplex Solutions, Inc., (and other companies listed on our ICMTS 2001 Proceedings paper) procedures and algorithms for CD extraction from electrical test structures having conformal coatings (Michael W. Cresswell)

University of Edinburgh, U.K., fabrication of test structures using buried-junction isolation VLSI Standards, development of single-crystal critical dimension and overlay reference materials (Michael W. Cresswell and Richard A. Allen)

VLSI Standards, Inc., and ISMT, development of commercial architecture and distribution plan for single-crystal CD reference materials (Michael W. Cresswell and Richard A. Allen)

Valtion Teknillinen Tutkimuskeskus (VTT), Technical Research Center of Finland, Electronics Division, P.O.B. 1101, FIN-02044 VTT, Finland

NIST Division 821, Mike Postek, CD-SEM/Electrical CD metrology

NIST Division 898, Will Guthrie, Traceability path for SC CD RMs

NIST Division 855, John Bonevich, HRTEM and CD SEM imaging.

Standards Committee Participation:

SEMI International Standards Electrical Metrology Test Structures Task Force, Co-Chair (Richard A. Allen)

SEMI International Standards Microlithography Committee, member (Richard A. Allen)

SEMI International Task-Force on X-Ray Lithography Mask Standard, Leader (Michael W. Cresswell)

Awards:

SEMI Certificate of Appreciation for Efforts and Support of SEMI International Standards Program (Richard A. Allen)

IEEE Fellow (Michael W. Cresswell)

Publications:

Allen, R. A., Linholm, L. W., Cresswell, M. W., and Ellenwood, C. H., A Novel Method for Fabricating CD Reference Materials with 100 nm Linewidths, 2000 International Conference on Microelectronic Test Structures, IEEE, pp. 21-24, 2000.

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Cresswell, M. W., Bonevich, J. E., Headley, T. J., Allen, R. A., Giannuzzi, L. A., Everist, S. C., Ghoshtagore, R. N., and Shea, P. J., Comparison of Electrical CD Measurements and Cross-Section Lattice-Plane Counts of Sub-Micrometer Features Replicated in (100) Silicon-on-Insulator Material, Proceedings of SPIE, Vol. 3998, pp. 74-83, Feb. 28 - Mar. 2, 2000.

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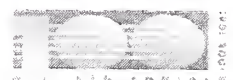

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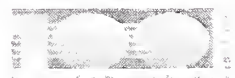
Cresswell, M.W.; Allen, R.A.; Murabito, C.E.; richter, C.A.; Gupta, A.; Linholm, L.W.; Pachura, D.; Bandix, P., Proceedings 2001, ICMT, March 12-16, 2001, Kobe, Japan.



Model-Based Dimensional Metrology

Technical Contacts:
J. S. Villarrubia, *A. E. Vladár, M. T. Postek*

"Physical metrology is challenged by the advancement of lithography capabilities and is not meeting required improvement for precision and reproducibility... Mask and wafer CD metrology tool resolution, accuracy, tool-to-tool matching, and reproducibility all require significant advancement if they are to meet the accelerating timing of the industry needs. Additionally, metrologists must learn how to effectively extract three-dimensional data from CD and overlay measurements to provide the maximum level of process control. **ITRS, p. 300 (1999).**

"CD measurements must account for sidewall shape." **ITRS, Table 81, "Metrology Difficult Challenges," p. 297 (1999).**

Objective:
To design and implement a provisional model-based shape-sensitive linewidth measurement system for an industrially relevant sub-500 nm sample.

Customer Needs:
A feature's width is one of its fundamental dimensional characteristics. Width measurement is important in a number of industries including the semiconductor electronics industry, which had more than $200 billion in worldwide sales in 2000.[1] As a measure of its importance in that industry, consider that the term "critical dimension" is used there nearly interchangeably with "linewidth" and semiconductor device generations are known according to the characteristic width of the features, as in "the 180 nm generation."

It is part of NIST's mission to provide SRMs and/or calibration services to meet the needs of U.S. industry. Presently, our only linewidth standards are optical photo-mask standards, the minimum linewidth of which is 0.5 μm combined expanded uncertainty of ≈37 nm (coverage factor 2). To support present and future semiconductor technologies, industry needs to measure sub-micrometer lines with total uncertainties, as identified by ISMT, of better than 10 nm and with measurement repeatabilities better than 2 nm. The magnetic recording and photographic industries have gap width and grain size measurement requirements at approximately the same scale. Neither NIST nor other national laboratories presently offer a linewidth measurement service or SRM with this level of accuracy.

A line's width must generally be determined from its image. However, the image is not an exact replica of the line. The scanning electron microscope (SEM), scanning probe microscope (SPM), and optical microscope all have image artifacts that are important at the relevant size scales. Physical linewidth determination therefore requires modeling of the probe/sample interaction in order to correct image artifacts and identify edge locations. Barriers to accurate linewidth determination include inadequate confidence in existing models, the complexity and consequent expense of using some models, inadequately quantified methods divergence, and ignorance of best measurement practices.

Technical Strategy:
The scope of the model-based linewidth metrology project includes the development and improvement of computational models to simulate the artifacts introduced by measuring instruments, inversion of these models (to the extent possible) to deduce the sample geometry that produced a measured image, validation of models by appropriate experiments, development and testing of measurement processes that provide the necessary inputs for model-based deduction of sample width and shape, estimation of uncertainties for the measurement process, assistance to industry linewidth measurement by communication of best practices, and laying of the necessary research groundwork for a future linewidth and/or line shape SRM.

NIST is uniquely positioned to execute such a project. NIST is a center of expertise in the instrument models to be tested, with the optical, SEM Monte Carlo, and SPM tip and sample reconstruction models all having been developed at NIST. Also, because NIST's standards function necessitates concern for accuracy, the NIST measurement tools are among the best characterized anywhere. For example, transmission optical

[1] Semiconductor Industry Association press release, Feb. 5, 2001.

measurements can be made here with the same instrument used to calibrate SRMs, and scale calibrations can be assisted by the NIST linescale interferometer.

In fiscal year 2001 our immediate goal is to implement and test data analysis procedures that will yield information on the shape and location of edges of polycrystalline silicon lines using top-down SEM images, the measurement configuration employed by industry CD-SEMs. The edge locations would tell us the line's width (the "CD" desired by industry). But lines with different sidewall geometries appear to have different widths when measured using algorithms that are standard today on CD-SEMs. That is, sidewall variation masquerades as width variation. Accordingly, we seek a model-based algorithm that explicitly accounts for the physics of the interaction of the electron beam with the sample and the effect of sidewall geometry. We plan to compare linewidth and line shape as determined by this method to cross sectional SEM images of the same lines.

Accomplishments:

We reported results from our previous year's study to ISMT directly (in the form of a project report that is accessible to member companies via the web). We reported them to the semiconductor metrology community and public generally via oral presentation at the SPIE Micrometrology Symposium and publication in the symposium proceedings. These were results of a linewidth measurement comparison between SEM and ECD (electrical critical dimension) on preferentially etched single crystal silicon lines on a thick insulating oxide. The single crystal nature of the sample and preferential etching were intended to produce samples of nearly ideal rectangular cross sectional shape in order to simplify the measurement problem. For our SEM linewidth measurement of the average linewidth between electrical taps, we reported 6 nm total uncertainty (coverage factor 3). This is within the current road map requirements.

This year we extended our study to measurements on polysilicon, a system that is more difficult due to the less ideal sample geometry, but which more closely resembles actual industry product. We used a Monte Carlo trajectory tracking method developed at NIST to calculate the expected SEM images for lines in polysilicon. The line edges were allowed to have varying sidewall angle and upper corner radius. The results were compiled into a database, or "library" of shapes and their corresponding images. (See Fig. 1.) We developed software that interpolates this library, and searches for the best match between the interpolated library and a measured image. In consultation with representatives of semiconductor manufacturers, we designed linewidth test patterns that ISMT printed for us in polysilicon on a thin gate oxide. We exercised our library matching method on these samples. This method has become the basis for our FY2001 activities (last paragraph of "Technical Strategy," above).

We reported results of an experimental test of blind reconstruction. Blind reconstruction is the name of a procedure we previously developed for determining the shape of an AFM (atomic force microscopy) or STM (scanning tunneling microscopy) tip by using the tip to image a "tip characterizer" sample. (It is important to know the tip shape in order to "deconvolve" it from images to obtain linewidths using these scanning probe microscopes.) The unique aspect of our method is that the detailed shape of the tip characterizer need not be known in advance in order to place limits on the tip shape. The difficulty with performing an independent experimental verification of blind reconstruction is the paucity of other trustworthy methods for measuring tip shapes. However there are special circumstances under which the SEM can provide an independent measurement. For those circumstances, we reported agreement between the methods to within experimental uncertainty.

We collaborated with a group in NIST's Building and Fire Research Laboratory and Dow Chemical on a project to use nanoindentation to measure mechanical properties of thin polymer films. This group asked us to apply our Blind Reconstruction technique to determine information they needed concerning the geometry of their nanoindentor tips. While this is not linewidth metrology (and was funded separately from this project) the activity nevertheless represents a "spin-off" application of methods originally developed by this project.

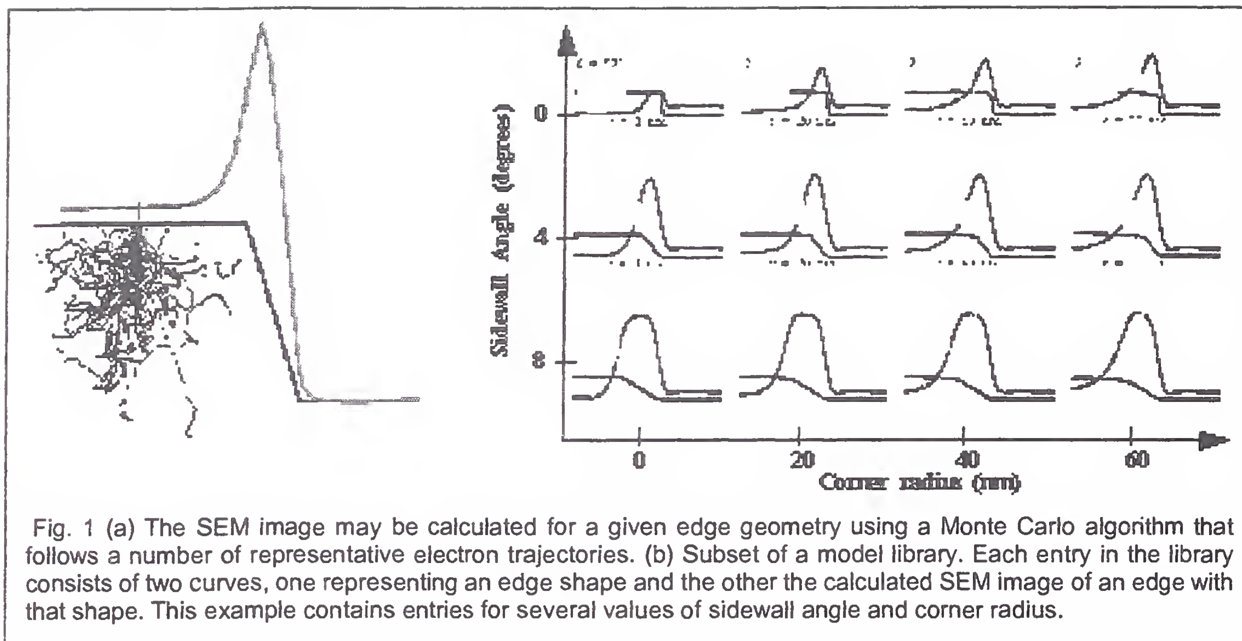


Fig. 1 (a) The SEM image may be calculated for a given edge geometry using a Monte Carlo algorithm that follows a number of representative electron trajectories. (b) Subset of a model library. Each entry in the library consists of two curves, one representing an edge shape and the other the calculated SEM image of an edge with that shape. This example contains entries for several values of sidewall angle and corner radius.

Future Plans:

Transfer measurement capabilities to industry by one or more of these methods: transfer of best measurement practices by publication, transfer of best measurement practices by collaboration with instrument suppliers to replace automated measurement algorithms with improved ones, work with ISMT to implement appropriate measurement procedures in their proposed "Reference Measurement System," issuance of appropriate Reference Material (RM) together with comparisons of measurements of those materials by NIST and industry, eventual issuance of standard reference material (SRM).

Collaborations:

The project maintains a CRADA with ISMT, which provides approximately 25 % of project funding and provides extensive feedback at semiannual meetings with member company representatives.

The project's scanning probe microscopy model was applied to nanoindentation of polymers in a collaboration with NIST's Building and Fire Research Laboratory and Dow Chemical.

External Recognition:

Commercial products based on Blind Reconstruction (the project's model for scanning probe microscopy) were announced this year by two companies (Applied Probes and Image Metrology).

Results of linewidth intercomparison on SIMOX were featured in the October *Quality* Magazine.

ISMT member representatives at Fall 1999 meeting of the Advanced Metrology Advisory Group gave the Project 100% of the possible score in the "results" category.

Invited presentation: "Intercomparison of SEM, AFM, and Electrical Linewidths," J. S. Villarrubia, Texas Instruments, Dallas, TX, 9/27/99.

Invited presentation: "Intercomparison of SEM, AFM, and Electrical Linewidths," J. S. Villarrubia, meeting of the Metropolitan Microscopy Society of New York, Thornwood, NY, 10/20/99.

Publications:

"Experimental Test of Blind Tip Reconstruction for Scanning Probe Microscopy," S. Dongmo, J. S. Villarrubia, S. N. Jones, T. B. Renegar, M. T. Postek, and J. F. Song, *Ultramicroscopy* **85**(3), pp. 141-153 (2000). (Also available at http://www.elsevier.nl/gej-ng/10/42/20/53/29/26/article.pdf).

"Linewidth Measurement Intercomparison on a BESOI Sample," J. S. Villarrubia, A. E. Vladár,

J. R. Lowney, M. T. Postek, R. A. Allen, M. W. Cresswell, and R. N. Ghoshtagore, Proc. SPIE **3998**, pp. 84-95 (2000).

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"Is a production critical scanning electron microscope linewidth standard possible?" M. T. Postek, A. E. Vladár, and J. S. Villarrubia, Proc. SPIE **3998**, pp.42-56 (2000).

"Applications of SEM Monte Carlo Modeling to Geometry Determination in Single-Crystal Silicon Test Patterns," J. S. Villarrubia, A. E. Vladár, J. R. Lowney, S. Jones, and M. T. Postek, Scanning **22**(2) pp. 108-109 (2000).

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"Recent Progress in Nanoscale Indentation of Polymers Using the AFM," M. R. VanLandingham, J. S. Villarrubia, and G. F. Meyers, *Proc. of the SEM IX International Congress on Experimental Mechanics,* Society for Engineering Mechanics, Bethel, CT, 2000, pp.912-915.

C. Thin Film and Shallow Junction Metrology Program

The dimensions of the active transistor areas are approaching the spacing between dopant atoms, the stochastic regime, complicating both modeling and doping gradient measurements. Thin dielectric and conducting films are approaching monolayer thicknesses.

As device dimensions continue to shrink, junctions and critical film thicknesses approach the realm of several atoms thick, challenging gradient, thickness and roughness metrology as well as electrical and reliability characteristics. The gate dielectric, traditionally SiO_2, will soon no longer be viable. The overall task is to provide suitable metrology and reference materials for thin dielectrics and conducting barrier films, including electrical characterization, gradient, thickness and roughness metrology and overall reliability metrology.

Two- and Three-Dimensional Profiling

Technical Contacts:

Joseph J. Kopanski, Jay F. Marchiando, David S. Simmons, Greg Gillen

"Two-Dimensional dopant profiling has been a highly ranked need in both the process integration and TCAD (simulation) sections of the National Technology Roadmap for Semiconductors (NTRS) since its inception."
Michael Duane, Advanced Micro Devices, *Characterization and Metrology for ULSI Technology*, D. Seiler, et. al., eds, A.I.P. Press 2000, p.715.

Objective:

To provide industry with the metrology infrastructure needed to measure two- and three-dimensional dopant/carrier profiles in the ultra-shallow junction regime. The project is divided into two thrusts (SIMS and SCM):

1) Improve the capabilities for compositional depth-profiling by defining optimum procedures for ultra-high depth resolution by Secondary Ion Mass Spectrometry (SIMS), developing depth-profiling reference materials needed by U.S. industry, and improving the uncertainty of implant dose measurements by SIMS.

2) Provide measurement methodologies, theoretical models, and data interpretation software necessary to make the Scanning Capacitance Microscope (SCM) a useful two-dimensional dopant-profiling tool.

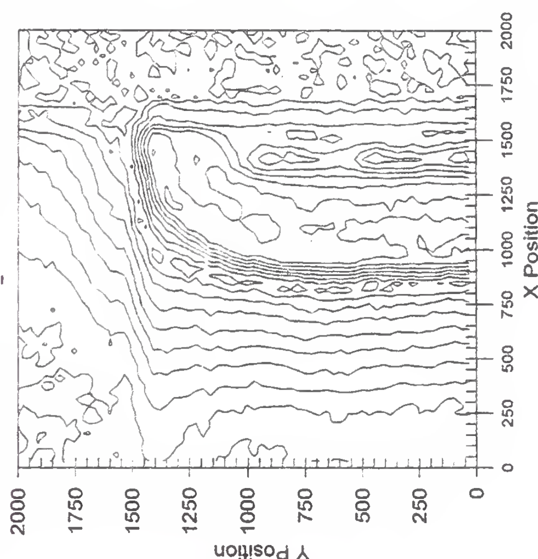
Customer Needs:

The 1999 SIA ITRS discusses the need for improved SIMS capabilities and development of two- and three-dimensional profiling techniques for measurements of ultrashallow dopant profiles and offline doping process control. Under Front End Processes, the need for thin-film reference materials is delineated, and, under Metrology, the increasing precision requirements for dopant concentration measurements are indicated. The Roadmap specifies requirements for at-line dopant profile concentration measurements improving from a spatial resolution of 3 nm and precision of 4 % in 2001 to 1.0 nm and 2 % in 2008.

SIMS is most likely to provide the solution to precision requirements for dopant concentration measurements. These goals can be achieved by careful control of SIMS depth-profiling conditions and by developing and making available implant reference materials for common dopant elements. Scanning Capacitance Microscopy (SCM) has emerged as a leading contender to provide 2-D carrier profiles. Relatively accurate two-dimensional profiles of the dopant concentration can be obtained when SCM images are combined with SIMS measurements.

Technical Strategy:

The SCM group is developing tools that are intended to enable scanning capacitance micro-



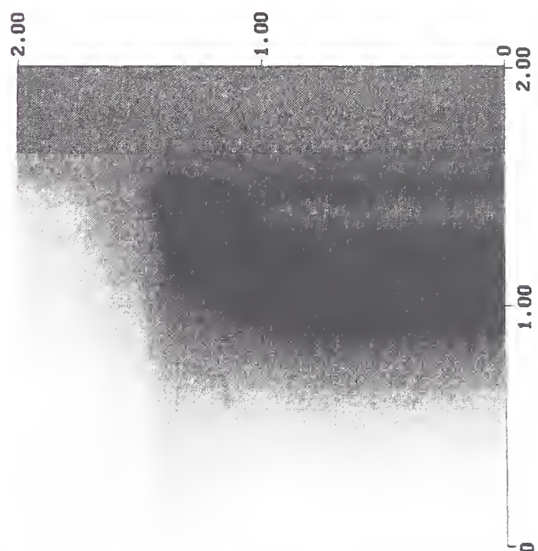


Fig. 1. SCM image of a p+/n junction

NIST
National Institute of Standards and Technology
Technology Administration, U.S. Department of Commerce

scopes to function as two-dimensional dopant profiling tools. This work is divided into four tasks: Task 1 is to develop SCM measurement methodologies. We are investigating low-temperature ozone-enhanced oxidation of silicon as a means of forming a high-quality oxide at least 5 nm thick and at temperatures less than 300 C. Current practice produces oxides that are 2 nm thick and result in SCM images that are subject to distortion due to tunneling. We are also investigating the effect of operating parameters of various commercial SCM sensors on the resulting 2-D dopant profiles. The theoretical models of SCM are validated by detailed comparison of experimental and calculated SCM signal over a range of measurement conditions.

Task 2 is to develop theoretical models of the SCM. We have previously developed a quasi-3-D model of the SCM that predicts the essential behavior of the SCM measurement. However, for the required dopant profiling performance goals, a more rigorous approach is necessary. Towards this end, the finite element method has been employed to solve Poisson's Equation for the SCM geometry in three-dimensions. Three-dimensional solutions for uniformly doped material have been employed to interpret SCM images. We are currently working towards extending the 3-D model to practically simulate rapidly varying dopant profiles, both with and without the presence of a p-n junction. Accuracy requirements may also force the consideration of quantum mechanical effects, necessitating the solution of the coupled Poisson and Schrödinger Equations. We have also begun investigating techniques to include the effect of the dopant gradient and curvature on the extracted dopant profile.

Task 3 is to use the theoretical models of the SCM to extract dopant profiles from SCM images. Task 4 is to transfer the NIST developed technology to industry. We have developed the ***FASTC2D*** software package for the interpretation of SCM images. Version one of ***FASTC2D*** and the accompanying comprehensive Users' Guide will be published this year.

The SIMS group is investigating the use of polyatomic primary ion beam species in commercial SIMS instruments to improve depth resolution for SIMS depth-profiling. Different sources have been developed for producing SF_5^+ or C_n^- beams. The sources are designed to attach to a commercial SIMS instrument, thus leveraging the high capital investment of the equipment. Standard reference materials certified for implanted doses of boron and arsenic have been released, and we are developing certification procedures for the implanted dose of phosphorus using radiochemical neutron activation analysis (RNAA). We are also developing and validating SIMS methods for measuring implanted doses of arsenic and phosphorus with a repeatability of better than 2 %.

Accomplishments:

The SCM group completed their ***FASTC2D*** version 1 code. ***FASTC2D*** extracts 2-D carrier profiles from SCM images of dopant gradients in silicon. Beta copies of this code were distributed to forty industrial users who are members of the ISMT working group on 2-D dopant profiling. The code can be obtained via the Internet at the Semiconductor Electronics Division's web site. User feedback and comments have been incorporated in the code.

NIST began collaboration with Los Alamos National Laboratories (LANL) to use their LaGriT (Los Alamos Gridding Toolkit) software package. LaGriT is a library of user callable tools that provide 3-D mesh generation, mesh optimization, and dynamic mesh maintenance for finite element methods. Access to such code will enable more efficient 3-D simulations of the SCM measurement across dopant gradients and p-n junctions. Dr. Jay Marchiando spent June, July, and August at LANL learning to use and applying LaGriT. During this time, a new vector nonlinear Poisson solver using LaGriT tools to manage the grid was developed. This should provide a substantial improvement over our original 3-D solver. Preliminary inverse solutions of SCM based on 2-D models were also demonstrated in FY-2000.

Initial study of low-temperature oxides on silicon for SCM samples was completed. Two processes, one thermal and one based on ozone, have been identified which produce oxides with 2 nm thickness and electrical properties suitable for SCM. More importantly, we have identified ozone, rather than UV light, as the significant catalyst for growth of a high quality oxide for SCM. A detailed study of ozone-enhanced oxide growth is underway.

From the SIMS group, SRM 2134, a reference material for arsenic implant dose in silicon, was released by NIST for public sale. The dose, certified by instrumental neutron activation analysis, has an expanded uncertainty of 0.38 %. The developers of this SRM were recognized with the 2000 Technical Achievement Award of the Chemical Science and Technology Laboratory at NIST. This SRM was used in a joint project between NIST and Lucent Technologies to demonstrate that SIMS could be used to distinguish 5 % relative dose differences for arsenic implants in silicon. Figure 2 shows results of an experiment in which each lab determined implant doses of 3 samples with 5 % dose differences. Both labs were able to determine the correct order of the implants. The source of a systematic difference of about 2.5 % between labs is being investigated. Work has progressed on understanding and reducing the sources of error in the RNAA measurement of phosphorus, especially in sample area and in blank correction. A project was initiated with ISMT to study improved methods for depth-profiling of thin ZrO_2 gate dielectric materials. Depth profiles conducted with the NIST SF_5^+ primary ion source demonstrated superior depth resolution and minimal artifacts compared to SIMS depth-profiling with more conventional Cs^+ or O_2^+ primary ion beams.

Future Plans:

The SCM group has begun developing a second generation of SCM data interpretation techniques that can account for the effect of the local dopant gradient and curvature. This requires a more comprehensive approach to dopant profile extraction, such as development of an inverse solution of the SCM modeling problem. An inverse solution of the SCM requires repeated solutions of the forward problem, i.e. calculation of the SCM signal from candidate carrier profiles. The candidate carrier profile is adjusted until a carrier profile is found that yields a calculated SCM signal that agrees with the measured SCM signal. We are developing improved 3-D Poisson solvers using the LaGriT grid management toolbox in collaboration with Los Alamos National Laboratories. Practical application requires finding shortcuts that will achieve the 3-D result without having to complete the entire round of 3-D simulations. The final goal is to implement a second version of the ***FASTC2D*** software that can rapidly approximate the dopant profile obtained through a detailed inverse solution.

We are also developing an additional tool for technology transfer: a new generation of test structures consisting of fully processed and partially processed transistors. These will eventually be produced in sufficient numbers so that every ***FASTC2D*** user can get a set. A round-robin set of measurements based on these structures and using an easy to implement measurement procedure, is planned, with devices to be distributed through the ISMT 2-D dopant profiling working group.

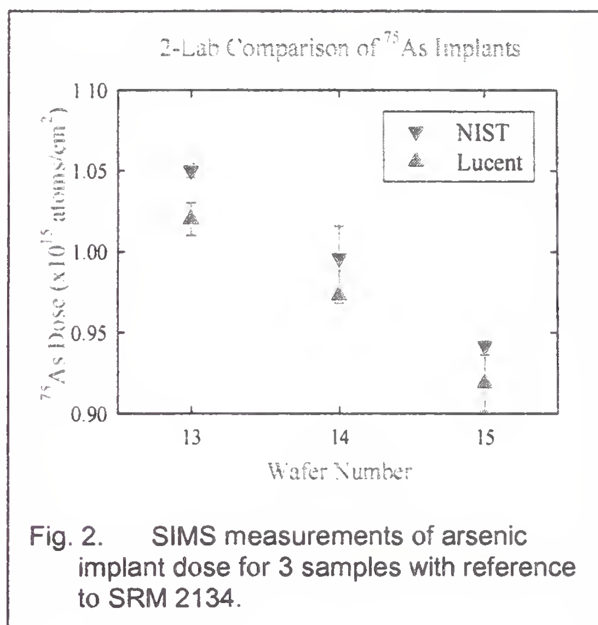


Fig. 2. SIMS measurements of arsenic implant dose for 3 samples with reference to SRM 2134.

The SIMS group intends to acquire new phosphorus implant material and to certify the dose by RNAA. We will determine SIMS protocols for good repeatability of phosphorus dose measurements and publish these results. We will determine the capabilities of dual-beam time-of-flight SIMS measurements for high depth resolution profiling of shallow implants. A low-cost modification to a standard SIMS ion source will be investigated for the capability of producing a usable SF_5^+ ion beam.

Collaborations:

Atolytics Inc, Paul Weiss – Phase II SBIR to develop a commercial version of their scanning microwave microscope

Howard University, Gary Harris – Application of SCM to high bandgap semiconductors.

ISMT, Joe Bennett.

Los Alamos National Laboratory, Denise George and Charles Snell – Development of next generation 3-D Poisson simulators using the LaGrit grid management toolbox.

Lucent Technologies, Fred Stevie.

Manufacturing Instrumentation Consultant Co – Phase I SBIR to develop co-axial shielded scanning probe microscope tips.

External Recognition:

INVITED REVIEW ARTICLE

J. J. Kopanski, Scanning Capacitance Microscopy, *to be published in The Encyclopedia of Imaging Science and Technology, John Wiley & Sons, (New York, 2001).*

Invited Talks:

D. Simons, Richard Lindstrom and Robert Greenberg, "Development and Certification of Ion-Implanted Arsenic in Silicon SRM for the Semiconductor Industry," CSTL Colloquium, NIST, September 14, 2000.

J. Kopanski, "Scanning Capacitance Microscopy for Measuring Device Carrier Profiles Beyond the 100 nm Generation", 2000 International Microprocesses and Nanotechnology Conference (MNC 2000), The Univ. of Tokyo, JAPAN, July 11-13, 2000.

G. Gillen, "Cluster and Polyatomic Primary Ion Beams for SIMS," Argonne National Lab, April 7, 2000.

G. Gillen, "SIMS Research at NIST," University of Illinois at Chicago, April 6, 2000.

J. Kopanski, "On Being the Best in the World at: Carrier Profiling of Ultra-Shallow Junctions with Scanning Capacitance Microscopy," NIST Director's Seminar Series on Being the Best in the World, NIST, Gaithersburg, MD, February 28, 2000.

G. Gillen, "Cluster SIMS - A New Approach for Surface Analysis," Best in the World Presentation, NIST, February 2, 2000.

J. Kopanski, "Improving the 2-D Carrier Profiling Capability of the Scanning Capacitance Microscope," SEMATECH Analytical Lab Managers Working Group Meeting, NIST, Gaithersburg, MD, December 9, 1999.

J. Kopanski, "Scanning Capacitance Microscope for Two-Dimensional Carrier Profiling of Semiconductor Devices," Analytical Chemistry Seminar Series, Pennsylvania State University, State College, PA, Oct. 5, 1999.

Publications:

P. H. Chi, D. S. Simons, F. A. Stevie, J. M. McKinley, and C. N. Granger, "High Precision Measurements of Arsenic Implantation Dose in Silicon by Secondary Ion Mass Spectrometry," in *Characterization and Metrology for ULSI Technology*, D. Seiler *et al.,* eds., A.I.P Press, 2000, pp. 682-686.

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G. Gillen, M. Walker, P. Thompson, and J. Bennett, "Use of an SF_5^+ Polyatomic Ion Beam for Ultrashallow Depth Profiling on an Ion Microscope Secondary Ion Mass Spectrometry Instrument," J. Vac. Sci. Technol. B18 (2000) 503-508.

G. Gillen, S. Roberson, A. Fahey, M. Walker, J. Bennett, and R. T. Lareau, "Cluster Primary Ion Beam Secondary Ion Mass Spectrometry for Semiconductor Characterization," in *Characterization and Metrology for ULSI Technology*, D. Seiler *et al.,* eds., A.I.P Press, 2000, pp. 687-691.

R. R. Greenberg, R. M. Lindstrom, and D. S. Simons, "Instrumental Neutron Activation Analysis for Certification of Ion-Implanted Arsenic in Silicon," J. Radioanalytical Nuc. Chem. 245 (2000), 57-63.

K. D. Hobart, P. E. Thompson, S. L. Rommel, T. E. Dillon, P. R. Berger, D. S. Simons and P. H.

Chi, "A 'p-on-n' Si Interband Tunnel Diode Grown by Molecular Beam Epitaxy," J. Vac. Sci. Technol. B 19 (2001) 290-293.

J. J. Kopanski, J. F. Marchiando, and B. G. Rennex, "Carrier Concentration Dependence of the Scanning Capacitance Microscopy Signal in the Vicinity of p-n Junctions," *J. Vac. Sci. Technol. B* 18(1), 409-413 (Jan/Feb 2000).

J. F. Marchiando, J. J. Kopanski, and J. Albers, "Limitations of the Calibration Curve Method for Determining Dopant Profiles from Scanning Capacitance Microscope Measurements," *J. Vac. Sci. Technol. B* 18(1), 414-417 (Jan/Feb 2000).

D. E. McBride, J. J. Kopanski, and B. J. Belzer, "Gate Oxide Formation under Mild Conditions for Scanning Capacitance Microscopy," in *Characterization and Metrology for ULSI Technology*, D. Seiler *et al.*, eds., A.I.P Press, 2000, pp. 657-661.

R. L. Paul and D. S. Simons, "Neutron Activation Analysis for Calibration of Phosphorus Implantation Dose," in *Characterization and Metrology for ULSI Technology*, D. Seiler *et al.*, eds., A.I.P Press, 2000, pp. 677-681.

G. Ramanath, J. E. Greene, I. Petrov, J. E. Baker, L. H. Allen, and G. Gillen, "Channeling-Induced Asymmetric Distortion of Depth Profiles from Polycrystalline- TiN/Ti/TiN(001) Trilayers During Secondary Ion Mass Spectrometry," J. Vac. Sci. Technol. B18 (2000) 1369-1374.

B. G. Rennex, J. J. Kopanski, and J. F. Marchiando, "*FASTC2D*: Software for Extracting 2D Carrier Profiles from Scanning Capacitance Microscopy Images," in *Characterization and Metrology for ULSI Technology*, D. Seiler *et al.*, eds., A.I.P Press, 2000, pp. 635-640.

P. E. Thompson, K. D. Hobart, M. E. Twigg, S. L. Rommel, N. Jin, P. R. Berger, R. Lake, A. C. Seabaugh, P. H. Chi and D. S. Simons, "Epitaxial Si-Based Tunnel Diodes," Thin Solid Films, 380 (2000)145-150.

Advanced Gate Dielectric Metrology Overview

As device dimensions continue to shrink, the gate dielectric approaches the realm of several atoms thick, challenging all aspects of metrology including composition and thickness measurements of the films and electrical and reliability measurements of MOS devices. Due to increased power consumption, intrinsic device reliability and circuit instabilities associated with SiO_2 of this thickness, a high dielectric constant gate dielectric (e.g., Si_3N_4, $HfSi_xO_y$, ZrO_2) with low leakage current and at least equivalent capacitance, performance, and reliability will be required. These alternate dielectrics bring a host of additional problems including thickness dependent properties, large trap densities, unknown physical properties, and lack of physical models.

The overall goal of this task is to provide suitable metrology, standards, and reference materials for advanced gate dielectrics. This will be accomplished through three interrelated and often complementary projects that offer a diverse approach to arriving at solutions to advanced gate dielectric metrology. The first project, Compositional Metrology for Next Generation Gate Stack Materials, provides compositional and dimensional metrology for advanced gate dielectrics by developing and characterizing numerous thin film characterization methods including grazing incidence x-ray photoelectron spectroscopy (GIXPS), non-linear optical spectroscopies (NLO), and high-resolution transmission electron microscopy (HRTEM). The second project, Thin Film Process Metrology, focuses on the issues of (1) relating optical, electrical, and physical measurements of thickness, composition, and interface structure, (2) identifying structural models and developing preferred optical index dispersion models or data for improved ellipsometric analysis of future-generation gate dielectric film systems and (3) developing and providing the basis for traceability to NIST for film thickness measurements. The third project, MOS Device Characterization and Reliability, provides electrical and reliability measurement techniques, data, physical models, and fundamental understanding for ultra-thin silicon dioxide and alternate gate dielectrics for future MOS devices. These three projects are described in detail in the descriptions to follow.

Advanced Gate Dielectrics – MOS Device Characterization and Reliability

Technical Contacts:

Eric M. Vogel and J. S. Suehle

"Standard electrical test methods for reliability of new materials, such as ultra-thin gate and capacitor dielectric materials, are not available. The wearout mechanism for new, high k gate and capacitor dielectric materials is unknown."**[ITRS, p. 297]** "...the development of the test equipment and protocols to characterize the electrical and reliability characteristics of the dielectric layer and its interfaces to silicon and gate electrode [are required" **[ITRS, p. 106]**

Objective:

To provide electrical and reliability measurement techniques, data, physical models, and fundamental understanding for ultra-thin silicon dioxide and alternate gate dielectrics in future MOS devices. To increase the understanding of the relationship between the gate dielectric material/interface properties and device electrical and reliability measurements.

Customer Needs:

The semiconductor industry association's (SIA) International Technology Roadmap for Semiconductors indicates that the equivalent thickness of the gate dielectric will need to be 1.0 nm to 1.5 nm by 2004. Due to increased power consumption, intrinsic device reliability and circuit instabilities associated with SiO_2 of this thickness, a high permitivity gate dielectric (e.g., Si_3N_4, $HfSi_xO_y$, ZrO_2) with low leakage current and at least equivalent capacitance, performance, and reliability will be required. The physics of failure and traditional reliability testing techniques must be reexamined for ultra-thin gate oxides that exhibit excessive tunneling currents and soft breakdown. Electrical characterization of Metal Oxide Semiconductor (MOS) capacitors and Field Effect Transistors (FET) has historically been used to determine device and gate dielectric properties such as insulator thickness, defect densities, mobility, substrate doping, bandgap, and reliability. Electrical and reliability characterization methodologies need to be developed and enhanced to address issues associated with both ultra-thin SiO_2 and alternate dielectrics including large leakage currents, quantum effects, and thickness dependent properties. As compared to SiO_2, very little is known about the physical or electrical properties of high dielectric constant gate dielectrics in MOS devices. The use of these films in CMOS technology requires a fundamental understanding of the relationship between the gate dielectric material/interface and device electrical and reliability measurements.

Technical Strategy:

The strategy of this effort will be to obtain or fabricate both device samples and blanket films, to perform reliability and electrical characterization of the devices, and to collaborate with other researchers to perform analytical characterization. Many issues such as tunnel/leakage current and spatially dependent properties associated with metal oxide and silicate dielectrics are also present in ultra-thin oxide and oxide-nitride stacked dielectrics. Therefore, many of the characterization schemes will first be developed on the simpler ultra-thin oxide and oxide-nitride dielectrics and then be applied to the metal oxide and silicate dielectrics.

There are two main focus areas for this project. The first focus area investigates the physics of failure and the reliability testing techniques for ultra-thin SiO_2 and high dielectric constant gate dielectrics. The physical mechanism responsible for "soft" or "quasi" breakdown modes in ultra-thin SiO_2 films and its implications for device reliability will be investigated as a function of test conditions and temperature. Long-term time-dependent-dielectric breakdown tests will be conducted on SiO_2 films as thin as 1.5 nm at electric fields close to operating conditions. These tests will be used to determine the thermal and electrical acceleration parameters of device breakdown. Experiments will be conducted to investigate the differences of gate oxide breakdown and wear-out due to high oxide field and hot-carrier injection. This study will provide insight into the physical mechanism of ultra-thin gate oxide wear-out and breakdown. The understanding generated in this research will be used to continue generating standard measurements through a NIST coordinated collaboration between EIA-JEDEC (Electronic Industries Association Joint Electron Device Engineering Council) and the American Society for Testing and Materials (ASTM). Studies on the reliability of high dielectric constant dielectrics such as oxide-nitride stacks will also be performed.

The second focus area is to investigate electrical measurement techniques, procedures and analysis associated with devices having thin oxide and alternate gate dielectrics. The electrical measurement techniques that we are investigating include capacitance-conductance characterization, dielectric tunnel and leakage current characterization and defect density measurements such as charge pumping and conductance. Furthermore, standard properties and mechanisms/correlations for these dielectrics including defect centers, dielectric constant, defect generation rates, and leakage/tunnel current will be characterized.

Accomplishments:

A systematic study of the uncertainties, sensitivity and limitations of capacitance and conductance measurements for extracting device properties and interface state density of metal-oxide-semiconductor (MOS) devices with ultra-thin (< 3.0 nm) oxides was completed. Capacitance and conductance characterization of metal-oxide-semiconductor (MOS) devices is used to determine properties such as oxide thickness, substrate doping and interface state density. However, with the advent of ultra-thin oxides, effects such as tunnel current, series resistance and quantum mechanical confinement in the substrate require additional consideration. This work provides a detailed analysis of the impact of these effects on parameter extraction using conductance and capacitance characterization of MOS devices with ultra-thin oxides.

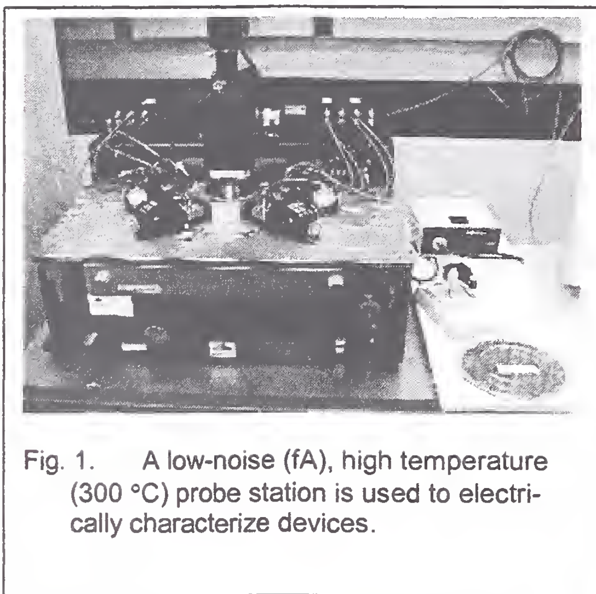

Fig. 1. A low-noise (fA), high temperature (300 °C) probe station is used to electrically characterize devices.

- Several extensive experimental investigations of the mechanisms responsible for defect generation and breakdown of thin silicon dioxide were performed. The results confirm that breakdown is directly related to the current passing through the dielectric. This confirms that the trap creation model based on energetic electrons creating damage and the statistical behavior of the number of defects at breakdown correctly describes the reliability of ultra-thin SiO_2 at both constant-voltage tunneling and substrate hot-electron conditions. Additional studies using substrate hot hole injection showed that holes are extremely effective in creating defects in the dielectric. However, these defects are ineffective in causing dielectric breakdown. These results shed doubt on the anode hole injection model for oxide breakdown.

- A detailed investigation of the reliability of various SiN_xO_y/SiO_2 (N/O) found that an N_2O anneal of a N/O stack results in device lifetime orders of magnitude greater than SiO_2 of the same equivalent oxide thickness. The results suggest that this lifetime improvement may be due to a high critical defect density at breakdown, low defect generation rate, and low leakage current of the N_2O-annealed stack. In collaboration with North Carolina State University, measurements and modeling were used to determine the impact of stacked dielectrics on charge-pumping measurements to determine interface and near interface defect densities.+

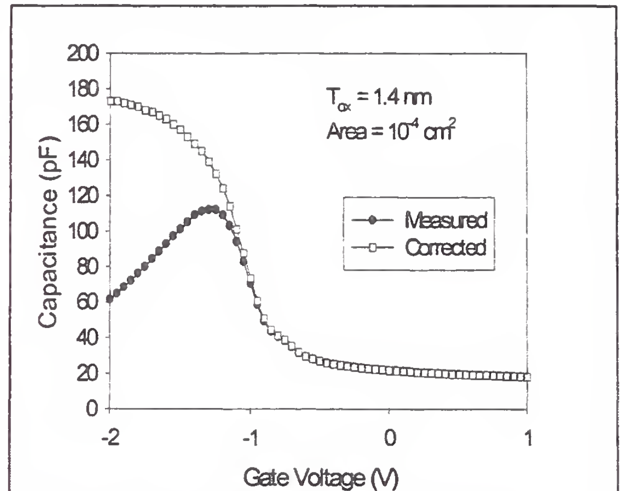

Fig. 2. Recent work has provided the methodology necessary to measure and correct the capacitance characteristics of MOS capacitors with "leaky" dielectrics.

■ A study was performed to investigate soft breakdown in ultra-thin silicon dioxide films and to investigate the temperature dependence of time-dependent dielectric breakdown. A more dramatic temperature dependence of wear-out was observed and raises serious reliability concerns. Thinner oxides and larger areas exhibited softer breakdown that requires the use of noise as the breakdown criteria. However, both hard breakdown and noise detection exhibited the same thermal activation. These tests provide critically important field acceleration parameters and thermal activation energies that are required for reliability extrapolation of ultra-thin oxides. Furthermore, the use of noise as a breakdown criterion was validated.

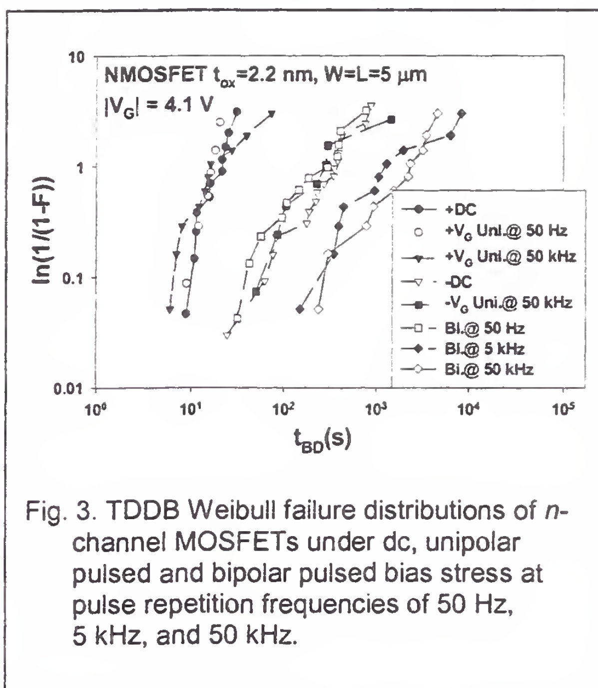

Fig. 3. TDDB Weibull failure distributions of *n*-channel MOSFETs under dc, unipolar pulsed and bipolar pulsed bias stress at pulse repetition frequencies of 50 Hz, 5 kHz, and 50 kHz.

■ The increased occurrence of soft breakdown in ultra-thin SiO_2 films makes reliability characterization very difficult and necessitates the development of more sophisticated techniques to detect breakdown. The effects of stress interruption on the time-dependent dielectric breakdown (TDDB) life distributions of 2.0 nm oxynitride gate dielectric films were studied. TDDB tests using two different breakdown detection techniques were conducted at several gate voltages. Additional tests were conducted using unipolar and bipolar pulsed bias with pulse repetition frequencies up to 100 kHz to study the effects of pulsed bias on the lifetime of 2 nm films. Our results show that: (1) stress interruption longer than 1 s does not affect the defect generation and TDDB life distributions, (2) both current noise and the increase in low-voltage stress-induced leakage current (SILC) detection techniques provide similar failure statistics for ultra-thin SiO_2, (3) TDDB lifetime for ultra-thin gate dielectrics under unipolar biased stress does not substantially depend on pulse repetition frequencies less than 1 MHz, and (4) lifetime under bipolar pulsed bias is significantly improved and exhibits a dependence on pulse repetition frequency.

■ A joint collaboration between NIST and JPL investigates what effect ionizing radiation experienced in deep space missions will have on the reliability of ultra-thin gate dielectrics. It has been previously reported that heavy ion bombardment can cause radiation-induced soft breakdown (RSB) in ultra-thin gate dielectrics. Heavy ion induced soft and hard breakdown were investigated in thin gate oxides ($t_{ox} \approx$ 3.0 nm) as a function of Linear Energy Transfer (LET), fluence, and voltage applied during irradiation. It is found that post-irradiation oxide conduction is well described by a quantum point contact model. This new work provides information about the physical nature of the soft breakdown path induced during irradiation and provides insight into the structure of the breakdown path in ultra-thin oxides induced under voltage stress.

Future Plans:

We will continue to develop reliability and electrical characterization techniques, data, physical models, and fundamental understanding for ultra-thin silicon dioxide and alternate gate dielectrics in future MOS devices. Our collaborations with standards committees will continue to develop standard reliability testing procedures. As industry and university researchers continue to narrow the selection and improve the electrical properties of high dielectric constant materials, our research characterization will continue to transition from ultra-thin silicon dioxide to these materials. An overview of the technological and scientific issues with these films will be performed to consolidate and focus our research efforts. Additional studies will be implemented to better correlate the electrical and physical/compositional properties of advanced gate dielectrics. Test structures will be fabricated to enhance the electrical and reliability characterization effort.

Collaborations:

AMD, George Washington University, Lucent, Motorola, North Carolina State University, ISMT, Texas Instruments, University of Delaware, University of Maryland

External Recognition:

E. M. Vogel, M. D. Edelstein, C. A. Richter, N. V. Nguyen, I. Levin, D. L. Kaiser, H. Wu, and J. B. Bernstein, "Issues in High-κ Gate Dielectrics for Future MOS Devices," Invited Talk, IEEE Microelectronics Reliability and Qualification Workshop, Glendale, CA, Oct. 31, 2000.

E. M. Vogel, "Reliability of Ultra-thin Silicon Dioxide for Future MOS Devices," Invited Talk, Penn State University, Dept. of Engineering Science, Oct. 4, 2000.

E. M. Vogel, 'High-κ Gate Dielectric Reliability – Issues in Characterization, Physical Modeling, and Assessment,' Invited Talk, Materials Research Society High-κ Gate Dielectric Workshop, New Orleans, LA, June 1-2, 2000.

J. Suehle, "Thin Gate Oxide Reliability Part I Physics, Statistics, and Models," Invited Talk, University of New Mexico Microelectronics Reliability Seminar Series, Albuquerque, NM, March 2, 2000.

J. Suehle, "Challenges in Reliability Characterization and Assessment of Sub-3nm Gate Oxides," Invited Talk, Reliability Engineering Seminar Series, College Park, MD, February 10, 2000.

J. S. Suehle, and E. M. Vogel, "Thin Gate Oxide Reliability," Invited Tutorial at International Reliability Physics Symposium, Apr. 10, 2000.

J. Suehle, "Challenges in Reliability Characterization and Assessment of Sub-3nm Gate Oxides," Invited Talk, Lucent Technologies, Orlando, FL, November 19, 1999.

E. M. Vogel, "Capacitance and Conductance Characterization of MOS Capacitors with Tunneling Gate Dielectrics," Invited Talk, SEMATECH Gate Stack Engineering Working Group Meeting, Raleigh, NC, November 11, 1999.

J. Suehle, "Challenges in Reliability Characterization and Assessment of Sub-3 nm Gate Oxides," Invited Talk, SRC Topical Research Conference on Reliability, Austin, TX, November 3, 1999.

E. M. Vogel, "Electrical Characterization and Reliability of MOS Devices with Tunneling Gate Dielectrics," Invited Talk, IBM, Yorktown Heights, NY, October 14, 1999.

John S. Suehle serves as secretary of the International Reliability Physics Symposium.

John S. Suehle serves on the technical program committee of the Integrated Reliability Workshop.

John S. Suehle serves as chairman of the Ultra-Thin Dielectric Reliability Technical Program for the Symposium on Plasma Process-Induced Damage (P2ID).

John S. Suehle serves as co-chair of the thin oxide section of the SRC Topical Research Conference on Reliability.

John S. Suehle serves as chairman of the JEDEC JC14.2 Dielectric Working Group.

E. M. Vogel serves on the ITRS FEP Thermal/Thin Film Technical Working Group.

E. M. Vogel co-organized the MRS Workshop on High-κ Gate Dielectrics, June 1, 2000.

E. M. Vogel serves on the technical program committee of the IEEE Semiconductor Interface Specialists Conference.

E. M. Vogel serves on the ISMT Reliability Engineering Working Group.

Publications:

E. M. Vogel, and V. Misra, 'MOS Device Characterization,' in *Handbook of Silicon Semiconductor Metrology*, Marcel-Dekker, ed. A. C. Diebold (in press).

J. S. Suehle, "Ultra-Thin Film Dielectric Reliability Characterization," Gate Dielectric Integrity: Material, Process, and Tool Qualification, ASTM STP 1382, D. C. Gupta and G. A. Brown. Eds., American Society for Testing and Materials, West Conshohocken, PA, 2000.

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H. Wu, E. M. Vogel, C. Weintraub, J. B. Bernstein, and J. S. Suehle, 'Reliability Study of SiN_xO_y/SiO_2 Stacks,' submitted *IEEE Elec. Dev. Lett.*

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J. S. Suehle, T. Myers, M. Edelstein, E. M. Vogel, and J. F. Conley, Jr., "The Effects of Ionizing Radiation on Wear-out and Reliability of Thin Gate Oxides," IEEE Microelectronics Reliability and Qualification Workshop, Glendale, CA, Oct. 31, 2000.

B. Wang, J. S. Suehle, E. M. Vogel, and J. B. Bernstein, "The Effect of Stress Interruption and Pulsed Bias Stress on Ultra-thin Gate Dielectric Reliability," 2000 IEEE International Integrated Reliability Workshop, Lake Tahoe, CA, Oct. 23-26, 2000.

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Advanced Gate Dielectric Metrology

Technical Contacts:

E. Steel and D. L. Kaiser

"New high κ transistor and capacitor dielectrics, new gate electrode materials, and new process flows require materials and electrical characterization and inline metrology development...Methods capable of characterizing and providing inline metrology for interface layers are required...Offline characterization of physical properties such as void content and size in porous low κ insulators, film adhesion, and mechanical properties, for example, is required for evaluation of new materials." ***- ITRS, 1999***

"Metrology metrics must go beyond precision specifications to include the total measurement uncertainty." **Kenneth Schroeder, Scott Ashkenaz, Matt Hankinson, KLA-Tencor Corp., Characterization and Metrology for ULSI Technology, D. Seiler, et al., eds, A.I.P. Press 2000, p. 38.**

Objective:

To develop and characterize microanalysis methods and test materials for thin film analysis. As films get thinner and devices get more complex, existing methods for the chemical and physical characterization of the films are being challenged. In this project electron, laser, and x-ray analysis methods are developed and applied to semiconductor thin films to understand the accuracy, precision, and uncertainty of the methods and the best analytical approaches for the semiconductor problem set. Test materials are manufactured internally or attained from external sources so that these measurement methods can be developed and characterized for materials that are of direct industry interest.

Customer Needs:

The microelectronics industry has a high demand for reliable thin film measurement methods that yield composition and dimension information with known accuracy and precision. The metrology section of the ITRS 1999 metrology section clearly states the needs for "reference materials and standard measurement methodology for new, high k gate and capacitor dielectrics with interface layers, thin films such as interconnect barrier and low k dielectric layers, and other process needs. Optical measurement of gate and capacitor dielectric averages over too large an area and needs to characterize interfacial layers. The same is true for measurement of barrier layers."

Technical Strategy:

Many of the existing and innovative analytical procedures for the analysis of thin films such as multiple voltage electron probe microanalysis (EPMA), x-ray photoelectron spectroscopy (XPS), non-linear optical spectroscopies (NLO), high resolution (HRTEM) and analytical electron microscopy (AEM) with x-ray and electron energy loss spectroscopies, low voltage scanning electron microscopy x-ray analysis, and Auger spectroscopy must be significantly improved to obtain accurate quantitative composition measurements on films with thicknesses below 10 nm. Our goals are to develop the necessary methods, analytical correction procedures, standard data and materials to determine realistically achievable accuracy levels for analysis of thin films by these techniques. Films for these measurement activities are obtained from industrial sources and fabricated in-house by spin coating metalorganic solutions. Current gate dielectric materials under investigation include silicon oxynitride, barium strontium titanate ($Ba_{1-x}Sr_xTiO_3$, BST), ZrO_2 and Zr silicates.

Vibrational spectroscopy is a powerful probe of chemical structure. Unfortunately, IR absorption studies of the development of a mature thin-film interface are impossible. The technique is sensitive to the *entire* film, and the film signal quickly overwhelms that of the interface structure. Second order nonlinear optical techniques such as second harmonic generation (SHG) and sum frequency generation (SFG) are symmetry forbidden in

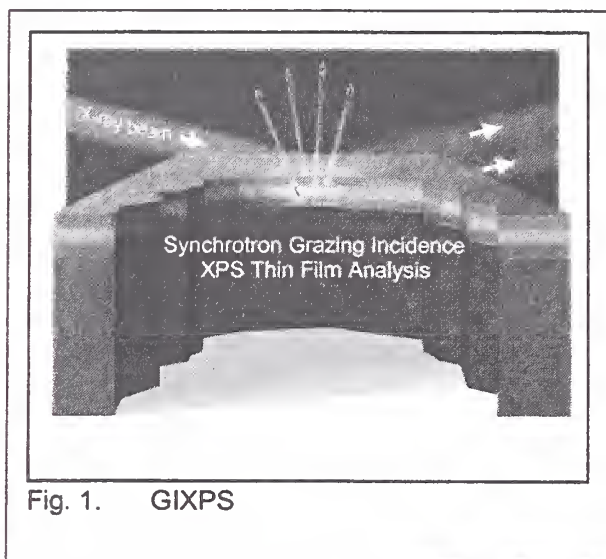

Fig. 1. GIXPS

centrosymmetric media such as bulk Si or SiO_2. Thus they are uniquely interface sensitive. SHG studies of SiO_2 films on Si have demonstrated empirical sensitivity to diverse properties of the interface, including strain, roughness, and midgap interface trap density. It is expected that properties such as interface roughness and midgap trap density will be correlated. We are investigating and developing nonlinear optical methods as probes of interfaces in semiconductor thin films.

Grazing incidence XPS (GIXPS) (fig. 1) allows both depth and chemical information to be attained from very thin (less than 10 nm) films. Using a NIST designed, built, and patented device on the Brookhaven synchrotron we have been developing the necessary instrumentation and data interpretation procedures to characterize ISMT silicon oxynitride films.

One of the more common methods of evaluating film thickness and composition is through the use of HRTEM and Analytical TEM, respectively. But the uncertainty of these approaches has only recently been looked at quantitatively. Films of dielectric materials grown on silicon were obtained from ISMT and analyzed to determine the accuracy of this HRTEM and AEM approach. Comparisons across many methods were made to determine the relative accuracy and precision of these approaches.

Recent Accomplishments:

A suite of projects involving electron, x-ray and laser beam inspection of thin films has been performed to develop new approaches and characterize existing techniques. Example accomplishments follow:

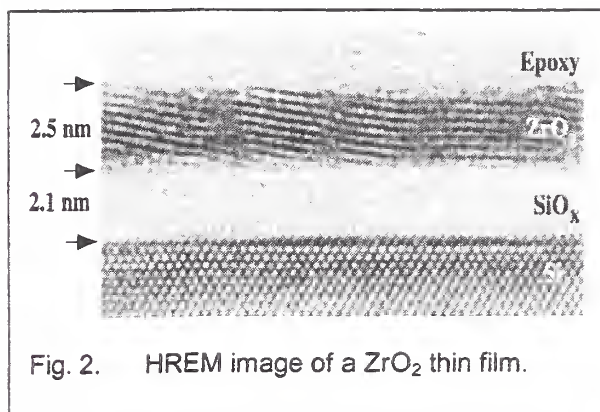

Fig. 2. HREM image of a ZrO_2 thin film.

- Test materials and method accuracy: A series of highly-stoichiometric BST thin films with thicknesses down to 6 nm was measured by EPMA; refinement of the analysis and correction procedures yielded an improved measurement precision of less than 2% relative for each element. We developed HRTEM quantitative image analysis approaches for measuring gate oxide thickness including two dimensional magnification calibration and uncertainty estimation, and compared the precision and accuracy of these HRTEM methods for thin film thickness metrology with other methods and industry labs. In collaboration with ISMT, we determined the extent of Zr diffusion by SIMS and analytical electron microscopy on a Zr silicate test sample. To provide test specimens for metrology studies, we developed spin coating procedures to fabricate smooth, uniform BST and ZrO_2 films with thicknesses below 3 nm.

- Nonlinear Optics: Procedures were developed to isolate the contributions to a vibrationally-resonant sum-frequency generation (VR-SFG) spectrum from the top and bottom interfaces of a single thin film on a semiconductor substrate. The procedures were successfully applied to the study of the free surface of a polystyrene test-film on Si. This work was the first to establish the complete orientational distribution for a pendant side group at a polymer surface. In the second half of 2000, the procedures were generalized to the analysis of multi-layer film stacks. They are being successfully applied to the study of the buried interface between polystyrene and a spin-on low-K dielectric, allowing molecular level insights into polymer/glass adhesion.

- Thickness and composition measurement: Methods of determining the thickness and composition of gate dielectric materials for CMOS devices on silicon run into difficulties when the total layer thickness is less than 100 nm. This problem becomes crucial in cases of the most advanced gate dielectrics which are grown as heterogeneous layers. A recent measurement by six techniques of silicon oxynitride samples circulated by ISMT pointed to variations between the total measured thickness of the order of 50% (see Figure 3). There are at least four reasons for this: 1) physical limitations in the accuracy of the methods on this fine scale, 2) accuracy of the

physical quantities which are the inputs for the methods, 3) diffusion in the layers, and 4) lack of detailed knowledge of the physical-chemical structure of the materials. The method of grazing incidence x-ray photoelectron spectroscopy (GIXPS), as developed at the NIST synchrotron radiation beamline X-24A at Brookhaven National Laboratory is highly suitable for analyzing the complex heterogeneous layers in the gate dielectric materials. The x-ray photoemission provides chemical analysis of the elements present in the layers, and the behavior of the x-ray fields at grazing incidence provide thickness information. Seven samples from ISMT that had been measured by other techniques were measured and analyzed. We performed analyses to estimate the variation in results expected due to inaccuracies of the published physical parameters that go into fitting the data. GIXPS fits of samples indicate the formation of an unexpected variation in the position of the nitride layer.

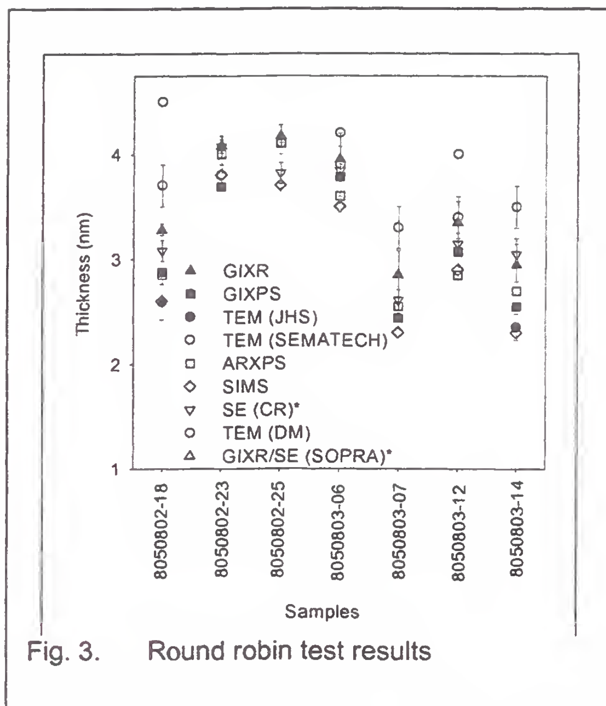

Fig. 3. Round robin test results

- Next generation analytical SEM/Auger system: NIST recently procured and installed a state-of-the-art field emission gun scanning Auger microscope. This system has the ultra-high vacuum necessary to evaluate ultra-thin films. We have worked with the manufacturers to develop this unique instrument capable of very low voltage performance, high spatial resolution, and simultaneous, high precision electron and x-ray measurements with both energy and wavelength dispersive x-ray detectors and a high-resolution electron spectrometer.

- Next generation x-ray detectors: This project is aiding the development of the high energy resolution x-ray microcalorimeter and the high efficiency and count-rate silicon drift detectors by testing the capabilities and applying the x-ray technology to chemical metrology semiconductor analytical problems. We are active collaborators (see publication list) with the Boulder, NIST developers of the microcalorimeter to develop it as a chemical metrology tool. Also, we are working through the NIST SBIR program with Photon Imaging, Inc. to encourage the development of a high collection angle, megahertz count-rate, near room temperature silicon drift x-ray detector.

- Ultrathin films of silicon dioxide (SiO_2) and silicon oxynitride (SiO_xN_y) on silicon substrates are used widely in the semiconductor industry as gate dielectrics in transistors. Gate oxide fabrication tools produce films with a tolerance of less than 0.3 nm, and require metrology tools with a precision of better than 0.1 nm. To evaluate HRTEM as a thickness measurement technique, blanket films of dielectric grown on silicon were obtained from ISMT. TEM samples were prepared in cross section by mechanical dimpling and ion milling. High resolution micrographs were acquired at 300 keV using a CCD camera (Figure 4, top). Digital image processing was used to calibrate the magnification (using the silicon substrate as an internal standard), identify the dielectric film boundaries, and extract the film thicknesses. New methods were developed for obtaining 2-dimensional calibration information from a lattice image of the silicon substrate. The spacings between atomic planes could be measured with sub-pixel accuracy by locating peaks using a weighted center-of-mass algorithm (Figure 4, bottom), followed by a least-squares fit of lattice basis vectors. The film/substrate interface was located using integrated intensity profiles. Films nominally 2 nm thick were measured with an estimated reproducibility of 0.2 nm.

- Standard data for thin film analysis by Auger and XPS: Three databases are now available for AES and XPS applications, and the development of another has commenced. Version 1.0 of the X-Ray Photoelectron Spectroscopy database (SRD 20) was released in 1989, and version 2.0 was released in 1997. Version 1.0 of the Electron Inelastic-Mean-Free-Path Database (SRD 71) was released in September, 1999. Version 2.0 of the Elastic-Electron-Scattering Cross-Section Database (SRD 64) was released in 2000. Work has commenced on a new database to be used for AES and XPS analyses of materials with complex morphologies. SRD 64 and SRD 71 will be combined with additional data to enable comparisons of measured and simulated spectra for particular specimen morphologies and specified analytical conditions. These are freely available through the NIST Standard Reference Data Program.

Future Plans:

We will continue to develop methods, materials and data and characterize the accuracy of measurement methods for chemical composition of nanoscale films found in gate dielectrics. Current metrology approaches (EPMA, Auger, AEM, GIXPS, NLO, NSOM, next generation X-ray detectors, and Standard Reference Data) will be further developed and critically applied to semiconductor thin film analysis problems. As a new effort, we will investigate the feasibility of direct measurement of the dielectric constant using EELS with nanometer spatial resolution; if feasible, thin dielectric films will be measured and the results compared with optical methods and scanned evanescent probe approaches. We will determine the accuracy achievable by TEM in determining gate thickness, leveraging work from John Mardinly et al. at Intel. Ultrathin (< 5nm) films of ZrO_2 and $ZrSiO_4$ will be fabricated by spin-coating for use as test vehicles for metrology studies; the compositional homogeneity, microstructure and electrical properties of these films will be characterized. We will explore potential new mechanisms for transferring thin film reference materials to industry.

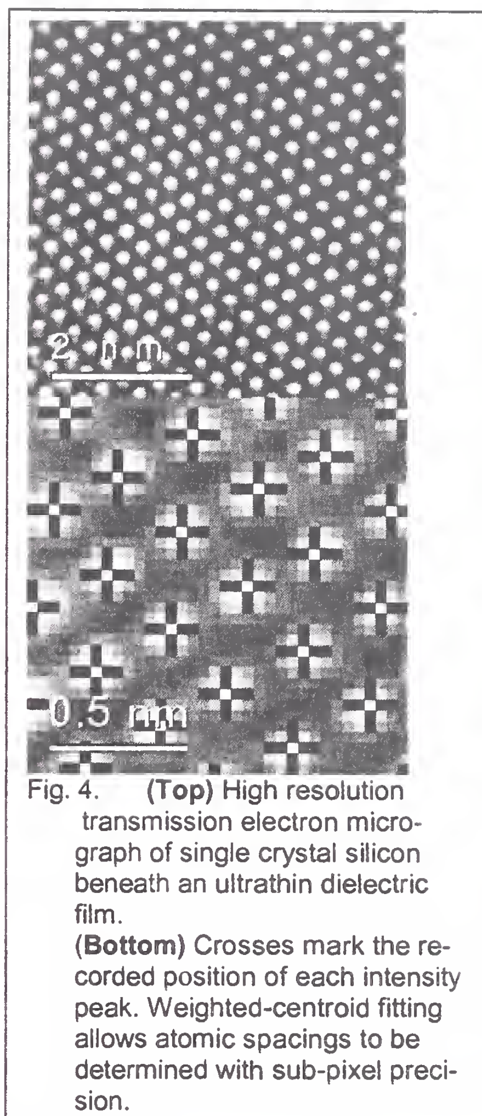

Fig. 4. **(Top)** High resolution transmission electron micrograph of single crystal silicon beneath an ultrathin dielectric film.
(Bottom) Crosses mark the recorded position of each intensity peak. Weighted-centroid fitting allows atomic spacings to be determined with sub-pixel precision.

Collaborations:

ISMT, University of Maryland, Lucent.

External Recognition:

Armstrong, J.T., "***Improving Analytical Accuracy in the Analysis Particles by Employing Low Voltage Analysis***," Microscopy and Microanalysis 2000 Conference, Philadelphia, PA, August 17, 2000. Invited

Bright, D.S., "***PC/Mac Image Processing Freeware for Examining Spectral Images***," Microscopy and Microanalysis 2000 Conference, Philadelphia, PA, August 17, 2000. Invited

Jach, T., "***Grazing Incidence X-Ray Photoemission Spectroscopy of Semiconductor Insulating Layers,***" 1999 X-Ray Group Meeting, Advanced

Photon Source, Argonne National Laboratory, Argonne, IL, October 25, 1999. Invited

Jach, T., "***Grazing Incidence X-Ray Photoemission Spectroscopy-A Method to Study Gate Dielectric Films on Si***," American Vacuum Society Regional Meeting, Purdue University, West Lafayette, IN, May 9, 2000. Invited

Newbury, D.E., "***The Approaching Revolution in X-Ray Spectrometry for Materials Characterization***," Department of Materials Science and Engineering, Pennsylvania State University, State College, PA, February 22, 2000. Invited.

Newbury, D.E., "***Revolutionary Advances in X-Ray Spectrometry***," Appalachian Regional Microscopy Society, Raleigh, NC, March 30, 2000. Invited.

Newbury, D.E., "***Spectral Simulation with NIST-NIH Desktop Spectrum Analyzer (DTSA): A Critical Tool for Estimating Limits of Detection***," Microscopy and Microanalysis 2000 Conference, Philadelphia, PA, August 15, 2000. Invited.

Powell, C.J., "***Recent Progress and Remaining Problems in Quantitative Surface Analysis by Auger-Electron Spectroscopy and X-Ray Photoelectron Spectroscopy***," Annual Symposium of the Florida Chapter of the American Vacuum Society, Orlando, FL, March 13, 2000. Invited.

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List of Other Presentations:

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Powell, C.J., "***The NIST X-Ray Photoelectron Spectroscopy Database***," 8th Topical Conference on Quantitative Surface Analysis, Puyallup, WA, October 22, 1999.

Powell, C.J., "***Relationships Between Parameters Describing Inelastic Electron Scattering in Solids***," American Vacuum Society International Symposium, Seattle, WA, October 27, 1999.

Powell, C.J., "***International Interlaboratory Comparison of Silicon Dioxide Film Thicknesses Measured by Different Techniques***," ISMT Analytical Laboratory Managers Council Meeting, Austin, TX, September 7, 2000.

Scott, J.H., "***Chemical and Structural Characterization of Ultrathin Dielectric Films Using Analytical Electron Microscopy***," Material Research Society Meeting, Boston, MA, November 29, 1999.

Scott, J.H., ***Silicon Oxynitride Film Thickness Measurements Using High Resolution Transmission Electron Microscopy and Grazing Incidence X-Ray Photoelectron Spectroscopy (GIXPS)***," Microscopy and Microanalysis 2000, Philadelphia, PA, August 15, 2000.

Small, J.A., "***Comparison of High- and Low-Voltage X-Ray Mapping of an Electronic Device***," International Conference on Characterization and Metrology for Ultra Large Scale Integration Technology, NIST, Gaithersburg, MD, June 28, 2000.

Thin Film Process Metrology

Technical Contacts:

J.R. Ehrstein, C.A Richter, N.V. Nguyen

New high-K transistor and capacitor dielectrics, and new process flows require materials and electrical characterization and inline metrology development. Near term metrology development will focus on extension of ellipsometry and electrical (C-V and I-V) methods to sub-2nm oxides and nitrogen-containing oxides....Potential solutions include ellipsometry in the ultra-violet wavelength range. Methods capable of providing in-line metrology for interface layers are required. (ITRS 1999)

Objective:

Develop new and improved electrical and optical measurements, models, data, and reference materials to enable better and more accurate measurements of select critical silicon CMOS-technology thin-film parameters. Major focus is placed on requirements for silicon dioxide, oxynitrides, and high-k (dielectric constant) gate stacks for advanced gate dielectrics detailed in the 1999 ITRS.

Customer Needs:

The evolving decrease of the gate dielectric film thickness to an oxide-equivalent value of 1 nm is identified as a critical front-end technology issue in the 1999 ITRS. For effective (oxide- equivalent) gate dielectric thicknesses below about 2.0 nm, SiO_2 is expected to be replaced, initially by oxynitrides or dielectric stacks utilizing silicon oxides and nitrides, and then by either metal oxides or silicates generally requiring one or two monolayers of additional interface dielectric. Process tolerance requirements for dielectric thickness are projected to be ±4 % (3σ), which translates to less than 0.1 nm for 2 nm films. Requirements for process control measurements are a factor of ten smaller still.

Spectroscopic ellipsometry (SE) is expected to continue as the preferred measurement for process monitoring of future gate dielectric films. Industry metrology needs include not only improved methods to accurately determine film thickness, but also: (1) techniques to determine the structure of the individual films and the interfaces between them, (2) an improved understanding of the relationship between physical, electrical, and optical determinations of film properties, and (3) mechanisms for traceability to NIST (such as reference materials) to support film metrology.

In order for SE to meet process control requirements of film thickness and unambiguously determine film composition and morphology, the optical properties of these advanced dielectric film systems must be thoroughly studied and well characterized.

Technical Strategy:

This project focuses on (1) relating optical, electrical, and physical measurements of thickness, composition, and interface structure, (2) identifying structural models and developing preferred optical index dispersion models or data for ellipsometric analysis of future-generation gate dielectric films, and (3) establishing the basis for accuracy of industrial film thickness measurements through traceability to NIST.

Relation of optical, electrical and physical measurements of thickness - Through collaborations with ISMT, IC industry companies, SRC university staff, and key researchers in other parts of NIST, project staff are leading and participating in a number of electrical, optical and physical method comparison studies of ultra thin gate dielectric films. The results of these studies improve the general understanding of state of the art (SOA) measurement capability for very thin

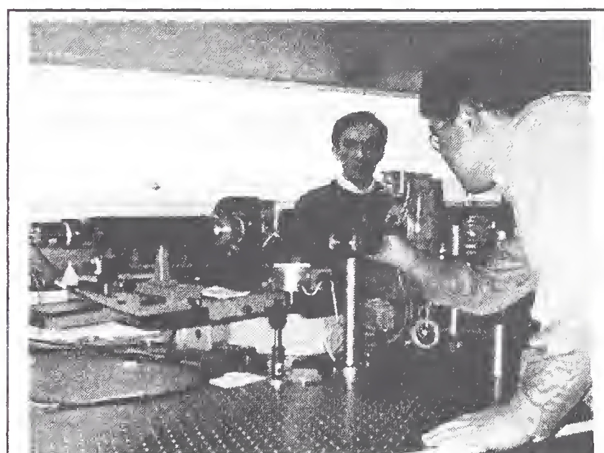


Fig. 1. Project scientists align gate dielectric specimen on spectroscopic ellipsometer.

films, and allow project staff to assess the results of various optical models being applied to the analysis of these films. SOA C-V and I-V measurement capability has been established for gate films. Advanced QM-based analysis software from commercial, and university sources has been implemented and benchmarked to determine the resulting differences in film thickness values calculated from C-V and I-V data

Structural and optical models for ellipsometry
Project staff is optically characterizing advanced oxynitrides and high-k films such as zirconium oxide and hafnium silicate. A custom, high-accuracy, spectroscopic ellipsometer with a spectral range of 1.5 eV to 6 eV is being used. Characterization will also be extended to 8.5 eV to include important optical index structure of these films beyond their bandgaps. Emphasis is on determining preferred structural models, and optical dispersion functions for each of these film systems, and the variability of these parameters due to differences in film fabrication processes. Analysis is done with NIST-developed software for spectroscopic ellipsometry; which allows maximum flexibility for addition of the latest published or custom-developed optical response models as appropriate for each material system investigated.

Establish and transfer basis of accuracy for thin dielectric films - Core ellipsometry measurement capability is being expanded and strengthened to meet industry needs for future thin dielectric film optical measurements and calibration standards as identified at a previous NIST-sponsored workshop. An investigation has been started into cleaning and recontamination issues for film calibration standards to determine whether a workshop-expressed goal of 0.015 nm long-term reproducibility of reference artifact values is obtainable. Procedures are being developed to enable traceability to NIST for suppliers of secondary thin-film reference materials without volume production of NIST SRMs.

Accomplishments:
Verified, using a specially prepared set of nominal 10 nm thick Ta_2O_5 (high-κ) films that were annealed in 50 °C intervals from 650 °C to 950 °C (RTA in nitrogen), the evolution of secondary structure in the real and imaginary parts of the dielectric function of the film. This structure, which begins to appear for samples that are annealed at temperatures above 700 °C, is most strongly manifested in major, at 4.7 eV, and minor, at 5.1 eV, peaks in the real part of the dielectric function. This structure in the dielectric function is attributed to the formation of a crystalline phase in the films when annealed at the higher temperatures, as recently reported in the literature. In addition, Project scientists found that the real and imaginary parts of the dielectric function decrease in magnitude as anneal temperature increased above 750 °C. Such a decrease, which normally is associated with a decrease in the density of a material, was found to correlate with AFM-determined surface roughness and pinholes. Thus, features of the optical dielectric function, which serve as rapid indicators of both crystalline

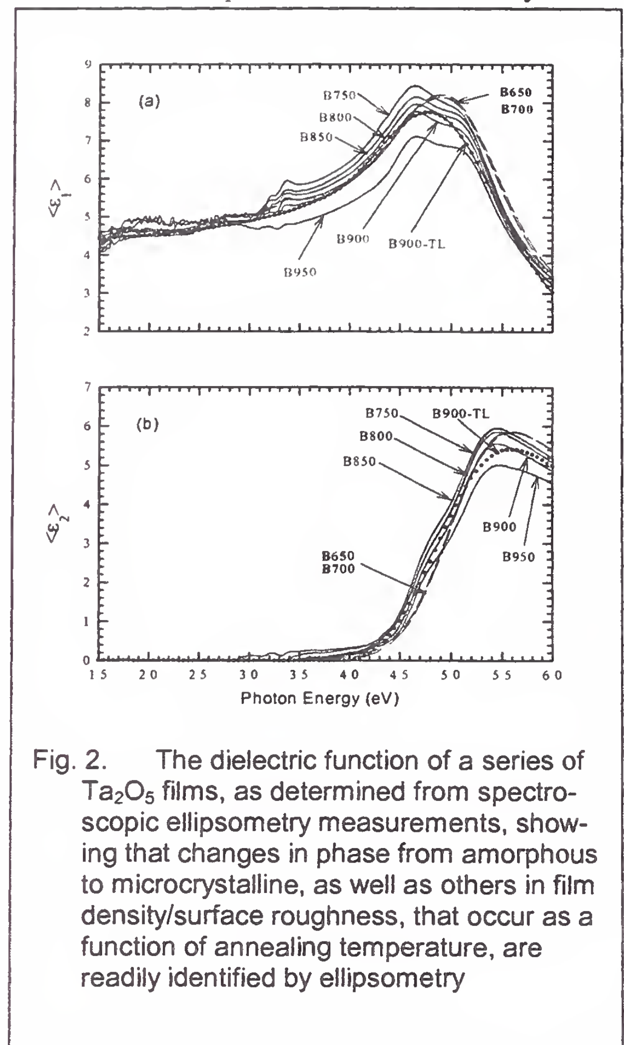


Fig. 2. The dielectric function of a series of Ta_2O_5 films, as determined from spectroscopic ellipsometry measurements, showing that changes in phase from amorphous to microcrystalline, as well as others in film density/surface roughness, that occur as a function of annealing temperature, are readily identified by ellipsometry

regions in the film as well as surface porosity, without the need to resort to TEM, have been confirmed.

Completed data acquisition from a multi-laboratory study of the thickness of two very thin SiO_2 films using spectroscopic ellipsometry, X-ray and neutron reflectivity, and C-V measurements. A thermal desorption cleaning process was developed to remove surface contaminants and was required just prior to measurement for all participating laboratories. Lab-to-lab differences in thickness values, both between and within different types of measurements, were larger than expected. Diagnostic work to understand these differences will include study of the effects of different modeling assumptions on the thickness values and the return of all samples to NIST for testing of the robustness of the recommended cleaning procedure and also of the thickness equivalence of all test samples as measured on a single instrument.

Demonstrated that the complementary manner in which the increased dielectric constant of high-κ gate dielectric materials affect the measurement of their electrical and optical properties may be leverageable to extract additional materials properties during characterization. The increased dielectric constant that is required of dielectric materials for replacement of SiO_2 as the MOS gate insulator has the effect of making them electrically thinner but optically thicker than a SiO_2 film of the same physical thickness. This property was shown to have the potential of enabling increased information to be obtained from the characterization of both oxynitride films and high-κ films such as metal oxides deposited over an SiO_2-like interface layer when electrical and optical analysis is used in tandem. In the case of single-layer oxynitride films, it may be possible to extract the fraction of the total film composition that is comprised of silicon nitride. In the case of films such as metal oxides over lower-κ, SiO_2-like, interface layers, the interface layer is relatively undetectable by optical measurements such as ellipsometry, whose response is dominated by the thickness and index of the high-κ film. However, C-V characterization of such a film stack is dominated by the low-κ interface layer; thus a combined electrical-optical analysis of such films may enable the determination of the thickness of both the interface and the high-κ component films.

Completed the 1-D comparison of six different sets of university and commercial sector software capable of accounting for polysilicon depletion and quantum mechanical effects in the substrate that obscure the determination of thickness of thin dielectric films from C-V and I-V measurements. A model structure consisting of a capacitor having several levels each of gate oxide thickness, gate poly-silicon doping, and substrate doping was used for the comparison. The results of the simulations, which were done from –5 V to 5 V, showed that the overall shape of the C-V curves were in generally good agreement. This instills confidence in their overall capability, particularly since very different fundamentals were generally incorporated in their development. Small differences in flatband and threshold values in one case were attributed to differences in default values for material properties. The largest differences among the software sets were in the accumulation capacitance, which is used for the electrical determination of the gate dielectric thickness. This resulted in thickness differences ranging from 0.17 nm for a nominal 3 nm film to 0.25 nm for a 1 nm film. These results demonstrate the effect of the choice of simulator when determining the effective electrical thickness of advanced gate materials and also the importance of knowing the details of the software used when comparing and interpreting reported results from different research teams.

Improved the statistical analysis procedures for Weak Localization measurements to improve the reliability with which interface roughness values at the 0.1 nm level can be extracted.

Future Plans:

Research on the relation between electrical, optical and physical measurement of dielectric film thickness will focus on improved understanding of the accuracy of QM based simulators for C-V measurements in order to establish a sounder basis for comparison with optical measurements of thickness. This will be done by studying the relation between the thickness values extracted from C-V measurements using a number of available 1D simulators and the nature of both the underlying physics approximations they incorporate and the mathematical implementation of these simulators. Results from the 1D simulators will be compared with those from a commercial 2-D simulator widely used in industry for modeling device characteristics. Knowledge gained will be applied to the analysis of C-V test data from 2nm oxide wafer sets, and other available relevant gate dielectric films, for comparison with optical film thickness values.

Research to identify preferred layer structure and optical index models for analyzing spectroscopic ellipsometry measurements of advanced gate dielectric materials will emphasize metal oxide and metal silicate films from a variety of sources and a variety of fabrication processes. These will be analyzed using a variety of models for layer structure including possible surface and interface roughness, as well as intended, or unintended, interface layers. An extended range of optical index dispersion functions will be evaluated for modeling the optical properties of these films. Metrics will include not only goodness of fit, but also the correlation matrix for the fitted parameters and the resulting uncertainty for key film parameters. Select samples will be evaluated by extended UV ellipsometry, out to at least 8.5eV, where there are possible benefits for identifying process-induced changes in the optical index/dielectric function beyond the band-gap. Investigations will also be initiated into the use of infrared absorption for the quantification of nitrogen content in oxynitride films.

Work to establish traceability to NIST for gate dielectric films will concentrate on two areas. The first is establishing spectroscopic measurement capability on the master ellipsometer reserved for standards activities with the goal of expanding from traditional single-wavelength HeNe laser based measurements to address current usage of spectroscopic measurements in the semiconductor industry. The second area is an investigation of the effect of core ellipsometer system components and measurement procedures on the short term and longer term precision of film thickness measurements. The goal is to identify improvements needed to enable standards-related and traceability activities at a level of uncertainty consistent with ITRS Roadmap specifications.

Collaborations:

Studies of Optical, Electrical and Physical measurements and properties of Oxynitrides and High-K Dielectric Films for Gate Insulators: Univ. Minnesota, NC State Univ., Stanford Univ., Univ. Texas-Austin, Yale Univ.; IBM, Intel, Jusung America, Lucent Technologies, Texas Instruments; ISMT.

Round Robin Multimethod Studies of the Thickness of Very Thin Oxides: Oak Ridge National Labs, John A. Woollam Inc., KLA -Tencor, n and k Technology, Four-Dimensions Inc., Solid State Measurements Inc., Therma-Wave Inc., Bede Scientific, Rutgers University Measurement Traceability Experiments for SiO_2 + Si_3N_4 film thickness: VLSI Standards Inc. and Rudolph Technologies, Inc.

Development and characterization of 2 nm thick silicon dioxide films for reference artifacts and investigation of contamination, storage, and cleaning of thin film reference artifacts, ISMT, NC State Univ., and KLA-Tencor.

Advanced ellipsometer design and extended modeling of high-κ film dielectric function, Penn State Univ.

Invited Talks:

Richter, C.A., Vogel, E, Hefner A., and Brown, G., Quantum Mechanical Device Simulation Benchmarking, ISMT Gate Stack Engineering Working Group, Raleigh, N.C., Nov. 11, 1999.

Richter, C.A., Nguyen, N.V., Huff, H, Shaapur and Brown, G. NIST/ISMT Optical/TEM Analysis of High-K Dielectric Films, ISMT Gate Stack Engineering Working Group, Raleigh, N.C., Nov. 12, 1999.

Publications:

Richter, C. A., Nguyen, N. V., Alers, G. B., Guo, X., Wang, X., Ma, T. P., and Tamagawa, T., Analytical Spectroscopic Ellipsometry of Ta_2O_5 and TiO_2 for Use As High-κ Gate Dielectrics, Workbook of the 30th IEEE Semiconductor Interface Specialist Conference, December 1999, p. 2.2.

Maher, D., and Richter, C. A., Gate Dielectric Metrology Review: Project FEPZ001 Year 2 Report, International ISMT Project, January 2000, 124 pages.

Gajewski, D. A., Nguyen, N. V., Guyer, J. E., Kopanski, J. J., Richter, C. A., and Pellegrino, J. G., In Situ and Ex Situ Spectroscopic Ellipsometry of Low-Temperature-Grown GaAs, Journal of Electronic Materials, special insert: 2000 Electronic Materials Conference Program (Denver, CO), Journal of Electronic Materials, Vol. 29, No. 7, July 2000, pp. 6-9.

Vogel, E. M., Henson, W. K., Richter, C. A., and Suehle, J. S., Limitations of Conductance to the Measurement of the Interface State Density of MOS Capacitors with Tunneling Gate Dielectrics, IEEE Trans. on Electron Dev., Vol. 47, No. 3, March 2000, p. 601.

Nguyen, N.V., Richter, C.A., and Cho Y.J., Effects of High-Temperature Annealing on the Dielectric Function of Ta_2O_5 Films Observed by Spectroscopic Ellipsometry, to be published in Applied Physics Letters, Nov. 2000.

Richter, C.A., Hefner, A., and Vogel, E., A Comparison of Quantum-Mechanical Capacitance-Voltage Simulators, to be published in IEEE Electron Device Letters, Jan. 2001.

Diebold, A. C., Chism, W. Canterbury, and Richter, C. Characterization and Production Metrology of Thin Transistor Gate Dielectric Films, to be published in Conference Proceedings of Ultra-Clean Processing of Silicon Surfaces 2000, Jan. 2001.

Richter, C.A., Nguyen, N.V., Gusev, E.P., Zabel, T.H., and Alers, G.B., Optical and Electrical Tickness Measurements of Alternate Gate Dielectrics: a Fundamental Difference, to be published in Proceedings of Characterization and Metrology for ULSI Technology, AIP Conference Proceedings 550, Feb. 2001.

Diebold, A.C., Canterbury, J., Chism, W., Richter, C. A., Nguyen, N., and Ehrstein, J., "Characterization and Production Metrology of Gate Dielectric Films", Paper No. 0748, to be published in Proceedings of Symposium on Advanced Characterization of Semiconductor Materials of the Spring 2000 meeting of the European Materials Research Society Meeting at The European Material Conference.

Ultra Shallow Depth Profiling by ToF-SIMS

Technical Contacts:

A. J. Fahey and S. R. Roberson

Objective:

To determine the operating parameters for time-of-flight secondary ion mass spectrometric (ToF-SIMS) depth-profiling analysis of nanometer-scale implants in Si wafers and to demonstrate this capability.

Customer Needs:

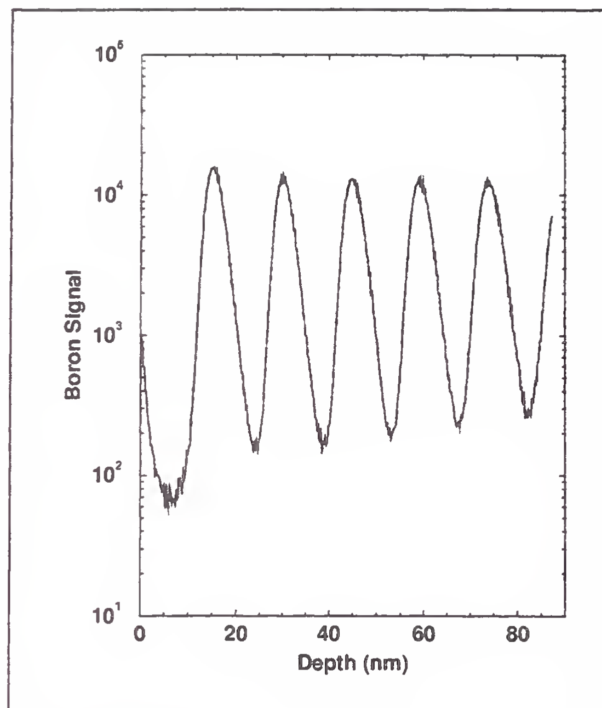
Reductions in the scale of semiconductor devices require SIMS measurements with depth resolutions on the nanometer scale. To achieve the necessary depth resolution various methods have been explored. It has been found that lower primary beam energies, the use of molecular species in the primary beam and the use of certain incidence angles all affect the depth resolution. The commercially available magnetic sector SIMS instruments are designed in such a way that it is difficult to achieve low primary ion beam energies. In addition, the commonly available ion sources are limited to producing simple atomic or diatomic ions.

Technical Strategy:

The ToF-SIMS at NIST is equipped with two ion sources that can be used for sputtering. One is an electron-impact source that is capable of generating ions from reactive as well as noble gases. We used this electron impact source with SF_6 gas to produce SF_5^+ ions for the sputtering beam with an impact energy of 3 keV. Conditions were optimized to minimize the decay length of the measured B signal in B-doped Si where the B was deposited in near-monolayer planes separated by 15 nm (generally referred to as a δ-doped sample). SIMS analysis was carried out with a pulsed Ga^+ ion beam.

Accomplishments:

The results of a depth profile taken under optimal conditions for a 3 kV SF_5^+ sputter beam are shown in Figure 1. The mean 1/e decay length for the 5 deltas is 1.52 nm on the trailing edge of the peaks, where the depth resolution is typically the poorest. The resolution degrades as deeper layers are probed, ranging from 1.45 nm at a depth of ≈ 20 nm to 1.66 nm at 78 nm. This resolution is consistent with previously measured resolutions under these conditions. One important analysis condition that is unmentioned in previous publications on ultra-shallow depth profiling with ToF-SIMS is the dose and energy of the primary Ga^+ analysis beam. Although ToF-SIMS is usually considered a low-dose "static SIMS" method, the dose for the *analyzing* beam can be high under depth profiling conditions and can lead to a degradation in resolution from this unexpected source. Thus, care was taken to reduce the Ga^+ dose. This has the consequence of making analysis times longer than desirable for industrial application of ToF-SIMS for depth profiling.



Future Plans:

We plan to investigate profiles done with lower sputter energies to determine the practical limits on depth resolution with this method. In addition we will document the effect of the primary ion dose on the depth resolution and the limits of sensitivity and dynamic range of this method. Publication of these results will provide informative data to the semiconductor-SIMS community.

Nuclear Measurement Methods for Chemical Characterization of As and P Implant Standards

Technical Contacts:

Richard M. Lindstrom, Robert R. Greenberg, Rick L. Paul

Objective:

To develop and apply the analytical methodology for characterizing benchmark Standard Reference Materials (SRMs) of thin films of interest to the semiconductor industry, with the goal of transferring the accuracy of high-quality NIST reference methods of analysis to the chip fabrication line.

Customer Needs:

Ion implantation is used to make conducting and insulating layers in solid-state electronic devices. It is necessary to know the thickness and composition of these films to control and model the deposition process and to provide the basis for international comparability via ISO standards. Secondary ion mass spectrometry (SIMS) is used to measure concentrations and depth profiles of key dopants in silicon, but because SIMS measurements are matrix dependent, accuracy-based standards are needed for absolute calibration. The ISMT Analytical Lab Managers' Working Group (ALMWG) listed SRMs for P, As, and B as the top three needs for ion implants in silicon.

Technical Strategy:

Because they exploit nuclear, not chemical, reactions, nuclear methods of analysis are independent of the chemical state and surroundings of the element measured. Neutron activation analysis is an isotope-specific analytical technique for qualitative identification and quantitative determination of arsenic content, with sensitivity, specificity, and accuracy well matched to the needs of these measurements. The physics is well understood and the analysis is nondestructive. The goal was to certify As mass per unit area with a fully evaluated uncertainty budget and relative expanded uncertainty of less than 1 %.

Results and Future Plans:

In the uncertainty analysis, 29 sources of uncertainty were quantitatively evaluated; seven sources accounted for 98 % of the combined expanded uncertainty. The measurement resulted in a mean an As content of 91.20 mg/cm^2, with an expanded uncertainty, U, of 0.38 %. As a result, NIST accuracy for ion-implanted arsenic in silicon is now transferable to the SIMS community in the semiconductor industry through SRM 2134. The 1999 International Technology Roadmap for Semiconductors (ITRS) specifies improvement in dopant profile concentration measurement from ± 5 % in 1999 to ± 2 % in 2008 with "low systematic error." SRM 2134 meets these requirements for arsenic now.

A similar approach is presently being applied to the certification of a phosphorus implant SRM. The procedure has been demonstrated to have the requisite sensitivity and accuracy. In a preliminary study, analyses of six samples of phosphorus implanted silicon by neutron activation analysis yielded a mean concentration of $(8.35 \pm 0.20) \times 10^{14}$ atoms•cm^{-2} (± 1 standard deviation), in agreement with the nominal implantation value of 8.5×10^{14} atoms•cm^{-2}. Efforts are currently underway to improve the precision of the measurements and to fully evaluate all sources of uncertainty.

Collaborations:

These materials are jointly developed by the Analytical Chemistry and Surface and Micro-Analysis Science Divisions of CSTL, guided by ISMT and other industry input.

External Recognition:

ISMT Analytical Lab Managers' Working Group (ALMWG)
CSTL 2000 Technical Achievement Award

Publications:

R. R. Greenberg, R. M. Lindstrom, and D. S. Simons, Instrumental Neutron Activation Analysis for Certification of Ion-Implanted Arsenic in Silicon, *J. Radioanal. Nucl. Chem.* **245** (2000), 57-63.

R. L. Paul and D. S. Simons, Neutron Activation Analysis for Calibration of Phosphorus Implantation Dose, in *Characterization and Metrology for ULSI Technology*, AIP Conference Proceedings 550, American Institute of Physics, Melville, New York, 2001, 677-681.

Boron and Nitrogen Thin Film and Implant Standards using Neutron Depth Profiling

Technical Contacts:
George P. Lamaze and Heather Chen-Mayer

Objective:

Develop and enhance neutron depth profiling (NDP) capabilities for determination of boron and nitrogen concentrations and profiles. Combine neutron depth profiling and neutron reflectometry results to obtain accurate boron depth profiles that are independent of assumed substrate densities.

Customer Needs:

Capabilities of measuring dopants in thin films and implants are needed for developing and producing reference materials, and for providing reference measurements to the semiconductor industry where SIMS is widely used as an in-house characterization technique, yet concentration standards are often needed for various matrices.

Technical Strategy: The technical strategy is the establishment of a quantitative measurement system to make neutron depth profiling a primary method of measurement for boron, nitrogen and lithium analysis in thin films. Assessing stopping power for various matrices and supplying system-specific new data where possible have also been a part of the program, as well as improved algorithms for data reduction. To provide better spatial resolution, neutron lenses have also been developed. We have also used other techniques for inter-comparison, such as neutron and x-ray reflectometry, and SIMS.

Results and Future Plans:

Routine calibrations of boron in semiconductor materials are now routinely provided at an accuracy of better than 2 % (2σ). Boron measurements are made with a detection limit of 2×10^{12} atoms/cm^2, which corresponds to less than a part per million for implants in silicon. A reference material for boron in silicon intended for the calibration of SIMS instruments has been issued. We have worked with industry to improve industrial processes, such as stoichiometry of TiN. Measurement of nitrogen in thin films such as TiN and SiN is now routine. Development of better neutron lenses for improved spatial resolution is continuing. The combination of NDP and neutron reflectometry has led to improved density information and depth distribution about samples.

Collaborations:

Dr. Kevin Coakley, Div. 898
Dr. Sushil Satija, Div. 856
Dr. Eric Steel, Div. 837
Dr. David Simons, Div. 837
Dr. Tim Hossain, Advanced Micro Devices
Dr. Harry Fujimoto, Intel
Dr. Eric Smith, Texas Instruments
Dr. Steve McQuire, LSU
Dr. Ron Goldner et al, Tufts
Dr. Larry Pilione et al, Penn State
Dr. Brock Weiss, University of Puerto Rico

External Recognition:

IR100 Award, 1995 – Neutron Focusing Lens
Returning industrial customers: Corning, Intel, Lucent, AMD

Publications:

(Partial List)

G.P. Lamaze, H.H. Chen-Mayer, and J.K. Langland, "Recent Developments in Neutron Depth Profiling at NIST," Proc. 1998 Itl. Conf. On Characterization and Metrology of ULSI Technology, AIP (1998)883-886

H. H. Chen-Mayer and G. P. Lamaze, *Depth distribution of Boron determined by slow neutron induced Lithium ion emission,* Proc. 17th International Conference on Atomic Collisions in Solids, Beijing, China, July 2 -6, 1997, Nucl. Instrum. & Meth. B **135** (1998) 407-412

George P. Lamaze and Heather Chen-Mayer, "Nitrogen Analysis In Thin Films Using Cold Neutron Depth Profiling," Proc. of 9th CIMTEC, Forum on New Materials, Florence, Italy, 1998 (in press).

G.P. Lamaze, H. Chen-Mayer, M. Badding and L. Laby, "In situ measurement of Lithium Movement in Thin Film Electrochromic Coatings using Cold Neutron Depth Profiling," Surf. Interface Anal., 27 (1999) 644-647.

H. H. Chen-Mayer, D. F. R. Mildner, G. P. Lamaze, R. L. Paul, and R. M. Lindstrom, "Neutron focusing using capillary optics and its applica-

tions to elemental analysis," in: Proc. 15th Intl. Conf. on the Application of Accelerators in Research and Industry, Denton, Texas, November 1998, J. L. Duggan and I. L. Morgan, Eds., AIP Conf. Proc. **475,** Woodbury, New York, 1999, 718-721.

H. H. Chen-Mayer, G. P. Lamaze, and S. K. Satija, "Characterization of BPSG films using Neutron Depth Profiling and neutron/x-ray reflectometry,", in: Proc. 2000 International Conf. on Characterization and Metrology for ULSI Technology, Gaithersburg, Maryland, June 2000 (in press).

K. J. Coakley, H. Heather Chen-Mayer, G.P. Lamaze, D.S. Simons, and P. E. Thompson, "Calibration of a Stopping Power Model for Silicon Based on Analysis of Neutron Depth Profiling and Secondary Ion Mass Spectrometry Measurements," Nucl. Instrum. Meth. A, 2001 (in WERB review).

Effects of Elastic-Electron Scattering on Measurements of Silicon Dioxide Film Thickness by X-ray Photoelectron Spectroscopy

Technical Contacts:

C. J. Powell *and A. Jablonski (Institute of Physical Chemistry, Warsaw, Poland)*

Objective:

To enable measurements of film thicknesses to be made with improved accuracy by Auger-electron spectroscopy (AES) and X-ray photoelectron spectroscopy (XPS) for nanotechnology, semiconductor metrology and other applications.

Customer Needs:

AES and XPS are used extensively in the semiconductor and other industries for determining thicknesses of thin (< 10 nm) overlayer films on substrates. Such measurements depend on the effective attenuation lengths (EALs) for the relevant electron energy and film material. The EAL differs from the corresponding electron inelastic mean free path (IMFP) because of elastic scattering of the signal electrons in the specimen. While the IMFP is a material property, the EAL depends on the film thickness and the XPS or AES measurement configuration. The extent to which the EAL differs from the IMFP has not been previously documented for films of SiO_2 on Si that are of high technological importance. Recent comparisons of SiO_2 film thicknesses measured with different techniques have shown significant differences. It is clearly desirable to identify the measurement uncertainties of each technique in greater detail.

Technical Strategy:

Calculations have been made of Si 2p photoelectron currents for a Si substrate and SiO_2 films of varying thickness, for Al and Mg characteristic X rays, and for three common XPS instrumental configurations. The calculations were made with an algorithm based on solution of the kinetic Boltzmann equation within the transport approximation to account for elastic scattering along the electron trajectories.

Results and Future Plans:

Figure 1 shows an example of the results. The ratio of the average EAL in the SiO_2 film, <EAL>, to the IMFP in the film is plotted against the SiO_2 film thickness for Mg Kα X rays and for an XPS configuration in which the angle ψ between the X-ray source and the electron energy analyzer is 54°. The solid lines show plots of this ratio for different electron emission angles α. The dashed lines indicate values of the <EAL>/IMFP ratio for constant attenuations of the substrate-signal current of 1 %, 2 %, 5 %, and 10 %. It is clear that for α less than about 60°, the <EAL>/IMFP ratio is approximately constant (within 3 %) for film thicknesses of practical relevance. The average value of this ratio varies between 0.906 and 0.935 depending on the X-ray source, the film-thickness range, and the particular value of ψ. For α greater than about 60°, the <EAL>/IMFP ratio changes appreciably with film thickness, and the <EAL> for the specific conditions needs to be determined

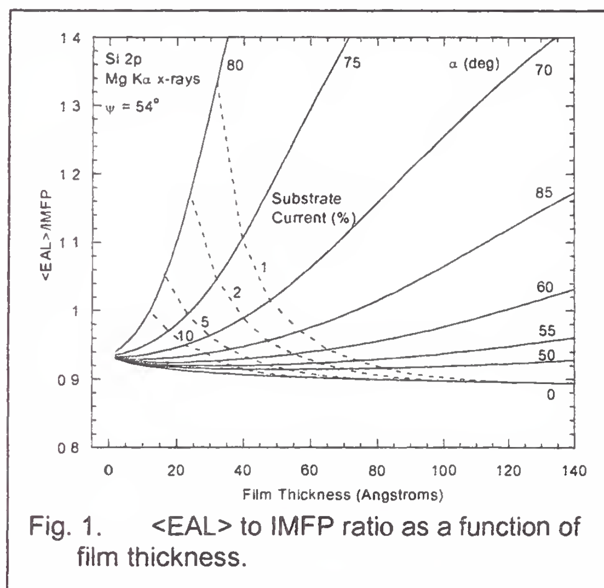


Fig. 1. <EAL> to IMFP ratio as a function of film thickness.

from the calculated curves. It is planned to extend these calculations to other materials for which film thicknesses are determined by XPS or AES.

Publications:

Powell, C. J. and Jablonski, A., "Measurements of Silicon Dioxide Film Thicknesses by X-ray Photoelectron Spectroscopy," in *Characterization and Metrology for ULSI Technology-2000* (in press).

Powell, C. J. and Jablonski, A., “Effects of Elastic-Electron Scattering on Measurements of Silicon Dioxide Film Thicknesses by X-ray Photoelectron Spectroscopy,” J. Electron Spectrosc. (in press).

Monte Carlo Methods For Optimizing the Quantitative Analysis Of Thin Layers, Microparticles and Irregular Surfaces

Technical Contact:
John T. Armstrong

Objective:
To determine test methods and standards that can be used to evaluate and optimize the various electron scattering models and other physical parameters that are used in Monte Carlo calculations of x-ray emission from layered and irregular sample surfaces.

Customer Needs:
Electron microbeam analysis is very well suited for *qualitative* characterization of layered materials, particles and rough surfaces; however accurate *quantitative* analysis of specimens with irregular boundaries has remained elusive. Many industrial applications require accurate analyses of such samples and a variety of methods have been proposed [1-2]. One of the most promising approaches is the use of Monte Carlo simulations to model the electron and x-ray path lengths in complex samples [1,3]. However, the various models and physical parameters commonly used in these calculations give significantly different analytical results.

Technical Strategy:
We have modified the Monte Carlo algorithms of Joy and Armstrong [3] to develop a versatile simulation program that calculates x-ray emission from thin films, particles and rough surfaces of given boundary conditions. The program allows defocusing or rastering of the electron beam to any given size, and bombardment of any portion of the particle or rough surface. The program calculates the electron trajectories at a rate of approximately one million electrons per minute and is modularized to allow for easy substitution for the various physical expressions that make up the model. We have applied this program to determine analytical, geometrical and compositional conditions that are particularly sensitive to the choice of physical parameters used in the Monte Carlo models.

Results and Future Plans:
The results are in generally good agreement with previously developed geometric corrections and with experimental analyses [1]. They are particularly useful in showing the magnitude of electron sidescattering and its effect on x-ray production. This scattering is sensitive to the parameters used by the program and results in large variation in the relative x-ray intensities with closeness to a sample side, with beam to sample angle, and with beam voltage. For example, Monte Carlo calculations show variation in emitted x-ray intensities of particles of AlNi by greater than a factor of 100 with model-dependent variations of over a factor of two.

The Monte Carlo calculations are being used to identify the best measurement experiments (such as stepping the beam toward sample edges or sequentially changing beam to sample angle) and sample compositions to test the physical parameters. Appropriate analyses will then be made on such specimens (in cooperation with the research efforts of John Small and Dale Newbury) to determine the best equations to use for quantitative analysis.

External Recognition:
Armstrong, J.T., "***Improving Analytical Accuracy in the Analysis Particles by Employing Low Voltage Analysis***," Microscopy and Microanalysis 2000 Conference, Philadelphia, PA, August 17, 2000. Invited

Publications:

Armstrong J T (1991) Electron Probe Quantitation, eds K F J Heinrich and D E Newbury (New York: Plenum) pp 261-315.

Small J A, Armstrong J T, Bright D S and Thorne B B (1998) Microscopy Microanal. 4 (suppl. 2) pp 184-5.

Armstrong J T (2000) Microbeam Analysis 2000, eds D B Williams and R Shimizu (Inst. Phys. Conf. Ser. No. 165) pp 429-430.

Phase Identification From sub 200 nm Particles by Electron Backscatter Diffraction (EBSD)

Technical Contacts:
John A. Small

Objective:

To develop methods to improve the quality of electron backscatter diffraction patterns from particles less than 300 nm in size.

Customer Needs:

In our initial work on the phase identification analysis of individual particles by EBSD, we observed that the quality of the EBSD patterns from particles less than about 300 nm in size was poor, especially for low density materials, when the particles were mounted on bulk carbon substrates. This poor quality limits the utility of the technique.

Technical Strategy:

As part of the division's program for materials characterization we are investigating methods for particle identification in the scanning electron microscope/electron microprobe based on electron backscatter diffraction from particles in the 100 nm and above size range. We suspect that the poor pattern quality from submicrometer particles is the result of electron scattering from areas other than the particle of interest. In the case of the very small particles many of the incident electrons exit the particle volume without diffracting and enter the substrate. This not only decreases the intensity of the diffraction signal but also increases the average noise in the EBSD pattern, reducing the signal-to-noise ratio in the pattern to an unacceptably low level.

To improve the EBSD pattern quality for submicrometer particles a sample holder was constructed that enables particle mounting on a thin, electron transparent, substrate. The thin substrate should dramatically reduce the noise contribution from electrons that scatter into the substrate and thus improve pattern quality from very small particles.

Results and Future Plans:

Figure 1c is the EBSD pattern from a 160 nm Al_2O_3 particle mounted on a bulk carbon substrate (Figure 1a). Figure 1d is the EBSD pattern from a 150 nm Al_2O_3 particle mounted on a 20 nm carbon thin-film (Figure 1b). The quality of the EBSD pattern from the particle mounted on the thin substrate is clearly superior to the pattern from the particle mounted on the bulk substrate and has a high enough signal-to-noise ratio to conduct a phase identification analysis of the particle and identify it as hexagonal Al_2O_3. Future plans include investigating other thin-film compositions and low accelerating voltages to extend the application of EBSD phase identification to particles less than 100 nm in size.

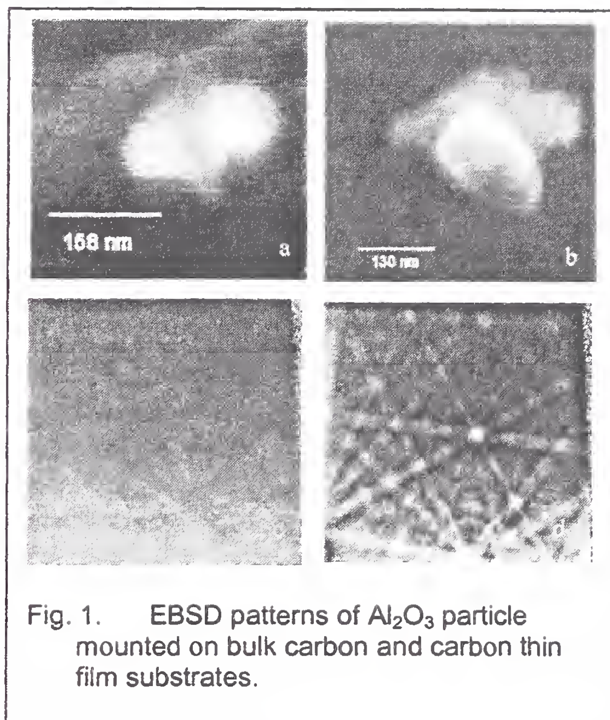


Fig. 1. EBSD patterns of Al_2O_3 particle mounted on bulk carbon and carbon thin film substrates.

Collaborations:

Sandia National Laboratory, Thermo-Noran Instruments.

Publications:

J.A. Small, J.R. Michael, and D.E. Newbury, *"Microbeam Analysis 2000,"* Institute of Physics Conference Series #165, 305-306, 2000.

J.A. Small, J.R. Michael, ***"Phase identification of individual crystalline particles by electron backscatter diffraction (EBSD),"*** Submitted to JOM (in press).

Thin Film Metrology Using X-Rays

Technical Contacts:

R. J. Matyi and R. D. Deslattes

"Often, offline methods provide information that inline methods cannot…..Grazing incidence X-ray reflectivity provides measurement of thin film thickness and density. Grazing incidence X-ray diffraction provides information about the crystalline texture of thin films." "Reference materials are a critical part of metrology since they establish a "yard stick" for comparison of data taken by different methods, by similar tools at different locations (internally or externally), or between model and experiment." **ITRS, 2000 update, p 311.**

Objective:

To provide industry with high-accuracy X-ray based methods, reference materials, and data for the geometrical characterization of simple and complex layer stacks.

Customer Needs:

Thin film thickness, density and interfacial roughness are critical parameters in the performance of conducting and dielectric layers in semiconductor devices. Sensitive and accurate measurements of such properties are needed in the process development phase as well as in subsequent manufacturing practice. In the process development phase the needs are for structural properties that can be associated with the electrical performance characteristics of subsequently patterned device arrays. In the subsequent manufacturing phase the need is principally to calibrate the responses of on-line measurement tools that do not deliver first-principles based data. These tools have been developed to meet the needs for high measurement throughput and compatibility with the production environment. Such tools have material-dependent calibration requirements that lead end users and tool manufacturers to look for alternatives that are less sensitive to materials properties and process variability.

These needs are most practically addressed by the use of well-characterized reference materials whose structural properties are certified by off-line measurements using X-ray reflectivity and diffraction in conjunction with robust analysis and well calibrated angle measurement instrumentation

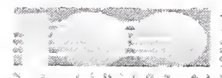
Technical Strategy:

The sub-nanometer wavelengths of X-ray probes and their relatively weak interactions with materials make them a nearly ideal means for determining the geometry of the thin film and multilayer structures that underlie modern semiconductor manufacturing. Our approach has been to develop advanced metrological capability in this area including high performance instrumentation and advanced forms of modeling and analysis. We have made these capabilities available for applications to a considerable range of structural problems involving metallic interconnect layers, advanced dielectrics, and diffusion barrier films. By responding to currently urgent problems, principally, but not exclusively, mediated through ISMT, it has been possible to develop first-hand knowledge of industrial needs as well as of the level of timely responsiveness needed to provide useful input to these problems.

Our program develops and applies X-ray methods to reveal the microstructure of thin film and multilayer structures produced by advanced semiconductor manufacturing. We also generate and certify reference structures for the calibration of in-line production tools. The main components of this work are the following: (1) Development and application of high-resolution X-ray diffraction techniques; (2) Advanced application of modeling methods to describe specular and diffuse scattering; (3) Production of reference samples of thin film and multi-layer structures; (4) Rapid response to urgent problems identified by ISMT. Both the details and the areas of emphasis of our program have evolved on the basis of this experience and guidance received during presentations to various specialized groups within the ISMT framework. Finally, we are in contact with commercial developers of X-ray instrumentation in order to facilitate their interactions through the documentation of best practices and characterization of reference materials.

Accomplishments:

Rapid responses to urgent problems: Our development of improved measurement and production capability has been staged so as to maintain rapid and effective response to urgent industrial needs.



Among the systems we have addressed in this context are: advanced oxynitride dielectrics, high-k dielectrics including barium strontium titanate, tantalum oxide, zirconium oxide and hafnium oxide, Ta_xN_y copper diffusion barriers, and a group of metal stacks including Cu, Ta, Cu/Ta, Ta_xN_y and W_xN_y films. In each case a summary report has been completed including the data obtained, its analysis and interpretation.

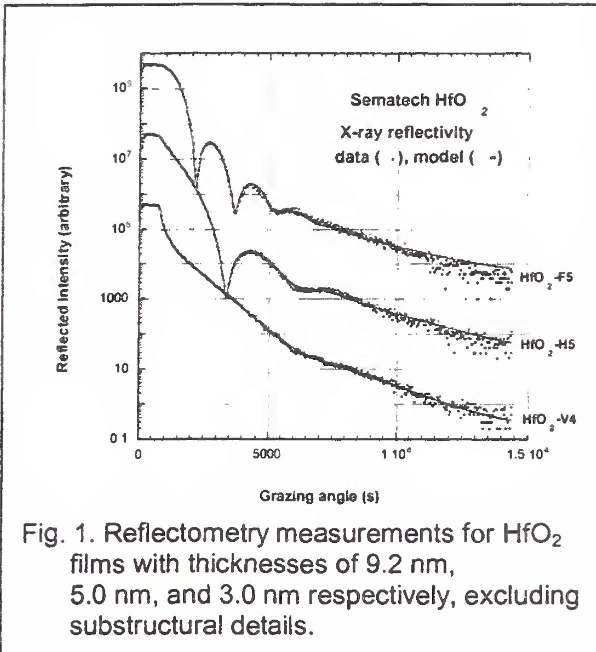


Fig. 1. Reflectometry measurements for HfO_2 films with thicknesses of 9.2 nm, 5.0 nm, and 3.0 nm respectively, excluding substructural details.

Some of our earliest results from reflectometry measurements gave unexpectedly diverse values for film densities as well as evidence of phase separation within layers initially presumed to be homogeneous. Such problems have been explored by means of grazing incidence "powder" diffraction that showed not only the presence of separate crystallographic phases, but also high degrees of preferred orientation in the microcrystalline films. In parallel there has been a process of incremental upgrades of instrumental capability and modeling software.

Important aspects of the potential for model-independent analysis of reflectometry data have been addressed through the development of a form of wavelet analysis particularly adapted to this specific experimental modality. This development has been highly successful and offers as well direct access to interfacial roughness characterization of each of the several interfaces even in a modestly complex layer stack. This form of analysis is computationally efficient, provides unique ordering of layer components, and yields objective starting points for more detailed analysis.

Future Plans:

In addition to maintaining an effective and responsive service capability we intend to pursue two complementary goals. The first is to establish the design of a synthetic multilayer structure that can serve as a certifiable reference material for both X-ray reflectometry and high resolution X-ray diffraction. The second is to establish a self-calibrating coaxial reflectometer/diffractometer by means of which the characteristics of the reference structure can be certified from first principles. The development of the reference structure is expected to proceed through the work of a newly established consortium of potential users and instrumentation vendors. The measurement capability will be established at NIST using best practice and a self-calibrated coaxial angle measurement system to realize the needed certifiable accuracy.

Collaborations:

ISMT, Alain Diebold

External Recognition:

"X-ray Reflectivity Analysis of Oxynitride, High-k and Metallic Thin Film Structures."

R. J. Matyi, Invited Presentation to Metrology Council of ISMT International (Austin, TX, November 4, 1999). "Advanced X-Ray Scattering Methods for Microelectronic Materials Analysis."

R. J. Matyi, Invited presentation at ISMT Analytical Lab Managers Council meeting (Newport Beach, CA, March 7, 2001).

Publications:

D. Keith Bowen and Richard D. Deslattes, "X-Ray Metrology by Diffraction and Reflectivity," in Characterization and Metrology for ULSI Technology 2000, 570-579 AIP 2001.

C. H. Russell, S. M. Owens, R. D. Deslattes, and A. Diebold, in Characterization and Metrology for ULSI Technology 2000, 140-143, AIP 2001.

Richard D. Deslattes and Richard J. Matyi, "Analysis of Thin Layer Structures by X-Ray Reflectometry," in Handbook of Silicon Semiconductor Metrology, A. Diebold, Ed., Chap.27. (in press).

I.R. Prudnikov, R.J. Matyi and R.D. Deslattes, "Wavelet Transform Approach to the Analysis of Specular X-ray Reflectivity Curves," (to be submitted to Journal of Applied Physics).

Optical Metrology of Si/Dielectric Interface

Technical Contacts:
S.T. Cundiff

Objective:

To develop a better understanding of optical second harmonic generation at the Si/SiO_2 interface, its sensitivity to roughness and to explore the potential of second harmonic generation for interface metrology.

Customer Needs:

Feature sizes in semiconductor integrated circuits have been decreasing relentlessly, resulting in remarkable performance gains. As lateral dimensions shrink, the dimensions of gate dielectrics must decrease proportionally. Surface second harmonic generation (SSHG) is an optical technique that is highly surface/interface selective. SSHG has been empirically shown to be sensitive to roughness at the Si/SiO_2 interface. The goal of this project is to obtain a better understanding of the basic physics that gives rise to this sensitivity to roughness. This will give insight into the morphology of the interface and into the potential for SSHG as a measurement tool. Limitation on how thin the gate oxide can be made presents a potential barrier to further reduction in device size by the semiconductor industry. In future generations of integrated circuits (ICs) the gate oxide thickness will be reduced to the point where monolayer fluctuations at the Si/SiO_2 interface will represent a significant percent fluctuation of the total oxide thickness. Hence the industry is in need of a greater understanding of the morphology of the interface. Additionally, methods of making in-situ measurements of the interface would be beneficial. SSHG may have advantages over other methods.

Technical Strategy:

The SSHG signal from Si/SiO_2 displays resonant behavior due to both features in the bulk band structure and the interface alone. We are studying how this resonant behavior changes with change in surface preparation. Specifically we are looking at samples with different miscut (and hence differing step edge density), different oxidation and different roughness (as characterized by x-ray scattering).

SSHG is a very weak effect because only a layer a few monolayers thick at the interface contributes. To obtain a measurable signal, without having to subject the samples to high average powers or high-energy pulses, we use 100 femtosecond pulses at a repetition rate of 76 MHz. This allows high peak powers to be obtained with a modest average power. Photon counting is used for signal detection. A tunable Kerr-lens-modelocked laser is used as the primary source. To extend the tuning range, an optical parametric oscillator is also employed.

A key challenge is to calibrate for changes in laser average power and pulse width that occur with tuning. The change in pulse width results in a change in peak power, and hence signal strength.

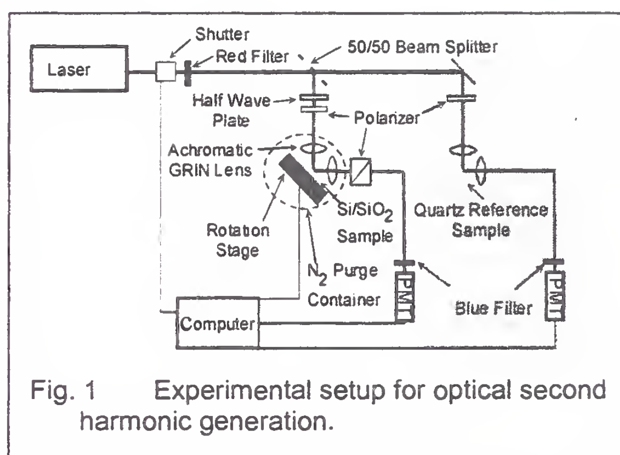


Fig. 1 Experimental setup for optical second harmonic generation.

To do this, a second reference arm is included in the experiment. The reference arm is virtually identical to the signal arm, but a quartz sample is used. Quartz generates a strong second harmonic signal, which is largely independent of laser tuning. A cross calibration between the signal and reference arms is obtained by installing a quartz sample in the signal arm and measuring the two signals versus tuning. The resulting calibration curve is used to correct all subsequent data.

Accomplishments:

Vicinal (miscut) wafers are being used to provide samples with known interface variations. A set of samples with known vicinal angle and direction have been prepared with native oxide and thermal oxide. Measurements on these are complete using the fundamental output from the modelocked Ti:sapphire laser. The results provide baseline data for comparison to samples with known roughness.

Future Plans:

The results show that resonant structure exists at wavelength shorter than those achievable using the modelocked Ti:sapphire laser. Measurements will be made using the frequency doubled output of an optical parametric oscillator. This will allow the short wavelength resonance to be characterized.

Collaborations:

University of Colorado, Bell Labs/Lucent Technologies.

External Recognition:

Invited Talk & Paper: S.T. Cundiff and T.M. Fortier, "Second Harmonic Generation from the Si/SiO_2 Interface," presented at SPIE 2000 conference, proceedings published in "Physics and Simulation of Optoelectronic Devices VIII," R.H. Binder, P. Blood and M. Osinski, eds., Proceedings of SPIE vol. 3944, 646-657 (2000).

Publications:

See above

D. Interconnect and Packaging Metrology Program

Advances in interconnect and packaging technologies have introduced rapid successions of new materials and processes. Environmental pressures are leading to the reduction and eventual elimination of lead in solder used for attaching chips to packages and packages to circuit boards. The overall task of this program is to provide critical metrology and methodology for mechanical, chemical, metallurgical, electrical, thermal, and reliability evaluations of interconnect and packaging technologies.

The function of packaging is to connect the integrated circuit to the system or subsystem platform, such as circuit board, and to protect the integrated circuit from the environment. The increasing number of input/output (I/O) on circuits with vastly larger scale of integration is forcing ever smaller I/O pitches, the use of flip chip bonding, and the use of intermediary platforms called interposers. The integration of sensors and actuators onto integrated circuits through MEMS technology and the increasing use of low cost integrated circuits in harsh environments is increasing the complexity of the packaging task. Environmental concerns are forcing the need for development of reliable lead-free solder and other low environmental impact packaging materials.

System reliability requirements demand modeling, testing methods, and failure analysis of the integrated circuits before and after packaging. Metrology is a significant component of reliability evaluation.

Measurements and Modeling of Electrodeposited Interconnects

Technical Contacts:
G.R. Stafford, T.P Moffat, D. Josell and L. Richter

"As features shrink, etching and filling high aspect ratio structures will be challenging, especially for DRAM. Dual damascene metal structures are also expected to be difficult."
1999 ITRS, page 164

Objective:

Develop measurement tools that assess the ability of electrolytes to show superconformal deposition of copper into small, high-aspect-ratio vias for on-chip interconnects. Use *in-situ* vibrational spectroscopy to determine competitive adsorption kinetics of additives used in copper plating baths. Develop models for superconformal deposition based on the thermodynamics and kinetics of electrochemical processing that will provide the electrodeposition industry with better control over processing at small dimensions.

Customer Needs:

The semiconductor industry has recently made a major shift in materials used for interconnects, or on-chip "wiring," in integrated circuits. After decades of using aluminum as conductors, a switch to copper has been made to take advantage of an inherently lower resistivity. Electrodeposition has been found to be the best means to deposit copper in the narrow, deep trenches used as circuitry, in that "superconformal" deposition that fills very narrow trenches without porosity can be accomplished when organic additives are present in the plating bath. These addition agents are also responsible for grain refinement in the deposited material which lead to secondary grain growth and improved resistivity. Although a phenomenological understanding of the influence of additives exists, a molecular level view of this process is totally absent. Consequently, there is a tremendous need for developing a predictive capacity for describing the influence of electrolyte species on the evolution and properties of electrodeposited Cu films.

Technical Strategy:

NIST researchers have developed a copper plating bath that produces copper films with recrystallization and superfill behavior identical to that reported by industry. The principal additives in this bath are NaCl, an organic compound known as MPSA, and polyethylene glycol (PEG). Understanding the surface chemistry under the chemical conditions and range of potentials normally used in commercial copper plating is required to extend the use of electrolytic copper to sub-100 nm length scales. The nonlinear optical technique of vibrationally resonant sum frequency generation (VR-SFG) is uniquely interface specific and can be applied to the *in-situ* study of electrodes. We expect to develop measurement tools to examine competitive adsorption of NaCl-MPSA-PEG during the electrolytic deposition of copper.

Accomplishments:

A model electrolyte that generates the essential characteristics required for successful copper Damascene metallization has been identified. Examination of binary combinations of Cl-PEG-MPSA additives clearly reveals the synergistic nature of the interactions between the three species required for void-free filling of ULSI features with the desired copper microstructure, Figure 1. The desired attributes appear to correlate with the hysteretic i-E response suggesting its utility as both an investigative screening and process control tool for assaying "brightener" activity. Although a detailed description of the system response remains to be developed, the measurement itself is a direct reflection of the deposition process as opposed to the widely employed, but somewhat more ambiguous, technique known as cyclic voltammetric stripping analysis (CVS). Experiments at NIST show that such hysteretic behavior by itself indicates an ability to fill narrow trenches eliminating the need to do more extensive experimental development. The Cl-PEG-MPSA electrolyte (a) yields superconformal copper deposition into trenches between 500 and 90 nm in width with an aspect ratio ranging from 1:1 to ≈ 6.6:1. In contrast, similar experiments using either an additive-free electrolyte, or an electrolyte containing the binary combinations Cl-MPSA (b) or Cl-PEG (c) resulted in the formation of a continuous void in the center of the trench, Figure 2.

We have successfully measured *ex-situ* VR-SFG spectra of MPSA on both gold and copper substrates. Five resonant features between 2800 and 2950 cm^{-1} can be attributed to the CH_2 groups of

the MPSA. *In-situ* measurements in 0.01 mol/L $HClO_4$ failed to show these features although a decrease in the non-resonant background due to the substrate was apparent. We attribute this to an all-trans conformation of the MPSA, resulting in unobservable resonance features. An *ex-situ* VR-SFG measurement of MPSA on Au, focusing on the symmetric stretch of the sulfonate end group at 1070 cm^{-1}, suggests that the kinetics of MPSA adsorption may be examined, *in-situ*, in this way. Future *in-situ* VR-SFG measurements will be made under potential control.

Future Plans:

In the coming year, we will address several short and long term objectives. These include 1) establishing a model which defines the role of adsorbates in superconformal deposition; 2) develop measurement tools to examine competitive adsorption on copper using vibrational spectroscopy; 3) pursue further interactions with chemical and bath monitoring industries to incorporate NIST-developed measurement tools.

Collaborations:

Feedback from the electroplating industry is extremely positive. ECI Technology, the industry wide recognized leaders in the implementation of CVS analysis for characterizing plating bath additive chemistry, is adding the NIST-developed measurement technology to their commercial software.

Publications:

T.P. Moffat, J.E. Bonevich, W.H. Huber, A. Stanishevsky, D.R. Kelley, G.R. Stafford, and D. Josell, "Superconformal Electrodeposition of Copper in 500-90 nm Features," J. Electrochem. Soc. 147, 4524-4535 (2000).

T.P. Moffat, D. Wheeler, W.H. Huber and D. Josell, "Superconformal Electrodeposition of Copper," Electrochem. Solid-State Lett. 4, C26 (2001).

Stafford, G., Moffat, T., Jovic, V., Kelley, D., Bonevich, J., Josell, D., Vaudin, M., Armstrong, N., Huber, W., and Stanishevsky, A., "Cu Electrodeposition for On-chip Interconnections," Characterization and Metrology for ULSI Technology: 2000, D. G. Seiler, A. C. Diebold, T. J. Shaffner, R. McDonald, W. M. Bullis, P. J. Smith, and E. M. Secula, Eds. (AIP, New York, 2001), pp. 439-443.

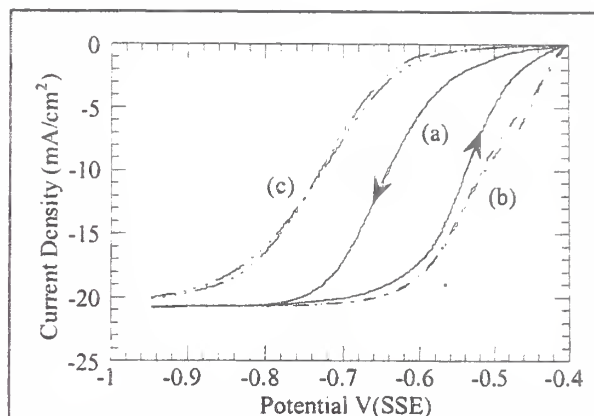
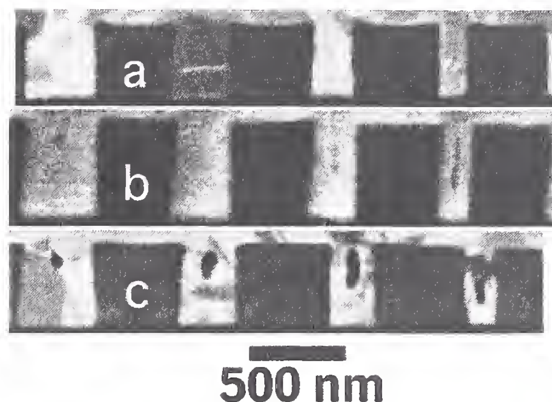


Fig. 1. Linear sweep voltammetric curves for copper deposition on a stationary polycrystalline copper disc electrode in CuSO4-H2SO4 containing (a) NaCl + MPSA + PEG, (b) NaCl + MPSA, and (c) NaCl + PEG.



500 nm

Fig. 2. FIB images of copper electrodeposited from an electrolyte containing (a) NaCl + MPSA + PEG, (b) NaCl + MPSA, and (c) NaCl + PEG. The trenches were patterned using electron beam lithography. Note that complete filling of the narrowest trenches, 100 nm, is void-free only with the ternary addition which also shows hysteresis in Figure 1.

Interconnect Materials and Reliability Metrology

Technical Contacts:

***D. T. Read**, R. R. Keller, F. R. Fickett*

"In the near term, the most difficult challenges for interconnect include the rapid introduction and integration of new materials and processes, dimensional control, physical/electrical reliability of interconnect structures and interconnect processes with low or no device impact."

ITRS 1999 Edition, SIA, p. 163.

"A microtensile methodology, developed at the National Institute for Standards and Technology, has been adopted and applied in Motorola to evaluate material properties of thin films. This methodology is a significant part of the materials technology development at Motorola."

Betty Yeung, (David Read), Yifan Guo, Bill Lytle, and Vijay Sarihan (Motorola AISL, Tempe, AZ), "Microtensile Methodology for Mechanical Characterization of Thin Films," manuscript in preparation for submittal to *Chip Scale Review.*

Objective:

The objectives of this project are: (1) to develop experimental techniques to measure the reliability-related properties of thin films, including basic tensile properties, fatigue, fracture resistance, and electromigration and stress-voiding resistance, in specimens fabricated and sized like materials used in actual commercial devices; (2) to relate thin film reliability to microstructure; (3) to extend test techniques from their present level (1 µm thick, 10 µm wide) to smaller specimens that are similar in size to the conductive traces used in contemporary VLSI circuits (widths of 0.1 to 1 µm).

Customer Needs:

Thin films are an essential component of all advanced electronic devices. Understanding of failure modes in these devices, especially interface delamination, requires knowledge of the mechanical behavior of the films. Resistance to electromigration and stress-voiding is controlled by microstructural features closely related to those that control mechanical behavior. Techniques for measuring the mechanical behavior of thin films are being developed and applied. Because the films are formed by physical vapor deposition, their microstructures, and hence their mechanical properties, are quite different from those of bulk materials of the same chemical composition. While the general principles of conventional mechanical testing are applicable to thin films, conventional test equipment and techniques are not. Because vapor-deposited films are of the order of 1 µm thick, the failure loads are of the order of gram-forces or less, and the specimens cannot be handled directly.

Technical Strategy:

This project develops measurement methods using specimens both obtained from industry and fabricated within NIST. We have developed apparatus and conducted measurements on AC electromigration, in order to better understand the processes of stress-voiding and practical electromigration. We have developed the silicon-frame tensile specimen and the piezo-actuated tensile tester, which operate successfully for specimens 100 µm wide and larger. We have continued to support one such apparatus at NIST and one at Motorola in Tempe. Another, which uses a different control software, exists at the University of Colorado at Boulder. Because problems were encountered with specimens narrower than 100 µm, a new technique, called the force-probe tensile test technique, has been developed. The apparatus includes a tensile loading system operable within the scanning electron microscope (SEM). This system has now been used on specimens as small as 2 µm wide. It is anticipated that the magnification of the SEM will allow testing even narrower specimens.

Accomplishments:

Our measurements of AC electromigration have produced microstructural features completely different in both quantity and quality from those seen in conventional DC electromigration testing (Fig. 1). Our measurements of the apparent static Young's modulus of pure aluminum thin films, resulting in values different from the annealed bulk polycrystalline value, hint at the presence of as yet undocumented features in the microstructure (Fig. 2). In the past fiscal year, we have performed successful tensile tests on three new types of specimens: electrodeposited gold 200 µm wide by 800 µm long, fabricated on copper foil; Al 1 percent Si specimens 10 µm wide and 200 µm long fabricated in a conventional CMOS fab under the MOSIS program; and MEMS polysilicon 2 µm by

2 µm by 60 to 1000 µm fabricated by Sandia National Laboratories to their own specimen design, which is independent of, though conceptually similar to, the NIST specimen.

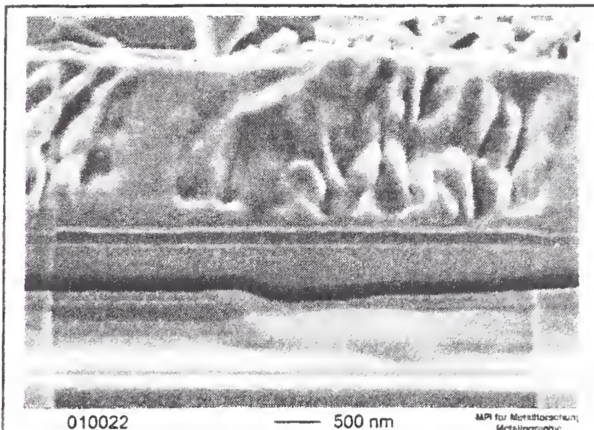


Fig. 1. SEM micrograph of features produced by AC electromigration, obtained by R. Keller during his visit at MPI in Stuttgart, Germany.

Our results are being disseminated in conference presentations and peer-reviewed articles in archival journals, as well as in presentations and written reports to the organizations that have supplied specimens.

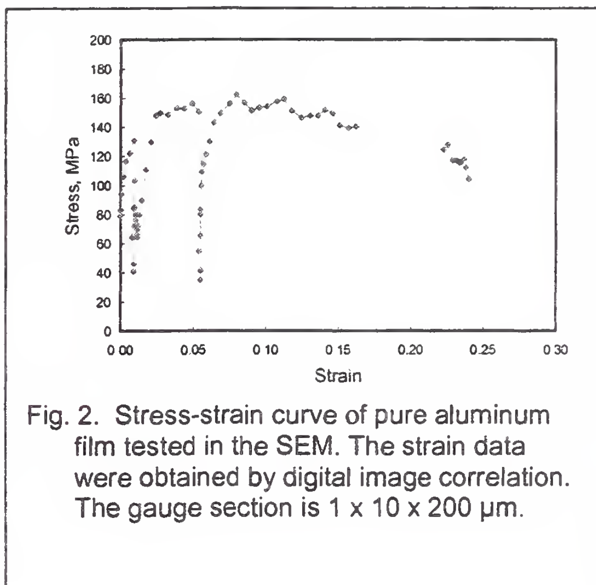


Fig. 2. Stress-strain curve of pure aluminum film tested in the SEM. The strain data were obtained by digital image correlation. The gauge section is 1 x 10 x 200 µm.

Future Plans:

Measure the mechanical properties of other materials that are important in microelectronic interconnect structures, such as interlayer dielectric. Measure specimens closer in size to actual production devices, which means measuring specimens much narrower than we do now. Use TEM observations to characterize the microstructures associated with AC electromigration and with mechanical deformation of thin films. Develop techniques for measurement of mechanical properties of thin films at elevated temperatures.

Collaborations:

In the current fiscal year, we tested specimens from Hutchinson Technologies, Hutchinson, Minnesota (electrodeposited gold), AMI Semiconductor, Pocatello, Idaho (CMOS aluminum, through the MOSIS service), and Sandia National Laboratories, Albuquerque, New Mexico (polysilicon), as well as specimens fabricated at NIST. We provided support for the piezo-actuated microtensile tester at Motorola Advanced Interconnect Systems Laboratory, at Tempe, Arizona.

External Recognition:

Motorola Patent Committe 2000 Invention Disclosure Award, a "routine" recognition for development of unpatented technology, obtained by D. T. Read while he was a NIST Industry Fellow with the Motorola Advanced Technology Center in Schaumburg, Illinois.

Publications:

Microstructural and Mechanical Characterization of Electrodeposited Gold Films, Long, G. S., Read, D. T., McColskey, J. D., and Crago, K, *ASTM STP 1413*, *Mechanical Properties of Structural Films.*

Jonnalagadda, Krishna, Read, David, and Skipor, Andrew, “Electrical Shield Design for Improved Mechanical Reliability,” *Motorola Technical Developments*, Volume 42, December 2000.

David T. Read, Krishna Jonnalagadda, William Olson, and Andrew Skipor, “Reinforcing Splint Between Shields on Printed Wire Board,” *Motorola Technical Developments*, Volume 42, December 2000.

Porous Thin Films Metrology for Low K Dielectrics

Technical Contacts:

Barry J. Bauer, Eric K. Lin, and Wen-li Wu

The need of low dielectric constant (κ) material for interlevel dielectrics (ILD) in next generation IC chips is well documented in Figure 30 of the "Dielectric Potential Solutions" **ITRS, SIA, 1999 edition, p. 173**

Objective:

To provide the semiconductor industry with unique on-wafer measurements of the physical and structural properties of porous thin films important to their use as low-κ dielectric materials..

Customer Needs:

As integrated circuit feature sizes continue to shrink, new low-k interlayer dielectric materials are needed to address problems with power consumption, signal propagation delays, and cross talk between interconnects. One avenue to low-κ dielectric materials is the introduction of nanometer scale pores into a solid film to lower its effective dielectric constant. However, the pore structure of these low-κ dielectric materials strongly affects important material properties other than the dielectric constant such as mechanical strength, moisture uptake, coefficient of thermal expansion, and adhesion to different substrates. The characterization of the pore structure is needed by materials engineers to help optimize and develop future low-κ materials and processes. Currently, there is no clear consensus among IC chip manufacturers for the selection of a class of material or a processing method of nanoporous films. Candidates include silica-based films, organic polymers, inorganic spin-on materials, chemical vapor deposited materials, and several others. With the large number of possible materials and processes, there is a strong need for high quality structural data to help understand correlations between processing conditions and the resulting physical properties.

Technical Strategy:

The small sample volume of 1 μm films and the desire to characterize the film structure on silicon wafers narrows the number of available measurement methods. NIST is using a combination of small angle neutron scattering (SANS), specular x-ray reflectivity (SXR) and high energy ion scattering to determine important structural and physical property information including average pore size, porosity, pore connectivity, film thickness, matrix material density, coefficient of thermal expansion, moisture uptake, and film composition.

Accomplishments:

Our efforts have been focused into three areas, characterizing current industrially relevant materials through ISMT, gaining fundamental understanding of different classes of material preparation, and conducting an international round robin comparison of different on-wafer measurement techniques. ISMT, a consortium of microelectronics companies, has provided more than 35 separate samples for characterization by NIST including spin-on glass materials, films from chemical vapor deposition, and organic thin films. The structural information provided by NIST is placed into a master database, combining data from a variety of sources, detailing both the structural and material properties needed to evaluate candidate materials. The data have been extensively used by member companies to guide the development of low-κ dielectric materials for integration into future devices. In addition, we have helped many US chemical industries, Dow Chemicals, Dow

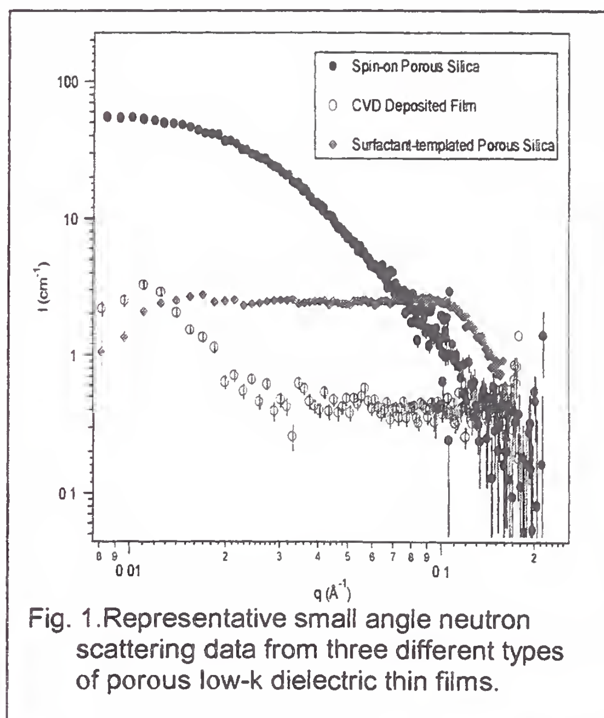


Fig. 1.Representative small angle neutron scattering data from three different types of porous low-k dielectric thin films.

NIST
National Institute of Standards and Technology
Technology Administration, U.S. Department of Commerce

Corning, Allied Signal, and Rohm & Haas in their effort developing low κ materials.

Future Plans:

Work is in progress to develop new techniques for measuring the size distribution of nanovoids as well as their distribution along film thickness direction.

Collaborations:

H. Lee, H. Wang, (Polymers Division, NIST), Jeffrey T. Wetzel, Changming Jin, Jeffrey Lee (ISMT), Mikhail Baklanov (IMEC), David Gidley (University of Michigan), Wei Chen, Eric Moyer (Dow Corning), Shu Yang (Lucent), Hongyou Fan, C. J. Brinker (Sandia National Laboratory)

External Recognition:

Mechel Lerme Best Paper Award, 1999 International Interconnect Technology Conference.

Wu, W.; Lin, E. K.; Jin, C., and Wetzel, J. T., "A Three-Phase Model for the Structure of Porous Thin Films Determined by X-ray Reflectivity and Small Angle Neutron Scattering," Materials Research Society Meeting; San Francisco, CA. 2000.

Publications:

Barry J. Bauer, Eric K. Lin, Hae-Jeong Lee, Howard Wang and Wen-li Wu. " Structure and Property Characterization of Low-κ Dielectric Porous Thin Films," J. Electronic Materials, 30(4), p. 304 (2001).

Wu, W. L.; Wallace, W. E.; Lin, E. K.; Lynn, G. W.; Glinka, C. J.; Ryan, E. T., and Ho, H. M., "Properties of Nanoporous Silica Thin Films Determined by High- Resolution X-Ray Reflectivity and Small-Angle Neutron Scattering," Journal of Applied Physics, 87(3):1193-1200 (2000).

Lin, E. K.; Lee, H. J.; Wang, H., and Wu, W. L.,"Structure and Property Characterization of Low-k Dielectric Porous Thin Films Determined by X-ray Reflectivity and Small-Angle Neutron Scattering," Proc. of the 2000 Intl. Conf. on Characterization and Metrology for ULSI Technology 2000.

Lin, E. K.; Wu, W. L.; Jin, C., and Wetzel, J. T., "Structure and Property Characterization of Porous Low-k Dielectric Constant Thin Films using X-ray Reflectivity and Small-angle Neutron Scattering," Proc. of the Materials Research Society Meeting. (2000).

Lee, H. J., Lin, E. K., Wu, W. L., Fanconi, B. F., Liou, H. C., Lan, J. K., Cheng, Y. L., Wang, Y. L., Feng, M. S., and C. G. Chao, "X-Ray Reflectivity Measurements of N2 Plasma Effects on the Density Profile of Hydrogen Silsesquioxane Thin Films," J. Electochem. Soc,.submitted (2000).

Interconnect Dielectric Characterization Using Transmission-Line Measurement

Technical Contacts:

Michael Janezic, Dylan Williams

"The high frequency measurements performed at NIST complement the ISMT DC characterization and provide the effective dielectric constant over a broad frequency range....since high performance microprocessors have recently broken the 1 GHz barrier, it is extremely important that new interconnect materials and structures be characterized at a high frequency." **Robert Haveman, ISMT**

Objective:

To develop methods to accurately measure the dielectric properties of low-k thin films from easy-to-perform in-situ transmission-line measurements. This project brings together the NIST Electromagnetic Properties of Materials Program and the NIST High-speed Microelectronics Program into a collaborative effort with ISMT and Dow Chemical to develop methods for semiconductor and material manufacturers for determining the dielectric properties of low-k thin films.

In this work, MMIC probing techniques are used to measure the capacitance and conductance per unit length of small printed transmission lines incorporating the materials to be characterized. The relative permittivity of dielectric thin films and the conductivity of the metals used in the lines construction are subsequently derived over broad frequency ranges.

Customer Needs:

To improve electrical performance of interconnects, the semiconductor industry is replacing traditional silicon dioxide thin films with lower permittivity (low-k) thin films. Reducing the permittivity of the dielectric separating the interconnects decreases the parasitic capacitive effects. As a result, smaller interconnects that operate at higher frequencies are feasible. Although many candidate low-k thin film materials exist, the permittivity of many of these new materials remains relatively unknown, especially at high frequencies.

The 1999 SIA ITRS identifies the development and characterization of low-k dielectrics as a critical component in the drive to increase processor performance. In the Critical Interconnect Measurement Needs Summary on page 309, it states, "Design of interconnect structures requires measurement of the high frequency dielectric constant of low-k materials."

Technical Strategy:

Our current primary goal is to develop the measurement methodology based on transmission line measurements for determining the dielectric constant of low-k thin films. Because semiconductor manufacturers and material suppliers have different needs and equipment, we are pursuing different approaches for each. We have nearly completed the development of methods for semiconductor manufacturers, and are now beginning to focus on material suppliers.

Early efforts revolved around coplanar waveguides fabricated at Texas Instruments, shown in Fig. 1. We performed measurements of the capacitance per unit length of these coplanar waveguides passivated with BCB, HSQ, and SiO_2 films. Although the measurements convincingly demonstrated the planar transmission-line approach, the test structures were difficult to analyze and lacked sensitivity.

Since our work with Texas Instruments we have focused on a simpler and more sensitive microstrip approach. In collaboration with ISMT we have designed microstrip test structures with greater sensitivity as a majority of the electromagnetic fields are confined to the low-k dielectric incorporated into the microstrip transmission lines.

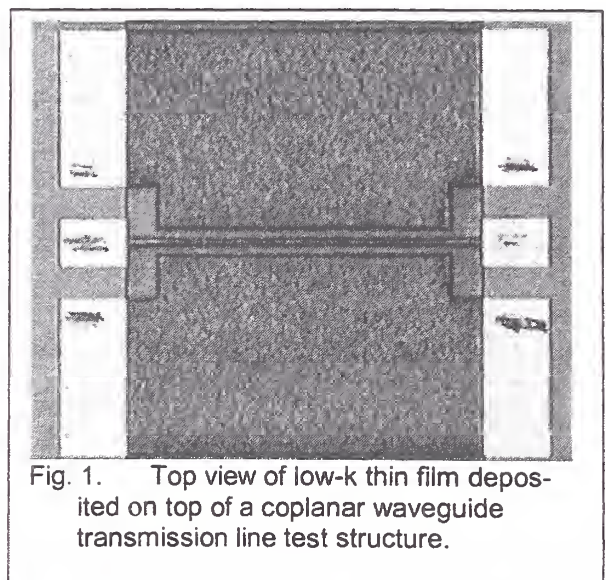


Fig. 1. Top view of low-k thin film deposited on top of a coplanar waveguide transmission line test structure.

Accomplishments:

In a joint effort with ISMT we have developed a method of accurately determining the dielectric properties of low-k dielectric and copper conductors. The method utilizes printed microstrip transmission line test structures that incorporate the low-k thin film. From measurements of the test structure's propagation constant and characteristic impedance, the thin film permittivity is determined at high frequencies. By measuring *both* the propagation constant and characteristic impedance, they demonstrated the ability to separate the electrical properties of the dielectric thin film from the metal conductors. Recent measurements, shown in Fig. 2, on both low-k and silicon oxide thin films confirm that the permittivity measurement accuracy is within the goal of ± 5 %.

Future Plans:

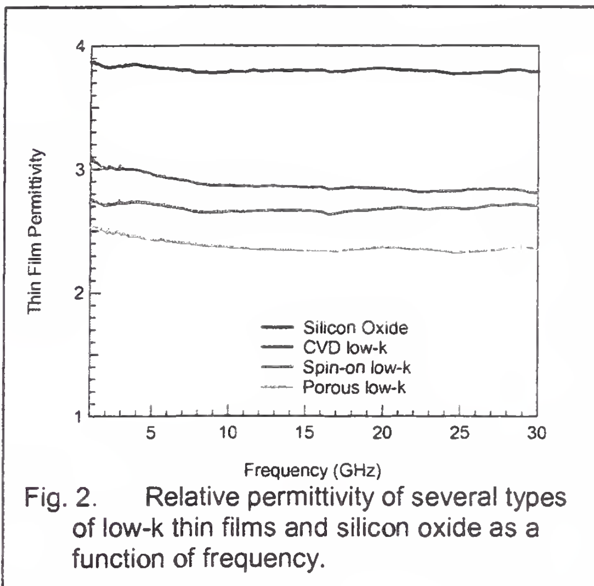


Fig. 2. Relative permittivity of several types of low-k thin films and silicon oxide as a function of frequency.

We are using NIST's unique processing capabilities to pursue a very different approach to dielectric thin-film characterization with Dow Chemical, a major supplier of low-K dielectrics. NIST will perform most of the microfabrication; Dow will simply deposit and pattern the low-k thin films on pretested circuits provided by NIST. A second set of measurements made at NIST will test for the differences in transmission-line capacitance. We have already fabricated and forwarded samples to Dow. This approach could result in the development of an important new method for the semiconductor industry.

Collaborations:

Texas Instruments - Studied initial design, fabrication and measurements of coplanar waveguide test structures.

ISMT - Developed microstrip transmission-line method and measured the permittivity of several classes of low-k thin film on structures fabricated at ISMT.

Dow Chemical - Developing improved coplanar waveguide method suitable for material manufacturers and suppliers.

External Recognition:

M.D. Janezic and D.F. Williams, "Permittivity Measurements of Low-k Thin Films from Transmission Line Measurements," ISMT Technical Advisory Board Meeting, Austin TX, Feb. 1999.

M.D. Janezic and D.F. Williams, "Permittivity Measurements of Low-k Thin Films from Transmission Line Measurements," ISMT Technical Advisory Board Meeting, Orlando, FL, March 1999.

M.D. Janezic and D.F. Williams, "Permittivity Characterization of Low-k Thin Films from Transmission-line Measurements," 2000 International Conference on Characterization and Metrology for USLI Technology, Gaithersburg MD, June 2000.

M.D. Janezic and D.F. Williams, "Permittivity Characterization of Low-k Thin Films from Transmission-line Measurements," ISMT Technical Advisory Board Meeting, Austin, TX, November 2000.

Publications:

D. F. Williams, M. D. Janezic, A. Ralston, S. List, "Quasi-TEM model for coplanar waveguide on silicon," 1997 EPEP Conference Digest, pp. 225-228, Oct. 27-29, 1997.

M. D. Janezic and D. F. Williams, "Permittivity Characterization from Transmission-Line Measurement," IEEE International Microwave Symposium Digest, vol. 3, pp. 1343-1345, June 10-12, 1997.

M. D. Janezic, D.F. Williams, V. Blaschke, A. Karamcheti, C. S. Chang, "Permittivity Characteri-

zation of Low-k Thin Films from Transmission-line Measurements" (in review).

X-Ray Tomography of Microstructures

Technical Contacts:
Zachary H. Levine

Objective:

The goals of this project are: (a) to demonstrate the feasibility of tomography of integrated circuit interconnects to kindle interest in a larger-scale implementation; (b) to aid in the development of tools for routine laboratory-scale integrated circuit tomography; and (c) to develop a leading edge synchrotron-based integrated circuit tomography capability for the calibration of laboratory instruments and to provide a capability for the most demanding problems. Integrated circuit interconnects are taken to include both aluminum and copper.

Customer Needs:

Failure analysis is a continuing and multifaceted challenge for the semiconductor industry. Yet, there is a need for a tool which can image a 10 micrometer cube with resolution below 100 nm. Most probes are two dimensional; an exception, TEM-based tomography operates on samples smaller than 1 micrometer diameter.

The customer requires a laboratory tool rather than a synchrotron beam line. This is because: (a) synchrotron schedules are not compatible with the customer's time-to-information requirements; and (b) outsourcing of analytical tools tends to create less meaningful information than that developed in-house.

Technical Strategy:

We partner with industry, national laboratories, and universities to achieve the project goals based on the use of the best available technology.

In addition to helping to develop the project goals, our partners in the semiconductor industry prepare samples. The sample preparation requirements are similar to that required for transmission electron microscopy, but less demanding. To date, we have partnered with people at national laboratories to use existing x-ray microscopes on synchrotron beam lines to perform x-ray tomography. We have partnered with universities to obtain tomographic reconstruction software. The actual acquisition of data --- which involved 24 hrs. operation at remote locations --- has been performed jointly with industry-, national laboratory- and university-based partners. We have taken responsibility for the actual processing of the data, tomographic reconstruction, and display. Software development is simplified by relying on high-level graphics packages supported by the NIST Visualization Group. This teaming approach has resulted in a relatively rapid first demonstration of integrated circuit tomography.

Two private companies (JMAR Research and XRadia) are now developing laboratory sources. The NIST role is now diminished; however, in 1998-2000, NIST consulted actively with JMAR, and a joint NIST-JMAR patent for a laboratory-based source is pending.

As the main effort in the near term, NIST is working with the Advanced Light Source of the Lawrence Berkeley National Laboratory to develop a dedicated beamline for deep submicron tomography. We anticipate two orders of magnitude improvement in throughput compared to the preliminary experiments, plus the ability to study multilayer copper stacks. The beamline is expected to open in 2002.

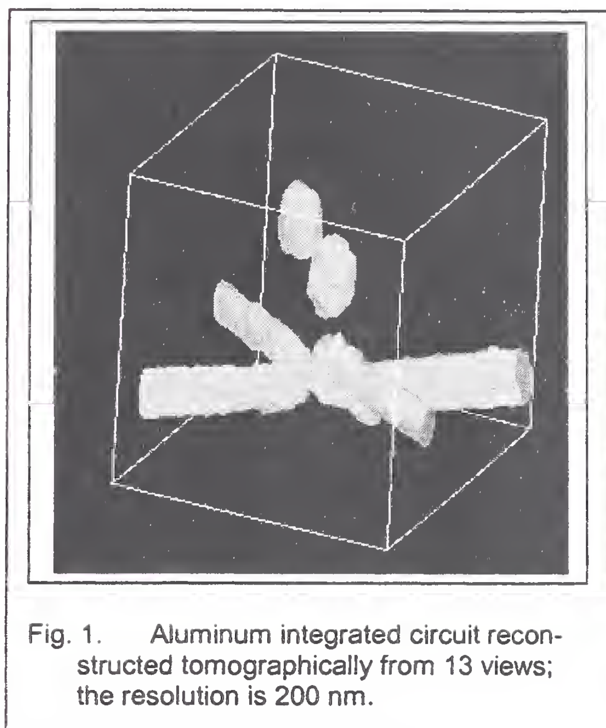


Fig. 1. Aluminum integrated circuit reconstructed tomographically from 13 views; the resolution is 200 nm.

Accomplishments:

First reconstruction of an integrated circuit interconnect: 400 nm resolution in 3D.

Improvement of resolution to 140 nm in 3D by improved hardware and software.

First three-dimensional information obtained from a copper integrated circuit using x-rays.

Approval of beamline 8.3.2 by Advanced Light Source Scientific Advisory Committee.

Solders and Solderability Measurements for Microelectronics

Technical Contacts:

F. W. Gayle, W. J. Boettinger, C. A. Handwerker, U. R. Kattner, and M. E. Williams

"NIST personnel brought unique skills and expertise to both NCMS projects [Lead-Free Solder Project, and High Temperature Fatigue Resistant Solder Project]. Without the support from NIST, both these projects would have extended over a longer period of time and would have been more costly to the project's industrial partners. In the case of the Lead-Free Program, a critical evaluation of the data would not have been done without NIST's leadership." Duane Napp, Program Manager, National Center for Manufacturing Sciences (NCMS).

"As a result of NIST's involvement, I feel NEMI has been successful in responsibly leading the effort to understand the implications of lead-free assembly in a way that is benefiting the entire electronics assembly industry."
Edwin Bradley, Motorola and National Electronics Manufacturing Initiative (NEMI).

The U.S. microelectronics industry has clearly articulated the measurement needs for Pb-free solders and for solderability and assembly. For example, the urgency for materials data for Pb-free solders has been specified in the 1997 Association Connecting Electronics Industries (IPC), 1999 ITRS, 2000 NEMI, and 2000 Lead-Free Solder Roadmaps. Pressure from the Japanese consumer product market and from the E.U. to produce lead-free microelectronics continues to increase. In addition, the lack of understanding and control of current standard solderability measurements has inhibited the development of improved measurements necessary for new solders and for new packaging schemes. These industrial needs are addressed under this NIST project.

Objective:

To provide data and materials measurements of critical importance to solder interconnect technology.

Customer Needs:

Solders and solderability are increasingly tenuous links in the assembly of microelectronics as a consequence of ever shrinking chip and package dimensions and of the movement toward environmentally friendly lead-free solders. We are providing the microelectronics industry with measurement tools and data to address solder problems. A thermodynamic database has been publicly distributed for modeling lead-free solder systems. We also work closely with industry groups on measurement tools needed for development of lead-free solders for use in harsh environments, and provide guidance for adoption of these solders into assembly processes through work with industrial standards organizations.

Technical Strategy:

Employ advanced methods of metallurgical microstructure analysis, phase diagram calculations and kinetic analysis to provide data and materials measurements of critical importance to solder interconnect technology.

Accomplishments:

NIST has taken a major role working with industry through a NEMI Task Force to identify and move Pb-free solders into practice. NIST co-chairs the NEMI alloy selection group which this year selected standard alloy compositions

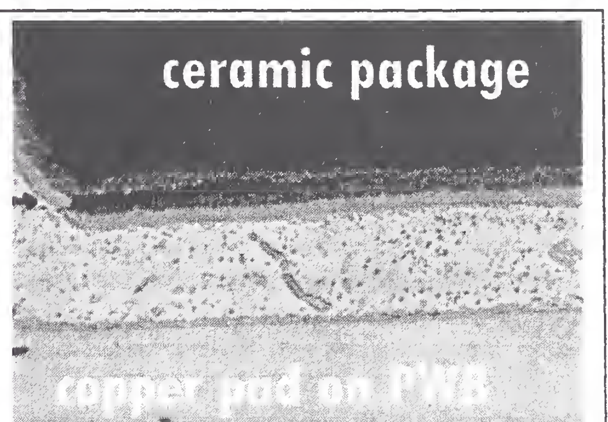


Fig. 1 - Metallographic cross-section of a new lead-free solder developed under the NCMS High-Temperature Fatigue Resistant Solder project. The alloy has excellent thermal fatigue properties.

for U.S. microelectronics assembly. NIST is also active in the NCMS High Temperature Fatigue Resistant Solder Consortium and, as in the NEMI Task Force, leads the alloy selection task group. The NCMS consortium, including Ford, Delphi, Allied Signal, Rockwell, Amkor, Heraeus, Johnson Manufacturing, and Indium Corporation, has identified and thermally cycle tested several Pb-free alloys for applications as high as 160 °C. In the past year NIST has been responsible for analyzing microstructure evolution during thermomechanical fatigue. A microstructure of one of the high temperature, high fatigue resistant, lead-free solders after thermal cycling is shown in Fig.1. The final report is due in early 2001.

NIST has developed the database necessary to calculate multicomponent phase diagrams essential for Pb-free alloy development. The experimental determination of phase diagrams is a time-consuming, costly task requiring expert interpretation of results. The calculation of phase diagrams significantly reduces the effort required to determine phase evolution in multicomponent systems and can provide quantitative information that is frequently needed in other modeling efforts. During the past year the NIST thermodynamics database for solders was expanded. Of particular importance is the development of a refined thermodynamic description for the Sn-rich part of the Sn-Ag-Cu system that was critical for alloy selection by the NEMI Lead-Free Task Force.

We are also working in collaboration with IPC Standards Committees (most closely with members from Celestica, Lucent, Raytheon, Rockwell, and Shipley-Ronel) to establish reproducible solderability test standards for board assembly. Activities include providing benchmark experiments for the wetting balance tests to predict on-line solderability for a wide range of surface finishes, lead materials, and solder alloys. New NIST research to develop electrochemical solderability tests and an understanding of whisker formation in Sn-based, Pb-free electroplated surface finishes complements the solderability studies. Highlights from this work include:

- Sources of uncertainty have been established for wetting balance solderability tests, leading to increased repeatability and reproducibility of tests.
- Recent flux studies performed at NIST have led to a change in test procedures for the IPC J-ANSI solderability standard.

Future Plans:

We will continue working with the NEMI consortium to establish suitability of particular lead-free solder compositions. In addition, solderability tests will be developed working with the IPC lead-free solder sub-committee. Databases for phase diagrams and thermodynamics critical to solder development and for mechanical properties of solder will be expanded and distributed via the web. In addition, a much needed guide to interpretation of thermal analysis data will be produced.

Collaborations:

D. Napp (National Center for Manufacturing Sciences, and associated consortium members); R. Gedney (NEMI Lead-Free Task Force, and associated consortium members).

External Recognition:

Best Technical Paper at the October 1999 IPC International Summit on Lead-Free Assemblies -- voted by the 400+ attendees of the Summit.

Publications:

K.-W. Moon, W. J. Boettinger, U. R. Kattner, F. S. Biancaniello and C. A. Handwerker, "Experimental and Thermodynamic Assessment of Sn-Ag-Cu Solder Alloys," J. Electronic Materials, 29 (2000), pp. 1122 - 1136.

K.-W. Moon, W. J. Boettinger, U. R. Kattner, F. S. Biancaniello and C. A. Handwerker, "The Ternary Eutectic of Sn-Ag-Cu Solder Alloys," Proceedings of 2000 SMTA Conference, (pub. by Surface Mount Technology Assoc. Edina, MN) 2000. p. 941-944.

K.-W. Moon, W. J. Boettinger, U. R. Kattner, C. A. Handwerker and D. –J. Lee, "The Effect of Pb Contamination on the Solidification behavior of Sn-Bi Solders," J. Electronic Materials, 30 (2001), pp. 45-52.

J. Bath, C. Handwerker, and E. Bradley, "NEMI Group Recommends 'Standardized' Lead-Free Solder Alternative," Circuits Assembly (2000).

C. Handwerker, R. Noctor, and G. Whitten, "Reliability of Lead-Free Solders," published in Lead-Free Solders, Ed. Jennie S. Hwang (2000).

Wire Bonding to Cu/Low-k Semiconductor Devices

Technical Contacts:

George Harman*, David Kelley, and Chris Johnson*

George Harman is the author of *Wire Bonding in Microelectronics* and an internationally acclaimed expert in the area of wire bonding and packaging of semiconductor chips. His current work with in collaboration with ISMT on the leading edge technology of wire bonding to advanced copper/Lo-K chips and measurements of temperature during wirebonding is critically important to advancing the industry. **Rod Auger, ISMT** (2002).

Objective:

To develop the best, most economical, practical bonding surface(s)/sub-surface support structures and techniques for wire bonding to advanced semiconductor devices with copper metallization and to resolve metallurgical diffusion issues that relate to these surfaces/structures.

Customer Needs:

The U.S. semiconductor industry needs to broadly implement copper intraconnections on the chip to maintain our competitive world position. Wire bonding is the dominant method of interconnecting the chip to the package. The work in this program is being developed in collaboration with ISMT. Through its consortial interactions, ISMT is uniquely able to provide the appropriate material samples for experimental work. In addition, NIST is able to supply new types of plating materials for evaluating the deposition processes and measurement techniques used therein.

Technical Strategy:

The highest priority is to determine the optimum (bondable/protective) metal surface to place on top of the copper pad. Gold plating, electro/electroless is considered the best, but diffusion of the base copper can limit its usefulness. The literature has contradictions as to diffusion coefficients, and they can vary, depending upon the impurities in both the copper and the gold. Measurements will be made on samples similar to those used in the industry. Other top metal surfaces will also be evaluated. As appropriate, such evaluations will be made using Auger and other measurement techniques. Verification will be carried out by wire bonding bondability experiments. A new approach is also being pursued in which copper pads are protected with a thin (50 Å) layer of inorganic material (patent applied for). ISMT is cooperating by supplying Cu LoK wafers.

Accomplishments:

Patent entitled: **"Inorganic Non-Metallic, Wire Bondable Top Surface Coating For Use In Wire Bonding To Copper Metallization On Semiconductor Chips."**

Tin Whisker Mechanisms

Technical Contacts:

C. E. Johnson, W. J. Boettinger, Kil-won Moon and M. E. Williams

The electrodeposition of metallic alloys has been central to the growth of the electronics and magnetic recording industries. This is largely due to the exceptional properties exhibited by electrodeposited material as well as the favorable economy of scale associated with electrodeposition processes. Composition and microstructure are generally controlled by electrolyte composition, solution hydrodynamics and electrode potential. A technology important to electronics manufacturing is the electrodeposition of lead-free Sn-based protective coatings to guarantee solderability during microelectronics assembly. Unfortunately, tin "whiskers" are prone to form in electrodeposited tin which can lead to short circuits of an assembly. Whiskers are generally believed to grow to relieve residual stress in electroplated Sn. However the origin of the stress is not clear. Grain size and deposit thickness also should play a role.

Objective:

Develop plating methods to control grain size, residual stress and alloy composition, and thereby elucidate the mechanism for whisker growth and develop suitable plating approaches to prevent their formation.

Customer Needs:

Through participation in the National Electronics Manufacturing Initiative (NEMI) working group on Pb-free solder alloys, it was learned that significant industrial problems had arisen due to contamination of Pb-free solders by the Pb contained in the protective solder coatings that are used on Cu leads. The protective layer deposited on Cu is usually referred to as a "pretinned" coating and is required to maintain solderability of the component during storage prior to assembly. Thus the development of Pb-free alloy platings to replace Pb-containing protective layers is considered important.

Technical Strategy:

It is well known that the use of pure Sn protective deposits has serious problems. Sn whiskers (1 μm diameter and several mm long) can grow from the Sn plate and cause electrical shorts and failure (see Fig. 1). Historically Pb was added to Sn plate to prevent whisker growth as well as to lower cost. In the current research program, it was decided to focus this project on Pb-free Sn-rich deposits with alloying additions that would retard whisker formation. The Sn-Cu system was chosen, as the Sn-Cu-Ag is likely to be the Pb-free bulk solder of choice for industrial application. The basic idea is that the substitution of a different solute for Pb in the Sn-rich deposit will also retard whisker growth.

Accomplishments:

Initial experiments were performed to establish the feasibility of Cu-Sn codeposition. In the case of the Sn-based electrolytes containing copper sulfate, one can assume that the copper deposition reaction proceeds at the diffusion-limited current density. The theoretical alloy composition can then be calculated assuming a Cu(II) diffusion coefficient of 5.0×10^{-6} cm^2/sec, a diffusion layer thickness of 100 μm, and a Sn current efficiency of 80 %. As expected, the theoretical alloy composition increased linearly with the Cu(II) electrolyte concentration. It is also clear that the experimental alloy compositions deviate from those expected based on calculations that assume a diffusion limited copper reaction. This is likely due to an error in our estimated diffusion layer thickness and indicates that rigorous hydrodynamic control should be implemented in future experiments. If such changes in the experimental set-up are implemented, rigorous control of the alloy composition can be obtained.

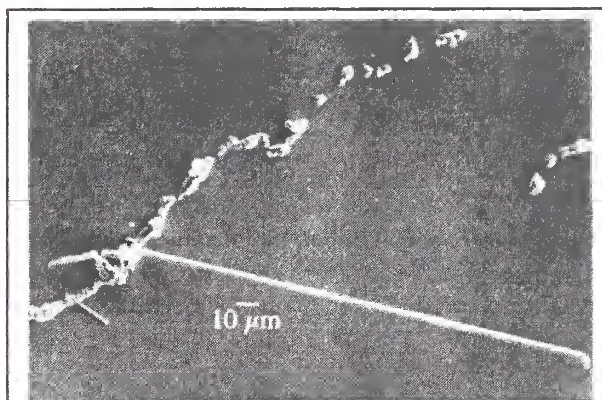


Fig. 1 - An example of a Sn whisker that grew from an electroplated deposit at room temperature.

We have constructed a rotation electrode plating cell to reproducibly deposit Sn and Sn alloy coatings. A variety of substrates will be employed to determine the effect of substrate including amorphous carbon, vapor deposited Cu and electroplated Cu and Sn. Special emphasis is being focused on the characterization of the grain size, surface topography and residual stress. The last is being measured using x-ray 'sine-squared - psi' analysis.

Future Plans:

A detailed microstructural comparison of deposits with high and low whiskering tendency is being conducted. Sn grain size, shape, preferred orientation and residual stress will be measured. The dominant mechanism(s) for whisker growth will be determined.

Wafer Level Underfill Experiment and Modeling

Technical Contacts:
D.Josell, W.E. Wallace, and D. Wheeler

Objective:

Provide computer simulation and materials data that show the behavior to be expected during assembly of flip chips that have an underfill/solder bump system applied at the wafer level. Examine experimentally the validity of computer modeling efforts.

Three specific goals of this project are: 1) create modeling software for evaluating capillary induced realignment forces; 2) carry out validation experiments for realignment forces provided by solder joint to misaligned pads; 3) develop a model incorporating capillary realignment forces as well as viscous forces retarding realignment associated with polymer underfill material.

Customer Needs:

For area array flip chip applications, the microelectronics industry has a well established need for an underfill system that obviates the time-consuming flow required by current viscous underfill materials. The most promising route to accomplishing this is the application of an integrated underfill/solder bump system at the wafer stage. Such a process involves the reflow of an area array of solder joints during attachment of the chip to the package or, as in direct chip attach, to a printed circuit board.

This project addresses the critical problem of wetting behavior of solder in such solder joint interconnections under the constraints found in the wafer-level underfill systems. The pre-existing underfill geometry provides constraints on the flow of the solder, influencing the self-alignment of the die and final solder joint geometry. These factors have profound effects on joint reliability. Thus, behavior of the solder during reflow is a critical aspect of the underfill system, which is itself supposed to enhance reliability.

Technical Strategy:

The technical approach is triparte, with the parts corresponding to each of the three principal goals of the project. The first part is creation of modeling software for evaluating capillary induced realignment forces. This is being accomplished within the larger framework of the NIST Center for Theoretical and Computational Materials Science (CTCMS) effort to create a library of code for evaluating industrially relevant solder joint geometries. As with the broader CTCMS effort, the codes for the solder joints relevant to this project are based on the Surface Evolver computer program. Benefits of this program are its substantial incorporation into industrial solder joint efforts and the generality of the joint geometries that it can be used to evaluate. A potential drawback of the code is that it includes only capillary and gravitational forces.

The second part of the project is an effort to experimentally measure the capillary realignment forces for different pad dimensions and solder volumes. In these experiments two eight-pad chips are joined using solder joints with volumes between 0.23 nm and 0.0019 mm^3. The loading conditions are systematically varied and the post-solidification solder joint geometry measured in order to obtain the force-displacement relationships for the solder joints under both aligned and misaligned conditions, see Fig.1. These results are

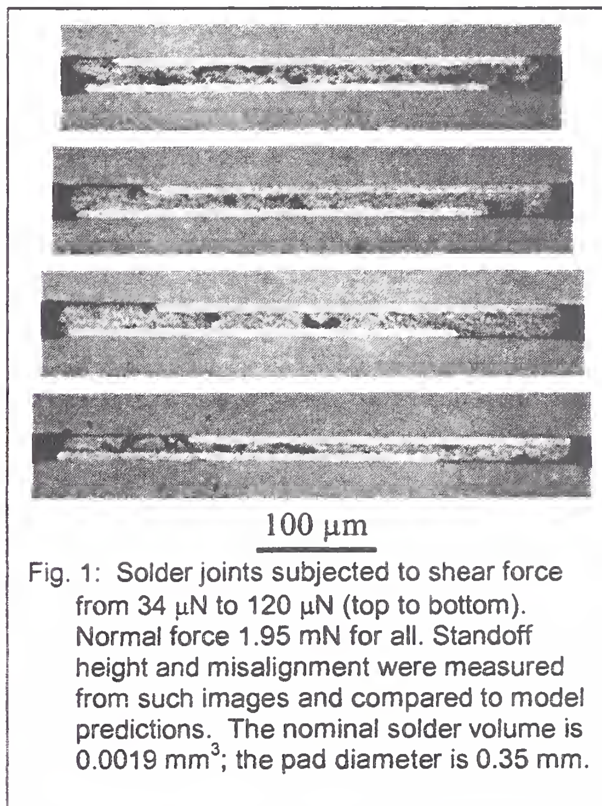


Fig. 1: Solder joints subjected to shear force from 34 μN to 120 μN (top to bottom). Normal force 1.95 mN for all. Standoff height and misalignment were measured from such images and compared to model predictions. The nominal solder volume is 0.0019 mm^3; the pad diameter is 0.35 mm.

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being compared to results predicted in the modeling effort in order to assess the validity of using only capillary and gravitational forces to predict solder joint geometries.

The third part of the this effort will incorporate the modeling and experimental solder joint results along with viscosity-temperature data for relevant polymer underfill material to predict self-alignment behavior as a function of temperature.

Accomplishments:

Software based on the freeware Surface Evolver code has been written that allows modeling of two relevant joint geometries. This software was placed in the CTCMS web site http://www.ctcms.nist.gov/~djl/solder/new.html as part of the library of Evolver files modeling different industrial solder joint geometries. Specific output of this software includes predictions of equilibrium solder joint geometries as well as force-displacement relationships for two pads joined by a solder joint. The user-specified separation between the pads can be such that they are aligned or misaligned.

Force-displacement relationships have been measured for solder joints with volumes between 0.23 and 0.0019 mm^3. The loading conditions were systematically varied and the joint geometry measured in order to obtain the force-displacement relationships for the solder joints under both aligned and misaligned conditions. These results have been compared to results predicted in the modeling effort to assess the validity of using only capillary forces to predict solder joint geometries. Wetting experiments were also conducted to obtain contact angles required for the modeling.

Future Plans:

We plan to measure viscosities of relevant underfill materials and incorporate them into a model with the restoring forces provided by the solder joints to facilitate prediction of processing cycles compatible with flip-chip self-alignment.

Publications:

D.Josell, W.E. Wallace, J.A. Warren, D. Wheeler, and A.C. Powell IV, "Misaligned flip-chip solder joints: predition and experimental determination of displacement curves," J.Electron. Pack., submitted.

Solder Interconnect Design

Technical Contacts:
J.A. Warren and C.A. Handwerker

"The introduction of the Surface Evolver software tool into Motorola's electronic packaging applications has proved that it is a very useful tool for eliminating any solder defect for reflow processing. Time and time again, it has reduced design cycle time, cost of tool or printed wire board (PWB) modifications, and cost of prototyping and testing. Right now, there are about 10 Evolver users in Motorola,"
Dr. Xiaohua Wu, Senior Staff Engineer, Motorola.

"Results from the solder interconnect design team (SIDT) workshops have provided guidance and root cause analysis (to Ford) to achieve projected manufacturing success,"
Dr. Tsung-Yu Pan, Ford Motor Company.

Objective:
The goal of the SIDT is to provide the industrial community with a suite of useful software tools for solder interconnect design, and to provide a set of standard reference problems. With this in mind, the SIDT actively supports the development of modeling tools based on the public domain program Surface Evolver, which has been shown to be extremely effective for computing equilibrium solder meniscus shapes (see Fig. 1).

Customer Needs:
The SIDT was formed to address several pressing issues in the design and assembly of circuit boards. This multi-billion dollar industry is highly dependent on solder interconnects as the primary method for attaching components to circuit boards. Such assemblies involve the correct application of thousands of solder interconnects. Failure of any of these joints due to short or open circuits can render the product useless or require expensive reworking. Thus the microelectronics industry benefits from any modeling technique which allows for accurate prediction of the failure of these solder interconnects. One of the key bottlenecks to accurate modeling of the failure of these joints has been the lack of realistic input shapes into existing finite element models of reliability.

Technical Strategy:
In order to achieve its goals, the SIDT has established and fostered an industry-academia-government laboratory working group on solder joint design for the exchange of information and collaboration on topics of special importance. The SIDT acts as a forum for discussion of Evolver calculations and models and, through the CTCMS, provides access to software through the Internet/WWW. Software downloads from the SIDT website number in the thousands per year. In addition, the SIDT also seeks to hold workshops and symposia to promote collaboration and bring the community toward a consensus on the features required for a useful solder joint modeling system.

Accomplishments:

The SIDT has had eight workshops over the past six years, providing the critical input from industrial partners necessary to ascertain what modeling priorities exist. Software downloads from the SIDT website number in the thousands per year, and this resource will remain after the SIDT ceases existence. In general, the designers of microelectronic assemblies are now aware of the modeling capabilities promoted by the SIDT, and thus are able to take advantage of the modeling resources that have been made available as the need arises. Generically, the SIDT-promoted technology allows

Fig. 1 Surface Evolver calculation of the geometry of a solder drop in a gull-wing lead.

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electronic devices to be designed to be smaller, lighter, cheaper and more durable, and second, failures of assembly processes can be analyzed and corrected far more easily, saving time and money. For example Motorola needed to solve a particular problem with their two-way radio applications. Namely "a serious, urgent problem was encountered with electromagnetic shield cans falling off from the PWBs as soon as the oven temperature exceeded the solder melting temperature. In spite of an elaborate, experimental based effort by the product group, the defect rate was still unacceptable (around 2 %). Typically, any modification of the production tooling and pad redesign will take anywhere from 2 to 6 weeks. To investigate the root causes of this fall-off phenomenon, [we simulated] the unbalanced surface tension in the molten solder, which caused the floating/twisting problem… Surface Evolver played a very important role in helping our engineers understand the root causes of the floating/twisting problem. This problem was completely eliminated after a new design, based on the simulation results, was implemented. This effort allowed products to be shipped 2 months earlier than what was scheduled." (X. Wu, Motorola)

Future Plans:

The SIDT exists purely as a WWW presence. The software archive will be maintained as long as is deemed necessary.

Collaborations:

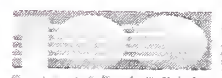
SIDT Partners include: Edison Welding Institute, DEC, Motorola, BOC Gasses, Ford Motor Co., Lucent Technology, AMP, Rockwell, Delphi Automotive Systems (Delco), Texas Instruments (Raytheon), Susquehanna University, University of Colorado, University of Massachusetts, University of Wisconsin, University of Loughborough, Lehigh University, University of Greenwich, Marquette University, RPI, University of Minnesota and Sandia National Laboratory.

External Recognition:

In recognition of its efforts, in 1999 several core members of the SIDT received the Federal Laboratory Consortium Award for Technology Transfer

Publications:

http://www.ctcms.nist.gov/programs/solder/



X-ray Studies of Electronic Materials

Technical Contacts:
T.A. Siewert, *D. Balzar, Chris McCowan*

Objective:

Develop high-energy x-ray diffraction, as a nondestructive technique, to identify and quantify intermetallic layers between solder balls and copper pads which may affect reliability.

Customer Needs:

The quality of the interface between solder and the copper pad (on the circuit board) is a key component in the reliability of printed-circuit boards. The reliability of these joints is becoming even more important with the advent of higher pin counts and finer pitch products, such as ball grid array (BGA) technology and chip-scale packages (CSP). Brittle failure of these joints (and so failure of the entire board or system) is observed in service under conditions of extended thermal cycling, vibration, and thermal or mechanical shock. The brittle fracture often initiates in and propagates through the intermetallics that grow at the interface between the solder and a protective buffer layer on the contact pads.

Currently the industry is switching to electroless Ni/Au, which is increasingly used in high-density BGA packages and flip-chip applications, where the problem of intermetallic growth is even more severe. The current interest in lead-free alloys, especially those high in Sn, increases the need for better measurement techniques for these degradation mechanisms.

Technical Strategy:

Currently, the growth of intermetallics is diagnosed destructively; shear testing is used to measure the joint integrity, then the fracture surfaces are examined by light and SEM. Unfortunately, the SEM's energy-dispersive x-ray capability has some limitations. The technique has a limited penetration depth (only a few micrometers) and then is able to identify only chemical elements and approximate stoichiometry of intermetallic compounds, not the crystallographic phases present at the interface. Perhaps the greatest disadvantage of optical or SEM examination of the intermetallics is that the short penetration depth requires the solder joint to be cross-sectioned. The x-ray diffraction technique permits direct and unequivocal identification of the crystallographic phases in a solder joint. Furthermore, a high-energy x-ray beam (up to 320 keV) can penetrate a circuit board and the attached devices to the buried intermetallic layer, and therefore nondestructively identify compounds detrimental to the package's reliability. Because the diffraction intensity is proportional to the concentration, the method can also estimate the relative concentration of the intermetallics.

Accomplishments:

We prepared bulk intermetallic samples from Cu and Sn powders by solid-state reaction at elevated temperature. The reference diffraction patterns of the Cu-Sn intermetallic phases were then recorded by 8 keV x-rays (Cu-Kα characteristic radiation), and found to be close to that of the $Cu_{6}.26Sn_{5}$ structure. Furthermore, we made samples with an intermetallic layer by prolonged aging of soldered copper boards at elevated temperature. We used lead-free solders with the composition Sn-3.7 % Ag. The existence of the intermetallic layer was confirmed by both light microscopy and SEM. Figure 1 shows an optical micrograph with intermetallic layer clearly visible. Its average thickness is estimated at 5 μm, and the approximate composition, as determined from the line

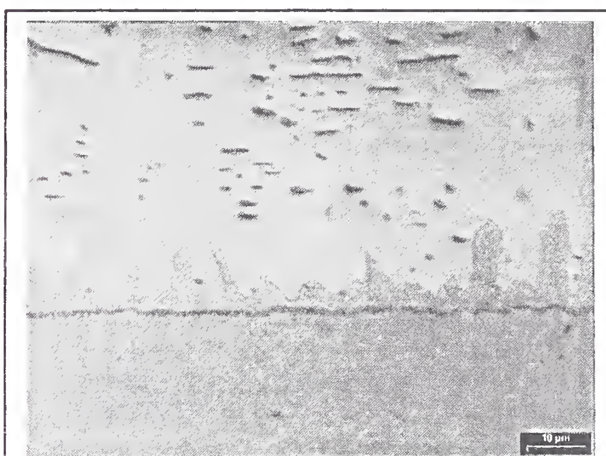


Fig. 1. Optical micrograph of the copper-solder interface. Adjacent to the copper (at the bottom) is a 1 μm thin darker region, Cu_3Sn, followed by the irregularly shaped Cu_6Sn_5 intermetallic layer, which ranges between 5 μm and 10 μm thick.

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EDS scan, is somewhat richer in tin than that of the $Cu_6.26Sn_5$ structure.

The 8 keV x-rays cannot penetrate more than 10 µm of Cu and much less of Pb. Therefore, we used a high-voltage (up to 320 kV) industrial x-ray tube with a W target to try to nondestructively identify buried intermetallic layers. A W target produces a characteristic Kα energy of 59 keV, which extends the penetration depth in most materials from the micrometer to the millimeter range. In this particular case, diffraction patterns can be recorded in both transmission and reflection geometries. We determined that the latter yields both better resolution and higher intensity. However, because at high energy Bragg reflections move to smaller diffraction angles, the diffraction pattern becomes even more cluttered, which makes the detection of intermetallics diffraction lines even more challenging. The calculated diffraction pattern at 59 keV for the solder alloy with intermetallics confirms that this pattern is complex and resolution is dependent on the instrument and the diffraction-line broadening. To test how much a high degree of diffraction-line overlap prevents a positive identification of the intermetallic layer, we prepared two samples: one was normally prepared by soldering and in the other solder was mechanically pressed and glued to the back of the Cu board, and so does not contain any intermetallic phase. This test illustrated that, although there is a strong indication that the additional peak is given by an intermetallic phase, the final proof is likely to require significantly improved instrumental resolution.

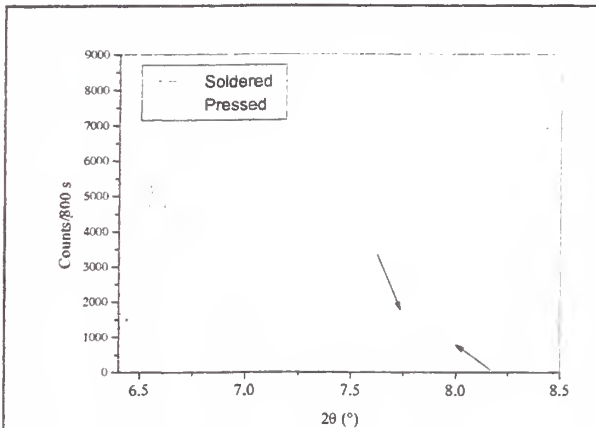

Fig. 2. Diffraction patterns of two specimens: soldered Cu board (solid line), where an additional reflection (indicated by an arrow) is possibly due to an intermetallic phase, and another specimen where solder was mechanically pressed and glued to the back of Cu board (dashed line).

Future Plans:

We just acquired a new high-brightness x-ray source and a very precise positioning stage that overcome the limitations of our existing equipment. New experiments with such improved equipment are under way, which should greatly improve our quantification of intermetallic buried layers.

Publications:

T.A. Siewert, D. Balzar, and C.N. McCowan, "Nondestructive Detection of Intermetallics in Solder Joints by High Energy X-ray Diffraction," Proceedings of ECTC, (2001).

Packaging Reliability

Technical Contacts:
E.S. Drexler and A.J. Slifka

"Packaging cost is a second area that could be an obstacle to realizing the potential of advances in silicon technology. …the average packaging share of total product cost will double over the next 15 years and, more significantly, the ultimate result will be greatly reduced gross profit margins, limiting investments in R&D and factory capacity." -- **2000 NEMI Roadmap**

Objective:

The goal of this program is to characterize the integrity of interfaces contained in electronic packaging through the use of thermal microscopy and electron-beam moiré. The complementary techniques reveal the change in thermal resistance across and the strains calculated at an interface that is experiencing thermal fatigue.

Customer Needs:

The trend in electronics is toward components of higher density and smaller size using less expensive materials. Materials used in packaging are many and display a variety of behaviors that are not always compatible. This makes interfaces particularly vulnerable to thermomechanical fatigue failures. The electron-beam moiré program seeks to offer support and verification of models conducted or sponsored by the microelectronics industry. The technique allows the researcher to observe the substrate throughout the thermal cycling so that one can identify the locations and materials in which deformations are occurring.

The physical size of nearly all electronic devices is decreasing rapidly and, at the same time, their capabilities are increasing dramatically. One move in this direction is the advent of integral passive components and another is the increasingly prevalent use of organic (polymeric) conductors and fillers. These organic materials have a large coefficient of thermal expansion, which can reduce the reliability of electronic packaging systems. We are investigating interfaces between organic materials and between organics and metals to determine the initiation of damage and failure mechanisms in these material systems.

Technical Strategy:

We are using two different measurement techniques to evaluate these materials. In characterizing thermomechanical fatigue; electron-beam moiré gives local strain data in small features in the package, whereas thermal microscopy provides data on initiation and evolution of thermal damage at interfaces. These two methods yield a more complete picture of the fatigue behavior of packaging materials. Electron-beam moiré is unique as it can measure small displacements (minimum displacements range from approximately 25 nm to 100 nm, depending on the pitch of the grating lines) at temperatures between –55 °C and 150 °C, the maximum range used by industry for qualification of packages. Fig. 1 shows data typical of electron-beam moiré. Thermal microscopy has a spatial resolution of 10 μm and thermal resolution of 0.3 °C on a 1.6 mm field of view.

Accomplishments:

A test on the Motorola specimen was completed and it was determined that the microvias resisted deformation despite the highly expansive material surrounding them. The results were presented and well received at Electronics Components and Technology Conference (ECTC) in May 2000. The accompanying paper was published in the Proceedings of ECTC. We commissioned an outside contractor to develop software to aid in fringe identification and analysis. The software was received and it greatly facilitates the reduction and analysis of the moiré fringe data. A new field emissions SEM (FE-SEM) was purchased. It is hoped that we will be able to transfer our lithography capabilities to that microscope.

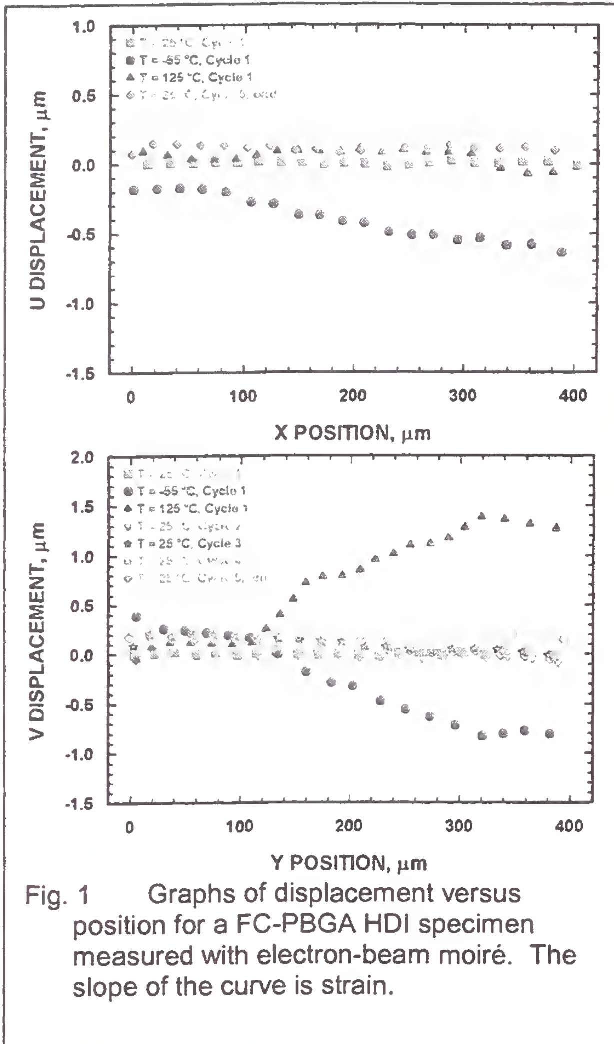

Fig. 1 Graphs of displacement versus position for a FC-PBGA HDI specimen measured with electron-beam moiré. The slope of the curve is strain.

We developed infrared (IR) microscopy for measurement of heat flow and examined interfaces in a sample containing two conductive adhesives, printed wiring board, and stainless steel. The sample was measured at various stages of thermal cycling from –55 °C and 125 °C. The regions examined by IR microscopy were also measured with electron-beam moiré. Moiré was able to show the regions where damage was most likely to initiate, while IR microscopy tracked changes in interfacial thermal resistance at the interfaces. IR microscopy was able to detect damage before it was manifested at the surface and viewable by common techniques such as optical or electron microscopies. Electron-beam moiré showed accumulated strain in the materials and evidence of residual accumulated stress at interfaces as thermal cycling progressed. This work was presented at the 50th ECTC.

Work has begun on IR microscopy of organic electronic elements using Joule heating. This approach will localize heat as it would occur in-service and allow us to assess the validity of thermal cycling as the accepted method of accelerated failure in electronic packaging materials. Fig. 2 shows an IR microscope image of an integral resistor sandwiched between printed wiring board and a thermally conductive adhesive.

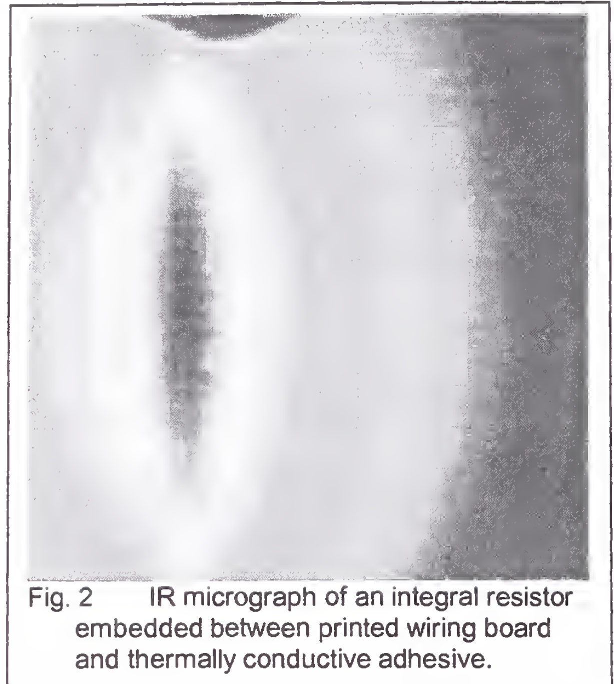

Fig. 2 IR micrograph of an integral resistor embedded between printed wiring board and thermally conductive adhesive.

Future Plans:

We will study embedded and integral passive components from industrial manufacturers. Joule heating and conventional laser heating of thermally-cycled specimens will be compared to determine if the heating mechanisms result in similar interfacial damage. The atomic force microscope will be utilized as a tool to extend these measurement techniques to ever-finer size scales.

Collaborations:

Robert Munroe, Motorola, Austin, TX; Joe Kuczynski, IBM, Rochester, MN; Virang Shah, MicroFab Technologies, Plano, TX

External Recognition:

Invited talk at the Annual Meeting 2001; invited talk at the Thermal Materials Workshop 2001

Publications:

Drexler, E.S., "Plastic Strain in Thermally Cycled Flip-Chip PBGA Solder Balls," Proceedings of the 1999 International Electronics Manufacturing Technology Symposium, Austin, TX, 239 (1999).

Drexler, E. S., "Thermally Induced Deformations in a Flip-Chip HDI Substrate," Proceedings of the 50th Electronic Components and Technology Conference, Las Vegas, NV, 650 (2000).

Slifka, A. J. and Drexler, E. S., "Characterization of Interfaces Involving Electrically Conductive Adhesives using Electron-Beam Moiré and Infrared Microscopy,",Proceedings of the 50th Electronic Components and Technology Conference, Las Vegas, NV, 403 (2000).

Drexler, E. S., "Plastic Strain in Thermally Cycled Flip-Chip PBGA Solder Bumps," IEEE Transactions on Advanced Packaging, 23, pp. 646–651 (2000).

Permittivity of Polymer Films in the Microwave Range

Technical Contacts:
J. Obrzut and *C. K. Chiang*

A need for a new standard test method for permittivity of high k films at frequencies from 1 GHz to 5 GHz was identified by **Standard 4902, Embedded Passive Devices, Task Group 3-12j.**

Objective:

To develop techniques for accurate measurement of permittivity at microwave frequencies and the fundamental framework for identifying the key structural and molecular attributes that control the dielectric properties of polymer composite films.

Customer Needs:

High dielectric constant polymer composite materials are being developed by the electronics industry in response to the need for power-ground decoupling to secure integrity of high speed signals and reduce radiated noise. Current technologies utilize surface mounted discrete chip capacitors, which can extinguish the power-bus noise at frequencies below 10 MHz. At higher frequencies, between 10 MHz and 100 MHz, only capacitors with the lowest connection inductance are able to source the charge. As the operating frequency increases above several hundred MHz, all the discrete capacitors become ineffective. To respond to these inherent problems, NIST and more than a dozen partners organized a collaboration research consortion with the purpose of developing and advancing the use of embedded-decoupling-capacitance (EDC) technology. The consortium identified a need to assess the feasibility of this design and to measure the materials dielectric characteristics at frequencies above 1 GHz.

Technical Strategy:

We investigated the possibility of measuring broadband permittivity of dielectric films by using coaxial configuration and by employing an appropriate theoretical model for the wave propagation in the specimen section. We found that neglecting the wave propagation, which is the current approach, leads to large systematic errors at microwave frequencies. This finding leads to a new analytic method of data reduction to cover a frequency range above 1 GHz (Fig. 1).

Accomplishments:

Using our new broadband technique we evaluated the microwave dielectric properties of several polymer-ferroelectric ceramic composites newly developed by the industry for applications: BC2000 and EmCap from PolyClad, CPly from 3M and HiK Polyimide from DuPont. The EDC materials measured in a functional test vehicle configuration showed an exceptionally low and flat impedance characteristic, indicating a much lower Q factor than could be expected from the dielectric properties of the organic and ceramic constituents.

Our study on model polymeric composites loaded with ferroelectric powders reveals an enhanced

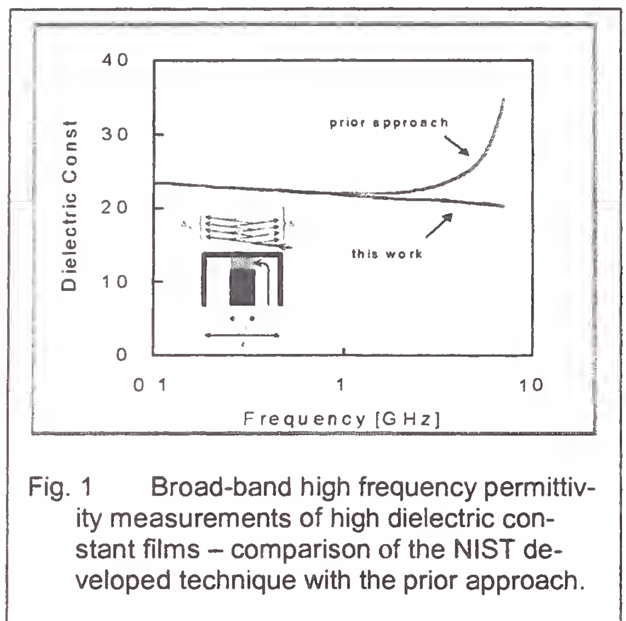

Fig. 1 Broad-band high frequency permittivity measurements of high dielectric constant films – comparison of the NIST developed technique with the prior approach.

high frequency relaxation behavior. The position of the loss peak is controlled by the dielectric relaxation of the polymer resin while its magnitude depends on the dielectric dispersion, and therefore, is amplified by the content and permittivity of the ferroelectric component. To control both the position and the magnitude of dielectric loss is highly desirable in EDC applications.

Future Plans:

We have initiated the process to promote our broadband high frequency technique as an IPC test standard. Work is also in progress to identify the molecular mechanism responsible for the enhancement of magnitude of dielectric loss in polymeric composites.

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Collaborations:

R. Nozaki, R. Popielarz (Polymers Division, NIST), J. Dougherty (Penn State Univ.), T. Hubbing (Univ. of Missouri), J. Parker (Allied Signal), Y. Lee (DuPont), J. Peiffer (3M), B. Vernell (Polyclad), T. DeRego (HADCO), J. Lauffer (IBM), D. Murry (Litton), J. Davignon (Merix), T. Tran (Raytheon), W. Li (Motorola), J. Mayers (Delphi-Delco), E. Cullens (TI), R. Charbonneau (Storage Tech.) R. Foly (DOD), L. Patch (NCMS)

Presentation:

Nozaki, R. and Obrzut, J., "Permittivity Measurements of Solid Film Dielectrics at Microwave Frequencies," IPC EXPO-00 Technical Conference.

Publications:

R. Nozaki and J. Obrzut, "Broadband complex permittivity measurements of solid films at microwave frequencies," submitted to IEEE Transactions on Instrumentation and Measurements.

Obrzut, J. and Chaing, C. K., "Microwave Dielectric Characterization of Polyaniline Composites," submitted to Organic Hybrid Materials.

Obrzut, J. and Chiang, C. K., " Embedded Capacitance Project Report," Aug. 2000

Obrzut, J.; Chiang, C. K.; Popielarz, R., and Nozaki, R.,"Evaluation of Dielectric Properties of Polymer Thin-Films Materials for Application in Embedded Capacitance," NISTIR 6537 2000 ED.

Popielarz, R.; Chiang, C. K.; Nozaki, R., and Obrzut, J., "Dielectric Properties of Polymer/Ferroelectric Cermanic Composites from 100 Hz to 10 Ghz," submitted to Macromolcules.

Popielarz, R.; Chiang, C. K., and Obrzut, J., "Polymer Composites of Very High Dielectric Constant," submitted to Thin Solid Films.

Chiang, C. K.; Popielarz, R.; Nozaki, R., and Obrzut, J., "Broadband Dielectric Relaxation of Polymer Composite Films;" MRS proceedings, Organic/Inrganic Hybrid Materials 2000; San Francisco, CA (2000).

Popielarz, R.; Chiang, C. K.; Nozaki, R., and Obrzut, J., "Preparation and Characterization of Photopatternable BaTiO3/Polymer Composites," MRS proceedings, Organic/Inorganic Hybrid Materials; San Francisco, CA. (2000).

Texture Measurements in Thin Film Electronic Materials

Technical Contacts:

M.D. Vaudin

"This is an excellent and thorough study that represents a significant improvement over the current state-of-the-art (in texture measurements)" **Thomas Shaw *(IBM Research)*, Elliott Philofsky *(Applied Ceramics Research)*, Robert Weissman *(Agilent Technologies)*; NIST Ceramics Division Thin Film Industrial Panel Report, January, 2000.**

Objective:

To provide industry with quantitative texture measurement techniques that use commonly available equipment.

Customer Needs:

Many thin film and bulk materials used in microelectronic applications have a preferred crystallographic orientation or texture. Properties of materials can be strongly affected by texture. To optimize the development and application of textured materials, it is desirable to quantify the effects of texture on properties, which requires accurate characterization tools. Specific customers in the microelectronics industry who have expressed a need for accurate texture measurements include IBM (for $Ba_{1-x}Sr_xTiO_3$ DRAM), Semitool Corporation (for Cu metallization) and Ramtron Corporation (for $PbZr_{1-x}Ti_xO_3$ nonvolatile RAM).

Technical Strategy:

Axisymmetric or fiber texture measurements in electronic films are typically reported as intensity ratios of peaks obtained from x-ray diffraction patterns. Our goal is to develop more accurate texture measurement techniques that use conventional θ-2θ x-ray diffractometers, equipment that is commonly available in industrial settings. Our approach is based upon collection of both θ-2θ and ω scans from a specimen. Texture distributions are then calculated using the θ-2θ scan to apply defocusing corrections to the ω scan intensities.

Accomplishments:

We developed a new technique for measuring fiber texture using conventional θ-2θ x-ray diffractometers. Our TexturePlus Software for data correction and texture calculation can be downloaded from the web at: *http://www.ceramics.nist.gov/webbook/TexturePlus/texture.htm*. To date, the technique has been used to measure texture in $Ba_{1-x}Sr_xTiO_3$ (BST) films for DRAM, $PbZr_{1-x}Ti_xO_3$ films for nonvolatile random access memory, and Cu films for advanced metallization. Texture profiles for a BST film with bimodal 100/110 texture are shown in Figure 1. From these results, the texture was determined to be 38 % (110) and 62 % (100); texture calculated simply from the intensity ratios yielded 25 % (110) and 75 % (100). Thus, there can be significant errors in calculating texture directly from intensity ratios without correcting for defocus in the measurement.

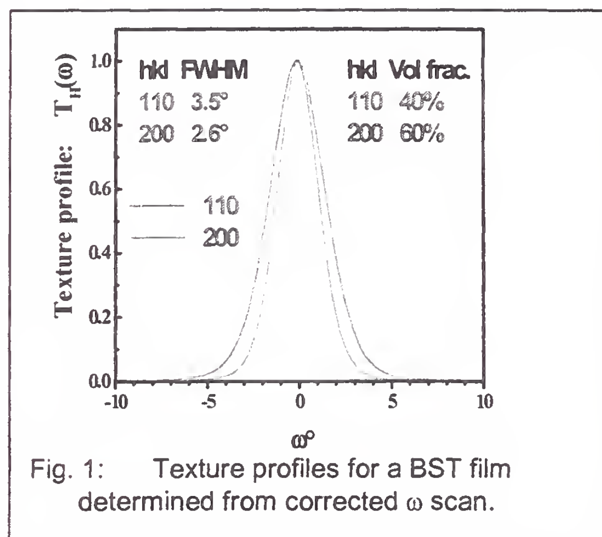

Fig. 1: Texture profiles for a BST film determined from corrected ω scan.

We organized and held a workshop on Texture in Electronic Applications at the NIST Gaithersburg site on October 10 and 11, 2000. The primary goal of the workshop was to provide a forum for the discussion of critical issues relevant to texture and texture measurement. The nearly 40 attendees were evenly divided between industry, universities and national labs. During roundtable discussions, it became clear that there is a strong need for a thin film texture standard for measurement calibration purposes. A prerequisite for standards development is interlaboratory comparisons of results obtained on the same specimens with different techniques, and also on the same specimens using the same

technique but different equipment. NIST agreed to take the lead in organizing such an activity.

Future Plans:

We will continue to design and validate texture measurement procedures for the specific needs of the microelectronics community. A round robin will be initiated this year on texture measurements; participants will include Oak Ridge National Labs, IBM, HKL Technologies and McGill University. NIST's role will be to coordinate the distribution of specimens, make measurements, and collect, collate and compare the results. In addition, NIST will work on a "Guide to Practice" on fiber texture measurements using conventional θ-2θ x-ray diffractometers. The guide will be aimed at the non-expert user, typically in an industrial setting.

Collaborations:

IBM Research *(T. Shaw)*; Ramtron Corporation *(G. Fox)*; Semitool Corporation *(T. Ritzdorf)*; Agere Systems *(G. Kowach)*; The Pennsylvania State University *(G. Messing)*; University of Pennsylvania *(P. Espinoza)*; U.C. Santa Barbara *(J. Speck)*; University of Texas *(D. Kovar)*; Carnegie Mellon *(G. Rohrer)*

External Recognition:

Invited talk: "Accurate Measurement of Texture in Thin Films," Thermec 2000, Las Vegas, NV, December 6, 2000.

Publications:

Mark D. Vaudin, Martin W. Rupich, Martha Jowett, G.N. Riley and J. F. Bingert, "A Method for Crystallographic Texture Investigations Using Standard X-ray Equipment," J. Mater. Res. 13, 10, 2910-2919 (1998). URL: ftp://www.ceramics.nist.gov/JMatRes98.pdf

Mark D. Vaudin, "Accurate Texture Measurements on Thin Films Using a Powder X-ray Diffractometer," Proceedings of the Twelfth International Conference on Textures of Materials, edited by J.A. Szpunar (NRC Research Press, Ottawa, 1999), p. 186-191.
URL: ftp://www.ceramics.nist.gov/ICOTOM.pdf

Mark D. Vaudin, Glen R. Fox, "Measuring Bimodal Crystallographic Texture in Ferroelectric $PbZr_xTi_{1-x}O_3$ thin films," to be published in "Ferroelectric Thin Films VIII, MRS Proceedings, 2000.
URL:
ftp://www.ceramics.nist.gov/BimodalTexture.pdf

Mark D. Vaudin, "Accurate Measurement of Texture in Thin Films," to be published in Journal of Materials Processing Technology, proceedings of Thermec 2000, Las Vegas, NV, Dec 4-8, 2000.

Ferroelectric Domain Stability Measurements

Technical Contacts:

G.S. White and J.E. Blendell

"Terrific work, state-of-the-art" **Thomas Shaw *(IBM Research)*, Elliott Philofsky *(Applied Ceramics Research)*, Robert Weissman *(Agilent Technologies)*, Lynn Schneemeyer *(Agere Systems);* NIST Ceramics Division Thin Film Industrial Panel Meeting, January 31, 2001.**

Objective:

1) To provide industry with quantitative measurement techniques which allow real-time determination of ferroelectric domain behavior as a function of applied electric field; 2) To provide basic understanding of microstructure effects on domain stability.

Customer Needs:

Ferroelectric thin films have the potential for making major impacts in high-density (>256 kB) non-volatile random access memory (RAM). The reliability of these devices depends upon stability of the switchable ferroelectric domains or regions containing electric dipoles of the same polarization. Industries concerned with the development of ferroelectric-based devices, which include Ramtron Corporation, Symmetrix and Agilent Technologies, need quantitative measurement techniques to evaluate domain stability (pinning, retention and fatigue) and assess the effects of microstructure and applied field on domain stability.

Technical Strategy:

The technique used to monitor domain motion is based on the piezoelectric response of a film to an applied electric field (Gruverman *et al.*, J. Vac. Sci. Tech. B, 14[2], 602 (1996)). In the measurements, an applied ac electric field (≈1 MV/m) changes the thickness of the ferroelectric film due to the piezo-electric response. Such changes are observed by atomic force microscopy (AFM) and the phase shift of the response is related to the orientation of the polarization of the sample (see Fig. 1). The spatial resolution of the technique is limited to ≈20 nm due to the contact area of the tip and spreading of the electric field. The response varies from in-phase response (polarization in the direction of the applied field) to response which is 180° out-of-phase (polarization in the opposite direction to the applied field). Various microstructural features such as grain boundaries, structural defects, and residual stress can have a strong effect on domain stability. Our approach is to measure domain stability in $PbZr_{1-x}Ti_xO_3$ (PZT) films using piezoresponse atomic force microscopy, and to correlate these measurements with local-scale residual stresses calculated from an object-oriented finite element (OOF) modeling approach developed at NIST.

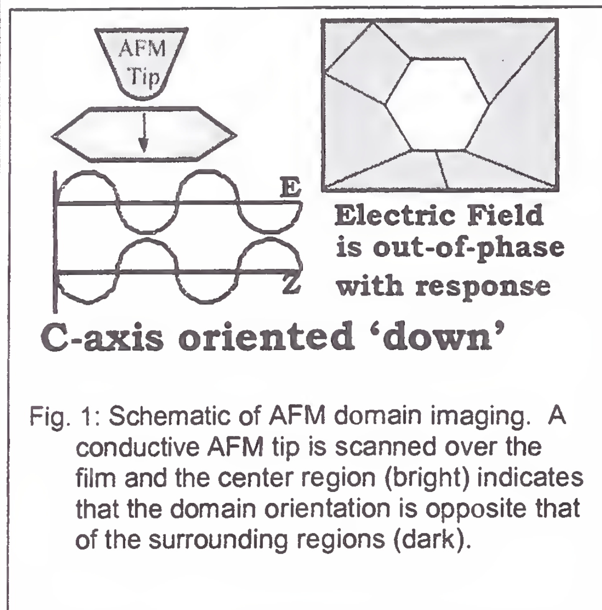

Fig. 1: Schematic of AFM domain imaging. A conductive AFM tip is scanned over the film and the center region (bright) indicates that the domain orientation is opposite that of the surrounding regions (dark).

Accomplishments:

We have observed the first direct evidence that domain pinning in PZT nonvolatile RAM films occurs at grain boundaries rather than within grains. As illustrated in Fig. 2, grain boundaries are the strongest pinning sites, with the adjacent regions resisting 180° polarization changes to higher fields. The grain boundary regions also initiate the rapid relaxation of the domains back to their original orientation. Further, these results demonstrate that domain pinning along a single grain boundary is nonuniform. Object-oriented finite element modeling has shown that stresses vary with grain-to-grain misorientation. These results are consistent with the nonuniform pinning along grain boundaries observed in the AFM measurements.

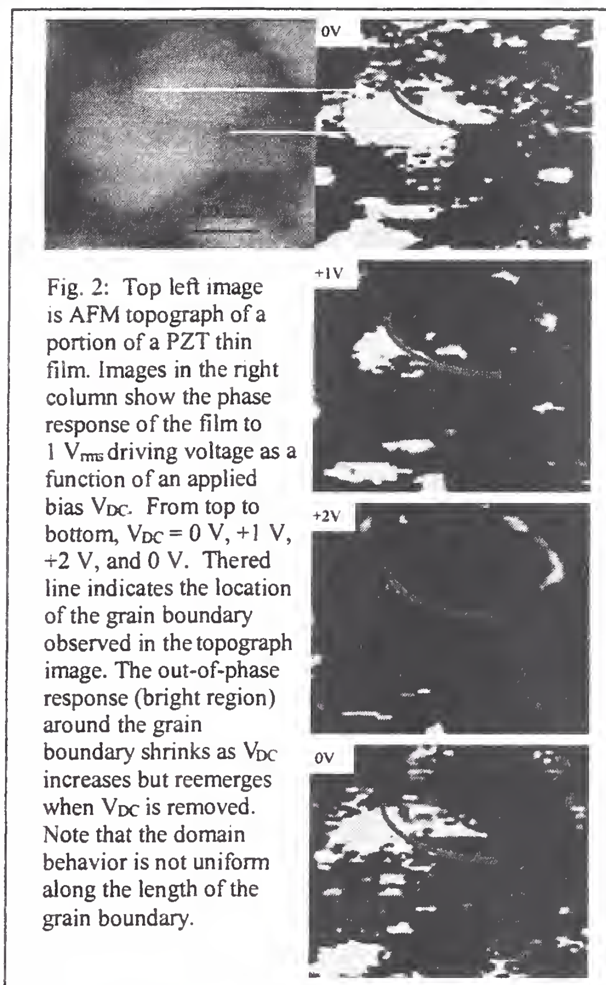

Fig. 2: Top left image is AFM topograph of a portion of a PZT thin film. Images in the right column show the phase response of the film to 1 V_{rms} driving voltage as a function of an applied bias V_{DC}. From top to bottom, V_{DC} = 0 V, +1 V, +2 V, and 0 V. Thered line indicates the location of the grain boundary observed in the topograph image. The out-of-phase response (bright region) around the grain boundary shrinks as V_{DC} increases but reemerges when V_{DC} is removed. Note that the domain behavior is not uniform along the length of the grain boundary.

Future Plans:

The domain pinning results will be correlated with crystallographic orientation of individual grains as measured using orientation imaging microscopy. We also plan to develop a method to determine if the pinning sites act as charge (electrons, holes or ions) traps. Our approach is to use the atomic force microscope coupled with an electrometer to measure current flow as the film is thermally or optically excited to release carriers.

E. Wafer Characterization and Process Metrology Program

Device scaling has been the primary means by which the semiconductor industry has achieved unprecedented gains in productivity and performance quantified by Moore's Law. Until recently only modest changes in the materials used have been made. The industry was able to rely almost exclusively on the three most abundant elements on Earth – silicon, oxygen, and aluminum.

Recently, however, copper has been introduced for interconnect conductivity, replacing aluminum alloys. A variety of low-dielectric constant materials are being introduced to reduce parasitic capacitance, replacing silicon dioxide. As dimensions continue to shrink, the traditional silicon dioxide gate dielectric thickness has been reduced to the point where tunneling current has become significant and is compromising the performance of the transistors. This is requiring the introduction of higher dielectric constant materials. Initially the addition of nitrogen to the gate material is sufficient, but in the near future more exotic materials such as transition metal oxides, silicates, and aluminates will be required. As dimensions are reduced, gate depletion effects and dopant diffusion through the gate dielectric are limiting transistor performance. With the replacement of the traditional silicon dioxide/ polysilicon gate stack processes with materials capable of supporting ever shrinking geometries, the task of the industry becomes more difficult. The overall task represented by the projects below reflects the need for analytical techniques with unparalleled spatial resolution, accuracy, robustness and ease of use.

Shrinking dimensions of transistors while simultaneously increasing the wafer diameter from 200 mm to 300 mm is placing more stringent requirements on wafer flatness, thickness and warp, ion and particle contamination.

Accurate metrology of process gases is essential for reproducible manufacture of semiconductor products. Critical physical parameters need to be measured on a wide variety of reactive and non-reactive process gases, allowing the accurate calibration of flow meters and residual gas analyzers. Water contamination at extremely low levels in process gases presents serious manufacturing difficulties. Accurate calibration of water vapor at extremely low vapor pressures is required.

Accurate metrology of process gases is essential for reproducible manufacture of semiconductor products and a wide variety of metrology issues emerge in plasma, chemical vapor, and rapid thermal processing steps used in semiconductor manufacture.

Detection and accurate sizing of particle contamination continues to challenge semiconductor manufacturing.

Wafer and Chuck Flatness Metrology

Technical Contacts:

Angela Davies, Chris Evans, Tony Schmitz,

Objective:

Provide measurement and infrastructural technology to support the generation and measurement of flat wafer surfaces, either free-form or as chucked. Specific goals are: to provide interferometric measurements of as-chucked 300 mm wafer flatness; to develop and demonstrate infra-red interferometric measurements of wafer thickness, thickness variation, and bow; and to develop new models of appropriate polishing processes including those using the NIST-patented Rapidly Renewable Lap.

Customer Needs:

Limited lithographic depth of focus budgets for finer features, combined with larger silicon wafers, pose new challenges for flatness and flatness metrology. Conventional vacuum chucks introduce additional distortions to the thickness variations in the wafer itself. These combined effects may reduce the process latitude.

Capacitance based tools are widely used today for wafer geometry measurements, but have some limitations. Optical techniques are being developed in a number of organizations, but initial intercomparisons show significant measurement divergence. At a recent NIST hosted workshop, instrument developers and wafer manufacturers both expressed the need for calibration artifacts – calibrated optical flats as references for the instrument makers and reference wafers with mapped thickness variations for the instrument users. The optical metrology tools developed in this project will provide traceable measurements for 300 mm wafers at uncertainties compatible with all lithographies envisioned in the NTRS; once that measurement capability is in place, the mechanism for providing industry with artifacts will be selected. Simultaneously, new polishing process understanding will support critical planarization process development.

Technical Strategy:

Our primary goal in this project is to develop full aperture interferometric methods to evaluate important wafer characteristics such as flatness, thickness, thickness variation and bow. In parallel we will continue to evaluate performance of novel polishing methods.

The main tool applied to the measurement of flatness will be a new 300 mm aperture, multi-purpose interferometer capable of measurement for flats, spherical and aspheric optics. The NIST **X**-ray Optics **CALIB**ration **I**nterferomete**R** has a target uncertainty for the measurement of flats of 0.25 nm. The instrument was installed at NIST in 3Q99 in a specially designed environment. Once fully operational, XCALIBIR will be available for measurement of as-chucked wafer flatness, over both full- and sub-apertures.

As-chucked wafer flatness depends both on the chuck and on thickness variations in the wafer. A second major tool to be applied in this project is the Flatmaster, a prototype infra-red interferometer built for NIST by Tropel Inc, based on a NIST patent. The instrument can now be configured to operate as a phase shifting Twyman-Green interferometer or to wavelength shift Haidinger fringes. Wafers may be measured either in a diverging wavefront or with a plane wave.

NIST developed, and received a patent for a novel lapping system compatible with both diamond lapping of semiconductor substrate materials and with chemo-mechanical polishing. The system is also a convenient platform for development of measurements and models to attempt to clarify the contributions of the various mechanisms in CMP. Through-sample microscopy provides insight into the grit motions in conventional mechanical polishing, and through sample thermal imaging provides information on polishing temperatures.

Accomplishments:

- Developed the Rapidly Renewable Lap concept. Demonstrated for diamond lapping of semiconductor substrates, lapping of photomask blank materials, and CMP for silicon, tungsten and sheet oxide. Patented, and lisenced to Rodel Inc, who is further developing technology at the Center for Nanomachined Surface, a University

–based research institution at the University of Delaware.

- Developed basic chemical kinetic model of CMP
- Demonstrated and obtained patent for IR interferometric measurement of wafer thickness, thickness variation, and bow using a spherical diverging wavefront in a Twyman-Green configuration. Instrument based on patent built by Tropel Inc and installed at NIST. Extended instrument capability to wavelength shifting.
- Demonstrated interferometric measurement of chuck-induced wafer distortions on 150 mm wafers. Demonstrated novel glass and foamed ceramic chucks.

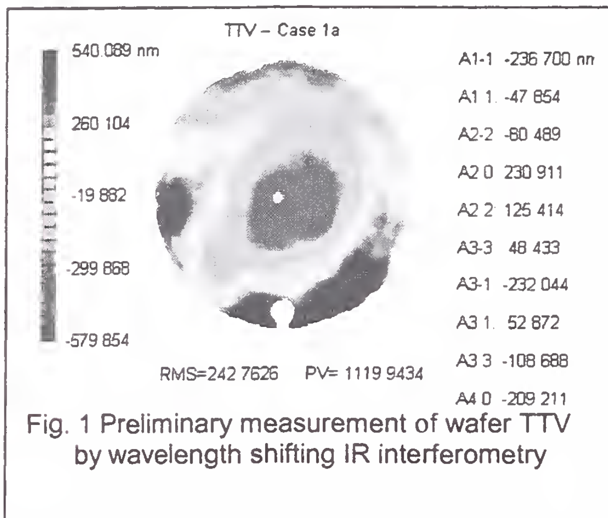

Fig. 1 Preliminary measurement of wafer TTV by wavelength shifting IR interferometry

- Developed new implementation of Ritchey-Common test allowing interferometric measurement of 300 mm diameter flats (wafers) in a diverging wavefront from a smaller aperture interferometer.
- Developed concept for XCALIBIR. Installed at NIST in 3Q99. Preliminary measurements made.

Future Plans:

We will complete measurements of the thickness variation of a 300 mm double side polished wafer by 3Q 2001 and report to industry workshop. Measurement of 300 mm optical flats using self-calibration techniques will be demonstrated on XCALIBIR in 2001. We will complete preliminary temperature measurements through a wafer and publish a chemical kinetics-based model of tungsten CMP.

Collaborations:

Corning-Tropel
Komatsu

Publications:

Evans C. J., Parks R. E., Shao L-Z., Schmitz T., and Davies A."Interferometric Testing of Photomask Blank Flatness" Proc SPIE 4344, in press.

Parks R. E., Shao L-Z., Davies A and Evans C. J.,"Haidinger interferometer for silicon wafer TTV measurement" Proc SPIE 4344, in press.

Paul E. "Theory of Chemical Mechanical Polishing" MRS Proceedings, Symposium of Chemical Mechanical Polishing (CMP), at the Spring 2000 meeting of the Materials Research Society, San Francisco.

Modeling, Measurements, and Standards for Wafer Surface Inspection

Technical Contacts:

T. A. Germer and G. W. Mulholland

By 2005, at the 100 nm node, particle having diameters 30 nm, 39 nm, and 100 nm or larger must be detectable on bare silicon and nonmetallic films, metallic films, and the backsides of wafers, respectively. No known solutions exist at this time. [1999 ITRS, p. 275]

Objective:

Provide industry with models, measurements, and standards for particles and other defects in order to improve the inspection of wafer surfaces. Develop facilities to accurately measure particle size and to deposit monosize particles on calibration artifacts to reduce the uncertainty in the sizes of particles used by the semiconductor industry to calibrate scanning surface inspection systems (SSIS). Investigate theoretically and experimentally the behavior of light scattering from particles, defects, and roughness on wafer surfaces.

Customer Needs:

The Semiconductor Industry Association's (SIA) International Technology Roadmap for Semiconductors identifies the detection and characterization of defects and particles on wafers to be a potentially show-stopping barrier to device miniaturization. The roadmap specifies that by 2005, 30 nm particles must be detectable on bare silicon and nonmetallic films, 39 nm particles on metallic films, and 100 nm particles on wafer backsides, for which no solutions currently exist. While the detection sensitivity for defects must be increased, the ability to characterize defects in terms of size, shape, composition, etc., is critical for yield-learning. Defects must be characterized independent of defect location and topology.

With the need to detect smaller defects, the costs of inspecting wafers are skyrocketing. In order for new advances to be implemented in production environments, improvements in sensitivity must be achieved without suffering a tradeoff in throughput and must be cost-effective. The drive towards in-situ sensors for production tools requires techniques which can be effectively miniaturized.

In order that wafer manufacturers and the device manufacturers have a common basis for comparing specifications of particle contamination, improved standards for particles are needed. A recent comparison of the measurements of calibration wafers by thirteen different SSISs indicated unacceptably large deviation between the SSIS results and the actual particle sizes. This study involved six particle sizes ranging from 88 nm to 290 nm and included the NIST SRM 1963 and two other sizes measured by NIST. For the two smallest particle sizes, 88 nm and 100.7 nm, the scanners systematically underestimated the size by about 8 %. By 2005, it is anticipated that accurate calibration particles as small as 30 nm will be needed.

Technical Strategy:

There are two major stratagies to improving the performance of scanning surface inspection systems. One strategy is to develop a fundamental understanding of optical scattering at surfaces so that tool manufacturers can optimize the performance of their instrumentation, in terms of defect detection limits and discrimination capabilities, to characterize the response of instrumentation to different types of defects, and to develop and calibrate particles of well-defined size and material. Recent work by this group has demonstrated that the polarization of light scattered by particulate contaminants, subsurface defects, and microroughness has a unique signature that can be used to identify the source of scatter. In particular, it was found that small amounts of roughness do not depolarize scattered light. This finding has enabled the development of instrumentation which can collect light over most of the scattering hemisphere, while being blind to microroughness. That instrumentation, for which a patent has been awarded, should result in a factor of two improvement in minimum detectable defect size.

A second strategy is to provide leadership in the development of low uncertainty calibration particles for use in calibrating surface scanners. A major focus has been development of the differential mobility analysis (DMA) method for accurately sizing monosize polystyrene spheres. This work together with a SSIS round robin has provided evidence that current SSIS measurements have an unacceptably large uncertainty for particle sizes in the 90 nm to 100 nm size range. The technical focus of our future work will be apply-

ing the DMA for accurately sizing calibration particle sizes as small as 30 nm and developing methods for generating other types of monosize particles.

Specific project elements are defined below:

Polarized Light Scattering Measurements – The Goniometric Optical Scatter Instrument (GOSI) enables accurate measurements of the intensity and polarization of scattered light with a wide dynamic range, high angular accuracy, and multiple incident wavelengths (visible and UV). We measure the light scattering properties of well-characterized samples exhibiting interfacial roughness, deposited particles, subsurface defects, dielectric layers, or patterns. The emphasis is on providing accurate data, which can be used to guide the development of light scattering instruments, and to test theoretical models.

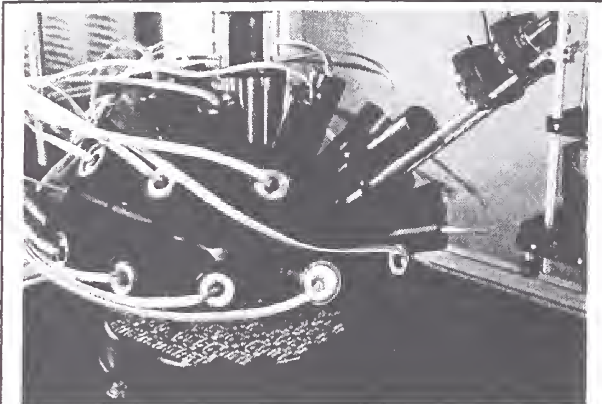

Fig. 1 The Multidetector Hemispherical Polarized Optical Scatter Instrument is a prototype for a wafer surface inspection system and was designed to demonstrate how polarized light scattering can be used to improve the detection and characterization of wafer surface defects.

Theoretical Light Scattering Calculations – The focus of our theoretical work is on (a) developing models that accurately predict the polarization of scattered light, and (b) determining what information can be efficiently and accurately extracted from light scattering measurements. Approximate theories are used in conjunction with more complex finite element time-domain and discrete-dipole approximation techniques to gain an understanding of which parameters affect the light scattering process. Particular cases that are being analyzed include (a) scattering by defects and roughness associated with dielectric layers, (b) scattering by particulate contamination on bare wafers, and (c) scattering by high aspect ratio vias.

Instrument Development – A second instrument, the Multidetector Hemispherical Polarized Optical Scatter Instrument (MHPOSI) complements the capabilities of GOSI as a prototype for a production-line light scattering inspection tool. An instrument with twenty-eight fixed detection elements covering the scattering hemisphere, MHPOSI enables a determination of the differential scattering cross section, for individual particles or defects on a wafer surface. This instrument can be configured so that it is blind to interfacial roughness. Together with an understanding of the light scattering functions for different imperfections, MHPOSI has a substantially improved capability for rapidly detecting and identifying defects, particles, and microroughness on wafers.

Size Distribution Measurements - Differential mobility analysis (DMA) has been shown to be capable of making accurate size measurements for the mean particle size for 100 nm monosize polystyrene spheres. There are promising results for the measurement of the size distribution for broader size distributions; however, the results are not quantitative. Work is in progress to quantify the uncertainty in the size distribution measurement and to extend the method to smaller particle sizes.

Aerosol Generation – An aerosol must be formed typically from a liquid spray of a particle suspension before the particles can be sized by the DMA or deposited on a wafer. Work is in progress to use a variety of innovative methods for generating, shaping the size distribution of the aerosol, and depositing the particles. These include the electospray for generating particle sizes smaller than 60 nm, impactor to remove the large size fraction of the aerosol and to deposit the particles, and an electrostatic chamber for depositing small particle sizes. Work is also in progress to generate copper particles from chemical precursors in a tube furnace.

Resource on Particle Science – Over the past five years, the particle related work has included projects with SEMATECH and particle suppliers to the semiconductor industry. A number of needs by particle related companies were expressed at the

NIST particle workshop including redoing the uncertainty assessments of existing particle SRMs and offering a particle sizing calibration service. Providing support for particle needs critical to the semiconductor industry will continue to be a priority.

Accomplishments:

- A NIST-sponsored workshop entitled "Issues Related to SSIS Calibration with Polystyrene Spheres" brought together suppliers of wafers, reference particles, particle sizing and deposition equipment, and wafer inspection instruments set the stage for developing a more responsive particle program.

- Determined that the electrospray technique can produce an aerosol having characteristics optimal for transferring particles in a liquid suspension onto wafers for particle diameters as small as 25 nm. This significant finding enables improved wafer depositions by reducing the number of contaminant residue particles, the number of doublets, and the amount of residue on the particles.

- In collaboration with the University of Maryland, developed a method for generating pure copper spheres with diameters ranging from 100 nm to 200 nm. These spheres, which mimic real-world particles better than polystyrene, will be used to validate the particle scattering theory in conditions for which models have a higher degree of uncertainty. Also, developed a method for depositing colloidal gold spheres onto silicon wafers, using a liquid phase process. Measured polarization of light scattered from 100 nm, 150 nm, and 200 nm gold spheres on silicon wafers, and found good agreement between the Bobbert-Vlieger theory for light scattering from a sphere above a surface.

- Developed a method, based upon scattering ellipsometry, for quantifying scatter from two sources and demonstrated its use by characterizing the roughness of both interfaces of an SiO_2/silicon system. This finding establishes the validity of the light scattering models for roughness in a dielectric film, which in turn limits the detection sensitivity of SSIS instruments. The method was also used to characterize scattering from steel surfaces, demonstrating capability to distinguish between scattering from surface roughness and material inhomogeneity. The method was further used to study the scatter from an anticonformal polymer film, helping to establish the limits of validity of the scattering theory.

- Developed the SCATMECH library of C++ routines for light scattering. Published the SCATMECH library, providing a means for distributing scattering models and polarized light calculations to others. From the time of its public availability in March 2000 to the end of December 2000, 186 copies of the library have been downloaded from the web. Future versions of the library will include theories for scattering from dielectric films and an exact theory for the scattering from a sphere above a surface.

Future Plans:

Milestone: By FY 2000, make models available publicly with a Polarized Light Scatttering C++ Object Library. Provide annual updates as models are developed.

Milestone: By FY 2001, develop plan for working with particle suppliers/depositers to reduce the uncertainty in the diameter of the calibration particles.

Milestone: By FY 2001, measure light scattered by spheres of different materials and sizes on silicon wafers. By FY 2002, extend the measurements to non-spherical particles.

Milestone: By FY 2001, in collaboration with the University of Maryland, deposit monosize copper particles on silicon wafers, characterize the particle chemistry, and the size distribution.

Milestone: By FY 2001, develop methodology for characterizing thin film topography using polarized light scattering and perform measurements demonstrating its effectiveness in a variety of systems.

Milestone: By FY 2001, develop analysis method and software for making automated size distribution measurements of polystyrene spheres.

Milestone: By FY 2002, demonstrate defect classification learning in a multidetector light

scattering instrument using pattern recognition techniques.

Collaborations:

We are collaborating with Professor Sheryl Ehrman of the University of Maryland on the synthesis and characterization of monosize copper and other metallic particles.

External Recognition:

GWM invited to give presentation entitled "Particle Size Standard Reference Materials from the National Institute of Standards and Technology' at University of Minnesota Shortcourse on Wafer Inspection, Cleaning, and Particle Analysis: Fundamentals and Recent Advances, June, 2001.

TAG invited to give presentation entitled "Polarized Elastic Light Scattering: A probe of interfacial roughness, defects, and particulate contamination," at a Joint Colloquium, Physics and Chemistry Departments, Georgetown University, Washington, DC, February 9, 2000.

TAG invited to give presentation entitled "Light Scattering Ellipsometry: A Quantitative Tool for Characterizing Defects and Roughness Near Interfaces," at the City College of New York, New York, NY, May 24, 2000.

Publications:

G.W. Mulholland, D. Chen, and D.Y.H. Pui, "Comparison of the Size Distribution of Polystyrene Spheres Produced by Pneumatic and Electrospray Nebulization," 2000 International Conference Characterization and Metrology for ULSI Technology, NIST, June.

G. W. Mulholland and B. Bauer, "Nanometer Calibration Particles: What is Available and What is Needed?," *J. Nanoparticle Research,* **2**: 5-15 (2000).

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Thomas A. Germer, "SCATMECH: Polarized Light Scattering C++ Class Library," online software and document published at http://physics.nist.gov/scatmech (March 2000).

Richard G. Priest and Thomas A. Germer, "Polarimetric BRDF in the Microfacet Model: Theory and Measurements," in *Military Sensing Symposia Specialty Group Meeting on Passive Sensors*, held March 21-23, 2000 in Charleston, SC.

Thomas A. Germer, "Measurement of Roughness of Two Interfaces of a Dielectric Film by Scattering Ellipsometry," *Phys. Rev. Lett.* **85** (2), 349–352 (2000).

Egon Marx, Thomas A. Germer, Theodore Vorburger, and Byong C. Park, "Angular Distribution of Light Scattered From a Sinusoidal Grating," *Appl. Opt.* **39**(25) 4473–4485 (2000).

Thomas A. Germer, "Characterizing Interfacial Roughness by Light Scattering Ellipsometry," in *Characterization and Metrology for ULSI Technology: 2000 International Conference*, D. G. Seiler, A. C. Diebold, T. J. Shaffner, R. McDonald, W. M. Bullis, P. J. Smith, and E. M. Secula, eds., *Proc. AIP* **550**, 186–190 (AIP, New York, 2001).

Thomas A. Germer, Thomas Rinder, and Hendrik Rothe, "Polarized light scattering measurements of polished and etched steel surfaces," in Scattering and Surface Roughness III, Z.-H. Gu, and A. A. Maradudin, Eds., *Proc. SPIE* **4100**, 148–155 (2000).

Thomas A. Germer, "Polarized light scattering by microroughness and small defects in dielectric layers," *J. Opt. Soc. Am. A*, in press (May 2001).

Thomas A. Germer and Clara C. Asmail, "Microroughness-blind optical scattering instrument," United States Patent 6,034,776, granted March 7, 2000.

High-Resolution Microcalorimeter X-Ray Spectrometer for Chemical Analysis

Technical Contacts:

David Wollman, 303-497-7457; Sae Woo Nam, 303-497-3148, Gene Hilton, 303-497-5679; Kent Irwin, 303-497-5911; John Martinis, 303-497-3597

Promising new technology such as high energy resolution X-ray detectors must be rapidly commercialized. ***1999 International Technology Roadmap for Semiconductors***

Objective:

To develop the ability to detect photons with high-energy resolution and near-unity quantum efficiency that will enable new generations of spectroscopic tools to be created. To use improved energy-dispersive X-ray spectroscopy to solve a wide range of problems in materials analysis. In the semiconductor manufacturing industry, improved X-ray materials analysis is needed to identify small contaminant particles on wafers.

Customer Needs:

The goal of the Microcalorimeter detector project is to use the unique low-noise, high-sensitivity properties of cryogenic electronics to create new generations of detectors for high energy-resolution measurements of the X-ray radiation produced in a Scanning Electron Microscope (SEM). Materials analysis and improvement in the level of that analysis is an integral part of the Metrology Roadmap in the 1999 ITRS. Advances in this area, through the use of MEMS technology, can enable particle analysis in SEMs located in the clean room.

Technical Strategy:

Introducing a radically new technology such as cryogenic microcalorimeters to a large community requires creating and demonstrating an entire measurement instrument, not just the detector. We have developed superconducting electronics to read the detectors, compact adiabatic demagnetization refrigerators to simplify cooling the detectors to milliKelvin operating temperatures, and room-temperature electronics to process the output signals. Our goal is to develop new detector systems and to apply those systems to problems of interest to our customers.

In the area of X-ray spectroscopy, the performance target depends on the application. For many semiconductor materials analysis problems, further improvements in energy resolution (beyond that already demonstrated with these detectors) are not as important as an increase in the maximum count rate and collection area. This can be achieved by the creation of multipixel arrays of detectors. In addition to the fabrication difficulties in making such arrays, the cold- and room temperature electronics to read out the arrays must also be created. The current approach to the electronics is to develop a superconducting quantum interference device (SQUID) multiplexer (MUX) circuit to read the array, and room-temperature digital signal processing (DSP) to process the MUX signals.

We will develop a small array of microcalorimeter detectors for X-ray analysis and read them out using SQUID MUX and DSP circuitry. The application of X-ray detectors to materials-analysis problems represents a test bed for this technology. With a focus towards the semiconductor manufacturing industry, problems in characterization of small particles and very thin layers of material are very important. The ability of the detector to differentiate overlapping X-ray lines at low energies enables analysis of previously inaccessible systems.

In collaboration with the Chemical Science and Technology Laboratory, we will install the microcalorimeter spectrometer on state-of-the-art microanalysis tools at NIST-Gaithersburg to further demonstrate the capabilities of the system for analysis of particles and thin films.

For some materials-analysis applications improvements in the energy resolution at relatively high X-ray energies (6000 eV) are still needed. In addition, large-format, densely packed arrays of detectors are required for imaging. Novel fabrication techniques will need to be developed to make densely packed arrays, and SQUID MUX and DSP circuitry will be required to read out the arrays.

We will develop models of single-pixel microcalorimeter performance to assist in improving detector sensitivity, and will fabricate and test novel detector designs based on these models. We will also develop small, densely packed arrays of detectors and instrument them with appropriate read out electronics.

Accomplishments:

The schematic in Fig. 1 shows a microcalorimeter energy-dispersive spectrometer (EDS) X-ray detector system inserted into a scanning electron microscope to allow chemical microanalysis of materials.

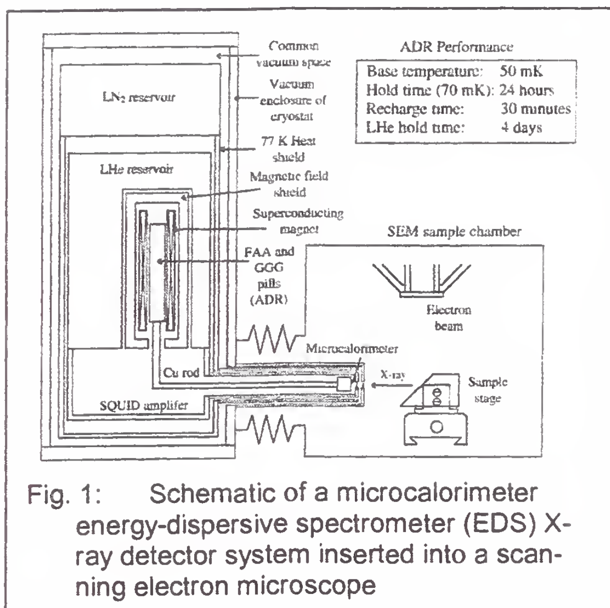


Fig. 1: Schematic of a microcalorimeter energy-dispersive spectrometer (EDS) X-ray detector system inserted into a scanning electron microscope

The microcalorimeter detector uses a superconducting/normal-metal bilayer to create a superconducting transition-edge sensor (TES). Using the proximity effect, the transition temperature of the bilayer can be selected to match each specific application. We created an accurate model of the proximity effect in this system, which allows the thickness for each layer to be calculated, minimizing trial-and-error fabrication.

Recent advances with Mo/Cu bilayers have allowed whole-wafer photolithographic processing with improved yield. The TES and appropriate X-ray absorber are fabricated on a Si_3N_4 micromachined membrane to produce the required thermal isolation. The device operates using a current bias and extreme negative electrothermal feedback, so that it self-regulates in temperature. Absorbed X rays produce heat pulses in the device, which are read out as pulses of reduced bias current by a first-stage, single-SQUID amplifier located adjacent to the detector to minimize inductance. The output of the first-stage SQUID is output via a unique 100-SQUID amplifier invented and fabricated by the Project specifically to allow direct coupling of the signal to room-temperature electronics. The detector is cooled to below 100 mK by a compact adiabatic demagnetization refrigerator, which has unique design features that produce nearly 24 hrs of continuous operation, and days of hold time for liquid helium.

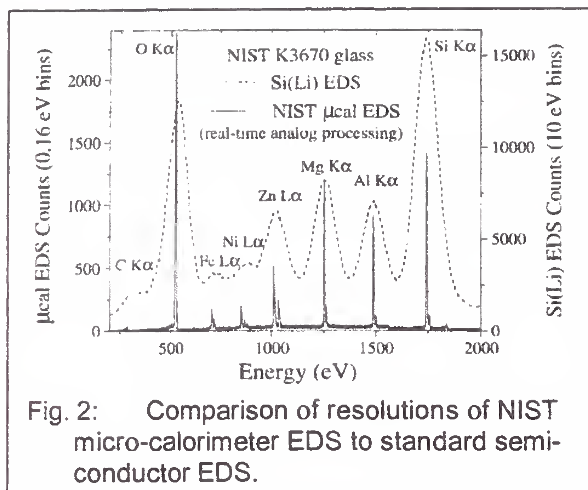
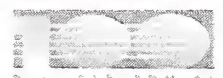


Fig. 2: Comparison of resolutions of NIST micro-calorimeter EDS to standard semi-conductor EDS.

This system holds the world record for energy resolution for an EDS detector of 2.0 eV at 1500 eV, which is over 30 times better than the best high resolution semiconductor-based detectors currently available as can be seen in Fig. 2. This figure above compares an X-ray spectrum obtained with this system to that from a semiconductor EDS, clearly demonstrating the remarkable improvement in resolution. The specimen was a glass prepared by Dale Newbury of NIST to use as a test standard for EDS. We have used the system to identify sub-micrometer particles of materials such as W on Si substrates, an identification problem that is impossible with standard EDS detectors and of great importance to the semiconductor industry. It has also demonstrated energy shifts in the EDS X-ray spectra of materials such as Al, Fe, and Ti, depending on their chemical bonding state, thus allowing differentiation between a particle of Al and Al_2O_3, for example.

In collaboration with researchers at Lucent Technologies in Orlando, Florida, we compared the trace Cu detection ability of microcalorimeter-based X-ray analysis with that of other industrial analytical techniques, including conventional semiconductor EDS, Auger Electron Spectrometry (see Fig. 3), and Secondary Ion Mass Spectrometry (SIMS). Although only SIMS is capable of trace Cu analysis down to the ≈ 0.02 % atomic level, microcalorimeter EDS fared very well in comparison with the other non-destructive analytical techniques.



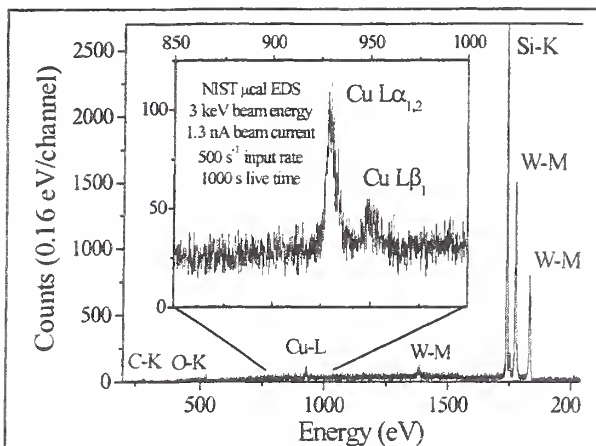


Fig. 3. A microcalorimeter EDS spectrum of 0.7 % by weight Cu/Al alloy thin film (from Lucent Technologies) demonstrating the sensitivity of microcalorimeter EDS for trace Cu analysis in the semiconductor industry.

Based on these types of results, two U.S. X-ray spectrometer companies have acquired licenses for a suite of patents covering this technology to begin commercialization. Technology transfer to both companies has occurred, and both are planning to have an initial system available soon.

More advanced applications of this technology to materials-analysis problems requires coupling the spectrometer to state-of-the-art analytical tools. The single-pixel spectrometer used in the above research has been relocated to Gaithersburg. Installation and qualification is nearly complete, and the system will be used to continue microanalytical work on problems of interest to the semiconductor and other materials-intensive industries.

Patents:

"Particle Calorimeter with Normal Metal Base Layer," issued June, 1997.

"Mechanical Support for a Two Pill Adiabatic Demagnetization Refrigerator," issued August 1999.

"Superconducting Transition-Edge Sensor," issued March 1999.
Microcalorimeter X-ray Detectors with X-ray Lens," issued March 1999.

"Superconducting Transition-Edge Sensor with Weak Links," filed November 1998.

"The Use of Superconductor-Insulator-Normal (SIN) Tunnel Junctions in Superconducting Quantum Interference Device (SQUID) Multiplexers," disclosure submitted, April 2000.

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Thermophysical Properties of Gases Used in Semiconductor Processing

Technical Contacts:
***J.J. Hurly**, K.A. Gillis, and M.R. Moldover*

"The industrial interest in this workshop showed that the industrial need for gas property values and flow standards is immediate and at least moderate. The rapid introduction of new processes by the semiconductor industry may make the need more urgent." Final Report on recommendations from the "Workshop on Mass Flow Measurement and Control for the Semiconductor Industry Workshop," 15-16 May 2000, NIST, Gaithersburg, MD.

Objective:

To provide industry with high-accuracy data for modeling CVD (chemical vapor deposition) processes and for calibration of MFCs (mass flow controllers) used in semiconductor processing.

Customer Needs:

Many process gases are toxic, and/or corrosive, and/or pyrophoric. The thermophysical property data for such gases are sparse and rarely accurate. Accurate thermophysical property data are required to model the gas streams that are used in CVD processes. (For example, models are needed for the velocity, temperature, and concentration profiles in the vicinity of a hot susceptor.) Accurate thermophysical property data are also needed to calibrate the MFCs used to meter process gases. These MFCs are calibrationed with benign "surrogate" gases (*e.g.*, N_2, CF_4, SF_6, or C_2F_6) but are used to deliver process gases (*e.g.* Cl_2, HBr, BCl_3, WF_6) for CVD, plasma etching, and other processes. Accurate calibrations are required to process scaling from prototype to pilot plant and to production. Since MFC operation depends upon heat transfer, converting a surrogate gas calibration to a process gas use requires the heat capacity, thermal conductivity, density, and viscosity of both gases as functions of the temperature and the pressure.

Technical Strategy:

The Fluid Science Group is using acoustic techniques to measure the thermophysical properties of three classes of gases: (1) binary mixtures of CVD carrier gases with process gases, (2) pure process gases, and (3) surrogate gases. The Group is developing a comprehensive, reliable database for these gases that provides the heat capacity, thermal conductivity, viscosity, and the pressure-density-temperature relation. The database will include diffusion coefficients for mixtures of the gases. Values for diffusion coefficients will be obtained from models for the intermolecular potentials between carrier gases and process gases.

Accomplishments:

We developed a facility for safely measuring the properties of these hard-to-handle gases. During FY00, we measured the speed of sound in $(CH_3)_3Ga$ (a pyrophoric organo-metallic) and NF_3 (an aggressive oxidizer), two gases given high priority by the SEMATECH MFC Working Group. Figure 1 displays speed-of-sound data for $(CH_3)_3Ga$. Typically, the data range from below the boiling temperature to 200 °C and from 25 kPa to 1500 kPa or 80 % of the vapor pressure. The acoustic data are analyzed to determine the ideal-gas heat capacity and the equation of state with uncertainties of approximately ±0.1 %. Model pair potentials are also derived from the data. These models are used to reliably extrapolate the equations of state to temperatures above 1000 K and to estimate the transport properties.

The NIST results are being disseminated through the internet in a user-friendly database at *http://properties.nist.gov/semiprop/* and also in

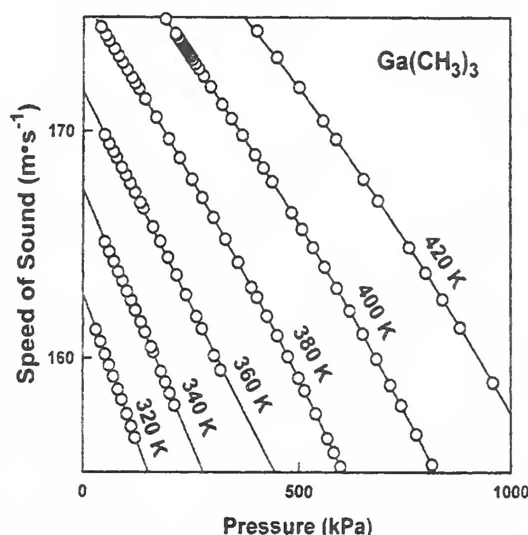

Fig. 1 Speed-of-sound measurements in tri-methylgallium.

NIST
National Institute of Standards and Technology
Technology Administration, U.S. Department of Commerce

review publications and peer-reviewed articles in archival journals.

Future Plans:

We plan to measure the speed of sound in other poorly characterized process gases. Acoustic measurements of the transport properties have begun, starting with the viscosity of the calibration gases CF_4, C_2F_6, and SF_6. These will be extended to process gases and the Prandtl number will be measured. As data are acquired, the on-line data base will be updated.

Collaborations:

Semiconductor Equipment and Materials International, Gas Standards Committee

External Recognition:

Hurly, J.J., "Progress Report: Thermophysical Properties of Semiconductor Process Gases," Semicon West 2000, San Francisco, CA, July 9, 2000. Invited

Hurly, J.J., ***"Thermophysical Properties of Semiconductor Process Gases,"*** 5th Intl. Symposium on Ultra Clean Processing of Silicon Surfaces, Ostende, Belgium, September 21, 2000. Invited

Moldover, M.R., "Standards of Temperature, Pressure, and Transport Properties from Ab Initio Calculations for Helium," University of Delaware, Physics Dept., Newark, DE, December 8, 2000. Invited

Publications:

J.J. Hurly, "Thermophysical Properties of Gaseous Tungsten Hexafluoride from Speed of-Sound Measurements," Int. J. Thermophysics, 21, pp. 185-206 (2000).

J.J. Hurly, D.R. Defibaugh and M.R. Moldover, "The Thermodynamic Properties of Sulfur Hexafluoride," Int. J. Thermophysics, 21, pp. 739-765 (2000).

J. Wilhelm, K.A. Gillis, J.B. Mehl, and M.R. Moldover, "An Improved Greenspan Viscometer," Int. J. Thermophysics, 21, pp. 983-997 (2000).

M.R. Moldover, K.A. Gillis, J.J. Hurly, J.B. Mehl, and J. Wilhelm, "Acoustic Measurements in Gases: Applications to Thermodynamic Properties, Transport Properties, and the Temperature Scale," Vol. IV, Chap. 12 in Handbook of Elastic Properties of Solids, Fluids, and Gases, edited by R. Raspet and M. Levy, Academic Press (in press).

Models and Data for Chemical Vapor Deposition

Technical Contacts:

***R. W. Davis**, D. R. Burgess, Jr. (838), J. E. Maslar, E. F. Moore, R. L. Axelbaum (Washington University), and S. H. Ehrman (University of Maryland)*

Customer Needs:

Reactor and process design are often limited to empirical trial and error approaches that tend to converge slowly, if at all, to semi-optimized states. This implies that important industrial processes are not adequately investigated prior to final implementation. This situation manifests itself in more expensive, lower quality products produced by processes that may be less environmentally acceptable.

Objective:

To provide the necessary information and scientific infrastructure to enable the application of semiconductor process models and controllers that are well-grounded in fundamental physical laws.

Technical Strategy:

Process simulation has the potential to significantly enhance the design phase of process development so as to improve both efficiency and quality. This is because computational power has evolved to the point where highly sophisticated models can be constructed for a variety of complex semiconductor processes. However, the increasing complexity of these models implies a greater need for accurate fundamental thermochemical and kinetic data, which are not presently available. Our approach is both to develop and use methods for reliably generating the data necessary for process modeling. The reliability, quality and utility of the generated data must also be demonstrated to the user community. Consequently, the development of process models of wide applicability is essential, as is model validation carried out in reference reactors prototypical of industrial processing equipment. This typically requires the development of reacting flow computer simulations that employ the aforementioned data for input.

Accomplishments:

Our effort in the area of microcontamination in CVD reactors continued with the most significant numerical/experimental comparisons of particle layer characteristics during silane decomposition to date. The reactor conditions employed were a pressure of 200 torr, a susceptor temperature of 1050 K, and susceptor rotation rates of 500, 750, and 1000 rpm with 0.25 mole percent silane in helium. Particle scattering intensities were measured experimentally via laser light scattering. These intensity profiles were compared with those generated numerically by the semi-empirical NIST microcontamination model. This model contains two empirical parameters relating to thermophoretic force and condensational sticking coefficient. With these parameters properly chosen, the numerical/experimental comparisons were observed to be excellent, as shown in the figure for a rotation rate of 750 rpm. Both intensity profiles are seen to depict very similar narrow particle layers at a height above the susceptor of 4.86 mm. This height was found to decrease with increasing susceptor rotation rate, which is consistent with the thinning of the thermal boundary layer as rotation-induced suction increases. During FY2001, efforts will continue to characterize the particle layer as

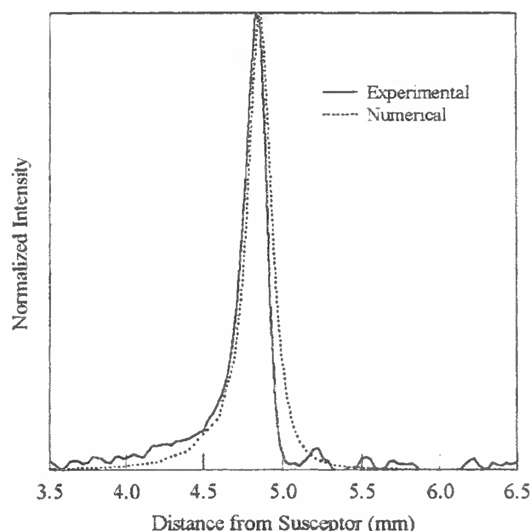

Fig. 1 Numerical and experimental scattering intensity profiles as a function of height above the susceptor surface for a disk rotation rate of 750 rpm both show a thin particle layer.

well as to determine the gas-phase species concentrations in the region of the layer.

Finally,a new website *(http://www.cstl.nist.gov/div836/836.02/cvd/toppage.html)* has been established in order to serve as a comprehensive source of public information on this research effort.

Our work in database compilation for chemical species of importance in semiconductor processing continued. Good results were obtained for bond dissociation energies during the decomposition of fluorinated ethanes.

Future Plans:

An experimental effort to measure decomposition rates for organometallic CVD precursors was initiated and will continue during FY2001.

Collaborations:

University of Maryland
Washington University

Publications:

Davis, R. W. and Moore, E. F., ***"Two Model Problems for Testing Aerosol Dynamics Algorithms for Stagnation-Flow Reactors,"*** Aerosol Science and Technology, 31, pp. 456-462 (1999).

Davis, R. W., Moore, E. F., Maslar, J. E., Burgess, D. R., Kremer, D. M. and Ehrman, S. H., ***"A Numerical/Experimental Investigation of Micro-contamination in a Rotating Disk Chemical Vapor Deposition Reactor,"*** Proceedings of the 2000 International Conference on Characterization and Metrology for ULSI Technology, Gaithersburg, MD, American Institute of Physics (in press).

Maslar, J.E., Aquino-Class, M.I., Bowers, W.J., Hendricks, J.H., Hurst, W.S., ***"In Situ Raman Spectroscopic Investigation of Aqueous Iron Corrosion at Elevated Temperatures and Pressures,"*** J. Electrochemical Soc. 147 (7), p. 2532-2542 (2000).

Maslar, J.E., Wang, C.A., and Oakley, D.C., ***"In Situ Raman Spectroscopic Characterization of Compound Semiconductor Free Carrier Concentration,"*** 2000 Digest of the LEOS Summer Topical Meetings, p. 31 (2000).

Maslar, J.E., Hurst, W.E., Vanderah, T.A., and Levin, I., ***"The Raman Spectra of Cr_3O_8 and Cr_2O_5,"*** J. of Raman Spectroscopy (in press).

Temperature Measurements and Standards for Rapid Thermal Processing

Technical Contacts:
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Objective:

To improve the accuracy of surface temperature measurements, with emphasis in the area of rapid thermal processing (RTP) of semiconductors.

Customer Needs:

The semiconductor manufacturing industry requires improved accuracy in measuring the temperature of silicon wafers during processing because accurate temperature measurements are critical to product quality and device performance. As a result, the industry has an uncertainty requirement of 2 °C at 1000 °C for RTP for the next generation of wafer patterning. ITRS 1999

Technical Strategy:

Light pipe radiation thermometers (LPRTs) are non-contacting and the sensor of choice in RTP. Thermocouple instrumented wafers are used to calibrate LPRTs in-situ. NIST efforts are based on combinations of stable thin-film and Pt/Pd wire thermocouples (TCs). The thin-film TCs (TFTCs) minimize errors from heat transfer present with other types of contact temperature sensors. This technique permits an expanded uncertainty of less that 1 °C when the wafer temperature is uniform to within 10 °C. Additionally, the effect of the environment of an LPRT on the temperature it measures was investigated to determine the proper procedure for calibrating an LPRT.

Accomplishments:

In the past we have reported on TFTCs that were useful up to 900 °C, but problems of SiO_2 electrical conductivity, coalescence of the thin films, and oxidation of the films have precluded their use at 1000 °C. During FY00 we found solutions to those problems consistent with maintaining a standard uncertainty target of 0.4 °C for the surface temperature measurement. We have found that it was necessary to increase the thickness of the thermal SiO_2 to 690 nm from the 310 nm previously used. In order to improve the stability of the Pt against coalescence and pore growth, we have made the traces thicker (>1 µm) and covered them with sputtered SiO_2. We also developed a method to calibrate the thin-film TCs on the wafer *in situ* in the RTP tool using Pt/Pd wire thermocouples; previously we could only calibrate the thin film TCs externally on separate coupons. The new method may be used to validate the previously used calibration technique or as a substitute.

We also have expanded our technology transfer activities. Our cooperative project with SEMATECH, University of Texas, and Sensarray Inc. has included both the design, fabrication,

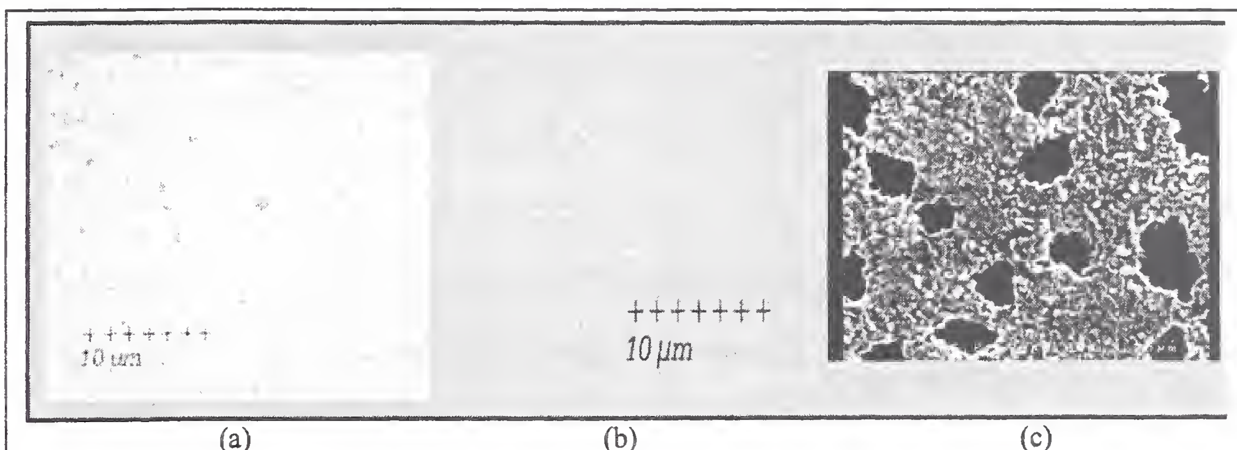


Fig.1. (a) Sputtered Pt (0.7 µm thick) on a Si wafer with thermal oxide after 2 h in N_2 at 1000 °C. The 1 µm to 3 µm medium gray areas are pores reaching the Si wafer.
(b) Same specimen with 0.4 µm of sputtered SiO_2 coating. No observed change from the un-annealed specimen.
(c) SEM of sputtered Pt (0.7 µm thick) on Si wafer with thermal oxide (2 h / 1000 °C). 2 µm to 4 µm dark spots were identified as Si using X-ray analysis.

testing, calibration, and delivery of two thin-film calibration wafers. These will be used for their unique RTP instrumentation test bed, and advisory services on the design of the facility and measurement methods used at the University of Texas. Other industrial and academic technology transfer activities have included providing thin-film calibration wafers to Applied Materials and Vortek Industries for test and evaluation in commercial RTP tools. Results from these collaborations provide valuable feedback on performance characteristics of the NIST calibration wafer.

Finally, we have performed experiments to study the environmental effects on the accuracy of LPRTs. The experiments demonstrated that the temperature of a light pipe and the radiation surroundings significantly affect the temperature displayed by the LPRT. The scaling of the data with temperature implies that the effect is the result of self-emission and of scattering of extraneous radiation by the light pipes. The measurement uncertainty due to environmental influence can be minimized by calibrating the LPRT in an environment similar to that in which it will be used. Some light pipes are less affected by their environment than others, suggesting that better manufacturing techniques for light pipes can also minimize the measurement uncertainty.

Future Plans:

Future activities include a concentrated effort to establish the repeatability, durability, and stability of the calibration wafers especially as it relates to their uncertainty in temperature measurement. We are improving the design to reduce the uncertainty in temperature measurement between 700 °C and 1000 °C. Our cooperative projects with the semiconductor processing industries will be expanded to assure the suitability of the wafer for their *in situ* calibrations. In addition we are exploring the use of thin-film calibration wafers for improving the accuracy of temperature measurement in photoresist curing and have a cooperative research project with MIT and SVG Inc. on these measurements.

Collaborations:

International SEMATECH and the University of Texas at Austin
Watlow-Gordon Inc.
Vortek Industries
Applied Materials

External Recognition:

Patent #6,037,645 Issued March 14, 2000, licensed to Watlow Gordon Inc.

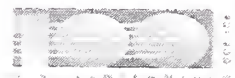
Publications:

Kreider, K.G., Ripple, D.C., and DeWitt, D.P., ***"Calibration of Thin-Film Thermocouples on Silicon Wafers,"*** Proc. of TEMPMEKO '99, p. 286-291, Delft, The Netherlands (1999).

Kreider, K.G., DeWitt, D.P., Meyer, C.W., Scheuerman, V.P., ***"Calibration of Lightpipe Radiation Thermometers in a RTP Tool at 1000 °C,"*** Proc. 8th Intl. Conf. on Adv. Therm. Process. of Semicond.-RTP 2000, IEEE, p. 64-70, (2000).

Meyer, C.W., Strouse, G.F., and Tew, W.F. ***"Non-Uniqueness of the ITS-90 from 13.8033 K to 24.5561 K,"*** Proc. of TEMPMEKO '99, p. 89-94, Delft, The Netherlands (1999).

Meyer, C.W., DeWitt, D.P., Kreider, K.G., Lovas, F.J., and Tsai, B.K., ***"ITS-90 Calibration of Radiation Thermometers for RTP Using Wire/Thin Film Thermocouples on a Wafer,"*** Proc. of 2000 Intl. Conf. on Characterization and Metrology for ULSI Technology, Gaithersburg, MD, (in press).



Standards for Low Concentrations of Water Vapor in Gases

Technical Contacts:

J. T. Hodges, G. E. Scace, P. H. Huang, W.W. Miller

Objective:

To provide absolute standards for water vapor generation and measurement in the mole fraction range 1 to 1000 nmol of H_2O per mol of carrier gas.

Customer Needs:

Strict monitoring and control of trace quantities of water vapor are required in numerous industrial processes related to the fabrication of microelectronics, photonics and semiconductors. Regrettably, metrology-grade standards are not well established in this range, and existing hygrometers are inadequate as they often suffer from hysteresis, irreproducibility and relatively slow response. Further, measurements of low levels of water vapor are complicated by poorly understood interactions between the water vapor, carrier gases and transfer lines, as well as uncertainty in thermodynamic properties of water vapor and carrier gas mixtures.

Technical Strategy:

The strategy of this program is to develop standard sources of humidity and complementary methods of humidity measurement spanning the same range. Both the generation and measurement schemes are optimized for stability, and both are based on processes that can be modeled from first-principles so that the respective uncertainties can be estimated with confidence.

Accomplishments:

A thermodynamically based standard humidity source, known as the Low Frost-Point Generator (LFPG), was developed. Its output is linked primarily to the vapor pressure of ice and therefore is governed by the system temperature and pressure, two quantities that can be precisely controlled and accurately measured. The LFPG delivers water-vapor concentrations as low as 3 nmol/mol, with a long-term stability of better than ±0.2 % in water vapor concentration and a relative uncertainty (coverage factor = 2) of better than 1 %. Comparison of the new generator with another long-established NIST standard generator indicates that in the region of overlap of the two systems, the two agree to within the stated uncertainty of the reference generator. The LFPG is now available to provide special test services for clients desiring direct traceability to National humidity standards. Commercial sensors being characterized include chilled-mirror devices, optical absorption spectrometers, electrolytic and capacitive devices, and vibrating crystal transducers.

Using a stable hygrometer as a nulling device, the LFPG provides a reference to which other precision humidity generators may be compared. This approach enables the measurement of water vapor mole fractions differing by less than 1 nmol/mol. A comparison of several standard generators (based on permeation tube/flow dilution schemes) spanning the water vapor mole fraction range (10 to 100) nmol/mol. was recently completed using the above technique, with measurement uncertainties of less than 1%. This measurement technique will also be utilized for routine calibration of permeation tubes. A single point permeation tube calibration against the LFPG will economically eliminate the need for long term gravimetric studies previously required to establish water permeation rates while improving accuracy. This new calibration service is expected to reduce permeation rate uncertainties by a factor of 5 over current values.

Two techniques based upon absorption spectroscopy are being developed for absolute measurement of water vapor concentration. With the first approach, called wavelength modulation spectroscopy (WMS), we demonstrated relatively fast time response, linearity over two decades of water vapor mole fraction in the range (3 to 3000) nmol/mol, and precision of better than 1 nmol/mol. The other laser absorption technique being developed is cavity-ring-down spectroscopy (CRDS). It is expected to be more accurate than WMS as it provides a fundamental measure of water vapor concentration linked to measurements of time and frequency and referenced to the triple point of water.

Collaborations:

Southwest Sciences
Air Products
Air Liquide

Matheson
Delta F
Meeco
Kin-Tek
Ametek
General Eastern
Innovative Laser
Midac
MBW
Thunder Scientific

Publications:

1. J.T. Hodges, J.P. Looney and R.D. van Zee, "Laser bandwidth effects in quantitative cavity ring-down spectroscopy," Appl. Opt. **35**, 4112-4116, 1996.

2. J.T. Hodges, J.P. Looney and R.D. van Zee, "Response of a ring-down cavity to an arbitrary excitation," J. Chem. Phys., **105**, 10278-10288,1996.

3. G.E. Scace, P.H. Huang, J.T. Hodges, D.A. Olson and J.R. Whetstone, "The new NIST low frost-point Humidity generator,"National Conference of Standards Laboratories, Proceedings of the 1997 Workshop and Symposium, **2**, 657-673, July 27-31, 1997, Atlanta, GA.

4. G.E. Scace, D.C. Hovde, J.T. Hodges, P.H. Huang, J.A. Silver and J.R. Whetstone, Performance of a precision Low frost-point humidity generator," 3rd International Symposium on Humidity and Moisture, National Physical Laboratory, Teddington Engl., April 6-8, 1998.

5. G.E. Scace, D.C. Hovde, J.T. Hodges, P.H. Huang, J.A. Silver and J.R. Whetstone, "The NIST Low Frost- Point Humidity Generator A New Standard for Trace Humidity Measurement," Workshop on Gas Distribution Systems, Semicon West 98, San Francisco,CA, July 12, 1998.

6. R. D. van Zee, J. P. Looney, and J. T. Hodges, "Measuring pressure with cavity ring-down spectroscopy," in *Advanced Sensors and Monitors for Process Industrial Environment*, W. A. de Groot, ed., SPIE Proc. **3535**, 1998.

7. J.P. Looney, J.T. Hodges and R.D. van Zee, "Quantitative absorption measurements using cavity-ringdown spectroscopy with pulsed lasers," Chapter 7, in Cavity-Ringdown Spectroscopy-A New Technique for Trace Absorption Measurements, ed. K.W. Busch, American Chemical Society Symposium Series No. 720, 1999.

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10. A.C.R. Pipino and J.T. Hodges, "Evanescent wave cavity ring-down spectroscopy for trace water detection," Proc. SPIE, **4205**, 1-11, 2001.

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12. P.H. Huang, G.E. Scace and J.T. Hodges, "Measuring technique for quantifying performance of dilution- based trace moisture generators," 8th Intl. Symp. Temp. Therm. Meas. Indust. Sci., Berlin Germany, June 19- 21, 2001.

13. G.E. Scace and J.T. Hodges, "Uncertainty of the NIST low frost-point humidity generator," 8th Intl. Symp. Temp. Therm. Meas. Indust. Sci., Berlin Germany, June 19-21, 2001.

Plasma Process Metrology

Technical Contacts:

M. Sobolewski(836), K. Steffens(836), J. Olthoff (811), Y. Wang (811), L. Christophorou (811), A. Goyette (811), and E. Benck (842).

Objective:

To provide advanced measurement techniques, data, and models needed to characterize plasma etching and deposition processes important to the semiconductor industry, enabling continued progress in model-based reactor design, process development, and process control.

Customer Needs:

To maintain its competitive world position, the U.S. semiconductor industry is continually developing microelectronic devices with smaller feature dimensions. This trend requires ever increasing control of the plasma discharges used in the fabrication processes. Additionally, the development of new reactors and processes relies increasingly on predictive system modeling due to the increasing cost and complexity of the fabrication tools and systems. Consequently, model-based process design and control are important needs identified in the *International Technology Roadmap for Semiconductors*. To obtain more reliable predictions of the spatial uniformity, chemistry, and electrical properties of processing plasmas, further progress in model development and validation is required. Also, to enable improvements in process monitoring and control, a need exists to develop measurement techniques that are compatible with the manufacturing environment.

Technical Strategy:

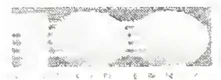
Our experimental program uses a variety of techniques to measure the chemical, physical, and electrical properties of plasmas. The measurement techniques provide an understanding of plasma properties and data for testing and validating models. We use research reactors, known as Gaseous Electronics Conference (GEC) Radio-Frequency Reference Cells, which are compatible with our wide range of diagnostic techniques. GEC cells are attractive platforms for model validation because of the large body of data previously accumulated on such cells. Commercial plasma reactors have also been used for some measurements. Measurement techniques that are well suited for use in process monitoring applications in commercial reactors are first validated by comparisons to laboratory diagnostics in our research reactors. In addition, to further aid in the development of more accurate plasma models, we also determine and assess fundamental data describing collision processes in reactive plasmas.

Accomplishments:

A new technique for *in situ* monitoring of the total ion flux at a wafer surface during plasma processing was developed and validated in Ar plasmas. The method relies on non-perturbing measurements of the radio-frequency current and voltage applied to the plasma reactor. These signals are analyzed using a new model of the discharge which includes the plasma sheaths at both the powered and grounded electrodes. Using this model, one obtains values for the total ion flux and the ion energy distributions at both electrodes. The technique was validated by comparing to independent measurements of sheath voltages at both electrodes and mass spectrometer measurements of ion energy distributions at the grounded electrode.

Absolute, mass-resolved ion fluxes were measured in high density, inductively coupled plasmas generated in a wide range of processing gases, including C_2F_6, C_4F_8, CF_3I, and CF_3CH_2F. The latter two gases possess low global warming potentials that make them potential environmentally-friendly processing gases. The results indicate a large number of ions being produced by each gas as evidence of the complex chemistries present in the plasmas. These results have been used to validate and refine reactor modeling codes used in the development of plasma processes by industry.

We measure the two-dimensional spatial distribution of reactive chemical species in the capacitively coupled GEC Reference Cell using 2-D planar laser-induced fluorescence (PLIF) imaging. In these studies, the concentration of CF_2 in fluorocarbon etching and chamber-cleaning plasmas is monitored as a marker of chemical uniformity. Correlations between PLIF results, optical emission and electrical measurements provide an explanation for observed changes in CF_2 distributions. Recent measurements have characterized the effect of varying electrode gap, rf



power, and the presence of a silicon wafer on CF_2 uniformity and density. The results provide a data set for testing the ability of commercial plasma simulations to predict plasma chemical uniformity.

Horizontal two-dimensional maps of plasma species are being measured with a new type of fiber optic based optical tomography sensor. This new sensor simultaneously acquires optical emission measurements from 82 different directions through two small windows in less than a second. Recent measurements with a quartz confinement ring, which is used to increase the stable operating range of electronegative plasmas in the inductively coupled GEC cell, demonstrate improved plasma confinement and radial symmetry. In addition a new type of inversion algorithm has been developed to more effectively convert the raw data from the optical tomography sensor into a two-dimensional plasma species map.

Initial broadband absorption measurements have been made of several different molecular species (C_2, CN and CF_2) in the capacitive and inductive GEC Reference Cells. These type of measurements will eventually enable a determination of the rotational temperature distributions within the plasma. Such plasma temperature distributions are of interest to plasma modelers and for the interpretation of other optical diagnostics such as laser induced fluorescence.

Electron-interaction data were reviewed for SF_6 and CF_3I, a gas being considered for plasma etching because of its very low global warming potential. The reviews revealed extensive data that were previously unavailable to industry. SF_6 data were subsequently used by industry to improve deep silicon etch processes. Reviews were published in the Journal of Chemical and Physical Reference Data, and the resulting data were posted on the internet (www.eeel.nist.gov/811/refdata). This web site, which also provides recommended electron interaction data from previous reviews of CF_4, CHF_3, CCl_2F_2, C_2F_6, C_3F_8, and Cl_2, experienced over 2000 hits in FY00.

Future Plans:

Tests of ion flux and ion energy sensors based on radio-frequency electrical measurements in etching gases and in commercial reactors are planned. Mass spectrometer measurements of ionic species, fluxes, and energies in reactive plasmas exposed to semiconductor wafers will be pursued and compared with optical measurements of etching byproduct species. PLIF measurements will be extended to additional radicals, such as CF. We are investigating modifications of our research reactors to enable operation in dual-frequency, capacitively coupled mode, which is increasingly used by industry for state-of-the-art dielectric etching processes, particularly for low k dielectrics.

Collaborations:

Collaborations with two plasma equipment manufacturers, Axcelis and Novellus Systems, have been established. The collaborations involve electrical measurements performed on existing and prototype reactors in the manufacturers' R&D facilities.

Electrical measurement and analysis software developed at NIST was provided to Novellus Systems, Inc. Novellus is using the software to analyze the electrical characteristics of their plasma reactors and improve the tool-to-tool reproducibility of one of their plasma processes.

An interlaboratory ATP Intramural project is developing sub-mm wave absorption spectroscopy as a plasma species diagnostic. Accurate measurements of the densities of a wide variety of plasma species made with a single diagnostic tool is of interest to the semiconductor industry and plasma etching tool manufacturers such as LAM Research.

Modeling of electron transport in SF_6 using the NIST standard reference data for electron interactions is being performed in collaboration with researchers from Keio University, Japan.

Electron transport measurements in plasma processing gases are being made in collaboration with researchers from Centro de Cincias Fisicas, UNAM, Mexico.

External Recognition (invited talks):

1. K. L. Steffens, "Optical and Electrical Measurements in Fluorocarbon Plasmas in the GEC Cell," 3rd International Workshop on Fluorocarbon Plasmas (Sarcenas, France) March 22, 2000. *INVITED.*
2. J. K. Olthoff, "Plasma Processing and Diagnostics at NIST," Motorola, Austin, TX, June 8,

2000. *INVITED.*

3. M. A. Sobolewski, "Electrical Measurements and Modeling of Radio-Frequency Discharges," Naval Research Laboratory, Washington, DC, November 12, 1999. INVITED.
4. E. C. Benck, "RF Plasma Research and the GEC Reference Cell at NIST", State University of New York - Buffalo, Buffalo, NY, April 28, 2000. INVITED.
5. K. L. Steffens, "Planar Laser-Induced Fluorescence Investigations of Fluorocarbon Plasmas," 47th International Symposium of the American Vacuum Society, Boston, MA, October 3, 2000. INVITED.
6. J. K. Olthoff, "The GEC Cell: An "Historical" Overview," 53rd Gaseous Electronics Conference, Houston, TX, October 25, 2000. INVITED.
7. M. A. Sobolewski, "Using Radio-Frequency Electrical Measurements as a Plasma Diagnostic," 53rd Annual Gaseous Electronics Conference, Houston, TX, October 25, 2000. INVITED
8. M. A. Sobolewski, "Determining Ion Flux and Ion Energies from Radio-Frequency Electrical Measurements," Sematech RF Plasma Processing Technology Forum, Sunnyvale, CA, November 1, 2000. INVITED
9. L. G. Christophorou, "Electron Collision Cross Sections and Their Technological Significance," Hokkaido University, Sapporo, Japan, May 8, 2000. INVITED
10. L. G. Christophorou, "Electron Interactions with Plasma Processing Gases: The NIST Program," Hokkaido University, Sapporo, Japan, May 10, 2000. INVITED
11. L. G. Christophorou, "Needed Data on Electron Collisions for Plasma Processing," Muroran Institute of Technology, Muroran, Japan, May 15, 2000. INVITED
12. L. G. Christophorou, "Electron Interactions with Excited Atoms and Molecules," Sophia University, Tokyo, Japan, May 22, 2000. INVITED
13. L. G. Christophorou, "Electron-Molecule Interactions: Basic Studies and Applications," Keio University, Tokyo, Japan, May 23, 2000. INVITED
14. L. G. Christophorou, "Electron Interactions with Excited Atoms and Molecules," RIKEN Institute, Tokyo, Japan, May 25, 2000. INVITED
15. L. G. Christophorou, "Electron Interactions with Excited Atoms and Molecules," Workshop on Electron-Driven Processes: Scientific Challenges and Technological Opportunities, Stevens Institute of Technology, Hoboken, NJ., May 16-17, 2000. INVITED
16. L. G. Christophorou, "Assessed Cross Sections and Transport Coefficients for Plasma Processing Gases," Motorola, Austin, TX, June 8, 2000. INVITED
17. L. G. Christophorou, "Electron Collision Cross Sections and Rate Coefficients for Plasma Processing Gases Derived from Critically Assessed Data," International Conference on Pulse Investigations in Chemistry, Biology, and Physics, Leba, Poland, September 9-13, 2000. INVITED
18. L. G. Christophorou, "Electron Interactions with Excited Atoms and Molecules," 53rd Gaseous Electronics Conference, Houston, TX, October 24, 2000. INVITED

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1. M. A. Sobolewski and K. L. Steffens, "Electrical control of the spatial uniformity of reactive species in plasmas," J. Vac. Sci. Technol. A 17, 3281-3292 (1999).
2. W. R. Entley, J. G. Langan, B. S. Felker, and M. A. Sobolewski, "Optimizing utilization efficiencies in electronegative discharges: The importance of the impedance phase angle," J. Appl. Phys. 86, 4825-4835 (1999).
3. M. A. Sobolewski, "Dynamic model of the plasma sheath in high-plasma-density, radio-frequency discharges," in Proceedings of the 1999 International Conference on Phenomena in Ionized Gases, Warsaw, Poland, Vol. 1, pp. 141-142 (1999).
4. Y. Wang, A. N. Goyette, M. Misakian, and J. K. Olthoff, "Mass-resolved studies of positive ions in high density plasmas generated in CHF3, C2F6, and CH2FCF3 and their mixtures with Ar," in Proceedings of the XIII International Conference on Gas Discharges and their Applications, Glasgow, Poland, Vol. 2, pp. 655-658 (2000).
5. L. G. Christophorou and J. K. Olthoff, "Electron interactions with SF6," J. Phys. Chem. Ref. Data 29, 267-330 (2000).
6. Y. Wang, E. C. Benck, M. Misakian, M. Edamura, and J. K. Olthoff, "Time-resolved measurements of ion energy distributions and optical emissions in pulsed radio-frequency discharges," J. Appl. Phys. 87, 2114-2121

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7. M. Misakian and Y. Wang, "Calculation of ion energy distributions from radio frequency plasmas using a simplified kinetic energy approach," J. Appl. Phys. 87, 3646-3653 (2000).
8. A. N. Goyette, Y. Wang, M. Misakian, and J. K. Olthoff, "Ion fluxes and energies in inductively coupled radio-frequency discharges containing C2F6 and c-C4F8," J. Vac. Sci. Technol. A 18, 2785-2790 (2000).
9. A. N. Goyette, Y. Wang, and J. K. Olthoff, "Inductively coupled plasmas in low global-warming-potential gases," J. Phys. D: Appl. Phys. 33, 2004-2009 (2000)M. Misakian, E. Benck, and Y. Wang, "Time evolution of ion energy distributions and optical emission in pulsed inductively coupled radio frequency plasmas," J. Appl. Phys. 88, 4510-4517 (2000).
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11. L. G. Christophorou and J. K. Olthoff, "Electron collision data for plasma-processing gases," Advances At. Mol. Opt. Phys. 44, pp. 59-98 (2000).
12. L. G. Christophorou and J. K. Olthoff, "Electron interactions with excited atoms and molecules." Advances At. Mol. Opt. Phys. 44, pp. 155-293 (2000).
13. Y. Wang, M. Misakian, A. N. Goyette, and J. K. Olthoff, "Ion fluxes and energies in inductively coupled radio-frequency discharges containing CHF3," J. Appl. Phys. 88, 5612-5617 (2000).
14. M. A. Sobolewski, "Sheath model for radio-frequency-biased, high density plasmas valid for all ω/ωi," Phys. Rev. E, 62, 8540-8553 (2000).

Development of Quantitative Measurements for Vacuum Process Control

Technical Contacts:
J.P. Looney, R.F. Berg, D.S. Green (University of Maryland)

Objective:

Develop a quantitative measurement capability to enable a real-time, *in-situ* semiconductor process-control scheme, building upon competence in optical diagnostics and flow calibration techniques.

Customer Needs:

The increasing volume and complexity of vacuum processing, most notably in the semiconductor industry, requires real-time monitoring and control of process gases, reaction products, and gaseous contaminants. Our previous work demonstrated that residual gas analyzers (RGAs) could be made quantitative for *in-situ* monitoring of reaction products, but the ±5 to 10 % imprecision (from analyte generation in the ionizer) was too large for process control, as is variability among mass flow controllers. Optical techniques are promising for real-time monitoring, but realizing their potential requires a better understanding of the factors limiting their performance. For mass flow controllers (MFCs), we need the industry to help identify key measurement and operational challenges to more consistent performance.

Technical Strategy:

In FY00 we began developing an advanced chemical process monitor based on cavity ring-down spectroscopy (CRDS) to quantify the HF generated in the thermal chemical vapor deposition (CVD) of tungsten metal films (WF_6 in an H_2-rich environment). Our approach is to establish compact, low-cost and robust optical diagnostic hardware at NIST, then transition it to Prof. Gary Rubloff's CVD facility at the University of Maryland for process control trials. With CRDS, we expect to achieve the desired measurement precision, and hope to use it to improve other detection methods such as RGAs. For MFCs, we convened industry leaders to help develop programmatic targets for NIST.

Accomplishments:

Our initial focus was to develop a measurement strategy utilizing low-cost continuous wave (CW) diode lasers. Given the HF partial pressures expected in the CVD reactor (1 Pa to 10 Pa) and the weak (0 to 4) overtone band of HF, we chose the 670nm -700 nm region as the target band as measurements here are vastly easier than in the mid-infrared where fundamental-band transitions exist. Calculations were completed to check the line strengths and CRD absorption characteristics for this band. Absorption lines of H_2O, a potential contaminant, were also identified in this region. Next, diode lasers at 670 nm and 685 nm were acquired and re-engineered to interface with current and temperature controllers. Problems persist in the temperature control and tuning capabilities of these diodes, and new strategies are being implemented to overcome them. A 50 cm transfer cavity and electronics were built for frequency stabilization of the diode laser. Electronics and initial tests of locking the transfer cavity to a frequency-stable HeNe laser were completed. Partially-reflective custom optics and special glass tubes were made for this cavity. Initial trials were conducted to test various optical configurations, including a fast (100 ns rise-time) acousto-optic deflector to rapidly switch the diode laser. The acousto-optic modulator and switching circuit have been tested and optimized. Work is in progress to lock the diode laser to the same transfer cavity and implement an acousto-optic modulator in a double-passed configuration for continuous laser tuning. Robust laboratory realization of this CW-CRDS approach is expected in FY01.

In order to promote more accurate and precise measurements with MFCs, we convened a workshop that identified five major recommendations for NIST. These were to 1) increase the range of transfer standards for round-robin tests (0.01 sccm to 1000 slm), 2) reduce uncertainty of primary (0.025 %) and transfer (0.1 %) standards for gas flow, 3) expand, reprioritize and conduct thermophysical measurements for the priority list of electronic gases, 4) establish and maintain a public, Web-based database of gas properties, and 5) develop metrology to characterize liquid flow controllers. These recommendations now form the basis of new and ongoing projects in the Division.

External Recognition:

Looney, J.P., ***"Highlights Below 100kpa of the 3rd CCM Pressure and Vacuum Conference,"*** 2000 Measurement Science Conference, Anaheim, CA, January 19, 2000. Invited

Looney, J.P., ***"Cavity Ring-down Spectroscopy,"*** Dept. of Physics, University of Toronto, Toronto, Canada, April 16, 2000. Invited

Looney, J.P., ***"Cavity Ring-down Spectroscopy,"*** Center for Process Analytical Chemistry, Spring Meeting, Seattle, WA, May 5, 2000. Invited

Looney, J.P., ***"XHV Measurement Techniques,"*** Workshop on Extreme High Vacuum and Surface Conditioning, Jefferson Laboratory, Newport News, VA, June 5, 2000. Invited

Publications:

Berg. R.F., Tison, S.A., ***"Laminar Flow of Four Gases Through a Helical Rectangular Duct,"*** AIChE Journal (in press).

Green, D.S., Herron, J.T., and Sieck, L.W., ***"Chemical Kinetics Database and Predictive Schemes for Humid Air Plasma Chemistry. Part I: Positive Ion-Molecule Reactions,"*** J. of Plasma Chemistry and Plasma Processing (in press).

Green, D.S., Herron, J.T., and Sieck, L.W., ***"Chemical Kinetics Database and Predictive Schemes for Humid Air Plasma Chemistry. Part II: Neutral Species Reactions"*** J. of Plasma Chemistry and Plasma Processing (in press).

Green, D.S., Looney, J.P., and Rubloff, G.W., ***"Application of CW-CRDS to Monitor and Control Chemical Vapor Deposition,"*** Proc. IEEE/LEOS Summer Topicals 2000, Optical Sensing in Semiconductor Manufacturing, (in press).

F. Modeling and Design Metrology Program

Device scaling to atomic dimensions and integration of components on single chips exceeding a billion active components requires new concepts in modeling of processes, circuit performance, and thermal management. Lead counts of several thousand per chip and test frequencies in the microwave regime challenge current test methodologies. The overall task is to develop modeling and test methodologies to address these new requirements.

The industry needs very efficient and reliable simulation methods as device structures and packages continue to rapidly evolve. Conventional methods are no longer suitable and simulators must include quantum mechanical physics. Benchmarking semiconductor device simulation tools that include quantum mechanical effects are important facets of the overall strategy.

Accurate at-speed test methodology of digital integrated circuits is also a critical requirement. Traditional methods utilizing IC contact probing technology requires large contact pads incompatible with current IC designs. The development of alternative probing approaches through non-contact and intermittent probing techniques appear very promising. However, to implement these techniques, solving the at-speed test calibration issues is crucial.

With the challenges facing designers and the rising costs of development, it is crucial to develop accurate testing, modeling and simulation strategies. Keeping pace with the technology and serving the needs of the industry involve more than basic measurements.

Metrology for Simulation and Computer-Aided Design

Technical Contacts:

Allen R. Hefner, Jr.

"The NIST Insulated-Gate Bipolar Transistor model is internationally accepted as the standard by which other IGBT models are compared."
Benefit Analysis of IGBT Power Device Simulation Modeling, Research Triangle Institute, 1999

Objective:

To facilitate the efficient and reliable application of semiconductor computer-aided design (CAD) tools and System-on-a-Chip (SoC) design methodologies by providing leadership for the development of an industry infrastructure for establishing model accuracy, developing methods for simulator model validation and benchmarking, developing metrology necessary for providing model data and model parameter extraction sequences, and developing metrology infrastructure required for a block-based design paradigm.

Customer Needs:

Efficient and reliable simulation methods are becoming more important as device structures and packages rapidly evolve. In addition, higher speed and higher power devices increase the importance of including the effects of packages in system performance simulation. However, advanced device electrical and thermal characterization procedures and validation of models used in computer-aided design tools have not kept pace with the application of the new device types and processes.

Several device technologies have evolved to an extent that conventional modeling and simulation capabilities are not suitable. For example, as CMOS devices are scaled to atomic dimensions, simulators must include quantum mechanical physics. The SRC/NIST/NSF Workshop on Nanoscale Transistors: Technology, Physics, and Simulation (Feb. 1999) identified quantum mechanical device simulation as an area required for device simulator progress. In addition, the device types used for power and microwave applications can no longer be represented by conventional device models provided in circuit and system simulation programs.

The driving force in today's semiconductor industry is the need to maintain a rate of improvement of 2x every two years in high-performance components. Currently, these improvements rely exclusively on advances made in semiconductor miniaturization technology. The 1999 ITRS (International Technology Roadmap for Semiconductors) suggests that, "innovation in the techniques used in circuit and system design will be essential to maintain the historical trends in performance improvement." Achievement of this advancement in circuit and system design techniques is increasingly becoming dependent on integrating multiple silicon technologies into an SoC. Design challenges for SoC are overcome with the use of block-based design approaches that emphasize design reuse that include Built-In-Self-Test (BIST) functions and accommodate Design-For-Test (DFT).

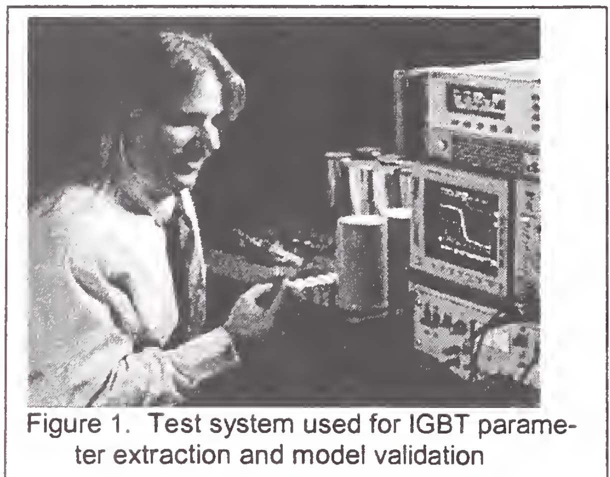


Figure 1. Test system used for IGBT parameter extraction and model validation

Technical Strategy:

NIST addresses these needs by developing the theoretical foundations, standards, model validation procedures, and associated experimental techniques for the measurement of device system block electrical and thermal characteristics, and package electrical and thermal characteristics. NIST is developing, with industry, accepted procedures for validating device models for circuit simulation. NIST is developing procedures for characterizing the thermal and electrical performance of micro-electronic packages that are compatible and useful for CAD of boards and systems.

Device and Process Simulation Benchmarking

Accurate models and benchmarking procedures are becoming more important for device and process simulators. Current tasks include development of mobility, band gap, and intrinsic carrier concentration models for accurate simulation of compound semiconductor devices, and benchmarking of semiconductor device simulation tools that include quantum mechanical effects, including MEDICI, UTQuant, NCSU code, and NEMO.

Milestone: By 2002, complete benchmarking of QM effects in 2-D device simulator for MOSFET with ultra thin gate oxide.

Compact Package Electrical Interconnect Models
Interconnect structures are becoming a dominant factor in limiting the performance of modern computer, communication, and power systems. Various multi-chip modules and discrete package interconnect systems are characterized using the Time Domain Reflectometry Technique (TDR).

Milestone: By FY 2001, develop a TDR test system with low source impedance (10 Ω), and characterize low-impedance interconnects used in microprocessor voltage regulator modules, advanced memory busses, and power electronic systems.

Package Thermal Metrology and Models
Accurate and timely simulation of system thermal performance requires new temperature measurement methods, new simulation methodologies, and validation procedures. Currently we use NIST electro-thermal network simulation methodology, including thermal network component models for semiconductor packages and heatsinks, and development of methodologies to validate the performance and accuracy of compact package thermal models.

Compact Device Electrical Models
Only recently has there been a significant effort in developing an infrastructure for validating the performance of compact models. An example of this activity is the NIST/IEEE Model Validation Working Group, founded in 1994 and now having over 200 members from 100 different technical organizations. For more information see http://ray.eeel.nist.gov/modval.html.

Milestone: By FY 2002, develop test system and models for SiC three terminal device.

Metrology for Multi-Technology SoC System Blocks
The emergence of the block-based design paradigm that emphasizes design reuse imposes various metrology and standardization challenges. The NIST research provides the metrology infrastructure required to facilitate the emergence of effective SoC design methodologies for multi-technology systems. Current tasks include (1) development of test structures for multi-technology process monitoring, (2) development of measurement infrastructure to calibrate multi-technology built-in self test (BIST) functions for system sub-blocks; (3) development of metrology to validate behavioral models for the multi-technology system blocks, and (4) development of benchmarking procedures for system block simulation based Analog Hardware Description Language design.

MILESTONE: By 2002, complete development of test bench on a chip metrology necessary for multi-technology System-on-a-Chip, block-based design and develop test structures for monitoring multi-technology SoC processes.

Accomplishments:

Provided leadership in developing a national agenda for modeling and simulation. Hefner presented an invited talk entitled, "Model Verification, Validation, and Accreditation of Semiconductor Device CAD Systems," at the National Academy of Sciences, National Research Council Workshop on Modeling and Simulation Opportunities in Manufacturing, April 26-27, 1999. The talk described the methodology for model validation being applied by the NIST/IEEE Working Group on Model Validation. The objective of the workshop was to develop a prospectus for a study that will recommend a national research agenda to address shortcomings in current modeling and simulation capabilities and to develop enhanced opportunities for coupling modeling and simulation with manufacturing.

- Impact study published on NIST models. An assessment of the U.S. economic impacts of the NIST IGBT model is detailed in a recent study entitled "NIST Planning Report 99-3: Benefit Analysis of IGBT Power Device Simulation," prepared by M. Gallaher and S. Martin, Research Triangle Institute Center for Economic Research (April 1999). The press release

announcing this study appeared on the front page of the NIST Web site, appeared in the NIST Update, and was highlighted in the NIST Director's "State-of-the-Institute" speech. The economic impact study quantified the direct impacts of the NIST IGBT modeling at $18M (30 times the cost of the NIST program) and the indirect benefits at $40M/year, largely due to energy savings.

- NIST interconnect metrology proves valuable for EMI simulation. Models obtained from recent interconnect metrology research at NIST enabled the simulation of the EMI performance of various power converter topologies, as described in two NIST publications. In recent years, Electro-Magnetic-Interference (EMI) considerations have become increasingly important as Electro-Magnetic-Compatibility (EMC) regulations have become more stringent. The NIST metrology provides, for the first time, the capability to use simulation in the design of power converters with reduced EMI emissions.

- Developed High-Speed Semiconductor Device Transient Thermal Image System. The system provides the capability to measure the transient temperature distributions on the surface of a silicon chip with 10 ns temporal, 15 μm spatial resolution. The system uses computer-control software with a graphical user interface for controlling the translation stages, digitizing oscilloscope, and device test fixture temperature controller. The system also required the development of algorithms for calibrating and extracting the transient temperature waveform from an infrared microscope signal.

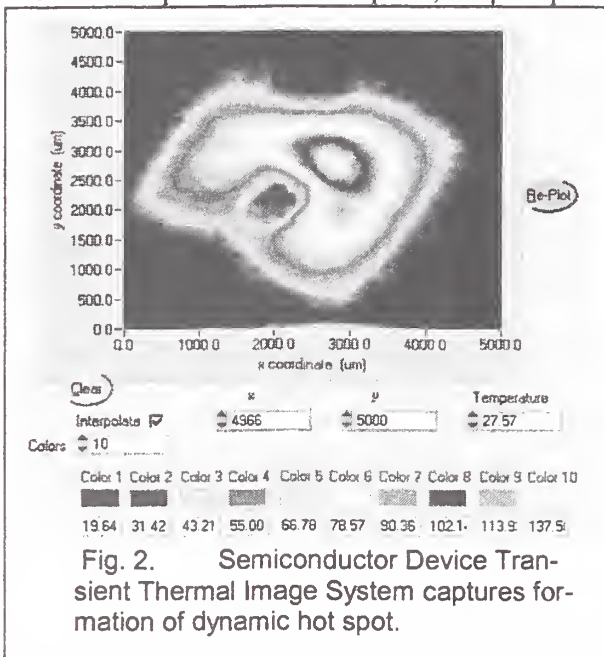
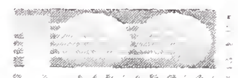


Fig. 2. Semiconductor Device Transient Thermal Image System captures formation of dynamic hot spot.

- Developed IGBT model validation procedures and applied to component library. Developed circuits and measurement methods for validating IGBT models for soft-switching conditions, applied the methods to models provided in a software vendors component library, and published results. Enhancements were made to the Hefner IGBT model that is provided in commercial circuit simulators as a result of this validation work. The NIST IGBT model was then used to simulate IGBT soft-switching performance in two papers; one describing reduced EMI emissions for soft-switched inverters, and the other describing the difference in soft-switching performance between different IGBT types.

- Developed capability to characterize and predict IGBT dynamic failures. The dynamic failure characteristics and avalanche-sustaining capability of various IGBT types, including new high-energy capable IGBTs, were measured using the unique NIST nondestructive failure tester and simulated using the NIST IGBT model. The measurements and simulations enabled the prediction of the mechanism resulting in High Avalanche Energy IGBTs and demonstrated the capability of the NIST IGBT model to predict the sustaining time and conditions for failure of both high-energy and conventional IGBT types.

- Developed software package for IGBT model parameter extraction (IMPACT). The software consists of five programs, LINMSR, SATMSR, LFTMSR, BTAMSR, and CVMSR, that extract the 20 physical and structural parameters of the most recent version of the NIST IGBT model. The programs have a graphical user interface, use the IEEE 488 bus to control the measurement instruments and collect data, and use various algorithms for fitting the IGBT model equations to the data. The new software package will facilitate the development of IGBT component libraries and enable end users of the simulation software products to extract model parameters themselves.



- SRC/NIST/NSF Workshop held at NIST. The Workshop, "Research Issues and Directions for Nanotransistors: Technology, Physics, and Simulation," was attended by over 50 researchers from industry, academia, and government. The Workshop identified critical modeling and simulation issues, such as quantum effects, that must be solved if modeling and simulation are to have a significant impact on the development of future nano-transistors. Modeling and simulation can speed progress in the development of future transistors if the infrastructure and physics are in place to attack relevant problems. As a result of this workshop, NIST developed a benchmarking procedure for quantum mechanical simulations that lead to an improvement in performance of one of the software products.

- Developed metrology for SiC diode characterization. As a result of NIST collaboration with CREE and Virginia Polytechnic Institute and State University (VPISU), under DARPA funding, it was demonstrated for the first time that SiC MPS (Merged PIN-Schottkey) diodes can substantially reduce energy consumption and EMI emissions for power converters and adjustable-speed drives. This reduction was demonstrated for diodes with ratings in the 300 V to 1500 V range, which represents the bulk of the applications in power electronics. CREE has decided, based on this demonstration, to pursue the commercialization of these diodes. This development is critically important to EPRI (Electric Power Research Institute) because 60 % of electrical power used in the U.S. is delivered to motors through IGBTs using adjustable speed drives, and the performance improvements offered by SiC diodes over Si diodes enhance the efficiency and reliability of these IGBT-based drives. DARPA is funding development of this technology for use in applications ranging from all-electric tanks to all-electric ships. NIST's interest in SiC devices is driven by our analysis that recent materials advances make these devices commercially attractive.

Future Plans:

Benchmarking 2-D Quantum Mechanical Effects in Device Simulators: The benchmarks will extend the NIST work on benchmarking 1-D QM device simulators for MIS capacitors to: 1) benchmarking 2-D QM device simulators for MIS capacitors, and 2) benchmarking 2-D QM effects in MISFETs devices.

SoC Test Bench on a Chip: Develop test bench on a chip to measure the performance of multi-technology system blocks used by SoC designs. The test system will enable high precision calibration of integrated sensor built-in-self-test functions and evaluation of the interaction between system blocks used in multi-technology SoC designs.

SiC avalanche uniformity and robustness metrology: SiC power diodes andpower MOSFETs will be subjected to avalanche breakdown voltage pulses, and the high-speed transient thermal imaging system will be used to observe the uniformity of chip heating. This new metrology provides insights into the influence of materiel defects on device performance and reliability.

Thermal analysis of MEMS micro-hotplate based sensors: The transient thermal imaging system will be used to examine the high speed heating and cooling properties of the suspended MEMS structures that form micro-hotplate based sensors. The transient thermal imaging metrology will be used to validate the thermal system sub-blocks of microfluidic chamber heaters and integrated gas sensors.

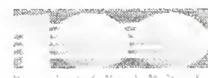
High speed transient thermal imaging system refinement: This work involves adding and/or changing code to add flexibility, such as user-selectable averaging for noise rejection, emissivity calibration options, and a number of enhancements to improve data acquisition time.

Collaborations:

Analogy/IR/NIST, development of hundreds of IGBT library component models (Allen R. Hefner)
Analogy/IR/NIST, development of package thermal model library component models (Allen R. Hefner)

Analogy/POWERX/NIST, development of high power IGBT module library component models (Allen R. Hefner)

Avanti Inc./University of Arkansas, SiC power diode model library (Allen R. Hefner)



CREE, SiC diodes (David W. Berning)

CREE/NIST, development of SiC MPS-diode electro-thermal model (Allen R. Hefner)

DELPHI/Virginia Polytechnic Institute and State University, electronic interconnect characterization for vehicle auxiliary motor drive interconnects (Allen R. Hefner)

Division 811, development of low-characteristic impedance time domain reflectometry (Allen R. Hefner)

Division 811, Jim St. Pierre, collaborating on defining research goals for metrology and benchmarking related to Systems-on-a-Chip (Angela M. Hodge)

Division 812, J. J. Kopanski, TCAD simulations (John Albers)

Division 812 (Nick Paulter), under ATP project to develop low-impedance transmission line characterization (David W. Berning)

Division 812, SCM Project, implant simulation and device simulation (Allen R. Hefner)

Division 812, Thin-Film Process Metrology Project and Gate Dielectric and Interconnect Reliability Project, new task on benchmarks for quantum-mechanical device simulation (Allen R. Hefner)

General Electric CRD/NIST, development of IGBT module models and parameter extraction tools (Allen R. Hefner)
Harris Semiconductor, development of component models for Harris IGBTs (Allen R. Hefner)

Rockwell Science Center/NIST, development of SiC transistor models (Allen R. Hefner)

TMA, implementation of new device physics into Medici device simulator (Allen R. Hefner)

University of Maryland, development of multi-technology System-on-a-Chip (Allen R. Hefner)
University of Maryland, Professor Neil Goldsman, collaborating on benchmarking quantum mechanical simulators for semiconductor devices (Angela M. Hodge)

University of Maryland, Professor Robert Newcomb, collaborating on defining research goals and objectives for NIST/SED initiative on Systems-on-a-Chip (Angela M. Hodge)

University of Maryland, quantum mechanical effects in 2-D semiconductor devices simulators (Allen R. Hefner)

University of Maryland, Reliability Physics Department, reliability issues for PEBB-like devices (Allen R. Hefner)

Virginia Polytechnic Institute and State University, package interconnect electrical characterization (Allen R. Hefner)

Virginia Polytechnic Institute and State University, SiC power device utilization (Allen R. Hefner)

Virginia Tech, SiC diodes (David W. Berning)

Standards Committee Participation:

ASTM Committee, F107 Packaging, member (George G. Harman)

EIA/SEMATECH Compact Model Council (Allen R. Hefner)

IEEE Electron Devices Society, Standards Technical Committee, Chairman (Allen R. Hefner)

Software:

HOTPAC (Programs for Thermal Analysis) distributed (John Albers)

IGBT Model PArameter extraCTion (IMPACT) software (Allen R. Hefner)

IGBT Network Simulation and Transient Analysis Tool (INSTANT) software package (Allen R. Hefner)

Igbt3.sin MAST circuit simulator model template (Allen R. Hefner)

NIST buffer layer IGBT model and library, distributed by Avanti Inc. as part of Saber simulator package (Allen R. Hefner)

NIST chip, package and heatsink thermal network component models, distributed by Avanti Inc. as part of Saber simulator package (Allen R. Hefner)

NIST IGBT electro-thermal model and library, distributed by Avanti Inc. as part of Saber simulator package (Allen R. Hefner)

NIST IGBT model and library, distributed by Avanti Inc. as part of Saber simulator package (Allen R. Hefner)

NIST IGBT model and library, distributed by OrCAD Inc. as part of PSPICE simulator package (Allen R. Hefner)

RESPAC (a collection of computer programs for two-probe resistance (spreading resistance) and four-probe resistance calculations) distributed (John Albers)

External Recognition:

Received the IEEE Third Millennium Medal (George G. Harman)

Publications:

Adams, V. H., Joshi, Y., and Blackburn, D. L., Three-Dimensional Study of Combined Conduction, Radiation, and Natural Convection from an Array of Discrete Heat Sources on a Horizontal Board in a Narrow-Aspect-Ratio Enclosure, Journal of Heat Transfer, Vol. 121, November 1999, pp. 992-1001.

Berning, D., and Hefner, A., IGBT Model Validation for Soft Switching Applications, IEEE Transactions on Industry Applications, Society Meeting, 1999, pp. 683-691.

Berning, D. W., and Hefner, Jr., A. R., IGBT Model Validation for Soft-Switching Applications, Conference Record IEEE Industry Applications Society Annual Meeting, Phoenix, Arizona, October 3-7, 1999, pp. 683-691.

Harman, G. G., The Effect of Polymer Material Properties on Wire Bonding to MCMs and Advanced Copper-Low-k Integrated Circuits, Proceedings of the 2nd Annual IEEE-CPMT/ASME/SPE/SPIE/MRS/ARM/SF2M Workshop (POLY'99), Paris, France, December 12-15, 1999.

Hefner, A., and Bouche, S., Automated Parameter Extraction Software for Advanced IGBT Modeling, Proceedings of the IEEE Workshop on Computers in Power Electronics (COMPEL 2000), July 2000, pp. 9-17.

Hefner, A. R., Singh, R., Lai, J. S., Berning, D. W., Bouche, S., and Chapuy, C., SiC Power Diodes Provide Breakthrough Performance for a Wide Range of Applications, in the extended abstracts of 1st International Workshop on Ultra-Low-Loss Power Device Technology, pp. 140-147, June 2000, Nara Japan.

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Hefner, A. R., Singh, R., Lai, J. S., Berning, D. W., Bouche, S., and Chapuy, C., SiC Power Diodes Provide Breakthrough Performance for a Wide Range of Applications, Japanese Future Electron Devices Journal, Vol. 11, August 2000, pp. 122-130.

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Song, B. M., Zhu, H., Lai, J. S., and Hefner, Jr., A. R., Switching Characteristics of NPT- and PT-IGBTs under Zero-Voltage Switching Conditions, 1999 IEEE Industry Applications Society Meeting, pp. 722-728.

Zhu, H., Lai, J.-S., Tang, Y., Hefner Jr., A. R., and Chen, C., Modeling Based Examination of Conducted EMI Emissions from Hard- and Soft-switching PWM Inverters, Proceedings of the IEEE Industrial Applications Society Meeting, Phoenix, Arizona, October 3-7, 1999, pp. 1879-1886.

Non-Linear Device Metrology and Modeling

Technical Contacts:

D. DeGroot

"Agilent Lightwave Division would like to encourage NIST's continued work to develop the … characterization, so that the technology can become more widely available." **Dennis Derickson, Aglient Technologies**.

Objective:

Develop and support general methods of characterizing nonlinear devices, components, and circuits used in digital wireless communications; refine and transfer these methods through interactions with industrial research and development laboratories.

Fig. 1. Dr. Kate Remley performs large-signal measurements of an RF power amplifier using the Nonlinear Network Measurement System

Customer Needs:

Radio-Frequency measurements are applied extensively in the deployment of commercial wireless communication systems. They are crucial to all stages of system development, from device modeling, to circuit design and system performance characterization. NIST's RF and microwave measurement support recently expanded to address the critical need for accurate measurements of nonlinear electrical devices and networks, and to support industrial standards development.

Technical Strategy:

The Nonlinear Device Characterization Project is focusing on the verification of model- and measurement-based descriptions of devices and circuits containing nonlinear elements, primarily transistors and RF power amplifiers. The strategy is to develop a world-class measurement facility that will be used as the reference system in model and measurement intercomparison. The reference system will be used to develop new modeling methods and to build "traceable models" with accuracy linked to measurements used to form them.

Traditional microwave circuit design has relied on the ability to cascade circuit elements through simple linear operations and transformations. When an RF circuit includes a nonlinear element, engineers lose the ability to predict circuit performance across operating environments or states. With the wireless revolution, many researchers have devoted their time to developing models of nonlinear devices that will work with existing computer-aided design (CAD) techniques. Others have worked on developing specialized and functional tests that show how nonlinear behavior might affect system performance. Presently, there is a critical need for fundamental RF measurement techniques to verify and validate these models and figures of merit. Contributions in this area will significantly improve design-cycle efficiency and trade between manufacturers, and will eventually facilitate improvements in communications through the full incorporation of nonlinear models at the system design level.

The project recently acquired and established a new measurement facility known as the Nonlinear Network Measurement System (NNMS). The system provides the most general approach to measuring large-signal responses. It is a stimulus-response network analyzer that supplies periodic signals, then acquires broadband incident and reflection waveforms at the device under test. The NIST facility will be used as a reference system in measurement and model comparisons.

The Nonlinear Network Measurement System is first being applied to canonical circuits to compare general measurements with predictions made by commercial CAD simulators and new behavioral models. The goal is to develop a stable verification

device that can be used in inter-laboratory comparisons.

Accomplishments:

- Collaborated with the Intel Technical CAD (TCAD) Division to measure the behavior of high-speed digital transistors (MOSFETs) and to extract accurate device parameters. The key technological hurdles were the measurement of three-port devices when the three ports are connected in different metalization layers, and the high RF losses encountered in commercial CMOS technology. NIST personnel designed two sets of calibration standards for the three-port devices. Intel fabricated three generations of test wafers and worked with NIST in verifying the calibrations. This activity also relied on new software developed by the High-Speed Microelectronics Project to remove contact-pad effects. The new approach is being used by TCAD engineers to quantify device behavior with a much higher degree of accuracy.

- In collaboration with Professor K. C. Gupta of the University of Colorado at Boulder, applied artificial neural networks (ANNs) to improve the modeling of on-wafer open-short-load-thru (OSLT) standards and coaxial line-reflect-match (LRM) calibrations used for calibrating vector network analyzers. The new methods will be used in TDNACal and new NNMS software.

- Developed a complete Open-Short-Load-Thru (OSLT) calibration for the NIST TDNACal software that implements equivalent circuit model descriptions. This new calibration is a significant enhancement to existing software, and for the first time, allows NIST to study measurement uncertainty in OSLT calibrations that make use of the equivalent-circuit model parameters. Presentation of this work at the 54th ARFTG Conference received the Best Paper Award.

- Characterized the accuracy of several proposed calibration techniques for microwave vector network analyzers (VNA). Project staff discovered significant errors in the proposed methods and introduced a new robust OSLT calibration method that offers demonstrably improved accuracy in four-sampler VNA measurements.

- Discovered nonlinear error mechanism in the Nose-to Nose calibration. Through an innovative combination of large-signal and small-signal analyses, showed how nonlinear junction capacitance in the sampler circuit induces an error that had been ignored in the initial Nose-to-Nose analysis.

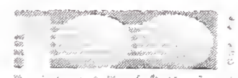
- Initiated NIST's Nonlinear Network Measurement System (NNMS) and conducted NIST's first large-signal nonlinear device verification experiments. Agilent Technologies delivered the NNMS instrument in fulfillment of a custom equipment contract and extensive collaborative research effort with NIST.

Future Plans:

The project team is developing accurate calibration and measurement techniques for the NNMS, including validation of the Nose-to-Nose calibration technique, the only practical method of measuring the phase relations of components in signals with 50 GHz bandwidths. The project team is now refining the statement of measurement uncertainty in the Nose-to-Nose method and will apply it to the NNMS measurements.

MILESTONES By 2001, bound the measurement uncertainty of the Nose-to-Nose calibration; bound uncertainty in NNMS measurements; implement advanced OSLT calibration methods; develop user-friendly interface for the NNMS. By 2002, refine phase calibration uncertainty statement; add multiline TRL calibrations; add modulated signal stimuli; track changes in NNMS measurement uncertainty with impedance tuning.

Secondly, the measurement system is being applied to develop and verify artificial neural network (ANN) models for nonlinear active circuits being developed in cooperation with the University of Colorado. NNMS data will be used to train ANN models, to verify circuit operation and model predictions, and to validate a circuit optimization approach.
MILESTONES: By 2001, develop portable models for a nonlinear verification device; conduct measurement intercomparison using verification device; apply new modeling techniques to diode circuit design; develop generalized frequency-domain nonlinear models based on NNMS data; characterize example power amplifier and compare to advanced simulation results. By 2002, compare



sparse tone and modulated signal characterizations of power amplifiers; apply new nonlinear measurement-based models to power amplifier design; simulate link between system performance and amplifier nonlinearity.

Collaborations:

Intel, TCAD Department. To characterize MOSFETs at high-frequencies using vector network analysis techniques.

Agilent Technologies, Inc., Network Measurement and Description Group. To develop measurement uncertainty statement for NNMS and NNMS-like instruments.

University of Colorado, Electrical and Computer Engineering Department. To develop new measurement-based behavioral models of nonlinear RF circuits and devices.

NIST, N-WEST, EEEL Electromagnetic Technology Division, ITL Statistical Engineering Division. To develop standard nonlinearity, then use it to verify NNMS calibrations and modeling approaches; to extend nonlinear circuit models to system characterization.

External Recognition:

Automatic RF Techniques Group's Best Paper Award, 54th ARFTG Conference, 1999.

Automatic RF Techniques Group's Best Poster Paper Award, 55th ARFTG Conference, 2000.

Publications:

Jargon, K. C. Gupta, and D. C. DeGroot, "Artificial neural network modeling for improved on-wafer OSLT calibration standards," *Int. J. RF Microwave Computer-Aided Engin.*, vol. 10, no. 5, pp. 319-328, Sep., 2000.

L. Rouault, B. Verbaere, D. DeGroot, D. LeGolvan, and R. Marks, "Measurements and models of a power amplifier suitable for 802.16.1," IEEE 802.16.1p-00, Sep. 13 2000.

P. D. Hale, T. S. Clement, K. S. Coakley, C. M. Wang, D. C. DeGroot, and A. P. Verdoni, "Estimating the magnitude and phase response of a 50 GHz sampling oscilloscope using the "Nose-to-Nose" method," *55th ARFTG Conf. Dig.*, pp. 35-42, June 13, 2000.

D. C. DeGroot, P. D. Hale, M. Vanden Bossche, F. Verbeyst, and J. Verspecht, "Analysis of interconnection networks and mismatch in the Nose-to-Nose calibration," *55th ARFTG Conf. Dig.*, pp. 116-121, June 16, 2000.

K. A. Remley, D. F. Williams, and D. C. DeGroot, "Realistic sampling-circuit model for a Nose-to-Nose simulation," *2000 IEEE MTT-S Int. Microwave Symp. Dig.*, June 11-16, 2000.

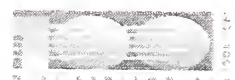
J. A. Jargon and D. C. DeGroot, "NIST unveils status of PIM testing," *Microwaves & RF*, pp. 78-81, Jan., 2000.

D. C. DeGroot, K. L. Reed, and J. A. Jargon, "Equivalent circuit models for coaxial OSLT standards," *54th ARFTG Conf. Dig.*, pp. 103-115, Dec. 3-4, 1999.

G. Test Metrology Program

Lead counts of several thousand per chip and test frequencies in the microwave regime challenge current test methodologies. The overall task is to develop test methodologies to address these new requirements.

Accurate at-speed test methodology of digital integrated circuits is a critical requirement. Traditional methods utilizing IC contact probing technology requires large contact pads incompatible with current IC designs. The development of alternative probing approaches through non-contact and intermittent probing techniques appear very promising. However, to implement these techniques, solving the at-speed test calibration issues is crucial. With the challenges facing designers and the rising costs of development, it is crucial to develop accurate testing strategies.



At-Speed Test of Digital Integrated Circuits

Technical Contacts:
Dylan Williams, *John Moreland, Joseph Kopanski*

Objective:

Develop and demonstrate metrology for the at-speed test of digital integrated circuits. The program will resolve the essential metrology issues of at-speed digital integrated circuit test. It will apply its results to atomic force microscopes (AFMs) modified to precisely position field probes above the surface of the integrated circuit and push the current on-chip sampling technologies now being explored by the industry.

Customer Needs:

The semiconductor industry needs accurate metrology for the at-speed test of digital integrated circuits ("Grand Challenges", page 11, 1999 National Technology Roadmap for Semiconductors). Traditional IC contact probing technology requires large contact pads incompatible with the operation and economic constraints of modern IC designs. Alternative probing approaches use non-contact probes, the intermittent-contact mode of the scanning capacitance microscope, electron beams, optical beams, or on-chip samplers that respond to either electric or magnetic fields near transmission lines in the circuits. AFM appears to be one of the most promising in the long term with prospects for 50 nm resolution and voltage sensitivities below 1 mV. However, the uncalibrated field measurements performed by these systems are a far cry from the precise measurements of voltages and currents required for electrical design.

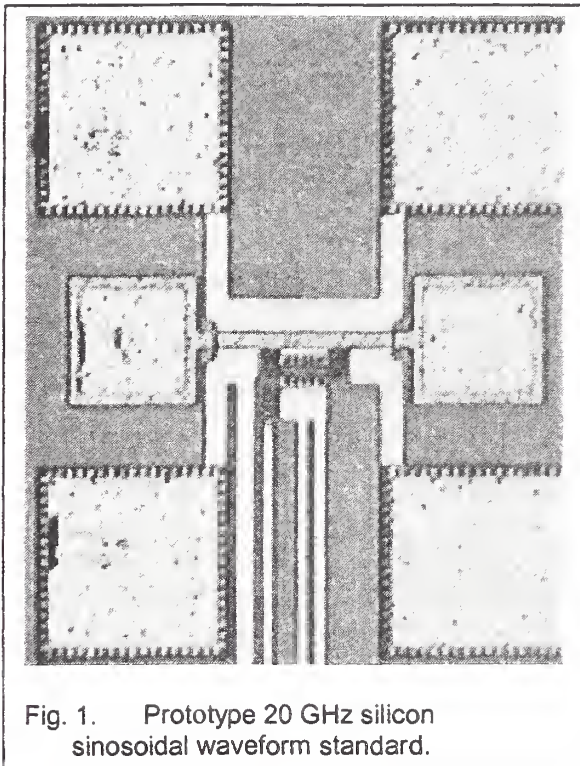


Fig. 1. Prototype 20 GHz silicon sinosoidal waveform standard.

Solving the critical at-speed test calibration issues will add enormous value to the probing systems currently being used or developed for high-performance digital integrated circuits. Implementing the methods on atomic-force microscopes, which we have already proven capable of performing these tests, will help speed the development and implementation of these new measurement tools, and so create a new paradigm for the at-speed test of high-speed digital integrated circuits.

Technical Strategy:

We will develop calibration artifacts with precisely known high-frequency voltages and circuits suitable for calibrating field probes and samplers of all types. We will focus on fundamental calibration issues: transforming the response of the probes to the electric and magnetic fields above the integrated circuit into accurate voltages and currents inside the circuit. The calibration artifacts will take the form of custom integrated circuits with special test structures evaluated by NIST.

We will first apply the calibration procedures to miniature AFM probes suspended on custom cantilevers designed for high frequency measurements. We will test both the intermittent-contact mode of the scanning capacitance microscope and noncontact probes of our own design. We will follow up with a round robin, and will use the results to help other groups to develop calibration approaches. We will also investigate the application of the calibration artifacts to the on-chip samplers now being pursued by a number of large semiconductor manufactures, including Intel, Motorola, and IBM.

After verifying the calibration approaches with sinusoidal signals, we will develop a waveform measurement capability on special test structures, and eventually on silicon. We will use this capabil-

ity to develop pulsed versions for calibrating time-domain measurement systems.

Milestone: By Oct 2000, construct and test electro-optic sampling system.

Milestone: By Oct 2001, develop 10 GHz sinusoidal voltage standard and test with the intermittent-contact mode of the scanning capacitance microscope, noncontacting AFMs, and/or e-beam system.

Milestone: By Oct 2001, demonstrate calibrated on-wafer waveform measurement.

Milestone: By Oct 2002, design and layout pulsed version of voltage source with built-in on-chip sampler. Design custom noncontacting probes for AFM test station.

Accomplishments:

- We have designed and tested a prototype sinusoidal waveform standard.
- We have constructed an electro-optic sampling system.
- We have performed feasibility tests of a ferromagnetic-resonance scanning probe.

Future Plans:

We will develop sinusoidal and digital waveform standards. We will disseminate our methods through industry presentations and conference and journal publications.

Publications:

D.F. Williams and D.K. Walker, "0.1-10 GHz CMOS Voltage Standard," IEEE Workshop on Signal Propagation on Interconnects, Titisee-Neustadt, Germany, May 19-21, 1999.

K.A. Remley, D.F. Williams, and D.C. DeGroot, "Realistic sampling-circuit model for a nose-to-nose simulation,"2000 International Microwave Symposium Digest, June 11-16, 2000.

U. Arz, D.F. Williams, D.K. Walker, J.E. Rogers, M. Rudack, D. Treytnar, and H. Grabinski, "Characterization of Asymmetric Coupled CMOS Lines,"2000 International Microwave Symposium Digest, June 11-16, 2000.

D.F. Williams, K.A. Remley, and D.C. DeGroot, "Nose-to-Nose Response of a 20-GHz Sampling Circuit," 54th ARFTG Conference Digest, Dec. 1-2, 1999.

U. Arz, H. Grabinski, and D.F. Williams, "Influence of the Substrate Resistivity on the Broadband Propagation Characteristics of Silicon Transmission Lines," 54th ARFTG Conference Digest, Dec. 1-2, 1999.

D.F. Williams, P.D. Hale, T.S. Clement, and J.M. Morgan "Mismatch corrections for electro-optic sampling systems," 56th ARFTG Conference Digest, Nov. 30-Dec. 1, 2000.

U. Arz, D.F. Williams, D.K. Walker, and H. Grabinski, "Asymmetric Coupled CMOS Lines: An Experimental Study," IEEE Trans. On Microwave Theory and Tech., vol. 48, no. 12, pp. 2409-2414, Dec. 2000.

D. F. Williams, B.K. Alpert, U. Arz, and H. Grabinski, "Causal characteristic impedance of planar transmission lines," submitted to IEEE Trans. Advanced Packaging.

D. F. Williams and K. Remley, "Analytic sampling-circuit model," IEEE Trans. on Microwave Theory and Tech., vol. 49, no. 6, June 2001.

Albrecht Jander, Pavel Kabos, and John Moreland, "Magnetic field imaging with a scanning ferromagnetic resonance probe," submitted to Applied Physics Letters, July 2000.

Albrecht Jander, John Moreland, and Pavel Kabos, "Micromechanical Detectors for Local Field Measurements Based on Ferromagnetic Resonance," submitted to Journal of Applied Physics, October 2000.

Measurements for Complex Electronic Systems

Technical Contacts:
Gerad N. Stenbakken

Objective:
To develop and disseminate methods and techniques for optimum testing scenarios by using new or improved modeling and test procedures, and estimating confidence levels and test coverage.

Customer Needs:
The U.S. test equipment industry is maintaining its world position through the development and deployment of increasingly accurate, easier-to-use automatic test systems that can also achieve high throughput rates. Both the manufacturers and users of such systems often need to prove their productivity in a highly competitive environment. Optimizing the testing procedures and reducing the test time required are goals beneficial to realizing the return on investment for expensive automatic test systems. Hence, there is an urgent need for better modeling methods and testing algorithms that can reduce the number of test points while maintaining a comprehensive test coverage. With the advent of embedded firmware in not only digital but also mixed-signal devices and instruments, the task of accounting for pernicious nonlinear, time-variant interactions between the hardware and software becomes more difficult in an efficient, yet comprehensive, testing strategy.

Technical Strategy:
Expansion of the present NIST expertise in modeling and testing complex electronic systems requires the investigation and application of statistical analysis methods to ill-posed problems. Appropriate inverse transformations may be required to "de-embed" the effects of firmware, along with modeling and accounting for time dependencies. Improved methods are needed to efficiently test nonlinear behavior.

The High-dimensional Empirical Linear Prediction (HELP) testing approach developed at NIST has generated considerable industry interest since it provides fewer test points needed to predict global behavior. Recent investigations into the use of artificial neural networks have shown promise of achieving efficient models for handling nonlinear dependencies. Of particular interest is the employment of nonlinear principle component neural networks, which reduce the data dimensionality relative to linear modeling for nonlinear devices.

MILESTONE: By 2001, develop a neural network-based approach that can realize a significant improvement to the present HELP testing strategy for modeling the behavior of instruments.

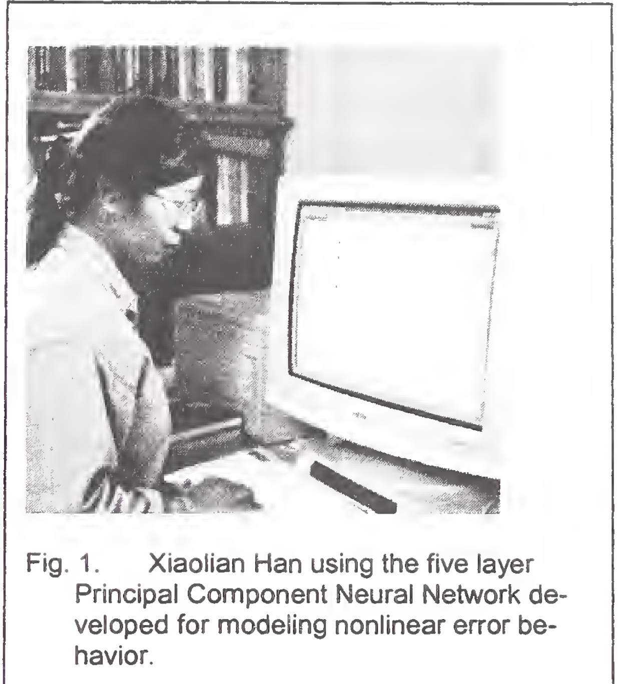


Fig. 1. Xiaolian Han using the five layer Principal Component Neural Network developed for modeling nonlinear error behavior.

MILESTONE: By 2001, implement online dissemenation of the HELP Toolbox and documentation via the Internet.

Incomplete data sets cannot be used in conventional empirical model building. For example, when new test points are added to the requirements for test coverage, this means that the older data sets cannot be used to build new models that predict these new test points. But with the use of a statistical prediction method, expectation maximization, this old data can be used along with new data sets. The incorporation of both old and new data sets using expectation maximization provides data points with more accurate predictions.

MILESTONE: By 2002, add the capability to include incomplete data sets into the HELP Toolbox.

The ability to make engineering changes quickly in the design of a complex electronic product is

necessary to meet the demands of the marketplace. To achieve these changes by simply modifying the embedded software used in the product is very cost effective. However, such changes are likely to change the model that has been developed to predict the performance of the product and, thus, its testing strategy.

MILESTONE: By 2003, develop the means for an adaptive modeling approach that can be incorporated into the present HELP testing strategy, which can be applied to changes in product design.
Correlated noise, such as 1/f noise, can enter the modeling process in the form of drift in the instrumentation making measurements used for the modeling set. This noise has a characteristic structure. The data sets used at NIST to model an instrument's error behavior have been analyzed to show a significant amount of 1/f noise. Since 1/f noise in measured data can substantially affect the empirical error models built from that data, and since 1/f noise is ubiquitous, this is a potentially serious problem in time-variant behavior in general. The fact that we are able to glean this information from an instrument's calibration data indicates there may be ways to reduce this error source.

MILESTONE: By 2004, develop methods for determining the amount of 1/f noise in a modeling data set, the effect this noise has on the confidence intervals predicted using this model, and methods for reducing these errors.

Accomplishments:

- A Workshop on Software-Embedded Systems Testing (WSEST) was held at NIST-Gaithersburg on November 8-9, 1999. Sixteen attendees represented government (6), academia (7), and industry (3), where the focus was on problems in testing mixed-signal systems with embedded software. Topics included metrology support for built-in-test, controlling test complexity, maintaining accurate models, and software validation. The subjects covered a wide range of disciplines, including metrology, software, hardware, mathematical algorithms, and instrument manufacturing. A concluding panel discussion was held on research needs in the testing of software-embedded systems.

- Further research was pursued on modeling nonlinear behavior in error data. A Neural Network Toolbox was used in conjunction with Constructive Neural Network software to build models of simulated nonlinear data. The limitations of this approach were explored in terms of speed of convergence, noise immunity, and level of complexity. In modeling a five-parameter bandpass filter, for example, it was found that a five-fold improvement in the mean squared error was obtained using a neural network nonlinear modeling approach vs a linear model when the parameter values change by 20 %. A paper on this research was presented at the Instrumentation and Measurement Technology Conference (IMTC) 2000.

- The algorithm for minimizing cumulative time-base quantization errors was presented at the WSEST and documented in a paper given at the IMTC 2000. It describes the errors expected as a function of the number of samples taken, the number of signal cycles sampled, and the number of bits for the reference digital-to-analog converter used in the time-base. However, further study of nonrandom amplitude errors in sampling systems did not lead to a generic approach to correcting such sources of error as was hoped.

- A comparative analysis was begun of the data from a manually operated, multi-range thermal transfer instrument with that from an automated version of the manual one, using a linear empiricalIn conjunction with the NIST-developed HELP (High-dimensional Empirical

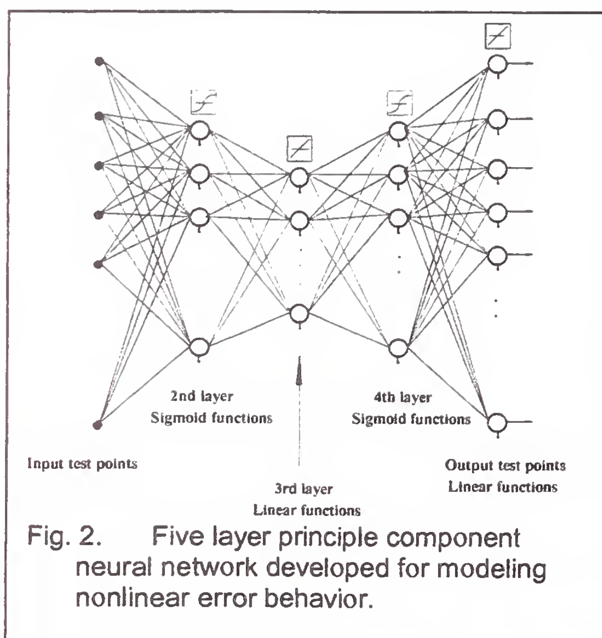


Fig. 2. Five layer principle component neural network developed for modeling nonlinear error behavior.

Linear Prediction) Toolbox. The results thus far indicate that error structure of the automated version exhibits fewer degrees of freedom, i.e., less complexity than its manual counterpart, contrary to what was expected. Model prediction variance as a function of model size and number of test points selected has also been investigated.

Collaborations:

Collaborative work with Prof. Gene Hwang of Cornell University continues, with a grant from the Information Technology Laboratory (ITL) at NIST, on missing data analysis using an expectation maximization approach. This work also involves Hung-kung Liu in the ITL.

Prof. Fernando Von Zuben of the State University of Campinas, Brazil spent a week at NIST helping the project members understand neural networks and how they can be incorporated into the NIST HELP Toolbox. Prof. Von Zuben consults with the project periodically.

Standards Committee Participation

IEEE Computer Society standards committees on P1149 Standard Testability Bus, WG.04 Mixed Signal Test Bus, and P1500 Standard Testability Method for Embedded Core-based ICs: G. N. Stenbakken is a member of these various standards committees.

Publications:

G. N. Stenbakken, D. Liu, J. A. Starzyk, and B. C. Waltrip, "Nonrandom Quantization Errors in Timebases," Proc. of 17th Instrumentation and Measurement Technology Conference (IMTC/2000), 1, May 1-4, 2000, Baltimore, MD, pp. 235-240 (May 2000).

X. Han, G. N. Stenbakken, F. J. Von Zuben, H. Engler, "Application of Neural Networks in the Development of Nonlinear Error Modeling and Test Point Prediction," Proc. of 17th Instrumentation and Measurement Technology Conference (IMTC/2000), 2, May 1-4, 2000, Baltimore, MD, pp. 641-646 (May 2000).

G. Stenbakken, A. D. Koffman, and T. M. Souders, "Software to Optimize the Testing of Mixed-Signal Devices," Proc. 5th IEEE Intl. Mixed Signal Testing Workshop, Jun 15-18, 1999, Whistler, British Columbia, Canada, spons. IEEE/TTTC, 1474 Freeman Dr., Amissville, VA, pp. 29-33 (Jun 1999).

H. Manufacturing Support

Certain disciplines such as statistical process control are generic to all aspects of manufacturing. These disciplines are equally applicable to the manufacture of the materials and the manufacturing equipment as well as the manufacturing of the integrated circuits, their packaging and testing. NIST has one project jointly with ISMT in this category, the creation of an engineering statistical handbook on the internet.

NIST/SEMATECH Engineering Statistics Internet Handbook

Technical Contacts:

***M.C. Croarkin**, W.F. Guthrie, and A. Heckert*

"I am thoroughly enjoying your Engineering Statistics Handbook. Thanks so much for adding real value to the information available on the Internet!!!" Paul Zaremba, Systems Engineer, Agilent Technologies, email message received December 19, 2000 at handbook@nist.gov, an archived mailing list for feedback on the NIST/ISMT Engineering Statistics Internet Handbook

Objective:

The goal of the NIST/SEMATECH Engineering Statistics Internet Handbook project is to produce an online resource to help scientists and engineers incorporate statistical methods into their work more efficiently. An online publication and a practical, example-driven format were chosen to make the Handbook readily accessible to its target audiences in industry, including the semiconductor manufacturing industry in particular.

Customer Needs:

Semiconductor manufacturing requires extraordinary discipline in process control. For example, a typical integrated circuit manufacturing process involves several hundred steps. These steps may include as many as thirty lithographic levels, which require extremely precise alignment with respect to one another. Tight process control is essential to produce a functional circuit. ISMT has recognized the importance of statistical process control in semiconductor manufacturing and has developed and maintained expertise in this field since its inception in 1988. Two of the more difficult issues impeding routine implementation of these techniques, however, include educating the users and making the tools easy to use.

Technical Strategy:

NIST and ISMT formed a collaboration under the umbrella Cooperative Research and Development Agreement (CRADA), combining the general expertise in engineering statistics at NIST with the semiconductor manufacturing expertise resident at SEMATECH.

Accomplishments:

Since the beta release of the Handbook last year, efforts have focused on responding to feedback

Fig. 1. NIST Engineering Statistics Internet Handbook team (left to right, Alan Heckert, Mark Reeder, Will Guthrie, and Carroll Croarkin) reviewing a page from the chapter on product reliability

from users, developing, implementing and testing additional case studies, chapter editing and addressing accessibility issues. User feedback has been very positive and constructive and has helped us prepare for the release of the final version the Handbook at this year's Quality and Productivity Research Conference in late May.

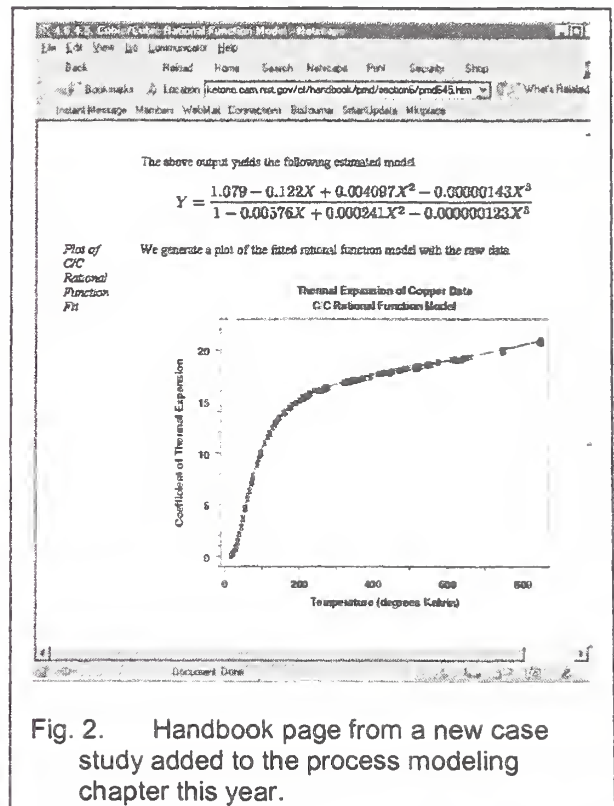


Fig. 2. Handbook page from a new case study added to the process modeling chapter this year.

Collaborations:

This project has been supported by funding or staff participation from ISMT, AMD, Motorola, the NIST Information Technology Laboratory, and the NIST Systems Integration for Manufacturing Applications (SIMA) program.

External Recognition:

Invited session at the 2001 Quality and Productivity Research Conference:
A Brief Tour of the NIST/ISMT Engineering Statistics Internet Handbook
"An Overview of the Handbook", William Guthrie, NIST

Incorporating Material from the ESI Handbook into Corporate Training", Barry Hembree, AMD

"Interfacing Statistical Software with the Handbook", Neil Polhemus, Statpoint, LLC

Publications:

Croarkin, M.C. and Tobias, P. eds.,
NIST/SEMATECH Engineering Statistics Internet Handbook,
http://www.nist.gov/stat.handbook/.

III. Appendix A

Project Title	Technical Contacts	Phone Number	Email
Metrology Supporting Deep Ultraviolet Lithography	J. Burnett M. Dowell R. Gupta T. R. Scott	(301) 975-2679 (303) 497-7455 (301) 975-2325 (303) 497-3651	john.burnett@nist.gov mdowell@boulder.nist.gov rejeev.gupta@nist.gov scott@boulder.nist.gov
Metrology Supporting Extreme Ultraviolet Lithography	T. Lucatorto A. Davies	(301) 975-3734 (301) 975-3743	thomas.lucatorto@nist.gov angela.davies@nist.gov
Lithographic Polymers	E. Lin C. Soles W. Wu	(301) 975-6743 (301) 975-8087 (301) 975-6839	eric.lin@nist.gov christopher.soles@nist.gov wen-li.wu@nist.gov
Atom-Based Dimensional Metrology	R. Silver	(301) 975-5609	richard.silver@nist.gov
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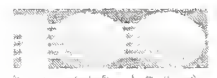
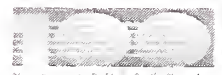


IV. Abbreviations and Acronyms

AC	alternating current
ADR	adiabatic demagnetization refrigerator
AEM	analytical electron microscopy
AES	Auger-electron spectroscopy
AFM	atomic force microscope
ALMWG	Analytical Laboratory Managers Working Group (ISMT)
AMAG	Advanced Metrology Advisory Group (ISMT)
ANSI	American National Standards Institute
ARXPS	angle resolved x-ray photoelectron spectroscopy
ASPE	American Society of Professional Engineers
ATP	Advanced Technology Program (NIST)
BCB	benzocyclobutene
BESOI	bond and etch-back silicon-on-insulator
BGA	ball-grid array
BIPM	Bureau International des Poids et Mésures
BIST	built-in self-test
BST	barium strontium titanate
C-AFM	calibrated atomic force microscope (NIST)
C-V	capacitance-voltage
CAD	computer-aided design
CCD	charge-coupled device
CD	critical dimension
CMOS	complementary metal oxide semiconductor
CMP	chem-mechanical polishing
CRADA	Cooperative Research and Development Agreement
CRDS	cavity ring-down spectroscopy
CSP	chip-scale package
CTCMS	Center for Theoretical and Computational Materials Science (NIST)
CVD	chemical vapor deposition
DC	direct current
DFT	design-for-test
DMA	differential mobility analyzer
DRAM	dynamic random-access memory
DSP	digital signal processing
DUV	deep ultraviolet
EBSD	electron backscatter diffraction
EELS	electron energy loss spectroscopy
EDC	embedded decoupling capacitance
EDS	energy-dispersive spectroscopy
EMC	electromagnetic compatibility
EMI	electromagnetic interference
EPMA	electron probe microanalysis
EUV	extreme ultraviolet
FIFEM	field ion field emission microscope
FIM	field ion microscope
FWHM	full-width half-maximum
GIXR/SE	grazing incidence x-ray reflection/spectrascopic ellipsometry
GIXPS	grazing incidence x-ray photoelectron spectroscopy
HRTEM	high resolution transmission electron microscope
HSQ	hydrogen silsesquoxane



I-V	current-voltage
IGBT	insulated-gate bipolar transistor
IPC	Association Connecting Electronics Industries
ISMT	International SEMATECH
ISO	International Organization for Standardization
ITRS	International Technology Roadmap for Semiconductors
LEED	low-energy electron diffraction
LER	line-edge roughness
LFPG	low frost-point generator
LOCOS	LOCal oxidation of silicon
LPP	laser-produced plasma
LPRT	light-pipe radiation thermometer
MBE	molecular beam epitaxy
MEMS	micro-electro-mechanical systems
MFC	mass flow controller
MMIC	millimeter and microwave integrated circuits
MOS	metal-oxide-semiconductor
MOSFET	metal-oxide-semiconductor field-effect transistor
MUX	multiplex
NCMS	National Center for Manufacturing Sciences
NDP	neutron depth profiling
NGL	next generation lithography
NEMI	National Electronics Manufacturing Initiative
NIST	National Institute of Standards and Technology
NLO	non-linear optical
NSOM	nearfield scanning optical microscopy
OMAG	Overlay Metrology Advisory Group (ISMT)
PED	Precision Engineering Division (NIST)
PLIF	planar laser-induced fluorescence
PMI	phase-measuring interferometer
PTB	Physikalisch-Technische Bundesanstalt
PZT	lead zirconium titanate
QM	quantum mechanics
RAM	Random-access memory
RGA	residual gas analyzer
RTA	rapid thermal annealing
RTP	rapid thermal processing
SANS	small-angle neutron scattering
SBIR	Small Business Innovative Research
SCM	scanning capacitance microscope
SEM	scanning electron microscope
SHG	second harmonic generation
SIA	Semiconductor Industry Association
SIMOX	separation by implantation of oxygen
SIMS	secondary-ion mass spectrometry
SoC	system-on-chip
SOI	silicon on insulator
SPM	scanning probe microscope
SRC	Semiconductor Research Corporation
SRM®	Standard Reference Material
SSHG	surface second-harmonic generation
SSIS	surface-scanning inspection system
SURF III	Synchrotron Ultraviolet Radiation Facility III

TCAD	technology computer-aided design
TDDB	time-dependent dielectric breakdown
TDR	time-domain reflectometry
TEM	transmission electron microscope
TFTC	thin-film thermocouple
TOF	time-of-flight
TMAH	tetramethyl ammonium hydroxide
UHV	ultra-high vacuum
UV	ultraviolet
WMS	wavelength modulation spectroscopy
VUV	vacuum ultraviolet
XPS	x-ray photoelectron spectroscopy