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Technology Administration

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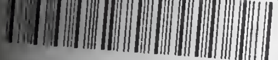
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NIST PUBLICATIONS

Electronics and Electrical Engineering Laboratory

Semiconductor Electronics Division

Programs, Activities, and Accomplishments

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The Electronics and Electrical Engineering Laboratory

Through its technical laboratory research programs, the Electronics and Electrical Engineering Laboratory (EEEL) supports the U.S. electronics industry, its suppliers, and its customers by providing measurement technology needed to maintain and improve their competitive position. EEEL also provides support to the federal government as needed to improve efficiency in technical operations, and cooperates with academia in the development and use of measurement methods and scientific data.

EEEL consists of five programmatic divisions, two matrix-managed offices, and a special unit concerned with magnetic metrology:

- Electricity Division
- Semiconductor Electronics Division
- Radio Frequency Technology Division
- Electromagnetic Technology Division
- Optoelectronics Division
- Office of Microelectronic Programs
- Office of Law Enforcement Standards
- Magnetics Group

This document describes the technical programs of the Semiconductor Electronics Division. Similar documents describing the other Divisions and Offices are available. Contact NIST/EEEL, 100 Bureau Drive, MS 8100, Gaithersburg, MD 20899-8100, Telephone: (301) 975-2220, On the Web: www.eeel.nist.gov

Cover Caption: (front to back) effective isotropic radiated MEMS-based microwave power sensor, 1.7 mm^2 wire-bonded chip in a ceramic pin grid array (PGA) package, test wafer from SEMATECH (provided by Gennadi Bersuker), and a close-up of copper circuitry for IBM's CMOS 7S chip, the first to exploit copper circuitry.

Electronics and Electrical Engineering Laboratory

Semiconductor Electronics Division

Programs, Activities, and Accomplishments

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January 2001

U.S. DEPARTMENT OF COMMERCE
Norman Y. Mineta, Secretary

Technology Administration
Dr. Cheryl L. Shavers, Under Secretary of Commerce for Technology

National Institute of Standards and Technology
Karen H. Brown, Acting Director

Contents

Welcome iv

Mission, Vision, Values, and Goals vi

Semiconductors: Backbone of the Electronic/Digital Revolution vii

Semiconductor Electronics Division Organization ix

Metrology for Compound Semiconductor Manufacturing... 1

Scanning-Probe Microscope Metrology.. 5

Thin-Film Process Metrology 9

Metrology for Simulation and Computer-Aided Design (includes Power Electronics) 13

MicroElectroMechanical Systems (MEMS) 18

Linewidth and Overlay Standards for Nanometer Metrology 22

Dielectric and Interconnect Reliability Metrology..26

Major Facilities / Laboratories...30

Microfabrication Process Facility 31

National Research Council (NRC) Postdoctoral Opportunities...33

Semiconductor Characterization Conference at NIST Draws World's Metrology Experts........38

Science Magazine Recommends Division Hall Effect Web Site As "Hot Pick" 39

Major Division Staff Awards...40

NIST's Gaithersburg Campus and Surrounding Area 44

Welcome

David G. Seiler, Division Chief

"The Semiconductor Roadmap is a blueprint for technology development required to maintain the productivity of the semiconductor industry. It does this by targeting research for leading edge technology."

Karen Brown, Deputy Director of NIST, Characterization and Metrology for ULSI Technology, AIP Press, 1998

The Semiconductor Electronics Division (SED) provides leadership in developing the semiconductor measurement infrastructure essential to improving U.S. economic competitiveness. It provides necessary measurements, physical standards, and supporting data and technology; associated generic technology; and fundamental research results to industry, government, and academia. The primary mission of the Division is to provide the measurement infrastructure to U.S. industry for mainstream silicon CMOS (complementary metal-oxide semiconductor) technology. The Division's programs also respond to industry measurement needs related to compound semiconductors, power electronics, and MicroElectroMechanical Systems (MEMS).

The Division has extensive interactions with individual companies, industry organizations, and professional groups; these activities enable the development of a research agenda responsive to the needs of industry. Active participation in industry roadmapping, such as the Semiconductor Industry Association's International Technology Roadmap for Semiconductors, and standards activities, such as committee work for the American Society for Testing and Materials, also is practiced extensively by the Division to prioritize and establish programs with the highest potential impact.

The Division, with a staff of about 50, is based in Gaithersburg, Maryland. The Division is one of five divisions within the Electronics and Electrical Engineering Laboratory at NIST. The Division's technical activities are organized into three Groups: the Materials Technology Group, the Device Technology Group, and the IC Technology Group. The Division affects industry by providing tools such as standard reference materials (SRMs), test chips, standard reference data, and software that support the needed measurement infrastructure. Division personnel visit industrial sites, host a variety of visitors, and make available tutorial material on an as-needed basis. We also are active in conference and workshop activities that directly benefit the industry. The Division receives and is responsive to hundreds of special requests for assistance from industry each year.

A broad array of activities that serve the semiconductor industry is currently underway in the Division. The staff of the SED addresses projects ranging from materials qualification to test structures for integrated circuits. Some of these projects are supported by the NIST National Semiconductor Metrology Program (NSMP), which is managed by the Electronics and Electrical Engineering Laboratory's Office of Microelectronic Programs. For more information on the NSMP, go to www.eeel.nist.gov/omp.

The Division widely disseminates the results of its research, especially in the areas of standardized test methods and SRMs, through a variety of channels - publications, software, conferences and workshops, and participation in standards organizations and consortia. NIST also actively seeks industrial, academic, and non-profit research partners to work collaboratively on projects of mutual benefit. We welcome new Ph.D. graduates to investigate our Division's National Research Council (NRC) Postdoctoral Opportunities (see page 33).

The technical programs, activities, and accomplishments described here for each Division Project clearly demonstrate the SED's leadership and effective service as it continues to respond to the needs of industry and to contribute to the scientific and engineering communities.

Thank you for your interest in our Division! I welcome your comments and suggestions. Feel free to e-mail me at david.seiler@nist.gov.

David G. Seiler

David G. Seiler

Semiconductor Electronics Division Staff

For additional information, contact

Division/Office Telephone: 301-975-2054
Division/Office Facsimile: 301-975-6021
On the Web: www.eeel.nist.gov/812/

Mission

"The nature of the vision's purpose is not only to achieve a meaningful strategic or company goal, but also to build a dedicated community"

Jay A. Conger, The Brave New World of Leadership Training, IEEE Eng. Mgmt. Review (1996)

The **Semiconductor Electronics Division** provides leadership in developing the semiconductor measurement infrastructure essential to improving U.S. economic competitiveness by providing necessary measurements, physical standards, and supporting data and technology; associated generic technology; and fundamental research results to industry, government, and academia. The primary focus is on mainstream silicon. The Division's programs also respond to industry measurement needs related to compound semiconductors, power electronics, and MicroElectroMechanical systems (MEMS).

Vision

The **Semiconductor Electronics Division** is recognized as a dynamic world-class resource for semiconductor measurements, data, models, and standards focused on enhancing U.S. technological competitiveness in the world market.

Values

The **Semiconductor Electronics Division** values its commitment to identify and to meet crucial measurement technology needs. The Division values its collaboration with all segments of the semiconductor community. It strives for integrity, excellence, objectivity, responsiveness, and creativity, while maximizing and utilizing the potential of its employees.

The Division mission, vision, values, and goals were developed by a strategic planning process facilitated by a professional consultant. This process involved extensive workforce involvement, the Division leadership, and numerous meetings and informal discussions.

Goals

The Division will:

- Aggressively pursue and achieve select metrology needs as identified in the International Technology Roadmap for Semiconductors for mainstream silicon.
- Develop new and improved process-monitoring tools, methodologies, and data for the more efficient manufacture of silicon and compound-semiconductor devices.
- Develop cooperative, multidisciplinary projects within the Division and synergistic external collaborative efforts to better meet the critical needs of the semiconductor industry.
- Support novel research that has high potential for providing break-throughs in materials, process, devices, and measurement technologies for the semiconductor industry.

Semiconductors: Backbone of the Electronic/Digital Revolution

"This year, the semiconductor industry will produce about 20 million transistors for every man, woman and child on earth. By 2008, we will be producing 1 billion transistors or more per person per year. Those transistors improve our lives in countless ways - they make cars safer and more fuel-efficient, they enable personal communication devices, they promote medical breakthroughs, and they improve the quality of education. Chips have become the foundation upon which the world's progress is built. So even as we honor semiconductors as an invention, a prodigy of engineering prowess, we overlook this even greater miracle: that it is the culmination of forces stretching back a thousand generations into pre-history. That's what gives it its power in our imaginations; what makes it a kind of talisman, a magical object of almost supernatural powers. A tiny sliver of glass that brings the world into a vast conversation, heals the sick, sees to the edge of the universe, imagines worlds never seen. Even in our jaded age, the chip can still command awe."

- The Silicon Century, Semiconductor Industry Association (SIA) Annual Report and Directory 2000

"No other human invention is the equal of the semiconductor device - if only because no other invention has been adopted so quickly and pervasively as the integrated circuit. Since the invention of the planar process forty years ago, billions of transistors are now in use beneath, around and above the earth. The microprocessor is the defining invention of the electronic age, the inventor of inventions from the personal computer to the internet."

The Silicon Century, Semiconductor Industry Association (SIA) Annual Report and Directory 2000

Semiconductors, transistors, and their applications represent one of the greatest scientific and technological breakthroughs of the twentieth century. Consider their far reaching influence on our society in general and on our daily lives. Can you imagine life without them? Semiconductors are pervasive in the microelectronic components used in computers, entertainment equipment, automotive electronics, medical instrumentation, telecommunications, space technology, television, radio, cell phones, and a whole host of other information technologies. Today, you can even purchase a CDMA-based watch phone, which combines the functions of a digital watch with that of a wireless communications handset. Every hospital, school, factory, car, airplane, office, bank, and household contains transistors, microprocessors, and other semiconductor devices.

These breakthroughs are possible because of the miniaturization of the transistor dimensions, which allow the construction of compact systems with tremendous computing power and memory. Miniaturization, in turn, is possible because of the perfection of fabrication techniques that allow the "integration" of circuits and thus the production of chips containing millions of elements per square centimeter. The foundation stone of this complex technology is silicon. Meeting the demands for these large-scale, complex, integrated circuits (ICs) continues to require technological advances in materials, processing, circuit design, characterization, testing, and standards.

The semiconductor electronics industry is outstripping the measurement capability needed for maintaining and improving U.S. international competitiveness. Important factors affected include product performance, price, quality, compatibility, and time to market. The Division provides three major classes of deliverables: measurement capability, technology development, and fundamental research. It provides the measurement capability needed to support the efforts of U.S. industry to improve its competitiveness. In order to support this effort, the Division also engages in technology development and fundamental research, and makes the findings available to industry.

The Division focuses the largest part of its resources on the development and delivery of measurement capability for two principal reasons: measurement capability has a very high impact on U.S. industry because measurement capability supports manufacturers in addressing so many of the challenges that they face in realizing competitive products in the marketplace, and NIST is the official lead U.S. Government agency for measurements.

The Division focuses on developing measurement capability that is beyond the reach of the broad range of individual companies. Companies seek NIST's help for several reasons:

- The companies need NIST's special technical capability for measurement development.
- The companies need NIST's acknowledged impartiality for diagnosing a measurement problem affecting the industry broadly or for achieving adoption of a solution across the industry.

- The companies cannot develop the measurement capability needed by the industry broadly because they cannot individually capture the returns of the cost of development.
- Industry's quality standards require that key measurements be traceable to the national measurement reference standards that NIST maintains. This is a requirement of growing importance in export markets.

"Sometime toward the end of 2000 or the beginning of 2001, sales to the communications sector will exceed those of the PC sector, marking the end of perhaps 20 years of domination of the PC sector dominating semiconductor chips... In the Internet Era, it's no longer microprocessors and memory that are the primary semiconductor components - it's DSP Digital Signal Processing plus analog"

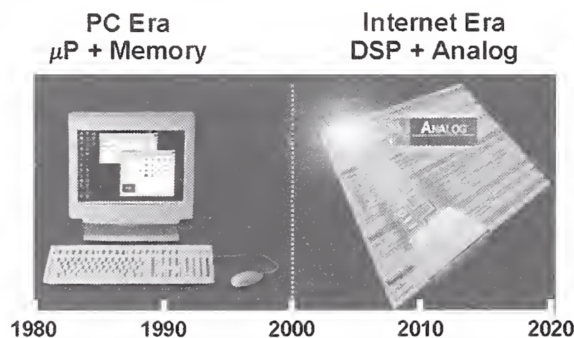
Dennis Buss, Vice-President of Mixed-Signal Technology, Texas Instruments, at the 2000 International Conference on Characterization and Metrology for ULSI Technology

The Division continues to interact/collaborate with a wide variety of companies, consortia [such as International Semiconductor Manufacturing Technology (SEMATECH), Semiconductor Equipment and Materials International (SEMI), and the Semiconductor Research Corporation (SRC)], academia, and other government labs to accomplish its mission. Specific details are given in the Project Sheets that follow. Work in the Division results in extensive outputs or deliverables that cover knowledge/improvements in physical understanding, test methods/measurements, Standard Reference Materials (SRMs), Standard Reference Data (SRD) sets, standards, test structures/test chips, software, measurement accuracy/traceability, publications/reports, patents/Cooperative Research and Development Agreements (CRADAs), round robins, data and models, talks/short courses, company visits, conferences/workshops, consortia participation, and various activities and leadership roles on committees and working groups.

Division staff serve the semiconductor community in leadership roles on standards committees such as American Society for Testing and Materials (ASTM) and Electronic Industries Alliance (EIA) / Joint Electron Device Engineering Council (JEDEC), societies such as IEEE and ECS, and on numerous semiconductor conferences/workshops. A large number of test methods and standards has been developed and written over the years by NIST staff for ASTM and EIA/JEDEC, including ones for resistivity, oxygen in silicon, thin dielectrics, electromigration, and device characterization. Staff serve on various Technical Working Groups to help put together the 1999 International Technology Roadmap for Semiconductors (ITRS). These Groups are Process Integration, Devices, and Structures; Assembly and Packaging; Lithography; Interconnect; and Front End Processes. The ITRS provides targets for equipment, material, and software suppliers; provides targets for researchers; and serves as a common reference for the semiconductor industry.

The Division has also impacted the semiconductor community by producing a number of SRMs. To date, over 2,500 SRMs have been sold and distributed for resistivity, oxygen in silicon, and optical thickness by ellipsometry. Hundreds of companies throughout the world have purchased these SRMs to maintain and improve their measurement capability.

According to Dennis Buss, Vice-President of Mixed-Signal Technology, Texas Instruments, the semiconductor industry is moving from an era dominated by PC sales to one heavily dominated by communications. As the industry progresses along this new avenue, the leadership in measurement infrastructure that this Division provides continues to be important.



The Internet Era. (Used with permission from Dennis Buss' talk "Technology in the Internet Era," presented at the 2000 International Conference on Characterization and Metrology for ULSI Technology.)

Semiconductor Electronics Division Organization

Division Office (812.00)

2054 SEILER, David G., Chief
2068 BLACKBURN, David L., Deputy
2054 PRINTZ, Lori A., Secretary
2230 COOK, Sharon W., AO
5633 MURPHY, Joan, Assistant AO (PT)
2079 BENNETT, Herbert S., NIST Fellow
2097 HARMAN, George G., NIST Fellow
2242 BUCK, Laurence M.
2081 ROACH, Ramona
2050 SECULA, Erik M.
2054 OETTINGER, Frank F. (GR)

Materials Technology Group (812.01)

8009 SHAFFNER, Thomas J. (GL)
2053 HUFF, Barbara, Secretary

Metrology for Compound Semiconductor Manufacturing

2123 PELLEGRINO, Joseph G. (PL)
2082 SMIRL, Arthur, L. (GR)
2067 THURBER, W. Robert
5291 TSENG, Wen F.

Scanning-Probe Microscope Metrology

2089 KOPANSKI, Joseph J. (PL)
3466 HANDY, Brenda (S)
2088 MARCHIANDO, Jay F.
2045 MAYO, Santos (GR)
5466 McBRIDE, Duncan (GR)
2108 RENNEX, Brian G. (PT)

Thin-Film Process Metrology

2060 EHRSTEIN, James R. (PL)
5974 AMIRTHARAJ, Paul M. (GR)
2248 BELZER, Barbara J.
2084 CHANDLER-HOROWITZ, Deane
2053 CHO, Yong J. (GR)
2044 NGUYEN, Nhan V.
2082 RICHTER, Curt A.
2065 RICKS, Donnie R.

Device Technology Group (812.03)

2071 HEFNER, Allen R., Jr. (GL)
2056 MAIN, Brenda L. (CTR)
2077 ROITMAN, Peter (detailed to TS)

Metrology for Simulation and Computer-Aided Design

2071 HEFNER, Allen R., Jr. (PL)
2075 ALBERS, John (detailed to ATP)
2079 BENNETT, Herbert S.
2069 BERNING, David W.
2068 BLACKBURN, David L.
6586 BOUCHE, Sebastian (GR)
8777 HODGE, Angela
4709 JOSHI, Yogendra K. (GR)
2056 KAMGAING, Telesphor (GR)

MicroElectroMechanical Systems

2070 GAITAN, Michael (PL)
5484 GEIST, Jon (GR)
2049 MARSHALL, Janet C. (PT)
2052 ZAGHLOUL, Mona E. (FH)
2073 ZINCKE, Christian A. (GR)

Microfabrication Process Facility

2699 HAJDAJ, Russell (FM)
2095 KREPPS, Guilford J. (CTR)

Assembly and Packaging

2097 HARMAN, George G.

IC Technology Group (812.04)

2052 LINHOLM, Loren W. (GL)
2052 WILKES, Jane M., Secretary
2236 ELLENWOOD, Colleen E.
8193 MURABITO, Christine E. (S)

Linewidth and Overlay Standards for Nanometer Metrology

2072 CRESSWELL, Michael W. (PL)
5026 ALLEN, Richard A.
4446 GHOSHTAGORE, Rho (GR)
2182 GUILLAUME, Nadine (GR)
5623 OWEN, James C.

Dielectric and Interconnect Reliability Metrology

2247 SUEHLE, John S. (PL)
5420 AFRIDI, Muhammad Y. (GR)
2078 EDELSTEIN, Monica D.
5466 HEAD, Linda (GR)
2234 SCHAFFT, Harry A. (GR)
4723 VOGEL, Eric
2111 WANG, Bin (GR)

Legend:

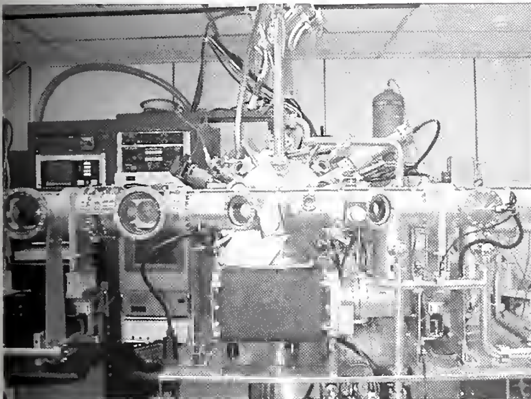
AO = Administrative Officer
CTR = Contractor
FH = Faculty Hire
FM = Facility Manager
GL = Group Leader
GR = Guest Researcher
PL = Project Leader
PT = Part Time
S = Student
ATP = Advanced Technology Program
TS = Technology Services

Telphone numbers are: (301) 975-XXXX, (the four digit extension as indicated)

Metrology for Compound Semiconductor Manufacturing

Project Goals

Provide technological leadership to semiconductor and equipment manufacturers by developing and evaluating the methods, tools, and artifacts needed to improve the state-of-the-art in compound-semiconductor growth and nanometrology (measurements on a scale of 1 nm to 100 nm). Provide measurements of growth and structural parameters in addition to fabrication properties required for the reliable manufacture of nanostructure devices. Develop research materials and methods to improve measurement standards. Provide reference methods and reference materials to assist the U.S. III-V manufacturing community.



The molecular beam epitaxy machine is used for growing and utilizing high-quality epitaxial films of III-V compound semiconductors and for developing in-situ metrology to control their growth properties.

Customer Needs

The GaAs and III-V compound semiconductor manufacturing community has experienced tremendous growth in the last several years. A large part of this growth has been due to the wireless and cellular phone market. These growth opportunities are also coupled with new technological challenges for the GaAs manufacturing industry. This growth has resulted in new demand for equipment manufacturers. End users of III-V material now require epilayer heterostructures with compositional tolerances less than one percent and for some devices, thickness tolerances at the atomic monolayer level. In-situ probe equipment vendors look to NIST for cross-correlation of their probes with complementary measurements. Increasingly, epilayer foundries are looking to real-time process monitors to reduce costs and improve manufacturing efficiency. In-situ metrology has emerged as a key enabling technology to improve real-time monitoring and control. With new and improved real-time probes, manufacturers look forward to reduced losses from material that is not within spec. As the cost and complexity of epilayers increases, the epilayer growers and end users need to be able to reliably and reproducibly generate epilayers with thickness control at the atomic level as well as temperature control to within 1 °C! Controlling thickness, temperature, and composition are among the greatest challenges that currently confront manufacturers. In-situ growth control offers the tools for advancing epilayer deposition technology.

Technical Strategy

There are several technical thrusts within the Project. A major focus involves the deployment of in-situ techniques to advance real-time control of the III-V deposition process, based on an array of optical, electron, and X-ray probes. These probes are used to determine layer thickness, composition, and temperature in real time. This includes a one-of-a-kind in-situ, X-ray emission probe capable of detecting the surface epilayer composition in real time, even while the substrate rotates. An in-situ diffuse reflectance probe makes use of the substrate's absorption edge to monitor surface temperature to within 1 °C while the sample rotates. This probe can be used passively or in an active feedback mode to both control and monitor surface temperature during growth. Other in-situ probes include spectroscopic ellipsometry for composition, thickness, and temperature monitoring during the deposition process as well as Reflection High Energy Electron Diffraction (RHEED) and desorption spectroscopy.

One of the Project's on-going efforts is to correlate the material parameters measured during the growth of III-V heterostructures with the electrical properties of devices fabricated from this same material. The psuedomorphic high electron mobility transistor (pHEMT) is one device we are addressing within the Project. Working with GaAs manufacturers, e.g., IQE, Raytheon, and OSEMI, we are able to provide advice on the efficiency of a specific probe as a

Technical Contact:
Joseph G. Pellegrino

Staff-Years:
3.5 professionals
1.0 technician
1.0 guest researcher

Funding Sources:
NIST (100%)

Parent Program:
Semiconductors, Compound

"We have learned that real-time process control by in-situ monitoring is essential for fabricating high quality, epitaxial layers on compound semiconductor wafers at low cost and high yields."

Harvey Serreze, Director of R&D, Spire Corporation, June 8, 1999

real-time monitor on our in-situ MBE growth chamber. Companies use our in-situ facility as a testbed for new probes as well as a resource for additional in-situ information to compare with their own measurements. In this way, the Project provides a valuable service to sensor manufacturers. By providing dielectric optical parameters to ellipsometer manufacturers and pHEMT transport properties to discrete IC manufacturers, we help the III-V manufacturers to more efficiently control the epilayer growth process in order to meet new technology challenges. Project goals also include efforts to build measurement consensus among major GaAs manufacturers.

Project staff work to provide the III-V community with benchmarks for artifacts and procedures. A recent example is the collaboration with IQE, in which NIST measured the surface roughness of epilayers for comparison with company measurements. These efforts also include an electronic Web site for Hall measurements, which is described in more detail on page 39.

SED is working with Raytheon to assess whether an in-situ diffuse reflectance probe can be employed to make a better state-of-the-art pHEMT.

MILESTONE: By 2001, correlate the use of in-situ diffuse reflectance versus conventional thermocouple control to fabricate psuedomorphic high electron mobility transistors. Collaborate with a commerical manufacturer to obtain device characteristics.

Project staff have also initiated an international Hall round robin among major GaAs manufacturers in order to assess and ultimately establish measurement consensus related to mobility and sheet carrier concentrations.

MILESTONE: By 2001, produce a compilation of the industrial Hall round robin results for public dissemination.

Project activities include a collaboration with other NIST Divisions (Optoelectronics, Ceramics, Surface and Microanalysis Science) to develop III-V compositional standards. This is part of an intramural program sponsored by NIST's Advanced Technology Program (ATP).

Project staff are working with the Manufacturing Engineering Laboratory (MEL) to develop an artifact transferal system that allows transport of an MBE wafer in a UHV environment to MEL's STM facility for surface characterization. This work is part of the National Manufacturing Testbed (NAMT) program within MEL. Collaboration with MEL includes work on a GaAs-based linewidth artifact for use by semiconductor equipment manufacturers. The artifact will be used for pitch as well as linewidth measurements.

The Project received competence funding to explore the metrology and properties of a new class of semiconductor materials called Photonic Crystals. The competence program includes the Optoelectronics Division and the Electromagnetic Technology Division. Project goals are to use MBE growth, in-situ monitoring and control, as well as post-growth processing to explore the metrology of photonic crystals and molecules. Applications for this new class of material include photon-generator turnstiles and wave-guides. Focused ion beam technology and wet chemistry facilities within the Division are used by Project staff for processing.

MILESTONE: By 2002, fabricate and characterize a photonic molecule which operates in electro-luminescence mode.

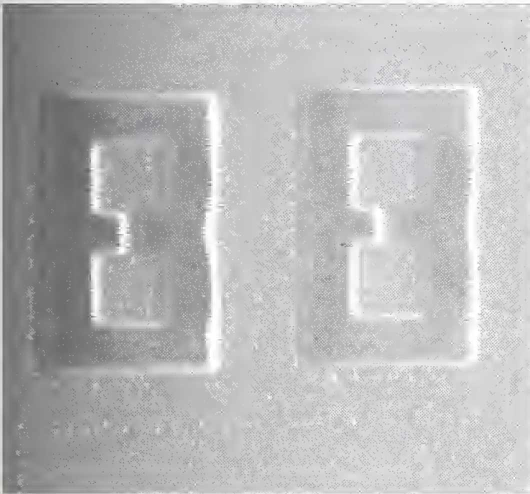
Accomplishments

- Demonstrated a new normalization scheme for obtaining quantitative composition measurements using an in-situ X-ray emission probe. This probe has reduced the discrepancy between in-situ RHEED and XRF from 15% to 6%. A showstopper for any quantitative electron beam microprobe analysis is the need for reliable standards. What's more, the spectra for these standards need to be obtained under the same conditions as the unknown. Making this happen in an ultra-high vacuum environment adds a layer of difficulty. The new normalization technique involves benchmarking the standards relative to the unknown by making use of the signal from the molybdenum sample holder. By adjusting the electron beam to obtain identical k-ratios for the standards and unknown, conditions are well established for quantitative analysis. Work is ongoing to improve k-ratio consistency through focusing and electron beam control. This probe represents the first time this approach has been used in MBE growth of semiconductors.

- Implemented the second phase of the Hall round robin. Began distribution of samples to domestic and international companies for measurements. Samples were laser marked and first measured at NIST before distribution. The

round robin involves 11 companies (domestic and foreign): AXT, QED, Airtron, Picogiga, Aixtron, Ovation, Emcore, M/A-COM, Epitronics, Hitachi Cable, and Freiburger.

- Calculated the uncertainty associated with the RHEED measurements (X_1 and X_2) for the AlGaAs compositional standards project. Demonstrated, for the first time, that the uncertainty associated with X_1 was an order of magnitude larger than the X_2 value. These results suggest that controlling the composition within specification using the RHEED technique is better accomplished using the X_2 value. X_2 is calculated from the slower growth rates of AlAs and GaAs whereas X_1 depends on the AlGaAs and GaAs growth oscillations. A Fast Fourier Transform algorithm is typically used to convert the oscillatory data into growth rates and the effects of FFT truncations errors are more pronounced for the faster growth rates. Osemi Inc., a III-V foundry, is incorporating these results in order to better target composition for applications of resonant cavity LEDs.



VCSEL structure processed by in-house focused ion beam facility.

- Established an extensive Web site at www.eeel.nist.gov/812/itrcs.html to disseminate information about compound semiconductors and to gather comments from industry concerning the proposed International Technology Roadmap for Compound Semiconductors.

- Measured the dielectric parameters (Del and Psi) of low temperature GaAs (LT GaAs) using in-situ spectroscopic ellipsometry. LT GaAs is important for circuit manufacturers because LT GaAs has excess arsenic defects that result in a high resistivity substrate useful for preventing side gating and back gating latch-up problems. A unique feature of this effort is that Diffuse Reflectance Spectroscopy was employed to measure wafer surface temperature during growth with an accuracy of ±1 °C. A series of LT GaAs wafers were fabricated between 180 °C - 260 °C and measured during, as well as after, growth. In addition to disseminating the information publicly, the ellipsometer manufacturer (J.A. Woollam) incorporated the dielectric data into their database. This database becomes part of every new ellipsometer that is sold. The low temperature growth was facilitated by use of SED's unique configuration of the Diffuse Reflectance in-situ probe that was used to accurately control the wafer temperature at low growth temperatures. Such control is not possible with conventional pyrometry.

- Grew a series of InGaAs vertical cavity surface emitting lasers (VCSELs) that were processed with a photonic molecule geometry. The etching of the photonic molecule was done using a hybrid approach; first, the samples were etched with GaAs specific and AlAs specific etches in order to digitally remove the upper mirror. The focused ion beam was used for final lithographic trimming. We have demonstrated design, growth, fabrication, and characterization of the VCSEL structure into photonic molecules. The next phase of the work will involve advanced optical characterization of how light is emitted in the coupled cavities of the photonic molecules.

- Demonstrated that the vacuum suitcase could be used to transport samples grown in the MBE at a pressure of 10^{-9} millitorr. These samples were then inserted into a UHV STM apparatus at MEL as part of a collaborative effort of the NAMT program.

- Analyzed the RHEED surface reconstructions on GaAs (001) as a function of temperature and As-2 (arsenic dimer) pressure. Characterized the effective adsorption ratio of As-2 and Ga as functions of temperature and As-2 pressure. This data will permit calibration of the ion gauge beam equivalent pressures, which are not currently quantitative.

"If the compound semiconductor industry is to achieve low cost and high performance in submicron devices, there needs to be established various in-situ control schemes to ensure high yield to very tight specifications on layer thickness, doping concentration and profiles, and layer composition."

Dan Rode, President, Pendragon Corporation, March 1, 1998

FY Deliverables

Collaborations

Divisions 815 and 814, Photonic Molecules, Lattices, and Turnstiles, competence project (Joseph G. Pellegrino and Thomas J. Shaffner)

NIST - Div 855, develop ohmic contact system on gallium nitride (GaN) and investigate its ohmicity, entire fiscal year (Wen F. Tseng)

Raytheon, assess impact of temperature measurements on product yield and strengthen pHEMT processing lab (Joseph G. Pellegrino)

Pendragon Corporation, compound semiconductor roadmapping and Hall round robin, continuing (Thomas J. Shaffner)

Wright Patterson Air Force Base Sensors Directorate, compound semiconductor fabrication, began in June 2000 and continuing (Thomas J. Shaffner and Joseph G. Pellegrino)

Standards Committee Participation

ASTM F1.15 and SEMI Compound Semiconductor, interacting with for Hall effect round robin, entire FY (Joseph G. Pellegrino and W. Robert Thurber)

Publications

Gajewski, D. A., Nguyen, N. V., Guyer, J. E., Kopanski, J. J., Richter, C. A., and Pellegrino, J. G., In Situ and Ex Situ Spectroscopic Ellipsometry of Low-Temperature-Grown GaAs, J. Electronic Materials, 29(7), 2000.

Guyer, J. E., Tseng, W. F., and Pellegrino, J. G., Diffuse Reflectance Spectroscopy for In Situ Process Monitoring and Control During Molecular Beam Epitaxy Growth of InGaAs / AlGaAs Pseudomorphic High Electron Mobility Transistors, JVST B 18(5), Sept/Oct, 2000, pp. 2518-2522.

Gajewski, D. A., Guyer, J. E., and Pellegrino, J. G., Real-time Measurements of the Psuedodielectric Function of Low-Temperature Grown GaAs, Appl. Phys. Lett., 77(4), 2000, pp. 540-542.

Kolbensen, B. O., Claeys, C., Stallhofer, P., Tardif, F., Benton, J., Shaffner, T., Schroder, D., Kishino, S., and Rai-Choudhury, P., Eds., Analytical and Diagnostic Techniques for Semiconductor Materials, Devices, and Processes, The Electrochemical Society, ECS PV 99-16, SPIE Volume 3895, 1999.

Pursch, M., Vanderhart, D. L., Sander, L. C., Gu, X., Nguyen, T., Wise, S. A., and Gajewski, D. A., C_{30} Self-Assembled Monolayers on Silica, Titania, and Zirconia: HPLC Performance, Atomic Force Microscopy, Ellipsometry, and NMR Studies of Molecular Dynamics and Uniformity of Coverage, Journal of the American Chemical Society, Vol. 122, No. 29, pp. 6997-7011.

Bennett, H. S., and Filliben, J. J., A Systematic Approach for Multidimensional, Closed-Form Analytic Modeling: Minority Electron Mobilities in GaAlAs Heterostructures, Journal of Research of the National Institute of Standards and Technology, Volume 105, Number 3, May - June 2000, pp. 441-452.

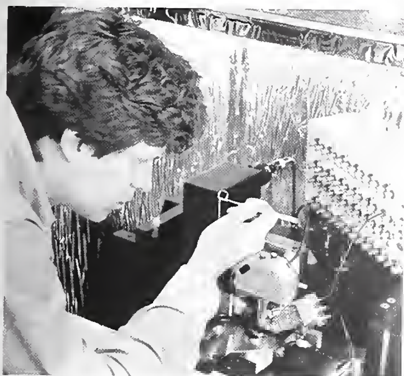
Bennett, H. S., Technology Roadmaps for Compound Semiconductors, Journal of Research of the National Institute of Standards and Technology, Volume 105, Number 3, May - June 2000, pp. 429-439.

Bennett, H. S., Technology Roadmaps for Compound Semiconductors, in the Proceedings of the International Conference on Compound Semiconductors Outlook 2000, Gorham Advanced Materials, Gorham Conferences, Gorham, Maine, USA, Feb 28 – March 1, 2000, San Francisco Airport Marriott, San Francisco, CA, pp. 35-69.

Scanning-Probe Microscope Metrology

Project Goals

Provide technological leadership to semiconductor and equipment manufacturers and other government agencies by developing and evaluating the methods, tools, and artifacts needed to apply scanning-probe microscopy and other electrical characterization methods to semiconductor materials and processes; provide silicon and compound semiconductor manufacturers with advanced scanning-probe electrical metrology techniques and models to improve device performance and reliability. A specific goal is to provide the technology computer-aided design (TCAD) community with quantitative two-dimensional dopant profiles to calibrate and enhance the predictivity of simulators.



Loading a sample into the scanning capacitance microscope.

Customer Needs

The Semiconductor Industry Association's (SIA) International Technology Roadmap for Semiconductors (ITRS) identifies two- and three-dimensional carrier profiling as a key enabling technology for the development of next-generation integrated circuits. In 2000, it is desired to know 2-D carrier profiles with spatial resolution of 5 nm and with a precision (in concentration) of ±5%; these demands increase to less than 1 nm and ±2% by 2015. Scanning Capacitance Microscopy (SCM) has emerged as the leading contender to provide 2-D carrier profiles.

While SCMs are commercially available, techniques to interpret accurately SCM images have lagged. Much work remains to be done to develop three-dimensional physical models of SCM and techniques to use these models to extract quantitative carrier profiles from SCM images of differential capacitance. Likewise, the measurement methodology for quantitative SCM is still evolving. The need for, and form of, standard reference materials for SCM have yet to be defined. Other scanning probe microscopy (SPM) based techniques for semiconductor metrology suffer similar problems – microscopes have been invented, but standard measurement and interpretation techniques are not available.

Technical Strategy

Currently, our primary goal is to develop the measurement methodology, physical models, and interpretation formalisms to make SCM a practical metrology for 2-D carrier profiling of silicon. Best measurement practices are being determined via collaborative projects with industrial users and research into the physics of the silicon surface preparation. The focus of our modeling effort has been to develop 2-D and 3-D finite-element solutions of Poisson's equation for the SCM geometry. Our expertise with interpreting SCM images is being transferred to industry through our software program *FASTC2D*. The program features an easy-to-use interface and a rapid profile extraction, and operates in a Windows environment.

The Project is also actively investigating other SPM based characterization techniques. We plan on extending the SCM carrier profiling capacity to SiC and III-V semiconductors. Intermittent-contact SCM is sensitive to variations in the dielectric constant of thin films and can detect metal layers buried beneath insulating films. Optically-pumped SCM is sensitive to variations in carrier lifetime. The scanning microwave microscope (SMWM) is of interest because it can provide both the real and imaginary parts of impedance at frequencies from dc to 50 GHz.

The version of *FASTC2D* currently available utilizes a database of pre-calculated solutions that can very rapidly determine a 2-D carrier profile from an SCM image. When used in conjunction with SIMS measurements or a reference sample, relatively accurate profiles can be obtained. Proper interpretation of carrier profiles of current interest to the semiconductor industry will require consideration of the local dopant gradient. We have estimated the magnitude of the dopant gradient effect through simulations.

SCM signals measured in the vicinity of a p-n junction are not readily explainable with a simple

Technical Contact:
Joseph J. Kopanski

Staff-Years:
3.3 professionals
3.0 guest researchers

Funding Sources:
NIST (100%)

Parent Program:
Semiconductors, Silicon

model. In conjunction with better theoretical understanding, we are developing new multiplexed measurement approaches to acquire the volume of data needed to interpret successfully SCM images of samples containing p-n junctions, on both sides of the junction.

MILESTONE: By 2001, develop second-generation code that can correct for the effect of the local dopant gradient and the presence of p-n junctions.

"Two-Dimensional dopant profiling has been a highly ranked need in both the process integration and TCAD (simulation) sections of the National Technology Roadmap for Semiconductors (NTRS) since its inception."

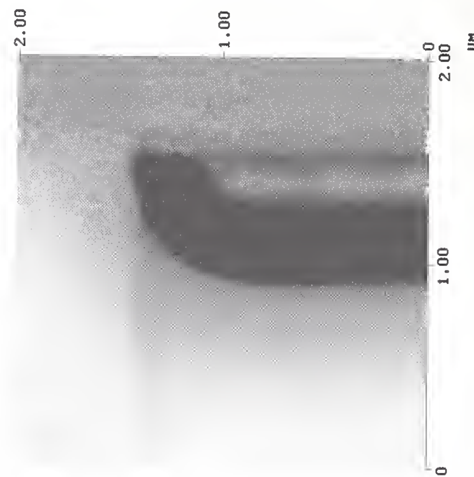
Michael Duane, Advanced Micro Devices, Characterization and Metrology for ULSI Technology, p. 715.

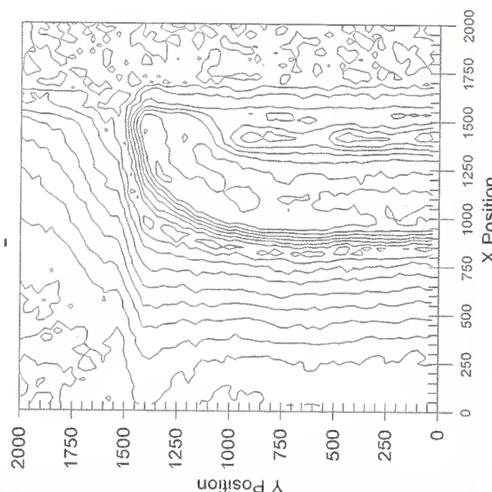
Meeting industrial needs for 2-D dopant profiling to the end of the ITRS requires a physically accurate 3-D model and determination of dopant profile by an inverse solution. An inverse solution of the SCM requires repeated solutions of the forward problem, i.e., calculation of the SCM signal from candidate carrier profiles. The candidate carrier profile is adjusted until a carrier profile is found that yields a calculated SCM signal that agrees with the measured SCM signal. Project staff have demonstrated techniques necessary to do this with a 2-D solver. We are developing improved 3-D Poisson solvers using the LaGriT grid management toolbox in collaboration with Los Alamos National Laboratories.

Successful model development depends on experimental validation. We plan on working with industrial collaborators to demonstrate 2-D dopant profiling of ultra-shallow junctions with continually improving spatial resolution and accuracy in carrier concentration. To improve the spatial resolution of SCM, we are working with collaborators on the use of ultra-sharp, co-axially shielded tips. To make SCM samples with better surface properties, we have an effort to investigate ozone enhanced low-temperature oxidation of silicon.

MILESTONE: By 2002, demonstrate 3-D calculations of the SCM signal across dopant gradients and junctions. Demonstrate inverse solutions of the SCM based on 2-D models.

The final level of refinement is to use the full 3-D model as the basis of inverse solutions of the SCM. However, the volume of data to be processed and the time required for calculation makes this intractable for routine profile extraction. Practical application requires finding shortcuts that will achieve the 3-D result without having to complete the entire round of 3-D simulations. Quantum mechanical effects for very thin insulating layers on SCM samples may also need to be included. This would require the solution of the coupled Poisson and Schrödinger Equations.





SCM image of a p+/n junction (above). Dopant contours extracted with FASTC2D (below).

MILESTONE: By 2003, develop a computationally efficient method of determining carrier profiles from inverse solutions of SCM based on 3-D models.

Accomplishments

- *FASTC2D* version 1 code completed. *FASTC2D* extracts 2-D carrier profiles from SCM images of dopant gradients in silicon. Beta copies of this code were distributed to 40 industrial users who are members of the SEMATECH working group on 2-D dopant profiling. The code can be obtained via the Internet at the Semiconductor Electronics Division's Web site. User feedback and comments have been incorporated in the code. A Users' Guide for *FASTC2D* in the form of a

Special Publication is planned for December 2000.

- Began collaboration with Los Alamos National Laboratories (LANL) to use their LaGriT (Los Alamos Gridding Toolkit) software package. LaGriT is a library of user callable tools that provide 3-D mesh generation, mesh optimization, and dynamic mesh maintenance for finite element methods. Access to such code will enable more efficient 3-D simulations of the SCM measurement across dopant gradients and p-n junctions. Dr. Jay Marchiando spent June, July, and August at LANL learning to use and applying LaGriT.

- Developed new vector nonlinear Poisson solver using LaGriT tools to manage the grid. This should provide a substantial improvement over our original 3-D solver. Testing on model SCM based problems will begin in fall 2000.

- Used established models to better understand and interpret SCM measurements. Began a theoretical/experimental study to better understand the double zero crossing in SCM signal sometimes observed at p-n junctions. Conducted simulations of SCM signal measured across p-n junctions for profiles intended to imitate double implanted junctions. Developed preliminary inverse solution of SCM.

- Completed an extensive set of SCM measurements on a set of six samples for the IMEC/SEMATECH round robin on measuring junction depth and channel length with SCM and other techniques.

- Completed an extensive review article on Scanning Capacitance Microscopy for The Encyclopedia of Imaging Science and Technology, to be published by John Wiley & Sons. Entries in the encyclopedia are intended to: "be recognized as the definitive work on the subject and of lasting value."

- Duncan McBride completed his Com-Sci Fellowship and produced a publication summarizing his studies of surfaces for SCM. Two processes, one thermal and one based on ozone, have been identified which produce oxides with thickness and electrical properties suitable for SCM. More importantly, we have identified ozone, rather than UV light, as the significant catalyst for growth of a high quality oxide for SCM. Dr. McBride will continue to contribute to further studies of oxide using high concentrations of ozone.

- Based on topics suggested by the Project, a phase II DoC SBIR grant has been made to Atolytics, Inc. in State College, PA, to develop a commercial version of their scanning microwave microscope, and a phase I SBIR has been made to Manufacturing Instrumentation Consultant Co. of Cleveland, OH, to develop co-axial shielded scanning probe microscope tips.

- Began collaboration with Howard University and others to apply SCM to high bandgap semiconductors. Brenda Handy, a senior at Howard University, worked at NIST for the summer of 2000 to learn to operate the scanning capacitance microscope and to begin preliminary studies of SCM applied to SiC.

FY Deliverables

Collaborations

Digital Instruments Inc, Andy Erickson, received upgrade to 2nd generation SCM head (Joseph J. Kopanski)

Dr. Srinivasan Anand, The Royal Institute of Technology, Stockholm, Sweden, FASTC2D feedback (Brian G. Rennex)

Howard University, Gary Harris, application of SCM to high bandgap semiconductors (Joseph J. Kopanski)

Lorenzo Ciampolini, Integrated Systems Laboratory, Swiss Federal Institute of Technology, FASTC2D feedback (Brian G. Rennex)

Los Alamos National Laboratory, Charles Snell with UT-MARLOWE Software (Jay F. Marchiando)

Los Alamos National Laboratory, Denise George, LaGrit software (Jay F. Marchiando)

Natasja Duhayon Imec - STDI/MCA, Belgium, FASTC2D feedback (Brian G. Rennex)

NIST, B. Belzer, gate oxide formation under mild conditions for scanning capacitance microscopy (Joseph J. Kopanski)

Texas Instruments Inc., Hal Edwards, comparison of measured and modeled SCM signal across p-n junctions (Joseph J. Kopanski)

Thermomicroscopes Inc., Ralph Nyfenegger, cooperative SCM measurements on prototype reference sample (Joseph J. Kopanski)

Software

FASTC2D beta-2 code distributed to 40 members of the SEMATECH Working Group on 2-Dimensional Carrier Profiling (Joseph J. Kopanski and Brian G. Rennex)

Incorporated user feedback on FASTC2D (Brian G. Rennex)

Revised FASTC2D to make the critical conversion coefficient calculations three times faster (Brian G. Rennex)

External Recognition

International Invited Talk: Scanning Capacitance Microscopy for Measuring Device Carrier Profiles Beyond the 100 nm Generation, 2000 International Microprocesses and Nanotechnology Conference (MNC 2000), The Univ. of Tokyo, JAPAN, July 11-13, 2000 (Joseph J. Kopanski)

Invited Encyclopedia Entry: Scanning Capacitance Microscopy, The Encyclopedia of Imaging Science and Technology, John Wiley & Sons, 2000 (Joseph J. Kopanski)

Publications

Gajewski, D. A., Nguyen, N. V., Guyer, J. E., Kopanski, J. J., Richter, C. A., and Pellegrino, J. G., In Situ and Ex Situ Spectroscopic Ellipsometry of Low-Temperature-Grown GaAs, Journal of Electronic Materials, special insert: 2000 Electronic Materials Conference Program (Denver, CO) July 2000.

Kopanski, J. J., Marchiando, J. F., and Rennex, B. G., Carrier Concentration Profile Dependence of the Scanning Capacitance Microscopy Signal in the Vicinity of p-n Junctions, J. Vac. Sci. Technol. B 18 (1), Jan/Feb 2000, pp. 409-413.

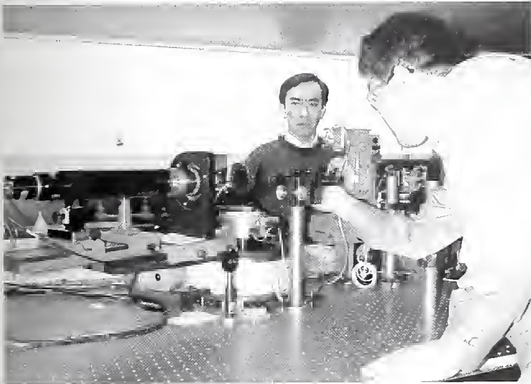
Kopanski, J. J., Marchiando, J. F., and Rennex, B. G., Scanning Capacitance Microscopy for Measuring Device Carrier Profiles Beyond the 100 nm Generation, Digest of Papers of the 2000 International Microprocesses and Nanotechnology Conference, at The University of Tokyo, Tokyo, Japan, July 11-13, 2000, pp. 250-251.

Marchiando, J. F., Kopanski, J. J., and Albers, J., Limitations of the Calibration Curve Method for Determining Dopant Profiles from Scanning Capacitance Microscope Measurements, J. Vac. Sci. Technol. B 18 (1), Jan/Feb 2000, pp. 414-417.

Thin-Film Process Metrology

Project Goals

Develop new and improved electrical and optical measurements, models, data, and reference materials to enable better and more accurate measurements of select, critical, silicon Complementary Metal Oxide Semiconductor (CMOS) technology thin-film parameters. Major focus is placed on requirements for oxynitrides, and metal-oxide and metal-silicate films and stacks for advanced gate dielectrics detailed in the 1999 International Technical Roadmap for Semiconductors (ITRS).



SED researchers align sample on custom-built high-accuracy spectroscopic ellipsometer.

Customer Needs

The evolving decrease of the gate dielectric film thickness to an oxide-equivalent value of 1 nm is identified as a critical front-end technology issue in the ITRS. For effective gate dielectric thicknesses below ~ 2.0 nm, SiO_2 is being replaced, initially by oxynitrides or oxide/nitride stacks, and then by either metal-oxides or metal-silicates. Process control tolerance needs for dielectric thickness are projected to be ±4 % (3σ), which translates to less than 0.1 nm for 2 nm films. Requirements for process control measurements are a factor of ten smaller still.

Spectroscopic ellipsometry (SE) is expected to continue as the preferred measurement for process monitoring of future gate dielectric films. Industry metrology needs not only improved methods to determine film thickness accurately, but also (1) techniques to determine the structure of the individual films and the interfaces between them; (2) an improved understanding of the relationship between physical, electrical, and optical determinations of film properties; and (3) mechanisms, such as reference materials, for traceability of measurements to NIST to support film metrology.

In order for SE to meet process control requirements of film thickness and unambiguously determine film composition and morphology, the optical properties of these advanced dielectric film systems must be characterized and understood.

Technical Strategy

This project focuses on the issues of (1) developing and providing the basis for traceability to NIST for film thickness measurements, (2) identifying structural models and developing preferred optical index dispersion functions or data for improved ellipsometric analysis of future-generation gate dielectric film systems, and (3) correlating optical, electrical, and physical measurements of thickness, composition, and interface structure.

Establish and transfer basis of accuracy for thin dielectric films

Industry requirements for future thin dielectric film optical measurements and calibration standards were identified at a NIST-sponsored workshop in FY 98. Core ellipsometry measurement capability is being expanded and strengthened to meet these requirements. An investigation has been started into cleaning and recontamination issues for film calibration standards to determine whether a workshop-expressed goal of 0.015 nm long-term reproducibility of reference artifact values is obtainable. Procedures are being developed to enable traceability of instrument accuracy to NIST for suppliers of secondary thin-film reference materials without volume production of NIST standard reference materials.

MILESTONE: By 2001, enable traceability to NIST to 1st Level commercial suppliers of reference materials for oxide films down to 2 nm.

Structural and optical models for ellipsometry

A custom-built, high-accuracy spectroscopic ellipsometer with a spectral range of 1.5 eV - 6 eV is being used for this task, and Project staff are working with SEMATECH, IC industry companies, and SRC university staff to obtain and optically characterize advanced oxynitrides, oxide/nitride stacks, and metal oxide and silicate films such as zirconium oxide and hafnium

Technical Contact:
James R. Ehrstein

Staff-Years:
3.5 professionals
1.7 technicians
1.0 guest researcher

Funding Sources:
NIST (99%)
Other Government Agencies (1%)

Parent Program:
Semiconductors, Silicon

"The development of innovative optical models that correlate with electrical measurements are especially needed as film thicknesses shrink below 2 nm."

National Technology Roadmap for Semiconductors

"Reference material, optical constants of one to two monolayers of gate dielectric materials, standard procedures, and optical models for non SiO_2 materials need to be developed."

National Technology Roadmap for Semiconductors

silicate. Characterization will be extended to 8.5 eV to include important optical index structure of these films beyond their bandgaps. This work is directed at determining preferred structural models, spectroscopic index of refraction values, or preferred optical dispersion functions for each of these film systems, and, where possible, the variability of these parameters due to differences in film fabrication processes. Analysis is done with software developed by NIST for spectroscopic ellipsometry; this software allows maximum flexibility for addition of the latest published or custom-developed optical response models as appropriate for each material system investigated.

MILESTONE: By 2002, establish preferred process-monitor capable ellipsometric models and analyses for stable-process replacement gate dielectric materials.

Relation between optical, electrical, and physical measurements of thickness

Through collaborations with SEMATECH, IC industry companies, and SRC university staff, as well as with key researchers in other parts of NIST, Project staff are leading and participating in a number of multimethod comparison studies of various ultra-thin gate dielectric films. These multimethod studies utilize techniques such as X-ray and neutron reflectivity, high resolution TEM, EELS, angle-resolved XPS, SIMS, C-V and I-V analysis, as well as spectroscopic ellipsometry and reflectivity. The results of these multimethod studies improve the general understanding of state-of-the-art (SOA) measurement capability for very thin films, and also allow Project staff to assess the results of various optical models being applied to the analysis of these films with respect to interface layers and structural composition, morphology, and uniformity. SOA C-V and I-V measurement capability for gate films has been established in the Project. Advanced 1-D analysis software from commercial and university sources has been established and benchmarked to determine the effect of model and algorithm sophistication on oxide film thickness values calculated from C-V and I-V data; extension to 2-D modeling is planned. An in-situ two-terminal electrical evaluation technique for buried interface roughness is being extended to 0.25 mm MOSFETs and beyond.

MILESTONE: By 2003, integrate preferred advanced electrical analysis software and structural analyses of high-κ dielectrics to improve agreement between electrical and ellipsometric thickness scales.

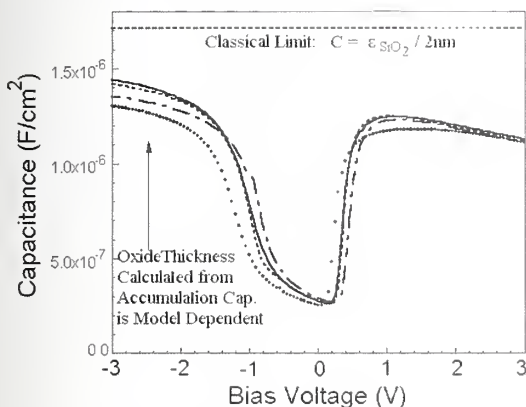
Accomplishments

- Verified, using a specially prepared set of nominal 10 nm thick Ta_2O_5 (high-κ) films that were annealed in 50 °C intervals from 650 °C to 950 °C (RTA in nitrogen), the evolution of secondary structure in the real and imaginary parts of the dielectric function of the film. This structure, which begins to appear for samples that are annealed at temperatures above 700 °C, is most strongly manifested in major, at 4.7 eV, and minor, at 5.1 eV, peaks in the real part of the dielectric function. This structure in the dielectric function is attributed to the formation of a crystalline phase in the films when annealed at the higher temperatures, as recently reported in the literature. In addition, Project scientists found that the real and imaginary parts of the dielectric function decrease in magnitude as anneal temperature increased above 750 °C. Such a decrease, which normally is associated with a decrease in the density of a material, was found to correlate with AFM-determined surface roughness and pinholes. Thus, features of the optical dielectric function, which serve as rapid indicators of both crystalline regions in the film as well as surface porosity, without the need to resort to TEM, have been confirmed.

- Completed data acquisition from a multi-laboratory study of the thickness of two very thin SiO_2 films using spectroscopic ellipsometry, X-ray and neutron reflectivity, and C-V measurements. A thermal desorption cleaning process was developed to remove surface contaminants and was required just prior to measurement for all participating laboratories. Lab-to-lab differences in thickness values, both between and within different types of measurements, were larger than expected. Diagnostic work to understand these differences will include study of the effects of different modeling assumptions on the thickness values and the return of all samples to NIST for testing of the robustness of the recommended cleaning procedure and also of the thickness equivalence of all test samples as measured on a single instrument.

- Demonstrated that the complementary manner in which the increased dielectric constant of high-κ gate dielectric materials affect the measurement of their electrical and

optical properties may be leverageable to extract additional materials properties during characterization. The increased dielectric constant that is required of dielectric materials for replacement of SiO_2 as the MOS gate insulator has the effect of making them electrically thinner but optically thicker than a SiO_2 film of the same physical thickness. This property was shown to have the potential of enabling increased information to be obtained from the characterization of both oxynitride films and high-κ films such as metal oxides deposited over an SiO_2-like interface layer when electrical and optical analysis is used in tandem. In the case of single-layer oxynitride films, it may be possible to extract the fraction of the total film composition that is comprised of silicon nitride. In the case of films such as metal oxides over lower-κ, SiO_2-like, interface layers, the interface layer is relatively undetectable by optical measurements such as ellipsometry, whose response is dominated by the thickness and index of the high-κ film. However, C-V characterization of such a film stack is dominated by the low-κ interface layer; thus a combined electrical-optical analysis of such films may enable the determination of the thickness of both the interface and the high-κ component films.



CV response for 2 nm gate oxide from 4 QM simulators

- Completed the 1-D comparison of six different sets of university and commercial sector software capable of accounting for polysilicon depletion and quantum mechanical effects in the substrate that obscure the determination of thickness of thin dielectric films from C-V and I-V measurements. A model structure consisting of a capacitor having several levels each of gate oxide thickness, gate poly-silicon doping, and substrate doping was used for the comparison. The results of the simulations, which were done from –5 V to 5 V, showed that the overall shape of the C-V curves were in generally good agreement. This instills confidence in their overall capability, particularly since very different fundamentals were generally incorporated in their development. Small differences in flatband and threshold values in one case were attributed to differences in default values for material properties. The largest differences among the software sets were in the accumulation capacitance, which is used for the electrical determination of the gate dielectric thickness. This resulted in thickness differences ranging from 0.17 nm for a nominal 3 nm film to 0.25 nm for a 1 nm film. These results demonstrate the effect of the choice of simulator when determining the effective electrical thickness of advanced gate materials and also the importance of knowing the details of the software used when comparing and interpreting reported results from different research teams.
- Improved the statistical analysis procedures for Weak Localization measurements to improve the reliability with which interface roughness values at the 0.1 nm level can be extracted.

FY Deliverables

Collaborations

Division 830, R. vanZee, molecular electronics (Curt A. Richter)

Division 837, E. Steel, high-resolution TEM capability applied to ongoing Project studies of various gate dielectric films (Curt A. Richter)

Division 837, L. Richter and E. Steel, optical characterization of semiconductor/dielectric interfaces and multimethod characterization of structure and composition of high-κ gate dielectrics (James R. Ehrstein and Curt A. Richter)

Division 842 R. Matyi, physical and optical properties of high-κ gate dielectrics (Curt A. Richter and Nhan Van Nguyen)

Division 852, D. L. Kaiser, BST and ZrO_2 thin dielectric films (Curt A. Richter)

Division 854, Wen-Li Wu, spectroscopic ellipsometry characterization of low-κ SiO_2 thin films (Nhan Van Nguyen)

Division 856, J. Pedulla and J. Dura, round robin on very thin thermal oxide films (James R. Ehrstein and Curt A. Richter)

Division 898, S. Leigh, statistical properties of weak-localization analysis (Curt A. Richter)

IBM, E. Gusev, optical and electrical thickness of oxynitrides (Curt A. Richter and James R. Ehrstein)

INTEL and Stanford University, C. M. Perkins, electrical and physical properties of ZrO_2 gate dielectrics (Curt A. Richter)

Jusung America, M. Gilmer, optical properties of HfO_2 gate dielectrics (Curt A. Richter and James R. Ehrstein)

Lucent Technologies, G. B. Alers, optical properties of high-κ gate dielectrics (Curt A. Richter and Nhan Van Nguyen)

Lucent Technologies, S. Martin, correlation of interface roughness and device noise (Curt A. Richter)

NIST, SED Scanning Probe Microscope Metrology Project, J. J. Kopanski, gate oxide formation under mild conditions for scanning capacitance microscopy (Barbara J. Belzer)

University of Maryland, J. N. Kidder, Jr., use of spectroscopic ellipsometry modeling software (SE Studio) and growth of high-κ dielectric thin films (Nhan Van Nguyen)

Pennsylvania State University, R. W. Collins, instrumentation for rotating compensator ellipsometers (Nhan Van Nguyen)

Pennsylvania State University, R. W. Collins, modeling of high-κ dielectric thin film using Urbach-Cody-Lorentz model (Nhan Van Nguyen)

Rudolph Technologies, Inc., D. Pelcher, traceability of SiO_2 + Si_3N_4 (Barbara J. Belzer)

Oak Ridge National Labs, John A. Woollam Inc., KLA - Tencor, n and k Technology, Four-Dimensions Inc., Solid State Measurements Inc., Therma-Wave Inc., Bede Scientific, Rutgers University, multimethod comparison of very thin thermal oxide films (James R. Ehrstein and Curt A. Richter)

SEMATECH, Changminh Jin, spectroscopic ellipsometry characterization of low-κ SiO_2 thin films (Nhan Van Nguyen)

SEMATECH, NC State Univ., KLA-Tencor, A. Diebold, D. Maher, and C. Hayzelden, development and characterization of 2 nm thick silicon dioxide reference artifacts (James R. Ehrstein, Curt A. Richter, and Nhan V. Nguyen)

SEMATECH, NC State Univ., KLA-Tencor, A. Diebold, D. Maher, and C. Hayzelden, investigation of contamination, storage, and cleaning of thin film reference artifacts (James R. Ehrstein, Curt A. Richter, and Nhan V. Nguyen)

SEMATECH, NC State Univ., KLA-Tencor, A. Diebold, D. Maher, and C. Hayzelden, optical and electrical characterization of high-κ gate dielectric films (James R. Ehrstein, Curt A. Richter, and Nhan V. Nguyen)

SEMATECH, W. Chism and A. Diebold, ellipsometry modeling of oxynitrides and high-κ gate dielectrics (Curt A. Richter and Nhan Van Nguyen)

Texas Instruments, D. Mercer and L. Columbo, process metrology for hafnium silicates (Curt A. Richter and James R. Ehrstein)

U. Texas at Austin, J. Lee, optical properties of ZrO_2 and HfO_2 for use as high-κ gate dielectrics (Curt A. Richter and Nhan Van Nguyen)

VLSI Standards, M. Tortonese, evaluation of experimental protocol for ellipsometry measurement traceability on Si_3N_4 films (James R. Ehrstein, Nhan V. Nguyen, and Barbara Belzer)

Standards Committee Participation

ASTM F-1 on Electronics, Executive Subcommittee, (James R. Ehrstein)

ASTM F-1 on Electronics, Subcommittee F1.06 on Silicon Materials and Process Control, Chairman (James R. Ehrstein)

ASTM F-1 on Electronics, Subcommittee F1.06, Section B on Thin Film Characterization, Section Chair, (James R. Ehrstein)

Publications

Gajewski, D. A., Nguyen, N. V., Guyer, J. E., Kopanski, J. J., Richter, C. A., and Pellegrino, J. G., In Situ and Ex Situ Spectroscopic Ellipsometry of Low-Temperature-Grown GaAs, Journal of Electronic Materials, special insert: 2000 Electronic Materials Conference Program (Denver, CO) Journal of Electronic Materials, Vol. 29, No. 7, July 2000, pp. 6-9.

Maher, D., and Richter, C. A., Gate Dielectric Metrology Review: Project FEPZ001 Year 2 Report, International SEMATECH Project, January 2000, 124 pages.

Richter, C. A., Nguyen, N. V., Alers, G. B., Guo, X., Wang, X., Ma, T. P., and Tamagawa, T., Analytical Spectroscopic Ellipsometry of Ta_2O_5 and TiO_2 for Use As High-κ Gate Dielectrics, Workbook of the 30th IEEE Semiconductor Interface Specialist Conference, December 1999, p. 2.2.

Vogel, E. M., Henson, W. K., Richter, C. A., and Suehle, J. S., Limitations of Conductance to the Measurement of the Interface State Density of MOS Capacitors with Tunneling Gate Dielectrics, IEEE Transac. on Electron Dev., Vol. 47, No. 3, March 2000, p. 601.

Metrology for Simulation and Computer-Aided Design

Project Goals

The goal of the Project is to facilitate the efficient and reliable application of semiconductor computer-aided design (CAD) tools by providing leadership for the development of an industry infrastructure for establishing model accuracy, developing methods for simulator model validation and benchmarking, developing metrology necessary for providing model data and model parameter extraction sequences, and developing models and techniques necessary for advanced device, process, package, and system simulation.

Test system used for IGBT parameter extraction and model validation.

Customer Needs

Efficient and reliable simulation methods are becoming more important as device structures and packages rapidly evolve. In addition, higher speed and higher power devices increase the importance of including the effects of packages in system performance simulation. However, advanced device electrical and thermal characterization procedures and validation of models used in computer-aided design tools have not kept pace with the application of the new device types and processes.

Several device technologies have evolved to an extent that conventional modeling and simulation capabilities are not suitable. For example, as CMOS devices are scaled to atomic dimensions, simulators must include quantum mechanical physics. The SRC/NIST/NSF Workshop on Nanoscale Transistors: Technology, Physics, and Simulation (Feb. 1999) identified quantum mechanical device simulation as an area required for device simulator progress. In addition, the device types used for power and microwave applications can no longer be represented by conventional device models provided in circuit and system simulation programs.

Technical Strategy

NIST addresses these needs by developing the theoretical foundations, standards, model validation procedures, and associated experimental techniques for the measurement of device electrical and thermal characteristics, and package electrical and thermal characteristics. NIST is developing, with industry, accepted procedures for validating device models for circuit simulation. NIST is developing procedures for characterizing the thermal and electrical performance of micro-electronic packages that are compatible and useful for CAD of boards and systems.

Device and Process Simulation Benchmarking

Accurate models and benchmarking procedures are becoming more important for device and process simulators. Current tasks include development of mobility, band gap, and intrinsic carrier concentration models for accurate simulation of compound semiconductor devices, and benchmarking of semiconductor device simulation tools that include quantum mechanical effects, including MEDICI, UTQuant, NCSU code, and NEMO.

Compact Package Electrical Interconnect Models

Interconnect structures are becoming a dominant factor in limiting the performance of modern computer, communication, and power systems. The Time-Domain Reflectometry (TDR) technique is being applied to characterize various multi-chip module and discrete packages interconnect systems.

MILESTONE: By FY 2001, develop a TDR test system with low source impedance (10 Ω), and characterize low-impedance interconnects used in microprocessor voltage regulator modules, advanced memory busses, and power electronic systems.

Package Thermal Metrology and Models

Accurate and timely simulation of system thermal performance requires new temperature

Technical Contact:
Allen R. Hefner, Jr.

Staff-Years:
4.0 professionals
4.0 guest researchers

Funding Sources:
NIST (99%)
Other Government Agencies (1%)

Parent Program:
Semiconductors, Silicon

The National Research Council (NRC) Workshop on Modeling and Simulation Opportunities in Manufacturing identified the process of model validation and accreditation as an issue to be addressed in developing a national research agenda for modeling and simulation.

measurement methods, new simulation methodologies, and validation procedures. Current tasks include the NIST electro-thermal network simulation methodology, including thermal network component models for semiconductor packages and heatsinks, and development of methodologies to validate the performance and accuracy of compact package thermal models.

Compact Device Electrical Models

Only recently has there been a significant effort in developing an infrastructure for validating the performance of compact models. An example of this activity is the NIST/IEEE Model Validation Working Group, founded in 1994 and now having over 200 members from 100 different technical organizations. For more information see http://ray.eeel.nist.gov/modval.html.

MILESTONE: By FY 2002, develop test system and models for SiC three terminal device.

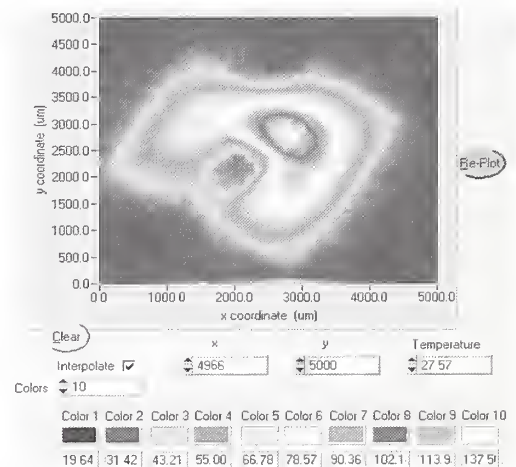
Accomplishments

- Provided leadership in developing a national agenda for modeling and simulation. Hefner presented an invited talk entitled, "Model Verification, Validation, and Accreditation of Semiconductor Device CAD Systems," at the National Academy of Sciences, National Research Council Workshop on Modeling and Simulation Opportunities in Manufacturing, April 26-27, 1999. The talk described the methodology for model validation being applied by the NIST/IEEE Working Group on Model Validation. The objective of the workshop was to develop a prospectus for a study that will recommend a national research agenda to address shortcomings in current modeling and simulation capabilities and to develop enhanced opportunities for coupling modeling and simulation with manufacturing.

- Impact study published on NIST models. An assessment of the U.S. economic impacts of the NIST IGBT model is detailed in a recent study entitled "NIST Planning Report 99-3: Benefit Analysis of IGBT Power Device Simulation," prepared by M. Gallaher and S. Martin, Research Triangle Institute Center for Economic Research (April 1999). The press release announcing this study appeared on the front page of the NIST Web site, appeared in the *NIST Update*, and was highlighted in the NIST Director's "State-of-the-Institute" speech. The economic impact study quantified the direct impacts of the NIST IGBT modeling at $18M (30 times the cost of the NIST program) and the indirect benefits at $40M/year, largely due to energy savings.

- NIST interconnect metrology proves valuable for EMI simulation. Models obtained from recent interconnect metrology research at NIST enabled the simulation of the EMI performance of various power converter topologies, as described in two NIST publications. In recent years, Electro-Magnetic-Interference (EMI) considerations have become increasingly important as Electro-Magnetic-Compatibility (EMC) regulations have become more stringent. The NIST metrology provides, for the first time, the capability to use simulation in the design of power converters with reduced EMI emissions.

- Developed High-Speed Semiconductor Device Transient Thermal Image System. The system provides the capability to measure the transient temperature distributions on the surface of a silicon chip with 10 ns temporal, 15 μm spatial resolution. The system uses computer-control software with a graphical user interface for controlling the translation stages, digitizing oscilloscope, and device test fixture temperature controller. The system also required the development of algorithms for calibrating and extracting the transient temperature waveform from an infrared microscope signal.



Semiconductor Device Transient Thermal Image System captures formation of dynamic hot spot.

- Developed IGBT model validation procedures and applied to component library. Developed circuits and measurement methods for validating IGBT models for soft-switching

conditions, applied the methods to models provided in a software vendors component library, and published results. Enhancements were made to the Hefner IGBT model that is provided in commercial circuit simulators as a result of this validation work. The NIST IGBT model was then used to simulate IGBT soft-switching performance in two papers; one describing reduced EMI emissions for soft-switched inverters, and the other describing the difference in soft-switching performance between different IGBT types.

- Developed capability to characterize and predict IGBT dynamic failures. The dynamic failure characteristics and avalanche-sustaining capability of various IGBT types, including new high-energy capable IGBTs, were measured using the unique NIST nondestructive failure tester and simulated using the NIST IGBT model. The measurements and simulations enabled the prediction of the mechanism resulting in High Avalanche Energy IGBTs and demonstrated the capability of the NIST IGBT model to predict the sustaining time and conditions for failure of both high-energy and conventional IGBT types.

- Developed software package for IGBT model parameter extraction (IMPACT). The software consists of five programs, LINMSR, SATMSR, LFTMSR, BTAMSR, and CVMSR, that extract the 20 physical and structural parameters of the most recent version of the NIST IGBT model. The programs have a graphical user interface, use the IEEE 488 bus to control the measurement instruments and collect data, and use various algorithms for fitting the IGBT model equations to the data. The new software package will facilitate the development of IGBT component libraries and enable end users of the simulation software products to extract model parameters themselves.

- SRC/NIST/NSF Workshop held at NIST. The Workshop, "Research Issues and Directions for Nanotransistors: Technology, Physics, and Simulation," was attended by over 50 researchers from industry, academia, and government. The Workshop identified critical modeling and simulation issues, such as quantum effects, that must be solved if modeling and simulation are to have a significant impact on the development of future nano-transistors. Modeling and simulation can speed progress in the development of future transistors if the infrastructure and physics are in place to attack relevant problems. As a result of this workshop, NIST developed a benchmarking procedure for quantum mechanical simulations that lead to an improvement in performance of one of the software products.

- Developed metrology for SiC diode characterization. As a result of NIST collaboration with CREE and Virginia Polytechnic Institute and State University (VPISU), under DARPA funding, it was demonstrated for the first time that SiC MPS (Merged PIN-Schotkey) diodes can substantially reduce energy consumption and EMI emissions for power converters and adjustable-speed drives. This reduction was demonstrated for diodes with ratings in the 300 V to 1500 V range, which represents the bulk of the applications in power electronics. CREE has decided, based on this demonstration, to pursue the commercialization of these diodes. This development is critically important to EPRI (Electric Power Research Institute) because 60 % of electrical power used in the U.S. is delivered to motors through IGBTs using adjustable speed drives, and the performance improvements offered by SiC diodes over Si diodes enhance the efficiency and reliability of these IGBT-based drives. DARPA is funding development of this technology for use in applications ranging from all-electric tanks to all-electric ships. NIST's interest in SiC devices is driven by our analysis that recent materials advances make these devices commercially attractive.

FY Deliverables

Collaborations

Analogy/IR/NIST, development of hundreds of IGBT library component models (Allen R. Hefner)

Analogy/IR/NIST, development of package thermal model library component models (Allen R. Hefner)

Analogy/POWERX/NIST, development of high power IGBT module library component models (Allen R. Hefner)

Avanti Inc./University of Arkansas, SiC power diode model library (Allen R. Hefner)

CREE, SiC diodes (David W. Berning)

CREE/NIST, development of SiC MPS-diode electro-thermal model (Allen R. Hefner)

DELPHI/Virginia Polytechnic Institute and State University, electronic interconnect characterization for vehicle auxiliary motor drive interconnects (Allen R. Hefner)

A recent Benefit Analysis Study by the Research Triangle Institute identified areas where NIST future involvement could significantly increase benefit: supporting enhancements to IGBT model, developing extraction tool/procedure eliminating need for structure data, and supporting model development of other classes of devices identified as weak links in the modeling chain.

Benefit Analysis of IGBT Power Device Simulation Modeling, Research Triangle Institute, 1999

Division 811, development of low-characteristic impedance time domain reflectometry (Allen R. Hefner)

Division 811, Jim St. Pierre, collaborating on defining research goals for metrology and benchmarking related to Systems-on-a-Chip (Angela M. Hodge)

"The NIST IGBT model is internationally accepted as the standard by which other IGBT models are compared."

Benefit Analysis of IGBT Power Device Simulation Modeling, Research Triangle Institute, 1999

Division 812, J. J. Kopanski, TCAD simulations (John Albers)

Division 812 (Nick Paulter), under ATP project to develop low-impedance transmission line characterization (David W. Berning)

Division 812, SCM Project, implant simulation and device simulation (Allen R. Hefner)

Division 812, Thin-Film Process Metrology Project and Gate Dielectric and Interconnect Reliability Project, new task on benchmarks for quantum-mechanical device simulation (Allen R. Hefner)

General Electric CRD/NIST, development of IGBT module models and parameter extraction tools (Allen R. Hefner)

Harris Semiconductor, development of component models for Harris IGBTs (Allen R. Hefner)

Rockwell Science Center/NIST, development of SiC transistor models (Allen R. Hefner)

TMA, implementation of new device physics into Medici device simulator (Allen R. Hefner)

University of Maryland, development of multi-technology System-on-a-Chip (Allen R. Hefner)

University of Maryland, Professor Neil Goldsman, collaborating on benchmarking quantum mechanical simulators for semiconductor devices (Angela M. Hodge)

University of Maryland, Professor Robert Newcomb, collaborating on defining research goals and objectives for NIST/SED initiative on Systems-on-a-Chip (Angela M. Hodge)

University of Maryland, quantum mechanical effects in 2-D semiconductor devices simulators (Allen R. Hefner)

University of Maryland, Reliability Physics Department, reliability issues for PEBB-like devices (Allen R. Hefner)

Virginia Polytechnic Institute and State University, package interconnect electrical characterization (Allen R. Hefner)

Virginia Polytechnic Institute and State University, SiC power device utilization (Allen R. Hefner)

Virginia Tech, SiC diodes (David W. Berning)

Standards Committee Participation

ASTM Committee, F107 Packaging, member (George G. Harman)

EIA/SEMATECH Compact Model Council (Allen R. Hefner)

IEEE Electron Devices Society, Standards Technical Committee, Chairman (Allen R. Hefner)

Software

HOTPAC (Programs for Thermal Analysis) distributed (John Albers)

IGBT Model PArameter extraCTion (IMPACT) software (Allen R. Hefner)

IGBT Network Simulation and Transient Analysis Tool (INSTANT) software package (Allen R. Hefner)

Igbt3.sin MAST circuit simulator model template (Allen R. Hefner)

NIST buffer layer IGBT model and library, distributed by Avanti Inc. as part of Saber simulator package (Allen R. Hefner)

NIST chip, package and heatsink thermal network component models, distributed by Avanti Inc. as part of Saber simulator package (Allen R. Hefner)

NIST IGBT electro-thermal model and library, distributed by Avanti Inc. as part of Saber simulator package (Allen R. Hefner)

NIST IGBT model and library, distributed by Avanti Inc. as part of Saber simulator package (Allen R. Hefner)

NIST IGBT model and library, distributed by OrCAD Inc. as part of PSPICE simulator package (Allen R. Hefner)

RESPAC (a collection of computer programs for two-probe resistance (spreading resistance) and four-probe resistance calculations) distributed (John Albers)

External Recognition

Received the IEEE Third Millennium Medal (George G. Harman)

Publications

Adams, V. H., Joshi, Y., and Blackburn, D. L., Three-Dimensional Study of Combined Conduction, Radiation, and Natural Convection from an Array of Discrete Heat Sources on a Horizontal Board in a Narrow-Aspect-Ratio Enclosure, Journal of Heat Transfer, Vol. 121, November 1999, pp. 992-1001.

Berning, D., and Hefner, A., IGBT Model Validation for Soft Switching Applications, IEEE Transactions on Industry Applications, Society Meeting, 1999, pp. 683-691.

Berning, D. W., and Hefner, Jr., A. R., IGBT Model Validation for Soft-Switching Applications, Conference Record IEEE Industry Applications Society Annual Meeting, Phoenix, Arizona, October 3-7, 1999, pp. 683-691.

Harman, G. G., The Effect of Polymer Material Properties on Wire Bonding to MCMs and Advanced Copper-Low-κ Integrated Circuits, Proceedings of the 2nd Annual IEEE-CPMT/ASME/SPE/SPIE/MRS/ARM/SF2M Workshop (POLY'99), Paris, France, December 12-15, 1999.

Hefner, A., and Bouche, S., Automated Parameter Extraction Software for Advanced IGBT Modeling, Proceedings of the IEEE Workshop on Computers in Power Electronics (COMPEL 2000), July 2000, pp. 9-17.

Hefner, A. R., Singh, R., Lai, J. S., Berning, D. W., Bouche, S., and Chapuy, C., SiC Power Diodes Provide Breakthrough Performance for a Wide Range of Applications, in the extended abstracts of 1st International Workshop on Ultra-Low-Loss Power Device Technology, pp. 140-147, June 2000, Nara Japan.

Hefner, A. R., Singh, R., Lai, J. S., Berning, D. W., Bouche, S., and Chapuy, C., SiC Power Diodes Provide Breakthrough Performance for a Wide Range of Applications, in the National Science Foundation Center for Power Electronic Systems Seminar, September 2000, pp. 17-24.

Hefner, A. R., Singh, R., Lai, J. S., Berning, D. W., Bouche, S., and Chapuy, C., SiC Power Diodes Provide Breakthrough Performance for a Wide Range of Applications, Japanese Future Electron Devices Journal, Vol. 11, August 2000, pp. 122-130.

Lai, J.-S., Song, B. M., Zhou, R., Hefner, Jr., A. R., Berning, D. W., and Shen, C.-C., Characteristics and Utilization of a New Class of Low On-Resistance MOS-Gated Power Device, Proceedings of the IEEE Industrial Applications Society Meeting, Phoenix, Arizona, October 3-7, 1999, pp. 1073-1079.

Marchiando, J. F., Kopanski, J. J., and Albers, J., Limitations of the Calibration Curve Method for Determining Dopant Profiles from Scanning Capacitance Microscope Measurements, J. Vac. Sci. Technol. B 18 (1), Jan/Feb 2000, pp. 414-417.

Shen, C. C., Hefner, A. R., Berning, D. W., and Bernstein, J. B., Failure Dynamics of the IGBT During Turn-Off for Unclamped Inductive Loading Conditions, IEEE Transaction on Industry Applications, vol. 36, pp. 614-624 (March 2000).

Singh, R., Ryu, S., Palmer, J., Hefner, A., and Lai, J., 1500 V, 4 Amp 4H-SiC JBD Diodes, in the Proceedings of 2000 International Symposium on Power Semiconductor Devices and ICs, pp. 101-104, May 2000, Toulouse France.

Song, B. M., Zhu, H., Lai, J. S., and Hefner, Jr., A. R., Switching Characteristics of NPT- and PT- IGBTs under Zero-Voltage Switching Conditions, 1999 IEEE Industry Applications Society Meeting, pp. 722-728.

Zhu, H., Lai, J.-S., Tang, Y., Hefner Jr., A. R., and Chen, C., Modeling Based Examination of Conducted EMI Emissions from Hard- and Soft-switching PWM Inverters, Proceedings of the IEEE Industrial Applications Society Meeting, Phoenix, Arizona, October 3-7, 1999, pp. 1879-1886.

MicroElectroMechanical Systems (MEMS)

Technical Contact:
Michael Gaitan

Staff-Years:
2.5 professionals
5.0 guest researchers

Funding Sources:
NIST (100%)

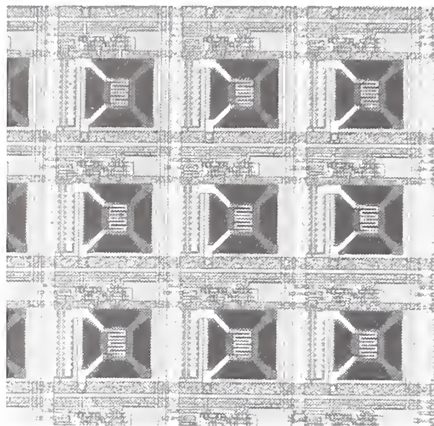
Parent Program:
Semiconductors, Silicon

"... Standardization of test methods such as residual stress and elastic modulus will save manufacturers time and money."

Nicholas Swart, Analog Devices

Project Goals

Provide domestic industry with MEMS-based standardized test structures and test methods for characterizing the thermo-electro-mechanical properties of materials and thin films used in integrated circuit (IC) and MEMS technologies. Work with IC foundries to develop measurement infrastructure for improved system-on-a-chip manufacturing. Research and develop novel metrology applications of MEMS technology.



Optical micrograph of a 3x3 section of microheating elements that are part of a larger array. These microheating element arrays are being used in a thermal-flat panel display for testing and calibration of night vision equipment in collaboration with Optical ETC, a CRADA partner.

Customer Needs

The MEMS Project serves its customers in the following three areas: ITRS Roadmap, System-On-A-Chip, and Micro-Metrology Tools.

ITRS Roadmap

Increasing device density in integrated circuits leads to more interconnect layers with smaller cross-sectional area and higher aspect ratio; all of which increase the probability of failure by mechanisms such as electromigration, stress migration, and delamination. These reliability problems reside in the interconnect and dielectric layers of the IC. The interconnect and dielectric layers of an IC can be thought of as laminates of a multilayer film composite. The IC industry requires new measurement methods to characterize the mechanical strain in these multilayer films. Results can then be used to verify finite element models of the stress in the films and to correlate mechanical stress data with reliability testing. MEMS-based test structures being developed in this Project offer new ways to characterize the mechanical stress in multilayer films.

System-On-A-Chip

Manufacturers of MEMS products, such as acceleration sensors for automotive air bag exploders and deformable mirror displays for projection imaging, are mainstream U.S. IC companies. These products integrate electromechanical elements within the IC. This integration of mixed technologies is part of the semiconductor industry's move towards "system-on-a-chip."

System-on-a-chip will link the functionality of the IC (information processor) with information gathering (sensing the environment) and actuation (changing the environment). System-on-a-chip ICs will include mixed-signal RF, MEMS, electro-optical, and micro-fluidic systems.

New test structures, test methods, and standards are required for improving device and reliability characterization. The Project's customers are MEMS IC manufacturers and government laboratories.

Micro-Metrology Tools

Miniaturization technologies developed by the semiconductor industry such as thin-film deposition and growth, photolithography, etching, and micromachining are increasingly being used to make new metrology tools. Such tools can improve the way we presently measure things or create totally new ways to measure things. To this end, the Project's customers come from within the NIST laboratories and other government agencies to draw on the Project staff expertise in micro fabrication.

Technical Strategy

MEMS Test Structure Standardization

The MEMS technical community, composed of companies, universities, and government laboratories, has developed many types of test structures to characterize the fabrication process and device performance. What is lacking is standardized test methods and standard reference materials. The MEMS Project plays an active role in the new ASTM Task Group E08.05.03, metrology for thin-film electromechanical properties of MEMS-based IC technologies.

MILESTONE: By 2001, develop a standard test method for measurement of MEMS test structure length required by the MEMS industry for measurements of residual stress and elastic modulus.

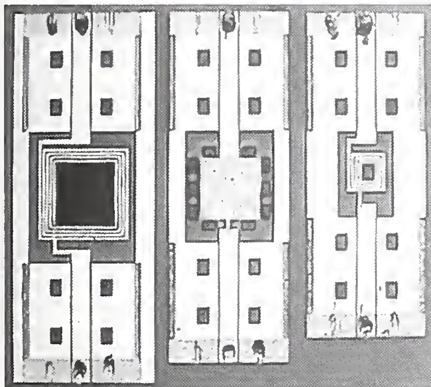
MILESTONE: By 2002, develop a standard test method for measurement of residual stress in MEMS devices.

MILESTONE: By 2003, develop a standard test method for measurement of elastic modulus in MEMS devices.

IC Interconnect Characterization

Micromachining techniques, test structures, and test methods are being developed to characterize the stress, elastic modulus, and adhesion properties in IC interconnects. These test structures are fabricated in the standard IC process on fully fabricated ICs. Fixed-fixed beam and cantilever test structures with interconnect layers are micromachined in the fully processed IC. Measurements of the deflection of buckled beams give information on the stress in each interconnect layer. Measurements of mechanical resonance give information on the elastic modulus of the films. These test structures can also be integrated with microheating elements for accelerated testing.

MILESTONE: By 2001, develop a test method for elastic modulus of CMOS IC dielectric and interconnet layers that is based on mechanical resonant test structures.



Optical micrograph of micromachined spiral inductor and capacitor coplanar transmission line test structures fabricated in a commercial CMOS process available from the MOSIS service.

Micro Fabrication Laboratory

Micro fabrication methods developed by the semiconductor industry can be used to create new measurement tools. The MEMS Project is utilizing this technology to develop tools for the IC industry. The Project is also working with other NIST Groups and Divisions to create new metrology tools for U.S. industries.

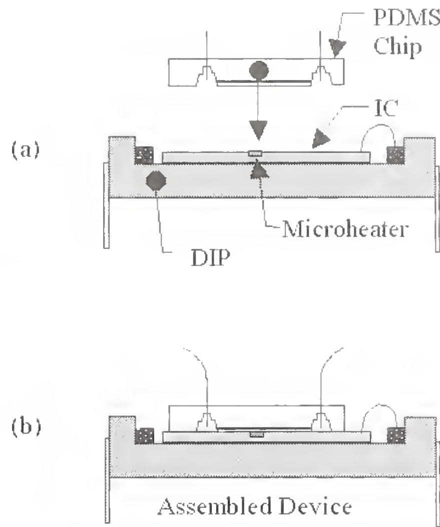


Diagram of the assembly process that has been developed for embedding an IC containing a microheating element in a plastic-based microfluidic system.

"Janet Marshall and others in the MEMS program at NIST are an integral part of the core group of the ASTM standardization effort. Through their involvement, NIST plays a crucial role in the development of standards and shapes the future of the MEMS industry in the United States."

Chris Muhlstein, ASTM Committee

Accomplishments

- Test structures and analysis to measure mechanical stress/strain of interconnects in fully fabricated ICs were developed. A test chip containing the new test structure designs was fabricated by the commercial foundry MOSIS, based on 1.2 µm CMOS technology. Following fabrication, the test structures were silicon-micromachined in order to mechanically release them. These test chips contained test structures to measure the longitudinal stress component in IC interconnects. New designs are being developed to measure the lateral and normal components of stress as well. As IC device sizes shrink, thermo-mechanical stress in interconnects is an ever-increasing reliability concern. Current state-of-the-art IC technology uses 5 interconnect layers with aspect ratios (height/width) of 1.8. According to the 1999 International Technology Roadmap for Semiconductors, these numbers are expected to increase to 9 and 3, respectively, by the year 2012. Despite the increasing number of interconnect layers in IC technology, existing stress determination and modeling studies have been limited to single level metallization, with few exceptions. This is due, in large part, to the lack of experimental techniques for measuring strain in narrow linewidth

(< 10 mm) multilayer structures. This work allows, for the first time, the measurement of stress in multilayer structures in fully fabricated ICs.

- The first round robin experiment was completed for the ASTM Task Group formed on MEMS. The experiment explored the precision and bias associated with the residual stress test structures in a round robin experiment for residual stress. The round robin, which involved 11 other organizations, was sponsored by the ASTM Task Group E08.05.03 on "Structural Films for MEMS and Electronic Applications," which develops standards for electronic and MEMS applications. This task group has undertaken sponsorship of a series of round robin testing of residual stress and elastic modulus in test structures on a die passed among participating laboratories. These parameters are important to the fabrication of MEMS devices. The first series of tests for this round robin emphasized the metrology of the structures that is required for the calculations of residual stress. Participation in the ASTM Task Group gives NIST a leadership role in the development of measurement standards for the semiconductor industry. In addition, measurement methods that are discussed and developed at the task group meetings are useful to the MEMS Project activities.

- A MEMS test structure was developed in collaboration with Analog Devices that was based on prior work by Liwei Lin, UC Berkeley. The new test structure was optimized to measure appropriately tensile strain in the Analog Devices' commercial MEMS process; however, it can be used to measure compressive strain as well. This new "folded beam micro strain gauge" has a vernier resolution of 0.1 mm. It was fabricated in Analog Devices' process. Theories and designs from this activity are available to other MEMS manufacturers. The MEMS industry requires standardized tools such as test methods and test structures to manufacture their products. Analog Devices supplied test chip space to the NIST designs in their commercial process. This test structure has been passed on to the ASTM E08.05.03 Task Group for possible inclusion in a residual stress round robin.

- Invented CMOS 1D and 2D accelerometers that operate based on heat convection. This device differs from the traditional MEMS-based accelerometers in that its operation is not based on a solid proof mass. The device consists of microheating elements and thermocouple sensors separated by a gap and placed in differential configurations. Thermocouple sensors measure the temperature difference between the two sides of the microheater caused by the effect of acceleration on free convection in the surrounding gas. The devices show a small linearity error of <0.5% under tilt conditions from –90 degrees to 90 degrees, and <1.6% under acceleration from 0 g to 8 g.[1] Sensitivity of the devices is a nearly linear function of heater power (temperature). For operating power between 35 mW and 45 mW, a sensitivity of 20 μV/g to 30 μV/g was measured. This is a spin-off of OA-sponsored work on Micromachined Passive Microwave Components in CMOS Technology. An invention disclosure was written which resulted in material that was patented by NIST and our CRADA partner, RF Microsystems. This activity exemplifies our leadership role in MEMS/Microsystems Technology (MST).

- A shared-access micro fabrication laboratory has been developed. The facility provides accessibility of micro fabrication processes to other NIST groups, increases the payoff to investment, and facilitates an environment where scientists can interact with each other on cross-disciplinary applications.

FY Deliverables

Collaborations

Advanced Technology Program/Materials and Manufacturing Technology Office, development of MEMS programs in ATP. Workshop held in November at the ATP National Meeting in San Jose, CA (Michael Gaitan)

Analog Devices, MCNC, MSEL Materials Reliability Division, metrology for thin-film electromechanical properties for MEMS and IC technologies (Janet C. Marshall and Michael Gaitan)

ASTM Task Group E08.05.03, metrology for thin-film electromechanical properties of MEMS-based IC technologies (Janet C. Marshall)

CSTL Analytical Chemistry Division, Microfluidic Systems (Michael Gaitan)

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[1] Data published in Milanovic, V., Bowen, E., Zaghloul, et al., Micromachined Convective Accelerometers in Standard Integrated Circuits Technology, Applied Physics Letters, Volume 76, Number 4, January 24, 2000, pp. 508-510.

CSTL Biotechnology Division, BioMolecular Systems (Michael Gaitan)

EU & NEXUS, Fraunhofer Institute for Manufacturing Engineering and Automation, YOLE Development Co, France, EPFL, Switzerland, Keio University, Japan, Canadian Microelectronics Corporation, Canada, Internet-Based MEMS International Standardization Forum (Michael Gaitan)

MOSIS, Optical ETC, American Microsystems Incorporated (AMI), development of CMOS MEMS foundry fabrication services (Michael Gaitan)

NIST Nano/Micro/Meso-Scale Coordination Committee, EEEL, MEL, PL, CSTL (Michael Gaitan)

Optical ETC, integrated thermal emitter arrays (Michael Gaitan)

PL Atomic Physics Division, microsystems for laser tweezers (Michael Gaitan)

PL Optical Technology Division, single molecule florescence imaging (Michael Gaitan)

UMD, MEMS Exchance, JHU Applied Physics Labs, NRL, GWU, Georgetown U, NASA, Army Research Lab, NSWC Indian Head, MEMS Alliance (Michael Gaitan)

Standards Committee Participation

ASTM MEMS 2nd Residual Stress Round Robin, recommended delaying the 2nd residual stress round robin to accommodate the more complete analyses of fixed-fixed beam and cantilever test structures (Janet C. Marshall)

ASTM Task Group E08.05.03, wrote a first draft of a NIST-IR currently entitled "Linear Metrology and Curvature Measurements Using an Optical Interferometer." The purpose of the NIST-IR is to provide the technical basis for the two new MEMS metrology standards (Janet C. Marshall)

ASTM Task Group E08.05.03, out of four possible standards that could immediately be pursued, two have been selected which benefit the broadest segment of the MEMS community (Janet C. Marshall)

ASTM Task Group E08.05.03, will be the lead writer for the two MEMS standards (Janet C. Marshall)

Software

Software was developed to decrease the time required for the complete analyses of fixed-fixed beams and cantilever test structures (Janet C. Marshall)

MEMS Test Structure Web Pages, the 3-point analysis of fixed-fixed beam and cantilever test structures was placed on the Division's Web pages (under the MEMS Project) so that these analyses can be performed on-line, developed and distributed (Janet C. Marshall)

Publications

Milanovic, V., Bowen, E., Zaghloul, M. E., Tea, N. H., Suehle, J. S., Payne, B., and Gaitan, M., Micromachined Convective Accelerometers in Standard Integrated Circuits Technology, Applied Physics Letters, Volume 76, Number 4, January 24, 2000, pp. 508-510.

Ozgur, M., Milanovic, V., Zincke, C., Gaitan, M., and Zaghloul, M. E., Quasi-TEM Characteristic Impedance of Micromachined CMOS Coplanar Waveguides, IEEE Trans. Microwave Theory and Techniques, May 5, 2000, pp. 852-854.

Smee, S. A., Gaitan, M., Novotny, D. B., Joshi, Y., and Blackburn, D. L., IC Test Structures for Multi-Layer Stress Determination, IEEE Electron Device Letters, Vol. 21, No. 1, January 2000, pp. 12-14.

Xu, J., Locascio, L., Gaitan, M., and Lee, C., Room Temperature Imprinting Method for Plastic Microchannel Fabrication, Anal. Chem., 2000, 72(8), 1930-1933.

Locascio, L. E., and Gaitan, M., Integrated Silicon Microheating Elements Using Silicon-on-Plastic Drop-In Functionality, Micro Total Analysis Systems 2000, May 2000.

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Ozgur, M., Zaghloul, M. E., and Gaitan, M., Micromachined 28-GHz Power Divider in CMOS Technology, IEEE Microwave and Guided Wave Lett., 10(3), March 2000.

Ozgur, M., Milanovic, V., Zincke, C., Gaitan, M., and Zaghloul, M. E., Quasi-TEM Characteristic Impedance of Micromachined CMOS Coplanar Waveguides, IEEE Tran. on Microwave Theory and Tech., pp. 852-854, May 2000.

Invited Talks

Marshall, "Optomechanical Technique for Measuring MEMS Layer Thickness," ASTM E08.05.03 Task Group Meeting, King of Prussia, PA, June 13, 2000.

Marshall, "Static Deflection Analyses for MEMS Fixed-Fixed Beam and Cantilever Test Structures," ASTM E08.05.03 Task Group Meeting, King of Prussia, PA, June 13, 2000.

Gaitan, "Integration of Microreactive Elements in Plastic Microfluid Systems," at the 1999 ATP National Meeting, Nov 15-17, 1999, San Jose, CA.

Gaitan, "Micromachined Passive Microwave Elements for Effective Isotropic Radiated Power Sensor," invited, 1999 IEEE Solid-State Circuits and Technology Workshop on MEMS Interface Circuits at the Key Bridge Marriott, Arlington, VA, October 14, 1999.

Gaitan, "Integrated Circuit MicroHeating Elements," UMD Short Course Instructor, April 6, 2000.

Gaitan, "Integration of Microreactive Elements in Plastic Microfluid Systems," George Washington University Seminar Series, January 27, 2000.

Gaitan, "NIST MEMS Project," NASA Goddard Seminar, Feb 16, 2000.

Gaitan, "MicroHotplate Devices and Arrays," NIST Workshop on NonContact Thermometry, April 14, 2000.

Gaitan, "MEMS Based IC Test Structures for Mechanical Stress in Interconnects," Topical Research Conference on Reliability, Nov 1, 1999.

Gaitan, "MicroElectroMechanical Systems (MEMS)," 2015 Future Threat Technologies Panel, Science and Technology Expert Partnership, CIA Headquarters, McLean, VA, August 4, 2000.

Linewidth and Overlay Standards for Nanometer Metrology

Technical Contact:
Michael W. Cresswell

Staff-Years:
3.0 professionals
1.0 technician
2.0 guest researchers

Funding Sources:
NIST (99%)
Other Government Agencies (1%)

Parent Program:
Semiconductors, Silicon

Project Goals

Develop test-structure-based electrical metrology methods and related reference materials with primary emphasis on linewidth metrology and calibration and overlay; contribute to standards organizations supporting the development of metrology standards for the semiconductor tool industry.

Lattice-plane selective etches provide reference features with atomically planar sidewalls.

Customer Needs

The Semiconductor Industry Association's (SIA) International Technology Roadmap for Semiconductors (ITRS) states that it is critically important to have suitable reference materials for lithography support available when on-wafer measurements are made as a new technology generation in integrated circuit (IC) manufacturing is introduced, and particularly during development of advanced materials and process tools. Each generation of ICs is characterized by the transistor gate length whose control to specifications during IC fabrication is a primary determinant of manufacturing success. The SIA projects the decrease of gate linewidths used in state-of-the-art IC manufacturing from present levels of up to 250 nm to below 90 nm within several years. Scanning electron microscopes (SEM) and other systems used for traditional linewidth metrology exhibit measurement uncertainties exceeding ITRS-specified tolerances for these applications. It is widely believed that these uncertainties can be at least partially managed through the use of reference materials with linewidths traceable to nanometer-level uncertainties. Until now, such reference materials have been unavailable because the technology needed for their fabrication and certification has not been available. It is also widely believed that the usefulness of SEM metrology for monitoring wafers in advanced development and production will become inadequate at some future IC generation. Thus, there exists a need for new methodology to meet future metrology requirements.

Technical Strategy

The technical strategy that the Project staff have developed for fabricating linewidth and overlay reference materials is known as the Single-Crystal Silicon-on-Insulator Reference-Material implementation. Patterning with lattice-plane selective etches of the kind used in silicon micromachining provides reference features with atomically planar sidewalls, as shown in the figure to the left. Selection of bond and etch-back silicon-on-insulator (BESOI) starting material with (110) surface orientation that is thermo-mechanically bonded to a (100) handle wafer provides reference-feature-sidewall verticality.

The traceability path for dimensional certification is provided by High Resolution Transmission Electron Microscopy (HRTEM) imaging. This method provides nanometer-level accuracy, but is sample-destructive and prohibitively costly to implement. This Project's unique traceability strategy thus features the sub-nanometer repeatability of electrical CD metrology as a secondary reference means. Low-cost, whole-wafer electrical measurements are effectively calibrated with a few local HRTEM lattice-plane image counts. Typical reference features are several-thousand lattice planes wide. HRTEM lattice-plane image counts, achieved by high-density digitization and numerical differentiation of the photographic record, require 3000 bpi digitization and highly-specialized, but proven image-analysis software. Both Sandia National Laboratories and Los Alamos National Laboratory have provided invaluable assistance in the development of this procedure.

The technical strategy has to be responsive to industry's requirement for reference materials to have the physical properties of standard 200 mm wafers. This Project's technical strategy is to dice

each 150 mm wafer and mount the separate chips in micromachined standard 200 mm wafers to accommodate the test chips. The result is that finished units are user-friendly at an acceptable cost. The entire fabrication and certification process is being transferred to a commercial standards vendor.

Project staff use the Single-Crystal Silicon-on-Insulator technical strategy also for a class of overlay reference materials known as tool-induced shift extractors. The special requirement here is the replication of features with different heights from the same photo-lithographic reticle. Project staff have devised a way of doing this with a unique selection of otherwise standard CMOS fabrication steps.

A key requirement that linewidth reference materials must satisfy is edge-definition sufficient to render width certification as meaningful. The fabrication and certification strategy complies with this requirement. Project staff have devised a method for fabricating the reference materials with suitable geometries and a method of certifying their widths at an acceptable cost. The next milestone is to perform electrical measurements and HRTEM on the same features and, through their correlation, to establish low-cost electrical linewidth metrology as a secondary reference means for the SOI-BESOI implementation.

Aligning probe card to silicon subtrate under test.

MILESTONE: By 2001, fabricate and certify Single-Crystal Silicon-on-Insulator Reference-Materials with linewidths traceable to silicon lattice counts with an uncertainty goal of less than 5 nm.

The certification of tool-induced shift extractors will require (110) handle wafers and (100) surface wafers, the inverse of that employed for the linewidth reference materials. This approach allows the utilization of HRTEM images of lattice planes for the determination of the pitches of line pairs.

MILESTONE: By 2002, demonstrate the fabrication and certification of overlay reference materials with uncertainties below the 5 nm level and extend the technology to pitch reference materials.

The technical strategy for on-reticle linewidth metrology is to extract linewidths of control features electrically from test pads located outside the pellicle and therefore accessible to both the user and the supplier. These, in effect, serve as a built-in reference for the calibration of the optical microscopes used by both parties. In this application, the < 2 nm repeatability and robustness of electrical metrology is anticipated to have unique advantages.

MILESTONE: By 2002, demonstrate electrical CD metrology as a means of providing on-reticle CD calibration.

Accomplishments

- High-resolution transmission electron microscopy has revealed (111) lattice fringes spanning the entire width of a NIST [112] mono-crystalline linewidth reference feature patterned on (110) BESOI material. A preliminary lattice-plane count of the HRTEM image was made by inspection of a photographic print obtained by an optical microscope. Use of a drum scanner has demonstrated that the lattice-plane count can be fully automated. The width of the feature was determined to be 583 nm, with a combined standard uncertainty (coverage factor $k = 2$) of 2.5 mm.
- Standard 200 mm wafers were micromachined to serve as reference-material test-chip carriers. The fabrication process features three-step lithography and etching with thermal oxide and low-temperature nitride hard masking. A technique for mounting the reference-material test chips in the carriers was developed. Samples of the carriers were delivered to, and used by, all major semiconductor manufacturers.
- In collaboration with Photronics Laboratories, Inc., Project staff developed and fabricated electrical linewidth-control features for inspection of photo-mask reticles used in integrated-circuit manufacture. The design

"The Photomask industry as well as the Semiconductor industry have a problem meeting the technical road map using optical systems to measure IC patterns. As the time line moves forward we get closer to a point that our current measurement systems will not be able to satisfy the requirements. This is why the project of electronic measurement has appeal to Photronics. We would like to continue supporting this project and hopefully as the electronic measurement tools become viable NIST has a traceable standard. Thanks for your continuation of this standard."

Dave Owens, Photronics Laboratories

allows probe-card access to electrical test pads advantageously located outside the pellicle while uniquely providing for electrical testing of the process-replicated linewidth-control features at the wafer level. Tests are in progress.

- A process for fabricating microstructures for calibrating optical-overlay metrology tools used in the manufacture of integrated circuits was developed. It features a unique combination of process steps extracted from CMOS processing, SOI, and silicon micromachining unit-processes. These structures have all the properties, such as atomically-planar feature side-walls, geometrical symmetry, material uniformity, and provisions for traceability, that are necessary for monitoring the fabrication of emerging generations of sub-tenth micrometer integrated circuits. A unique fabrication process in which different layers of the micro-structure are imaged at the same time from a single reticle enhances built-in overlay-vector traceability.
- A new generation of Single-Crystal Silicon-on-Insulator Reference-Material test chips fabricated on BESOI starting material and having feature linewidths less than 200 nm was delivered to a consortium of 11 integrated-circuit manufacturers for evaluation. The distribution was accompanied by NIST electrical-linewidth measurements for the respective features. The consortium members returned their own measurements. The consortium's measurements track this Project's measurements, in most cases, to within less than 25 nm.
- The effective electrical linewidths of single-crystal linewidth reference features replicated on (100) BESOI substrates were modulated by DC biasing the handle wafer with respect to the cross-bridge resistor in which the reference feature was embedded. Both the sheet resistance and the electrical linewidths of the reference features closely tracked the predictions of theoretical models.
- The use of off-lattice alignment of reference features to enable their replication with linewidths as narrow as 90 nm with a 0.5 µm lithography projection aligner was demonstrated. The results of this activity may enable the narrower features to be routinely replicated using an all-optical standard fabrication process.

"The single crystal linewidth standard project currently under joint development by NIST and Sandia National Labs will satisfy a major void that has previously existed in the metrology section of the International Roadmap for Semiconductors. The researchers from NIST have also, very cleverly, devised a rock-solid traceability methodology into the standard that starts with counting atom pairs within the silicon lattice. This atomic count is the basis for final certification of the quantity of standards that the industry will require. The final manufacturable phase is accomplished by employing a direct correlation between the atomic count and an electrical certification."

Bradley W. Scheer, then Director of Research, VLSI Standards, Incorporated

FY Deliverables

Collaborations

International SEMATECH member companies (AMD, Compaq, Conexant, Hewlett-Packard, IBM, Intel, Lucent Technologies, Motorola, Texas Instruments, Hyundai, Infineon Technologies, Philips, STMicroelectronics, TSMC), development of single-crystal critical dimension reference materials (Michael W. Cresswell and Richard A. Allen)

International SEMATECH, development of single-crystal critical dimension reference materials (Michael W. Cresswell and Richard A. Allen)

Solecon Laboratories, evaluating SOI substrates for reference materials (Michael W. Cresswell)

NIST Division 812, Performed focused ion beam (FIB) cut of silicon lines (Richard A. Allen and Wen F. Tseng)

Photronics Laboratories, development of optical/electrical hybrid critical dimension measurement for photomasks (Richard A. Allen and Michael W. Cresswell)

Sandia National Laboratories Microelectronics Development Laboratory, Sandia National Laboratories Compound Semiconductor Research Laboratory, Sandia National Laboratories Integrated Materials Research Laboratory, Los Alamos National Laboratory, NIST Statistical Engineering, Precision Engineering Divisions, and International SEMATECH, fabrication and certification of reference materials for linewidth and overlay metrology (Michael W. Cresswell, Loren W. Linholm, and Richard A. Allen)

Sandia National Laboratories, Statistical Engineering Division, Metallurgy Division, University of Central Florida, and Precision Engineering Division, SEMATECH, reference artifacts for critical dimension measurements (Michael W. Cresswell, Loren W. Linholm, and Richard A. Allen)

Scientific Computing Division, Hai Tang, assistance with ANSYS model of single crystal CD reference material project (Colleen H. Ellenwood)

Simplex Solutions, Inc., procedures and algorithms for CD extraction from electrical test structures having conformal coatings (Michael W. Cresswell)

University of Edinburgh, U.K., modeling of current flow in three-dimensional Van der Pauw test structures (Michael W. Cresswell, Loren W. Linholm, and Richard A. Allen)

VLSI Standards, development of single-crystal critical dimension and overlay reference materials (Michael W. Cresswell and Richard A. Allen)

VLSI Standards, Inc., and International SEMATECH, development of commercial architecture and distribution plan for single-crystal CD reference materials (Michael W. Cresswell and Richard A. Allen)

Standards Committee Participation

SEMI International Standards Electrical Metrology Test Structures Task Force, Co-Chair (Richard A. Allen)

SEMI International Standards Microlithography Committee, member (Richard A. Allen)

SEMI International Standards, Global Microlithography Coordinating Committee (Michael W. Cresswell)

SEMI International Standards, NA Regional Micro-Lithography Committee, Co-chair (Michael W. Cresswell)

SEMI International Task-Force on X-Ray Lithography Mask Standard, Leader (Michael W. Cresswell)

External Recognition

SEMI Certificate of Appreciation for Efforts and Support of SEMI International Standards Program (Richard A. Allen)

Publications

Allen, R. A., Linholm, L. W., Cresswell, M. W., and Ellenwood, C. H., A Novel Method for Fabricating CD Reference Materials with 100 nm Linewidths, 2000 International Conference on Microelectronic Test Structures, IEEE, pp. 21-24, 2000.

Cresswell, M. W., Allen, R. A., Ghoshtagore, N. M. P., Shea, P. J., Everist, S. C., and Linholm, L. W., Characterization of Electrical Linewidth Test Structures Patterned in (100) Silicon-on-Insulator for Use as CD Standards, International Conference on Microelectronic Test Structures ICMTS Proceedings, IEEE, pp. 3-9, 2000.

Cresswell, M. W., Bonevich, J. E., Headley, T. J., Allen, R. A., Giannuzzi, L. A., Everist, S. C., Ghoshtagore, R. N., and Shea, P. J., Comparison of Electrical CD Measurements and Cross-Section Lattice-Plane Counts of Sub-Micrometer Features Replicated in (100) Silicon-on-Insulator Material, Proceedings of SPIE, Vol. 3998, pp. 74-83, Feb. 28 - Mar. 2, 2000.

Penzes, W. B., Allen, R. A., Cresswell, M. W., Linholm, L. W., and Teague, E. C., A New Method to Measure the Distance Between Graduation Lines on Graduate Scales, IEEE Transactions on Instrumentation and Measurement, Vol. 48, No. 6, December 1999, pp. 1178-1182.

Villarrubia, A. E., Vladar, A. E., Lowney, J. R., Postek, M. T., Allen, R. A., Cresswell, M. W., and Ghoshtagore, R. N., Linewidth Measurement Intercomparison on a BESOI Sample, Proceedings of SPIE, Vol. 3998, pp. 84-95 (2000).

Dielectric and Interconnect Reliability Metrology

Technical Contact:
John S. Suehle

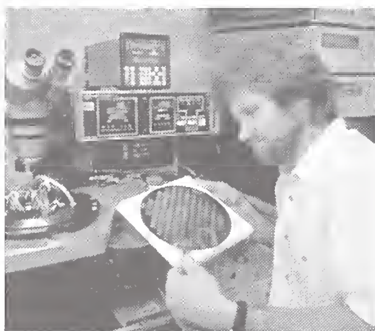
Staff-Years:
2.0 professionals
1.0 technician
4.0 guest researchers

Funding Sources:
NIST (99%)
Other Government Agencies (1%)

Parent Program:
Semiconductors, Silicon

Project Goals

Provide technological leadership to semiconductor and equipment manufacturers by developing and evaluating the methods, tools, diagnostic procedures, data, and physical models for understanding and improving the reliability of (1) ultra-thin silicon dioxide and alternative gate dielectric films, and (2) metal interconnects, such as copper, used in advanced CMOS technologies.



Test wafer being loaded on wafer prober for long-term dielectric testing.

Customer Needs

Ultra-thin gate dielectrics for future microelectronic device scaling are regarded as one of the most difficult challenges by the Semiconductor Industry Association's (SIA) International Technology Roadmap for Semiconductors (ITRS). As the semiconductor industry continues to scale device dimensions to achieve channel lengths below 180 nm, gate dielectrics must be scaled to have an equivalent thickness below 2 nm. Ultra-thin SiO_2 dielectrics exhibit high tunneling currents, and the impact on device reliability is not well understood. The physics of failure and traditional reliability testing techniques must be reexamined for ultra-thin gate oxides that exhibit excessive tunneling currents and soft breakdown.

As device scaling continues, an alternative high-dielectric constant (high-κ) gate dielectric system will be required due to the excessive tunneling currents exhibited by sub 2 nm SiO_2 films. The ITRS states that no suitable alternative high dielectric constant material has been identified with the stability and interface characteristics to serve as a gate dielectric. Years of research and development are required to identify and qualify a suitable alternative material.

"The gate dielectric has emerged as one of the most difficult challenges for future device scaling. ... No suitable alternative high dielectric constant material has been identified with the stability and interface characteristics to serve as a gate dielectric. Years of research and development are required to identify and qualify a suitable alternative material.

SIA International Technology Roadmap for Semiconductors

This project focuses on (1) the physics of failure and the reexamination of traditional reliability testing techniques of ultra-thin SiO_2 gate oxides that exhibit excessive tunneling currents and soft breakdown, (2) providing an understanding of the electrical characterization methodologies and reliability characterization required for alternative high-κ gate dielectrics for advanced CMOS devices, and (3) developing critical electromigration standards and metrology methods for advanced metallization systems, including copper.

Technical Strategy

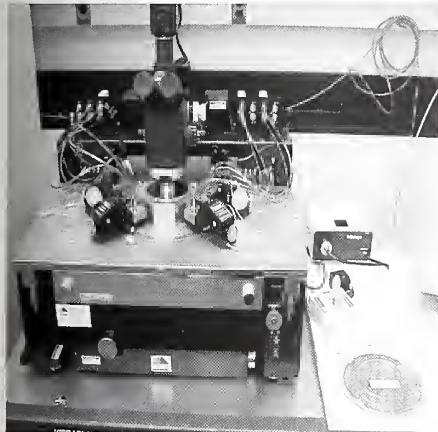
Test structure designs and test methods for characterizing copper interconnects will also be developed in collaboration with partners in the Semiconductor Industry. Special NIST-designed test chips include numerous structures for evaluating via and straight line electromigration and will be used as a vehicle to develop and validate test procedures and analysis techniques.

MILESTONE: By 2001, reliability test chips NIST 33 and 34 will be designed for experiments that include the determination of the precision of three electromigration standards: ASTM F1260 (constant current density and temperature test), JEP119 (SWEAT test), and JESD61 (isothermal test) for single-level metal.

The physical mechanisms responsible for "soft" or "quasi" breakdown modes in ultra-thin SiO_2 films and their implications for device reliability will be investigated as a function of test conditions and temperature. Long-term time-dependent-dielectric breakdown tests will be conducted on SiO_2 films as thin as 1.5 nm at lower electric fields closer to operating conditions. These tests will be used to determine the thermal and electrical acceleration parameters of device breakdown. Experiments will be conducted to investigate the differences of gate oxide breakdown and wear-out due to high oxide field and hot-carrier injection. This study will provide insight into the physical mechanisms of ultra-thin gate oxide wear-out and breakdown.

Highly accelerated breakdown tests used to monitor manufacturing by the U.S. Semiconductor Industry must also be reevaluated for ultra-thin gate oxides. Traditional ramped voltage and current breakdown tests are not able to detect breakdown in films less than 4 nm thick.

In FY 2000, the development of a new test procedure for characterizing the reliability of ultra-thin dielectrics was initiated through a NIST-coordinated collaboration between the Electronic Industries Association Joint Electron Device Engineering Council (EIA-JEDEC) and American Society for Testing and Materials (ASTM). NIST will continue its leadership role in the JEDEC and ASTM standards committees.



Probe station shown above allows femto-amp current measurements on advanced gate dielectric films for characterizing leakage current and reliability.

MILESTONE: By 2001, a new standard constant voltage stress test will be developed for determining Time-Dependent-Dielectric Breakdown (TDDB) acceleration parameters in sub 3 nm thick SiO_2 films. The new test will utilize current or voltage noise as breakdown criteria when films exhibit soft breakdown. Such a test will find application by the semiconductor industry when qualifying new manufacturing processes.

High-κ gate dielectric films will be obtained from key industrial and university groups. Electrical characterization methodologies will be developed to address various issues associated with these films, including large leakage currents, quantum effects, thickness dependent properties, large trap densities, transient (non-steady state) behavior, unknown physical properties, and the lack of physical models.

Examples of measurement problems that are being addressed include modifying and verifying electrical defect density measurement techniques, including conductance-frequency, capacitance-voltage, and charge-pumping.

MILESTONE: By 2002, electrical and reliability characterization methodologies and analysis will be established for high-κ dielectric materials. These methodologies will include the characterization of interface electrical properties, dielectric integrity, and long-term electrical stability and reliability.

Accomplishments

- A systematic study of the uncertainties, sensitivity, and limitations of the conductance technique for extracting the interface state density of metal-oxide-semiconductor (MOS) devices with ultra-thin (< 3.0 nm) oxides was completed. Capacitance and conductance characterization of MOS devices are used to determine properties such as oxide thickness, substrate doping, and interface state density. However, with the advent of ultra-thin oxides, effects such as tunnel current, series resistance, and quantum mechanical confinement in the substrate require additional consideration. This work provides a detailed analysis of the impact of these effects on parameter extraction using conductance and capacitance characterization of MOS devices with ultra-thin oxides.

- A new Standard Reference Database (SRD) program was initiated to provide the semiconductor industry with electrical and physical properties of alternative gate dielectrics for MOS devices from peer-reviewed journal articles. The goal for the first year of the program is to collect articles representing the main body of knowledge on alternative dielectrics for silicon. Due to increased power consumption and device and circuit instabilities associated with ultra-thin SiO_2, a high permittivity gate with low leakage current and at least equivalent capacitance, performance, and reliability will be required. However, as compared to SiO_2, very little is known about the electrical and physical properties of these films as gate dielectrics. The formation of an SRD to document the properties of these materials would provide the semiconductor industry a comprehensive database of evaluated properties from a variety of sources to use in the further research and development of alternative gate dielectrics.

- A new study has been initiated to examine soft breakdown in 1.3 nm to 2.5 nm SiO_2 films and to study the temperature dependence of time-dependent dielectric breakdown. A more dramatic temperature dependence of wear-out has been observed, which raises serious reliability concerns. The purpose of this study is to obtain the temperature dependence of time-dependent dielectric breakdown for films as thin as 1.3 nm and to determine if soft breakdown modes influence the temperature

"For 100 nm devices and below, the gate dielectrics will be so thin that gate current will become a very important design factor. Improvements in basic understanding are needed, including reliability aspects."

SIA National Technology Roadmap for Semiconductors

"Time-Dependent-Dielectric Breakdown (TDDB) voltage and temperature dependence of new gate stack materials are not known."

SEMATECH Reliability Technology Advisory Board Supplement to the 1999 International Technology Roadmap for Semiconductors

dependence. The reliability of gate oxides is becoming a critical concern in advanced CMOS technologies where devices will operate with higher gate electric fields and direct tunneling currents. The physical mechanism responsible for new "soft" breakdown modes and its implications for device reliability were investigated as a function of test conditions and temperature. These tests provide critically important field acceleration parameters and thermal activation energies that are required for reliability extrapolation of ultra-thin oxides.

- A new research program to develop metrology for the semiconductor industry's next generation gate dielectric has been established at NIST. The program concentrates on the development of techniques and analysis for the electrical and reliability characterization of alternative dielectric materials for advanced microelectronics. Collaborations have been established with Texas Instruments, University of Delaware, the SRC/SEMATECH Front End Processing Center, the University of Minnesota, North Carolina State University, and Lucent Technologies. No suitable alternative high dielectric constant material has been identified with the stability and interface characteristics to serve as a gate dielectric. Significant research and development are required to identify and qualify a suitable alternative material.
- Interconnect reliability test chips NIST 33 and NIST 36 were designed and fabricated, and are being used. These chips are a collection of test structures designed in collaboration with members of JEDEC Committee JC14.2 on Wafer Level Reliability and with industry researchers. They are vehicles for improving existing reliability standards and for developing new ones for interconnects that are based on the results of inter-laboratory and other experiments. Wafers of NIST 33 were fabricated by the Stanford Nanofabrication Facility using single-level metal structures of an Al 1% Si alloy. Wafers of NIST 36 were recently fabricated for NIST by Silicon Graphics (formerly Cray Research) using a cladded Al-1% Cu metallization. Inter-laboratory experiments with these wafers are underway with LSI Logic Corporation and Infineon Technologies serving as additional reference laboratories. NIST 36 contains a variety of single-level metal and via-type electromigration test structures for evaluating the designs of these test structures and their use in test methods to characterize the reliability of interconnects. It also includes structures to measure stress voiding, electromigration-driven noise, metal sheet resistance and linewidth, and oxide thermal conductivity. The availability of via-type test structures on NIST 36 is intended to stimulate critically needed activities in JEDEC for the development of metrology tools for characterizing stress voiding and electromigration in vias.

FY Deliverables

SRDs

SRD in progress on alternate gate dielectrics (Eric M. Vogel)

Collaborations

Advanced Micro Devices, ultra-thin oxide reliability (John S. Suehle)

Analog Devices, Limerick, Ireland, ultra-thin gate oxide reliability (John S. Suehle)

Cree Research, gate dielectrics on SiC (John S. Suehle)

CSTL/Process Measurements Division, microhotplate-based sensor arrays (John S. Suehle and Michael Gaitan)

Divisions 836 and 837, M. Tarlov, molecular electronics (Curt A. Richter and John S. Suehle)

Dynamic Research Corporation, ultra-thin gate oxide reliability (John S. Suehle)

Fairchild Semiconductor, ultra-thin gate oxide reliability (John S. Suehle)

General Electric, gate dielectrics on SiC (John S. Suehle)

George Washington University, microhotplate-based chemical sensors (John S. Suehle)

Lucent Technologies, ultra-thin gate oxide reliability (John S. Suehle)

MIT Lincoln Laboratories, microhotplate-based chemical sensors (John S. Suehle)

Motorola, ultra-thin gate oxide reliability (John S. Suehle)

N.C. State University (oxynitrides, nitrides, ultra-thin SiO_2), alternative gate dielectrics (Eric M. Vogel)

National Microelectronics Research Center, ultra-thin gate oxide reliability (John S. Suehle)

National Semiconductor, ultra-thin gate oxide reliability (John S. Suehle)

Penn State University, ultra-thin gate oxide reliability (John S. Suehle)

SRC/SEMATECH Front End Processing Center, alternative gate dielectrics (Eric M. Vogel)

Sterling Semiconductor, gate dielectrics on SiC (John S. Suehle)

Texas Instruments, electrical and reliability characterization of ultra-thin gate oxides (John S. Suehle and Curt A. Richter)

Texas Instruments, ultra-thin gate oxide reliability (John S. Suehle)

University of Delaware, alternative dielectrics (John S. Suehle)

University of Delaware, Newark, alternative gate dielectrics (Eric M. Vogel)

University of Maryland, College Park, microhotplate-based chemical sensors (John S. Suehle)

University of Maryland, College Park, ultra-thin gate oxide reliability (John S. Suehle)

University of Maryland, gate dielectric reliability (Eric M. Vogel)

University of Maryland, microhotplate-based sensor arrays (John S. Suehle)

Standards Committee Participation

JEDEC JC14.2 Dielectric Working Group, Chairman (John S. Suehle)

JEDEC JC 14.2 Electromigration Working Group, consultant (Harry A. Schafft)

Publications

Head, L. M., and Schafft, H. A., An Evaluation of Electrical Linewidth Determination Using Cross-Bridge and Multi-Bridge Test Structures, 1999 IEEE International Integrated Reliability Workshop Final Report, Lake Tahoe, CA, p. 41.

Henson, W. K., Yong, N., Kubicek, S., Vogel, E. M., Wortman, J. J., De Meyer, K., and Naem, A., Analysis of Leakage Currents and Impact on Off-State Power Consumption for CMOS Technology in the 100 nm Regime, IEEE Transactions on Electron Devices, Vol. 47. No. 7, pp. 1393-1400.

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Suehle, J. S., Ultra-Thin Film Dielectric Reliability Characterization, Gate Dielectric Integrity: Material, Process, and Tool Qualification, ASTM STP 1382, D. C. Gupta and G. A. Brown. Eds., American Society for Testing and Materials, West Conshohocken, PA, 2000, p. 27.

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Major Facilities / Laboratories

Microfabrication Process Facility

See next page for facility description

Contacts: Russell Hajdaj, 301-975-2699
Guilford L. Krepps, 301-975-2095

Molecular Beam Epitaxy Facility

A research facility for growing and utilizing high-quality epitaxial films of III-V compound semiconductors and for developing *in-situ* metrology to control their growth properties.

Dual-chamber MBE growth system

Contact: Joseph G. Pellegrino, 301-975-2123

Materials Characterization Labs

High-Resolution Optical:

Spectroscopic Ellipsometry, High-Resolution Fourier Transform Infrared Spectroscopy, Photoluminescence, Raman Scattering, Photoreflectance, and other Modulation Spectroscopies

Electrical:

Resistivity, Spreading Resistance, Lifetime, Hall Effect, Deep-Level Transient Spectroscopy, Deep-Level Optical Spectroscopy, Charge-Pumping Measurements, Capacitance-Voltage (high frequency & quasi-static), Surface Photovoltage, AC Impedance Analysis, Scanning Capacitance/Atomic Force Microscopy

X-Ray:

Double-Crystal Rocking Curve, Laue Orientation Facility

Device and Test Structure Characterization Labs

Semiconductor Electrical and Package Thermal
Power Device Model Extraction and Validation
Packaging, Assembly, and Bonding Evaluation
Package Interconnect
Scanning-Electron Microscope
Scanning-Probe Microscope
Automatic Wafer-Level Measurement
Gate Dielectric Integrity
MEMS Electrical, Mechanical, Optical, and Microwave

Computer-Aided Design Labs

Test Structure Layout and Design
Integrated Circuit Layout, Design, and Simulation
Finite Element Thermal Analysis Tools and Computational Fluid Simulations
System, Device, Process, Interconnect, and Virtual Fabrications Simulations

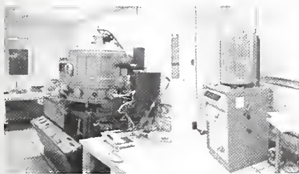
Microfabrication Process Facility

Description

As integrated circuit (IC) sizes increase to more than 1 cm^2 and feature sizes within the circuits decrease to less than 1/10 μm, critical demands are placed on the measurement capability required to control and monitor IC fabrication successfully. To meet the demand, NIST researchers are developing state-of-the-art measurement procedures for microelectronics manufacturing.

The Microfabrication Process Facility provides a quality physical environment for a variety of research projects in semiconductor microelectronics as well as in other areas of physics, chemistry, and materials research. The laboratory facilities are used for projects addressing many areas of semiconductor materials and processes, including process control and metrology, materials characterization, and the use of integrated circuit materials and processes for novel applications.

The laboratory complex occupies about 5200 square feet, approximately half of which is composed of Class 1000 cleanroom space. Within the cleanroom, work areas are maintained at class 30. The facility is designed so the work areas can be modified easily to accommodate the frequent equipment and other changes required by research.



Metallization: sputter and evaporation.

Objective

Current objectives are to develop and fabricate structures and devices to fulfill the needs of metrology projects within SED and NIST. These structures include MEMS-based devices, micro-electronic devices, and other specialized devices.

Capabilities

The facility has a complete capability for IC fabrication. Principal processing and analytical equipment is listed below.

Diffusion, Oxidation, and Annealing

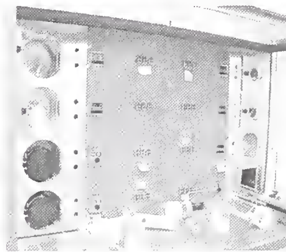
Six furnace tubes for up to 75 mm diameter wafers and 5 tubes for up to 100 mm diameter wafers.

Photolithography

Research mask aligner (proximity and contact) for wafers up to 100 mm in diameter and irregularly shaped samples, and 10 × direct-step-on wafer system for 75 mm diameter wafers. Photoresist spin coating and developing and related chemical processing, including oxygen plasma stripping. E-beam writing and scanning electron microscope examination of nano-features on 75 mm wafers.

Thin-Film Deposition

Low-pressure chemical vapor deposition systems for depositing silicon nitride, polysilicon, and low-temperature silicon dioxide. Radio frequency and dc vacuum sputtering of metals and dielectrics.



Film deposition and diffusion furnaces.

Etching

Wet and dry etching processes. Plasma barrel etching of nitride films and wet chemical etching of silicon for micromachining. Xenon Difluoride silicon etch process.

Wet chemical processing.

Analytical Measurements

Thin-film reflectometry and other thickness measurements, optical microscopy, and grooving and staining.

In-Situ Metrology

In-situ, real-time, multiple wavelength ellipsometry to measure optical constants of silicon and other chemical vapor deposition materials such as silicon dioxide, polysilicon, and silicon nitride.

Post Processing Equipment

DISCO HI-Tech America Inc. 8" wafer dicing saw and SEM cross-section sample prep equipment.

Applications

Small quantities of specialized semiconductor test specimens, experimental samples, prototype devices, and processed materials can be produced. The processes and processing equipment can be monitored during operation to study the process chemistry and physics. The effects of variations in operating conditions and process gases and chemical purities can be investigated. Research is performed under well-controlled conditions.

A research-oriented facility, the laboratory is not designed to produce large-scale ICs or similar complex structures. Rather, the laboratory emphasizes breadth and flexibility to support a wide variety of projects.

Automatic 8" wafer dicing saw.

Currently, research projects address many aspects of microelectronic processing steps and materials as well as silicon micromachining. Examples include: metal-oxide-semiconductor measurements; metal-semiconductor-specific contact resistivity; uniformity of resistivity, ion-implanted dopant density, surface potential, and interface state density; characterization of deposited insulating films on silicon carbide; ionization and activation of ion-implanted species in semiconductors as a function of annealing temperature; electrical techniques for dopant profiling and leakage current measurements; and processing effects on silicon-on-insulator materials. A simple CMOS process has been established. Recent work has also begun in the field of molecular electronics.

Availability

Facility staff welcome collaborative research projects consistent with the research goals of the NIST semiconductor program. Work is performed in cooperation with the technical staff of the laboratory.

The most productive arrangements begin with development of a research plan with specific goals. The commitment of knowledgeable researchers to work closely with NIST staff and the provision of equipment and other needed resources are required. Because hazardous materials are present, laboratory staff must supervise all research activities.

Tasks

- Design and develop optical thermometer (bi-material cantilever with optical coupling for measurement).
- Fabricate Multi-Junction Thermal Converter (MJTC) in collaboration with Electricity Division.
- Fabricate structures for thermal conduction of silicon dioxide round robin.
- Investigate over-etching phenomena that occurs in Si at the (111) - (001) plane junction with anisotropic etchants.
- Publish MJTC fabrication procedure and process data, as a NIST Special Publication.
- Develop and organize equipment and processes for molecular electronics research.

Recent Process Equipment Additions

- SEM with E-Beam Writing Capability
- 8" Wafer Dicing Saw

National Research Council (NRC) Postdoctoral Opportunities

The Semiconductor Electronics Division at the National Institute of Standards and Technology (NIST), in cooperation with the National Research Center (NRC), offers awards for postdoctoral research for American citizens in the fields described below. The Division conducts research in semiconductor materials, processing, devices, and integrated circuits to provide, through both experimental and theoretical work, the necessary basis for understanding measurement-related requirements in semiconductor technology.

NIST affords great freedom and an opportunity for both interdisciplinary research and research in well-defined disciplines. These technical activities of NIST are conducted in its laboratories, which are based in Gaithersburg, a large complex of modern laboratory buildings in a Maryland suburb of metropolitan Washington, DC. Applications for NIST Research Associateships are evaluated by the panels only during February. To be eligible for review in February, completed application materials must be postmarked no later than January 15, 2001, and received by the Associateship Programs office no later than January 25, 2001. Supporting documents must be received by the Associateship Programs by February 15, 2001. These times will also be approximately the same in 2002.

Scanning Probe Metrology

This project explores scanning probe microscope techniques to measure the spatial variation of physical and electrical properties of electronic devices and materials to the nanometer resolution scale. Scanning capacitance microscopy is being developed as a tool for measuring the dopant profile in two dimensions across a silicon p-n junction. Our project is developing both the experimental apparatus, which is based on an atomic-force microscope, and the theoretical modeling needed to interpret the results. Interests extend to other scanning probe techniques, including nano-spreading resistance, various optically pumped scanning probes, and scanning microwave microscopy.

Contact: David G. Seiler, 301-975-2054

Overlay- and CD-Metrology Development for Characterization of Advanced Lithography Systems

Projected CD and overlay control-tolerances for emerging generations of ICs drive final output-metrology uncertainty requirements down to the several-nanometer region. Similar requirements apply to metrology for the characterization of lithographic tools used for wafer processing. However, the development of CD and overlay metrologies is not maintaining the pace of lithographic resolution capabilities of the advanced imaging systems that will be coming on line in the near future. In addition, preferred processing options such as chemical/mechanical polishing tend to render existing overlay-metrology less effective for key process steps. The IC Technology Group seeks individuals interested in conducting further research into novel overlay-sensing instruments and techniques, and CD-extraction methodologies that are specifically optimized for lithographic tool characterization. We also encourage applicants with research experience in noncontact/nonintrusive electrical CD extraction and multimode overlay-sensor development, including overlay and CD-target and test-structure designs which are customized for the subject application.

Contact: Michael W. Cresswell, 301-975-2072

Reference Materials for the Evaluation of CD, Overlay, and Placement Instrumentation Traceable to Fundamental Length Standards

Participants in the National Semiconductor Metrology Program, which has been established at NIST, are regularly contacted by IC-industry groups for reference-material substrates that have structures and grids with certified CDs, overlay, and feature placements consistent with SIA-projected requirements. Applications include validating metrology-instrument performance and optimizing image-deconvolution algorithms. In the case of CDs, citing such reference materials is especially difficult because features having definitive cross-section profiles of particular geometries, dimensions, and material uniformity

are difficult to manufacture, thus challenging the reference-material certification process. In collaboration with other national laboratories and several commercial organizations, the IC Technology Group has recently begun a new project to fabricate and evaluate artifacts fabricated by novel techniques involving silicon-on-insulator materials to address the stated purposes. Our goal is to enable the low-cost manufacture and certification of reference materials to support the calibration and maintenance of metrology instruments used in advanced semiconductor manufacturing.

Contact: Michael W. Cresswell, 301-975-2072

Electrical Characterization of Semiconductor Compounds, Alloys, and Microstructures

A wide variety of electrical and magnetotransport techniques are being developed and utilized to characterize the electronic properties of compound semiconductor materials and microstructures. Measurement techniques include CV dopant profiling, deep-level transient spectroscopy, magnetotransport ($H \leq 8$ T), and conventional and photo Hall methods. Our goal is to understand the physical phenomena associated with these techniques and use them to investigate and characterize compound semiconductors of interest to industry.

Contact: David G. Seiler, 301-975-2054

Optical and Spectroscopic Properties of Semiconductors

Research focuses on understanding the electronic behavior of semiconductor materials and microstructures from their optical and spectroscopic response. Areas of investigation include the role of impurities and native defects in bulk crystals, and novel and useful optical properties induced by quantum confinement in reduced dimensional structures (heterostructures, quantum wells, superlattices, and quantum wires and dots). The broad range of cw optical probes that is available include reflection, transmission and absorption (1 meV to 7 eV), and modulation spectroscopy; photoluminescence and photoluminescence excitation; Raman and resonant-Raman scattering; and spectroscopic ellipsometry. Emphasis is placed on understanding technology relevant properties, developing accurate measurement techniques, and producing standard reference materials and data required by U.S. industry.

Contact: David G. Seiler, 301-975-2054

Molecular Beam Epitaxy: Characterization and In-Situ Metrology

The unique growth capabilities of molecular beam epitaxy (MBE) have resulted in a variety of new electronic and optical devices which depend on engineered bandgaps and controlled interfaces. NIST's MBE facility consists of a dual chamber GaAs-based III-V system. One side is devoted to the growth of GaAs-based heterostructures to address the materials and growth metrology issues for electronic and opto-electronic devices. This includes confinement-type devices such as high electron mobility transistors, resonant tunneling devices, and laser structures. A current research area involves correlating the structural properties of interfaces with the transport and optical properties for modulation-doped field effect transistors. The other GaAs chamber is used to develop the essential metrology for implementing in-situ electrical, optical, and X-ray-based probes in an ultrahigh vacuum growth environment. These probes include X-ray fluorescence, specular and off-specular reflectance, and spectroscopic ellipsometry probes. The MBE effort is interactive because growth and characterization within the MBE facility is supported by a comprehensive set of ex-situ electronic, structural, optical, and magnetotransport spectroscopies. In addition, facilities exist within the Division for simple III-V processing. Opportunities are available for candidates interested in studying growth and materials-related issues of semiconductors, as well as implementing real-time in-situ probes for better control over growth parameters.

Contact: Joseph G. Pellegrino, 301-975-2123

Physics of Semiconductor Devices

Device-modeling and theoretical-device physics research are in progress to interpret measurements of model parameters. One goal of this work is predictive physical models of devices with high carrier and doping concentrations. For example, topics include high-concentration effects, carrier lifetimes, carrier mobilities, and radiation effects that affect the operation and performance of semiconductor devices. The approach in this work involves the careful examination, extension, and experimental verification of the theoretical basis used in device

models for silicon, gallium-arsenide, and other compound semiconductor devices. Collaborations are in progress to include these improved physical models in device simulations and then to verify, validate, and benchmark these enhancements.

Contact: Herbert S. Bennett, 301-975-2079

Microelectronic Package Characterization

Research focuses on the electrical and thermal properties of microelectronic packages and interconnects. Our objectives are to improve methods for characterizing these properties for advanced packages and modules; improve measurement methods and techniques; and verify "compact" electrical and thermal models for packages and modules, and parameter extraction techniques for the models. We have fully equipped thermal and electrical characterization laboratories including an infrared thermal imager and a time domain interconnect parameter analyzer, and several computer workstations with a compliment of thermal and electrical modeling and analysis software.

Contact: David L. Blackburn, 301-975-2068

Silicon-Based Quantum Devices for Room Temperature ULSI Circuits

The complementary-metal-oxide-semiconductor (CMOS) field-effect-transistor is showing fundamental limits associated with the laws of quantum mechanics and the limitations of fabrication techniques. This is driving research on innovative solutions to augment or replace CMOS technologies. Silicon-based quantum devices such as quantum dots, resonant tunneling devices, and single-electron transistors deliberately exploit quantum and size effects. We are interested in fundamental research in any aspect of silicon-based quantum devices, including but not limited to fabrication, simulation, and characterization of device structures and constituent materials/processes. Our primary expectation is to be able to identify and address critical metrology issues for this emerging technology of silicon-based quantum devices. In support of this research, we have a clean room with a variety of fabrication equipment including furnaces, evaporators, and optical and electron-beam lithography tools. We have numerous software packages available for device, electrical, and physical simulation, including the NanoElectronic Modeling program, NEMO; and the molecular simulation program, CerisII/CASTEP. We have a wide range of electrical characterization equipment that allows device characterization at temperatures ranging from approximately 1 K to 700 K. This includes ultra-low noise probe stations, cryostats, semiconductor parameter analyzers for current-voltage measurements and AC capacitance-conductance-inductance measurements, specialized setups for Hall and Magnetotransport measurements, and a variety of additional electronics. We also have numerous supporting analytical measurement techniques available including spectroscopic ellipsometry, atomic force microscopy, and scanning capacitance microscopy.

Contact: David L. Blackburn, 301-975-2068

Modeling Advanced Semiconductor Devices for Circuit Simulation

Accurate circuit simulator models for advanced semiconductor devices are required for effective computer-aided design of electronic circuits and systems. However, the semiconductor device models provided in most commercial circuit simulators (e.g., simulation program with integrated circuit emphasis) are based on microelectronic devices, and they do not adequately describe the dynamic behavior of advanced semiconductor devices. Therefore, research focuses on the following: (1) physics-based models - for advanced semiconductor devices such as power and compound semiconductor devices (these models are implemented into available circuit and system simulation programs); (2) parameter extraction algorithms - for obtaining model parameters from terminal electrical measurements; and (3) characterization procedures - for verifying the models' ability to simulate the behavior of the devices within application circuits. NIST also works closely with commercial software vendors to make the new models available to circuit design engineers, and has established the NIST/IEEE Working Group on Model Validation to develop comprehensive procedures for evaluating the performance of circuit simulator models. (For more information, see ray.eeel.nist.gov/modval.html.)

Contact: Allen R. Hefner, Jr., 301-975-2071

Ultrasmall Devices and Nanoelectronics

The objective of this research is to develop the principles behind new fabrication technologies and highly accurate metrology of nanometer-scale devices for application to quantum standards and quantum-based nanoelectronics. The ultrasmall devices are based on quantum resonant tunneling, Coulomb blockade, ballistic transport, and mesoscopic effects. Research includes the development of (1) technologies needed for cost-effective ways to fabricate device structures in nanometer scale dimensions in order to improve performance of these new devices, (2) improved methods to characterize and model their electrical and optical behavior, and (3) capabilities to measure and understand quantum devices that are necessary for future electrical standards.

Contact: Wen F. Tseng, 301-975-5291

MicroElectroMechanical Systems

The MicroElectroMechanical Systems (MEMS) project centers on the development and modeling of novel electro-mechanical sensors and actuators manufactured by integrated circuit fabrication techniques. Research includes the design, fabrication, and modeling of microheating elements, mechanically resonant structures, optical systems on a chip, microwave transmission lines, power sensors, antennas, and microfluidic systems. Metrology efforts involve developing MEMS test structures and test methods to characterize device properties, test their performance and reliability, and develop device models based on these measurements. MEMS-based test structures are also being utilized to characterize film properties in mainline semiconductor fabrication processes.

Contact: Michael Gaitan, 301-975-2070

Microfabrication and Application of Microthermal Fluidic Systems

Microheating elements have been recently used as microchemical reactors and fluid flow sensors in microfluidic systems. This technology will allow researchers to harness heat for monitoring and controlling chemical reactions in microfluidic systems that provide active control of processes in picoliter volumes. The microreactors are fabricated using a silicon integrated circuit (IC) process followed by post process bulk and surface micromachining steps. The ICs are embedded in the plastic and/or polymeric-based substrates that contain a network of microchannels. Fabrication methodology is fully compatible with the monolithic integration of digital and analog circuits. We believe that integration is the key issue for advancement of the Microanalytical Laboratory of the future and it is the basis of drop-in functionality for microfluidic integration. Because of the multidisciplinary nature of this work, we are interested in postdoctoral candidates in engineering, chemistry, materials science, and physics. Research would focus on the development of new fabrication methodologies, design and fabrication of new thermal-fluidic systems, and device modeling and characterization.

Contact: Michael Gaitan, 301-975-2070

Reliability of Integrated Circuit Dielectric Films

Aggressive scaling of gate oxide thickness used in silicon integrated circuits necessitates the understanding of the physical mechanisms responsible for dielectric degradation and breakdown. We are particularly concerned with the reliability of ultra-thin gate oxides that are in the direct tunneling regime during circuit operation. Research focuses on (1) identifying parameters to determine the physics of time-dependent dielectric breakdown of ultra-thin dielectric films in the tunneling regime; (2) determining the effectiveness of highly accelerated stress tests to predict long-term reliability of thin dielectric films; (3) relating analytical characterization of oxide bulk and interfaces to electrical behavior; (4) identifying and controlling fabrication process parameters that affect intrinsic and extrinsic failure modes; and (5) characterizing and evaluating alternate dielectrics for use as substitutes for silicon oxide in advanced circuit technologies.

Contact: John S. Suehle, 301-975-2247

Physical and Electrical Properties of Thin Dielectric Films

It is becoming difficult to characterize ultrathin gate dielectric films (typically less than 5 nm) used in MOS devices because technology is driving them thinner. We are developing electrical test methods (using conventional techniques such as I-V and C-V, as well as low-temperature magnetotransport techniques) to measure the physical properties (e.g., film thickness and permittivity) of such films.

Electrical results are compared with those of optical and other measurement methods, and physical models are developed to be effective for more than one measurement technique. The interface between the dielectric film and the silicon substrate is critical to understanding these measurements. We are also developing techniques to characterize buried interfaces (i.e., interface roughness) and are determining how the interface and physical properties affect device performance and reliability.

Contact: Curt A. Richter, 301-975-2082

In-Situ and Real-Time Thin-Film Metrology and Material Process Control

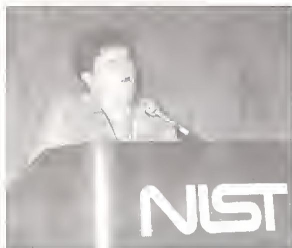
To improve reliability and throughput, integrated circuit device fabrication techniques require rigorous control of material growth and deposition. In-situ measurements and methods are seen as effective tools for such a requirement. We have set up a sophisticated, flexible ultrahigh vacuum system to investigate the various in-situ metrology techniques and to apply these techniques to real thin-film fabrication processes. At this early stage, research focuses on producing an accurate optical database for semiconductor materials and thin films at room and higher temperatures. The metrology techniques of interest are mostly optical probes including spectroscopic ellipsometry, light scattering, and vapor deposition and plasma processes. Opportunities exist for proposals that center on instrumentation, thin-film fabrication, and characterization. Various ex-situ material characterization techniques are also available in collaboration with other projects in this Division.

Contact: Nhan V. Nguyen, 301-975-2044

Measurement Traceability for Thin Dielectric Films

The development and fabrication of ultrathin, increasingly sophisticated gate dielectrics is a key technology for integrated circuits at the 0.25 micrometer feature size and beyond. With the use of single-wavelength and spectroscopic ellipsometry, thin dielectric films are characterized for use in the calibration of instruments to monitor and control gate dielectric fabrication. Research involves the development of physical standards and supporting methodologies that will provide traceability to NIST for advanced gate dielectrics. Input from various physical, optical, and electrical techniques is needed to improve our knowledge of the structure and composition of advanced dielectrics and their interfaces for correct interpretation of ellipsometric measurements. Research will focus on relating the analyses of XTEM, surface second harmonic generation, scanning probe methods, X-ray reflectance, and various electrical techniques to improve our understanding of the structure of thin dielectric films, which would strengthen and extend NIST's capability for providing thin dielectric measurement traceability.

Contact: Curt A. Richter, 301-975-2082, or Nhan V. Nguyen, 301-975-2044



Karen Brown, Deputy Director of NIST, opened the Conference with a brief overview of NIST.

"Semiconductor metrology is becoming increasingly critical, and I think that this workshop is an excellent, excellent opportunity for us to learn from each other"

Karen Brown, Deputy Director of NIST, at the 2000 International Conference on Characterization and Metrology for ULSI Technology

"Metrology challenges facing the semiconductor industry will spur rapid growth and research in the sector ... New metrology approaches discussed at the event may offer solutions for an industry confronting the deadlines and the red roadblock imposed by the International Technology Roadmap for Semiconductors."

Micro, September 2000, on the 2000 International Conference on Characterization and Metrology for ULSI Technology

2000 Semiconductor Metrology Conference at NIST Draws World's Metrology Experts

The 2000 International Conference on Characterization and Metrology for ULSI Technology was hosted by NIST from June 26-29, 2000. The Conference is the third in a series; the first was held at NIST in 1995 and the second in 1998. The 2000 Conference was highly successful, bringing in over 235 attendees from the United States, the Netherlands, Belgium, France, Spain, Germany, Switzerland, Israel, Korea, China, Japan, and Taiwan. Forty invited talks were presented, nearly 100 poster papers were displayed, and a panel was hosted to summarize key issues emerging from the Conference. Conference attendees gave overwhelmingly favorable reviews of the conference, stating that it contained "top quality talks," the "technical quality was excellent," and "each conference gets better."

Dennis Buss, Vice-President of Mixed-Signal Technology, Texas Instruments.

In addition to the Semiconductor Electronics Division (SED) and the National Semiconductor Metrology Program of NIST, sponsors included International Semiconductor Manufacturing Technology (SEMATECH); National Science Foundation; American Vacuum Society, Manufacturing Science and Technology Technical Group; Semiconductor Equipment and Materials International (SEMI); American Physical Society, Forum for Industrial and Applied Physics; The Electrochemical Society; and the Semiconductor Research Corporation. Additional sponsors for poster sessions were Applied Materials; Boxer Cross; Charles Evans and Associates; Digital Instruments, Veeco Metrology Group; Dupont Photomasks, Inc.; KLA Tencor; MEMC Electronic Materials, Inc.; Rudolph Technologies, Inc.; SensArray; and Solid State Measurements.

Kenneth L. Schroeder, President and Chief Executive Officer, KLA-Tencor.

Under the leadership of David G. Seiler, the SED Division Chief, and with the support of Tom Shaffner, Leader of the Materials Technology Group, the Conference Committee organized the Conference to provide extensive coverage of metrology and characterization methods. Perspectives on industrial metrology requirements were highlighted as well as a review of the 1999 International Technology Roadmap for Semiconductors as a benchmark for characterization and metrology needs. Topics for the Conference included challenges, front-end processing, contamination and defect analysis, lithography, interconnect and back-end processing, thin films, and critical analytical techniques. Keynote speakers included Dennis Buss, vice-president and director, Texas Instruments; Kenneth Schroeder, president and CEO, KLA-Tencor; Jaim Nulman, vice-president and general manager for Applied Materials' Factory Efficiency Technology Group; and Alain Diebold, technical manager of Metrology / Yield Management Tools at International SEMATECH.

The Conference Proceedings, entitled *Characterization and Metrology for ULSI Technology: 2000* will be available in Spring 2001 from American Institute of Physics (AIP). To order, please contact orders@springer-ny.com or visit the AIP Web site at http://www.aip.org/catalog/cpreq_form.html

Science Magazine Recommends Division Hall Effect Measurements Web Site as "Hot Pick"

In the July 21, 2000, issue of *Science* Magazine, the Division's new Hall Effect Measurements Web site was recommended as a "Hot Pick" in the magazine's "NetWatch" section. This new Web site can be accessed at www.eeel.nist.gov/812/hall.html.

The Semiconductor Electronics Division (SED) prepared the Hall Effect Measurements Web site to address an identified gap in the metrology of semiconductor materials. It projects a simple tutorial style, with fundamental equations and concepts relevant to the practicing industrial engineer, and includes worksheets and references for data acquisition and reduction. To encourage user participation and to increase awareness of the technique, an electronic bulletin board is also included, where those interested in the methodology can exchange ideas and information.

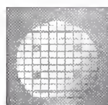
The site also responds to a need expressed during the last National Research Council (NRC) panel review of SED programs to leverage the Internet for dissemination of technical information. The Web site is managed by the Division's Bob Thurber.

Over a century ago, Edwin Hall discovered that a small transverse voltage appears across a current-carrying thin metal strip in an applied magnetic field. Today, this effect bears his name (the Hall effect), and has since evolved in the form of an indispensable characterization tool, capable of determining the density and mobility of free carrier electrons and holes in semiconductor materials and devices. The broad acceptance of the technique in both academic and industrial laboratories is attributed to its simplicity, low cost, and minimal time required for analysis. In spite of such a key role, only a single ASTM document (ASTM F-76) was previously available for outlining standard procedures and practices for the Hall measurement of semiconducting materials.

The appearance of modern equipment and new engineering graduates in industrial laboratories has opened this opportunity for a more readily available and user-friendly presentation of the Hall effect, which encompasses simple theory, modern equipment, and measurement practices. This was one of the major findings of Dr. Rode's (Pendragon Corporation) recent survey of industrial users, and was identified as an important gap in the industrial metrology roadmap he formulated for our SED project in compound semiconductor materials.

"Wow! What a terrific site. Thanks for all the work you did putting this great resource together."

Andrew Jackson, Cielo Communications



Hall Effect Measurements

Contents

I. Introduction

II. The Hall Effect

- Evolution of Resistance Concepts
- The Hall Effect and the Lorentz Force
- The van der Pauw Technique

III. Resistivity and Hall Measurements

- Sample Geometry
- Definitions for Resistivity Measurements
- Resistivity Measurements
- Resistivity Calculations
- Definitions for Hall Measurements
- Hall Measurements
- Hall Calculations

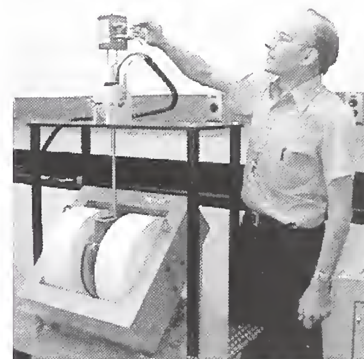
IV. Hall Worksheet and Algorithm Example

- Sample Hall Worksheet
- Worksheet with Typical Data
- Algorithm Example

V. References

VI. Bulletin Board

- Leave or View Comments!



The Materials and Technology Group's Bob Thurber connecting cables to the sample holder for a Hall effect measurement.

Screen capture from the Hall Effect Measurements Web site (www.eeel.nist.gov/812/hall.html)

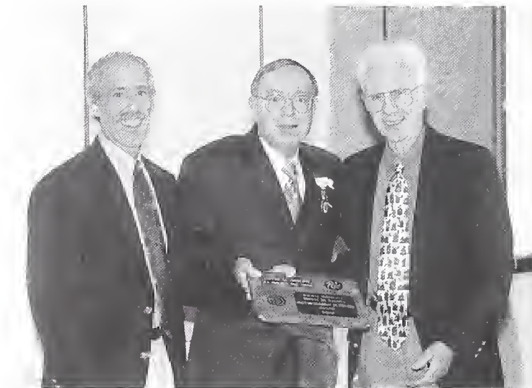
Seiler Receives Distinguished Alumnus Award for Semiconductor Physics Leadership

"(Dr. Seiler's) leadership role in the study of semiconductors has led to penetrating insights into their band structures through the observation of remarkable inversion asymmetry splittings and warping effects."

Professor Andrew Hirsch, Purdue University

On April 28, 2000, David G. Seiler was awarded a Purdue University School of Science Distinguished Alumnus Award. Harry Morrison, the Dean of Science at Purdue University, nominated Dr. Seiler for the award, stating that "he is recognized internationally as a leader in the field of narrow gap semiconductors." Dr. Seiler, Morrison concluded, "has made some of (the) most important and innovative contributions to semiconductor physics."

With this award, Purdue's School of Science recognizes its graduates whose outstanding achievements in professional and related fields of endeavor merit particular distinction. The award consists of a plaque, which was presented to Dr. Seiler at a banquet on the evening of April 28, 2000. In addition, Dr. Seiler's name and picture will be added to a permanent Distinguished Alumni display located in the School of Science.



David Seiler (middle) displays his plaque with Professor Andy Hirsch, chair of Purdue's Physics Department (left) and Dr. William M. Becker, Seiler's major professor at Purdue (right).

David G. Seiler is the Chief of the Semiconductor Electronics Division in the Electronics and Electrical Engineering Laboratory at the National Institute of Standards and Technology (NIST) in Gaithersburg, Maryland. Dr. Seiler received his Ph. D. and M.S. Degrees in Physics from Purdue University and a B.S. in Physics from Case Western Reserve University. He is a Fellow of the American Physical Society and a Senior Member of the Institute of Electrical and Electronic Engineers (IEEE). Over the past 36 years, Dr. Seiler has developed an extensive research background in many areas of semiconductor physics. He has worked with the characterization of the electrical, optical, and nonlinear optical properties of numerous semiconductors and artificially structured materials, concentrating on quantum transport effects, two-photon absorption spectroscopy, and magneto-optical effects. His current focus is on understanding and advancing the metrology and characterization measurements needed by the semiconductor industry. The results of his research have been disseminated in over 200 publications and 100 talks throughout the world.

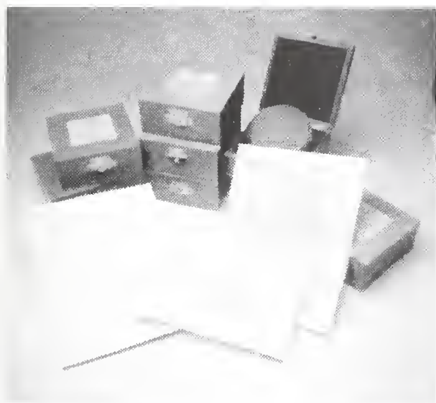
David Seiler (middle) interacts with James G. Mullen (left) and Anant Ramdas (right) during a reception at the Physics Department at Purdue University.

Dr. Seiler's current leadership activities include serving on the executive committee of the Manufacturing Science and Technology Group of the American Vacuum Society. He was also recently elected to serve as vice-chair of the Instrument and Measurement Science Topical Group of the American Physics Society.

Prior to joining NIST in 1988, Dr. Seiler served as a Solid State Physics Program Director in the Materials Research Division at the National Science Foundation, spent a year's sabbatical at the MIT Francis Bitter National Magnet Laboratory, and had been a Regents Professor of Physics at the University of North Texas. Prior to becoming Division Chief, he served as the Materials Technology Group Leader in the Division and as a Program Analyst in the Program Office for the Director of NIST.

Bronze Medal Awarded for Vital Resistivity SRMs for Semiconductor Industry

James Ehrstein, Project Leader of the Thin-Film Process Metrology Project in the Semiconductor Electronics Division, received the Bronze Medal Award for superior federal service for the second time in his career at NIST. Dr. Ehrstein was cited for developing artifact standards and associated test methods that provide the base for resistivity measurements in the U.S. semiconductor industry. Ehrstein was recognized for the award during the 27th Annual Awards Ceremony, held on December 1, 1999, at NIST, Gaithersburg.



Various NIST Standard Reference Materials for resistivity displayed with certificates.

Resistivity is the most important parameter for specifying silicon starting and epi materials, and determining the resistivity of wafers is an important concern to the multibillion-dollar semiconductor industry. Ehrstein has spearheaded the research, development, production, and delivery of resistivity Standard Reference Materials (SRMs), including a recent new series of standards. These SRMs are used by all U.S. manufacturers as a basis for specifying the quality and properties of silicon materials. Ehrstein's work has led to the sales of more than 2,300 SRM units to more than 250 companies worldwide. The SRMs that Ehrstein has been responsible for providing are used for the calibration and performance verification of reference instruments, commonly four-point probes and eddy-current testers for substrate resistivity, epi/implant sheet resistance, and depth profiling by spreading resistance, and generally through secondary standards for the calibration of instruments on the fabrication line.

Under Ehrstein's guidance, seven new silicon resistivity SRMs have recently been released for sale. These respond to industry's request for reduced uncertainty and a configuration more appropriate for modern instrumentation. Ehrstein's extension of four-point probe methodology and elaborate experimental control procedures resulted in unprecedented 2 sigma uncertainties that will enable manufacturers and users to calibrate resistivity test instruments to 0.3 %, or better, with 95 % confidence. This advance cuts resistivity measurement uncertainty by approximately a factor of five and significantly surpasses the accuracy and precision requirements set forth at the 1991 "SEMATECH Workshop on Silicon for Mega-IC Applications."

James Ehrstein received his Ph. D. in Physics from Catholic University of America. Since joining the Semiconductor Electronics Division at NIST, he has worked on the development and improvement of measurement techniques for resistivity, dopant profiling, and dielectric characterization. He initiated the implementation of SRMs within the Division, and has developed or contributed to the development of more than a dozen SRMs for silicon technology. He has been an active contributor to the standardization procedures of ASTM Committee F1 on Electronics, where he is Chairman of the Subcommittee on Silicon Materials and Process Control. He is a member of APS, ECS, and IEEE.

Donnie Ricks of the Thin-Film Process Metrology Project mounting a silicon wafer on the resistivity instrument stage prior to taking measurements for SRM certification.

"Before the July 1997 advance release of J. R. Ehrstein and M. C. Croarkin's NIST special publication 260-131 ...which used ASTM 1529-96 'Sheet Resistance Uniformity Evaluation by In-Line Four Point Probe with the Dual-Configuration Procedure' ... methods for resistivity standards followed the procedures outlined in ASTM F84-93 ... Ehrstein's NIST Special Publication 260-131 changed everything."

The Quarterly Standard, VLSI Standards Incorporated, Technology Update, Volume 3, Issue 2

Three Division Members Receive Bronze Medal for Scanning Capacitance Microscopy

The Bronze Medal Award is the highest honorary recognition available for Institute presentation. The award, approved by the Director, recognizes work that has resulted in more effective and efficient management systems as well as the demonstration of unusual initiative or creative ability in the development and improvement of methods and procedures. It also is given for significant contributions affecting major programs, scientific accomplishment within the Institute, and superior performance of assigned tasks for at least five consectutive years. The award was initiated in 1966.

The team of Mr. Joseph J. Kopanski, Dr. Jay F. Marchiando, and Dr. Brian G. Rennex, all of the Electronics and Electrical Engineering Laboratory's Semiconductor Electronics Division, NIST, was recognized on November 29, 2000, with the Department of Commerce Bronze Medal for greatly accelerating the development of scanning capacitance microscopy (SCM) as a practical measurement tool, now regarded as the instrument of choice for two-dimensional semiconductor dopant profiling. The team helped bring what was a qualitative inspection tool to an instrument capable of measuring quantitative carrier profiles, thereby meeting a critical requirement identified in the International Technology Roadmap for Semiconductors (ITRS). In so doing, the team has worked with instrument manufacturers to develop the tool and developed a complete set of measurement procedures, theoretical models, and data interpretation software.

Background

As semiconductor devices shrink in size, industry needs tools of increasing spatial resolution and sensitivity for looking into the crystal lattice of a fabricated device to determine the distribution of atoms intentionally introduced as part of the fabrication process to tailor the electrical performance characteristics of the device. Both two-dimensional information, for example from a cross section or profile through a junction between two materials having differing electrical characteristics, and three-dimensional information are needed. These doped junction profiles are challenging to measure, because they contain only parts-per-million levels of the electrically active dopants in a highly localized region. Analyzing fabricated devices for advanced design purposes requires precise description of the dopant distribution with spatial resolutions better than 10 nanometers, a target met by the team. The microscope senses capacitance between the doped region and an ultra-sharp tip positioned in close proximity to the surface of the device.

The ITRS identified SCM as a critical-path metrology and in 1993, the Roadmap Association took the extraordinary step of tasking NIST with ownership of the 2-D dopant profiling problem, largely as a result of team leader Kopanski's reputation.

The team was the first to recognize and then demonstrate that SCM capabilities could be added to an existing commercial atomic force microscope (AFM) platform, the breakthrough that ultimately enabled the successful introduction of the tool into over 100 process and research laboratories to date. Previous SCM platforms had limited stability and usefulness. The team's innovations included novel electronics (an ultra-sensitive capacitor sensor with 10^5 high-gain feedback and interface for the existing commercial AFM platform), and an explanation of the fundamental phase differences between the SCM measurements of basic n- and p- conductivity type materials. This work convinced Digital Instruments, the major commercial instrument supplier, to enter into a CRADA with NIST.

(from left to right) Jay Marchiando, Brian Rennex, and Joseph Kopanski.

Recognizing that on-screen pictures of device cross sections may be initially impressive but do not yield quantitative data without rigorous analysis, the team developed both the necessary underlying theory and procedures for data interpretation. The team devised algorithms for rapid image interpretation and provided them to industry and other SCM users in a compact and efficient software suite, *FASTC2D*. The team designed *FASTC2D* to be user friendly through the incorporation of a graphical interface on a desktop PC; extremely fast, requiring only a few seconds for calculation; and highly accurate, by condensing a first-principles, full 3-D Poisson solver developed by the team. A large U.S.-based semiconductor company has tested the code and reports that it opens new avenues for speeding their transistor model verification.

Harman Receives IEEE Third Millennium Award

George Harman was awarded the Institute of Electrical and Electronics Engineers, Inc. (IEEE) Third Millennium Medal "for outstanding achievements and contributions" in his area of expertise to the IEEE. Other IEEE honors Harman has received during his distinguished career include the Centennial Medal in 1984, the Components, Packaging, and Manufacturing Technology Society (CHMT) Outstanding Contributions Award in 1992, and the Harry Diamond Memorial Award in 1996.

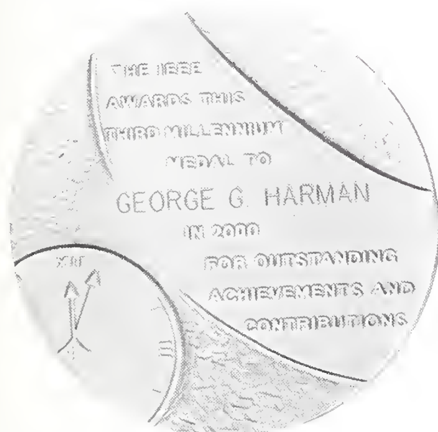
Harman is an internationally-acclaimed expert in the area of wirebonding and packaging of semiconductor chips. He is a Fellow at NIST and a former President of the International Microelectronics And Packaging Society (IMAPS). He is considered to be the world's foremost authority on wire bonding. He presents numerous seminars and short courses on wire bonding, packaging reliability, and acoustic emission testing in electronics. His book, *Wire Bonding in Microelectronics, second edition* (McGraw Hill, 1997), is considered to be the "bible" in terms of wire-bonding information. He is a Fellow of the IEEE and IMAPS, and has received numerous domestic and foreign awards and recognition.

Harman is currently working on wirebonding to advanced copper/Lo-κ chips and measurements of temperature during wirebonding.

George G. Harman, NIST Fellow, the Semiconductor Electronics Division, NIST

"Not since the 1984 IEEE Centennial Medal has the IEEE given an Institute-wide award to honor such a select and special group of members. Now the IEEE will mark the end of one millennium and the beginning of another with such an award. The Third Millennium Medals will honor ... outstanding members ... The criteria for members to be named a Third Millenium Medal recipient includes outstanding contributions to a section, community, chapter, area of technology or outstanding contributions to their board."

IEEE's The Institute, July 1999



The Third Millennium Award was presented to George Harman "for outstanding achievements and contributions" to the IEEE.

NIST's Gaithersburg Campus and Surrounding Area

NIST MISSION -

To strengthen the U.S. economy and improve the quality of life by working with industry to develop and apply technology, measurements, and standards.

NIST VISION -

To provide U.S. industry with the world's best technical infrastructure and return the best possible value to the economy and society.

"Washington is located in a region that is rich in historic lore and natural beauty. From the bustling sounds of a Chesapeake Bay harbor to the utter stillness of a Blue Ridge mountaintop, from the small, old tobacco farms of southern Maryland to the grand estates of Virginia's hunt country, you will find a richness of scenery and history."

"Welcome to Washington" brochure, National Park Service, U.S. Department of the Interior

About NIST

The National Institute of Standards and Technology (NIST) is an agency of the U.S. Department of Commerce's Technology Administration. NIST was established in 1901 by Congress "to assist industry in the development of technology ... needed to improve product quality, to modernize manufacturing processes, to ensure product reliability ... and to facilitate rapid commercialization ... of products based on new scientific discoveries."

Location

Located approximately 25 miles Northwest of Washington, D.C., on a 234-hectare campus, NIST Gaithersburg offers the advantages of being in close proximity to government offices, while maintaining the seclusion of a rural setting. The site is beautifully landscaped and features mature trees and ponds as well as a herd of white-tailed deer and Canada geese. Walking paths and picnic areas provide easy and pleasant access for outdoor repasts, biking, walking, and jogging. The campus is also easily accessible, offering a shuttle service to a nearby metro (subway) station and being located near three major airports.

NIST's 11-story Administration Building.

Staff

NIST's staff is comprised of about 3,300 scientists, engineers, technicians, business specialists, and administrative personnel. About 1,500 visiting researchers complement the staff. In addition, NIST partners with 2,000 manufacturing specialists and staff at affiliated centers around the country.

Some Nearby Attractions

Landmarks

Arlington National Cemetery
Bureau of Engraving and Printing
Capitol Building
Daughters of the American Revolution
Ford's Theater
Franklin Delano Roosevelt Memorial
I.R.S. Building
J. Edgar Hoover F.B.I. Building
Jefferson Memorial
Library of Congress
Lincoln Memorial
National Archives
National Mall
Supreme Court
Union Station
Vietnam Veterans Memorial
Washington Monument
White House

The NIST Gaithersburg campus is home to many different types of wildlife.

Museums and Other Attractions

Capital Children's Museum
Corcoran Gallery
Kennedy Center
MCI Center
National Geographic Society
National Sports Gallery
National Theater
Smithsonian Institute
United States Holocaust Memorial Museum
Washington D.C. Convention Center

Outdoor Attractions

Antietam National Battlefield Site
Catoctin Mountain Park
C&O Canal National Historical Park
Clara Barton National Historic Site
Eisenhower National Historic Site
Fort McHenry
Fort Washington
Gettysburg National Military Park
Glen Echo Park
Great Falls Park
Greenbelt Park
Mount Vernon
Oxon Hill Farm
Prince William Forest Park
Rock Creek Park
Shenandoah National Park
Wolf Trap Farm Park for the Performing Arts

January 2001

For additional information contact:
Telephone: (301) 975-2054
Facsimile: (301) 975-6021
On the Web: http://www.eeel.nist.gov/812/