NISTIR 6522

Silicon Microelectronics Programs at the National Institute of Standards and Technology

Programs, Activities, and Accomplishments

Edited by
Joaquin V. Martinez de Pinillos,
Stephen Knight,
and Alice Settle-Raskin

Office of Microelectronics Programs

June 2000

NIST
National Institute of Standards and Technology
Technology Administration, U.S. Department of Commerce

Cover Picture Captions (left to right):

Picture 1.

Silicon and Oxygen are the most abundant elements on the surface of the earth. When combined chemically, they form quartz—in fine form, sand.

Picture 2.

Purified single crystal silicon is the underlying material supporting the silicon integrated circuit industry, a major technology driver in today's modern economies (photo of silicon ingot courtesy of MEMC).

Picture 3.

Silicon integrated circuits—active transistor switches and amplifiers, passive components, and many layers of dense interconnecting wiring—are formed by complex processing on silicon wafers (photo of silicon integrated circuit wafer courtesy of Austria Mikro System International AG).

Pictures 4 and 5.

Metrology is critical to the successful processing of silicon into integrated circuits. Two examples are: The image of a critical dimensional artifact obtained with a calibrated atomic force microscope (CAFM) (Picture 4); and an X-ray tomograph of a wiring interconnect picture (Picture 5). Both projects underway at NIST are among those described in this document.

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U.S. DEPARTMENT OF COMMERCE
William M. Daley, Secretary

Technology Administration
Dr. Cheryl L. Shavers, Under Secretary of Commerce for Technology

National Institute of Standards and Technology
Raymond G. Kammer, Director

Disclaimer: Certain commercial equipment and/or software are identified in this report to adequately describe the experimental procedure. Such identification does not imply recommendation or endorsement by the National Institute of Standards and Technology, nor does it imply that the equipment and/or software identified is necessarily the best available for the purpose.

References: References made to the *International Technology Roadmap for Semiconductors* (ITRS) apply to the most recent edition, dated 1999. This document is available from the Semiconductor Industry Association (SIA), 181 Metro Drive, Suite 450, San Jose, CA 95110, phone: (408) 436-6600, fax: (408) 436-6646.

Appendices: The reader will notice that there are acronyms and abbreviations throughout this document that are not spelled out due to space limitations. To enable the reader to learn more about the these acronyms and abbrevations, we have included an appendix toward the back including an acronyms/abbreviations list. We have also included a list of the NISMP projects which demonstrates the synergism resulting through this matrix-managed program.

Contents

Appendices

Welcome

The microelectronics industry is a driving force fueling the U. S. economy, leading to rapid improvements in productivity, and enabling other new high technology growth industries such as electronic commerce and biotechnology. The National Institute of Standards and Technology, NIST, in fulfilling its mission of strengthening the U. S. economy and improving the quality of life by working with industry to develop and apply technology, measurements and standards, is devoting considerable effort supporting the semiconductor industry and its infrastructure. This document describes the many projects being conducted at NIST that constitute that effort.

The first metrology development activities at NIST, then called the National Bureau of Standards, in support of the semiconductor manufacturing industry began when the industry was in its infancy. As the industry grew and matured the number of projects expanded rapidly. In 1968, a division was formed expressly to address semiconductor metrology issues. Now the breadth of skills required to address semiconductor manufacturing metrology issues encompasses all of the laboratories at NIST. To address the coordinated response to industry needs, Congress established the National Semiconductor Metrology Program (NSMP) in 1994. Matrix managed by the Office of Microelectronics Programs, the NSMP is currently funded at $12M annually[1], and is forty projects in six of the seven laboratories at NIST. Most, but not all, of the projects described in this document, are partially funded by NSMP. Additional funding comes from the Advanced Technology Program intramural funding, from the laboratories themselves, from other agencies, and from Cooperative Research and Development Agreements (CRADAs) with industry.

Industry Metrology Needs

Meeting the metrology needs of the industry is a real challenge because the industry tends to outstrip its metrology capability quickly. For decades the industry has doubled its productivity every eighteen months, and this trend is likely to continue for some time. What makes it possible? Continuous improvements in semiconductor processing – such as using ever shorter optical wavelengths to achieve higher circuit densities, using ever larger diameter wafers to achieve greater economies of scale, increasing the ways that sensors are used to monitor and control chemical and physical processes, and by introducing new process materials into the mix.

NIST's Metrology Contributions – Paving the Way

Outcomes from the NSMP which have been of critical importance to the industry include standard reference materials (SRMs®), "NIST-traceable" reference materials (NTRMs®), chemical and plasma reaction kinetics, sensor and instrument calibration techniques, and new metrology techniques. Examples which are used extensively by the semiconductor industry include: NIST SRMs® for bulk resistivity of silicon covering over four orders of magnitude in resistivity; NIST SRMs® calibrated diameter small particles relevant to semiconductor manufacturing; NIST SRMs ® for thin silicon dioxide dielectrics are enabling industry to create larger diameter "NIST-traceable" dielectric film reference materials; chemical and plasma reaction kinetics for chemical species used in semiconductor processing have been and are being published; calibration techniques and calibration services for residual gas analyzers and gas flow meters; data for inert and reactive process gases; a calibration instrument and technique for measuring water vapor in the parts per billion range; techniques for measuring physical and electrical properties of interconnect materials; and techniques and modeling software to extend critical dimension measurements down to the ever-shrinking dimensions of

[1] The ultimate funding level established by Congress is $25M annually.

integrated circuit structures. *In short, critical metrology technology developments extend across all the myriad of disciplines required for the semiconductor industry.*

Fostering NIST's Relationships with the Industry

NIST's relationships with the Semiconductor Industry Association (SIA), SEMATECH, and the Semiconductor Research Corporation (SRC) are also managed through the Office of Microelectronics Programs (OMP). Staff from OMP represent NIST on the SIA committees that develop the National Technology Roadmap for Semiconductors as well as on numerous SRC technical management committees. OMP staff also act on behalf of NIST in the semiconductor standards development work of the American Society for Testing and Materials (ASTM), the Deutsches Institut für Normung (DIN), the Electronic Industries Association (EIA), the International Organization for Standardization (ISO), and the Semiconductor Equipment and Materials International (SEMI).

Learn More about Semiconductor Metrology at NIST

This booklet was prepared to help you learn more about the 49 metrology projects for the silicon semiconductor manufacturing industry at NIST. In all, they NIST's effort to meet the highest-priority measurement needs of the silicon semiconductor industry. You will see the direct correlation between the gaps in technology expressed in the 1999 International Technology Roadmap for Semiconductors and other authoritative industry sources and the focus of the program at NIST. It demonstrates NIST's ability to listen to the needs of the industry and respond with the measurement means to solve the problems. For further information let us know your specific questions, needs or concerns, please use any one of the following means to reach us:

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Projects

Nanometer-Scale Dimensional Metrology with SEM and Scanned Probe Techniques

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Funding Sources:
NIST OMP/NSMP
Other Agency

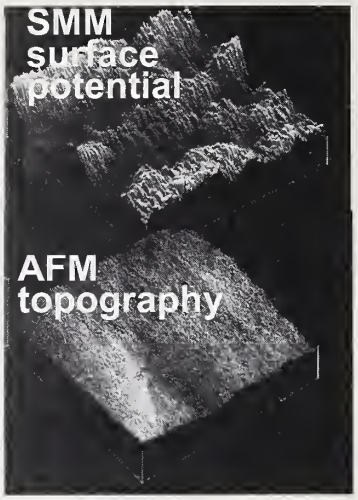
Project Goals

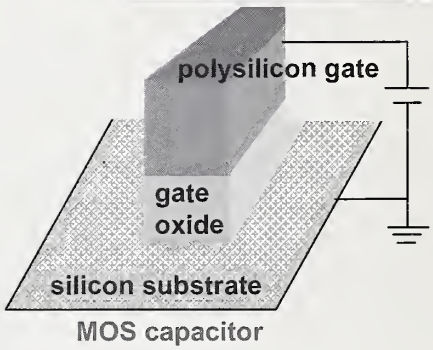
Improve the measurement uncertainty of scanning electron microscope-based, critical-dimension measurements in the semiconductor industry.

Customer Needs

Metrology is mentioned throughout the Lithography chapter of the 1999 SIA ITRS. Requirements are defined on page 298, Table 82a. Potential solutions are on page 301, Figure 59. Critical dimension metrology is cited as one of the grand challenges on page 21, Table M.

The SEM is the current tool of choice for inspection and metrology of sub-micrometer features in the semiconductor industry. Scanned probe microscopes, SPMs, possess unique capabilities which may significantly enhance the performance of SEMs for in-line CD measurements. A creative strategy, which successfully harnesses the strong points of both techniques to reduce the measurement uncertainty of sub-micrometer features while minimizing their limitations, will help NIST meet the expectations of the semiconductor industry expressed in the 1999 SIA ITRS.





Comparison of the topographical and electrical homogeneity of a polysilicon gate using atomic force microscopy (AFM) and Scanning Maxwell-stress Microscopy (SMM).

Technical Strategy

Combined SEM and SPM instrumentation and analysis. Although SEM instruments are capable of high-precision lateral measurements, modeling of intensity profiles is required in order to obtain a reliable estimate of the height of semiconductor test structures. This is because an SEM electron beam penetrates the sample under inspection differently depending upon the materials and local structural environment of a feature. Because of the sophisticated nature of the calculations, it has proven difficult to implement such modeling into practical calibration situations. On the other hand, SPM instruments provide excellent height information, with the drawback that the finite tip shape must be deconvoluted from SPM images by modeling in order to get meaningful linewidth information. NIST has, in-house, a combined SEM/SPM system which enables us to obtain images of a test structure with both techniques simultaneously. To derive full benefit from the data flow available from a combined SEM/SPM system, it would be ideal to create a composite dataset which includes the precise SEM lateral

and SPM vertical information only, and excludes the problematic measurement components. Beginning in FY00 the principal investigators started a partnership with a university group to develop a software strategy which permits 3-dimensional image reconstruction and overlay of SEM and SPM datasets. This novel approach offers NIST a powerful method for direct experimental verification of SEM model calculations, consistency checking between SEM and SPM modeling, and a potential real-time imaging strategy.

MILESTONE: Initial efforts employing two NIST standard reference materials, SRM 2090 and SRM 2091, which are currently under development as SEM magnification and sharpness standards, respectively, will be completed and the potential of this software approach will be assessed.

The geometric constraints imposed by the presence of a traditional SPM instrument upon the design and functioning of an SEM stage make a combined SEM/SPM instrument somewhat impractical. These constraints to full SEM operational performance are being addressed by the implementation of a novel force sensor based on a quartz microfabricated tuning fork (TF) sensor. An important issue that we will investigate with this enhanced system is the stability and wear of probe tips. These properties depend on the angular orientation of the probe tip to the surface plane of the sample. Misalignment may expose different crystalline regions of the silicon tip, each of which possesses somewhat different mechanical and chemical resistance when in contact with sample material.

MILESTONE: During FY00 benchtop operation of the TF sensor on a second SPM will continue and it is anticipated that the modification necessary to transfer this sensor to the SEM/SPM instrument will begin as well.

Polysilicon gate metrology. Local, nanometer-scale electrical characterization of semiconductor test structures can provide an entirely new level of understanding of how the level and types of surface defects in silicon and dielectrics lead to inhomogeneous charging and how a build-up of charge promotes the subsequent growth of hydrocarbon contamination. SPM-based techniques are under development at NIST to obtain simultaneous capacitance and surface potential measurements of active devices.

MILESTONE: Electronics needed to perform the electrical measurements have been procured and an SPM-based system capable of obtaining electrical and materials information for semiconductor test structures and devices will be demonstrated during FY00.

Accomplishments

- Performed simultaneous capacitance, surface potential, and topographic imaging of an electrically active device. Studies include the investigation of SPM cantilever dynamics under oscillating mechanical and electrostatic loads.
- Performed analysis of density variations in SPM oxide nanostructures using high-resolution cross-sectional transmission microscopy.
- Collaborated on the fabrication of a room-temperature single-electron memory device using advanced SPM oxidation techniques. (collaboration with a research group at the Electrotechnical Laboratory, Tsukuba Japan).

FY Deliverables

Demonstrated methods for assembling microfabricated silicon probe tips onto tuning fork (TF) sensors and the dynamics of the assembled structures were evaluated. This work was performed in collaboration with TopoMetrix (Santa Clara CA), John Suehle (SED), and with NT-MDT (Russia).

Completed procurement and initiated testing of the additional electronic components necessary for in-house SPM-based electrical measurements.

Publications

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Nanometer-Scale Dimensional Metrology with Atomic Force Microscopy

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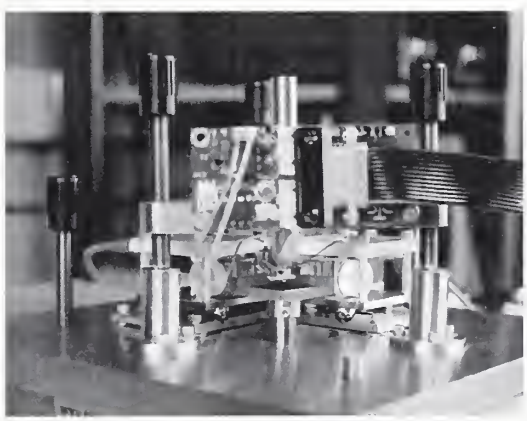
NIST OMP/NSMP
NIST STRS
NIST ATP
CRADA

Project Goals

Provide technological leadership to semiconductor, data storage, and equipment manufacturers and government agencies by developing and evaluating the methods, tools, and artifacts needed to apply atomic force microscopes as dimensional measurement tools in these industries. Presently, NIST has a two element program to extend the understanding of uncertainty sources in AFM dimensional measurements and facilitate the application of AFMs for such measurements. These elements are: (1) the development of a metrology AFM, (2) collaboration and interaction with industrial users, vendors, and academic researchers on metrology applications of commercial instruments. A specific goal is to develop an AFM dimensional calibration service and an appropriate SRM for AFM calibration.



Customer Needs

The 1999 SIA ITRS identifies dimensional metrology as a key enabling technology for the development of next-generation integrated circuits. For example, the goal in 1999 for lines is ± 2.6 nm; this demand tightens to ± 0.4 nm by 2014.

AFMs, which are capable of sub-nanometer resolution, have emerged as important new instruments for semiconductor applications. Among the advantages of AFMs are their ability to image features of almost any material. Measurements commonly performed with AFMs are feature spacing (pitch), feature height (or depth), feature width (critical dimension), and surface roughness. To perform accurate measurements, the scales of an AFM must be calibrated. Traceable standards for sub-micrometer lateral calibration are not yet available.

Technical Strategy

The goal of this program has been the development of a dimensional metrology AFM, called the calibrated atomic force microscope (C-AFM). This research instrument is specifically designed to aid development of suitable AFM standards, and is capable of nanometer-scale dimensional measurements, with metrology traceable to the wavelength of light in all three axes. Its pitch, height, and width measurement capabilities have been evaluated and validated by internal comparisons. They are presently at or near desired performance levels. Pitches ranging up to 20 μm can be measured, using an edge-to-edge measurement method, with uncertainties (1σ) of .1.5 nm at sub-micrometer scale and .0.07 % at the largest scales.

During FY98 we evaluated and distributed a set of silicon step samples, prepared at the University of Maryland, to various industrial collaborators. During FY99, we conducted a preliminary analysis of the data received from the participants. The observed spread was larger than expected, and the reasons for this will be investigated during the further analysis that we will conduct in FY00.

Data sets have been received from the industrial participants. Early analysis indicates a larger than expected spread in the results, underscoring the need to establish uniform procedures for the acquisition and analysis of this type of data.

MILESTONE: ***By 2000, complete analysis of industrial round robin measurements of Si single atom step height.***

Since correction for tip size is a major challenge in width measurements, we have been exploring means to overcome this challenge. Because the influence of the tip shape on the measured width decreases with the size of the tip, the use of very sharp tips such as carbon nanotubes or focused ion beam-milled silicon tips seems promising. We started exploring this during FY99 and will continue in FY00.

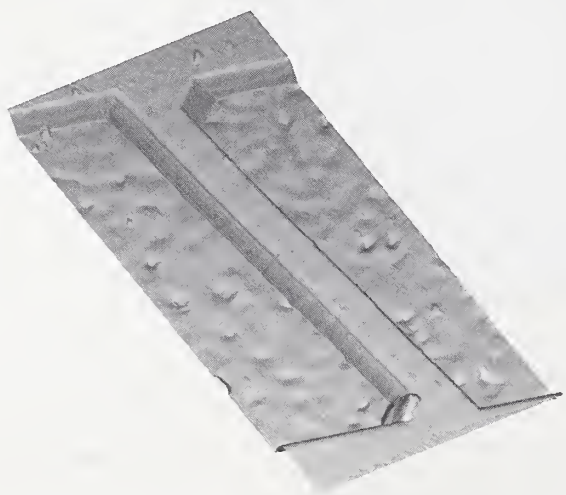
MILESTONE: ***By 2001, demonstrate improved uncertainty for linewidth measurements using sharpened tips.***

The goal of a combined pitch height AFM standard to be measured on the C-AFM is being pursued. During FY00, fabrication of test samples will be performed at the Naval Research Laboratory. If the test samples show adequate surface properties (roughness, uniformity, etc.), then a propotype of SRM 2089 will be fabricated.

MILESTONE: ***By 2002, release SRM 2089, a combined pitch and height standard for AFM.***

The BIPM is sponsoring international measurement comparisons in 1D pitch, 2D pitch, step height, and linewidth. We have already taken data for the 1D comparison, and expect to perform the step height measurements late in FY00. The other comparisons will occur during FY01.

MILESTONE: By 2002, complete participation in four BIPM-sponsored international measurement comparisons.



A SIMOX linewidth sample supplied by R. Allen, M. Cresswell, et al. was measured in the C-AFM. This image is of an 8 micrometer segment of the specimen line.

Accomplishments

- An international, inter-method comparison of step height measurements with PTB was highly successful. On a 20 nm step, the C-AFM achieved a measurement uncertainty of 0.2 nm (k=2), and was in agreement with the PTB result within the combined uncertainty of the measurements. On a 6 nm step, the C-AFM achieved an expanded uncertainty (k=2) of 0.1 nm, also in agreement with the PTB result.

- We completed a new round of C-AFM linewidth measurements on one of the SIMOX samples we had previously obtained from Allen, Cresswell, et al., of the NIST Semiconductor Electronics Division. On a .450 nm line, the C-AFM measurement, combined with blind reconstruction analysis, achieved an expanded uncertainty (k=2) of 13 nm. The result was in agreement with an SEM measurement having a 5 nm expanded uncertainty, and was also in agreement with an electrical resistance determination having a 34 nm expanded uncertainty.

- We completed a new inter-method comparison, using a 90 nm step, between C-AFM step height measurements and the calibrated stylus profiler in our group. There was agreement well within the uncertainties, and the C-AFM expanded measurement uncertainty (k=2) of 0.25 nm was about one third that of the stylus. We are now using this 90 nm step as a new master step height for the stylus facility. This could mean a reduction of up to 50 % in the uncertainties that NIST quotes on stylus step height measurements for external customers. The stylus profilers function as step height comparators, with the master steps being calibrated by some other technique, previously interferometry. The importance of this is largely the fact that many step height measurements in industrial applications will be performed using profilers for the foreseeable future. Profilers are faster and offer larger ranges than many AFMs. Although the C-AFM itself is a step height measuring tool, the NIST profiler facility remains important and has been strengthened by this synergistic interaction with the C-AFM program.

- We completed pitch measurements on two gratings, one having a 700 nm pitch and the other a 300 nm pitch. These gratings are being circulated among the major national metrology institutes as part of a BIPM-sponsored international comparison of one dimensional pitch measurements.

FY Deliverables

Report for External Customer

We completed the first C-AFM step height report for an external customer. On measurements of a 20 nm step we achieved an expanded measurement uncertainty (k=2) of 0.25 nm, and on measurements of a 100 nm step we achieved an expanded uncertainty (k=2) of 0.45 nm.

Publications

Dixson, R., Köning, R., Tsai, V. W., Fu, J., Vorburger, T. V., Dimensional Metrology with the NIST Calibrated Atomic Force Microscope, Proceedings of the SPIE, The International Society for Optical Engineering, *Metrology, Inspection, and Process Control for Microlithography XIII*, Vol. **3677**, 20-34 (1999).

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Scanning Electron Microscope Dimensional Metrology

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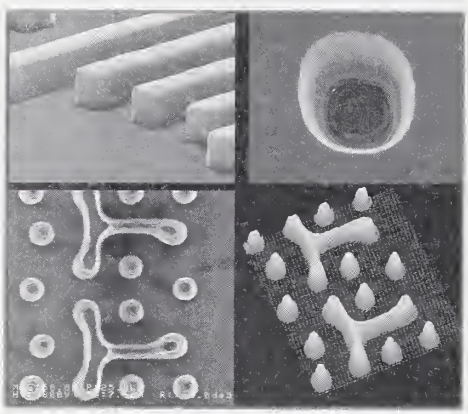
Funding Sources:
NIST OMP/NSMP
Other Agency
SEMATECH

Project Goals

The goal of the SEM Dimensional Metrology Project is to develop high accuracy SEM measurement capability, and the issuance of a set of standard artifacts to be used in manufacturing by the microelectronics industry. These artifacts are relevant to semiconductor wafers processes of 150 nm and smaller structures. This project emphasizes the development of models that can correctly describe and give clear details of image formation in scanning electron microscopes, especially in those that are used in the semiconductor industry. Through the understanding and ability to handle the subtle details of the sample–metrology tool interaction, this effort helps the US industry by fulfilling the stringent requirements of dimensional metrology. Model–based metrology is the path leading to more accurate dimensional metrology than is possible today.



Customer Needs

The semiconductor industry requires fully automatic size and shape measurements of very small, 3–dimensional features. These features are currently 180 nm and smaller in size and the measurements must be done in seconds with an accuracy and precision approaching atomic levels. Currently, specialized SEMs are, and will be for the foreseeable future, used for these measurements. Unfortunately, as SEMATECH and its member companies have determined, the SEM–based dimensional metrology today is not capable to deliver the high–quality, accurate results needed by today's production requirements. But, it is the only tool available which can handle the needed throughput with an acceptable level of precision. One main problem is that the measurements are done with primitive edge criteria. Many times these one–size–fits–all measuring algorithms fail to give satisfactory results on the smallest, so–called critical dimensions (CDs) of transistor gate structures.

The images and line scans taken with CD or laboratory SEMs contain much more information than is generally being used: for example, these images and the individual line scans differ for "same width" resist lines taken at various focus and dose settings. Beyond the fact that this is a source of measurement error, further information can be extracted, like whether or not the given line was exposed with the intended dose and focus. This information is essential in current and future UV lithography. Modeling the possible cases can help to draw correct conclusions and also makes possible the use of more accurate, customized measuring algorithms.

Metrology is mentioned throughout the Lithography Chapter of the 1999 SIA ITRS. Requirements are defined on page 94, Table 28. Potential solutions are on pages 298, Table 82, pages 301-302, Table 83. Metrology is cited as one of the grand challenges on page 10.

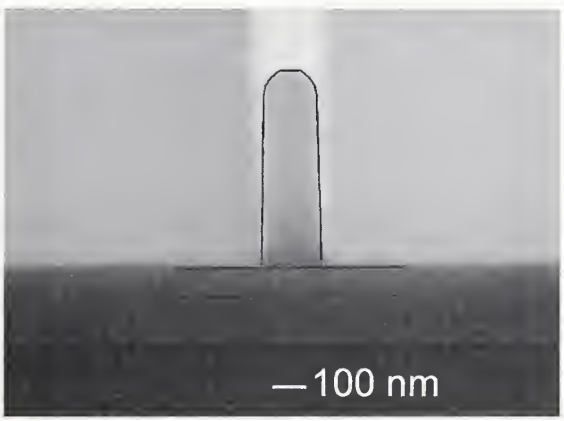
Technical Strategy

Accurate SEM metrology relies both on experimental and theoretical aspects. Experimental work is done with both a high–resolution field emission SEM and a SEM–based metrology instrument with a laser interferometer stage. The theoretical work is based on a new concept called model–based metrology. This concept will ultimately combine five currently developing areas into a single approach. These five areas are:

Adaptive Monte Carlo Modeling. Adaptive Monte Carlo modeling utilizes a database of measured video waveforms from production samples and compares it to a library of modeled waveforms;

- **Modeling/Image Simulation.** The various new Monte Carlo methods, especially those developed at NIST (MONSEL Series), are providing better and more accurate data than ever. The modeled results are very closely matching the results of real measurements;
- **Specimen Charging Modeling.** SEMATECH and the Advanced Metrology Advisory Group (AMAG) has identified charging as the biggest problem in accurate SEM–based metrology and the successful modeling of the geometry of real integrated circuits;
- **Signal Path Modeling.** The modeling of the signal path, including the electronics and signal processing of the SEMs remains a fertile area of research and is critical to the successful development of an accurate model; and
- **Algorithm Development and Analysis.** Algorithms currently used in metrology instruments have no statistical basis for analysis of the data.

MILESTONE: Issuance of standard artifact SRM 2091 and evaluation procedure suitable for correctly measuring image sharpness of scanning electron microscopes, especially of those that are used in the semiconductor industry by the end of FY2000. Completion of the current SEMATECH high accuracy SEM metrology contract during FY 2000.



Cross sectional view of a resist line overlaid with the structure calculated from top–down view of the line by Adaptive Monte Carlo Modeling.

Accomplishments

- The SEM Metrology Program was awarded a Department of Commerce Silver Medal for the joint development of SEM Monitor.
- The SEM Metrology Program was awarded an **R&D 100** for the joint development of SEM Monitor with Hewlett–Packard and SPECTEL Co.
- The video/CD "Telepresence – You don't have to be there" received the Communicator Award of Excellence.
- A Hitachi critical dimension SEM, donated by Texas Instruments, was installed and made operational.
- The new International SEMATECH contract on high–accuracy SEM Metrology was continued with modeling improvements, Spectel Co. collaborations and research into low–loss electron detection.
- The Line Width Correlation Project obtained agreement between SEM, AFM, and electrical line width measurements on a defined single crystal semiconductor line structure, published the results, and presented them at SPIE.

FY Deliverables

- Issuance of standard artifact SRM 2091
- Completion of the current SEMATECH contract.

Publications

Archie, C., Lowney, J. and Postek M. T., Modeling and Experimental Aspects of Apparent Beam Width as a Resolution Measure. Proceedings of the SPIE , The International Society for Optical Engineering, *Metrology, Inspection, and Process Control for Microlithography XIII , Vol.* **3677**, 669–685 (1999).

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Linewidth Correlation

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Funding Sources:
NIST OMP/NSMP
Other Agency
International SEMATECH

Project Goals

The goal of the Linewidth Correlation project is to improve linewidth measurement capabilities within NIST and in the semiconductor industry through comparative experiments among practitioners of different measurement techniques such as scanning electron, optical, scanned probe and electrical metrologies.

Customer Needs

NIST is responsible for providing linewidth SRM's and/or calibration services to meet the needs of U.S. industry. Presently, our only linewidth standards are optical photomask standards, the minimum linewidth of which is 0.5 μm with a total uncertainty of .37 nm 2σ. By 2002, the semiconductor industry wants to manufacture 130 nm gates with better than 10 nm control. Of this, 2 nm have been budgeted for metrology precision. The magnetic recording and photographic industries have gap width and grain size measurement requirements also below a micrometer. Neither NIST nor other national laboratories presently offer a linewidth measurement service or SRM with this level of accuracy.

Physical linewidth determination with any microscopic technique requires modeling of the probe/sample interaction in order to identify edge locations. Barriers to accurate linewidth determination include inadequate confidence in existing models, the complexity and consequent expense of using some models, inadequately quantified methods divergence, and ignorance of best measurement practices.

Metrology is mentioned throughout the Lithography Chapter of the 1999 SIA ITRS. Requirements are defined on page 94, Table 28. Potential solutions are on pages 298, Table 82, pages 301-302, Table 83. Metrology is cited as one of the grand challenges on page 10.

Technical Strategy

Linewidth measurement capabilities at NIST span several techniques, including optical, SEM, and SPM for physical linewidth as well as electrical techniques to measure the average width of conducting paths. This project is a cooperative interaction among practitioners of the various techniques to exchange information. This cooperation will include information exchange among practitioners of the various methods. It also includes design and eventual execution of experiments for cross-technique comparison of measurements. The scope of the project may include development and improvement of probe-specimen interaction models within the various techniques.

We cooperatively design experiments to measure the same linewidth artifacts by two or more techniques. Experimental design includes all factors relevant to good measurement practice, including sample handling, definition of linewidth for purposes of this experiment, and a manufacturable linewidth artifact or artifacts measurable by multiple techniques.

In the unlikely event that no discrepancies between methods are found, confidence in all of the techniques (including the probe/sample interaction models) will be enhanced. In the more likely event of discrepancies, identification of the sources and remediation will enhance NIST's overall linewidth capabilities. Dissemination of the knowledge will improve industrial linewidth measurement practices as well. Improved measurement practices will be applied to samples that progress naturally from relatively simple geometries and materials, which by limiting the number of variables make it easier to assign the cause of discrepancies, to more complex and industrially relevant geometries and materials, thereby laying the groundwork for an eventual NIST-issued wafer linewidth standard reference material.

MILESTONE: Design polycrystalline linewidth test pattern for SEMATECH AMAG wafer and submit to International SEMATECH. (11/99)

MILESTONE: ***Transfer software for morphological modeling of SPM to International SEMATECH. (11/99)***

MILESTONE: ***Obtain and analyze SEM images of BESOI samples. (1/00) for SEM/ECD intercomparison.***

MILESTONE: ***Completion of WERB review of paper describing experimental test of morphological modeling of SPM tip geometry. (3/00)***

Accomplishments

- Invited book chapter and two invited talks on AFM model methods developed for this project.
- Obtained agreement between SEM, AFM, and ECD for .450 nm Si line, published the results, and presented them at SEMATECH workshops and SPIE.
- Results of linewidth intercomparison were highlighted in SEMI newsletter, *Lithography Review.*
- Completed analysis of experiment to validate SPM model for tip shape reconstruction—achieved detailed agreement with SEM measurement even for complicated tip shape.

FY Deliverables

FY 1999

- Publication of completed intercomparison of CD, SEM and AFM linewidths on SIMOX

FY 2000

- Publication of results of experimental test of morphological modeling of SPM tip geometry.
- Completion of current SEMATECH contract.
- Completion of an intercomparison on a non-SIMOX sample.

Publications

Villarrubia, J. S., Dixson R., Jones, S., Lowney, J. R., Postek, M. T., Allen, R. A., and Cresswell, M. W., Intercomparison of SEM, AFM, and Electrical Linewidths, in *Metrology, Inspection, and Process Control for Microlithography XIII*, Bhanwar Singh, Editor, Vol. **3677**, pp. 587-598 (1999).

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Linewidth and Overlay Standards for Nanometer Metrology

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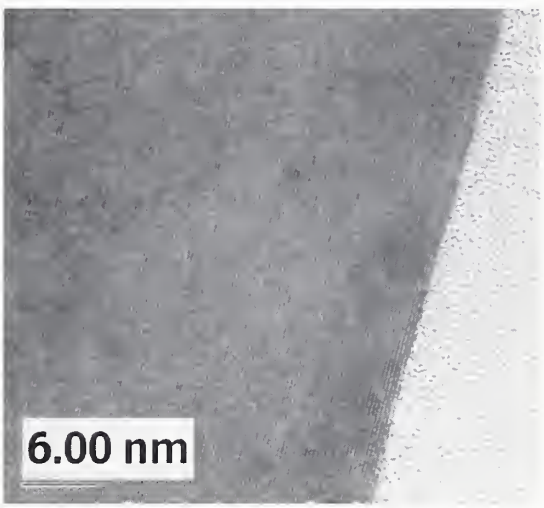
NIST OMP/NSMP
Other Agency
STRS

Project Goals

Develop test-structure-based electrical metrology methods and related reference materials with primary emphasis on overlay and linewidth metrology and calibration; contribute to standards groups supporting the development of a litho-metrology infrastructure for the semiconductor tool industry.



Customer Needs

The 1999 SIA ITRS states that it is critically important to have suitable reference materials for lithography support available when on-wafer measurements are made as a new technology generation in IC manufacturing is introduced, and particularly during development of advanced materials and process tools. Each generation of ICs is characterized by the transistor gate length whose control to specifications during IC fabrication is a primary determinant of manufacturing success. The 1999 SIA ITRS projects a decrease of gate linewidths used in state-of-art IC manufacturing from present levels of up to 350 nm to below 90 nm within several years. SEMs and other systems used for linewidth control exhibit measurement uncertainties exceeding SIA-specified tolerances for these applications. It is widely believed that these uncertainties can be at least partially managed through the use of reference materials with linewidths certified to nanometer-level uncertainties. Until now, such reference materials have been unavailable because the technology needed for their fabrication and certification has not been developed. The accompanying need for certified overlay reference materials is also unserved by any known instrument systems. The problem here is more complex because overlay measurement errors arise from two different sources. The fabrication and certification of reference materials for overlay metrology support must provide for these different sources separately, but as in the case of linewidth metrology, no such reference materials are available. Both overlay and linewidth errors on the wafer may arise from out-of-tolerance feature dimensions printed on the reticle. The best available means of making on-reticle linewidth measurements are subject to excessive instrument-to-instrument variations as well as to unacceptably high uncertainties. Thus, there is a need to reduce the uncertainty of on-reticle linewidth measurements to levels commensurate with the specifications for the features printed on the wafers. It is also widely believed that the usefulness of SEM metrology for monitoring wafers in advanced development and production will become inadequate for some future IC generation. Thus, there exists a need for new techniques that will replace the maturity of SEM systems in the not-too-distant future.

Technical Strategy

The technical strategy that we have developed for fabricating linewidth and overlay reference materials is known as the Single-Crystal Silicon-on-Insulator Reference-Material implementation. Patterning with lattice-plane selective etches of the kind used in silicon micro-machining provides reference features with atomically planar sidewalls. Selection of BESOI starting material with (110) surface orientation that is thermo-mechanically bonded to a (100) handle wafer provides reference-feature-sidewall verticality. Alternatively, (100) surface material generates features with a sloping sidewalls. In both cases, reference features having the unique

attributes of atomically-smooth sidewalls with one of two crystallographically-defined slopes are replicated on a background surface having perfectly uniform and thus highly-desirable photon- and electron-scattering properties. The baseline lithographic strategy features a custom-designed, hybrid optical-electron-beam, metal lift-off process for replicating linewidths as narrow as 0.08 nm.

The traceability path for dimensional certification is provided by HRTEM imaging. This method provides nanometer-level accuracy, but is sample-destructive and prohibitively costly. Our unique traceability strategy thus features the sub-nanometer repeatability of electrical CD metrology as a secondary reference means. Low-cost, whole-wafer electrical measurements are effectively calibrated with local HRTEM lattice-plane image counts. Typical reference features are several-thousand lattice planes wide. HRTEM lattice-plane image counts are achieved by high-density digitization, and numerical differentiation of the photographic record requires 3000 bpi digitization and highly-specialized, but proven image-analysis software. Both Sandia National Laboratories and Los Alamos National Laboratory have provided invaluable assistance in the development of this procedure.

Our technical strategy has to be responsive to industry's requirement for reference materials to have the physical properties of standard 200 mm wafers. Due to constraints in the availability of BESOI starting material, our Single-Crystal Silicon-on-Insulator Reference-Materials are fabricated as test-chips on 150 mm wafers. Each of these wafers is still unacceptably costly to make and certify, particularly in view of the fact that the user needs only a few reference features on each calibration artifact. Therefore, our technical strategy is to dice each 150 mm wafer and mount the separate chips in standard 200 mm wafers micromachined to accommodate the test chips. The result is that finished units are user-ready at an acceptable cost.

We use the Single-Crystal Silicon-on-Insulator technical strategy also for a class of overlay reference materials known as tool-induced shift extractors. The special requirement here is the replication of features with different heights from the same photo-lithographic reticle. We have devised a way of doing this with a unique selection of otherwise standard CMOS fabrication steps. Our tool-induced shift extractors can also be certified using HRTEM imaging. The other class of overlay reference material, known as an edge detector, is made using standard CMOS processing. It can be certified electrically. Preliminary indications are that process-specific, absolute, overlay can be determined to within several nanometers. This is adequate for all foreseeable road-map applications.

The technical strategy for on-reticle linewidth metrology is to extract linewidths of control features electrically from test pads located outside the pellicle, and therefore accessible to both the user and the supplier. These in effect serve as a built-in reference for the calibration of the optical microscopes used by both parties. In this application the < 2 nm repeatability and robustness of electrical metrology is anticipated to have unique advantages, although we have yet to develop a traceability strategy.

MILESTONE: By 2000, fabricate and certify Single-Crystal Silicon-on-Insulator Reference-Materials with linewidths traceable to silicon lattice counts with uncertainties less than 3 nm and that are Y2K compliant.

A key requirement that linewidth reference materials must satisfy is edge-definition sufficient to render width certification as meaningful. Our fabrication and certification strategy complies with this requirement. We have devised a method for fabricating the reference materials with suitable geometries and a method of certifying their widths at an acceptable cost. The next milestone is to perform electrical measurements and HRTEM on the same features and, through their correlation, to establish low-cost electrical linewidth metrology as a secondary reference means for the SOI-BESOI implementation.

MILESTONE: By 2001, demonstrate the fabrication and certification of overlay reference materials with uncertainties below the 5-nm level and extend the technology to pitch reference materials.

The certification of tool-induced shift extractors will require (110) handle wafers and (100) surface wafers, the inverse of that employed for the linewidth reference materials. This approach allows the utilization of HRTEM images of lattice planes for the determination of the pitches of line pairs.

MILESTONE: By 2002, demonstrate electrical CD metrology as a means of providing on-reticle optical calibration.

Accomplishments

- High-resolution transmission electron microscopy has revealed (111) lattice fringes spanning the entire width of a NIST [112] mono-crystalline linewidth reference feature patterned on (110) BESOI material. A preliminary lattice-plane count of the HRTEM image was made by inspection of a photographic print of it through an optical microscope. Use of a drum scanner has demonstrated that the lattice-plane count can be fully automated. The width of the feature was determined to be 580.5 nm. The significance of this result is that the unique benefits of HRTEM imaging for establishing linewidth traceability by lattice-plane counting is made cost effective by configuring the reference feature as the bridge of an electrical linewidth test structure. The unmatched repeatability of electrical measurements is then used in conjunction with the absolute measurements provided by lattice-plane counting to generate an affordable and fully traceable CD reference-material solution.

- Standard 200 mm wafer specifications were micro-machined to serve as reference-material test-chip carriers. The fabrication process features three-step lithography and etching with thermal oxide and low-temperature nitride hard masking. A technique for mounting the reference-material test chips in the carriers was developed. Samples of the carriers were delivered to, and used by, all the major semiconductor manufacturers. The significance of this accomplishment is that state-of-art metrology-systems used for dimensional metrology in semiconductor manufacturing are designed to inspect whole wafers rather than individual test chips. Therefore, there exists a need to incorporate individual test-chip reference artifacts into assemblies which appear as product wafers to the metrology system being calibrated. The new NIST assemblies comply with the dimensional specifications of standard product wafers.

- In collaboration with Photronics Laboratories, Inc., we developed and fabricated electrical linewidth-control features for inspection of photo-mask reticles used in integrated-circuit manufacture. The design allows probe-card access to electrical test pads advantageously located outside the pellicle while uniquely providing for electrical testing of the process-replicated linewidth-control features at the wafer level. The significance is that, as IC critical dimensions continue to shrink, communication between photo-mask suppliers and users is being increasingly challenged by linewidth-control feature metrology. The only practical tool for this task is transmission optical microscopy, which has well-known accuracy limitations. The result has been costly disputes over the actual dimensions of printed test features. The new technique developed by this project effectively locates a length standard into the linewidth control-feature set and allows electrical measurements with several-nanometer-level repeatability to be used for the linewidth traceability path.

- A process for fabricating micro-structures for calibrating optical-overlay metrology tools used in the manufacture of integrated circuits was developed. It features a unique combination of process steps extracted from CMOS processing, SOI, and silicon micro-machining unit-process. These structures have all the properties, such as atomically-planar feature side-walls, geometrical symmetry, material uniformity, and provisions for traceability, that are necessary for monitoring the fabrication of emerging generations of sub-tenth micrometer integrated circuits. A unique fabrication process in which different layers of the micro-structure are imaged at the same time from a single reticle enhances built-in overlay-vector traceability. The significance of this development is that, in overlay metrology, determination of the shift error attributable exclusively to the tool is key to

effective total shift management. The availability of reference materials of the type developed allows an optical overlay microscope to be calibrated for zero tool-induced shift at the several nanometer level.

- A new generation of Single-Crystal Silicon-on-Insulator Reference-Material test chips fabricated on BESOI starting material and having feature linewidths less than 200 nm were delivered to a consortium of eleven integrated-circuit manufacturers for evaluation. The distribution was accompanied by NIST electrical-linewidth measurements for the respective features. The consortium members returned their own measurements. The consortium's measurements track our measurements, in most cases, to within less than 25 nm. A measurement-reconciliation workshop was attended by all the members in September. In addition, a collaboration partner has agreed to conduct a commercial distribution of another 150 test chips to other companies, including the industry's leading metrology-tool manufacturers. The significance of this activity is that it enables IC manufacturers to calibrate their metrology tools to monitor the fabrication of chip generations having linewidths less than 100 nm in accordance with the requirements specified in the 1999 SIA ITRS.

- The effective electrical linewidths of single-crystal linewidth reference features replicated on (100) BESOI substrates were modulated by DC biasing the handle wafer with respect to the cross-bridge resistor in which the reference feature was embedded. Both the sheet resistance and the electrical linewidths of the reference features closely tracked the predictions of theoretical models. While this phenomenon has little known utility in the (110) implementation, in the sloping-sidewall (100) case, it illustrates the potential of developing fully traceable step-height reference materials that can be electrically calibrated. The electrical linewidth measurements made in this work are the first such measurements ever made.

- The use of off-lattice alignment of reference features to enable their replication with linewidths as narrow as 90 nm with a 0.5μm lithography projection aligner was convincingly demonstrated. The baseline process by which we are doing this is a hybrid optical e-beam scheme that is both logistically challenging and costly. The results of this activity may enable the narrower features to be routinely replicated using all-optical standard fabrication process.

- A first set of edge-detector test structures for the development of process-specific reference materials was fabricated using a standard 0.5μm CMOS interconnect process featuring tungsten-plug inter-level vias. Electrical testing has shown that such test structures may be useable as overlay reference materials with uncertainties as low as 10 nm. Such a structure is not currently available, but is in demand by industry.

- Sheet-resistance metrology is of central importance in electrical linewidth metrology. Established methods of sheet-resistance extraction from four-terminal sheet resistors are not generally valid for single-crystal applications because the resistors have non-planar, 3D geometries. Standard 4-point probe measurements are inapplicable because of their lack of spatial resolution. We have devised and tested algorithms for a new means of extracting sheet resistance from V/I measurements made on the three-dimensional four-terminal resistors that are characteristically replicated in single-crystal implementations.

FY Deliverables

Collaborations

Sandia National Labs, Statistical Engineering Division, and Precision Engineering Division, SEMATECH reference artifacts for critical dimension measurements (M. Cresswell, L. Linholm, and R. Allen)

International SEMATECH, development of single-crystal critical dimension reference

materials and development of electrical overlay techniques (M. Cresswell, R. Allen)

International SEMATECH member companies (AMD, Compaq, Conexant, Hewlett-Packard, IBM, Intel, Lucent Technologies, Motorola, Texas Instruments, Hyundai, Infineon Technologies, Philips, STMicroelectronics, TSMC), development of single-crystal critical dimension reference materials (M. Cresswell, R. Allen)

VLSI Standards, Inc.development of single-crystal critical dimension reference materials (M. Cresswell, R. Allen)

Photronics Laboratories, Inc. development of optical/electrical hybrid critical dimension measurement for photomasks (R. Allen, M. Cresswell)

Bio-Rad Semiconductor, evaluation of single-crystal CD structures using scatterometry techniques (R. Allen, M. Cresswell, and L. Linholm)

University of Edinburgh, National Semiconductor Ltd., modeling of current flow in three dimensional Van der Pauw test structures (M. Cresswell, L. Linholm, and R. Allen)

Sandia National Laboratories Microelectronics Development Laboratory, Sandia National Laboratories Compound Semiconductor Research Laboratory, Sandia National Laboratories Integrated Materials Research Laboratory, Los Alamos National Laboratory, NIST Statistical Engineering, Precision Engineering Divisions, and SEMATECH on fabrication and certification of reference materials for linewidth and overlay metrology (M. Cresswell, L. Linholm, and R. Allen)

VLSI Standards, Inc., and SEMATECH, development of commercial architecture and distribution plan for single-crytsal CD reference materials (M. Cresswell, and R. Allen)

Simplex Solutions, Inc., procedures and algorithms for CD extraction from test features having conformal coatings (M. Cresswell)

Standards Committee Participation

SEMI International Standards Microlithography Committee, member, FY 97-99 (R. Allen)

SEMI International Standards Electrical Metrology Test Structures Task Force, Co-Chair, FY 97-99 (R. Allen)

SEMI International Standards, NA Regional Micro-Lithography Committee, Co-chair (M. Cresswell)

SEMI International Standards, Global Microlithography Coordinating Committee (M. Cresswell)

SEMI International Task-Force on X-Ray Lithography Mask Standard, Leader (M. Cresswell)

External Recognition

R. Allen received the U.S. Department of Commerce Bronze Medal Award, December 1998. Citation reads: "For providing reliable measurements on experimental microelectronic test structures in support of NIST consortia, including single-crystal devices."

M. Cresswell received a certificate of appreciation from SEMI International Standards for standards committee and task-force leadership activities.

Publications

Allen, R. A., and Ghoshtagore, R. N., Evaluation of Surface Depletion Effects in Single-Crystal Test Structures for Reference Materials Applications, Proceedings of the 1998

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Cresswell, M. W., Guillaume, N. M. P., Allen, R. A., Guthrie, W. F., Ghoshtagore, R. N., Owen III, J. C., Osborne, Z., Sullivan, N., and Linholm, L. W., Extraction of Sheet-Resistance from Four-Terminal Sheet Resistors in Monocrystalline Films Having Non- Planar Geometries, Trans. Semi. manfactur. 12 (2), pp. 154-165 (May 1999).

Guillaume, N. M. P., Cresswell, M. W., Allen, R. A., Everist, S., and Linholm, L. W., Comparison of Sheet-Resistance Measurements Obtained by Standard and Small-Area Four-Point Probing, Proceedings of the IEEE International Conference on Microelectronics Test Structures, Goteborg, Sweden, March 15-18, 1999, pp. 62-66.

Smith, S., Lindsay, I. A. B., Walton, A. J., Cresswell, M. W., Linholm, L. W., Allen, R. A., Fallon, M., and Gundlach, A. M., Analysis of Current Flow in Mono-Crystalline Electrical Linewidth Structures, Proceedings of the 1999 IEEE International Conference on Microelectronic Test Structures, Goteborg, Sweden, March 15-18, 1999, pp. 7-12.

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Atom-Based Dimensional Metrology

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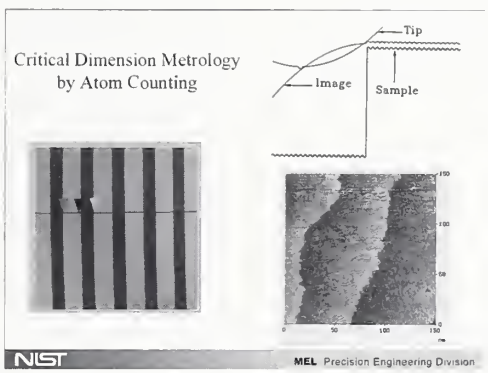
Funding Sources:
NIST OMP/NSMP
Other Agency
NIST STRS

Project Goals

To develop three dimensional structures of controlled geometry whose dimensions can be measured and traced directly to the intrinsic crystal lattice. These samples are intended to be dimensionally stable to allow transfer to other measurement tools which can measure the artifacts with dimensions known on the nanometer scale.



Customer Needs

NIST is responsible to U.S. industry for developing length intensive measurement capabilities and calibration standards in the nanometer scale regime. The new class of scanned probes have unparalleled resolution and offer the most promise for meeting these future needs of the microelectronics industry. One important application of the high resolution SPM methods is in the development of linewidth standards whose dimensions can be measured and traced through the crystal lattice from which they are made.

This project is for the development of atom-based linewidth standards to assist in the calibration of linewidth metrology tools. It is intended to enable the accurate counting of atom spacings across a feature in a controlled environment and to subsequently transfer that artifact to other measuring instruments as a structure with atomically known dimensions. As critical dimensions continue to shrink, the detailed atomic structure, such as edge roughness or sidewall undercut, of the features to be measured occupies a larger portion of the measurement uncertainty. Furthermore, particularly with SEMs, the instrument response and the uncertainty in the edge location within an intensity pattern becomes a significant issue due to the increased sensitivity to detailed elements of the edge detection model. The complexity of these models and large computer resources required for each individual computation make the idea of physical artifacts of known geometry and width essential. This project is intended to develop samples of known geometry and atomic surface structure which will yield measurements resulting in a specific number of atoms across the line feature. These samples will be measured in the UHV environment and then stabilized and subsequently transferred to other instruments.

There are two primary applications of this type of artifact after it has been atomically counted. The first method is the direct calibration in an SEM for a product wafer whose geometry and materials is near to the structure of the atomically counted sample. This method provides a direct calibration of an SEM although this calibration is valid only for the specific materials and geometries of the atomically counted sample. When using this method one cannot obtain a complete instrument calibration directly. However, when used in combination with Monte Carlo simulation models, it will be possible to calibrate the SEM over the entire range of desired parameters with a traceable calibration.

The second method uses an AFM to calibrate the SEMs with the AFM acting as an SEM matching tool. In this method, the AFM is calibrated with an atomically measured sample of the desired geometry as the product wafer to be measured by the SEMs. This sample only needs to have similar geometry to the product wafer but does require similarity in materials due to the insensitivity of an AFM to materials variations.

The AFM, which has been calibrated for a particular geometry by an atomic artifact, can then transfer that calibration to a product wafer of similar geometry and any material such as photo resist, resulting in a calibrated product wafer which can then be transferred to calibrate an SEM. With this technique the AFM is used exclusively in an SEM matching/calibration mode. In addition, this approach removes the need for AFM tip calibration as long as the tip is not damaged during the measurement process.

These methods of atom counting as outlined in this report are non-destructive and are intended to yield samples which can be measured by various instruments such as an SEM and subsequently re-measured atomically. This is a unique and important element of this work since there are no other known methods which allow this kind of atomic dimensional measurement **without being destructive**. In addition this new method opens up the possibilities of basing the measurement metric on the intrinsic crystal lattice rather than an external yard stick such as an interferometer or CCD calibration.

Technical Strategy

The technical work is focused into four thrust areas. The first area is the development of methods to prepare photolithographically patterned three-dimensional structures in semiconductor materials. These structures must be prepared in such materials as to allow the atomic surface reconstruction of those features such that the atomic order is commensurate with the underlying crystal lattice.

MILESTONE: Atom-based Artifacts: Develop methods to prepare photolithographically patterned three-dimensional structures in silicon and GaAs. These structures must be prepared in such materials as to allow the atomic surface reconstruction of those features such that the atomic order is commensurate with the underlying crystal lattice. FY 2001.

The second aspect is the development of techniques for the preparation of SPM tips with reproducible geometries and the direct characterization of the SPM tip geometry and dimensions on the atomic scale. These well characterized tip probes can then be used to measure the samples with photolithographically defined and canonically ordered surfaces on the sub-nanometer length scale.

The strategy is to develop PtIr and W tips for systematic measurements on atomically ordered silicon and GaAs surfaces. We are developing the STM tip etching, field evaporation, and cleaning procedures which reliably yield stable W tips and produce atomic resolution on Si (7x7) surfaces. The primary tools for direct tip characterization are the FIFEM for 1 to 100 nm radii tips, and SEM analysis for larger tip features.

MILESTONE: Atomic Imaging Tool Development: Develop the techniques for the preparation of SPM tips with reproducible geometries and the direct characterization of the SPM tip geometry and dimensions on the atomic scale. FY 2000

In parallel we continuously make a determination of the SPM performance in these dimensional measurements and improve the hardware through better vibration isolation, electical noise reduction etc. The last component of the work is to develop the methodology to enable the transfer of atom-counted samples to other measurement tools such scanning electron microscopes or atomic force microscopes.

The atom-based metrology effort is focusing on developing artifacts which can be atom counted and then measured in a number of different metrology tools such as SEM and AFM. The integrity of the line geometry, such as side wall angle, is crucial to having useful artifacts. The work therefore is focused on reducing the process temperatures required for atomic reconstructions. We have made wet chemical processing fully operational and are currently working on preparing atomically ordered Si surfaces at significantly reduced temperatures. For sample preparation, we are utilizing the existing in-situ processing apparatus and techniques from the UHV STM and concentrating on the reproducible production of atomically ordered Si surfaces and Si (111) step and terrace structures.

MILESTONE: Traceability Chain: Develop methods for the first demonstration of direct interferometer measurements of surface atom spacings. Complete this link to develop an unbroken traceability chain to the international unit of length. FY 2000

We have obtained atomically flat surfaces and are now trying to get atomic order using the low

temperature wet chemical based methods. We have a similar effort going on with GaAs which will be very useful for AFM and optical CD calibration. We have produced atomically ordered surfaces of GaAs at far reduced temperatures and will begin work shortly with patterned GaAs linewidth samples. We have designed and procured a reticle to have the desired GaAs linewidth features fabricated. The new reticle has been received and we have begun processing new patterned linewidth specimens.

The long term technical objective is the development of in-situ stabilized, atomically ordered surfaces which can be transferred to other measurement instruments such as scanning electron microscopes, AFMs, or optical metrology tools. These nanometer scale standard artifacts with atomically ordered surfaces will then act as linewidth calibration samples.

MILESTONE: Artifact Stability: Develop the methodology to enable the transfer of atom-counted samples to other measurement tools such scanning electron microscopes or atomic force microscopes. FY 2001

Accomplishments

- The photomask has been received for the new GaAs atom counted linewidth specimen. The actual reticle design is that from quadrant 1 of the silicon SEMATECH mask set repeated multiple times. We are now making several small GaAs wafers with this mask which should yield enough die to perform a thorough set of experiments to verify the process and demonstrate the method.

- We have attempted our first direct measure of the surface atom spacings based on a traceable interferometer measurement. We have fitted our UHV STM with a high accuracy sub-angstrom resolution interferometer. We have closed the loop and made our first atomic resolution measurements with full interferometer length basis. The successful completion of this aspect has enabled direct distance determination with simple atomic counting. We are in effect verifying the intrinsic ruler accuracy.

- We have produced atomically ordered surfaces of GaAs at far reduced temperatures and are now working with patterned GaAs linewidth samples. The new GaAs linewidth features have been fabricated and we have successfully prepared As capped samples without damaging the line geometry or integrity in any measurable way. These samples have been processed using the complete atomic surface preparation method, measured in UHV and then allowed to oxidize to create a stable surface for measurement in other tools. The samples have now been measured in other tools and the work is now focused on a quantitative evaluation of the .....

- The ability to prepare atomically sharp tips in W (111) has been demonstrated and the details of this methodology along with the new models we have developed for analyzing sharpness are currently being prepared as a journal article.

- The first demonstration transfer has been attempted between the EEEL MBE system and the PED UHV STM with minor difficulties which have been addressed. The sample was maintained in a UHV environment during the entire event.

FY Deliverables

Fabricate new linewidth photomask and have fabricated wafers specifically for linewidth metrology and atom counting. Complete mask designs and wafer fabrication. These wafers will be fabricated at SEMATECH this fiscal year.

Use the new interferometry setup in air to successfully make interferometer based measurements. Install system in UHV for first vacuum based measurements.

Presentations/Talks

"Atom-based CD metrology," the Nov. 1998 SEMATECH Metrology Workshop. (R. M. Silver *et al*)

"Length from Millimeters to Angstroms," Best in Length" series hosted by the NIST director, R. Kammer. presented the section on, March 1999. . M. Silver *et al*)

"Atom-Based Metrology," forr the NIST director, assistant director and undersecretary of commerce for technology, May 1999. (R.M. Silver)

"Atom-Based Metrology, SEMATECH metrology workshop, Austin TX, September 1999. (R. M. Silver)

Publications

Rao, P.V.M., Jensen, C., and Silver, R. M., A Generic Shape Model for STM Tip Geometry, to be submitted to Phys. Rev. B, (1999).

Silver, R. M., 1998-99 NIST/SEMATECH Collaboration to Develop Atom-based Linewidth Standards, Interim SEMATECH Report, July 1999.

Silver, R. M., Jensen, C., Tsai, V., Fu, J., Villarrubia, J., and Teague, E., Developing a Method to Determine Linewidth Based on Counting the Atom-Spacings Across a Line, , **3332**, p. 441 1998.

Optical Overlay and Critical Dimension Metrology

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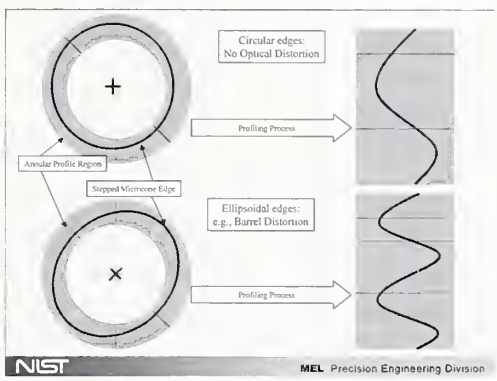
NIST OMP/NSMP
Other Agency
SEMATECH

Project Goals

Provide technological leadership to semiconductor and equipment manufacturers and government agencies by developing and evaluating the methods, tools, and artifacts needed to apply optical techniques to the CD and Overlay metrology needs of semiconductor manufacturing.



Customer Needs

Tighter tolerances on Overlay and CD measurements on photomasks and processed wafers are an inherent consequence of the need of the semiconductor industry to maintain rapid productivity improvements through feature size reduction . The 1999 SIA ITRS highlights these requirements on page 298, Table 82, and on pages 301-302, Table 83.

Pattern placement and overlay of the various lithographic levels is monitored with a series of box in box or frame in frame targets, each in a different plane. The overlay offset is then obtained by optical measurements with a determination of the relative target center lines. Any misalignment in the overlay metrology system will translate into an artificial overlay offset, referred to as tool induced shift (TIS). Additionally, there are residual errors caused by asymmetries in the target edges or covering layers (resist) known as wafer induced shift (WIS). A set of standard artifacts and procedures, under development at NIST, is designed to assist in aligning overlay measurement systems and eliminating TIS. After alignment, the tool must then be calibrated with standard artifacts to yield accurate overlay offsets.

Technical Strategy

The technical strategy for overlay metrology is divided into two segments: 1) instrumentation development and overlay metrology methodology and 2) design and calibration of standard artifacts. The measurement system is an optical reflection mode instrument, operational in either a bright field or confocal mode, with interferometry on three orthogonal axes also capable of monitoring the stage tilt. Additional hardware capabilities include the options to scan the sample while acquiring data with an on-axis photometer or high resolution image capture with a full field CCD data acquisition system. This latter mode has enabled a detailed study of CCD array performance and characterization.

MILESTONE: By FY 2000 complete the formal qualification process of the microscope optics and the x-y metrology and investigate the key issues in overlay metrology.

MILESTONE: By FY 2001 develop comprehensive modeling capabilities for centerline and edge detection methods and modeling techniques for edge analysis and pitch determination, in the reflection mode for overlay measurements.

The overlay program is focused on improving methods to characterize TIS by the development of a "tool kit" with both procedural and artifact standards to assist in alignment of the optical and mechanical elements of overlay metrology systems. Once the tool is aligned and TIS free, it may be used to characterize *wafer induced shift*.

As part of our hardware development program, we have performed a detailed study of CCD data acquisition cameras. In this work, several CCD acquisition systems are being evaluated and

improved edge detection and CCD array calibration procedures are being developed These same methods for 2-dimensional CCD array analysis are now being applied to optics analysis .

MILESTONE: By FY 2001 develop methods for CCD calibration and analysis. Utilize the new microgrid for calibration of optics and the CCD acquisition systems using the new self-calibration methods.

WIS-free standard overlay artifacts are currently being fabricated. These overlay artifacts are for the calibration of TIS free optical overlay tools. The artifacts are being fabricated in single crystal silicon and will provide an array of etched silicon three-dimensional targets with additional targets fabricated using industry standard process levels.

MILESTONE: By FY 2000 design 2-dimensional grid artifact, procure mask and make measurements with applications of the self-calibration algorithms.

MILESTONE: By FY 2001 design and procure metrology photomask. Work with Industry partners to determine designs and which levels are most appropriate for the silicon fabrication phase. Calibrate these overlay standards (both alignment and calibration) for SRM certification.

The technical strategy for linewidth standards is similarly divided into two segments: (1) instrumentation and model development and (2) design and calibration of standard artifacts.

An ultraviolet transmission microscope has been constructed that will replace the green light linewidth calibration system. This new instrument uses a unique geometry (a Stewart platform) as the main rigid structure and shows considerable improvement in vibration characteristics over a conventional microscope. Higher image resolution, reduced transmission of UV light through the chrome, and reduced instrument vibration will offer improved linewidth measurement uncertainties.

NIST has supplied a substantial number of photomask linewidth standards worldwide over the past decade. Chrome-on-quartz photomasks with linewidth and pitch artifacts in the range of 0.5 μm to 30 μm have been certified on a green light optical calibration system. Linewidth uncertainties have been reduced to 40 nm.

Two new dimensional standards are in development.

SRM 2800 Microscope Magnification Standard is a standard size microscope slide with calibrated pitch features ranging from 1 μm to 1 cm. It contains a lithographically produced chrome pitch pattern consisting of a single array of parallel lines with calibrated spacings. It contains no linewidth structures. This SRM is intended to be used for the calibration of reticles for optical or other microscopes at the user's desired magnification. The SRM may be used in either transmission or reflection mode optical microscopes, SEMs, or SPMs. Calibration is traceable to the meter through NIST Line Scale Interferometer.

MILESTONE: By Jan. 1, 2000 calibrate approximately 70 SRM 2800s and deliver to the Office of Standard Reference Materials.

SRM 2059 Photomask Linewidth Standard is the next generation NIST photomask linewidth standard, intended to replace SRM 473. Its design contains for linewidth and spacewidth features from 0.25 μm to 32 μm and pitch features from 0.5 μm to 250 μm

MILESTONE: By Sept. 30, 2000 calibrate the SRM 2059 photomask standards and deliver them to the Office of Standard Reference Materials.

Neolithography is the full integration of process simulation and metrology into the microlithography process, leading to a comprehensive and logical approach to photomask design and use. A Neolithography Consortium, a group of companies who produce simulation software and measuring tools, will be formed to accelerate the adoption of Neolithography by identifying impediments to the integration of simulation and metrology tools into the microlithography process, and finding solutions to remove these impediments.

MILESTONE: By Sept. 30, 2000 identify and invite appropriate companies to participate in the Neolithography consortium, and have the first meeting.

The *Bureau International des Poids et Mesurs* (BIPM) in Paris has commenced a series of interlaboratory key comparisons of measurements and standards among the National

Measurement Institutes (NMIs) of countries around the world. As the U.S. national standards institute, NIST is participating on several levels, and in particular, NIST is the pilot laboratory for nanometrology linewidth measurements. A NIST photomask linewidth standard SRM 475 will be circulated among nine countries in America, Europe, and Asia, who will measure the chrome features using various techniques of their choice. The measurement protocol, coordination of the measurements, and evaluation of the results are being done at NIST.

MILESTONE: By June, 2000 commence circulation of the NIST linewidth standards for the BIPM international comparison.

Accomplishments

- A comprehensive analysis of the available automated focus algorithms has been completed and involves a combination of experimental and theoretical results.

- The designs for a 6 inch photomask grid with micro grids also present are complete and the artifact has been received. This is the prototype standard with numerous two-dimensional calibration applications. Several feature sets have been measured

- The 6 inch grid standard prototype has been measured at PTB in a comparative test on the international unit of length. The round robin and PTB measurements have been used in the designs for the new grid artifacts. The new set of grid artifacts have been received and will become available as SRM 5000 in the near future. These grid artifacts have both the 5mm pitch 6 inch grids as well as the 100 micrometer microgrids.

- We have performed a detailed, in depth study of CCD data acquisition cameras. In this work, several CCD acquisition systems were compared and results demonstrate the significant performance differences and error sets.

- The round robin measurements on the 6 inch photomask grid proved successful. The measurements show that we are able to make available a standard artifact which meets industry need based on the outlined methodology. We have also completed a set of measurements with the microgrid which proved very useful in two-dimensional calibrations and characterization of optical tools. These microgrids are present on each 6 inch photomask are designed to assist in system alignment and calibration for both high accuracy x-y tools and overlay metrology tools.

- Consulted with Statistical Engineering Division on statistical control of SRM 2800 calibrations.

- Invited NMIs around the world to participate in the BIPM nanometrology linewidth comparison and wrote the measurement protocol.

- Developed new concepts for assessing the measurement uncertainty arising from artifact imperfections.

- Procured and inspected photomasks printed to SRM 2059 specifications.

FY Deliverables

- Complete the formal qualification process of the microscope optics and the x-y metrology. Investigate the key issues in overlay metrology..

- Preliminary use of new microgrid for calibration of optics and the CCD acquisition systems using the new self-calibration methods.Design and procure metrology photomask set. Have prototype overlay wafers faricated at SEMATECH and evaluate the new overlay standards.

Presentations/Talks

"Overlay Metrology," SEMATECH Metrology Workshop. Nov. 1998. (R. M. Silver et al)

"Automated Focus and Edge Detection Algorithms," Proceedings of the SPIE, The International Society for Optical Engineering, *Integrated Circuit Metrology, Inspection, and Process Control XIII,* Vol. **3677**, pp. 587-598 (1999). (S. Fox).

"Two dimensional Grid Standards," SPIE, The International Society for Optical Engineering, Metrology, Inspection, and Process Control for Microlithography XIII, 1999. (R. Silver)

"Linewidth, Then and Now," R. Larrabee, SPIE, The International Society for Optical Engineering, Metrology, Inspection, and Process Control for Microlithography XIII, 1999. (R. Larrabee),

"Overlay Metrology," SEMATECH Metrology Workshop. March 1999. (R. M. Silver)

"SEMI task force meeting on Grid Standards," Santa Clara, March, 1999. R. M. Silver,

"Overlay Metrology" SEMATECH AMAG Metrology Workshop, June 1999. (R. M. Silver)

"SEMI task force meeting on Grid Standards," Santa Clara, July, 1999. (R. M. Silver)

"Length from Millimeters to Angstroms," Best in World" series hosted by the NIST director, R. Kammer. March (1999). (R. M. Silver et al)

"Overlay Metrology," SEMATECH Metrology Workshop, Austin TX., October 1999 (R. M. Silver)

Publications

Fox, S., Silver, R., and Kornegay, E., Automated Focus and Edge Detection Algorithms, Proceedings of the SPIE, The International Society for Optical Engineering, Metrology, Inspection, and Process Control for Microlithography XIII (1999).

Larrabee, R., . Silver R., and Davidson, M., Linewidth, Then and Now, Proceedings of the SPIE, The International Society for Optical Engineering, Metrology, Inspection, and Process Control for Microlithography XIII (1999).

Potzick, J., "Measurement uncertainty and noise in nanometrology", *Proceedings of the International Symposium on Laser Metrology for Precision Measurement and Inspection in Industry*, Florianopolis, Brazil (1999).

Potzick, J., "Noise averaging and measurement resolution (or 'A little noise is a good thing')", *Review of Scientific Instruments*, vol. 70, no, 4, pp 2038-2040 (1999).

Silver R. M., and Potzick, J., Photomask Linewidth Standards, Benchmarking the Length Measurement Capabilities of the National Institute of Standards and Technology, R. M. Silver and J. L. Land, Eds., NISTIR 6036 (1998).

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Silver, R. M., 1997-98 NIST/SEMATECH Collaboration to Improve High-accuracy Overlay Metrology, Final Report, SEMATECH.

Silver, R., Doiron, T., Fox, S., Kornegay, E., Takac, M., and Rathjen, S., Two dimensional Grid Standards, Proceedings of the SPIE, The International Society for Optical Engineering, Metrology, Inspection, and Process Control for Microlithography XIII (1999).

High-Accuracy Two-Dimensional Measurements

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NIST OMP/NSMP

Project Goals

The ability to place features accurately in 2D has multiple impacts in the electronics industry. The situation regarding this critical capability is unusual in that state-of-the-art commercial measuring machines are so accurate that there is no available source of better 2D measurements from which standards can be established. As such, each user's measurements today are traceable only to one particular measuring machine. NIST clearly recognizes the industry-wide exposure inherent in this situation and is developing innovative approaches to solve the problem.

Customer Needs

Two-dimensional measurements are implicitly needed for controlling overlay capabilities of steppers and mask-making tools. Overlay is listed in Table 38, page 145 of the 1999 SIA ITRS as a difficult challenge for both >100 nm and <100 nm processes and states that overlay improvements have not kept pace with resolution improvements and will be inadequate for ground rules less than 100 nm. Also overlay over large field sizes will continue to be a major concern for sub-130 nm lithography. It also shows, in Table 41, pages 150-151, that two-point placement accuracy is and will be a critical issue for rules at 165 nm and less.

Technical Strategy

We are approaching the problem of two-dimensional measurements from a number of directions. The first, and most immediate, is to develop an artifact standard which can be used to bring all of the two dimensional based inspection instruments to the same metric. This work, done in conjunction with Dr. Richard Silver of the Precision Engineering Division, will develop a standard grid which will be sold as a NIST Standard Reference Material to standardize 2D measurements in the semiconductor industry. The effort has three main parts: development of a industry consensus standard grid, measurements by state-of-the-art measuring machines in private industry, and verification of the measurements using NIST capabilities. A prototype grid has been made and measurements begun. Each measurement of the grid will have data in each of at least two orientations. Rotating the grid 90 degrees between measurements samples a number of the geometric errors of the machine. The remaining geometric sources of uncertainty are the scale and some components of the straightness of each machine axis travel.

Verification of the grid measurements will be made at NIST. The overall scale of the grid will be checked with the NIST linescale interferometer, an instrument that is known to provide the most accurate 1D measurements available in the world. There are two sources of uncertainty not captured by these measurement methods, some components of the straightness and the effects of the plate bending when fixtured. We have begun work on methods to characterize both of these effects. These studies will allow us to have a complete error budget for the SRMs.

Another important factor in two-dimensional inspection is the performance of the video camera used as the main sensor in the newer instruments. There is increasing concern about how the camera chip geometry affects the accuracy of measurements. Since most measurement algorithms claim to have accuracies of much less than one pixel, the response of each pixel to the light is critical. To address this problem we have begun a program to explore the detailed response of typical CCD camera chip geometry to where on the chip the light falls.

Finally, the long-term solution for industry is to develop suitable self-calibrating measurement algorithms. We have had one SBIR grant to implement the most advanced algorithm for the self-calibration of measuring machines with grid plates, and are working with another company through the SBIR program to design, implement, and test new algorithm.

MILESTONE: By the end of FY 2000, deliver the first batch of Reference Material grid plates. Continue industrial and international interlaboratory tests of grid plates, using the NIST Prototype as the transfer artifact.

This will include finishing the detailed uncertainty budget with study of plate deformation and straightness. We will also be able to characterize the state of the art for two dimensional measurements from our interlaboratory tests. Finally we will begin experiments of the effects of CCD array geometry on measurement accuracy.

MILESTONE: By end of 2001,issue SRM grid plates, complete with detailed uncertainty budgets. Report on measurement errors from CCD array geometry and begin development of uncertainty budget.

By determining how the camera chip affects the accuracy of measurements we will be able to develop criteria for good camera metrology, and work towards determining the ultimate accuracy of current CCD based sensors.

Accomplishments

- First prototype grid plate built and measured at three industrial laboratories, one foreign National Measurement Institute, and the NIST linescale interferometer. The data shows excellent correlation for the state of the art instruments.

- Preliminary uncertainty budget for grid measurements has been developed and peripheral studies on various items have been, or are currently being, made.

- Studies of robust edge algorithms have been finished and submitted for publication.

FY Deliverables

First SRM grid plates will be issued.

Publish report on grid plate measurement uncertainties, including uncertainty budget and report on plate deformations, as well as international comparison data.

Publications

Meissner K., and Wegener, T., Robust Regression for Two Dimensional Coordinate Measurements, Proceedings of the International Symposium on Laser Metrology for Precision Measurement and Inspection in Industry, Florianoplis, Brazil, October 13-15, 1999.

Schroeck, M., and Doiron, T., Probing of two-dimensional grid patterns by means of camera based image processing, accepted by SPIE for January 2000.

Scanning Probe Microscope Metrology

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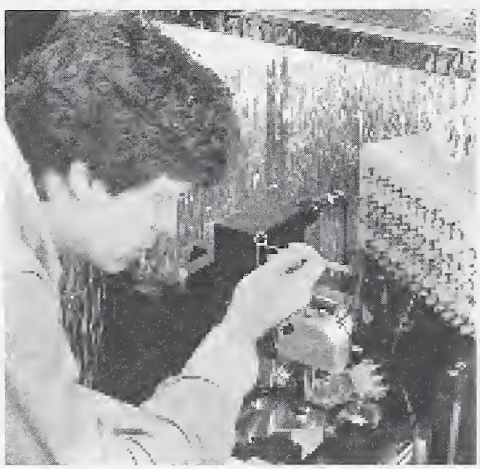
NIST OMP/NSMP

Project Goals

Provide technological leadership to semiconductor and equipment manufacturers and other government agencies by developing and evaluating the methods, tools, and artifacts needed to apply SPMs and other electrical characterization methods to semiconductor materials and processes; provide silicon and compound semiconductor manufacturers with advanced scanning-probe electrical metrology techniques and models to improve device performance and reliability. A specific goal is to provide the TCAD community with quantitative two-dimensional dopant profiles to calibrate and enhance the productivity of simulators.



Customer Needs

The 1999 SIA ITRS identifies two- and three-dimensional carrier profiling as a key enabling technology for the development of next-generation integrated circuits. The goals in 1999 for 2-D carrier profiles are for a spatial resolution of 5 nm and a precision (in concentration) of ±5%; these demands increase to less than 1 nm and ±2% by 2015. The SCM has emerged as the leading contender to provide 2-D carrier profiles.

While SCMs are commercially available, models to accurately interpret details of the SCM images have lagged. Much work remains to be done to develop robust three-dimensional physical models of SCM capable of extracting quantitative carrier profiles from SCM images. Likewise, the measurement methodology for quantitative SCM is still evolving. The need for, and form of, standard reference materials for SCM have yet to be defined. Other SPM based techniques for semiconductor metrology suffer similar problems – microscopes have been invented, but standard measurement and interpretation techniques are not available.

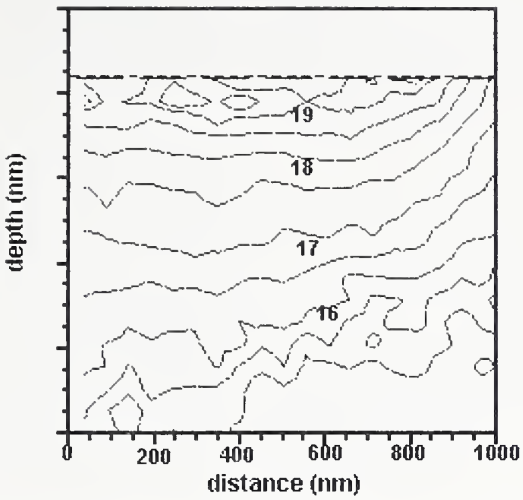
Technical Strategy

Our current primary goal is to develop the measurement methodology, physically based models, and interpretation formalisms to make SCM a practical metrology for 2-D carrier profiling of silicon. Best measurement practices are being determined via collaborative projects with industrial users and research into the physics of the silicon surface preparation. The focus of our modeling effort has been to develop 2-D and 3-D finite-element solutions of Poisson's equation for the SCM geometry. Our expertise with interpreting SCM images is being transferred to industry through our software program FASTC2D. The program features an easy to use interface, rapid profile extraction, and a Windows environment. Updates to the interpretation software will be available via the Internet in FY2000.

The project is also actively investigating other SPM based characterization techniques. We plan on extending the SCM carrier profiling capacity to SiC and III-V semiconductors. Intermittent-contact SCM is sensitive to variations in the dielectric constant of thin films and can detect metal layers buried beneath insulating films. Optically-pumped SCM is sensitive to variations in carrier lifetime. The SMWM is of interest because it can provide both the real and imaginary parts of impedance at frequencies from dc to 50 GHz.

Our first generation software utilizes a database of pre-calculated solutions that can very rapidly determine a 2-D carrier profile from an SCM image. When used in conjunction with SIMS measurements or a reference sample, relatively accurate profiles can be obtained. The

FASTC2D software package will be available to users in Fall of 1999.



Two-dimensional carrier profile of 50 keV boron implant into silicon extracted from SCM image using NIST's FASTC2D software.

MILESTONE: **By 2000, make SCM interpretation software based on a dopant gradient independent model available to industrial users.**

Proper interpretation of carrier profiles of current interest to the integrated circuit industry will require consideration of the local dopant gradient. We have estimated the magnitude of this effect through simulations. We have also investigated experimentally and theoretically the effect of the p-n junction on the SCM signal. We have developed techniques to help locate the p-n junction location in an SCM image.

MILESTONE: ***By 2001, release second-generation code that can correct for the effect of the local dopant gradient and the presence of p-n junctions.***

An inverse solution of the SCM requires repeated solutions of the forward (calculate SCM signal from carrier profile) problem. The candidate carrier profile is adjusted until a carrier profile is found that makes the calculated SCM signal self-consistent with the measured SCM signal. We have demonstrated the techniques necessary to do this with a 2-D solver. We are currently investigating various 3-D solvers.

MILESTONE: By 2002, demonstrate inverse solutions of the SCM measurement.

Accomplishments

- Determined the magnitude of the dopant gradient effect on carrier profiles measured with the SCM. The first part of the study was a full simulation, using a knife-edge probe, of the SCM signal across a model dopant gradient. The second part compared the model dopant profile with the gradient independent profile extracted from the simulated signal using the FASTC2D approach. We are now able to quantify how different tip radii and dopant gradients affect the accuracy of carrier profiles extracted using first generation models.

- Modeled SCM data for a set of abrupt-transition p-n junctions with finite-element software. Combination of measurements and simulations were used to validate an expression for locating a p-n junction with the SCM and to suggest a method of extending the calibration curve method to samples containing p-n junctions.

- Imaged with SCM a set of 18 samples consisting of ion implanted profiles and epilayers on both like-type and opposite-type substrates. A complete matrix of samples (n+ on n, n+ on p, p+ on n, and p+ on p) with high-to-low dopant gradients of 10, 100, and 1000 was available. The unique range in dopant gradient of these "known" samples allowed measurement of the dopant gradient and p-n junction effects that have been simulated.

- Coding of core functions of FASTC2D was completed. Our SCM signal extraction algorithm was re-written to include the effect of the high frequency voltage. The tip model has been extended to include both a flat and curved region. Two-dimensional data conversion and display has been coded and tested. An interactive help function has been added. An installable version of the code for WINDOWS 9x and NT has been tested.

- A DoC SBIR grant has been made to Atolytics, Inc. in State College, PA to develop their SMWM. The goals of phase I are to demonstrate both 1-D (surface into depth) and 2-D (x-y scanned) carrier profiling with the SMWM.

FY Deliverables

Software

Development of the first generation of FASTC2D (2-D SCM Image-to-Carrier Profile software) was completed (J. Kopanski, B. Rennex, and J. Marchiando)

Publications

Kopanski, J. J., Marchiando, J. F., Albers, J., and Rennex, B. B., Comparison of Measured and Modeled Scanning Capacitance Microscopy Images Across P-N Junctions, Proceedings of the 1998 International Conference on Characterization and Metrology for ULSI Technology, Gaithersburg, Maryland, March 23-27, 1998, pp. 725-729.

Kopanski, J. J., Marchiando, J. F., and Rennex, B. G., Carrier Concentration Profile Dependence of Scanning Capacitance Microscopy Signal in the Vicinity of p-n Junctions, Proceedings of the Fifth International Workshop on the Measurement, Characterization, and modeling of Ultra-Shallow Doping Profiles in Semiconductors, at Research Triangle Park, NC, March 28-31, 1999, p. 202.

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Ukraintsev, V. A., Llist, R. S., Chang, M.-C., Edward, H., Machala, C. F., Martin, R. S., Zavyalov, V., McMurray, J. S., Williams, C. C., De Wolf, P., Vandervorst, W., Venables, D., Neogi, S. S., Ottaviant, D. L., Kopanski, J. J., Marchiando, J. F., Rennex, B. G., Nxumalo, J. N., Proceedings of the 1998 International Conference on Characterization and Metrology for ULSI Technology, Gaithersburg, Maryland, March 23-27, 1998, pp. 741-745.

Thin-Film Profile Measurement Methods and Reference Materials

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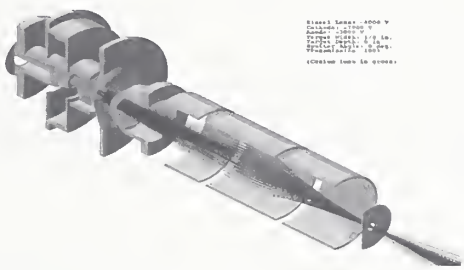
Funding Sources:
NIST OMP/NSMP

Project Goals

Improve the capabilities for compositional depth-profiling in the following areas to support the U.S. semiconductor industry; define optimum procedures for ultra-high depth resolution and ultrashallow profiling by Secondary Ion Mass Spectrometry (SIMS); develop depth profiling reference materials needed by U.S. industry; develop methods to improve the uncertainty of implant dose measurements by SIMS.



Customer Needs

The 1999 SIA ITRS discusses the need for improved SIMS capabilities for ultrashallow doping profile measurements and offline doping process control in several sections. Under Process Integration, the requirements for 2-D and 3-D dopant profiles for verification of TCAD models are described. Under Front End Processes, the need for thin-film reference materials is delineated. Under Metrology, the increasing precision requirements for dopant concentration measurements are indicated, with improved SIMS as the most likely candidate to provide the solution.

Technical Strategy

We are investigating the use of novel primary ion beam species in commercial SIMS instruments to improve depth resolution. Working with a U.S. instrument manufacturer, a filament-based duoplasmatron ion source has been developed to produce molecular ion beams such as SF_5^+ with sufficient beam current to be practical for depth-profiling applications. A different ion source under development (computer model shown above) produces cluster ion beams from a target material under Cs^+ ion bombardment. For both types of sources, the low effective bombardment energy can produce depth profiles with little beam-induced kinetic distortion. These sources are designed to attach to a commercial SIMS instrument that is widely used in the U.S. semiconductor industry, thus leveraging the high capital investment of the equipment.

MILESTONE: ***By FY 2001, test Cs cluster ion source (CsC_6^-) on magnetic sector SIMS. Collaborate with SEMATECH on comparison of shallow As implant profiles.***

A phosphorus implant in silicon standard reference material for SIMS calibration of implant doses is the next step in the development of ion-implanted SRMs. This follows the already produced boron- and arsenic-implanted standards. The previous standards were certified by nuclear methods, the boron by a neutron reaction method and the arsenic by instrumental neutron activation analysis. The proposed method for phosphorus certification is by radiochemical neutron activation analysis, which is more challenging than the other two because a chemical separation is required before counting the beta particles emitted from the activated ^{32}P.

MILESTONE: ***By FY 2000 investigate measurement of P implant dose in Si by RNAA.***

We have previously developed and validated SIMS methods for measuring boron implant doses and concentrations in silicon with a repeatability of better than 2 %. We are extending this work to the measurement of arsenic in silicon, which is more complicated than boron because care must be taken to exclude a possible spectral interference from Si_2O ion

MILESTONE. By FY 2001, establish precision of As implant dose measurements with SIMS

Accomplishments

- Demonstrated feasibility of using polyatomic ion sources on commercially available SIMS instrument.

- Demonstrated significant improvements in depth resolution for SIMS depth profiles of low energy As implants using CsC_6^- cluster primary ion beam (see figure below). Sample supplied by SEMATECH, where additional SIMS measurements were made.
- Measured six P-implanted Si samples from same wafer and four solution standards by RNAA, with relative standard deviation of 2 %. Mean value was within 2 % of nominal implanted dose.
- Precision of multiple dose measurements by SIMS of NIST SRM 2134 (Arsenic implant in silicon) has been reduced to <1 % relative standard deviation.

Presentations/Talks

"Polyatomic Primary Ion Beams for Spatially Resolved Molecular Imaging and Depth Profiling," presented at the 15th International Conference on the Application of Accelerators in Research and Industry, Denton, TX , November 6, 1998 (Invited). (G. Gillen)

"Ultrashallow Depth Profiling with Polyatomic Primary Ion Beams," Proceedings of the 5th International Workshop on the Measurement, Characterization and Modeling of Ultra-Shallow Doping Profiles in Semiconductors, Research Triangle Park, NC, March 28-31, 1999. (G. Gillen)

"SIMS Using Polyatomic and Cluster Primary Ion Beams," 12th Annual Workshop on SIMS, Gaithersburg, MD, April 26, 1999. (G. Gillen)

"Recent Developments in Ultrashallow Depth Profiling at NIST," SEMATECH Analytical Laboratory Managers Working Group Meeting, NIST, Gaithersburg, MD, April 27, 1999. (G. Gillen)

"Ultrashallow Depth Profiling SIMS Using SF_5^+ Polyatomic Primary Ion Bombardment, " 12th Annual Workshop on SIMS, Gaithersburg, MD April 27, 1999. (G. Gillen,)

"Ultrashallow Depth Profiling with an SF_5^+ Primary Ion Beam," SIMS XII Conference, Brussels, Belgium, Sept., 1999. (G. Gillen)

"Organic SIMS Using Polyatomic and Cluster Primary Ion Beams," SIMS XII Conference, Brussels, Belgium, Sept., 1999. (G. Gillen)

"A Negative Cesium Sputter Ion Source for Cluster SIMS," SIMS XII Conference, Brussels, Belgium, Sept., 1999. (G. Gillen)

"The Development of Standard Reference Material 2134 - An Arsenic Implant in Silicon Standard for Secondary Ion Mass Spectrometry," International Symposium on Practical Surface Analysis PSA-98, Matsue, Japan, October 19, 1998. (D. S. Simons)

"Ion Implant Standards from NIST," SEMATECH Analytical Laboratory Managers Working Group Meeting, NIST, Gaithersburg, MD, April 27, 1999. (D. S. Simons)

Publications

Gillen, G., Bennett, J., Thompson, P. and Walker, M., The use of an SF_5^+ Polyatomic Primary Ion Beam for Ultra Shallow Depth Profiling on an Ion Microscope SIMS Instrument, Proceedings of the 5th International Workshop on the Measurement, Characterization and Modeling of Ultra-Shallow Doping Profiles in Semiconductors, Research Triangle Park, NC March 28-31, 1999, pp. 129-136.

Gillen, G., King, L. R., and Chmara, F., Development of a Triplasmatron Ion Source for Generation of SF_5^+ and F^- Primary Ion Beams on an Ion Microscope Secondary Ion Mass Spectrometry Instrument, J. Vac. Sci. Technol. A17, 845-852 (1999).

Gillen, G., Roberson, S., Preliminary Evaluation of a Polyatomic Primary Ion Beam for Analysis of Organic Thin Films by Secondary Ion Mass Spectrometry, Rapid Communications in Mass Spectrometry, 12, 1303-1312 (1998).

Thompson, P. E., Hobart, K. D., Twigg, M., Jernigan, G., Dillon, T. E., Rommel, S., Berger, P., Simons, D. S., Chi, P. H., Lake, R., and Seabaugh, A. C., "Si Resonant Interband Tunnel Diodes Grown by Low Temperature Molecular Beam Epitaxy," Appl. Phys. Lett. 79, 1308-1310 (1999).

Thompson, P. E., Silvestre, C., Twigg, M., Jernigan, G., and Simons, D. S., The formation of abrupt n+ doping profiles using atomic hydrogen and Sb during Si MBE, Materials Research Society Symposium Proceedings, Vol. 533 (1998), pp. 367-372.

Alternate Gate Dielectric Metrology for CMOS Technology

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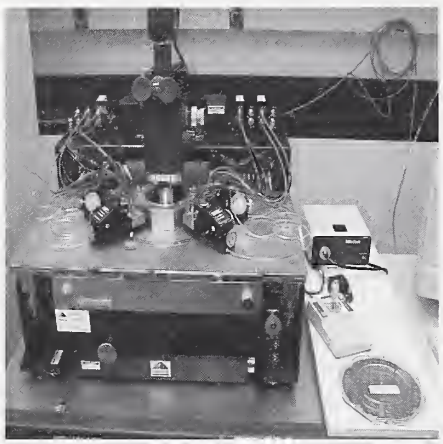
Funding Sources:
NIST OMP/NSMP
NIST SRD

Project Goals

Provide standards, techniques and data for the comparison and development of alternate gate dielectrics fabricated throughout the research community; increase the understanding of the relationship between the gate dielectric material/interface and device electrical measurements.



Customer Needs

The 1999 SIA ITRS indicates that by the years 2003-2005, the equivalent thickness of the gate dielectric will need to be approximately 1.5 nm. Due to increased power consumption, intrinsic device reliability and circuit instabilities associated with SiO_2 of this thickness, a high permitivity gate dielectric (e.g. Si_3N_4, Ta_2O_5, $HfSi_xO_y$, ZrO_2) with low leakage current and at least equivalent capacitance, performance, and reliability will be required. SIA has identified the finding of a high permitivity gate dielectric to replace SiO_2 as one of the most difficult challenges to further scaling of MOS device dimensions.

Electrical characterization of MOS capacitors and FET, have historically used to determine device and gate dielectric properties such as insulator thickness, defect densities, mobility, substrate doping, bandgap, and reliability. Electrical and reliability characterization methodologies need to be developed and enhanced to address issues associated with these films including large leakage currents, quantum effects, thickness dependent properties, large trap densities, transient (non-steady state) behavior, unknown physical properties, and lack of physical models. As compared to SiO_2, very little is known about the physical or electrical properties of these films as gate dielectrics in MOS devices. The use of these films as gate dielectrics in CMOS technology requires standard data and a fundamental understanding of the relationship between the gate dielectric material/interface and device electrical measurements.

Technical Strategy

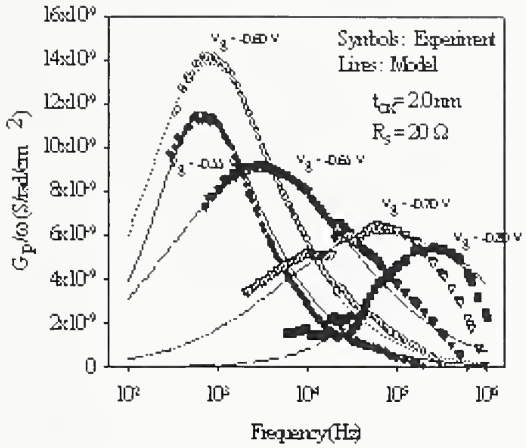
The strategy of this effort will be to obtain both device samples and blanket films from other industrial and university groups, to perform electrical characterization of the devices samples, and to collaborate with other researchers to perform analytical characterization.

Many issues, such as tunnel/leakage current and spatially dependent properties associated with metal oxide and silicate dielectrics, are also present in ultra-thin oxide and oxide-nitride stacked dielectrics. Therefore, many of the characterization schemes will first be developed on the simpler ultra-thin oxide and oxide-nitride dielectrics and then be applied to the metal oxide and silicate dielectrics. This project will also collaborate with the dielectric reliability project to assess the degradation and breakdown of these films under electrical stress.

There are two main focus areas for this task. The first focus area is to investigate electrical measurement techniques, procedures and analysis associated with devices having thin oxide and alternate gate dielectrics. The electrical measurement techniques that we are investigating include capacitance-conductance characterization, dielectric tunnel and leakage current characterization, defect density measurements such as charge-pumping and

conductance, and defect generation/reliability characterization.

MILETONE: ***By 2001, assess, modify and standardize electrical characterization methodologies and data for devices with ultra-thin oxide and oxide-nitride dielectrics. Initiate studies of metal oxide and silicate dielectrics.***



Experimental and modeled interface state conductance for a tunneling gate dielectric.

The second major focus area is to determine standard electrical and physical properties and mechanisms of thin oxide and alternate gate dielectrics. This includes characterizing standard properties and mechanisms/correlations for these dielectrics including defect centers, dielectric constant, defect generation rates, and leakage/tunnel current.

MILESTONE: ***By 2002, provide standard electrical and reliability measurements, standard electrical data and improved fundamental understanding of electrical properties associated with metal oxide and silicate dielectrics.***

Accomplishments

- A semiconductor parameter analyzer, LCR meter, other associated electronics, and a 20 cm semi-automatic fA probe station with thermal chuck was acquired and set up. A Windows-based program was written to perform a large number of characterizations including: a variety of current-voltage testing for both transistors and capacitors; capacitance and conductance measurements as a function of frequency and voltage; charge pumping measurements for diverse measurement conditions; reliability characterization including the capability of doing any of the above measurements intermittently during stressing; automatic wafer probing and mapping.

- A study was performed and a paper written and submitted on the application, theory and limitations of capacitance and conductance characterization of MIS capacitors with thin alternate dielectrics. The study used theory, experiment and simulations to determine the impact of leakage current, quantum-mechanical confinement in the substrate, series resistance, and other mechanisms associated with thin and alternate dielectrics on the conductance technique. The technique was applied to a variety of dielectrics including Si_3N_4 and TiO_2.

- A study was completed and a paper written and submitted on the effects of substrate hot electron injection on the reliability of ultra-thin SiO_2. This work provides an important understanding of the mechanisms governing reliability of ultra-thin SiO_2 and provides additional physical understanding that will be necessary for describing the reliability of alternate dielectrics with thin SiO_2 interfacial layers. Furthermore, this work will provide an important avenue for measuring the spatially (in the thickness direction) non-uniform defect generation expected for these stacked materials. All of this work will eventually lead to the development of new lifetime characterization methods for stacked alternate dielectrics.

Presentations/Talks

"Alternate Dielectric Technology and Metrology," Lecture at University of Delaware, Dept. of Electrical and Computer Engineering, July 13, 1999. (E. M. Vogel)

"Thin Film Metrology for CMOS and Beyond," EEEL Project Reviews, June 24, 1999. (E. M. Vogel, T. Shaffner, J. Ehrstein, and J. Suehle)

"Reliability of Ultrathin Oxides for MOS Devices," Lecture at North Carolina State

University, Dept. of Electrical and Computer Engineering, Apr. 22, 1999. (E. M. Vogel)

Publications

Vogel, E. M., Henson, W. K., Richter, C. A., and Suehle, J. S., Limitations of Conductance to the Measurement of the Interface State Density of MOS Capacitors with Tunneling Gate Dielectrics, accepted IEEE Trans. Elec. Dev.

Vogel, E. M., Suehle, J. S., Edelstein, M. D., Wang, B., Chen, Y., Bernstein, J. B., Reliability of Ultra-thin Silicon Dioxide Under Combined Substrate Hot Electron and Constant Voltage Tunneling Stress, submitted IEEE Trans. Elec. Dev.

Vogel, E. M., and Wortman, J. J. Properties of N-channel and P-channel MOSFETs with Ultrathin RTCVD Oxynitride Gate Dielectrics, Proceedings of the 1999 Electrochemical Society Spring Meeting.

Optical Second Harmonic Generation at the Si/SiO_2 Interface

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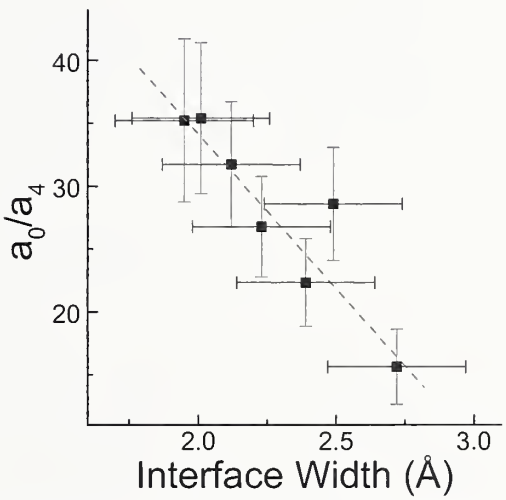
Funding Source:
ATP (100%)

Project Goals

Feature sizes in semiconductor integrated circuits have been decreasing relentlessly, resulting in remarkable performance gains. As lateral dimensions shrink, the dimensions of gate dielectrics must decrease proportionally. Surface second harmonic generation (SSHG) is an optical technique that is highly surface/interface selective. SSHG has been empirically shown to be sensitive to roughness at the Si/SiO_2 interface. The goal of this project is to obtain a better understanding of the basic physics that gives rise to this sensitivity to roughness. This will give insight into the morphology of the interface and into the potential for SSHG as a measurement tool.



Comparison of a_0/a_4, which is derived from SSHG, to the interface width measured by X-ray scattering. The interface width is a measure of roughness. [from S.T. Cundiff et al., Appl. Phys. Lett. 70, 1414 (1997)]

Customer Needs

Limitation on how thin the gate oxide can be made presents a potential barrier to further reduction in device size by the semiconductor industry. In future generations of integrated circuits (ICs) the gate oxide thickness will be reduced to the point where monolayer fluctuations at the Si/SiO_2 interface will represent a significant percent fluctuation of the total oxide thickness. Hence the industry is in need of a greater understanding of the morphology of the interface. Additionally, method of making in-situ measurements of the interface would be beneficial. SSHG may have advantages over other methods.

Technical Strategy

The SSHG signal from Si/SiO_2 displays resonant behavior due to both features in the bulk band structure and the interface alone. We are studying how this resonant behavior changes with change in surface preparation. Specifically we are looking at samples with different miscut (and hence differing step edge density), different oxidation and different roughness (as characterized by X-ray scattering).

SSHG is a very weak effect because only a layer only a few monolayers thick at the interface contribute. To obtain a measurable signal, without having to subject the samples to high average powers or high-energy pulses, we use 100 femtosecond pulses at a repetition rate of 76 MHz. This allows high peak powers to be obtained with a modest average power. Photon counting is used for signal detection. A tunable Kerr-lens-modelocked laser is used as the primary source. To extend the tuning range, an optical parametric oscillator is also employed.

A key challenge is to calibrate for changes in laser average power and pulse width that occur with tuning. The change in pulse width results in a change in peak power, and hence signal strength. To do this, a second reference arm is included in the experiment. The reference arm is virtually identical to the signal arm, but a quartz sample is used. Quartz generates a strong second harmonic signal, which is largely independent of laser tuning. A cross calibration between the signal and reference arms is obtained by installing a quartz sample in the signal arm and measuring the two signals versus tuning. The resulting calibration curve is used to correct all subsequent data.

Accomplishments

The entire SSHG apparatus is operational. Calibration of the arms has been performed and verified. Preliminary data on a set of miscut samples have been taken to verify performance of the apparatus. A new set consistent set of samples has been obtained. The apparatus for oxidizing them is in place.

FY Deliverables

Publications:

Fortier,T.M and Cundiff, S.T. Second Harmonic Generation at the Si/SiO_2 interface, to appear in the proceedings of the 2000 SPIE conference.

Thin-Film Process Metrology

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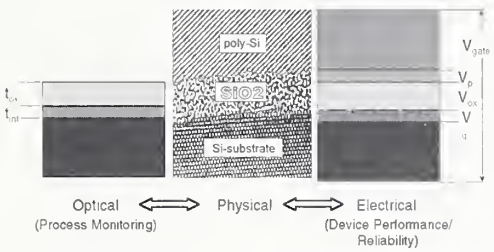
NIST OMP/NSMP
Division 812 STRS
SEMATECH

Project Goals

Develop new and improved electrical and optical measurements, models, data, and reference materials to enable better and more accurate measurements of select critical silicon CMOS technology thin-film parameters. Major focus is placed on requirements for silicon dioxide, oxynitrides, and high-k (dielectric constant) gate stacks for advanced gate dielectrics detailed in the 1999 SIA ITRS.



A cross section of an advanced gate-oxide structure probed by HRTEM and schematic represenations of that gate structure as "seen" by optical process monitor measurementsand by device electrical measurements.

Customer Needs

The evolving decrease of the gate dielectric film thickness to an oxide-equivalent value of 1 nm is identified as a critical front-end technology issue in the 1999 SIA ITRS. For effective (oxide-equivalent) gate dielectric thicknesses below about 2.0 nm, SiO_2 is expected to be replaced, initially by dielectric stacks utilizing silicon oxides and nitrides, and then by either metal oxides or silicates generally requiring one or two monolayers of additional interface dielectric. Process tolerance requirements for dielectric thickness are projected to be ±4 % (3σ), which translates to less than 0.1 nm for 2 nm films. Requirements for process control measurements are a factor of ten smaller still.

Spectroscopic Ellipsometry (SE) is expected to continue as the preferred measurement for process monitoring of future gate dielectric films. Industry metrology needs include not only improved methods to accurately determine film thickness, but also: (1) techniques to determine the structure of the individual films and the interfaces between them, (2) an improved understanding of the relationship between physical, electrical, and optical determinations of film properties, and (3) mechanisms for traceability to NIST (such as reference materials) to support film metrology.

For SE to meet process control requirements of film thickness and unambiguously determine film composition and morphology, the optical properties of these advanced dielectric film systems must be thoroughly studied and well characterized.

Technical Strategy

This project focuses on the issues of (1) relating optical, electrical, and physical measurements of thickness, composition, and interface structure, (2) developing and providing the basis for traceability to NIST for film thickness measurements, and (3) identifying structural models and developing preferred optical index dispersion models or data for improved ellipsometric analysis of future-generation gate dielectric film systems.

Relation of optical, electrical and physical measurements of thickness - Through collaborations with SEMATECH, IC industry companies, and SRC university staff, as well as with key researchers in other parts of NIST, project staff is leading and participating in a number of multimethod comparison studies of various ultra thin gate dielectric films. These multimethod studies utilize techniques such as X-ray and neutron reflectivity, high resolution TEM, angle-resolved XPS, SIMS, CV and IV analysis as well as spectroscopic ellipsometry and reflectivity. The results of these multimethod studies improve the general understanding of state-of-the-art (SOA) measurement capability for very thin films, and also allow project staff to assess the results of various optical models being applied to the analysis of these films. SOA CV and IV measurement capability for gate films has been established in the project. Advanced analysis software from commercial, and university sources is being established and benchmarked to determine the effect of model

sophistication on film thickness values calculated from C-V and I-V data. An *in-situ* two-terminal electrical evaluation technique for buried interface roughness is being extended to 0.25 μm MOSFETs and beyond.

MILESTONE: ***By 2000, identify preferred advanced electrical analysis software and use to improve agreement between electrical and ellipsometric thickness scales.***

Establish and transfer basis of accuracy for thin dielectric films - Industry requirements for future thin dielectric film optical measurements and calibration standards were identified at a NIST sponsored workshop in FY 98. Core ellipsometry measurement capability is being expanded and strengthened to meet these requirements. An investigation has been started into cleaning and recontamination issues for film calibration standards to determine whether a workshop-expressed goal of 0.015 nm long-term reproducibility of reference artifact values is obtainable. Procedures are being developed to enable traceability to NIST for suppliers of secondary thin-film reference materials without volume production of NIST SRMs.

MILESTONE: ***By 2001, transfer to 1st Level commercial suppliers of Reference Materials traceability to NIST for oxide films down to 2 nm.***

Structural and optical models for ellipsometry - A custom-built high-accuracy spectroscopic ellipsometer with a spectral range of 1.5-6 eV is being used, and project staff are working with SEMATECH, IC industry companies, and SRC university staff to obtain and optically characterize advanced oxynitrides, oxide/nitride stacks, and metal oxide films such as tantalum pentoxide and titanium dioxide. This work is directed at determining preferred structural models, spectroscopic index of refraction values, or preferred optical dispersion models for each of these film systems, and, where possible, the variability of these parameters due to differences in film fabrication processes. Analysis is done with software developed by NIST for SE; this software allows maximum flexibility for addition of the latest published or custom-developed optical response models as appropriate for each material system investigated.

MILESTONE: By 2002, establish preferred process-monitor capable ellipsometric models and analyses for stable-process replacement gate dielectric materials.

Accomplishments

- Showed, for a series of expected oxide/nitride/oxide stacks in the 3 nm to 4 nm thickness range, that there was no optical evidence of a Si_3N_4 layer. These films were best modeled as effective single-layer films using a Sellmeier dispersion for the index of refraction. The film thicknesses by ellipsometry were in the same relative order as determined by X-ray diffraction and SIMS, although the differences in absolute thicknesses by these techniques ranged from 0.1 nm to 0.3 nm. Relative nitrogen content, as determined by the index of refraction, was in the same relative order as determined by SIMS and XPS.
- Determined for a series of amorphous, low temperature annealed, Ta_2O_5 (high-K) films over a silicon oxide transition layer that a Tauc-Lorentz dispersion provides a good fit of the index of refraction, and that the optical gap for these films is 4.1 eV. Project staff showed that the variation in the value of the index of refraction among these films is strongly related to the film quality due to different anneal cycles, and to the thickness of the silicon-oxide interlayer, as determined by TEM. Project staff also found that while high temperature annealed, polycrystalline Ta_2O_5 films are not well described by the Tauc-Lorentz dispersion, it is readily evident from the ellipsometric data in the 4 eV to 6 eV range, whether the films are amorphous or polycrystalline.
- Designed and initiated a multilaboratory comparison study of the thickness of very thin SiO_2 films using spectroscopic ellipsometry, X-ray and neutron reflectivity, and C-V measurements. A thermal desorption cleaning process just prior to measurement was required for all participating laboratories. This procedure was based on results obtained during initial studies at NIST on the effectiveness of a variety of cleaning procedures.
- Initiated the process of adding spectroscopic capability to the master high-accuracy ellipsometer that is used for Reference Material and traceability activities. Prior to the completion of that upgrade, we are evaluating a hybrid process for establishing traceability to NIST for spectroscopic measurements in conjunction with VLSI Standards Inc. This activity focuses on spectroscopic measurements of silicon nitride films, and will be based on comparison of spectroscopic measurements at VLSI Standards and at NIST, done on a separate research spectroscopic ellipsometer. In addition, measurements at 632.8 nm on the NIST master ellipsometer will be compared with values at 632.8 nm extracted from data of the two spectroscopic instruments. Two wafers at each of three film thicknesses will be exchanged three times to complete this evaluation.
- Acquired, installed, and determined the operating capabilities of six different suites of advanced university and commercial sector software capable of accounting for polysilicon depletion and quantum mechanical effects that obscure the determination of thickness of thin dielectric films from C-V and I-V measurements. The relative performance of these software sets, which have various levels of sophistication, will be determined by comparing results for a model capacitor test structure having a range of polysilicon and substrate doping levels, as well as oxide thicknesses. It is necessary to understand the role of advanced analysis software in order to improve the understanding of electrical versus optical measurement of thin dielectric film thickness.
- Demonstrated that Weak Localization can be applied to measuring interface roughness down to 0.1 nm for 0.25 µm technology node structures.

FY Deliverables

SRMs

Issued SRM 2543 for Silicon Resistivity (D. Ricks and J. Ehrstein)

Collaborations

VLSI Standards (Prabha Durgapal) comparative spectroscopic and single-wavelength ellipsometry

measurements on Si_3N_4 thin films (B. Belzer, N. Nguyen, and J. Ehrstein)

Atomic Physics Division (R. Deslattes), Polymers Division (W. L. Wu), and NIST Center for Neutron Research (J. Dura), Bede Scientific, Four-Dimensions Inc., J. A. Woollam Co., KLA-Tencor, n and k Technology Inc., NC State Univ., Oak Ridge Nat. Labs, Rudolph Technologies, Solid State Measurements Inc., and Therma-Wave, Inc. multi-method comparison of very thin SiO_2 on Si (co-organized with Rutgers University, E.Garfunkel) (J. Ehrstein, C. Richter)

SEMATECH (A. Diebold), NCSU (D. Venables and D. Maher), and KLA-Tencor Corporation (C. Hayzelden), metrology for ultra-thin oxides, gate stacks and high-K dielectric materials (J. Ehrstein, C. Richter and N. Nguyen)

SEMATECH (A. Diebold and D. Brady), Lucent Technologies (R. Opila), and Div. 842 (R. Deslattes), study of oxynitride ultra thin films (C. Richter, N. Nguyen)

NIST Center for Neutron Research (J. Dura), spectroscopic ellipsometry, neutron reflectivity, and X-ray reflectivity measurement comparison for thin SiO_2 on Si (C. Richter, N. Nguyen)

Lucent Technologies (Glenn B. Alers) and SEMATECH (H. Huff and M. Gilmer), optical properties of Ta_2O_5 for use as a gate dielectric (N. Nguyen, C. Richter)

Jet Process Corporation (T. Tamagawa) and Yale Univ. (Prof. T. P. Ma), electrical and optical properties of jet vapor deposited high-K gate dielectrics (C. Richter, N. Nguyen)

U. Texas at Austin (Prof. J. Lee), optical properties of ZrO_2 and HfO_2 for use as high-K gate dielectrics (C. Richter, N. Nguyen)

Texas Instruments (G. Brown), ASTM, JEDEC, electrical and reliability characterization of ultra-thin gate oxides (J. Suehle, C. Richter)

Polymers Division (W. Wu), X-ray and optical study of low-K "spin-on" dielectric films (N. Nguyen)

SEMATECH/U. Texas at Austin (A. Diebold and J. Canterbury), spectroscopic ellipsometry analysis of oxynitrides (C. Richter, N. Nguyen)

Semiconductor Electronics Division (D. Gajewski and J. Pellegrino), *ex-situ* and *in-situ* characterization of AlGaAs films and surface oxidation (N. Nguyen)

COMPAQ, silicon interface property measurements (C. Richter)

Lucent Technologies (S. Martin), correlation of interface roughness and device noise (C. Richter)

Standards Committee Participation

ASTM F-1 on Electronics, Subcommittee F1.06, Section B on Thin Film Characterization, Leader, FY 97-99 (J. Ehrstein)

ASTM F-1 on Electronics, Subcommittee F1.06 on Silicon Materials and Process Control, chair, FY 84-99 (J. Ehrstein)

ASTM Committee F-1 on Electronics, Executive Committee, FY 84-99 (J. Ehrstein)

Software

Development of a second generation modeling and analysis program for spectroscopic ellipsometry: Spectroscopic Ellipsometry Studio V.2. Copies distributed for evaluation and use to VLSI Standards Inc., SEMATECH, Gaertner Instruments, Penn State Univ. (N. Nguyen)

External Recognition

Curt Richter was invited to co-organize a Symposium on Ultrathin SiO_2 and High-K Materials for ULSI Gate Dielectrics in conjunction with the Spring 1999 General Meeting of the Materials Research Society.

Publications

Dura, J. A., Richter, C. A., Majkrzak, C. F., and Nguyen, N. V., Neutron Reflectometry, X-ray Reflectometry, and Spectroscopic Ellipsometry Characterization of Thin SiO_2 on Si, App. Phys. Lett. 73 (15), 2131-2133 (12 October 1998).

Durgapal, P., Ehrstein, J. R., and Nguyen, N. V., Thin-Film Ellipsometry Metrology, Proceedings of the 1998 International Conference on Characterization and Metrology for ULSI Technology, Gaithersburg, Maryland, March 23-27, 1998, pp. 121-131.

Ehrstein, J. R., and Croarkin, M. C., NIST Special Publication 260-131, Standard Reference Materials: The Certification of 100 mm Diameter Silicon Resistivity SRMs 2541 through 2547 Using Dual-Configuration Four-Point Measurements, Revised June 1999.

Huff, H. R., Richter, C. A., Green, M. L., Lucovsky, G., and Hattori, T., eds., Ultrathin SiO_2 and High-K Materials for ULSI Gate Dielectrics, Mater. Res. Soc. Proc., Vol. 567, Pittsburgh, September 1999, 615 p.

Richter, C. A., Nguyen, N. V., and Alers, G. B., Spectroscopic Ellipsometry of Ta_20_5 On Si, in Ultrathin SiO_2 and High-K Materials for ULSI Gate Dielectrics, edited by H. R. Huff, C. A. Richter, M. L. Green, G. Lucovsky, and T. Hattori, Mater. Res. Soc. Proc., Vol. 567, Pittsburgh, September 1999, pp. 559-566.

Richter, C. A., Nguyen, N. V., Dura, J. A., and Majkrzak, C. F., Characterization of Thin $Si0_2$ on Si by Spectroscopic Ellipsometry, Neutron Reflectometry, and X-ray Reflectometry, Proceedings of the 1998 International Conference on Characterization and Metrology for ULSI Technology, Gaithersburg, Maryland, March 23-27, 1998, pp. 185-189.

X-ray Measurement Methods for Characterization of Thin Films and Their Microstructures

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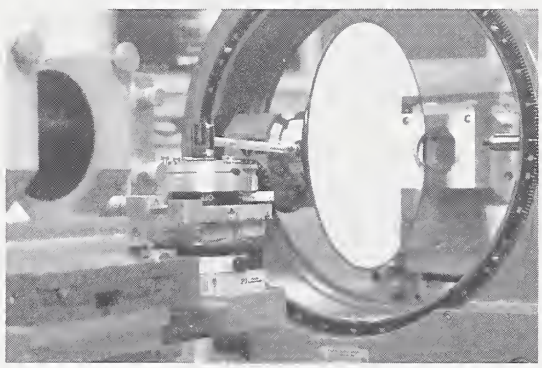
Funding Sources:
NIST OMP/NSMP
Physics Laboratory STRS
Cost Recovery

Project Goals

To provide an accurate system of measurements for structural parameters for semiconductor thin film and multilayer systems. Embodiments of the measurement system need to be non-destructive, non-invasive and give results robustly connected to the SI. In addition to development and application of these measurements, the project aims to communicate and disseminate this technology in the industry.



Customer Needs

Aside from the statements of specific needs found in the 1999 SIA ITRS, general scaling trends and increasing use of non-traditional materials in manufacturing require measurement technology of increased sensitivity and generality.

In our experience to date, the most frequent requirements have been associated with the calibration of metrology tools used in the control of developmental production processes. These tools have been developed to meet the needs for high measurement throughput and compatibility with the production environment. Such tools have material-dependent calibration requirements that lead end users and tool manufacturers to look for alternatives that are less sensitive to materials' properties and process variability.

Aside from average geometrical characteristics, there are additional requirements in specific applications such as internal microstructure within thin film layers and characterization of the interface region between layers for which needs have been encountered.

Technical Strategy

The program emphasizes the application of X-ray probes and methods to the characterization of thin films and their microstructures. This emphasis is based on the their small wavelengths, the ease with which they penetrate thin film structures, and the slow variation of their interaction coefficients with elements. Their phase velocities in solids differ only slightly from that in vacuum, allowing robust geometric metrology of thin layer stacks.

Our program develops and applies X-ray methods to reveal the microstructure of thin film and multi-layer structures produced by advanced semiconductor manufacturing. We also generate and certify reference structures for the calibration of in-line production tools. The main components of this work are the following: (1) Development and application of high-resolution X-ray diffraction techniques; (2) Advanced application of modeling methods to describe specular and diffuse scattering; (3) Production of reference samples of thin film and multi-layer structures; (4) Rapid response to urgent problems identified by International SEMATECH.

In addition to the development and application of these methods, we have made and continue to make frequent presentations to various specialized groups within the SEMATECH framework. Most recently this outreach has been extended to include the inaugural meeting of a Metrology working group in the framework of International SEMATECH.

Finally, we are in contact with commercial developers of X-ray instrumentation in order to

facilitate their interactions through the documentation of best practices and the production of reference materials.

*MILESTONE: **To have fundamental capabilities in place by the year 2000.***

1. High-resolution X-ray methods - A new high throughput large capacity diffractometer was built and commissioned in the previous fiscal year. This automated apparatus can accommodate 200 mm and 300 mm wafers, and has advanced beam preparation optics that offer combinations of resolution and flux optimized to specific applications.

2. Advanced modeling methods - Our original modeling software (developed in-house) has now been augmented by several public domain and commercial analysis packages. The problem of assigning meaningful uncertainties to the model parameters emerging from the fitting procedures needs attention. A highly qualified scientist will join this effort if support can be obtained for his/her participation.

3. We have established a reference materials production capability based on a highly developed ion beam sputtering apparatus. This facility produces single layer samples and multi-component multi-layer stacks with atomic scale resolution and reproducibility. In the last fiscal year, a second sputtering chamber was added which has the capacity to produce uniform coatings on 200 mm wafers. The exceptional quality of the structures produced in this facility supports their application as reference samples for other thin film measurement systems including those based on ellipsometry, and ultrasonic propagation. Over 30 materials are available for production of complex reference structures.

*MILESTONE: **By 2001, complete next generation high accuracy reflectometer.***

The basic goniometer, developed to our specifications under DOC SBIR funding by Optra, Inc. was delivered in late 1999. Commissioning and integration will be undertaken in 2000 with full operation expected by year's end.

*MILESTONE: **By 2002, develop a new approach to model-independent analysis of X-ray reflectometer data based on wavelet methods. This MILESTONE depends on securing the visit of an outstanding scientist from Moscow State University who has the needed capability and has indicated interest and willingness.***

Accomplishments

- Rapid responses to urgent problems - Our development of improved measurement and production capability has been staged so as to maintain rapid and effective response to urgent industrial needs. Among the systems we have addressed in this context are: advanced oxynitride dielectrics, Ta_xN_y copper diffusion barriers, high-k materials such as tantalum pentoxide and barium strontium titanate, and a group of metal stacks including Cu, Ta, Cu/Ta, Ta_xN_y and W_xN_y films. In each case a summary report has been completed including the data obtained, its analysis and interpretation.

FY Deliverables

Book chapter

A book chapter is in initial draft form. The book is to be edited by Alain Diebold who has a publishing contract in place.

Publications

Remmel, T., Schulbert, M., Singh, K., Fujimura, S., Owens, S., Deslattes, R., Pedulla, J., Averitt, J., Barium Strontium Titanate Thin Film Analysis, Proceedings of 1999 Denver X-ray Conference, Advances in X-ray Analysis (in press).

Compositional Metrology for Next Generation Gate Stack Materials

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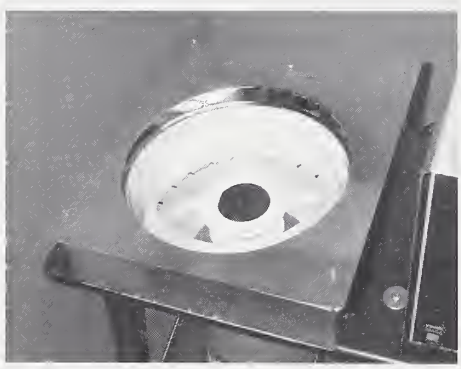
Project Goals

The goals for this project are two-fold:

1) develop an approach to fabricate BST ($Ba_{1-x}Sr_xTiO_3$) thin film reference standards; and 2) develop the capability to analyze films with thicknesses ranging from hundreds of nanometers (where metrology tools exist) down to a few atomic layers. The design goal for the fabrication facility is to produce highly stoichiometric films with compositional precisions on the order of 1 % relative or better. Analytical goals include the refinement of various electron-beam-based microanalytical methods to obtain high-accuracy quantitative results while investigating issues necessary to obtain highly accurate composition measurements of increasingly thinner layers. X-ray and backscattered EBSD, FESEM, TEM, AEM, SAM, and HREM will be used to characterize film microstructure; and film thickness will be measured by reflectance mode spectrophotometry, multiple-voltage electron probe microanalysis, analytical electron microscopy, and grazing incidence X-ray reflectivity.



Customer Needs

The 1999 SIA ITRS projects that gate dielectrics with oxide equivalent thicknesses down to 1 nm will be required in the N+2 or 3 technology nodes. To achieve the necessary performance of CMOS transistors, several materials and structures are under consideration. High dielectric materials, e.g., silicon oxynitrides, barium strontium titanate, tantalum oxide, and aluminum oxide, are promising candidates. The properties and performance of these materials are highly dependent upon thickness and composition, so analytical methods for precise film fabrication, both thickness and composition, and highly accurate determination of film composition are critical.

Technical Strategy

Spin coating was selected as the technique for fabricating the film standards. The precursor solution for the spin coating process is highly stoichiometric, with molar ratios $Ti/(Ba+Sr) = 1.00 \pm 0.01$ and $Ba/Sr = 2.43$. Films fabricated from this solution will have the same composition precision as the precursor and thus may be used as reference standards in the analytical measurements. The analytical work will begin with relatively thick BST films, where film composition, thickness and density can be measured with high accuracy using established methods.

Various electron probe-based microanalytical methods will be used to obtain quantitative results while investigating issues necessary to obtain high accuracy composition measurements of increasingly thinner layers. Many of the existing analytical correction procedures currently used for analysis of thin films as MVEMPA, AEM/EDS and electron EELS, low voltage probe analysis, and Auger spectroscopy must be significantly modified to obtain accurate quantitative results on the BST system. The spin-coated films will provide the means to investigate the necessary analytical correction procedure modifications and to determine realistically achievable accuracy levels.

Film microstructure will be characterized by X-ray diffraction, SEM, TEM, and HREM, and film thickness will be measured by reflectance mode spectrophotometry and grazing incidence X-ray reflectivity; knowledge of the film microstructure and thickness is important for interpretation of the composition measurements.

MILESTONES: For FY 2000 . . .

Modify processing conditions (spin rate, precursor solution composition) to fabricate BST films of reduced (< 70 nm) thickness.

Improve measurement precision on Ba-Sr-Titanate layered samples, concentrating on the effects of mild surface charging and Si-K X-ray peak overlaps with Sr-L X-ray peaks.

Characterize the microstructure and the thickness of existing films.

Determine the minimum thickness of continuous BST films fabricated by spin coating.

MILESTONES: For 2001 . . .

Develop a spin coating procedure for a different dielectric candidate material; e.g., tantalum oxide, aluminum oxide.

Develop a simpler, salt-based BST precursor solution for spin coating.

Investigate/develop methods to analyze the chemical phase and homogeneity of BST thin films by EBSD.

Provide cross-comparison information on compositional characteristics and compositional and thickness homogeneity by EBSD, multivoltage EPMA, and by AEM imaging and analysis of cross sectioned samples.

Determine homogeneity in depth of Ba-Sr-Titanate layered samples by combined ion sputtering, Auger electron spectrometry, and X-ray emission analysis.

Compare analytical measurements of composition and thickness of Ba-Sr-Titanate layered samples by EPMA and Auger electron spectrometry.

Accomplishments

- We have developed analytical methods and correction procedures to characterize BST films using MAP-EPMA . Samples are analyzed at each of several carefully chosen electron beam energies using wavelength dispersive X-ray analysis. The X-ray intensity data are processed using procedures developed in at NIST and yield independent estimates of both layer composition and thickness. In well-behaved cases the estimates of thickness and composition agree to better than 5% relative and agreements with other techniques (such as RBS spectrometry) are as good as 2% relative.
- A MOD facility has been set up to fabricate BST thin films. The facility consists of a programmable spin-coating apparatus (purchased with IE funds from NSMP), several temperature-calibrated hot plates, and an oxygen atmosphere annealing furnace. Two liters of stoichiometric BST metalorganic source solution of precise composition ($Ti/(Ba+Sr) = 1.00 \pm 0.01$, $Ba/Sr = 2.43 \pm 0.05$) were obtained for the production of the films.
- BST thin films have been deposited on 2" diameter (100) silicon wafers in the MOD facility. Preliminary experiments were conducted using four different solvents: ethylene glycol, propylene glycol, propylene glycol methyl ether, and EGME. The highest quality films (uniform surface appearance, very few streaks or bare spots) were fabricated from the EGME-containing solutions.
- Selected films were measured XRD for crystalline phase identification XRF spectrometry for composition and thickness. BST was found to be the only crystalline phase in the films. The one film measured by XRF had a composition of 49.7 %Ti, 37.3 %Ba and 13.0 %Sr, and a BST thickness of 58 nm.
- A substrate surface cleaning procedure was developed that permitted the deposition of smooth, optically-uniform BST films on 2" silicon wafers.
- Film thickness profiles of selected specimens were measured by reflectance mode spectrophotometry. The BST film thickness values ranged from 70 nm to 120 nm. For each specimen measured, the thickness values agreed to within ± 4%, indicating good thickness uniformity.
- An exploratory experiment to fabricate specimens that would permit a combinatorial approach to film evaluation was conducted. Pieces of both the homogeneous BST film and the combinatorial "dot" film specimens were provided for composition analysis.

FY Deliverables

Several preliminary BST reference thin films have been produced in the new metalorganic deposition facility.

Publications

Armstrong, J.T., Quantitative Electron Probe Microanalysis: Fifty Years of Developments in the Application of castaing's "Z" and "A" Corrections, Microscopy and Microanalysis, Vol 5 Supplement 2, Springer, 1999, p. 560.

Kaiser, D. L., Vaudin, M. D., Rotter, L. D., Bonevich, J. E., Levin, I., Armstrong, J. T., Roytburd, A. L., and Schlom, D. G., Effect of Film Composition on the Orientation of (Ba,Sr)TiO3 Grains in (Ba,Sr)yTiO2+y Thin Films, J. Materials Res., vol. 14, 1 (1999).

Ultra-Thin Dielectric Reliability Metrology

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NIST OMP/NSMP
NIST STRS

Project Goals

Provide technological leadership to semiconductor and equipment manufacturers by developing and evaluating the methods, tools, diagnostic procedures, data, and physical models for understanding and improving the reliability of (1) ultra-thin silicon dioxide and alternative gate dielectric films, and (2) metal interconnects, such as copper, used in advanced CMOS technologies.

Test wafer being loaded on wafer prober for long-term dielectric testing.

Customer Needs

Ultra thin gate dielectrics for future microelectronic device scaling are regarded as one of the most difficult challenges by the 1999 SIA ITRS. As the semiconductor industry continues to scale device dimensions to achieve channel lengths below 180 nm, gate dielectrics must be scaled to have an equivalent thickness below 2 nm. Ultra-thin SiO_2 dielectrics exhibit high tunneling currents, and the impact on device reliability is not well understood. The physics of failure and traditional reliability testing techniques must be reexamined for ultra-thin gate oxides that exhibit excessive tunneling currents and soft breakdown.

As device scaling continues, an alternative high-dielectric (high k) constant gate dielectric system will be required due to the excessive tunneling currents exhibited by sub-2 nm SiO_2 films. The 1999 SIA ITRS states that no suitable alternative high dielectric constant material has been identified with the stability and interface characteristics to serve as a gate dielectric. Years of research and development are required to identify and qualify a suitable alternative material.

This project focuses on (1) the physics of failure and the reexamination of traditional reliability testing techniques of ultra-thin SiO_2 gate oxides that exhibit excessive tunneling currents and soft breakdown, (2) providing an understanding of the electrical characterization methodologies and reliability characterization required for alternative high-k gate dielectrics for advanced CMOS devices, and (3) developing critical electromigration standards and metrology methods for advanced metallization systems, including copper.

Technical Strategy

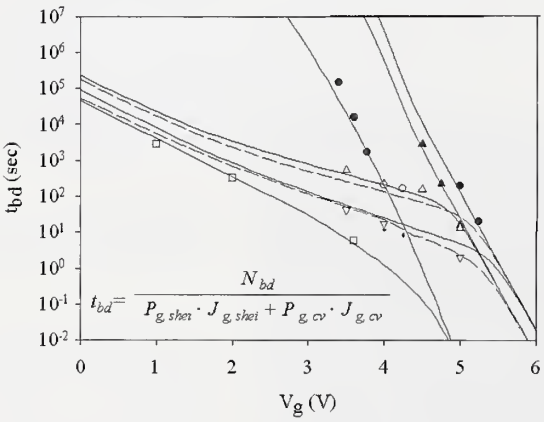
The physical mechanisms responsible for "soft" or "quasi" breakdown modes in ultra-thin SiO_2 films and its implications for device reliability will be investigated as a function of test conditions and temperature. Long-term time-dependent-dielectric breakdown tests will be conducted on SiO_2 films as thin as 1.5 nm at lower electric fields closer to operating conditions. These tests will be used to determine the thermal and electrical acceleration parameters of device breakdown. Experiments will be conducted to investigate the differences of gate oxide breakdown and wear-out due to high oxide field and hot-carrier injection. This study will provide insight into the physical mechanisms of ultra-thin gate oxide wear-out and breakdown.

MILESTONE: By 2000, reliability test patterns NIST 33 and 34 will be designed for experiments that include the determination of the precision of three electromigration standards: ASRM F1260 (constant current density and temperature test), JEP119 (SWEAT test), and JESD61 (isothermal test) for single-level metal.

Highly accelerated breakdown tests used to monitor manufacturing by the U.S. Semiconductor Industry must also be reevaluated for ultra-thin gate oxides. Traditional ramped voltage and current breakdown tests are not able to detect breakdown in films less than 4 nm thick. In FY98, a new voltage ramp technique had been

developed through a NIST-coordinated collaboration between the EIA-JEDEC and ASTM. A round-robin was planned and initiated to evaluated the new test. Twelve laboratories are currently participating. NIST will continue its leadership role in the JEDEC and ASTM standards committees.

MILESTONE: By 2001, a new standard constant voltage stress test will be developed for determining Time-Dependent-Dielectric Breakdown (TDDB) acceleration parameters in sub-3 nm thick SiO_2 films. The new test will utilize current or voltage noise as breakdown criteria when films exhibit soft breakdown. Such a test will find application by the Semiconductor Industry when qualifying new manufacturing processes.



Plot above shows model and data for the combined effects of substrate hot-electron injection and high voltage stress on the lifetime of ultra-thin gate oxides.

High dielectric constant (high-k) gate dielectric films will be obtained from key industrial and university groups. Electrical characterization methodologies will be developed to address various issues associated with these films, including large leakage currents, quantum effects, thickness dependent properties, large trap densities, transient (non-steady state) behavior, unknown physical properties, and the lack of physical models.

Examples of measurement problems that are being addressed include modifying and verifying electrical defect density measurement techniques, including conductance-frequency, capacitance-voltage, and charge-pumping.

MILESTONE: By 2002, electrical and reliability characterization methodologies and analysis will be established for high-k dielectric materials. These methodologies will include the characterization of interface electrical properties, dielectric integrity, and long-term electrical stability and reliability.

Accomplishments

- A systematic study of the uncertainties, sensitivity, and limitations of the conductance technique for extracting the interface state density of MOS devices with ultra-thin (< 3.0 nm) oxides was completed. Capacitance and conductance characterization MOS devices are used to determine properties such as oxide thickness, substrate doping, and interface state density. However, with the advent of ultra-thin oxides, effects such as tunnel current, series resistance, and quantum mechanical confinement in the substrate require additional consideration. This work provides a detailed analysis of the impact of these effects on parameter extraction using conductance and capacitance characterization of MOS devices with ultra-thin oxides.
- A new SRD program was initiated to provide the semiconductor industry with electrical and physical properties of alternative gate dielectrics MOS devices from peer-reviewed journal articles. The goal for the first year of the program is to collect articles representing the main body of knowledge on alternative dielectrics for silicon. Due to increased power consumption and device and circuit instabilities associated with ultra-thin SiO_2, a high permittivity gate with low leakage current and at least equivalent capacitance, performance, and reliability will be required. However, as compared to SiO_2, very little is known about the electrical and physical properties of these films as gate dielectrics. The formation of an SRD to document the properties of these materials would provide the semiconductor industry a comprehensive database of evaluated properties from a variety of sources to use in the further research and development of alternative gate dielectrics.
- A new study has been initiated to study soft breakdown in 1.3 nm to 2.5 nm SiO_2 films and to study the temperature dependence of time-dependent dielectric breakdown. A more dramatic temperature dependence of

wear-out has been observed and raises serious reliability concerns. The purpose of this study is to obtain the temperature dependence of time-dependent dielectric breakdown for films as thin as 1.3 nm and to determine if soft breakdown modes influence the temperature dependence. The reliability of gate oxides is becoming a critical concern in advanced CMOS technologies where devices will operate with higher gate electric fields and direct tunneling currents. The physical mechanism responsible for new "soft" breakdown modes and its implications for device reliability will be investigated as a function of test conditions and temperature. These tests will provide critically important field acceleration parameters and thermal activation energies that are required for reliability extrapolation of ultra-thin oxides.

- A new research program to develop metrology for the semiconductor industry's next generation gate dielectric has been established at NIST. The program concentrates on the development of techniques and analysis for the electrical and reliability characterization of alternative dielectric materials for advanced microelectronics. Collaborations have been established with Texas Instruments, University of Delaware, the SRC/SEMATECH Front End Processing Center, the University of Minnesota, North Carolina State University, and Lucent Technologies. Thin gate dielectrics for future device scaling is regarded as one of the most difficult challenges by the 1999 SIA ITRS. No suitable alternative high dielectric constant material has been identified with the stability and interface characteristics to serve as a gate dielectric. Significant research and development are required to identify and qualify a suitable alternative material.
- Interconnect reliability test chips NIST 33 and NIST 36 were designed, fabricated, and are being used. These chips are a collection of test structures designed in collaboration with members of JEDEC Committee JC14.2 on Wafer Level Reliability and with industry researchers. They are vehicles for improving existing reliability standards and for developing new ones for interconnects that are based on the results of inter-laboratory and other experiments. Wafers of NIST 33 were fabricated by the Stanford Nanofabrication Facility using single-level metal structures of an Al 1% Si alloy. Wafers of NIST 36 were recently fabricated for NIST by Silicon Graphics (formerly Cray Research) using a cladded Al-1%Cu metallization. Inter-laboratory experiments with these wafers are underway with LSI Logic Corporation and Infincon Technologies serving as additional reference laboratories. NIST 36 contains a variety of single-level metal and via-type electromigration test structures for evaluating the designs of these test structures and their use in test methods to characterize the reliability of interconnects. It also includes structures to measure stress voiding, electromigration-driven noise, metal sheet resistance and linewidth, and oxide thermal conductivity. The availability of via-type test structures on NIST 36 is intended to stimulate critically needed activities in JEDEC for the development of metrology tools for characterizing stress voiding and electromigration in vias.

FY Deliverables

SRDs

SRD program on alternate dielectrics initiated (E. Vogel)

Collaborations

Revised JESD35 (EIA-JEDEC) procedures for wafer-level testing of thin oxides (J. Suehle)

Analog Devices, Dynamic Research Corporation, Fairchild Semiconductor, National Semiconductor, Lucent Technologies, Texas Instruments, Advanced Micro Devices, Motorola, National Microelectronics Research Center, Penn State University, University of Maryland, ultra-thin gate oxide reliability (J. Suehle)

CSTL/Process Measurements Division, University of Maryland, microhotplate-based sensor arrays (J. Suehle, M. Gaitan)

General Electric, Sterling Semiconductor, Cree Research, gate dielectrics on SiC (J. Suehle)

University of Maryland, George Washington University, MIT Lincoln Laboratories, microhotplate-based chemical sensors (J. Suehle)

Texas Instruments, electrical and reliability characterization of ultra-thin gate oxides (J. Suehle, C. Richter)

University of Delaware, alternative dielectrics (J. Suehle)

NIST Boulder, National Semiconductor, SEMATECH, Rowan University, electromigration of Cu interconnects (H. Schafft)

LSI Logic Infineon, interlaboratory electromigration experiment (H. Schafft)

UMC, Silicon Graphics, electromigration of Al interconnects (H. Schafft)

Statistical Engineering Division, temperature dependence of copper resistivity (H. Schafft)

SRC/SEMATECH Front End Processing Center, University of Delaware, University of Minnesota (TiO_2), N.C. State University (oxynitrides, nitrides, ultra-thin SiO_2), alternative gate dielectrics (E. Vogel)

University of Maryland, gate dielectric reliability (E. Vogel)

Standards Committee Participation

JEDEC JC14.2 Dielectric Working Group, Chairman
(J. Suehle)

ASTM, F-1 on Electronics, Subcommittee F1.11 on Quality and Hardness Assurance, member, FY 82-99 (H. Schafft)

EIA/JEDEC JC 14.2 on Wafer Level Reliability, Technical Advisor, FY 93-99 (H. Schafft)

Software

Windows-based electrical characterization software developed (E. Vogel)

Presentations/Talks

"Reliability Characterization of Ultra-Thin Film Dielectrics," at the ASTM Conference on Gate Dielectric Integrity: Material, Process, and Tool Qualification on January 25 in San Jose, CA. (J. Suehle)

"Round-Robin on GOI Measurements being Conducted in the USA," at the ASTM Conference on Gate Dielectric Integrity: Material, Process, and Tool Qualification on January 25 in San Jose, CA. (J. Suehle)

"Ultra-Thin Film Oxide Reliability," NASA Jet Propulsion Laboratory, Pasadena, CA, January 25, 1999. (J. Suehle)

"Properties of N- and P- Channel MOSFETs with Ultra-thin RTCVD Oxynitride Gate Dielectrics," Electrochemical Society Spring Meeting, Seattle, Washington, May 5, 1999. (E. Vogel)

"Reliability of Ultra-thin Oxides for MOS Devices," Short Course at North Carolina State University, Dept. of Electrical and Computer Engineering, April 22, 1999. (E. Vogel)

"Alternative Dielectric Technology and Metrology," University of Delaware, Dept. of Electrical and Computer Engineering, July 13, 1999. (E. Vogel)

Publications

Allen, R. A., Vogel, E. M., Linholm, L. W., and Cresswell, M. W., Sheet and Line Resistance of Patterned SOI Surface Film CD Reference Materials as a Function of Substrate Bias, the Proceedings of the 1999 IEEE International Conference on Microelectronic Test Structures, Goteborg, Sweden, March 15-18, 1999, pp. 51-55.

Milanovic, V., Bowen, E., Tea, N., Suehle, J. S., Payne, B., Zaghloul, M., and Gaitan, M., Convection-Based Accelerometer and Tilt Sensor Implemented in Standard CMOS, Proceedings of the 1998 International Mechanical Engineering Congress and Exposition, Anaheim, California, November 15-20, 1998, pp. 487-490.

Chemical Characterization of Thin Films and Particle Contaminants

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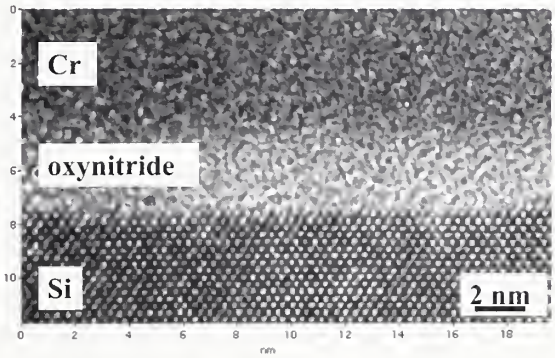
NIST OMP/NSMP

Project Goals

To make measurements on sets of well-prepared thin-film insulator samples that will highlight discrepancies between well-established techniques. Using an iterative analysis between the methods, we aim to arrive at corrections that can be applied to each technique to give them absolute subnanometer accuracy in the thickness range of 1 nm to 8 nm.

A second objective is to develop analysis methods to improve the accuracy of analysis for particles less than 100 nm in size. Our approach is to employ new chemical measurement technologies such as the X-ray microcalorimeter detector, high-speed silicon drift detectors, and EBSD. Finally we plan to develop analytical standards in support of these measurements efforts.



Customer Needs

Dielectric gate insulators proposed for future CMOS devices present problems in chemical state and layer thickness determination when the thicknesses become less than 8 nm. While individual measurements of thickness are capable of great precision, absolute accuracy depends on techniques and data inputs which are not yet refined to the level required. Improvement in this measurement accuracy requires the development of new techniques, the reanalysis of old techniques, and an improvement in the data that are used to analyze Si and the dielectric layers that can be grown on it.

In addition, as the analytical demands, both spatial resolution and composition, increase for the next generation devices the need to analyze and identify increasing smaller particle contaminates becomes critically important. Improvements in the analysis of ultra fine particles, less than 100 nm in size, will require the development of new analytical techniques employing low voltage electron microscopy coupled with low energy X-ray analysis including low-voltage EBSD.

Technical Strategy

Silicon wafers grown with thin films of silicon oxide or silicon- oxinitride layers are used as characterization samples because it is possible to grow layers of great interface smoothness and homogeneity. These include samples obtained from SEMATECH and other sources.

We are refining two existing techniques, EPMA and AEM cross-sections to give accurate chemical and thickness determinations. This includes 1) the development of capping for the thin dielectric overlayers on Si which eliminates uncertainties in observing the oxide layer in TEM cross sections and 2) the upgrade of data acquisition of the analytical electron microscope. For EPMA new procedures must be adapted to correct from bulk analysis programs to multiple thin layer specimens and modeling to test the results.

We are developing a new technique, GIXPS, which obtains both thickness and chemical state information by taking advantage of the optical constants in overlayers at soft X-ray energies, as well as the binding energy dependence in photoemission that the chemical constituents of the layers manifest. This promises to provide better constraints on compositions than simple angle resolved X-ray photoemission spectroscopy when multiple layers are involved.

The measurements of the insulating layer thicknesses and compositions are correlated where possible with additional measurements using ellipsometry, atomic force microscopy, and X-ray reflectometry to constrain thicknesses and determine the effects of surface and interface roughness. Finally, it is necessary to investigate the accuracy of the data that provides the inputs to the thickness determinations. Cross-sections, optical constants, densities, and inelastic electron mean free paths have to be known to an accuracy of a few percent in order to obtain reliable thicknesses. An iterative process between the different methods of measurement should provide indications of anomalous values in the inputs, particularly where there are discrepancies between different data compilations.

In addition we plan to use a combination of ion sputtering, Auger electron spectrometry, multiple accelerating potential X-ray emission analysis, and soft X-ray spectroscopy to provide accurate elemental analysis and chemical species determination of layered thin films and particles. We are about to install a unique high resolution, UHV, FEASAM, fitted with energy and wavelength dispersive X-ray detectors that will be used for these studies. The high spatial and depth resolution capabilities of such an instrument make it especially useful in analyzing the type of samples that are of interest in this field. Analytical developments will include extensive analysis of standards, refinement of Monte Carlo algorithms for modeling the behavior of low energy electrons, and improvement of the correction methods.

MILESTONES: FY 2000

Improve the focus of the synchrotron beamline optics to concentrate the X-ray flux for GIXPS measurements.

Develop small angle cleavage technique for rapid TEM cross section sample preparation.

Improve measurement precision on $Si(O,N)_x$ layered samples, concentrating on the effects of mild surface contamination by C or F in the shapes of the background near the N and O peaks.

Develop methods for quantitative particle analysis employing low voltage electron beams and the NIST microcalorimeter X-ray detector.

Develop methods to identify the chemical phase of individual submicrometer particles using backscattered electron diffraction.

Analyze oxide and selected SEMATECH samples using combines Auger electron spectroscopy with ion sputtering and multiple accelerating potential X-ray emission analysis. 9/01

MILESTONES: FY 2001

Refine analytical and correction procedures for simultaneous Auger electron spectroscopy and multiple accelerating potential X-ray emission analysis of layered thin specimens and particles.

Correlate soft X-ray emission spectra and Auger electron spectra of standards samples to refine means of determining surface chemistry with these techniques and compare with analyses of selected oxide and SEMATECH samples.

Analyze oxide and selected SEMATECH samples with complementary thickness techniques of multi-wavelength ellipsometry and X-ray reflectometry.

Provide cross-comparison information on compositional characteristics and compositional and thickness homogeneity by GIXPS, Auger spectrometry, soft X-ray emission spectroscopy, and by TEM cross-sectional images.

Accomplishments

- SEMATECH silicon oxynitride samples have been measured using GIXPS on the X-24A synchrotron radiation beamline at the National Synchrotron Light Source.
- The variation of thickness and layer density obtained by GIXPS was modeled from uncertainties in X-ray optical constants, inelastic electron mean free paths, and photoemission cross sections.
- Developed analytical protocol for analyzing SiO_2 and $Si(O,N)_x$ thin layers on Si metal substrates. Determined optimal correction procedures for analysis of O and N in silicon bulk matrices. Determined their accuracy and self-consistency of results at various electron beam accelerating potentials.
- Data from two samples of SiO_2 thin films on Si metal substrates previously measured by GIXPS were analyzed by multivoltage electron probe analysis to obtain chemical constituents and thicknesses.
- Performed Monte Carlo simulations to determine optimum electron beam accelerating potentials to use when analyzing SiO_2 and $Si(O,N)_x$ layers of different thicknesses.

- Performed multiple-voltage EPMA analysis of SEMATECH samples of $Si(O,N)_x$ films on Si metal substrates.
- Multi-signal data acquisition system installed on the electron microscope to perform electron energy loss spectroscopy and energy dispersive X-ray spectrometry.
- SEMATECH silicon oxynitride samples were measured for thickness, film structure, and interface morphology, and roughness using TEM cross sections.
- Performed a series of EBSD measurements on standard particles to determine the ability of EBSD to identify the phase of individual submicrometer particles.

FY Deliverables

A suite of thin-film samples have been characterized by a series of complementary analytical techniques designed to measure composition and or thickness. The results of these analyses are being used to evaluate the discrepancies between the different techniques and to characterize the accuracy, precision, and measurement biases associated each.

Publications

Jach, T., Gormley, J., and Thurgate, S., Grazing Incidence X-ray Photoemission Spectroscopy of SiO_2 on Si, accepted for publication in Spectrochimica Acta B.

Small, J. , and Michael, J. Phase Identification of Individual Particles by electron Backscatter Diffraction (EBSD), Microscopy and Microanalysis, Vol 5 Supplement 2, Springer, 1999, p. 226.

High-Resolution Microcalorimeter X-Ray Spectrometer for Chemical Analysis

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Funding Sources:
NIST OMP/NSMP
Other Agency

Project Goals

Our broad goal is to use the unique low-noise, high-sensitivity properties of cryogenic electronics to create new generations of detectors for high-energy-resolution measurements of radiation from infrared through X-ray and for mass spectrometry of large molecules. With OMP's support, we specifically target the needs of the semiconductor industry for improved particle analysis through the development and demonstration of a complete microcalorimeter energy-dispersive X-ray spectrometer system.

Customer Needs

Improved X-ray detector technology has been cited by SEMATECH's ALMWG (now ALMC) as one of the most important metrology needs for the semiconductor industry. In the Metrology Roadmap section of the 1999 SIA ITRS, improved X-ray detector technology is listed as a key capability that addresses analysis requirements for small particles and defects. The TES microcalorimeter X-ray detector developed at NIST has been identified as a primary means of realizing these detector advances, which will greatly improve in-line and off-line metrology tools that currently use semiconductor energy-dispersive spectrometers EDS. At present, these metrology tools fail to provide fast and unambiguous analysis for particles less than approximately 0.1 μm to 0.3 μm in diameter. Improved EDS detectors such as the TES microcalorimeter are necessary to extend the capabilities of existing SEM-based instruments to meet the analytical requirements for future technology generations. To make this technology available to the semiconductor industry and other materials analysis communities, NIST has licensed several patents to two U.S. companies, EDAX and NORAN, for commercialization. With commercialization and continued development, microcalorimeter EDS should be able to meet both the near-term 1999 SIA ITRS goal of analyzing particles as small as 0.08 μm in diameter and the longer-term requirements of the semiconductor industry for improved particle analysis.

Technical Strategy

Introducing a radically new technology such as cryogenic microcalorimeters to a large community requires creating and demonstrating the entire measurement instrument, and not just the detector. In this case our project has developed superconducting electronics to read out the detectors, compact adiabatic demagnetization refrigerators to simplify cooling the detectors to milli-kelvin operating temperatures, and room temperature electronics to process the output signals. The resulting system makes a much more compelling case for the technology than the performance specifications of the detector alone.

The application of X-ray detectors to materials analysis problems in the semiconductor industry represents the test bed for this technology in house. The ability of the microcalorimeter detector to differentiate overlapping X-ray lines at low energies (< 3 keV) enables high-spatial-resolution analysis of small contaminant particles and other features of interest in semiconductor samples.

MILESTONE: By 2000 (ongoing), analyze samples as requested and supplied by SEMATECH companies to demonstrate microcalorimeter capabilities, with particular focus in FY00 on Cu-related analysis problems.

MILESTONE: By early 2000, demonstrate a capability to perform spatial mapping of the chemical bonding state of various elements. For example, image a sample differentiating Al from Al_2O_3 from the chemical shifts of the Al-K and satellite lines.

With improvements in the entire detector system (in particular, using a microcalorimeter EDS coupled to a field emission SEM), it is anticipated that the NTRS goal of identifying 0.08 μm particles should be achievable in the near future. To work towards this goal, we are currently collaborating with Dale Newberry (CSTL) to develop a microcalorimeter EDS for the field emission SEM located in Gaithersburg.MILESTONE: By mid 2000, construct and test ADR and associated

electronics for the Gaithersburg microcalorimeter system.

In addition, we are working to improve the microcalorimeter count rate in order to reduce analysis time. Our newly developed Mo-Cu photolithographic fabrication process will allow the development of arrays of microcalorimeters with greatly improved total count rate and larger area. One of our goals for this year will be to develop a small microcalorimeter array with a total count rate approaching that of the semiconductor EDS. With additional resources, we will also be able to optimize our single pixel detector design for higher count rate.

MILESTONE: By early 2001, fabricate and test a small (2 by 2) microcalorimeter array with a total count rate > 1000 cps.

MiILESTONE: By 2000 or 2001, with additional resources, design and fabricate single pixel microcalorimeters optimized for count rates of .1000 cps or higher.

As part of our push towards arrays, with support from both NIST and OA funding sources, we are also developing digital feedback electronics to read out the SQUID amplifiers to measure the current through the detectors. With further development, the system will allow real-time digital signal processing of microcalorimeter X-ray pulses; benefits include better energy resolution for real-time analysis and the ability to read out large numbers of detector channels without radically increasing system cost.

MILESTONE: By 2000, demonstrate the read-out of one detector channel using a digital feedback system.

Accomplishments

- Measured chemical shifts of sub-micrometer particles to distinguish Al, Al oxide.
- Measured chemical shifts in Ti-L lines to distinguish Ti, TiOx and TiN.
- New "best-in-world" energy resolutions: 4.5 eV at 5.9 keV and 2.0 eV at 1.5 keV.
- Implementation of real-time nonlinearity correction simplifies operation.
- Commercialization in progress, licenses signed with EDAX and NORAN.

FY Deliverables

Recognition:

Department of Commerce Gold Medal, 1998

NIST Applied Research Award, 1998

Patents:

"Particle Calorimeter with Normal Metal Base Layer", Issued June, 1997.

"Superconducting Transition-Edge Sensor", Issued March, 1999.

"Microcalorimeter X-ray Detectors with X-ray Lens", Issued March, 1999.

"Mechanical Support for a Two Pill Adiabatic Demagnetization Refrigerator" Issued August, 1999.

"Superconducting Transition-Edge Sensor with Weak Links, Filed Nov., 1998.

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Interconnect Materials and Reliability Metrology

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Project Goals

Modern multiplayer interconnects, composed of layered metal and dielectric thin films, must withstand severe conditions: triaxial tensile stresses due to passivation, and mechanical/thermal stresses caused by high current density. This project focuses on three areas an their goals are the following:

Interconnect Reliability

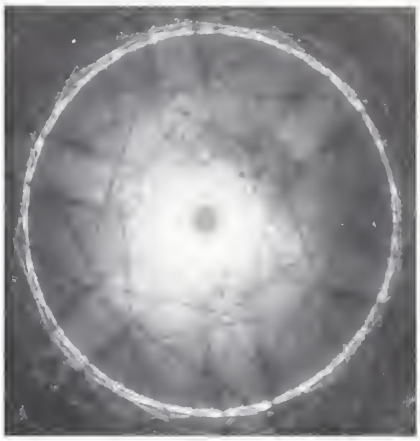
- Develop, evaluate and refine test structures, test methods and diagnostic procedures to improve reliability of metal interconnects.

Mechanical behavior of Interconnect Films

- Develop experimental techniques for measuring the mechanical properties of thin films, including basic tensile properties, fatigue, and fracture resistance, in specimens fabricated and sized to match materials used in actual commercial devices;
- Relate thin film mechanical behavior to microstructure;
- Extend test techniques from their present level (1 μm thick, . 10 μm wide) to smaller specimens that are similar in size to the conductive traces used in contemporary VLSI circuits (widths of 0.1 μm to 1 μm).

Microstructural Influences on Interconnect Reliability

- Support the semiconductor industry by performing basic research and developing novel measurement methods using established experimental techniques such as electron microscopy.
- Develop a mechanistic understanding of the microstructural processes controlling stress voiding (SV), electromigration (EM), and residual mechanical stresses in interconnects.



- Assess and, when necessary, modify microstructurally-based models that sufficiently describe similar behavior in bulk metals.

Customer Needs

Test structure designs and test methods for characterizing copper interconnects will also be developed in collaboration with partners in the Semiconductor Industry. Special NIST-designed test chips include numerous structures for evaluating via and straight line electromigration and will be used as a vehicle to develop and validate test procedures and analysis techniques.

Technical Strategy

Interconnect Reliability:

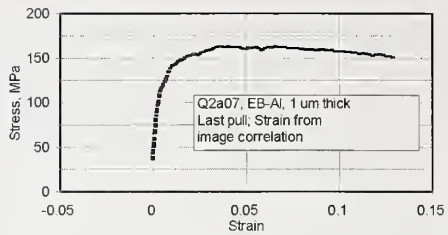
Test structure designs and test methods for characterizing copper interconnects will also be developed in collaboration with partners in the Semiconductor Industry. Special NIST-designed test chips include numerous structures for evaluating via and straight line electromigration and will be used as a vehicle to develop and validate test procedures and analysis techniques.

Mechanical behavior of Interconnect Films:

The main track in the technical approach continues be to develop thin-film tensile test techniques that are the same in principle as standard macroscopic tensile tests. The key element with thin films is that the specimens are

so small and delicate that they cannot be handled directly. Hence a handling strategy must be utilized. The framed tensile specimen is one answer. This specimen consists of a frame that carries a tensile coupon. The frame is conveniently handled, for attachment to the grips of the testing device and for alignment. Just before the test, the frame is carefully cut. This strategy can be applied where photolithography and etching techniques allow the definition of the frame geometry. Typically, the frame is patterned in the substrate. The main challenge in specimen fabrication is chemically removing the substrate in the interior of the frame, and especially from underneath the specimen, without damaging the specimen. The classic example is aluminum and copper films on silicon substrates. Most popular silicon etchants, such as potassium hydroxide, dissolve aluminum rapidly. We have used hydrazine hydrate for etching away silicon under aluminum tensile coupons. The main challenge in conducting the test is cutting the frame without damaging the specimen. With silicon-framed specimens, we have had good results using a dental drill for this purpose.

It is questionable whether the silicon-framed tensile specimen will work for specimens with widths below 10 µm. The specimens may be too delicate. Building on the "skyhook" approach discussed in last year's report, we have developed this year a new conceptual approach to these tests, which we call the force-probe tensile test (see title photo). The specimen film is deposited on silicon and patterned into a tensile strip, 10 µm wide by 200 µm long at present, surrounded by a frame of the specimen film. The tensile strip is connected to this frame at one end, but the other ends in a tab about 150 µm wide with a 50 µm hole in it. The tab is tethered to the frame with thin strips of the specimen film. The silicon is etched away from the under specimen and from the surrounding area within the frame, to a depth of about 50 µm, using xenon difluoride. The force probe is similar to a micromanipulator-mounted needle probe used to make electrical contact to thin-film conductors on silicon wafers, with three important differences: the probe tip is reshaped to form a hook, to serve as the "skyhook;" a force sensor is added between the probe tip holder and the micromanipulator.; and the micromanipulator is motorized with very accurate positioners on all 3 axes. Tensile testing is carried out under a microscope by, first breaking the tethers to free the specimen, and then engaging the specimen



tab end with the force-probe's hook and pulling until the specimen fails. The displacement comes from the micromanipulator motor, and is controlled by computer. The force is measured by the force sensor. The displacement is measured by digital image correlation of a series of typically 100 images obtained during the test.

In initial tests of aluminum films under the optical microscope, the strength of 1 µm thick aluminum films, made in the same way as previously tested films, was similar to the previous results. The forces involved were much smaller, about 2 milligram-force. However these tests revealed a surprise: the elongation to failure of these 10 µm wide by 200 µm-long films was up to 20 percent, while that of 200 µm wide by 700 µm long specimens has consistently been around 1 percent.

In the force-probe tensile test, the elongation is measured using digital images. Optical images will not suffice for few- and sub-micrometer-width specimens. Therefore, fixtures for performing this test within the specimen chamber of an SEM were sought. This year, progress items included development, fabrication, and testing of a set of apparatus for force-probe tensile tests within the chamber of the NIST 853 SEM, including the force sensor and a micromanipulator with inchworm-style piezoelectric motors on 3 axes.

MILESTONE: In FY2000, design and submit to MOSIS a test structure for tensile testing of metal interconnect layers.

The force-probe approach has scored some successes in experimental tests of some materials that could not be successfully tested by the silicon-frame approach: SiO_2 and intermetallic Al_3Ti. Both of these materials are quite brittle. In both cases the specimens on the wafer failed during the process of etching the silicon away using hydrazine hydrate. When tensile tests were attempted with surviving specimens, the

specimens broke during the cutting of the silicon frame. In the new approach, xenon difluoride can be used for the silicon etch, and it is better than hydrazine hydrate on two counts: first, it is a gas, rather than a liquid; second, it is less aggressive than hydrazine hydrate. And, the smaller specimens seem more robust. Some damaged and broken specimens were seen on the wafers after fabrication, but many were intact. A few successful experimental tests were achieved.

Microstructural Influences on Interconnect Reliability:

The primary reliability issue in this project is the formation and growth of voids in interconnects due to the development of severe tensile stresses; such voids can lead to open circuit failures. Stresses result from differential thermal expansion among the metal, substrate and rigid passivation overlayer, or from atomic flux divergences due to strongly non-uniform local diffusion during electrical current stressing. Complicating matters is a new issue associated with the integration of copper into chip-level interconnects, namely the development of residual stresses that vary with time. Such stresses are believed to originate from the presence of impurities introduced during the electrodeposition process, and may play an important role in both the measurement and control of SV and EM reliability. Interconnects become less homogeneous as dimensions scale downward, since the structures then comprise individual grains through the film thickness and across the line width. Behavior also becomes less homogeneous, and even small variations in microstructure can have detrimental effects on reliability. Measurement research must focus on methods that can resolve spatially these microstructural variations.

One approach to controlling interconnect reliability centers on the fact that stress- and electromigration voids typically nucleate at intersections of metallization grain boundaries and the passivation/interconnect interface. Interface flaws serve to decrease the activation energy for void nucleation according to thermodynamic calculations. In addition, debonded regions can modify the local stresses in the interconnect line. In an attempt to control the occurrence of voids, we perform interface modification by controllably depositing photoresist onto patterned metal lines prior to passivation deposition. Accelerated testing then reveals how voiding has been changed from non-modified structures.

Another novel approach to interconnect reliability control focuses on the measurement of microstructure distributions within thin films using SEM, and the concurrent determination of property distributions. The complete structure of grain boundaries can be measured by automated orientation mapping methods and analyzed in a statistical manner. Individual boundary structures are then related to specific properties such as diffusivities. This allows for the determination of a property map of thin film microstructure, which could potentially be incorporated into interconnect design rules for SV and EM reliability.

The issue of understanding stresses in narrow interconnects is addressed by TEM methods to measure lattice constants in damascene copper interconnects with high precision. This approach requires very specialized knowledge of diffraction effects in crystals, and hence we are actively collaborating with a world leader in this field (Max-Planck-Institut für Metallforschung). We relate our localized measurements to global measurements that are more typically used by industry; this is done via collaboration with Lucent Technologies.

*MILESTONE: **In 2000, make first SEM measurements of complete grain boundary structures.***

Grain boundaries have historically been investigated through the fabrication of geometrically simple bicrystals. For this work to be useful to industry, we must make them on more relevant boundary distributions, such as those that form in thin films. Also, we must gather such data from a large number of boundaries in order to accurately predict transport properties.

*MILESTONE: **In 2000, make first measurements of crystal distortions in copper specimens, with extrapolation to interconnect stress and strain states.***

Interconnect stress measurement requires quantitative knowledge of dynamical diffraction effects in crystals, which are not insignificant in copper. Models exist, however, to begin such

assessments. Further, we must quantitatively understand the effects of TEM specimen thinning on specimen stress relaxation.

This requires specialized TEM holders that allow for both electrical current flow as well as heating, both within the microscope. Further, energy filtering of the diffraction patterns should allow for the acquisition of useful data at elevated temperatures that simulate accelerated testing conditions.

*MILESTONE: **In 2001, make measurements of crystal distortions in specimens that are undergoing electromigration stressing.***

Accomplishments

- Successful tests of aluminum films using the force-probe technique under the optical microscope.
- Force-probe apparatus installed and operated in SEM.
- First successful tensile tests of thin films in the SEM with the force-probe.
- Tested electrodeposited gold films from Hutchinson Technology. Specimens with six heat treatments were tested using the copper-foil-frame tensile specimens and the piezo-actuated tensile tester.
- Completed EM and SV testing on passivated aluminum alloy interconnects containing modified interfaces. Observations indicate that void densities are increased in modified regions, presumably due to changes in void nucleation energies. Potential competition between decreased nucleation energies and kinetically favorable sites for rapid void growth depends upon the distribution of grain boundary structures within the unmodified regions.
- Developed methodology for performing convergent-beam electron diffraction measurements of lattice constants in damascene copper interconnects. Preliminary results indicate that elastic lattice strains in the range 0.1 to 0.3% can be routinely detected. Have laid out the framework for automating the process, as well as for improving strain resolution.

FY Deliverables

Demonstrate tensile testing in the SEM by the force-probe technique with automated, rapid acquisition of a series of images to allow measurement of the progressive elongation of the specimen.

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Measurements for Electrodeposited Copper Interconnects

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NIST OMP/NSMP
NIST STRS

Project Goals

The primary objective of our research is to provide the electrodeposition community with a better understanding of the mechanism by which organic addition agents inhibit the copper deposition reaction which in turn promotes the bottom-filling of trenches and vias used for on-chip metallization. An additional goal is to provide an understanding of the factors controlling the recrystallization behavior of copper electrodeposits, particularly with respect to additive chemistry. A proper model of the recrystallization process would help industry design the deposition conditions and subsequent sequence of processing operations such as thermal anneals to obtain the maximum performance.

Customer Needs

As cited on page 99 in the 1999 SIA ITRS, the introduction of copper metallization and low dielectric constant materials should lead to a six-fold improvement in signal delay. The introduction of these new materials also represents the most difficult interconnect challenges in the near future. Current and future feature scaling requires metallization into vias and trenches with aspect ratios as high as 10:1. An advantage of Cu electrodeposition over Al physical deposition is the ability to 'superfill' high aspect ratio features when inhibitors are added to the plating bath. These addition agents are also responsible for grain refinement in the deposited material, which subsequently leads to recrystallization and an order of magnitude increase in grain size. Recrystallization results in a 20 % to 25 % decrease in resistivity and is necessary to achieve the required electrical resistivity and electromigration resistance. Although a phenomenological understanding of the influence of additives exists, a molecular level view of this process is totally absent. Consequently, there is a tremendous need for developing a predictive capacity for describing the influence of

electrolyte species on the evolution and properties of electrodeposited Cu films.

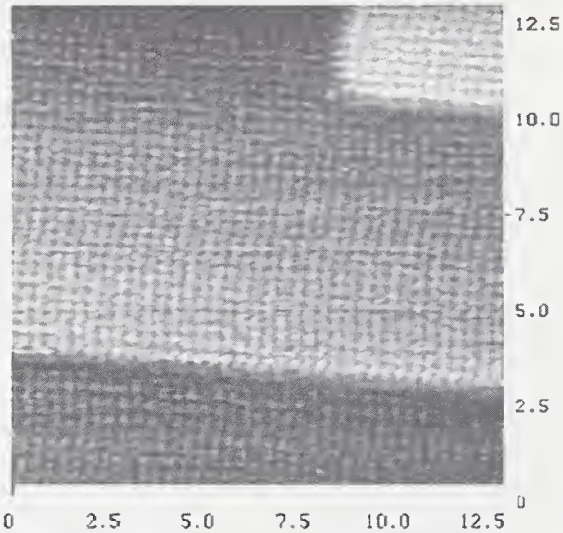
Although it is recognized that copper inhibition is critical to achieving superfill, the overall mechanism and role of each additive in achieving superfill is under debate. Current models attempting to describe superfill are based on assumptions about the surface dynamics of the additives that have little experimental basis. Consequently, predictions of process extendibility to feature sizes of 150 nm and smaller may not be reliable.

Technical Strategy

Our research activities will focus on the incorporation of additives in electrodeposited copper and the correlation of the copper recrystallization kinetics to these impurities. We have recently developed a copper plating bath that produces copper films with recrystallization behavior identical to that reported in the literature. The superfill capability of this bath is currently being evaluated. The principle addition agents in this bath are NaCl, sodium 3-mercapto-1propanesulfonate (MPSA), and polyethylene glycol (PEG). Significant room temperature recrystallization is observed only when MPSA and PEG are present in the electrolyte together, particularly in the presence of chloride. The influence of deposition current density and film thickness on the recrystallization kinetics has yet to be examined.

We have determined from *in-situ,* high resolution scanning tunneling microscopy (STM) studies that chloride is strongly adsorbed on the copper surface and forms ordered adlayers at saturation coverage (see picture on next page). Moving the potential towards negative values leads to an order-disorder transition and eventual desorption of the chloride adlayer. In the case of the above polyether-sulfide-chloride electrolyte, the ordered chloride adlayers formed on immersed copper surfaces likely facilitate the formation of a well ordered organic layer which inhibits copper deposition. The blocking nature of this organic overlayer may be subsequently disrupted at more

negative potentials where the halide layer becomes mobile due to an order-disorder or some other phase transition. It is likely that competitive adsorption of MPSA onto the copper surface contributes to the destabilization of this inhibiting Cl-PEG film.



A 13 x 13 nm STM image of (√2 x √ 2)R45° chlorine adlattice on Cu(100) at -0.169 V vs. Cu/Cu^+ in 10 mmol/L HCl.

MILESTONE: By 2000, determine the recrystallization kinetics of copper films as a function of deposition current density and film thickness.

We have developed a copper electrolyte chemistry which produces copper films with recrystallization behavior consistent with that reported in the literature. However, it is not clear how the recrystallization kinetics are influenced by the electrodeposition current density and film thickness, both of which will change as feature sizes continue to decrease.

MILESTONE: By 2000, determine the feasibility of using VR-SFG to characterize adsorption behavior in polyether-sulfide-chloride electrolytes.

VR-SFG provides a unique opportunity to probe the electrolyte/copper electrode interface, while under potential control, in the copper plating bath. Although this technique has been successfully applied to examine the chemically similar mercapto-octadecane covered gold surface, it has yet to be applied to the thiol-sulfonate/copper surface.

MILESTONE: By 2001, determine the impurity levels (C,N,O,S) as well as the defect density in electrodeposited copper films.

To properly characterize the structure and dynamics of the solid/electrolyte interface and to specifically determine the role of the inorganic and organic adsorbates on the evolution of thin film microstructure and morphology requires the development and implementation of new *in-situ* measurement methods. Vibrational spectroscopy is a powerful tool for the study of surfaces that is complementary to STM. Because each chemical bond has a characteristic vibrational frequency, vibrational spectroscopy can determine the identity of species adsorbed at surfaces, and the nature of the adsorption, i.e. whether the parent molecule stays intact, or fragments upon interaction with the surface. Detailed analysis of vibrational spectra can provide information on the local order of species, and their orientation. Traditional vibrational spectroscopies, such as IR absorption or Raman scattering are difficult to apply to *in-situ* studies of electrodeposition, as species in the electrolyte, and the electrolyte itself, can produce large competing signals. However, the nonlinear optical technique of vibrationally resonant sum frequency generation (VR-SFG) is uniquely interface specific and can be applied to the *in-situ* study of electrodes.

SIMS is being used to examine the impurity levels in copper electrodeposits. In addition X-ray diffraction peak profiles will be analyzed in terms of particle size, microstrain (edge and screw dislocations) and stacking faults using a modified Williamson-Hall approach and also the Warren-Averbach method. Early results show that films that recrystallize rapidly initially have a large screw dislocation density and also a high density of stacking faults.

Accomplishments

- We have begun to isolate the effects of individual additives on the room temperature recrystallization of electrodeposited copper. Adsorbed chloride limits the interaction of MPSA and PEG with the copper surface when they are present separately in the electrolyte. Significant room temperature recrystallization is observed only when MPSA and PEG are present in the electrolyte together, particularly in the presence of chloride.

- The room-temperature recrystallization kinetics of electrodeposited copper are linked to initial grain size. This inverse relationship between initial grain size and recrystallization rate identifies the grain refinement brought about by different bath chemistries as a critical parameter in controlling subsequent changes in film properties.

- X-ray diffraction examination supports our resistivity measurements. Films which show a large decrease in resistance also show a significant increase in grain size and texture. Early results show that these initially have a large screw dislocation density as well as a high density of stacking faults.

Publications

Stafford, G.R., Vaudin, M.D., Moffat, T.P., Armstrong, N., and Kelley, D.R., The Influence of Additives on the Room-Temperature Recrystallization of Electrodeposited Copper, in Advanced Metallization Conference in 1999, T. Gessner and M. Gross Editors, Materials Research Society, Warrendale, Pennsylvania (2000).

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Thin-Film Characterization from Transmission-line Measurement

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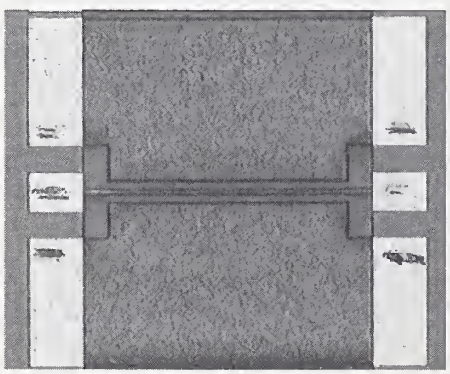
NIST OMP/NSMP

Project Goals

To develop methods to accurately measure the dielectric properties of "low-k" thin films from easy-to-perform in-situ transmission-line measurements. This project brings together the NIST Electromagnetic Properties of Materials Program and the NIST MMIC Program into a collaborative effort with SEMATECH and DOW Chemical to develop methods for semiconductor and material manufacturers for determining the dielectric properties of low-K thin films.

In this work, MMIC probing techniques are used to measure the capacitance and conductance per unit length of small printed transmission lines in which the materials to be characterized are incorporated. The relative permittivity of the dielectric thin films and the conductivity of the metals used in the lines construction are subsequently derived over broad frequency ranges.



Customer Needs

The 1999 SIA ITRS identifies the development of low-k dielectrics as a critical component in the drive to increase processor performance. In the Priority of Technology Needs section (for interconnect) on page 103, it states, "It is expected that low dielectric-constant materials will have an even greater impact than low-resistance metals." SEMATECH ranked the electromagnetic characterization of thin-films as the fourth most important metrology need in the semiconductor industry.

Technical Strategy

Our current primary goal is to develop the measurement methodology based on transmission line measurements for determining the dielectric constant of low-k thin films. Because semiconductor manufactures and material suppliers have different needs and equipment, we are pursuing different approaches for each. We have nearly completed the development of methods for semiconductor manufactures, and are now beginning to focus on material suppliers.

Early efforts revolved around coplanar waveguides such as fabricated at Texas Instruments (pictured on the left). We performed measurements of the capacitance per unit length of these coplanar waveguides passivated with BCB, HSQ, and SiO_2 films. Although the measurements convincingly demonstrated the planar-transmission-line approach, the test structures were difficult to analyze and lacked sensitivity.

Since our work with Texas Instruments we have focused on a simpler and more sensitive microstrip approach. In a joint effort with SEMATECH, we have designed microstrip test structures with greater sensitivity. We have already completed testing of new low-k dielectric and copper conductors supplied by SEMATECH. We hope to expand this effort to include the characterization of other low-k dielectrics and metal systems. We plan to complete this work in FY2000.

We are using NIST's unique processing capabilities to pursue a very different approach to dielectric thin-film characterization with DOW Chemical, a major supplier of low-k dielectrics. NIST will perform most of the microfabrication; DOW will simply deposit and pattern the thin films on pretested circuits provided by NIST. A second set of measurements made at NIST will test for the differences in transmission-line

capacitance. We have already fabricated and forwarded samples to DOW. This approach could result in the development of an important new SRM for the semiconductor industry.

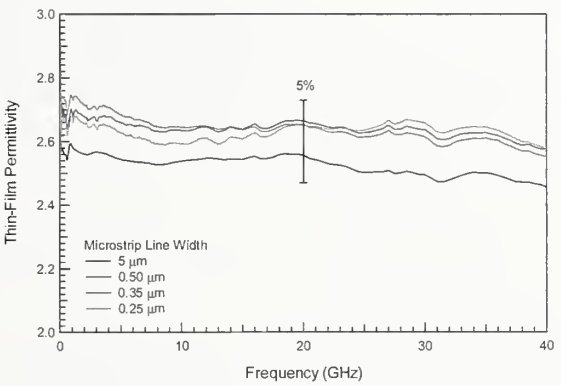
MILESTONE: ***By June 2000, submit publication detailing accurate method for low-k dielectric constant determination from transmission-line measurement for semiconductor manufacturers.***

MILESTONE: ***By 2001, demonstrate alternate method for accurate low-k dielectric constant determination for material manufacturers.***

MILESTONE: ***By 2002, finalize method for accurate low-k dielectric constant for material manufacturers and explore the possibility of a new NIST SRM to support the method.***

Accomplishments

- In a joint effort with SEMATECH we have developed a method of accurately determining the dielectric properties of low-k dielectric and copper conductors. The figure below shows our measurements of the dielectric constant of a low-K thin film supplied by SEMATECH. Our characterization of the electrical properties of the copper conductors allows us to link microwave performance to dc measurements.



- We have designed and fabricated test structures for DOW Chemical and preformed a preliminary analysis.

FY Deliverables

We will characterize low-K thin films provided to us by SEMATECH. We will disseminate our methods through industry presentations and conference and journal publications.

Industry Presentations

Janezic, M. and Williams, D., "Permittivity Measurements of Low-K Thin Films from Transmission Line Measurements", 2/4/99, SEMATECH Focused Technical Advisory Board (FTAB) Meeting, Austin TX.

Janezic, M. and Williams, D., "Permittivity Measurements of Low-K Thin Films from Transmission Line Measurements", 3/11/99, SEMATECH Project Technical Advisory Board (PTAB) Meeting, Orlando, FL.

Publications

Janezic, M. D., and Williams, D. F.., Permittivity Characterization from Transmission-Line Measurement, IEEE International Microwave Symposium Digest, vol. 3, pp. 1343-1345, June 10-12, 1997.

Williams, D. F., Janezic, M. D. , Ralston, A., List, S., Quasi-TEM model for coplanar waveguide on silicon, 1997 EPEP Conference Digest, pp. 225-228, Oct. 27-29, 1997.

Properties of Nanoporous Thin Films Using High Resolution X-Ray Reflectivity and Small-Angle Neutron Scattering

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Funding Sources:
NIST ATP

Project Goals

The goal of this project is to provide the semiconductor industry unique on-wafer measurements of physical and structural properties of porous thin films important to their use as potential low-k interlevel dielectric materials. More specifically, we aim to develop a novel methodology to quantitatively measure the average pore size, pore connectivity, film thickness, matrix material density, coefficient of thermal expansion, moisture uptake, and film composition. These properties are provided to aid industry in the selection and optimization of candidate materials and processes to be used in next generation integrated circuits.

Customer Needs

The development of low-k dielectric materials has been identified by the microelectronics industry as a critical factor to enable deep submicron technology for improved performance of integrated circuits. With decreasing line widths, low-k materials are required to increase the signal propagation speed, decrease the energy needed to send a signal, and decrease cross-talk between adjacent conducting lines. Nanoporous materials are an important class of low-k dielectric materials because the incorporation of voids provides an effective route to reduce the dielectric constant of a solid film. Unlike traditional homogeneous dielectric materials, the structure of the porous network affects properties needed for their integration into current fabrication lines. It is critical to be able to measure the structural properties of these thin films to understand the correlation between processing conditions and the resulting physical properties. Additionally, methods must be developed to measure the structural and physical properties of thin films as prepared on silicon wafers to enable analysis of the effect of actual fabrication processes on the material.

Technology Strategy

We have developed a novel combination of small angle neutron scattering (SANS), high resolution X-ray reflectivity (HRXR), and ion scattering techniques to determine important structural information about the film. These measurements are performed directly on films supported on silicon substrates. HRXR is used to accurately measure the film thickness, electron density depth profile, and the coefficient of thermal expansion. SANS is used to determine the pore structure providing information such as the average pore size, pore connectivity, and moisture absorption. Several analysis models have been developed to quantitatively describe the pore structure within thin films. We have successfully determined the pore structure of films less than 0.5 μm thick. Ion scattering techniques are used to determine the elemental composition of the films. By combining information from all three of these techniques, we provide the first measurements of important quantities such as the porosity and the pore wall density. By measuring the properties of a wide range of materials and processing conditions, we help the U.S. microelectronics industry to develop the proper materials and processing conditions for low-k dielectrics needed for the commercial production of next generation integrated circuits.

Accomplishments

- A methodology was successfully developed using the combination of small-angle neutron scattering, high resolution X-ray reflectivity, and ion scattering to determine the average pore size, porosity, pore wall density, pore connectivity, film thickness, film composition, coefficient of thermal expansion, and moisture uptake of porous thin films up to 1.4 μm thick supported on silicon wafers.

- The experimental methodology was first demonstrated on a porous silica thin film, Allied Signal Nanoglass, prepared from spin-coating and sol-gel methods. This film was determined to have an average pore size of (65 ± 1) Å, a pore wall density of (1.16 ± 0.05) g/cm^3, and a porosity of (53 ± 1) %. The pore size results are supported by positron annihilation lifetime measurements.

- Under a contract from SEMATECH, this methodology was applied to more than 20 different samples including sol-gel materials, silsesquioxane-based materials, CVD films, and high Tg porous polymers as well as varying processing conditions. Three different data analysis schemes have been developed to accommodate the large variety of sample types.

Publications

Wu, W. L., Wallace, W. E., Lin, E. K., Lynn, G. W., Glinka, C. J., Ryan, E. T., and H. M. Ho, "Properties of nanoporous silica thin films determined by high-resolution X-ray reflectivity and small-angle neutron scattering," J. Appl. Phys., **87** (3) 1193. (2000).

Lin, E. K., Wu, W. L, Jin, C., and J. T. Wetzel, "Structure and property characterization of porous low-k dielectric constant thin films using X-ray reflectivity and small-angle neutron scattering," Proceedings of the Materials Research Society, San Francisco, CA, 2000, submitted.

Wu, W. L, Lin, E. K., Jin, C., and J. T. Wetzel, "A three phase model for the structure or porous thin films determined by X-ray reflectivity and small-angle neutron scattering," Proceedings of the Materials Research Society, San Francisco, CA, 2000, submitted.

Polymer Composite Dielectrics for Thin Film Capacitors

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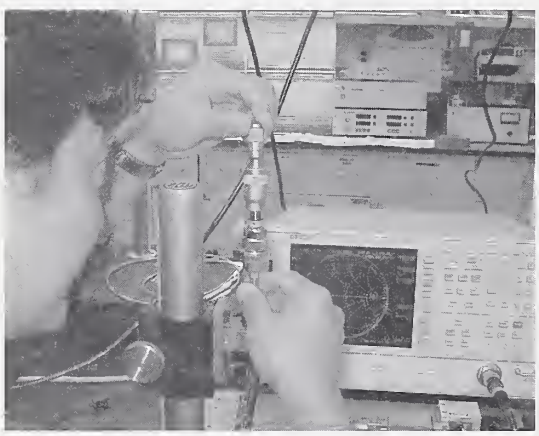
Funding Sources:
NIST STRS
NIST ATP
Industry

Project Goals

Provide measurement methods, standards, data and fundamental knowledge on polymer dielectric composites to support the U.S. microelectronic industry in the development of high-speed electronics and wireless communications applications.

Current focus is on the microwave dielectric permittivity measurements of polymer films for embedded passive components and low impedance power planes.



Customer Needs

There is a widespread need for power-ground decoupling in today's high-speed electronic circuits to assure signal integrity and to reduce electromagnetic noise for adequate performance at microwave frequencies. According to 1999 SIA ITRS, dielectric films capable of providing the embedded capacitance density in the order of 20 nF /cm^2 to 100 nF /cm^2 will be required by the year 2006 for wireless communication and computer technologies. The current state of the art reached 2.5 nF/cm^2.

In order to develop and successfully commercialize such materials, the industry needs a suitable test method to measure dielectric properties and to assess the functional performance of these materials at microwave frequencies in planar, thin film configuration.

An immediate need was specified for low impedance power plane materials that would enable electronic applications operating above 1 GHz .

Technical Strategy

Develop common test vehicles and test protocol for comparative evaluation of embedded capacitance films:

> High-dielectric constant composite films for low impedance power planes pose specific requirements that are difficult to address using existing techniques. Best measurement practices are being determined through collaborative effort with industrial partners that are working on novel materials.

Develop a broad band microwave measurement method for high dielectric constant polymer films:

> The structure-dielectric property relationship in these materials is poorly understood. This situation is due mostly to lack of an appropriate test method and consequently, lack of experimental permittivity data in the frequency range of practical importance, from 0.5 GHz to 10 GHz.

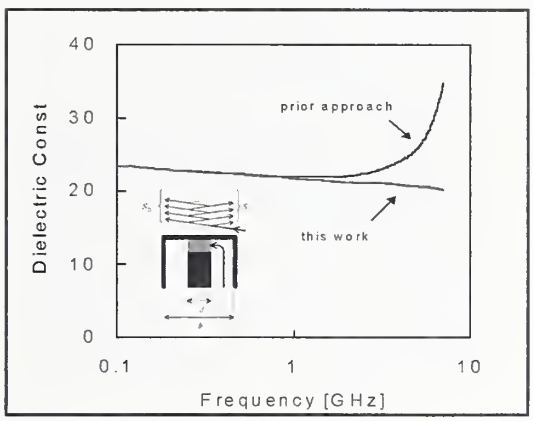
Develop suitable model materials to explore the fundamentals underlying the dielectric dispersion and relaxation mechanism in high dielectric constant films:

> Apply a broad band dielectric spectroscopy technique for verification of functional capabilities and performance of polymer composite films at high frequencies.

Specific Tasks:

- Complete the design of the dielectric test vehicles and implement the corresponding test protocol for embedded capacitance films.

- Evaluate dielectric permittivity of selected high dielectric constant polymer composites developed by the industry.
- Identify the key structural/dielectric attributes of the composite material, which can be used to optimize the dielectric performance.
- Determine the materials functional properties, such as the charge storage and relaxation processes that would allow minimizing impedance of embedded capacitance at high frequencies.
- Complete design and evaluation of the coaxial test fixture for dielectric films.
- Demonstrate the coaxial test method to the industry as a new test method for microwave permittivity measurements of dielectric films.



Accomplishments

A joint project with microelectronic companies resulted in an innovative test structure and procedure for standardized measurements of dielectric films. Implementation of the test protocol and verification of experimental data generated by industrial and academic partners, with those obtained at NIST, have been successfully accomplished.

Microwave dielectric data of several industry-developed polymer composite film materials have been delivered to the NCMS Consortium on Embedded Capacitance and member companies.

Developed a novel time-domain-reflectometry test to analyze the transient-charging behavior of thin film capacitors in the sub-nanosecond time frame.

The testing methodology designed at NIST is being used by the industry in the development of new products.

Identified a fundamental dielectric relaxation process in polymer composites that is beneficial in low impedance power planes, enabling packaging solutions above 1 GHz.

FY Deliverables

Publications

Chiang, C.K., Popielarz,R., Nozaki, R., and Obrzut, J. Broadband dielectric relaxation of polymer composite films. Proceedings of the MRS Symposium on Organic / Inorganic Hybride Materials, April 2000.

Nozaki, R. and Obrzut, J., Microwave permittivity measurements of dielectric films by using TDR, International Union of Radio Science Meeting, 4-8 January, 2000, Denver CO.

Obrzut J., and Nozaki, R. Permittivity measurements of high dielectric constant films at microwave freequencies, IPC Technical Publications EXPO 2000 (2000).

Obrzut, J., and Chiang, C. K., Dielectric measurements of embedded capacitance materials , Embedded De-coupling Capacitance Project, NCMC Technical Report No. 0091RE00, April 2000 (2000).

Obrzut, J., and Chiang, C. K., Dielectric measurements of embedded capacitance materials, NCMS Conference on Development and Use of Embedded Capacitance, February 28-29, 2000, Tempe, AZ (2000).

Obrzut, J., Polymer composite dielectrics for integrated thin film capacitors", NIST ATP Workshop, November 15-17, 1999, San Jose, CA.

Popielarz, R., Chiang, C.K., Nozaki, R., and Obrzut, J., Preparation and characterization of photopatternable BaTiO3/polymet composites Proceedings of the MRS Symposium on Organic / Inorganic Hybride Materials, April 2000.

Test Structures for Mechanical Strain Characterization in IC Interconnects

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Funding Sources:
NIST OMP/NSMP Other Agencies

Project Goals

Provide domestic industry with MEMS-based test structures and standardized test methods for characterizing the thermo-electro-mechanical properties of thin films used in ICs.

Fixed-fixed beam test structure array for measurement of mechanical strain and interconnects in multilayer structures.

Customer Needs

Increasing device density in integrated circuits leads to more interconnect layers with smaller cross-sectional area and higher aspect ratio; all of which increase the probability of failure by mechanisms such as electromigration, stress migration, and delamination. These reliability problems reside in the interconnect and dielectric layers of the IC. The interconnect and dielectric layers of an IC can be thought of as laminates of a multilayer film composite. The IC industry requires new measurements methods to characterize the mechanical strain in these multilayer films. Results can then be used to verify finite element models of the stress in the films and to correlate mechanical stress data with reliability testing. MEMS-based test structures offer new ways to characterize the mechanical stress in multilayer films.

Technical Strategy

Micromachining techniques, test structures, and test methods are being developed to characterize the stress, elastic modulus, and adhesion properties in IC interconnects. These test structures are fabricated in the standard IC process on fully fabricated ICs. Fixed-fixed beam and cantilever test structures with interconnect layers are micro machined in the fully processed IC. Measurements of deflection of buckled beams give information on the stress in each interconnect layer. Measurements of mechanical resonance give information on the elastic modulus of the films. These test structures can also be integrated with micro heating elements for accelerated life testing.

MILESTONE: By 2001, develop a test method for elastic modulus in IC interconnects to derive the mechnican stress of interconnects.

Accomplishments

Test structures and analysis to measure mechanical stress/strain of interconnects in fully fabricated ICs were developed. A test chip containing the new test structure designs was fabricated on the commercial foundry 1.2 μm CMOS technology run through MOSIS. Following fabrication, the test structures were silicon micromachined in order to mechanically release them. These test chips contained test structures to measure the longitudinal stress component in IC interconnects. New designs are being developed to measure the lateral and normal components of stress as well. As IC device sizes shrink, thermo-mechanical stress in interconnects is an ever-increasing reliability concern. Current state-of-the-art IC technology uses 5 interconnect layers with aspect ratios (height/width) of 1.8. According to the 1999 SIA ITRS, these numbers are expected to increase to 9 and 3.0, respectively, by the year 2012. Despite the increasing number of interconnect layers in IC technology, existing stress determination and modeling studies have been limited to single level metalization, with few

exceptions. This is due, in large part, to the lack of experimental techniques for measuring strain in narrow linewidth (< 10 mm) multilayer structures. This work allows, for the first time, the measurement of stress in multilayer structures in fully fabricated ICs.

FY Deliverables

Collaborations

University of Maryland, Department of Mechanical Engineering. (M. Gaitan)

ASTM Task Group E08.05.03, metrology for thin-film electromechanical properties of MEMS-based IC technologies (J. Marshall)

Statistical Engineering Division, metrology for thin-film electromechanical properties of MEMS-based IC technologies (J. Marshall)

Standards Committee Participation

ASTM MEMS Residual Stress Round Robin, ensured round robin's success with the development of the MEMS Linear Dimensional Metrology (J. Marshall)

Publications

Smee, S., Gaitan, M., Joshi, Y., and Blackburn, D. L., MEMS-Based Test Structures for IC Technology, Mechanical Behaviour of Advance Materials, ASME 98, Anaheim CA, Nov 15 – 20, 1998.

Smee, S., Gaitan, M., Novotny, D. B., Joshi, Y., and Blackburn, D., IC Test Structures for Multilayer Interconnect Stress Determination, Accepted for publication IEEE EDL.

Tomography of Microstructures: Absorption and Diffraction

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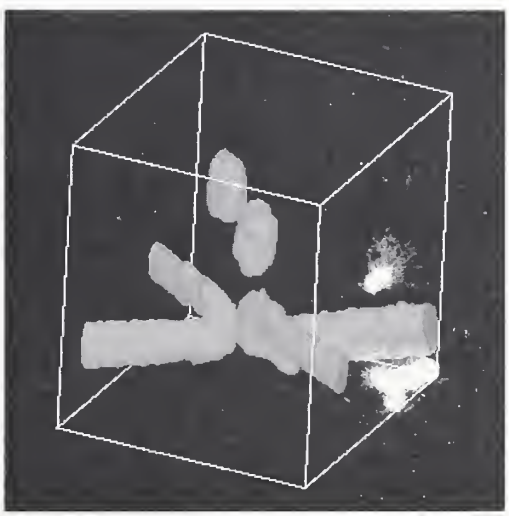
Funding Sources:
NIST STRS (PL)
NIST ATP
Other Agencies

Project Goals

Demonstrate the feasibilty of tomography of integrated circuit interconnects to kindle interest in a larger-scale implementation. Aid in the development of tools for routine laboratory-scale integrated circuit tomography. Develop a leading edge synchrotron-based integrated circuit tomography capability for the calibration of laboratory instruments and to provide a capability for the most demanding problems. Integrated circuit interconnects are taken to include both aluminium and copper.



Aluminium integrated circuit reconstructed tomographically from 13 views; the resolution is 200 nm.

Customer Needs

Failure analysis is a continuing and multifaceted challenge for the semiconductor industry. Yet, there is a need for a tool which can image a 10 :m cube with resolution below 100 nm.

Most probes are two dimensional; an exception, TEM-based tomography operates on samples smaller than 1 micrometer diameter.

The customer requires a laboratory tool rather than a synchrotron beam line. This is because: (a) synchrotron schedules are not compatible with the customer's time-to-information requirements; and (b) outsourcing of analytical tools tends to create less meaningful information than that developed in-house.

Technical Strategy

We partner with industry, national laboratories, and universities to achieve the project goals based on the use of the best available technology.

In addition to helping to develop the project goals, our partners in the semiconductor industry prepare samples.

The sample preparation requirements are similar to that required for transmission electron microscopy, but less demanding.

To date, we have partnered with people at national laboratories to use existing X-ray microscopes on synchrotron beam lines to perform X-ray tomography. We have partnered with universities to obtain tomographic reconstruction software. The actual acquisition of data --- which involved 24-hours operation at remote locations --- has been performed jointly with industry-, national laboratory- and university-based partners. We have taken responsibility for the actual processing of the data, tomographic reconstruction, and display. Software development is simplified by relying on high-level graphics packages supported by the NIST Visualization Group. This teaming approach has resulted in a relatively rapid first demonstration of integrated circuit tomography.

Separately, we partner with industry and national laboratories to develop a laboratory-based system for integrated circuit tomography below the 100 nm length scale. We have developed an ambitious but coherent plan to build such a system pending major funding.

Accomplishments

- First reconstruction of an integrated circuit interconnect: 400 nm resolution in 3D.
- Improvement of resolution to 140 nm in 3D by improved hardware and software.
- Development of a plan and a team to achieve laboratory-based integrated circuit tomography.

Electron-Beam Moiré

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Funding Sources:
NIST OMP/NSMP
NIST STRS: MSEL, Materials Reliability Division

Project Goals

Develop and apply the electron-beam moiré technique to measurement of strain and observation of deformation at high magnification. Use the observations to characterize failure modes and to verify mathematical models and simulations of microscale mechanical behavior. Modify the technique to remain current with industry requirements for resolution and conditions. Reach out to industry to make them aware of the technique and its potential to solve their reliability issues.

Customer Needs

Failure of electronic packaging is a major source of concern in modern electronics. In this project we seek to improve the usefulness of modeling and simulation in the design and manufacture of advanced electronic packaging and interconnect structures by providing direct quantitative experimental verification of predicted deformations, and by characterizing actual failure modes. This work contributes to the areas of modeling and simulation, advanced packaging, and reliability listed in the 1999 SIA ITRS.

Technical Strategy

Local displacements on the order of 100s to 10s of nanometers can be measured and strain calculated using the electron-beam moiré technique. Deformations are measured over fields ranging from 50 μm by 50 μm to 500 μm by 500 μm. This is accomplished by preparing the specimen surface with crossed-line gratings at pitches of 180 nm to 1 μm and dot-array gratings at pitches of 100 nm to 200 nm, using electron-beam lithography, and observing them in the scanning electron microscope at magnifications from 200x to 2000x. Deformations produce changes in the local moiré fringe density. These changes are induced by thermal or mechanical loading, and are analyzed to give the complete normal and shear displacements from which strains may be calculated.

MILESTONE: By 2000, assess new method for making moiré gratings with the goal of sub-25-nanometer pitches. Apply electron beam moiré to measure displacements at a suspected interfacial flaw indentified by thermal microscopy.

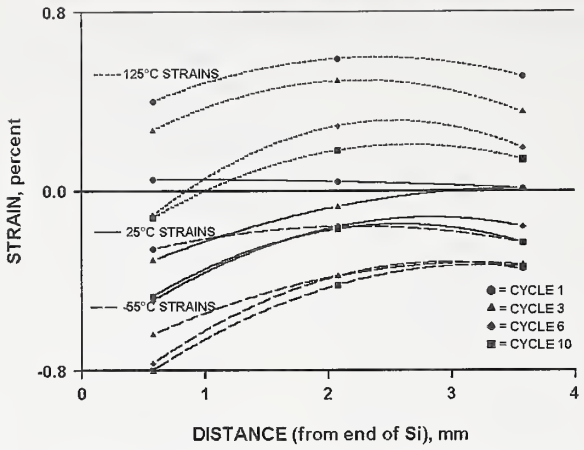
The outer crystalline shell of the *Sulfolobus acidocaldarius* bacteria is a regular, two-dimensional, hexagonal array with a 22 nm pitch lattice constant. Using this bacteria outer shell, in collaboration with researchers at the University of Colorado, we will attempt to selectively place the array in a strategic location. If this is successful, we will thermally load a specimen with an attached grating to determine if the grating will adhere and produce the moiré effect at elevated temperatures.

The interfacial degradation between a printed circuit board and an integral resistive element from a U.S. manufacturer will be measured with electron-beam moiré and correlated with the results of IR microscopy.

MILESTONE: By 2001, apply atomic-force moiré to measure the thermomechanical deformations of an on-chip interconnect. Use electron-beam moiré to observe thermal fatigue at a known interfacial flaw.

We have in our possession specimens from Intel containing on-chip interconnects and microvias. With atomic-force moiré, we will now have a technique sensitive enough to measure the displacements found in these features upon thermal cycling

MILESTONE: By 2002, evaluate atomic-force moiré as a complementary technique to stress-voiding measurements.



Strain distribution in the solder balls across a flip-chip PBGA package from Motorola. Figure shows how the strains vary with temperature, increasing number of thermal cycles, and location of the solder ball with respect to the edge of the Si chip.

Accomplishments

- Two new designs for the flip-chip PBGA specimens were received from Motorola, prepared, and tested in FY99. Tests used electron-beam moiré and were thermally cycled between –55 °C and 125 °C.

- The tests were analyzed and the results reported to Motorola directly in a plant visit that took place in February. The results were welcomed by the Motorola staff and generated much discussion and interaction.

- Motorola requested our help in identifying failure modes in the latest product they are attempting to qualify for low-temperature applications, the high-density interconnect substrate. The specimens were received, prepared, and tested in FY99.

- The moiré effect was observed in the AFM using the crystalline outer shell of the *Sulfolobus acidocaldarius* bacteria on a Si substrate, obtained from Dr. Winningham of the University of Colorado. This was our first proof that it is possible to scale-down the moiré technique to the AFM, offering us the potential to measure displacements of on-chip features.

- Performed experiments to verify that the results of electron-beam moiré and IR microscopy experiments can be correlated. Interfacial cracks were detectable with both techniques.

- We researched, evaluated, and purchased a new image acquisition system that will collect and store high-resolution images from the SEM. The improved resolution will allow us to identify moiré fringe centers with greater confidence.

Publications

Drexler, E.S., Reliability of a Flip-Chip Package Thermally Loaded between –55°C and 125 °C, presented at the InterconnectPACK symposium of the TMS Annual Meeting in San Diego, CA on March 1, 1999, *Journal of Electronic Materials* **28**, 1999, pp.1150–1157.

Drexler, E.S., Strain Measurements in a Thermally-Cycled Flip-Chip-on-Board Solderball, Presented at the Microelectronics Reliability symposium of the Spring Meeting of MRS in San Francisco, CA on April 6, 1999, in the Proceedings *Materials Reliability in Microelectronics IX*, D.D Brown, A.H. Verbruggen, and C.A. Volkert, Eds., 1999, pp. 9–14.

Drexler, E.S., and Berger, J.R., Mechanical Deformation in Conductive Adhesives as Measured with Electron-Beam Moiré, *Journal of Electronic Packaging* **121**, 1999, pp. 69–74.

Hygrothermal Expansion of Polymer Thin Films

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Funding Sources:
NIST OMP/NSMP

Project Goals

Provide industry with robust measurement tools and data for characterizing the dimensional stability of polymers. In particular, the project is focused on the measurement of changes with temperature and humidity on the out-of-plane dimensions of thin films. NIST has designed, built and demonstrated a capacitance cell with outstanding sensitivity for measuring the out-of-plane expansion of polymer films.

Customer Needs

Polymers are widely used in electronic packaging in many applications. These include interlayer dielectrics, underfills in ball grid arrays, adhesives, encapsulants and substrates. In many of these applications, the polymer is in the form of a thin film on another material with significantly different physical properties. Knowing and predicting the dimensional changes of these films with temperature and humidity are important for modeling the performance and reliability of complex assemblies. The properties of these films can be significantly different from the material in bulk form, especially in a constrained geometry. In addition, these materials may only be available in the form of thin films. The most commonly used technique, thermomechanical analysis (TMA) has been previously demonstrated by round robin tests to be inadequate for determining these very small changes in film thickness.

The 1999 SIA ITRS pinpoints "Areas of concern with the new materials and architectures are as follows: in-film moisture content, film stoichiometry, mechanical strength/rigidity, local stress (versus wafer stress), line resistivity (versus bulk resistivity), available of high frequency dielectric constant values..." This project is working to introduce the measurement standards needed to describe the thin films used in these applications.

Technical Strategy

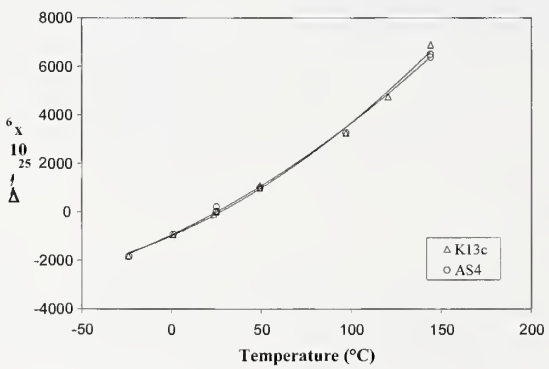
To achieve the goal of this project of providing industry with a robust measurement technique for characterization of dimensional stability, several activities are currently in progress. These activities are (1) determining the accuracy and precision of the technique applied to a variety of polymer measurements; (2) working with standards-setting bodies to explore the desirability of introducing the technique as a standard method for measuring thermal and hygrothermal expansion; (3) providing industry with materials property data on selected packaging materials; and (4) expanding the capabilities of the measurement techniques to electrically conducting materials and to thinner films.

The expansion of the capabilities of the measurement technique is currently in progress. The capacitance cell for semiconducting and conducting samples has been developed and is being calibrated and tested to determine the accuracy and precision of the new design. These measurements are being performed on p-type <100> oriented single crystal silicon samples, the results of which will be compared with standard reference data. The second area in which the capabilities need to be expanded is the dimensional range over which the coefficient of thermal expansion can be determined. Currently, the dimensional range of the capacitance cell is limited to 5 μm to 1.5 cm. To expand this dimensional range, X-ray reflectivity techniquesare being developed which will allow measurements from 1.4 μm down to the order of

several hundred Ångstoms. The main thrust of this portion of the research is the automation of the technique to increase the repeatability of the measurements and thus facilitate its use by industry.

To aid in the introduction of the capacitance cell metrology as an industry standard, discussions are being held with several U.S.-based companies to examine the possibility of commercialization of the capacitance cell. Commercialization would dramatically aid in the introduction of a standard test method based on the capacitance cell and would facilitate its adoption by industry. Prior to, or concurrently with, commercialization, the capacitance cell will be submitted to The Institute for Interconnecting and Packaging Electronic Circuits' (IPC) HDIS Test Methods Group as a standard test method with schematics for manufacture of non-commercial equipment, a rare but not unheard of procedure.

In the course of the work, data on several materials of importance to the electronics industry, have been and will be, generated and disseminated through the appropriate venues.



Thermal expansion of 0.5 cm carbon fiber

MILESTONE: By 2000, complete and test new capacitance cell design and make available to industrial users. Begin process of introduction of the capacitance cell as an IPC standard test method.

MILESTONE: By 2001, capacitance cell commercialized and/or established as an IPC standard test method for characterization of lymer thin films. Have X-ray reflectivity automation completed.

MILESTONE: By 2002, have automated X-ray reflectivity technique reproducibility and limitations completely determined and make technique available to industrial users.

Accomplsihments

- The accuracy of the previous capacitance cell design for thermal expansion measurements on thicker samples was demonstrated on several 5 mm thick carbon fiber composite samples in collaboration with the Applied Physics Laboratory at Johns Hopkins University – this demonstrated the capabilities for measuring PWB composite materials.

- Coefficient of thermal expansion data of Cyclotene (a potential inner-layer dielectric) requested by and provided to the CINDAS database and SEMATECH.

- Through the OMP office, initial contacts have been made with several companies to explore the possibility of commercialization of the capacitance cell.

- Design for modified capacitance cell that can measure silicon and conducting materials completed; components constructed (nichrome plated electrodes and brass electrode holder); cell assembled; and calibration begun.

FY Deliverables

Hardware

Capacitance cell development for measurement of semiconducting and conducting samples completed.

Publications

Snyder, C.R. and Mopsik, F.I., High Sensitivity Technique for Measurement of Thin Film Out-of-Plane Expansion, Proceedings of the 1998 International Conference on Characterization and Metrology for ULSI Technology, Gaithersburg, Maryland, March 23-27, 1998, pp.835-838.

Snyder, C.R. and Mopsik, F.I., A precision capacitance cell for measurement of thin film out-of-plane expansion. II. Hygrothermal expansion, Review of Scientific Instruments, 70 (5), pp. 2424-2431 (1999).

Thermal Conductivity of Microelectronic Structures

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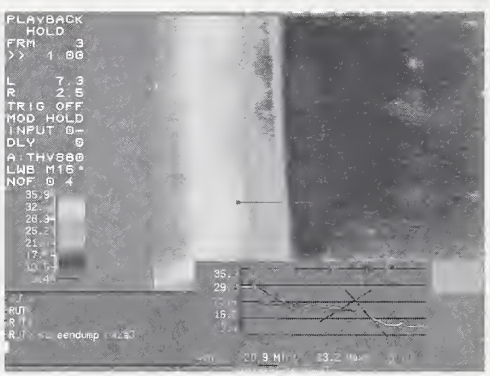
Funding Sources:
NIST OMP/NSMP
NIST STRS: MSEL, Materials Reliability Division

Project Goals

Demonstrate advanced methods of measurement of thermal effects within packaging structures and their components. Develop a measurement method for absolute thermal conductivity of interconnect structures at the micron scale. Demonstrate quantitative application of infrared microscopy to thermal transport measurement and detection of incipient failure in microelectronic packages. Combine the IR technique with electron-beam moiré to assess failure mechanisms.



Customer Needs

The removal of heat from microelectronics remains a key issue limiting the ability to create smaller packages with higher component densities. Heat flow through the package structure is critical to design. The large number of diverse materials and their interfaces creates a complex problem. Modeling and simulation provides some help, but the need for actual data to support the models is critical.

Technical Strategy

The project uses two approaches. IR microscopy is the basis for both. The main effort in FY2000 and beyond is the application to package structures. Here sectioned samples are heated either externally by a laser system or internally by electrical means and the heat flow monitored by the IR system which has the capability of detecting thermal barrier regions and regions where anomalies in the heat flow indicate potential failure sites. In FY1999 and earlier, the thermal work concentrated on developing techniques for measurement of the absolute thermal conductivity using microscale bridge structures designed to simulate interconnects in a variety of environments. That part of the work has been successfully completed.

MILESTONE: By 2000, demonstrate capability of detecting interfacial flaws by thermal microscopy both using external laser heating and internal electrical heating. Correlate with electron-beam moiré data.

MILESTONE: By 2001, develop the technique and demonstrate quantitative measurement of interfacial thermal conductivity across the build-up layers of an HDI substrate.

MILESTONE: By 2002, assess the feasibility of using the AFM in a thermal mode to increase the spatial resolution of the thermal technique to coincide with the spatial resolution of the moiré techniques.

Accomplishments

- The IR microscope facility was modified for application in package evaluation. Preliminary tests demonstrate feasibility of measurements in the 20 μm –50 μm size range using a laser heat source.
- Bridge structures were designed and produced by MEMS technology. A vacuum chamber system was built and installed in the IR microscope facility, which we found was needed to eliminate excessive conduction losses from the bridges.
- Bridge structures with various dimensions and combinations of layers were measured, each at several different input powers. The resulting data was fitted to theory and the results showed that quantitative thermal conductivity data could be obtained by this method.

Solderability Measurements for Microelectronics

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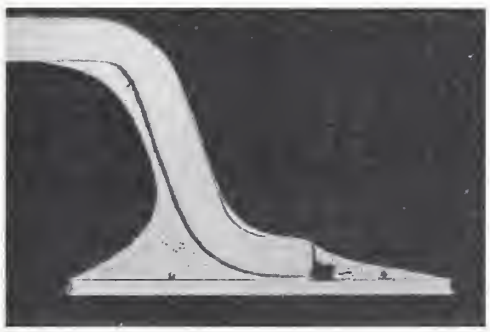
NIST OMP/NSMP

Project Goals

The goals for this project are two-fold: 1) develop test techniques and scientific guidelines that U.S. manufacturers can use to evaluate solder and solderability of components before committing them to the production line, and 2) assess solderability and reliability of new high-reliability solders, especially environmentally friendly lead-free solders, for a range of demanding microelectronics applications. NIST collaborates with industry groups which are pursuing projects in this area, including groups developing standard tests for solderability, identifying and testing environmentally friendly lead-free solders, and identifying and testing fatigue-resistant solders suitable for higher temperature automotive, telecommunications, and avionics applications.



Customer Needs

As documented in the Assembly and Packaging section of the 1999 SIA ITRS, the decrease in dimensions of electronic devices has resulted in dramatic increases in interconnect density as well as a trend toward packaging schemes, such as ballgrid arrays (BGAs), chip scale packages, and flip chips, where inspection of solder joints is problematic. These developments have introduced stringent new demands on solder and the soldering process and produced a need for improved solderability tests and standards. Furthermore lead-free solders are likely to be required in most products sold in Japan and Europe in the 2002-2004 time frame, and U.S. manufacturers are not prepared for incorporation of these alloys in their products. The advent of lead-free solders necessitates difficult changes in assembly processes. Elimination of Pb is identified as a major NTRS Environmental Safety and Health Crosscut Issue, and action to eliminate lead for most applications in microelectronics is well under way in Europe and Japan. In addition, the IPC National Technology Roadmap for Electronic Interconnections identifies improved solderability tests and lead-free solders as necessary to achieve industry goals for the next 2 to 4 years.

Technical Strategy

Improved solderability test methods will lead to improved manufacturability and reliability in microelectronic devices. Current work emphasizes solders designed for high temperature application, for PWB and hybrid assemblies as well as for die attach. We are addressing the reliability of lead-free and lead-containing solders during high temperature thermal cycling in a collaborative project coordinated by the National Center for Manufacturing Sciences with Ford, Delphi/Delco, Rockwell International, AlliedSignal and various solder suppliers. Through this High Temperature Fatigue Resistant Solder Consortium we are evaluating a number commereial and novel solders for application temperatures of 160°, 175°, and 205° C.

We have instituted an electrochemical study of the root causes of solderability with the goal of improved solderability tests for industry. The growth of oxides on surfaces is a frequent cause of loss of solderability of PWBs and component leads. Electrochemical tests, especially SERA, are being applied to measure the chemical nature of the species produced by oxidation, the structures and thicknesses of surface layers, their role in the degradation of solderability on copper surfaces, and the effectiveness of oxidation inhibitors. We have established an electrochemieal quartz crystal microbalance (EQCM) capability which will provide an in-situ mass measurement, with sub-monolayer resolution, during the electrochemical

examination of copper in solution. Mass and charge associated with the formation and removal of copper oxides will be correlated and may become instrumental in understanding SERA transients, which the industry is currently considering as a test for determining solderability.

MILESTONE: By FY 2000, Characterize –55 to 160° C fatigue performance of new lead-free solders through reliability tests with a range of surface mount packages, including BGAs, on printed circuit boards. Testing and analysis will be conducted through the NCM5 High Temperature Fatigue Resistant 5older Consortium.

MILESTONE: By FY 2000, conduct preliminary evaluation of fatigue performance of lead-free and lead-based solder alloys cycled from 0 to 175° C for hybrid assemblies (ceramic substrates). Evaluate metallographically and through Weibull analysis.

MILESTONE: By FY 2000, conduct preliminary evaluation of lead-based solder alloys cycled from 0 to 205° C for hybrid assemblies (ceramic substrates) and die attach. Evaluate metallographically and through Weibull analysis of fatigue performance. Pursue patent application for low cost die attach alloy.

MILESTONE: By FY 2000, quantify in-situ EQCM measurements for copper. Develop software and hardware for determination of components of the equivalent circuit of the EQCM and assign physical meaning to the changes of measured values. The instrument employed in our laboratory allows us to determine all of the components of the equivalent electrical circuit representing the quartz crystal. Changes in the resonant frequency will be used to see if the changes in resonant frequency are due to mass variations, as assumed in conventional measurements, or by other effects related to frictional energy losses. Measurements will be made concerning, for instance, surface roughness and film stiffness.

MILESTONE: By FY 2001, characterize –55 to 175° C thermal fatigue performance of new lead-free and lead-based solders through a reliability test vehicle containing a range of surface mount packages, including BGA, on hybrid assemblies (ceramic substrates). Testing and analysis will be conducted through the NCM5 High Temperature Fatigue Resistant 5older Consortium.

MILESTONE: By FY 2001, characterize –55 to 205° C thermal fatigue performance of new and conventional lead-based solders through a die attach test vehicle. Testing and analysis will be conducted through the NCM5 High Temperature Fatigue Resistant 5older Consortium.

MILESTONE: By FY 2001, use the Electrochemical Quartz Crystal Microbalance to determine the mass changes associated with the oxidation and reduction of copper oxide layers electrochemically formed in borate buffer and other electrolyte solutions. These measurements will be carried out in situ, in order to correlate electrical charge passed with mass changes, and determine the potential ranges at which these processes occur. Comparison between these two measurements will allow us to determine the losses due to dissolution of the oxidation products and lead to a better understanding of SERA transients.

Accomplishments

- NIST led the Materials Task Group of the NCMS High Temperature Fatigue Resistant Solder Consortium. The literature was critically analyzed to determine promising solder candidates for the three application temperatures of interest. New alloy compositions were developed based on metallurgical principles. Metallographic evaluations of a large number (52) of candidate alloys in simple solder joints were conducted at NIST. These analyses were used to downselect 22 alloys for analysis within the ThermoMechanical Test Vehicle for each application temperature, 160 °C, 175 °C, and 205 °C.

- Assembly behavior and thermal fatigue performance of 12 commercial and experimental lead-free solders were characterized in the range of –55 °C to 160 °C. Testing and analysis of these PWB assemblies was conducted through the NCMS High Temperature Fatigue Resistant Solder Consortium. Metallographic evaluations at NIST and Weibull analysis to characterize fatigue performance were used to evaluate performance.

- Oxidation effects which influence solderability on copper components have been identified by electrochemical examination in boric acid-borate buffer. Three main constituents of electrochemically grown surface films have been tentatively identified: Cu_2O, CuO and $Cu(OH)_2$.

- Measurements with the EQCM with results close to the theoretical limit have been achieved, and sub-monolayer resolution, while controlling the potential of an electrode in solution has been demonstrated. Initial versions of software designed to operate the electrochemical instrumentation

and continuously measure the elements of the equivalent circuit of the quartz crystal resonator are complete and being tested.

FY Deliverables

Deliverables for 2001 include publication of electrochemical data showing regions of stability for various copper oxides in borate buffer solutions and the current-potential behavior of their electrochemical reduction. This will allow the production of wetting balance standards to be used by industry to calibrate equipment.. We also plan to publish a major document in FY2001, including CD-ROM, with all data from the NCMS High Temperature Fatigue Resistant Solder Consortium. Additionally, some data may be released in FY2000 regarding lead-free alloy performance if an early release is deemed critical to U.S. microelectronics industry development of lead-free capability.

Assembly of IC Chips Using Wafer-Level Underfill

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NIST ATP
NIST STRS

Project Goals

Provide computer simulation and materials data that show behavior to be expected during assembly of flip chips that have an underfill/solder bump system applied at the wafer level. Examine experimentally the validity of computer modeling efforts.

Three specific goals of this project are: 1) create modeling software for evaluating capillary induced realignment forces; 2) carry out validation experiments for realignment forces provided by solder joint to misaligned pads; 3) develop a model incorporating capillary realignment forces as well as viscous forces retarding realignment associated with polymer underfill material.

Customer Needs

For area array flip chip applications, the microelectronics industry has a well established need for an underfill system that obviates the time-consuming flow required by current viscous underfill materials. The most promising route to accomplishing this is the application of an integrated underfill/solder bump system at the wafer stage. Such a process involves the reflow of an area array of solder joints during attachment of the chip to the package or, as in direct chip attach, to a printed circuit board.

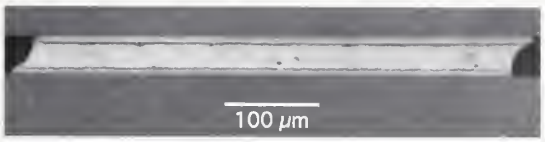
This project addresses the critical problem of wetting behavior of solder in such solder joint interconnections under the constraints found in the wafer-level underfill systems. The pre-existing underfill geometry provides constraints on the flow of the solder, influencing the self-alignment of the die and final solder joint geometry. These factors have profound effects on joint reliability. Thus, behavior of the solder during reflow is a critical aspect of the underfill system, which is itself supposed to enhance reliability.

Technical Strategy

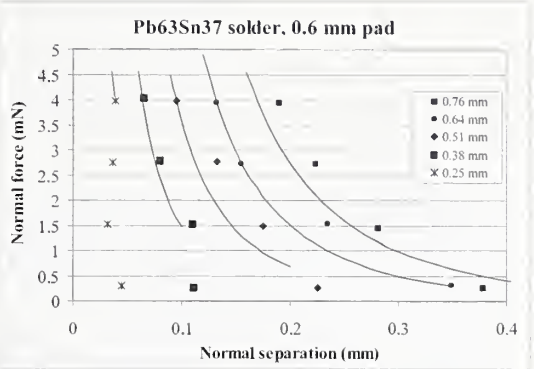
The technical approach is tripartite, with the parts corresponding to each of the three principal goals of the project. The first part is creation of modeling software for evaluating capillary induced realignment forces. This is being accomplished within the larger framework of the NIST Center for Theoretical and Computational Materials Science (CTCMS) effort to create a library of code for evaluating industrially relevant solder joint geometries. As with the broader CTCMS effort, the codes for the solder joints relevant to this project are based on the Surface Evolver computer program. Benefits of this program are its substantial incorporation into industrial solder joint efforts and the generality of the joint geometries that it can be used to evaluate. A potential drawback of the code is that it includes only capillary and gravitational forces.

The second part of the project is an effort to experimentally measure the capillary realignment forces for different pad dimensions and solder volumes. In these experiments two eight-pad chips are joined using solder joints with volumes between 0.23 and 0.0086 mm^3. The loading conditions are systematically varied and the post-solidification solder joint geometry measured in order to obtain the force-displacement relationships for the solder joints under both aligned and misaligned conditions. These results are being compared to results predicted in the modeling effort in order to assess the validity of using only capillary and gravitational forces to predict solder joint geometries.

The third part of this effort will incorporate the modeling and experimental solder joint results along with viscosity-temperature data for relevant polymer underfill material to predict self-alignment behavior as a function of temperature.



Solder volume of 0.0086 mm^3 connecting 0.5 mm diameter pads under a tangential loading of 0.13 mN and normal loading of 1.8 mN.



Preliminary data on applied normal load vs chip-to-substrate separation (symbols) for a range of solder volumes, expressed by solder ball diameters. Model results based on zero free parameters are shown (curves) only for the conditions under which the solder is extruded beyond the copper pad onto the silicon substrate.

Accomplishments

- Software based on the freeware Surface Evolver code has been written that allows modeling of two relevant joint geometries. As part of the library of Evolver files modeling different industrial solder joint geometries, this software was placed in the following CTCMS web site: http://www.ctcms.nist.gov/~djl/solder/new.html. Specific output of this software includes predictions of equilibrium solder joint geometries as well as force-displacement relationships for two pads joined by a solder joint. The user-specified separation between the pads can be such that they are aligned or misaligned.

- Force-displacement relationships have been measured for solder joints with volumes between 0.23 and 0.0086 mm^3. The loading conditions have been systematically varied and the joint geometry measured in order to obtain the force-displacement relationships for the solder joints under both aligned and misaligned conditions. These results are being compared to results predicted in the modeling effort to assess the validity of using only capillary forces to predict solder joint geometries.

- Wetting experiments were conducted on relevant polymer and metal thin films to obtain contact angles required for the modeling.

FY Deliverables

Software

Software based on the freeware Surface Evolver code was placed at the CTCMS web site http://www.ctcms.nist.gov/~djl/solder/new.html as part of the library of Evolver files modeling different industrial solder joint geometries. Specific output of this software includes force-displacement relationships for underfill geometry solder joints.

Packaging Studies for Copper/Low-K Semiconductor Devices

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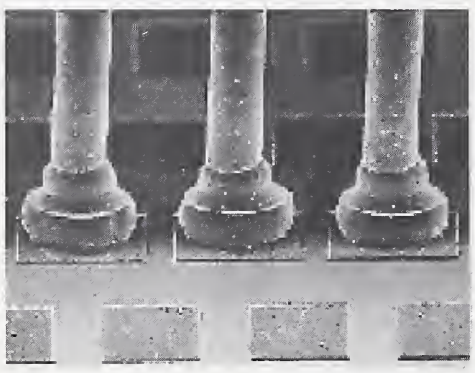
Funding Sources:
NIST OMP/NSMP
NIST STRS

Program Goals

To develop the best, most economical, practical bonding surface(s)/sub-surface support structures/and techniques for wire bonding to advanced semiconductor devices with copper metallization and to resolve metallurgical diffusion issues that relate to these surfaces/structures.



Customer Needs

To maintain our competitive world position, the US semiconductor industry must broadly implement copper intraconnections on the chip. Wire bonding is the dominant method of interconnecting the chip to its package. Thus the work developed in this program will assist industry in this important objective.

Technical Strategy

The highest priority is to determine the optimum (bondable/protective) metal surface to place on top of the copper pad. Gold plating, electro/electroless is considered the best, but diffusion of the base copper can limit its usefulness. The literature has contradictions as to the diffusion coefficients, and they can vary, depending upon the impurities in both the copper and the gold. Measurements will be made on samples similar to those used in the industry. Other top metal surfaces will also be evaluated. As appropriate, such evaluations will be made using Auger and other measurement techniques. Verification will be carried out by wire bonding bondability experiments. Other objectives/strategies will include determining the effect on bondability of polymers under the pad, and under-pad chip support structures.

MILESTONE: By FY 2001, determine the diffusion coefficients of copper into gold using metal films deposited in the same manner as on copper-conductor-chips and evaluate the results with actual wire bonding experiments.

MILESTONE: By FY 2002, study and evaluate other appropriate top coatings and develop appropriate gold/other plating baths to optimize the surface preparation/coating/polymer and bondability.

Accomplishments

- Presentation/Talk given in December in at a Workshop on "Mechanics, Physics & Reliability of Polymeric Materials for Microelectronics (POLY=99), December 12-15, 1999, entitled AThe Effect of Polymer Material Properties on Wire Bonding to Advanced Copper-Low Dielectric Constant Integrated Circuits@.

- A presentation/talk also given at the ASTM meeting in Tempe, AZ, January 19, 2000, which will discuss the metallurgical options for coating copper bond pads as well as the required support structures within the chip.

FTIR Methodology for Quantifying Oxygen in Heavily Doped Silicon

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NIST OMP/NSMP

Project Goals

Develop FTIR methodology for metrology of interstitial oxygen in conducting silicon wafers.

Examining the optical collimator and sample. The sample is loaded into the Fourier transform interferometer for high-resolution, high-accuracy, mid-infrared refractive index measurements in silicon.

Customer Needs

Rapid developments in the Si IC industry, driven by advances in scaling and functionality, are leading to ever increasing demands for quantitative analytical techniques with unprecedented accuracy, robustness and ease of use. The 1999 SIA ITRS, page 109, Table 32a, and page 111, Table 32b mentions bulk oxygen content as a critical parameter. Optical techniques have been called upon to fill some of these critical needs because they are nondestructive, contactless, and are compatible with most materials growth and processing environments. This project has focused on applying infrared absorption to detect and quantify oxygen impurities in silicon.

Technical Strategy

While often the basic physics of the interaction of light with semiconductor materials is well understood, it is not possible to translate the knowledge for accurate measurements. The emphasis in published literature has been on the spectroscopic aspects achieved at the expense of photometric accuracy. Our approach has been to place equal emphasis on both which has led to unprecedented accuracy in measuring the optical response, which in turn has translated to superior metrological accuracy.

*MILESTONE: By 2001, **Develop FTIR measurement of interstitial oxygen in conducting wafers.***

(a) Complete modeling of IR response of conducting Si wafers.

(b) Complete 300K reflection and transmission measurements on wafers with $\rho \geq 0.02\ \Omega$.cm (n-type) and $\rho \geq 0.1\ \Omega$.cm (p-type) wafers.

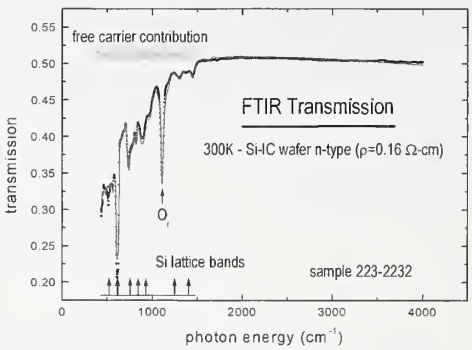
The semiconductor industry has relied on high accuracy and precision measurements of oxygen in silicon by FTIR since the early 1970's. At that time, it was first recognized that oxygen when precipitated, results in crystal defects that entrap metal impurities away from active device junctions at the surface. In spite of the successful development of this technology over the past two decades, little progress has been made in measuring interstitial oxygen (O_i) in heavily doped silicon, the material of choice for current and future IC fabrication. The problem arises from free carrier induced reflection and absorption of infrared light in such conducting substrates. We have developed FTIR methodology to determine the concentration of oxygen in medium resistivity wafers and are working towards a technique capable of analyzing heavily doped wafers.

Accomplishments

- The capability to perform IR transmission measurements using polarized light has been added. IR polarizers were borrowed from the Physics lab for these measurements. The added capability is required to crosscheck n and k measurement results we obtained in FY98. Completed preparing ultrahigh purity silicon wafers ($\rho \cong 30{,}000\ \Omega$·cm) to

cross check earlier measurements. Improved modeling capability to accommodate small deviation from collimation, thereby increasing the measurement signal-to-noise by a factor of 10. Completed study of temperature effects to eliminate error due to temperature variations. Completed n and k measurements on several new of samples to establish the statistical limits of the measurement. Our analyses indicate that n can be determined to an accuracy of better than a part in 10^4 and k can be measured to better than $\pm 5 \times 10^{-5}$, absolute.

- Completed rewriting FORTRAN codes, developed earlier for compound semiconductors, to model the IR response of the silicon wafer in the 400 cm^{-1} to 4000 cm^{-1} region. The model takes into account the absorption by the Si lattice, free carriers, and the interstitial oxygen. The model reproduces all the observed spectroscopic features, namely the multiphonon bands in the 400 cm^{-1} to 1050 cm^{-1} frequency region, the oxygen absorption at 1107 cm^{-1} and, most notably, the large, monotonic low frequency dip in the transmission due to the free carriers. Obtained a complete set of 11 samples with resistivities ranging from 0.3 to 10 Ω.cm (p-type) and 0.02 to 3 Ω.cm (n-type). Virginia Semiconductors polished these wafers on both sides for optical measurements. Measured the transmission of the medium resistivity wafers and modeled the response satisfactorily using the above mentioned procedure for all but the 0.02 3 Ω.cm (n-type) The medium resistivity wafers are essential to validate the model calculations. The predictions of the model for heavily doped wafers ($\rho < 0.01$ Ω.cm) indicate reflectivity changes of less than 1 part in 10^4 which strongly suggests the need for specialized measurement procedures for the heavily doped wafers.



Infrared transmission spectrum from a conducting Czochralzki wafer: data (line) and model calculations (dots) are shown. Note that all the observed features Si lattice, oxygen impurity and the charge carriers are observed and reproduced by the model.

- Contacted Dr. K. Krishnan, Bio-Rad, Inc., a major metrology toolmaker for the Si IC fabrication industry, regarding development of methodology for oxygen metrology in conducting wafers. Bio-Rad has shared with us the details of their FTIR transmission measurement procedure and results, which are being evaluated. Dr. K. Krishnan, Bio-Rad Corp. has provided us with a set of FTIR transmission curves that he measured on medium resistivity wafers. We are used these spectra to guide the model calculations during the initial phase of the model validation.

Publications

Chandler-Horowitz, D., Amirtharaj, P. M., and Stoup, J. R., High-Resolution, High-Accuracy, Mid-IR ($450cm^{-1} \leq \omega \leq 400\ cm^{-1}$) Refractive Index Measurement in Silicon, Proceedings of the International Conference On Characterization and Metrology for ULSI Technology (ICMUT'98) NIST 3/23-3/27/98 (AIP, NY, 1998), p. 207-21.

Wafer and Chuck Flatness and Thickness

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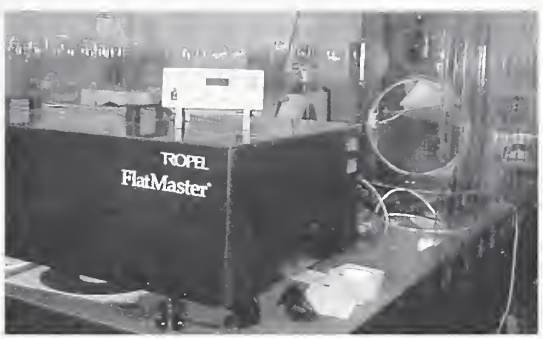
NIST OMP/NSMP

Project Goals

Provide measurement and infrastructural technology to support the generation and measurement of flat wafer surfaces, either free-form or as chucked. Specific goals are: to provide interferometric measurements of as-chucked 300 mm wafer flatness; to develop and demonstrate infra-red interferometric measurements of wafer thickness, thickness variation, and bow; and to develop new models of appropriate polishing processes including those using the NIST-patented Rapidly Renewable Lap.



IR Interferometer Installed at NIST

Customer Needs

Limited lithographic depth of focus budgets for finer features, combined with larger silicon wafers, pose new challenges for flatness and flatness metrology. The 1999 SIA ITRS describes critical site flatness requirements on page 109, Table 32a, and page 111, Table 32b. Conventional vacuum chucks introduce additional distortions to the thickness variations in the wafer itself. These combined effects may reduce the process latitude. The optical metrology tools developed in this project will provide traceable measurements for 300 mm wafers at uncertainties compatible with all lithographies envisioned in the SIA ITRS. Simultaneously, new polishing process understanding will support critical planarization process development.

Technical Strategy

Our primary goal in this project is to develop full aperture interferometric methods to evaluate important wafer characteristics such as flatness, thickness, thickness variation and bow. In parallel we will continue to evaluate performance of novel polishing methods.

The main tool applied to the measurement of flatness will be a new 300 mm aperture, multi-purpose interferometer capable of measurement for flats, spherical and aspheric optics. The NIST **X**-ray Optics **CALIB**ration **I**nterferomete**R** has a target uncertainty for the measurement of flats of 0.25 nm. The instrument was installed at NIST in 3Q99 in a specially designed environment. Once fully operational, XCALIBIR will be available for measurement of as-chucked wafer flatness, over both full- and sub-apertures.

MILESTONE: By FY 2000, demonstrate traceable maeasurement of 300 mm diameter flats.

MILESTONE: By FY 2001,demonstrate measurement of as-chucked 300 mm wafers on XCALIBIR

As-chucked wafer flatness depends both on the chuck and on thickness variations in the wafer. A second major tool to be applied in this project is the Flatmaster, a prototype infrared interferometer built for NIST by Tropel Inc, based on a NIST patent. Using a diverging wavefront, the instrument is designed to provide measurements of thickness, thickness variation and bow. For single-side polished wafers, the scale of the back surface structure limits system performance. Competing measurement strategies for double-side polished wafers must be evaluated.

MILESTONE: By FY 2000, demonstrate measurements of single and double sided wafers using Flatmaster IR interferometer.

NIST developed, and received a patent for a novel lapping system compatible with both diamond lapping of semiconductor substrate materials and with chemo-mechanical polishing.

The system is also a convenient platform for development of measurements and models to attempt to clarify the contributions of the various mechanisms in CMP.

MILESTONE: By FY 2002, develop a model separating chemical and mechanical components in CMP and test experimentally.

Accomplishments

- Developed the Rapidly Renewable Lap concept. Demonstrated for diamond lapping of semiconductor substrates, lapping of photomask blank materials, and CMP for silicon, tungsten and sheet oxide. Patented, and licenced to Rodel Inc, who is further developing technology the the Center for Nanomachined Surface, a University –based research institution at the University of Delaware.
- Demonstrated and obtained patent for IR interferometric measurement of wafer thickness, thickness variation, and bow. Instrument based on patent built by Tropel Inc and installed at NIST.
- Demonstrated interferometric measurement of chuck-induced wafer distortions on 150 mm wafers. Demonstrated novel glass and foamed ceramic chucks.
- Developed new implementation of Ritchey-Common test allowing interferometric measurement of 300 mm diameter flats (wafers) in a diverging wavefront from a smaller aperture interferometer.
- Developed concept for XCALIBIR. Installed at NIST in 3Q99. Preliminary noise floor measurements made.

Set-up for environmental enclosure test after XCALIBIR installation at NIST (above) and preliminary evaluation of high spatial frequency noise (below) of 0.037 nm rms.

Fundamental Process Control Metrology for Gases

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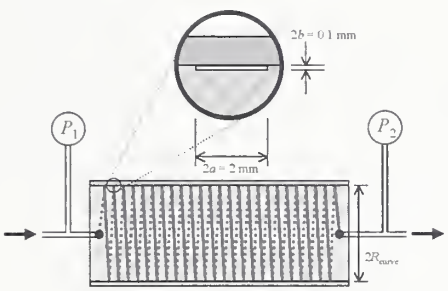
Funding Sources:
NIST OMP/NSMP

Project Goals

Develop primary flow standards in the flow range from 10^{-7} mol/s to 10^{-3} mol/s and transfer this flow measurement capability to the U.S. semiconductor industry. (10^{-3} mol/s corresponds to 1344 sccm (standard cubic centimeters per minute).)

Support semiconductor process-control development with improved residual gas or partial pressure analyzers (RGAs or PPAs), and *in situ* RGA and gas flow calibration techniques.



Laminar flow element (S.A. Tison & L. Berndt, 1997)

Customer Needs

Many industrial processes require the accurate metering of mass flow rate over the range from 10^{-7} mol/s to 10^{-3} mol/s. In particular, the SEMI/SEMATECH Mass Flow Controller working group identified the need to measure flow rates in this range with uncertainties of 1% or less and identified the need for national flow standards with uncertainties of 0.2% or less. To meet these needs, new primary flow standards and improved flow measurement techniques for industrial applications must be developed.

The increasing volume and complexity of vacuum processing in the semiconductor industry requires improved real-time process monitoring and control of process gases, reaction products, and gaseous contaminants. RGAs are the most promising candidates for this task, and are already used in a variety of vacuum processes, but their often unpredictable performance has limited these applications. Realizing their potential requires a better understanding of the factors limiting their performance, particularly when operating with reactive process gases, and the development of *in situ* calibration techniques to compensate for instrument drifts in process applications.

Technical Strategy

Recent work has made use of a constant-volume (pressure rate-of-rise) primary standard that we developed to measure flows up to 1000 standard cm^3 with uncertainties of about 0.1%. A newly completed constant-pressure (variable volume) standard is under evaluation, and it will extend the range to 10,000 standard cm^3.

We have developed very stable transfer standards based on laminar flow through a thermostatted helical channel. Such standards have been used to perform on-site proficiency tests of industrial flow standards at a number of fabrication facilities and TMFC manufacturers. An improved transfer standard based on a metal capillary is nearly complete.

Current meter designs have calibrations that depend on gas properties such as heat capacity or viscosity. An ideal flowmeter either would have no such dependence or would measure the required properties *in situ*. A candidate for such a flowmeter is one that measures the phase shift of a sound wave propagating in the flowing gas. A prototype acoustic flowmeter has been constructed and characterized. Knowledge of the sound speed, obtained from *in situ* measurements, allows conversion of the flow-induced phase shift to a flow velocity, and thus a volumetric flow rate. The gas's equation of state (nearly ideal) plus measurements of pressure and temperature allow conversion to a mass flow rate. The acoustic flowmeter's present resolution is approximately 0.05 % of the full scale flow of 10^{-3} mol/s. Future measurements will test recently developed theories of sound in ducts with flow.

Improved theoretical understanding will allow reduction of the flowmeter's uncertainties.

NIST vacuum (partial-pressure) standards have been used to examine the performance characteristics of commercial RGAs, the most flexible instruments available for *in situ* monitoring of process gas composition. These studies found that the performance of RGAs depends not only on instrument design, but also on instrument operating parameters. In particular, these parameters can significantly affect electron and ion space charge within the RGA, which in turn can change performance characteristics by orders of magnitude. For most RGAs the performance can be optimized by proper adjustment of instrument operating parameters, guided by *in situ* calibration results. Within the past year the RGA studies have been extended to the new CIS instruments.

The performance of RGAs is also significantly affected by the gases being measured, which is a critical issue for the reactive gases used in many semiconductor processes. We have explored these problems in a collaboration with the University of Maryland on the use of RGAs to control a tungsten deposition process in a commercial tool. This experiment involves the measurement of two highly reactive gases, WF_6 and HF. The objectives are threefold: To test *in situ* RGA-calibration procedures in a process tool, to examine the quantitative behavior of RGAs operating under process conditions, and to examine the feasibility of using RGAs for process control.

MILESTONE: By 2000, complete testing of a primary flow meter based on constant-pressure operation.

This flowmeter uses optical interferometry to measure and control the displacement of a piston of known cross-section. Controlling the piston's rate of displacement maintains a constant pressure in the gas accumulation volume. Preliminary tests against the NIST transfer standard show agreement to within 0.2 %.

MILESTONE: By FY 2000, develop species-independent, acoustic flow meter techniques for rapid (<1 sec), accurate (<1%) measurement of corrosive, reactive process gases.

Measurements made with a prototype acoustic flowmeter were analyzed and compared them with a new theory of sound in ducts with flow. Remaining work has been postponed to 2001 to allow completion of the new primary and transfer standards.

MILESTONE: By FY 2000, characterize new flow transfer standard.

Construction of a new transfer standard based on a laminar flow impedance is nearly complete. It is expected to operate at higher flow rates with a smaller slip correction and much smaller centrifugal effects than the existing standard.

MILESTONE: By FY 2000, hold workshop at NIST on mass flow control for the semiconductor industry.

Industry needs identified at this workshop will be used to guide work on gas flow standards at NIST. Issues and potential participants for the workshop, scheduled for May 2000, have been identified.

MILESTONE: By FY 2000, Complete development of in-situ calibration techniques for residual gas analyzers that are applicable to semiconductor processing equipment.

The system has been designed, constructed, installed, and preliminarily operated on the tool at the University of Maryland.

MILESTONE: By FY 2000, demonstrate control methodology for plasma processing by integrating flow controllers and gas analyzers for real time process control and end-point detection.

A semi-quantitative, real-time process sensor was demonstrated in 1999. Feedback control processes have been delayed pending resolution of quantification issues

Accomplishments

- We improved the theory for transfer standards based on a laminar flow impedance. The present NIST transfer standard for low flow rates below consists of a channel that is rectangular in cross-section and is curved into a helix. After accounting for slip at the walls and acceleration of the gas along the channel, the results for helium,

nitrogen, argon, and sulfur hexafluoride agreed with the improved theory to within 0.2% over a factor of 1000 in Reynolds number. A centrifugal instability due to the helical shape occurs at the Reynolds number predicted by theory, and the centrifugal effects agree with a rescaled numerical calculation to within 1 %.

- Initial results using an RGA to monitor the tungsten deposition process at the University of Maryland showed little correlation between the RGA signals and the process. Over the course of the past year this situation has been dramatically improved by several changes in the system and measurement methodology. Key factors are sampling of the process gases directly from the process chamber, use of clean and heated sampling system with minimum surface area, analysis techniques to account for the high level of background gases, and calibration techniques to compensate for instrument drift.
- A significant amount of data have been obtained that show strong correlations between the RGA signals for HF and H_2 and the deposited tungsten. Most of these data were obtained using alternate cold wafers (no W deposition) to calibrate the RGA. While effective, any technique that requires 50% non-product wafers will be unacceptable to industry. More recently, equivalent results, but without non-product wafers, have been obtained using a NIST-constructed *in situ* RGA calibration system.
- Using the calibrated RGA signals, process-control experiments have been conducted with control of the tungsten deposition maintained within about ± 5%. These results are surprisingly good because the process that can be operated in the University of Maryland tool, as presently configured, is very inefficient. Modifications are underway to increase the efficiency by an order of magnitude, which should result in a corresponding increase in the RGA signals relative to background noise.

Low Concentration Humidity Standards

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Funding Sources:
NIST OMP/NSMP
Other Agency

Project Goals

The primary objective is to establish quantitative standards enabling the accurate measurement of trace quantities of water vapor ($< 10^{13}$ molecules cm^{-3}). This effort supports the development and application of commercial humidity sensors used for gas purity measurements, and inline monitoring and process control – functions that are relevant to minimizing wafer misprocessing.

Customer Needs

As discussed previously in the 1997 NTRS in the chapter entitled Metrology, the evolution of sensor-based metrology for integrated manufacturing requires the development of in-situ sensors enabling in-time measurements. In Table 60 entitled Metrology Difficult Challenges, the need for robust and accurate sensor technology and impurity detection in starting materials is highlighted. Of the known impurities in processing gases, water vapor is one of the most ubiquitous and difficult to eliminate. Thus its measurement and control is often critical to various semiconductor-related processes.

Although a variety of high sensitivity sensors of water vapor are available, most do not directly measure water in the gas phase. Rather they typically respond to moisture-induced changes in bulk or surface properties associated with the adsorption of water vapor. Consequently, a rigorous first-principles determination of sensor response is often precluded, thus compromising accuracy. Moreover, since many such devices exhibit drift and poor reproducibility frequent recalibration is required. Interpretation of these measurements is also complicated by complex physical interactions of water vapor with technical surfaces in transfer lines, in reaction chambers and in sensor housings.

The development of accurate and robust water vapor sensors requires well-characterized reference standards against which such devices can be evaluated. This should include a primary method of measurement for water vapor concentration and a complementary method yielding high-precision and stable sources of water vapor. By providing access and traceability to the unique capabilities at NIST discussed below, instrument manufacturers and sensor users can assess the overall performance and accuracy of their measurements.

Technical Strategy

Our strategy is to establish complementary capabilities in high-precision generation and measurement of water vapor. Accordingly we have developed a thermodynamically based humidity source capable of delivering 3 mmol to 3 nmol of water vapor per mole of dry gas. This unique system, known as the low frost-point generator (LFPG), serves as the project cornerstone. Here the water vapor concentration in a gas stream is precisely controlled by active regulation of the saturator temperature and pressure. The LFPG saturator has a temperature stability of better than ± 2.5 mK (see Fig. 1) giving a relative precision of better than ± 0.5 % in the generated water vapor concentration. With this level of stability and range of operation, the LFPG is ideally suited as a platform for testing the performance of various sensing and humidity generation technologies. To date, it is has been used to characterize systems at the research and development stage as well as commercial devices.

On the measurement side, we are developing absolute techniques based upon the absorption of optical or near-infrared laser radiation. It has long been known that molecular concentration

can be inferred from first-principles through spectroscopic measurements. Recent advances in source and detector technology, and new techniques that extend the sensitivity of laser absorption measurements now enable the precise sensing of water vapor at concentrations below 10^{10} molecules cm^{-3}. As an example of this approach, we measured nmol/mol levels of water vapor generated by the LFPG using a custom-designed diode laser hygrometer (DLH). The linear range of response and resolution were demonstrated to be greater than 1000/1 and less than 0.25 nmol/mol, respectively. See Fig. 2. Also as an indication of the potential for making absorption spectroscopy quantitative, absolute response of the system was measured to within 5 % of its expected value. These experiments were critical to the development of a similar DLH that is expected to be commercially available in the near future.

A common technology used by the semiconductor industry for delivering controlled quantities of water vapor is based upon the

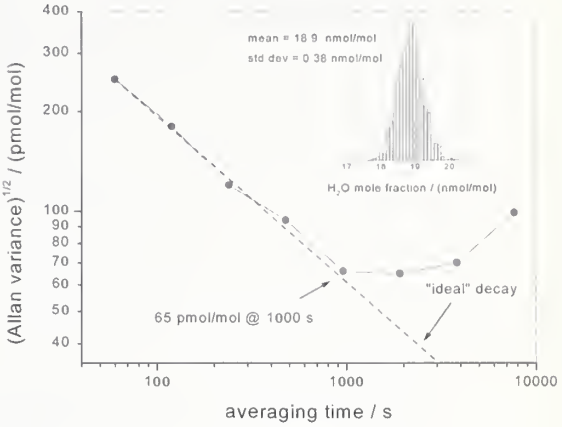

Fig. 2: Allan variance plot and histogram (inset) illustrating the combined stability of the LFPG and DLH detection system.

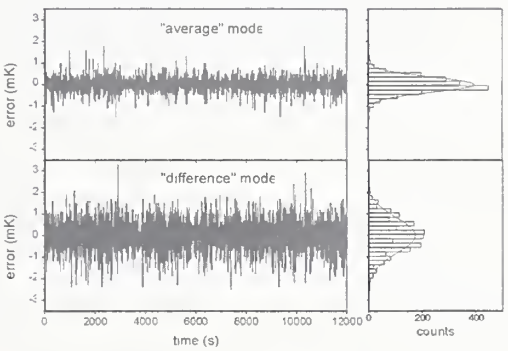

Fig. 1: Steady state response of saturator control thermometers in NIST low frost-point humidity generator.

Of the absorption methods, the cavity ring-down spectroscopy (CRDS) is expected to be the most suitable for a primary method. In CRDS the measured concentration is directly linked to observations of time and frequency and requires no absolute determination of system responsivity. Ultimately, our intent is to realize a new primary method of water vapor measurement based upon CRDS.

MILESTONE: By 2000, complete intercomparison of commercial standard humidity generators for the range (10^{10} to 10^{12} molecules cm^{-3}).

controlled permeation of water vapor through a material, followed by mixing and dilution with a dry gas of known flow rate. In FY 2000 we are comparing a representative sample of such standard generators to the LFPG using a commercial water vapor sensor as a nulling device. A precision of approximately 1 nmol/mol has been achieved with this approach. The results of these experiments will be disseminated to the instrument owners and the technical community at large through oral presentations, technical reports and archival publication. We anticipate that these measurements will help harmonize known disparities in these industrial standards.

MILESTONE: By 2001, demonstrate CRDS as primary method of measurement for low concentration humidity standards.

Initially we will measure the output of the LFPG over its entire operating range using CRDS, and compare these observations to existing gravimetric standards. Eventually, this spectroscopic approach will supplant the gravimetric methods and provide a basis for all measurements of water vapor relying upon absorption spectroscopy. To this end, the line

strengths of relevant absorption transitions will be referenced to the known concentration of plasma process measurements water vapor at the triple point of water.

MILESTONE: By 2002, extend the lower operating limit of the LFPG to –120 °C.

This modification to the LFPG will enable us to reduce by nearly two orders of magnitude the minimum water vapor concentration, thus expanding our capabilities to address ultra-trace levels in the parts-per-trillion range.

Accomplishments

- Developed a high-precision humidity generator suitable as reference standard and useful for testing and calibration of high sensitivity hygrometers.
- Demonstrated quantitative measurements of water vapor concentration in the range 1 to 1000 nmol/mol using laser absorption spectroscopic techniques.
- Developed a precise experimental technique for intercomparing other standard generators to NIST's humidity standards.
- Developed CRDS system for absolute measurements of water vapor concentration.

FY Deliverables

Experiments

In FY 2000 we will complete the intercomparison of standard humidity generators. Using the CRDS technique, we will also measure trace levels of water vapor in commercially supplied source gases used for epitaxial growth of semiconductor films.

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Plasma Process Measurements

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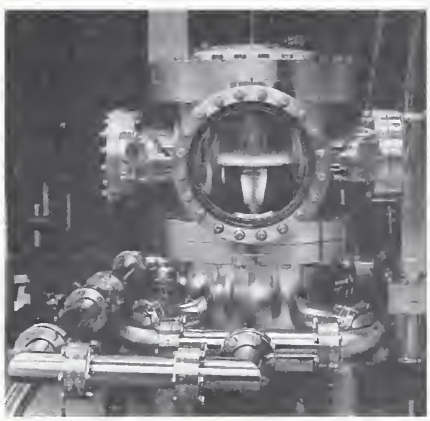
NIST OMP/NSMP
NIST ATP
NIST SRD
NRC
Other NIST STRS

Project Goals

To develop the diagnostic techniques and physical understanding of low temperature discharges necessary for real-time control and predictive modeling of semiconductor plasma etching and deposition processes.



Customer Needs

To maintain its competitive world position, the U.S. semiconductor industry is continually developing microelectronic devices with smaller feature dimensions. This trend requires ever increasing control of the plasma discharges used in the fabrication processes, preferably in real time. Additionally, the development of new processes relies increasingly on predictive system modeling due to the increasing complexity of the fabrication tools and systems. The activities performed in this project assist the industry in developing and using real-time plasma diagnostics, and provide the fundamental data required to develop and validate plasma models.

Technical Strategy

Standardized, reference discharges are used to develop and validate mass spectrometric and optical diagnostics for use as plasma monitors. The most intensively studied discharges are generated in GEC Radio Frequency Reference Cells, which are used by numerous research labs around the world. By studying well defined discharges, the performance of diagnostics can be determined, and the measurements can be used to validate various plasma models. Additionally, the assessment and determination of fundamental data describing collision processes in reactive plasmas allows for the development of accurate plasma models.

Many existing plasma diagnostic techniques are not compatible with the manufacturing environment. To enable improvements in process control, a need exists to develop new types of sensors that are compatible with industrial reactors and processes. Radio-frequency electrical measurements show much promise as a sensing technique, since they are minimally intrusive and contain valuable information about the flux and energy of the ions bombarding wafers during processing. The electrical models and algorithms needed to extract this information are currently under development.

MILESTONE: By 2001, develop rf-based ion flux and ion energy measurement technology, transfer the technology to industrial partners, and assess its utility in commercial plasma processes.

The determination of the identity and energy of ions generated in plasma discharges is critical for the understanding and modeling of reactive plasmas, particularly those containing complex gas mixtures. Mass spectrometry is being applied to high density, inductively coupled plasmas generated in common plasma processing gases in the GEC Cell to measure absolute ion fluxes, relative ion intensities, and ion energies.

MILESTONE: By 2000, complete measurement of ion fluxes and energies in reference plasmas containing CHF_3, C_2F_6, c-C_4F_8, and CF_3I.

MILESTONE: By 2002, measure the composition and energies of the ion fluxes generated in reactive plasmas exposed to semiconductor wafers.

Fluorocarbon plasmas are widely used by the semiconductor industry to etch silicon, silicon dioxide, and silicon nitride films and to clean the reactors which deposit these films. In both etching and chamber cleaning, the spatial distribution of chemical species in the plasma is

an important concern. The development of predictive models for species distributions is currently limited by a lack of experimental measurements needed to validate the models.

MILESTONE: By 2001, provide 2-d maps of the spatial distribution of multiple chemical species in fluorocarbon plasmas, for validation of plasma simulation codes.

Plasma uniformity across the diameter of the wafer is a critical control parameter for ensuring high etch yields. Optical tomography can be used to determine the plasma uniformity in a plasma source. A fiber optic based optical tomography sensor is being designed at NIST for use on commercial-type plasma reactors. This requires an optical system designed to work with small diameter optical ports combined with a fast data acquisition system.

MILESTONE: By 2001, complete development of optical tomography as a plasma uniformity diagnostic, and demonstrate performance on a commercial etching reactor.

Electron-interaction data are the most fundamental input parameters of plasma processing models. NIST provides the most reliable source of such data in the world for a small number of plasma processing gases. The assessment and derivation of available electron-interaction data continues for gases of interest to the plasma processing community as determined by interactions with semiconductor manufacturers and plasma tool companies.

MILESTONE: By 2001, complete an assessment of the available electron-interaction data for the most commonly used plasma processing etching gases.

MILESTONE: By 2003, complete an assessment of the available electron-interaction data for the most commonly used plasma processing deposition gases.

Increased control over semiconductor manufacturing processes requires the development of new real-time and in-time diagnostics as part of open- and closed-loop plasma process control systems is becoming increasingly important. Various new diagnostics, such as optical tomography, teraHertz spectroscopy, diode lasers and cavity ring down spectroscopy, show promise as plasma process control instruments.

MILESTONE: By 2003, demonstrate new plasma diagnostics as part of a plasma process control system.

Accomplishments

- A new method for monitoring the total ion flux at wafers during high-density plasma processing was developed. The method relies on measurements of the radio-frequency bias current and voltage supplied to the wafer electrode. The measurements were interpreted using a new model of the sheath region adjacent to the wafer. The sheath model was tested by experiment and found to be accurate. Algorithms for monitoring the ion flux using the new sheath model were derived and were found to be an order of magnitude more accurate than previous methods.

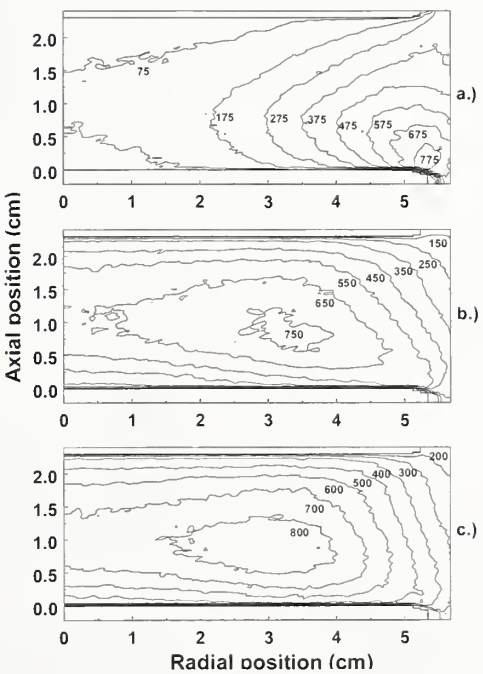
- Absolute, mass-resolved ion fluxes were measured in high density, inductively coupled processing plasmas in CHF_3 as a function of plasma pressure, power, and reactor geometry. These data are essential to understanding the etch process in CHF_3 plasmas, and are used by industry to validate plasma reactor models. CHF_3 has become one of the most commonly used processing gas, and these are the first measurements indicating the identity, energy, and intensity of the ion flux generated in these discharges.

- The NIST standard reference database for electron interactions with CF_4, CHF_3, C_2F_6, and C_3F_8 were updated to include recent experimental measurements of several important parameters. Many of these measurements were prompted by the original NIST assessments of the available data. Additionally, recommended data for Cl_2 were derived and published. The new data were made available on the NIST website. This update enables NIST to continue to provide the best available fundamental data to the semiconductor industry for modeling and reactor design purposes.

- A new fiber optic based optical tomography sensor has been built to measure 2-D plasma

uniformity. This new sensor simultaneously acquires 82 different optical emission measurements through two small windows, significantly reducing the required data acquisition time (<1sec) from the previous single detector tomography sensor (>30min.). Initial plasma distributions have been obtained with this detector from the GEC-ICP RF Reference Cell.

- A new technique was demonstrated for controlling the spatial characteristics of chamber-cleaning plasmas using a variable-impedance load attached to one electrode of the GEC Reference Cell. Varying the load impedance allows one to control the path of radio-frequency current through the plasma, which in turn allows control of the spatial distribution of reactive species in the plasma, as verified by two-dimensional planar laser-induced fluorescence measurements of the CF_2 radical. This control method could be used to direct reactive species in chamber-cleaning plasmas toward the reactor surfaces most in need of cleaning, or to increase the uniformity of reactive species across the wafer surface during etching.



2-D maps of CF_2 density in the GEC cell with various impedances: a) minimized current, b) intermediate current, and c) maximized current.

- Pulsed operation of the GEC-ICP RF Reference Cell was investigated. Interruption of rf power to the inductive coil collapses the sheaths within the plasma which neutralizes accumulated surface charges and improves the etching process. Different time-resolved diagnostics (optical emission, diode laser absorption, intensified CCD imaging, mass spectrometry, Langmuir probe, coil current and voltage, reflected power) have been applied to study this new mode of discharge operation and are being investigated as potential process control parameters. With electronegative gases, such as O_2 and CF_4, the GEC-ICP RF Reference Cell exhibits an exceptionally long capacitive mode plasma when the rf power to the coil is resumed. This enables detailed studies of the processes responsible for the E (capacitive) to H (inductive) mode transition.

FY Deliverables

Standard Reference Data

In FY99, additions to the "Electron Interactions with Plasma Processing Gases" database (www.eeel.nist.gov/811/refdata) included: posting of the recommended data for Cl_2, and the updating of the data for CF_4, CHF_3, C_2F_6, and C_3F_8. This site experienced over 3000 hits in FY99.

Collaborations

Modeling of electron transport in CF_4 using the NIST standard reference data for electron interactions was performed and published in collaboration with researchers from the Universite Paul Sabatier, Toulouse, France.

A measurement of total electron scattering cross sections from Cl_2 was published in collaboration with researchers at the University of Maryland, College Park, Maryland.

Plasma-ion data from NIST was combined with ion-molecule cross section measurements from the College of William and Mary, Williamsburg, VA, to obtain a fuller understanding of ion transport in CF_4 and CHF_3 discharges. The collaboration resulted in a joint archival publication.

The University of Texas-Dallas and NIST are collaborating on the design of a new inductively coupled plasma coil. The uniformity of plasma production by the new coil will be investigated using optical computer aided tomography being developed at NIST. The new coil is designed to alleviate problems associated with transmission line effects on the coil, thereby improving the uniformity of commercial etching reactors.

An ongoing effort continues with ATP Intramural funding to develop a plasma uniformity process control sensor based on optical computer aided tomography. Real or in-time measurements of plasma uniformity is of interest to the semiconductor industry and plasma etching tool manufacturers such as LAM Research.

In collaboration with scientists at Air Products and Chemicals, Inc., the destruction efficiencies of CF_4, C_2F_6, and NF_3 in chamber-cleaning plasmas were measured and published. The highest destruction efficiencies were observed at conditions predicted by previous studies, at which the applied rf power is most efficiently utilized by the plasma.

A collaboration was initiated with Eaton Semiconductor to investigate whether plasma photoresist ashing processes can be improved by applying rf power to microwave downstream plasma ashing reactors.

Committee Participation

Gaseous Electronics Conference Executive Committee – Kristen Steffens serves as the treasurer of the GEC.

SEMATECH Radio Frequency Advisory Group – Mark Sobolewski serves as a member of this group.

Technical Working Groups on Front-End Processing and Environmental Health & Safety – David Green serves as a member of these working groups.

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Metrology for Contamination-Free Manufacturing

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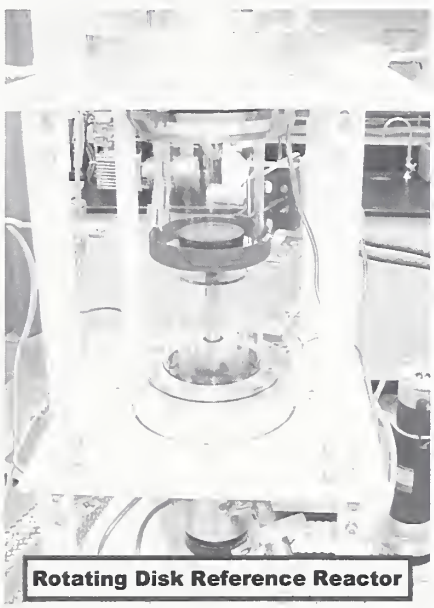
Project Goals

Acquire an improved understanding of the physics/chemistry of gas-phase generated microcontaminants in thermal CVD reactors. Develop a predictive capability for this phenomenon that can be utilized to guide process parameter selection and develop microcontamination standards. The development of experimentally-validated numerical models for microcontaminant formation, growth and transport in rotating disk CVD reactors is a specific goal of this project.



Rotating Disk Reference Reactor

Customer Needs

The 1999 SIA ITRS identifies the need for a more fundamental understanding of reactor contaminant formation and transport. It also calls for the development and experimental validation of advanced chemistry/contamination models for defect-free equipment. These needs are being driven by the relentless decrease in feature size. As feature size decreases, the allowable particle contaminant size also decreases. Upon attainment of the 100 nm technology node in 2006, the allowable particle size will only be 33 nm. The current understanding of particles in this size range is extremely limited. These particles are primarily gas-phase generated as opposed to the larger particles that may enter the reactor in the process stream or flake off equipment surfaces. Thus, there is a critical need for the type of research effort being carried out by this project. It will be very difficult to attain particle control in this size regime without the more fundamental understanding of the physics/chemistry of gas-phase generated particles being sought here. This enhanced understanding will underpin the development of the microcontamination models that are necessary for particle control in thermal CVD reactors.

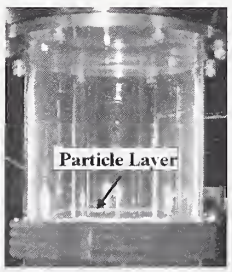
Technical Strategy

The approach being employed here is to carry out a combined numerical/experimental effort in which particle dynamics are probed optically in a rotating disk CVD reactor in close coordination with the development of several microcontamination models. This type of synergistic multimode approach is optimal for achieving an enhanced understanding of the basic physics/chemistry underlying the microcontamination phenomenon. The rotating disk configuration is ideal for this type of study because of its simple and well-defined flow in which particles form in a highly accessible region of the reactor.

An optically-accessible rotating disk CVD reactor has been constructed and installed for detailed experimental investigation of microcontaminants. This reference reactor can achieve a substrate temperature of up to 1300 K and a rotation rate of 1000 rpm. Silicon CVD can be performed at the purity levels required for microelectronics fabrication. Raman spectroscopy is utilized for *in situ* temperature measurements in this reactor, while light scattering is employed to observe particle behavior.

Several microcontamination models are being developed in close conjunction with the experimental effort. These models are based on aerosol dynamics algorithms for particle formation, growth and transport. Two models employ a one-dimensional formulation valid in

the central portion of the reactor. Each utilizes a different type of aerosol model, thus enabling synergistic comparisons and cross checks between them. A third model in early development is a full two-dimensional axisymmetric formulation that will enable the prediction of particle behavior anywhere in the reactor. Experimental data will be compared with results from these models in order both to validate them and help guide the experiments.



Silicon particle layer above heated rotating disk produced by silane injection in helium carrier gas at a reactor pressure of 150 torr.

MILESTONE: By 2000, complete both Raman scattering (for temperature) and particle scattering measurements over an extended process parameter range [(e.g., disk rotation (500 – 1000 rpm) pressures (100 – 300 torr) temperatures (1000 K – 1200 K)] and compare with results from numerical models.

Experimental data on microcontaminant behavior is essential for gaining a fundamental understanding of the physics/chemistry of this phenomenon as well as for validating the numerical models currently under development. The laboratory installation of the rotating disk reference reactor has been completed, and the data acquisition phase of this project can commence.

MILESTONE: By 2001, complete development of both one and two-dimensional experimentally-validated models for microcontamination in rotating disk CVD reactors.

The development of the microcontamination models is a synergistic activity in close conjunction with the experimental portion of this project. The models are all in various phases of development but currently lack any experimental validation. The quality of the numerical/experimental comparisons over ranges of process parameters will determine which of these models will ultimately be of use in a predictive capability for microcontamination in semiconductor processing. The selected models can then be used to obtain information on microcontaminant behavior that is difficult or impossible to obtain experimentally.

MILESTONE: By 2002, complete investigation of microcontamination in rotating disk CVD reactors utilizing numerical models over a wider process parameter range than is possible experimentally.

Accomplishments

- Performed flow visualizations in the experimental rotating disk reactor over an extended process parameter range. The parameter regimes for which uniform stagnation flow occurs were identified. It was determined that it is important to utilize a light gas, such as helium, in order to obtain suitable background flows for the microcontaminant studies.

- Initiated microcontaminant light scattering experiments in the rotating disk reactor. These experiments, utilizing silane injection in a helium carrier gas, revealed a highly visible narrow layer of particles just above the heated rotating disk. Variations in pressure and flow rate provided an indication of the behavior of this layer with process parameter adjustments.

- Significantly improved the operation of the NIST one-dimensional microcontamination model. This effort involved error removal and extension of the parameter range over which solutions can be obtained. Both the robustness and efficiency of this numerical model have been greatly enhanced. In particular, the algorithm that computes particle growth via condensation has undergone significant improvement.

- Completed development of a suite of model problems that can be utilized for assessing

the accuracy of microcontamination algorithms for stagnation-flow reactors. These model problems represent various physical aspects of the aerosol dynamics but are simplified in order to allow analytical solutions to be obtained. Due to the lack of experimental contamination data for this type of reactor, comparisons with model problems can often be the only means of testing microcontamination codes.

FY Deliverables

Data

Thermochemical data for silicon hydrides and fluorinated hydrocarbons, both species of importance in semiconductor processing, were made available at the following on-line location: http://www.nist.gov/cstl/div836/ckmech/ess.html.

Publications

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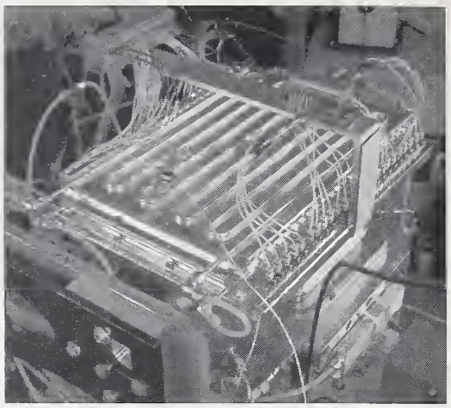
Temperature Sensing for Rapid Thermal Processing



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Project Goals

The goal is to develop the technologies required to enable the measurement of RTP wafer absolute temperatures with uncertainties of 2° C at 1000° C as prescribed in 1999 SIA ITRS.

Our project, initiated in FY97, has approached this goal with four objectives: (1) To improve calibration wafer technology to a 1 °C standard uncertainty by demonstrating the use of TFTCs in conjunction with Pt/Pd wire TCs on test wafers in RTP tools; (2) To develop methods for in-tool RT calibration, which relate TFTC wafer temperatures to indicated radiance temperatures; (3) To develop and validate models to account for wafer emissivity and chamber reflected-irradiation effects on temperatures determined from model-corrected RTs calibrated against blackbodies; and (4) To collaborate with the semiconductor industry in implementing new methods for reliable and traceable temperature measurements.

Customer Needs

The measurement needs of the semiconductor manufacturing industry have been stated the 1999 SIA ITRS which includes a requirement of measurement and control of RTP tools to +/- 2° C at 100 °C during processing with traceable calibrations to the ITS-90. Current industry measurement capabilities are +/- 6° C or three times that uncertainty and major producers have voiced concerns to SEMATECH.

Our customers are the device manufacturers and the suppliers of thermal processing equipment and temperature measurement instrumentation. This community forms our project's Advisory Group (20 companies meeting annually at NIST since 1997). They serve as a bridge between research and practice, provide advice on shaping objectives, and generate opportunities for technology transfer. This community is also represented by SEMATECH, which has set the roadmap requirement for the year 2000. In a recent planning meeting for demonstrations of the NIST technology, SEMATECH stated: "Based upon the progress at NIST, it appears that the ITRS roadmap requirements are within reach " [B. Van Eck, SEMATECH, November 5th, 1999].

Technical Strategy

Our strategy is to address the three core elements of our research that will enable the semiconductor industry to meet the roadmap requirement: improved thin-film thermocouple technology; test bed demonstration experiments and associated thermal modeling on sensors systems; and, calibration and characterization of light-pipe radiation thermometers.

The present scope of the thin-film thermocouples (TFTC) technology work includes improving the high temperature capabilities of the calibration wafer and demonstrating TFTC performance to 1000 °C. We are also providing SEMATECH with suitable reference-quality test wafers. These wafers must have temperature measurement combined standard uncertainties of 1 °C. Arrangements are in progress to work with a major equipment manufacturer to demonstrate use of the NIST Test Wafer in a production tool.

We are using the NIST Test Bed to perform inter-comparisons between the TFTC and LPRTs. The aims are (a) to demonstrate calibration procedures for and establish uncertainties of the LPRTs against the TFTCs, and (b) to establish uncertainties for model-corrected LPRTs calibrated against blackbodies. Experimental studies are being designed for these conditions: a higher temperature range (to 1000 °C), a range of wafer emissivities, variable separation distance between wafer and LPRT, and variable chamber wall reflectance. These studies require concurrent efforts to develop and validate radiation heat transfer models to estimate wafer effective emissivities that are essential for establishing uncertainty limits for LPRTs in our Test Bed, and in production tools.

Understanding the performance of LPRT is a recent task that integrates and extends earlier separate studies. LPRTs are the sensor system of choice for high temperature semiconductor materials processing, and are the weak link in establishing improved, reliable temperature measurements. The technical issues are (a) calibration against blackbodies and (b) thermal and optical characterization. We have calibrated three different types of LP systems (light pipe plus interconnects, optical-fiber cable, and detectors). We are quite satisfied with uncertainty results, but need to double the ensemble of LPs examined under a wider set of blackbody conditions (position in the cavity, cooling effects, aperture sizes, etc.). We have determined that the temperature of LPs significantly affects their performance. We seek to thermally characterize the LP and explain calibration and in-tool performance differences through combined experimental and analytical studies. Optically characterizing the LP involves understanding spatial (point-spread function or field-of-view) and directional effects.

MILESTONE: By FY 2000, (1) achieve a combined standard uncertainty of 2°C of surface measurement in the RTP Test Bed up to 1000 °C, (2) evaluate wafer-chamber effects on radiation thermometer uncertainties through detailed thermal models, and (3) provide TFTC test wafers for evaluation in a production tool.

MILESTONE: By 2001,(1) establish calibration procedures for LPRTs using TFTC test wafers with coatings having emissivities ranging from 0.1 to 0.9 to simulate a broad range of industrial conditions and (2) demonstrate radiation thermometer calibration using the NIST TFTC test wafers in an industrial production rapid thermal processing tool with a standard uncertainty of 2°C .

Accomplishments

- Demonstrated uncertainties of less than 1 °C for wafer temperature measurement up to 900 °C in an RTP test bed using new thin-film thermocouple technology. This is a 3x improvement over best industry practice.

- Demonstrated that light pipe radiation thermometers can be calibrated with an uncertainty of 2 °C in an RTP test bed using a TFTC test wafer.

- Demonstrated that light pipe radiation thermometers can be calibrated with an uncertainty of 0.3 °C against a reference-grade blackbody. This is a 5x improvement over best industry practice.

- Developed models to characterize the radiation environment surrounding the wafer in the RTP test bed allowing a radiation thermometer to determine wafer temperature with uncertainty less than 3.5 °C.

- Developed the technology and defined the performance of Pd, Pt, Rh, and Ir thin films on oxidized silicon wafers up to 1000 °C.

- Reduced the uncertainty of calibration of thin-film thermocouples by a factor of two.

Publications

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Particle Measurements in Support of the Semiconductor Industry

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NIST OMP/NSMP
Other Agency

Project Goals

To develop a facility for accurately measuring particle size/concentration and for depositing monosize particles on calibration artifacts to support the 1999 SIA ITRS' goal of quantifying 60 nm diameter particles by 2001 and 33 nm by 2006.

Customer Needs

The detection, quantification and characterization of particulate contamination on semiconductor surfaces is essential to advanced semiconductor manufacturing. The present practical limit for particle detection is 90 nm diameter. The 1999 SIA ITRS calls for the ability to detect and quantify particles with a 54 nm diameter by 1999 and a 21 nm diameter by 2008, pages 275-276, Tables 78a – 78b. There is currently a need for accurately sized monosize particles in the size range from 60 to 200 nm for developing and calibrating improved scanning surface inspection systems.

Technical Strategy

Last year an electrostatic deposition facility was developed for depositing monosize spheres on a 2.5 cm diameter silicon wafer. This year the performance of this facility along with a low pressure impactor will be characterized using a differential mobility analyzer and electron microscopy in terms of the deposition efficiency and the fraction of muliplet particles deposited (doublets and triplets). In addition, the facility will be used for depositing monosize gold particles for use by Tom Germer in the Physics Laboratory in his study of light scattering by particles on a silicon surface.

MILESTONE: By July 2000, accurately size nominal 65 nm polystyrene spheres and deposit on silicon wafers for use by Physics Laboratory for testing their particle scattering model.

A second focus is on the continued development of the electrospray system, which will be needed for calibration particle sizes smaller than about 70 nm. Efforts will be made to minimize the clogging of the 25 μm diameter capillary. The data will be analyzed and paper written based on last year's size distribution measurements for the electrospray system and the pneumatic atomizer. In addition, electrospray and electrical mobility classification will be used to measure the size distribution of nominal 65 nm particle diameter. This is an important size because it is approximately half of the targeted lithography linewidth for year 2001

MILESTONE: By March 2000, complete a paper on comparing the size distribution of polystyrene aerosols produced using electrospray with that obtained using pneumatic atomization.

MILESTONE: By 2001, complete particle size measurements of nominal 30 nm and 50 nm particles using differential mobility analysis and transmission electron microscopy (CSTL).

MILESTONE: By 2002, complete the necessary modeling for quantifying the uncertainty in the two sizing measurements.

Accomplishments

- Assisted Scatter Works Inc. in establishing traceability to NIST for deposits of eight particle sizes ranging in size from 65 nm to 291 nm. This company was able to establish traceability by using three NIST measured calibration particle sizes including the 100 nm SRM® 1963 and by carrying out a quantitative uncertainty analysis including Type A and Type B uncertainties

- Monosize polystyrene spheres of size 100 nm, 125 nm, 180, nm, and 220 nm were deposited on 2.5 cm diameter wafers at a density of about 30,000 particles/cm^2. The particles were first size classified using a differential mobility analyzer and then deposited using a low pressure impactor. Tom Germer and Liipin Sung from the Physics Laboratory obtained good agreement between their measurements and Germer's

theory for the light scattered by these particles on a surface

- Electrospray technology was demonstrated to be superior to pneumatic nebulization for generating monosize polystyrene spheres of sizes 50 nm and 30 nm. The 10 times larger droplets produced by pneumatic nebuliztion resulted in aggregates of the 30 nm spheres while the electrospray system produced individual 30 nm particles with little evidence of aggregation.

- A manuscript was written summarizing the monosize polystyrene calibration spheres with diameters of 100 nm or less that are available from NIST as well as commercial suppliers. The issues of difference between international standards and traceability to the NIST Standard Calibration Particles are discussed.

FY Deliverables

Deposited monosize polystyrene spheres of size 100 nm, 125 nm, 180 nm, and 220 nm on 2.5 cm diameter silicon wafers for use by Physics Laboratory in testing Germer's model for light scattering by spheres on a wafer surface.

Developed traceability document for The Scatter Works Inc. establishing the traceability of their particle sizing method to NIST.

Publications

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Optical Scattering for Wafer Surface Metrology

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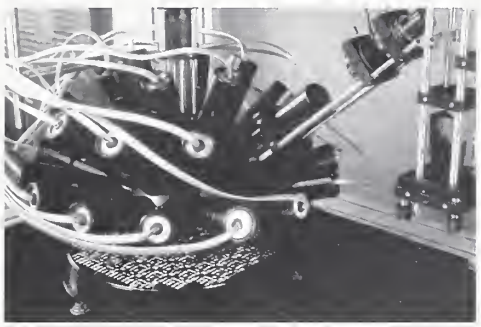
Project Goals

Provide technological leadership to semiconductor and equipment manufacturers by improving the understanding of the behavior of light scattering from defects, contaminants, and roughness needed to improve the optical inspection and characterization of wafer surfaces. A specific goal is to develop the technique of light scattering ellipsometry for defect characterization, and to demonstrate how that technique can yield improvements in defect detection sensitivity.



Customer Needs

The 1999 SIA ITRS identifies the detection and characterization of defects and particles on wafers to be a potentially show-stopping barrier to device miniaturization on pages 275-276, Tables 78a – 78b. The SIA ITRS specifies that in 1999, 54 nm particles must be detectable on bare silicon and nonmetallic films, 69 nm particles on metallic films, and 180 nm particles on wafer backsides. By 2008, these values are expected to decrease to 21 nm, 29 nm, and 70 nm, respectively, for which no solutions currently exist. While the detection sensitivity for defects must be increased, the ability to characterize defects in terms of size, shape, composition, etc., is critical for yield-learning. Defects must be characterized independent of defect location and topology.

With the need to detect smaller defects, the costs of inspecting wafers are skyrocketing. In order for new advances to be implemented in production environments, improvements in sensitivity must be achieved without suffering a tradeoff in throughput and must be cost-effective. The drive towards in-situ sensors for production tools requires techniques which can be effectively miniaturized.

Technical Strategy

Our primary strategy is to develop a fundamental understanding of optical scattering at surfaces so that tool manufacturers can optimize the performance of their instrumentation, in terms of defect detection limits and discrimination capabilities, and characterize the response of instrumentation to different types of defects. Recent work by this group has demonstrated that the polarization of light scattered by particulate contaminants, subsurface defects, and microroughness has a unique signature that can be used to identify the source of scatter. In particular, it was found that small amounts of roughness do not depolarize scattered light. This finding has enabled the development of instrumentation which can collect light over most of the scattering hemisphere, while being blind to microroughness. That instrumentation, for which a patent has been applied, should result in a factor of two improvement in minimum detectable defect size. Specific program elements include:

Polarized Light Scattering Measurements – The goniometric opitical scatter instrument (GOSI) enables accurate measurements of the intensity and polarization of scattered light with a wide dynamic range, high angular accuracy, and multiple incident wavelengths (visible and UV). We measure the light scattering properties of well-characterized samples exhibiting interfacial roughness, deposited particles, subsurface defects, dielectric layers, or patterns. The emphasis is on providing accurate data, which can be used to guide the development of light scattering instruments, and to test theoretical models.

Theoretical Light Scattering Calculations – The focus of our theoretical work is on (a)

developing models that accurately predict the polarization of scattered light, and (b) determining what information can be efficiently and accurately extracted from light scattering measurements. Approximate theories are used in conjunction with more complex finite element time-domain and discrete-dipole approximation techniques to gain an understanding of which parameters affect the light scattering process. Particular cases that are being analyzed include (a) scattering by defects and roughness associated with dielectric layers, (b) scattering by particulate contamination on bare wafers, and (c) scattering by high aspect ratio vias.

Instrument Development – A second instrument, the MHPOSI complements the capabilities of GOSI as a prototype for a production-line light scattering inspection tool. An instrument with twenty-eight fixed detection elements covering the scattering hemisphere, MHPOSI enables a determination of the differential scattering cross section, for individual particles or defects on a wafer surface. This instrument can be configured so that it is blind to interfacial roughness. Together with an understanding of the light scattering functions for different imperfections, MHPOSI has a substantially improved capability for rapidly detecting and identifying defects, particles, and microroughness on wafers.

Numerous models have been developed by this group to calculate the scattering from certain ideal scatterers. As a way of accelerating the rate at which these models are applied in industry, a set of programs, organized as a C++ object class library, will be published on the World Wide Web. By providing a uniform interface for all light scattering models, this library is easily extensible, allowing us and others to add models as they are developed.

MILESTONE: By FY 2000, make models available publicly with a Polarized Light Scattering C++ Object Library. Provide annual updates as models are developed.

PSL spheres are used throughout the industry to calibrate surface inspection instruments. However, they are not representative of defects found in production environments. In order to test theoretical models for light scattering, more complex particles must be studied. The first stage of this work involves studying the behavior of spheres consisting of metals and high dielectric insulators of different sizes. The second stage involves the characterization of scattering from non-spherical particles.

MILESTONE: By FY 2001, measure light scattered by spheres of different materials and sizes on silicon wafers. By FY 2002, extend the measurements to non-spherical particles.

Recent theoretical calculations have shown that the polarization of light scattered by two interfaces is a function of the power spectra of the roughnesses of each interface and a cross correlation function. Experimental measurements are in progress which demonstrate the application of these theories. Algorithms must be developed to allow the roughness parameters to be extracted from experimental data. This work will allow light scattering measurements to fully characterize thin films and will allow inspection instruments to improve their sensitivity to defects on wafers with dielectric layers.

MILESTONE: By FY 2001, develop methodology for characterizing thin film topography using polarized light scattering and perform measurements demonstrating its effectiveness in a variety of situations.

Measurements performed on the MHPOSI demonstrated that PSL spheres of different sizes could be easily distinguished from each other and from residual roughness. While the typical defect in a production environment does not resemble a PSL sphere, the results demonstrate the feasibility of using pattern recognition techniques to enhance the ability of a MHPOSI to learn to characterize defects that are actually found. Interfacing the instrument with an off-line instrument, such as an SEM, would reduce the reliance on those off-line instruments over time by training a MHPOSI to classify defects on its own.

MILESTONE: By FY 2002, demonstrate defect classification learning in a multidetector light scattering instrument using pattern recognition techniques.

Accomplishments

- Measured the polarization of light scattered by polystyrene latex spheres on silicon wafers with and without dielectric layers. The comparison of the measurement results with theoretical predictions was very good, and suggested that light scattering may be competitive with other standard techniques for accurately determining the diameters of standard reference particles.

- Constructed and demonstrated the MHPOSI. Spheres of diameters 100 nm, 180 nm and 217 nm, and microrough wafers were shown to be distinguishable based upon the response of each of the detectors to different incident polarizations. The findings suggest that pattern recognition techniques could be employed with such instrumentation to allow for on-line learning of defect classification.

- Calculations using FETD code have been carried out, to compare the technique with the discrete dipole approximation and perturbation theory techniques. While the FETD code is inefficient, it is expected to have a wider range of applicability than the other techniques, and will become a primary method for performing calculations from structures on surfaces, and for evaluating approximate methods.

- Developed second-order vector perturbation theory for light scattering from roughness. First-order theory has been successful at predicting the polarization of light scattered by roughness for a wide variety of samples, some of which violate assumptions of the theory. The second-order calculations demonstrate the wider application of the polarized light scattering technique for characterizing rough surfaces.

- Measured polarization of light scattered by roughness of the top interface of a dielectric layer on silicon, improving the utility of bidirectional ellipsometry for determining the roughness characteristics of dielectric layers, and improving the ability to detect small defects near rough dielectric layers.

- Improved the GOSI by increasing the detection sensitivity by a factor of twenty and by developing an operating routine that enables full Stokes vector measurements of the scattered light. These modifications allow the instrument to characterize smaller defects on higher quality wafers, and enhances the instrument's ability to fully characterize the light scattered by them.

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Thermophysical Property Data for Modeling CVD Processes and for the Calibration of Mass Flow Controllers

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Funding Sources:
NIST OMP

Project Goals

NIST will measure the thermophysical properties of process gases, "surrogate" gases, and binary mixtures of process and carrier gases. The process gases are used in CVD and the surrogate gases are used to MFCs. The results will be disseminated as a data base providing the heat capacity, thermal conductivity, viscosity, and the pressure-density-temperature relation for the process gases and diffusion coefficients for the gas mixtures.

Principal Investigator, John Hurly, standing beside the gas box containing the acoustic resonators used to measure the speed of sound in process gases.

Customer Needs

The 1999 SIA ITRS identifies "Equipment Modeling" as first in a list of "Technology Requirements" and states that "the drivers for equipment modeling are *equipment design, process control*, . . . " The *Roadmap* indicates that continuing research is needed to obtain experimental data for "transport and thermal constants." This Project will generate transport and thermodynamic property data for the gases used in semiconductor processing. The data will be useful for equipment modeling in CVD processes and the data will also provide a rational basis for the calibration of MFCs used to meter process gases.

Technical Strategy

In the first phase of the work, NIST will measure the speed of sound in the process gases. The data will have uncertainties of 0.01 %, or less. The initial results will range up to 200EC and from 25 kPa to 1500 kPa (or to 80% of the vapor pressure for condensable gases). Later results will reach higher temperatures.

The speed-of-sound data will be used to determine the ideal-gas heat capacities $C_p^0(T)$ with uncertainties of $0.001 \times C_p^0$. Also from the speed-of-sound data, we shall derive pair and three-body intermolecular potentials. For gases at low density, these potentials will be used to compute the virial equation of state $P(V,T)$, the viscosity $\eta(T)$, and the thermal conductivity $\kappa(T)$. For gases where other data exist, results calculated in this way have errors that are less than $0.001 \times V$, $0.1 \times \eta$, and $0.1 \times \kappa$ from 200 K to 1000 K at pressures up to 1.5 MPa or 80 % of the vapor pressure. Later in the program, acoustic techniques will be used to measurement the transport properties, thereby reducing their uncertainties to less than 1 %.

MILESTONE: Measure speed of sound in WF_6, the seventh high-priority gas for MFCs. Publish results

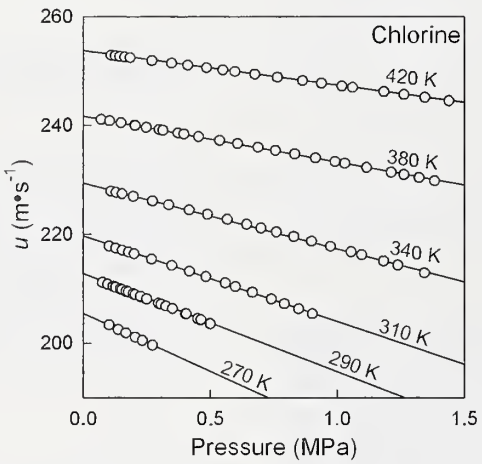
MILESTONE: Publish results on speed-of-sound measurements in HBr and BCl_3.

MILESTONE: Use acoustic techniques to measure the viscosity and thermal conductivity of process gases near 300 K.

MILESTONE: Feasibility test of an acoustic measurement of the diffusion constant of a process gas mixed in a carrier gas.

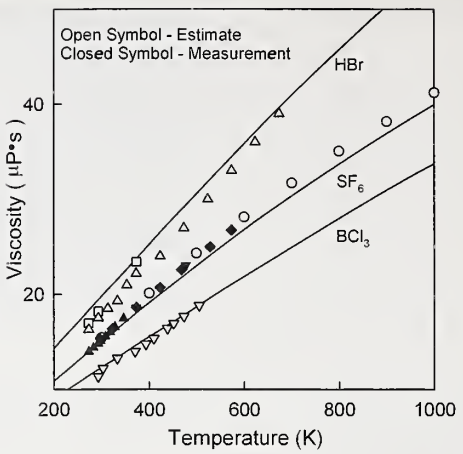
Accomplishments

- During FY98 and FY99, we completed the acoustic facility shown in Fig. 1, completed shake-down tests, and measured the speed-of-sound in CF_4, C_2F_6 Cl_2, HBr, BCl_3, and SF_6.



Representative data. NIST speed-of-sound data for chorine as a function of pressure on various isotherms.

- Developed software for reducing speed of sound data to parameters for hard-core Lennard-Jones intermolecular potentials. Developed software for calculating second and third virial coefficients and transport properties from intermolecular potentials.



Viscosity of gases at low density. The solid curves are computed by NIST using potential models parametrized by speed-sound-data. Solid points are measurements. Open points are published estimates. There are no published measurements for HBr and BCl_3.

FY Deliverables

Software

Prepare first release of a user-friendly data base to disseminate results for C_p^0, P(V,T), of η(T) and κ(T) for process gases and surrogate gases.

Presentations/Talks

"Thermophysical Properties of Process Gases", to the Gas Distribution Systems Working Group, Sunday July 11, at the SEMICON west 1999 conference in San Francisco, CA. (J. J. Hurly)

"Thermophysical Properties of Process Gases", to the SEMI Gas Committee, Tuesday October 19, at the SEMICON Southwest 1999. (J. J. Hurly)

Publications

Hurly, J. J., Thermophysical Properties of Gaseous CF_4 and C_2F_6 from Speed-of-Sound Measurements, *International Journal of Thermophysics*, Vol **20**, (2) 455-484 Mar. 1999.

Hurly, J. J., "Thermophysical Properties of Gaseous HBr and BCl_3 from Speed-of-Sound Measurements" is in progress.

Hurly, J. J., Defibaugh, D. R., and Moldover, M. R., The Thermodynamic Properties of Sulfur Hexafluoride, accepted by the International Journal of Thermophysics.

Hurly J. J., and Moldover, M. R., Thermophysical Properties of Process Gases, Proceedings of SEMICON West 1999.

Radiometric Metrology for Deep Ultraviolet Lithography

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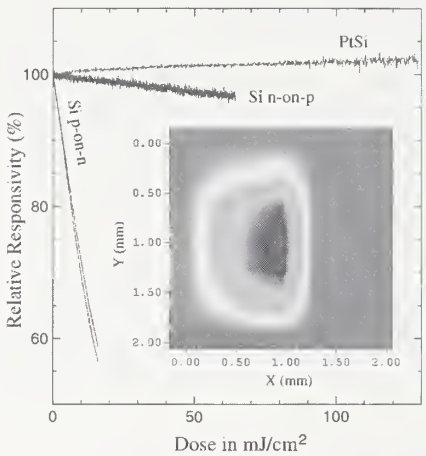
NIST STRS (PL)

Project Goals

Characterize the optical properties of materials and detectors in the DUV and VUV needed for the design of future-generation photolithography steppers operating at 193 nm and 157 nm. Deliver the results of the key optical measurements to the industry to the high accuracy required in the time frame needed to meet their development schedule.



Customer Needs

Over the past several years the semiconductor microelectronics industry has committed itself to the development of 193 nm and 157 nm optical lithographies as successor technologies to enable an uninterrupted Moore's Law decrease in integrated circuit feature sizes. According to the 1999 SIA ITRS, these technologies may carry the industry from the present pilot line 180 nm node down to the 70 nm node, page 154, Figure 23.

The design of these lithography tools requires accurate measurements near 193 nm and 157 nm of the index of refraction, its dispersion, and its temperature dependence of the materials to be used for the optics. However, no accurate measurements of these properties were known for any optical material at these wavelengths until our recent measurements of fused silica and calcium fluoride near 193 nm. The present 193 nm stepper designs are based on these measurements. The optics for 157 nm steppers are expected to be made of calcium fluoride, with index properties determined recently by us, possibly combined with a second material with index properties suitable for chromatic aberration corrections. The choice of this second material depends primarily on the index properties. The industry is awaiting our index measurements for candidate second materials, such as barium fluoride and strontium fluoride. These measurements are in progress. There is also a need to characterize the optical properties of new grades of fluorine-doped fused silica which transmit at 157 nm. These materials may be used as 157 nm masks and possibly lenses.

High accuracy transmittance and reflectance measurements are also needed to identify stable materials that can be used to fabricate the stepper optics. Along with these measurements, we are also currently making scattering measurements in an attempt to make a complete characterization of all the key optical properties of the materials.

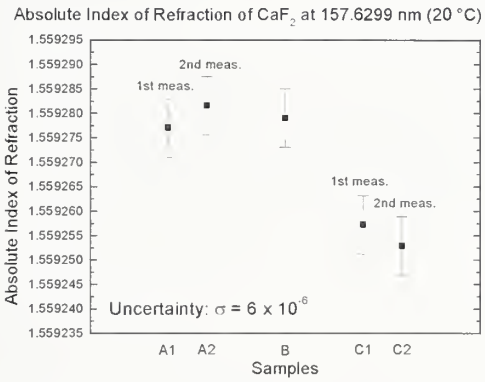
Another key issue is tight exposure control, which is required for satisfactory device fabrication. This calls for investigation of new stable detector and source standards and also the development of accurate radiometric scales in the DUV and VUV.

Technical Strategy

We have developed a way of accurately determining the index of refraction of materials in the UV using the minimum deviation method, by combining measurements using a visible goniometric refractometer with measurements using a UV goniometric refractometer. The UV refractometer can be operated in the VUV using a nitrogen gas purge chamber to allow measurements down to 140 nm with an accuracy of .5 ppm. This is the only facility in the world with this capability, and our index results at

157 nm are the only accurate measurements reported at this short wavelength. Our measurements of the index of nitrogen gas in the VUV using our unique VUV Fourier transform spectrometer allows us to convert our measurements of the indices relative to nitrogen to absolute indices. Use of spectral line sources, with emission wavelengths accurately measured with our VUV Fourier transform spectrometer, allows us to determine the index dispersion, $dn/d\lambda$, in the VUV. Control of the sample and gas temperature to 0.05 °C allows us to determine the temperature dependence of the index, dn/dT.

We have obtained samples of calcium fluoride and fused silica for our index measurements from all the major UV materials suppliers, either through SEMATECH or directly from the stepper manufacturers and materials suppliers. Appropriate samples of alternate 157 nm materials such as barium fluoride and strontium fluoride have been prepared through a collaboration with several major UV materials suppliers. These measurements are done in conjunction with other optical measurements such as transmission, stress birefringence, and laser durability by us and our collaborators for complete optical characterization of these materials.



Measurements of the absolute index of refraction of 3 samples of calcium fluoride near 157 nm at 20 °C.

MILESTONE: By FY 2000, determine the index properties near 157 nm of calcium fluoride and other candidate 157 nm materials such as barium fluoride, strontium fluoride, and modified fused silica. Characterize any sample variations.

In parallel to our goniometric index measurements, we are developing a new interferometric method for measuring the index to higher accuracy, .1 ppm, in the DUV and VUV using our VUV Fourier transform spectrometer. This method is directed to measurements near 193 nm using a deuterium lamp as a continuum source, and may be extendable to 157 nm using synchrotron radiation.

MILESTONE: By FY 2001, make measurements of the index of refraction of calcium fluoride and fused silica near 193 nm interferometrically to an accuracy .1 ppm.

Our efforts for complete characterization of the optical properties of materials involve measuring the transmittance, reflectance, surface and bulk scatter, and surface and bulk absorption. This characterization is done on one of the beamlines at the NIST Synchrotron Ultraviolet Radiation Facility (SURF) which is devoted to material and detector characterization in the wavelength range 120 nm – 320 nm. We have used this method to characterize various samples of calcium fluoride where the transmittance and reflectance was measured with an uncertainty of better than 1%.

SURF II acts as the primary standard for both sources and detectors in the DUV and VUV spectral region. An upgrade to SURF III which included both increase in electron energy to allow useful emission of radiation down to 2 nm, an enhancement in absolute current determination, and the addition of two new beamlines, has been completed as of January 1999. Efforts are underway to use this facility to achieve a 0.1% standard uncertainty of UV irradiance from 3 nm to 400 nm, and will enable accurate, direct radiance and irradiance comparisons with new as well as existing source transfer standards.

Monochromatized radiation from the recently upgraded SURF III along with a cryogenic radiometer is used to provide absolute detector-based radiometric calibrations in the spectral range from 125 nm to 320 nm with a standard uncertainty of better than 1%. This facility has also been used to study the degradation in diodes induced by exposure to UV radiation. A wide variety of diodes (Si diodes from Hamamatsu, nitrided Si diodes from IRD, PtSi, GaN, GaP, GaAsP, and diamond) were characterized for spectral responsivity and uniformity mapping, and the degradation in these diodes at 135 nm was also measured.

A new facility for characterizing the degradation of diodes to excimer radiation at 193 has been completed. This facility allows the measurement of the spectral responsivity of the devices in the spectral range from 180 nm to 500 nm along with the measurement of the reflectivity of the diodes as the devices are irradiated by the excimer radiation. This allows identification of potentially stable diodes for UV irradiance measurements. The facility can also be used to characterize other types of detectors such as photochromic films.

MILESTONE: By FY 2000, characterize the stability of a variety of semiconductor diodes to excimer radiation at 157 nm.

In order to meet the industrial demand for identifying stable diodes suitable for operation at 157 nm, we will characterize detectors for stability towards excimer radiation. The spectral responsivity and the spectral reflectivity of the diodes will be monitored as the diodes are irradiated with excimer radiation at 157 nm.

MILESTONE: By end of 2001, build a state of the art facility for an accurate and complete characterization of the optical properties of transmissive materials.

We plan to use the synchrotron radiation in conjunction with a cryogenic radiometer to measure the transmittance, reflectance, and surface and bulk losses, which would lead to a complete optical characterization of the transmissive samples. Capability will also be developed to make polarization dependent measurements in the spectral range from 125 nm to 320 nm.

Accomplishments

- Developed a method and a facility to measure the absolute index of refraction of materials with an accuracy of 5 ppm down to .140 nm. It also enables measurements of the dispersion and index temperature coefficient at these wavelengths. It is the only facility in the world with this capability.

- Made the world's first and to this date only accurate measurements of the absolute index of refraction of calcium fluoride near 157 nm, and obtained preliminary evidence for supplier variations. These results have been delivered to the semiconductor lithography industry and have gone into the design of the optics for all major 157 nm photolithography stepper development projects around the world.

- Completed construction of our FT700 VUV Fourier transform spectrometer which operates down to .140 nm with an accuracy of $.10^{8}$. It is the most accurate UV spectrometer in the U.S., and only one other in the world has similar capabilities.

- Used our new VUV Fourier transform spectrometer to make the first measurements of the index of refraction of nitrogen gas down to .150 nm. We used this result to obtain absolute indices of materials near 157 nm from relative indices measured in nitrogen gas. The measurements are also needed by the stepper designers to design the stepper optics operating in a nitrogen purge environment.

- Designed and built a facility for characterization of the stability of photodiodes towards irradiation from an excimer laser source operating at 193 nm. The facility measures the spectral responsivity and spectral reflectivity changes as a function of the amount of radiation delivered from the excimer source. A variety of semiconductor detectors such as nitrided Si, PtSi, and GaN has been characterized using this facility. The facility was also used to characterize other types of detectors such as photochromic films.

- Made high accuracy measurements of the transmittance of calcium fluoride using the monochromatized radiation from the synchrotron source coupled with a cryogenic radiometer in the spectral range from 125 nm to 300 nm. Some preliminary results of the reflectance and surface and bulk losses were also obtained. Efforts are underway to study these effects in more detail.

FY Deliverables

Index measurements

Measurement of the index of refraction to .5ppm, along with its dispersion and temperature dependence, near 157 m of calcium fluoride samples from all the major suppliers to establish the extent of a supplier and grade variation.

Characterization of alternate 157 materials

Characterization of the optical properties of materials other than calcium fluoride that may be candidates for 157 nm optics. Alternate materials are needed for 157 nm masks and for second materials to be combined with calcium fluoride for correction of chromatic aberrations. The optical characterization measurements near 157 nm include transmission and index of refraction to .5ppm, along with its dispersion and temperature dependence.

Detector measurements

Characterization of the spectral responsivity of a large number of photodiodes in the spectral range from 125 nm to 320 nm. Measurements of the stability of detectors towards excimer radiation at 193 nm and synchrotron radiation at 135 nm.

Optical characterization of CaF_2

High accuracy transmittance, reflectance and surface and bulk losses for calcium fluoride in the spectral range from 125 nm to 300 nm.

Publications

Burnett, J. H. and Gupta, R., Optical Materials and Detector Characterization for 193nm and 157nm Lithography, in *Future Fab International, 8th edition*, to be published by Technology Publishing, London, January 2000.

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Shaw, P. S., Lykke, K. R, Gupta, R., O'Brian, T. R., Arp, U., White, H. S., Lucatorto, T. B., Dehmer, J. L., and Parr, A. C., Ultraviolet radiometry with synchrotron radiation and cryogenic radiometry, Applied Optics, Vol. 38, No. 1, p. 18, (1999).

Shaw, P. S., Lykke, K. R., Gupta, R., Arp, U., Lucatorto, T. B., and Parr, A. C., The New UV Radiometry Facility at SURF, submitted to SRI Proceedings.

Deep Ultraviolet Laser Lithography for Semiconductor Photolithography

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Funding Sources:
NIST OMP/NSMP
NIST STRS
Other Agency

Project Goals

Provide support to the semiconductor manufacturing industry through the development of ultraviolet laser measurement methods and technology. Establish calibration services for laser power and energy meters and develop transfer standards for pulsed-laser measurements using DUV excimer lasers.

Customer Needs

Beginning with the first edition of the NTRS in 1992, the semiconductor industry has made an organized, concentrated effort to reduce the feature sizes of integrated circuits. As a result, there has been a continual shift towards shorter exposure wavelengths in the optical lithography process. Because of their inherent characteristics, DUV lasers, specifically KrF (24 nm), ArF (193 nm), and more recently F_2 (157-nm) excimer lasers, are the preferred sources for high-resolution lithography at this time. To meet the laser metrology needs of the optical lithography community, the NIST Optoelectronics Division has developed primary standards and associated measurement systems at 193 nm and 248 nm, and is in the process of developing standards for 157 nm.

In addition to existing DUV laser measurement services, there is increasing demand for laser dose, *i.e.*, energy density, measurements, where the detector samples a fraction of the total laser beam. Accurate laser dose measurements are important because small area detectors are widely used to monitor laser pulse energy density at the wafer plane of a lithographic tool. Accurate measurements of laser dose are especially crucial to the development of new mask and resist materials, since lower dose requirements lead to greater wafer throughput and also extend the lifetime of an exposure tool's optical components as well.

According to the 1999 SIA ITRS, optical lithography will be viable through the 90 nm generation of integrated circuits using 193 nm exposure tools, and may be extended to 70 nm using 157 nm exposure tools, page 154, Figure 23. NIST is participating in the SEMATECH and MIT Lincoln Laboratory collaboration project on DUV photolithography in an effort to provide needed critical data and measurement support as quickly as possible. One critical requirement that has been identified by both MIT Lincoln Laboratory and International SEMATECH is the availability of calibration services for 193-nm laser energy meters. This requires the development of a 193 nm primary standard, a calibration facility, and appropriate transfer standards to transfer calibrations to the industry customers. Furthermore, the SIA ITRS has identified the need for improved process control at the wafer plane. This requirement mandates the need for improved laser dose metrology which can only be accomplished through the development of primary standards and improved transfer standards that are both stable and accurate, as well as a calibration facility to provide the means to calibrate these transfer standards and customer-supplied laser detectors.

Technical Strategy

Presently, NIST provides 248 nm and 193 nm laser power and energy measurement services to the semiconductor community with approximately ± 1 - 2 % overall uncertainties. In addition, the 193-nm calibration turn around time is currently limited by the time required to purge the measurement system enclosure of oxygen. Because NIST is the only national laboratory in the world that supports DUV excimer laser measurements, it is important that the measurement uncertainties and turn around times be reduced. Furthermore, to address the emerging need of the next generation of optical lithography tools, it is essential that 157 nm measurement capability be developed to support the growing demands of the semiconductor industry. At the

present time, no standards exist for 157 nm excimer laser power and energy measurements.

MILESTONE: By 2001, develop primary standards and measurement services for DUV laser power and energy meters at 157-nm. Reduce the uncertainty of measurements at 248-nm and 193-nm, and improve turnaround time for calibrations supplied to customers.

We are currently developing new standards and calibration procedures for energy density measurements to provide improved measurement accuracy for the end user. One difficulty associated with dose calibrations is the angular response of the detector. Ideally, dose meters are calibrated using a parallel laser beam with a uniform energy density that overfills the detector surface. However, with the move toward variable numerical aperture lithographic tools, significant measurement errors can be introduced when extrapolating a value for laser dose with the assumption of a cosine function for the dose meter angular response. Measurements of dose meter angular response functions have recorded 40 % deviations from a cosine response function [Ref. Cromer, C. L. and Bridges, J. M., "NIST Characterization of I-Line Exposure Meters," SEMATECH Technology Transfer Document, No. 91040516A-ENG (1991)].

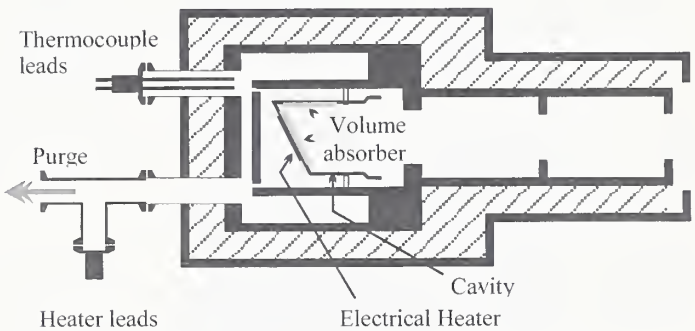
MILESTONE: By 2000, develop measurement capabilities for DUV energy density (dose) calibrations at NIST, and develop improved transfer standard dose meters to improve the accuracy of end user measurements.

At this time, birefringence measurements of optical materials, such as fused silica and calcium fluoride, are made at visible wavelengths. These visible wavelength measurements, which are used as specifications by tool suppliers, underestimate the birefringence that occurs in these materials when exposed to ultraviolet light. (Light of orthogonal polarizations propagates at different speeds in birefringent materials. Therefore, orthogonally-polarized light will travel different optical paths in birefringent material, thus introducing a phase difference between the two polarizations.) Birefringence in exposure masks is of great concern since phase variations in the source beam can translate into intensity variations at the wafer plane.

MILESTONE: By 2002, develop measurement methods and instrumentation for birefringence measurements of optical materials using DUV excimer lasers.

Accomplishments

- **193 nm excimer laser power and energy meter calibration services.** Completed development of a new DUV primary standard calorimeter for measurement of 193 nm excimer laser pulse energy with partial support from SEMATECH. Completed design, construction, and testing of an N_2-purged, beamsplitter-based, 193-nm excimer laser measurement system. Established a new service to calibrate customer power and energy meters for 193 nm excimer lasers with an uncertainty of . ± 1.5 %. (Collaboration with NIST Division 844 and MIT Lincoln Laboratories)



- **DUV Excimer laser beam attenuator.** Accurate measurements using DUV excimer lasers frequently require the adjustment of the laser energy and power in a stable and repeatable way. This cannot be accomplished easily with the laser discharge control system, since the laser becomes unstable near threshold. We have developed a novel multi-reflection attenuator for DUV excimer lasers which has improved stability over traditional attenuators that use bulk material absorption. This attenuator enables adjustment of the laser energy without disturbing other laser beam characteristics. (Collaboration with NIST Division 844 and MIT Lincoln Laboratories)

- **DUV excimer laser transmittance of optical materials.** Applications for 193 nm excimer lasers require accurate transmittance measurements of system components to assure performance and to meet design tolerances. Industry measurements of transmittance using both excimer lasers and traditional spectrophotometers have shown considerable disagreement (.5%). Therefore, we have developed a system to measure the transmittance of optical materials, *e.g.*, fused silica and calcium fluoride, using a 193-nm excimer laser. Measurements are performed in a nitrogen gas environment with an uncertainty of $< \pm$ 1%, and are available to customers as a special test. (Collaboration with NIST Division 844 and MIT Lincoln Laboratories)

FY Deliverables

16 calibrations performed for customers of 248 nm excimer laser power and energy meters. Established new power and energy calibration service at 193 nm, and developed a special test measurement service for transmittance of optical materials at 193 nm.

Publications

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Leonhardt, R.W., Calibration service for laser power and energy at 248-nm, NIST TN 1394: 1-34; Jan 98.

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Extreme Ultraviolet Lithography

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Funding Sources:
NIST OMP/NSMP

Project Goals

Provide leading-edge metrology for the development and characterization of optical components and detectors used in extreme ultraviolet lithography (EUVL).

Customer Needs

As the features and design rules of the components used in semiconductor chips continue to shrink, we approach the limit at which the diffraction of the DUV used for the lithography will prevent further reduction of the dimensions. Thus, within the next few years, the industry will need to identify a suitable "new generation lithography" (NGL) beyond the current DUV-based tools. A leading contender for the NGL is EUVL. In this country its development is being intensely pursued by the EUV-Limited Liability Corporation (EUV-LLC).

High resolution imaging with EUV radiation was not possible until the development of multilayer EUV mirrors in the early 80s. This development has spawned the relatively new field of EUV optics and its associated set of new metrological challenges. Among these are: 1) nanometer level optical figure measurement; 2) precise EUV reflectivity maps; 3) EUV dosimetry; and 3) EUV defect analysis.

Technical Strategy

Nanometer level optical figure measurement.

The approach to measurement of optical figure is to use phase measuring interferometry (PMI). Commercially available phase measuring interferometers (PMIs) can be extremely repeatable; an array of techniques, including some developed in this program, are now available for separation of part errors from the signature of the instrument - at least for some classes of surface. Such approaches have shown that they can provide measurement uncertainties of the order of 1 nm for flats and near flats.

For the measurement of aspheric optics (i.e., systematic deviations from a base sphere), such as those needed for EUVL, there are some basic limitations to the potential of the commercially available PMIs. Concepts for a system combining a PMI with high precision slideways have been developed and implemented (in collaboration with an industrial vendor) in a new measurement capability, known as the NIST X-ray Optics Calibration Interferometer (XCALIBIR). The goal is 0.25 nm rms uncertainty in measurement of aspheric optics up to 300 mm diameter with focal lengths up to 2 m. XCALIBIR -- designed to have the flexibility to measure flats, spherical, and aspheric optics – was installed at NIST in the fourth quarter of FY99; a calibration service will be developed based on this capability.

A critical part of the uncertainty evaluation of an ultra-precision interferometric measurement is a ray-trace evaluation of the test. The uncertainty in the radius of curvature of spherical optics in the test limits the accuracy of the models. Currently NIST offers no measurement service for radii. With some adaptation, XCALIBIR can be used to provide state-of-the-art radius of curvature measurements to address this problem.

Precise EUV reflectivity maps.

The present EUV Reflectometry Facility is a multipurpose beamline covering the 3 nm to 40 nm (400 eV to 30 eV) spectral range. Although dedicated to serving the EUV optics community by providing accurate measurements of multilayer mirror reflectivities, this versatile

beamline has been used for many other types of measurements since its commissioning in early 1993. Among the other measurements performed recently are grating efficiencies, photocathode conversion efficiencies, phosphor conversion efficiencies, film dosimetry, and determination of EUV optical constants though angle dependent reflectance measurements.

The EUV reflectometry beamline consists of a grazing incidence, varied line space grating monochromator and a sample chamber able to accommodate optics up to 10 cm in diameter. The downstream part of the beamline is shown schematically in Figure 1. Not shown are the collection mirror, which collects 3 mrad vertically by 20 mrad horizontally of the output from SURF III, the entrance slit, and a set of elemental filters to reject out-of-band radiation. Two interchangeable varied line spaced gratings enable scanning of the wavelength region from 3 nm to 40 nm, and an adjustable slit varies the resolving power from 200 to 2000. The wavelength is scanned by rotating and translating a plane mirror. The radiation is detected by an EUV sensitive photodiode. The combination of high throughput and sensitivity of the photodiode leads to a dynamic range of six orders of magnitude.

The current sample chamber is capable of accepting optics up to 10 cm in diameter and scanning an area of 25 mm x 50 mm through angles of 3 Eto 85 E from normal incidence. This chamber will be replaced by a large chamber that will allow us to generate a reflectivity map of the entire surface of large optics (up to 35 cm in diameter and 40 kg in mass) such as those expected to be used in such applications as EUV astronomy and lithography. We expect delivery of this chamber in the second half of FY 2000

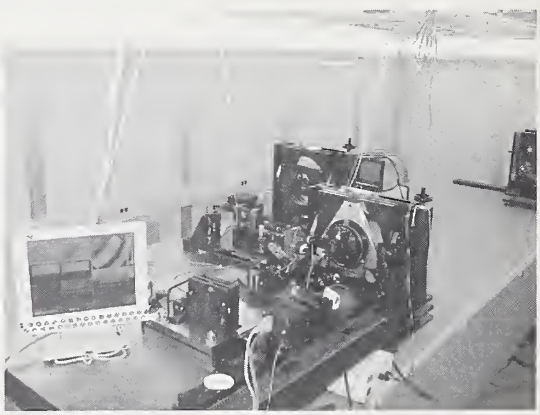
EUV dosimetry.

NIST is the primary source for the radiometric calibration of detectors from the infrared to the soft X-ray regions of the spectrum. Presently, we have a special project funded by the OMP for the calibration of DUV detectors. (See "Deep Ultraviolet Lithography for Semiconductor Photolithography.") NIST is presently expanding its capabilities to include the special requirements for the calibration of detectors of pulsed EUV radiation.

EUV defect analysis.

The mask and mask reticle present an especially difficult problem. The reticle, or mask blank, consists of a multilayer mirror similar to those used in the imaging system. However, where small imperfections that won't impact the overall performance of the mirrors may be tolerated, just one or two sub-μm imperfections in the reticle will cause zero yield of useful devices. The mask itself is an absorbing layer deposited by electron-beam lithography on the reticle. It must also be perfect on a sub-μm scale over the entire surface.

We propose to develop a hybrid photon-electron optical camera that can be used for high resolution imaging over a broad range of wavelengths. The camera converts an EUV image into an electron image using a thin-film transmission photocathode. This electron image is then magnified and focused using a custom designed electron lens column. The low-energy electron microscope is a mature technology and is predicted to have a magnification of over 1000X and resolution of about 20 nm. Both of these figures are appropriate for EUV mask inspection.



Accomplishments

- XCALIBIR is in the final phases of being commissioned.
- The present capability for producing reflectivity maps extends to samples that are 100 nm (4 inches) in diameter. We shall receive a new reflectometer this spring that will allow measurements on mirrors up to 350 nm (14 inches) in diameter, the largest

size expected for the optics in the EUVL steppers.

- NIST already is the primary source for the calibration of detectors of cw EUV radiation. This summer we shall have added a pulsed EUV source specially designed for the calibration of dosimeters of pulsed EUV.
- The EUV camera is operational at resolutions of order 150 nm. Refinements are underway to improve the resolution to the 20nm to 30 nm level. The EUV – LLC has agreed to provide a projector and samples of multilayer mask substrates with programmed defects for analysis.

Metrology for Simulation and Computer-Aided Design

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NIST OMP/NSMP
NIST STRS
Other Agency
Other NIST

Project Goals

The goal of the project is to facilitate the efficient and reliable application of semiconductor CAD tools by providing leadership for the development of an industry infrastructure for establishing model accuracy, developing methods for simulator model validation and benchmarking, developing metrology necessary for providing model data and model parameter extraction sequences, and developing models and techniques necessary for advanced device, process, package, and system simulation.

Test system used for IGBT parameter extraction and model validation.

Customer Needs

Efficient and reliable simulation methods are becoming more important as device structures and packages rapidly evolve. In addition, higher speed and higher power devices increase the importance of including the effects of packages in system performance simulation. However, advanced device electrical and thermal characterization procedures and validation of models used in computer-aided design tools have not kept pace with the application of the new device types and processes.

Several device technologies have evolved to an extent that conventional modeling and simulation capabilities are not suitable. For example, as CMOS devices are scaled to atomic dimensions, simulators must include quantum mechanical physics. The SRC/NIST/NSF Workshop on Nanoscale Transistors: Technology, Physics, and Simulation (Feb. 1999) identified quantum mechanical device simulation as an area required for device simulator progress.

Technical Strategy

NIST addresses these needs by developing the theoretical foundations, standards, model validation procedures, and associated experimental techniques for the measurement of device electrical and thermal characteristics, and package electrical and thermal characteristics. NIST is developing, with industry, accepted procedures for validating device models for circuit simulation. NIST is developing procedures for characterizing the thermal and electrical performance of micro-electronic packages that are compatible and useful for CAD of boards and systems.

Device and Process Simulation Benchmarking Accurate models and benchmarking procedures are becoming more important for device and process simulators. Current tasks include development of mobility, band gap, and intrinsic carrier concentration models for accurate simulation of compound semiconductor devices, and collaboration with the Scanning Capacitance Microscopy Project to validate process simulators for ultra-shallow junctions.

MILESTONE: By FY 2000, complete benchmarking of semiconductor device simulation tools that include quantum mechanical effects including: MEDICI, UTQuant, NCSU code, and NEMO.

Compact Package Electrical Interconnect Models - Interconnect structures are becoming a dominant factor in limiting the performance of modern computer, communication, and power systems. The Time-Domain Reflectometry TDR technique is being applied to characterize various multi-chip module and discrete packages interconnect systems.

MILESTONE: By FY 2001, develop a TDR test system with low source impedance (10 Ω), and characterize low-impedance interconnects used in microprocessor voltage regulator modules, advanced memory busses, and power electronic systems.

Package Thermal Metrology and Models - Accurate and timely simulation of system thermal performance requires new temperature measurement methods, new simulation methodologies, and validation procedures. Current tasks include the NIST electro-thermal network simulation methodology, including thermal network component models for semiconductor packages and heatsinks, and development of methodologies to validate the performance and accuracy of compact package thermal models.

Compact Device Electrical Models - Only recently has there been a significant effort in developing an infrastructure for validating the performance of compact models. An example of this activity is the NIST/IEEE Model Validation Working Group, founded in 1994 and now having over 200 members from 100 different technical organizations. For more information see http://ray.eeel.nist.gov/modval.html.

MILESTONE: By FY 2002, develop test system and models for SiC three terminal device.

Accomplishments

- Provided leadership in developing a national agenda for modeling and simulation. Hefner presented an invited talk entitled, "Model Verification, Validation, and Accreditation of Semiconductor Device CAD Systems," at the National Academy of Science, National Research Council Workshop on Modeling and Simulation Opportunities in Manufacturing, April 26-27, 1999. The talk described the methodology for model validation being applied by the NIST/IEEE Working Group on Model Validation. The objective of the workshop was to develop a prospectus for a study that will recommend a national research agenda to address shortcomings in current modeling and simulation capabilities and to develop enhanced opportunities for coupling modeling and simulation with manufacturing.
- Impact study published on NIST models. An assessment of the U.S. economic impacts of the NIST IGBT model is detailed in a recent study entitled NIST Planning Report 99-3: Benefit Analysis of IGBT Power Device Simulation, prepared by M. Gallaher and S. Martin, Research Triangle Institute Center for Economic Research (April 1999). The press release announcing this study appeared in the front page of the NIST web site, appeared in the NIST Update, and was highlighted in the NIST directors State-of-the-Institute (also in NIST Connections article entitled "NIST Measuring Up, Kammer Says"). The economic impact study quantified the direct impacts of the NIST IGBT modeling at $18M (30 times the cost of the NIST program) and the indirect benefits at $40 M/year largely due to energy savings.
- NIST interconnect metrology proves valuable for EMI simulation. Models obtained from recent interconnect metrology research at NIST enabled the simulation of the EMI performance of various power converter topologies, as described in two NIST publications. In recent years, EMI considerations have become increasingly important as Electro-Magnetic-Compatibility (EMC) regulations have become more stringent. The NIST metrology provides, for the first time, the capability to use simulation in the design of power converters with reduced EMI emissions.
- Developed IGBT model validation procedures and applied to component library. Developed circuits and measurement methods for validating IGBT models for soft-switching conditions, applied the methods to models provided in a software vendors component library, and published results. Enhancements were made to the Hefner IGBT model that is provided in commercial circuit simulators as a result of this validation work. The NIST IGBT model was then used to simulate IGBT soft-switching performance in two papers; one describing reduced EMI emissions for soft-switched inverters, and the other describing the difference in soft switching performance between different IGBT types.
- Developed High-Speed Semiconductor Device Transient Thermal Imaging System. The system provides the capability to

measure the transient temperature distributions on the surface of a silicon chip with 100 ns temporal, 15 :m spatial resolution. The system uses computer-control software with a graphical user interface for controlling the translation stages, digitizing oscilloscope, and device test fixture temperature controller. The system also required the development of algorithms for calibrating and extracting transient temperature waveform from an infrared microscope signal.

- Developed Capability to Characterize and Predict IGBT Dynamic Failures. The dynamic failure characteristics and avalanche-sustaining capability of various IGBT types, including new high-energy capable IGBTs, were measured using the unique NIST nondestructive failure tester and simulated using the NIST IGBT model. The measurements and simulations enabled the prediction of the mechanism resulting in High Avalanche Energy lGBTs and demonstrated the capability of the NIST IGBT model to predict the sustaining time and conditions for failure of both high-energy and conventional IGBT types.
- Developed Software Package IMPACT. The software consists of five programs, LINMSR, SATMSR, LFTMSR, BTAMSR, and CVMSR, that extract the 20 physical and structural parameters of the most recent version of the NIST IGBT model. The programs have a graphical user interface, use the IEEE 488 bus to control the measurement instruments and collect data, and use various algorithms for fitting the IGBT model equations to the data. The new software package will facilitate the development of IGBT component libraries and enable end users of the simulation software products to extract model parameters themselves.
- Plasma doping meeting organized by NIST-sponsored Ion Implant Users Group. Albers spearheaded the planning and organization of the First Joint Ion Implant Users Group / Plasma Doping Users Group Meeting held on Thursday, April 22, 1999 at the Peabody Marriott, Peabody, MA, USA. The primary topic for the meeting was Plasma Doping, which is an up-and-coming doping technology that will be providing the ultra-shallow junctions envisioned in the SIA ITRS.
- SRC/NIST/NSF Workshop Held at NIST. The Workshop, "Research Issues and Directions for Nanotransistors: Technology, Physics, and Simulation, " was attended by over 50 researchers from industry, academia, and government. The Workshop identified critical modeling and simulation issues, such as quantum effects, that must be solved if modeling and simulation is to have a significant impact on the development of future nano-transistors. Modeling and simulation can speed progress in the development of future transistors if the infrastructure and physics are in place to attack relevant problems.

FY Deliverables

Collaborations

SCM Project and Analytical Chemistry Division, metrology and benchmarking of simulators for ultra-shallow junctions (A. Hefner)

MEMS Project, compact modeling of MEMS devices from CIF files (A. Hefner)

Thin-Film Process Metrology Project and Gate Dielectric and Interconnect Reliability Project, benchmarking quantum-mechanical device simulation (A. Hefner)

Electricity Division, development of low-characteristic impedance time domain reflectometry (A. Hefner)

Analogy and IR, development of IGBT and thermal model component library (A. Hefner)

Analogy and POWERX, development of high power IGBT module component library (A. Hefner)

Harris Semiconductor, development of component models for Harris IGBTs (A. Hefner)

General Electric CRD, development of IGBT module parameter extraction tools (A. Hefner)

CREE, development of SiC MPS-diode electro-thermal model (A. Hefner)

Rockwell Science Center, development of SiC transistor models (A. Hefner)

University of Maryland, Reliability Physics Department, IGBT dynamic failure (A. Hefner)

Virginia Tech., electrical characterization of power module and system interconnects (A. Hefner)

NIST ITL, regression analyses of electron mobility model for p-type AlGaAs (H. Bennett)

Semiconductor Research Corporation (SRC), Blackburn assigned as SRC Director for Advanced Devices and Technology (D. Blackburn)

NIST Center for Building and Fire Research, Heat Flux Metrology Competence, modeling of conduction heat flux gauge calibration fixture (D. Blackburn)

Standards Committee Participation

EIA/SEMATECH Compact Model Council, FY 96-99
(A. Hefner)

IEEE Electron Devices Society, Standards Technical Committee, Chairman, FY 96-99 (A. Hefner)

Software

Copies of the RESPAC (NIST SP 400-91) and HOTPAC (NIST SP 400-96) software packages have been distributed
(J. Albers)

Copies of NIST IGBT Simulation Software INSTANT and Saber IGBT model template were distributed (A. Hefner)

External Recognition

J. Albers received, in April 1999, an award from Eaton and Varian, the two primary U.S. ion implanter manufacturers, citing, "In appreciation for your continued commitment and support to the East Coast Implant Users Group and the ion implant community. "

Publications

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Kopanski, J. J., Marchiando, J. F., Albers, J., and Rennex, B. B., Comparison of Measured and Modeled Scanning Capacitance Microscopy Images Across P-N Junctions, Proceedings of the 1998 International Conference on Characterization and Metrology for ULSI Technology, Gaithersburg, Maryland, March 23-27, 1998, pp. 725-729.

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Zhu, H., Hefner, Jr., A. R., and Lai, J., Characterization of Power Electronics System Interconnect Parasitics Using Time Domain Reflectometry, in IEEE Transactions on Power Electronics, p. 622, vol. 14, July 1999.

Zhu, H., Lai, J.-S., Tang, Y., Hefner, Jr., A. R., and Chen, C., Analysis of Conducted EMI Emissions from PWM Inverters Based on Empirical Models and Comparative Experiments, in Proceedings of 1999 Annual Power Electronics Specialist Conference, p. 861 (June 1999).

Nonlinear Device Characterization and Modeling

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Funding Sources:
NIST
Other Agency

Project Goals

Develop new and general methods of characterizing nonlinear devices and components used in digital wireless communications, and to transfer the methods to industrial research and development laboratories.

Measuring a PIM artifact

Customer Needs

Radio-Frequency measurements are applied extensively in the deployment of commercial wireless communication systems. They are crucial to all stages of system development, from physics-based device modeling, to circuit design and system performance characterization. NIST's RF and microwave measurement support recently expanded to include methods of verifying nonlinear network models and measurements and methods for supporting industrial standards development.

Technical Strategy

The Nonlinear Device Characterization Project is focusing on the verification of model- and measurement-based descriptions of active devices and circuits containing nonlinear elements. Traditional microwave circuit design has relied on the ability to cascade circuit elements through simple linear operations and transformations. When a RF circuit includes a nonlinear element, engineers lose the ability to predict circuit performance across operating environments or states. With the wireless revolution, many researchers have devoted their time to developing models of nonlinear devices that will work with existing computer-aided design (CAD) techniques. Others have worked on developing specialized and functional tests that show how nonlinear behavior might effect system performance. Presently, there is a critical need for fundamental RF measurement techniques to verify and validate models and specialized tests. Contributions in this area will significantly improve design-cycle efficiency and trade between manufacturers.

The project's near-term goal is to establish a calibrated Nonlinear Network Measurement System (NNMS) at NIST with verifiable measurement uncertainty. The system will first be used to verify sample circuits developed at NIST and to predict functional test results based on the acquired waveform data. A custom instrument has been ordered and much research is under way to develop accurate calibration and measurement techniques for this system. Particularly, the Nonlinear Device Characterization Project is investigating the validity and measurement uncertainty of the Nose-to-Nose calibration, the only known method of measuring total phase delay of signals with bandwidth of 50 GHz.

***MILESTONE** By 2000, validate the Nose-to-Nose calibration. By 2001, verifiy the operation of a nonlinear network measurement system and implement advanced calibration methods.*

The Nonlinear Network Measurement System (NNMS) will be applied first to canonical active circuits to compare general measurements with predictions made by commercial CAD simulators. Secondly, the measurement system will be applied to verify artificial neural network (ANN) models for sample class-E amplifier

circuits being developed in cooperation with the University of Colorado. NNMS data will be used to train the ANN model, to verify circuit and model operation, and to validate a possible circuit optimization approach.

MILESTONE: By 2002, quantify uncertainty in commercial CAD simulator predictions for canonical circuits; develop and verify ANN models for example class-E amplifier circuits.

NIST is also conducting research into passive sources of nonlinearity found in wireless communications base stations. Key industry representatives have requested NISTs participation in passive intermodulation measurements. The Nonlinear Device Characterization Project responded by establishing relationships with a working group of the International Electrotechnical Commission that is developing PIM standards for connectors and cable assembly manufacturers. From this interaction, the project designed and conducted the first phase of a PIM measurement intercomparison. The study shows the level of agreement achieved by the participants, but does not show the impact of a given PIM level on system performance. The latter has become important in directing future NIST activities.

MILESTONE: By 2001, correlate PIM with system performance; conclude 2nd phase PIM intercomparison study.

Time-domain measurements form an interesting alternative to continuous wave nonlinear device measurements. Presently, NIST is investigating full vector correction of a time-domain network analyzer system. These time-domain methods have been applied to linear passive networks up to 20 GHz, but they can be extended to enable broadband instrumentation for the mm-wave region.

MILESTONE: By 2001, Add multiline TRL calibrations to TDNACal; complete two-port error model.

Accomplishments

- In response to requests by U.S. industry and members of the International Electrotechnical Commission (IEC), members of the Nonlinear Device Characterization Project conducted the first phase of the Passive Intermodulation Measurement Intercomparison for the U.S. Wireless Industry. While the study shows reasonable standard deviations about the expected mean values for most of the data sets, it reveals significant discrepancies reported by some participants and large standard deviations in other cases. This study is already enabling these companies to improve their PIM measurement capabilities.
- Through a collaborative effort, members of the RF Electronics and RF Fields Groups provided US West with the means to measure passive intermodulation distortion in base-station antennas. This work made use of the new anechoic chamber and new measurement techniques under development at NIST. NIST provided support and advice to US West engineers throughout the measurements. In addition, the collaboration allowed NIST to conduct PIM measurement experiments for the development of a new de-embedding technique. US West found the data collected in the anechoic chamber to be superior to data collected from their previous open range measurements.
- Developed a complete Open-Short-Load-Thru (OSLT) calibration for the NIST TDNACal software that implements equivalent circuit model descriptions. This new calibration is a significant enhancement to TDNACal, and for the first time, allows NIST to study measurement uncertainty in OSLT calibrations that make use of the equivalent-circuit model parameters.
- Collaborated with the Intel Technical CAD (TCAD) Division to measure the behavior of high-speed digital transistors (that is, MOSFETs) and to extract accurate device parameters. After much effort and several inter-laboratory visits, the first phase of the project has culminated in great success. The key technological hurdles were the measurement of three-port devices when the three ports are connected in different metalization layers, and the high RF losses encountered in commercial CMOS technology. NIST personnel designed two sets of calibration standards for the three-port devices. Intel fabricated three generations of test wafers and worked with NIST in verifying the calibrations. This activity also relied on new software developed by the High-Speed Microelectronics Project to remove contact-pad effects. The new approach is being used by TCAD engineers to quantify device behavior with a much higher degree of accuracy.

- Characterized the accuracy of several proposed calibration techniques for microwave vector network analyzers (VNA). Project staff discovered significant errors in the proposed methods and introduced a new robust SOLT Calibration method that offers demonstrably improved accuracy in four-sampler VNA measurements

At-Speed Test of Digital Integrated Circuits

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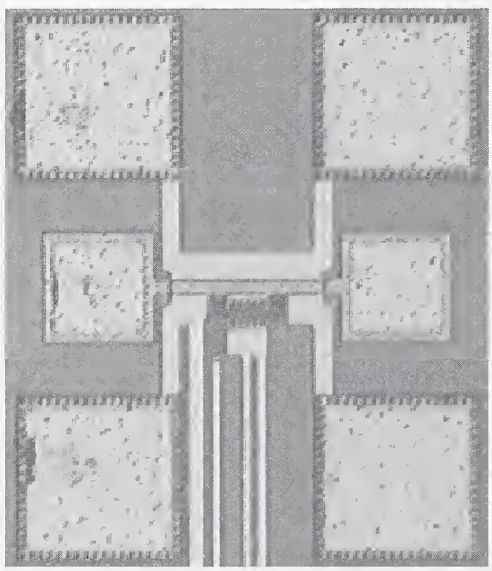
NIST OMP/NSMP

Project Goals

Develop and demonstrate metrology for the at-speed test of digital integrated circuits. The program will resolve the essential metrology issues of at-speed digital integrated circuit test. It will apply its results to AFMs modified to precisely position field probes above the surface of the integrated circuit and push the current on-chip sampling technologies now being explored by the industry.



Customer Needs

The semiconductor industry needs accurate metrology for the at-speed test of digital integrated circuits ("Difficult Challenges," page 11, 1999 SIA ITRS. Transional IC contact probing technology requires large contact pads incompatible with the operation and economic constraints of modern IC designs. Alternative probing approaches use non-contact probes, the intermittent-contact mode of the scanning capacitance microscope, electron beams, optical beams, or on-chip samplers that respond to either electric or magnetic fields near transmission lines in the circuits. AFM appears to be one of the most promising in the long term with prospects for 50 nm resolution and voltage sensitivities below 1 mV. However, the uncalibrated field measurements performed by these systems are a far cry from the precise measurements of voltages and currents required for electrical design.

Solving the critical at-speed test calibration issues will add enormous value to the probing systems currently being used or developed for high-performance digital integrated circuits. Implementing the methods on atomic-force microscopes, which we have already proven capable of performing these tests, will help speed the development and implementation of these new measurement tools, and so create a new paradigm for the at-speed test of high-speed digital integrated circuits.

Technical Strategy

We will develop calibration artifacts with precisely known high-frequency voltages and circuits suitable for calibrating field probes and samplers of all types. We will focus on fundamental calibration issues: transforming the response of the probes to the electric and magnetic fields above the integrated circuit into accurate voltages and currents inside the circuit. The calibration artifacts will take the form of custom integrated circuits with special test structures evaluated by NIST.

We will first apply the calibration procedures to miniature AFM probes suspended on custom cantilevers designed for high frequency measurements. We will test both the intermittent-contact mode of the scanning capacitance microscope and noncontact probes of our own design. We will follow up with a round robin, and will use the results to help other groups to develop calibration approaches. We will also investigate the application of the calibration artifacts to the on-chip samplers now being pursued by a number of large semiconductor manufactures, including Intel, Motorola, and IBM.

After verifying the calibration approaches with sinusoidal signals, we will develop a waveform measurement capability on special test structures, and eventually on silicon. We will use this capability to develop pulsed versions for calibrating time-domain measurement systems.

MILESTONE: By October 2000, develop 10 GHz sinusoidal voltage standard and test with the intermittent-contact mode of the scanning capacitance microscope, noncontacting AFMs, and/or e-beam system.

MILESTONE: By October 2001, demonstrate calibrated on-wafer waveform measurement.

MILESTONE: By October 2002, design and layout pulsed version of voltage source with built-in on-chip sampler. Design custom noncontacting probes for AFM test station.

Accomplishments

- We have designed and tested a prototype sinusoidal waveform standard.

FY Deliverables

We will develop sinusoidal and digital waveform standards. We will disseminate our methods through industry presentations and conference and journal publications.

Publications

Williams, D.F., and Walker, D. K., 0.1-10 GHz CMOS Voltage Standard, IEEE Workshop on Signal Propagation on Interconnects, Titisee-Neustadt, Germany, May 19-21, 1999.

Measurements for Complex Electronic Systems

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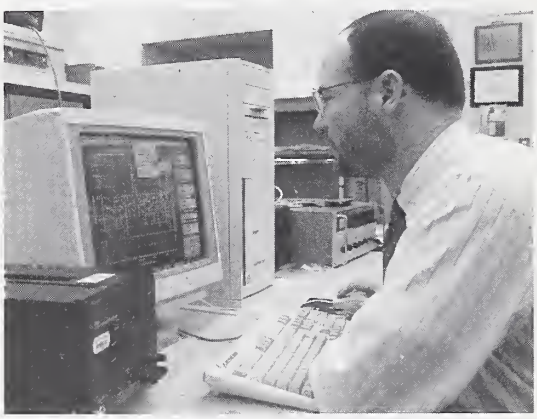
Funding Sources:
NIST

Project Goals

To develop and disseminate methods and techniques for optimum testing scenarios by using new or improved modeling and test procedures, estimating confidence levels and test coverage, and extending this methodology to address software-embedded systems.

Customer Needs



The U.S. test equipment industry is maintaining its world position through the development and deployment of increasingly accurate, easier-to-use automatic test systems that can also achieve high throughput rates. Both the manufacturers and users of such systems often need to prove their productivity in a highly competitive environment. Optimizing the testing procedures and reducing the test time required are goals beneficial to realizing the return on investment for expensive automatic test systems. Hence, there is an urgent need for better modeling methods and testing algorithms that can reduce the number of test points while maintaining a comprehensive test coverage. With the advent of embedded firmware in not only digital but also mixed-signal devices and instruments, the task of accounting for pernicious nonlinear, time-variant interactions between the hardware and software becomes more difficult (in an efficient, yet comprehensive, testing strategy).

Technical Strategy

Expansion of the present NIST expertise in modeling and testing complex electronic systems requires the investigation and application of statistical analysis methods to ill-posed problems. Appropriate inverse transformations may be required to "de-embed" the effects of firmware, along with modeling and accounting for time dependencies. Improved methods are needed to efficiently test nonlinear behavior.

As an example of a software-embedded instrument, nonrandom quantization effects have been observed in the time-base of the NIST-developed wideband sampling voltmeter. This phenomenon has been the source of inexplicably large measurement errors in the performance of the voltmeter at certain input signal frequencies. Research investigations have led to the development of a new algorithm for correcting the cumulative timing errors in the voltmeter, which has reduced the measurement uncertainties. Further study of nonrandom effects in sampling systems may provide a more generic solution to correcting this source of error in the measurement data collected by signal sampling devices and virtual instruments.

MILESTONE: By 2000, complete the study of nonrandom quantization effects in sampling systems and report these results in conference and archival publications.

The High-dimensional Empirical Linear Prediction (HELP) testing approach developed at NIST has generated considerable industry interest since it provides fewer test points needed to predict global behavior. Recent investigations into the use of artificial neural networks have shown promise of achieving efficient models for handling nonlinear dependencies. Of particular interest is the employment of so-called constructive neural networks, which permit the use of projection pursuit to reduce data dimensionality.

MILESTONE: By 2001, develop a neural network-based approach that can realize a significant improvement to the present HELP testing strategy for modeling the behavior of instruments.

The ability to make engineering changes quickly in the design of a complex electronic product is necessary to meet the demands of the marketplace. To achieve these changes by simply modifying the embedded software used in

the product is very cost effective. However, such changes are likely to change the model that has been developed to predict the performance of the product and, thus, its testing strategy.

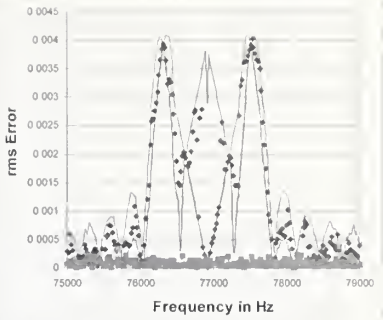
MILESTONE: By 2002, develop the means for an adaptive modeling approach that can be incorporated into the present HELP testing strategy, which can be applied to changes in product design.

The ability to separate the effects of embedded software from the hardware-dependent effects on the performance of an electronic product or device can greatly simplify its testing. An approach using a forward transformation has been tried with some success for predicting the parametric yield of complex mixed-signal devices. This kind of separation of effects is a difficult problem and necessitates a unique inverse relationship that often does not exist, e.g., saturation, hysteresis, and slew limiting conditions where there is not a one-for-one relationship between the input and output variables. However, if this is not the case, then the inverse transformations required to de-embed software would be very beneficial.

MILESTONE: By 2003, realize a new method for inversely transforming the effects of embedded software from those of the hardware in predicting the performance of a relatively simple mixed-signal device.

Accomplishments

- The "High-Dimensional Empirical Linear Prediction (HELP) Toolbox User's Guide, Version 2.2" was published and distributed as NIST Technical Note 1428. The HELP Toolbox allows test engineers to formulate abbreviated test plans that are economical to execute but still yield accurate measures of the overall performance of electronic devices and instruments. Products that can benefit from this approach range from multi-range precision instruments to programmable filters to integrated circuit analog-to-digital (A/D) and digital-to-analog (D/A) converters. Copies of Tech Note 1428 have been requested by Hewlett Packard, Sandia National Labs, and Signal Processing Technologies, Inc., among others.
- The timebase quantization errors for the wideband sampling voltmeter were modeled. The error data shows an unusual statistical distribution with long "tails." An algorithm was developed for minimizing the cumulative errors that are generated in the timebase of the voltmeter. This algorithm has been implemented in the software of the voltmeter and has improved these timebase errors to below the noise level of the voltmeter (see accompanying graphic).
- Methods were investigated for modeling nonlinear behavior, as a way to further reduce the number of test points needed or as a better way to represent a device model. A software program has been developed for implementing an artificial neural network approach for nonlinear modeling. A projection pursuit technique has been implemented and shown to handle nonlinear second and third order terms very effectively.
- A nine member Executive Committee was convened at NIST to plan a Workshop on Software Embedded Systems Testing (WSEST) to be held on November 8-9, 1999 in Gaithersburg, MD. A preliminary schedule was prepared of technical presentations and panel discussions. A WSEST home page was established with links to the NIST web site and the workshop was advertised on several e-mail lists.



Reduction in the relative rms error of the wideband sampling voltmeter from 75 kHz to 79 kHz. Diamonds are the measured errors before and squares are the measured errors after applying the correction algorithm. Solid lines are the simulated errors prior to correction.

FY Deliverables

Collaborations

A grant was given to Cornell University for collaborative work with Prof. Gene Hwang on missing data analysis using an expectation maximization approach. This work also involves Hung-kung Liu in the Information Technology Laboratory at NIST.

Dong Liu, a Guest Student from Ohio University, is collaborating with G. N. Stenbakken on development of an algorithm to minimize cumulative errors in the timebase of the wideband sampling voltmeter. For modeling nonlinear system behavior a projection pursuit technique, by Prof. Fernaldo von Stuben at the State University of Campinas in Brazil, has been incorporated into NIST models.

The 1997 NIST Competence project funding received by this project is being coordinated through the Manufacturing Engineering Laboratory.

Standards Committee Participation

IEEE Computer Society standards committees on P1149 Standard Testability Bus, WG.04 Mixed Signal Test Bus, and P1500 Standard Testability Method for Embedded Core-based ICs: G. N. Stenbakken is a member of these various standards committees.

Publications

Koffman, A. D., Souders, T. M., Stenbakken, G. N. , and Engler, H., High-Dimensional Empirical Linear Prediction (HELP) Toolbox User's Guide, Version 2.2, NIST TN 1428, Natl. Inst. Stand. Technol. (U.S.), 28 pages (May 1999).

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Engler, H. , Souders, T. M., and Stenbakken, G. N. , Efficient Testing of Electronic Devices, Proc. of INTERFACE 97-Computing Science and Statistics, May 14-17, 1997, Houston, TX, 29, No. 1, pp. 592-596 (1998).

Stenbakken, G. N. and Deyst, J. P., Comparison of Time Base Nonlinearity Measurements Techniques, IEEE Trans. Instrum. Meas. Special Issue on Selected Papers IMTC'97, 47, No. 1, pp. 34-38 (Feb 1998).

Engineering Statistics Internet Handbook

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Funding Sources:
NIST STRS
Other Agency

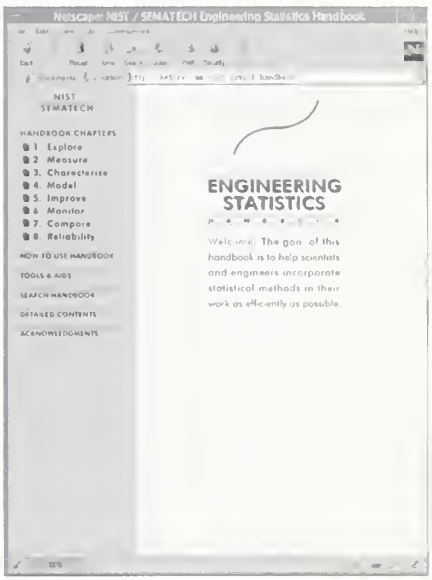
Project Goals

The goal of the NIST – SEMATECH Engineering Statistics Handbook Project is to produce a Handboook of Engineering Statistics for distribution on the Web. Supported by SEMATECH, AMD, Motorola, the NIST Information Technology Laboratory and the NIST Systems Integration for Manufacturing Applications (SIMA) program, the goal of the project is to produce an online resource that will be readily available and useful to engineers and scientists in industry, particularly the semiconductor manufacturing industry. This tool will enable them to incorporate statistical methods into their work more efficiently.

NIST Engineering Statistical Internet Handbook team (Mark Reeder, Alan Heckert, Will Guthrie and Carroll Croarkin) reviewing a page from the chapter on Reliability

Customer Needs

Semiconductor manufacturing requires extraordinary discipline in process control. For example, a typical integrated circuit process involves several hundred steps, including as many as thirty lithographic levels, which must be precisely aligned with respect to one another. Tight process control is essential for successful yielding of functional product. SEMATECH has recognized the importance of statistical process control in semiconductor manufacturing and has maintained expertise in this field since its inception in 1988. Two of the more difficult tasks facing widespread implementation is educating the users and making the tools easy to use.



Home page of Engineering Statisitical Internet Handbook

Technical Strategy

NIST and SEMATECH formed a collaboration under the umbrella Cooperative Research and Development Agreement (CRADA), combining the generalist expertise in engineering statistics at NIST with the semiconductor manufacturing expertise resident at SEMATECH.

Accomplishments

During FY 1999 we focused our efforts on creating chapter pages, assembling case studies with interactive computational capabilities, and integrating software with the handbook on multiple computer operating systems.

Early this year we released the handbook for beta testing at NIST and SEMATECH. As reviews for each chapter were completed, they were released to the public at the Web site

http://www.itl.nist.gov/div898/projects/handbook.html. Current plans are for full public release of web pages and CD ROM at the end of the year 2000

MILESTONE: By 2001, the handbook team will: i)enlist the services of a technical editor to integrate the eight chapters into a smoothly flowing document; ii) address issues of accessibility; and iii) produce generic scripts that enable vendors of statistical software to easily link their products to the Handbook.

Appendix A.

Acronyms and Abbreviations

AEM, Analytical Electron Microscopy

AEM/EDS, analytical electron microscopy/energy dispersive spectrometry

AFM, atomic force microscope

ALMC, Analytical Laboratory Managers Council

ALMWG, Analytical Lab Managers Working

AMAG, Advanced Metrology Advisory Group

ASME, American Society for Mechanical Engineers

ASTM, American Society for Testing and Materials

BCB, Benzo cyclo butenes

BESOI, bond and etch back silicon-on-insulator

BFRL, Building and Fire Research Labororatory

BGA, ball grid array

BIPM, Bureau International de Poids et Mesurs

BRDF, bidirectional reflectance distribution function

BST, Barium strontium titanate

CAD, computer-aided design

C-AFM, calibrated metrology AFM

CCD, charged coupled device

CD, critical dimension

CFM, contamination-free manufacturing

CINDAS, Center for information and Numerical Data Synthesis and Analysis

CIS, closed ion source

CMOS, complementary metal-oxide semiconductor

CMP, chemo-mechanical polishing

CRADA, Cooperative Research and Development Agreement

CRDS, cavity ring-down spectroscopy

CSTL, Chemical Science and Technology Laboratory

CV, Capacitance-Voltage

CVD, chemical vapor deposition

DIN, Deutsches Institut für Normung

DLH, diode laser hygrometer

DUV, deep ultraviolet

EBSD, electron backscattered diffraction

EELS, Electron Energy Loss Spectrometry

EEEL, Electronics and Electrical Engineering Laboratory

EGME, ethylene glycol methyl ether

EIA, Electronics Industry Association

EIA-JEDEC, Electronic Industries Association-Joint Electron Device Engineering Council

EM, electromigration

EMC, Electromagnetic compatibility

EMI, Electromagnetic interferences

EPMA, electron probe microanalysis

EQCM, Electronic Quartz Crystal Microbalance

FEASAM, field emission analytical scanning auger microprobe

FESEM, field emission SEM

FET, field emission transistor

FETD, finite element time domain

FIFEM, field ion field electron microscope

FTIR, Fourier transform infrared

GEC, Gaseous Electronics Conference

GIXPS, grazing incidence X-ray photoelectron spectroscopy

GOSI, goniometric optical scatter instrument

HDIS, high density interconnect structures

HRTEM, high resolution transmission electron microscopy

HSQ, hydrogen silsesquioxane

IC, integrated circuit

ICP, inductively coupled plasma

IEEE, Institute of Electrical and Electronics Engineers

IGBT, insulated gate bipolor transistor

IPC, Institute for Interconnecting and Packaging Electronic Circuits

IR, infrared

ISO, International Organization for Standardization

ITRS, International Roadmap for Semiconductors

IV, current-voltage

JEDEC, Joint Electron Device Engineering Council

LFPG, low frost-point humidity generator

LPRT, light-pipe radiation thermometer

MAP-EPMA, multiple accelerating potential electron probe microanalysis

MEL, Manufacturing Engineering Laboratory

MEMS, microelectromechanical systems

MFC, mass flow controller

MHPOSI, multidetector hemispherical polarized optical scatter instrument

MIT, Massachusetts Institute of Technology

MMIC, monolithic microwave integrated circuit

MOD, metal organic deposition

MOS, metal-oxide semiconductor

MOSIS, metal-oxide semiconductor implementation service

MPSA, sodium 3-mercapto-1 propanesulfonate

MSEL, Materials Science and Engineering Laboratory

NCMS, National Center for Manufacturing Sciences

NIST, National Institute of Standards and Technology

NMI, National Measurement Institute

NSMP, National Semiconductor Metrology Program

NTRM, NIST Traceable Reference Material

NTRS, National Technology Roadmap for Semiconductors

PBGA, plastic ball grid array

PEG, polyethylene glycol

PEVCD, plasma enhanced chemical vapor deposition

PL, Physics Laboratory

PPA, partial pressure analyzer

PPM, scanning proximal probe

PSL, polystyrene latex

PTB, Physikalisch-Technische Bundesanstalt

PWB, printed wiring board

RBS, Rutherford back-scattering

RF, radio frequency

RGA, residual gas analyzer

RM, reference material

RT, radiation thermometer

RTP, rapid thermal processing

SAM, scanning auger microprobe

SBIR, Small Business Innovation Research program

SCM, scanning capacitance microscope

SE, spectroscopic ellipsometry

SEM, scanning electron microscope

SEMATECH, SEmiconductor MANUfacturing TECHnology

SEMI, Semiconductor Equipment and Materials International

SEMI/SEMATECH, Semiconductor Equipment and International/ SEmiconductor MANUfacturing TECHnology

SERA, sequential electrochemical reduction analyses

Si, silicon

SIA, Semiconductor Industry Association

SIMS, secondary ion mass spectrometry

SiO_2, Silicon dioxide

SMWM, scanning microwave microscope

SOA, state-of-the-art

SOI, silicon-on-insulator

SOSI, scanning opitcal scatter instrument

SPM, scanning probe instruments

SRD, Standard Reference Data

SRM, Standard Reference Material

STM, scanning tunneling microscope

SURF, Synchrotron ultroviolet radiation facility

SV, stress voiding

TC, thermocouple

TCAD, technology computer aided design

TDDB, time-dependent dielectric breakdown

TDR, time domain reflectometry

TEM, transmission electron microscopy

TES, transition edge sensor

TF, tuning fork

TFTC, thin-film thermocouples

TIS, tool induced shift

TMA, thermomechanical analysis

TMA, thermomechanical analysis

TMFC, thermal mass flow controllers

UHV, ultra-high vacuum

UV, ultraviolet

VR-SFG, vibrationally resonant sum frequency generation

VUV, vacuum ultraviolet

WIS, wafer induced shift

XRD, X-ray diffraction

XRF, X-ray fluorescence

Appendix B.

NIST-Wide Matrix Managed Projects[✍]

National Semiconductor Metrology Program FY 2000

Building and Fire Research Laboratory (BFRL)

- Particle Measurements in Support of the Semiconductor Industry

Electronics and Electrical Engineering Laboratory (EEEL)

- Linewidth and Overlay Standards for Nanometer Metrology
- Scanning Probe Microscopy for Dopant Profiling
- Alternate Gate Dielectric Metrology for CMOS Technology
- Thin-Film Process Metrology
- Ultra-Thin Dielectric Reliability Metrology
- Test Structures for Mechanical Strain Characterization in IC Interconnects
- High-Resolution X-Ray Spectrometer for Chemical Analysis
- Interconnect Materials and Reliability Metrology (& MSEL)*
- FTIR Methodology for Quantifying Oxygen in Heavily Doped Silicon
- Plasma Process Measurements (also CSTL & PL)*
- Deep Ultraviolet Laser Metrology for Semiconductor Photolithography
- Metrology for Simulation and Computer-Aided Design
- Thin-Film Characterization from Transmission-line Measurement
- At-Speed Test of Digital Integrated Circuits
- Packaging Studies for Copper/Low-K Semiconductor Devices

Chemical Science and Technology Laboratory (CSTL)

- Thin-Film Profile Measurement Methods and Reference Materials
- Compositional Metrology for Next Generation Gate Stack Materials (& MSEL)*
- Chemical Characterization of Thin Films and Particle Contaminants
- Fundamental Process Control Metrology for Gases
- Low Concentration Humidity Standards
- Plasma Process Measurements (also EEEL & PL)*
- Metrology for Contamination-Free Manufacturing
- Temperature Sensing for Rapid Thermal Processing (& PL)*
- Thermophysical Property Data for Modeling CVD Processes and for the Calibration of Mass Flow Controllers

Manufacturing Engineering Laboratory (MEL)

- Nanometer-Scale Dimensional Metrology with SEM and Scanned Probe Techniques
- Nanometer-Scale Dimensional Metrology with Atomic Force Microscopy
- Scanning Electron Microscope Dimensional Metrology
- Linewidth Correlation
- Atom-Based Dimensional Metrology
- Optical Overlay and CD Metrology
- High-Accuracy Two-Dimensional Metrology
- Wafer and Chuck Flatness and Thickness

[✍] Listed by Operating Units (OUs) and by projects.

*Projects marked with asterisks are listed multiple times because they cut across multiple OUs.

Materials Science and Engineering Laboratory (MSEL)

- Compositional Metrology for Next Generation Gate Stack Materials (& CSTL)*
- E-Beam Moiré
- Interconnect Materials and Reliability Metrology (& EEEL)*
- Hygrothermal Expansion of Polymer Thin Films
- Thermal Conductivity of Mieroelectronie Structures
- Solderability Measurements for Microelectronics
- Measurements for Electrodeposited Copper Interconnects

Physics Lab (PL)

- X-ray Measurement Methods for Characterization of Thin Films and Their Mierostructures
- Plasma Process Measurements (also CSTL & EEEL)*
- Temperature Measurement for Rapid Thermal Processing (& CSTL)*
- Optical Seattering for Wafer Surface Metrology
- Radiometric Metrology for Deep Ultraviolet Lithography