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DISPLAY FORUM '97

Jointly sponsored by:

Information Technology Laboratory
NIST
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Video Electronics Standards
Association (VESA)

Editor:

John Roberts
NIST

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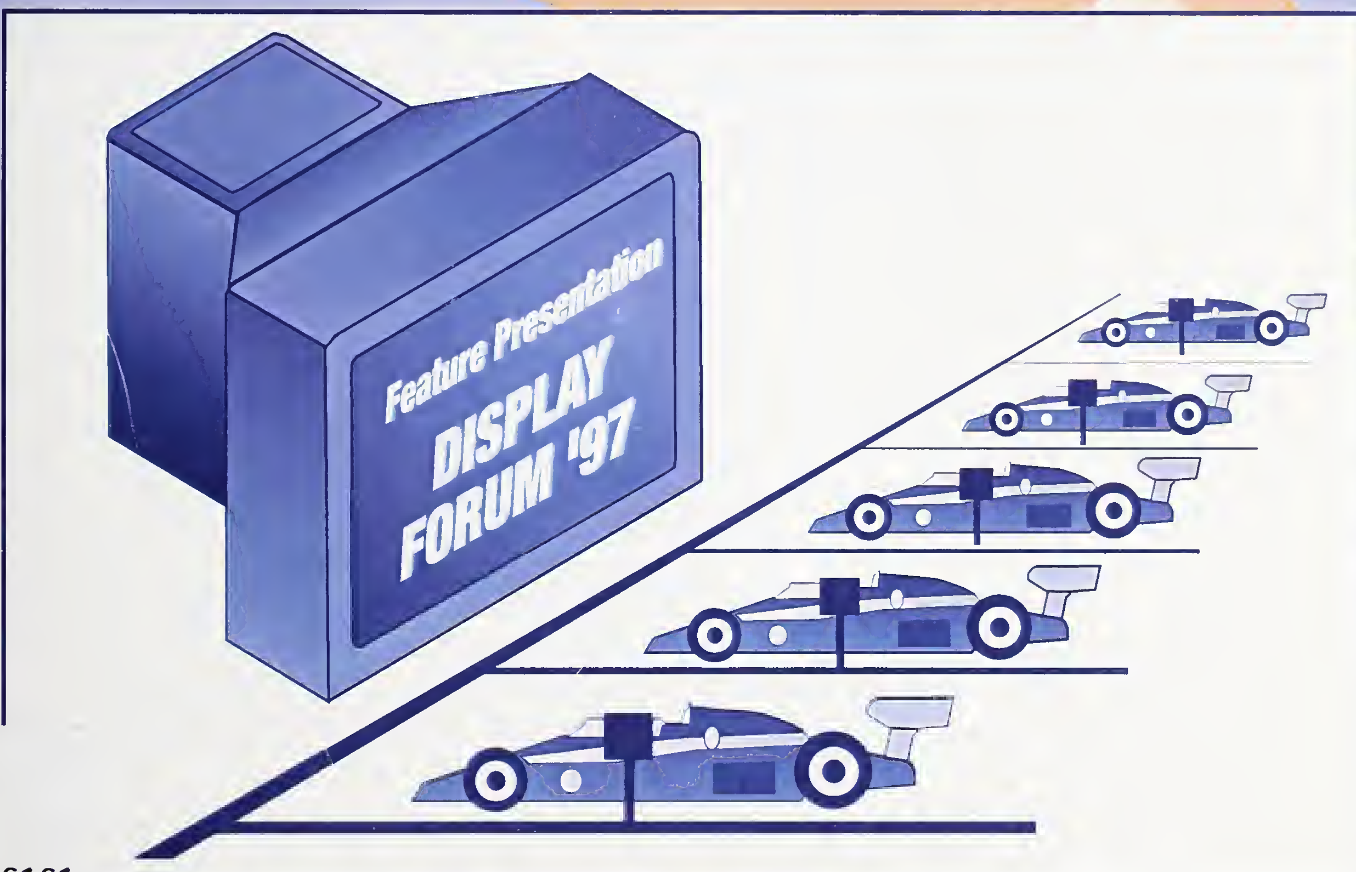

NIST Internal Report 6161

Display Forum '97
Workshop Proceedings - October 20, 1998
Gaithersburg Hilton, Gaithersburg, MD

John W. Roberts Editor

Information Technology Laboratory

National Institute of Standards and Technology
Gaithersburg, MD 20899

October 1997

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Display Forum '97

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I. Preface & Acknowledgements

The Display Forum '97 Workshop was conceived as a means of collecting and disseminating information on the display industry. Some of the topics have been discussed in industry standards meetings - the purpose of this workshop was to devote time to explore them outside the normal format of a standards meeting, and to invite participation from outside the traditional standards organizations. The topics of focus were:

- Today's technology and future trends
- Current standards and near-term developments
- Future needs (standards and technology)

The workshop was jointly hosted by the Information Technology Laboratory (ITL), part of the National Institute of Standards and Technology (NIST), and by the Video Electronics Standards Association (VESA). NIST has participated in the display standards effort at VESA since January, 1994. VESA, an international fast-track industry standards organization with a primary emphasis on display technology, was established in 1989, and was recently approved as a Publicly Acceptable Submitter (PAS) under the JTC100 ANSI establishment.

The morning session started with a keynote address and overviews of display research, development, and standardization at VESA and NIST. Part of the morning session was divided into two parallel tracks, representing the chief areas of interest of the majority of the participants:

- Track I was directed toward display interfaces and display interface standards, together with related technology issues.
- Track II covered the latest developments in the measurement of flat panel (and CRT) displays.

The morning session consisted of presentations by members of the display community. Tours of the display-related laboratories at NIST were made available at lunchtime, and in the evening. The afternoon session started with a keynote address on the current state of the technology and the market, followed by a report on results of a survey on display issues conducted for the workshop. A panel discussion followed, giving all the participants an opportunity to pose questions for discussion and for answers from a number of key industry experts. An open "brainstorming" session produced a set of conclusions and goals for the future. After closing comments, there was a reception, and company exhibitors demonstrated their products.

We would like to thank Carlos Grinspon of the Advanced Technology Program at NIST for his sponsorship of display-related projects within ITL that made the ITL participation in this workshop possible; the ITL management and its director, Dr. Shukri Wakid, for support of this work, the assistance of Ed Kelley in EEEL in organizing the measurement-related technical session and lab tours; the VESA Board of Directors and Executive Director for their support of the workshop, and the extensive efforts of organizers Molly Klupfell and Cathy Egan in planning, recruiting, and logistics. We would also like to thank the many speakers and panel members who contributed their time and knowledge to this workshop, and the participants who attended.

February 3, 1998

Dear Display Forum Attendee:

VESA STANDARDS was pleased to work with **NIST**, in hosting **Display Forum '97**, held on October 20, 1997. This unique forum, whose speakers and invited guests presented the latest information and developments in the display industry, gave us a chance to offer up-to-the-minute information to our members and other interested participants supporting growth and development of the best technology has to offer. We would like to sincerely thank everyone who participated, and the industry specialists who presented.

On the following pages you will find a proceedings package which contains presentations and summaries from the workshop. It is our sincere hope that the information presented will be utilized by many of you in the industry to support you technology efforts. Our sincere thanks to John Roberts of NIST, who edited these proceedings and summarized presentations for easier review.

If you have questions about the contents of any technical material presented, please contact John Roberts at NIST. His email address is roberts@cmr.ncsl.nist.gov (alias roberts@nist.gov).

For information about current and future standards that are being worked on at VESA STANDARDS, please contact Cathy Egan at VESA. Her email is cegan@vesa.org.

Again, we appreciate your interest and look forward to continuing our association throughout the coming year.

PJ Stegen
Executive Director
VESA STANDARDS

II. Summary

[Note: the presentations from the workshop are included in Sections V-VIII. This section is included for quick reference, and to cover items which were discussed but which did not appear on the presentation slides.]

Morning Session

The morning Keynote Speaker was Dr. Shukri Wakid, Director of the Information Technology Laboratory at NIST. His keynote address covered selected projects ITL is undertaking, and the importance of issues surrounding this work, such as the increasing importance of information networks and the Internet, the increasing value of software, ease of use of the user interface, and computer security. Embedded computing is considered to be a major area of growth, and along with immersive displays and wearable computers, will tax the capabilities of the display industry.

PJ Stegen, the Executive Director of VESA, emphasized the unique role of VESA as an open international trade organization developing standards on video displays and display interfaces. Ms. Stegen named the members of the Board of Directors, and explained the committee structure and the topics covered by the committees. She described the current standards and discussed standards soon to be released, and highlighted VESA's upcoming activities and events.

Mike Marentic of Hitachi, Chairman of VESA's Board of Directors and Flat Panel Display Interface Committee Chairman, gave a report on the FPDI Committee. FPDI was formed as a result of a NIST-hosted workshop similar in nature to Display Forum '97. The Committee has concentrated its efforts on the connector interface for integrated environments, such as notebook computers (and the internal interface to the panel in a desktop flat panel monitor). The FPDI-1 and FPDI-1B standards address existing designs, while FPDI-2 is directed toward future designs. In parallel with the connector interface work, the VESA Flat Panel Display Measurement (FPDM) Workgroup under Ed Kelley of NIST has enlisted the cooperation of key companies, of the National Information Display Laboratory (NIDL), and of other standards organizations such as EIAJ and ISO, to put together a proposed flat panel display measurement standard.

Ian Miller of IBM reported as Chair of the Plug and Display (P&D) Committee. This committee became active around the beginning of 1997, as a joint effort by the FPDI and Monitor Committees. The P&D standard addresses displays that have both analog and digital interfaces, and concentrates on external interfaces such as desktop monitors. The P&D standard is compatible with FPDI-2, and with the Monitor Committee's EVC standard. The Physical Mounting workgroup under Harry Sweere of Ergotron has developed a mounting specification for flat panel monitors.

Bob Myers of Hewlett-Packard, former Chair of the Monitor Committee, reported on monitor standards development activities. The VESA Monitor Committee has concentrated on monitors with primarily analog interface, but also addresses issues such as device ID and control that affect all types of displays. The charter and goals cover formats and timing, interface and control, and there has also been a standard on CRT display performance measurement. The Committee has long been known in industry for standards such as Display Data Channel (DDC) and Extended Display Identification Data (EDID), and for its many monitor timings - other VESA Monitor standards have also played an important role in the industry. Recent efforts include development of the Enhanced Video Connector (EVC), a high-performance analog video interface that also includes USB/1394, audio, and stereoscopic 3D among other features; a Generalized Timing Formula (GTF); the Monitor Control Command Set (MCCS); and a standard for stereoscopic display hardware. The Monitor Committee continues to sponsor "plug tests" (compatibility test meetings that include seminar briefings).

John Frederick of Compaq, Chair of the VESA PC Theatre Committee, presented a PC Theatre Committee report. The PC Theatre concept encompasses development of a home entertainment device which merges the functions of multimedia computing and television. Using the VESA standards plus IEEE 1394 and USB as resources, the Committee aims to develop a useful standard which will allow the manufacture of compliant computing and display components. Once the standard is in place, the Committee plans a series of plug tests to allow manufacturers to check compatibility.

Joel DiGirolamo of Lexmark reported on the Home Network Committee. The home network concept provides for digital automation of devices in the home, connected by a network. Devices such as compact disc player and PC require high speed communications, while other devices such as lamps and water heaters can get by with lower speed communications. Local clusters can use IEEE 1394, while "backbone" paths will require modified 1394.

John Roberts reported on the Display Interface and Technology research within the Information Technology Laboratory (ITL) at NIST. The charter of the project is to conduct laboratory research on display interfaces and advanced display technology, to support development of VESA standards, and to develop technology for measurement of electrical signals, timing, etc. This work complements the display programs of the EEEL and Physics Laboratories at NIST. Two specific projects were disclosed: the Resolution Mapping Algorithm project, which seeks to investigate the properties of remapped images on a flat panel or other fixed pixel display through the development and repeated modification of a remapping algorithm, and the Display Interface/Technology Testbed project, which is developing instrumentation to insert "noise" and other stimuli into the signal path of a display, and record the result - this technology can be replicated in industry, to determine display signal tolerance characteristics and enable uniform signal tolerance specifications.

Ed Kelley of the Electical and Electronics Engineering Laboratory (EEEL) at NIST reported on the metrology work of his Flat Panel Display Laboratory. The FPD Laboratory assists industry in creating standards for display measurements, and has extensive capability to develop and verify measurement techniques. Ed described the benefits of the proposed VESA Flat Panel Display Measurement standard - it gives clear descriptions, is metrologically based; it offers a "buffet" of measurements of various parameters, and of varying degrees of complexity and accuracy. FPDM emphasizes measurement techniques, not compliance requirements. Ed also noted the display work of the Optical Technology Division of the Physics Laboratory at NIST, which maintains national standards of radiometry, photometry, colorimetry, and other metrology.

Track I

Ian Miller of IBM, Chair of VESA's Plug and Display Committee, gave a detailed description of the features of the new Plug and Display standard, including the multiple features and the options available. Features presented include both high bandwidth analog and digital video interfaces, PanelLink(TM) low-voltage signals on the digital interface, DDC/EDID device ID, auto configuration, and hot plugging. Options include USB, IEEE

1394, and charge power. Two connector host receptacles are defined, one that supports both analog and digital signals (P&D-A/D), and one that supports only digital video interface (P&D-D). A monitor plug, compliant with the EVC analog video standard will plug into both the EVC receptacle and the P&D-D receptacle, but not the P&D-D receptacle. A P&D digital-only monitor plug will plug into a P&D-A/D or a P&D-D receptacle, but not an EVC receptacle. Together, EVC and P&D provide for hosts that can provide analog-only, digital-only, or both analog and digital video signals, and monitors with digital or analog video inputs (it is considered that there would be no purpose in building a monitor with both analog and digital video inputs). A monitor and a host that do not use compatible signals will not physically connect. Ian's presentation included a paper co-written with Shaun Kerigan of IBM, giving an additional technical description of P&D.

James Kim of Silicon Image presented a paper on the PanelLink(TM) technology used in VESA's Plug and Display and FPDI-2 standards. Within the standards, the transmission protocol is called Transition Minimized Differential Signaling (TMDS). PanelLink transmits digital data as differential low-voltage signals, with control signals encoded following a patented protocol, and a Digital Phase Lock Loop (DPLL) permits multiple bits of data to be transmitted per cycle of the transmission clock. The recommended implementation of the current drive benefits EMC, and low-voltage swing and impedance can be adjusted to meet specific needs. The paper described the capabilities of current and future devices, and explored potential future applications.

Larry Kopp of AMP, a VESA Board member, described the AMPSLIM 1.25mm connector, which was chosen as the connector for the VESA FPDI-2 standard. The connector is noted for an extremely low profile. Contacts are tin plated - for applications needing more than 30 cycles, a gold plated interface could be implemented. The receptacle can be used with discrete wires, twisted pair wires, or flexible printed circuits. The connector has been characterized up to 6 GHz. This is an open standard - other manufacturers can duplicate the connector interface.

John Frederick discussed the proposed VESA PC Theatre standard. The planned specification includes a high resolution computing device, connected to a progressively scanned large (television-size) display. Wireless input devices provide control. The P&D Standard connector is used to connect computing device and display. The device can operate in different modes, for both PC graphics and television mode functionality. The presentation included typical system configurations. The PC Theatre Committee has established a liaison with the Consumer Electronics Manufacturers' Association (CEMA) a related standards group, to insure agreement on a single realization.

Carlos Grinspon of the NIST Advanced Technology Program (ATP) gave an introduction to the ATP. This organization seeks to stimulate economic growth through cost-shared partnerships with industry, to develop high risk and enabling technologies. The target is technology areas that have high potential, but which also carry such a high risk that industry is unwilling to pursue them alone. ATP offers both general competitions (for all technologies and industries), and focused program competitions (directed toward one of the specific areas for which there has been enough interest to justify the formation of a focused program). ATP has provided significant funding in the areas of display and electronics, among others, and welcomes new proposals. Carlos said for more information, refer to the contacts in the presentation, including the web page at http://www.atp.nist.gov .

Joel DiGirolamo gave a presentation with extensive examples of how the Home Network concept would work. An overall access network reaches into a backbone network which spans an entire house with a high bandwidth, ~100 meter link to local digital clusters in multiple rooms. Television, telephony, and control of appliances are included. Unique wall outlets provide for connection between rooms. Important issues include bandwidth and security. Because of its widespread application, multiple industrial groups have become involved in this effort.

Dr. Bruce Gnade of the Defense Advanced Research Projects Agency described the DARPA High Definition Systems (HDS) program. DARPA is concerned with availability of advanced devices for purchase by the Department of Defense. Components can often be bought off the shelf, but in some cases there is a need for improved performance, readiness, and reliability. The HDS program considers one of the main issues to be how fast the user can assimilate data - the display being one of the critical elements in this process. In the past there had been greater emphasis on "dual-use" (civilian and military) applications - DARPA is now more oriented toward specific military applications. The emphasis of the program is on technology development, not manufacture. The immediate goal is to accelerate the development of flexible, rugged displays. Some of the technologies being explored are organic electroluminescent displays, reflective displays, self-assembled electronics, large plasma displays, organic LEDs, and non-traditional substrates such as plastic and flexible stainless steel. HDS would like to make use of commercial standard interfaces, such as P&D/FPDI-2. DARPA would like industry to be aware of the technologies it will require, as a possible influence for the future direction of technology development.

Track II

Steve Brown from the Optical Technology Division of the Physics Laboratory at NIST discussed the NIST Calibration Scheme for Colorimetry of Displays. The uncertainties in color measurement have led to a need for improved accuracy to facilitate applications requiring precise color reproduction. The objectives are to establish NIST calibration services for color measuring instruments for display colors, and to develop the needed instrumentation and methodologies for this service. The presentation described new measurement methods and evaluated their performance.

Hector Lara of Photo Research gave a presentation on Display Measurement Techniques and Standards. His paper discussed the need for reliable flat panel display measurements, then described the optics of three measurement approaches: Prichard Spot Optics, Fourier Optics, and Collimated Optics. The implications of the twelve parameters or "f-functions" recommended by the CIE (International Commission on Illumination) for evaluation of light measuring devices were considered, and the various bodies of experts in the field listed.

Mike Brill of the National Information Display Laboratory (NIDL) discussed a Procedure to Verify Digital Color Systems. The problem addressed was how to verify the degree of success in reproducing colors on a new device. The objective was to detect digital protocol errors, and to avoid confusing the results of these errors with other error sources. An approach is the use of adaptive color test patterns - find the digital inputs needed to produce specified colors on a standard video display unit (VDU), then feed these inputs to a test VDU and compare the results. The presentation described the mathematics needed for this procedure, and gave an example.

Mike Grote of NIDL reported on a flat panel measurement round robin that had been conducted using two NIDL notebook computers (one passive matrix, one active matrix) which were sent around to a number of different labs, where a suite of basic measurements were performed according to a specified procedure. Measurement equipment from a wide variety of manufacturers was used, and results were reported on a form of the type to be included in the VESA FPDM standard. Setup conditions were found to be crucial to the reproducibility of measurements. A mathematical analysis was applied to the results. With some exceptions, the degree of uniformity of measurements was greater than expected. A second round robin has been initiated.

Joe Lee Frank, Director of Operations at NIDL, gave a presentation on the need for FPD measurement standards. The end goal is that an end user can buy a display, turn it on, and the display will perform as desired. Results will depend on both display and systems standards. The FPDM standard is considered to be a major accomplishment in this area. Joe Lee predicted that projection displays will play an increasingly important role in the future. NIDL was formed seven years ago, to facilitate the use of displays by government users. NIDL foresees displays of the future with better image quality and more "intelligence", millions of pixels, stereo and video for some applications. Collaborative display systems for simultaneous use by multiple users will be meters to tens of meters across, have up to hundreds of millions of pixels, and be visible in ambient office lighting. Because of the demanding needs of human perception, and the sometimes life-and-death importance of correct image analysis, high quality displays will be essential, and good performance measurement will help to make sure they are available.

Paul Boynton of the EEEL at NIST described Interference Filter Testing for Color Measurement Accuracy. The idea is that interference filters can be used to evaluate light measuring devices (LMDs). Light from an integrating sphere serves as the source - it passes through a neutral density filter, then a diffuser, then the interference filter and an aperture, after which it is detected by the LMD. Proper alignment and linearity are important issues. Results of actual measurements were presented, and the sources of error were discussed.

George Jones of the EEEL at NIST discussed Display Reflection Characterization. The objective he stated is to evaluate the method of measuring undesirable reflection from the face of a display. With typical anti-reflection treatments, a bright light is typically reflected from a FPD as a fuzzy blob. The three-component model of reflection divides this reflection up into Lambertian (diffuse), specular (mirror-like), and haze (intermediate) components. Mathematical expressions can be used to describe each of these reflection components. The presentation described the measurement techniques used, and the results of actual measurements of reflection (Bidirectional Reflectance Distribution Function, or BRDF) as a function of angle. A specially prepared sample exhibits all three reflection components. A set of photographs showed the actual reflection.

Ed Kelley of the EEEL at NIST presented on Advantages of Using a Gloss-Black Cone Mask for Contrast and Black Measurements. The problem addressed is that an LMD is affected by light from parts of the screen that are not supposed to be viewed. To get around this problem, the Flat Panel Display Lab developed a technique of putting a hollow cone made of gloss black plastic (with the sides sloping at 45 degrees) between the screen and the LMD, to block or reflect away the light from unwanted areas of the screen. A second technique uses a black plastic strip laid directly onto the screen. Use of these techniques makes possible a great improvement in contrast measurements.

Afternoon Sessions

Mitch Halpern of SRI Consulting provided insight on the current status and the future of the display industry. The focus of the talk was on LCDs versus alternative display technologies, and whether alternative technologies can catch up to the entrenched position of LCDs. Mitch pointed out the fallacies that people often fall into when trying to predict the future of a particular technology.

Mark Kirstein of In-Stat reported on the results of a survey of attendees, showing what they believe the future holds for the display industry, and what issues they believe should be addressed. The survey responses include both the technical and the business issues facing the industry, as well as the roles of traditional computing and video / television.

[The Panel Discussion, Proposals for Future Development, and Closing Remarks are summarized in the following sections of the proceedings.]

III. Workshop Agenda

SPEAKER SCHEDULE FOR DISPLAY FORUM - FALL'97

Date:	Monday, October 20, 1997	
Location:	Gaithersburg Hilton, Gaithersburg, Maryland (near Washington D.C.)	
Schedule		
8:00 a.m-8:15 a.m.	**Keynote Speaker** **Dr. Shukri Wakid, director of Information Technology Lab, NIST** will deliver an informative address on "Emerging Trends in Information Technology".	
8:15 a.m.-8:45 a.m.	**VESA overview:** "Future Display Directions"	
	PJ Stegen	VESA Executive Director
	Mike Marentic	Hitachi, Flat Panel Display Interface Committee Chair
	Ian Miller	IBM, Plug & Display Committee Chair
	Bob Myers	Hewlett Packard, Monitor Committee
	John Frederick	Compaq, VESA PC Theatre Committee Chair
	Joel DiGiralamo	Lexmark, Intl., Home Network Chair
8:55 a.m.-9:05 a.m	**NIST overview**	
	Ed Kelley	NIST, Flat Panel Display Measurement
	John Roberts	NIST, Display Interface Laboratory
9:05 a.m	Break out into Parallel Tracks I & II	

9:15 a.m.-12:30 p.m.	**Track I: Display Interface Workshop**
1. Ian Miller, IBM	*"VESA Plug & Display: A New Video Interface Standard"*
2. James Kim, Silicon Image	*"VESA P&D TMDS (PanelLink Technology) and its Applications for Flat Panel Displays"*
3. Larry Kopp, AMP	*"AMPSLIM 1.25mm Connector for the VESA FPDI-2 Flat Panel Display Interconnect Standard"*
4. John Frederick, Compaq	*"PC Theatre Initiative—Open Industry Interconnect Standards for the Convergence of the TV and PC"*
5. Carlos Grinspon, NIST	*"Introduction to the Advanced Technology Program"*
6. Joel DiGirolamo, Lexmark International	*"1394 and the VESA Home Network"*
7. Bruce Gnade, DARPA	*"HDS Program and Future Vision"*

9:15 a.m. -12:30 p.m.	**Track II: Display Measurement Workshop**
1. S.W. Brown,NIST	*"NIST Calibration Scheme for Colorimetry of Displays"*
2. Hector Lara,Photo Research	*"Display Measurement Techniques and Standards"*
3. Mike H. Brill,NIDL	*"Procedure to Verify Digital Color Systems"*
4. Mike D. Grote,NIDL	*"Flat Panel Display Measurement Round Robin Results"*
5. J.L. Frank, NIDL	*"After FPD Measurement Standards"*
6. Paul A. Boynton,NIST	*"Interference Filter Testing for Color Measurement Accuracy"*
7. G.R. Jones,NIST	*"Display Reflection Characterization"*
8. Ed F. Kelley,NIST	*"Advantages of using a Gloss-Black Cone Mask for Contrast and Black Measurements"*

12:30 p.m.-1:30 p.m.	LUNCH NIST pre-registered lab tours during lunch
1:30 p.m.-1:45 p.m.	**Keynote Speaker** **Mr. Mitch Halpern, Manager of Business Intelligence Center, SRI Consulting** will speak on *"Shooting at a Moving Target – Alternative Display Technologies and LCD's."*

1:45 p.m.-2:15 p.m.	**In-Stat Report: Mark Kirstein, director of Research, Computer Market Services** *"Displays for Convergence"* Results of attendee surveys on future direction and requirements in the display field presented and discussed.
2:15 p.m.-3:45 p.m.	Panel discussion- *Critical Display Issues*
3:45 p.m.-4:45 p.m.	Display Technology Roadmap - *Proposals for Future Development*
4:45 p.m.-5:00 p.m.	Closing Remarks - *Technology Advancement and Future Vision*
5:00 p.m.-6:00 p.m.	Conference Adjourns, NIST pre-registered lab tours
5:30 p.m.-7:30 p.m.	Reception and company exhibits

IV. List of Attendees

DISPLAY FORUM '97
ATTENDEES

Name	Title	Company Name	Street Address	City	ST	ZIP CODE
Juan Pulido-No		3M				
Ken Wolfswinkel	Market Dev. Manager	3M	6801 Riverplace blvd (M/S A130-3N-17	Austin	TX	78726
Robert Moshrefzadeh	Research Specialist	3M	3M-Center-bldg.201-1C-18	Maplewood	MN	55144
Fred Meyer	Electronics Engineer	Air Force Research Lab	2210 8th St., bldg.146 Rm. 122	Wright AFB	OH	45433-7511
Lt. Tim Jackson	Lt.	Air Force Research Lab	WL/AAJD Old G 146 Rm122, 2210 8th st. :	Wright AFB	OH	45433-7511
Larry Kopp	Manager	Amp Inc.	P.O.Box 3608	Harrisburg	PA	17105-3608
Bill Bucklen	Product Line Manager	Analog Devices	7910 Triad Center Drive	Greensboro	NC	27409
Doug Bartow	Strategic Mrkt. Mgr.	Analog Devices	7910 Triad Center Drive	Greensboro	NC	27409
Gary Hendrickson	Staff Engineer	Analog Devices	7910 Triad Center Drive	Greensboro	NC	27409
Jiang Liu	Researcher	ARL US Army Research	2800 Powder Mill Rd.	Adelphi	MD	20783
Niles Burbank	Prod.Marketing Eng.	ATI Technology	33 Commerce Valley Drive East	Thornhill, Canada		L3T7N6
Alan Budreau	Engineer	AWACS	3 Eglin St.,	Hanscom AFB	MA	1731
Bill Russell	Manager	Canon Information	3188 Pullman Street	Costa Mesa	CA	92626
Steve Preston	Manager Graphics	Chips & Technology	2950 Zanker Rd.	San Jose	CA	95127
John Fredericks	Electrical Engineer	Compaq	20555 SH 249	Houston	TX	77070
Giang Dao	Sr. Software Engineer	Compaq Computers	22040 SH 249	Houston	TX	77070
Ronald Schulman	Senior Engineer	Compaq Computers	MC540101, 20555 SH 249	Houston	TX	77070
Wayne Mercer	Sr. Engineer	Computing Dev. Canada	P.O. Box 8508, M.S. 5324	Ottawa	ON	K1G 3M9
Ed Vambutas	Vice President R&D	Cyberchron	US RT 9, P.O. Box 160	Cold Spring	NY	10516
Bruce Gnade	Program Manager	DARPA	3701 N. Fairfax Drive	Arlington	VA	22203
Larry Lee	Sr. Product Manager	Diamond Multimedia	2880 Junction Avenue	San Jose	CA	95134
Mok Siu Cheung	President	Display Research Lab.	1/F, Hong Kong Industrial Tech. Centre	Kowloon Tong	HK	
George Leopold	Writer	EE Times	529 14th Street, NW, Suite 1170	Washington	DC	20045
Thierry Leroux	CEO	Eldim	4 Rue Alfred Kastler	CAEN	FR	
Pat Anthony	Director of Engineering	Electrohome Limited	809 Wellington St., N.	Kitchener, ON	CN	N2G4J6
Auri Raimzadeh	Digital Networks Editor	Envisioneering	615 Blossom Hill Road #4	Los Gatos	CA	95032
Richard Doherty	Editor in Chief	Envisioneering	3864 Bayberry Lane	Seaford	NY	11783
Ming Wu	Sales & Marketing	Hamamatsu Corp.	360 Foothill Road	Bridgewater	NI	8807
Bob Myers	Senior Engineer	Hewlett Packard	3404 E. Harmony Road	Ft. Collins	CO	80525
Mike Marentic	Manager	Hitachi America	1740 Technology Drive, Suite 420	San Jose	CA	95110
Ian Miller	Senior Project Eng.	IBM	Inverkip Road, Greenock, PA16 0AH	Scotland		
Jim Reger	Doctor	Independent Consultant	P.O. Box 5510, 100 Bay Drive	Key West	FL	33040
Mark Kirstein		INSTAT				
Don Chambers	NPPC Group Mgr.	JAE	142 Technology Dr., Suite 100	Irvine	CA	92618-2401

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ATTENDEES

Dr. Miltos Hatalis	Professor	Lehigh University	16A Memorial Drive East	Bethlehem	PA	18015
Joel DiGiralamo	Engineer	Lexmark International	740 New Circle Road, M/S C12/035-3	Lexington	KY	40511-1876
Dan Schinasi	Trade Show Manager	Minolta Corporation	101 Williams Drive	Ramsey	NJ	7446
Edgardo Rodriguez	Prod.Marketing Mgr.	Mitsubishi	1050 E Arques Avenue	Sunnyvale	CA	94086-4601
Gary Manchester	Strategic Prod. Mgr.	Molex	2222 Wellington Ct.	Lisle	Il	60532
Joe Nelligan	Product Manager	Molex	2222 Wellington Ct.	Lisle	Il	60532
Jeffrey W. Samilton	Electronics Technician	Naval Air Warfare Center	48110 Shaw Road, Unit 5, Bldg. 2187	Patuxent River	MD	20670-1906
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Paul Bishop	Electrical Engineer	Navy Coastal Systems	6701 W Highway 98	Panama City	FL	32407-7001
Robert Metz	Product Development	NEC	1250 N Arlington Heights Road	Itasca	IL	60443-1248
Stephen Butkus	Engineer	Newport News Shipbuildi	2711 S. Jefferson Davis Highway, #1100	Arlington	VA	22202
Dennis Bechis	Program Manager	NIDL	201 Washington Road	Princeton	NJ	8540
Joe Lee Frank	Director Operations	NIDL	P.O. Box 8619	Princeton	NJ	8543
Mike Grote	Proj. Leader	NIDL	P.O. Box 8619, 201 Washington Road	Princeton	NJ	08543-8619
Mike H. Brill	MTS	NIDL	CN5300	Princeton	NJ	8543
James Watson	Project Manager	NIMA	NIMA/TRN.M/S N-06,1200 1st st., SE	Washington	DC	20303
Carlos Grinspon	Program Manager	NIST	A415 Admin. Bldg.	Gaithersburg	MD	20899
David L. Staebler	Director	NIST	CN-5300	Princeton	NJ	08543-5300
Dr. Shukri Wakid	Director Info. Lab.	NIST	Bldg. 225, Rm. B263	Gaithersburg	MD	20899
Ed Kelley	Physicist	NIST	Bldg. 225, Rm. A53	Gaithersburg	MD	20899
Eung Gi Paek	Physicist	NIST	270 Clopper, bldg.225, Room #B255	Gaithersburg		
Fernando Podio	Electronics Engineer	NIST	270 Clopper, bldg.225, Room #B255	Gaithersburg	MD	20899
Fred Byers	Computer Specialist	NIST	270 Clopper, Bldg.225, Room B255	Gaithersburg	MD	20899
George R. Jones	Physicist	NIST	A108 Build. 225	Gaithersburg	MD	20899
John Roberts	Electrical Engineer	NIST	Bldg.225, Room B255	Gaithersburg	MD	20899
Paul A. Boynton	Electrical Engineer	NIST	Bldg. 220, Rm. A53	Gaithersburg	MD	20899
Steven W. Brown	Physicist	NIST	220/A320	Gaithersburg	MD	20899
Victor McCrary	Supv.Phycial Sci.	NIST	270 Clopper, Bldg.225, Room A255	Gaithersburg	MD	20899
Bill Grinnelwald	Sales Manager	Optical Coating	1405 Thunderbolt Way	Santa Rosa	CA	95407
Michael Phillips	Product Specialist	Panasonic Industrial Co.	2 Panasonic Way, M/S 7H-7	Secaucus	NJ	7094
Nick De Gaetano	Sr. Product Manager	Panasonic Industrial Co.	2 Panasonic Way, M/S 7H-7	Secaucus	NJ	7094
Hector Lara	Marketing Manager	Photo Research, Inc.	9330 Desoto Avenue	Chatsworth	CA	91311
J. Michael James	CEO	Portrait Displays, Inc.	6665 Owens Drive	Pleasanton	CA	94588
Joseph R. Visinki	Field Emission Display	Raytheon Electronic	1001 Boston Post Road, M/S 1-1-1174	Marlborough	MA	01752-3789
Donald Carlin	Head Luminescent	Sarnoff Corp./NIDL	CN5300	Princeton	NJ	8543
Dr. John L. Kulp, Jr.	Director- BSL	Sarnoff Corp./NIDL	201 Washington Road, CN5300	Princeton	NJ	08543-5300

DISPLAY FORUM '97

ATTENDEES

Leon Shapiro	Group Head	Sarnoff Corp./NIDL	CN-5300	Princeton	NJ	08543-5300
James Kim	Manager	Silicon Image	10131 Bubb Road	Cupertino	CA	95014-4976
John Nelson	Director	Silicon Image	10131 Bubb Road	Cupertino	CA	95014
Mitch Halpern	Program Manager	SRI Consulting	333 Ravenswood	Menlo Park	CA	94025
Bill Milford	Engineer	STB Systems	1651 N. Glenville, STE 210, P.O.Box 8509	Richardson	TX	75081
Toru Miyazaki	Research Scientist	Toshiba America Cons.	202 Carnegie Center, Suite 102	Princeton	NJ	8540
Chris Tutt	Sales	Vermont Electromagnetics	P.O. Box 940 - 7 Avenue D	Williston	VT	5495
Sam Miller	Mgr., New Product	ViewSonic	381 Brea Canyon Rd.	Walnut	CA	91789
Phillip A. Downen	Sr. Engineer	Westar Corporation	11520 St. Charles Rock Road	Bridgeton	MO	63044

V. Morning Session - Introductions

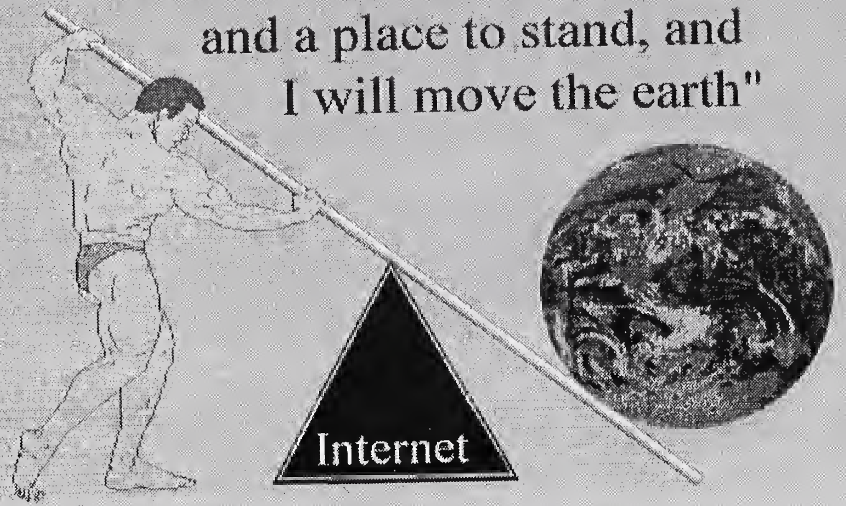
Future Directions of Information Networks

Dr. Shukri Wakid
Director, Information Technology Laboratory
NIST

Leveraging Cyberspace

Archimedes:

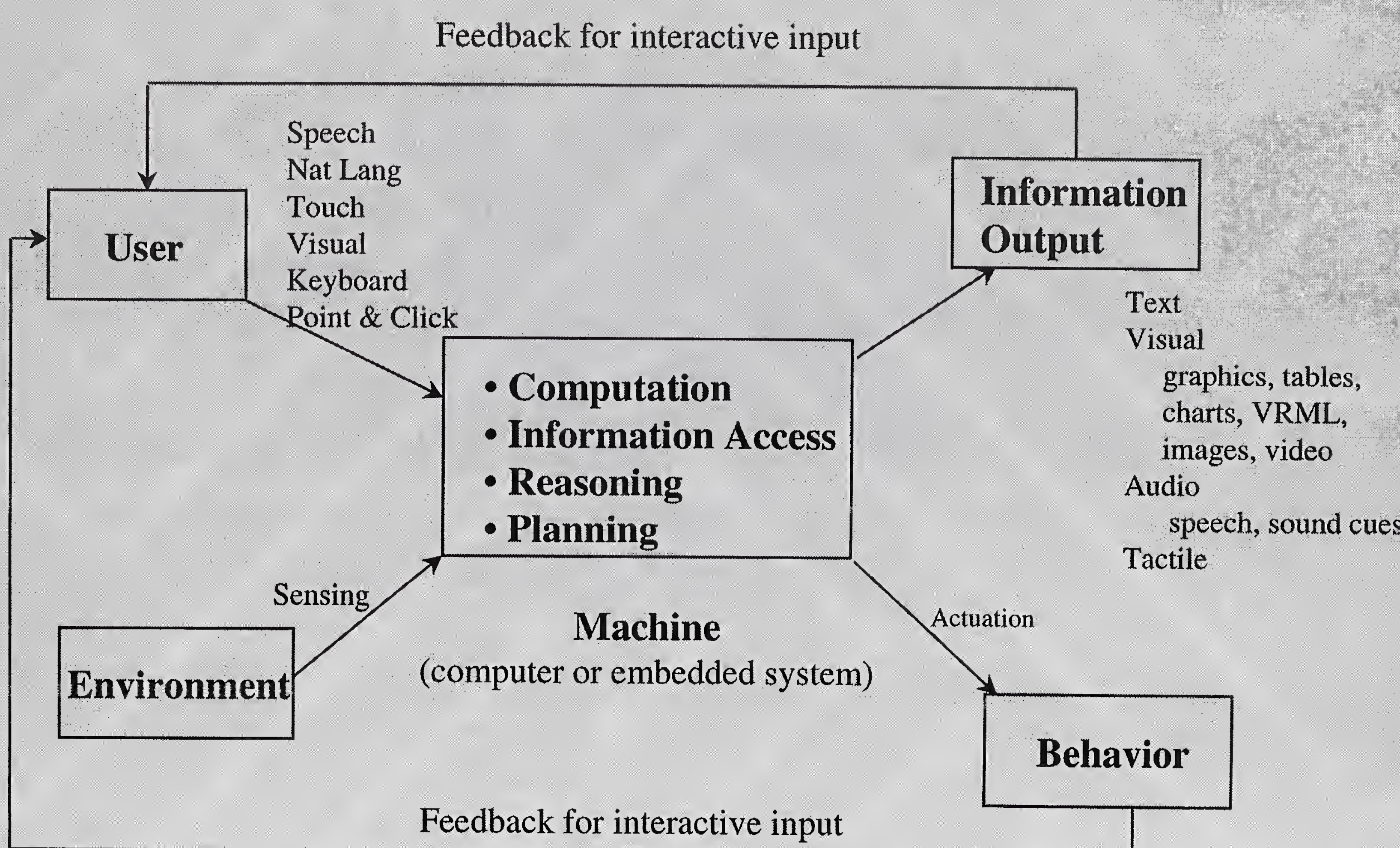
"Give me a lever long enough
and a place to stand, and
I will move the earth"



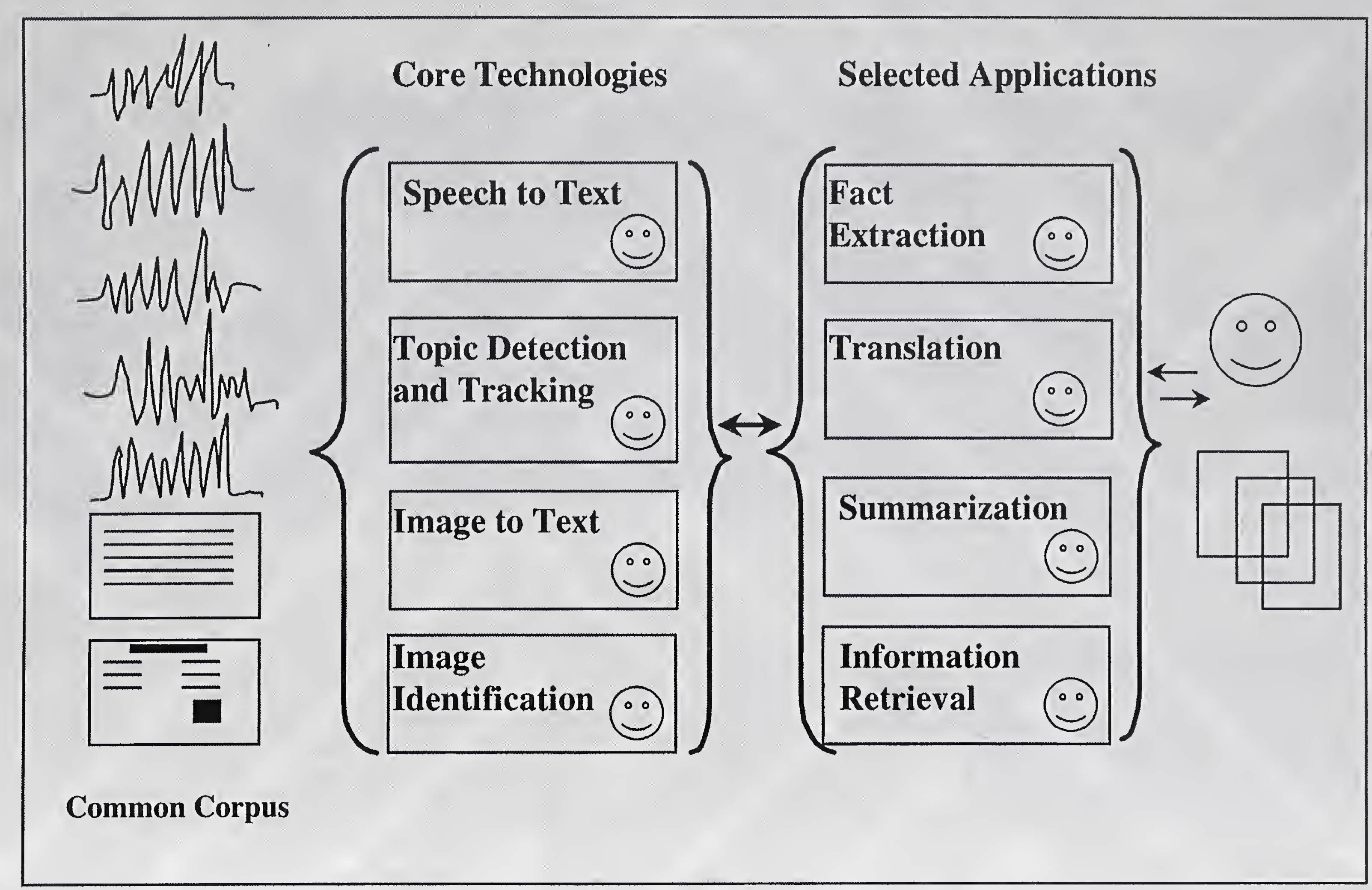
Emerging Trends

- Internet
  - IPv6, QOS, bundling of services, more "LANs"
  - Network centric versus desktop computing
  - Commerce of digital objects
- Future: Information Networks
  - Embedded computing (including diagnostics and management)
  - Adaptive networks
  - New Browsers, knowledge management, and human language technology
  - Computer Security

Computing Machines and their Inputs and Outputs



Interactive Human Language Technology



NIST

Information Technology Laboratory

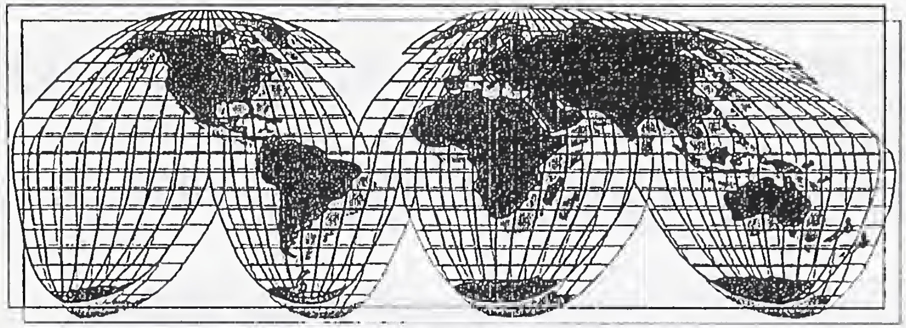
Telecommunications	Electric Power	Banking and Finance	Transportation, Oil & Gas Delivery and Storage, Emergency Services, Water	Continuity of Government Operations
Some DES cryptography	None	DES cryptography and proprietary	None	Federal Computer Incident Response Capability

OPPORTUNITIES RELEVANT CURRENT

Authentication and non-repudiation technology
Public key infrastructure
Internet/Intranet firewall technology
Role based access contr ol

Advanced standard cryptography and authentication
Secure operating systems
Intrusion detection
Criteria, assurance, and testing
Audit trails and traceability
Security management and incident response

VESA STANDARDS



Introduction

PJ Stegen

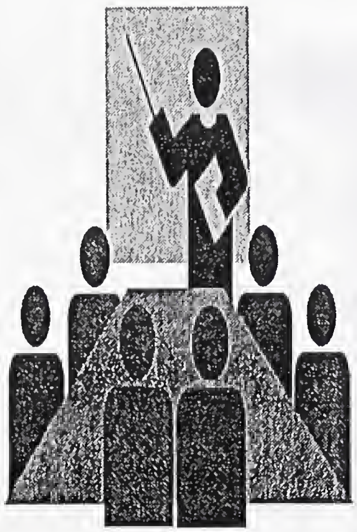
VESA Executive Director

PROGRAM

At the Starting Line...
VESA Drives Displays

- Welcome
- VESA - Who We Are
- VESA - What Makes Us Different
- Standards Update - "News You Can Use"
- What's Coming Up?

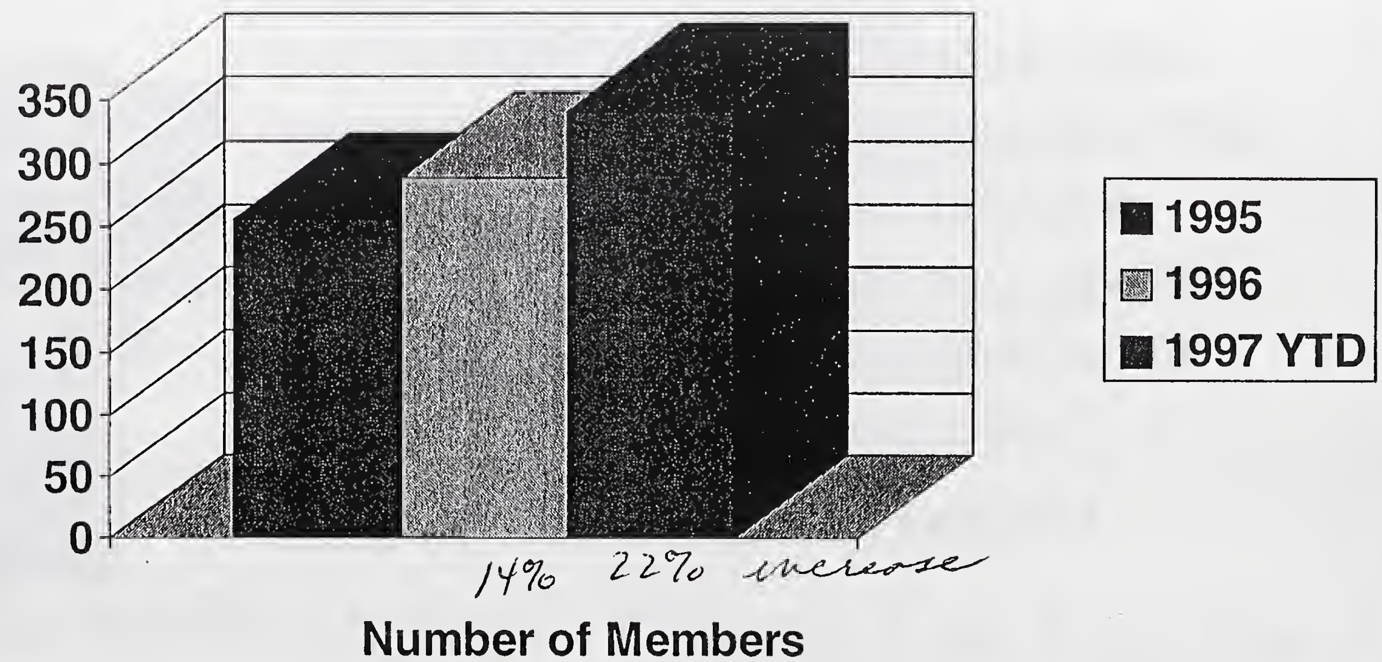
VESA - Who We Are



- VESA's Mission Statement:
- VESA is the first and *only* open, international organization developing, setting, promoting timely and relevant video display and display interface standards ensuring interoperability and encouraging innovation for the video industry.

WHO WE ARE

Membership



Display Forum '97 10/20/97

WHO WE ARE
VESA BOARD OF DIRECTORS

- Mike Marentic, Hitachi
  Chairman
- David Penley, Cirrus Logic, Inc.
  Vice Chairman
- Ian Miller, IBM
  Treasurer/Secretary

VESA BOARD OF DIRECTORS

- David Troup, AMD, *Director*
- Larry Kopp, AMP Incorporated, *Director*
- Dick Cappels, Apple Computers, *Director*
- Scott Vouri, Binar Graphics, *Director*
- Bob Myers, Hewlett-Packard, *Director*
- Hans Van Der Ven, Panasonic Industrial Co., *Director*

COMMITTEE OVERVIEW

- DISPLAY GROUP
  - Flat Panel Display Committee
    - FPDI-2
    - FPD Measurements
  - Monitor Committee
    - Discrete Monitor Timing
    - Display Data Channel
    - Enhanced Video Connector
    - Generalized Timing Formula
    - Monitor Control Command Set
    - Stereoscopic Display
  - Plug and Display Committee
    - VP&D, Version 1
    - Physical Mounting Interface
- INTERACTIVE MEDIA GROUP
  - Video Port Committee
  - Home Network Committee
    - Applications
    - Connector
    - Internetworking
    - Physical Layer
    - Wiring Infrastructure
  - PC Theater Committee
- SYSTEM GROUP
  - Software Committee
    - VBE/AF
    - VBE Core
    - VBE/FP

GII Operational Roundtable 7/23/97

VESA STANDARDS

COMMITTEES SUPPORTED BY 5-YEAR MEMBERS

ACER PERIPHERAL LABS
ADVANCED MICRO DEVICES
APPLE COMPUTER, INC.
ARTIST GRAPHICS
AST RESEARCH, INC.
ATI TECHNOLOGIES
AURAVISION CORPORATION
AVANCE LOGIC, INC.
BINAR GRAPHICS, INC.
BROOKTREE CORPORATION
CANON INFORMATION SYSTEMS, INC.
CAPETRONIC
CHIPS & TECHNOLOGIES, INC.
CHRONTEL, INC.
CIRRUS LOGIC, INC.
COMPAQ COMPUTER CORPORATION
CORNERSTONE IMAGING
CREATIVE LABS, INC.
CTX INTERNATIONAL, INC.
DAEWOO ELECTRONICS CO., LTD.
DELL COMPUTER CORPORATION
DIAMOND FLOWER INTERNATIONAL
DIAMOND MULTIMEDIA SYSTEMS, INC.
DIGITAL EQUIPMENT CORPORATION
EIZO NANAO TECHNOLOGIES
EPSON RESEARCH CENTER
EPSON RESEARCH & DEVELOPMENT CORP.
FUJITSU ICL COMPUTERS
GATEWAY 2000
HEWLETT-PACKARD
HITACHI/NSA
HITACHI AMERICA, LTD.
IBM CORPORATION
INTEL CORPORATION
LSI LOGIC COMPUTER PRODUCTS
MACRONIX INTERNATIONAL CO., LTD.
MAG INNOVISION
MATROX ELECTRONIC SYSTEMS, LTD.
MICRON ELECTRONICS INC.
MICROSOFT CORPORATION

VESA STANDARDS

5-YEAR MEMBERS (Continued)

MIRO COMPUTER PRODUCTS AG
MITSUBISHI ELECTRONICS AMERICA
NATIONAL SEMICONDUCTOR CORP.
NEC TECHNOLOGIES, INC.
NETWORK COMPUTING DEVICES
NOKIA DISPLAY PRODUCTS OY.
NUMBER NINE VISUAL TECHNOLOGY
OAK TECHNOLOGY, INC.
OKI ADVANCED PRODUCTS
OLIVETTI ADVANCED TECH
OPTI COMPUTER, INC.
PANASONIC
PHILIPS MONITORS
PHILIPS MULTIMEDIA PRODUCTS
PHOENIX TECHNOLOGIES, LTD.
RAMBUS, INC.
S3 INCORPORATED
SAMPO TECHNOLOGY
SAMSUNG INFORMATION SYSTEMS
SGS THOMSON
SONY ELECTRONICS, INC.
STB SYSTEMS, INC.
SUN MICROSYSTEMS/SUNSOFT
TATUNG COMPANY OF AMERICA, INC.
TEXAS INSTRUMENTS
TOSHIBA AMERICA INFORMATION SYSTEMS
TRIDENT MICROSYSTEMS
TRITECH MICROELECTRONICS INTL.
TSENG LABS, INC.
ULSI SYSTEMS
UNISYS CORPORATION
VIDEOLOGIC LIMITED
VLSI TECHNOLOGY INC.
WYSE TECHNOLOGY
YAMAHA CORPORATION OF AMERICA

COMMITTEES SUPPORTED BY 5-YEAR MEMBERS

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VESA STANDARDS

5-YEAR MEMBERS (Continued)

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PHOENIX TECHNOLOGIES, LTD.
RAMBUS, INC.
S3 INCORPORATED
SAMPO TECHNOLOGY

SAMSUNG INFORMATION SYSTEMS
SGS THOMSON
SONY ELECTRONICS, INC.
STB SYSTEMS, INC.
SUN MICROSYSTEMS/SUNSOFT
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TOSHIBA AMERICA INFORMATION SYSTEMS
TRIDENT MICROSYSTEMS
TRITECH MICROELECTRONICS INTL.
TSENG LABS, INC.
ULSI SYSTEMS
UNISYS CORPORATION
VIDEOLOGIC LIMITED
VLSI TECHNOLOGY INC.
WYSE TECHNOLOGY
YAMAHA CORPORATION OF AMERICA

What Makes Us Different

- Dynamic industry organization - open to all companies interested in video display standards development
- Develops more new standards faster than any other open industry organization.
- Membership is made up from among both the largest and most innovative computing & electronics companies worldwide.

STANDARDS UPDATE-
"NEWS YOU CAN USE"

- COMMITTEE ACTIVITIES

Standards Update
"News You Can Use"

IN THE RACE

- Display Data Channel 3.0 (DDC)
- Display Data Channel (DDC) 2bi 1.0
- Flat Panel Display Interface - 2
- Flat Panel Display Measurements 1.0

VESA STANDARDS

Standards Update
"News You Can Use"

IN THE RACE

- Monitor Control Command Set 1.0
- PC Theatre Initiative 1.0
- VESA Bios Extensions (VBE) Core 3.0
- VBE/Display Data Channel (DDC) 2.0
- VBE/Flat Panel (FP) 1.0

Standards Update
"News You Can Use"

NEARING THE FINISH LINE

- Extended Data Info Display 3.0 (EDID)
- Enhanced Video Connector (EVC) Physical Connector
- Physical Mounting Interface Proposal
- Video Interface Port

Standards Update
"News You Can Use"

GRAND PRIX WINNERS

- Connector & Signal Standard for Stereoscopic Display Hardware
- Enhanced Video Connector (EVC) Pinout & Signal
- Plug & Display

WHAT'S COMING UP

- Plug & Display (Ask for the Icon)
- COMDEX/Fall '97
  - PC Theatre Panel
  - VIP Recommended in Microsoft PC 98
- Member Newsletter
- Plug Tests for Monitor & Video Port
- Expanded World Wide Web Page

VESA STANDARDS

WHAT'S COMING UP

GRANDSTAND ACTIVITIES

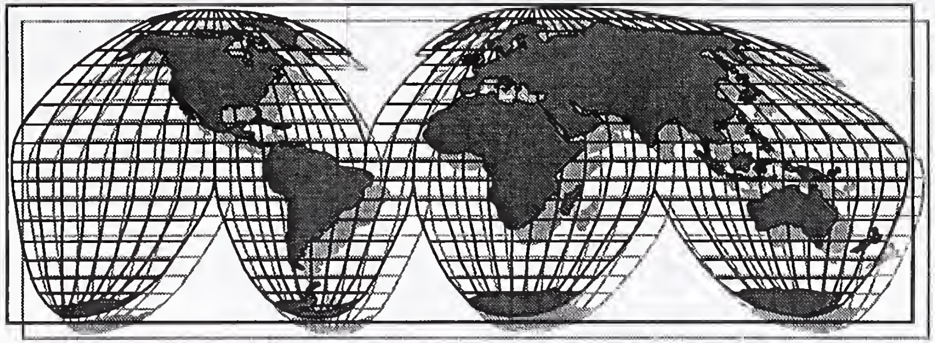
- DisplayWorks'98-Jan 29-30, San Jose CA
- WINhec '98 - April 8-11, Orlando FL
- SID '98 - May 19-21, Anaheim CA
- COMTEX '98 - June, Taiwan ROC
- COMDEX/Fall '98 - Nov 17-21, Las Vegas, NV

VESA STANDARDS

COMMITTEE OVERVIEW PRESENTERS

- FPDI - Michael Marentic, Chair Leader
- P & D - Ian Miller, Chair Leader
- Monitor - Bob Myers, Past Chair Leader*
- Home Network - Joel Digirolamo, Chair Leader
- PC Theatre, John Frederick, Chair Leader

VESA STANDARDS



FPDI Committee Report

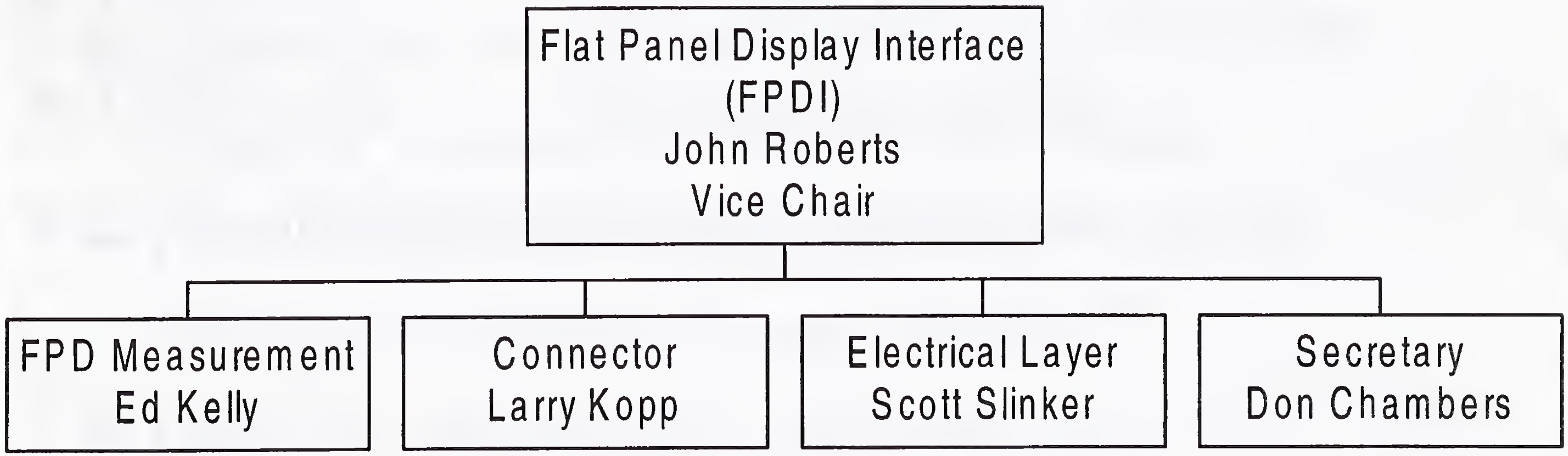
Presenter: Michael Marentic, Manager Technical Center, Hitachi

VESA, Flat Panel Display Interface Committee Chairman

COMMITTEE CHARTER AND GOALS

- Standardize the internal connector interface on Flat Panel Displays for use in closed system environments
- Provide practical, thorough metrology for characterizing display devices

COMMITTEE STRUCTURE



Why A FPDI Committee ?

- Difficult to interface different FPDs to a single graphics controller board design
- Incompatible electrical interfaces, signal timings, connectors, pin assignments
- Variety of optical measurement conditions
- Membership consists of Users, Manufacturers, Component Suppliers

RELEASED STANDARDS SUMMARY

- FPDI-1 October 1995
- FPDI-1B September 1996
- Both documented existing designs

CURRENT STANDARDS SUMMARY

- FPDI-2 Winter 97
  - Leads the Industry
  - Addresses the EMI problem
  - Innovative, Scaleable Electrical Layer selected
  - Defined Connector and Pinout
  - Optional DDC
- FPDI - Timing

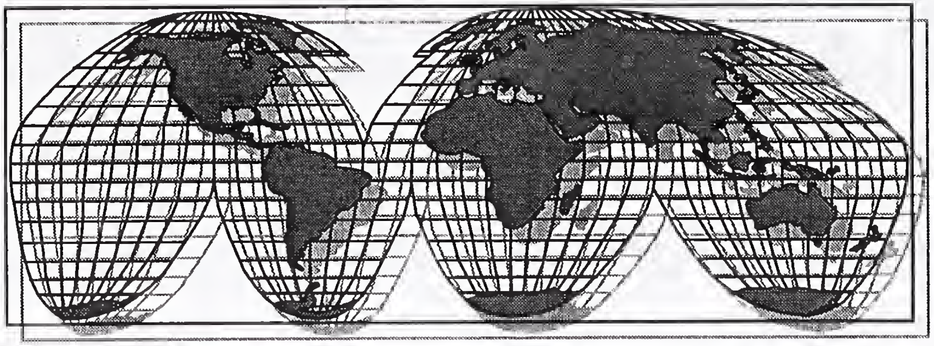
FPDI-2 SUMMARY

- Electrical Layer is Panel Link™
  - Transition Minimized Differential Signaling
- Mandatory single row 20 pin connector
- Optional 8 pin connector for monitor applications - DPMS, stereo sync
- Pixel mapping formats - TFT and DST

STANDARDS DESIGN

- Identify Need
- Define Requirements
- Solicit Proposals
- Vote for Solution
- Write Document

VESA STANDARDS



P&D Committee Report

Presenter: Ian Miller, Consultant

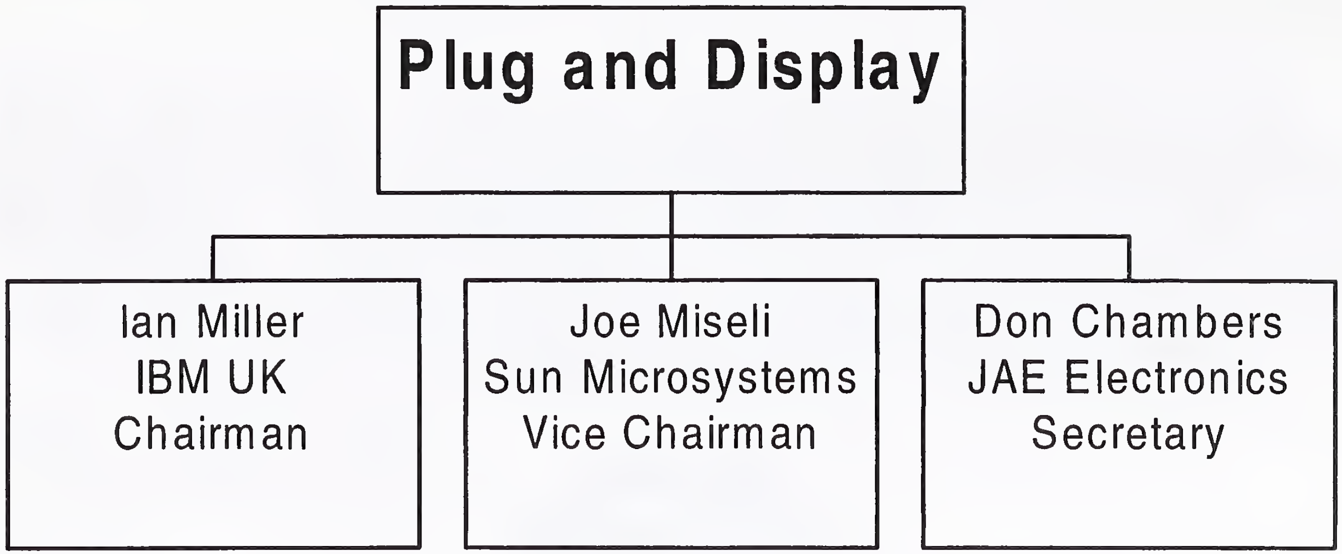
Visual Products, Technical Office, IBM

VESA, Plug and Display Committee, Chairman

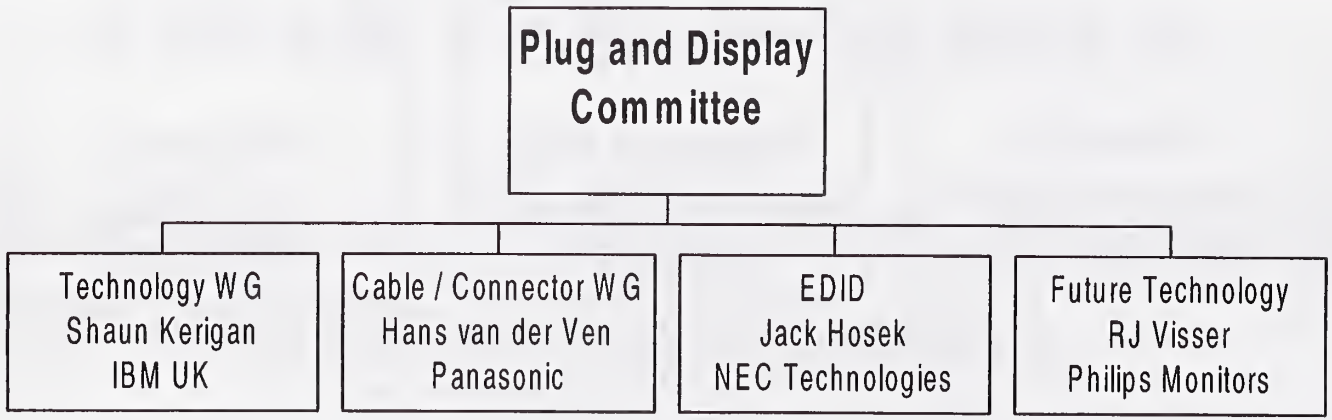
PLUG & DISPLAY COMMITTEE CHARTER & GOALS

- To develop an efficient digital interface for fixed pixel format video displays
- To develop standard within an architectural framework

COMMITTEE STRUCTURE



Committee Workgroups



Why A P&D Committee ?

- To provide a Focus for Digital Monitor Interface Standards Development
- To Support an Interface for Emerging Flat Monitors

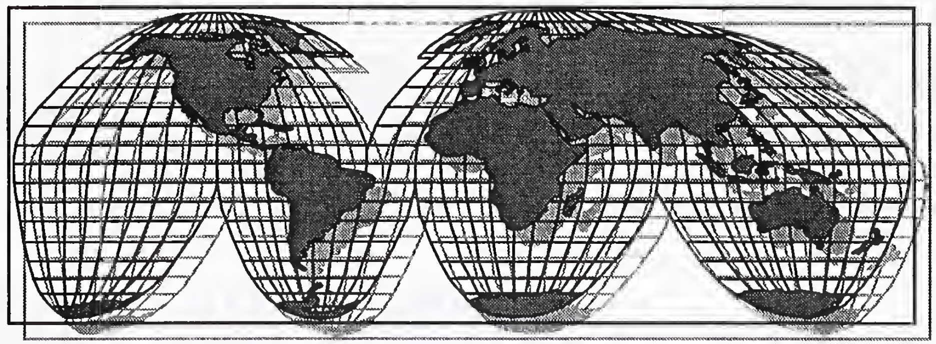
Objectives of P&D Standard

- Single Host Socket for any Display Device
  - Based on EVC Connector
- Auto Configuration
  - Uses DDC2 and revised EDID
- Cost Efficient Implementation
- Optional Support for Analog Video I/F
  - Backward Compatibility & Transition
- Support of Serial Digital Buses

STANDARD SUMMARY

- P&D Proposal is in Committee Review
- VESA Membership Review Shortly
- Ratified Standard in 1Q '97 (Target)

VESA STANDARDS



Monitor Committee Report

Presenter: Bob Myers
Senior Engineer
Hewlett-Packard

MONITOR COMMITTEE CHARTER & GOALS

- To develop practical, relevant standards for the computer display and graphics controller industries in a timely manner, and in the following areas - - -

MONITOR COMMITTEE CHARTER & GOALS (2)

- Display formats and timing standards
- Display interface and control
- Display performance measurement

COMMITTEE STRUCTURE

VESA MONITOR COMMITTEE

Chairman
Jack Hosek, NEC Technologies

Display Data Channel/
EDID Workgroup
Workgroup Leader:
Jack Hosek, NEC Technologies

Generalized Timing Formula
and DMT Workgroup
Workgroup Leader:
Bob Myers, Hewlett-Packard

EMC Workgroup
Workgroup Leader:
Hans van der Ven
Panasonic

Monitor Command Set Workgroup
Workgroup Leader
R.J. Visser
Philips

STANDARDS DEVELOPMENT IN 1997

- New timing standards for >1600 x 1200 formats.
- Release of the Generalized Timing Formula (GTF) standard.
- New versions of the Display Data Channel (DDC) and Extended Display Identification Data (EDID) standards (now in final voting)
- Revision of the Enhanced Video Connector (EVC) standard, for better compatibility with the new VESA Plug & Display standard.
- A new connector standard for stereoscopic display hardware (LCD glasses, etc.)

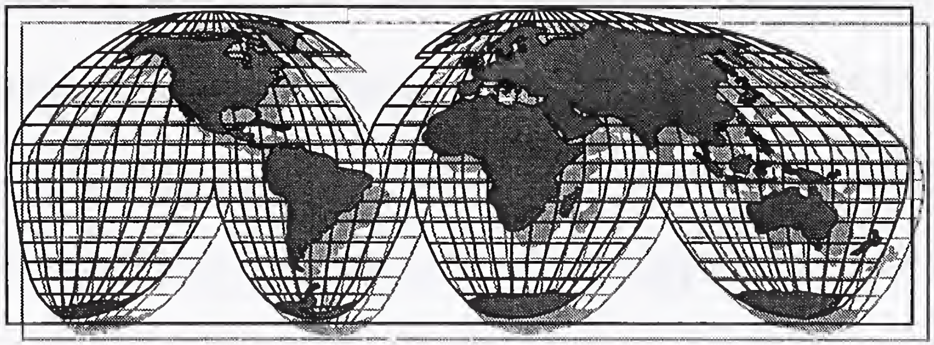
OTHER MONITOR COMMITTEE ACTIVITIES IN '97

- Continued support of DDC "Plug Test" events, where monitor and system manufacturers can verify their implementation of the DDC and EDID standards.
- Ongoing work with the Electric Utilities to resolve issues relating to the performance of CRT displays in power-frequency magnetic fields.

Monitor Committee Future Plans

- Continued development of new timing standards, including those required for the PC Theatre initiative.
- DDC/EDID revisions
- Continue to support DDC/EDID Plug Test events.

VESA STANDARDS



PC Theatre Committee Report

John Frederick

COMPAQ

PC Theatre Product Description

PC Theatre is a consumer living room entertainment device that merges computing and traditional forms of media and entertainment content. This system combines the best features of a TV and multimedia PC, delivering more entertainment options in a truly converged environment. The consumer may watch TV, use the PC, or both at the same time.

PC THEATRE COMMITTEE CHARTER

To develop a PC Theatre Interconnectivity standard using existing VESA, USB, and 1394 standards as building blocks that allows PC and CE manufacturers to produce PC Theatre computer and display products that are compatible, work together as a single system, are easy to use, and support automatic configuration.

PC THEATRE COMMITTEE GOALS

- To develop a standard that will enable PC and display manufacturers to build PC Theatre compatible products
- To use existing VESA, USB, and 1394 standards as building blocks in the overall PC Theatre standard
- To release the first version of the standard by 3Q98

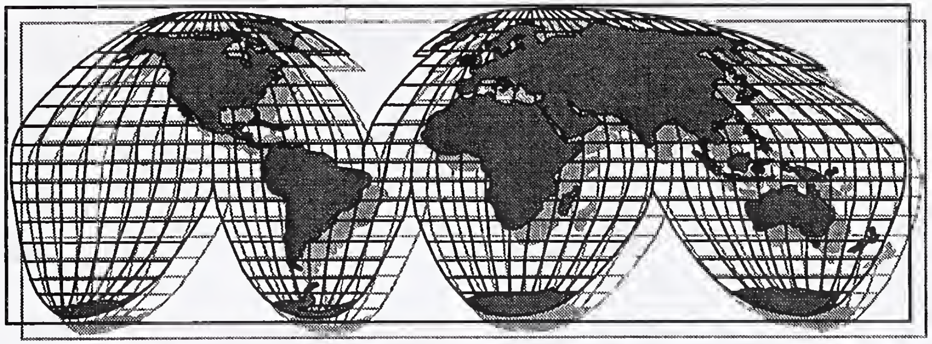
PC THEATRE COMMITTEE ACTIVITIES IN '97

- First Special Interest Group meeting August 97
- Committee formed August 97
- First draft of the PC Theatre Standard proposal released October 97

PC Theatre Committee Future Plans

- Release first version of the PC Theatre Standard in 1997
- Promote PC Theatre product category
- Start compatibility testing - VESA PC Theatre PlugTests
- Investigate further PC Theatre standard needs

VESA STANDARDS



Home Network Committee Report

Presenter: Joel DiGirolamo

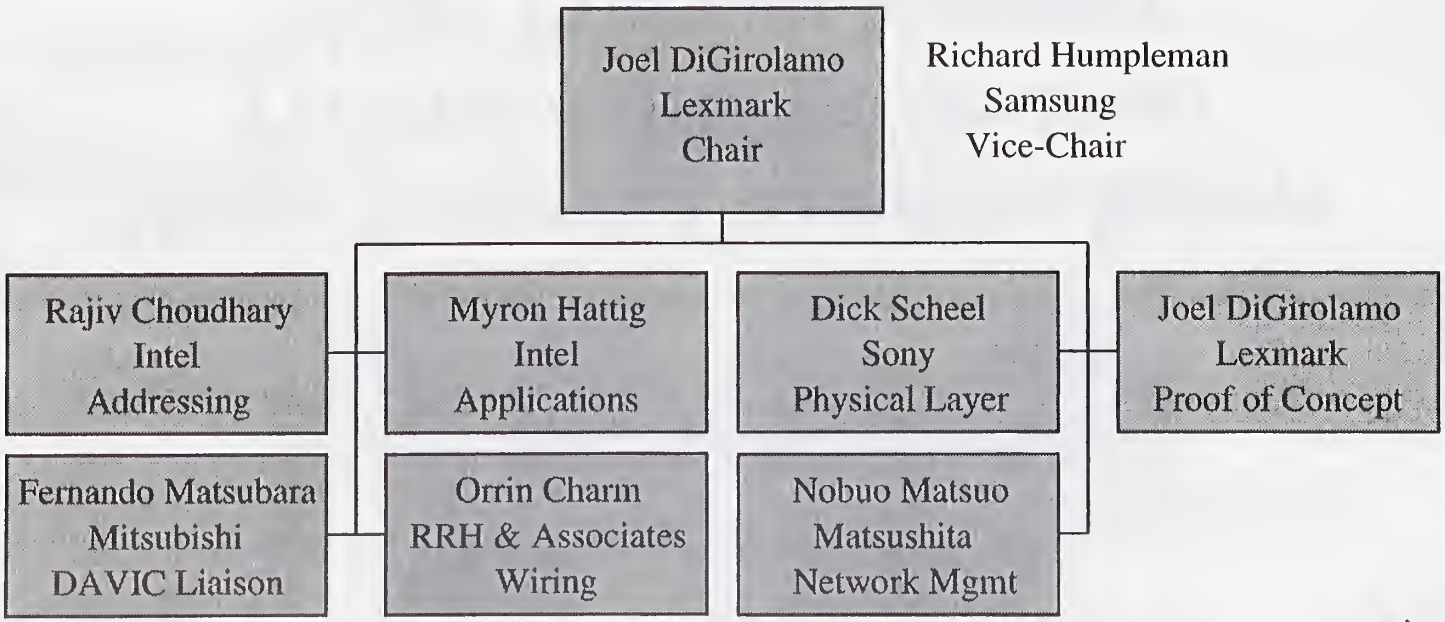
Senior Program Manager

Lexmark International

VESA, Home Network, Chairman

COMMITTEE STRUCTURE

HOME NETWORK COMMITTEE



Why A Home Network Committee ?

- Emergence of digital consumer electronics
- Convergence of computer & consumer devices
- Availability of digital home automation
- Availability of digital services to the home
- Make it all work together seamlessly!

STANDARDS PROGRESS

- Architecture defined
- High speed digital technology chosen
- Internetworking defined
- Addressing, NW mgmt., control in progress
- Draft standard writing in progress
- Technology development in progress

STANDARD SUMMARY

- Peer to peer network
- Handles multiple external services
  - Standard interface that each provider can design Network Interface Unit (NUI) to connect to
- High and low speed devices in the home
  - High speed: TV, VCR, CD, PC
  - Low speed: lamp, water heater
  - Data, control, and status on the same wires

STANDARDS SUMMARY

- Local cluster (usually one room)
  - IEEE 1394 - 100/200/400 Mbps
- Backbone
  - 100 Mbps 1394 modified for long distance
  - Aiming for 100 m maximum cable lengths
  - UTP Cat 5 and OF under consideration

STANDARDS SCHEDULE

- 6/97: Proof of concept phase 1
- 12/97: Proof of concept phase 2
- 12/97: First draft
- 1Q98: Specification ready for VESA review / vote process

DISPLAY INTERFACE/TECHNOLOGY RESEARCH AT NIST

JOHN ROBERTS

ADVANCED DISPLAY TECHNOLOGY SYSTEMS

INFORMATION STORAGE & INTERCONNECT SYSTEMS (ISIS)

SCALABLE PARALLEL SYSTEMS & APPLICATIONS GROUP

HIGH PERFORMANCE SYSTEMS AND SERVICES DIVISION

INFORMATION TECHNOLOGY LABORATORY (ITL)

NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY (NIST)

phone 301-975-5683 fax 301-869-7429 roberts@nist.gov

CHARTER

TO ASSIST INDUSTRY THROUGH:

- **RESEARCH**
  - Technology/Interface research in lab
- **STANDARDS**
  - Support development of VESA standards
- **MEASUREMENT**
  - Electrical signals, timing, etc.
  - (Not duplicate EEEL, Physics photometric, colorimetric research)

TWO RESEARCH EXAMPLES:

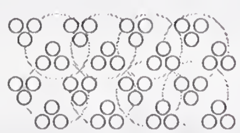
- RESOLUTION MAPPING ALGORITHM

- DISPLAY INTERFACE/TECHNOLOGY TESTBED

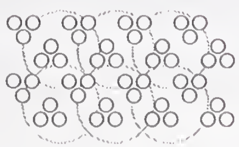
RESOLUTION MAPPING ALGORITHM:

Objective: to develop methods to characterize algorithms which remap images and text to different resolutions on fixed-pixel displays.

CRT CHARACTERISTICS



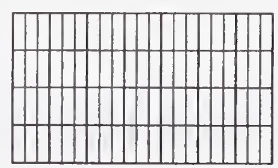
PIXELS OVERLAP, DO NOT CORRESPOND TO PHOSPHOR DOT PITCH



CHANGING HORIZONTAL, VERTICAL SWEEP RATE CHANGES RESOLUTION / PIXEL SIZE

LINES ARE INDISTINCT, BUT RELATIVELY SMOOTH

FPD CHARACTERISTICS



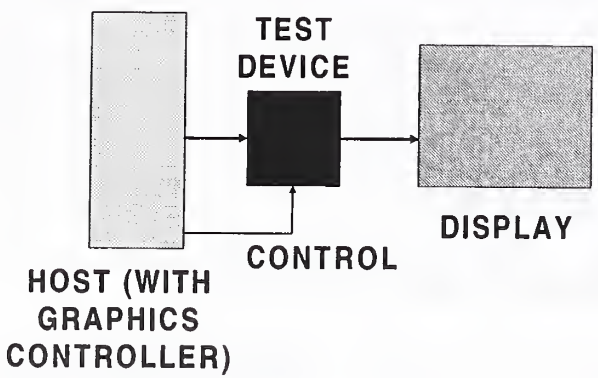
PIXELS ARE FIXED SIZE, DO NOT OVERLAP

LINES ARE SHARP, BUT MAY BE JAGGED

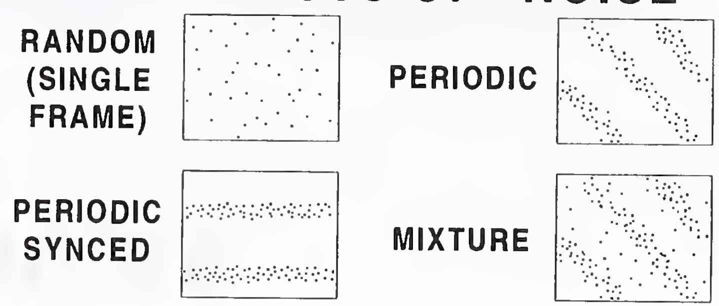
DISPLAY INTERFACE/TECHNOLOGY TESTBED

Objective: Develop an instrumentation to evaluate the characteristics of displays and display interfaces through manipulation of signals (from host or test generator) at the display interface.

TESTBED - HARDWARE IMPLEMENTATION



EXAMPLES - EFFECTS OF "NOISE"



HSYNC, VSYNC ARE LOW FREQUENCY - NOISE MAY CAUSE "JITTER"

SUMMARY

- Targeted research in specific areas can provide new insights on how host/display/user interfaces function.

- By supplementing the work done by industry, this research can provide useful information to industry, for technology and standards development.

DISPLAY METROLOGY AT NIST

FLAT PANEL DISPLAY MEASUREMENTS

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National Institute of Standards and Technology

DISPLAY METROLOGY AT NIST

- **FLAT PANEL DISPLAY LABORATORIES**

  REFINE MEASUREMENT METROLOGY OF DISPLAYS, ESPECIALLY FPDS.

  "Black Lab" (on tour) and "Black Hole"

- **FLAT PANEL DISPLAY INTERFACE LAB.**

  DEVELOPMENT OF INTERFACE STANDARDS

  (on tour)

- **OPTICAL TECHNOLOGY DIVISION**

  MAINTAIN NATIONAL STANDARDS OF RADIOMETRY, PHOTOMETRY, COLORIMETRY, AND RELATED METROLOGY

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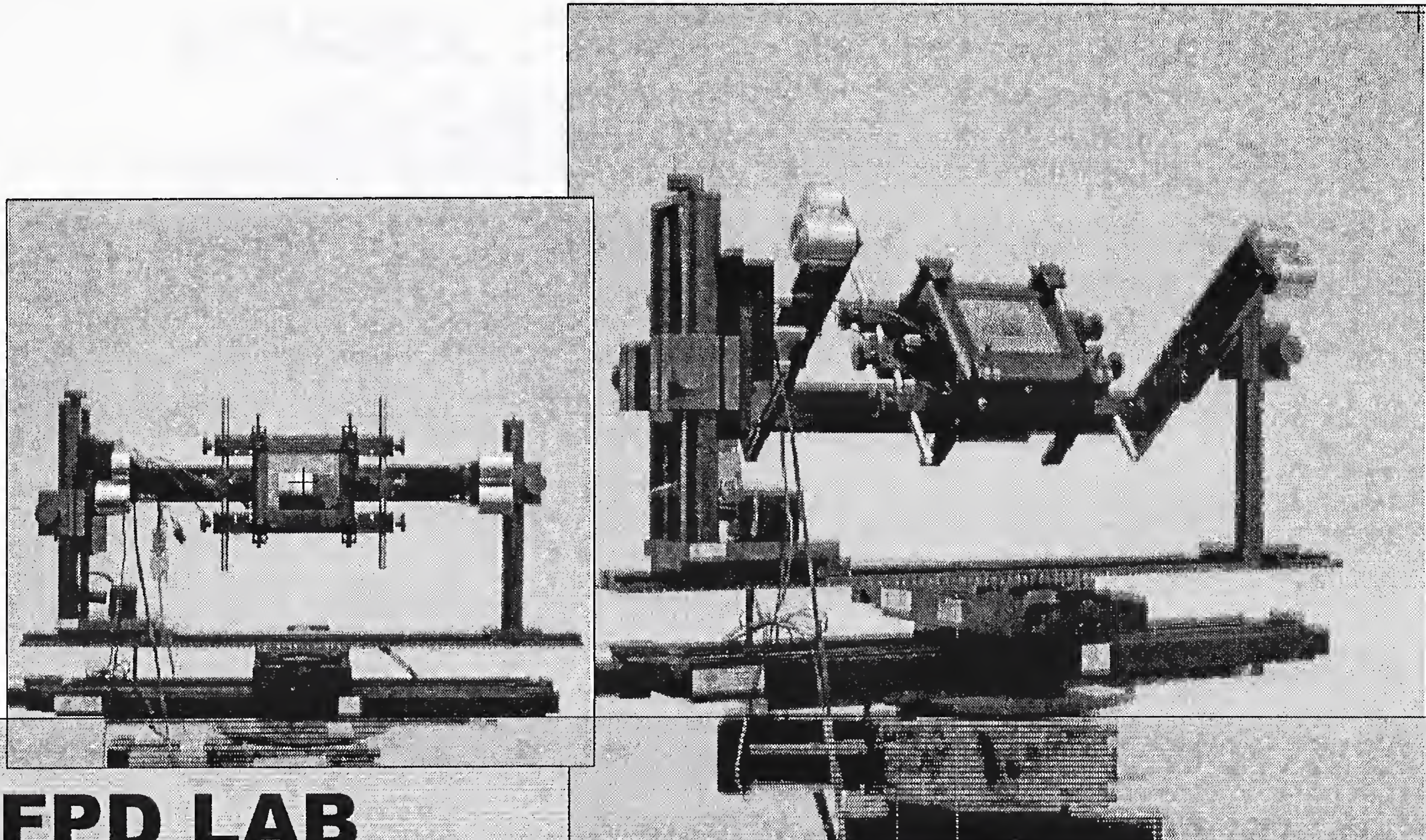

FPD LAB

DEVELOPED TO ASSIST INDUSTRY IN CREATING STANDARDS FOR DISPLAY MEASUREMENTS

NIST FLAT PANEL DISPLAY LABORATORY
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FLAT PANEL DISPLAY MEASUREMENTS

- **FPD MEASUREMENTS STANDARD**

  MEASUREMENTS—NOT COMPLIANCE

- **VESA WORKING GROUP**

  PARENT COMMITTEE: FPDI (INTERFACE)

- **ANSWERS CRITICAL INDUSTRY NEED**

  GOALS: *LEVEL PLAYING FIELD, SPECIFICATION LANGUAGE, UNAMBIGUOUS, METROLOGICALLY BASED, SIMPLE AS POSSIBLE, EXTENSIBLE ...*

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ADVANTAGES OF FPDM

- **BUFFET—EXTENSIBLE**
  PROCEDURES CAN BE EASILY ADDED
- **MEATBALLS, NOT SPAGHETTI**
  PROCEDURES COMPLETE, WELL-DEFINED
- **SAMPLE DATA AND EXAMPLES**
  ASSURE USER OF PROPER UNDERSTANDING
- **TOLERANT OF DEVIATIONS, ADAPTABLE**
  CHANGE TO SUIT TASK AND APPLICATIONS

AND ...

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VESA DOCUMENT
DRAFT #7
FPDM###
Doc. #### — September ?, 1997

FPDM

FLAT PANEL DISPLAY MEASUREMENTS STANDARD (Proposal)

Version 1.0P, Revision 0.0

VESA

VIDEO ELECTRONICS STANDARDS ASSOCIATION
Flat Panel Display Interface Committee
Flat Panel Display Measurements Standard Working Group

Abstract: This is a standard to provide measurement procedures to quantify flat panel display characteristics. Performance criteria or performance minima are not specified; rather, a series of measurements are clearly detailed to enable unambiguous and reproducible measurements of displays using the simplest instrumentation that will provide adequate results. All measurements need not be performed. The measurements that are most applicable to the display purposes can be selected as desired. Diagnostics and metrological difficulties are addressed, and technical discussions are presented to assist those unfamiliar with light measurements

September ?, 1997

DRAFT #7

LOOK, YOU CAN READ THE TITLE!

IT IS CLEAR “WHO DONE IT” AND WHAT VERSION YOU HAVE!

IT DOESN’T LOOK LIKE IT WAS MADE IN THE ‘60s WITH A TYPEWRITER.

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A Suite of Basic Measurements is identified with a suggested reporting format.

SBM

DISPLAY INFO: Manufacturer: ____ Model No: ____ Serial No: ____
DESCRIPTION: Diagonal Size: ____ Pixels: ____(hor) × ____(ver) Technology: ____
PITCH: Horizontal: Pixel: ____ Subpixel (Dot): ____ Other: ____ Measurement Direction: ____
Vertical: Pixel: ____ Subpixel (Dot): ____ Other: ____ Location of Center Meas.: ____
COLORS: Bits/color: ____ Color bits: ____ Gray Levels: ____ Total Colors: ____ Signal Source: ____ Power Source: ____
SIZE: Active Area: ____(hor) × ____(ver) LMD: Make: ____ Model: ____ Serial No: ____ Distance: ____ AFOV: ____
OVERALL: Dimensions: ____(hor) × ____(ver) Depth: ____ Mass (weight): ____ Design Viewing Direction: ____
Test Person: ____ Date: ____ Warm-Up Time: ____ min Temperature: ____ °C Run: ____ Page 1/2

Full-Screen Center (302-1...4)	L cd/m²	x	y
White			
Black			
C_R		No Units for C_R	
Red			
Green			
Blue			

Full-Screen Gray Scale (302-5)			
Level	L cd/m²	Opt-16	L cd/m²
Wht-7		Wht-15	
6		14	
5		13	
4		12	
3		11	
2		10	
1		9	
Blck-0		8	
Gamma			

Uniformity: Nonuniformity = 100% x [1-(Min/Max)] (306-1...4)							
9 point	5 point	L_w	L_b	C_U	x	y	CCT(K)
1	1						
2							
3	2						
4							
5	3						
6							
7	4						
8							
9	5						
Ave.							
Min.							
Max.							
Nonuniformity							
Anomalous Low							
Anomalous High							
Anom. Nonunif							

Power Consumption (401-1)			
Pattern Used:			
Supply	Volts	I(A)	(W)
High			
Panel			
Low			
High			
Inverter			
Low			
High			
Other			
Low			
High			
TOTAL			
Low			

L-P Performance (402-1)		
Input Power, P		
Pattern	White Full Screen	
Voltage		V dc/ac(rms)
Current		A dc/ac(rms)
Power, P		W dc/ac(rms)
Output Luminance, L_w		
L_w		cd/m²
Result: L-P Performance		
L_w/P		cd/m²W
Response Time (305-1)		
Blk-Wht		ms
Wht-Blk		ms
Total		ms

Ambient Contrast (308-2)									
White L_{AW}		L_w		L_b		L'_w		L'_h	
Black L_{AB}		L_{aw}		L_{ab}		L_{std}		D_{std}	
C_A		E				E_L			

Shad.=100%|L_{box}-L_{bkg}|/L_{bkg} (303-4)		
Box at (A-E)	Lum. (cd/m²)	
Box (0-7)	L_{box}	
Bkgnd. (0-7)	L_{bkg}	
Shadowing %		

Viewing Angle (307-1 or 2)		White				Black				Red			Green			Blue		
Direct'n	Angle	L_w	x_w	y_w	CCT(K)	L_b	x_b	y_b	C_R	L_{red}	x_{red}	y_{red}	L_{grn}	x_{grn}	y_{grn}	L_{blu}	x_{blu}	y_{blu}
Up θ_U																		
Dwn θ_D																		
Right θ_R																		
Left θ_L																		

Comments:

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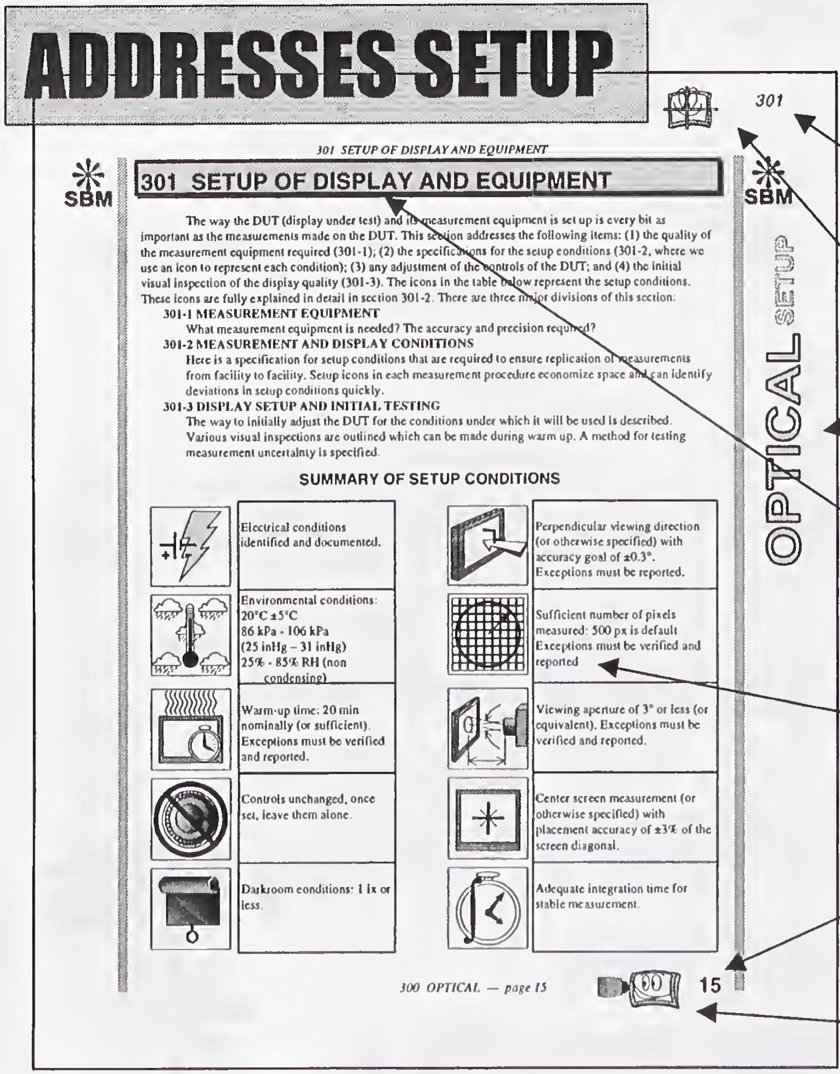
GENERAL FORMAT


ADDRESSES SETUP

301

301 SETUP OF DISPLAY AND EQUIPMENT

SBM

301 SETUP OF DISPLAY AND EQUIPMENT

The way the DUT (display under test) and its measurement equipment is set up is every bit as important as the measurements made on the DUT. This section addresses the following items: (1) the quality of the measurement equipment required (301-1); (2) the specifications for the setup conditions (301-2, where we use an icon to represent each condition); (3) any adjustment of the controls of the DUT; and (4) the initial visual inspection of the display quality (301-3). The icons in the table below represent the setup conditions. These icons are fully explained in detail in section 301-2. There are three major divisions of this section:

301-1 MEASUREMENT EQUIPMENT
What measurement equipment is needed? The accuracy and precision required?

301-2 MEASUREMENT AND DISPLAY CONDITIONS
Here is a specification for setup conditions that are required to ensure replication of measurements from facility to facility. Setup icons in each measurement procedure economize space and can identify deviations in setup conditions quickly.

301-3 DISPLAY SETUP AND INITIAL TESTING
The way to initially adjust the DUT for the conditions under which it will be used is described. Various visual inspections are outlined which can be made during warm up. A method for testing measurement uncertainty is specified.

SUMMARY OF SETUP CONDITIONS

	Electrical conditions identified and documented.		Perpendicular viewing direction (or otherwise specified) with accuracy goal of ±0.3°. Exceptions must be reported.
	Environmental conditions: 20°C ±5°C 86 kPa - 106 kPa (25 inHg – 31 inHg) 25% - 85% RH (non condensing)		Sufficient number of pixels measured: 500 px is default Exceptions must be verified and reported
	Warm-up time: 20 min nominally (or sufficient). Exceptions must be verified and reported.		Viewing aperture of 3° or less (or equivalent). Exceptions must be verified and reported.
	Controls unchanged, once set, leave them alone.		Center screen measurement (or otherwise specified) with placement accuracy of ±3% of the screen diagonal.
	Darkroom conditions: 1 lx or less.		Adequate integration time for stable measurement.

OPTICAL SETUP

300 OPTICAL — page 15

15

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302-1 LUMINANCE AND COLOR OF FULL-SCREEN WHITE

(brightness*, white screen, screen brightness*)

SBM

DESCRIPTION: We measure the luminance and optionally the chromaticity coordinates (also optionally the correlated color temperature [CCT]) of full-screen white at the center of the screen. Units: cd/m^2, none for chromaticity coordinates, K for CCT. Symbols: L_W, x_w, y_w, none for CCT.

The luminance of full-screen white (the screen's "brightness") is one of the most important metrics for a display and is used for several other measurements and calculations.

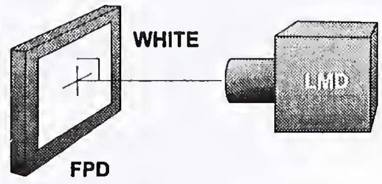
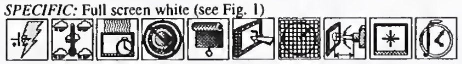


Fig. 1. Center luminance of full-screen white

SETUP: Display a white full-screen test pattern. See Section 301 for any standard setup details.
SPECIFIC: Full screen white (see Fig. 1)



PROCEDURE: Measure the center-screen luminance and optionally the chromaticity coordinates (also optionally the CCT) of full-screen white subject to above set-up conditions.

ANALYSIS: None. If you have made several measurements, you may calculate the mean values for full-screen white.

REPORTING: Report the luminance (optionally the chromaticity coordinates) of full-screen white to no more than three significant figures. If the CCT is measured it may be reported to four significant figures. If you have made several measurements, you may report the mean values.

Reporting Results - Sample Data			
Full Screen Center Performance			
	L (cd/m^2)	CIE x	CIE y
White	43.9	0.277	0.285
[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	No Units for C_R		
[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]

SAMPLE

COMMENTS: If you haven't already tested the uncertainty in the luminance measurement, now is a good time to do it; see sections Adequate Integration Time (301-2i) and Luminance Measurement Repeatability (301-2k) for instructions. Bear in mind that all the full-screen measurements are made with the same equipment configuration.

* Note: Luminance and brightness are not the same thing. Two colors can appear to have the same brightness and exhibit different luminances. Brightness should not be used synonymously with luminance. We include it here because of tradition and history. See Glossary and A201.

MEASUREMENT STRUCTURE:

DESCRIPTION
(DISCUSSION)
SETUP
PROCEDURE
ANALYSIS
REPORTING
COMMENTS

SAMPLE DATA AND EXAMPLES CLEARLY MARKED

302-3 CONTRAST RATIO OF FULL SCREEN

SBM

(contrast, full-screen contrast, full-screen contrast ratio, maximum contrast)

DESCRIPTION: We calculate the contrast ratio of full-screen white and black. Units: none, a ratio; symbol: C_R. (Note: we prefer the use of "contrast ratio" rather than just "contrast" in order to avoid confusion with other contrast metrics).

The full-screen contrast ratio is probably the second most notable metric for displays other than the luminance of full-screen white. A display with high contrast capabilities is often better able to create more realistic images and to provide better readability; especially when the black or dark regions of the image constitute a substantial amount of the screen surface in which case the eye appreciates the greater contrast. The full-screen contrast ratio is the most simple and reproducible contrast measurement to make.

SETUP: None. Measurements of full-screen white and black are made previously (302-1 and 302-2).

PROCEDURE: None. Measurements of full-screen white and black are made previously (302-1 and 302-2).

ANALYSIS: Calculate the contrast ratio $C_R = L_W / L_b$.

REPORTING: Report the contrast ratio to no more than three significant figures using the values for L_W and L_b obtained in the previous sections. Report as a single number with or without a colon, such as "232" or "232:1".

COMMENTS: The contrast ratio of a display is very sensitive to an accurate black measurement (see Contrast Measurement Errors in the Metrology Section).

Reporting Results - Sample Data			
Full Screen Center Performance			
	L (cd/m²)	CIE x	CIE y
White	[illegible]	[illegible]	[illegible]
Black	[illegible]	[illegible]	[illegible]
C_R	243	No Units for C_R	
Red	[illegible]	[illegible]	[illegible]
Green	[illegible]	[illegible]	[illegible]
Blue	[illegible]	[illegible]	[illegible]

SAMPLE

NOTE: The full-screen contrast ratio is the contrast metric to be measured and reported for comparisons between direct-view display technologies (not necessarily projection systems). Any other contrast metric must be properly identified explicitly if it is not this full-screen contrast ratio. Always provide the above C_R in any characterization of the display. If a non-perpendicular viewing angle is used it must be reported with the contrast.

For example, if someone simply says that the contrast of their display is such-and-such, it must be referring to the C_R above. If a box contrast is used then it must be stated "the box contrast is…," similarly for a 4 x 4 checkerboard contrast, "the 4 x 4 checkerboard contrast is…." In any case we strongly suggest that the above C_R always be reported.

If a viewing angle is employed such as 4° down vertically and $C_R = 400$ whereas $C_R = 250$ for the perpendicular we strongly suggest both be reported explicitly, such as, "The contrast at a 4° vertically down from perpendicular is 400:1. The contrast at the perpendicular is 250:1."

SBM

NUMBERING SYSTEM AVOIDS 3.9 < 3.10 AND 3.17.2.11.4.3.2.1.7

A VARIETY OF CONTRAST MEASUREMENTS IS SPECIFIED, HOWEVER ...

FULL-SCREEN CONTRAST RATIO MEASUREMENT IS ALWAYS REQUIRED

THUS, NOBODY CAN CHEAT!

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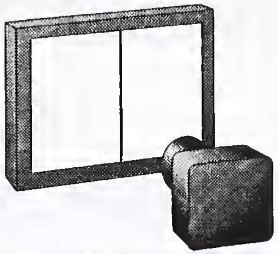
APPROPRIATE WARNINGS ARE PROVIDED

AND ADEQUATE GRAPHICS

303-1 LINE CONTRAST RATIO

WARNING
This measurement can be grossly inaccurate unless proper accounting (and/or correction) is made for veiling glare or lens flare.



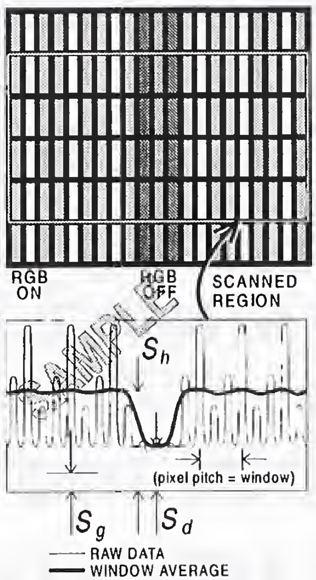
DESCRIPTION: Measure the contrast of a single-pixel vertical (optionally horizontal) black line against a white screen (positive configuration) attempting to correct for some of the veiling glare in the LMD. **Units:** none, a ratio. **Symbol:** C_L

The display of a black character on a white screen can be one of the most important functions of a display used in a workplace environment. Unfortunately, measuring the contrast of a character is difficult and usually very inaccurate. Rather than measuring a character, we recommend a single line in order to provide a more reproducible measurement. See the Comments Section below for more discussion. The problem is to accurately determine the contrast ratio of the luminance of the white area L_w to the black line L_b

$$C_L = L_w / L_b$$

without corruption from, for example, the lens system of the LMD or reflections between the LMD and the FPD.

Note: In this measurement a horizontal line can be used, or perhaps a measurement of both vertical and horizontal lines will be desired. The procedure is the same for horizontal lines as for vertical lines; read "horizontal" rather than "vertical" in the following procedure should horizontal lines need to be measured Additionally, if it is desired to measure the contrast of a white line on a black screen (negative configuration), the same procedure can be used with "black" and "white" switched around. This may be a simple approximate measurement to provide an indication of the character contrast; see Comments below.



305-2 RESIDUAL IMAGE

(latent image, burn-in, image retention)

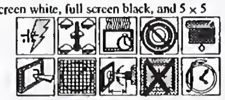
NOTE: This measurement can cause irreparable damage to the display.

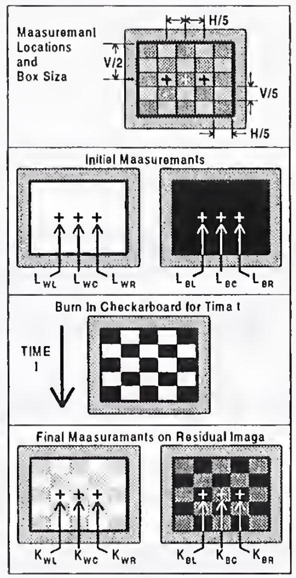
DESCRIPTION: Measure the residual image of a high-contrast checkerboard. **Units:** in percent of full-screen white. **Symbol:** R_W for white, R_B for black.

This is a measurement of how the screen is affected by long-term static images. We will see how a long-term static 5 x 5 checkerboard affects the display of a full-white screen and a full-black screen. Initially, we will measure the full screens of both white and black at three locations to account for any local luminance nonuniformities. Then we burn in the checkerboard. Finally examine full screen white and black to see if there is any residual image.

SETUP: Arrange to measure the display at three points left of center a distance of the checkerboard box width, at center, and right of center a distance of a box width. Depending upon how uniform the screen is, it may be necessary to measure at the exact same three locations throughout the procedure. This will require a reproducible positioning of the LMD relative to the screen. You will need to display a white full screen, a black full screen, and a 5 x 5 checkerboard pattern of black and white boxes with a black box at the center and box size of 1/5 of the screen.

SPECIFIC: Full-screen white, full screen black, and 5 x 5 checkerboard patterns.





DANGER
DAMAGE TO DISPLAY POSSIBLE

PROCEDURE:

Initial Measurements: Display a white full screen and measure the center luminance L_{WC} and the luminance on each side of center L_{WR} and L_{WL} (for right and left) a distance of 20% ($H/5$) of the screen horizontal width H. Similarly, display a full black screen and measure the luminances L_{BC}, L_{BR}, L_{BL} at the same three locations.

Burn-In: Burn-in the checkerboard image by allowing it to remain displayed continuously for the a certain number of hours t agreed to by all interested parties (the number of hours t is reported). Near the end of the burn-in time align the LMD to measure at the same three locations.

Final Measurements: At the end of the burn in time, switch the DUT directly from a checkerboard to a white full screen, and as soon as possible measure the luminance at the three locations (center, right, left) K_{WC}, K_{WR}, K_{WL}. Then switch the display to a black full screen, and measure the luminances at the three locations (center, right, left) K_{BC}, K_{BR}, K_{BL}. These measurements should be made in as small a time as is easily possible.

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OTHER FEATURES

- **METROLOGY SECTION**

  DETAILS ABOUT HOW TO MAKE GOOD MEASUREMENTS AND DIAGNOSE THE RESULTS

- **TECHNICAL DISCUSSION SECTION**

  PHOTOMETRIC UNITS ARE VERY DIFFICULT TO UNDERSTAND. CUTE LITTLE PROBLEMS ARE PRESENTED. ADDITIONALLY, OTHER TOPICS OF INTEREST ARE INCLUDED.

- **GLOSSARY**

  COMPREHENSIVE

- **TABLES**

  SUMMARY OF IMPORTANT TABLES, ETC.

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VI. Track I: Display Interface Workshop

VESA PLUG and DISPLAY

A NEW VIDEO INTERFACE STANDARD

Ian Miller, IBM PC Co.
Greenock, Scotland

P&D : WHY A NEW STANDARD ?

- INCREASING MONITOR PERFORMANCE
  - Inadequate bandwidth on "VGA Interface" with 15 pin D-shell connector
- INTRODUCTION OF NEW DISPLAY TECHNOLOGIES e.g. LCD monitor
  - Not well suited to analogue video interface
  - Digital Interface
    - No Industry Standard Exists
  - Several Proprietary Interfaces
    - Very Limited Compatibility

P&D : WHAT IS IT ?

- HIGH BANDWIDTH ANALOGUE VIDEO
  - e.g. CRT MONITORS
- DIGITAL VIDEO
  - e.g. LCD MONITORS
- DISPLAY DATA CHANNEL
  - AUTO CONFIGURATION; MONITOR CONTROL
- USB (OPTION)
- IEEE-1394 (OPTION)
- CHARGE POWER (OPTION)

Ian Miller, IBM PC Co. 06/10/97 3

P&D : Key Features - 1

- High Bandwidth RGB2S Interface
- Digital Interface
  - PanelLink (TM) Technology
- DDC2B (or higher level)
- USB Option
- IEEE-1394 Option
- Charging Power Option

Ian Miller, IBM PC Co. 06/10/97 4

P&D : Key Features - 2

- Auto Configuration
- Hot Plugging and Automatic Re-configuration
- Independence from Display Technology
  - CRT, LCD, Plasma, DMD, etc
- Uses DDC Ver. 3 and EDID Ver. 3
  - New Proposed Standards from Monitor Committee
- Cable Length to 10 m
- Complements EVC Standard

P&D : ANALOGUE INTERFACE

- Impedance Matched Video Path
  - VGA Interface System has Bandwidth Limit Caused by Impedance Mis-Match
    - Details of High Information Content Images are Being Lost
- Bandwidth of Video Lines
  - Connector System Specified at 2.4 GHz min.
- PC97 and PC98 have High Addressibility Requirements and Recommendations
  - A New High Bandwidth Interface is Required

P&D : DIGITAL INTERFACE

- Three Differential Signals for Data and Control
- One Differential Signal for Clock
- Data and Control Signals Encoded to Minimise Transitions
- Up To 1280 x 1024 @ 60 Hz at 24 bpp
- Extension to 1600 x 1280 @ 60 Hz at 24 bpp

P&D : OPTIONAL FEATURES

- USB
- IEEE-1394
- Charging power
- Can Be Selectively Loaded
  - Any Combination

P&D : HOT PLUGGING

- Basic Protection
- Automatic Re-configuration When New Monitor Plugged
- Uses +5V (DDC) to Signal from System Unit
- Uses Charge Power Line to Signal from Monitor to System Unit

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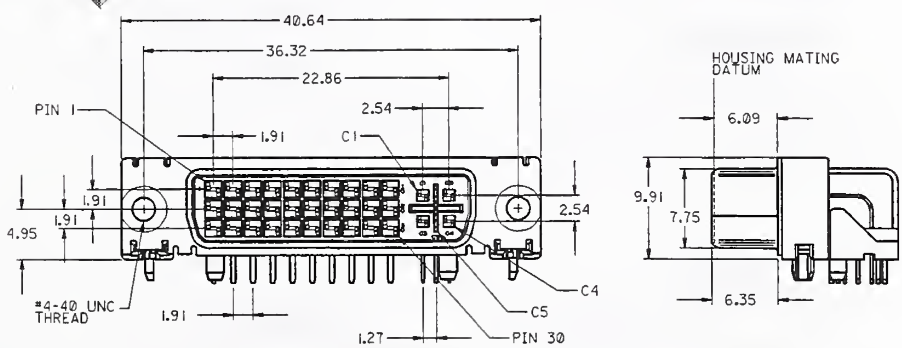
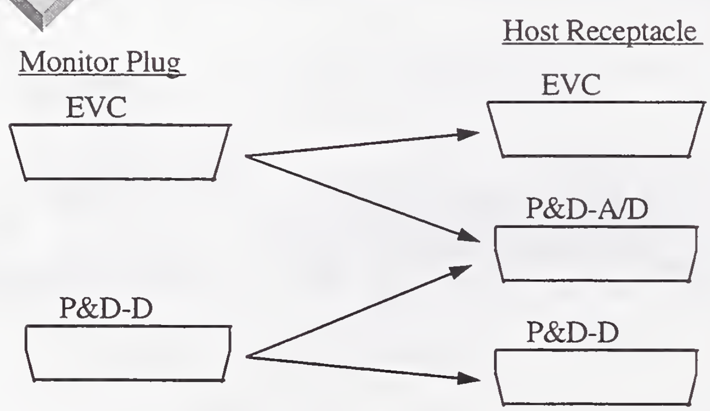
P&D : RECEPTACLE



P&D : RELATIONSHIP WITH EVC

- Identical Contact Layout
- Same Pin Numbers for All Signals That are Carried by Both Connectors
- Different Shell Profiles and Mechanical Details in Microcross area to Protect Against Inappropriate Plugging
- Together they Form a Family

P&D : CONNECTOR FAMILY



Note: Other connections are physically impossible

P&D : CONCLUSION

- P&D IN HOST SYSTEM
  - Any Display technology
  - Optimal Video Interface
  - Auto Configuration
  - Hot Plugging
  - Serial Bus Options
- Interoperable, One Stop Plugging for Monitors

P&D : A New Video Interface Standard

Shaun Kerigan and Ian Miller
IBM PC Co.
Greenock
Scotland

Abstract:

This paper reviews the recently ratified VESA ™ P&D™ standard which incorporates high performance analogue and digital video together with USB and IEEE 1384 options in a single connector. With automatic configuration, the optimal video interface for each display technology is selected and used.

Background

The predominant interface used for monitors today is analogue video with horizontal and vertical synchronisation pulses (RGB2S), using a 15 pin D-shell connector and with a cable length of approximately 1.8m.

The analogue video of this interface is well suited to CRT technology but image quality is adversely affected at high addressibilities since the 15 pin D-shell connector has a limited bandwidth.

However, this interface is not well suited to most flat panel technology monitors which require the analogue video signals to be converted back to digital signals. Achieving this conversion requires a pixel clock to be generated and locked to the horizontal synchronisation pulses. This process is difficult and expensive to engineer but, even more importantly, results in image quality loss and the possible introduction of image artefacts.

These problems together with the benefits arising from a single video port capable of allowing optimal connection of a wide variety of display technologies have been realised by a number of engineers working for member companies of the Video Electronics Standard Association (VESA), (Myers (1) (2) and Schussler (3). In early 1996 activity was started at VESA which resulted in the formation of the P&D committee.

P&D Objectives

One of the first actions of the P&D committee was to agree a set of key objectives, in summary:

- A single industry standard connector
- Scaleable cost structure
- Scaleable digital support from 640 x 480 to 2.5K x 2K at up to 75Hz. and 30bpp.
- High bandwidth RGB2S
- A flexible cable of $\geq$ 2m
- Automatic configuration using DDC and EDID
- Hot plugging protection
- Independent hardware and software layer
- Independence from the OS
- A bidirectional control channel
- A high speed bidirectional data channel
- Based on demostrable prototype

The P&D Standard

The P&D standard was ratified in June 1997 and meets most of the objectives outlined above.

When power is applied the interface will automatically use the contents of the Extended Display Identification Data (EDID ™) transmitted from the monitor to the system unit using the Display data Channel (DDC ™) bus to set optimal conditions.

The analogue video interface has a bandwidth of 800MHz, able to handle the highest requirements today with scope for even higher requirements in the future.

The digital video interface uses Transition Minimised Differential Signalling (TMDS ™ [1]) technology (Lee (4)), capable of supporting TFT-

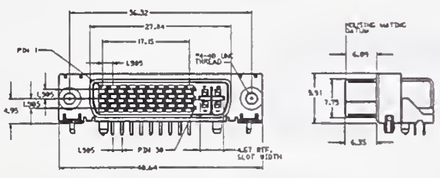
[1] TMDS uses PanelLink ™ technology developed by Silicon Image

LCD and both single and dual scan STN displays from 640 x 480 to 1280 x 1024 pixels (25 Mpixels/s to 112 Mpixels/s). Future TMDS technology supporting 1600 x 1200 displays at 160 Mpixels/s is expected. An important aspect of the digital interface is standardisation of the pixel mapping to be used for LCD display technologies.

Today TMDS (Lee(7)) supports between VGA @ 60 Hz (25 Mpixels/sec) to SXGA @ 60 Hz (112 Mpixels/sec) for TFT-LCD display in addition to support for single and dual scan STN displays and other temporal modulated displays at up to 10 meters cable length. In the future TMDS will support up to UXGA (1600X1200) @ 60 Hz (160 Mpixels/sec). The pixel mapping for TFT-LCD's, STN Single and Dual Scan are defined for TMDS within the P&D Standard.

The P&D connector (Fig 1) differs from the VESA Enhanced Video Connector (EVC) only by the shape of the shell.

Figure 1



The following signal sets are supported:

- RGB2S video
- TMDS video
- DDC2
- Universal serial bus (USB)
- IEEE-1396-1995
- Charge Power

The USB and IEE1394 buses are optional and may be used to provided support for audio, video in / out, keyboards, mice etc.

The following section dealing with ac coupling of the TMDS bus is directly extracted from the P&D standard:

Cable lengths of up to 10m are permitted although this may be restricted to 5m if either the USB or IEEE-1394 options are used.

The P&D standard requires use of capacitor coupling between the TMDS transmitter and receiver, see Figure 2

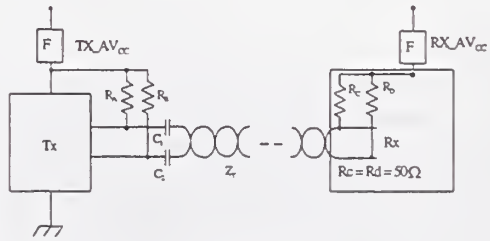


Figure 2

The purpose of R_A and R_B is to provide an average DC level on the TX side and provide source termination. R_C & R_D are on-chip termination resistors in the TMDS receiver.

Note:
$R_A = R_B = \frac{1}{2} Z_T$, with $Z_T = 100\Omega$,
T_{CLK} = 25MHz - 112MHz,
$C_1 = C_2$, $1nF < C_1 < 100nF$,
$R_C{*}RX\_AV_{CC} = R_D{*}RX\_AV_{CC} = 1/2V_{SWING}$

	25 - 65 MHz	**65 - 112 MHz**
Z_T	100 Ω	100 Ω
C_1	10 nF +/- 20%	10 nF +/- 20%
C_2	10 nF +/- 20%	10 nF +/- 20%
R_A	100 Ω	100 Ω
R_B	100 Ω	100 Ω
R_C	50 Ω	50 Ω
R_D	50 Ω	50 Ω

The RGB2S analogue red, green, blue, horizontal sync., vertical sync. with optional pixel clock) are supported with a bandwidth of 800 Mhz.
The high frequency analogue signals are connected via the MicroCross ™ section of the connector.

Can EVC and P&D Co-exist ?

The answer is clearly yes, EVC and P&D are complementary, each with advantages for particular market segments.

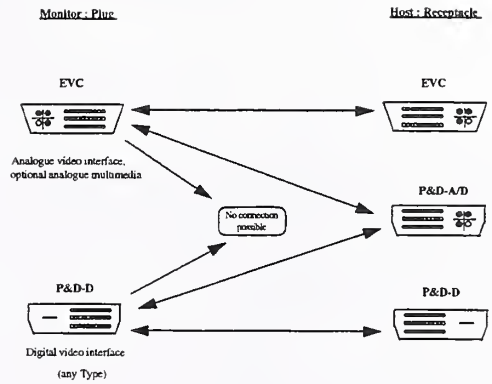
Figure 3 provides a comparison of the signals and functions available in the system receptacles under EVC and P&D standards:

	EVC	P&D A/D
RGB2S	Yes	Yes
TMDS	No	Yes
IEEE-1394	Optional	Optional
USB	Optional	Optional
Charge power	Optional	Optional
DDC	Yes	Yes
Analogue video	Optional	No
Analogue audio	Optional	No
Hot plugging Re-configuration	Optional	Yes

Figure 3

Signals common to both interfaces are allocated the same pin number, this allows an EVC plug to mate with the P&D receptacle making connection with RGB2S, DDC, USB, IEEE-1394 and Charge Power Signals but the P&D plug cannot mate with the EVC receptacle due to the different shell shapes.

Certain other undesirable combinations of EVC and P&D connectors are not possible due to mechanical differences in the MicroCross area. This is summarised by Figure 3.



Conclusion

If implemented in the host system, the P&D interfaces provides a single connector capable of optimally supporting a wide range of display technologies. Additionally, the P&D standard introduces the only standard for digital video, ensuring that hardware from different companies is Interoperable.

Trademarks:

1. VESA, EVC, P&D and TMDS are trademarks of the Video Electronics Standards Association
2. PaneLink is a trademark of Silicon Image Inc.
3. MicroCross is a trademark of Molex Corp.

References:

1) An Overview of the needs for a Unified Display Interface. B Myers 16.4 SID 96 San Diego.
2) VESA Standards for “Plug and Play“ Monitors. Myers Flat Panel Information Displays ‘96
3) A Universal Monitor Interface. J. E Schussler 16.5 SID 96 San Diego.
4) High Speed Digital Video Signal Transmission System using small swing serial link technique. K Lee et al 12.4 SID 97 Boston
5) VESA P&D Standard
6) VESA EVC Standard
7) VESA EDID Standard
8) VESA DDC Standard

VESA® P&D™ TMDS™ (PanelLink™ Technology) and Its Applications for Flat Panel Displays

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Introduction

As Flat Panel Displays (FPDs) increase in size, color depth, and resolution, the clock speeds and number of parallel data bits to drive them also increases. A new interface standard is required to deliver high bandwidth and reliable images that are comparable to or better than CRTs. Moreover, to achieve true "plug-and-play" capability, this new interface standard must be reliable, compatible, scaleable, affordable, and integrateable over a wide range of FPD technologies. To accomplish these goals, the Video Electronics Standards Association (VESA®) has released its Plug and Display (P&D™) FPD interface standard for desktop applications. It is also in the process of reviewing the final draft of the Flat Panel Display Interface - 2 (FPDI-2™) standard for notebook applications. Both standards are based upon the key technological features and architecture of PanelLink Technology from Silicon Image. These VESA standards define a low cost, scaleable digital interface, which overcome today's incompatibilities in connector types, cabling, and data formats for notebook and FPD monitor displays. These standards promises to accelerate the FPD monitor and notebook markets and elevate the multimedia experience to the next level via the use of large, true color, high resolution FPDs.

This paper will present a brief overview of the features and architecture that made PanelLink Technology the interface of choice for the VESA P&D and FPDI-2. It will then present some applications of VESA P&D TMDS that could open up new markets and accelerate wide market acceptance.

PanelLink Technology

PanelLink Technology is Silicon Image's solution to the FPD interconnect issues due to increasing number of signal lines, increasing clock speeds, and lack of a interface standard. PanelLink Technology is a patented high-performance, Transition-Minimized Low-Voltage Differential Signaling (TMDS™) technology that transmits graphics and video data at greater than gigabit per second on a single channel from a Flat Panel Multimedia Accelerator (FPMA) to a TFT (Thin-Film Transistor or Active) or DSTN (Dual-Scan Twisted-Nematic or Passive) FPD. There are three high speed serial data channels per link which gives a total transmission throughput of greater than 3 Gbits/sec. This link transfers data, clock, and control signals from the FPMA to the FPD using high speed patented TMDS and DC-balanced encoded data. It can transmit high speed data over copper media up to 10m and interface directly to fiber optic transceivers to transmit up to 500m. It has been integrated into FPMA and FPD controllers. PanelLink Technology defines a single, logical, simple interface that spans VGA (640x480) to UXGA (1600x1200) resolutions and beyond with the same interface; the exact same number of serial channels, which is only 3 data channels and 1 clock channel.

Transition Minimized Low Voltage Differential Signaling (TMDS)

The only way to achieve high serial data transmission speeds with low cost standard CMOS process technology is to use Low Voltage Differential Signaling (LVDS). This helps reduce the Electro-Magnetic Interference (EMI) generated by the high speed serial signals by reducing the voltage swing of the signal. Unfortunately, just doing a simple high speed parallel-to-serial conversion of the data using LVDS is not enough. The voltage swing of the transmitted signals is reduced, but the signal transitions of the high speed serial data transmission are dramatically increased. This increase in signal transitions has an impact on EMI. Therefore, PanelLink Technology's patented encoded TMDS method, which controls the number of signal transitions, will help reduce the total number of signal transitions. The voltage swing, rise/fall times, pulse width, and period of a signal will have an effect on the frequency spectrum of a signal which will, in turn, have an impact on EMI. The higher the voltage swing, the shorter the period, the faster the rise/fall times; the larger the power of the frequency spectrum which will impact EMI. Using high speed serial TMDS, all the variables that affect the frequency spectrum of a signal will be reduced which in turn will help in reducing EMI.

As any Electro-Magnetic Compliance (EMC) expert understands, EMI is a system related issue. TMDS helps reduce EMI with the above mentioned features, but it is not the cure-all of system related EMI. Proper system PCB layout, mechanical, and EMC circuitry implementations are very important in reducing the overall system EMI. No one solution can solve all of the system related EMI, but PanelLink Technology can help in reducing its portion.

Data Over-Sampling

PanelLink Technology does three times over-sampling of the received serial data. This enables reliable data reception, than just single-sampling, in the presence of system noise which is inevitably present. Also, PanelLink Technology only uses the frequency information, and not phase, of the transmitted clock to generate the three times over-sampling clocks. This method allows clock-to-data skew tolerant designs.

Phase and Byte Alignment

Noise, jitter, and normal signal drift will affect the over-sampling clocks. PanelLink Technology uses a Digital Phase Lock Loop (DPLL) tracking mechanism by encoding the transmitted data to differentiate between display and non-display data. During non-display time, special synchronizing encoded data is transmitted. The DPLL uses these special synchronizing data to maintain the correct sampling points of the three over-sampling clocks every line and frame (during non-display time). Of the three over-sampled data of each serial bit, the DPLL recovers the correct data by obtaining only the center bit of the three over-sampled data. The DPLL continuously keeps track of the center of each serial bit, which results in skew-insensitive data recovery. Therefore, every line and frame, the received data will be aligned to the correct over-sampling clocks.

The DPLL also implements byte alignment by, again, using the special synchronizing encoded data during non-display time. A byte alignment logic finds the start position of the special encoded synchronizing data transmitted during non-display time from the recovered data. So, every line and frame, the received serial data will also be byte aligned. These two aligning mechanisms, with special encoded synchronizing data during non-display time, will enable reliable data reception. This allows long distance support with inexpensive standard twisted pair cables.

Multi-Channel Synchronization

Multi-Channel Synchronization is accomplished to minimize the inherent differences in the length of wires between each channel (channel-to-channel or data-to-data skew). By encoding the data to differentiate between display and non-display data, a status signal is used to determine if there is any skew between the serial channel data. PanelLink Technology uses DE (display enable), that each serial channel generates, to determine if there is any channel-to-channel skew. Each serial channel DE is compared with the other two serial channel DE to see if there is any channel-to-channel skew. If there is channel-to-channel skew, then the appropriate delay, up to one clock cycle, is implemented on the channel data with the skew to match the other non-skew channel data.

The data recovery method with data over-sampling, phase and byte alignment, and multi-channel synchronization allows clock-to-data and data-to-data skew to be tolerated. It also allows jitter and noise, inevitably present, to be tolerated. Therefore, this reliable data recovery method offers a very low error rate in the presence of extreme noise and skew, allowing long distance support using inexpensive standard twisted pair cables.

Current Drive

Current drive is the preferred method of implementing TMDS (LVDS) which eases the design for EMC and enables reliable data transmission. In a differential signal driver system, it is essential to make the signals symmetric so that the two differential signals cancel each other to nullify the common mode signal and also to make the differential signal "eye" wave-form as large as possible for better detection on the receiver side. The differential driver with a current source offer such symmetry by drawing two currents from the same source. The sum of the two output currents is constant and, therefore, the only common mode signal is DC which does not contribute to any AC signal. When the DC component, is subtracted from the two differential signals, only AC components remain and the two currents are in the opposite direction, canceling each other. Therefore, the two signals are differential in the AC sense.

An alternative method is to use two source followers for driving differential signals, known as voltage drive. Due to unequal drive capabilities of PMOS and NMOS transistors, symmetry on the differential signals are inherently difficult. When the output switches from high to low or low to high, the rise and fall times can not match since the pull-up current is driven by the NMOS transistor and the pull-down current is pulled-down by the PMOS transistor. The sum of the two signals is not a pure DC and a common mode signal is developed, causing EMI. This will also cause signal integrity issues due to the uneven shape of the differential signal "eye" wave-form.

Therefore, in low cost standard CMOS process technology, a current drive technique offers an inherently superior symmetry and thus is a better choice than a voltage drive technique. PanelLink Technology uses current driving method.

Adjustable Low Voltage Swing and Internal Impedance Matching Control

The signal driven through a cable will be degraded, mainly due to attenuation and skin effect, depending upon the type and length of the cable. Therefore, with PanelLink Technology's adjustable voltage swing, a wide variety of cable types and lengths can be supported. The larger the voltage swing, the better the signal to noise ratio for lower grade and longer cables. For shorter and higher grade cables, a smaller voltage swing can be used. This allows the receiver to sample reliable data over a wide variety of cable lengths and types. This also allows the customer to select a wide variety of cable types for its specific type of applications.

In transmission lines, if the characteristic impedance of the cable is not matched to the impedance of the load, there will be signal reflections. This will degrade the signal, which could have an effect on correct sampling on the receiver end. PanelLink Technology uses internal impedance matching control to minimize signal reflections to again, enable reliable data reception.

Standard Interface - Inter-Operability

The FPD data mappings for the popular FPMAs that support color TFT and DSTN FPDs are not compatible with one another. The FPD data mappings are all different from manufacturer to manufacturer for the different FPD technologies. The FPD interfaces for the popular color 24-bit and 16-bit color DSTN and 18bpp 1-pixel/clock and 2-pixel/clock TFT FPDs are all different from manufacturer to manufacturer. The connector type used for the FPD interface of these popular TFT and DSTN FPDs are also different from manufacturer to manufacturer. Therefore, with such incompatibilities no standard interface could be achieved. With one interconnect system, FPMAs and FPDs are not inter-operable and therefore, not "plug-and-play" like CRT monitors. This limits the interconnect system to custom designs.

Scaleability

A critical aspect of any standard interface is scaleability. Scaleability for an FPD interface means that one transmitter and one receiver pair must operate from 25MHz (VGA) all the way up to 202.5MHz (UXGA) and beyond with the same, constant number of serial data channels. It must support up to 24-bpp and up to 75Hz refresh as well as various FPD technologies. Table 1 shows the clock speeds required for various resolutions for the associated VESA CRT compatible 60Hz and 75Hz refresh rates with maximum blanking times. Table 2 shows the clock speeds required for various resolutions for the associated VESA Generalized Timing Format (GTF™) CRT compatible 60Hz and 75Hz refresh rates with minimum blanking times.

Table 1. Clock Speeds and Blanking Times for Various Resolutions for VESA Compatible CRT Refresh Rates[1]

Resolution	60Hz Refresh	Horizontal Blanking	Vertical Blanking	75Hz Refresh	Horizontal Blanking	Vertical Blanking
640 x 480 (VGA)	25MHz	18 characters	29 lines	31.5MHz	25 characters	20 lines
800 x 600 (SVGA)	40MHz	32 characters	28 lines	49.5MHz	32 characters	25 lines
1024 x 768 (XGA)	65MHz	40 characters	38 lines	78.75MHz	36 characters	32 lines
1280 x 1024 (SXGA)	108MHz	51 characters	42 lines	135MHz	51 characters	42 lines
1600 x 1200 (UXGA)	162MHz	70 characters	50 lines	202.5MHz	70 characters	50 lines

Table 2. Clock Speeds and Blanking Times for Various Resolutions for VESA Compatible GTF CRT Refresh Rates[2]

Resolution	60Hz Refresh	Horizontal Blanking	Vertical Blanking	75Hz Refresh	Horizontal Blanking	Vertical Blanking
640 x 480 (VGA)	19MHz	2 characters	3 lines	24MHz	2 characters	3 lines
800 x 600 (SVGA)	30MHz	2 characters	3 lines	37MHz	2 characters	3 lines
1024 x 768 (XGA)	48MHz	2 characters	4 lines	60MHz	2 characters	4 lines
1280 x 1024 (SXGA)	81MHz	4 characters	5 lines	101MHz	4 characters	5 lines
1600 x 1200 (UXGA)	120MHz	6 characters	5 lines	149MHz	6 characters	5 lines

Table 3 shows a list of PanelLink Technology's products and its associated maximum data rates. As shown, the data rates that PanelLink can support are more than enough for the above FPD resolutions at 60Hz, as well as some 75Hz, refresh rates for both normal VESA CRT as well as GTF timings. PanelLink Technology can do this with only 1 Transmitter/Receiver pair with the exact same interface of 3 data and 1 clock channel. PanelLink Technology does not have to increase the number of chips nor increase the number of data channels to support the various resolutions and refresh rates.

Table 3. PanelLink Technology's Performance Scaling

Silicon Image Part #	CMOS Process Technology	Max. Specified Speed	Max. Specified Data Throughput	Max. Lab Speed	Max. Lab Data Throughput	Status	# of Chips	# of Serial Channels
SiI100/101	0.5u 5V	68MHz	2.04Gbits/sec	86MHz	2.58Gbits/sec	Production	**1 Transmitter & 1 Receiver w/ Same Interface**	**3 Data and 1 Clock**
SiI140/141	0.5u 3.3V	86MHz	2.58Gbits/sec	100MHz	3Gibts/sec	Sampling		
SiI150/151	0.35u 3.3V	112MHz	3.36Gbits/sec	135MHz	4.05Gbits/sec	Q4 '97		

PanelLink Technology products are all fully compatible with each other. The only restriction is the maximum operating frequency would be the lower of the two. As an example, if a SiI140 transmitter was used with a SiI151 receiver, the maximum specified operating frequency would be that of the SiI140 which is 86MHz.

Standard Interface

Table 4 shows the data mapping scheme for the VESA P&D and FPDI-2 standard for 24-/18-bit per pixel (bpp) 1-pixel/clock input/output TFT and 16-/24-bit input/output DSTN FPD support. The data mapping to the transmitter input is the exact same as the data mapping from the receiver output for color TFT and DSTN FPDs always using only 3 serial data channels. Table 5 shows the data mapping scheme for 2-pixel/clock input/output TFT FPD support. Table 6 shows the data mapping scheme for 1-pixel/clock input to 2-pixel/clock output TFT FPD support. Table 7 shows the data mapping scheme for 2-pixel/clock input to 1-pixel/clock output TFT FPD support. All 1-pixel/clock input or output data mapping schemes are the same. All 2-pixel/clock input or output data mapping schemes are the same. This mapping scheme now allows true inter-operability between various FPMAs and FPDs. This will enable true "plug-and-play", wide market acceptance, new applications, and healthy competition.

The data mapping scheme transmits the RED data on serial data channel 3, the GREEN data on serial data channel 2, and the BLUE data on serial data channel 1 for both 1-pixel/clock and 2-pixel/clock TFT FPDs. This is the same as how analog RGB data is transmitted over three individual channels to the CRT monitor. This is a very logical data mapping scheme already familiar to the market.

Table 4. VESA P&D & FPDI-2 Data Mappings for 24-/18-bpp 1-pixel/clock TFT & 24-/16-bit DSTN Input/Output FPD Support[3]

Transmitter Input				Transmission				Receiver Output			
TFT		DSTN		TFT		DSTN		TFT		DSTN	
24-bpp	18-bpp	24-bit	16-bit	24-bpp	18-bpp	24-bit	16-bit	24-bpp	18-bpp	24-bit	16-bit
R7	R5	LB3						R7	R5	LB3	
R6	R4	LG3						R6	R4	LG3	
R5	R3	LR3						R5	R3	LR3	
R4	R2	UB3		**Serial Channel 3**				R4	R2	UB3	
R3	R1	UG3						R3	R1	UG3	
R2	R0	UR3						R2	R0	UR3	
R1		LB2						R1		LB2	
R0		LG2	SCLK					R0		LG2	SCLK
G7	G5	LR2	LG2					G7	G5	LR2	LG2
G6	G4	UB2	LR2					G6	G4	UB2	LR2
G5	G3	UG2	LB1					G5	G3	UG2	LB1
G4	G2	UR2	LG1	**Serial Channel 2**				G4	G2	UR2	LG1
G3	G1	LB1	UG2					G3	G1	LB1	UG2
G2	G0	LG1	UR2					G2	G0	LG1	UR2
G1		LR1	UB1					G1		LR1	UB1
G0		UB1	UG1					G0		UB1	UG1
B7	B5	UG1	LR1					B7	B5	UG1	LR1
B6	B4	UR1	LB0					B6	B4	UR1	LB0
B5	B3	LB0	LG0					B5	B3	LB0	LG0
B4	B2	LG0	LR0	**Serial Channel 1**				B4	B2	LG0	LR0
B3	B1	LR0	UR1					B3	B1	LR0	UR1
B2	B0	UB0	UB0					B2	B0	UB0	UB0
B1		UG0	UG0					B1		UG0	UG0
B0		UR0	UR0					B0		UR0	UR0

Table 5. PanelLink Technology Data Mappings for Color 24-bpp and 18-bpp 2-pixel/clock TFT Input/Output FPD Support

Transmitter Input		Transmission		Receiver Output	
TFT		TFT		TFT	
2-pixel/clock		2-pixel/clock		2-pixel/clock	
24-bpp	18-bpp	24-bpp	18-bpp	24-bpp	18-bpp
R7-1	R5-1			R7-1	R5-1
R6-1	R4-1			R6-1	R4-1
R5-1	R3-1			R5-1	R3-1
R4-1	R2-1	Serial Channel 3		R4-1	R2-1
R3-1	R1-1			R3-1	R1-1
R2-1	R0-1			R2-1	R0-1
R1-1				R1-1	
R0-1				R0-1	
G7-1	G5-1			G7-1	G5-1
G6-1	G4-1			G6-1	G4-1
G5-1	G3-1			G5-1	G3-1
G4-1	G2-1	Serial Channel 2		G4-1	G2-1
G3-1	G1-1			G3-1	G1-1
G2-1	G0-1			G2-1	G0-1
G1-1				G1-1	
G0-1				G0-1	
B7-1	B5-1			B7-1	B5-1
B6-1	B4-1			B6-1	B4-1
B5-1	B3-1			B5-1	B3-1
B4-1	B2-1	Serial Channel 1		B4-1	B2-1
B3-1	B1-1			B3-1	B1-1
B2-1	B0-1			B2-1	B0-1
B1-1				B1-1	
B0-1				B0-1	
R7-2	R5-2			R7-2	R5-2
R6-2	R4-2			R6-2	R4-2
R5-2	R3-2			R5-2	R3-2
R4-2	R2-2	Serial Channel 3		R4-2	R2-2
R3-2	R1-2			R3-2	R1-2
R2-2	R0-2			R2-2	R0-2
R1-2				R1-2	
R0-2				R0-2	
G7-2	G5-2			G7-2	G5-2
G6-2	G4-2			G6-2	G4-2
G5-2	G3-2			G5-2	G3-2
G4-2	G2-2	Serial Channel 2		G4-2	G2-2
G3-2	G1-2			G3-2	G1-2
G2-2	G0-2			G2-2	G0-2
G1-2				G1-2	
G0-2				G0-2	
B7-2	B5-2			B7-2	B5-2
B6-2	B4-2			B6-2	B4-2
B5-2	B3-2			B5-2	B3-2
B4-2	B2-2	Serial Channel 1		B4-2	B2-2
B3-2	B1-2			B3-2	B1-2
B2-2	B0-2			B2-2	B0-2
B1-2				B1-2	
B0-2				B0-2	

Table 6. `PanelLink` Technology Data Mappings for Color 24-bpp and 18-bpp 1-pixel/clock Input to 2-pixel/clock Output TFT FPD Support

Transmitter Input		**Transmission**		**Receiver Output**	
TFT		**TFT**		**TFT**	
1-pixel/clock		**1-pixel/clock**		**2-pixel/clock**	
24-bpp	**18-bpp**	**24-bpp**	**18-bpp**	**24-bpp**	**18-bpp**
R7	R5			R7-1	R5-1
R6	R4			R6-1	R4-1
R5	R3			R5-1	R3-1
R4	R2	**Serial Channel 3**		R4-1	R2-1
R3	R1			R3-1	R1-1
R2	R0			R2-1	R0-1
R1				R1-1	
R0				R0-1	
G7	G5			G7-1	G5-1
G6	G4			G6-1	G4-1
G5	G3			G5-1	G3-1
G4	G2	**Serial Channel 2**		G4-1	G2-1
G3	G1			G3-1	G1-1
G2	G0			G2-1	G0-1
G1				G1-1	
G0				G0-1	
B7	B5			B7-1	B5-1
B6	B4			B6-1	B4-1
B5	B3			B5-1	B3-1
B4	B2	**Serial Channel 1**		B4-1	B2-1
B3	B1			B3-1	B1-1
B2	B0			B2-1	B0-1
B1				B1-1	
B0				B0-1	
				R7-2	R5-2
				R6-2	R4-2
				R5-2	R3-2
		Serial Channel 3		R4-2	R2-2
				R3-2	R1-2
				R2-2	R0-2
				R1-2	
				R0-2	
				G7-2	G5-2
				G6-2	G4-2
				G5-2	G3-2
		Serial Channel 2		G4-2	G2-2
				G3-2	G1-2
				G2-2	G0-2
				G1-2	
				G0-2	
				B7-2	B5-2
				B6-2	B4-2
				B5-2	B3-2
		Serial Channel 1		B4-2	B2-2
				B3-2	B1-2
				B2-2	B0-2
				B1-2	
				B0-2	

Table 7. `PanelLink` Technology Data Mappings for Color 24-bpp and 18-bpp 2-pixel/clock Input to 1-pixel/clock Output TFT FPD Support

Transmitter Input		Transmission		Receiver Output	
TFT		TFT		TFT	
2-pixel/clock		2-pixel/clock		1-pixel/clock	
24-bpp	18-bpp	24-bpp	18-bpp	24-bpp	18-bpp
R7-1	R5-1			R7	R5-1
R6-1	R4-1			R6	R4-1
R5-1	R3-1			R5	R3-1
R4-1	R2-1	Serial Channel 3		R4	R2-1
R3-1	R1-1			R3	R1-1
R2-1	R0-1			R2	R0-1
R1-1				R1	
R0-1				R0	
G7-1	G5-1			G7	G5-1
G6-1	G4-1			G6	G4-1
G5-1	G3-1			G5	G3-1
G4-1	G2-1	Serial Channel 2		G4	G2-1
G3-1	G1-1			G3	G1-1
G2-1	G0-1			G2	G0-1
G1-1				G1	
G0-1				G0	
B7-1	B5-1			B7	B5-1
B6-1	B4-1			B6	B4-1
B5-1	B3-1			B5	B3-1
B4-1	B2-1	Serial Channel 1		B4	B2-1
B3-1	B1-1			B3	B1-1
B2-1	B0-1			B2	B0-1
B1-1				B1	
B0-1				B0	
R7-2	R5-2				
R6-2	R4-2				
R5-2	R3-2				
R4-2	R2-2	Serial Channel 3			
R3-2	R1-2				
R2-2	R0-2				
R1-2					
R0-2					
G7-2	G5-2				
G6-2	G4-2				
G5-2	G3-2				
G4-2	G2-2	Serial Channel 2			
G3-2	G1-2				
G2-2	G0-2				
G1-2					
G0-2					
B7-2	B5-2				
B6-2	B4-2				
B5-2	B3-2				
B4-2	B2-2	Serial Channel 1			
B3-2	B1-2				
B2-2	B0-2				
B1-2					
B0-2					

Integration

To meet the demands of the PC market, PanelLink Technology is manufactured using cost effective standard CMOS process technology. This allows PanelLink Technology to be easily integrated into FPMA and FPD controllers. This integration helps reduce EMI by eliminating the wide high speed parallel data bus from the FPMA and transmitter as well as from the receiver to the FPD controller. Integration will also reduce cost by eliminating components.

An important benefit of integrating the receiver into the FPD controller is that it can be made "Intelligent". More functions and programmability can now be implemented allowing FPD manufacturers to differentiate their panels with rich features. This will also reduce development cycles of the FPD manufacturer of new FPDs, which will in turn reduce total cost.

In the near future, some features that could be implemented through integration in an Intelligent FPD controller are bi-directionality, USB and P1394 interfaces, precise gamma correction, and better display quality for passive DSTN and large size active TFT FPDs. Figure 1 shows what the future FPD monitor could be with an Intelligent FPD controller.

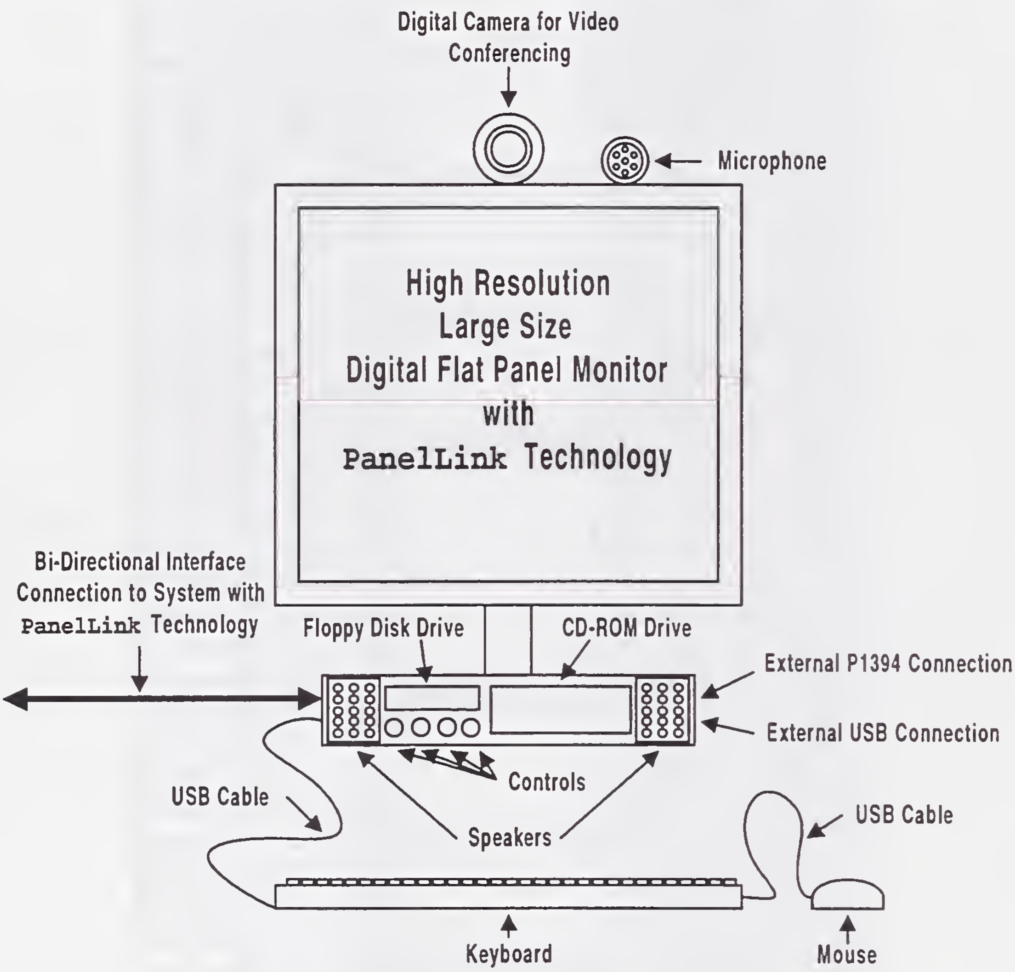


Figure 1. Possible Future Intelligent FPD Monitor

With a "Bi-directional Intelligent FPD Interface Controller", the FPD monitor now becomes an intelligent terminal. The keyboard, mouse, speaker, and microphone can be connected via the USB port of the Intelligent FPD Interface Controller. Optional USB devices can also be connected via an external USB connector. The video camera, FDD, and CD-ROM can be connected via the P1394 port of the Intelligent FPD Controller. Optional P1394 devices can also be connected via an external P1394 connector. The main server is located elsewhere and connected via the new bi-directional high speed serial interface. There is no need for an expensive PC motherboard with CPU, Memory, Graphics controller, and HDD. The Intelligent Monitor now becomes the true low cost NetPC, Network PC, Web Browser, Set-Top Box, etc. of the future.

VESA TMDS Applications

A. High Refresh and Reduced Blanking Support

From Tables 1, 2 and 3 above; it clearly shows that with VESA P&D TMDS, the following can be supported with the current specified operating frequencies :

Table 8. Refresh Rates Supported of Various Resolutions with VESA P&D TMDS Specified Frequencies

SiI Part #	VGA		SVGA		XGA		SXGA		UXGA	
	VESA Timings		VESA Timings		VESA Timings		VESA Timings		VESA Timings	
	Normal CRT Timings w/ Max. Blanking Times	GTF Timings w/ Min. Blanking Times	Normal CRT Timings w/ Max. Blanking Times	GTF Timings w/ Min. Blanking Times	Normal CRT Timings w/ Max. Blanking Times	GTF Timings w/ Min. Blanking Times	Normal CRT Timings w/ Max. Blanking Times	GTF Timings w/ Min. Blanking Times	Normal CRT Timings w/ Max. Blanking Times	GTF Timings w/ Min. Blanking Times
100/101	> 80Hz	> 80Hz	> 80Hz	> 80Hz	< 62Hz	> 80Hz	NA	NA	NA	NA
140/141	> 80Hz	> 80Hz	> 80Hz	> 80Hz	< 79Hz	> 80Hz	NA	< 63Hz	NA	NA
150/151	> 80Hz	> 80Hz	> 80Hz	> 80Hz	> 80Hz	> 80Hz	< 62Hz	> 80Hz	NA	< 56Hz

From Tables 1, 2 and 3 above; it clearly shows that with VESA P&D TMDS, the following can be supported with the current lab tested operating frequencies :

Table 9. Refresh Rates Supported of Various Resolutions with VESA P&D TMDS Lab Tested Frequencies

SiI Part #	VGA		SVGA		XGA		SXGA		UXGA	
	VESA Timings		VESA Timings		VESA Timings		VESA Timings		VESA Timings	
	Normal CRT Timings w/ Max. Blanking Times	GTF Timings w/ Min. Blanking Times	Normal CRT Timings w/ Max. Blanking Times	GTF Timings w/ Min. Blanking Times	Normal CRT Timings w/ Max. Blanking Times	GTF Timings w/ Min. Blanking Times	Normal CRT Timings w/ Max. Blanking Times	GTF Timings w/ Min. Blanking Times	Normal CRT Timings w/ Max. Blanking Times	GTF Timings w/ Min. Blanking Times
100/101	> 80Hz	> 80Hz	> 80Hz	> 80Hz	< 79Hz	> 80Hz	NA	< 64Hz	NA	NA
140/141	> 80Hz	> 80Hz	> 80Hz	> 80Hz	> 80Hz	> 80Hz	< 56Hz	< 75Hz	NA	< 51Hz
150/151	> 80Hz	> 80Hz	> 80Hz	> 80Hz	> 80Hz	> 80Hz	< 76Hz	> 80Hz	< 50Hz	< 68Hz

The market is already very familiar with the fact that a higher refresh rate produces a better display on the CRT monitor. This is due to the characteristic of the CRT. TFTs do not have the same characteristic and a higher refresh rate will not necessarily produce a better display on the TFT monitor. But since the market is already very familiar with higher refresh rate producing a better display, the FPD monitor manufacturer must be able to support higher refresh to satisfy the market. In this way, the FPD monitor manufacturer does not have to educate the market that TFT monitors require only 60Hz refresh, and a higher refresh rate will not necessarily produce a better display like that of CRT monitors.

Being able to support higher refresh rate also allows support for the newer higher refresh DSTN panels. These high refresh DSTN panels have been advertised as having response times coming close to that of TFT panels, so having higher refresh support will produce a better display on higher refresh DSTN monitors.

VESA P&D TMDS allows FPD monitor manufacturers to support a wide variety of FPD monitors (VGA to UXGA) with a wide variety of refresh rates (with normal or reduced blanking) using a wide variety of FPD technologies (TFT, normal refresh DSTN, high refresh DSTN, etc.).

B. Analog Multimedia Accelerator and FPD Projection Support

Currently, the majority of FPD monitors are used with existing Analog CRT Multimedia Accelerators like how CRT monitors are used as shown in Figure 2. This is because there is a large installed base of Analog CRT Multimedia Accelerators in the market. This means that the interface of the FPD monitor is analog RGB and multi-sync frequency. Unfortunately, an FPD is digital and fixed frequency. Therefore, there must be some kind of analog-to-digital as well as multi-sync frequency-to-fixed frequency conversion support. These conversion logic resides on the FPD monitor side and is custom designed by each FPD monitor manufacturer. The display quality is highly dependent upon the quality of the custom conversion logic. Usually, the better the display the more expensive the conversion logic since better quality chips are used. Figure 4 shows a block diagram of what could be on this custom conversion logic module. All of these statements also holds true for the FPD projector market. Figure 3 shows a similar connection as in Figure 2 using a notebook computer and a digital FPD projector.

If the conversion logic was removed from the FPD monitor and placed on the driving system side as shown in Figure 5, it would offer tremendous benefits. A few of the major benefits would be (1) the FPD monitor manufacturer now has to only support one interface - digital VESA P&D TMDS, to support both analog and digital markets. (2) Display quality could be improved by moving the conversion logic closer to the source and transmitting the data digitally via VESA P&D TMDS. (3) EMI could be reduced by moving the high frequency conversion logic to the system side where it could be better shielded. (4) The conversion logic can become an add-in card on the driving system side. This will drive down costs tremendously with many add-in card manufacturers offering this type of conversion add-in card. (5) All of these benefits will, in the end, lower the FPD monitor costs and open up new markets.

If, instead of having the conversion logic on an add-in card, if a module was implemented instead, then this conversion logic module could be used for the digital FPD projector market as well. Having both an add-in card and a module version of the conversion logic would give customers tremendous choice allowing them to choose either using their existing Analog CRT Multimedia Accelerator or using a Digital FPMA. This will allow FPD monitor manufacturers to enter new markets with new applications. This is described more in the following sections.

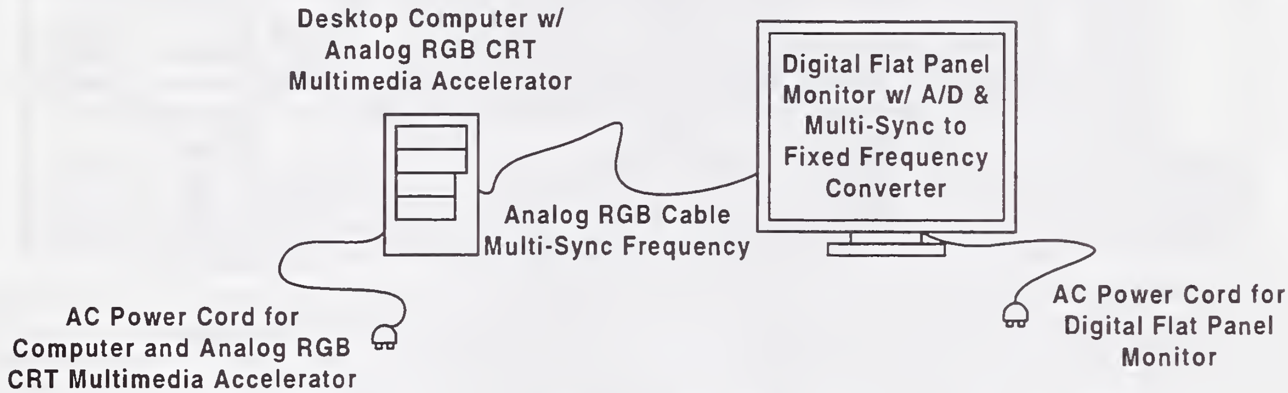


Figure 2. Digital FPD Monitor Connection with an Analog CRT Multimedia Accelerator

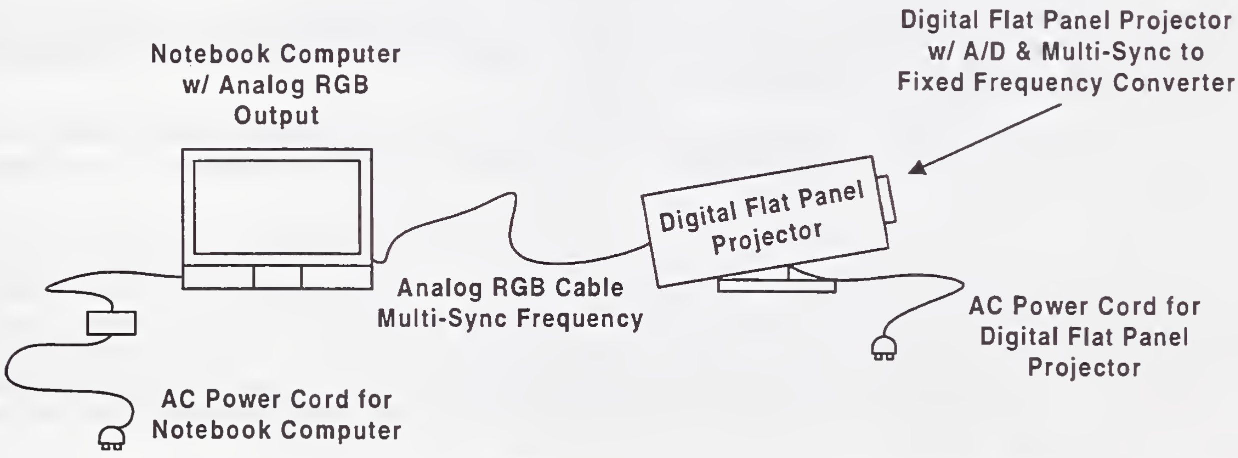


Figure 3. Digital FPD Projector Connection with an Analog Multi-Sync Frequency RGB Output from a Notebook

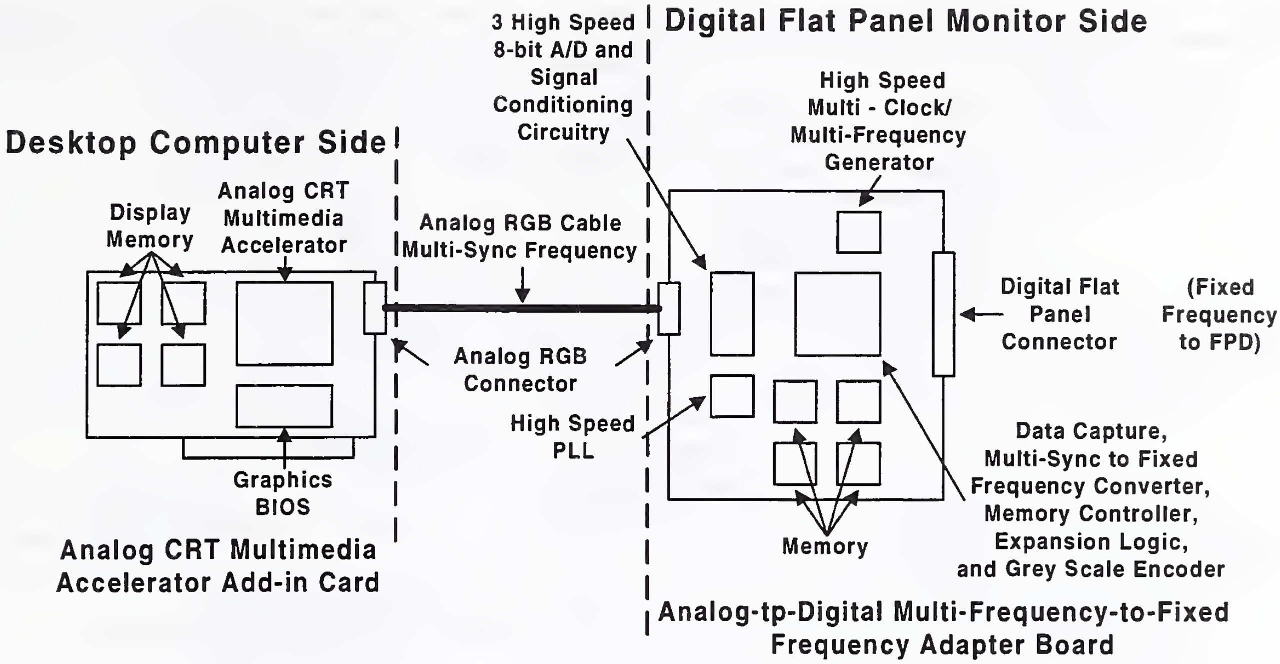


Figure 4. Block Diagram of Digital FPD Monitor Connection w/ Analog CRT Multimedia Accelerator

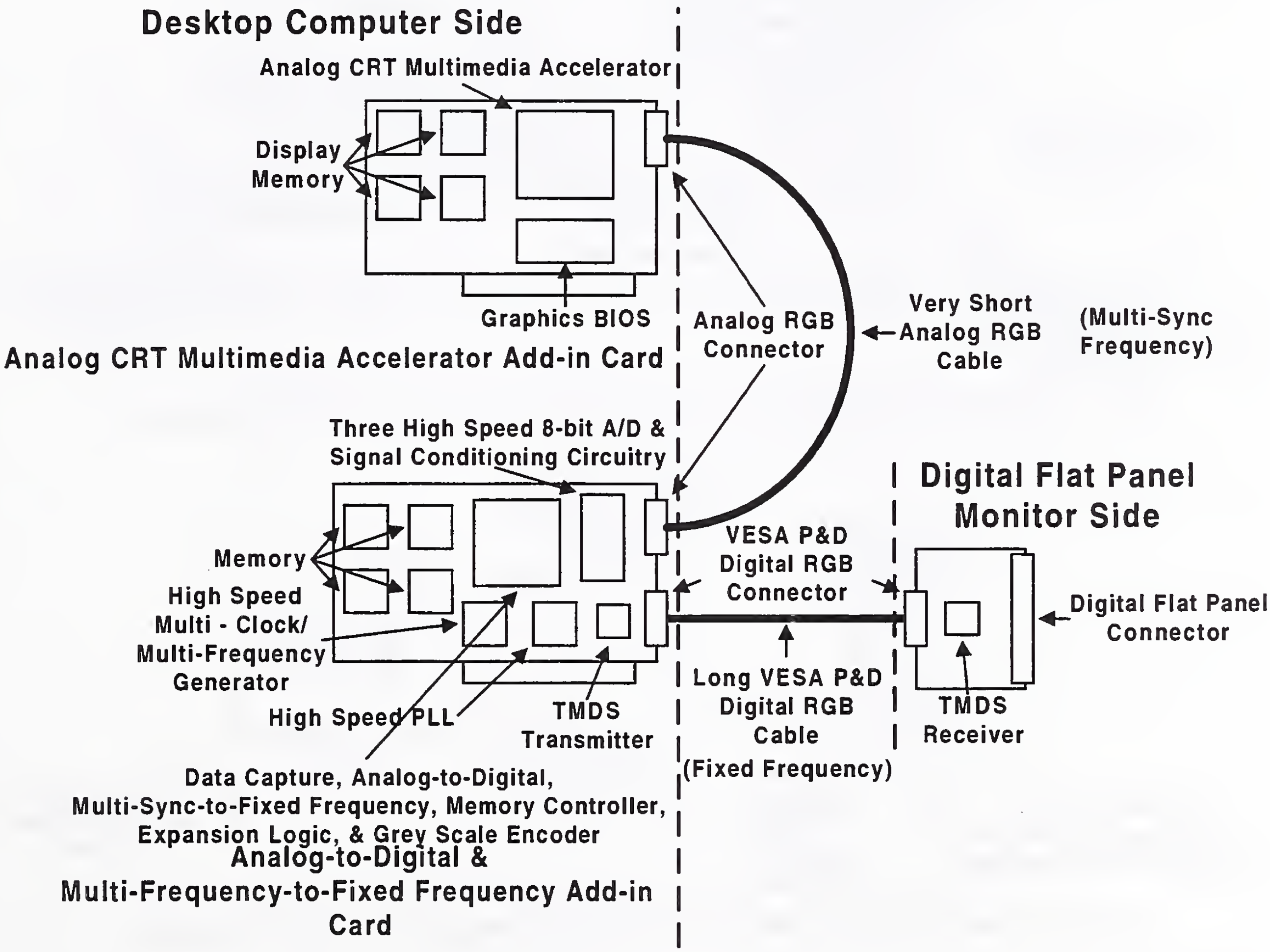


Figure 5. Block Diagram of Analog-to-Digital and Multi-Frequency-to-Fixed Frequency Conversion Logic Module Moved to Driving System Side as an Add-in Card using VESA P&D TMDS

Figures 6 - 10 shows a few examples of some implementations of the one digital VESA P&D TMDS interface that supports both Analog CRT and Digital Flat Panel Multimedia Accelerators.

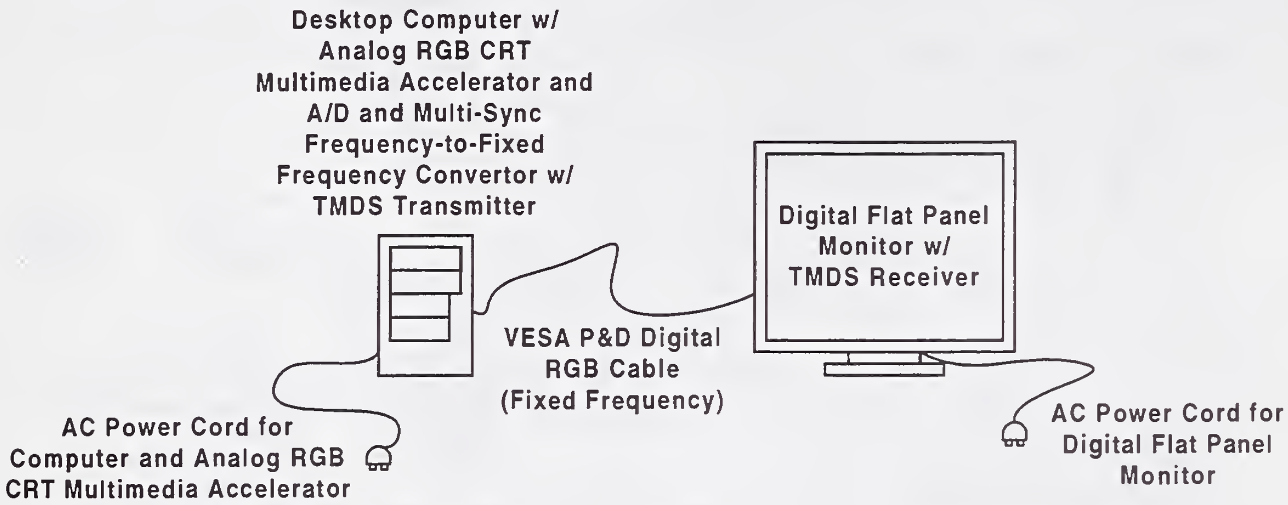


Figure 6. Digital VESA P&D TMDS FPD Monitor with an Analog CRT Multimedia Accelerator

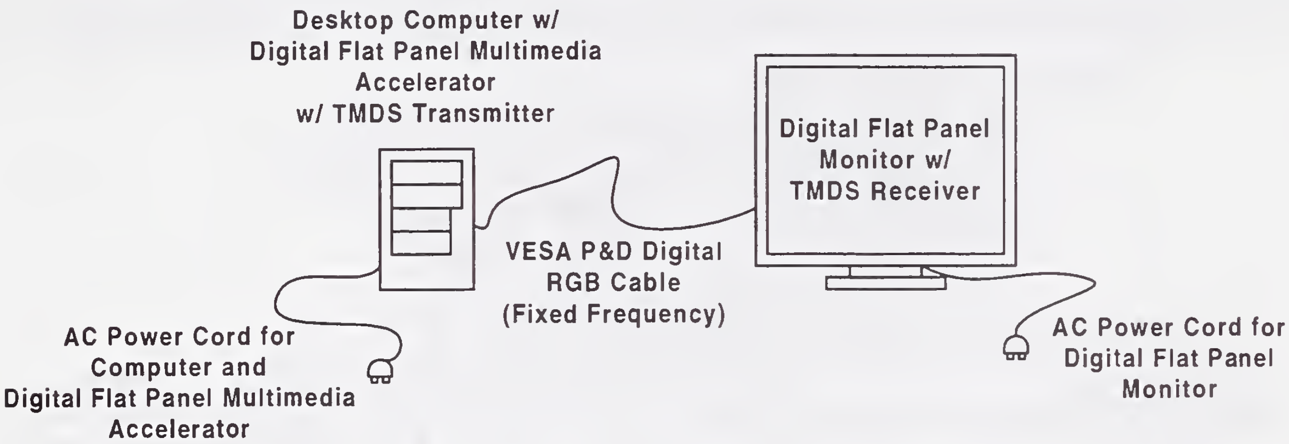


Figure 7. Digital VESA P&D TMDS FPD Monitor with Digital Flat Panel Multimedia Accelerator

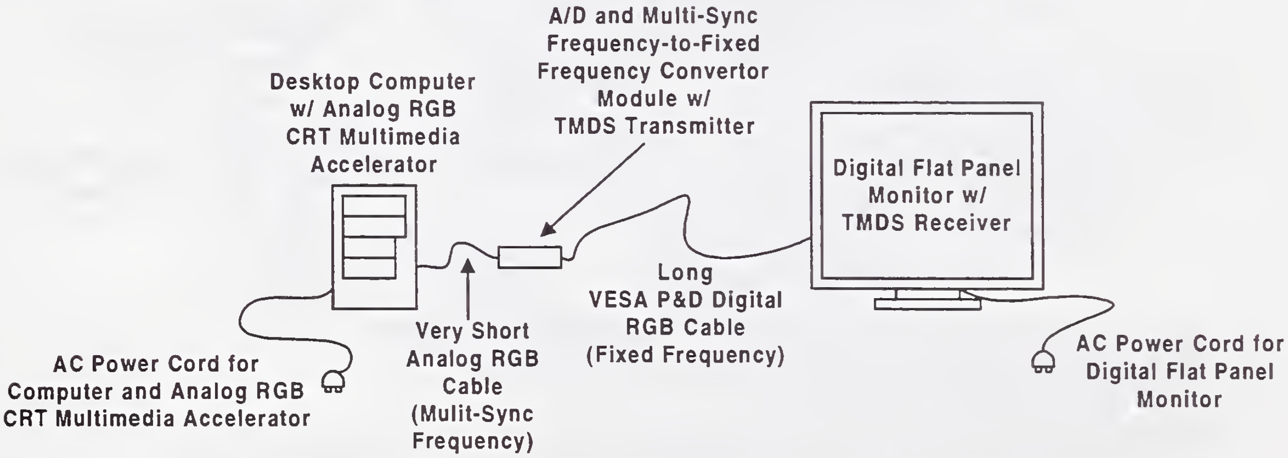


Figure 8. Digital VESA P&D TMDS FPD Monitor with Analog CRT Multimedia Accelerator

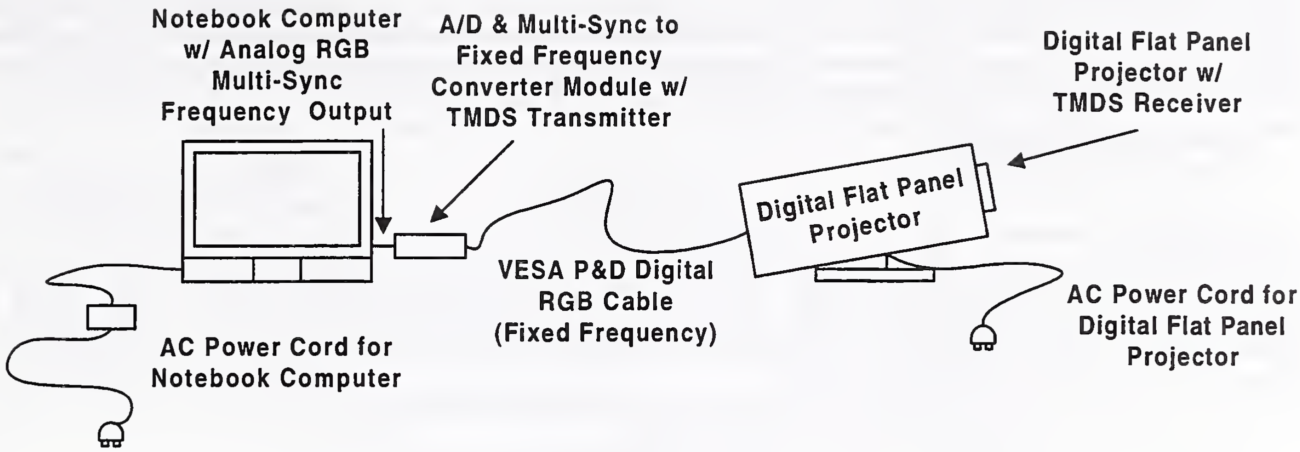


Figure 9. Digital FPD Projector with an Analog Multi-Sync Frequency RGB Output with a Notebook

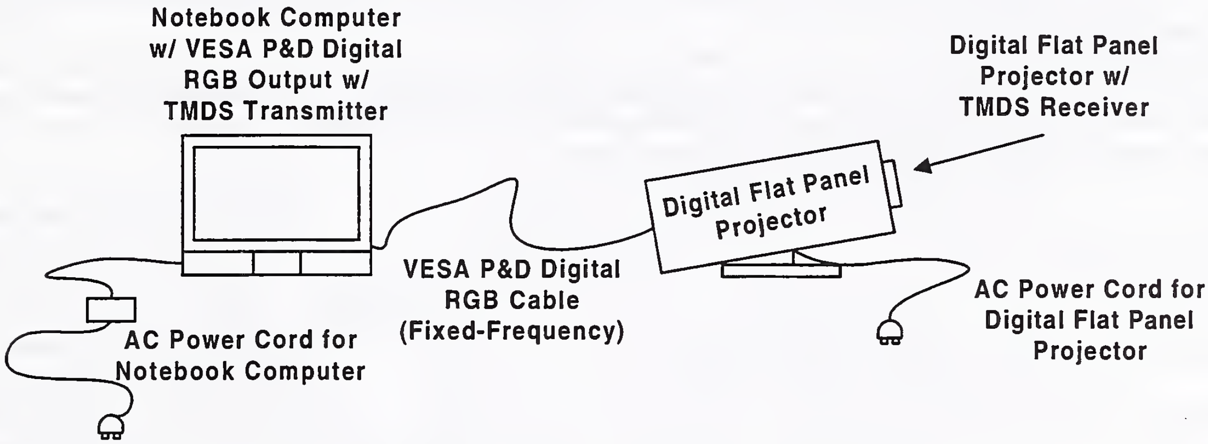


Figure 10. Digital FPD Projector with Digital FPD RGB Output with a Notebook

C. Long Distance Copper Cable Support

VESA P&D TMDS can support copper cables up to 10m. If there are some applications that require further distance support, then a simple TMDS repeater can be built every 10m until the desired distance is achieved. An example of an application of this is Point of Sales (POS). Figure 11 shows a block diagram of a 20m distance support. Longer distances can be supported with additional TMDS repeaters, which could theoretically produce infinite distance support.

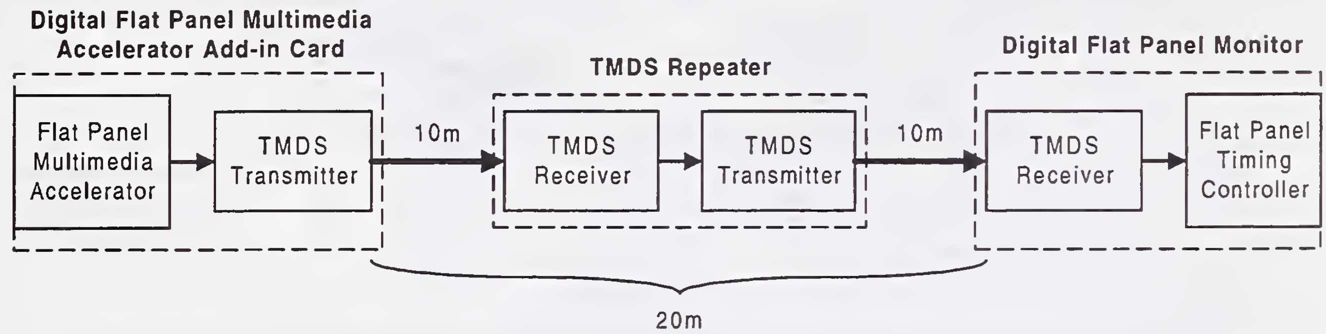


Figure 11. Block Diagram of TMDS Repeater Application for Very Long Distance Using Copper Cables

D. One-to-Many Support

Most applications of FPD monitors are single unit applications. There are some applications that require more than a single unit FPD monitor. An example of this could be board conference room where each person has an individual FPD monitor to view. There could also be a projection of the image being viewed on the individual FPD monitors for presentations. Figure 12 shows a block diagram of a one to 4 FPD monitor and 1 projection system.

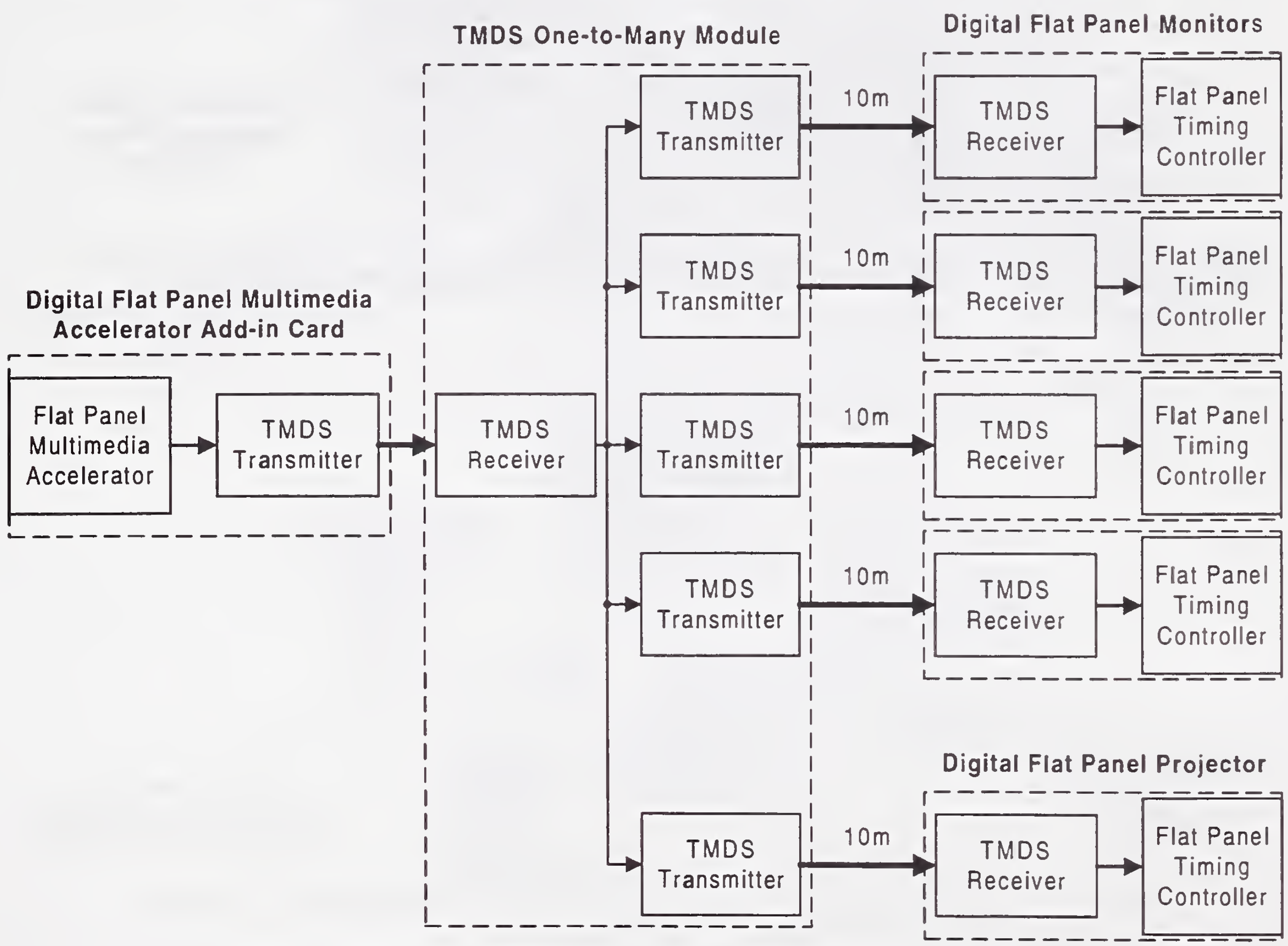


Figure 12. VESA P&D TMDS One-to-Many Application using Copper Cables

E. Fiber-Optic Support

VESA P&D TMDS can support copper cables up to 10m. If there are some applications that require very long distance support, then a fiber-optic transmitter/receiver link can be directly connected to TMDS transmitter/receiver. No additional logic is required to interface TMDS to a fiber-optic. TMDS has been tested up to 500m with a fiber-optic link. This is shown in Figure 13. The distance limit for a single fiber-optic link is set by the limitations of the fiber-optic link itself. For longer distances, the above TMDS repeater used in conjunction with a fiber-optic link could theoretically produce an infinite fiber-optic distance support.

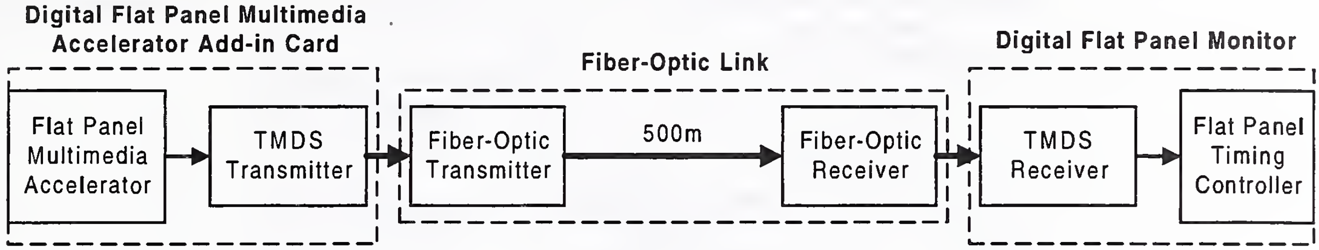


Figure 13. 500m VESA P&D TMDS Fiber-Optic Application

With a fiber-optic splitter, the above mentioned concept of One-to-Many FPD can also be accomplished. This is shown in Figure 14.

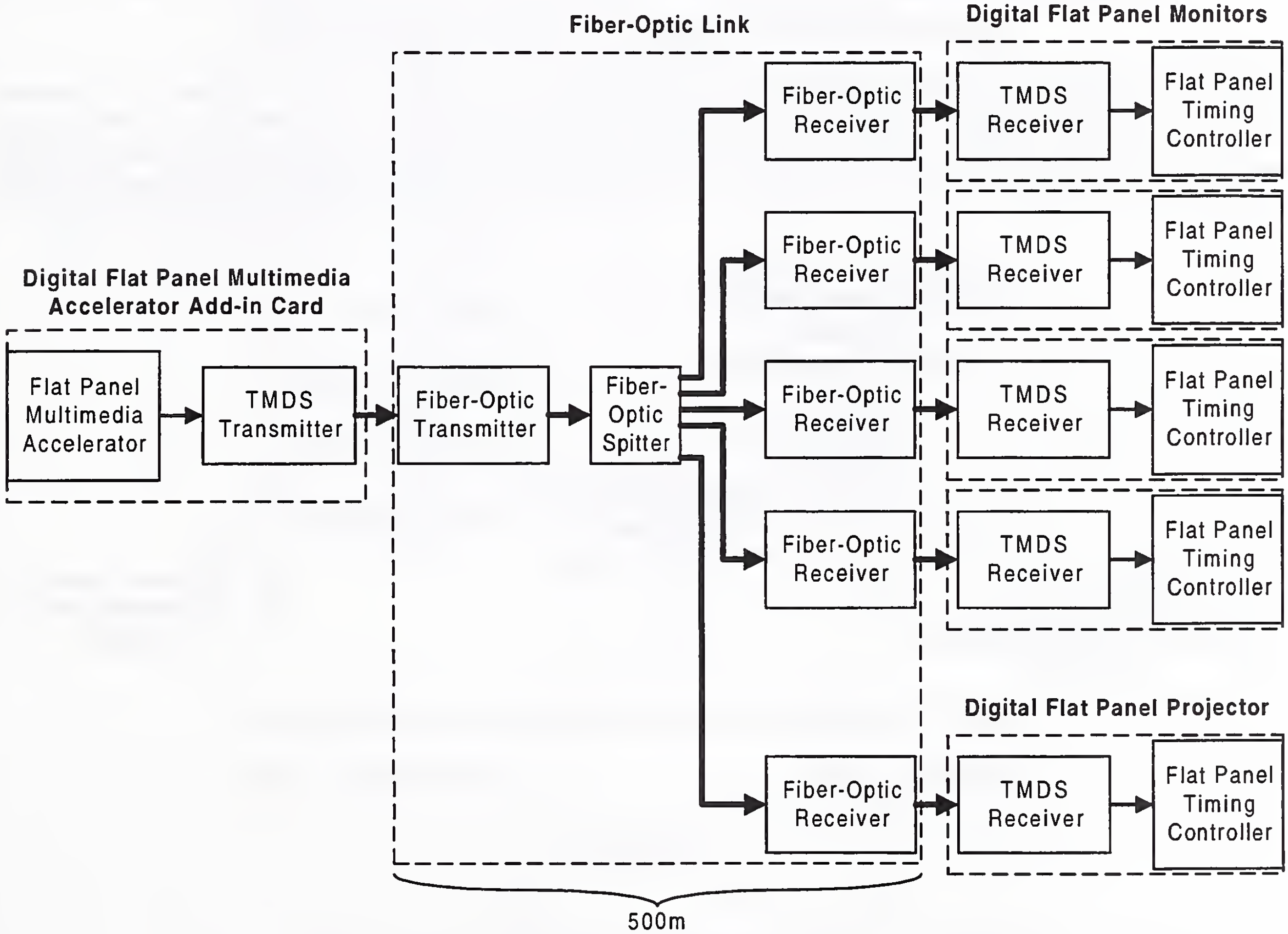


Figure 14. 500m Fiber-Optic with VESA P&D TMDS using Fiber-Optic Splitter for One-to-Many Application

F. Remote Terminal with Shared and Separate Power Supply Support

Some applications of FPD monitors use one power supply. The power from the computer system is used to power the FPD monitor as well through the interconnect cable. They share one power supply. As shown in Figure 15. In this application, the TMDS transmitter is connected directly to the TMDS receiver. TMDS allows the voltage margin to be +/-10% VCC in this application.

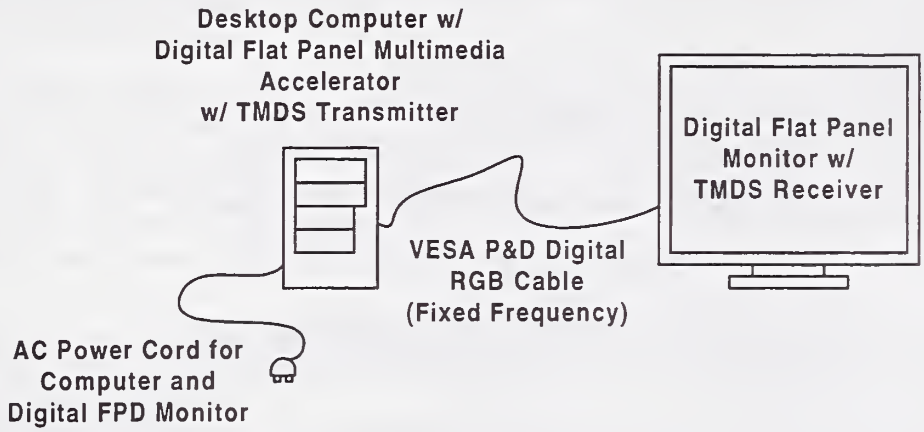


Figure 15. Single Power Supply for Both Computer and FPD Monitor

In some other applications, the FPD monitor has its own separate power supply source, as shown in Figure 16. The computer and FPD monitor have separate power supplies. In this application, the TMDS transmitter is connected to the TMDS receiver via capacitor-coupling as shown in Figure 17. TMDS allows the voltage margin to be +/-10% VCC of the individual power supplies. This translates into a total VCC margin of +/-20%, as an example +10% on the computer VCC and -10% on the FPD monitor VCC.

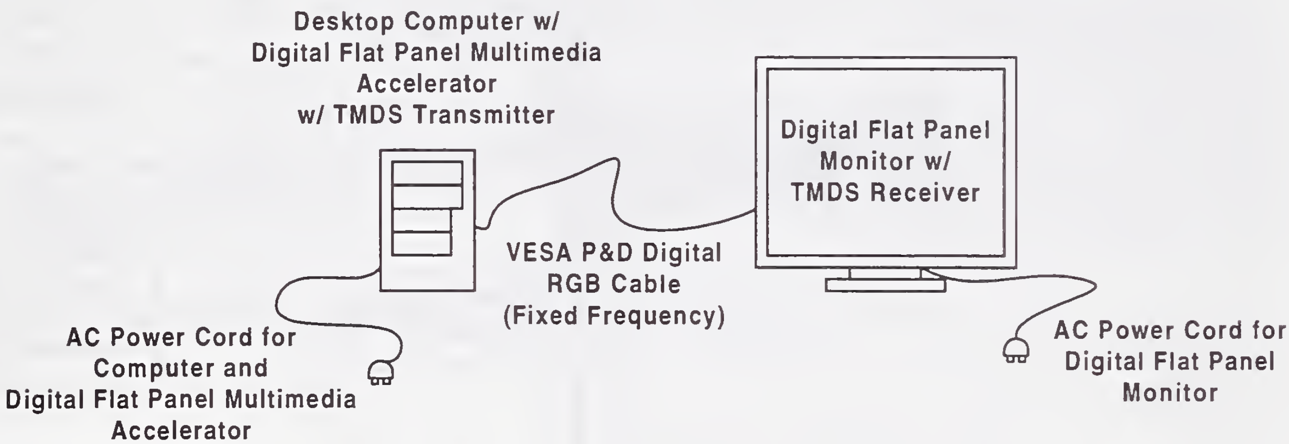


Figure 16. Separate Power Supplies for Computer and FPD Monitor

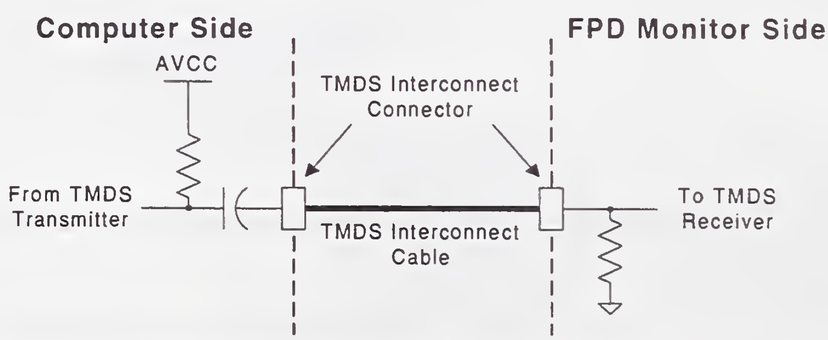


Figure 17. TMDS Capacitor Coupling for Separate Power Supply Applications

Conclusion

A single, simple, scaleable, logical, and standard interface that spans VGA to UXGA resolutions and beyond, and supports various FPD technologies is the ideal interface that will accelerate the FPD monitor, notebook, and embedded markets. This interface that incorporates all of the above mentioned major features - reliable, scaleable, and integrateable - is the interface of choice. It is the VESA P&D standard, which is based on the features and architecture of `PanelLink` Technology (TMDS). It now allows manufacturers to design FPD systems with confidence knowing that the interface will remain constant through various technology and performance generations. It provides true inter-operability which will enable new applications and wide market acceptance.

Chips & Technologies, Trident Microsystems, Cirrus Logic, and LG have all licensed the transmitter to be integrated into their respective FPMAs. Silicon Image has integrated the receiver into the FPD controller to produce an Intelligent FPD controller.

Chips & Technologies and Hyundai have signed on as alternate sources of the discrete transmitter/receiver products.

References :

1. *VESA CRT Monitor Timing Specification*
2. *VESA GTF Timing Proposal*
3. *VESA P&D Specification and FPDI-2 Proposal*

AMP

AMPSLIM™ 1.25 MM CONNECTOR

for the

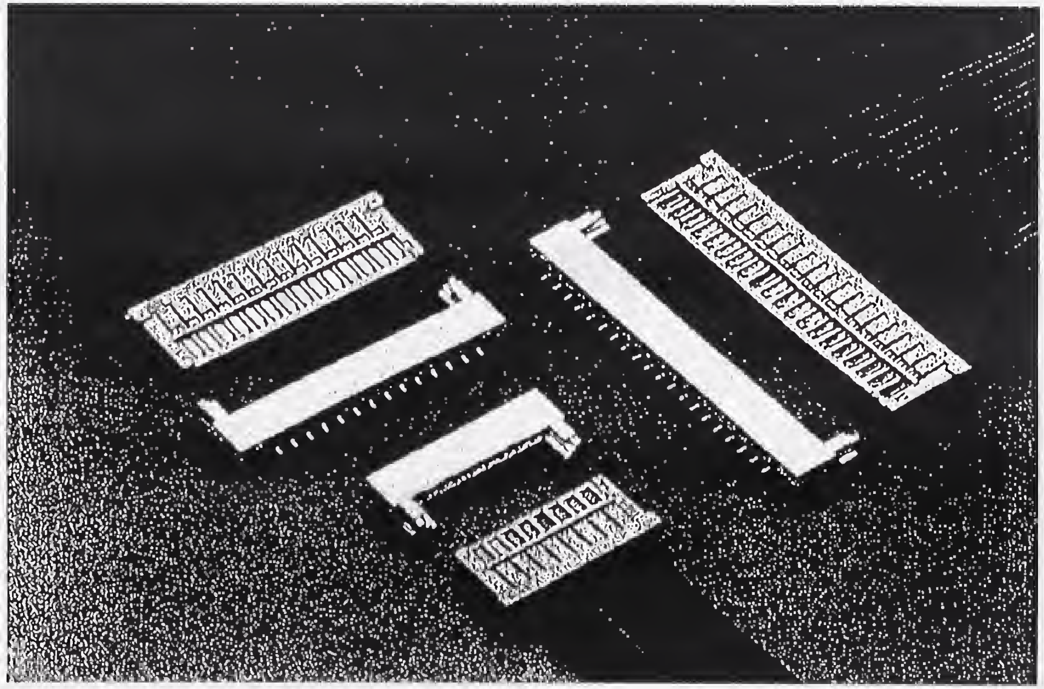
VESA FPDI-2 · Flat Panel Display Interconnect Standard

10/97

HIGHLIGHTS OF THE AMPSLIM CONNECTOR SYSTEM

Position Sizes 20 and 8 for the FPDI-2 Standard

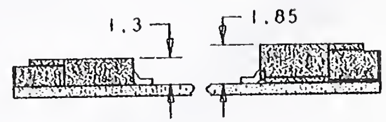
- Low Profile
- Light Weight
- Cost Effective
- Reliable
- Scaleable
- High Performance
- Available
- Offered as an Open Interface for this Standard



Position Sizes 8, 14, and 20 Shown

PRODUCT FEATURES AND BENEFITS

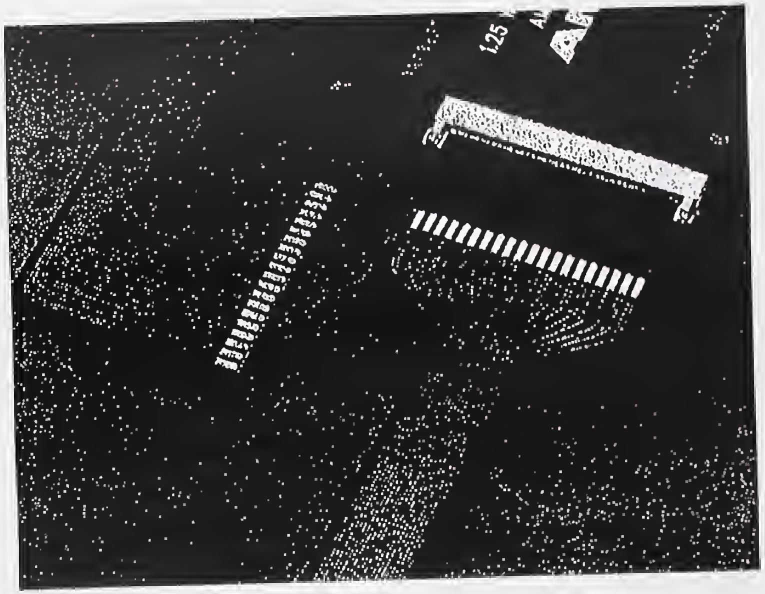
AMPSlim 1.25 mm Wire to Board Connector for the VESA FPDI-2 Standard



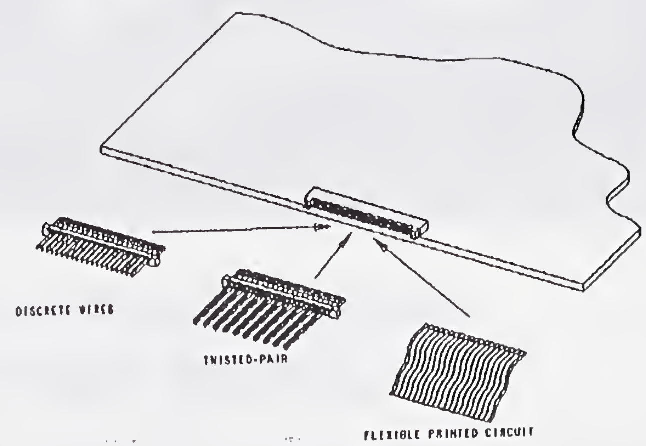
- **Low Profile** Connector Minimizes Signal Path And Right Angle Transitions Providing Exceptional Electrical Performance. Near Zero Skew Due To The Single-Row Design, Short Connector Length And Low Profile Height
  - Ultra-low Profile Offset Mount Has a Height of Only 1.30 mm
  - Horizontal Mount Has a Profile Height of 1.85 mm
- Very Light Weight, Low Mass Connector System **Stays Mated** During Shock and Vibration -- Total Weight per Connector Set Is about ½ Gram
- **Cost Effective** Tin Interface Design Meets the Flat Panel Interconnection Needs of Today's Systems with the Flexibility to use the Same Interface on Tomorrow's High Performance Systems
- **High Reliability** of the Separable Interface Is Provided by the High Normal Force, Tin-plated Contact Design. Issues of Fretting Corrosion Due to Vibration or Micro-motion at the Separable Interface Are Addressed by this Design
- **Uniquely Compatible with Flexible Printed Circuits** Which Plug Directly Into the Board Mounted Receptacle -- A Plug Connector is Not Needed

PRODUCT FEATURES AND BENEFITS

AMPSlim 1.25 mm Wire to Board Connector for the VESA FPDI-2 Standard



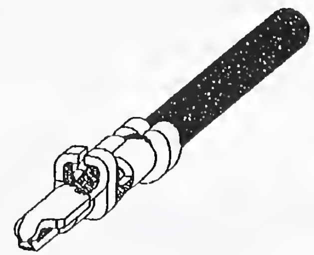
- **Unique Receptacle Connector**
  Permits the Interconnection of Flat Panels with Either:
  ❶ Discrete Wires,
  ❷ Twisted Pair Wires, or
  ❸ Flexible Printed Circuits



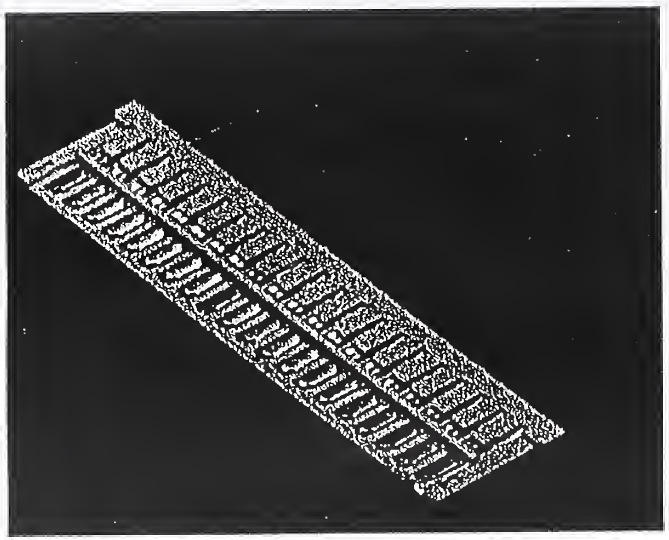
PRODUCT FEATURES AND BENEFITS

AMPSlim 1.25 mm Wire to Board Connector for the VESA FPDI-2 Standard

Cable Connectors



- Rugged Tab Contact, Is Applied to the Wire, **Endures Handling and Insertion Forces**
- Designed for **Fast and Easy Application** of Crimp-snap Style Contacts to Twisted Pair or Discrete Wires Using AMP's High Speed Applicators



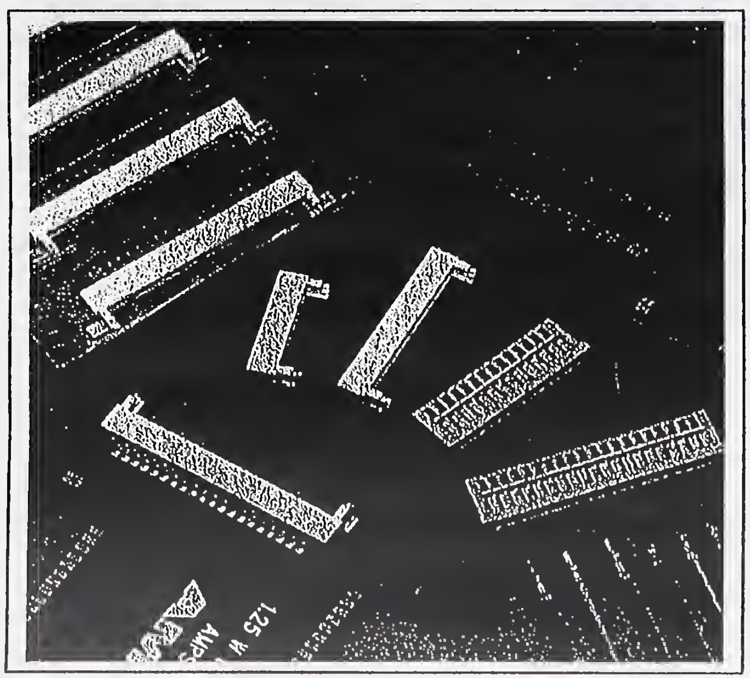
- Accommodates **Wide Wire Range** of #28 to #32 AWG Wires with Insulation Diameters of 0.45 mm to 0.92 mm
- **Very Stable Mating Interface** Is Provided by the Rugged Tab Contact Which Is Surrounded by Plastic, Allowing for Flexing of Cable
- Proper Mating Is Signaled by Both **Visual and Tactile Feedback** Features

PRODUCT FEATURES AND BENEFITS

AMPSlim 1.25 mm Wire to Board Connector for the VESA FPDI-2 Standard

Board Connectors (Horizontal and Offset Mount Designs)

- Unique Design **Permits FPC to Be Mated Directly** to the Receptacle Connector Without the Use of a Plug Connector, Thereby Reducing Costs by Eliminating the Second Connector and the Associated Handling and Processing Costs



- Board Mounted Product Is **Compatible with Hand Placement** for Fast and Easy Prototyping and **Packaged for High Speed** Pick-and-place Equipment for Your High Volume Production Needs

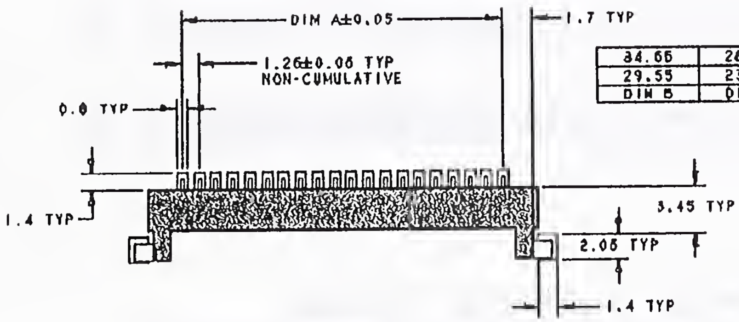
- Surface Mount Design, Utilizing Only One Side of the Circuit Board **Minimizes Board Space** and **Requires No Holes** in the Circuit Board,

- **Solderable Hold-downs** Retain the Connector During Mating and Unmating

Circuit Board Illustrations

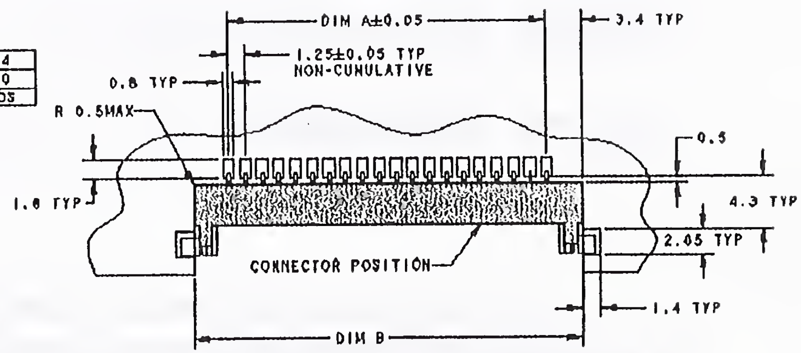
AMPSlim 1.25 mm Wire to Board Connector for the VESA FPDI-2 Standard

❖ **Skew is virtually zero** due to the single-row design, low profile height, and short connector length.



Horizontal Mount

34.66	28.75	24
29.55	23.75	20
DIM B	DIM A	POS



Offset Mount

Mechanical Performance Requirements

AMPSlim 1.25 mm Wire to Board Connector for the VESA FPDI-2 Standard

- Connector Mating Force (20 Position) .... 39 N, max — EIA-364-13A
- Connector Unmating Force (20 Position) .... 7.8 N, min — EIA-364-13A
- Physical Shock .... 50 G's — EIA-364-27A Condition A
- Vibration, Low Frequency .... 10-50-10 Hz — EIA-364-28A Condition I
- Durability (Tin interface) .... 30 cycles, min — EIA-364-09A

ELECTRICAL PERFORMANCE REQUIREMENTS

AMPSlim 1.25 mm Wire to Board Connector for the VESA FPDI-2 Standard

- Voltage Rating .... 30 vac EIA-364-13A
- Current Rating w/#28 AWG Wire .... 1.5 Amp
- Dielectric Withstanding Voltage .... 500 V, min EIA-364-20A
- Insulation Resistance .... 500 megohms, min EIA-364-21A
- Contact Resistance .... 30 milliohms, max EIA-364-23A

Environmental Performance Requirements

AMPSlim 1.25 mm Wire to Board Connector for the VESA FPDI-2 Standard

- Operating Temperature Range .... - 30°C to +85°C
- Thermal Shock .... 5 cycles, - 55°C and 85°C EIA-364-32A
- Humidity, Steady State .... 40°C at 90-95% RH for 96 Hours EIA-364-31A Method I, Condition B
- Mixed Flowing Gas .... Environmental Class III, 20 Days
- Temperature Life .... 85°C for 96 Hours EIA-364-17 Method 1005

Proposed AMPSlim Connector Pin-out

AMPSlim 1.25 mm Wire to Board Connector for the VESA FPDI-2 Standard

20 POSITION CONNECTOR

PIN #	DESCRIPTION
1	VCONTRAST
2	+5 VDC
3	DDC Clock
4	DCC Data
5	VDD2
6	VDD1
7	Ground/VDD Return
8	Ground/VDD Return
9	TMDS Data 2 +
10	TMDS Data 2 -
11	TMDS Data 2 Shield
12	TMDS Data 1 +
13	TMDS Data 1 -
14	TMDS Data 1 Shield
15	TMDS Data 0 +
16	TMDS Data 0 -
17	TMDS Data 0 Shield
18	TMDS Clock +
19	TMDS Clock -
20	TMDS Clock Shield

Notes: The differential pairs for the data clock and TMDS links each have an isolated return line. These return lines are also isolated from each other.

OPTIONAL 8 POSITION CONNECTOR

PIN #	DESCRIPTION
1	VSYNC_OUT (from TMDS Rx)
2	HSYNC_OUT (from TMDS Rx)
3	TIMINGVALID
4	Stereo Sync (TMDS Control Bit 3)
5	CTL2 (TMDS Control Bit 2)
6	CTL1 (TMDS Control Bit 1)
7	Ground/+ 12 VDC Return
8	+ 12 VDC

Notes: Optional connector for FPD customization and added functionality needed for desktop monitor applications.

SUMMARY

The AMPSlim 1.25 mm Wire to Board Connector Provides:

- Single-Row High Performance Connector System Which Exceeds The Critical VESA Performance Requirements For Applications Using TMDS
- Low Profile Height And Light Weight Required For Notebook Display Systems
- Cost Effective Solution For Both Low And High Performance Systems Using Twisted-Pair Wires Or FPC
- Provides System Manufacturer With Numerous Interconnection And Cabling Options To Fit Demanding Packaging Requirements.
- Easily Scaleable To Other Sizes And Configurations For Future VESA Requirements Associated With XGA And Other High Resolution Graphics Enhancements
- Tooled Product, Available Now
- Open Interface Standard

VESA's selection of this connector system not only provides industry with a standard interface for XGA systems, but is applicable to SXGA systems, with room for future performance requirements.

AMPSlim Contacts

AMPSlim 1.25 mm Wire to Board Connector for the VESA FPDI-2 Standard

CONTACT	E-MAIL	VOICE	FAX
Engineering **Earl Myers**	emyers@amp.com	717-592-4819	717-592-5266
Product Manager **Joseph Byouk**	jrbyouk@amp.com	704-824-6343	704-824-6268
Standards **Larry Kopp**	lskopp@amp.com	717-592-6267	717-592-6179

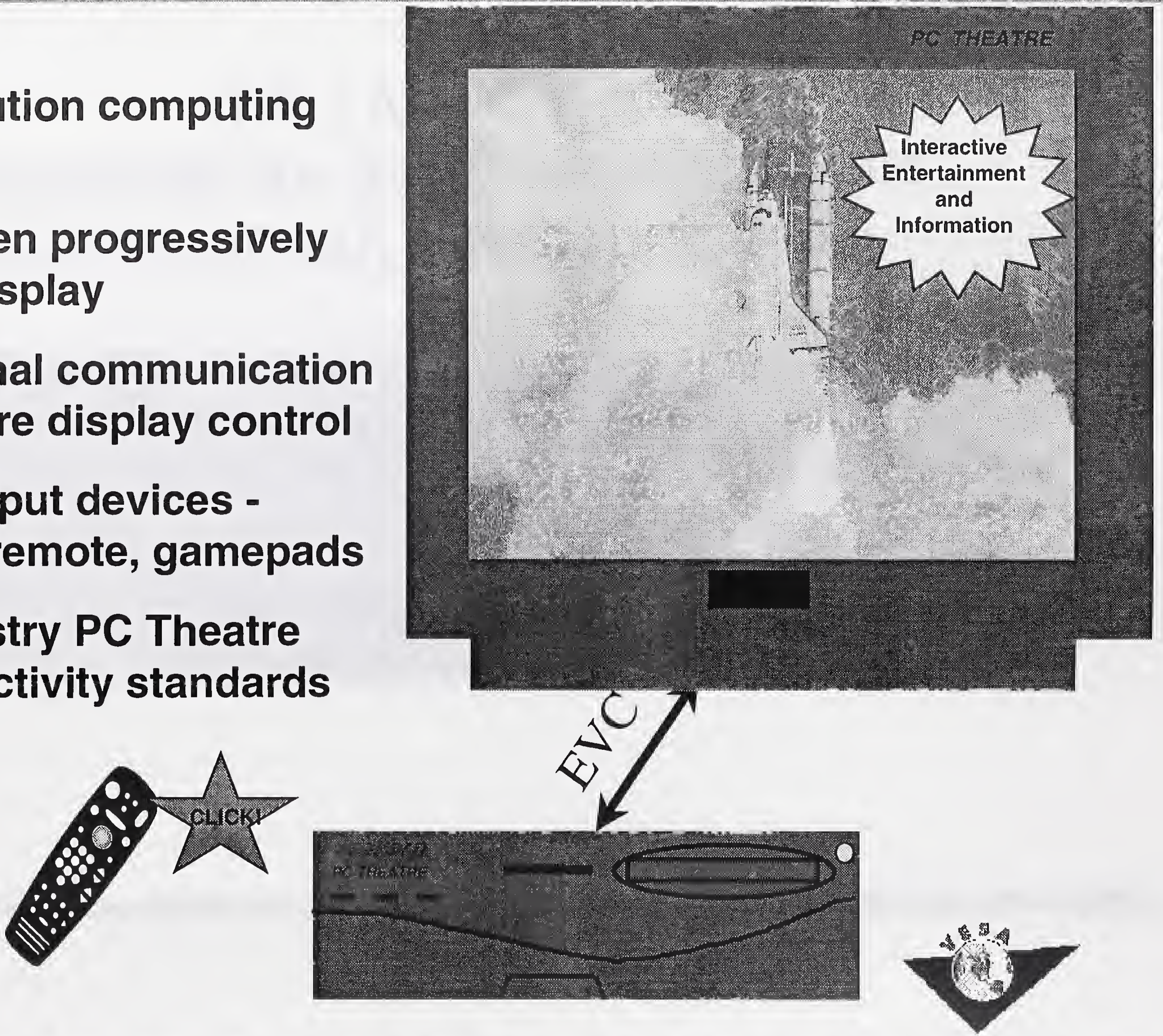
PC Theatre Initiative

Open Industry Interconnectivity Standards for the Convergence of the TV and PC

VESA

PC Theatre Interconnect Vision

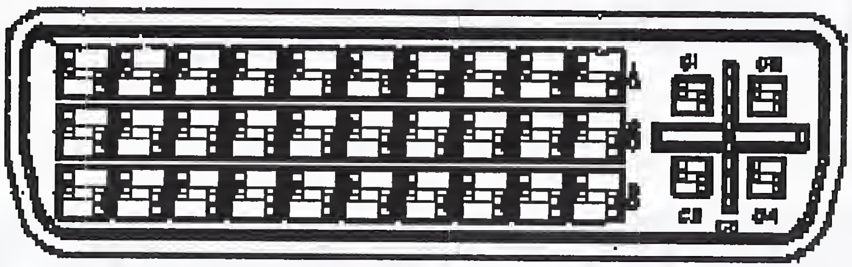
- High resolution computing device
- Large screen progressively scanned display
- Bi-directional communication and software display control
- Wireless input devices - keyboard, remote, gamepads
- Open industry PC Theatre interconnectivity standards



PC Theatre Interface Proposal Overview

The PC and display use the VESA Plug and Display (P&D) connector

- Connector supports RGB, PanelLink, Pixel clock, 1394, USB, and DDC
- Single cable between PC and Display
- PC Theatre products must provide adapter cable if P&D connector is not used



The PC and display support two different viewing modes

- PC Mode - configured for the display of PC graphics
- TV Mode - configured for the display of TV video
- Video enhancements can be used to improve TV video quality, or make it more like that of a standard TV (overscan, VSM, white peaking)

PC Theatre Interface Proposal Overview

USB supported in the PC and display

- Bi-directional to support display control and sending user input (front button panel, IR receiver) to the PC for processing
- VESA Monitor Control Command Set (MCCS) standard defines display control commands
- USB HID Monitor Control Class Definition for display control
- USB Audio Class Definition for audio control
- USB HID Usage Tables for IR receiver and front button panel communication

PC Theatre Interface Proposal Overview

The PC and display support VESA Display Data Channel (DDC-2B) and Extended Display Identification Data (EDID) standards

- PC uses EDID to identify the capabilities of the display
- Support EDID Version 1.0, Revision 1, with Version 2.0 as an option
- Compatible with standard PCs and monitors

PC Theatre Interface Proposal Overview

The PC and display support VESA Display Power Management Signaling (DPMS) standard

- PC uses DPMS to control display's power state using H and V sync lines
- PC Supports all states (On, Standby, Suspend, Active-Off)
- Display must provide minimum support (On, Active-Off), but full support recommended
- Compatibility with standard PCs and monitors

PC Theatre Interface Proposal Overview

User input (remote, keyboard, gamepads, display front button panel) is passed to the PC for processing

- PC and display act as one system
- Common user interface generated by the PC, with optional support of display user interface
- Display can support stand-alone and slave modes

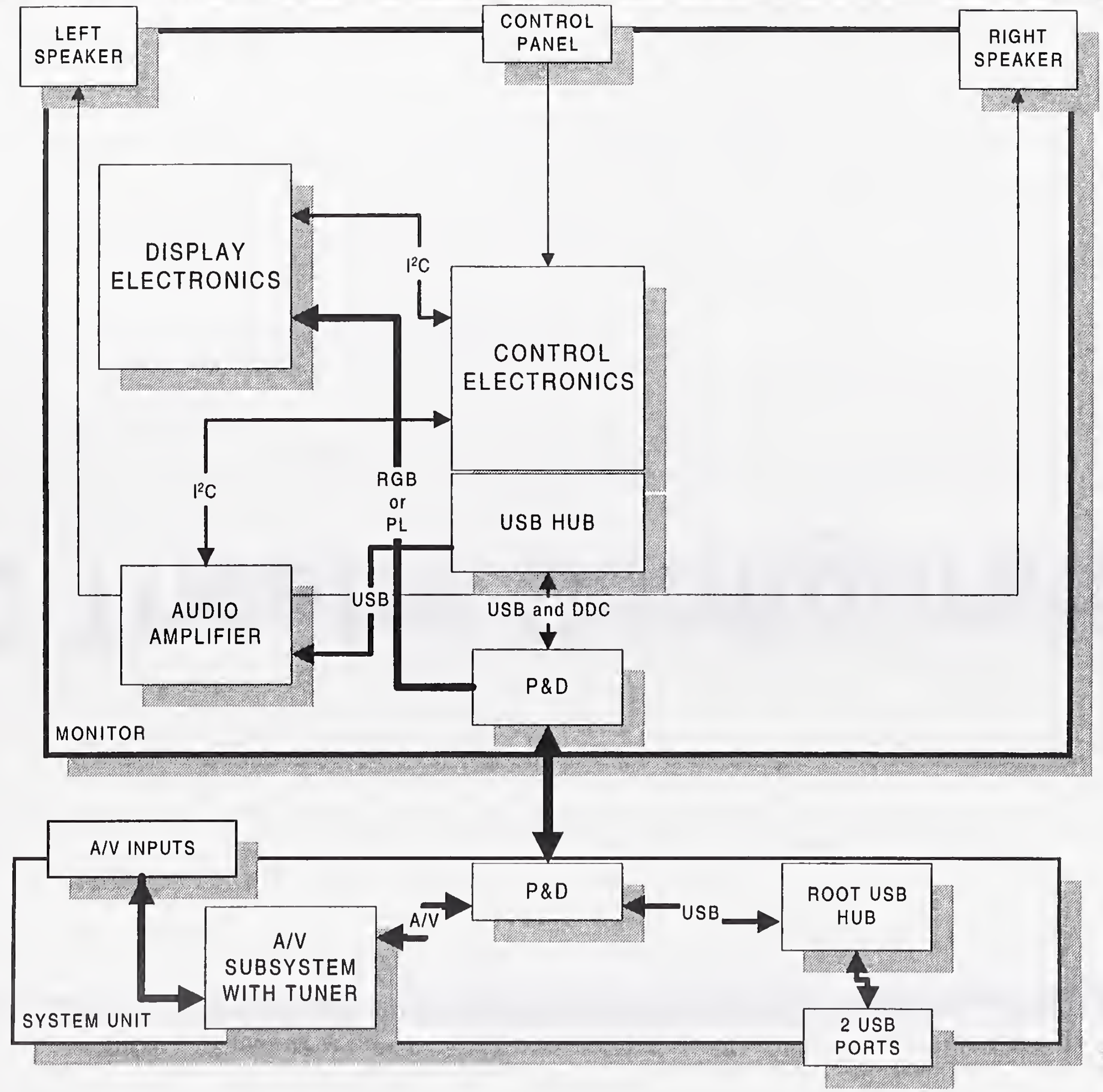
PC Theatre Interface Proposal Overview

Basic operation is standardized

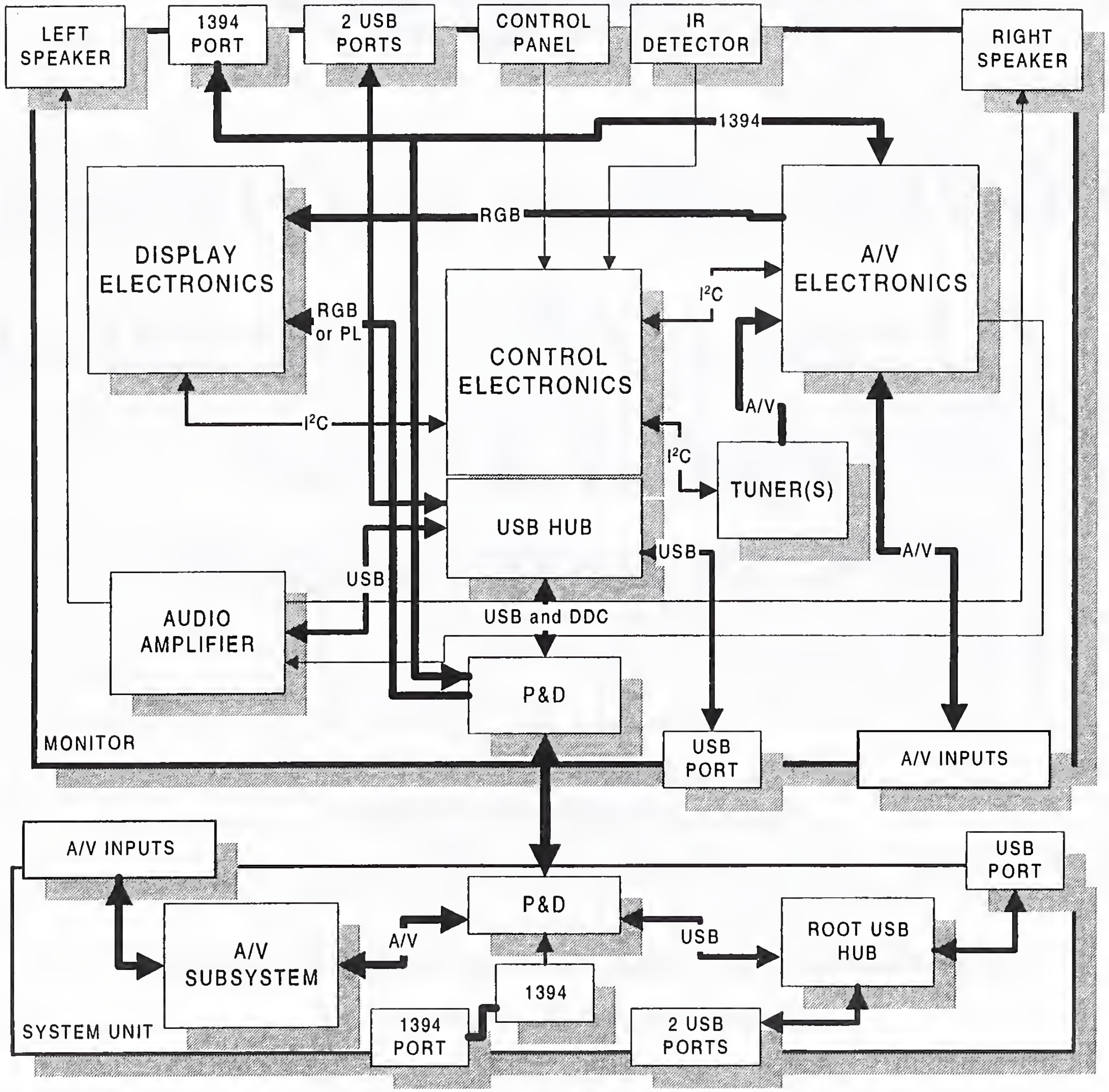
- Insure compatibility
- Enable PC to share display's resources
  - Tuner
  - Remote
  - Front button panel
  - Rear connector panel
- Improve customer understanding and acceptance

PC Theatre Configuration

PC Theatre System with Minimum Support



PC Theatre System with Full Support



NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY

ADVANCED TECHNOLOGY PROGRAM

Introduction to the Advanced Technology Program (ATP)

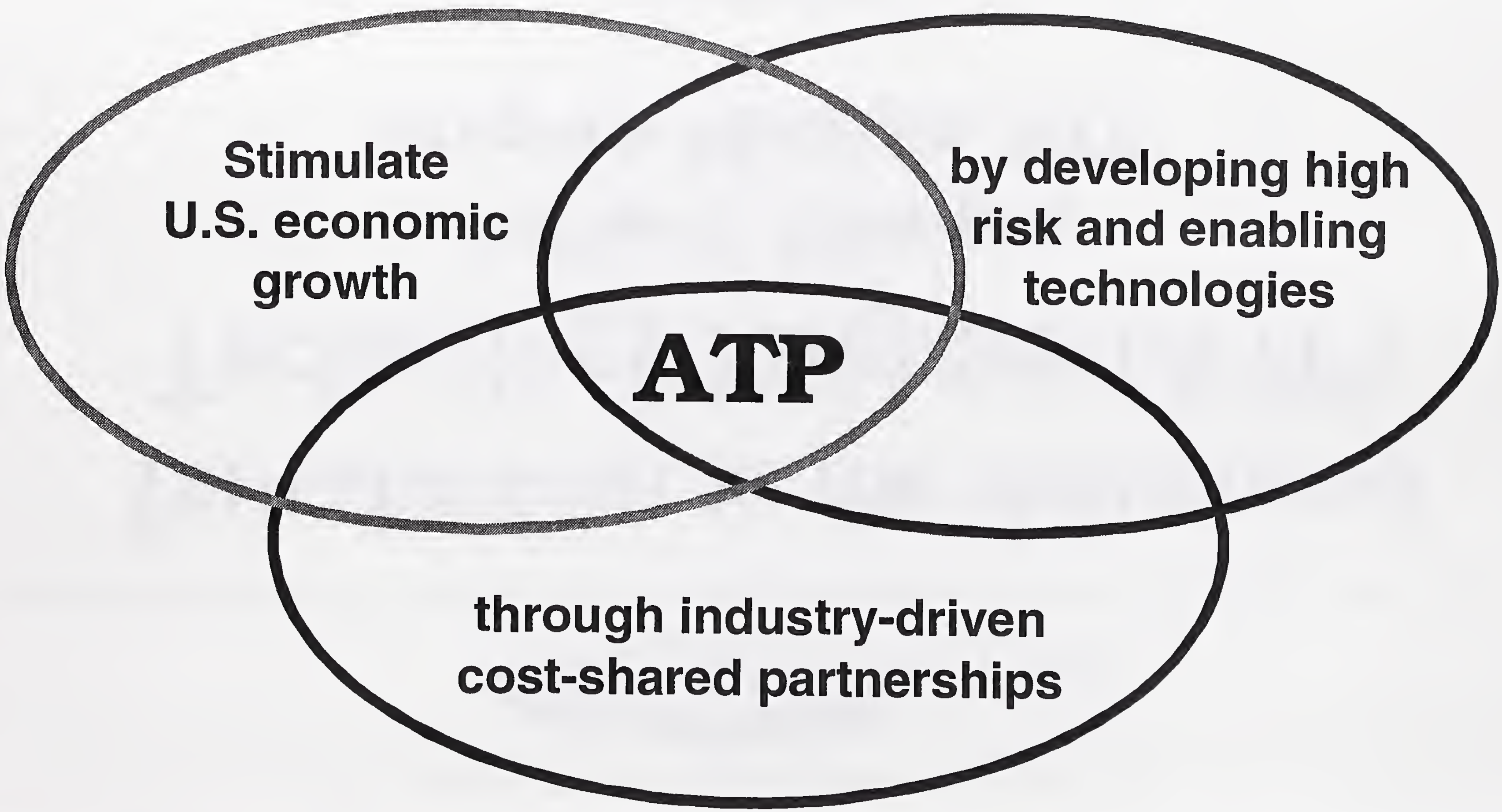
Carlos E. Grinspon

Program Manager, ATP

Tel: 301-975-4448
Fax: 301-926-9524
E-mail: carlos.grinspon@nist.gov
URL: www.atp.gov

National Institute of Standards and Technology
Technology Administration
U.S. Department of Commerce

ATP Mission


Stimulate U.S. economic growth
by developing high risk and enabling technologies
ATP
through industry-driven cost-shared partnerships

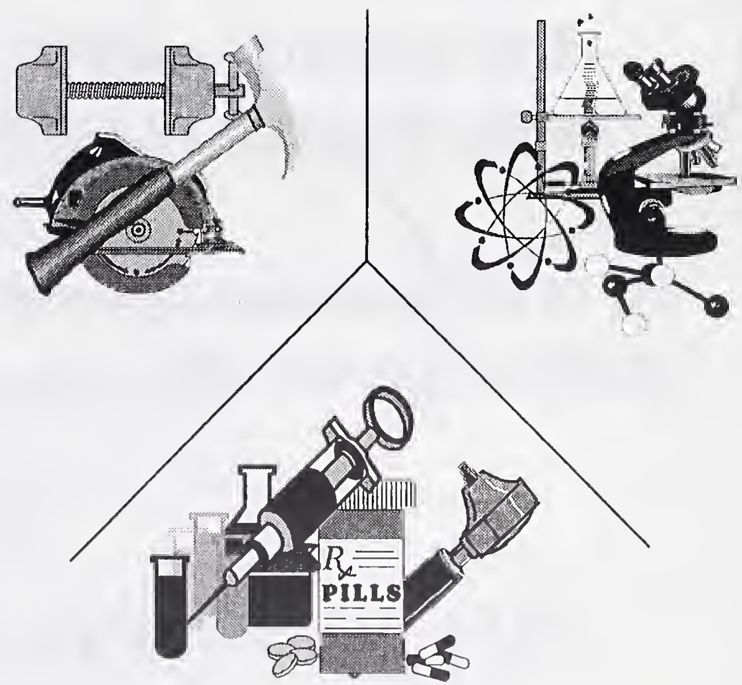
Basic Characteristics of the ATP

- Unique mission focus - high risk, high-payoff projects likely to stimulate economic growth, but unlikely to be undertaken without cost sharing
- Partnership with industry - industry proposes ideas for projects and programs, manages projects, cost-shares with NIST
- Published selection criteria (factors include both technical merit and credibility of business plans)
- Built-in sunset provisions
- Extensive rigorous peer review
- Rigorous project and program impact assessment underway, preliminary results are encouraging
- General competitions plus focused programs

Two Ways to Participate in ATP

- **General Competitions** (Open to all technologies/ industries

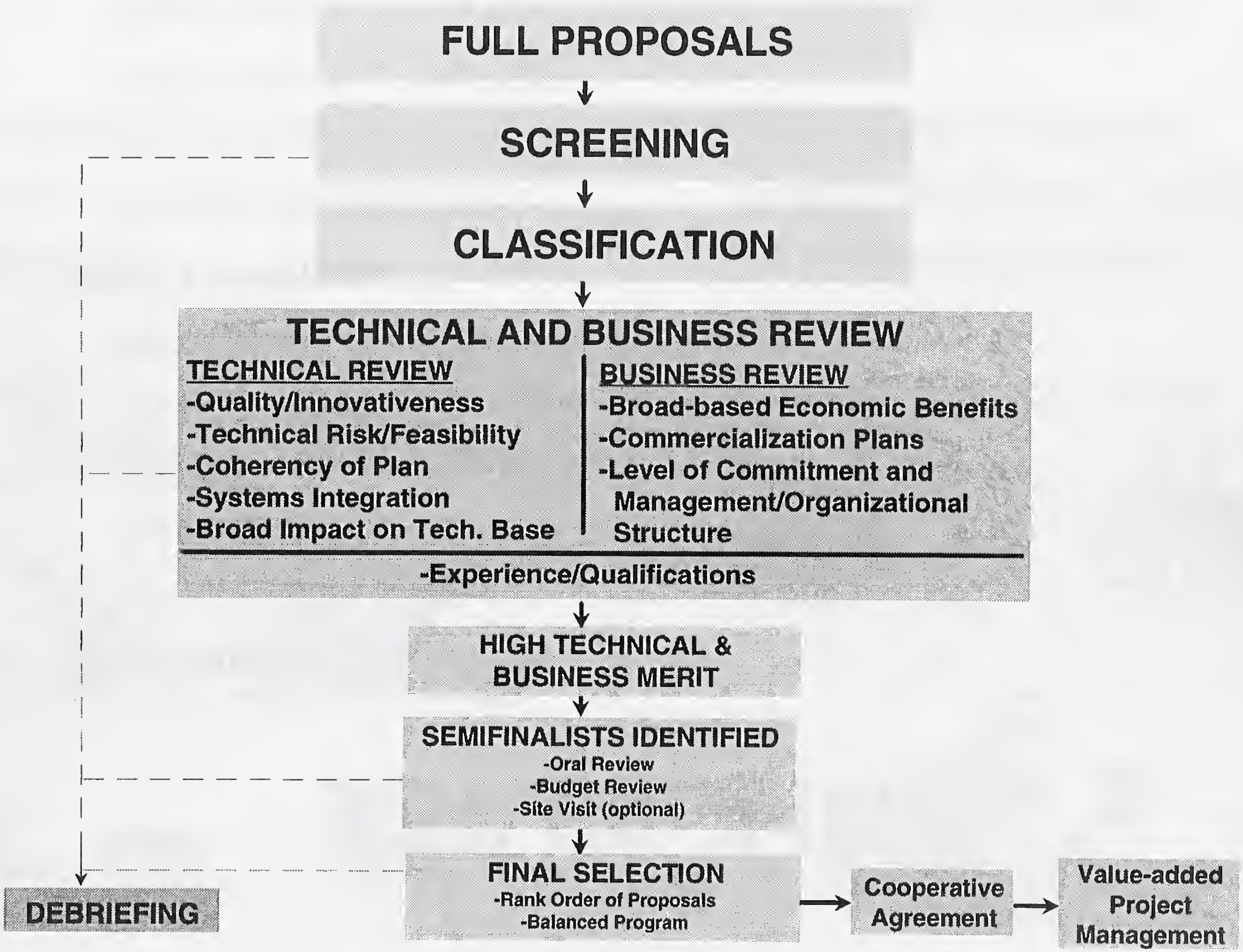
- **Focused Program Competitions** (Clusters of related projects



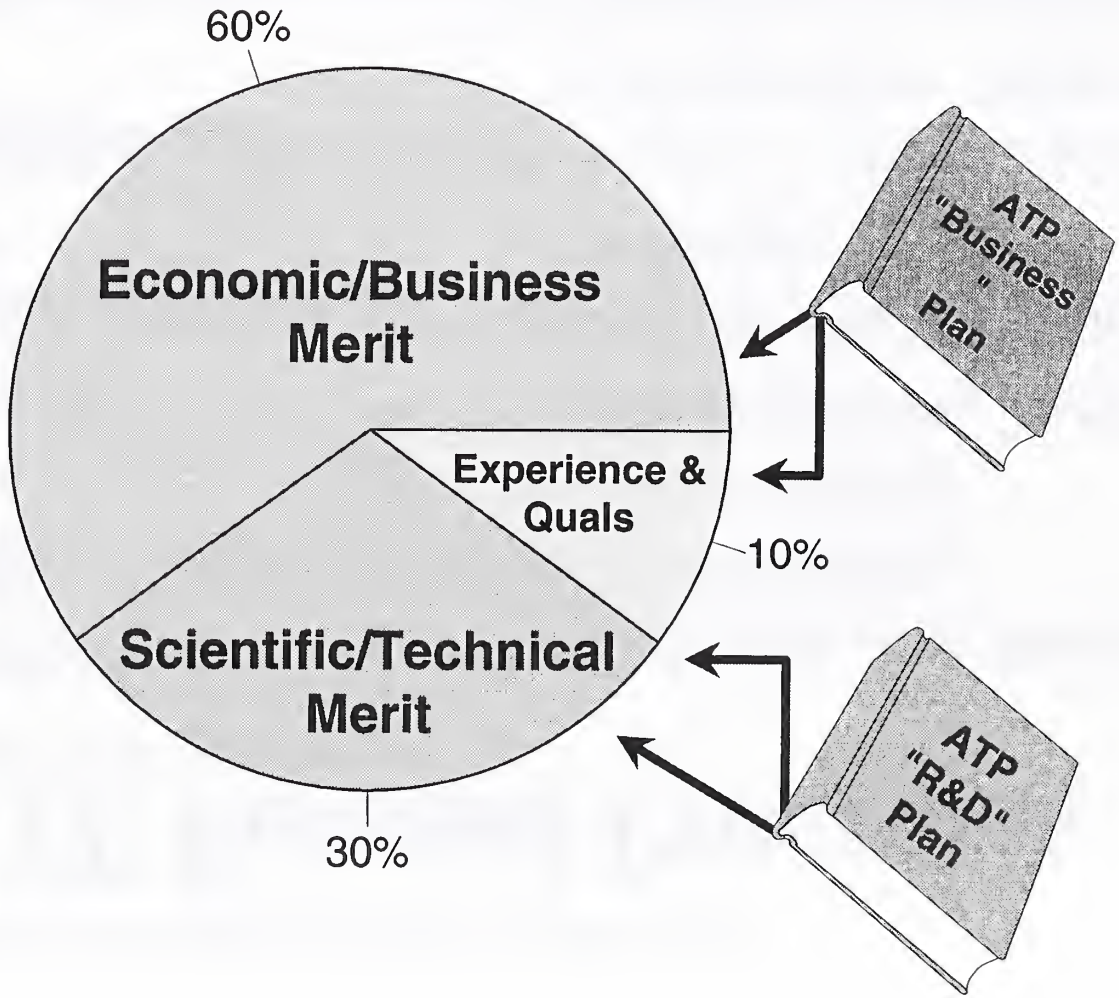
ATP Eligibility

- **Individual Companies**
  - No more than 3 years
  - Up to $2M total
  - NIST pays only direct costs
  - No direct funding to universities, government agencies or non-profit independent research institutes
- **Joint Ventures**
  - No more than 5 years
  - No limit on award amount
  - NIST share less than 50%
  - Must involve two or more for-profit companies, both doing research, and both contributing to the match
  - JV administrator may be industry or independent research organization

ATP Project Selection Process



Project Selection Criteria



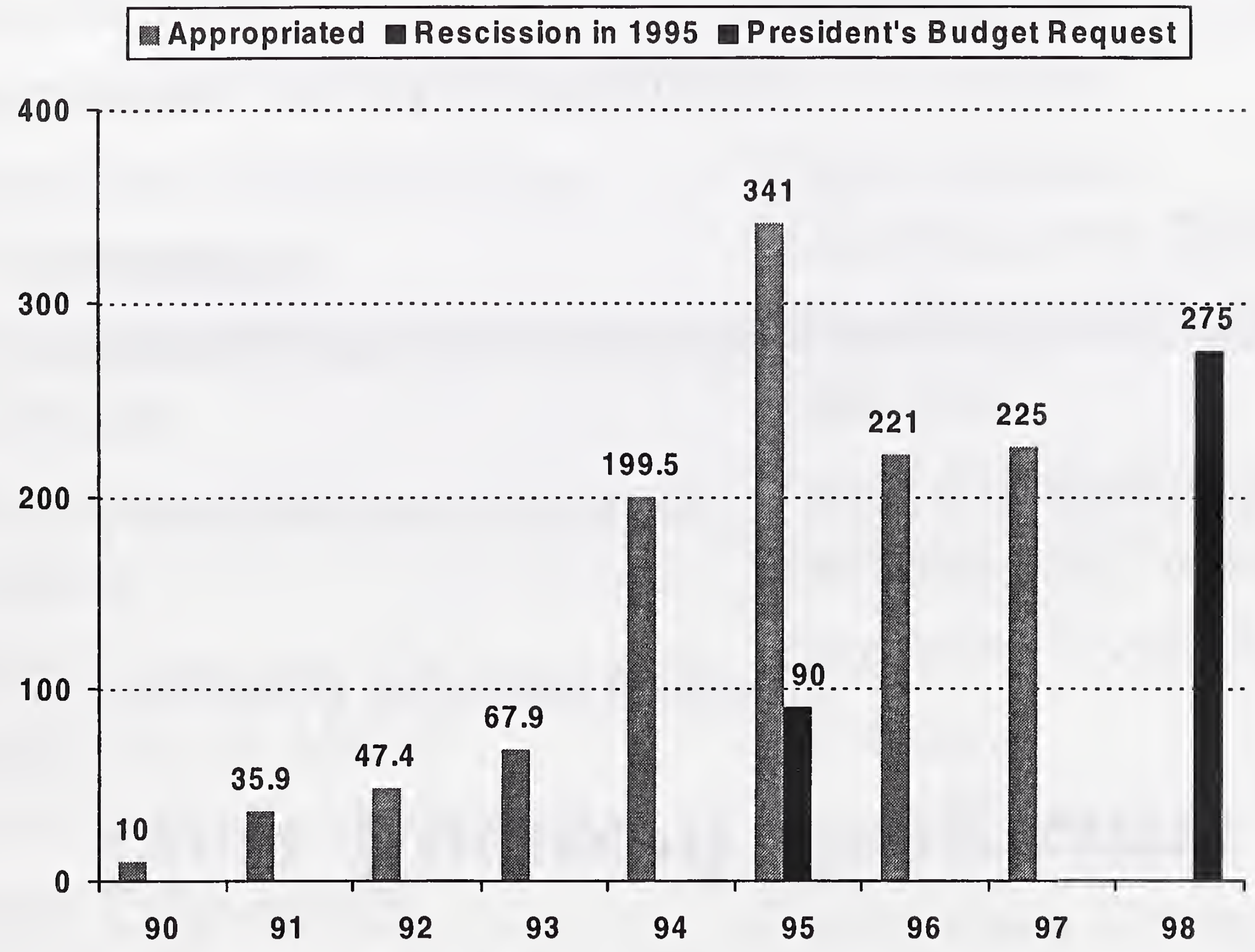
ATP Focused Programs

- Tools for DNA Diagnostics
- Information Infrastructure for Healthcare
- Manufacturing Composite Structures
- Component-Based Software
- Technologies for the Integration of Manufacturing Applications
- Tissue Engineering
- Catalysis and Biocatalysis Technologies
- Motor Vehicle Manufacturing Technology
- Digital Video in Information Networks
- Vapor Compression Refrigeration Technology
- Materials Processing for Heavy Manufacturing
- Digital Data Storage

New Focused Programs

- Industrial Process Controls
- Learning Technologies
- Microelectronics Manufacturing Infrastructure Initiative
- Photonics Manufacturing
- Premium Power
- Selective-Membrane Platforms

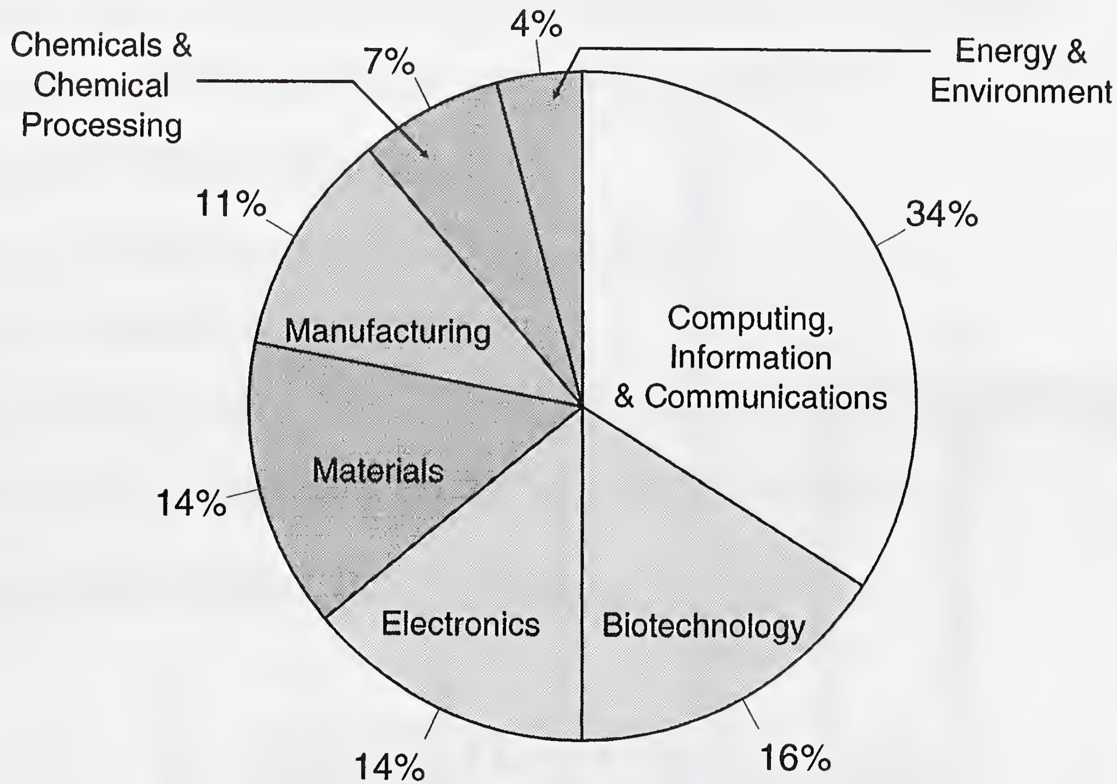
ATP Budget Profile



Status of ATP

- ✓ 3,083 Proposals submitted by industry
- ✓ 352 projects funded with 842 participants
- ✓ $2.32 billion advanced technology development funded
  - $1.15 billion in ATP share
  - $1.17 billion in industry cost share
- ✓ Small business are thriving
  - >50% of projects are led by small businesses
  - Joint ventures have many small business participants
- ✓ Universities play a significant role
  - More than 100 different universities involved
  - More than 250 instances of participation
- ✓ Numerous partnerships with NIST Laboratories

352 ATP Awards
By Technology Area
(As a percent of $1,151 M)



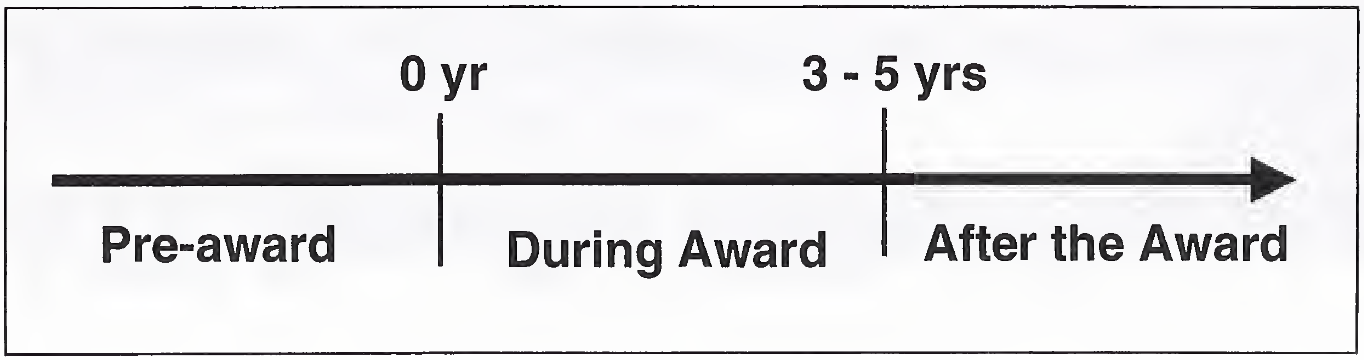
Thirty Competitions (1990-1997)

Award Life Cycle

- Proposal Development
- Merit Review
- Selection or Debriefing
- Award Negotiations

- Project Kickoff
- Reporting & Payment
- Project Adjustments
- Audits
- Annual Reviews
- Project Closeout Meeting

- Post Project Updates
- Impact Analysis

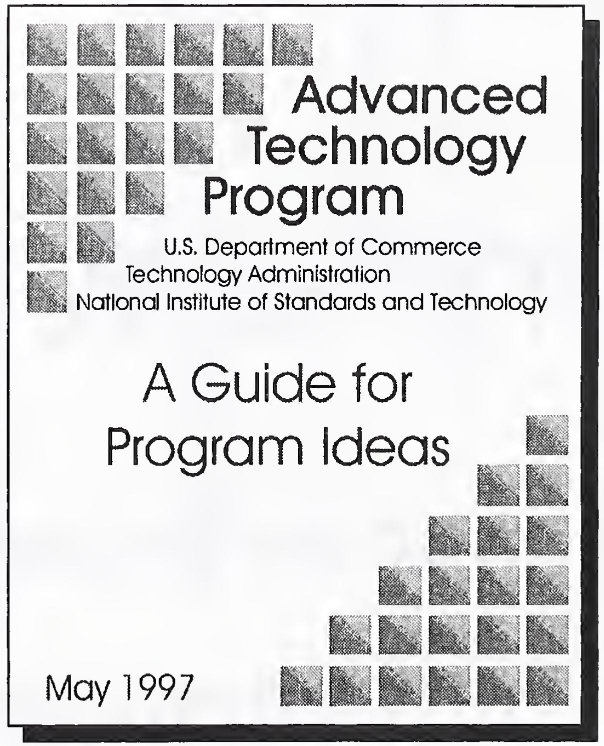


ATP Benefits (Silber Survey)

- Facilitated and accelerated high risk research
- Stimulated collaboration and formation of strategic alliances
- Shortened R&D cycle
- Accelerated commercialization of the ATP-related technology
- Attracted additional funding
- Improved competitive standing
- Discovery of new applications for ATP technology
- Change in corporate philosophy

Guide for Submitting Program Ideas to ATP

- We are looking for revolutionary programs with the potential to bring fundamental change to industry.
- ***Make your voice Heard!*** See the May 1997 Guide booklet for submitting your ideas to ATP.



To Browse ATP Information

World Wide Web: http://www.atp.nist.gov

To Get on the ATP Mailing List

CONTACT

Call toll-free:	800-ATP-FUND (800-287-3863)
Fax your name and address to:	(301) 926-9524
Send an e-mail message to:	atp@nist.gov

1394 and the VESA Home Network

Joel DiGirolamo
Program Manager New Applications
Business Development
Lexmark International

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VESA HNW Goals

- Interoperability
  - Any Device to Any Other Device
  - Low Bandwidth to High Bandwidth
- Common Interface & Protocols on Home Side for Access Providers
- Directory Services
- Plug and Play
- Provide Transition - Analog to Digital
- Connect "Islands" of Technology

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The Vision

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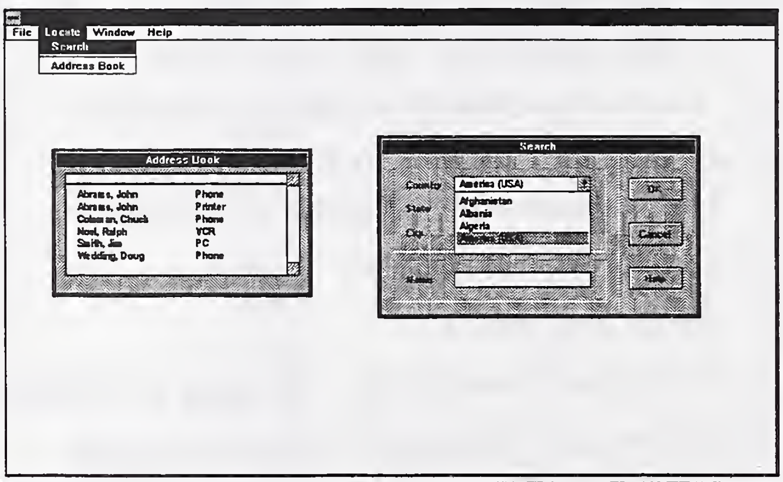
Country Search



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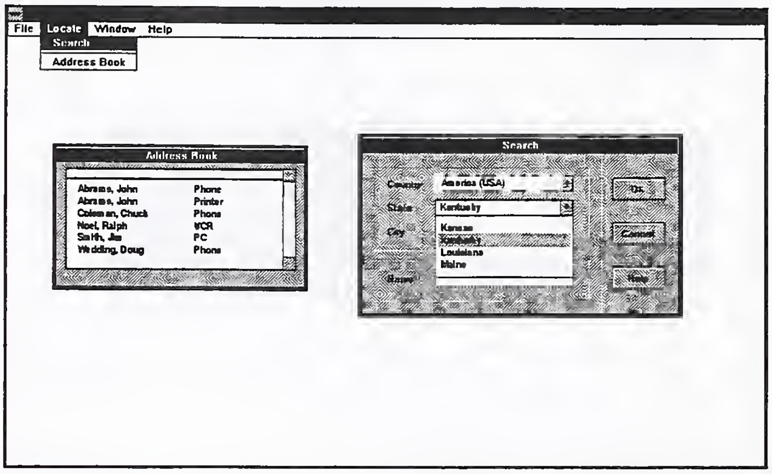
State Search



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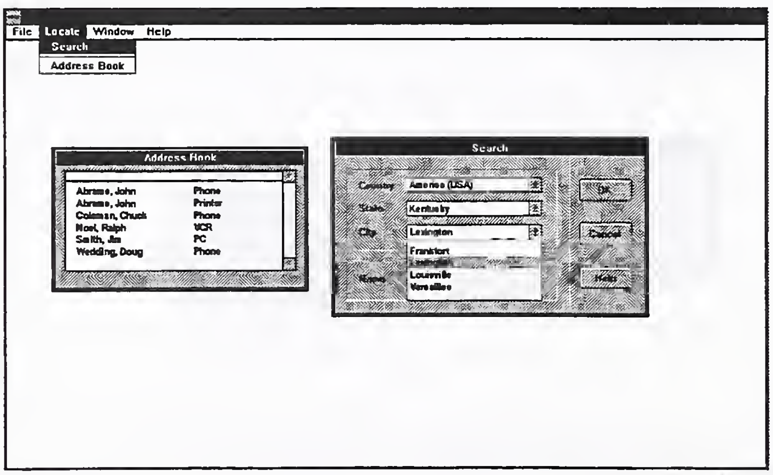
City Search



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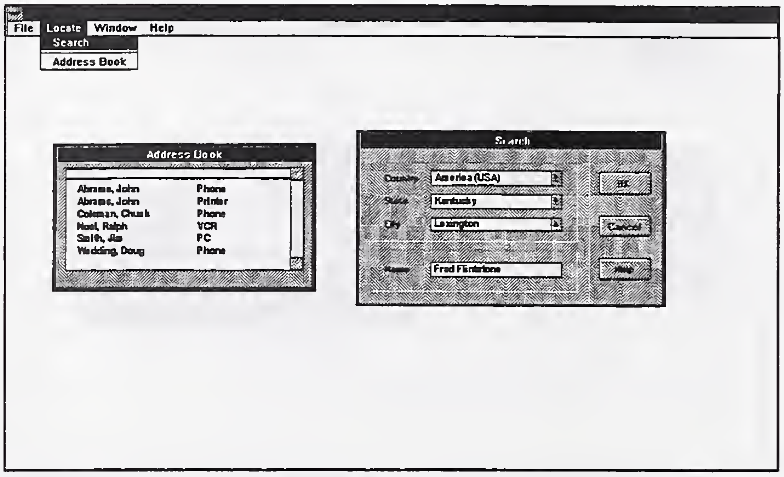
Final Destination



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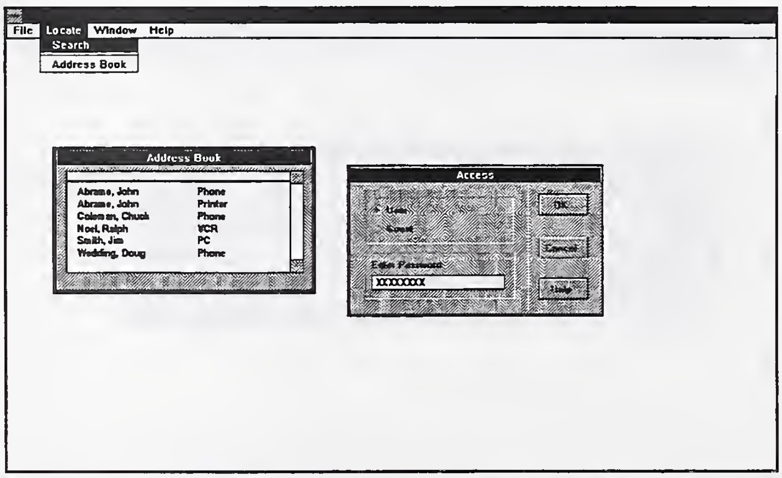
Access Control



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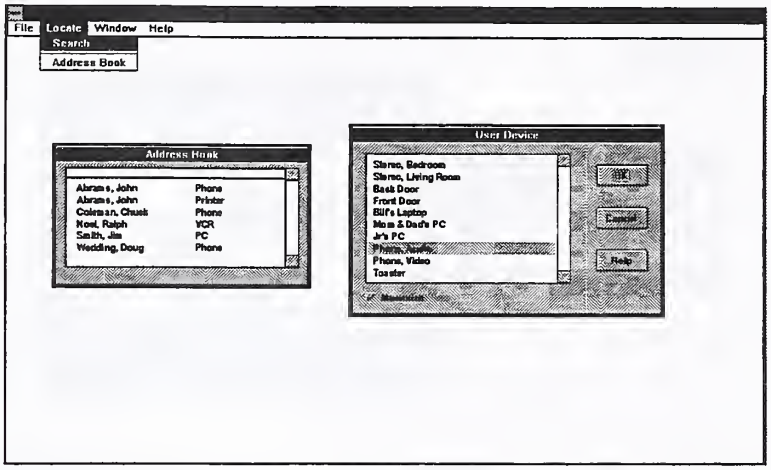
User Devices



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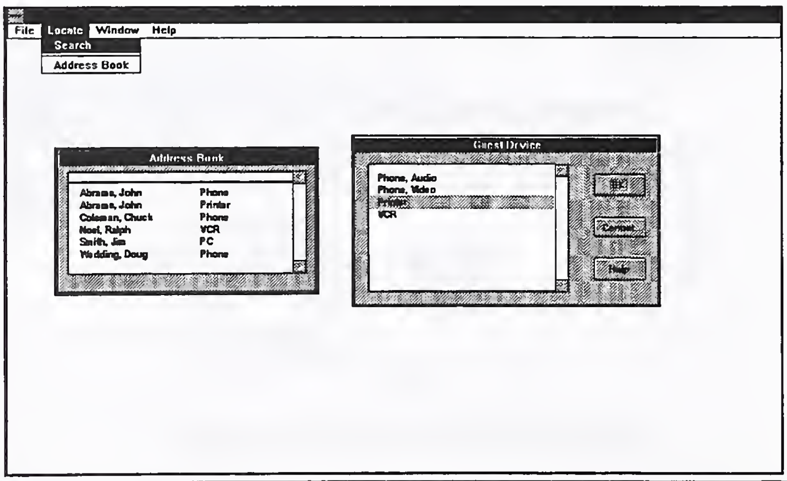
Guest Devices



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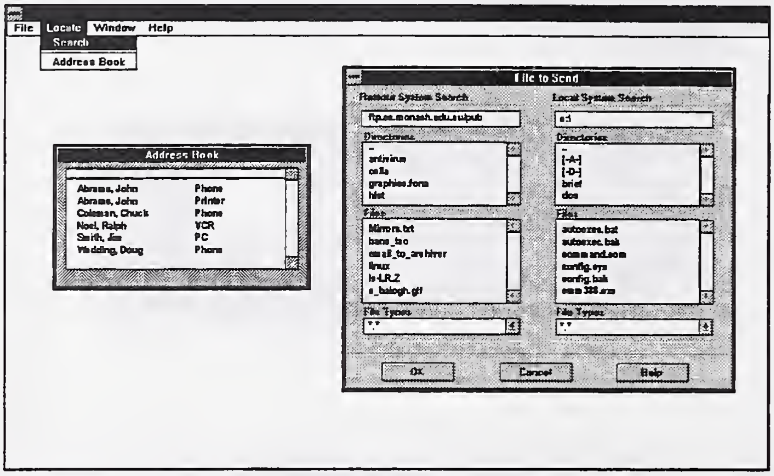
Send File



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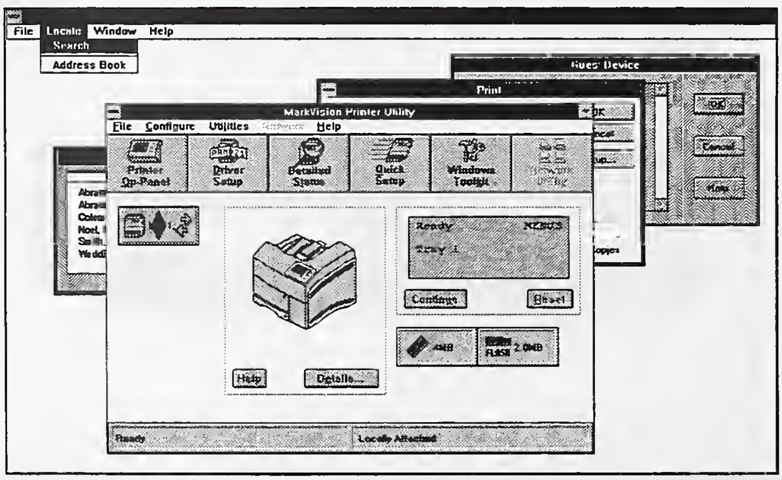
Printer Management



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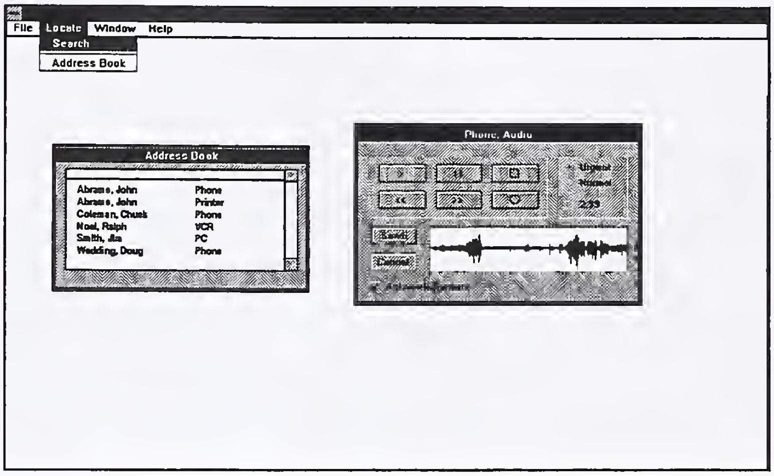
Audio Message



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Applications

- Appliances ⟶ HDTV

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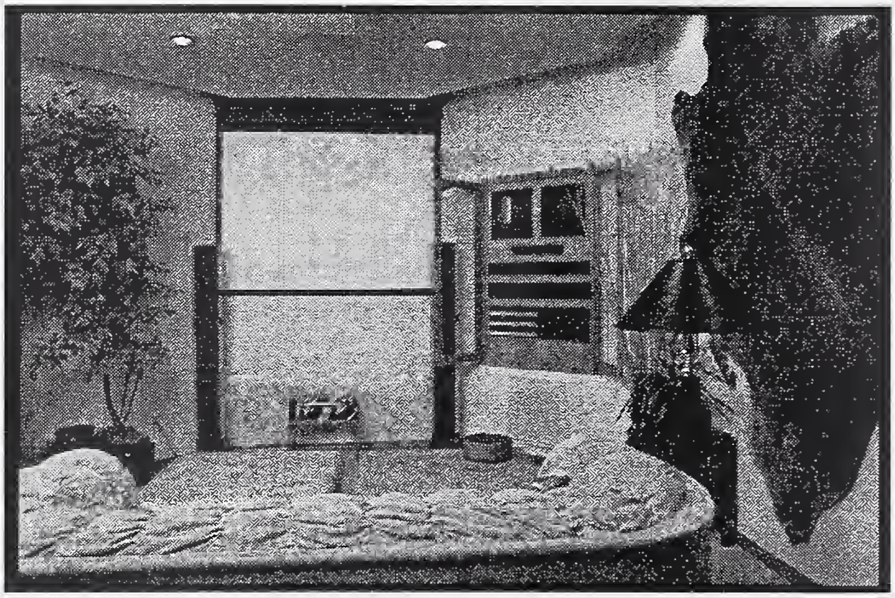

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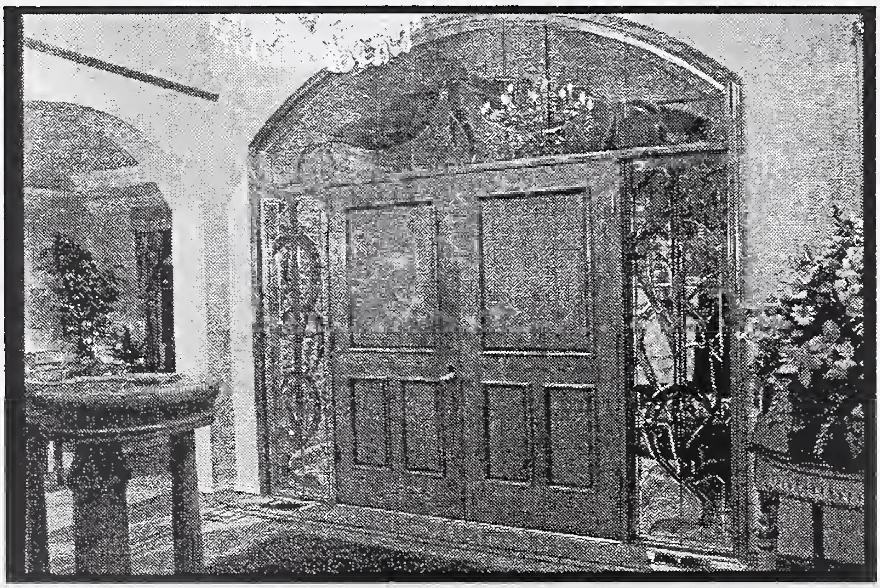

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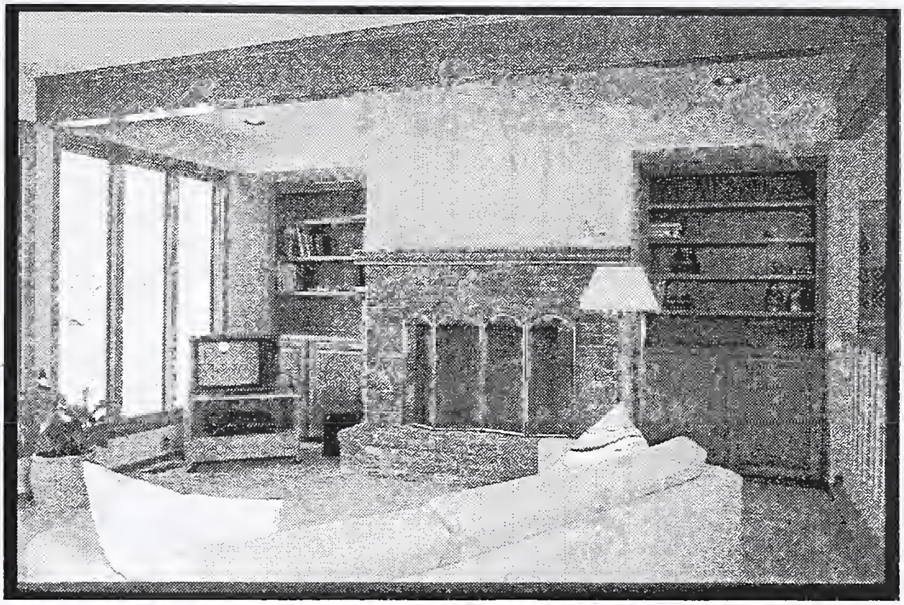

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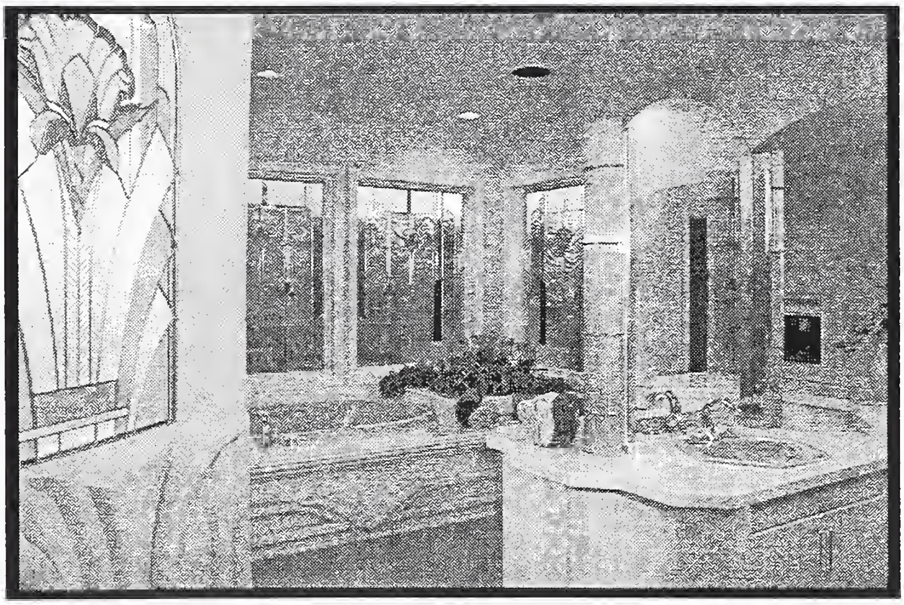

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Application Types

- Home Automation
- High Bandwidth
- Analog TV
- Telephony

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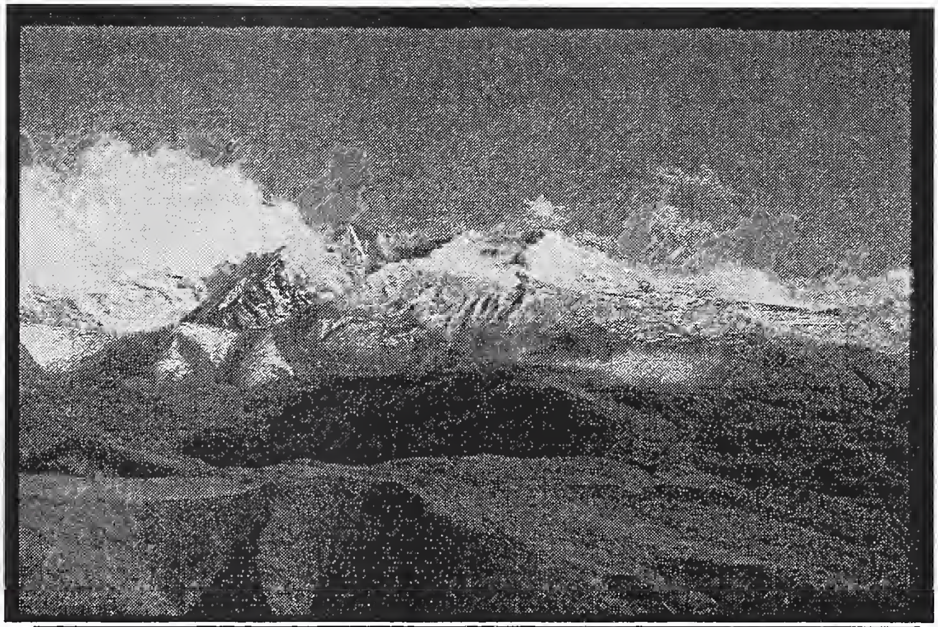

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Architecture Overview

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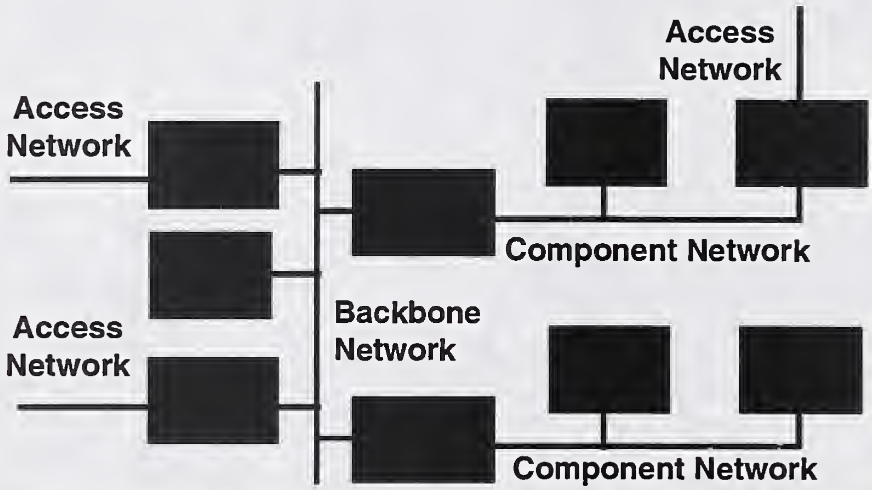
VESA Architecture



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Architecture Features

- Allows Separate Networks to Co-Exist
  - Keep Low Speed Devices on Own NW
- All Devices on Home Network Can Interoperate
- Compatibility with Existing Networks

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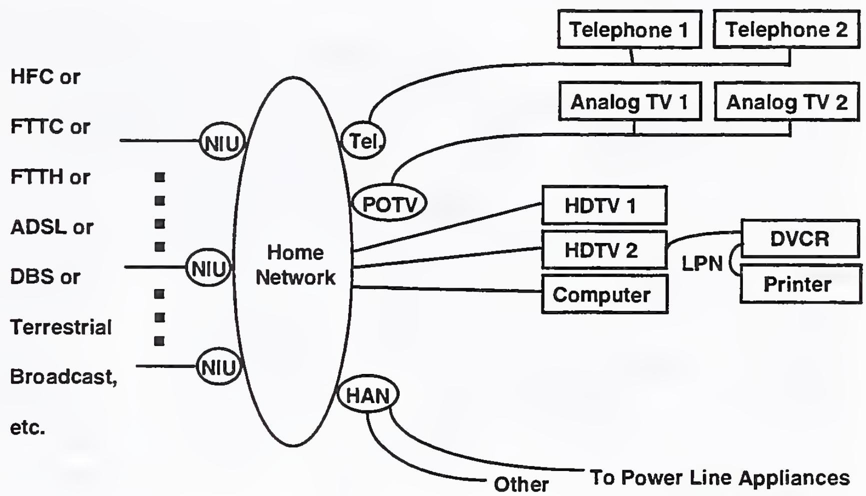
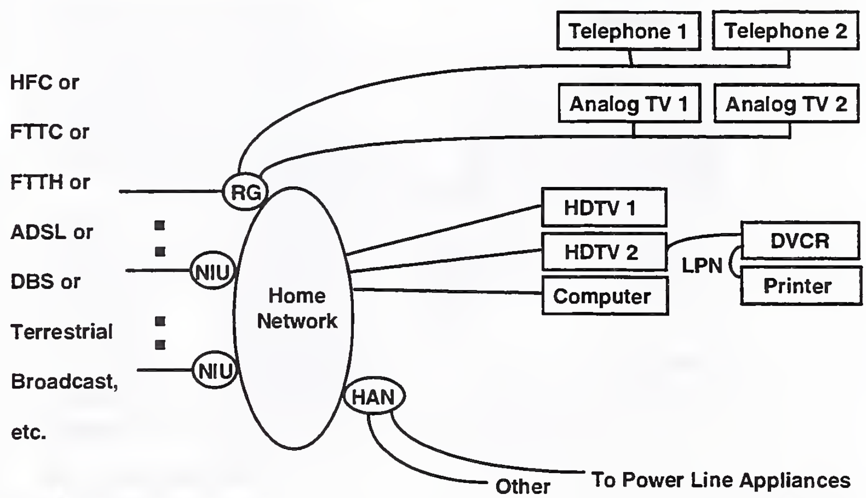
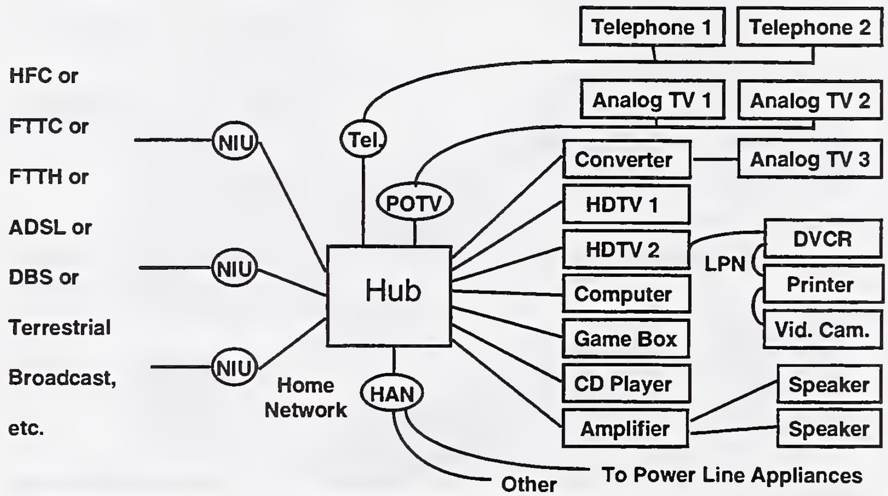
Architecture Example #1



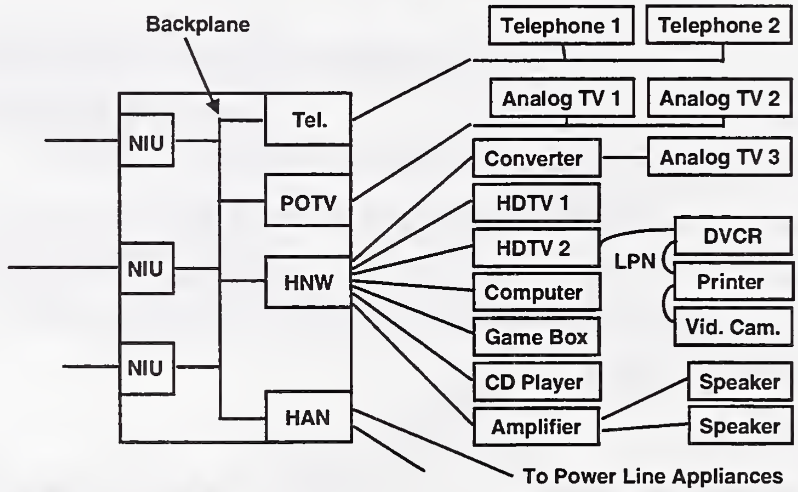
Architecture Example #2



Embodiment #1



Embodiment #2



1394 Extensions

- Need Long Distance
  - Goal is 100Mbps at 100 meters
  - Standard (1394b)
- Need Media Other Than UTP

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Architecture Details

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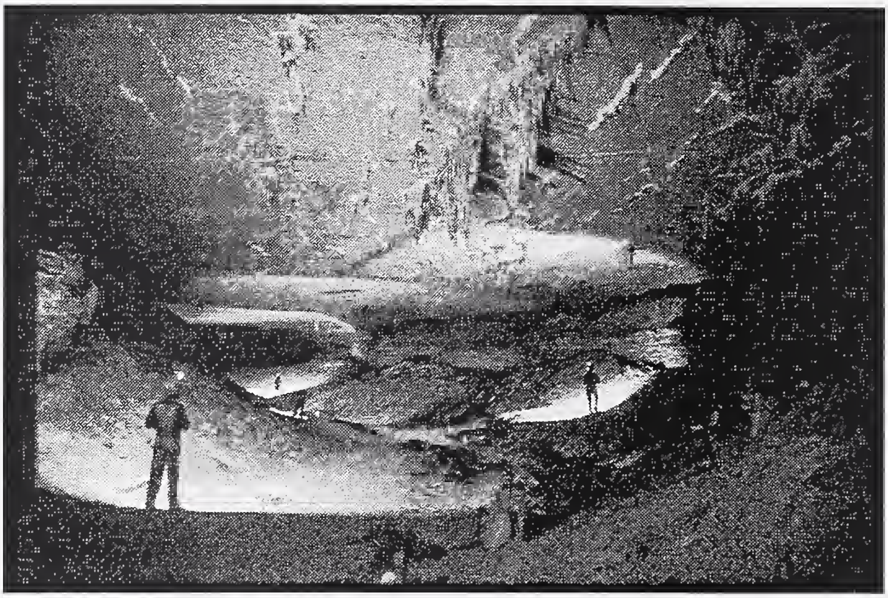

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Backbone Network

- Spans Whole House
- Provides Sufficient Quality of Service for All Applications and Devices
- Very High Bandwidth
- Serve Digital Clusters in Multiple Rooms
- Provide for at Least 2 HDTV Signals Into a Room
  - One TV with PIP
  - Two TVs

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Component Network

- Separate Network with Device Specific Needs
  - Lower Cost, Reduced Protocol Complexity
- Uses Network Device to Interface to Home Network

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Local Peripheral NW (LPN)

- High Bandwidth
- Short Cable Runs
- Hot Plugging
- Polarized Plugs
- Flexible Cable

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LPN Continued

- Connect:
  - Advanced TV (ATV), Digital VCRs (DVCR)
  - Camcorders, Audio Equipment
- Asynchronous & Isochronous Data
- Protocols Same as Home Network

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Access Devices

- Connection to External Access Network
  - e.g. POTS Modem, ISDN Adapter, Residential Gateways

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End Device

- Provides Utility to End User
- Examples:
  - Printers, TVs, Security Sensors, HVAC

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Network Devices

- Provide Network Services to End Devices
- Could be a Bridge or Repeater
  - Protocol and Address Translation

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Plain Old TV (POTV)

- Connect to Existing Analog Coax Network
- Should Allow Same Services Consumers Get Now
  - e.g. Picture In Picture (PIP)

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Telephony (Med. B/W)

- Uses Today's Twisted Pair
- Lower Bandwidth
- Keep Lower Bandwidth Devices Cheaper

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Home Automation NW

- Primarily Power Line
- Control
  - Appliances, Thermostats, Security Systems, etc.
- Cost is Significant Factor

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Star Topology

- Preserve Bandwidth on the Network
- Data May Be Isolated on Individual Segments

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Proof of Concept

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Proof of Concept Goals

- Multiple Simultaneous Digital Video Streams
- Multiple Types of Datastreams
- Multiple Types of Network Segments
- Transport 100 Mbps Over 100 Meters is Goal

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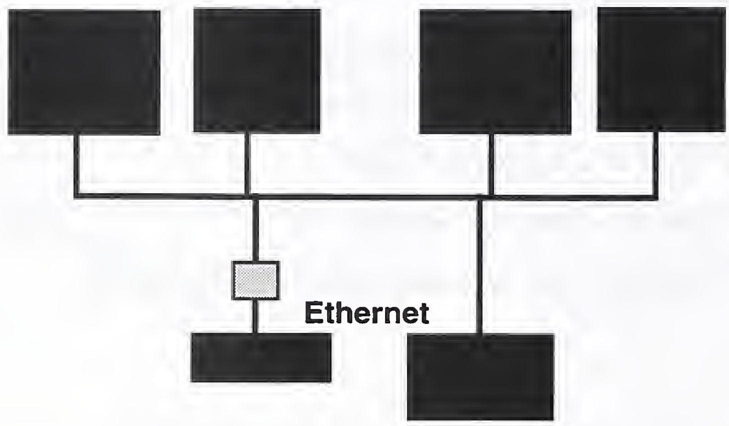
Proof of Concept



Proof of Concept Status

- Phase 1 Complete
  - 1394-1995
  - All Function Except Long Distance
- Phase 2 Completion Fall 1997
  - Chips in Prototype Stage

Media Under Consideration

- UTP Category 5
  - "Proven" Technology
  - Emissions and Susceptibility Concerns
- Plastic Optical Fiber
- Glass Optical Fiber
- Beginning Wireless Investigation

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Wall Outlets

- Unique VESA Home Network Connector
  - Prevents Inadvertent Contact with Incompatible Equipment
- No Active Electronics in Wall Outlet
  - TIA, NEC and Other Concerns
- Most Likely Wall Adapters to LPN or Other In-Room Network

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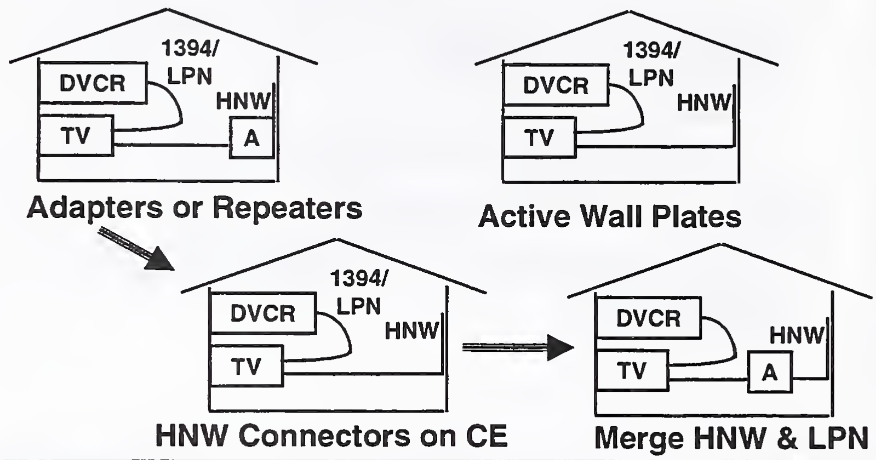
LPN to Home Network



Common Internetworking Protocol

- Requirement to Connect Heterogeneous Networks
- Need Basic Device Communications
  - Transport, Control, Management
- Allows Network Devices, End Devices and Access Devices to Communicate
- Considerations:
  - Addressing, Isochronous Capability, NW Management and NW Configuration

Directory Services

- Devices and Applications Locate Devices on the NW
  - Access Services Entering RG Can Locate Devices in User's Home
- Plug and Play Capability
- Locate Resources on Component Networks

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Security

- Firewalls to Outside World
- Data Security
  - Copies of Movies, Credit Card Numbers
- Device Access Security
- Work with Standards Groups Such as CPTWG

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Issues

- Decompress at Final Destination
- Channel Selection at Access Device or Before
- Must Support Upstream Video
- Error Handling & Conditional Access at Access Device

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Issues Continued

- Security at Access Device (RG)
- Address Quality of Service & NW Scalability
- Bounded Jitter in Whole System
- Seamless Effect of Bus Reset

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Status

- IP Accepted as Common Protocol
- Addressing Schemes Adopted
- Web Servers As User Interface
- Multiple Device Classes
- Compiling Directory & Mgmt Technologies

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Liaisons

- TIA TR 41.5
- TIA TR 41.2
- DAVIC
- 1394 Trade Association
- CEMA (EIA)
  - R 4.1
- CableLabs

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Industry Participation

- Consumer Electronics
- Computer
- Telecomm.
- Networking
- Cable TV
- Silicon Chip
- Home Automation
- Connector
- Media

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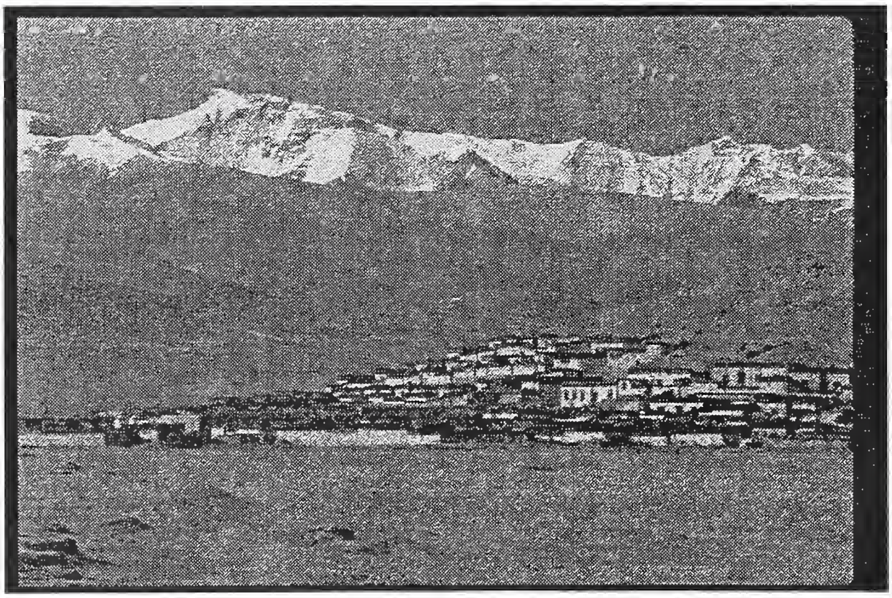

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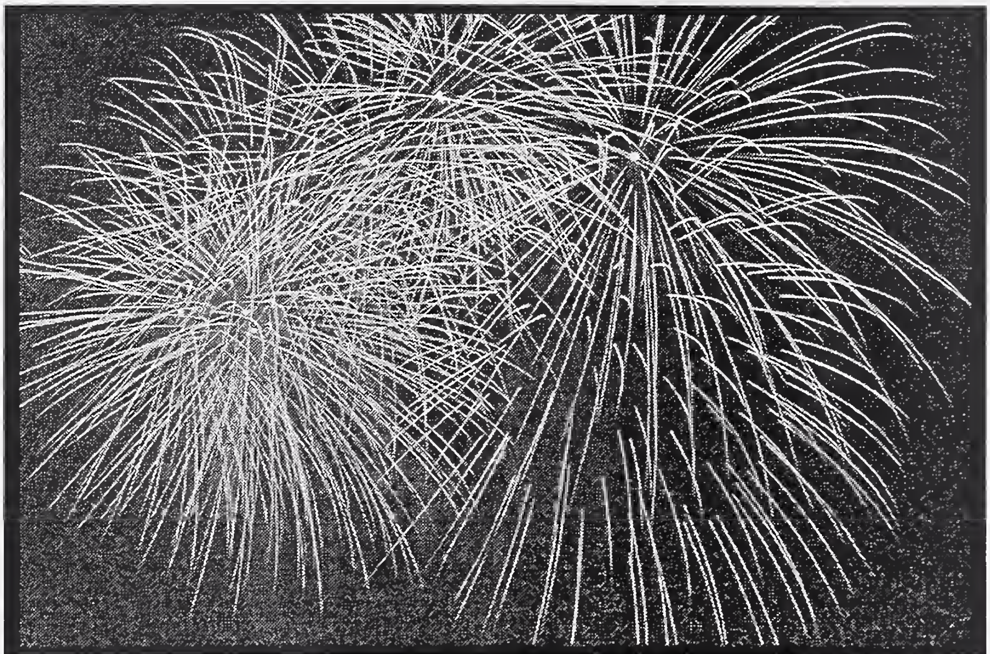

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DARPA HDS Program
Display Forum '97 Workshop
10/20/1997

Bruce Gnade
High Definition Systems
Electronics Technology Office
DARPA

WHAT DO DISPLAYS BRING TO DoD

- IMPROVED PERFORMANCE FOR THE WARFIGHTER

  -Displays often control information uptake impacting the speed and effectiveness of decision making

  -Essential for the digital battlefield from command-and-control to the foot soldier

- INCREASED RELIABILITY AND READINESS

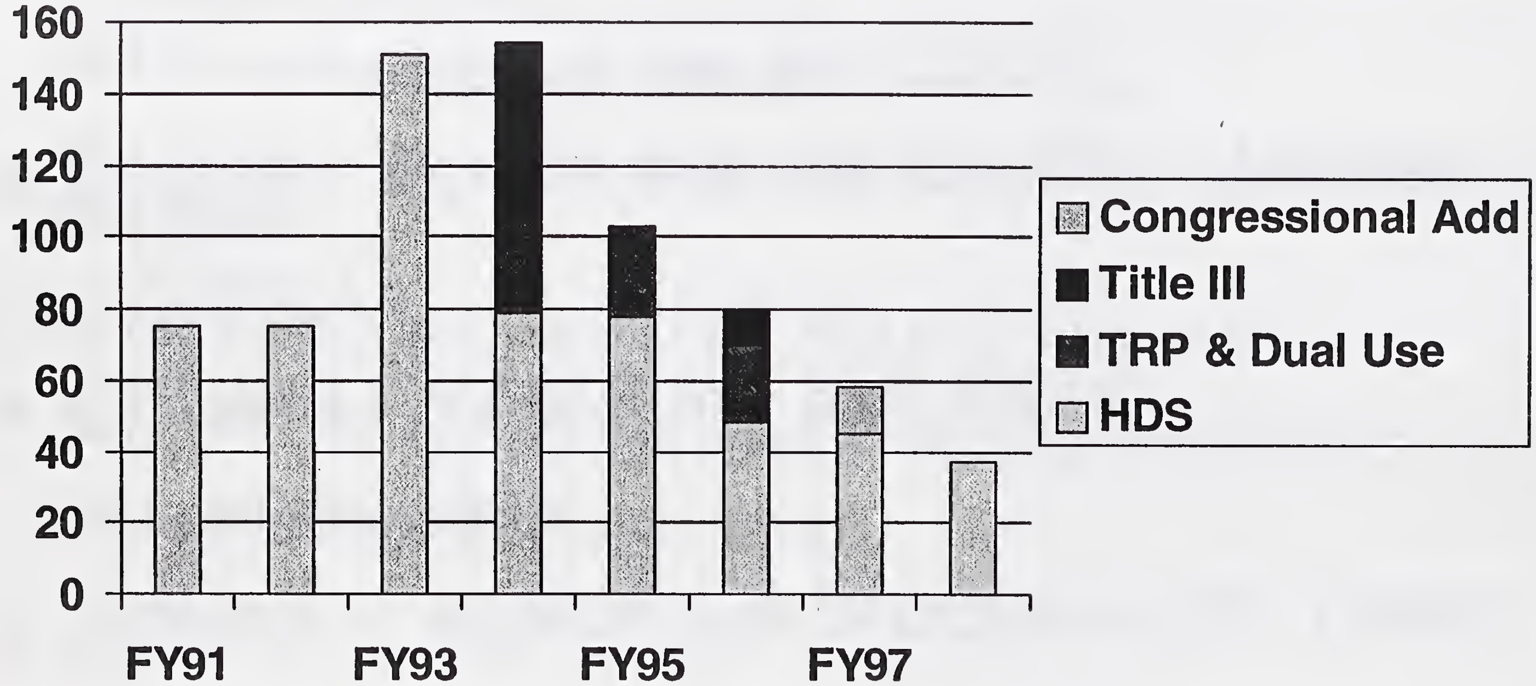
  -Typical MTBF for CRT's or mechanical instruments is 300 hrs

  -Major reduction in Lifecycle Costs

DARPA HDS Program

- History - where the program has been
  - (1990-1996)
- Current - where we are today
  - (1997)
- Future - where are we going? / where should we be going?
  - (1998-2000)

HDS Display Funding History



DoD Display Programs

DARPA CORE TECHNOLOGY AND SYSTEMS PROGRAMS

PROGRAM	YEARS	PURPOSE
High Definition Systems (HDS)	89 - Pres.	Create new display technology
Head Mounted Display Systems (HMDS)	93 - 97	Demonstrate HMDs in field
United States Display Consortium (USDC)	93 - Pres.	Provide industry a voice
Advanced Information Component Manufacturing (AICM)	93	Access DoE labs expertise
Phosphor Technology Center of Excellence (PTCOE)	94 - Pres.	Establish phosphor research
Thin Film Transistor Teams (TFT Teams)	94 - Pres.	Team academia with industry

AMLCD MANUFACTURING TESTBEDS AND DOMESTIC CAPACITY FUNDED BY DARPA

Program	YEARS	PURPOSE
AMLCD Manufacturing Technology ($50M)	93 - 94	Manufacturing testbed (OIS)
High Density AMLCD Mfg Technology ($25M)	94 - 95	Testbed (Xerox/Standish/ATT)
Defense Production Act Title III for AMLCD ($30M)	94 - Pres.	Increase domestic capacity

DoD Display Programs (cont.)

TECHNOLOGY REINVESTMENT PROGRAM (TRP) DUAL USE

PROGRAM	YEARS	PURPOSE
Active matrix electroluminescent, inorganic ($16M)	94 - 97	Develop advanced EL (Planar-led)
Field Emission Display, High Volume ($20M)	94 - 97	Use US Intel. Prop. (Candescent-led)
Field Emission Display, High Performance ($13M)	94 - 97	French Intel. Prop. (Raytheon/Motorola)

HDS AND TACOM HTP FOR VERTICAL INTEGRATION

PROGRAM	YEARS	PURPOSE
Field Emission Display, (FED OEM)	97 - 98	Integrate FPD w/OEM (Micron)

HDS PROGRAM GOALS

OBJECTIVE:

Develop leading-edge display technology to meet diverse, but specific, DoD needs. The goals include increased power efficiency, reduced weight and improved ruggedness, while pushing the state-of-the-art in display performance. Demonstrate DARPA-funded technology in military applications.

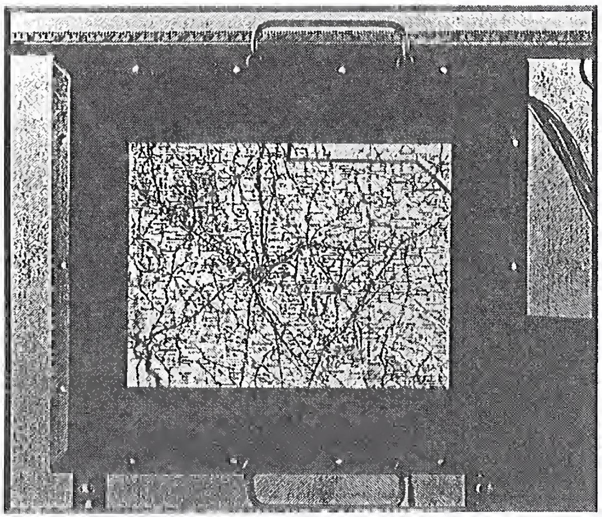
High Definition Systems Program

- Current emphasis for HDS program
  - accelerate the development of flexible, rugged displays (**organic EL, zero-power reflective, self-assembled electronics, etc.**)
  - push maturing technologies to demonstration phase (**FED, Color EL, etc.**)
  - increase the demonstrations/evaluations of HDS developed technology (**DMD, TFEL, plasma, etc.**)

21” Color Plasma Display

PROBLEM: Aging large screen cathode ray tube (CRT) display systems used in applications such as AWACS, JSTARS and ABCCC are becoming unsupportable:

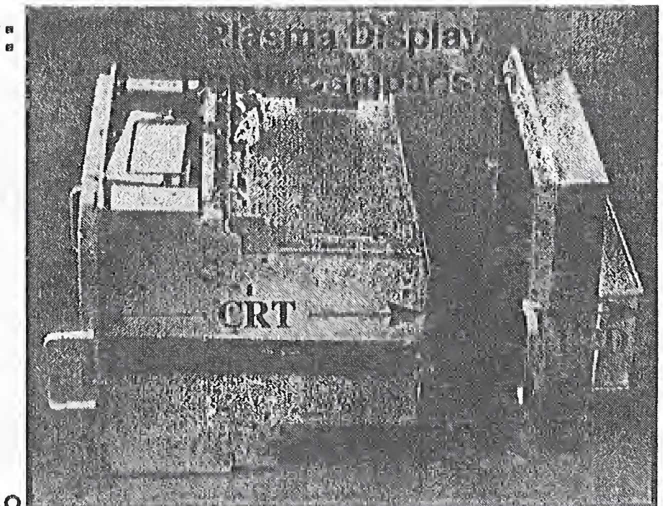
- Availability: Single foreign supplier
- Logistics Support: $208K/CRT, not field repairable
- Maintenance Resources: MTBF ~ 500 hours
- AWACS has 14 displays per plane - flying now with 12-14 operational
- Use of Platform Resources: E-3 maxed out in weight, volume, and power



1280 x 1024
SXGA Resolution

Impact of FPD Technology:

- Weight reduction/aircraft:
  1064 lb..
- Power reduction/aircraft:
  1750 watts
- R&M:
  MTBF > 3300 hours,
  replace in field
- Viewing area increase: 70%



Digital Micromirror Device

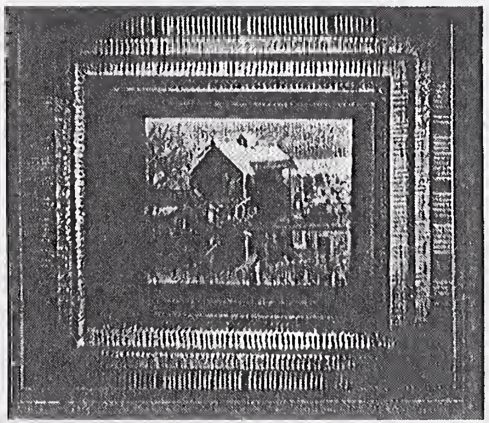
Demonstrated resolution of 2048 x 1152

21" Rear projection system

> Evaluated for CLADS program

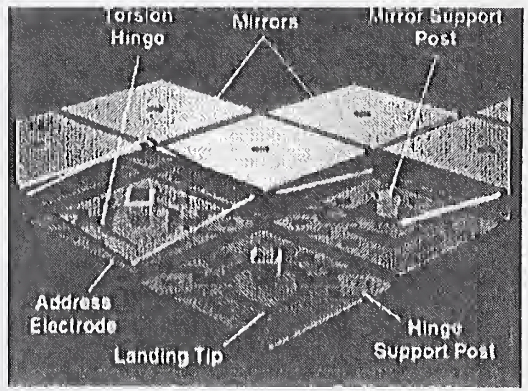
40" Rear projection system

> Evaluated at Prairie Warrior exercise



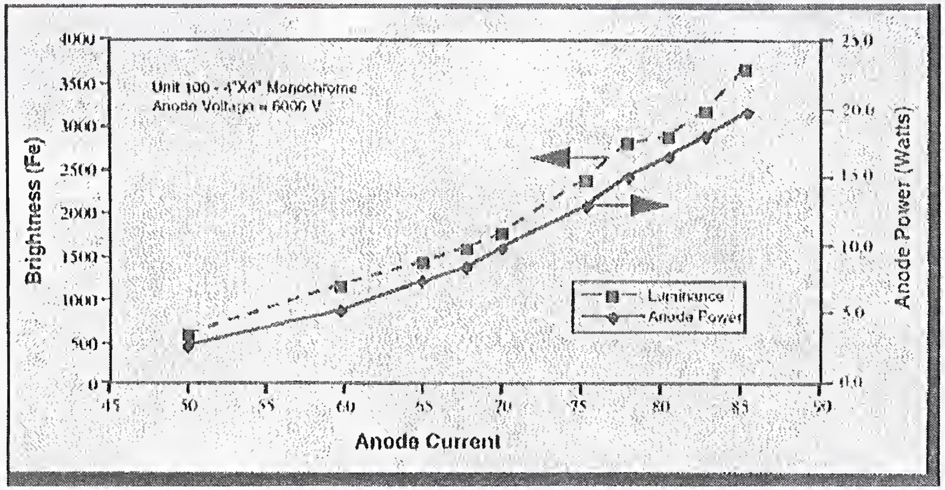
Recent Improvements

- 17μm x 17μm pixel
- Spring-tip design
- Improved hinge



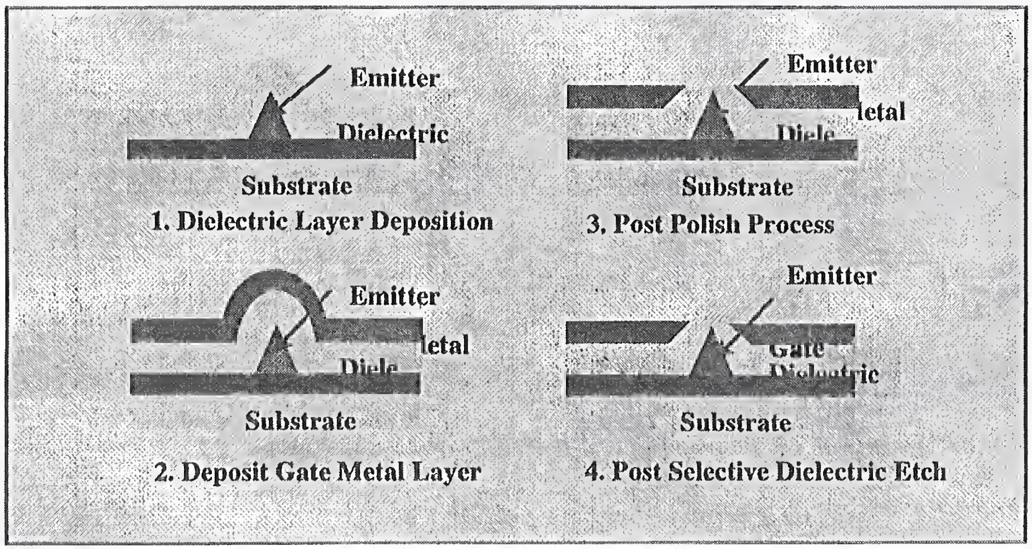
Field Emission Displays

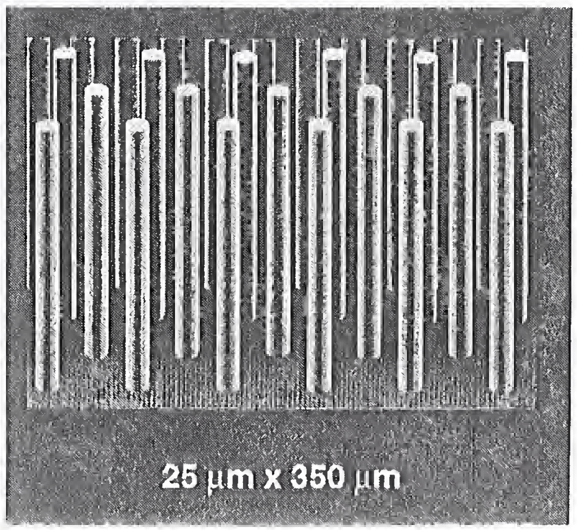
Raytheon High Brightness Display



1) Low Power
2) Wide Temp Range
3) Full Video Rate
4) Capable of High Brightness

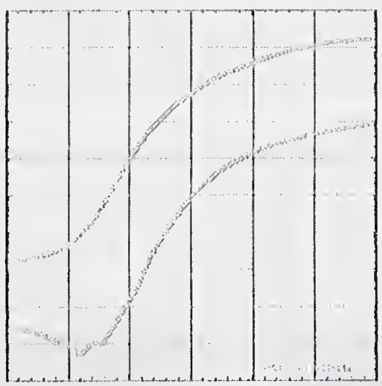
Micron Technology

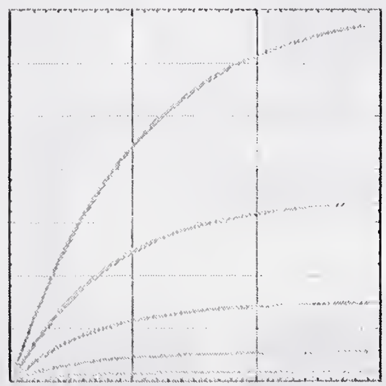


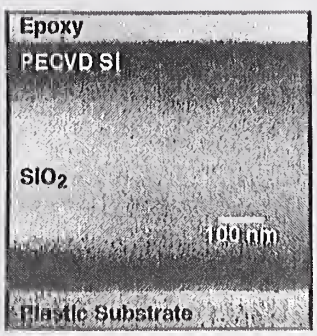


LLNL Poly-Si TFT's on Plastic

- Fabricated entirely below 100°C on polyester.
- Laser crystallized channel, laser doped source-drain.

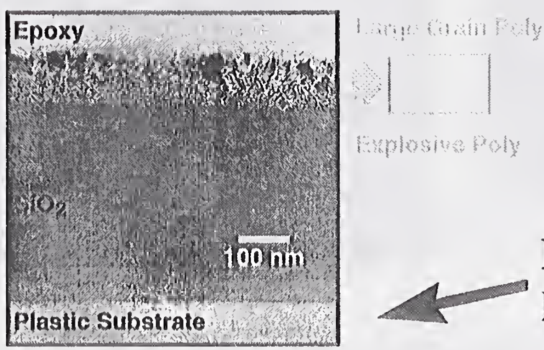






As Deposited

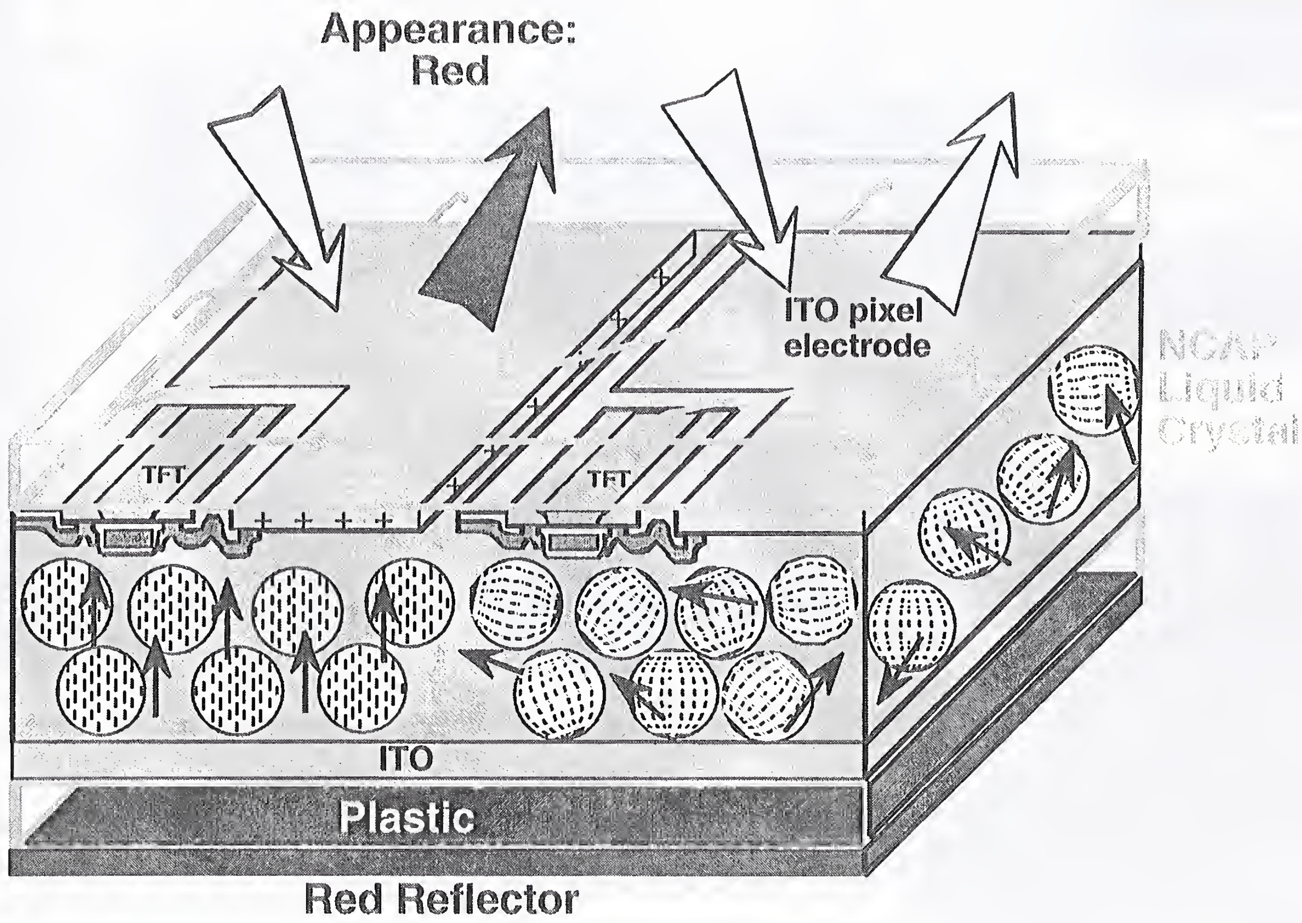
Laser → Crystallization



After 180 mJ/cm^2

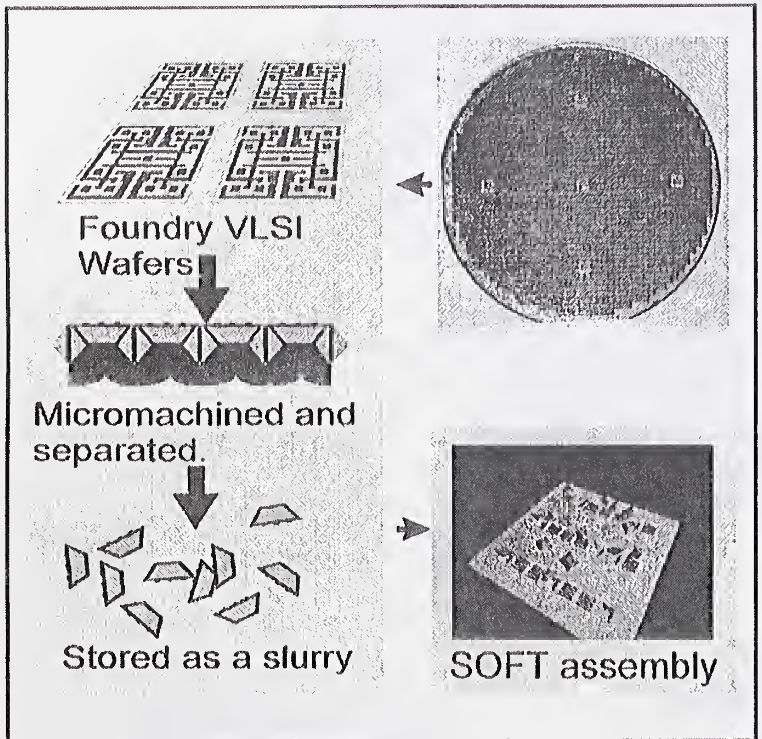
Plastic undamaged during laser processing

LLNL PDLC Display



Self Orienting, Fluidic Transport
SOFT -- Beckmen Displays

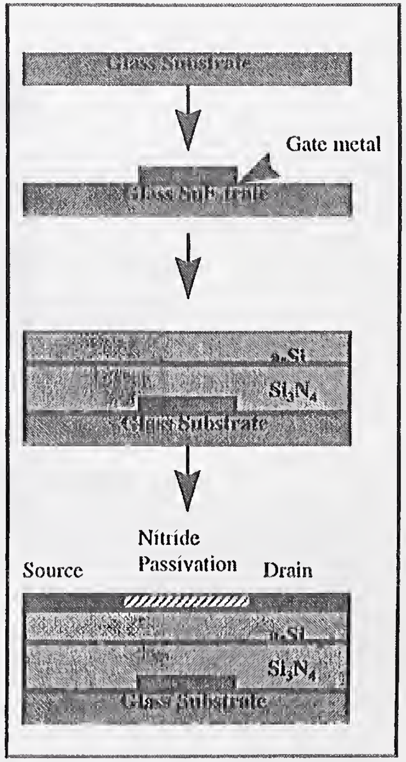
SOFT process Flow



SOFT Advantages

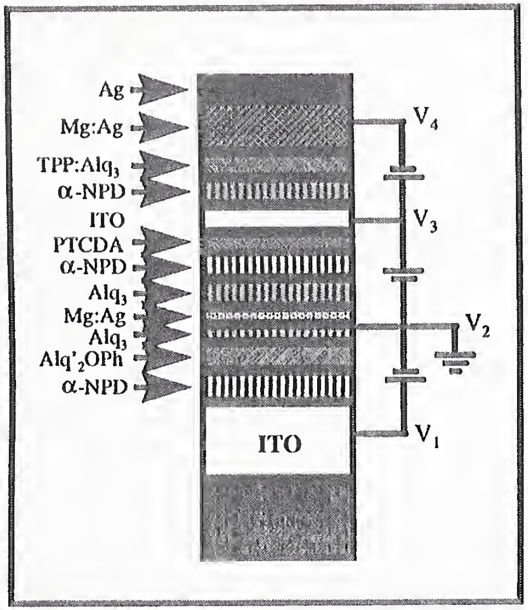
1) higher performance electronics
2) display technology independent
3) display size independent
4) low temperature processing
5) small capital investment
6) $2x10^7$ pixels/8" wafer

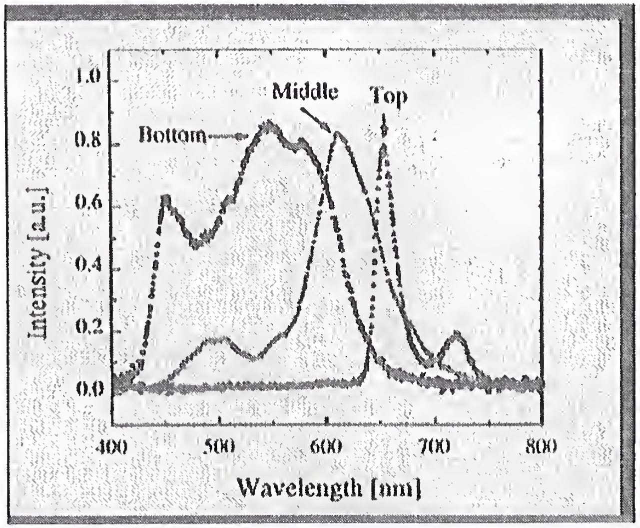
TFT process Flow

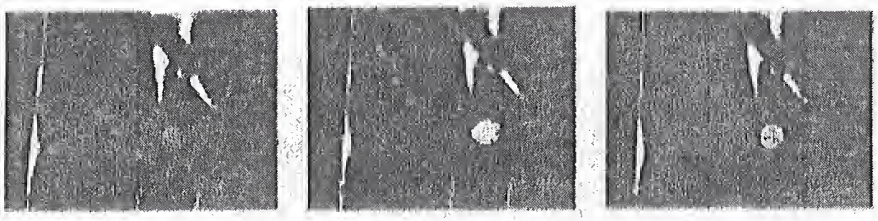


Display Process

Organic-based Displays



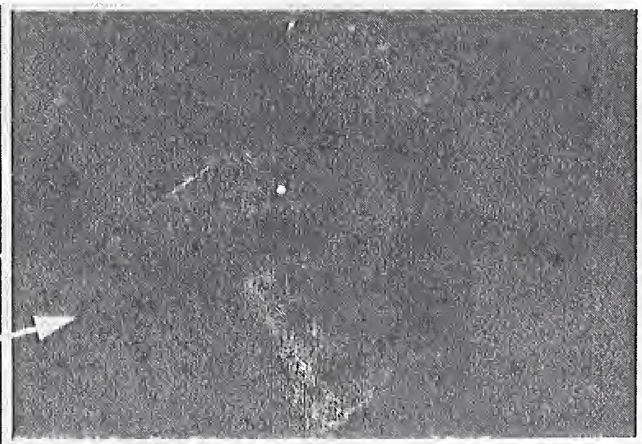




S.R. Forrest

1.) Low voltage
2.) Large
3.) Rugged
4.) Potentially Inexpensive

Princeton Univ. - Steve Forrest
First demonstration of stacked RGB OLED



Penn State / Princeton -> S. Fonash, S. Wagner

<u>TFT/OLED on a Flexed Steel Foil</u>

• radius of curvature ~3.5"

VII. Track II: Display Measurement Workshop

NIST Calibration Scheme for Colorimetry of Displays

Steve Brown and Yoshi Ohno

N.I.S.T.

Collaborators: Jonathan Hardis, Thom Germer

Partially supported by the Air Force: CCG97-42

Motivation

- The uncertainties of color measuring instruments (tristimulus colorimeters and spectroradiometers) are often not well known or not are not satisfactory for high-accuracy applications.
  - Uncertainties of tristimulus colorimeters often exceed Ò .01 in x,y and 10 % in luminance.
- Needs for improved accuracy and uniformity of display measurements in
  - color reproduction
  - the display industry
  - the aircraft industry
  - the optical radiation measurement community

Goals

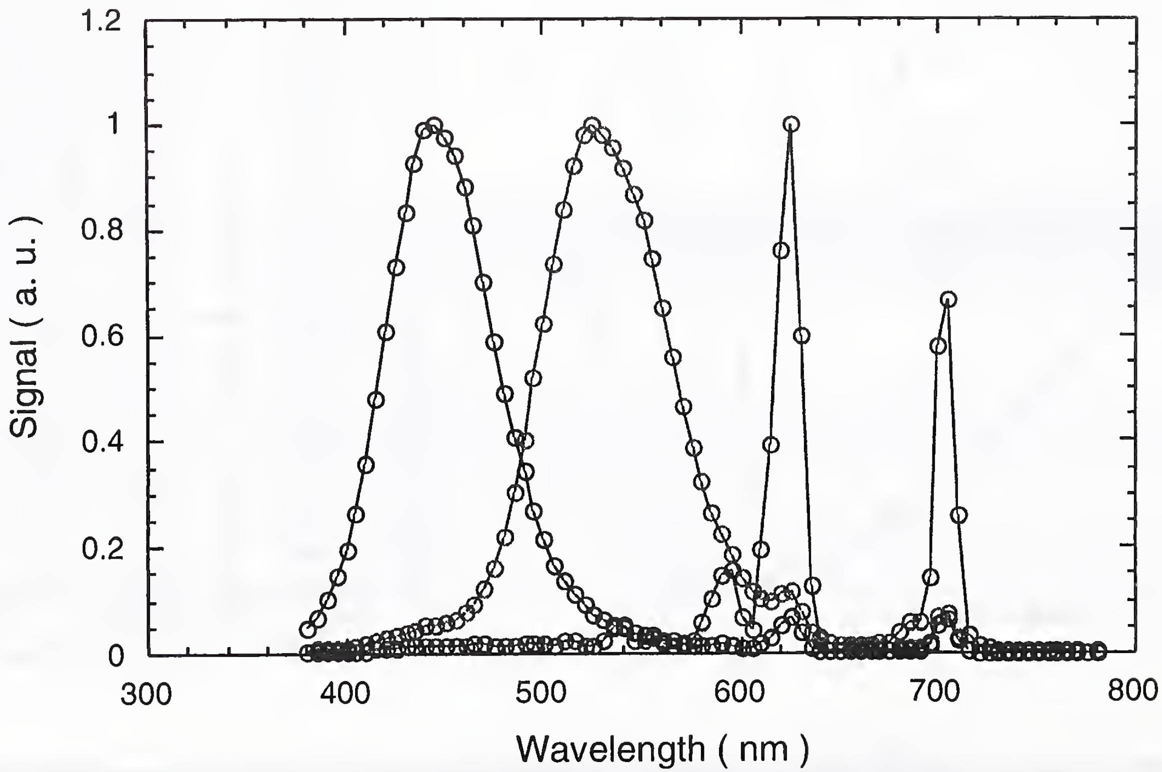
- Develop a reference instrument to enable measurements of display colors at the lowest possible uncertainty.
  - — +/- .001 in x,y and 1 % in luminance.
- Establish NIST calibration services for color measuring instruments for various display colors.
  - — Develop improved calibration methods that allow simple and accurate calibration of tristimulus colorimeters for all colors of a display.
- Develop instrumentation and methodologies to measure additional properties of displays and their influence on color measurement.

Outline

- Factors Contributing to Measurement Error in x,y
  - Noise
  - Stray Light
- NIST Calibration Schemes
  - Colorimeter Calibration Facility
    - > Reference SpectroRadiometer
  - Goniometric Aspects of Displays
- Tristimulus Colorimeters
  - Evaluate Matrix Methods
    - > Four Color Method (Y. Ohno and J. Hardis)
- Summary

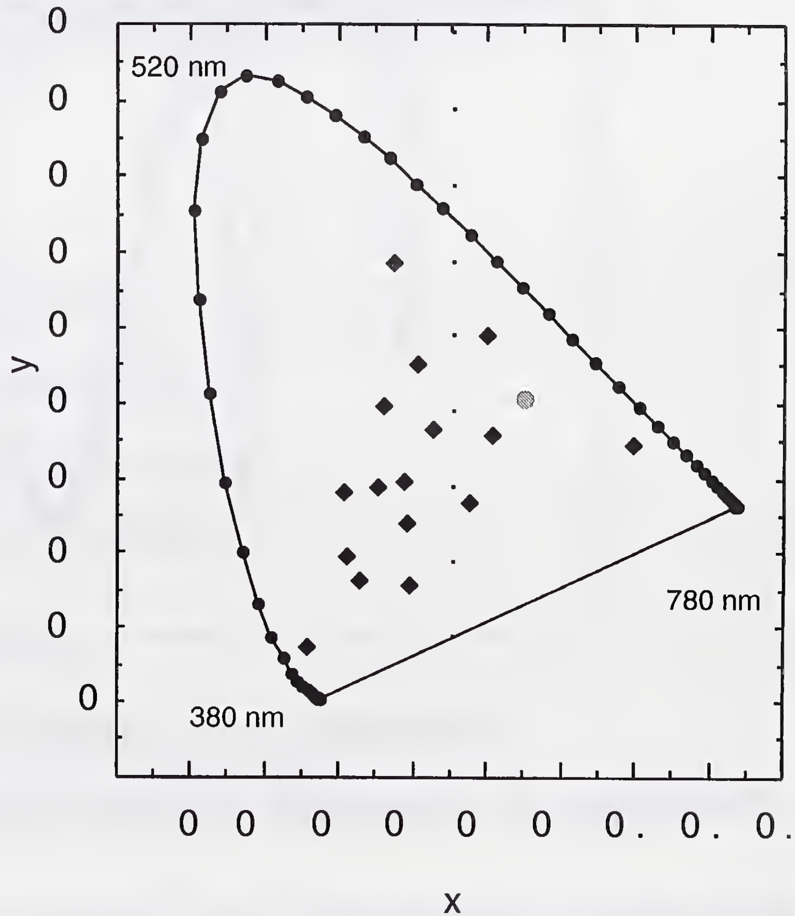
Simulations

Mix Red, Green, and Blue from a Ref. Monitor in different combinations to form colors used in simulations.

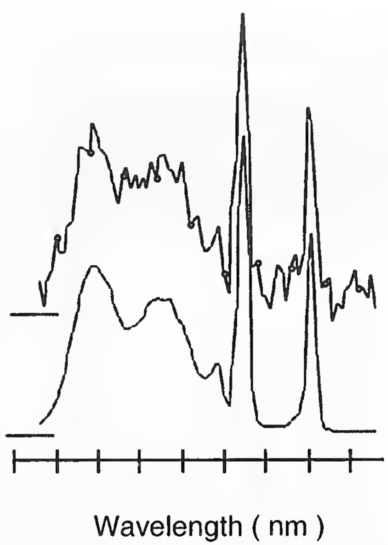


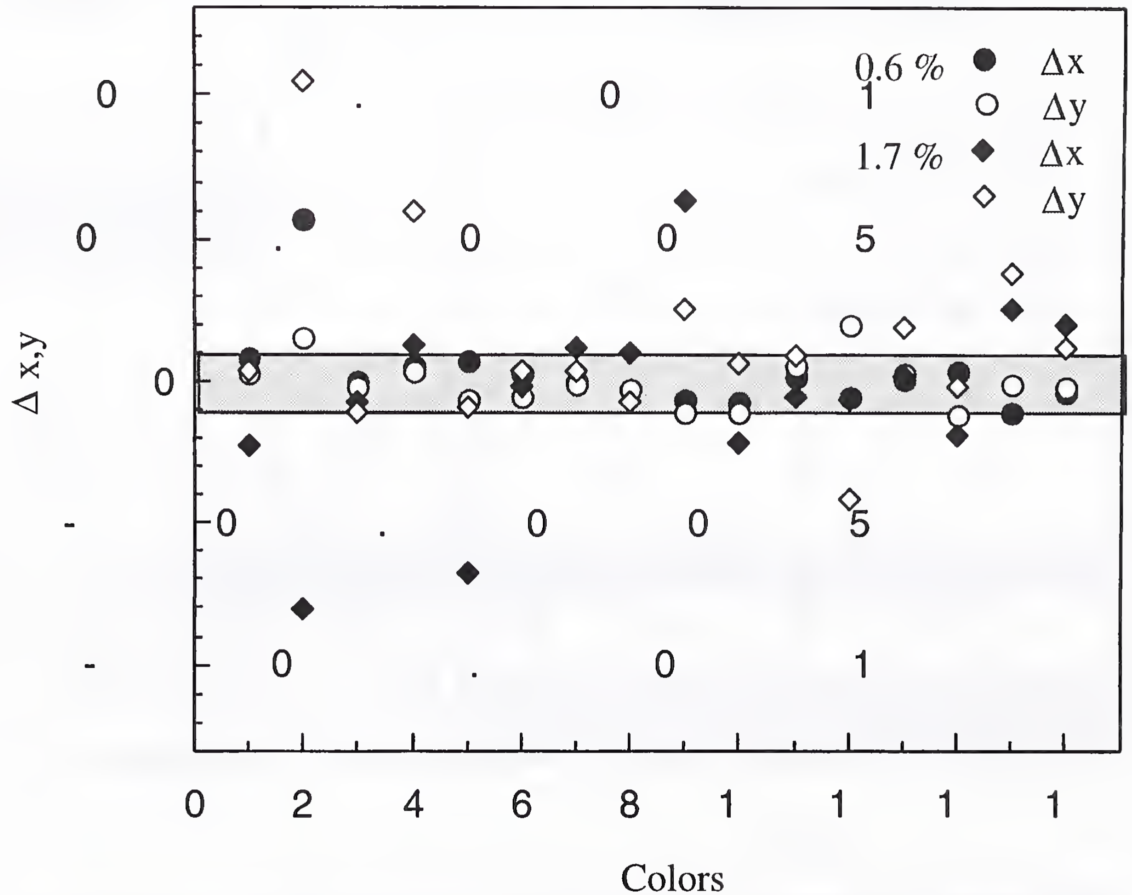
Simulated Colors

Red	Green	Blue
255	255	255
255	0	0
0	255	0
0	0	255
255	255	0
0	255	255
255	0	255
50	100	255
255	50	100
100	255	50
100	50	255
255	100	50
50	255	100
100	50	100
100	100	50
50	100	100

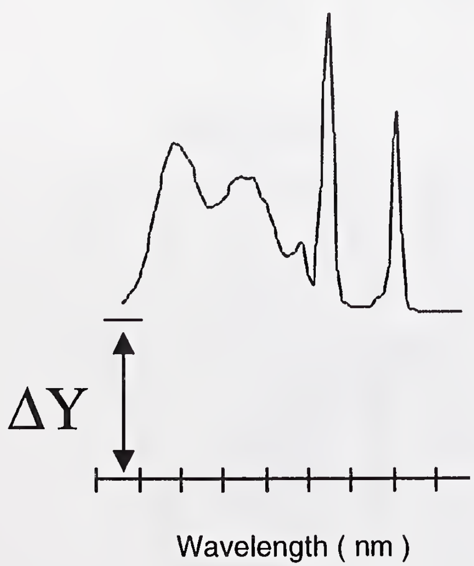


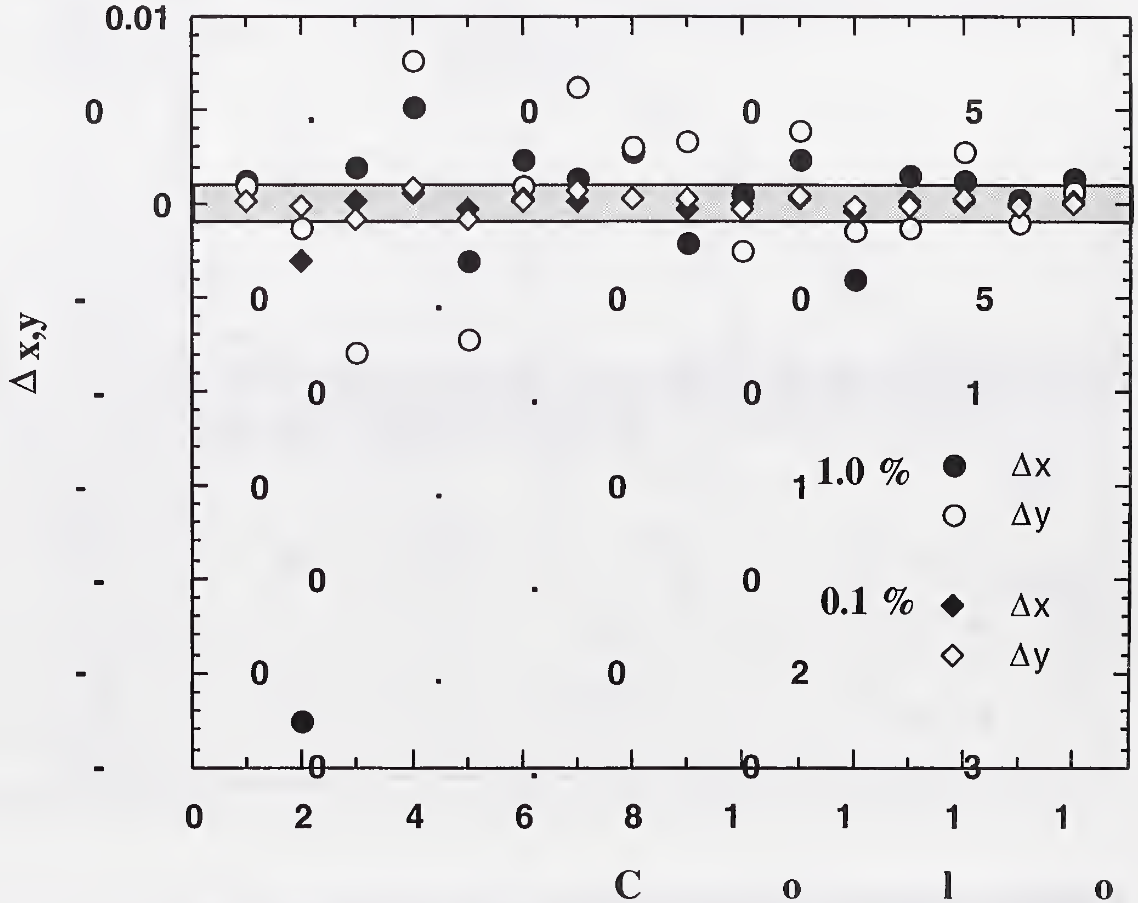
Effects of Random Noise on x,y





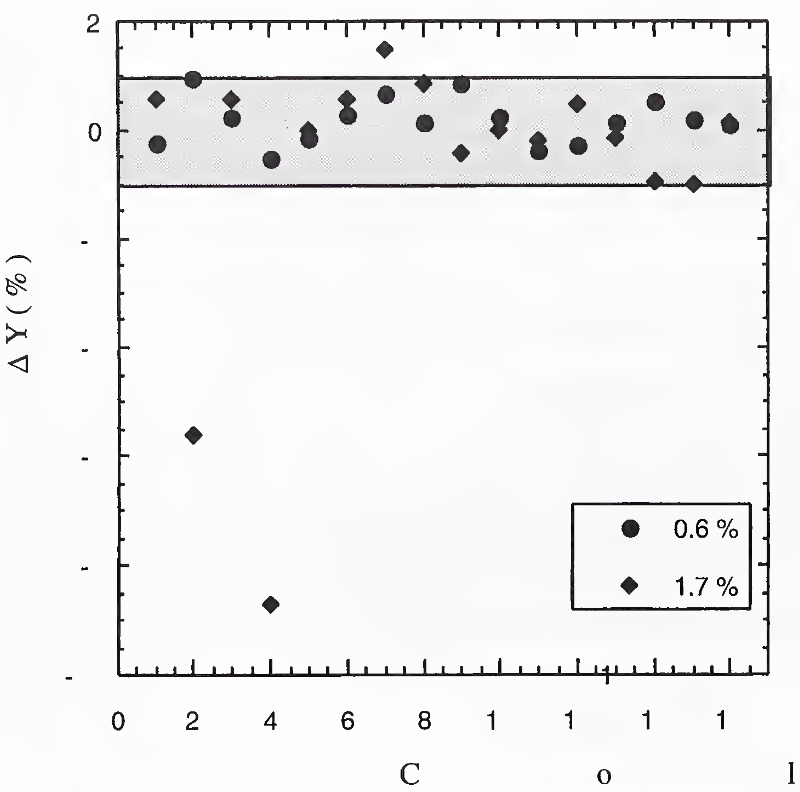
ects of Stray Light on x,y



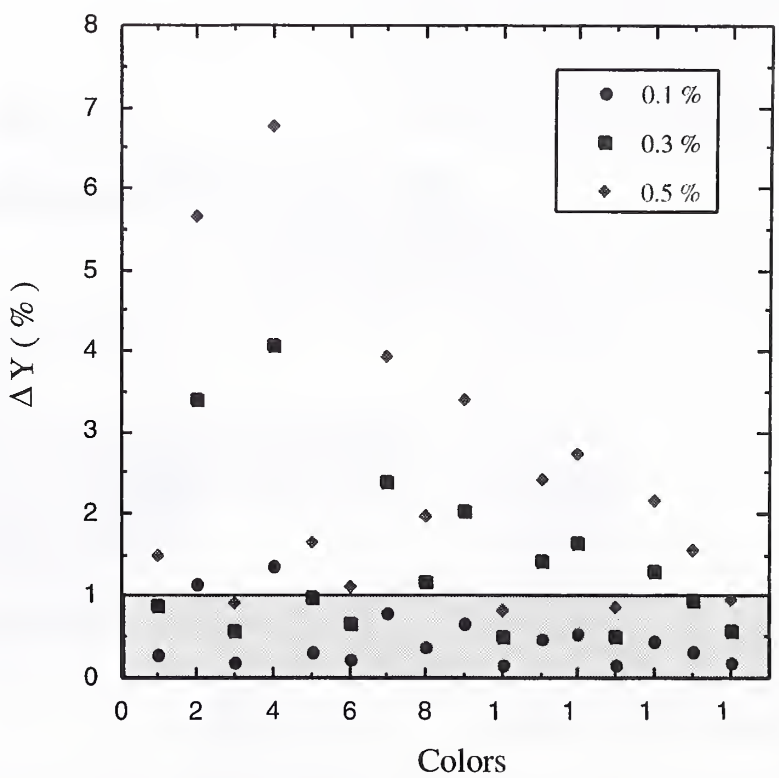


Effects on Y

Random Noise



Stray Light

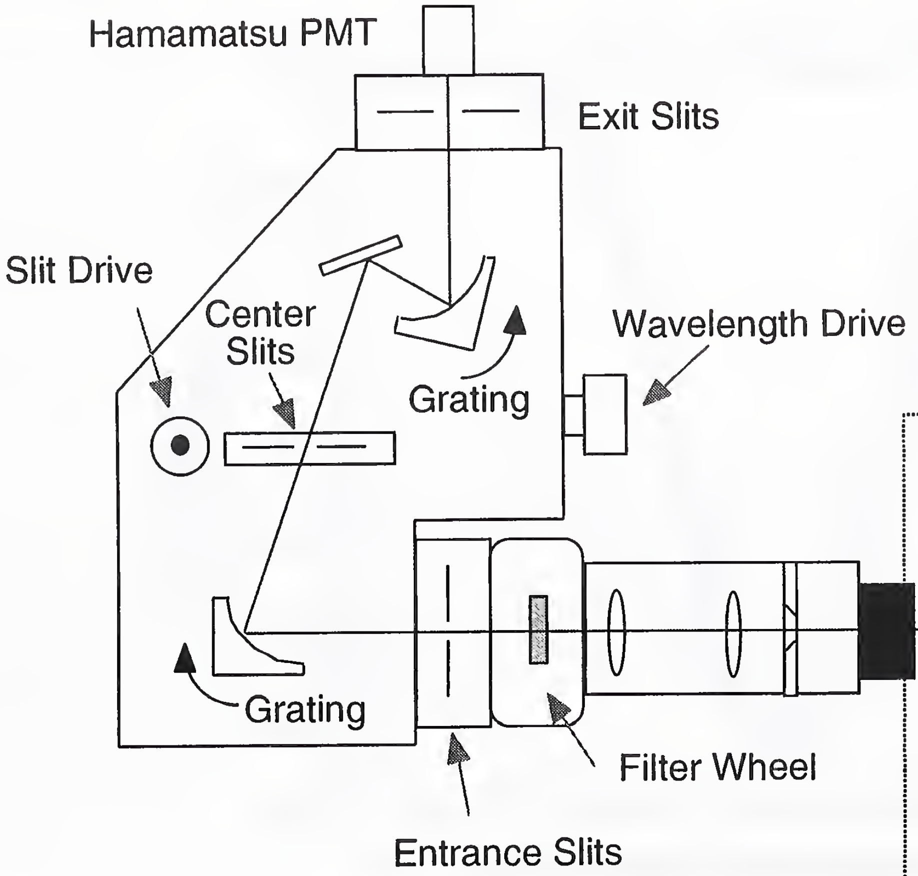


Results of Simulations

- ♦ Measurement noise and stray light can have a large effect on x,y, Y.
  - To achieve +/-.001 in x,y for all colors
    - Noise < 0.5 %
    - Stray Light < 0.1 %.

> Study effects of wavelength error and variable bandpass on x,y.

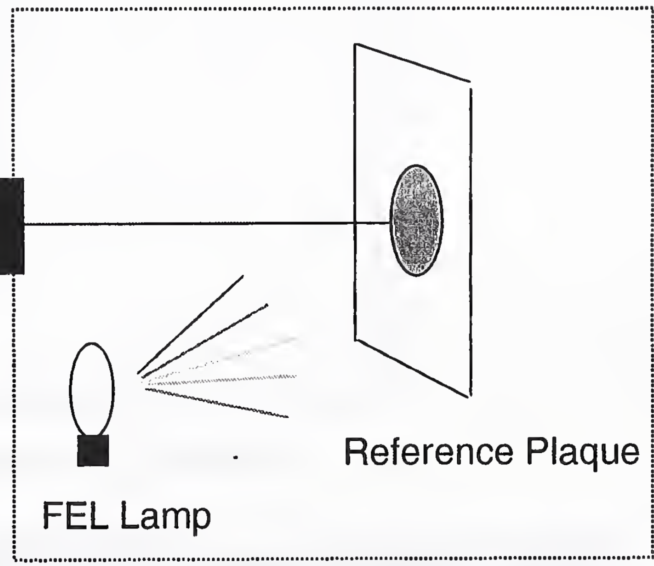
Reference Spectroradiometer



Characterize for

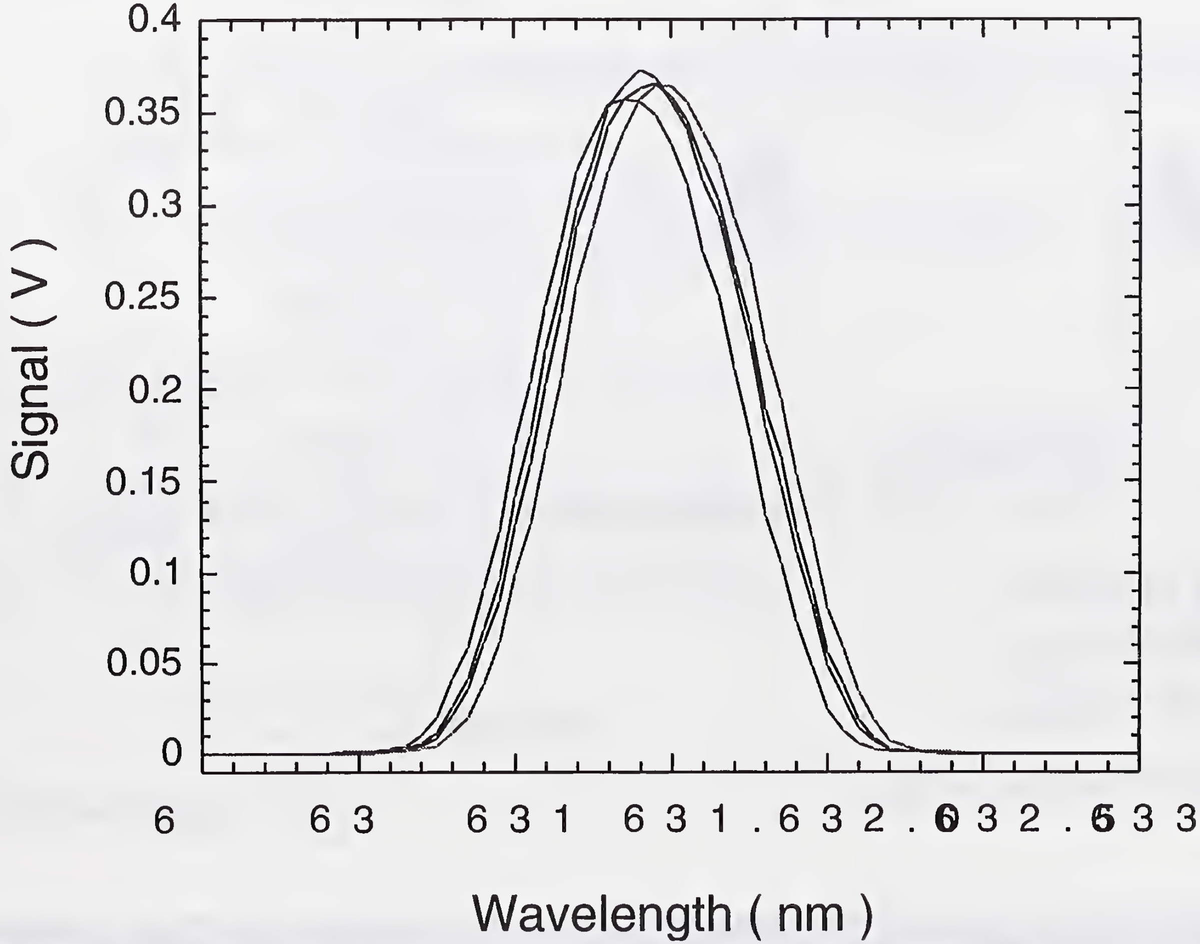
- Stray Light Rejection
- Wavelength Error
- Variable Bandpass

Calibration

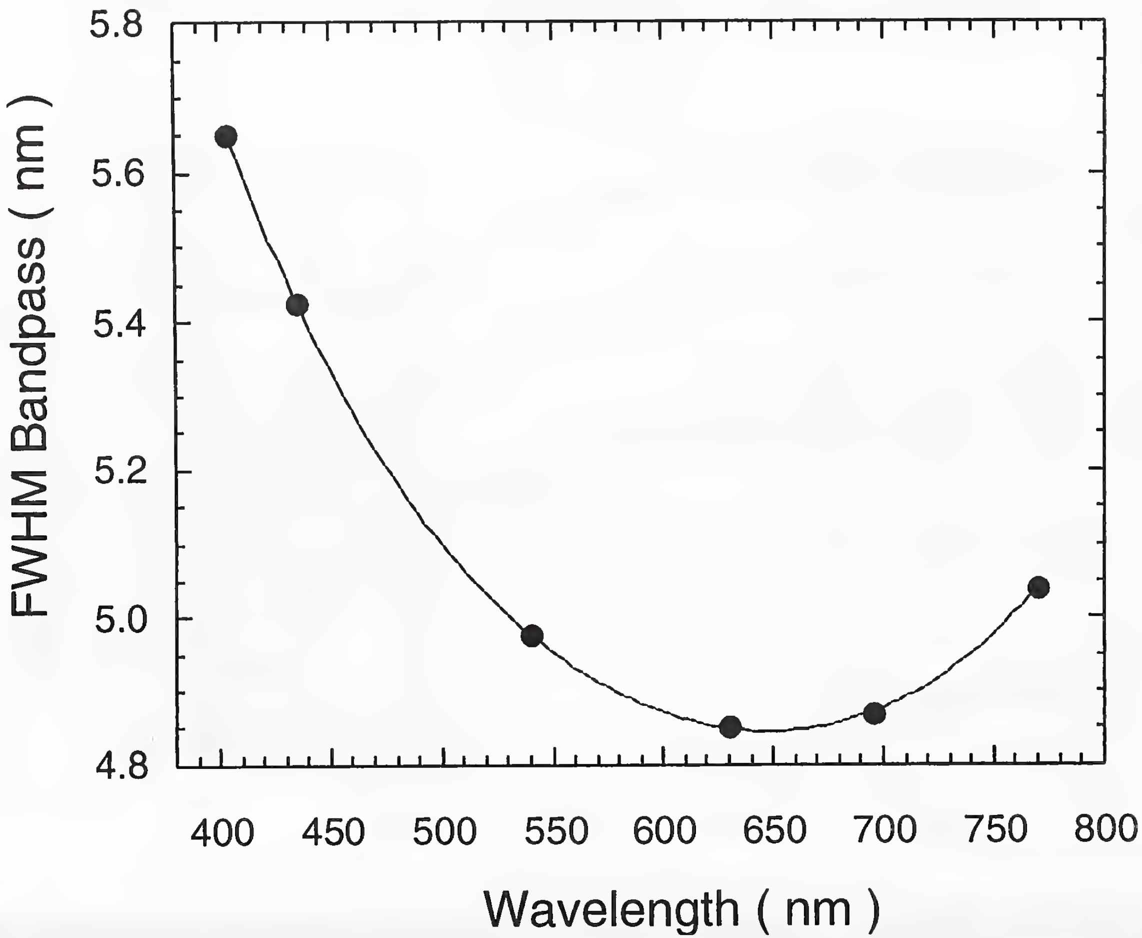


Wavelength Reproducibility

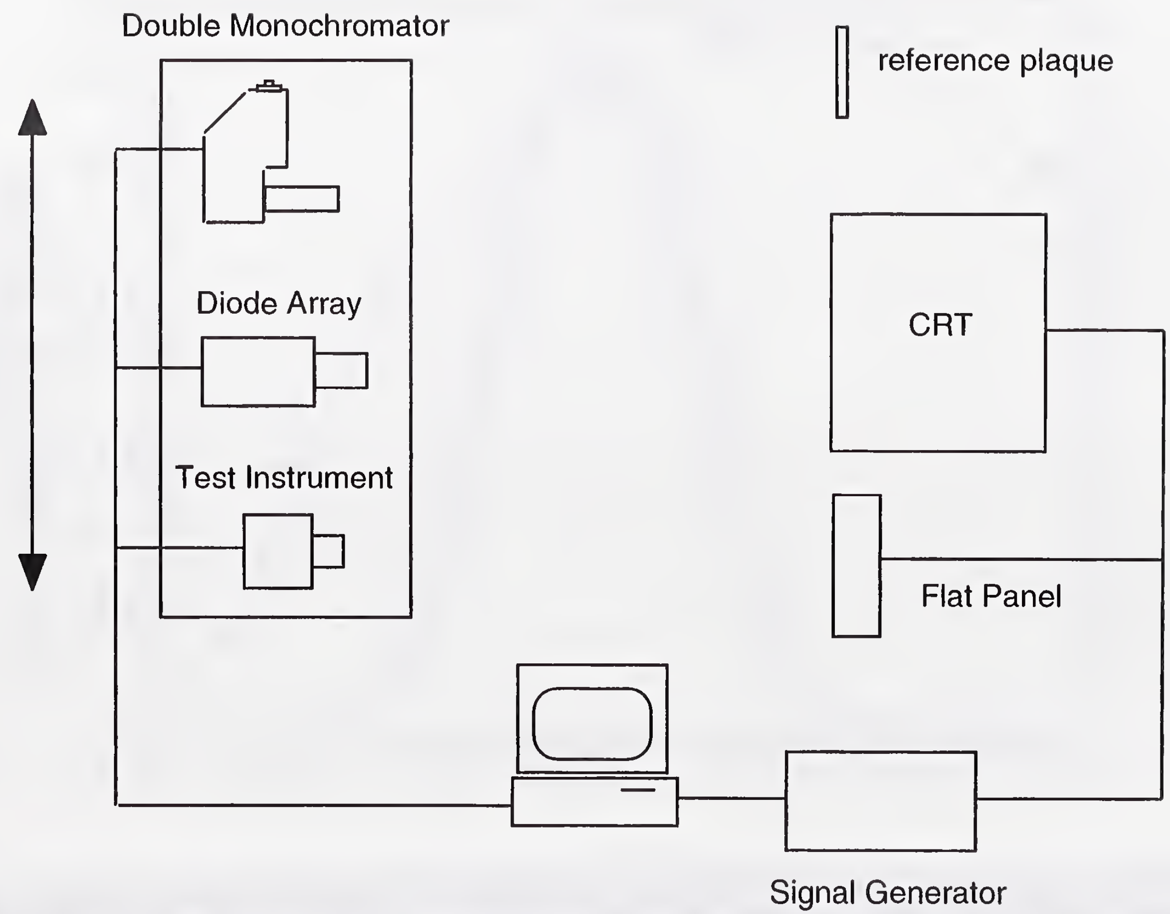
Standard Deviation: .05 nm



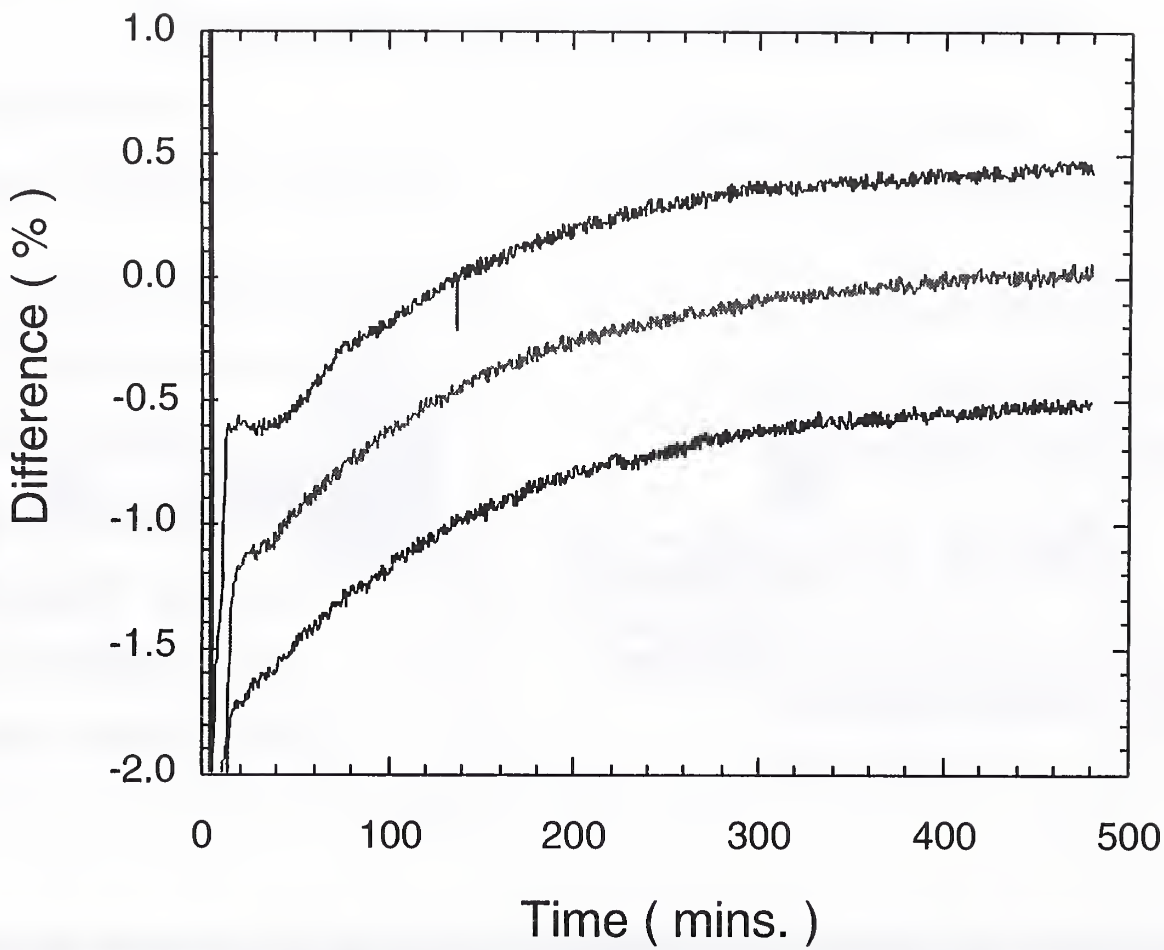
Variable Bandpass



Display Colorimeter Calibration Facility

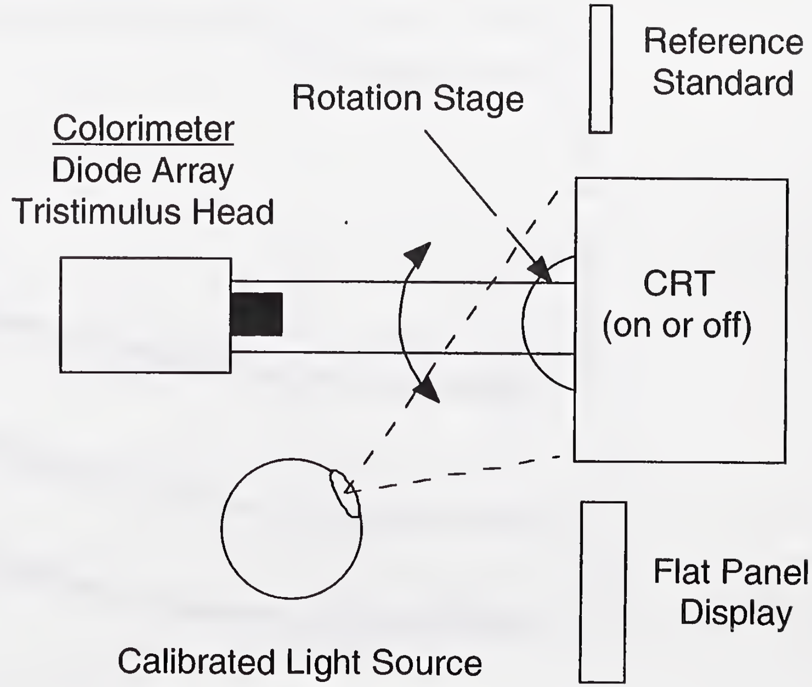


CRT Stability

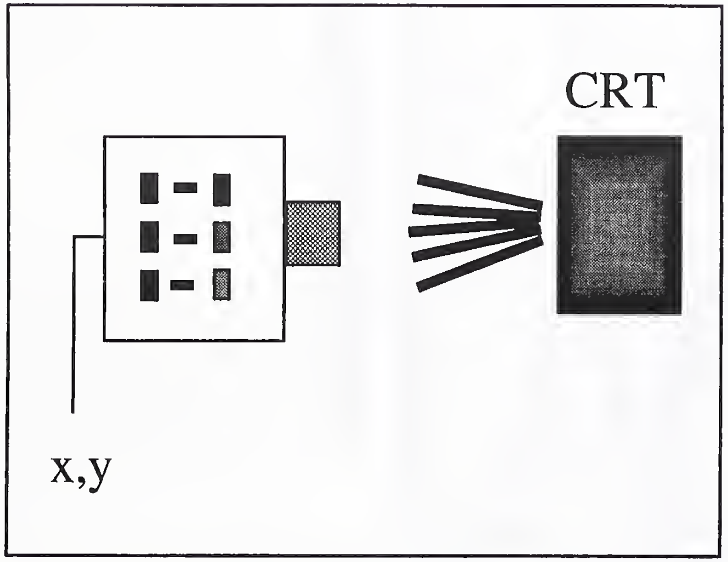


Goniometric Aspects of Color Measurement

- Evaluate spatial and angular aspects of colorimetric VDU measurements including
  - uniformity
  - angular dependence of color measurement
- Evaluate display surface characteristics



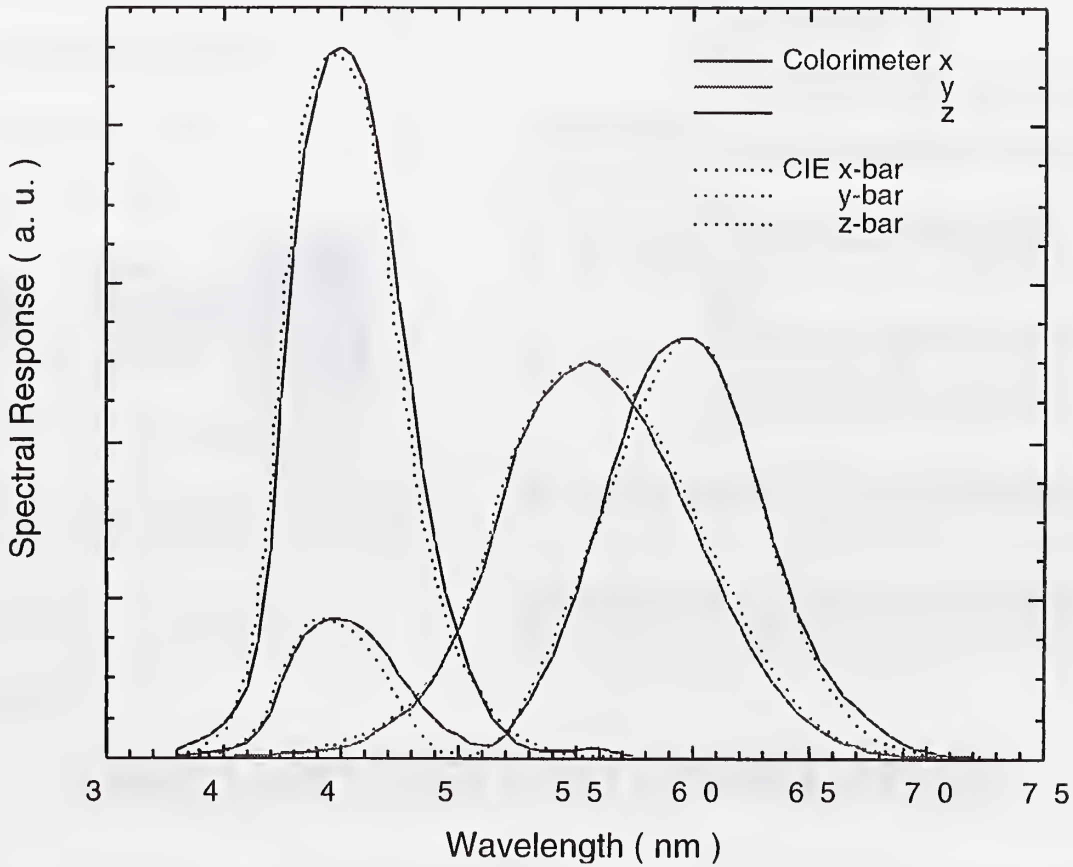
TRISTIMULUS COLORIMETERS



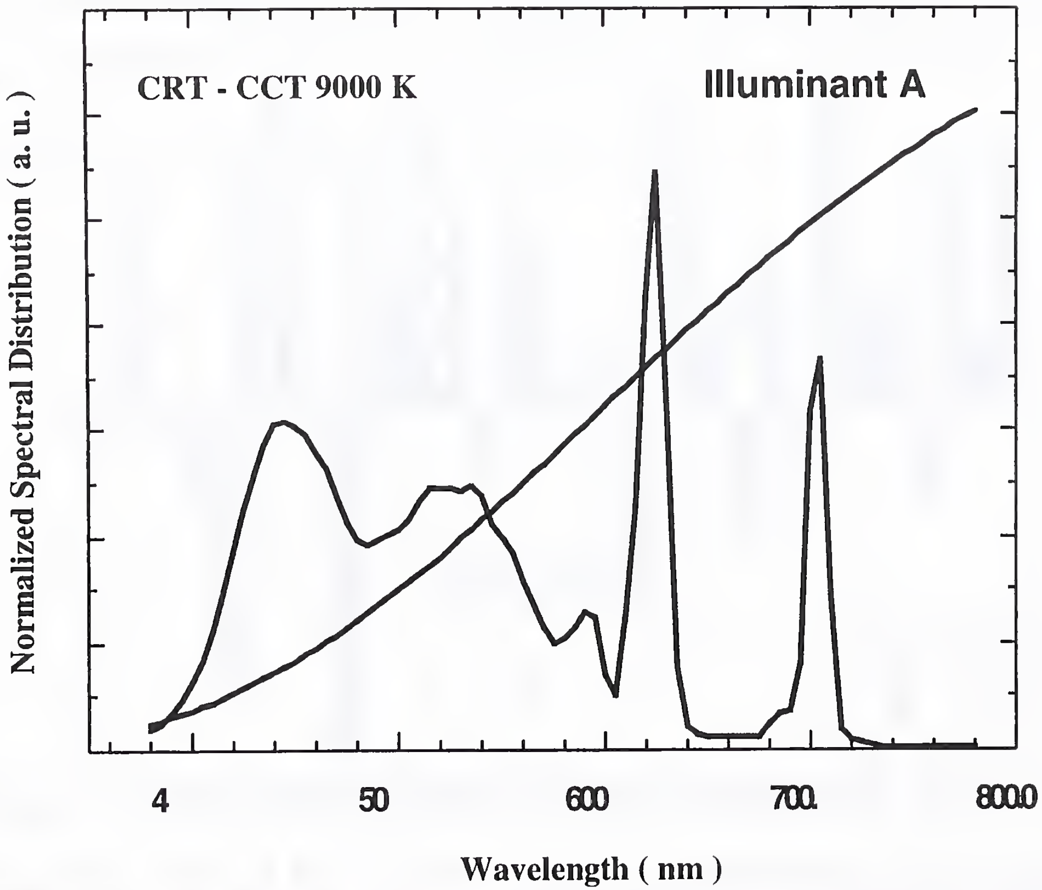
Sources of Uncertainty in x,y

- Accuracy limitations
  - Spectral mismatch is inevitable in tristimulus colorimeters.
- Calibration method
  - Colorimeters are normally calibrated against CIE Illuminant A.

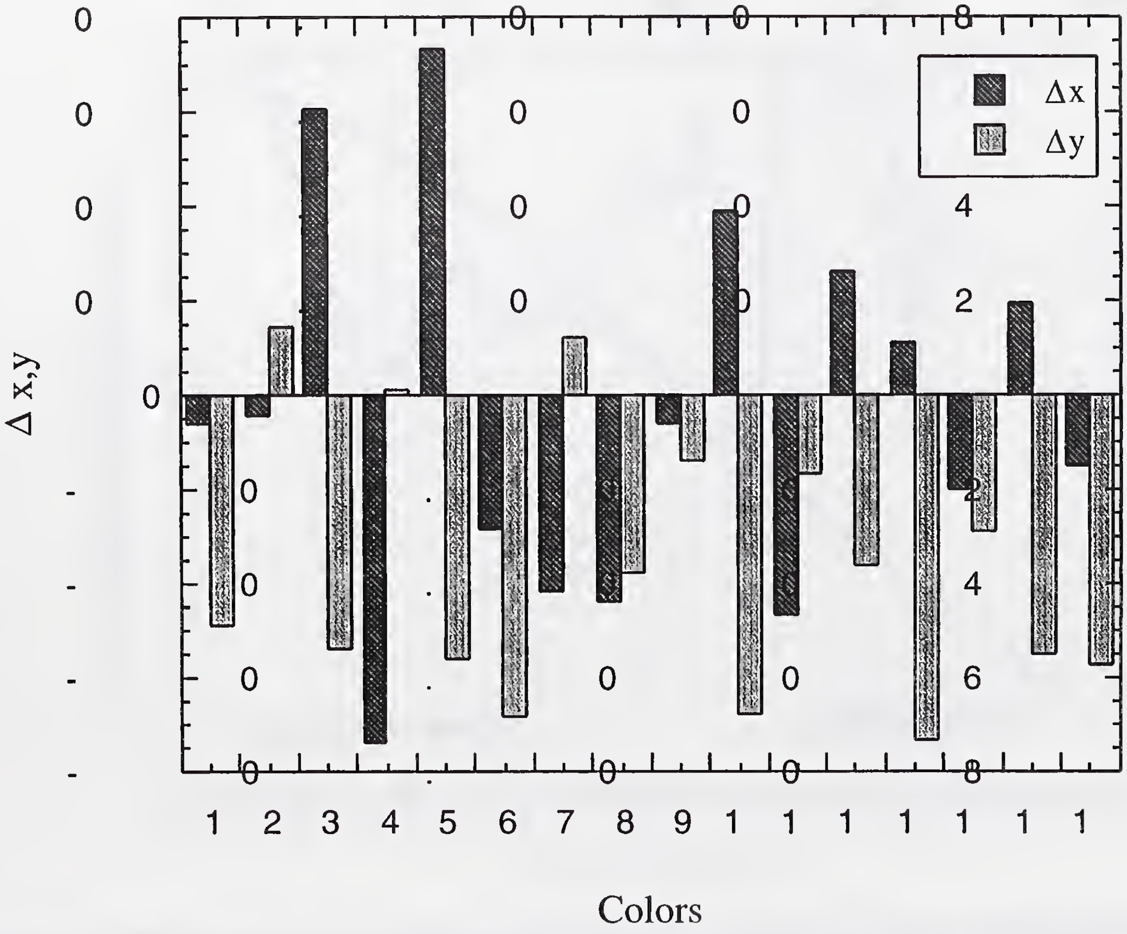
Spectral Mismatch



Illuminant A and CRT RGB



Errors in x,y



Matrix Methods

- Matrix transformations designed to minimize the difference between measured X,Y,Z and actual (ref) X,Y,Z for a number of display colors.

$$\begin{bmatrix} X_c \\ Y_c \\ Z_c \end{bmatrix} = \underbrace{\begin{bmatrix} a & a & a \\ b & b & b \\ c & c & c \end{bmatrix}}_{\text{R}} \begin{bmatrix} X_m \\ Y_m \\ Z_m \end{bmatrix}$$

- Differences between the various methods lie in the approaches used to derive the transformation matrix R.

New Matrix Method

Assumption: Many sources of error mostly affect *Y*.

- ♦ Measurement noise due to flicker effect
- ♦ Instability of display during comparison measurement
- ♦ Measurement instrument nonlinearities
- ♦ Interreflections between the display and the colorimeter

➡ Measurement variation in *Y* is then a major source of *x,y* error using matrix correction methods.

FOUR COLOR METHOD (Y. Ohno and J. Hardis)

Minimizes error in x,y

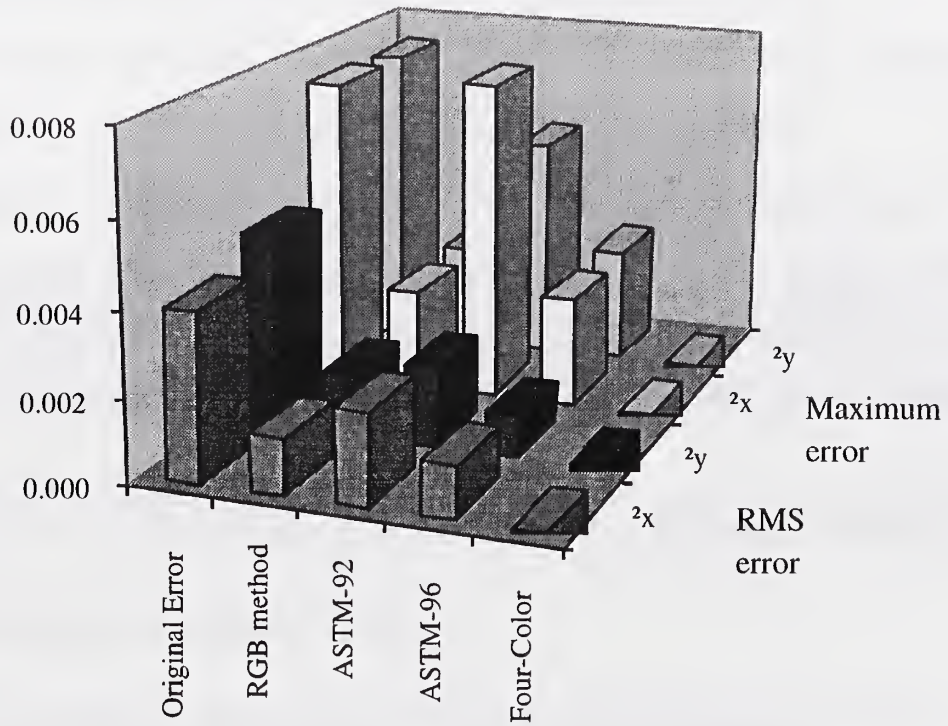
* **Insensitive to errors in Luminance (*Y*)**

New Matrix Method

Y. Ohno and J. Hardis, “Improved Matrix Methods for Tristimulus Colorimetry of Displays,” Proceedings of the 8th Congress of the International Color Association, Kyoto, Japan, May 1997 (to be published).

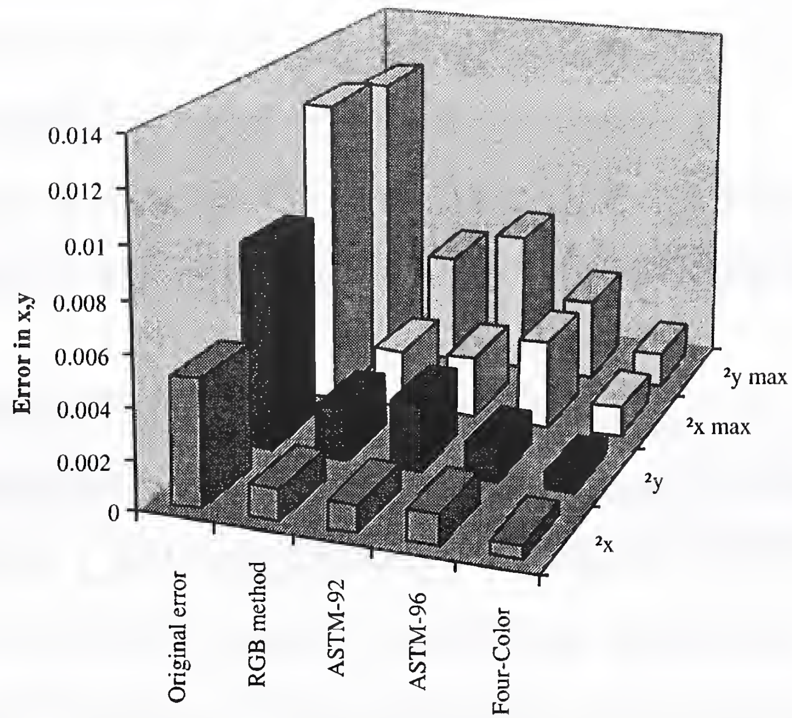
Luminance Noise (1.7 % RMS)

(Average of 10 Readings)



Results of CRT Measurement

Measured 16 colors of a display



Four Color Method

- ♦ Four Color Method has demonstrated the potential to reduce errors in x,y arising from luminance noise.

- > Study effects of different spectral power distributions (from different displays, for example).

y

- Simulations to study contributions of measurement errors — noise and stray light — to uncertainties in x,y and Y.
- Described colorimeter calibration facility.
- Described plans for study of goniometric aspects of display color measurements.
- Evaluated matrix methods used for calibration of tristimulus colorimeters.

VESA/NIST Display Forum '97

Display Measurement Techniques and Standards

By Hector Lara, Photo Research, Inc.

October 20, 1997
Gaithersburg, Maryland

Reliable Flat Panel Display (FPD) measurements have become a necessity in the display industry for manufacturers, system Integrators and researchers. The proliferation of standard methods for measurement is demanding efficient, accurate and repeatable analysis of such displays.

In the simplest form, a suitable measuring system should have five (5) axis motion (for 'viewing angle dependant displays'), an accurate light measuring device (LMD) and Display Under Test (DUT) control. We will discuss such systems along with a unique approach that does not use any motion to perform multi-angle measurements.

Currently there are several solutions that address most of the identified needs to characterize a flat panel display. These systems mostly differ from each other in the method they use to gather the light intensity from the display being measured.

The systems discussed here are:

- ✓ Pritchard Spot Optics
- ✓ Fourier Optics
- ✓ Collimated Optics

Pritchard Spot Optics

(Figures 1A & 1B Below)

An advantageous way is to take a photometer/colorimeter and a spectroradiometer having Pritchard spot optics and integrate them with a high precision five (5) axis motion system that will achieve high accuracy and reproducibility of all light and color measurements.

Pritchard optics provide the means of having a non-ambiguous alignment to the desired area which can be from a few centimeters in size down to a sub-pixel level.

The colorimetric measurements of an FPD in an R&D environment are best performed with a spectroradiometer that is inherently more accurate than a filter colorimeter. The use of a spectroradiometer prevents the user from having to perform additional calibrations to characterize the shortcomings of a filter colorimeter. The advantage is that a spectroradiometer is utilized to perform spectral analysis of the display which provides high accuracy colorimetric analysis that is mathematically derived from the spectral data. Luminance and contrast measurements typically require a system that possesses enough sensitivity, like a PMT based filter photometer. Because of its higher sensitivity, a photometer provides the means to accurately measure the background that is found to be at much lower levels than images (or characters) on a display. It is then reccommended that a combination of a spectroradiometer and photometer is used in high accuracy applications.

Contrary to an R&D environment, in a manufacturing environment a PMT based filter instrument is desirable as it can serve the function of a photometer and a colorimeter.

Such instrument can be calibrated with a known standard (first article display of a production run) to achieve the desired chromaticity accuracy and its inherent sensitivity can be utilized for luminance and contrast measurements. In such application a single instrument (filter photometer/colorimeter) will meet the needs of all measurements.

The motion equipment utilized in these systems are high precision motorized linear and rotary stages. These lend themselves for flexibility in mechanical design to accomodate different instruments and displays types. The DUT controlling of patterns and characters can be carried out using pattern generators or simply displaying canned-patterns. This can all be performed from the computer controlling the photometer (and spectroradiometer) and the motion stages.

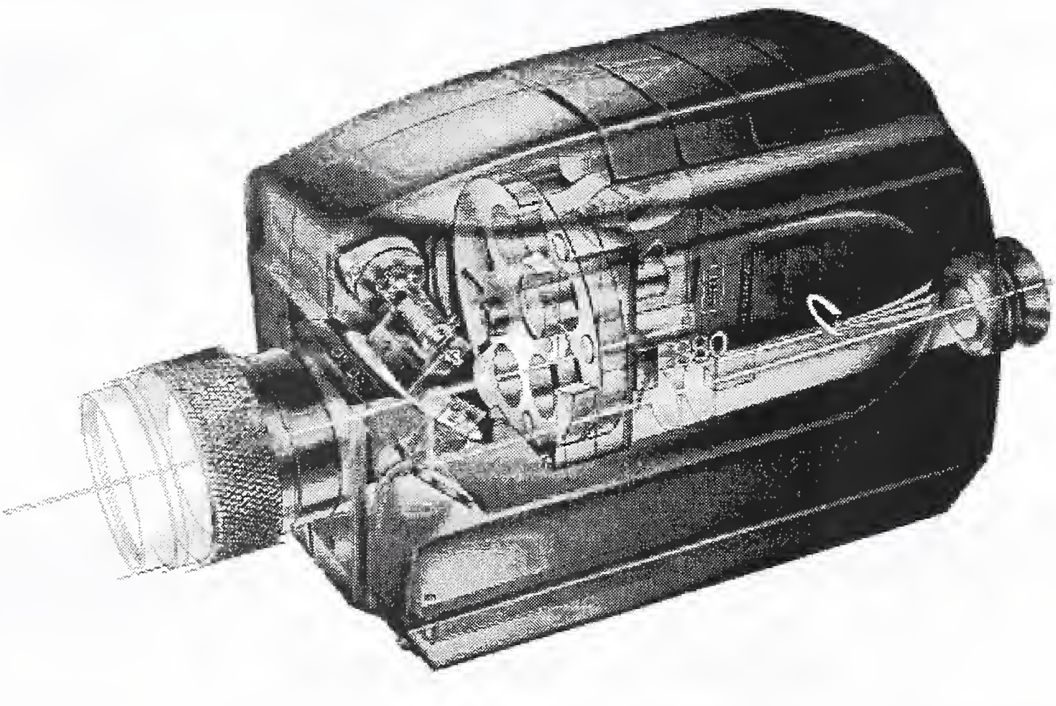


Figure 1A – Pritchard Optical System

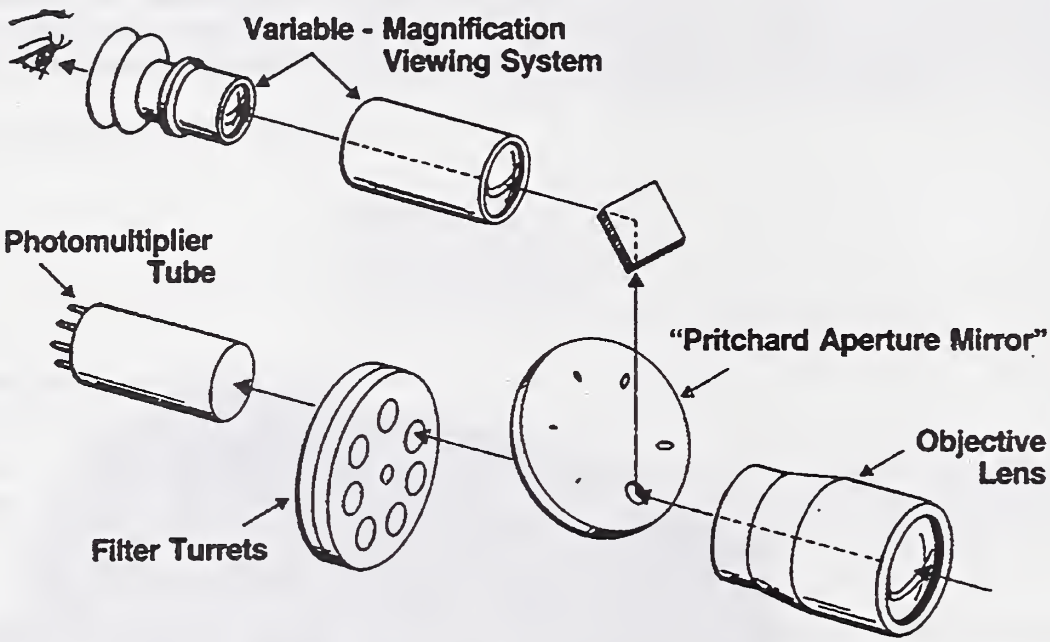


Figure 1B – Pritchard Optical System

Collimated Optics

(Figure 2 Below)

The advantage that this approach presents is that the system can be reduced to a desirable size as simple lens and a fiber are used to navigate in relatively small three dimensional space. These optics are used to transfer the intensity to a single detector or a spectrometer for analysis. The geometry is determined by the lens fiber combination and the measuring angle is typically in the 1° range.

The collection optics in these systems are kept at the goniometer head and its detectors are coupled via the fiber optic to a stationary location.

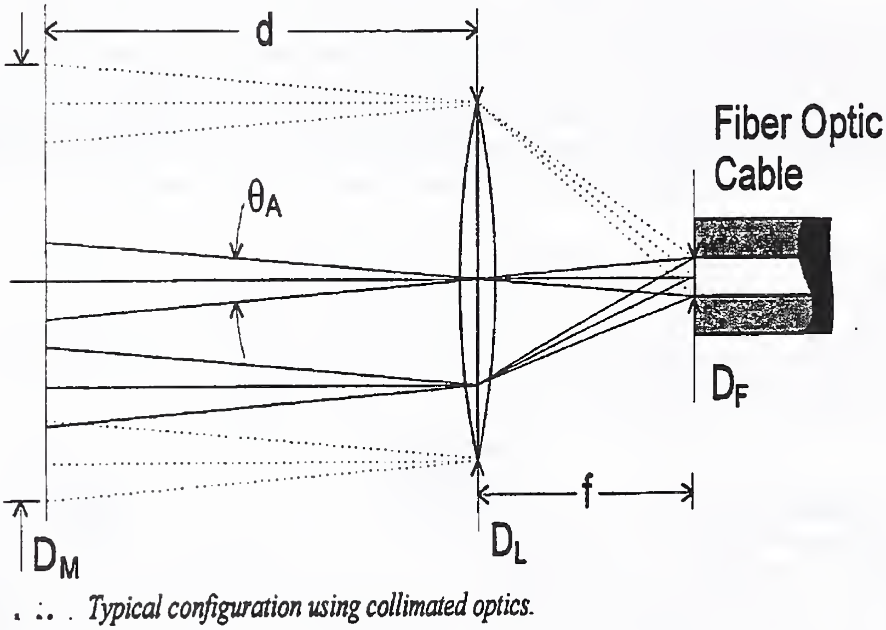


Figure 2 – Collimated Optics (Courtesy of Bruce Denning)

The diameter of the measurement area is controlled by the lens diameter D_L , the aperture angle θ_A , the focal length f, the diameter of the fiber D_F , and the measurement distance d as follows:

$$\theta_A = 2\arctan(D_F/2f), \text{ and } D_M = d_L + 2d\tan(\theta_A/2)$$

The motion in these systems is based on linear motion stages and the angular positioning is achieved by small angular motions of the collection optics (lens/fiber combination).

Fourier Optics

(Figure 3)

Optical-Fourier transform LMDs simultaneously capture data in an up to ± 80° angular range to perform the optical analysis. This means the capture of multiple angles from a single measurement using a two-dimensional array as a detector. In such system the video photometer concept is utilized to take the image collected by a high numerical aperture objective. This energy is then focused at the Fourier plane crated at the focal plane of the objective which is then optically relayed onto the array to evaluate the intensity of each angle collected.

The first lens provides a Fourier transform image of the display surface. Every light beam emitted from the tested area with a θ incident angle will be focused on the focal plane at the same azimuth and at a position x= F(θ). This gives a way to quickly measure the angular characteristics of the sample without any mechanical movement.

Simply, the optical relay system scales the Fourier transform image of the measured surface on the CCD sensor. The captured image is used in order to obtain, after a suitable computation, the viewing angle map of the measured display. A system of this type will capture measuring areas of approximately 1.5mm in size. Further, the system must be moved about the display to analyze different areas of the FPD.

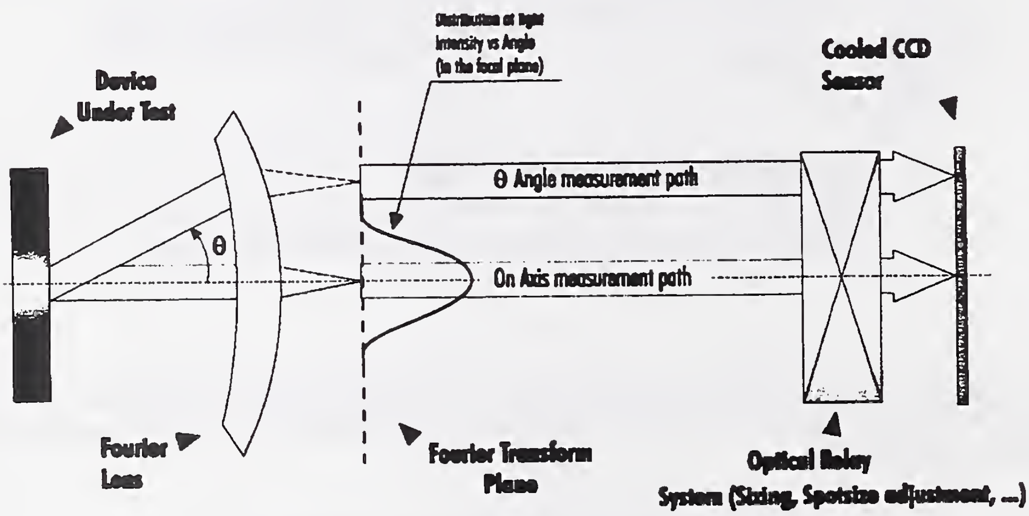


Figure 3 - Optical Fourier Transform Optics (Courtesy of Eldim)

The three configurations shown above have their advantages as well as disadvantages for each specific application. It is suggested that the specifications and capabilities of each system be thoroughly analyzed for best fit to your needs.

Characterizing Measuring Instruments

These systems all share one thing, and that is that they must comply with several characteristics to be useful in the characterization of displays. The CIE (Commission Internationale De L'Eclairage or International Commission on Illuminantion) recommends twelve parameters known as the "f-functions" to fully characterize an LMD. The VESA (Video Electronics Standards Association) FPD Measurements Standard discusses these in a simpler format, but it is reccommended to review the following 'f-functions' to understand the performance of light measuring devices.

To be practical, in the US the Illumination Engineers Society (IES) recommends that at a **minimum f1 through f5** should be performed. The f1 error function specifies that a relative spectral response curve be provided with every filtered function for which the instrument is used. From this data, it is than possible to calculate how the photometer will respond to light sources other than the illuminant A (at 2856 Kelvin) which is what a photometer or colorimeter is typically calibrated with in the laboratory.

The CIE recommends that if only one error is reported, that it should be the f1' error. This error specifies to the user the degree to which the relative spectral responsivity matches the spectral standard observer function $V(\lambda)$ of the human eye for photopic vision. The calculation consists of comparing the systems integrated photopic response to the CIE $V(\lambda)$ function normalized to the illuminant A that is used for calibration. The f1' error is typically presented in percentage with the best commercially available illuminance and luminance meters being at 2 to 3%.

Errors caused by an imperfect $V(\lambda)$ matching can be corrected by knowing the instrument's relative spectral responsivity of its filter(s). The spectral power distribution of the calibration source (2856 Kelvin) and the spectral power distribution of the source being measured. With the proper calculations the f1(Z) error can be derived.

If the spectral power distribution of the source being measured is not known, the CIE has recommended five standard sources for determining the f1(Z) errors. These sources are a fluorescent, high pressure mercury, high-pressure sodium, metal halide and rare earth metal halide. CIE recommends that the manufacturer report the worst error of the five calculated.

The **f2** error function specifies the directional response of a luminance or illuminance meter. For an illuminance meter the CIE recommends characterizing cosine response (f_2), spherical response ($f_{2,o}$), cylindrical response ($f_{2,z}$), and semi-cylindrical response ($f_{2,zh}$). For luminance meters they recommend directional response ($f_2(g)$) and effect from surrounding field ($f_2(u)$).

The typical f2 values for commercially available meters is as follows:

Illuminance Meters	Typical Value
Cosine Response (f_2)	1.5%
Spherical Response ($f_{2,o}$)	10%
Cylindrical Response ($f_{2,z}$)	5%
Semi-Cylindrical Response ($f_{2,zh}$)	5%

Luminance Meters	Typical Value
Directional Response ($f_2(g)$)	2%
Effect from Surrounding field ($f_2(u)$)	1%

The **f3** error function specifies the linearity error of the instrument. The detector in an instrument is usually linear only over a certain range of input levels. Outside this range, the instrument may be nonlinear which must be specified. The CIE recommends that the largest error from each range be reported. The typical linearity errors found in commercially available illuminance and luminance meters is 0.2%.

These errors can be calibrated out in the range of interest by creating a correction table as determined with a calibration source.

The **f4** error function specifies the accuracy of the instrument's display both for analog and digital displays. The CIE recommends that the display error be reported. The typical display errors found in commercially available illuminance and luminance meters is 0.2%.

The **f5** error function specifies the instrument's fatigue (primarily in PMT based instruments), which is the reversible temporal change in the responsivity, under constant operating conditions, caused by incident illumination. Fatigue is characterized by a single numerical value that is presented in percentage. The fatigue value is derived by calculating the ratio of the output signal 10 seconds after the beginning of illumination, to the output signal 30 minutes after the beginning of illumination and presented as a percentage. The test requires temporally stable illumination at a level close to that used in actual measurements. The typical fatigue errors found in commercially available illuminance and luminance meters is 0.2%.

The error due to fatigue can be reduced by exposing the instrument for a short period to the level being measured. The period can be established by conducting the test defined by the f5 error function and determining when the least change occurs due to exposure.

If the above suggested error functions are not available from the manufacturer an independent laboratory or the manufacturer themselves should be able to provide services to perform these tests.

It is of paramount importance that the user of a photometer, colorimeter or spectroradiometer understands all the possible errors that can be accumulated in light measurement. Errors during set-up, which can include the light source type, geometry and all the CIE defined errors that are inherent to the technology being used. The proper understanding and analysis of the instrument will result in high quality displays.

Types of Measurements

Upon characterizing the instrument, the user should establish the accuracy for performing the following measurements:

- ✓ *Luminance*
- ✓ *Contrast*
- ✓ *Chromaticity*
- ✓ *Grayscale*
- ✓ *Response Time*
- ✓ *Uniformity*
- ✓ *Viewing Angle Performance*

  &
- ✓ *Reflection*

Note: Refer to the VESA "Flat Panel Display Measurement Standard" as it addresses these Measurements in detail.

Agreement Between Measurements

Finding the proper light and color measuring system is a large portion of a solution to characterize a display, but measurement correlation may be the most important issue in a business dealing with multiple vendors and technologies.

There must be a clear understanding of all the measurements that need to be performed and assure that everyone involved in the process has the same understanding.

The Importance of Standards

Norms or Standards attempt to establish methodology to a process that can otherwise accumulate excessive errors that are costly if everyone uses their own criteria without agreement. For this reason is that discrete groups of experts have formed around the world to address the needs of their specific industries. Manufacturers are praising these efforts as it brings a better understanding of what their product needs for each type of application. Some of the standards have become more useful than others, but the dedication of each group is immeasurable. Their expertise has been made available to those that may otherwise would have to experience mistakes on their own at a great expense.

Some of the more noted active expert groups are;

ISO/ANSI (International Standard Organization) - The TC 159/SC4/WG2 group is an organization that is represented by countries from all over the world by ergonomic, metrology and video electronics experts. This organization's activities are managed by the ISO and they submit the work developed for review to every member country. In the US this work is managed by ANSI. They meet bi-annually and are actively developing methods that are relevant to visual perception vs. test methods. The ISO FPD standards (Ergonomic Requirements For The Use Of Flat Panel Displays, ISO 13406-1 &-2) are currently being reviewed by the ISO SC4 Secretariat and it is estimated that standards will be released for public use at the beginning of 1998.

SAE (Society of Automotive Engineers) – is a group of experts from the aerospace industry in the United States that have placed emphasis on the procurement of FPDs for aircraft applications. SAE's standards address both design criteria and measurement procedures in two separate documents. These are *SAE ARP4260 (Measurement Procedures)* and *ARP4256 (Design Criteria)*, have been recently completed.

VESA – Flat Panel Display Measurements Standards Working Group has put the most comprehensive measuring standard available for FPDs. Computer manufacturers and integrators have a discrete concern and it is to develop product with the high image quality that a computer user needs for extended use of displays. Having sat in numerous standards committees it is very evident to me that the FPD Measurements Standard is the most useful tool to date.

Others - The ARMY in the US has always given priority to the studies of visual ergonomics and they have ongoing efforts with the above mentioned committees a well as doing their own research.

Conclusion

Priority must be given by manufacturers and integrators to adopt a suitable standard that meets their needs in a practical manner. Analyze your needs to find the proper instrument and clearly understand the standards that you and your vendors are trying to comply with for design and measurements.

Additionally, we must remember that without the contribution and efforts made companies and their employees we would not be able to develop standards like the VESA FPDM. The efforts being lead by the NIST FPD Laboratory. Their efforts are filling a gap that has cost industry large amounts of revenue in the past.

NIDL

PROCEDURE TO VERIFY DIGITAL

COLOR SYSTEMS

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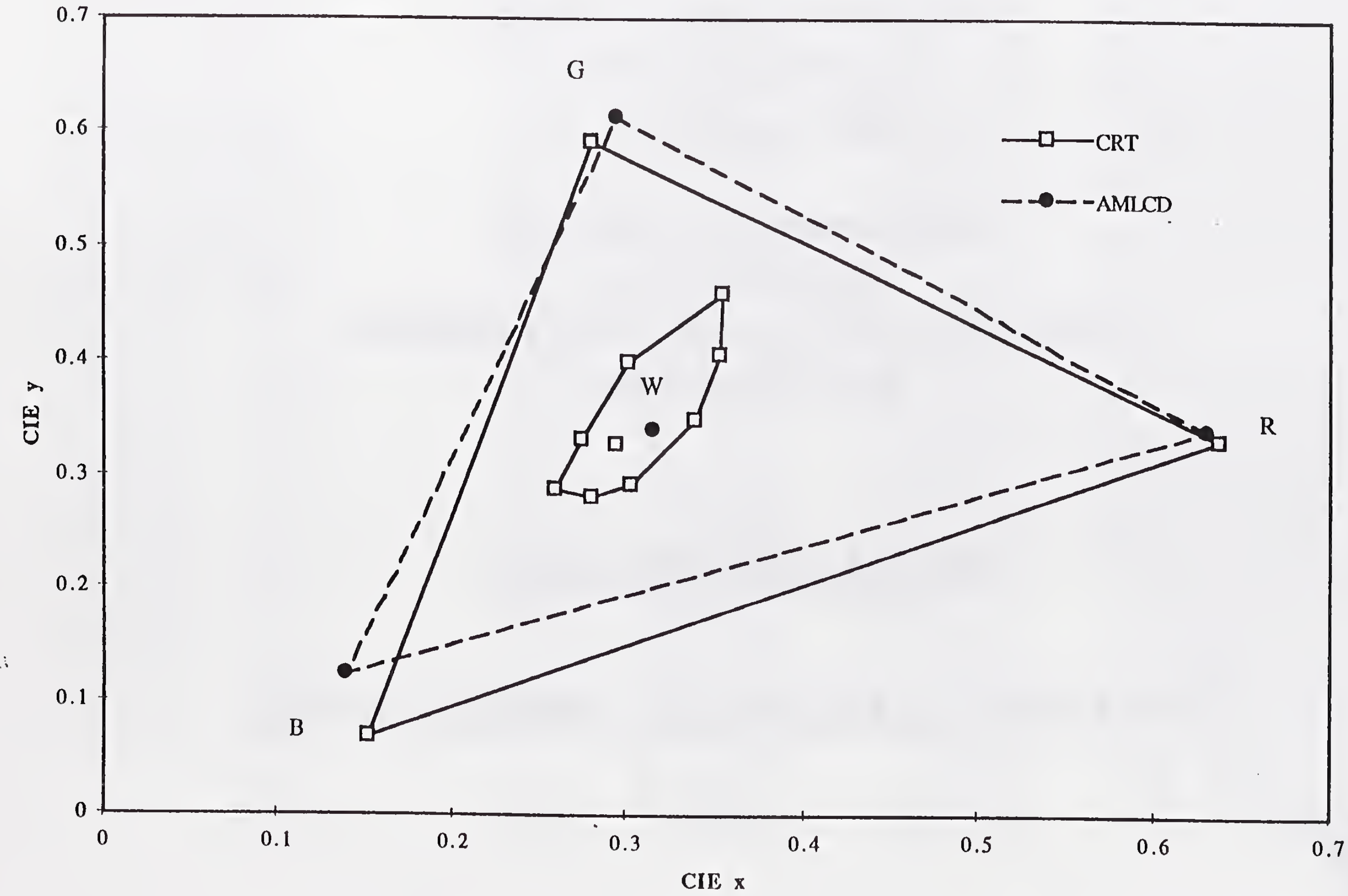
Presentation for Display Forum 97
20 October 1997

CIE (x,y) Plot of Test Colors for Two VDUs

Color Rendering Index Colors
displayed on a CRT



NIDL

APPROACH: ADAPTIVE COLOR TEST PATTERNS

-- Specify target colors that adapt to any VDU's white point

-- Specify digital inputs that make these colors on a standard VDU.

-- Feed test VDU with same inputs, & measure match of actual and target colors for that VDU.

NIDL

KEY CONCEPTS:

-- 9 Full-Screen Low-Chroma Colors

-- Target Tristimulus Values Match CRI Reflectances Under Model Light (Computed)

-- Model Light is Linear Combination of Daylight Eigenvectors that Matches Monitor White (Either Standard or Test)

OFF-LINE PROCESSING

Step 0. Compute tristimulus values (tsv's) of 9 reflectances as if lit by daylight-eigenvector spectra.

Inputs: -- 1931 CIE XYZ color-matching functions $x_j(\lambda_k)$
-- Daylight eigenvectors $S_0(\lambda_k)$, $S_1(\lambda_k)$, and $S_2(\lambda_k)$
-- First 8 CRI reflectances $r_i(\lambda_k)$

Outputs: 81 values.
-- 3x3 matrix A_{mj} (j'th tsv of m'th daylight):

$$A_{mj} = \sum_{k=1}^{31} S_m(\lambda_k)\, x_j(\lambda_k).$$

-- 3 x 3 x 8 array B_{mji} (j'th tsv of i'th CRI reflectance under m'th daylight):

$$B_{mji} = \sum_{k=1}^{31} r_i(\lambda_k)\, S_m(\lambda_k)\, x_j(\lambda_k).$$

NIDL

PREPARE TEST COLORS FOR STANDARD VDU

Step 1. Select VDU & measure its white point $\mathbf{X}_{nR}$.

Step 2. Compute target CIELUV values of CRI reflectances under model light.

-- Compute coeffs $(a_0, a_1, a_2) = \mathbf{a}$ for the l.c. of daylight eigenvectors:

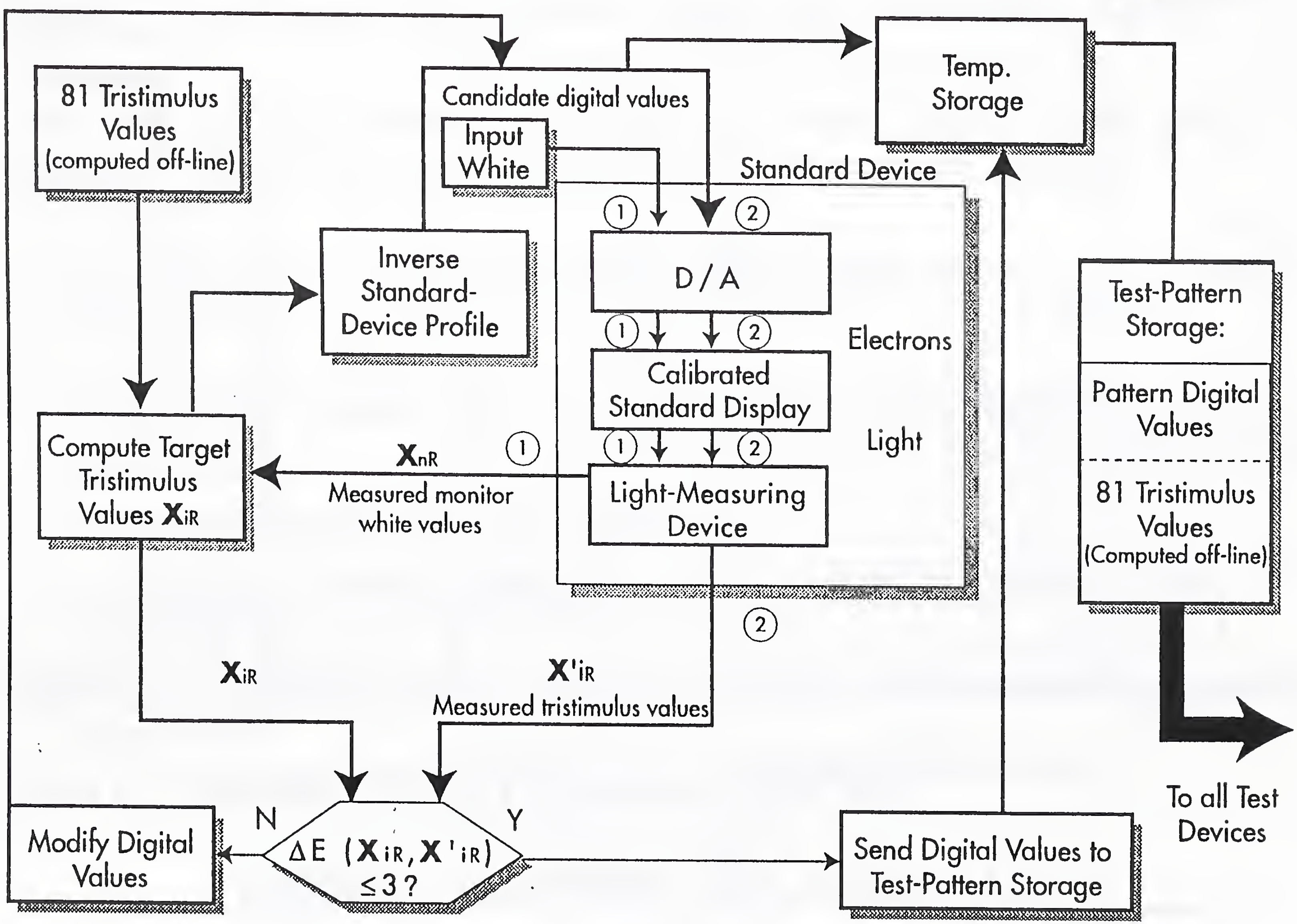
$$\mathbf{a} = \mathbf{X}_{nR} A^{-1}$$

-- Compute 8 target CRI XYZ values:

$$(X_{iR}, Y_{iR}, Z_{iR}) = \sum_{m=0}^{2} a_m (B_{m1i}, B_{m2i}, B_{m3i})$$

-- Convert to CIELUV using white point $\mathbf{X}_{nR}$

Step 3. Select digital colors so measured values match target. Use white point $\mathbf{X}_{nR}$. Criterion: $\Delta E < 3$


81 Tristimulus Values (computed off-line)
Candidate digital values
Input White
Temp. Storage
Standard Device
Inverse Standard-Device Profile
D / A
Electrons
Calibrated Standard Display
Light
Light-Measuring Device
Compute Target Tristimulus Values XiR
XnR
Measured monitor white values
Test-Pattern Storage:
Pattern Digital Values
81 Tristimulus Values (Computed off-line)
XiR
X'iR
Measured tristimulus values
To all Test Devices
N
Y
Modify Digital Values
ΔE (XiR, X'iR) ≤3?
Send Digital Values to Test-Pattern Storage
1
2

VERIFY COLORS ON TEST-VDU

Step 4. Measure test-VDU white point $\mathbf{X}_{nT}$.

Step 5. Compute target CIELUV values under model light.

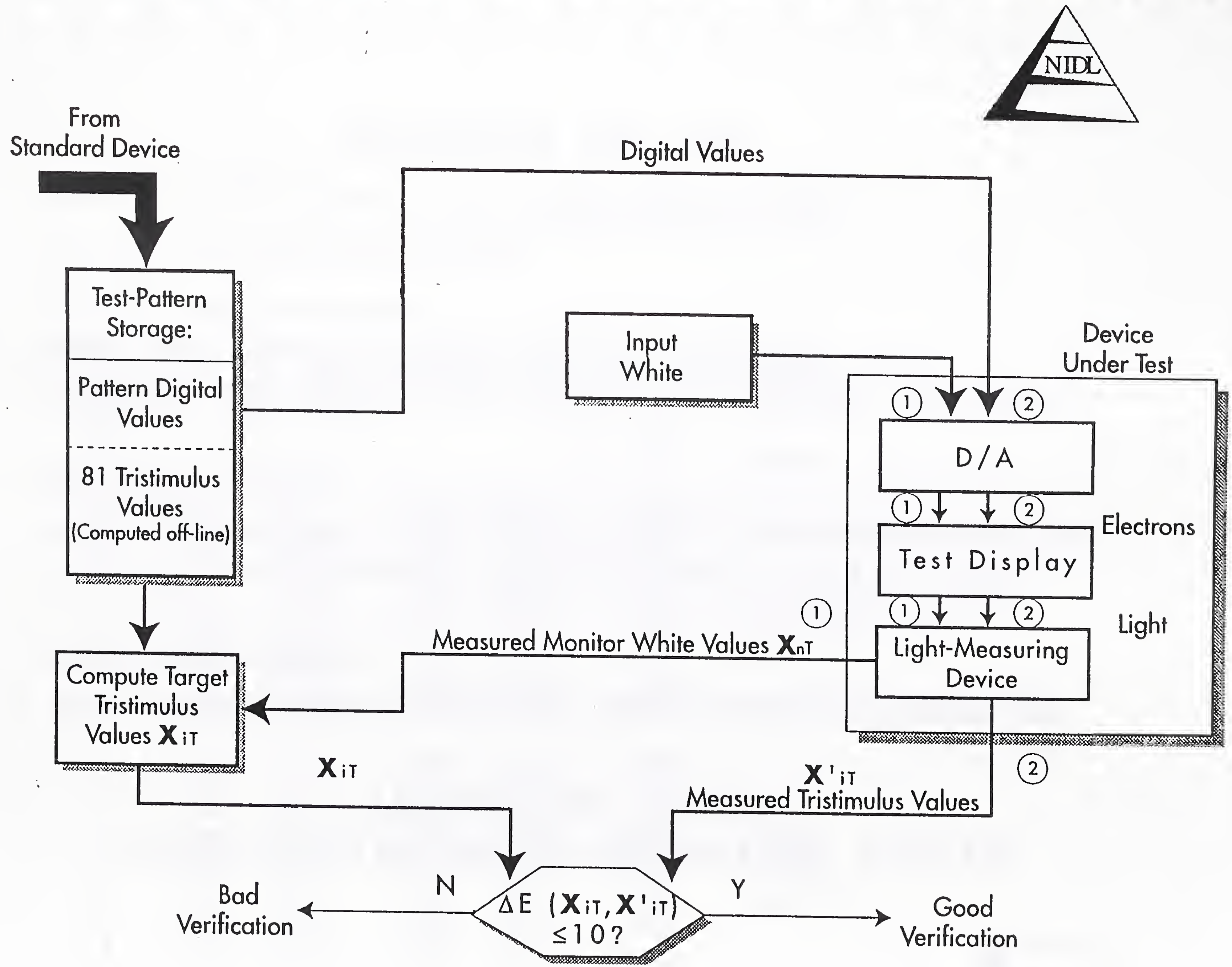
-- Compute coeffs **b** for the l.c. of daylight eigenvectors that matches $\mathbf{X}_{nT}$: $\mathbf{b} = \mathbf{X}_{nT}\,\mathbf{A}^{-1}$

-- Compute target $\mathbf{X}_{iT} = \sum_{m=0}^{2} b_m \,(B_{m1i}, B_{m2i}, B_{m3i})$

-- Convert to CIELUV using white point $\mathbf{X}_{nT}$.

Step 6. Drive test device with standard digital values, measure $\mathbf{X'}_{iT}$, & convert to CIELUV using white point $\mathbf{X}_{nT}$.

Step 7. Compute ΔE between target and measured colors. Criterion $\Delta E < 10$.


NIDL
From
Standard Device
Test-Pattern
Storage:
Pattern Digital
Values
81 Tristimulus
Values
(Computed off-line)
Digital Values
Input
White
Device
Under Test
D/A
Electrons
Test Display
Light
Light-Measuring
Device
Measured Monitor White Values X_{nT}
Compute Target
Tristimulus
Values X_{iT}
X_{iT}
X'_{iT}
Measured Tristimulus Values
N
$\Delta E\ (X_{iT}, X'_{iT})$
≤ 10?
Y
Bad
Verification
Good
Verification

NIDL

COMPARISON WITH PROPOSED SMPTE STANDARD 303M

-- Both derive target tristimulus values using an illuminant-reflectance model.

-- SMPTE pre-computes tristimulus values only for three white points (D65, D55, and 3100K). Our method accepts any white point.

-- SMPTE uses 24 reflectances (including highly chromatic ones), not tuned to testing digital protocols.

EXAMPLE OF USE

-- Standard is a CRT; Test VDU is a laptop computer (LCD).

-- 8-bit (R', G', B') drive both displays.

-- No color-management system.

-- For Std CRT, first digital estimate made with NTSC-based model.

CRI	COMPUTED		MEASURED			
Color	x	y	x	y	ΔE	Display
1	0.343	0.319	0.341	0.322	2.276	
2	0.356	0.390	0.355	0.391	0.656	
3	0.348	0.465	0.348	0.464	0.145	
4	0.265	0.393	0.264	0.391	0.637	STANDARD
5	0.238	0.293	0.238	0.292	0.558	Generator
6	0.222	0.230	0.222	0.230	0.257	CRT
7	0.258	0.226	0.259	0.227	0.628	
8	0.293	0.247	0.292	0.246	1.180	
1	0.374	0.349	0.334	0.352	68.68	
2	0.382	0.413	0.367	0.335	34.42	
3	0.368	0.481	0.381	0.375	49.34	TEST
4	0.285	0.422	0.345	0.441	29.74	Laptop
5	0.259	0.329	0.268	0.423	34.02	Computer
6	0.242	0.265	0.227	0.299	25.95	LCD
7	0.286	0.261	0.208	0.231	39.01	
8	0.326	0.281	0.267	0.245	33.56	

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CONCLUSIONS

-- ΔE values are acceptably small for standard VDU, but not for test VDU.

-- Further work will show if 10-unit criterion is realistic

-- Method shows lots of room for improvement using color-management systems (CMS's)

--> This is a promising way to evaluate a CMS

NIDL

ACKNOWLEDGEMENTS

-- Thanks to Mike Grote at NIDL for his help in reducing this procedure to practice.

-- Special thanks to Art Cobb (NIMA) for his patience in using the procedure for the first time outside NIDL.

-- Sam Grant, NIMA, for support of standards efforts.

-- NIMA for helpful discussions and encouragement

Flat Panel Display Measurement Round Robin Results

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Outline

- Needs
- Approach
- Benefits
- Round-Robin Results
- Lessons Learned
- Conclusions

NTA

NATIONAL IMAGERY AND MAPPING AGENCY

Needs

1. Test methods that have been validated to succeed in actual working environments
   - Comprehensible
   - Practical
   - Reproducible

2. User feedback to foster improvements

Approach

. . . obtain user feedback through round-robin experiments . . .

Provide and circulate displays to measure according to the standard methods

- Sample a wide variety of laboratory conditions
- Test a wide variety of measurement equipment
- Allow individual preferences to impact the set-up

Benefits

Proven standardized test methods

- Early exposure to ambiguities
- Identification of impracticalities
- Fewer revisions

Round-Robin Participants

. . . so far . . .

Autronic-Melchers, Germany

Eldim, France

Microvision, CA.

NIDL, NJ

NIST, MD

Photo Research, CA

SUN Microsystems, CA

TUV Rheinland, CA

Measurement Equipment

. . . a wide variety of manufacturers . . .

- Autronic-Melchers
  - DMS-501 System (Goniometer)
  - PMT-3 Photometer
  - CCDspect-2 Spectrometer
- Eldim EZContrast (Fourier Optics)
- Microvision SS220 Photometer (Goniometer)
- Minolta CL100 Spot Photometer
- Photo Research
  - PR-1980 Spot Photometer
  - PR-704 Spectroradiometer
  - PR-880 Spectroradiometer
- Princeton Instruments CCD Array
- TopCon BM-7 Spot Colorimeter

NTA

Displays

. . . .a sampling of two very different LCD technologies . . .

Two 10.4” 640 x 480 Laptop Computers

- Active Matrix LCD
- Passive Matrix LCD

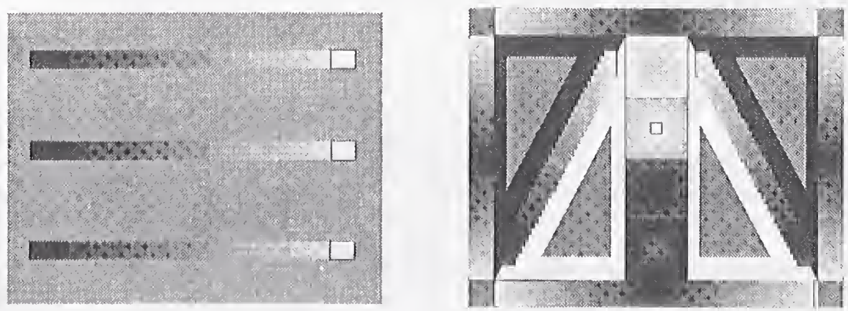
Suite of Basic Measurements

. . . a minimum "core" set of metrics . . .

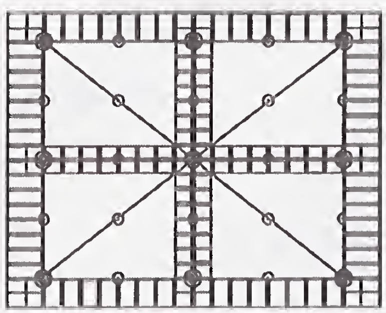
1. Setup
   - Brightness
   - Contrast
   - Others
2. Full-Screen Center
   - White
   - Black
   - Contrast Ratio
   - Colors
   - Gray Scale
3. Viewing Angle
   - Horizontal
   - Vertical
4. Shadowing
5. Ambient Contrast
6. Response Time
7. Uniformity
   - White
   - Black
   - Colors

Test Patterns

. . . provided using PowerPoint . . .



Gray Scale Set-Up

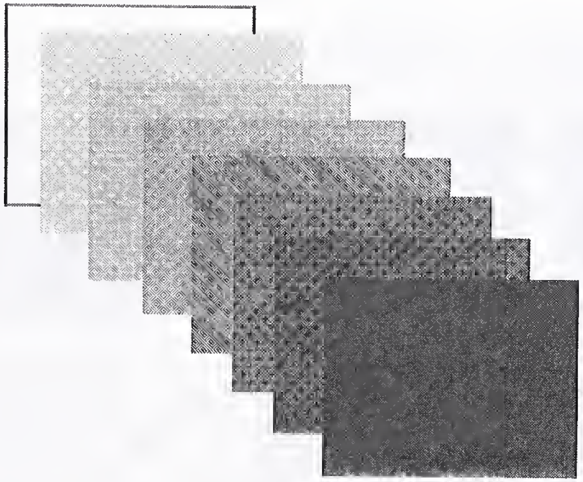


Test Points

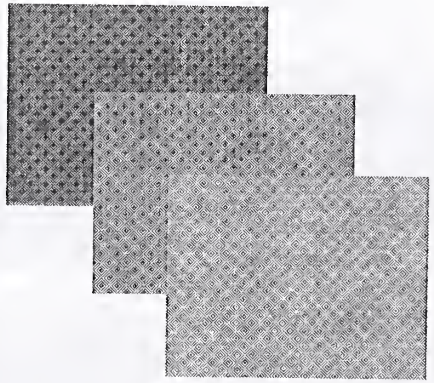
Full White and Black

Test Patterns

. . . for measurements of Grayscales and Primaries . . .



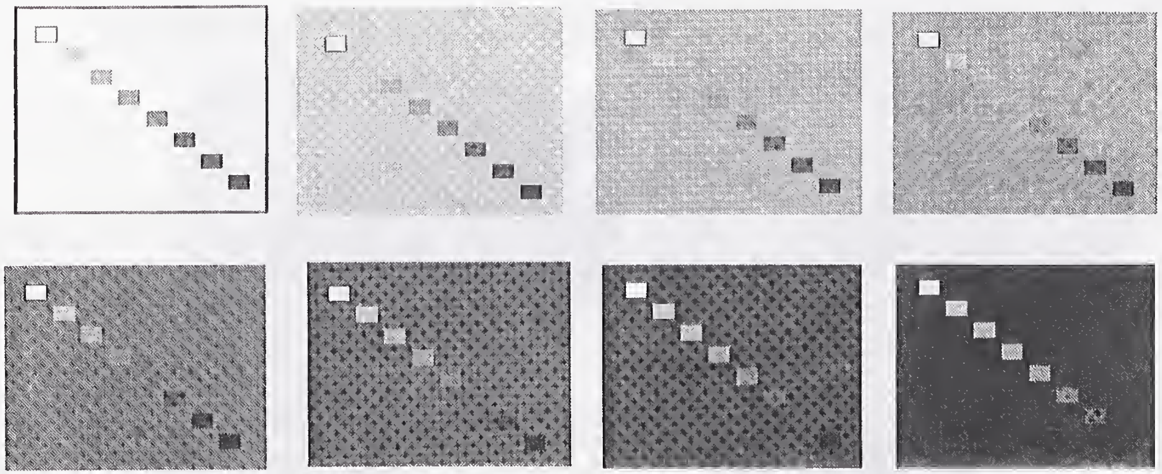
8-levels of Gray Scale



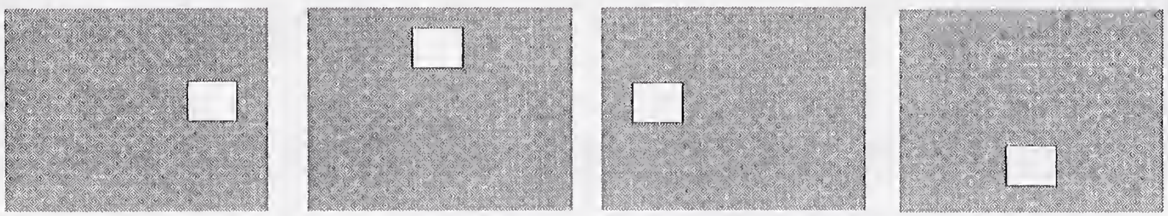
R,G,B Primaries

Test Patterns

. . . for measuring Crosstalk (Shadowing) . . .



Identification of worst-case crosstalk



Photometric measurement

Report Sheet

. . . an organized presentation of the measurement results . . .

FLAT PANEL DATA RECORD — SUITE OF BASIC MEASUREMENTS — *SAMPLE DATA*

DISPLAY INFO: Manufacturer: Whatever Co Model No: B119 Serial No: 123456 Rev. Level: A

DESCRIPTION: Diagonal Size: 375 mm Pixels: 640 (hor) × 480 (ver) Technology: DSTN

PITCH: Horizontal: Pixel: 0.489mm/px Subpixel (Dot): varies Other: ______ Viewing Direction: Perpendicular

Vertical Pixel: 0.489mm/px Subpixel (Dot): varies Other: ______ Location of Center Meas.: Center

COLORS: Bits/color: 6R,6G,6B Color bits: 18 Gray Levels: 64 Total Colors: 256 Signal Source: Internal Power Source: Internal

SIZE: Active Area: 300 mm (hor) × 225 mm (ver) LMD: Make: Wowor Model: 123 Serial No: 12345 Distance: 500 mm

OVERALL: Dimensions: 350 mm (hor) × 275 mm (ver) Depth: 27 mm Mass (weight): 0.621 kg AFOV: 1°

Test Person: Albert Date: 8/24/97 Warm-Up Time: 22 min Temperature: 21.2 °C Run: #1 Page 1/2

Full-Screen Center (302-1...4)

	L cd/m²	x	y
White	96.2	0.277	0.285
Black	0.411	0.247	0.242
C_R	234	No Units for C_R	
Red	28.9	0.594	0.319
Green	48.1	0.299	0.606
Blue	19.3	0.145	0.068

Full-Screen Gray Scale (302-5)

Level	L cd/m²	Opt-16	L cd/m²
Wht-7	106	Wht-15	
6	81.3	14	
5	55.6	13	
4	33.6	12	
3	17.4	11	
2	7.14	10	
1	1.68	9	
Blck-0	0.084	8	
Gamma	2.17		

Uniformity: Nonuniformity = 100% × [1-(Min/Max)] (306-1...4)

9 point	5 point	L_w	L_b	C_U	x	y	CCT(K)
1	1	109	1.02	107	0.250	0.650	
2							
3	2	87.8	0.91	96.5	0.235	0.690	
4							
5	3	115	1.05	110	0.250	0.700	
6							
7	4	75.1	2.15	34.9	0.262	0.765	
8							
9	5	97.3	1.53	63.6	0.225	0.722	
Ave.		96.8	1.33	82.4	0.244	0.705	
Min.		75.1	0.91	34.9	0.235	0.650	
Max.		115	2.15	110	0.262	0.765	
Nonuniformity		35%	58%	68%	10%	15%	
Anomalous Low		125					
Anomalous High		55.3					
Anom. Nonunif.		56%					

Power Consumption (401-1)

Pattern Used:

Supply		Volts	I(A)	(W)
Panel	High	5.50	0.523	2.88
		5.00	0.507	2.54
	Low	4.50	0.467	2.10
Inverter	High	12.5	0.628	7.85
		12.0	0.602	7.22
	Low	11.5	0.571	6.57
Other	High			
	Low			
TOTAL	High			10.73
				9.76
	Low			8.67

Conversion Efficiency (402-1)

White Full Screen	
Power in, P (W)	10.73
Light out, L_W (cd/m²)	102
L_W/P (cd/m²W)	9.51

Response Time (305-1)

Blk-Wht	17	ms
Wht-Blk	23	ms
Total	40	ms

Ambient Contrast (308-2)

White L_{AW}	196	L_W	105	L_b	0.512	L'_W	112	L'_b	3.21
Black L_{AB}	94	L_{aw}	180	L_{ab}	61.9	L_{std}	63.25	ρ_{std}	0.98
C_A	8.09	E (lx)	207			E_L	500		

Shad. = 100%(L_{box}-L_{bkg})/L_{bkg} (303-4)

Box at (A-E)	C	Lum. (cd/m²)	
Box (0-7)	0	L_{box}	95.0
Bkgnd. (0-7)	7	L_{bkg}	103
Shadowing %	7.8%		

Viewing Angle (307-1 or 2)

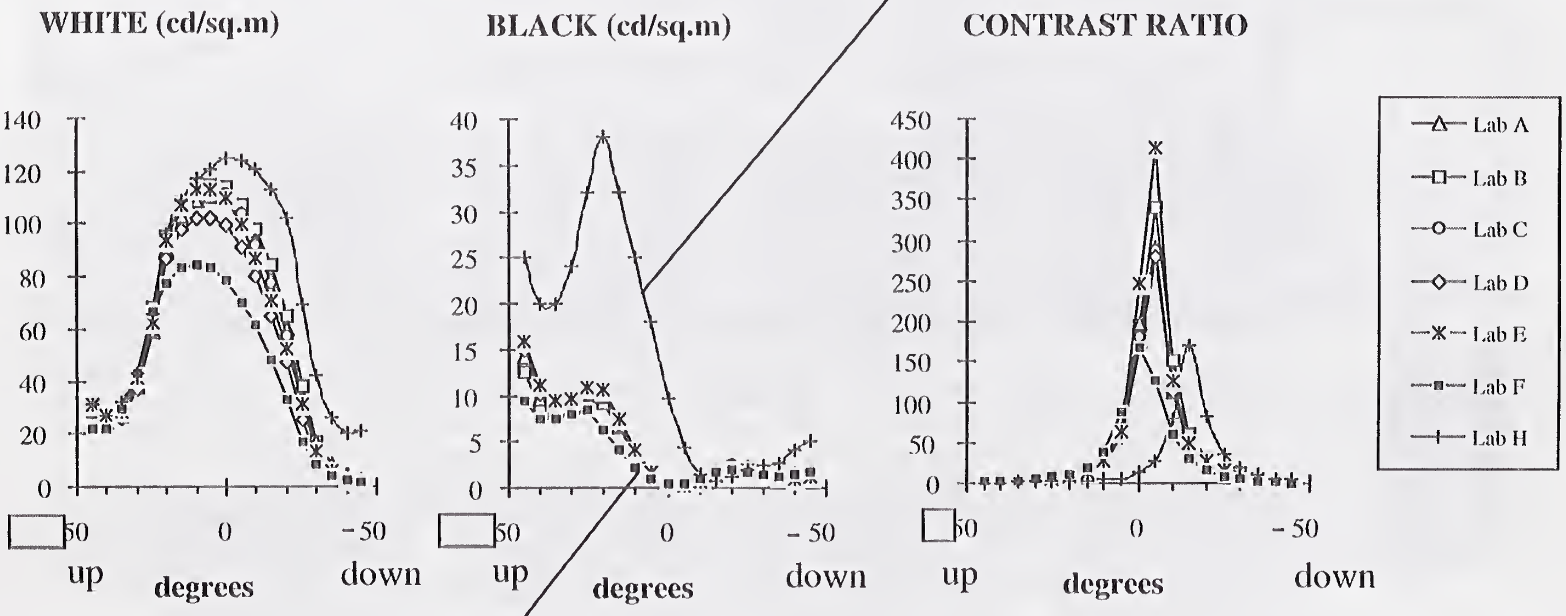
Direct'n	Angle	White L_W	x_W	y_W	CCT(K)	Black L_b	x_b	y_b	C_R	Red L_{red}	x_{red}	y_{red}	Green L_{grn}	x_{grn}	y_{grn}	Blue L_{blu}	x_{blu}	y_{blu}
Up θ_U	15°	85.6	.298	.322		1.59	0.271	0.292	52.9	25.9	0.521	0.350	50.2	0.296	0.521	16.1	0.157	0.140
Dwn θ_D	10°	111	.322	.348		3.79	0.269	0.285	29.2	35.4	0.520	0.349	63.5	0.305	0.518	20.3	0.166	0.165
Right θ_R	30°	39.4	.323	.346		0.553	0.268	0.290	71.2	12.1	0.550	0.354	22.5	0.307	0.541	6.23	0.158	0.150
Left θ_L	30°	39.9	.323	.345		0.609	0.270	0.297	65.4	12.3	0.548	0.353	22.7	0.306	0.540	6.34	0.158	0.150

Viewing Angle, Vertical

. . . results are critically dependent upon display set-up conditions. . .

AMLCD

Brightness and Contrast controls set to "maximum"



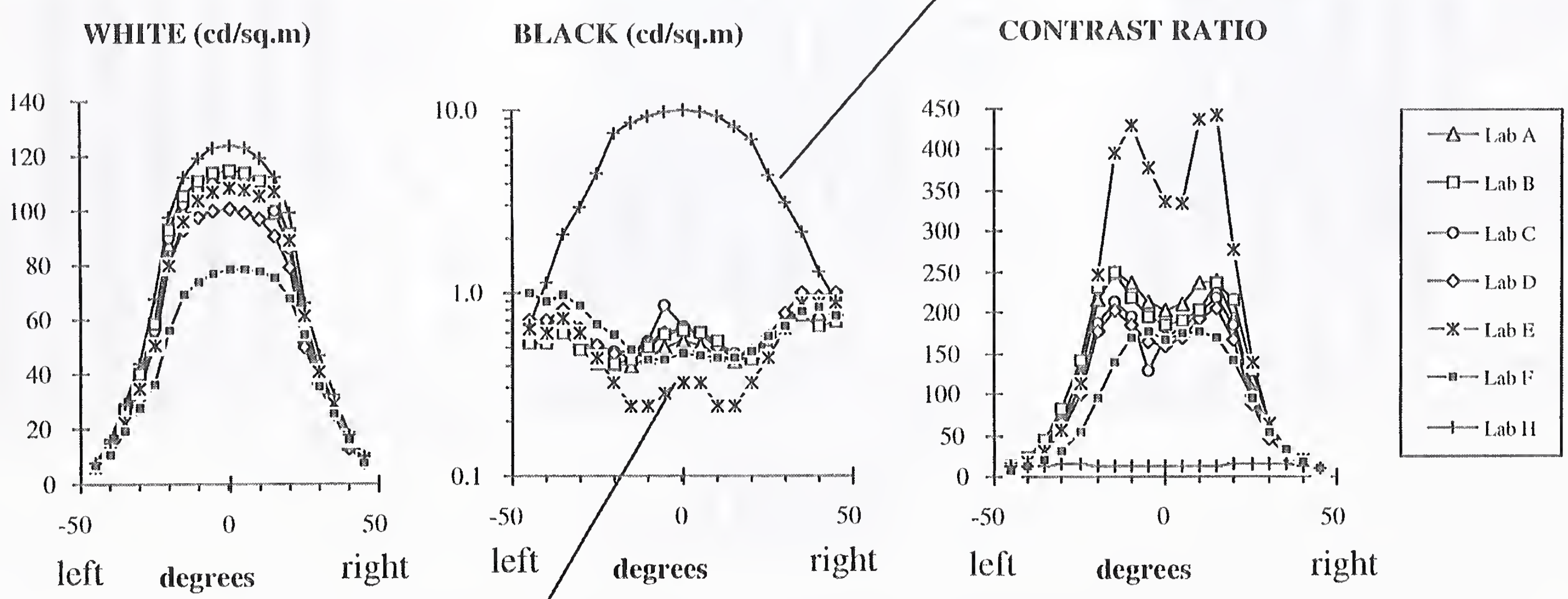
Brightness and Contrast controls adjusted by eye to avoid perceivable black-level clipping and white-level saturation

Viewing Angle, Horizontal

. . . results are critically dependent upon display set-up conditions. . .

AMLCD

Brightness and Contrast controls set to "maximum"

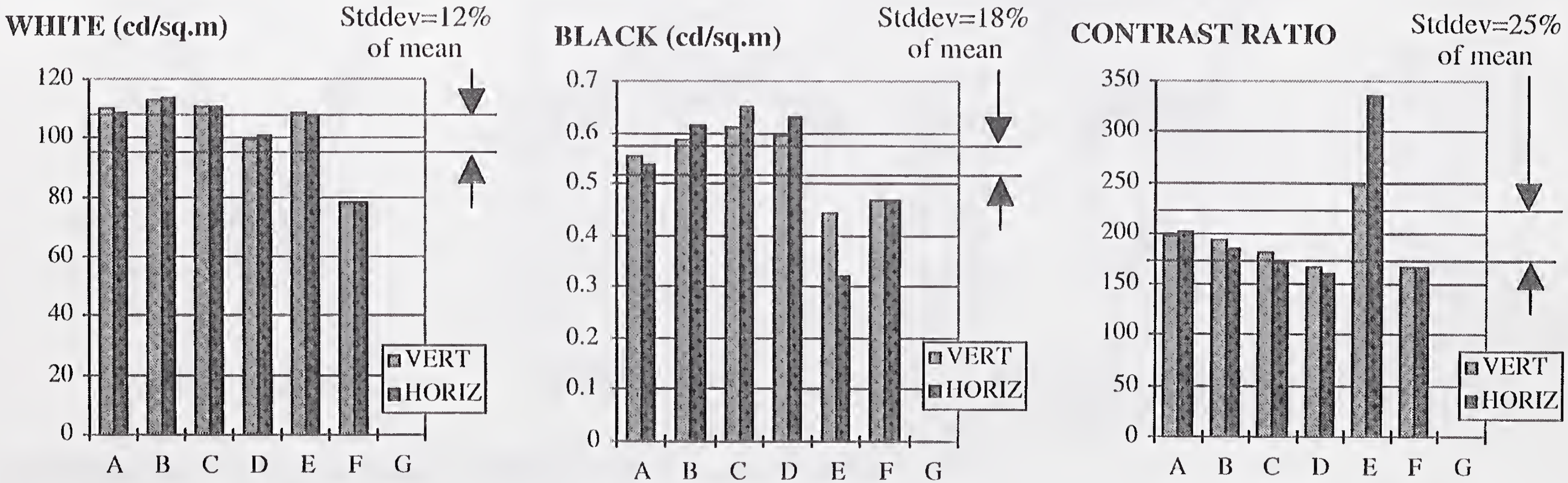


Brightness and Contrast controls adjusted by eye to avoid perceivable black-level clipping and white-level saturation

Luminance and Contrast

. . . high level of variability in results . . .

AMLCD

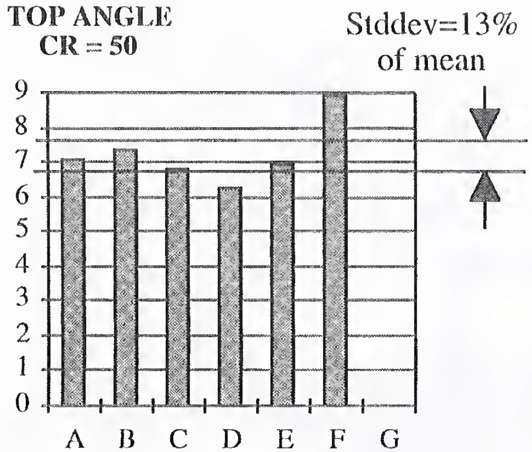


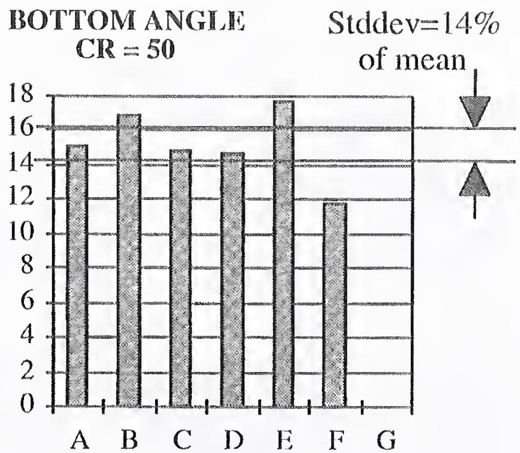
Laboratory

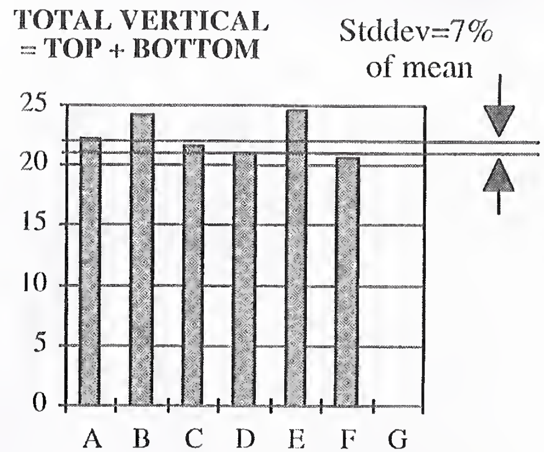
Viewing Angle, Vertical

. . . less variability in total angular range . . .

AMLCD





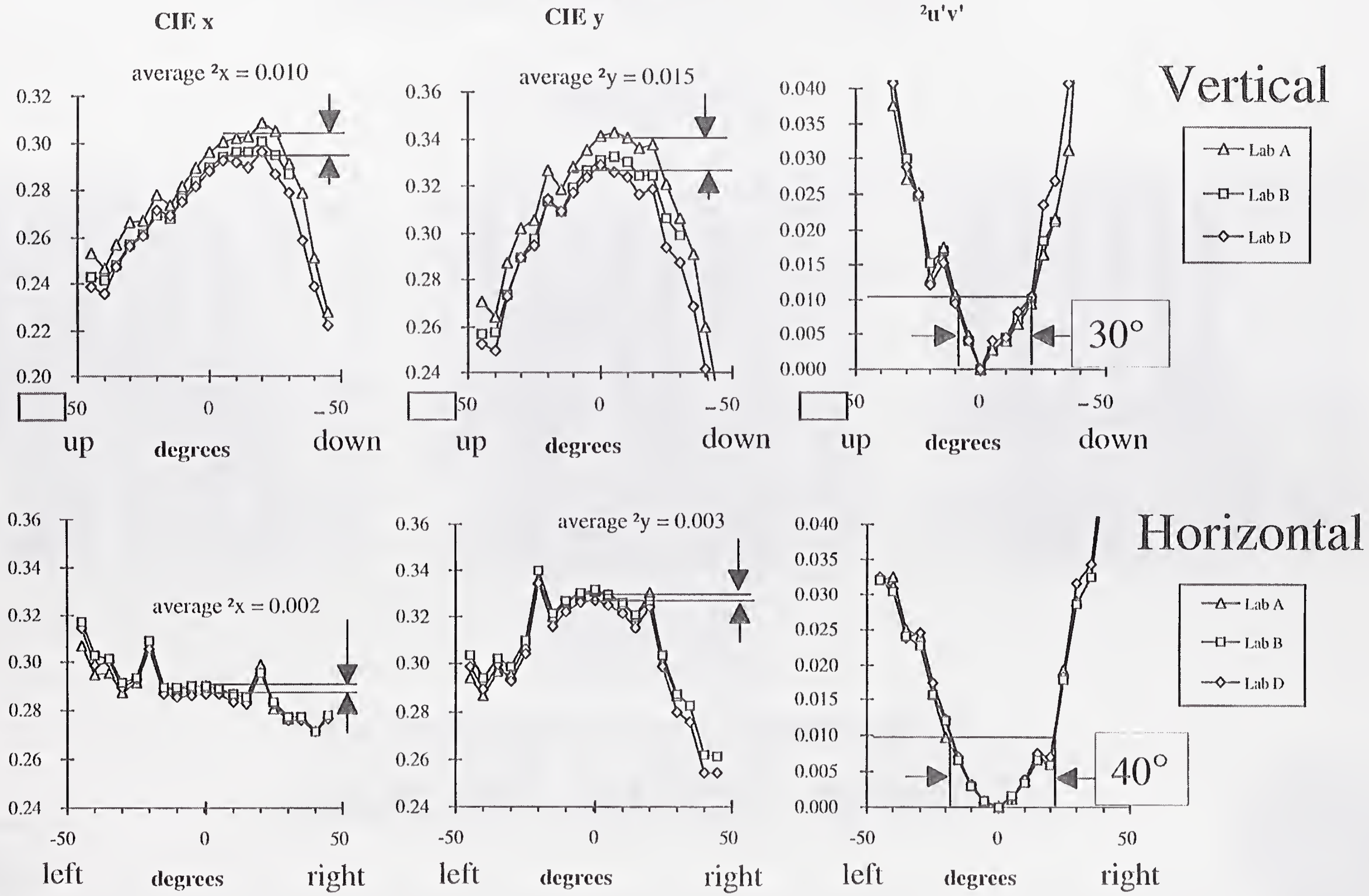


Laboratory

Chromaticity Viewing Angles

. . . use of ²u'v' metric reduces impact of variability . . .

PMLCD



Results Summary

. . . FPDM measurements succeed in quantifying differences between displays . . .

	AMLCD	PMLCD
Full Screen Center Luminance, cd/m^2		
• Lwhite	104 (12%)	103 (8%)
• Lblack	0.54 (18%)	5.96 (11%)
• Contrast Ratio	198 (25%)	17.6 (11%)
Threshold Viewing Angles, H x V		
• CR • 50	63°x 22° (7%)	-----
• CR • 10	------	61°x 34°(10%)
• ²u'v'Š 0.010	70°x 25° (8%)	40°x 30° (8%)

Standard deviations shown in parentheses (), expressed as percentage of average value.

NTA

Variability of Results

. . . Standard deviations of results expressed as percentage of mean . . .

** Use of total angle reduces impact of variability*

Full screen luminance	AMLCD	PMLCD
White	12%	8%
Black	18%	18%
Contrast ratio	25%	11%
Horizontal viewing angle		
Right	9%	10%
Left	4%	13%
Right + Left	6%	10%
Vertical viewing angle		
Up	13%	39%
Down	14%	20%
Up + Down	7%	10% *
Chromaticity (standard deviations in CIE x,y units)		
Horizontal	(.005, .002)	(.002, .003)
Vertical	(.006, .003)	(.005, .008)

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Lessons Learned

1. **Set-up is critical**.

2. Measurements do discriminate between displays.

3. Low variability obtained due to:
   - adherence to set up procedure, and
   - presence of NIDL coach.

Conclusions

Reasons why first round-robin results may be overoptimistic

- Display set-up guided by NIDL coach
- Narrow breadth of measurements

Reasons why first round-robin results may be pessimistic

- Performed under extreme time constraints
- Instances of less-than-perfect darkroom environments
- Instances of makeshift mechanical positioning devices

Second round-robin is now underway

- More thorough than first round-robin
- Displays are accompanied only by VESA FPDM draft standard
- New participants are welcome
- To sign up contact Mike Grote, (609)734-2506, mgrote@sarnoff.com

Acknowledgements

. . . THANK YOU to the Participants . . .

Michael Becker, autronic-Melchers

Jean-Noël Curt, Thierry Leroux, Eldim

Bruce Denning, Microvision

Ed Kelley, Paul Boynton, George Jones, NIST

Hector Lara, Manjit Daniel, Photo Research

Joe Miseli, SUN Microsystems

Sal Ghalya, TUV Rheinland

Acknowledgements (cont'd)

Sam Grant, NIMA, for support of standards efforts

Art Cobb, Jim Watson, Jon Leachtenauer

NIMA, for helpful discussions and encouragement

After FPD Measurement Standards

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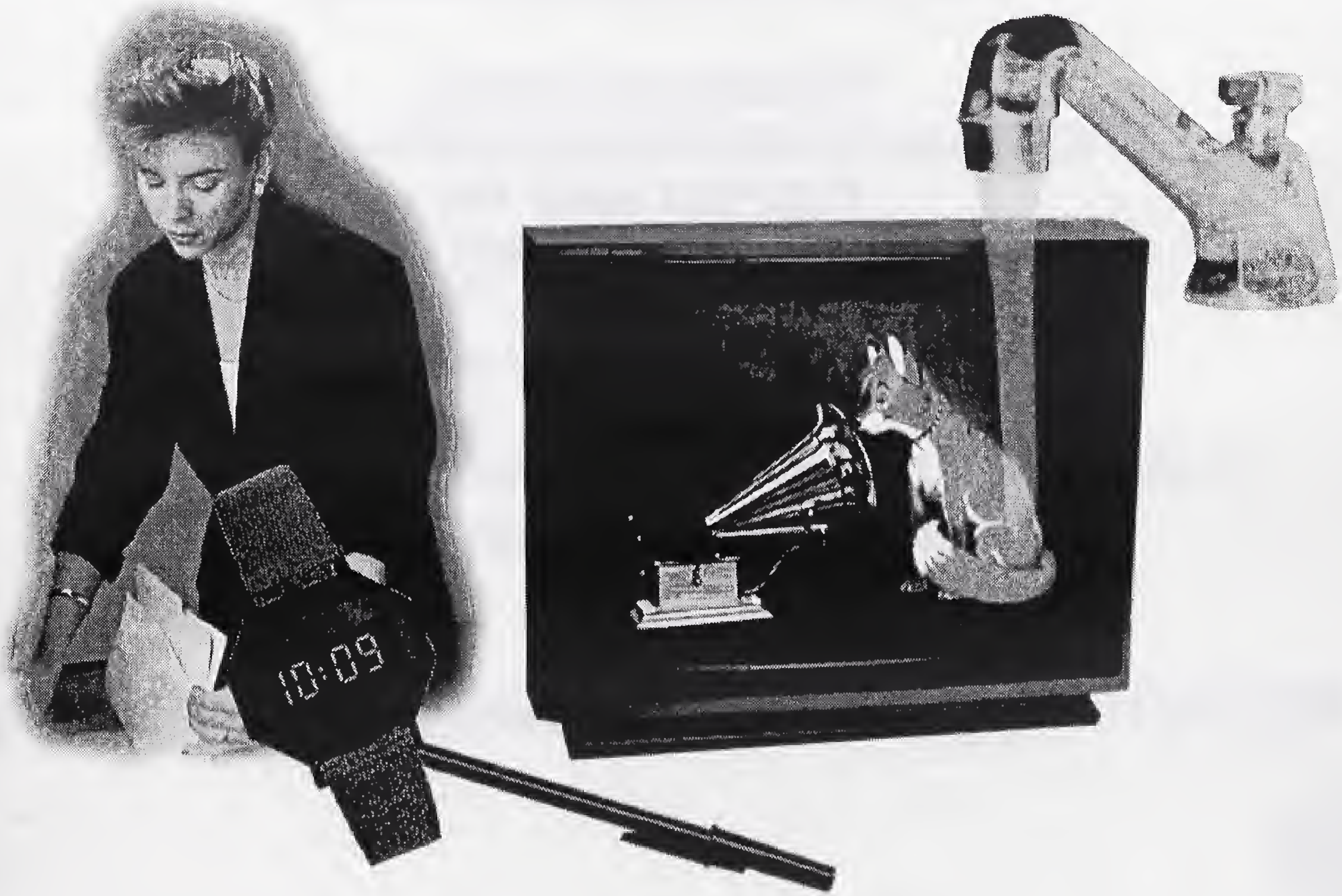
http://www.nidl.org

Presentation at Display Forum '97
Gaithersburg Hilton, Gaithersburg, MD
20 October 1997

What's Common?

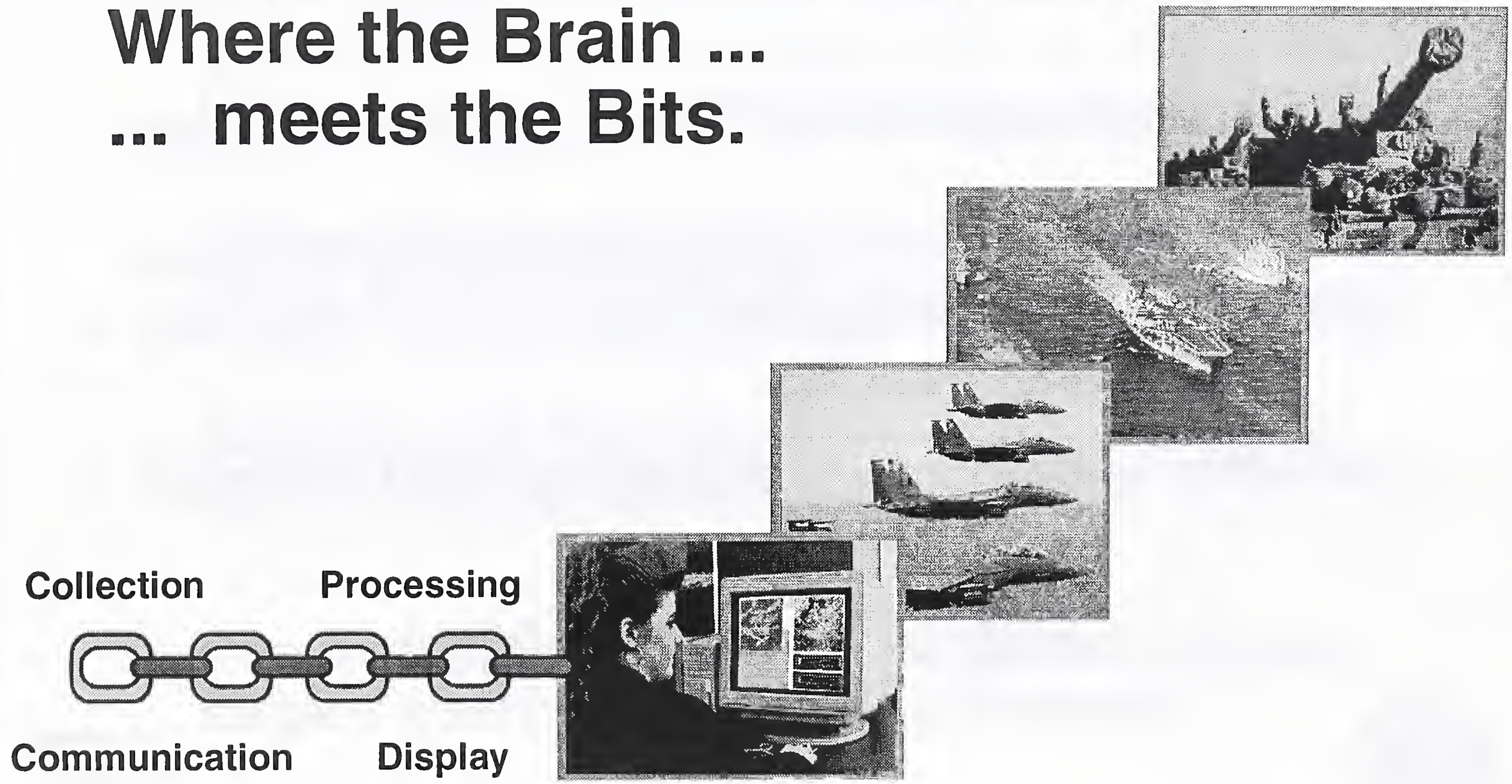
... what's most taken for granted? ...



The Display

... the last link in the information chain to the user ...

Where the Brain ...
... meets the Bits.



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NATIONAL IMAGERY AND MAPPING AGENCY

Message: Today

- All users need standards to select their displays.
- The NIDL works with industry and government to develop display standards.
- NIDL has a CRT Display Measurement Standard.
- VESA's FPDM Group led by NIST and NIDL will shortly have a Flat Panel standard that supports Government needs!

Message: Next Steps

- A level playing field needs to be set for FPDs, CRTs, Plasma Displays and Projectors.
- Performance standards need to be set for driver boards and image processing software.
- Methods and Standards are needed to better specify display system performance.
- Connection needs to be established between display metrics and task requirements.

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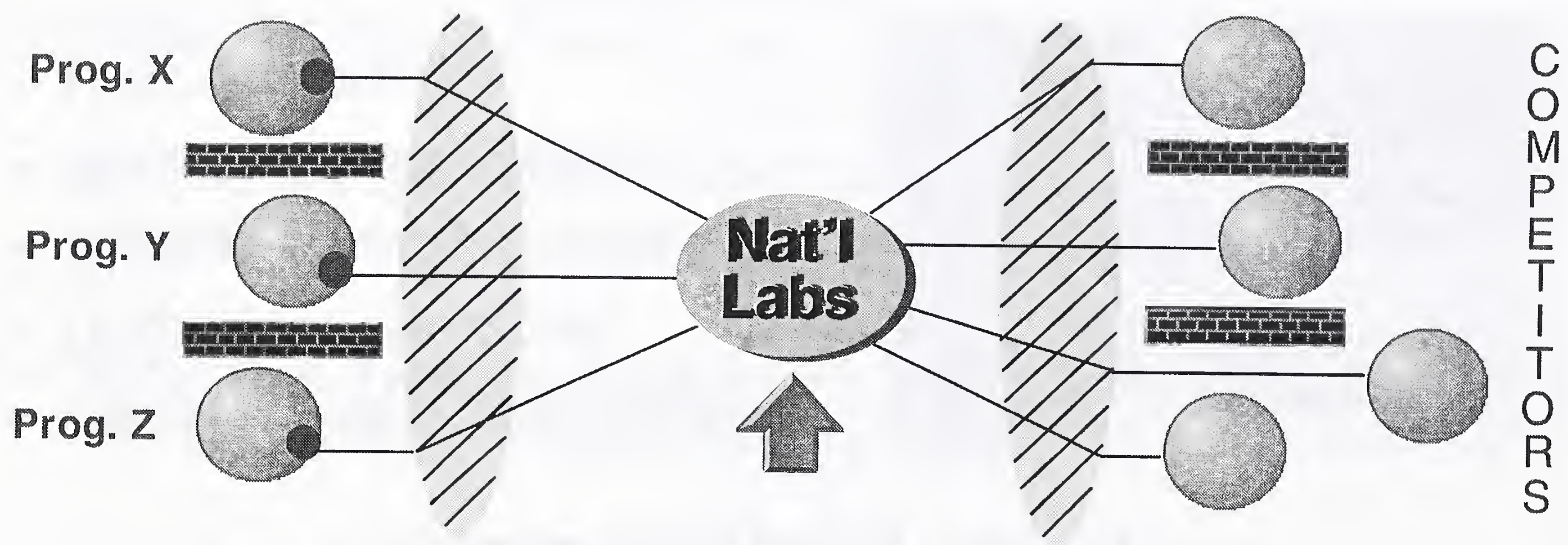
National Information Display Laboratory

Strategic Vision

Bring the right commercial technology to the government to get the right information to the right people in the right place at the right time in the right format.

National Information Display Laboratory *Approach*

... focusing the resources of industry onto Government Users needs ...



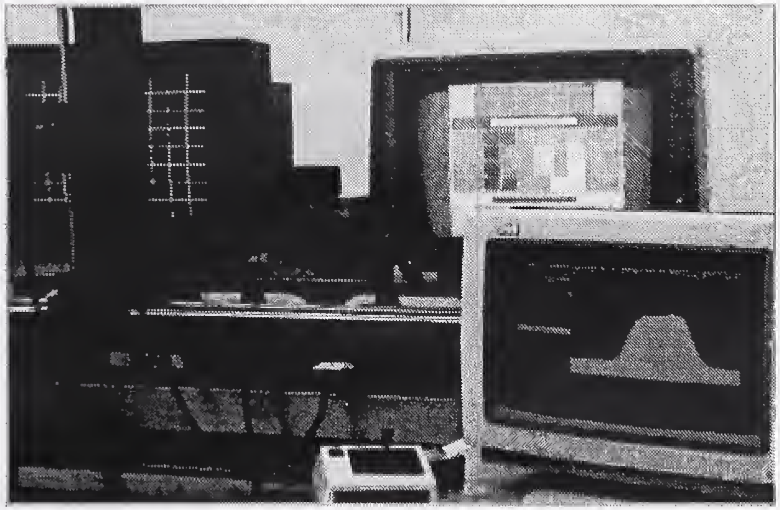
R&D Groups, Program Offices, Strategic and Tactical Users, Civilian Agencies

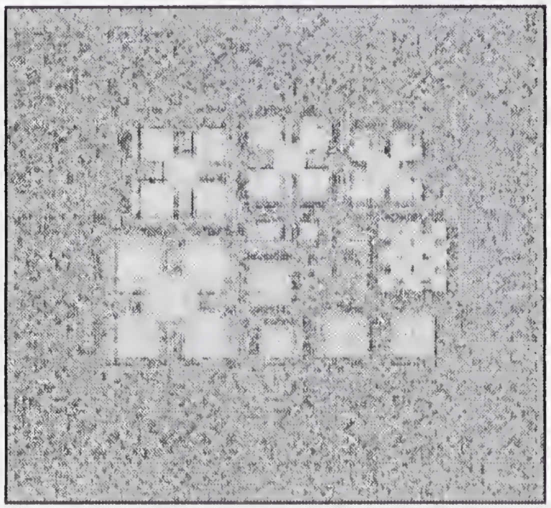
- **Focus**
- **Leverage**
- **Standards**
- **User Support**

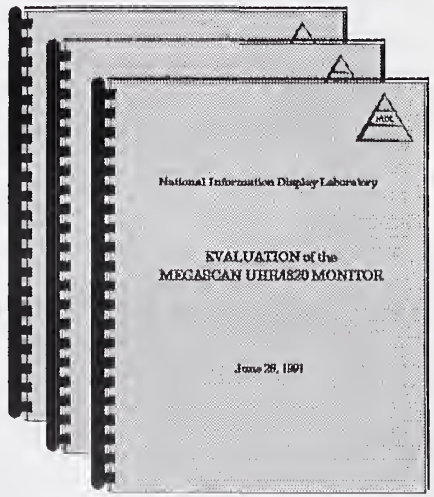
- **COTS & CDS**
- **R&D Centers**
- **Systems Developers**
- **Universities**

NIDL Display Work

- Measurement Techniques
- Display Evaluations
- Display Quality Control
- Display Development
- User Support







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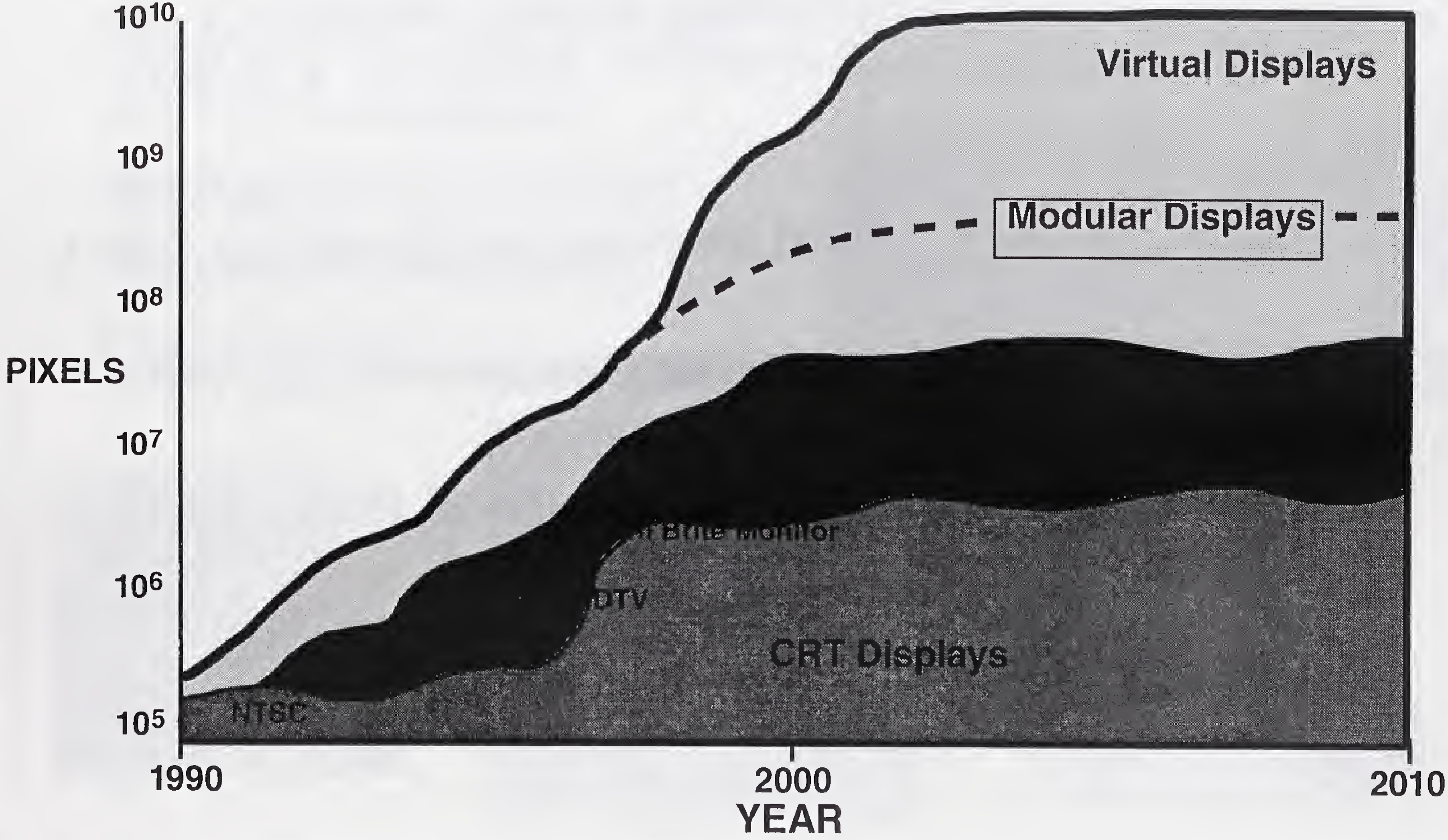
Current NIDL Standards Work

- VESA FPDM Working Group, Vice-Chair Mike Grote
- PIMA IT7 Committee, Chair, Leon Shapiro
- IEC TC100 SC100C Project Teams, Leon Shapiro, Mike Brill
- ANSI U.S. Technical Advisory Group to ISO TC159, SC 4, reviewer, Dennis Bechis

PIMA	Photographic and Imaging Manufacturers Association, Inc.
IEC	International Electrotechnical Committee
ISO	International Standards Organization

Display Directions

... technology waves toward higher performance ...



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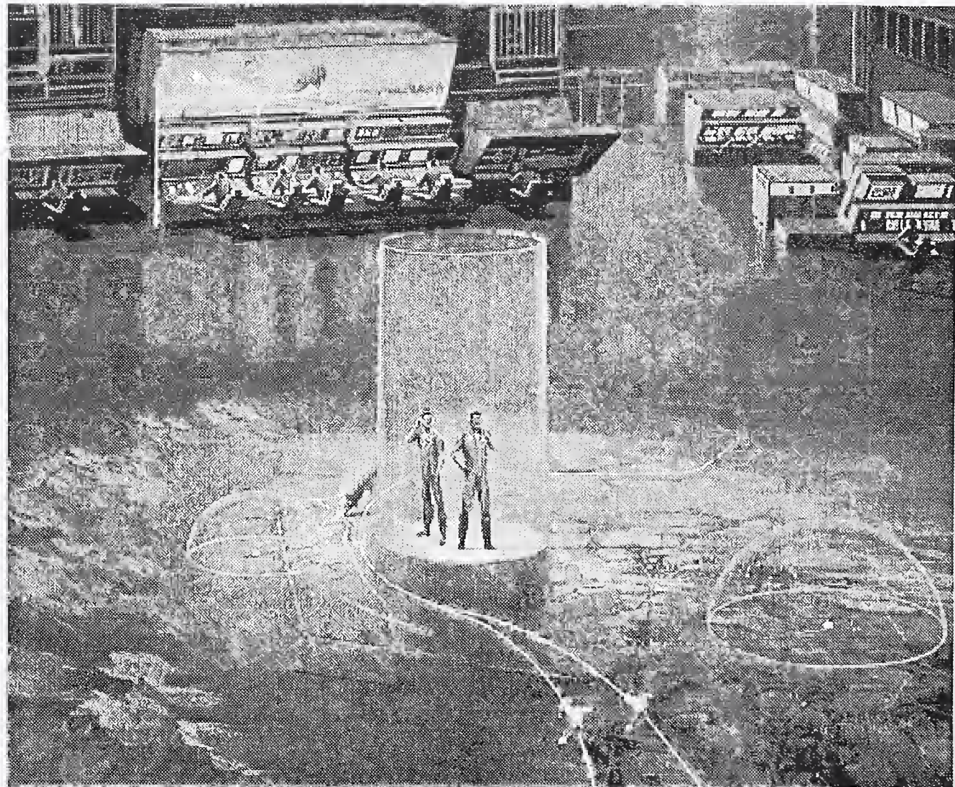
NATIONAL IMAGERY AND MAPPING AGENCY

Future Displays

... "higher IQ": Better Image Quality & More Smarts ...

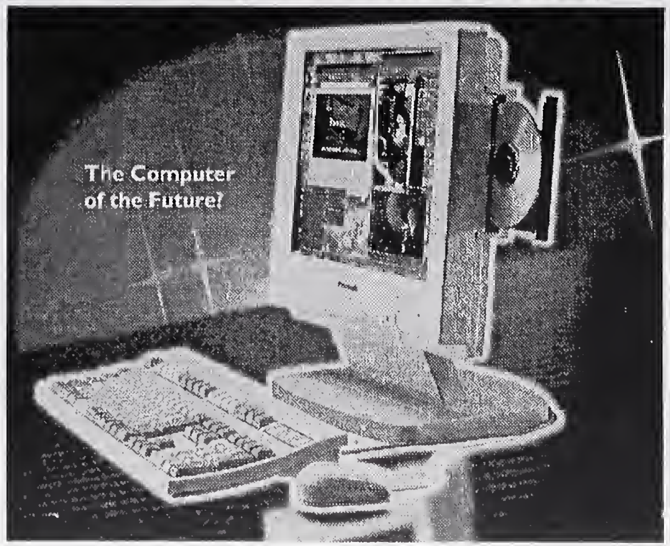
- Desk Display Systems
  - Image & geospatial analysis
  - Report generation
- Collaborative Display Systems
  - Situational awareness
  - Command & control



Desk Display Systems

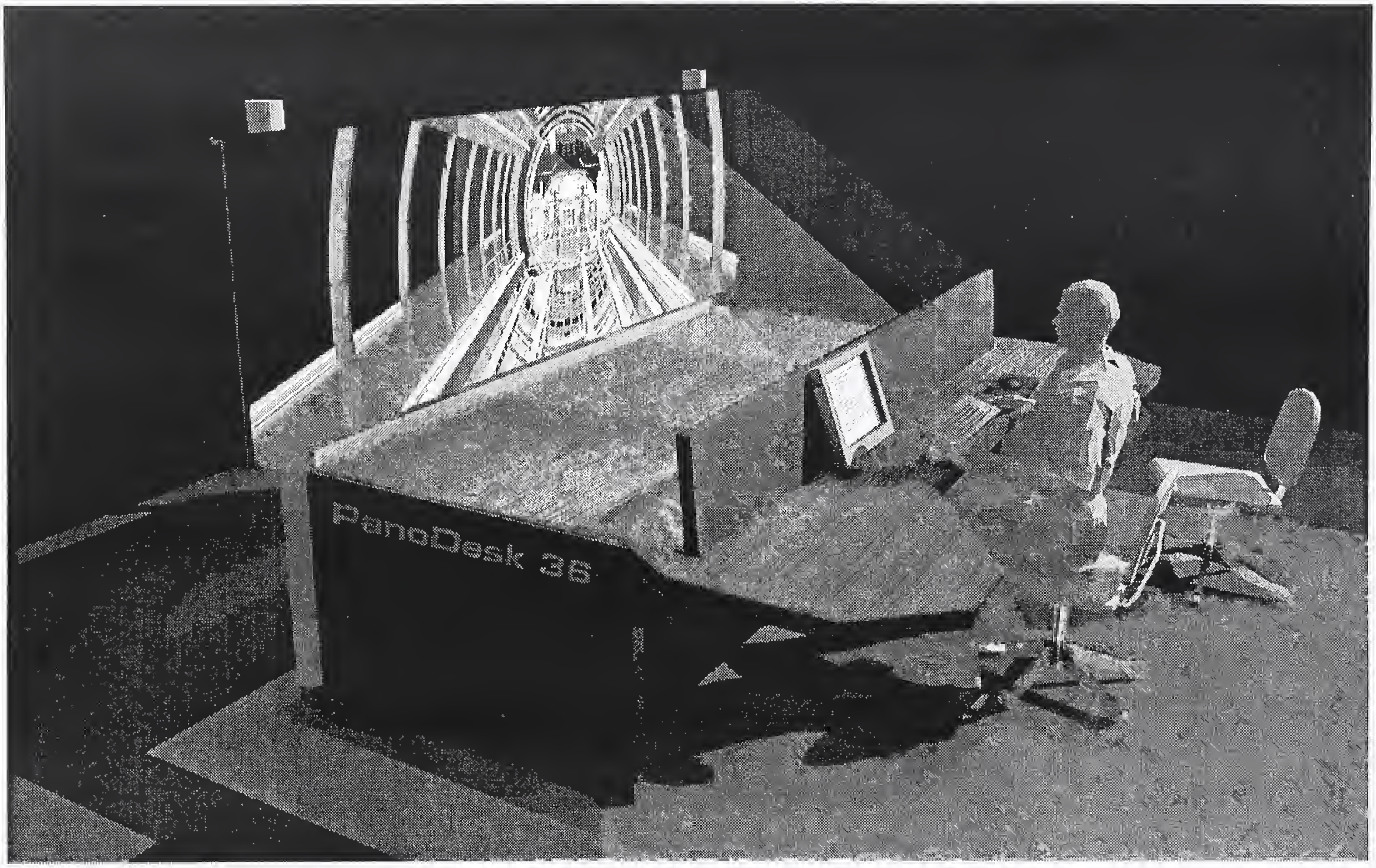
- Technologies
  - CRT, LCD, FED
  - Projection, Modular

- Large dynamic range ≥ 30 dB
- 2 to 10 Million Pixels
- Usable in office lighting
- Mono and color
- Stereo, video for some applications
- Controllable, specifiable grayscale and color
  - minimal loss of info due to display, driver or software
- Calibrated, stable, long-lived



Desk Display Systems

... 3Kx1K pixel displays ...



•Drawing Courtesy of Panoram Technologies, Inc.

Collaborative Display Systems

- Technologies
  - Modular, Projection
  - CRT, FED, LCD, Plasma
- 1 to Tens of meters
- $\geq 10^6$ to $\geq 10^8$ Pixels
- Seamless
- Viewable at different distances and angles
- Visible in ambient office lighting
- Calibrated, stable grayscale and color

Collaborative Display Systems

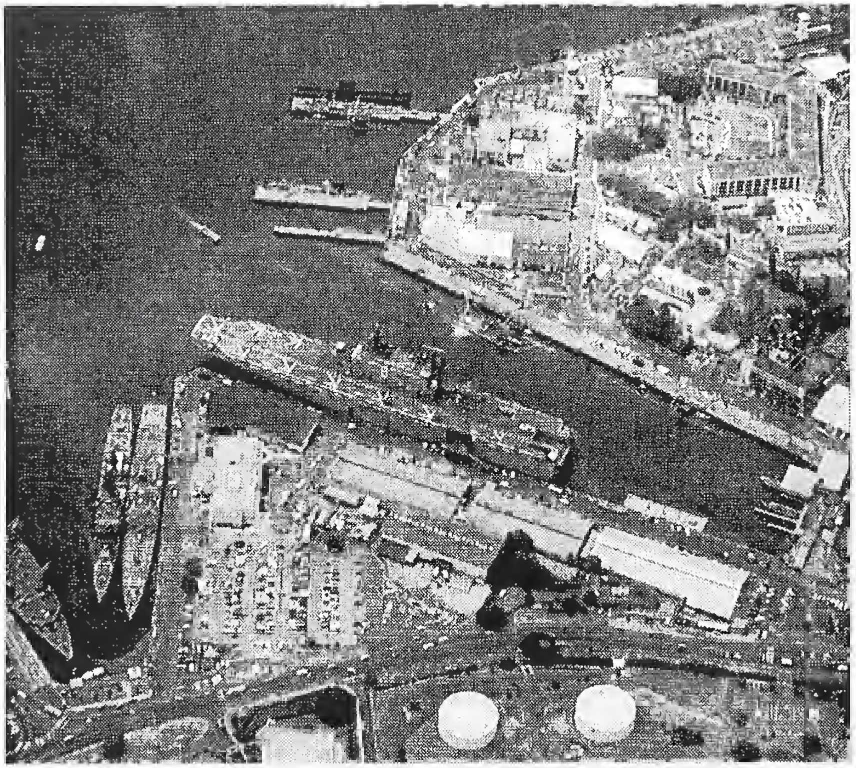
... will be seamless ...

More System Issues

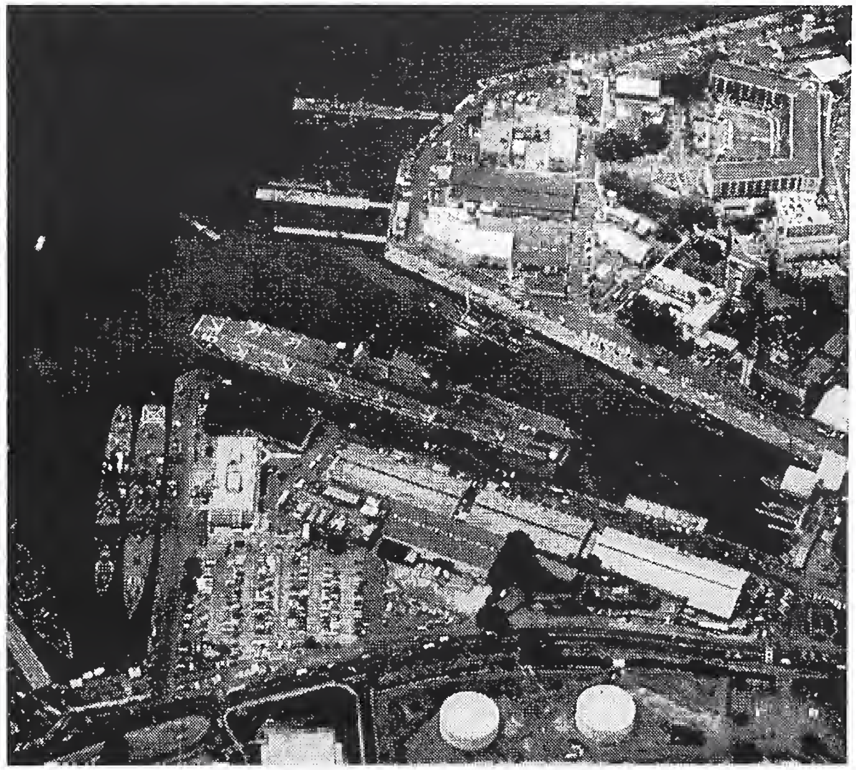
- Drivers
  - Linearity
  - Dynamic Range
  - Bandwidth
  - Stability
  - ...
- Image Processing Software
  - Seamless Format Translation
  - ...

Black Level Clipping

... unacceptable loss of low-luminance grayscale information ...



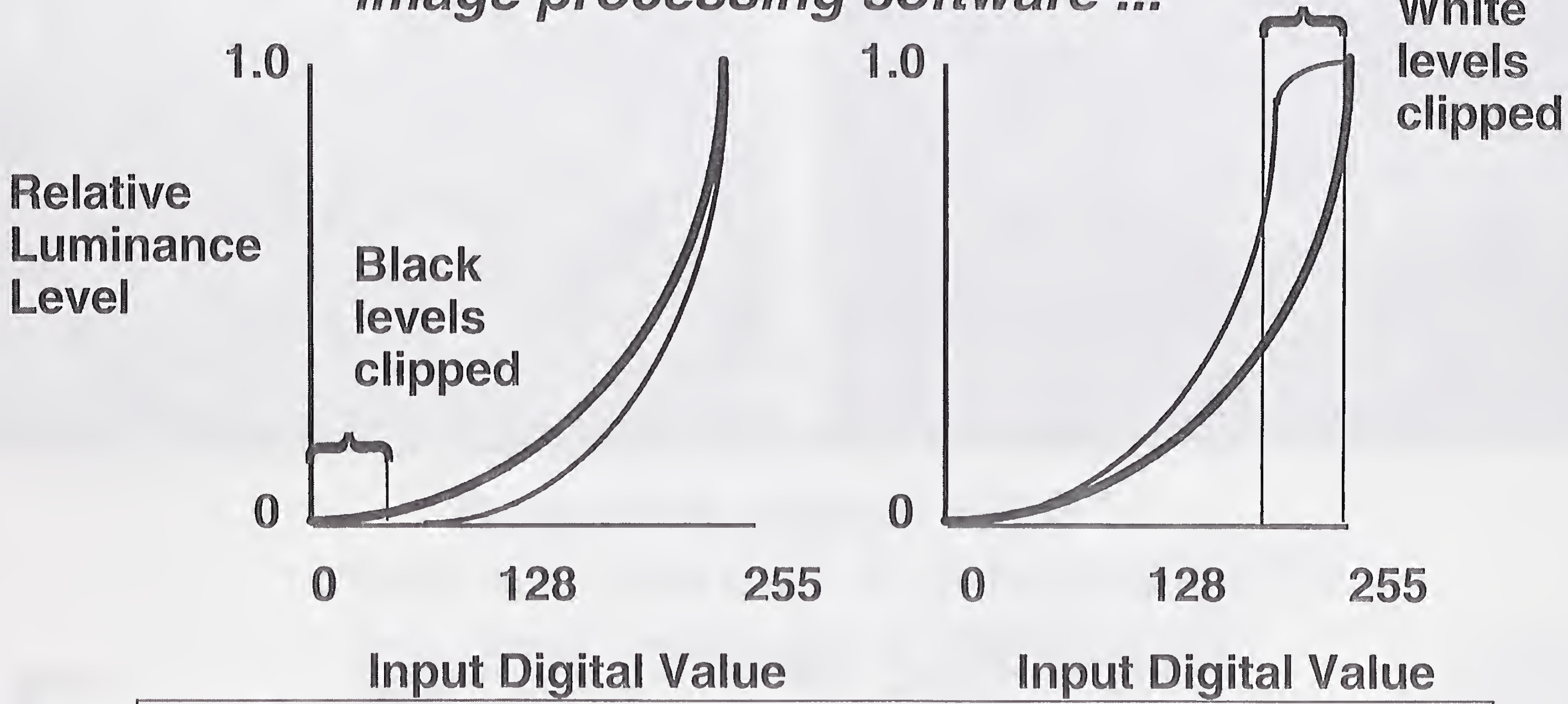
Calibrated Display System



Clipped Display System

Black and White Level Clipped Display Systems

... can be caused by display, drivers, and/or image processing software ...

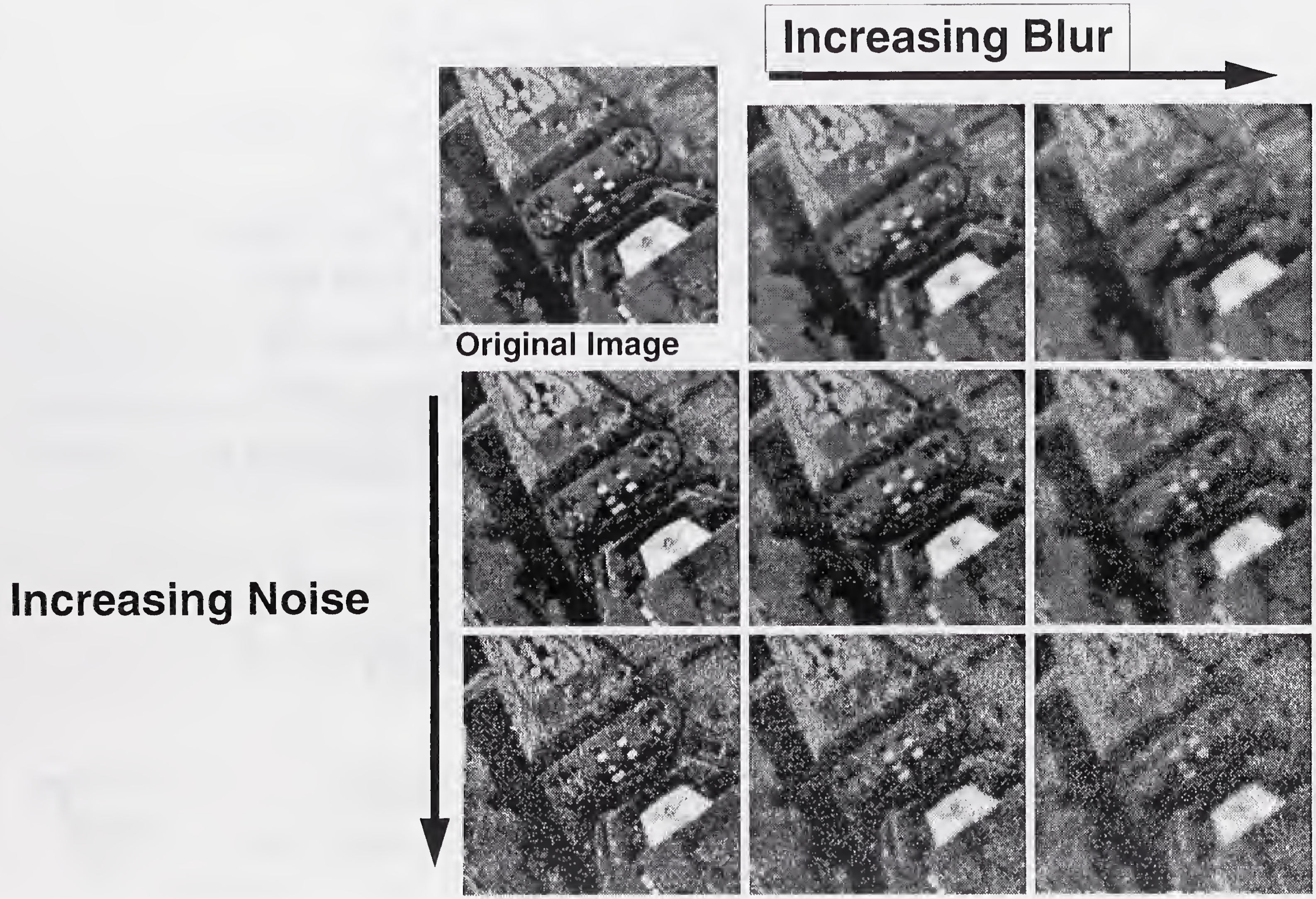


Aim: Optimal Curve for maximum discernible grayscale levels

Human Task Needs

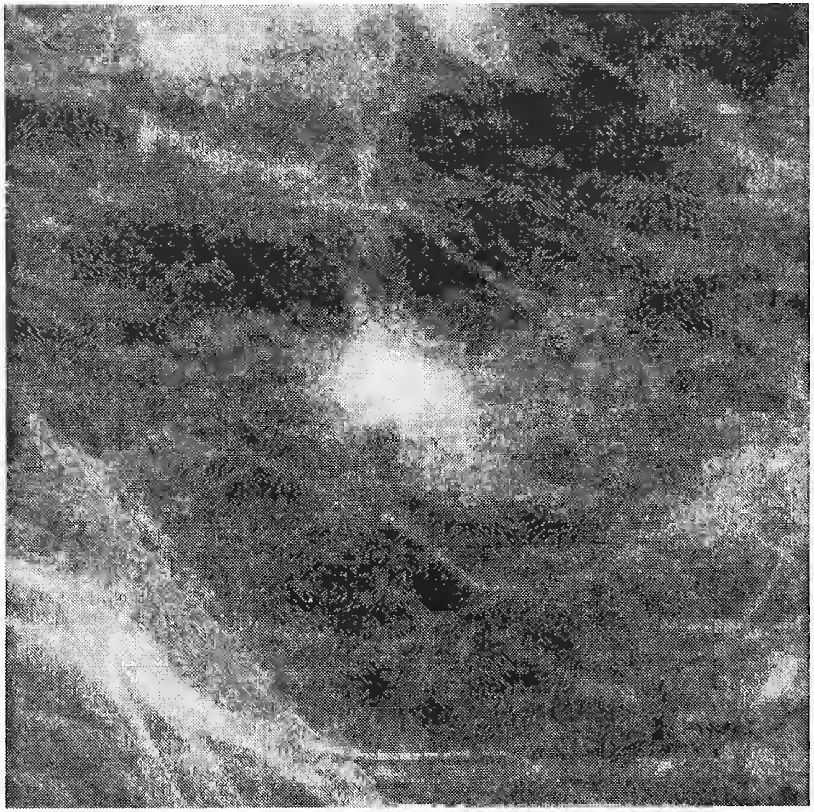
- A method to select display systems based on
  - how efficiently and reliably users accomplish their tasks
  - the viewing conditions
  - the type of data or images
  - the display system capabilities

What I.Q. Supports the Task?

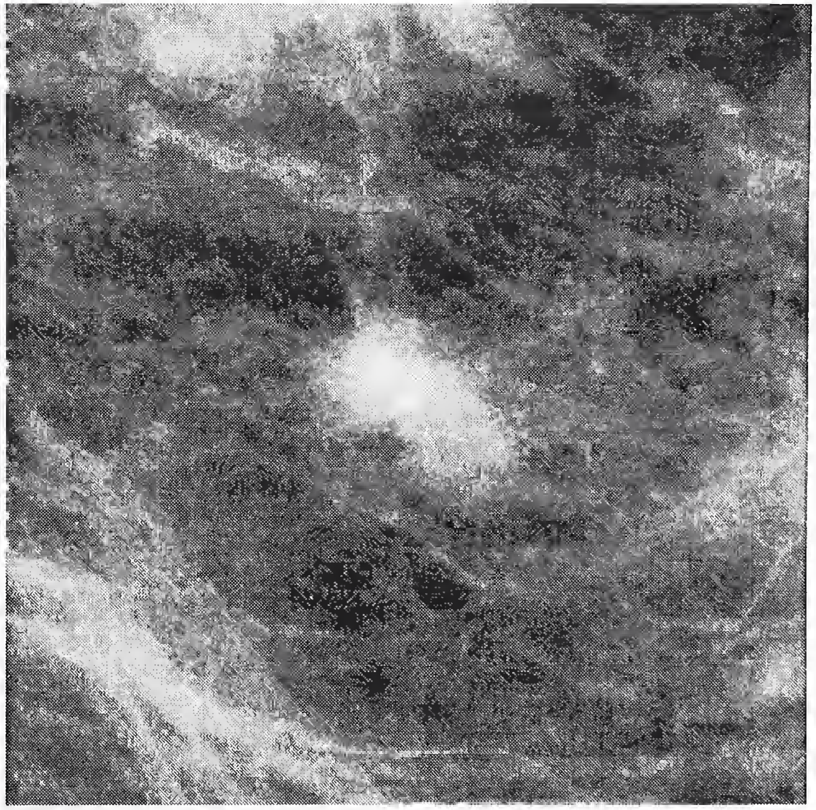


Life and Death Questions

... which display system enables the detection of cancer...



Display System A



Display System B

Next Steps

... technology-independent, task-dependent specification and measurement ...

- Lead the development of standards that put FPDs, CRTs, Plasma Displays, and Projectors on a level playing field.
- Develop and standardize evaluation methods for driver cards and image processing tools.
- Develop methods for connecting task requirements to display performance.

Benefits

... of scientific, technology-independent specification ...

- Improved task performance
- More efficient specification and design
- Larger selection of candidate display systems

Acknowledgements

- Sam Grant, NIMA, for support of standards efforts.
- Art Cobb, Jim Watson, Jon Leachtenauer, NIMA, for helpful discussions and encouragement.

INTERFERENCE FILTER TESTING FOR COLOR MEASUREMENT ACCURACY

Display Forum '97
October 20, 1997

Paul A. Boynton
Edward F. Kelley
National Institute of Standards and Technology
Gaithersburg, MD 20899

NIST FLAT PANEL DISPLAY LABORATORY
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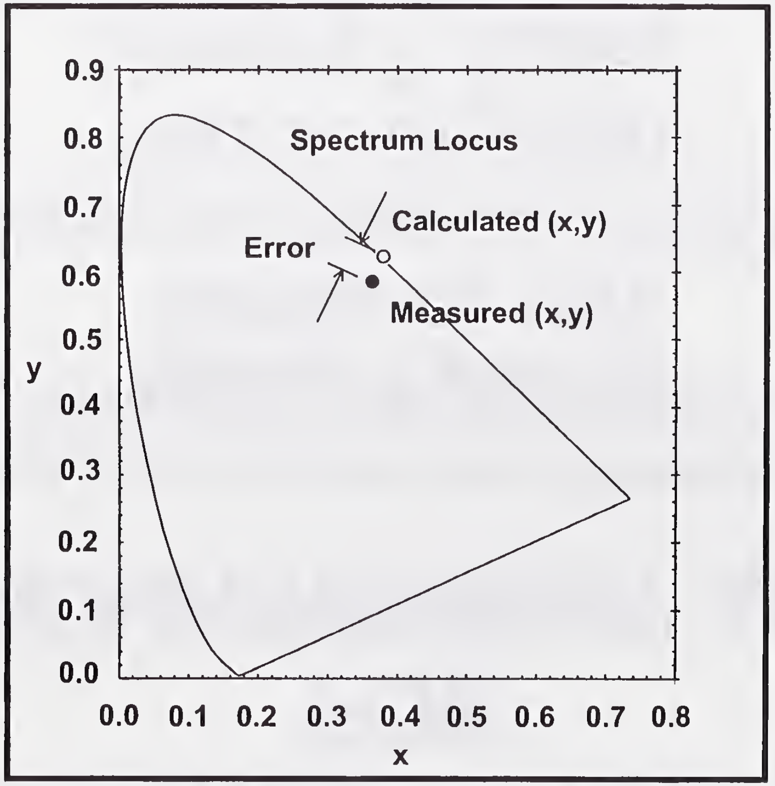
INTERFERENCE FILTERS CAN REVEAL INSTRUMENT PERFORMANCE



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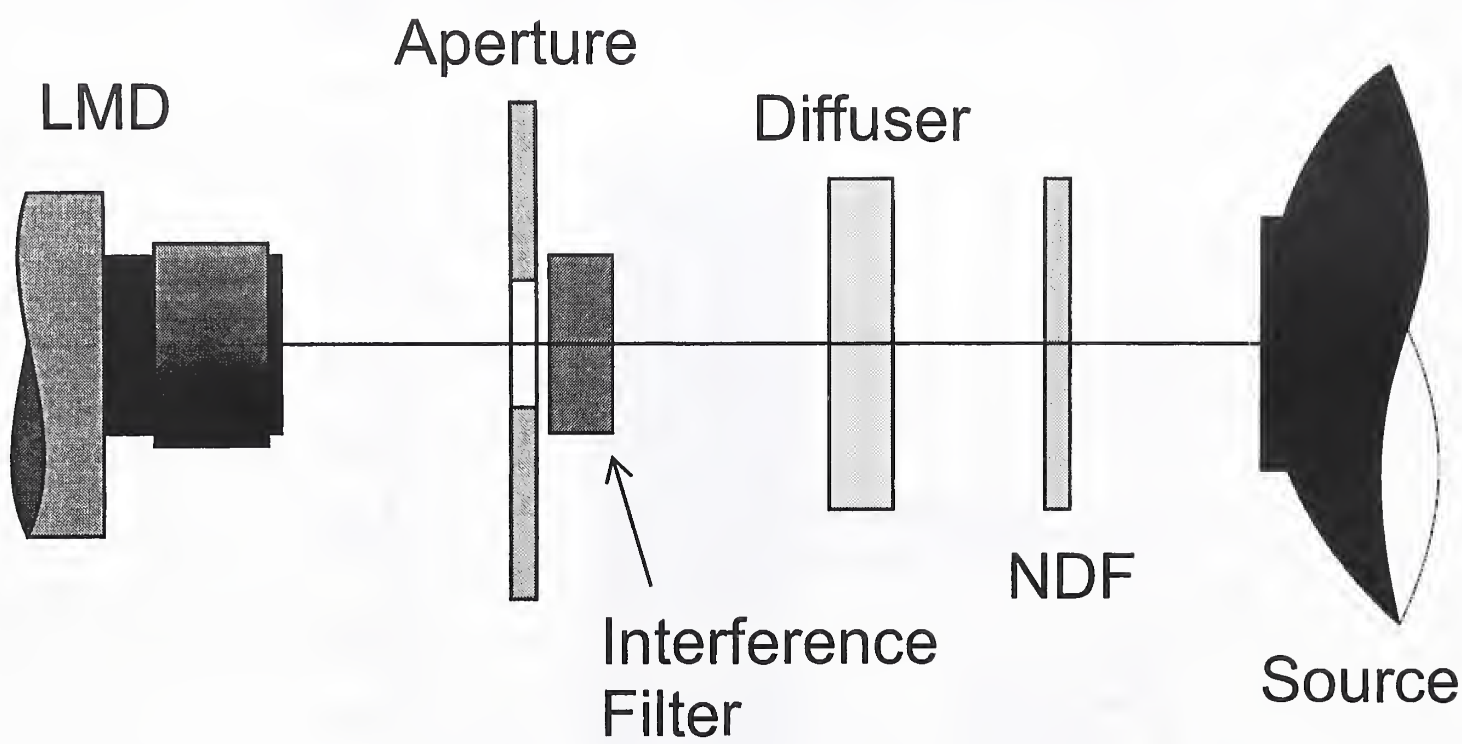
MEASUREMENT APPARATUS



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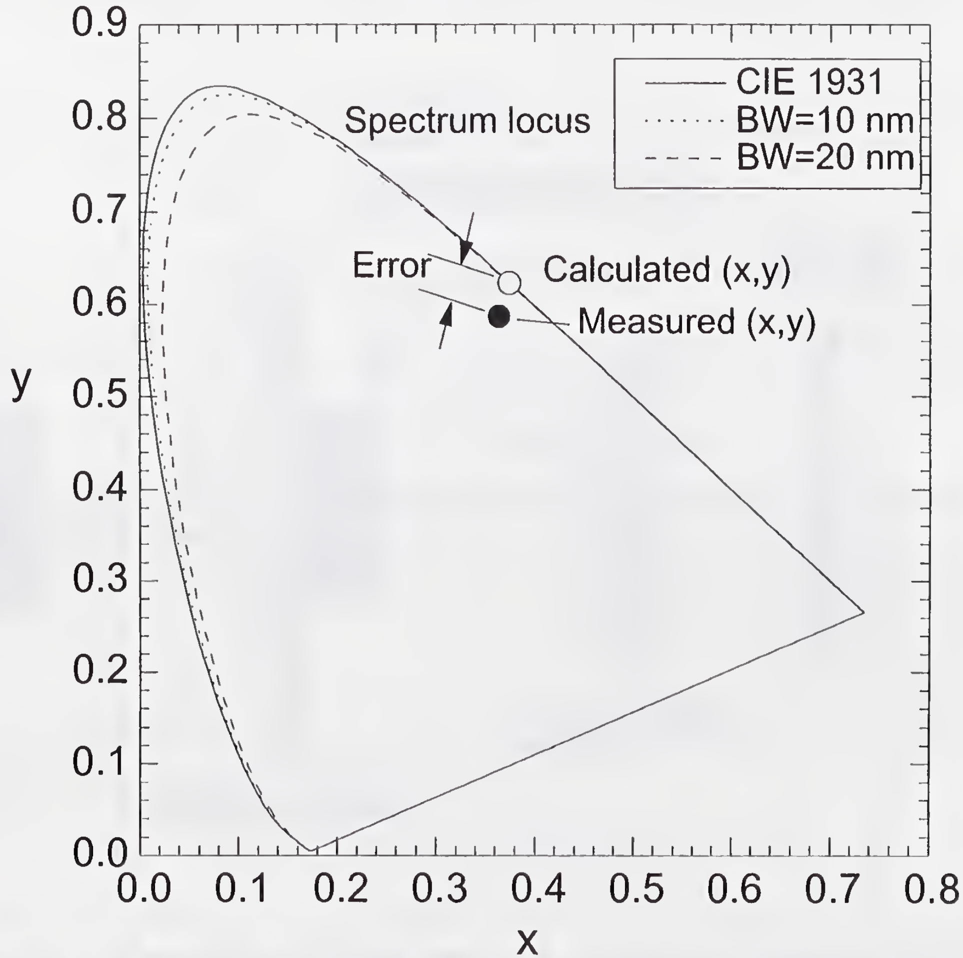
BANDWIDTH VARIATION



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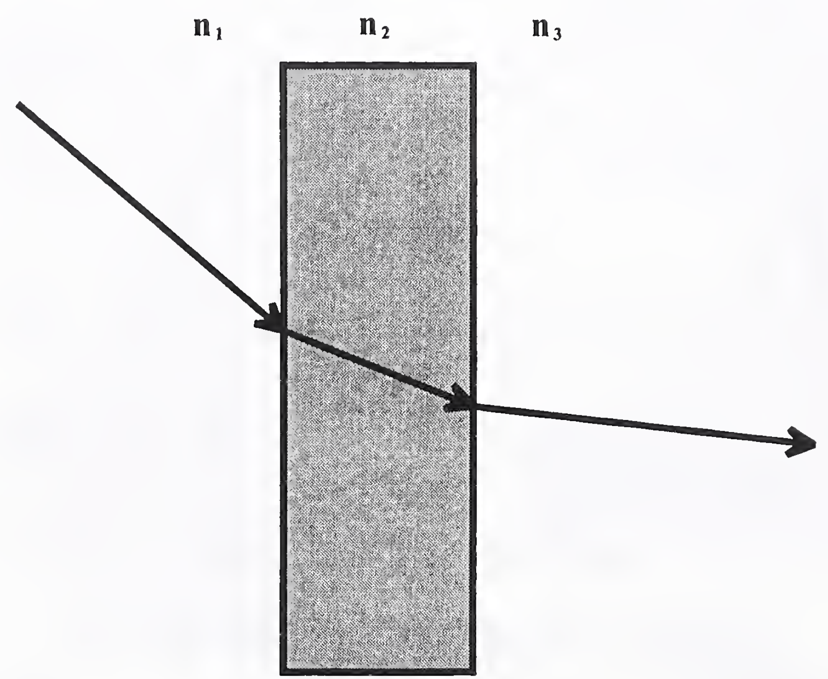
MISALIGNMENT

$$\lambda_\theta = \lambda_0 \left[1 - (n_1/n_2)^2 \sin^2\theta \right]^{1/2}$$



optical thickness = nt

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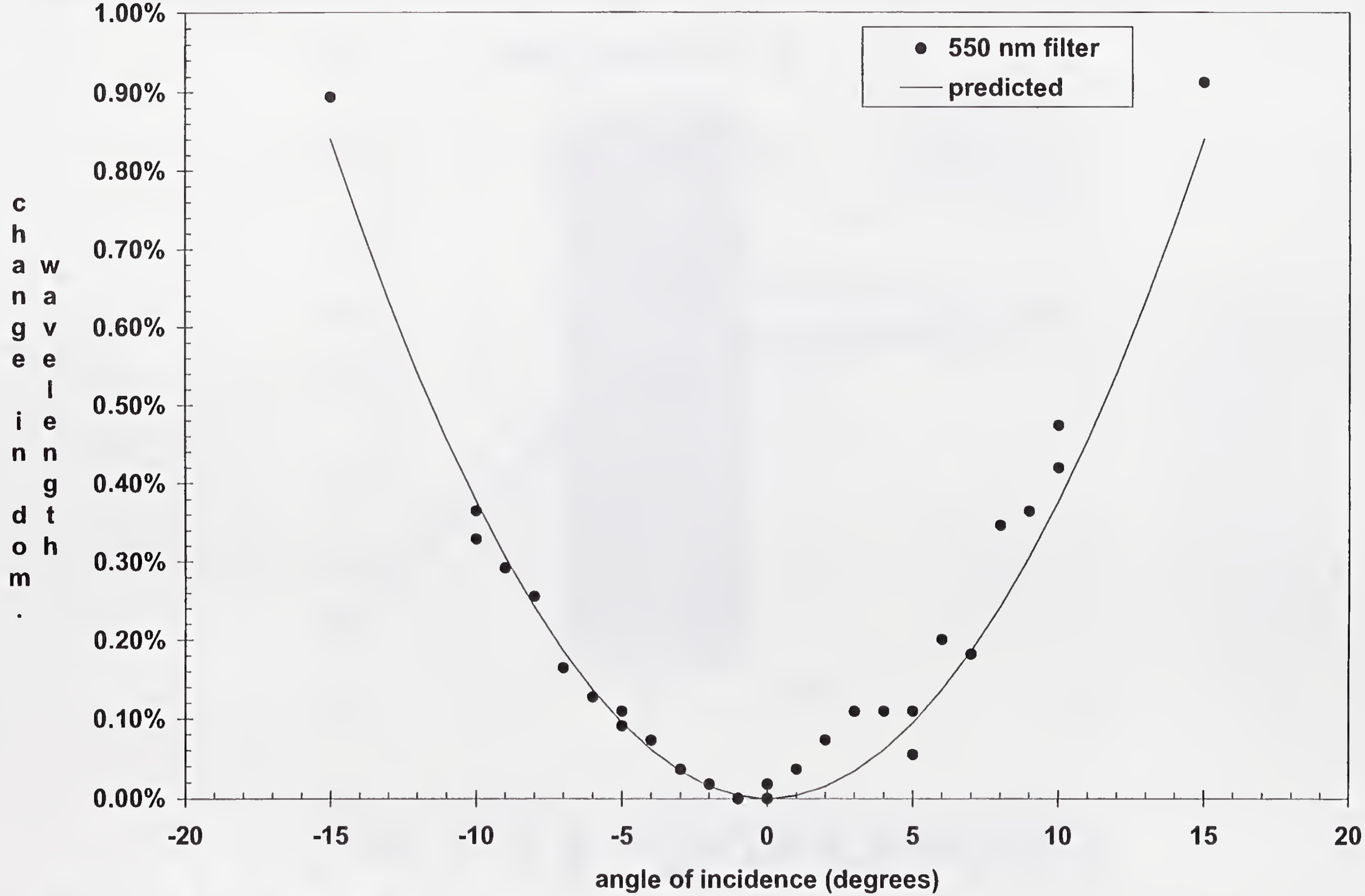
EFFECTS OF ALIGNMENT AND REFLECTION



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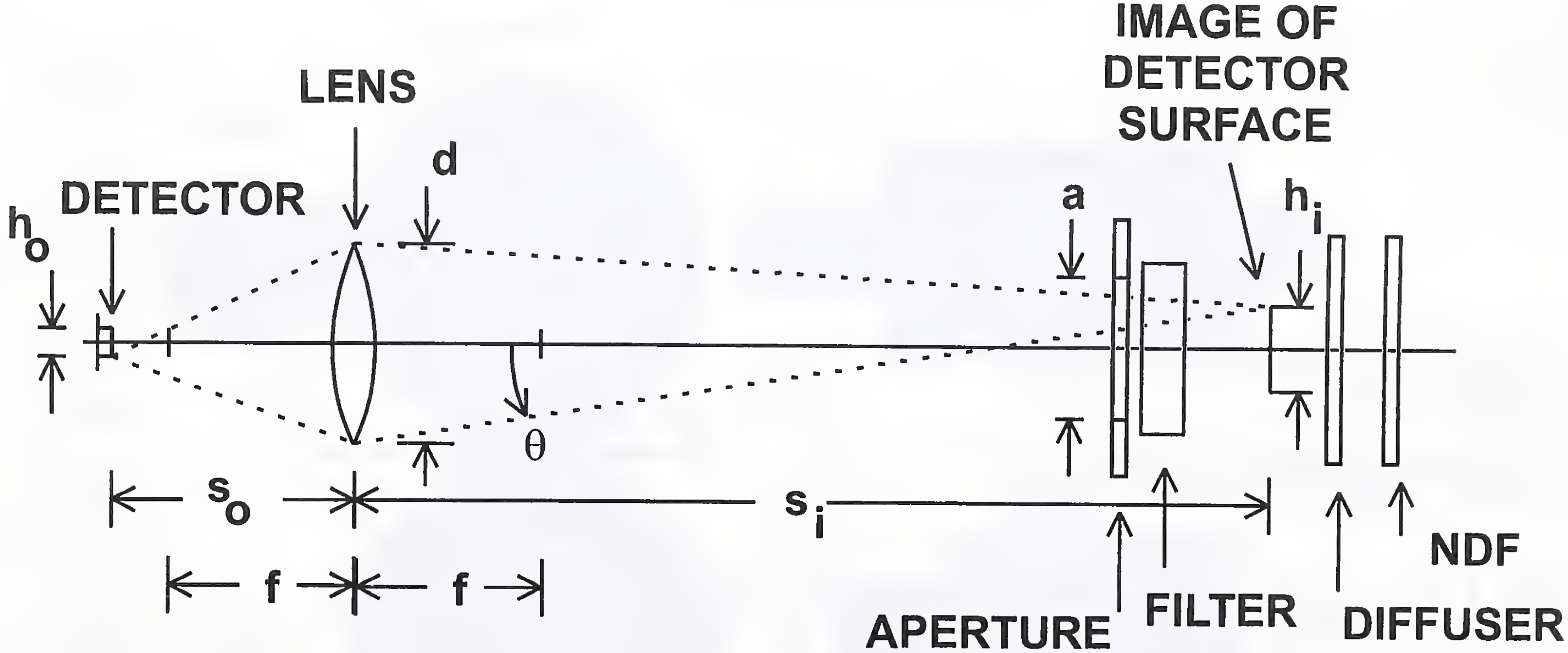
DIVERGENT ILLUMINATION



$$1/f = 1/s_o + 1/s_i$$

$$\theta = \arctan[1/s_i(h_i/2 + d/2)]$$

$$\lambda_\theta = \lambda_0 [\, 1 - (n_1/n_2)^2 \sin^2\theta]^{1/2}$$

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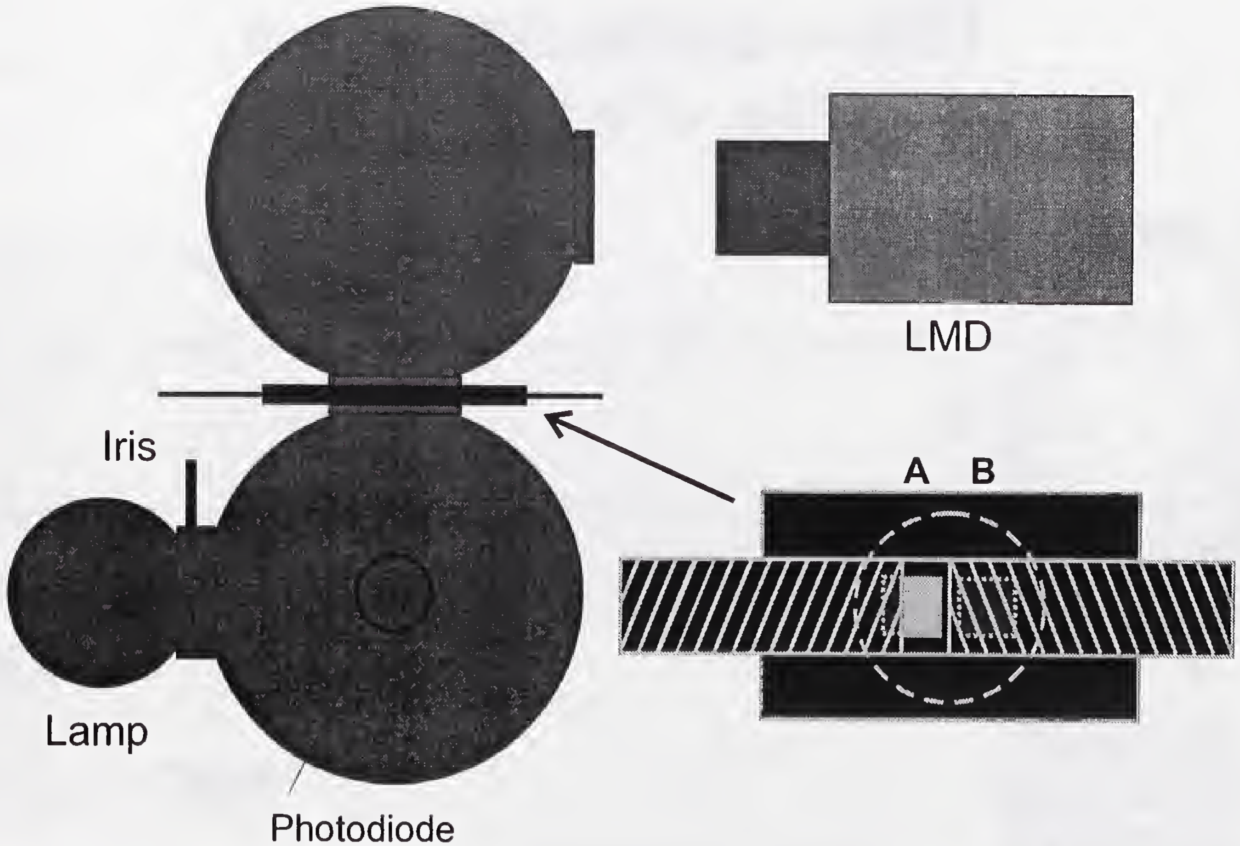
CHECKING LINEARITY



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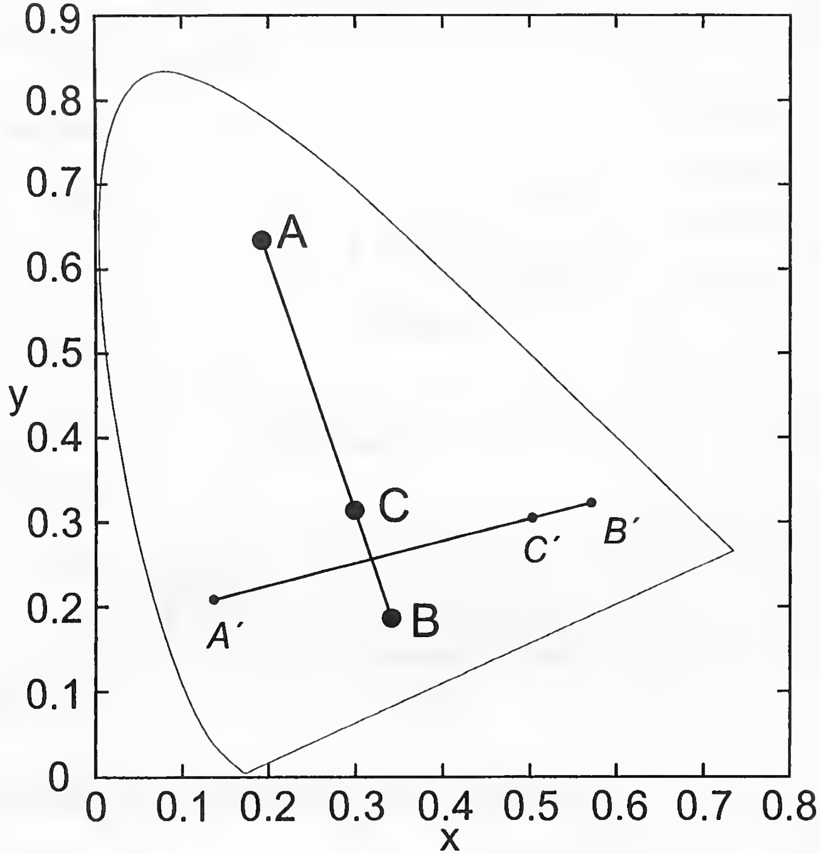
CHECKING LINEARITY



$$x'_C = x_A + k(x_B - x_A)$$

$$y'_C = y_A + k(y_B - y_A)$$

$$k = [1 + (y_B L_A / y_A L_B)]^{-1}$$

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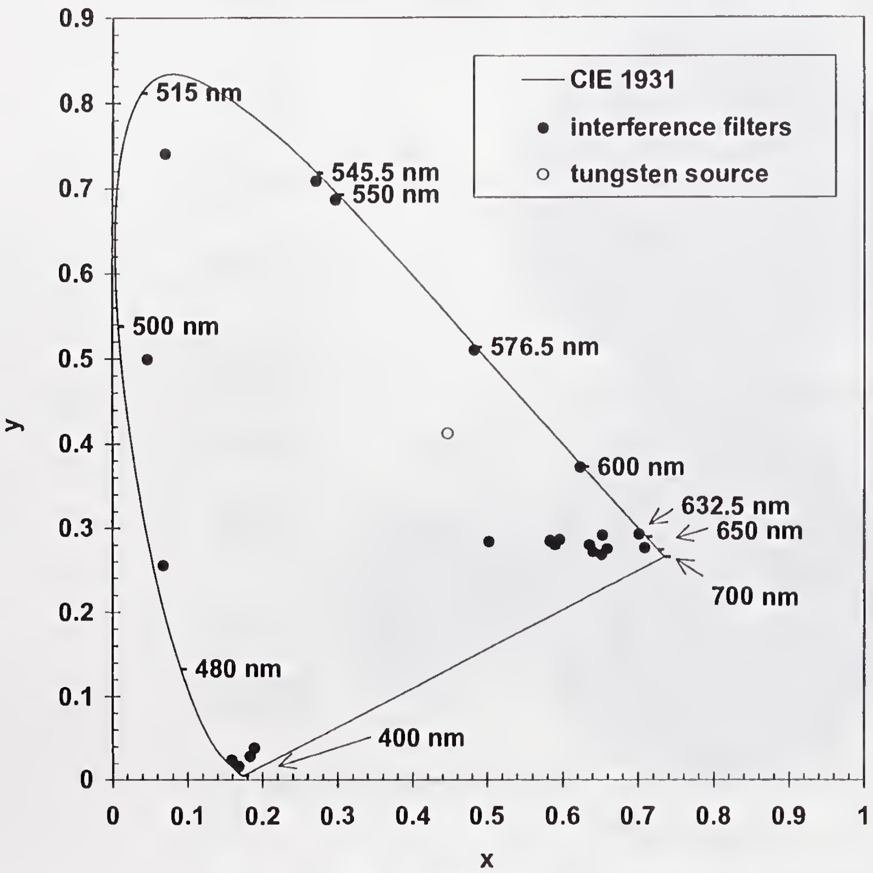
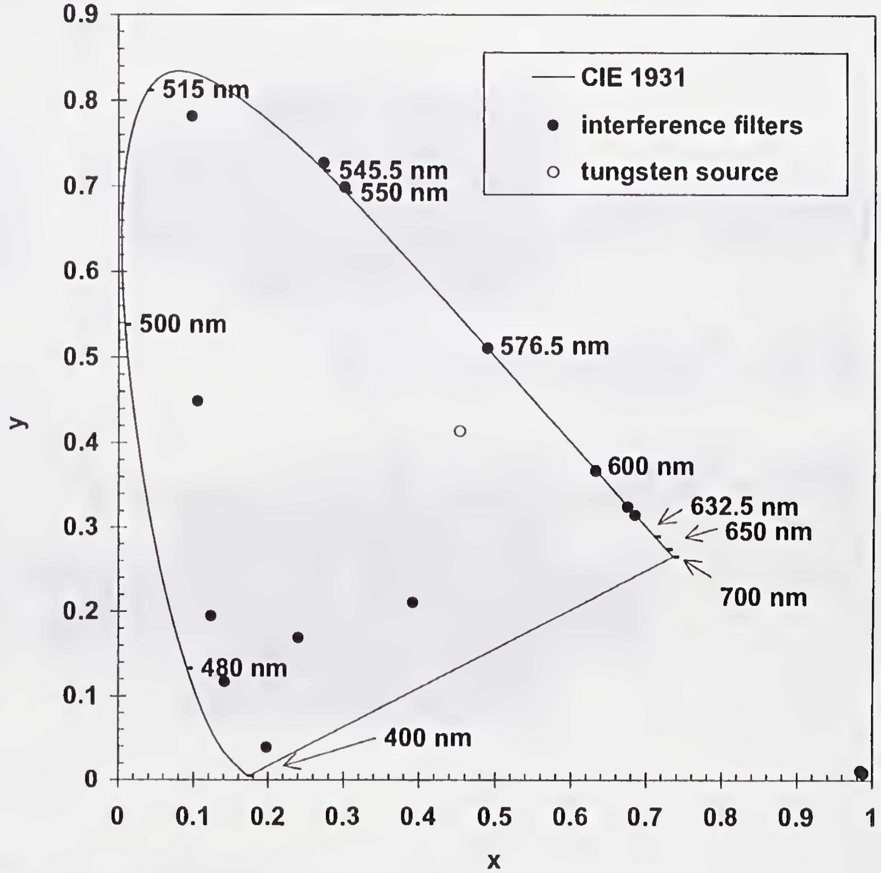
UNEXPECTED BEHAVIOR

Chromaticity Measurements with Spectroradiometer B



Chromaticity Measurements with Colorimeter A



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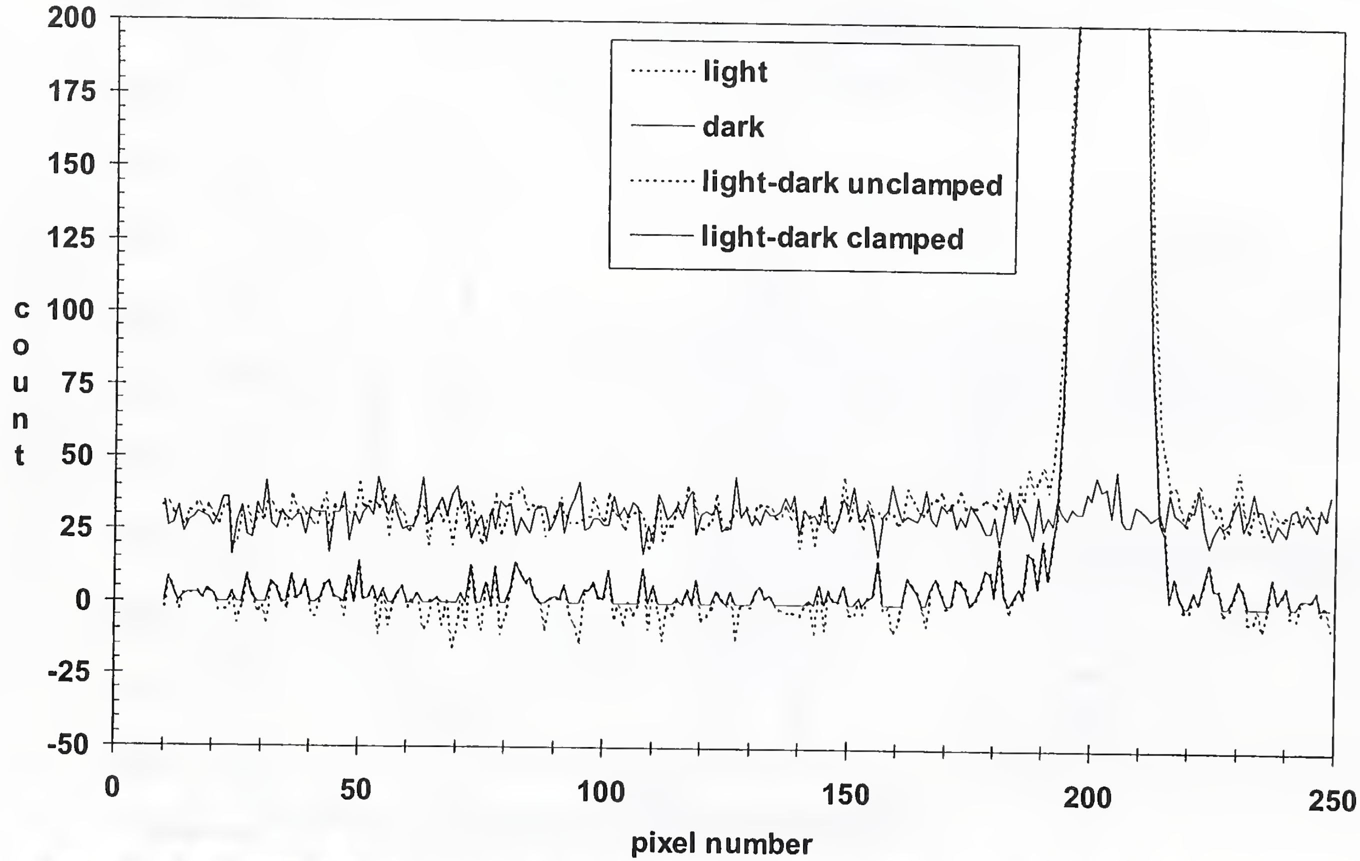
BACKGROUND NOISE AND SCATTERING

Raw Data of a Spectroradiometer Measuring a 700 nm Interference Filter



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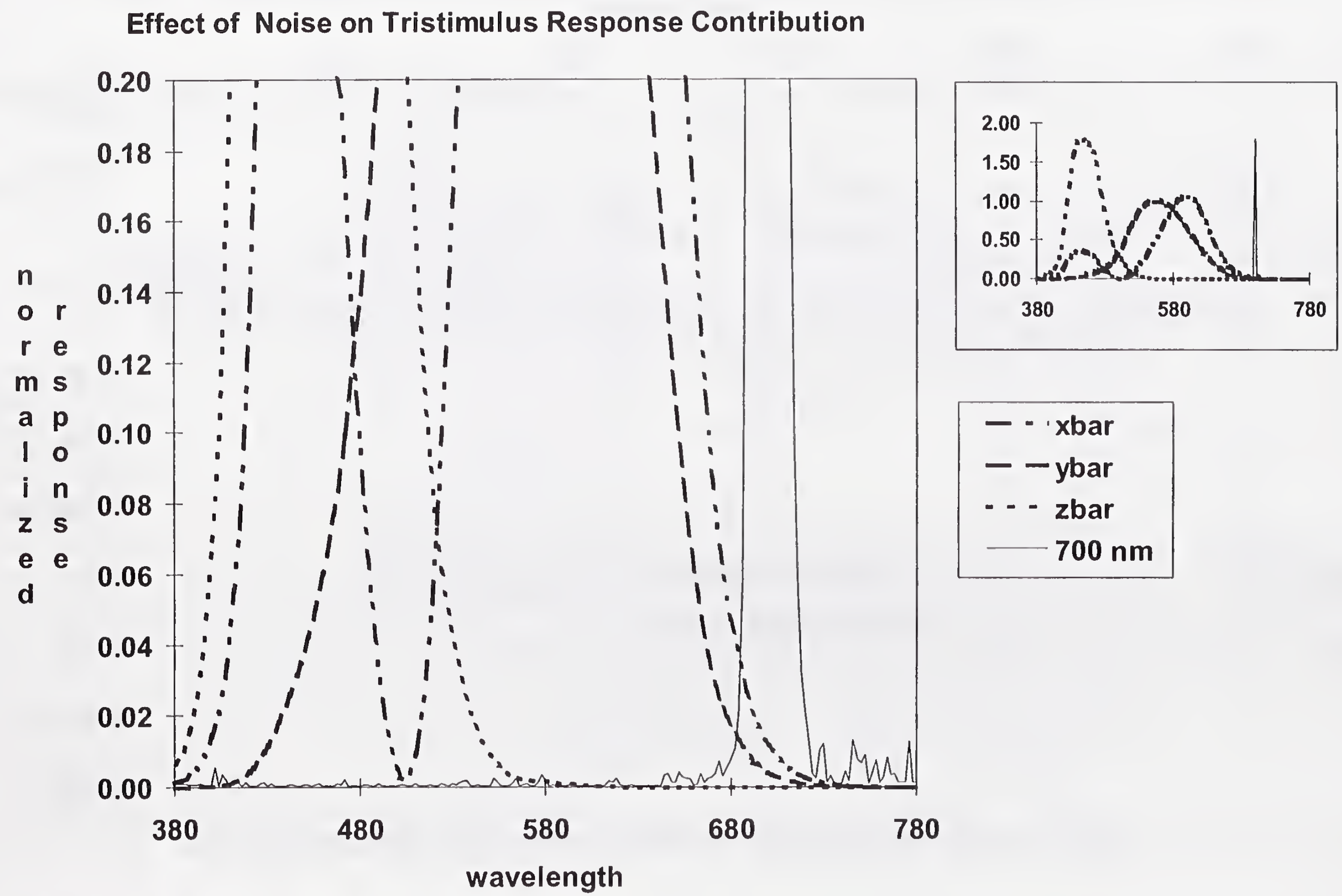
INWARD CURVING AT THE EXTREME VALUES



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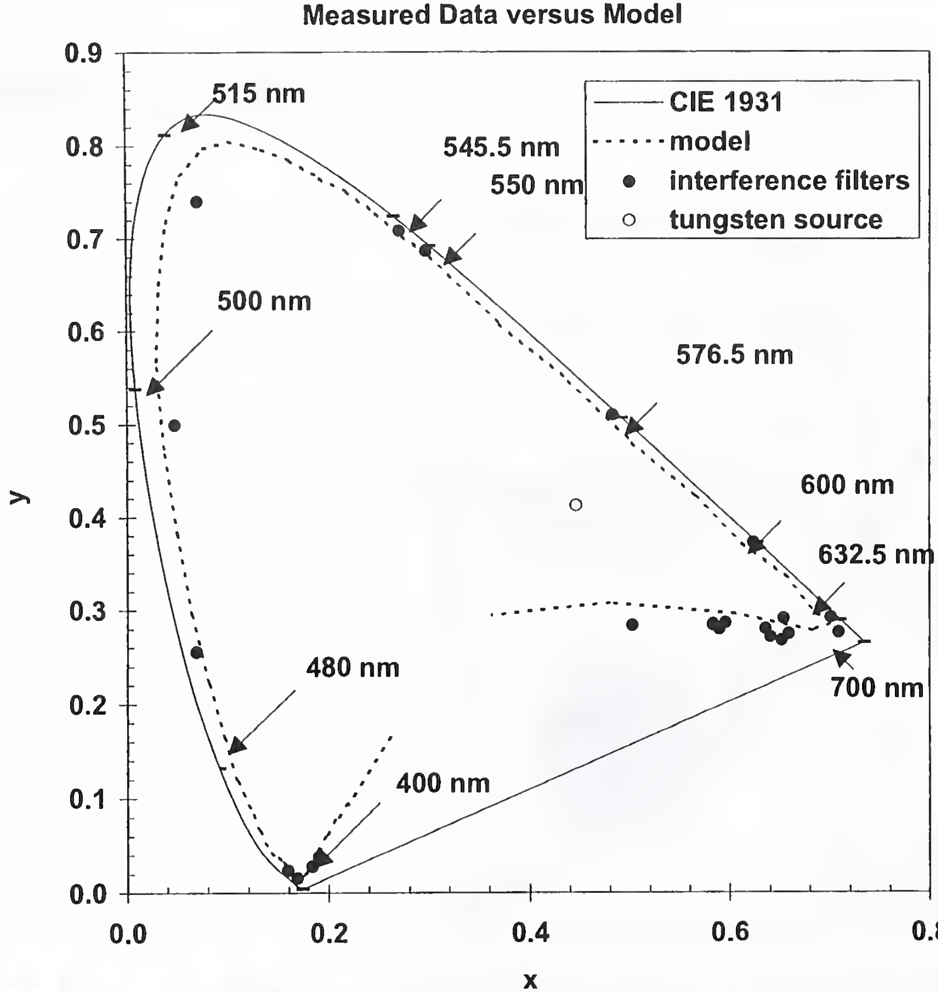
ERROR MODEL



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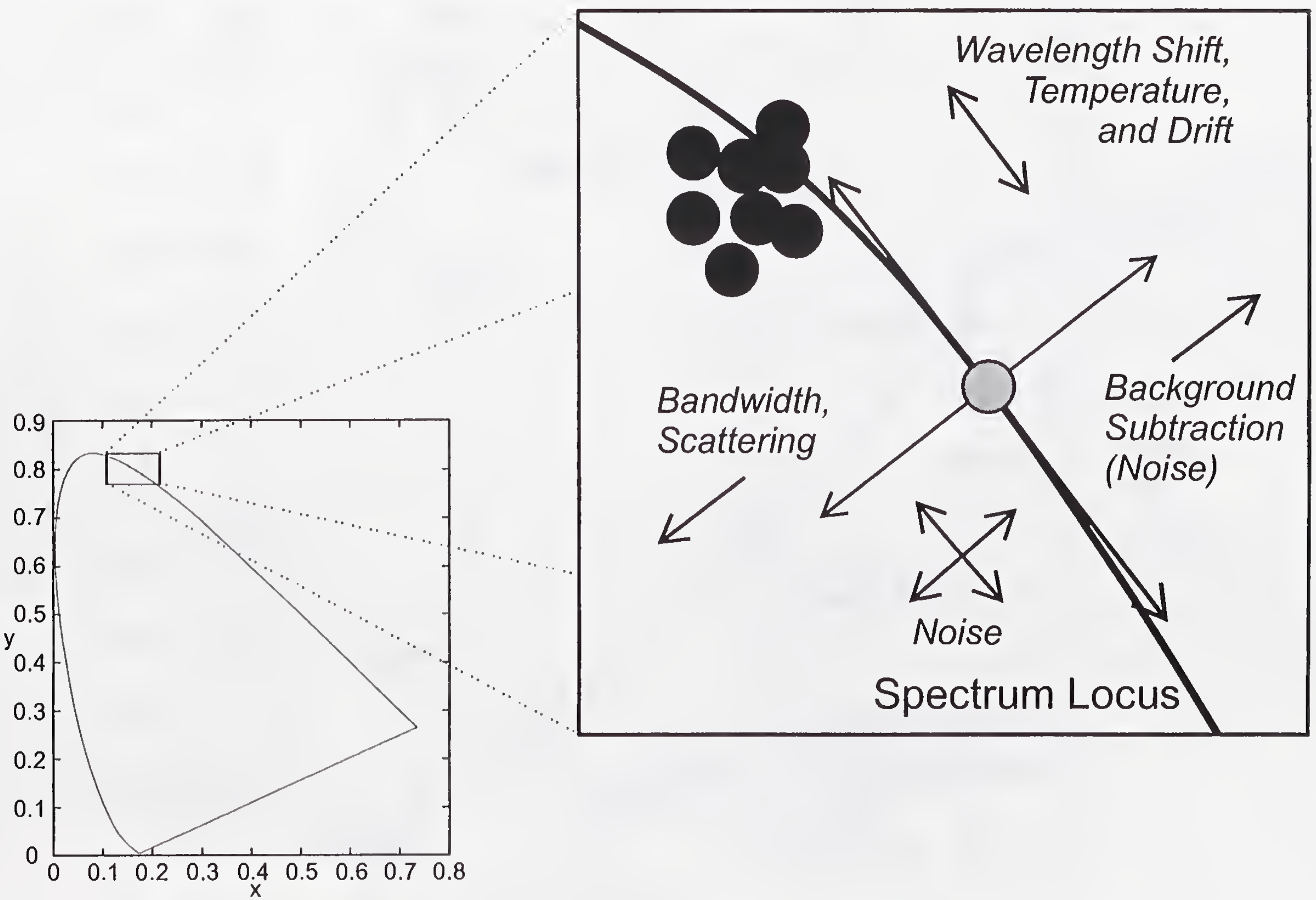
SOURCES OF ERROR



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DISPLAY REFLECTION CHARACTERIZATION

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REFLECTION

- **REFLECTIONS FROM DISPLAY SURFACE**

  REFLECTED LUMINANCE FROM A DISPLAY SURFACE IS USUALLY CHARACTERIZED AS BEING DIFFUSE (LAMBERTIAN) AND SPECULAR. IS THIS ACCURATE?

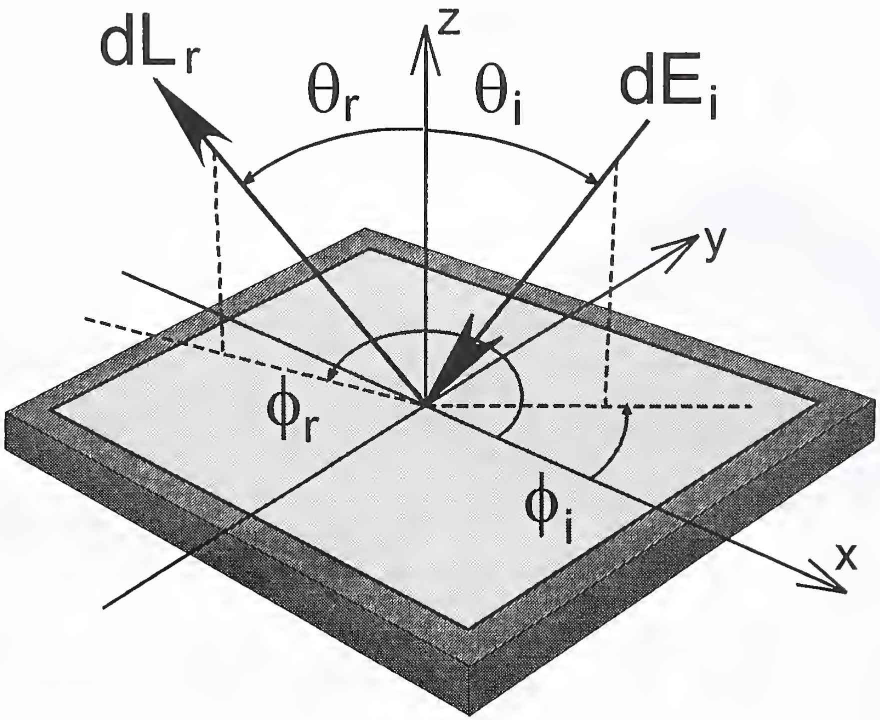
- **LENS FOCUS AND APERTURE PROBLEMS**

  DOES THE FOCUS LENGTH AND APERTURE OF THE MEASURING LENS HAVE AN EFFECT ON THE MEASURED REFLECTED LUMINANCE?

BRDF

GENERALIZATION OF

$$"L = qE"$$



$$dL_r(\theta_r,\phi_r) = B(\theta_i,\phi_i,\theta_r,\phi_r)dE_i(\theta_i,\phi_i)$$

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TOTAL REFLECTED LUMINANCE

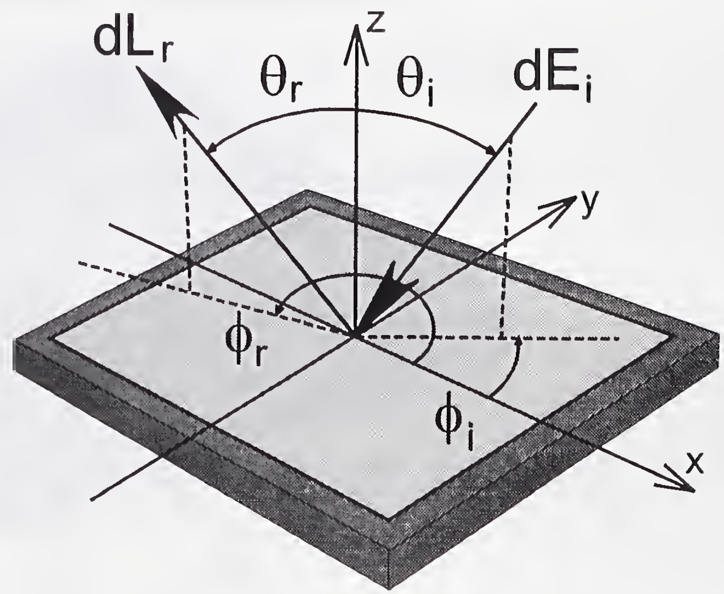
$$L_r(\theta_r,\phi_r) = \int_0^{2\pi}\int_0^{\pi/2} B(\theta_i,\phi_i,\theta_r,\phi_r)\,dE_i(\theta_i,\phi_i)$$

INCIDENT LUMINANCE

$$dE_i = L_i(\theta_i,\phi_i)\cos\theta_i\,d\Omega$$

ELEMENT OF SOLID ANGLE

$$d\Omega = \sin\theta_i\,d\theta_i\,d\phi_i$$



$$dL_r(\theta_r,\phi_r) = B(\theta_i,\phi_i,\theta_r,\phi_r)\,dE_i(\theta_i,\phi_i)$$

THREE-COMPONENT MODEL OF REFLECTANCE

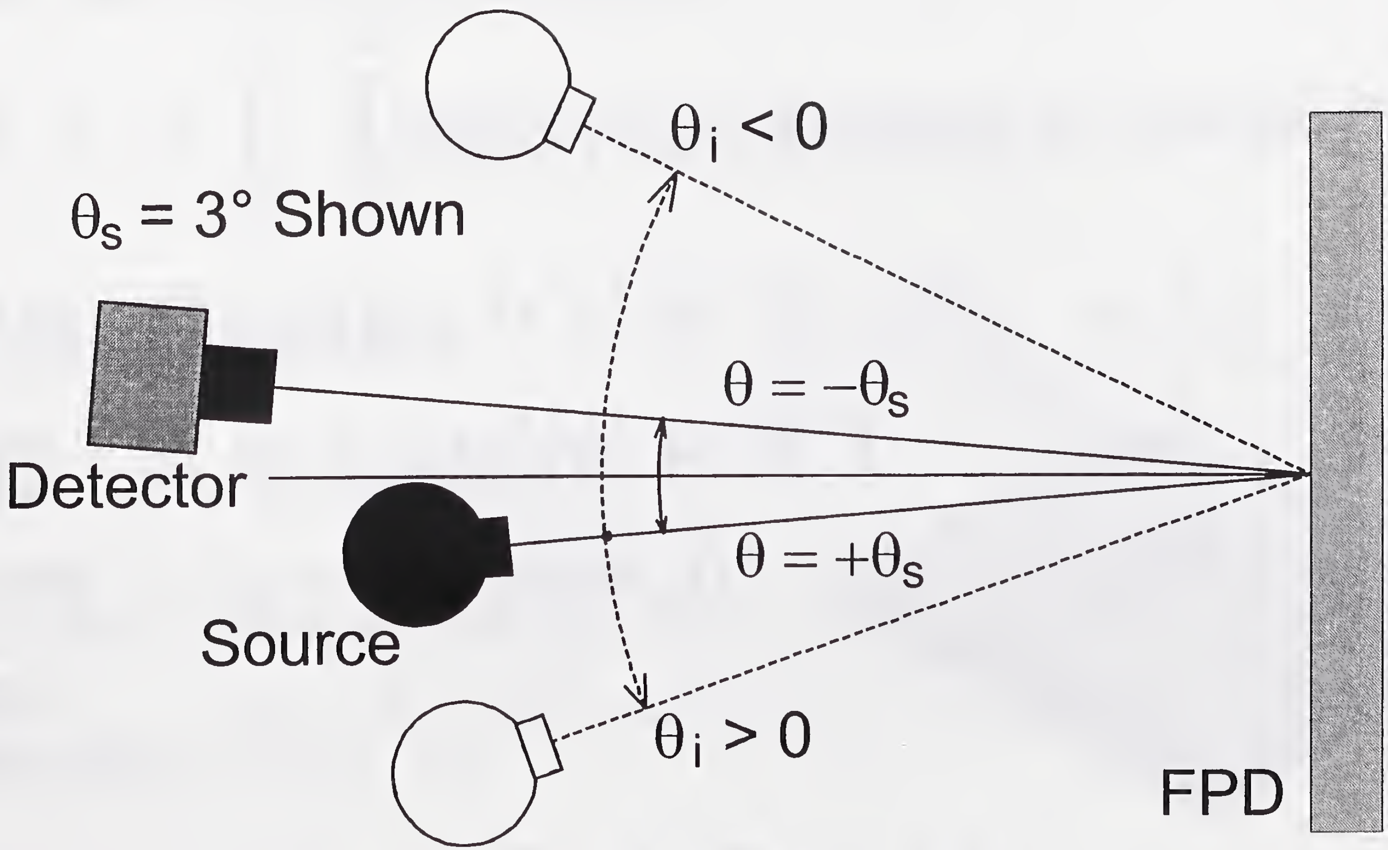
$$B = D + S + H$$

LAMBERTIAN (DIFFUSE) $D = q = \rho_d / \pi$

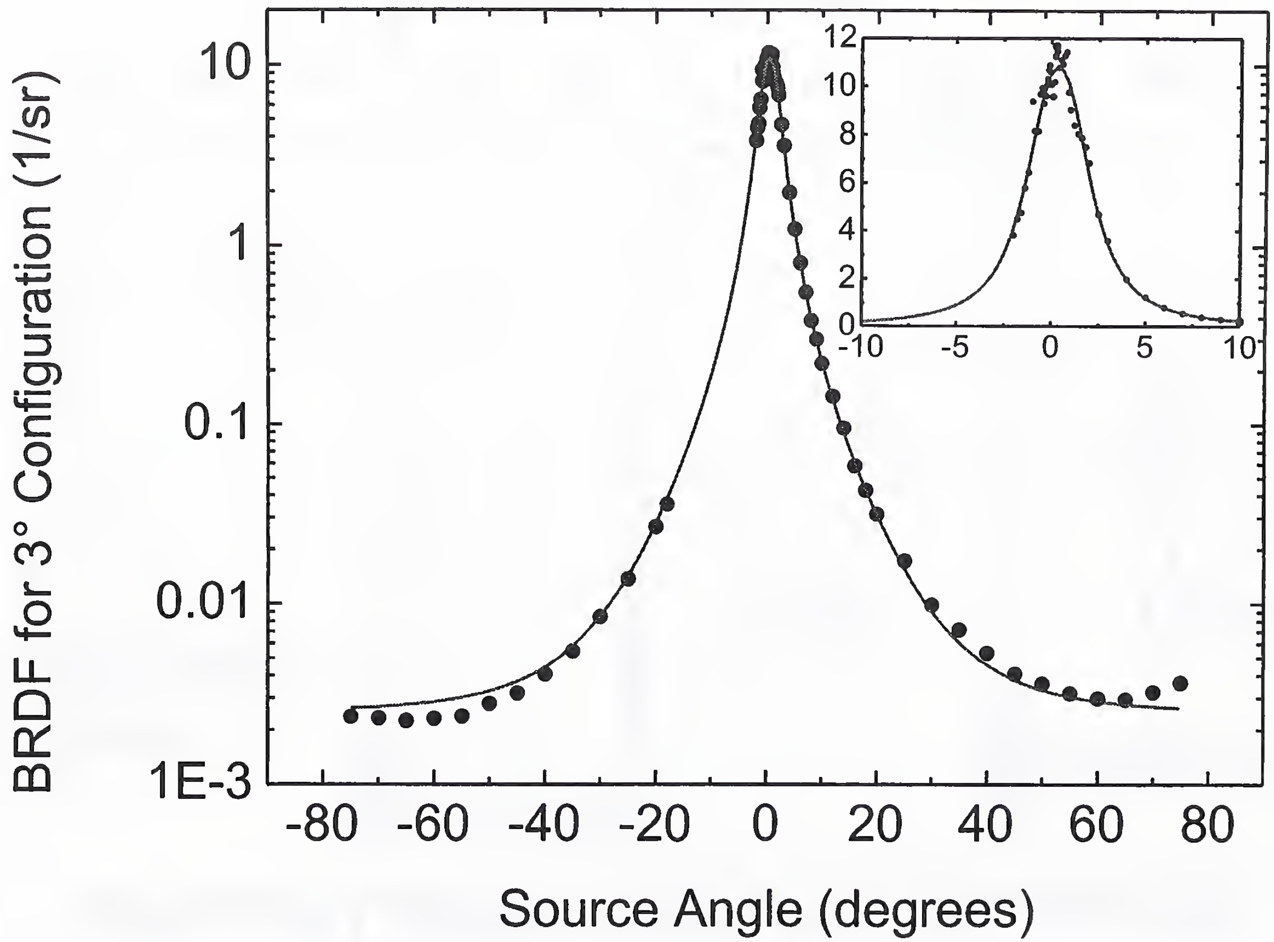
SPECULAR $S = 2\rho_s \delta(\sin^2\theta_r - \sin^2\theta_i)\delta(\phi_r - \phi_i \pm \pi)$

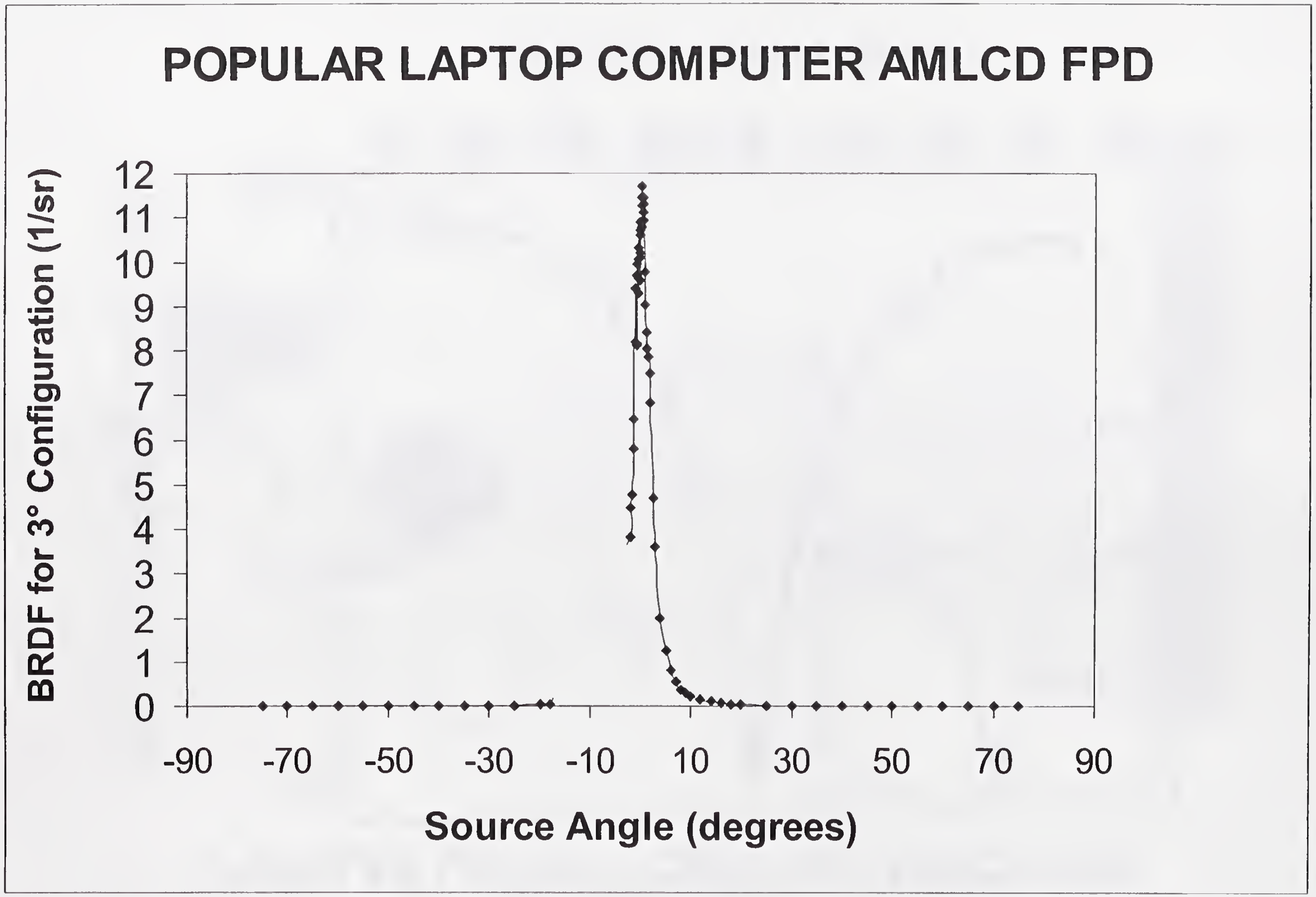
HAZE $H = H(\theta_i, \phi_i, \theta_r, \phi_r)$

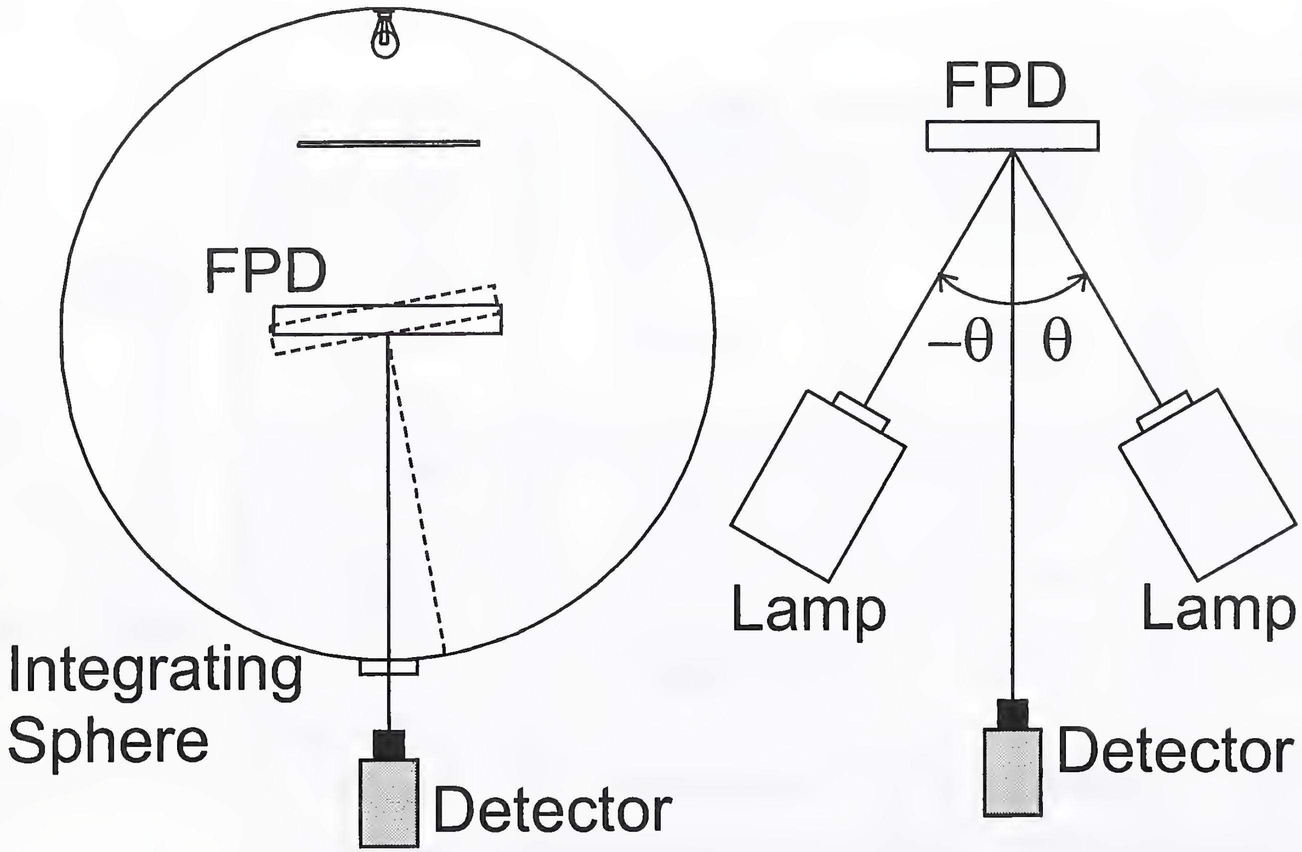
$$L_r(\theta_r, \phi_r) = qE + \rho_s L_s(\theta_r, \phi_r \pm \pi) + \int_0^{2\pi} \int_0^{\pi/2} H(\theta_i, \phi_i, \theta_r, \phi_r) L_i(\theta_i, \phi_i) \cos(\theta_i) d\Omega$$


θi < 0
θs = 3° Shown
θ = −θs
Detector
θ = +θs
Source
θi > 0
FPD

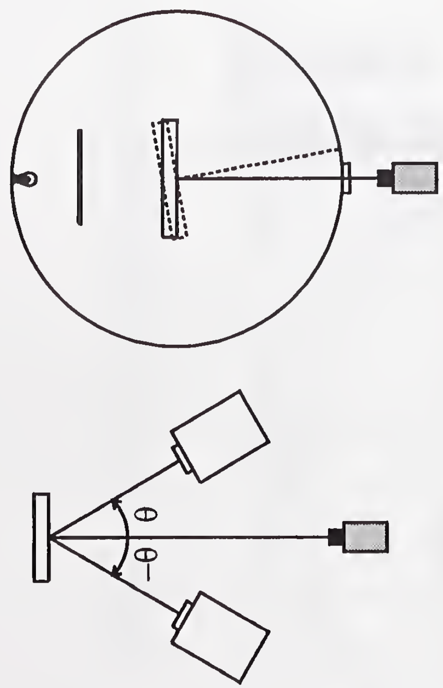
POPULAR LAPTOP COMPUTER AMLCD FPD



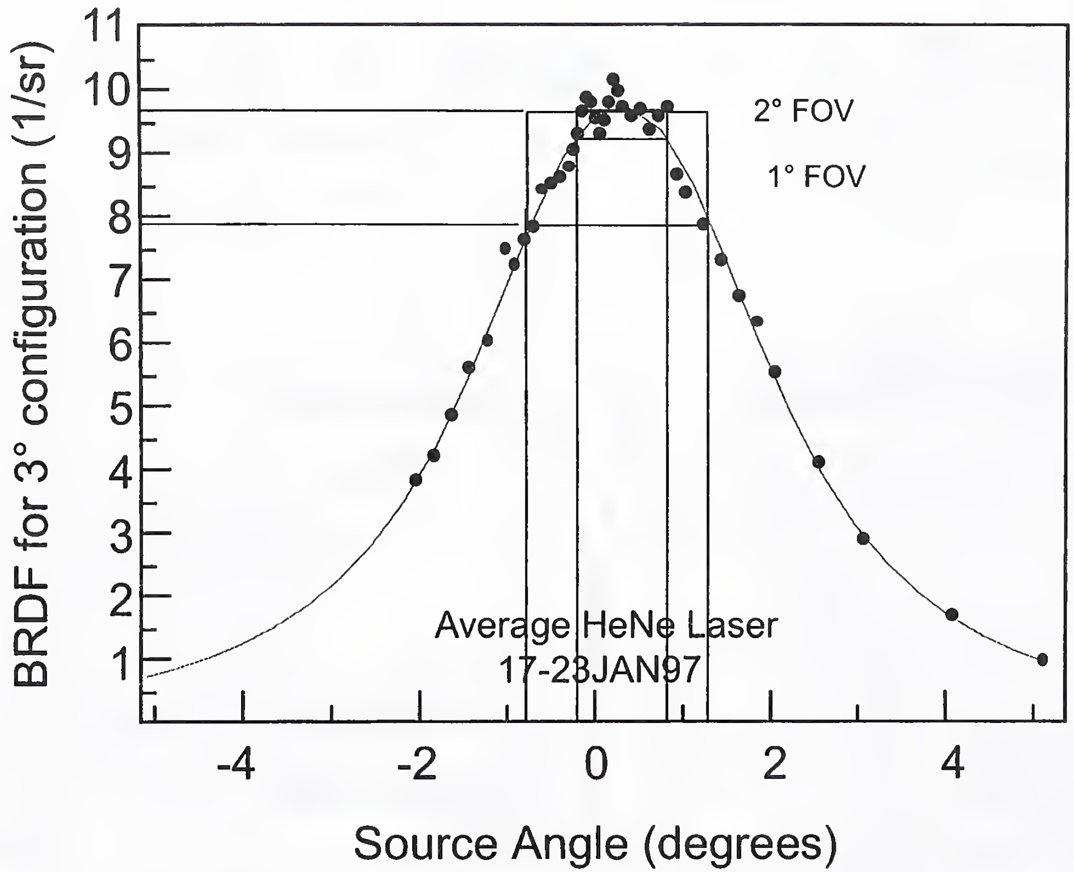

POPULAR LAPTOP COMPUTER AMLCD FPD
BRDF for 3° Configuration (1/sr)
12
11
10
9
8
7
6
5
4
3
2
1
0
-90
-70
-50
-30
-10
10
30
50
70
90
Source Angle (degrees)


FPD
Integrating
Sphere
Detector
FPD
$-\theta$
θ
Lamp
Lamp
Detector

BRDF Luminance Comparison (cd/m²)

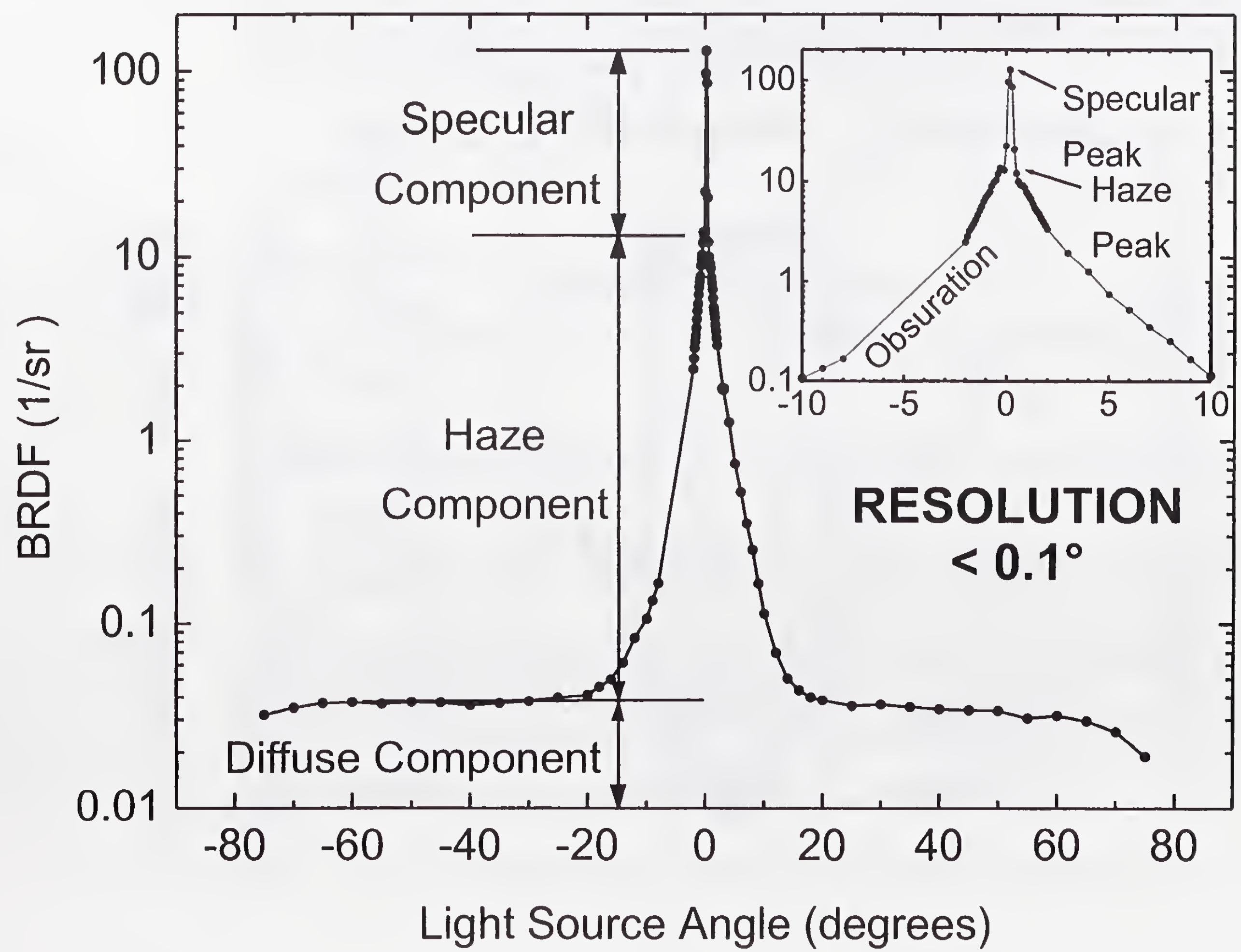


Case	Measured	Calculated	Error
Case 1 Int. Sph. + Hole	49.8	46.6	-6.3%
Case 2 Int. Sph.	75.3	77.7	3.2%
Case 3 Lamps $\theta = \pm 25°$	0.153	0.148	-3.2%
$\theta = \pm 30°$	0.0890	0.0861	-3.3%
$\theta = \pm 35°$	0.0535	0.0527	-1.4%



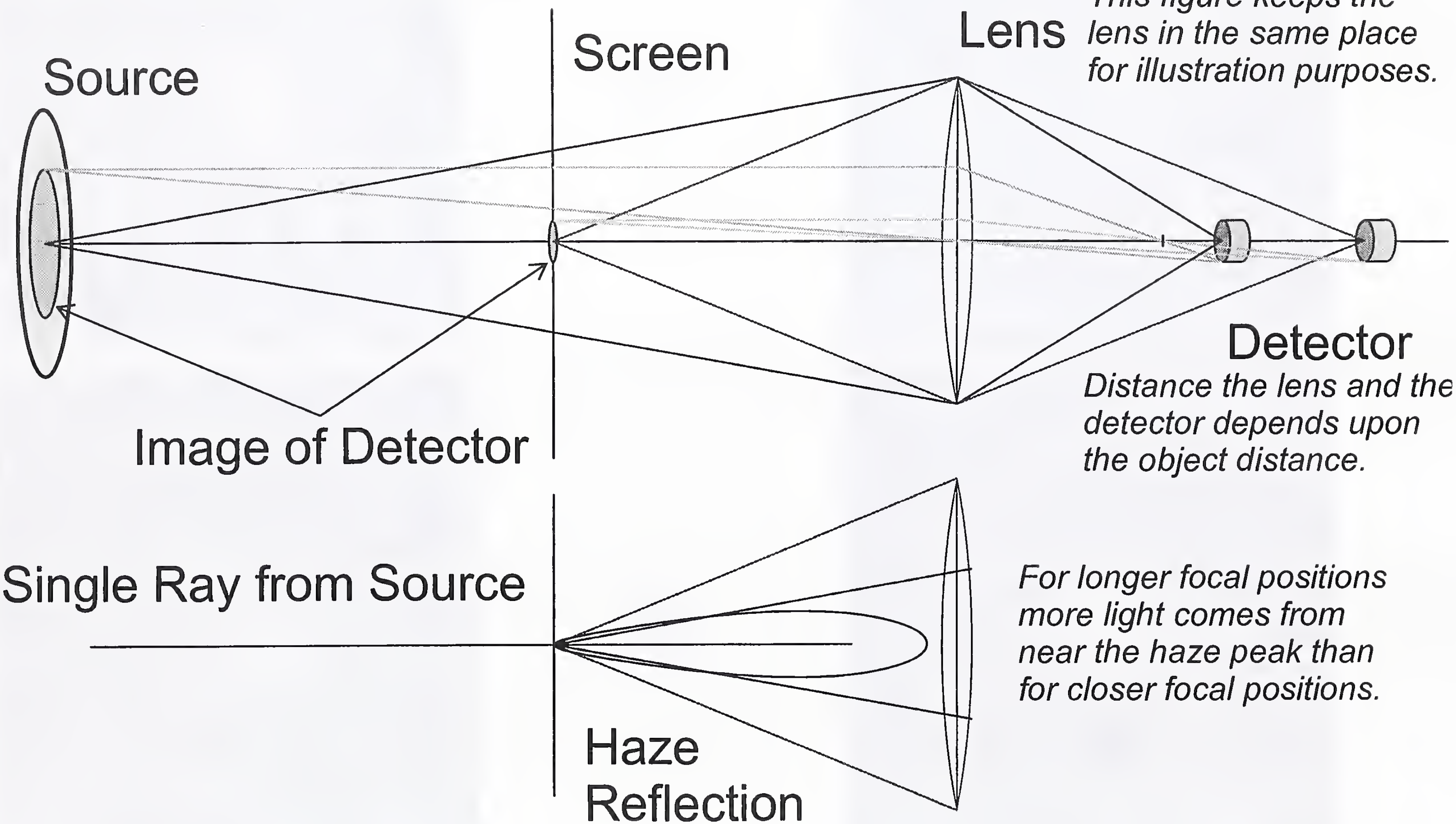
BRDF for 3° configuration (1/sr)
11
10
9
8
7
6
5
4
3
2
1
2° FOV
1° FOV
Average HeNe Laser
17-23JAN97
-4
-2
0
2
4
Source Angle (degrees)

SPECIALLY PREPARED SAMPLE (D + S + H)



UNFOLDED SPECULAR CONFIGURATION

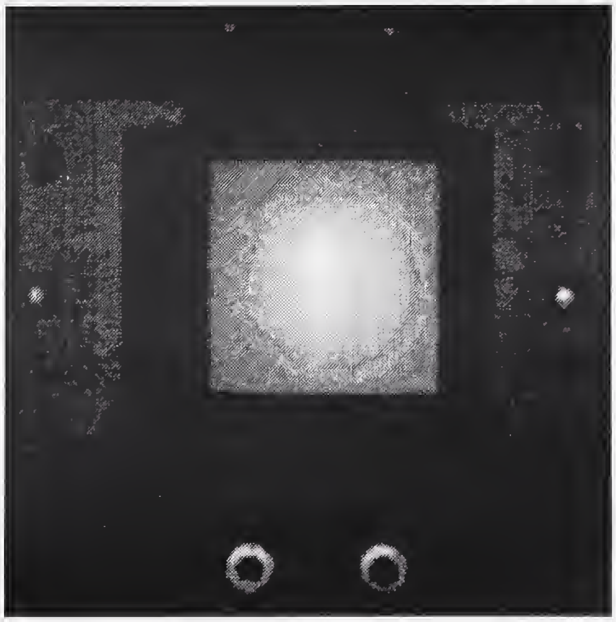
Focus on Screen or Source



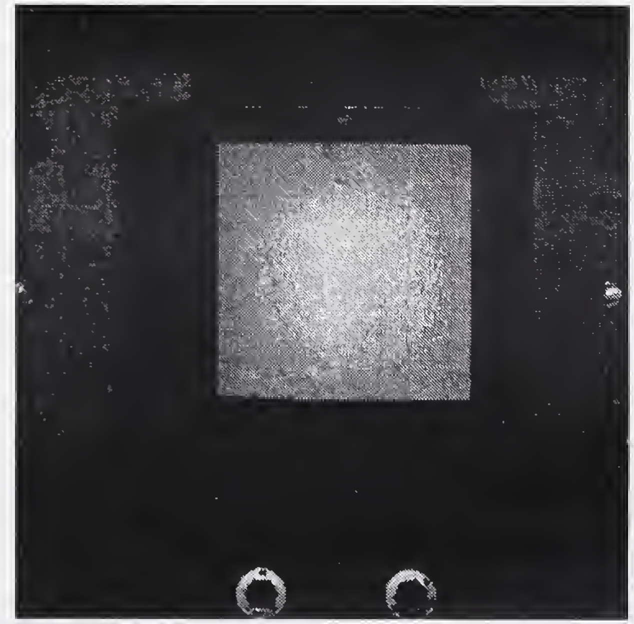
EXTENDED LIGHT SOURCE — HAZE SAMPLE

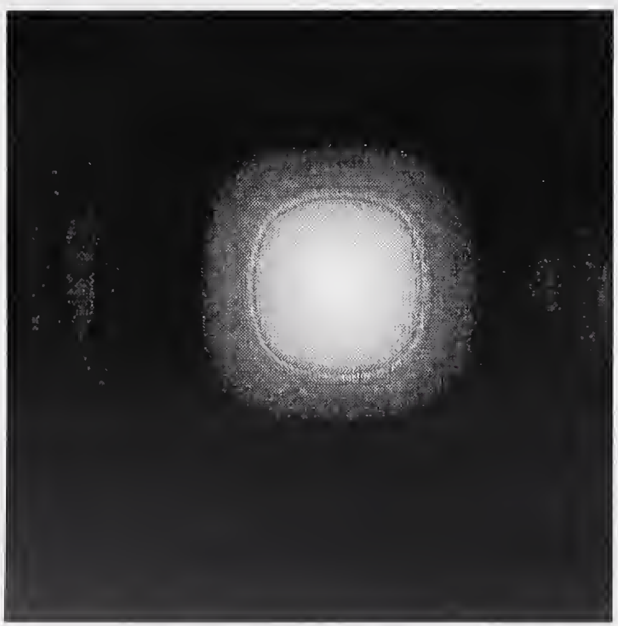
FOCUS ON SOURCE

FOCUS ON SCREEN

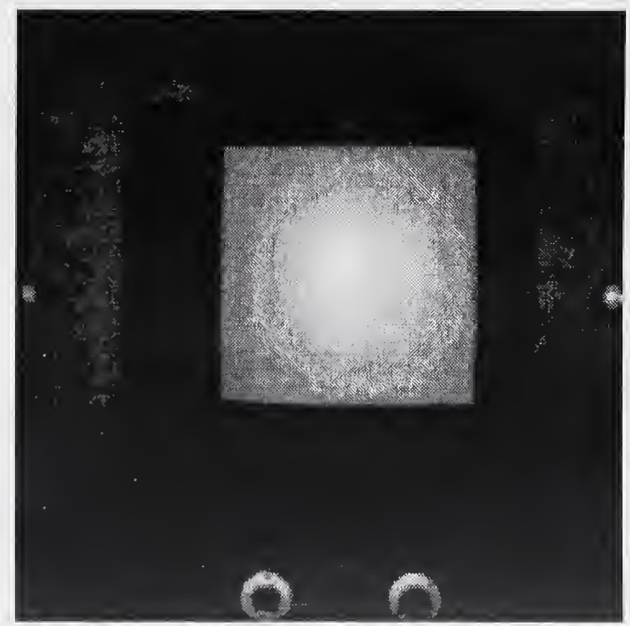


F32





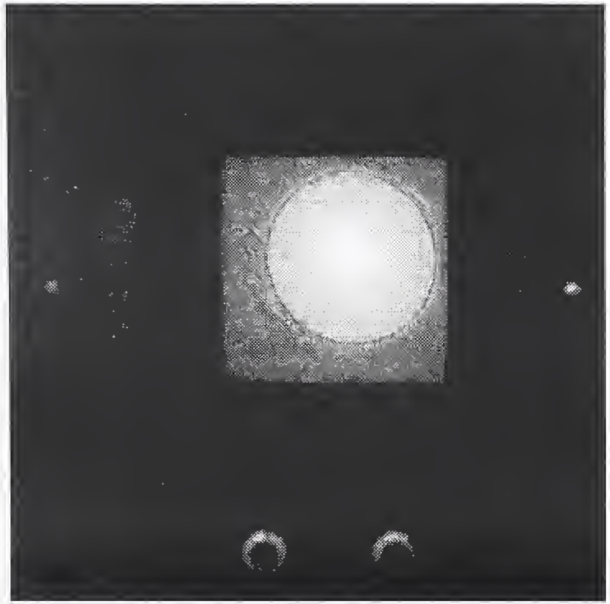
F2.8



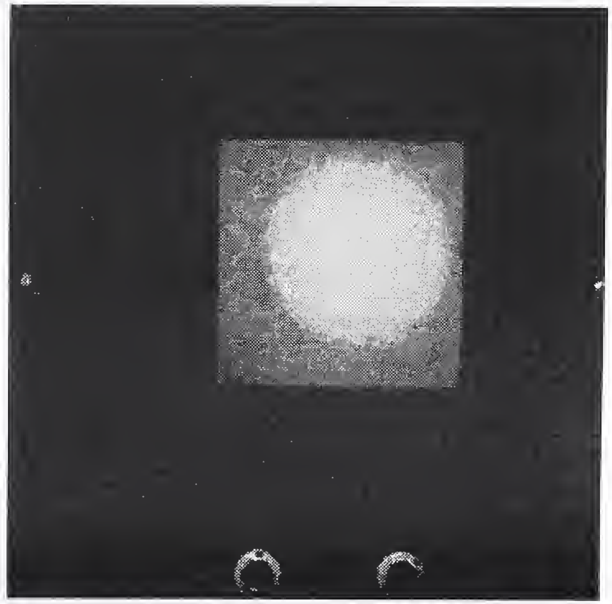
EXTENDED LIGHT SOURCE — SAMPLE A

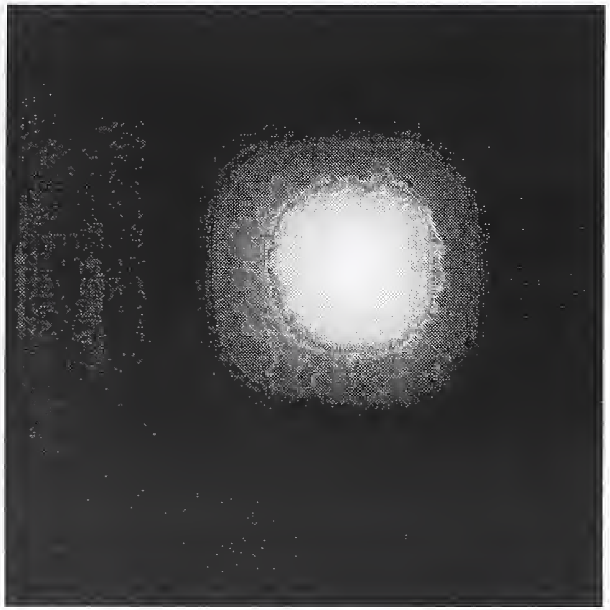
FOCUS ON SOURCE

FOCUS ON SCREEN

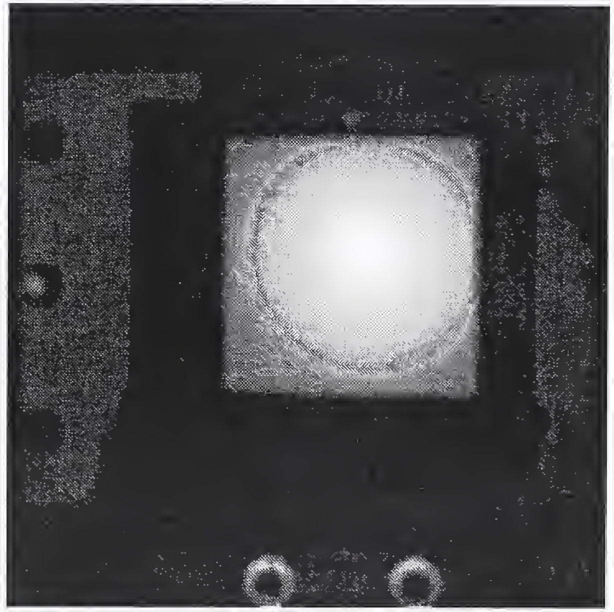


F32





F2.8

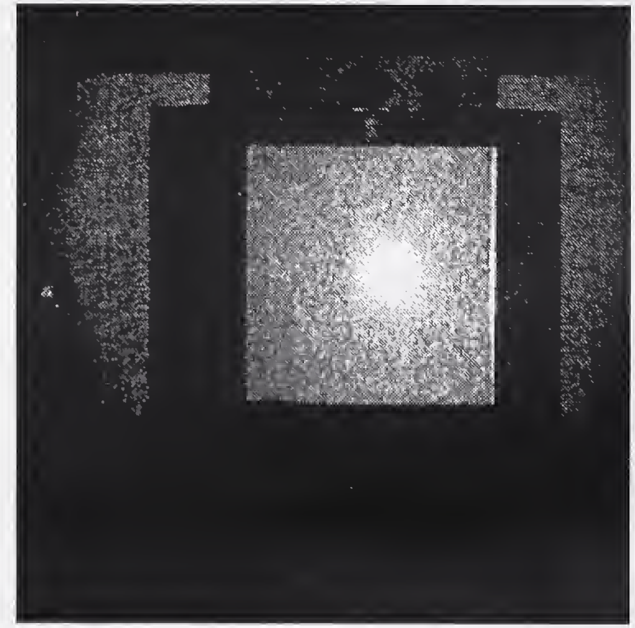


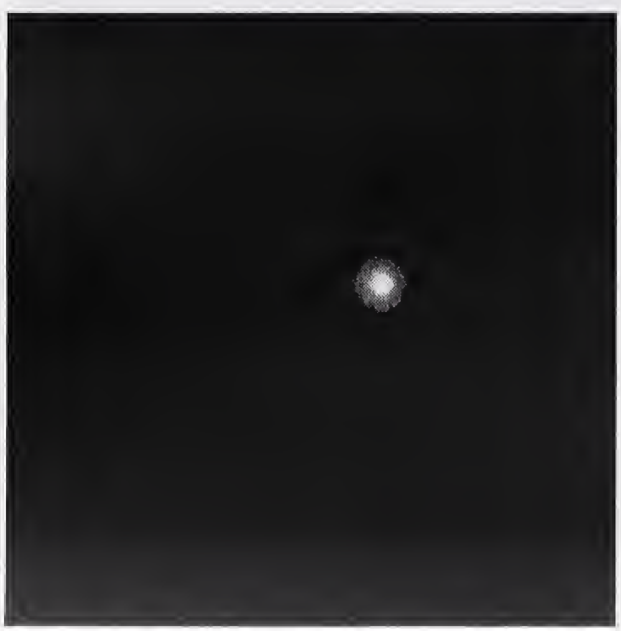
POINT LIGHT SOURCE — HAZE SAMPLE

FOCUS ON SOURCE

FOCUS ON SCREEN

F32

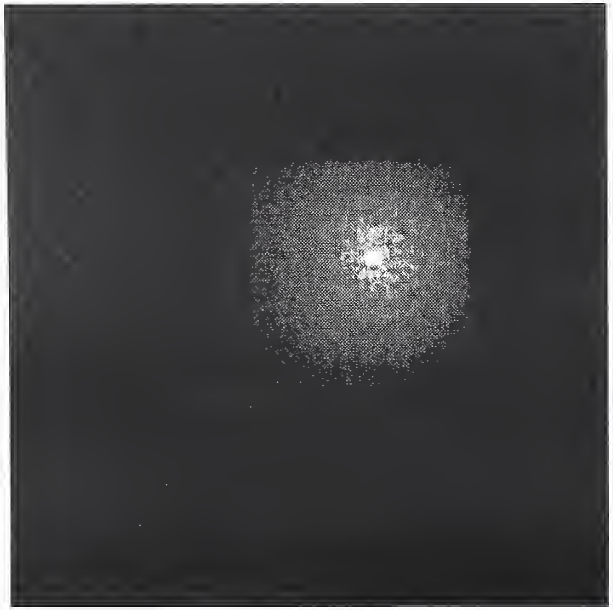




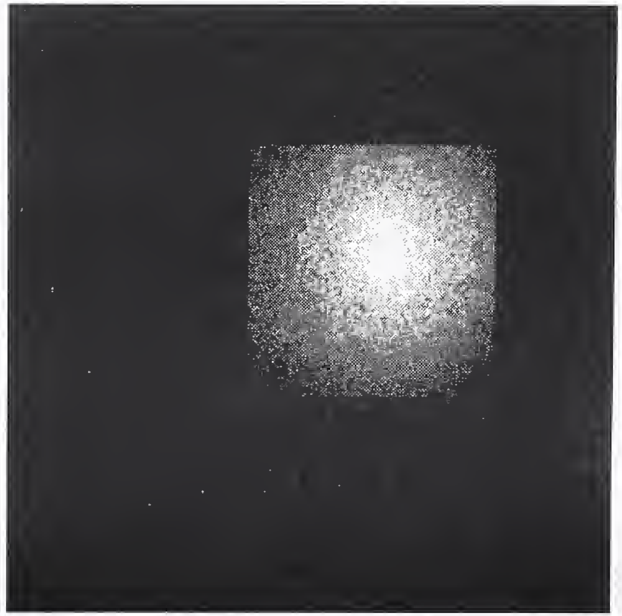
F2.8

POINT LIGHT SOURCE — SAMPLE A

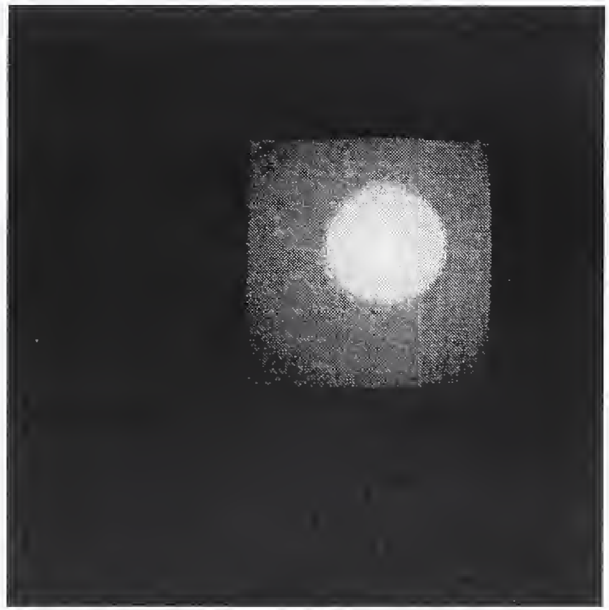
FOCUS ON SOURCE | FOCUS ON SCREEN



F32



F2.8



All measurements were made using a 31 x 31 pixel square center on the peak CCD reading (961 pixels)

The 2.3 m focus corresponds to focussing on the source.

The 1.3 m focus corresponds to focusing on the screen

Test Sample	Light Source	Aperture	Focus	Luminance (CCD Counts)	Reduction (%)
Haze	Extended	f32	2.3 m	5.42E+07	
	Extended	f32	1.3 m	4.34E+07	
					-20.0
Haze	Extended	f2.8	2.3 m	5.16E+07	
	Extended	f2.9	1.3 m	4.34E+07	
					-16.0
A	Extended	f32	2.3 m	5.75E+07	
	Extended	f32	1.3 m	4.77E+07	
					-17.0
A	Extended	f2.8	2.3 m	5.32E+07	
	Extended	f2.9	1.3 m	4.05E+07	
					-23.8
Haze	Point	f32	2.3 m	6.78E+06	
	Point	f32	1.3 m	6.19E+06	
					-8.7
Haze	Point	f2.8	2.3 m	1.52E+07	
	Point	f2.9	1.3 m	5.53E+06	
					-63.6
A	Point	f32	2.3 m	2.50E+06	
	Point	f32	1.3 m	2.39E+06	
					-4.6
A	Point	f2.8	2.3 m	2.07E+07	
	Point	f2.9	1.3 m	5.35E+06	
					-74.2

ADVANTAGES OF USING A GLOSS-BLACK CONE MASK FOR CONTRAST AND BLACK MEASUREMENTS

VESA/NIST Display Forum Workshop (Track II)

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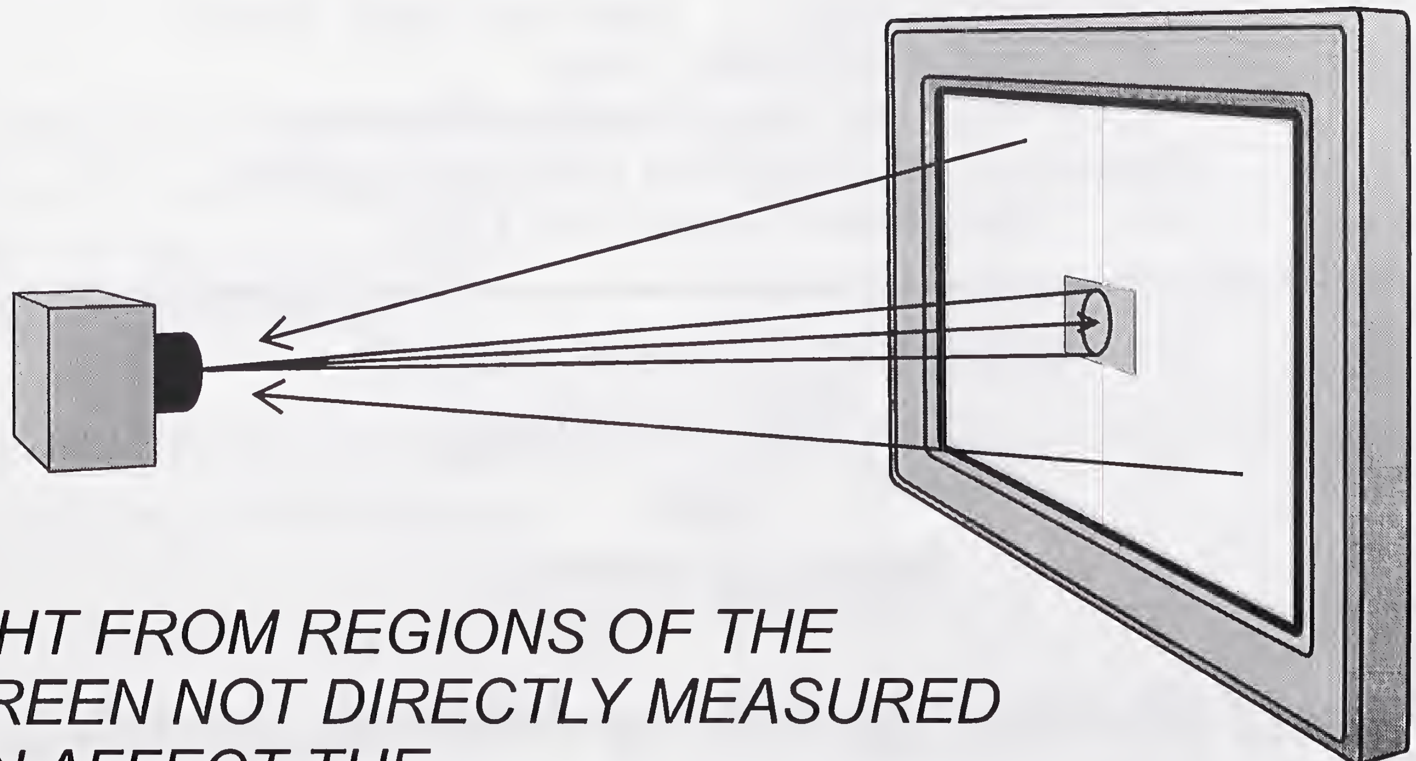
Phone: (301) 975-3842 Fax: (301) 926-3534



LIGHT FROM REGIONS OF THE SCREEN NOT DIRECTLY MEASURED CAN AFFECT THE MEASUREMENT—VEILING GLARE OR LENS FLARE—BLACK, WHITE, AND COLORS ARE CORRUPTED BY GLARE.

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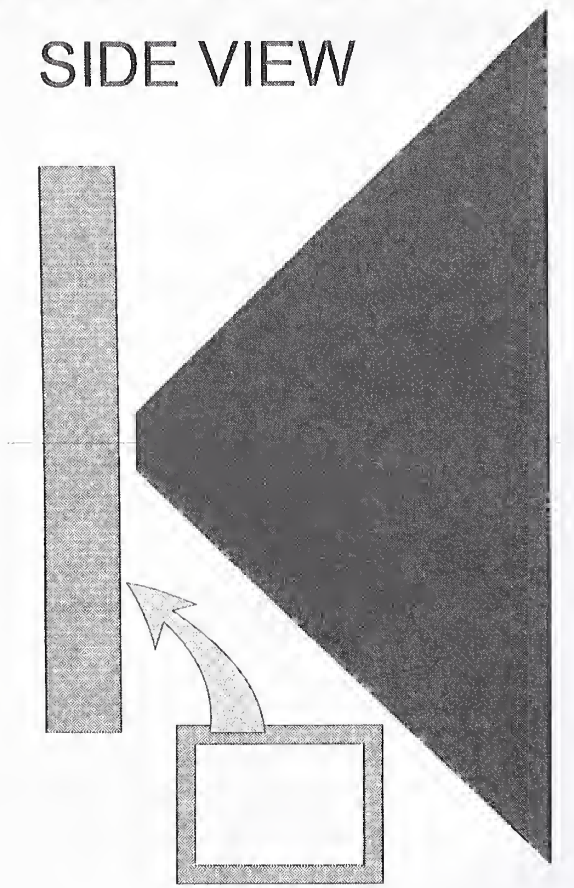
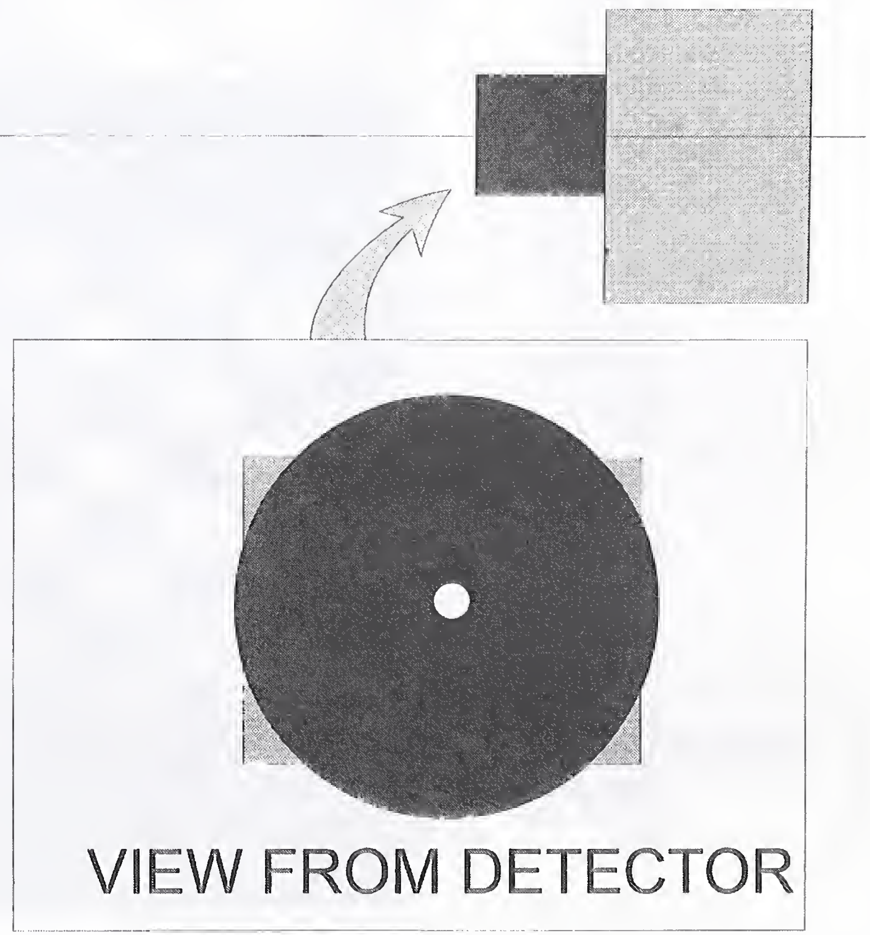
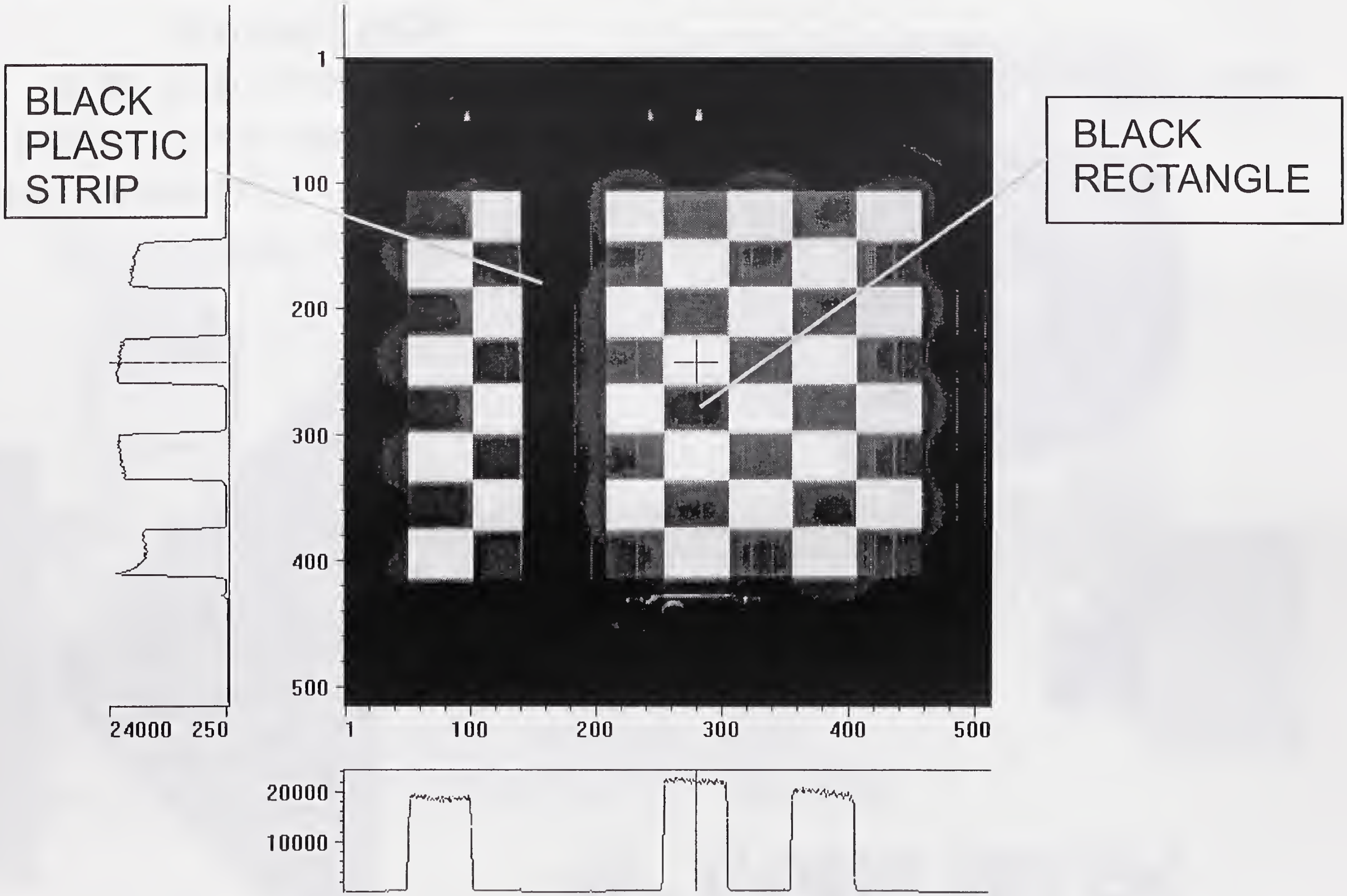
45° CONE MASK

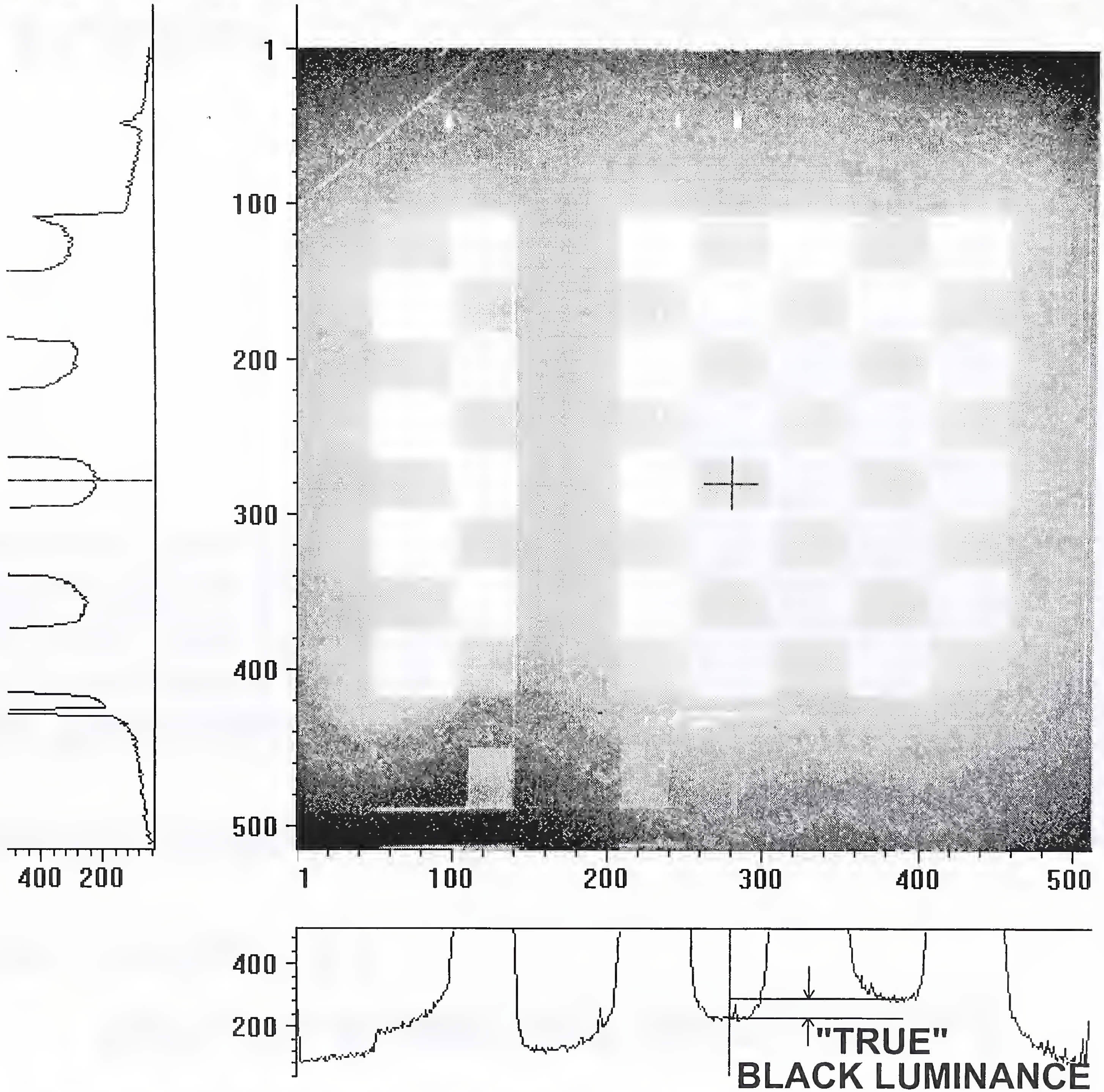




Gloss black plastic cone minimizes light reflecting back onto screen also minimizes light from rest of screen reaching lens.

USE OF REPLICA MASKS





1
100
200
300
400
500
400 200
"TRUE"
BLACK LUMINANCE

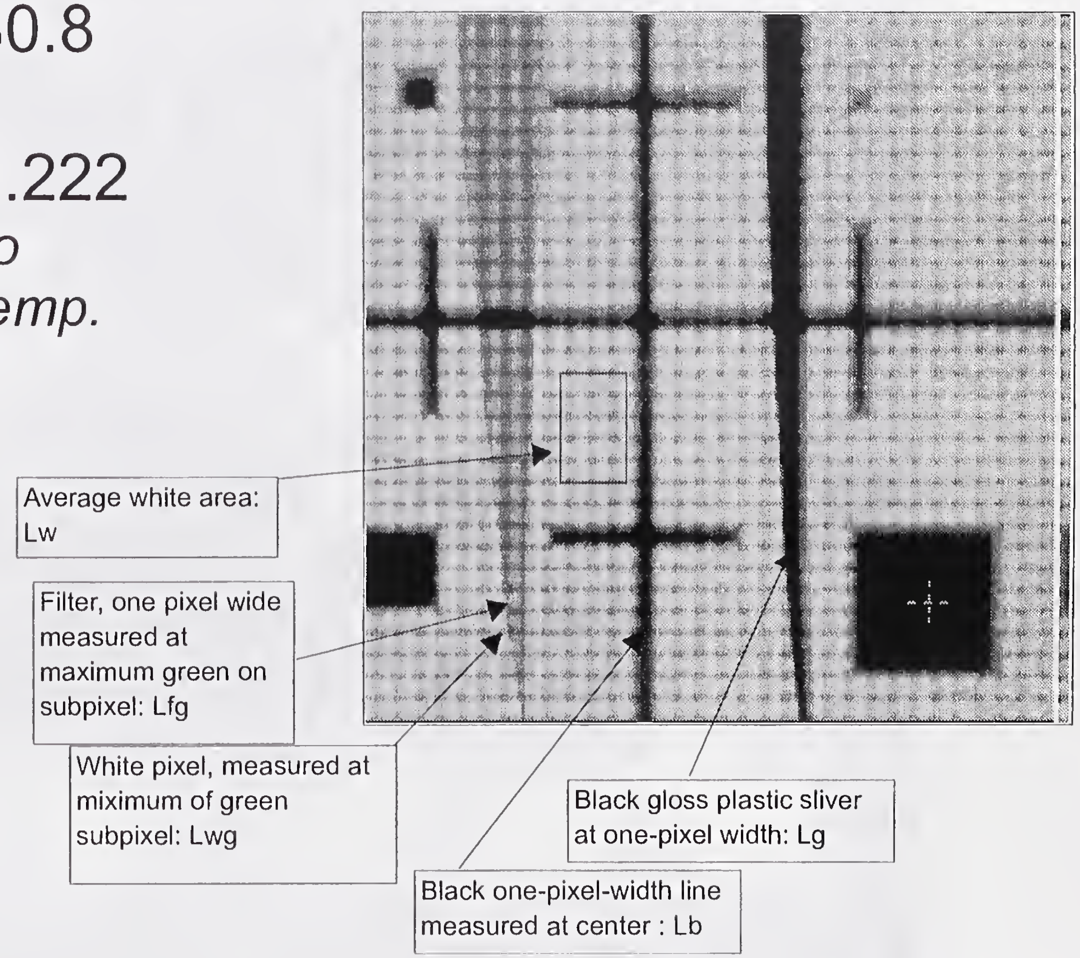
REPLICA MASKS FOR SINGLE PIXELS

Dumb Contrast = 8.6

Corrected Contrast = 30.8

Filter Transmission = 0.222

T = 0.173 room temp, if no temp. coef. 28% error, if temp. shift to 0.200 (anticipated) then have 11% error.



VIII. Afternoon Session - Conclusions

Shooting at a Moving Target:

Alternative Display Technologies and LCDs

SRI CONSULTING

Subsidiary of SRI International

Mitchell Halpern PhD

NIST/VESA Display Forum

October 20, 1997

Two Fundamental Phenomena Have Hindered Accurate Forecasts of New Technology Commercialization

- Selective Stoppage of Time
  - — The assumption that new technology progresses while "old" technology remains moribund
  - — Of course, the "multifaceted, dynamic status quo" much more often than not remains lively
- Hype
  - — Looking at the world through rose-colored glasses: Peer review and the New York Times
  - — Relying on the forecasts of scientists/engineers: "The fox watching the hen house" syndrome
  - — Forgetting the end-user

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(In)Famous Quotes Abound in the History of Technology Commercialization

- "The CRT will disappear by 1997...." (Uttered by more than one LCD analyst)
- "High-temperature superconductors will be a multi-billion dollar per annum business by 1995..."
- "GaAs will dominate silicon in the marketplace..."
- "Conductive polymers will substitute for copper wiring..."

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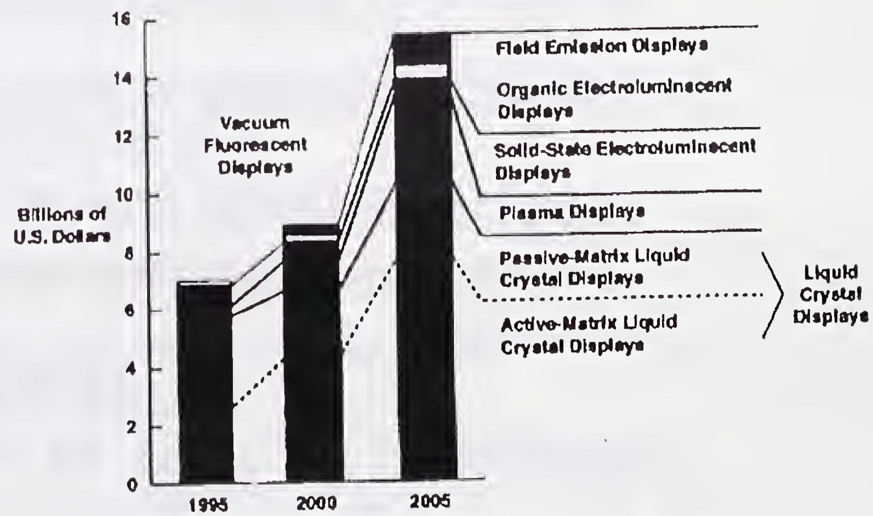
Market Projections for Alternative Display Technologies Have Been Affected by Hype and the Selective Stoppage of Time

- The commercialization of field-emission displays and even gas plasma displays has been much slower than predicted
  - Most original predictions from as late as 2-3 years ago were contemplating major markets for FEDs and PDPs by 1998-1999
  - The conventional wisdom now keeps moving major commercialization at least 3-5 years out

FLAT-PANEL-DISPLAY* WORLD MARKET PROJECTIONS



* High-information-content displays.

Source: SRI Consulting

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The Multifaceted Dynamic LCD Marches On....

- Increased viewing angles
- Increased brightness
- Increased efficiency
- Improved performance of passive devices
- Increased size via tiling
- Improved performance of portable, reflective color displays
- Dramatic cost reductions (more reflective of competition for market share than lower manufacturing costs)

Alternative Display Technologies Face a Rapidly Closing Window of Opportunity

Display Technology	Major Application/ (Size Range in Inches Diagonal)	Window of Opportunity	Comments
Gas-plasma displays	Consumer wide-screen TV (40 to 60)	Now through 2000	Other big-screen technologies such as projection, tiled liquid crystal displays (LCDs) will compete.
Field-emission cathode displays	Military systems, personal digital assistants, automotive displays (6 or less) workstation monitors (17 to 20)	Now through 1999 for smaller sizes; now through 2002 for larger sizes	Improvements in LCDs result in narrow opportunity windows. The 17- to 20-inch size range is still a weak spot for LCDs, but this situation won't last forever.
Solid-state electroluminescent displays	Military, transportation, and medical systems and equipment (6 to 12)	Now through 2005	Existing small niches in ruggedized markets will be difficult to displace.
Organic electroluminescent displays	Automotive systems, personal computer devices (including games), medical equipment, and transportation systems (3 to 12)	Now through 2005 and beyond	Many technical question marks preclude an accurate analysis.
LCD projection	Home theater (40 to 60); business presentations (larger than 60)	Now through 2001	The technology is extremely promising, but market size will depend strongly on cost.
Digital micromirror projection	Home theater (40 to 60); digital cinema and business Presentations (larger than 60)	Now through 2000 for home theater; now through 2005 for digital cinema and business presentations	Price and market size will depend on improvements in the production yields of micromirror devices.

Source: SRI Consulting

Subsidiary of SRI International

Displays for Convergence

Mark Kirstein, Director of Research

In-Stat

www.instat.com

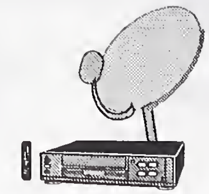
Where We Want to Go Today

- Digital TV and the Battle of the Boxes
- Every Box Needs to Display
- Content Drives Display Requirements
- PC Markets

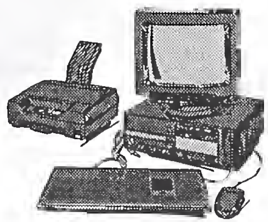
Two Keys to Digital TV

- Digital Transmission System
  - FCC Broadcast Standards
  - DSS/Digital DBS
  - Digital Cable
  - (DVD)
- Multiscan Display Screen
  - Resolution Changes
  - Interlaced vs Non-Interlaced
  - Scan Rate

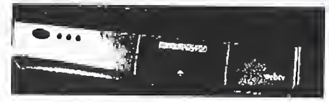
Today's Markets



Consumer Device	Rich Content	Interactivity	Box Cost	Content Cost
•Broadcast TV	↑	↓	↓	Advertising Subsidy ↓
•Analog Cable TV	↑	↓	Content Subsidy ↓	Advertising Subsidy →
•DBS (Direct Broadcast Satellite)	↑	↑	Content Subsidy ↓	Advertising Subsidy →



Today's Markets



Consumer Device	Rich Content	Interactivity	Box Cost	Content Cost
•Consumer PC	→	↑	↑	→
•Internet Appliance	↓	↑	↓	→
•Video Game Console	↑	↑	↓ Content Subsidy	↑

Emerging Markets

Consumer Device	Rich Content	Interactivity	Box Cost	Content Cost
•DVD	↑	↑	↓	↑
•Entertainment PC	↑	↑	↑	→
•Digital Cable TV	↑	↑	Content Subsidy ↓	Advertising Subsidy →
•Digital Broadcast TV	↑	↓	↓	Advertising Subsidy ↓

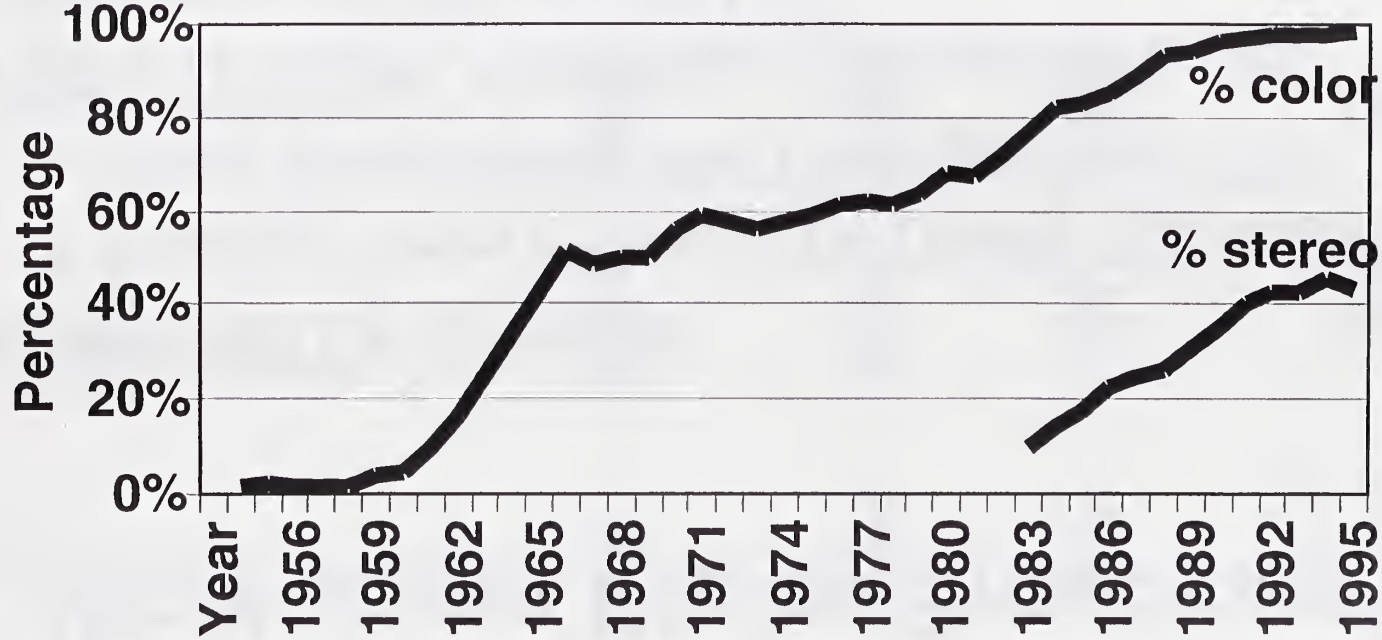
What about Digital Broadcast?

- Little HDTV Content
  - Existing 16mm Film and TV Library Captured at Lower Resolutions, don't look good on DTV
- 80% of North American Consumers get 'Broadcast' TV via Cable!
- Advertisers Pay for Eyes
  - More Digital Channels Gives Fewer eyes per Show
- Need Big $ - build out infrastructure & content

Digital Broadcast TV, Slow but Steady

- ✦ Digital TV (as Defined per FCC in the US, TV Networks worldwide)
  - Slow, Steady Migration, Not a Revolution!

Historical Penetration of North American TV Innovations



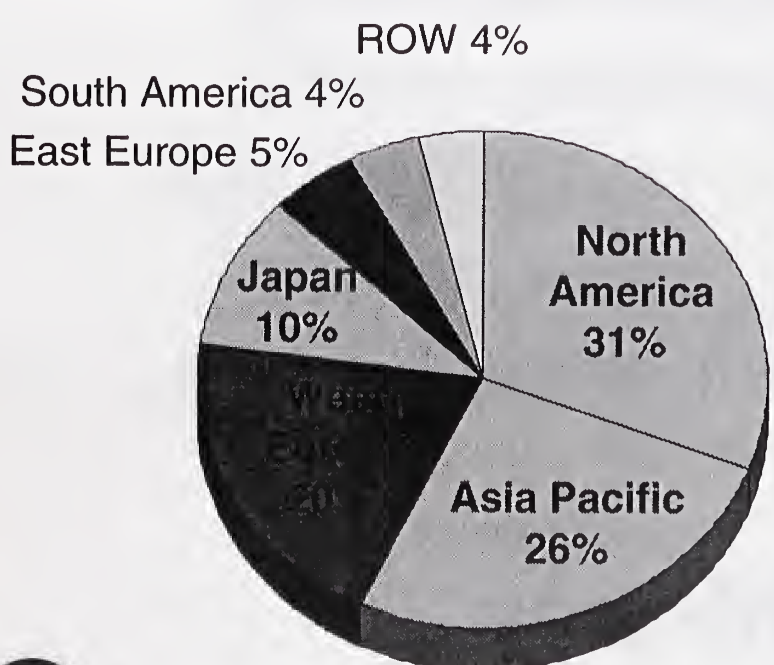
The Entertainment PC

- Open Architecture: A Blessing and a Curse
  - No Subsidies
- What is a PC?
  - When Intelligent Digital Appliances Compute
  - Java Brings General Purpose Apps to 'Single Function' Devices
- PC is Ease-of-Use Challenged
  - No Rebooting the TV!

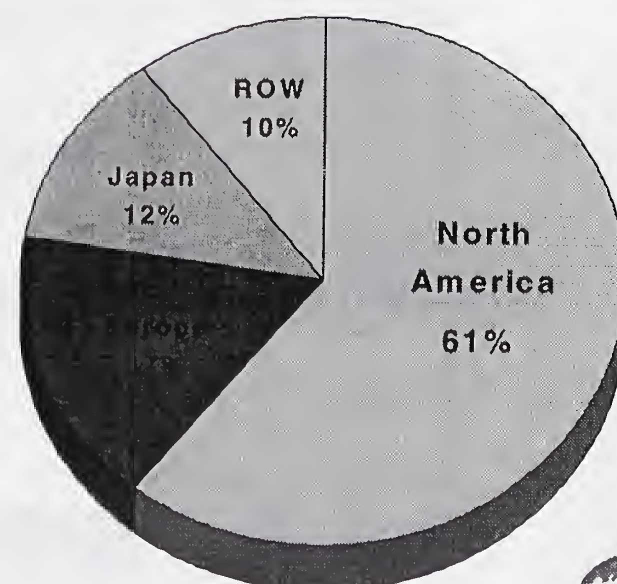
Worldwide Consumer Markets

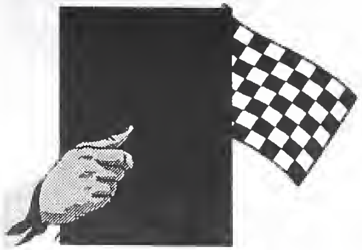
- Consumer PCs: North American Phenomenon
  - Even $1K is not Low Enough

1997 Consumer Electronics
406M Units



1997 Consumer PCs
19.5M Units





Box Winners

1) DBS
DVD
Video Game Console/DVD
\+ Internet Connectivity

2) Digital Cable TV

The Big Winner

- All the Digital 'Boxes' Need a **High-Resolution Display**
  - Multiscan 'TV' Monitors with RGB and IEEE 1394 Inputs
  - Monitor Matches Scan Rate, Resolution, Non-Interlaced/Interlaced Characteristics of the Content
    - DVD & Movies
    - Internet Appliances & Static Data
    - Old TV Programs
    - New TV *Content*

Talking the Same Language

The Computer World

- Non-Interlaced vs Interlaced
- Pixels per line First: 640x480
- Square Pixels
- Scan Rate: 50-100Hz
- 4:3 Aspect Ratio

The TV World

- Progressive vs Non-Progressive
- Horizontal Lines First: 720x1080
- Rectangular Pixels
- Frames Second: 30 NTSC /25 PAL
  Fields Per Second: 60 NTSC / 50 PAL
- 4:3 Aspect Ratio

The Film World

- Inherently Non-Interlaced
  or is it...Progressive
- 24 Frames per Second
- 16: 9 Aspect Ratio

Digital TV Requirements

- Per FCC: 18 Different Modes => 4 are Key

HDTV (High Definition TV)		SDTV (Standard Definition TV)	
Wide	Narrow	Wide	Narrow
16:9	4:3	16:9	4:3
1080x1920	720x1280	480x704	480x640
24, 30 or 60 Frames per second		24, 30 or 60 Frames per second	

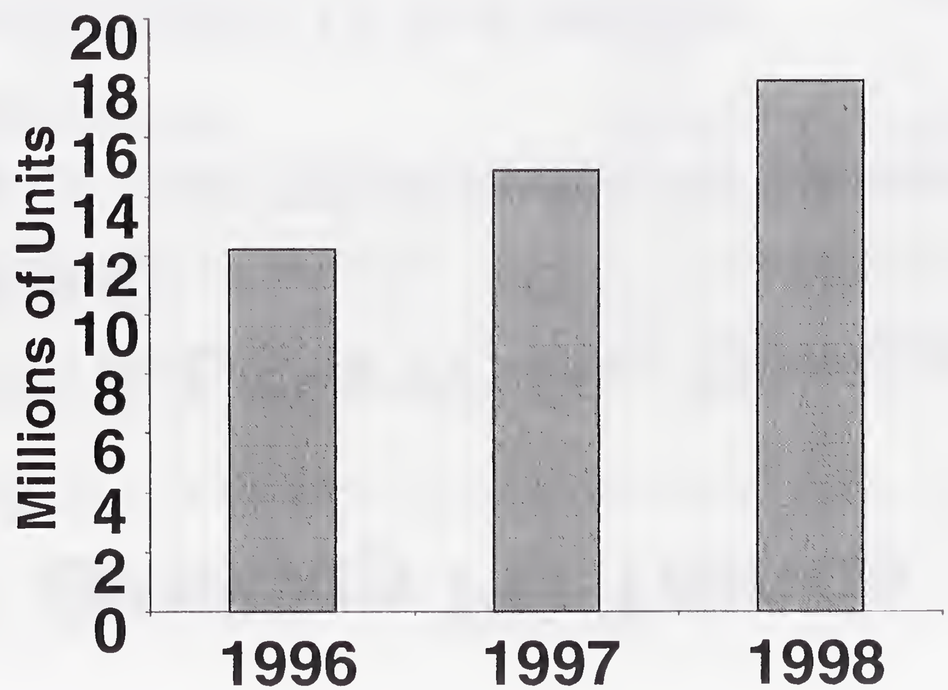
SDTV Essentially SVGA except for Rectangular vs Square Pixels

Desktop PC Trends

- Growth in Sub-$1K PC May Slow Screen Size Growth
  - Focus on Cost Drives to Smaller Monitor or no Monitor
  - TV-Out Enables TV as a Monitor
  - Will OEMs Bundle Non-Progressive Monitor for Lower Cost?
- PC Workstation Segment Expands Size of WW Workstation Market
  - 50+% Unit Growth vs. 1-2% Unix

Notebook PC Trends

- Growth Much Faster than Desktops :22% vs 15% in 1997
- Screen Sizes Getting Bigger
- Expanding into Lower Prices and Consumer Segments



Thank You!

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Panel Discussions

Bob Myers of Hewlett-Packard served as the moderator. Panel members:

Mitch Halpern, SRI Consulting
Mark Kirstein, In-Stat
John Frederick, Compaq
Hans van der Ven, Panasonic
Ian Miller, IBM

Bob Myers opened the discussion by stating that the objective was to find out where the group thinks things should be headed, particularly with respect to what VESA should do in the future, and what NIST can do in the future.

Q: How much longer will the CRT be with us, and will it go to a digital interface?
A: The CRT has always been good for "another 5-10 years". It's hard to get other displays within 1.5 times the cost. Plasma panels for TV in the home will come, but the CRT has a terrific cost advantage. The CRT needs the digital interface. A coming issue is DTV type, or 1394 type transmission throughout the house.
A: Agree - don't expect CRTs to go away any time soon.

Q: Which digital interface to run through the home?
A: 1394 is starting to show up in boxes in the home.

Q: Is there a "window of opportunity" for competitors to the LCD?
A: LCDs aren't going to be eliminated, but some applications are better served by alternative architectures, which may succeed if they hit the window of opportunity before LCDs become entrenched in those applications.

Q: What role can the government play in standards and technical development?
A: The government has played a major role in HDTV, DTV. There needs to be a balance between dictating and complete freedom. One issue is whether real HDTV will be broadcast, or whether the channels will be used for a lot of low-resolution signals. NIST has done a good job of bringing together interface, and measurements on flat panels.

A: Interoperability is a big issue. The government can focus on alternative technologies with reasonable market niches, possibly projection, FED, plasma, organic EL.
A: We are approaching having three incompatible HDTV standards in the world - it would provide a most useful benefit for the governments to get together, and agree on some level of commonality.
A: Agree - closer government involvement in HDTV standards would be much appreciated.

Q: What about 3D goggles?
A: They are expensive at the moment, people are looking at them for arcade games. The possible risk of visual problems due to discrepancies between accommodation and vergence needs to be addressed.

Q: Will CRT manufacturers go to the VESA P&D interface, or will they fall back to the VESA EVC interface?
A: Support of the digital video interface will be a key selling factor.
A: Agree - the fact that there will be a mix of displays is a very good argument for P&D. Within three years, as many as 15% of PC monitors will be LCDs.
A: Small screen CRTs with traditional VGA interface will last for a while, but as the market standardizes there will be an increasing switch over to EVC and P&D - they will tolerate a much higher bandwidth before EMI problems appear.
A: An advantage of P&D for an LCD monitor is that it makes it very easy to attach the LCD to the computer.

Q: Current LCD panels have a limited color capability. When will we see good LCD colors?
A: The tradeoff for color is power for the backlight - more saturated colors need more power for the backlight to produce a given level of luminance. Most LCDs have been optimized for portable applications, where power is at a premium. Within the last eight months there has been recognition that monitor LCDs with better color can represent a significant market. Within the next eight or nine months, expect flat panel displays that seriously rival the color of CRTs.

Q: It has been suggested that the government should be more aggressive in setting standards - the issue is <u>when</u> should a standard be set? You don't want to set it too early.

A: The government should be buying more market research.
A: In Europe, the government went along the analog HDTV path for a long time before abandoning it.
A: Setting a standard before the technology is practical is a mistake - it should be sometime nearer when the technology is ready for commercialization.

Q: What will be the dominant display technology for the automotive market?
A: It's a matter of timing. FED and organic EL have potential, but LCD may adapt itself to this market.
A: See a paper by Ford from the SID conference last year - it projects the roles of TFT LCD and FED.

Q: Are there any other niche markets not well served by current technologies?
A: Gas plasma, small LCD, micromirror, micromachined diffraction gratings. Micro- or mini-displays may be a market for other technologies.

Proposals for Future Development

[In this section, attendees voiced their comments, which were discussed and recorded.]

- Don't assume you know what the user is going to buy.
- There is a need for standards on security issues.
- There is a role for VESA and other standards bodies as an enabler.
- Is the rate of VESA standardization too slow, too fast, or just right? Are standards getting out in a timely manner?
- The lunchtime tour of NIST included speculation on different partitioning between the host and the display - what will the software issues be, and are standards needed for a smart display?
- In addition to new technology, VESA can document things that have already been done - specification of VGA was a good example.
- Perhaps there could be standards for embedded systems and niche applications.
- PICMG (PCI Industrial Computer Manufacturers Group) is working on embedded computing in general (PCI bus), not specifically directed toward displays.
- Perhaps could work with PICMG on embedded display standards.
- Standards on color definition?
- Standards on "goodness"? (Should there be a standard, or is that what differentiates products?)
- More mechanical standards? (Needed for true interoperability.) (Example: mounting standards.)
- Measurement standards for projection, head mounted, head up, stereoscopic, possibly CRT displays.
- Fast track standards, submitted through ISO.
- Need improved marketing of standards.
- Method for certifying compliance to VESA standards?
- Put tolerances in specifications.
- Request NIST involvement in compliance certification?
- Look into VESA stamp of approval.

Closing Remarks

Bob Myers of Hewlett-Packard gave the closing remarks, including the following:

- One thing about predicting the future of technology is that you can be sure you're wrong.

- Ideally, a standard should be completely transparent to the user - no wading through the user's manual. We're not there yet.

- The PC has become ubiquitous, but it is not yet an appliance. The difference: you don't teach classes in how to run a washing machine.

- The CRT is not the only game in town. LCDs and other technologies are coming - we have to make sure they are convenient to use as CRTs, by creating standards that makes this possible. The P&D standard is a good example - the PC Theatre Committee is going to try to meet this need as well.

- The display isn't just a box any more - what if it's a projector, or glasses, or something that acts a lot more like a newspaper or a book than a television set?

- We do need standards - they make flexibility of use possible.

- VESA will continue to have a very vital role in the industry. We invite you all to participate.