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Project Portfolio FY 1997

Edited by

Stephen Knight
and Alice Settle-Raskin
Office of Microelectronics Programs

U.S. DEPARTMENT OF COMMERCE

Technology Administration

National Institute of Standards and Technology

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U.S. DEPARTMENT OF COMMERCE
William M. Daley, Secretary

Technology Administration
Mary L. Good, Under Secretary for Technology

National Institute of Standards and Technology
Robert E. Hebner, Acting Director

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Foreword

The National Semiconductor Metrology Program (NSMP) is a NIST-wide effort designed to meet the highest priority measurement needs of the semiconductor industry as expressed by the *National Technology Roadmap for Semiconductors* and other authoritative industry sources. The NSMP was established in 1994 with a strong focus on mainstream silicon CMOS technology and an ultimate funding goal of $25 million annually. Current annual funding of approximately $11 million supports the 24 internal projects which are summarized in this Project Portfolio booklet.

The NSMP is operated by NIST's Office of Microelectronics Programs, which also manages NIST's relationships with the Semiconductor Industry Association (SIA), SEMATECH, and the Semiconductor Research Corporation (SRC). These include NIST's memberships on the SIA committees that develop the *Roadmap* and numerous SRC technical management committees. In addition, NIST is active in the semiconductor standards development activities of Ameican Society for Testing and Materials (ASTM), Deutsches Institut für Normung (DIN), Electronic Industries Association (EIA), International Organization for Standardization (ISO), and Semiconductor Equipment and Materials International (SEMI).

For further information about our program or how we can serve you, please contact us as follows:

Office of Microelectronics Programs
National Institute of Standards and Technology
Building 225, Room A323
Gaithersburg, MD 20899-0001
phone: (301) 975-4400
fax: (301) 948-0978
e-mail: nsmp@nist.gov
http://www.eeel.nist.gov/omp

Please note:

Certain commercial equipment and/or software is identified in this report to adequately describe the experimental procedure. Such identification does not imply recommendation or endorsement by the National Institute of Standards and Technology, nor does it imply that the equipment and/or software identified is necessarily the best available for the purposes.

References made to the National Technology Roadmap for Semiconductors (NTRS) apply to the most recent edition dated 1994. This document is available from the Semiconductor Industry Association (SIA), 181 Metro Drive, Suite 450, San Jose, CA 95110, phone: (408) 436-6600, fax: (408) 436-6646.

Table of Contents

Dimensional Metrology at the Nanometer Level

The scanning electron microscope (SEM) is the instrument of choice for IC manufacturing in-line process inspection and metrology. Scanning probe instruments (SPM) of various kinds have recently emerged to complement and extend the capabilities of the SEM. The atomic force microscope (AFM) is the most significant of these instruments for IC applications since it is capable of nanometer resolution on virtually any material. NIST has a three element program to expedite their application in the industry.

First is a calibrated metrology AFM (C-AFM) with three axis interferometric determination of tip position. This research instrument designed for development of AFM standards is capable of nanometer-scale measurements traceable to the wavelength of light in all three axes. Pitches ranging up to 20 μm can be measured with uncertainties of ~3 nm at sub-micrometer scale and ~0.1% at the largest scales, and heights ranging up to 1 μm can be measured with uncertainties of ~2%. The widths of sub-micrometer near-vertical features can be measured to ~30 nm. A new z-stage will be installed with lower tilt through the range of travel and additional evaluation of the tilting motion of the x-y stage is underway, which should allow us to accomplish our goal of calibrating sub-micrometer pitch artifacts with an uncertainty of less than 3 nm. A significant component of the C-AFM effort involves step-height metrology at the sub-nanometer level, being conducted in collaboration with researchers at the University of Maryland. Single atomic steps fabricated on single crystal silicon have been measured. The difference between the measured height of the steps of 0.270 nm ± 0.006 nm (where the uncertainty represents the same-step repeatability only) and the expected value from the bulk Si lattice of 0.314 nm is being investigated.

The second NIST program is to demonstrate capability for calibrated linewidth and sidewall angle measurements on a commercial non-contact SPM which uses a "boot" shaped tip. This work is managed through a Cooperative Research and Development Agreement (CRADA) with an IC manufacturer and uses an instrument installed in their facility. Evaluation of both commercially available and prototype characterization and linewidth artifacts are underway. In the first phase, comparison between these measurements and cross sectional TEM, good agreement was found with about 20 nm standard uncertainty in linewidth and 1° standard uncertainty in sidewall angle. In the second phase, six similar samples and a commercial "tip characterizer" were measured on this instrument. After an improved coarse sample positioning system is installed, the next phase will be to measure these samples on the C-AFM. Some of the samples will be cross sectioned and measured by TEM, and the remaining samples will be used in round robins with other users of AFMs using both conical and boot shaped tips.

Finally, NIST is developing another unique tool through the marriage of a compact SPM with a high-resolution field emission SEM. The proof-of-concept work is being facilitated through a CRADA with a commercial SPM instrument company. The combination of these two techniques is expected to yield an instrument with superior qualitative and quantitative capabilities. This is the first step in the development of a NIST "measurement engine" for advanced microelectronics. The two commercial instruments have been combined and tested. Improvements to the instruments for this unique application have been recommended to the manufacturers.

[Metrology is mentioned throughout the Lithography chapter of the 1994 National Technology Roadmap for Semiconductors (NTRS). Requirements are defined on page 85, Tables 17, 18. Potential solutions are on pages 89, 90, Tables 15, 16. Metrology is cited as a high-priority need on page 91.]

Contacts: Dr. Michael T. Postek, phone: (301) 975-2299, e-mail: michael.postek@nist.gov
Dr. Theodore V. Vorburger, phone: (301) 975-3493, e-mail: theodore.vorburger@nist.gov

Plasma and CVD Process Measurements

Improved characterization and control of etching and deposition plasmas are required for the next generation of semiconductor fab processes. NIST is addressing the metrology-related aspects of this problem through development of diagnostic tools and techniques on a simple yet highly-relevant reference platform. These tools probe the microscopic characteristics of the discharge, such as species densities, electron and ion energies, and optical emission characteristics. While these parameters are the most appropriate to describe plasma conditions, macroscopic parameters (power, pressure, gas flow) are used as control parameters today because the complex relationships among the microscopic variables are uncharacterized. A major task is the development of methods to translate microscopic plasma parameters into macroscopic control parameters.

Much of this work uses a universal plasma reactor called the GEC rf Reference Cell (GEC from the Gaseous Electronics Conference where the idea was conceived). More than 25 such cells are currently in use as a standard, reproducible platform for accurate intercomparisons of experimental data and results from plasma models. The GEC cells at NIST are equipped with a wide range of diagnostics including RF current and waveform analysis, Langmuir probes, optical emission, mass spectrometry with ion energy analysis, laser-induced fluorescence (LIF), and spectroscopic ellipsometry.

To date, these diagnostics have been applied to plasmas of Ar, He, O_2, H_2, N_2, SF_6, CF_4, CHF_3, Cl_2 and various mixtures of these gases. Results have identified diagnostics applicable to industrial reactors and the limits of those techniques, as well as the generation of basic plasma data suitable for the validation of various discharge models. Examples of specific results include:

1. A complete electrical characterization of the GEC cell resulting in improved plasma reproducibility. This knowledge has already been successfully applied to industrial reactors, and has recently been extended to processing gases, such as SF_6 and NF_3.
2. Development of a uniformity and reproducibility monitor for industrial reactors utilizing optical emission measurements.
3. Determination of neutral and ionic species in SF_6-containing plasmas, including measurement of the degree of gas dissociation for different plasma conditions in both capacitively coupled and inductively coupled plasmas.
4. Measurement of metastable and radical densities in CF_4-containing discharges for validation of plasma models.
5. Development of a database of fundamental electron-interaction data for plasma processing gases.
6. Development of measurement techniques for frequency-compensated electric probes applied to both capacitively-coupled and inductively coupled plasmas.

Several related projects supply basic support for modeling electric discharges used in semiconductor fabrication. These include modeling of particle formation in plasma-enhanced and thermal CVD reactors, measurement and analysis of fundamental reference data for industrially-relevant gases, and dissemination of experimental results to more than 20 different laboratories using GEC cells. Recently a WWW page was activated at NIST (http://physics.nist.gov/rfcell) that contains a bibliography of over 100 papers directly related to research performed on the GEC cell, along with other critical information about the reference cell.

Future plans include: (1) Development of a new reference reactor more closely resembling industrial designs; (2) Continued extension of all diagnostic techniques for application to inductively-coupled discharges; (3) Continued measurement, assessment, and distribution (via Internet) of fundamental data for plasma processing gases (C_2F_6, C_3F_8, and Cl_2) necessary to model commercial reactors and processes; (4) Investigatation of radical formation mechanisms in CH_xF_y plasmas using 2-D LIF; and (5) Measurement of plasma temperatures using absorption spectroscopy.

[The degree of empiricism embodied in the plasma tools of today is so well-known that it almost escapes mention in the NTRS. Needs for modeling (for process control) are indicated in Figure 31, page 129. Modeling and simulation of etch and deposition processes are essential for interconnect - see page 105 and Table 25. PECVD is one of the upper dielectric layer deposition tools mentioned in Figure 23 as a potential solution for interconnect.]

Contact: Dr. James K. Olthoff, phone: (301) 975-2431, e-mail: james.olthoff@nist.gov

Optical CD and Overlay Metrology

Tighter tolerances on CD measurements in wafer production place increasing demands on photomask linewidth accuracy and on overlay tolerances. NIST has a comprehensive program to both support and advance the optical techniques needed to make these measurements.

NIST has supplied a substantial number of photomask linewidth standards worldwide over the past decade. Chrome-on-quartz photomasks with linewidth and pitch artifacts in the range of 0.5μm to 30 μm are currently certified on a green light optical calibration system. Linewidth uncertainties have been reduced to 40 nm. These standards are being compared with linewidth measurements in other national standards laboratories, with excellent results to date [1].

An ultraviolet transmission microscope with quartz optics has been constructed that will replace the existing green light system mentioned above. This new instrument uses a unique geometry (a Stewart platform) as the main rigid structure and shows considerable improvement in vibration characteristics over a conventional microscope. It is also able to accept larger sample sizes. Reduced transmission of UV through the chrome and reduced instrument vibration will offer substantially improved linewidth uncertainties.

The overlay metrology program is investigating and designing a new set of overlay standards. These standards will consist of a set of artifacts which will allow users to align their particular overlay instrument properly and thereby eliminate or minimize tool-induced-shift. Currently under development is the stepped microcone alignment artifact [2]. Following the development of alignment artifacts and two-dimensional scale calibration standards is a research effort into material and geometry issues to determine the best candidate for a calibrated conventional box-in-box overlay pattern.

To meet the future challenges in overlay metrology, a new state-of-the-art reflection mode confocal microscope has been constructed at NIST. This instrument also utilizes a Stewart platform. Three-axis interferometry monitors sample position and a collimated laser beam coupled with a quadrant detector monitors stage tilt. The optical resolution is nominally 0.25 μm. A CCD camera and image acquisition electronics enable general use of the instrument in reflection mode on semiconductor (and other non-transparent) samples.

NIST is also developing a magnification standard for optical microscopes (SRM 2800) with certified pitch patterns from 1 cm to 1 μm to be produced on standard size slides. In addition, recent publications from NIST have outlined a new technique for measurement of photomask linewidths called Emulated Stepper Aerial Image Measurement. The ultraviolet microscope is being enhanced with the capabilities necessary to assess and verify this promising new concept.

[NTRS references are identical to those given for the Dimension Metrology work on page 1.]

Contacts: Mr. James Potzick, phone: (301) 975-3481, e-mail: james.potzick@nist.gov
Dr. Richard Silver, phone: (301) 975-5609, e-mail:richard.silver@nist.gov

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2. R. M. Silver, J. Potzick, F. Scire, C. Evans, M. McGlaughlin, E. Kornegay, and R. Larrabee, "A Method to Characterize Overlay Tool Misalignments and Distortions," Proc. SPIE Symposium on Microlithography, Santa Clara Calif., (1997).

Fundamental Process Control Metrology for Gases

Gas pressure, composition, and flow are fundamental operating variables in many semiconductor fab processes. NIST efforts in this important area have a dual focus. First, to ensure that the technical underpinnings of the measurements (including standards and calibration procedures) are available and widely disseminated. Second, NIST is examining the performance characteristics of process monitoring and control equipment to permit their optimum use by the industry.

Real-time monitoring of contaminants and gas composition in a process chamber also requires reliable process monitoring equipment. Preliminary NIST studies of commercial residual gas analyzers (RGAs) found undesirable performance characteristics in several instruments. Results from recent experimental studies on commercial RGAs indicate that most instruments can be optimized to minimize nonlinearities with pressure and "total pressure effects" upon the measured partial pressures of contaminant gases. The experimental data are in qualitative agreement with a theoretical model which ascribes high pressure non-linearities to electron and ion space charge effects in the ionizer, focusing electrode area, and in the mass filter. The experimental data and model indicate that non-linearities can be minimized through the appropriate selection of ionizer potential settings. Testing of this optimization technique with RGAs on a semiconductor tool is planned for the next year.

Responding to the SEMI/SEMATECH Thermal Mass Flow Meter Working Group, NIST has extended the range and improved the uncertainty of gas flow standards. The initial effort has resulted in a new standard for flows of inert gases between $7x10^{-8}$ moles/second and $7x10^{-4}$ moles/second with corresponding uncertainties from 0.1% to 0.05%, representing two standard deviations. A second standard under construction will extend the range to $7x10^{-3}$ moles/second and be compatible with some reactive gases. NIST designed ultra-stable laminar flowmeter transfer standards, covering the range $7x10^{-8}$ moles/second to $7x10^{-4}$ moles/second, have demonstrated a repeatability of 0.1% or better. These flowmeters have been used to perform on-site gas flow proficiency tests over the range of $7x10^{-7}$ moles/second to $7x10^{-4}$ moles/second at nine mass flow controller manufacturer calibration facilities during the past year.

NIST flow standards are being used in performance studies [1] of the commercial thermal-mass flow controllers commonly used for flow control in semiconductor process equipment and in the further development of stable laminar flowmeters and evaluation of alternate flowmetering technology.

[Residual gas analysis is mentioned in the NTRS on page 125. Fluid purity and residual matter in vacuo are discussed on page 127 and in Table 34. Key impurity levels in gases range down to a volume fraction of 10^{-11} (10 ppt) by the year 2007. Figure 30 outlines potential solutions.]

Contacts: Stuart A. Tison, phone: (301) 975-2857, e-mail: stuart.tison@nist.gov
Charles R. Tilford, phone: (301) 975-4828, e-mail: charles.tilford@nist.gov

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Measurements for Front-End Processes

Improved Measurements and Standards for Thin Dielectric Films: A collaborative series of single-wavelength ellipsometry measurements has been completed in a sample exchange experiment between NIST and a supplier of NIST-traceable SiO_2 film standards. The test sequence was designed to supplement NIST-generated SRMs in a more expedient way for establishing NIST-traceability for SiO_2 films at 5 and 7.5 nm. Statistical analysis of the experiment is being done for the ellipsometric parameters delta and psi and for layer thickness with single- and two-layer models, with results available in May 1997. Preliminary results indicate this approach is a viable means for determining an uncertainty of single-wavelength measurement traceability to NIST. In a related activity, a workshop to be sponsored by NIST on October 30-31, 1997 will focus on control, calibration and standards issues for optical measurements of thin dielectric films and is intended to lead to a consensus approach for meeting industry calibration and traceability needs for those measurements.

In order to improve the utility of in-situ optical monitoring of silicon thin-film fabrication processes, NIST is embarking on a program of developing accurate optical-constant data for silicon films at processing temperatures to 1000 °C. A custom-built UHV chamber with spectroscopic ellipsometer, RGA, and other instruments has been installed at NIST and is undergoing performance evaluation tests for all components. Acquisition and evaluation of data for silicon substrates, SiO_2, and other films, will begin by mid 1997.

Knowledge and control of the structure of the interface between thin gate dielectric films of SiO_2 and the silicon substrate are important both for device performance and reliability, and for the accurate measurement and fabrication of the layer itself. Previously, an electrical test method, based on a quantum mechanical interference effect, had been shown capable of measuring the roughness of such buried interfaces with the use of special Hall bar test structures. We have now demonstrated that interface roughness can be determined at the 0.1 nm level using this method, but requiring only two-terminal FET structures of a type commonly available on test chips for a production process. This measurement procedure is the only one known that is able to resolve in-situ interface roughness of fully fabricated devices with no removal of layers or sectioning of devices required.

2-D Dopant Profiling: The detailed 2-D and 3-D dopant profiles in silicon transistors are responsible for much of the performance and hot-carrier reliability of modern devices. NIST has constructed both a scanning capacitance microscope (SCM) and the required software analysis tools to measure 2-D dopant profiles in silicon. Precise and accurate measurement of 2-D dopant profiles in silicon could be used to calibrate technology computer-aided design (TCAD) simulations of the dopant profile produced by specified fabrication processes. Calibration of TCAD simulators could improve their predictive capability and, therefore, reduce the required number of process development cycles for next generation integrated circuits. The SCM is based on the more familiar atomic force microscope (AFM). The SCM acquires an image of the differential capacitance between a conducting probe and a wafer as a function of x-y position, along with a simultaneous image of topography. Through reference to a database of rigorous 3-D numerical solutions of Poisson's equation for the boundary conditions imposed by the SCM, NIST has extracted 2-D dopant profiles from SCM images of silicon test structures with better than 30 nm spatial resolution.

The NIST SCM models have been integrated into our *FASTC2D* SCM image-to-dopant profile interpretation software. *FASTC2D* uses a database of calculated SCM capacitance-voltage (C-V) curves to convert SCM signals rapidly to an equivalent dopant concentration. A personal computer-based version of *FASTC2D* with an intuitive graphical interface and performing at a level to allow rapid interactive extraction of dopant profiles is in preparation. The NIST SCM technology will be transferred to our industrial partners through distribution of our interpretation software and through cooperative research. Current research seeks to extend and validate the SCM technique. The model is currently being extended to include the effect of the dopant gradient in a computationally efficient way. An improved understanding of the technique in the vicinity of p-n junctions is being developed to allow accurate quantification of dopant profiles measured on real transistors. The first level of validation compares modeled SCM C-V curves to measured C-V curves. Second-level validation compares SCM-determined dopant profiles from test structures and state-of-the-art devices to profiles determined by other physical measurements of dopant profile (such as secondary ion mass spectroscopy, SIMS) and TCAD simulations.

[Thin film properties and doping distributions are discussed throughout the Materials and Bulk Processes and Interconnect chapters of the NTRS (pages 94, 106, 110, 119, 122, and 128; Figures 17, 25 and 31; Tables 25, 30, 32, 33, and 35). In-situ metrology of process performance will require optical measurements in high temperature environments, but these properties are largely unknown.]

Contacts: Dr. James R. Ehrstein, phone: (301) 975-2060, e-mail: james.ehrstein@nist.gov
Mr. Joseph J. Kopanski, phone: (301) 975-2089, e-mail: joseph.kopanski@nist.gov

Moisture Concentration Measurements in Process Gases

Moisture is a pervasive contaminant in semiconductor process gases. Current water vapor concentration measurement standards are limited to levels above a volume fraction of 2×10^{-6} ($2\ ppm_v$) while fabrication processes for sub-micrometer devices require measurements of humidity levels in the volume fraction of 10^{-8} (ppb_v) range. Improved measurement standards are needed to provide a sound basis for evaluation of existing measurement technology and development of improved methods useful for both diagnostic and on-line measurement. Both absolute and working standards are needed to support reliable measurements at these low levels. Working standards take the form of precision humidity generators that saturate input gas streams with predictable moisture concentrations. Absolute moisture concentration measurements are made using gravimetric methods, i.e., a gravimetric hygrometer, that separates and quantifies both the moisture and carrier gas. NIST is developing both capabilities as well as advanced quantitative spectroscopic techniques.

NIST has recently fabricated a gravimetric hygrometer to be used as a primary standard. Its lowest operating point is anticipated to lie between a volume fraction of 10^{-5} ($10\ ppm_v$)and a volume fraction of 10^{-4} ($100\ ppm_v$). Assessments of the uncertainties in the dry-gas collection and water vapor mass measurement subsystems of this gravimetric hygrometer are in progress. For the dry-gas collection system, relative uncertainties of a 10^{-5} (1000 ppm) level have been achieved. Relative uncertainties of better than 200 ppm are expected for the water mass measurement. These gravimetric-based measurements will be used to validate moisture generator performance in the overlapping part of their operating ranges.

A new precision generator, the low-frost-point moisture generator (LFPG), having an operating range of approximately a volume fraction of 5×10^{-9} ($5\ ppb_v$) to a volume fraction of 4×10^{-9} ($4000\ ppm_v$) has been constructed and is being tested. Saturator temperature control and stability of ± 2mK has been demonstrated down to -100 ° C. This corresponds to a reproducibility on the order of 0.1% in absolute moisture concentration at levels down to 10×10^{-9} ($10\ ppb_v$). The LFPG will be NIST's low concentration working standard. Its output is directly related to thermodynamic principles. It is fabricated to conform with high-purity-gas handling technology common to IC manufacturing.

Since the gravimetric hygrometer cannot be used to validate the LFPG output over its entire operating range, complementary techniques suitable for making direct standards-grade measurements of the lowest moisture levels attainable are required. Near-IR linear absorption techniques utilizing Cavity Ring-Down Spectroscopy (CRDS) has been selected as providing the highest sensitivity and potential for requisite accuracy. NIST has demonstrated that CRDS can be used to measure concentration accurately for transitions of known line strength using a weak transition of O_2 as a surrogate. The fundamental line strengths of the rotational transitions of water will be determined independently at relatively high concentrations using the LFPG as a moisture source and the gravimetric hygrometer to measure water vapor mass concentration. Independent measurement of water vapor concentration produced by the LFPG will yield ice-vapor pressure and non-ideal behavior of water-air mixtures over the range -100 ° C to 0 ° C. Once determined, these fundamental physical constants (both the line strengths and thermodynamic properties of ice) will function as reference standards. This approach will provide the means to extend optical techniques over many orders of magnitude with the potential to make reliable measurements into the ppt region, and will improve the accuracy of LFPG (as well as chilled mirror hygrometers) which are currently limited by uncertainty in the vapor pressure of ice.

[The NTRS discusses moisture in gases on page 125, Figure 30 and Table 34. There is a clear call to relate purity of fluids to the performance of processes and devices thereby avoiding unnecessary materials costs (pages 127 and 131).]

Contact: Dr. Joseph T. Hodges, phone: (301) 975-2605, e-mail: joseph.hodges@nist.gov

Contamination-Free CVD and Plasma Processes

NIST is addressing the chemistry of, and particle formation in, thermal and plasma reactors and developing micro-contamination standards. Improving the current limited understanding of chemical mechanisms causing the generation and growth of particles in the gas phase is critical to minimizing spontaneous particle formation in process reactors. Efforts here will address the measurement and modeling of chemistry and particle growth phenomena. Particle size measurement techniques are being developed for accurately sizing calibration standards to support the National Technology Roadmap for Semiconductors by addressing particles as small as 60 nm by year 2001.

The FY96 accomplishments included:

1. Developing ab-initio derived thermochemistry for the silicon-phosphorus-hydrogen system.
2. Determining the temperature dependent elementary rate constant for the reaction of TEOS with oxygen atoms.
3. Developing a new approach for the destruction of chlorofluorocarbons (CFCs). Sodium vapor is mixed with vapor phase CFCs resulting in rapid mineralization into sodium halide salts and elemental carbon aerosols.
4. Continuing efforts to characterize fluorocarbon etching plasmas in the Gaseous Electronics Conference (GEC) Plasma Cell by 2-D laser induced fluorescence imaging. Prior results on metastable argon are being modeled.
5. Developing a numerical model for microcontamination in a rotating disk CVD reactor, with a focus on chemical kinetics and transport. A 60-step reaction mechanism which simulates both silane decomposition and particle nucleation has been incorporated into the reactor performance maps have been generated which indicate the temperature regimes where surface growth and contamination rates are each within acceptable levels. Lower reactor pressure and higher disk rotation rate have been found to be beneficial. We anticipate commissioning a reference rotating disk CVD reactor designed for optical characterization in FY97.
6. Developing a WWW accessible, interactive database for chemical kinetic mechanisms called Web CKMech. It can be found through the group home page at <http://fluid.nist.gov:80/836.03/>. The interactive database was developed to make our prior compilations and computations (many of them computed by ab-initio methods) of fluorocarbons thermochemistry and kinetics more accessible. Data on CKMech can be searched by chemical formula or compound class, and will provide thermo-chemical functions, NASA thermochemical polynomial fits, molecular geometry data, vibrational frequencies, and molecular transport properties.
7. Accurately characterizing calibration particles for surface scanning inspection systems. A joint SEMATECH, NIST, and VLSI Standards, Inc. project was initiated to accurately characterize 10 monosize polystyrene sphere suspensions covering the particle diameter range from 70 to 900 nm. Screening measurements were made on 22 samples targeted at five sizes, and five samples were selected based on narrowness of the size distribution and closeness to targeted sizes. Accurate particle sizing analysis has been completed on three sizes with nominal diameters of 92 nm, 127 nm, and 218 nm.

[Particle contamination is one important class of CFM topics in the NTRS. Metrology for 0.1 μm particles and smaller is essential for lithography at 0.25 μm and beyond (Table 17), interconnect (Tables 21 and 26; pages 104 and 105), materials and bulk processes (pages 10, 112, 115, 119, 122, 125 and 128; Figures 25, 27, 30 and 31; Tables 26, 27, 28, 29, 32, 34 and 35) and factory integration (page 156; Tables 47 and 48).]

Contacts: Dr. Michael R. Zachariah, (301) 975-2063, e-mail: michael.zachariah@nist.gov
Dr. George Mulholland, (301) 975-6695, e-mail: george.mulholland@nist.gov

Thin-Film Profile Measurement Methods and Reference Materials

NIST is pursuing a multifaceted analytical approach to 2-D and 3-D compositional profiling. Main objectives of this work are to: (1) define optimum protocols for ultra-high depth resolution and ultra-shallow profiling by Secondary Ion Mass Spectrometry (SIMS); (2) develop a quantitative 3-D image-depth-profiling method with submicrometer lateral resolution using SIMS; (3) study by depth-profiling various processing issues such as transient-enhanced diffusion of boron in silicon; and (4) develop depth-profiling reference materials to assist the semiconductor industry.

For ultra-high depth resolution profiling, we have been exploring the use of a rotating SIMS sample stage to minimize sputtering-induced roughness as a factor in depth resolution. A large improvement in the profiling of metal multilayers has been demonstrated. Image depth profiling by SIMS uses a microbeam ion source to acquire sequential frames and subsequently to reconstruct 3-D profiles using advanced image processing methods. Proper account is taken of measurement effects such as matrix-dependent sputtering rates and secondary ion yields. This approach has been used to detect misalignment of FIB implant patterns of B and As. We have applied high-depth-resolution SIMS profiling to study transient-enhanced diffusion (TED) in shallow B^+-implanted Si in collaboration with the University of Florida under a SEMATECH-supported project. For low-dose B implants in crystalline Si, significant TED in the tail of the implant was observed without the presence of {311} defects, previously thought to be necessary for TED. The peak of the implant does not diffuse under these conditions, presumably because of the formation of immobile B-Si clusters. Diffusion behavior was also studied in pre-amorphized Si, for which the entire boron profile readily diffused.

The NIST boron-implant-in-silicon Standard Reference Material SRM 2137 has been used in an ISO international round-robin study among 16 laboratories to determine the boron concentration in an unknown boron-doped epitaxial Si sample by SIMS. The relative standard deviation of the boron determinations in the unknown was 8% among the 16 labs, and only 4% among the 6 U.S. participants. The excellent interlaboratory comparability is directly attributable to the availability of a common certified reference material.

NIST also helped to coordinate a round-robin study among 12 U.S. SIMS labs to determine the retained dose of an arsenic-implanted Si sample. In contrast to the boron study, the determinations among labs showed a range of over 60%. These results provided a strong motivation for NIST to develop an arsenic-implant Standard Reference Material, which has also been designated a priority item by the SEMATECH Analytical Laboratory Managers Working Group. We have obtained very uniform As-implanted Si wafers, had them diced into 1 cm square pieces, and measured the As content in representative pieces by neutron activation analysis (NAA), along with two independent solution standards. The NAA results will be used to calculate a certified As dose with a 95% confidence interval of about ±2%. This material, designated SRM 2134, is expected to be available by the fall of 1997.

[Thin-film properties and doping distributions are discussed throughout the Materials and Bulk Processes and Interconnect chapters of the NTRS (pages 94, 106, 110, 119, 122, and 128; Figures 17, 25, and 31; Tables 25, 30, 32, 33, and 35. Reference materials are cited as a need on pages 105, 112, and 128; in Figure 31 and in Tables 27 and 35.]

Contact: Dr. David S. Simons, phone: (301) 975-3903, email: david.simons@nist.gov

Radiometric Metrology for Deep Ultraviolet Lithography

The National Technology Roadmap for Semiconductors identifies the path to shorter wavelength photolithography as part of fabrication technology evolution. Improved measurement of absolute dose and uniformity over the exposure field is necessary for DUV lithography. Also improved measurements of the index of refraction of quartz and CaF_2 are essential for the realization of the optical components for 193 nm lithographic steppers. NIST is addressing these issues through improvements to present sources and detectors in the DUV as well as development of new sources, detectors, and more accurate radiometric scales. NIST is also partnering with Lincoln Laboratories in the SEMATECH/DARPA-sponsored 193 nm lithography demonstration project to refine the refractive index values of lens materials.

An important part of the infrastructure necessary for future work is an ongoing upgrade to the existing Synchrotron UV Radiation Facility (SURF II) which acts as the primary standard for both sources and detectors in the DUV spectral region. This upgrade project (to SURF III) will provide for hardware enhancements to the synchrotron itself, new beamlines dedicated to optical metrology and radiometry, and an increase in electron energy to allow useful emission of radiation down to 2 nm wavelength. Improvement in the measurement methods for more accurate index of refraction measurements of optical materials for 193 nm is being addressed with our current reflective refractometer. For wavelengths of 193 nm and below, a newly designed interferometer will be implemented.

Detailed activities of the DUV metrology program are:

1. Collaborate with Lincoln Laboratories' 193 nm lithography efforts to characterize the properties of UV transmitting materials, e.g., measurements of the index of refraction of quartz and CaF_2 to 1 part in 10^6 (currently at 1 part in 10^5).

2. Develop and characterize new stable, narrow linewidth UV sources and measurement technologies for optical materials characterization, especially refractive index determination in the spectral region 193 nm and below. Develop and characterize a new broadband UV source standard based on a high-power microwave discharge with a 0.2% standard uncertainty goal. Also, develop new improved exposure monitors for intense broadband UV sources used in photoresist stabilization (with a U.S. commercial firm).

3. Develop new DUV wafer-plane dose monitors for measurements at 248 nm and 193 nm (with a U.S. stepper manufacturer).

4. Achieve 0.1% standard uncertainty of UV irradiance from 3 nm to 400 nm (includes SURF II to III upgrade).
   a) obtain absolute beam current measurements on SURF II using a cryogenic radiometer.
   b) develop two new radiometric beamlines on SURF III with instruments.
   c) make source radiance and irradiance comparisons directly with SURF III.

5. Establish traceability of primary standard detectors to SURF III with detector spectral responsivity standard uncertainty goals of 0.2% from 100 nm to 400 nm.

6. Apply polarimetry characterization of optical materials from 3 nm to 400 nm utilizing SURF III.

[Radiometric improvements are behind-the-scenes metrology issues not mentioned in the Lithography chapter of the NTRS. They are clearly necessary for 248 nm (and beyond) for all of the exposure technologies listed in the lower half of Table 16.]

Contact: Dr. James R. Roberts, phone: (301) 975-3225, e-mail: james.roberts@nist.gov

Electrical Test Structure Metrology

NIST develops electrical test structures to determine metrological, reliability, process, and tool parameters.

Linewidth: Control of critical dimension (CD) is essential in the manufacture of advanced integrated circuits having feature widths below 0.5 μm. Physical standards for CD-instrument calibration having such narrow features are currently unavailable. NIST is collaborating with Sandia National Laboratories and SEMATECH in the development of physical standards for CD-instrument calibration having reference-feature widths ranging from 0.1 μm to 1.0 μm. The goal is commercial availability of linewidth calibration standards having acceptable cost as a result of CD certification by electrical means. Accordingly, the reference features of the new standards are embodied in electrical linewidth test structures but can also be inspected by SEM, by AFM, or by optical transmission methods. Feature-surface planarity and sidewall orientation are assured by feature-geometry alignment with specific crystallographic planes. Prototype samples have been distributed to 21 companies drawn from both the semiconductor manufacturing and the metrology tool industries under the terms of a CRADA-based consortium. Participating companies have agreed to exchange CD-measurement results at a meeting to be held at SEMICON/West in July 1997. A second CRADA, with a leading mask supplier to the semiconductor industry and an electrical test-equipment manufacturer, seeks to assure the reconciliation of CD measurements made by inspection facilities maintained at different locations, for example, by the mask supplier and by the mask user.

Overlay: Accurate level-to-level overlay metrology is critical for maintaining control of lithography processes used for manufacturing advanced integrated circuits. NIST has joined forces with a leading metrology-tool supplier to the semiconductor industry to identify key relationships between measurements extracted from targets using conventional optical microscopy and overlay-limited circuit performance. A second collaboration has an official consortium format and involves four instrument suppliers. The technical program, led jointly by NIST and SEMATECH, has been investigating the application of non-optical sensors to shift management and also the application of such sensors to the challenge of imaging target features concealed by CMP-planarized opaque films, a process being increasingly used in modern integrated-circuit fabrication. In a separate ongoing SEMATECH-sponsored collaboration between NIST and Sandia National Laboratories, a new type of optical target to facilitate the calibration of optical instruments, such as those used in overlay metrology, is being implemented in monocrystalline silicon.

Oxide reliability: As gate dielectrics are getting thinner with the aggressive scaling of device geometries, the long-term reliability of these ultra-thin layers is becoming a primary concern. NIST is collaborating with six U.S. semiconductor manufacturers in a joint research effort to understand the physical mechanism of time-dependent dielectric breakdown (TDDB). Measurements of stress-induced oxide traps provided evidence that the physical mechanism of dielectric breakdown at electric fields used during normal circuit operation is different from that at electric fields used during acceleration stress tests. NIST has developed failure acceleration techniques using high temperature such that dielectric breakdown occurs at electric fields near to those used in normal circuit operating conditions. These results are being used to develop a physically correct model to describe TDDB for ultra-thin dielectrics. Other work includes investigating highly accelerated wafer-level tests commonly used to characterize oxides in industry and comparing their results with those obtained from long-term stress tests. NIST also is organizing the development of a joint standard between JEDEC (EIA) and ASTM that describes several voltage- and current-ramp test procedures for characterizing ultra-thin dielectrics in the 2.5 to 5 nm thickness range. New research topics included plasma-induced damage effects on gate oxide reliability and characterization of alternative dielectrics for deep sub-micrometer technologies.

Electromigration: NIST works with standards organizations to develop and evaluate standard test methods and test structures important for reliability evaluations of metal interconnects. Semiconductor manufacturers, Sandia, and universities have been involved in inter-laboratory experiments for measuring metal temperature coefficient of resistance (TCR), joule heating, electrical linewidth, and wafer temperature to establish precision statements and to improve measurement methods for corresponding JEDEC and ASTM standards. Special test structure and experimental test designs have been included in a SEMATECH reliability test-chip program. Significant revisions of two other ASTM standards (for standard test-structure design guidelines and for electromigration testing) have been published. A new JEDEC standard for calculating the model parameters of electromigration will be published. A JEDEC standard for bond-pad layout has been published and is intended to facilitate the conduct of future inter-laboratory experiments involving wafer-level measurements.

[Test structures are called for in general terms on page 94 of the NTRS. The need for standardized test structures is stated on page 104 as a priority need. Quality and reliability concerns related to metal films and dielectrics are discussed on pages 105 and 106 and listed in Table 19. A related discussion on CD and overlay is covered on page 106 and in Table 25.]

Contact: Loren W. Linholm, phone: (301) 975-2052, e-mail: loren.linholm@nist.gov

Metrology for Modeling and Simulation

The name of the project formerly known as Metrology for Devices and Packages has been changed to Metrology for Modeling and Simulation to reflect the emphasis on helping to develop and support the infrastructure for validating device, package, and process models and simulations. An example of this activity is the NIST/IEEE Model Validation Working Group, founded in 1994 and now having over 150 members from 100 different technical organizations. This group's activities are discussed on its Web page at *http://ray.eeel.nist.gov/modval.html*. In addition to the tasks discussed below, a new effort in ion implant model validation has been initiated and one in thermal process modeling is being planned.

Compact Package Thermal Models: The accurate and timely simulation of the thermal performance of systems has become more important as competitive pressures have forced reduced and decreasing development times. Consequently, there has been increased activity in the development and use of simulations accounting for all modes of heat transfer; conduction, convection, and radiation. Just as for the electrical aspects, all of the complexities and details of the thermal aspects of electronic systems cannot be efficiently included in a system level simulation. Thus, simplified or "compact" thermal models must be used for the components, such as microelectronic packages and circuit boards. Many different types of compact models have been developed. The objective of this task is to develop methodologies to validate the performance and accuracy of compact package thermal models for use in system level thermal simulations for all types of applications. The first application selected was for horizontally mounted packages in a natural convection environment. A test bed was selected based upon an EIA/JEDEC-recommended free, natural convection test enclosure. The enclosure was modeled and experimentally characterized. Simulations were performed for a detailed package model and several compact package models. It was found that, while system level considerations, especially circuit board conductivity and radiative heat transfer had to be well characterized, the enclosure could be used to validate compact model performance. The experiments included temperature measurements with thermocouples and thermal test chips and flow visualization by smoke injection. It has also been shown that models validated in the free convection enclosure can be used to simulate the thermal behavior of a 3 by 3 array of packages in a confined, narrow aspect enclosure, representative of a lap top computer, for instance. This is the first attempt by anyone to demonstrate a procedure using a realistic but simplified standard test bed to validate the performance of package thermal models for use in real systems applications. The next phase of this work will be to develop a validation procedure for a forced convection environment and then possibly for vertical mounted packages in natural convection.

Compact Device Electrical Models: Compact models have long been used in the simulation of the electrical behavior of systems. Only recently, though, has there been a significant effort in developing an infrastructure for validating the performance of these models. In addition to founding and supporting the NIST/IEEE Model Validation Working Group, NIST has extensive laboratory efforts in this area. A test bed has been developed for validating the electrical performance of compact Insulated Gate Bipolar Transistor (IGBT) models. The IGBT is the power semiconductor device of preference for many, if not most, power applications. This is the first example of a formalized validation procedure being developed for a compact device model.

[Metrology and modeling of packages are both discussed on page 132 of the NTRS. NIST has long been a strong contributor on these topics. The wide divergence between power levels for hand-held vs. high-performance applications (Table 37) underscores the need for improved package designs (discussion, page 136). These can only be obtained with the aid of improved 3D models and the necessary data on materials properties to support them.]

Contacts: David L. Blackburn, phone: (301) 975-2068, e-mail: david.blackburn@nist.gov
Allen R. Hefner, phone: (301) 975-2071, e-mail: allen.hefner@nist.gov

Wafer and Chuck Flatness/Thickness

Limited lithographic depth-of-focus budgets for finer features on larger silicon wafers pose new challenges for flatness metrology. Mechanical distortions of wafers induced by conventional vacuum chucks are part of a manufacturing problem that NIST is also addressing. Work on surface preparation of silicon and other electronic materials is yet another part of this program.

NIST has further developed flat calibration capabilities using a commercial Fizeau interferometer (Wyko Model 6000) to uncertainties approaching 2 nm over diameters up to 150 mm. The entire wafer is imaged at once, unlike techniques using scanned probes. That image provides a useful qualitative picture of the flatness, while the quantitative description is extracted from on-line analysis of the data.

This method is being extended to 300 mm wafers using another commercial interferometer (Phase Shift Technology's MiniFiz) by applying a technique well known to the optics industry (the Ritchey-Common test). The optical system is in place to allow measurement of as-chucked wafer flatness for 300 mm wafers and, by Second Quarter 1997, this system will offer traceable flat metrology for 300 mm wafers. The uncertainty will be further reduced with a next-generation interferometer currently under development.

In a parallel development, the NIST team has developed a new concept for measurement of thickness, free-standing bow, and thickness variations. Wafers will be measured at three positions in a transmission infrared interferometer. The wafer is flipped front to back between two of the observations allowing bow to be separated from average thickness and mapped independently. Demonstration of principle is completed and an instrument capable of routine measurements is expected to be completed by Third Quarter 1997.

NIST capability in flatness measurement will be used to evaluate issues associated with specific vacuum chuck systems as well as to explore new chucking concepts. One important short-term issue is the differing distortions caused by chucks on actual lithography equipment versus those on commercial instruments designed to measure wafer flatness. NIST is developing chucks made of hard, porous ceramics which can be made extremely flat and provide superior support of the wafer from a large number of distributed points.

A novel lap concept has been developed (patent applied for) and applied to both diamond lapping and chemo-mechanical polishing (CMP) processes. Rapid, low-damage lapping of crystalline substrates (silicon, sapphire) has been demonstrated; the potential to reduce wafer fabrication times through combinations of diamond lapping and current processes has been demonstrated and the technology is now available for commercialization. The new lap concept also has potential to enable rapid pad changing in CMP processes; tungsten, copper, and sheet oxide have been polished using the system.

[Wafer metrology is described on page 112 of the NTRS. Site flatness (in 2004) on 300 mm wafers is specified to be better than 80 nm over a large field on page 113; Table 26. Flatness figures for planarization are given in Table 22. Flatness metrology is a high-priority topic on page 115; Table 27. Vacuum-chuck flatness is not mentioned in the NTRS but is a serious concern as revealed by direct industry contact. Planarization processes (CMP) that implicitly need flatness measurements are in Figure 18 and discussed on page 99.]

Contact: Dr. Chris J. Evans, phone: (301) 975-3484, e-mail: christopher.evans@nist.gov

Optical Scattering for Wafer Surface Metrology

Optical scattering metrology tools are indispensable in modern fab lines for defect and particle sizing and counting. Numerous commercial instruments are laser-based scanning systems that collect scattered light and process the resulting data in different ways. Each of these instruments uses a different subset of the more fundamental bidirectional reflectance distribution function (BRDF). If one considers a small, collimated beam of light impinging on a wafer surface at some angle, the BRDF describes the angular-resolved scattering of light into the hemisphere above the wafer. Appropriate integration of the BRDF therefore defines the response of any instrument to a given set of scattering features. Bidirectional ellipsometry yields additional information on the nature of the scattering features in the near-surface volume of materials.

Extensive BRDF measurement capability exists at NIST with wide dynamic range, high angular accuracy, very low instrumentation scatter contributions, multiple incident wavelengths (visible and UV), and polarization control on both the incident and viewing light. The Goniometric Optical Scatter Instrument (GOSI) is capable of measuring the polarized BRDF for nearly any two incident/viewing directions and is useful as a tool for calibrating angle-resolving and angle-integrating optical scatter instrumentation and well as a tool for research.

A second instrument, the Scanning Optical Scatter Instrument (SOSI), is under development to complement the capabilities of GOSI. As an angle- and polarization-resolving prototype of a scanning surface inspection system, its multiple collection systems will enable high-speed determination of the polarized BRDF at each location on a wafer surface. Together with an understanding of the light scattering functions for different types of scattering sources, SOSI will have a substantially improved capability for detecting and identifying defects, particles, and microroughness on a wafer surface.

The ultimate objective of this program is to develop an understanding of optical scatter mechanisms so that algorithms may be developed that will accurately interpret scatter data. Such capability will then allow NIST to develop standard artifacts and methodologies to extract information about particles, microroughness, contamination, films, and subsurface defects. Near-term work is aimed at:

1. Developing methodologies for characterizing commercial scanning surface inspection systems. Recently, a methodology was developed that can be used to describe the response of an instrument to surface microroughness. Software is being developed for distribution which will allow instrument manufacturers to determine the response function for their instruments.

2. Exploring bidirectional ellipsometry as a tool for identifying defects on silicon wafers. The polarization of light reflects the path that light travels from the source to the detector and is very sensitive to the source of optical scatter. This technique enables discrimination between a variety of defect types on silicon wafers.

3. Measuring the BRDF from particles on bare silicon wafers. This research will enable algorithms to allow scanning surface inspection systems to determine particle size and composition.

[Optical scattering methods used for detecting particles, haze, and microroughness on wafers are not well-quantified today. Needs for measurements are outlined in the NTRS on pages 111, 112, 115, and 119 and also in Tables 26, 27, 28 and 29. The work discussed here complements the spatially integrated work of Joseph Fine with the SSM (see next page).]

Contacts: Clara Asmail, phone: (301) 975-2339, e-mail: clara.asmail@nist.gov
Dr. Thomas Germer, phone: (301) 975-2876, e-mail: thomas.germer@nist.gov

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See also: http://physics.nist.gov/Divisions/Div844/Gp6/facilities/osm.html

Non-Destructive Microroughness Characterization of Buried Silicon Interfaces

Fabrication of defect-free ultra-thin (UT) insulating layers (2 nm to 5 nm) on silicon requires the development of deposition techniques that do not alter the topography of the silicon substrate. The development of such techniques for making oxide and oxy-nitride UT layers would benefit greatly from having a direct non-contact, non-destructive method for monitoring the buried Si/insulator interface roughness, both during and after film growth.

The NIST-invented optical scatter instrument, the scanning scattering microscope (SSM), has been further developed so that interface microroughness of UT insulating layers on silicon can be measured directly -- without destroying the outer, thin insulating layer. This optical-scatter technique generates two-dimensional images of surface defects and microroughness presently with a lateral resolution of about 5 μm. The microroughness sensitivity of the SSM has been substantially improved and is realistically in the sub-angstrom region. Use of calibrated AFM techniques has allowed us to determine the contribution of the outer SiO_2/air interface to the total optical-scatter roughness, and by modeling the two-interface scattering problem, the roughness contribution of the buried Si/SiO_2 interface can be determined.

We have measured the buried interface roughness of UT SiO_2 layers on Si. By combining the use of our SSM with AFM measurements on both pre- and post-stripped SiO_2 layers, we have been able to demonstrate that virtually all of the scattered light intensity is produced at the buried interface. This strongly suggests that the SSM can be used directly (without stripping) to characterize buried-interface topography with very little correction required (probably less than 10%) to account for the roughness of the outer SiO_2 surface.

In the course of these SSM measurements, we have been able to evaluate the roughness sensitivity of our instrument. In its present configuration, we can determine differences in rms surface roughness of 0.02 nm (0.2 Å).

A comparison of this technique with the Bidirectional Reflectance Distribution Technique described on page 13, "Optical Scattering for Surface Metrology," suggests that the latter technique is promising and more easily integrated into IC manufacturing metrology equipment, and therefore the above project title has been terminated.

[Microroughness values of 0.1 nm (!!) on wafers are specified in Table 26 of the NTRS for 0.18 μm products. Control of microroughness is a high-priority item in Table 27 and also Table 29. Defect limits are described throughout the Materials and Bulk Processes chapter, but near-surface defects are not specifically mentioned. Defect detection limits (80 nm will be needed by 1998, decreasing to 20 nm by 2010) imply the use of techniques not presently available. Exploratory work is clearly necessary.]

Contact: Dr. David S. Simons, phone: (301) 975-3903, e-mail: david.simons@nist.gov

High-Accuracy Two-Dimensional Measurements

The ability to place features accurately in 2-D has multiple impacts in the electronics industry. Manufacture of reticles, large high-resolution displays, and circuit boards involve different aspects of the same metrology problem.

The situation regarding this critical capability is unusual in that state-of-the-art commercial measuring machines (such as the Nikon 5I or Leica LMS 2010) are so accurate that there is no available source of better 2-D measurements from which standards can be established. As such, users today are "traceable" only to their particular measuring machine. NIST clearly recognizes the industry-wide exposure inherent in this situation and is developing innovative practical approaches to establish convergence in the absence of a conventional standard.

The NIST linescale interferometer is known to provide the most accurate 1-D measurements available in the world. Preliminary work has been carried out on algorithms which will allow the use of this tool on the 2-D problem. Multiple passes of linear artifacts with different orientations on the customer's measurement machine will provide a reasonable accuracy check. We are also working with industry to design a suitable interlaboratory test (round-robin) to assess the current industry capabilities.

In the shorter term, NIST is working toward a 2-D (200 mm x 200 mm) measuring machine at its Gaithersburg, MD facility to test algorithm designs and sensor effects. A larger range machine (750 mm x 750 mm) has been brought on line to make measurements on large grid plates used in PC board and flat-panel display fabrication. The uncertainty ($k = 2$) of measurements on this instrument is 0.4 μm over the full range of the machine.

[Two-dimensional measurements are implicitly needed for controlling overlay capabilities of steppers and mask-making tools. Overlay is listed in table 19 of the NTRS as a show-stopper for 0.18 μm technology. While production of 0.18 μm products is not expected until 2001, NTRS also points out that technology must be available five years earlier to allow the normal process of development and prototyping. Table 18 therefore implies a short-term need for overlay metrology with uncertainty of 5 nm (3σ).]

Contact: Dr. Ted Doiron, phone: (301) 975-3472, e-mail: theodore.doiron@nist.gov

Improved High-Temperature Wire Thermocouple Thermometry

Use of thermocouple (TCs) with wires made of metal alloys is ubiquitous throughout the semiconductor industry. Two assumptions are often made, i.e., that the TCs are stable with time and also that the TC measures the difference in temperature between the measuring junction and the reference junction independent of the thermoelectric quality, i.e., the homogeneity, of the thermoelements in the regions of temperature gradients. Careful examination of commercial TCs shows that these assumptions are incorrect due to phase changes in the alloy materials and to inhomogeneities, compositional or physical, along the length of the wires. For example, in commercial TCs types S, R, and B, errors as large as 10 °C at 1350 °C are not uncommon.

NIST has developed improved TCs consisting of high-purity Pt and Pd wires to minimize these errors. Such TCs constructed using 0.5 mm diameter wire have errors less than 0.03 °C below 960 °C and less than 0.5 °C at 1500 °C. Studies at NIST to evaluate the effects of annealing, heat treatment and oxidation of the pure Pt/Pd TCs were completed this year. Also, in collaboration with the Istituto di Metrologia "G. Colonetti," the Italian national standards laboratory, NIST has produced a highly accurate Pt/Pd reference function covering the range 0 °C to 1500 °C to facilitate the use of this new TC in industrial and scientific applications. Evaluations of some NIST-prepared Pt/Pd TCs are planned for later this year in industrial applications directly related to semiconductor production; work with the industrial partner to facilitate this application will continue into the next fiscal year. In a related project (see page 20, "Temperature Measurements for Rapid Thermal Processing"), Pt/Pd TCs fabricated from various small sizes of wires are being evaluated and installed in silicon calibration wafers.

[Temperature control by various means is outlined in Figure 31 on page 129 of the NTRS. The temperature errors in RTP are known to be large. Need for improvement is described on page 122 and in Table 32 and is a high priority item in Table 33. This work provides the best available thermocouple for high-temperature measurements and forms the foundation for follow-on efforts aimed at improving the situation in the RTP environment.]

Contact: Dr. Billy W. Mangum, phone: (301) 975-4808, e-mail: billy.mangum@nist.gov

Micromechanical Measurements[†]

Thin Film Mechanical Properties: Knowledge of the mechanical material properties and behavior of thin films is fundamental to design, fabrication, and reliability of advanced integrated circuits and interconnect systems. These properties differ from those of bulk material of the same chemical composition due to differences in the deposition conditions. Conventional mechanical testing apparatus are not applicable to thin films, simply because of the size scale. A new method for measuring the mechanical properties of thin films using lithographically produced mechanical test chips in the form of *silicon-framed tensile specimens*. These are tested reproducibly in a closed loop piezo-actuated tensile tester well-suited for thin films because of its precise control and measurement of imposed displacements and loads.

Tests have been conducted on thin film Al, Cu, Ti-Al, and Si materials deposited in a variety of ways. Results indicate that the metallic thin films studied behave differently from bulk materials. Yield and ultimate strengths are higher in the films than in pure, annealed bulk polycrystalline material. Elongation to failure in the films is about 1%, whereas in bulk materials it ranges from 20% to 50 %.

Stress Voiding and Electromigration: Stress-induced voiding in thin films is an important failure mode related to the same microstructural features that control mechanical behavior. During cooling from processing temperatures severe triaxial tensile stresses develop in passivated narrow metallizations. These stresses result from a combination of differences in thermal expansion between the metallization and surrounding materials and the strong adhesion among these materials, and are the driving force for the formation and growth of voids.

Voids grow exclusively at certain grain boundaries within a conductor. Backscatter Kikuchi diffraction characterizations of the crystallographic orientation of individual grains demonstrate that grains immediately adjacent to voids and grain boundaries intersecting voids have crystallographic orientations that deviate further from a perfect [111] orientation than those grains and grain boundaries in regions that remained unvoided. Large grain boundary misorientation angles correlate to high diffusivities, leading to growth of stress-induced voids forming in grain boundaries that are efficient paths for in-plane atomic transport. Current work focuses on possible connections between stress voiding and electromigration.

High Resolution Experimental Mechanics: Electron-beam moiré (EBM) is being developed and used for high resolution mechanical studies of electronic packaging and interconnect structures. This technique provides two-dimensional measurements of local displacements and strains on cross-sections subjected to thermal or mechanical loading. The effort concentrates on material configurations of industrial significance by obtaining specimens from industrial collaborators who are conducting modeling efforts. The data offer experimental verification of finite element modeling and confirmation of failure modes, thus reducing the uncertainty and adding value to the modeling effort.

EBM provides quantitative displacement data at resolutions below the wavelength of light. We now produce orthogonal line gratings on the cross-sectioned surface of specimens. The grating pitch has been limited to 350 nm routinely, and 175 nm with suitable substrate materials. Formation of gratings with dots instead of lines will result in smaller pitches, down to 100 nm. This improvement in resolution has applicability to the fine features found in conductive adhesives and layered interconnect structures. The ability to measure two-dimensional displacements on the order of a few tens of nanometers permits study of the behavior of individual conducting particles in anisotropic conductive adhesives.

[The NTRS states "... Materials characterization and process model accuracy in both two and three dimensions must improve to predict adequately the performance and reliability of future device structures" and calls for standard tests and measurement procedures for thin film systems as well as "aggressive materials, process, and film characterizations." The Interconnect Working Group calls for "standard test structures and methods for characterizing electromigration, stress voiding, and interfacial-related failure mechanisms in interconnects."]

Contacts: David T. Read, (303) 497-3853, e-mail: read@boulder.nist.gov
Robert R. Keller, phone: (303) 497-7651, e-mail: keller@boulder.nist.gov
Elizabeth S. Drexler, phone: (303) 497-5350, e-mail: drexler@boulder.nist.gov

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[†]This project was partially funded through the NIST National Semiconductor Metrology Program. For information on these or other NIST projects in electronics packaging and interconnect materials, contact: Michael A. Schen, phone: (301) 975-6741, e-mail: michael.schen@nist.gov.

Solderability Measurements for Microelectronics[†]

The decrease in dimensions of electronic devices has resulted in a dramatic increase in interconnection densities and movement toward replacement of through-hole with surface-mount connections. These developments have introduced new stringent demands on solder and the soldering process. Good first-pass solderability is an increasingly important industrial goal, especially for surface-mount connections and ball grid arrays. To meet the need for improved solder joint reliability, NIST is developing measurements, test techniques, and scientific guidelines for both Pb-Sn and Pb-free solders that manufacturers can use to evaluate components for solderability before committing them to the production line and applying them in the evaluation of solder joint designs for their manufacturability and reliability. For this purpose, measurements and modeling of wetting balance solderability tests, area-of-spread solderability tests, wetting phenomena, and oxidation effects on solderability are underway.

Since industry finds that the presently used wetting-balance tests are not sufficiently reliable, improved tests are needed. Predictive models are being developed for the rate and extent of reactive wetting of solder during solderability tests. Complicating factors in these models are solute diffusion and the Marangoni flow from temperature gradients expected under these conditions. Systematic solderability measurement and modeling efforts at NIST are being pursued in collaboration with the Institute for Interconnecting and Packaging Electronic Circuits (IPC) Wetting Balance Task Group and are directed toward developing an improved solderability test to provide more reproducible measurements of initial solderability and of the loss that can occur during storage. A NIST-designed accelerated test using steam-aging techniques to allow more rapid testing is under consideration by the IPC in collaboration with the IPC Steam Aging Task Group.

Characterization of substrate oxidation and its effect on solder/substrate interactions is being pursued in order to identify conditions that undermine solderability. Collaboration with industry on reproducibility of solderability measurements is underway in a round-robin wetting-balance testing program. The objective of this project is to develop a reliable solderability test methodology and produce guidelines and standards that will make quantitative wetting balance and electrochemical solderability tests useful for prediction purposes, with emphasis on evaluating solderability of production line components.

[This topic is of continuing concern to device makers and their customers. These solderability issues are also driven by the smaller pitch and footprint of leads on surface mount devices and by concerns raised by the advent of lead-free solders which will inevitably involve changes in soldering techniques.]

Contact: John Manning, phone: (301) 975-6157, e-mail: manning@nist.gov

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[†] This project was partially funded through the NIST National Semicondutor Metrology Program. For information on these or other NIST projects in electronics packaging and module interconnection materials, contact: Michael A. Schen, (301) 975-6741, e-mail: michael.schen@nist.gov.

Hygrothermal Expansion of Polymer Thin Films[†]

Polymers are widely used in electronic packaging for applications such as interlayer dielectrics, underfill in ball grid arrays, die attach adhesives, heat sink adhesives, conductive adhesives, encapsulants, and substrates for high-density interconnects. In many of these applications, the polymer is in the form of a thin film adhered to materials of radically different physical properties. Knowing and predicting the dimensional stability of materials in semiconductor packaging and interconnects are important for enhancing the performance and reliability of complex materials assemblies. The physical properties of such films, especially in a constrained configuration, can be significantly different from those of the same material in bulk form or in free-standing films. Traditional expansivity measurements based upon mechanical displacement are not sensitive to the small dimensional changes exhibited by the thin films encountered in electronic packaging and interconnects.

This effort has the primary objective of providing industry with robust measurement tools and data for characterizing the dimensional stability of polymers. In particular, the project is focused on the impact of changes in temperature and humidity on the out-of-plane dimensions of thin films. NIST has designed, built, and demonstrated a capacitor cell with outstanding sensitivity for measuring the out-of-plane expansion of polymer films. An environmental chamber to control temperature and humidity has been interfaced for computer control and sensors enable capacitance readings to be converted to values in vacuum. The project has three sets of activities: (1) determining the accuracy and precision of the technique applied to a variety of polymer measurements; (2) working with standards- setting bodies to explore the desirability of introducing the technique as a standard method for measuring thermal and hygroscopic expansion; and, (3) providing industry with materials property data on selected packaging materials.

In the first set of activities related to precision and accuracy, we are conducting extensive studies to determine the measurement uncertainties and limitations of the current capacitance-cell design and measurement method. This work is being conducted with the assistance of the Statistical Engineering Division. In the second set of activities, we plan to work with the test methods committees of IPC, SEMI, and ASTM to have the capacitance technique considered as an additional standard test method for the measurement of thermal expansion for cases in which the existing standards are inappropriate. Thirdly, in the course of the work, data on materials of importance to the electronics industry such as molding compound, underfill, encapsulants, and interlayer dielectrics are being generated which will be incorporated in the SRC-sponsored database maintained by CINDAS at Purdue. We expect to provide measurement expertise to consortia such as the NCMS-sponsored consortium on PWBs and the ITRI-sponsored October Project which is directed toward making high density interconnects compatible with chip scale packaging and direct chip attach.

[The NTRS pinpoints high-density substrates as an important enabling technology needed to capitalize on developments in chip-scale packaging and high-density interconnection. In addition, polymer dielectrics and standards for materials and processing are mentioned. This project is working to introduce the measurement standards needed to describe thin films used in these applications.]

Contact: G. Thomas Davis, phone: (301) 975-6725, e-mail: george.davis@nist.gov

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[†] This project was partially funded through the NIST National Semiconductor Metrology Program. For information on these or other projects in electronics packaging and module interconnection materials, contact Michael A. Schen, (301) 975-6741, e-mail: michael.schen@nist.gov

Improved Radiation Thermometry for Rapid Thermal Processing

Rapid Thermal Processing (RTP) is a key technology for manufacturing Ultra Large Scale Integrated Circuits. RTP offers faster processing with lower thermal budgets, and lower risks per batch; it is adaptable to large wafer size, and is compatible with multi chamber (cluster tool) vacuum or low pressure processing. However, problems with temperature measurement, and therefore temperature control and dynamic temperature uniformity, have impeded the widespread use of RTP in integrated circuit manufacturing. The primary causes of these problems are that the emissivity of the partially processed wafers is a widely varying parameter, depending on the detailed prior processing history; and that the radiation environment within the processing chamber includes reflections from the walls and wafer surfaces as well as partial transmissions through the wafer, of radiant power from the heating lamps. An additional difficulty is that the accuracy of temperature measurements with wire-thermocouple instrumented wafers is limited by the physical characteristics of these contact sensors including shading of lamp power by the leads, temperature non-uniformity about the bead-wafer region, and heat transfer from the wafer by conduction along the leads. Further, traditionally used Pt/Pt-Rh thermocouples are not stable enough at the desired operating range of up to 1000 °C.

The goal of this research is to develop the measurement technologies required to measure wafer temperature and temperature gradients across the wafer during RTP as prescribed by the NTRS. At 1000 °C, the requirement is for an uncertainty of ±2 ° C and temperature gradients across the wafer of ±0.25 °C which is about of an order of magnitude tighter than what is widely practiced today.

Using the industry's wire thermocouple technology as the starting point, the NIST project seeks first to improve contact-sensor practice by demonstrating the reliability of thin-film platinum-palladium thermocouples. The thin-film thermocouples could supplant the wire-thermocouples used with proof or calibration wafers to obtain baseline operating data (temperature-time history and temperature distributions) on rapid-thermal processors. Using the reliable wafer temperature information from the proof wafer, the radiation thermometers can be calibrated *in-situ* so that the indicated spectral radiance temperature(s) can be related to the wafer temperature. In order that the measurement method is platform- and proof-wafer non-specific, procedures will be developed to account for wafer emissivity and chamber reflected-irradiation effects. Improved proof or calibration wafers are being assembled using elemental Pt/Pd wire thermocouples developed in a companion project (see page 16, "Improved High-Temperature Wire Thermocouple Thermometry") and Pt/Pd thin-film thermocouples developed last FY in this project.

An RTP Temperature Sensors Test Bed has been designed and is operational. It provides a well characterized radiation environment to evaluate thermocouple and radiometer temperature measurement methods. A major feature of the Test Bed is flexibility in configuring the wafer thermal surroundings in order to control and model stray (lamp, wafer, and wall components) radiation. The Test Bed will serve as a platform to characterize a new generation of imaging and optical-fiber radiation thermometers which equipment and instrument manufacturers are being challenged to develop. Another major use of the Test Bed is to generate data that can be used to develop and validate modeling tools which aid in establishing the reliability of new radiation thermometry approaches.

An Advisory Group, with membership from 20 companies representing RTP users and RTP equipment and instrumentation manufacturers, was established to serve as a bridge between the research community at NIST and industry practice, to provide project management with advice on shaping the research objectives, and to generate opportunities for collaboration and technology transfer. The Advisory Group held its organizational meeting at NIST on January 30th, 1997, and will meet semi-annually for the duration of the project.

The accomplishments planned by the end of the FY include: (1) benchmarking the thermal performance of the Test Bed with the aforementioned advanced features, (2) characterization and calibration of new radiation thermometers made available through two instrumentation-related CRADAs, and (3) intercomparison of three radiation thermometers with the new thin film thermocouples on the first- and second-generation proof wafers.

[Strong support for this effort appears on pp. 122 of the NTRS where it states, "RTP offers the potential to significantly reduce the thermal budget, while affording single-wafer granularity and cluster compatibility . . . . Improving of RTP temperature control ability...will be the key." This is underscored in Table 33 on pp. 124.]

Contacts: Robert D. Saunders, phone: (301) 975-2355, e-mail: robert.saunders@nist.gov
David P. DeWitt, phone: (301) 975-4199, e-mail: david.dewitt@nist.gov

High-Frequency Characterization of Interlevel Dielectrics for Integrated Circuits

Improved performance from both dielectrics and conductors will be a pivotal part of realizing the advantages of feature size scaling for interconnect-dominated chip designs. Lowering the dielectric constant of the intermetal dielectric is a favored approach. Many of the candidate materials for this application are "foreign" in the sense that they have not been widely used in IC fabrication before and are difficult to integrate into the process sequence.

The primary focus of this effort is to provide the metrology necessary to make sure that the performance of these new thin-film materials in propagating high-speed pulses on-chip live up to the promise that improvements in the low-frequency dielectric constant would indicate. This will be accomplished by making frequency-domain measurements on a series of simple transmission line structures fabricated with the materials in question and rigorously extracting both the real and imaginary parts of the complex dielectric constant as a function of frequency to 40 GHz.

A secondary focus of this effort is to provide metrology for electrically characterizing important interconnect structures, including transmission lines, discontinuities, and coupling. These electrical characterizations are intended for the analysis of high-speed digital pulse propagation in interconnect and packaging structures.

This work is an extension of earlier methods used to characterize microwave structures and takes advantage of existing measurement methods and software tools.

The effort in Calendar Year 1997 has focused on proving basic ideas and methods and developing collaborations to facilitate test structure fabrication. Work at NIST demonstrated basic methods for determining material parameters, characterizing transmission lines, and coupling between transmission lines. Tests on foundry-fabricated test structures with conventional oxide dielectrics have identified the major design and fabrication issues and have guided the current designs. NIST collaborated with a major semiconductor manufacturer to design and fabricate test structures for dielectric characterization; a second set of more complex structures focusing on interconnect characterization is planned as well. NIST has also begun test-structure layout with another major manufacturer.

[The use of low-k dielectric appears several times in the Potential Solutions roadmaps on pages 100-102. In the Priority of Technology Needs section (for interconnect) on page 103, it states, "It is expected that low dielectric-constant materials will have an even greater impact than low-resistance metals (on performance)".]

Contact: Dylan Williams, phone: (303) 497-3138, e-mail: dylan@boulder.nist.gov

Thin-Film Reference Materials

All of the layers which combine to make a modern IC can be generally characterized as thin films. Some of these layers, e.g., grown gate oxide, have limited structural possibilities and have evolved with multiple methods of characterization which can be cross-checked (in our example, ellipsometry and specific capacitance). Other critical layers, notably those used in the interconnect sequences, are deposited during processing, have a broad range of structural possibilities and are not amenable to in-situ metrology. In the latter case, having a well-characterized reference material for comparison which represents the proper structure and/or composition is invaluable as an analytical reference in manufacturing.

A prioritized list of needs for thin-film reference materials was developed in collaboration with the SEMATECH Analytical Lab Managers Working Group (ALMWG). Thin films of titanium nitride (100 nm thick), often used as diffusion barriers for interconnect, emerged as the top priority for development of a reference material.

NIST has set up facilities to deposit TiN films on silicon, has prepared samples, and has characterized them using a combination of X-ray methods. X-ray reflection is used to obtain the thickness of these films and thereby to calibrate X-ray fluorescence equipment commonly used for the same purpose. Thin-films of TiN on silicon were prepared, characterized, and distributed to the SEMATECH ALMWG for evaluation.

(It is important to note that these reference materials are not subject to same intense analysis and certification requirements as NIST Standard Reference Materials. Rather, it is intended that these be useful materials that are placed in user's hands in a timely fashion to address a series of short-term technology issues.)

[The impetus for NIST to develop these materials comes from a request by the SEMATECH ALMWG and supported by a letter by Jim Owens, SEMATECH COO, to Mr. Robert Scace at NIST dated September 13, 1995. Item 5 in the letter's attached table, "Metrology Capabilities for IC Manufacturing," specifically calls for TiN barrier layers. The details of this work were established by consensus vote within the SEMATECH ALMWG on 3/5/96.]

Contact: Dr. Richard D. Deslattes, phone: (301) 975-4841, e-mail: richard.deslattes@nist.gov

High-Resolution X-Ray Spectrometer for Chemical Analysis

The familiar energy dispersive X-ray spectrometer is an ubiquitous accessory to the scanning electron microscope (SEM). It provides fast, convenient elemental analysis of whatever the SEM is imaging. The conventional lithium-drifted silicon or germanium X-ray detectors used for these spectrometers limit the energy resolution to the order of 100 eV and tend to give noisy responses to the low energy X-rays emitted by important light elements used in device fabrication, e.g., boron, carbon, nitrogen, and oxygen.

NIST has used a microcalorimetry technique to create an entirely new X-ray detector with energy resolution about an order of magnitude better than can be achieved with conventional detectors. In fact, the resolution of the NIST microcalorimeter in energy dispersive mode rivals that of complex wavelength dispersive electron microprobes. Output of the NIST detector is compatible with the same multichannel analyzers used in conventional spectrometers. The improved resolution of the NIST microcalorimeter allows strongly overlapping X-ray peaks to be separated, e.g., the nitrogen K-line and the titanium L-lines in TiN. Improved resolution also suppresses the X-ray background at low energies, significantly enhancing the detectability of light elements.

The NIST instrument uses cryogenic techniques, and an important part of the development has been to build a refrigeration system that is small and robust for industrial use. The resulting detector is somewhat larger than conventional ones but has been successfully mated to the standard port of a commercial SEM.

Work in Calendar Year 1997 continues to be directed at hardening the instrument and improving the effective area of the detector to enhance the counting rate. Prelimary measurements for particle identification on test wafers will be performed. Efforts will be directed at constructing a user facility to be installed on a commercial SEM at NIST in Boulder, CO for use by industrial visitors.

[Detailed guidance regarding instrumentation is outside the scope of the NTRS. However, strong industrial support for this effort has been registered by the SEMATECH Analytical Lab Managers Working Group.]

Contacts: Richard E. Harris, phone: (303) 497-3776, e-mail: richard.harris@nist.gov
John M. Martinis, phone: (303) 497-3597, e-mail: john.martinis@nist.gov

Chemical Characterization of Thin Films and Particle Contaminants

Characterization of the elemental composition, crystallographic phase, and chemical structure of microelectronic components and particle contaminants at nanometer spatial resolution is necessary for understanding and improving the performance of advanced devices. NIST is meeting these needs by: (1) developing high-resolution Transmission Electron Microscopy (TEM) preparation and analysis methods; (2) comparing existing particle analysis methods with new approaches; (3) developing variable angle grazing incidence X-ray photoelectron spectroscopy (GIXPS); and 4) applying the methods to real analytical problems via collaborations with the semiconductor industry.

The TEM allows direct imaging and analysis of the complex interlayered structures composing microelectronic devices. We are applying elemental analysis using Electron Energy Loss Spectrometry (EELS) and X-ray spectrometry combined with near atomic resolution imaging of cross sections to characterize devices. We have analyzed reference materials and real silicon devices to provide a check for the assumptions and artifacts of bulk-macroscopic characterization techniques. For example, the TiN reference film developed at NIST is being characterized by X-rays at a macroscopic level and verified by TEM at the nanometer level. TEM specimen preparation and analysis methods are being improved to allow the higher level of specificity, sensitivity, accuracy, and precision needed to support the manufacture of advanced devices.

Particle contaminants during device manufacture are a significant source of device failure. Characterization of particle composition allows the fabrication facility to identify and control the particle source. Field Emission Gun Scanning Electron Microscopy (FEGSEM) has been used to characterize the number density and type of particle on contamination standards developed at NIST. We are testing and developing new analytical approaches for determining the elemental composition of particles using energy dispersive X-ray spectrometry on the FEGSEM.

GIXPS is used to explore chemical bonding with nanometer spatial resolution. Taking measurements at various grazing angles of the incident X-ray beam allows GIXPS to map the chemical bonding of a device as a function of depth. We are applying this technique to analyze the structure of thin oxide films on silicon devices and improving the technique by developing a synchrotron based GIXPS.

A collaborative effort between NIST and M.I.T. Lincoln Laboratories has been established to address problems in deep submicrometer CMOS process technology. Advanced processing technologies are being developed for silicon-on-insulator (SOI) CMOS devices by the Lincoln Laboratories group. The multidisciplinary state-of-the-art analytical tools available at NIST are being applied to performance-limiting factors such as dopant diffusion, materials characteristics, and quality of device features.

Contact: Eric Steel, phone: (301) 975-3902, e-mail: eric.steel@nist.gov

Appendix A: Abbreviations and Acronyms

AFM, atomic force microscope
ALMWG, Analytical Lab Managers Working Group
ASTM, American Society for Testing and Materials
BRDF, bidirectional reflectance distribution function
C-AFM, calibrated metrology AFM
C-V, capacitance voltage
CD, critical dimension
CFCs, chlorofluorocarbons
CFM, contamination-free manufacturing
CKMech, chemical kinetic mechanisms
CMOS, complementary metal-oxide semiconductor
CMP, chemo-mechanical polishing
CRADA, Cooperative Research and Development Agreement
CRDS, cavity ring-down spectroscopy
CVD, chemical vapor deposition
DIN, Deutsches Institut für Normung
DUV, deep ultraviolet
EBM, electron-beam moiré
EELS, electron energy loss spectrometry
EIA, Electronics Industry Association
FEGSEM, field emission gun scattering electron microscopy
FET, field effect transmitter
FIB, focused ion beam
GEC, Gaseous Electronics Conference
GIXPS, grazing incidence X-ray photoelectron spectroscopy
GOSI, goniometric optical scatter instrument
IEEE, Institute of Electrical and Electronics Engineers
IGBT, insulated gate bipolar transistor
IPC, Institute for Interconnecting Packaging and Electronic Circuits
ISO, International Organization for Standardization
JEDEC, Joint Electron Device Engineering Council
LFPG, low-frost-point moisture generator
LIF, laser induced fluorescence
MIT, Massachusetts Institute of Technology
NAA, neutron activation analysis
NIST, National Institute of Standards and Technology
NSMP, National Semiconductor Metrology Program
NTRS, *National Technology Roadmap for Semiconductors*
PEVCD, plasma enhanced chemical vapor deposition
Pt/Pd, Platinum/Palladium
RGAs, residual gas analyzers
RTP, rapid thermal processing
SCM, scanning capacitance microscope
SEM, scanning electron microscope
SEMATECH, SEmiconductor MAnufacturing TECHnology)
SEMI, Semiconductor Equipment and Materials International
SIA, Semiconductor Industry Association
Si, Silicon
SiO_2, Silicon dioxide
SIMS, secondary ion mass spectrometry
SOI, silicon-on-insulator
SOSI, scanning optical scatter instrument
SPM, scanning probe instruments
SRC, Semiconductor Research Corporation
SRM, Standard Reference Materials
SSM, scanning scattering microscope
TCAD, technology computer-aided design
TCR, temperature coefficient of resistance
TDDB, time-dependent dielectric breakdown
TED, transient-enhanced diffusion
TEM, transmission electron microscopy
TEOS, Tetraethoxysilane
TiN, Titanium nitride
UT, ultra-thin
UV, ultraviolet

Appendix B: Key Word Index