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Computer Systems Laboratory

Operating Principles of the VME MultiKron Interface Board

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ABSTRACT

The MultiKron* Experimenter's Toolkit contains the VME MultiKron interface board (MIB), installation software, data logging software, and analysis software; all of the software supplied is written in C. The Toolkit allows users to take advantage of the NIST MultiKron performance measurement chip in systems that do not already have a MultiKron designed into them. The MIB is applicable to both multiprocessor systems and single-processor systems. The Experimenter's Toolkit allows researchers to obtain hands-on experience with the MultiKron performance measurement chip, without the engineering effort required to design and build a hardware interface between the MultiKron and their computer. Up to one million Trace Samples can be collected during an experiment to the MIB on-board memory; a practically-unlimited number of Samples can be collected if an optional external data-collection computer is used.

Key words: Computers; hardware support; MIMD; multiprocessor computers; performance characterization; printed circuit board; PCB; VLSI

INTRODUCTION

The MultiKron* Experimenter's Toolkit contains the MultiKron interface board (MIB), installation software, data logging software, and analysis software. The MIB is to be inserted into the VME bus of the computer being measured. All of the software supplied with MultiKron Experimenter's Toolkit is written in C and distributed in source code. The Toolkit allows users to take advantage of the MultiKron [MIN92] performance measurement chip in systems that do not already have a MultiKron designed into them. The MIB is applicable to both multiprocessor systems and single-processor systems. The Experimenter's Toolkit allows researchers to obtain hands-on experience with the MultiKron performance measurement chip, without the engineering effort required to design and build a hardware interface between the MultiKron and

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* MultiKron is a trademark of NIST.

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their computer. Up to one million measurements can be collected, during an experiment, to the MIB on-board memory; a practically-unlimited number of measurements can be collected if an external data-collection computer is used.

During execution of a program under test, performance measurement data (Samples) are acquired as directed by measurement probes. A measurement probe is the code that generates a Sample. For the MultiKron this code is an assignment statement to a memory mapped address. An experimenter wishing to obtain performance measurements via the MIB must insert measurement probes at points in their program and recompile the program. The Samples acquired can be processed on the fly, using a separate data-logging computer. Otherwise they are processed, after program execution, by reading the Samples out of the MIB local memory. A MIB/MultiKron initialization routine and analysis program are supplied as part of the MultiKron Experimenter's Toolkit, but the experimenter can replace or modify them as desired.

FUNCTIONAL OVERVIEW

The MIB provides the necessary interfacing capabilities between a processor and the MultiKron via a standard VME bus, and provides MultiKron output data collection facilities.

CPU Interface

The MIB is memory mapped, so all interactions are memory reads and writes (i.e., assignment statements in high level languages) to addresses listed in Table 1. The VME bus is an I/O bus and thus is a bit slower than if the MultiKron were directly interfaced to the processor memory bus. The MIB provides facilities to control, access, and test the MultiKron from the processor being measured. The MultiKron uses 64-bit data transfers, while the VME-to-MIB path is 32-bit data. Thus the MIB provides a separate input register and an output register for the high order MultiKron data bits, during the 32 <--> 64 conversions. Since the largest MultiKron input data value is 48 bits, the MIB high-order input register has only 16 bits. The high-order output register has a full 32 bits. The experimenter should first load the 16 bit high-order input register and then write the low-order 32 bits directly to the MultiKron causing a full 48 bit input to the MultiKron. Similarly for output, the experimenter should read the low-order 32 bits directly from the MultiKron, which causes the 32 bit high-order output register to be loaded. Then the experimenter can read the 32 bit high-order register to obtain the rest of the MultiKron output data.

Although the MIB provides the facilities to use the full 64-bit data width of the MultiKron, the interface to the VME does not provide the mechanism to do so as an indivisible operation. Thus, if an interrupt occurs between writing the MIB high-order input register and writing the low-order data to the MultiKron, another MultiKron write may occur that will overwrite the high-order input register. A similar problem could happen to the high-order output register. If the computer being measured is a multiprocessor the problem is even more pronounced. It is up to the experimenter to guarantee that if full data width MultiKron I/O is being used, register overwrite will not occur. Because of the anticipated processing overhead to handle this indivisibility correctly, it is recommended that only 32-bit data fields be transferred to the MultiKron in time critical, Sampling operations. This reduces the range of values possible in Sampling data by wasting the upper bits of the data path. Less time critical operations, for example to the MUX Select register, should occur very infrequently and can endure the required overhead.

A MIB Control register and a MIB Status register provide the means for an experimenter to control the MultiKron (see Tables 2 through 5). The MIB Counter Input Register (Table 3) values provide program controlled incrementation of the external signal inputs to the MultiKron

Resource Counters if they are not incremented by external electrical connections. The MultiKron Resource Counters increment on the rising edge of an external signal. If MIB Counter Input Register is to increment the MultiKron Resource Counters then the appropriate bits in this register need to be toggled and the MultiKron needs to be properly configured. These bits must be cleared and set under program control, in that changing from a cleared state to a set state increments the Resource Counters. Bit 12 of the MIB Control Register selects whether the MultiKron Resource Counter external inputs are connected to the electrical MIB external input signals that the experimenter may configure, or to the MIB register of Table 3.

Bits 0-7 of the MIB Control Register (Table 2) represent the individual CPU ID signals to the MultiKron. The CPU ID signals are used in multiprocessor applications to identify which CPU triggered each measurement Sample and select the corresponding MultiKron Source Address Register to be included in that Sample. Assuming a single processor, one can permanently set CPUID = 01 (Hex), resulting in Source Address Register 0 being selected for each Sample. Bit 13 of the MIB Control Register select whether the MultiKron CPU ID inputs are connected to the electrical MIB external input signals that the experimenter may configure, or to bit 0-7 of the MIB Control Register of Table 3.

Bits 16 and 17 of MIB Control Register set the number of wait states for the MultiKron on all bus transfers. These values are read by the MultiKron only upon a reset, either a hardware reset or a software reset. For fastest operation a wait state = 01 is recommended, because the MultiKron may not operate correctly at wait state = 00, but works correctly for all other values.

Bit 20 of MIB Control Register is the output enable signal to the MultiKron. If this bit is off (= 0) then ALL MultiKron output signals are disabled.

Bits 11, 22 and 23 of MIB Control Register are related to the MIB local memory and are discussed below.

Bits 8, 9, 10, 18, 19 and 21 of MIB Control Register are used for testing and should always be in the operational state indicated in Table 2.

Output Data Collection

The MIB provides two ways in which to collect MultiKron output, selectable via the "LOCAL" option, bit 22 of the MIB Control Register. One can collect samples directly to the MIB local memory, which is accessable immediately, without any additional devices or wires. The second is to collect Samples on an external machine. In this case an external cable connects the MIB to a hardware interface, such as an S16D commercially available Sbus interface [EDT91], on another machine. Information will be supplied by NIST to allow the experimenter to obtain the correct cable and connector. Using the S16D interface option on the MIB allows experimenters to perform "on-the-fly" analysis of the measurement data and store more Samples than the local MIB local memory.

The MIB local memory contains 16 megabytes, and can store up to one million Samples (16 bytes per Trace Sample). This memory can be read and written directly by the CPU as 32-bit words. The MIB can be directed to transfer all MultiKron output Samples, through the MIB Control Register (see Table 2), to the MIB local memory for storage until an analysis program can read it out for processing. The MIB has a dedicated address pointer which it uses to linearly place Samples into the MIB local memory. The CPU can read this address pointer to find out how many Samples are in the local memory and where the last Sample is located. The CPU can also write to this address pointer, but this is primarily for testing purposes and it is not expected to be used operationally.

The MIB local memory can be configured as a simple buffer, or as a circular buffer, via the "NOWRAP" option, bit 23 of the MIB Control Register. As a simple buffer, loading starts at address 0 and ends at FFFFFF. Once the memory address pointer reaches its maximum value, it stops incrementing, and new writes are disabled. When used as a simple buffer, it is recommended that the "DROP" option, bit 11 of the MIB Control register, be enabled. This option will discard all new Samples arriving after the buffer is full. If this option is not enabled, then any Samples arriving after the local memory is full, will back up through the MultiKron's FIFO. As a circular buffer, loading starts at address 0, but upon reaching FFFFFF the memory address pointer "wraps around" to 0 and starts overwriting older data. The "DROP" option should be disabled in this mode. Thus, when configured as a simple buffer the MIB memory will retain the oldest data, and when configured as a circular buffer it will retain the newest data (the cockpit voice recorder mode).

Default Configuration

Initially, it is anticipated the experimenter will not connect any external input wires to the MIB. Therefore, the MIB Counter Input Register (see Table 3), should be set to 0000 (Hex) and the MIB Control Register (see Table 2), should be set to D50C01 (Hex). This configuration sets all the test controls to inactive. It stores MultiKron Samples in the local memory, treating it as a simple buffer and discarding any new Samples when the memory is full. All Samples are identified with CPU ID 0 (bit 0-7 of the MIB Control Register set = 01 (Hex)) and Source Address Register 0. It selects all MultiKron external Resource Counter signals to come from the MIB registers, sets the MultiKron wait states to 01, and enables MultiKron outputs. This is the default setting used by the initialization routine supplied with the Experimenter's Toolkit.

HARDWARE ARCHITECTURE

The MIB is designed to provide control, access, and testing of the MultiKron, and also to provide collection of the MultiKron output measurement Samples. The principal MultiKron signals are the address and data lines (used for processor interaction), the output network lines (for output of measurement Samples), the processor ID input lines (used to identify the CPU triggering a Sample), the resource counter external inputs (a MultiKron selectable option used to count external signal occurrences), and control lines (used for testing and initialization). A block diagram of the MIB is shown in Figure 1 and the printed circuit layout is shown in Figure 2. Processor access to the MIB is provided via the VME interface. The MIB and the MultiKron are memory mapped into the 32 bit memory address space. The MIB address and control decoders recognize MIB accesses and convert them into the specified MIB operations. Control, access, and testing of the MultiKron are supported through VME access and MIB registers. Two MultiKron output Sample collection methods are supported by the MIB. One method is to a MIB local memory, which requires a memory arbiter/controller and a memory address pointer. The other method is via an external cable connected to an S16D interface card [EDT91] on a separate SUN workstation. The architecture of these facilities are discussed more fully below.

The MIB is based on a synchronous design using its own 40 MHz oscillator to derive the various clocks used on the MIB and the MultiKron. All decoding and controls are implemented in programmable array logic (PAL) devices, which are installed via sockets on the MIB for easy replacement. Several unused spaces, with holes, were left on the MIB for the addition of chips for any future enhancements.

VME Interface

The MIB is 6U wide by 280 (mm) long, fits into a VME slot (a 9U adapter is available if required), and is designed as a simple VME slave device. All accesses to the MIB are a full 32

bits (the two least significant address bits are not used). The VMEbus must be configured for a full 32-bit address range to support access to all of the local memory. Block transfer requests are not implemented.

Address and Control Decoder

The VME address and control decoder is implemented in PALs that can be reprogrammed to accommodate different VME base addresses. The MIB requires a 2,000,000 (Hex) byte address allocation to simplify the address decoding. The default VME base address (physical address) is 20,000,000 (Hex). The MIB relative address mappings are listed in Table 1. All MIB accesses are word length (32 bits) and aligned on word boundaries.

MultiKron Data Bus Interface

In adapting MultiKron to a 32-bit bus, two MIB registers were provided to store the high order bit for reads and writes. The MIB high-order input register is connected to bits 32-47 of the MultiKron data bus, and is written (via bits 0-15 of the VME data bus) as the first part of a MultiKron write that will require 48 data bits. Currently, the largest MultiKron write is 48 bits. Writing to the MultiKron (with bits 0-31 of the data coming from the VMEbus) enables the 3-state outputs of the MIB high-order input register to be activated, transferring bits 0-47 simultaneously. If the MultiKron write only uses the lower 32 bits, no harm is done, since the MultiKron then ignores the upper bits. Therefore, it is not necessary to clear the high-order holding register after use. Care must be taken when performing 48-bit writes, since no locking mechanism is provided by the MIB to insure these two writes are indivisible. Due to the software overhead of implementing a locking mechanism in the CPU, it is recommended that for time critical MultiKron writes (such as Sampling), only 32 bits be used.

The MIB high-order output register is loaded with bits 32-63 from the MultiKron data bus on every MultiKron read, which places bits 0-31 on the VMEbus. If 64 bits of data are needed, then a second read is required from the MIB high-order output register. Again, care must be taken when doing 64-bit reads since no locking mechanism is provided by the MIB to insure these two reads are indivisible, since the high-order read register is updated on every MultiKron read.

MultiKron CPU ID Signals

The processor ID lines (also called CPUID) are used to allow hardware identification of individual processors in multiprocessor environments. In its intended use, this feature has two functions: (1) it is encoded in a three-bit field in the Sample header to identify the processor taking the Sample (up to eight processors are supported by the current MultiKron), and (2) it selects the contents of one of the eight 32-bit Source Address registers to be placed in the Sample. The MultiKron Source Address registers are written before sampling starts and should be updated on context switches. They are intended to contain the node number (if applicable) and the process identification of the process writing the Sample. The processor ID input consists of eight input lines--one per processor, so only one line may be asserted at any time. The MIB provides for two options to drives these lines: (1) a MIB register--bits 0-7 of the Control Register, or (2) alternatively a MIB connector for external signal lines for hardware identification of the active processor. EXT_CPU, bit 13 of the Control Register (see Table 2) controls this selection. The connector option will require custom wiring to the connector and consultation with NIST to obtain the connector specification. For single processor machines, the MIB register option should be selected and initialized once. The effect is to select a single MultiKron Source Address Register for all Samples.

MultiKron External Counter Signals

The MultiKron external inputs are one of the selectable counting sources for the MultiKron Resource Counters. The MIB provides for two options to drive these lines: (1) a MIB Counter Input Register, or alternatively (2) a MIB connector for external signal lines. EXT_RSC, bit 12 of the Control Register (see Table 2), controls this selection. The connector option will require custom wiring to the connector and consultation with NIST to obtain the connector specification. The sixteen inputs must either all come from the external connector, or all be driven by the MIB Counter Input Register. The MultiKron Resource Counters are edge triggered, so they increment once per positive edge transition (i.e., changing from 0 to 1) of the corresponding input lines. If MIB Counter Input Register is selected as the source of these signals then the CPU must toggle (i.e., clear to 0 and and then set to 1) the data values in this register to simulate a positive edge transition. This MIB register is intended for testing only.

MIB FIFO

The MultiKron output network sends measurement Sample data to the MIB FIFO, which is 16 bits wide by 1024 ranks deep. Each transfer consists of eight data bits along with an "end of Sample" flag and an odd parity bit. Thus 6 of the 16 MIB FIFO bits are not used. The MIB FIFO provides buffer storage for up to 64 Trace Samples, to improve peak Sample rate performance and reduce the risk of Samples being lost due to collection delays. For diagnostic purposes, there are MIB commands to block the flow of data from MultiKron to the MIB FIFO, or to allow data to pass through one byte at a time.

The input and output of the FIFO are synchronous and independent of one another. A 20 MHz MIB FIFO write clock is produced by the MultiKron. The FIFO read clock is either 20 MHz when writing Samples into the MIB local memory, or 10 MHz when writing Samples to the external SBus interface. The FIFO full flag generated by the FIFO input logic is fed into the MultiKron, where it can stop further MultiKron output when the MIB FIFO is full. The MultiKron can continue to generate Samples until its small internal FIFO is filled, at which point it either forces the processor/VMEbus to wait until room is available or discards new Samples and sets an error flag. The course of action to take is determined by the configuration instructions which are written to the MultiKron prior to Sampling. The FIFO empty flag generated by the FIFO output logic is used to determine whether there is data available to read. This data will either be sent out over the external cable (16 bits at a time) to an SBus interface or written into the MIB local memory (32 bits at a time), depending on the MIB configuration option selected.

FIFO Testing

A test option, Single Pulse Mode (SPM) has been provided, in which the low active FIFO full (FFB) signal is blocked, and a single byte of Sample data is transferred from the MultiKron into the MIB FIFO each time the FPULSE command is activated (MultiKron-->FIFO). Each write to the MIB FPULSE address (see Table 1), causes a single activation of the FPULSE command.

A MIB Control Register option, MANPUL, causes the next entry in the MIB FIFO to be shifted out and placed on the VMEbus to be read by the processor (FIFO-->VME). A shiftout occurs only when the value of MANPUL is set to 1 (leading edge). MANPUL must be cleared before it can be set again.

A MIB Control Register option, MANSW, transfers the next four entries in the MIB FIFO to the MIB local memory (FIFO-->local memory). Although a FIFO entry is 16 bits, only 8 bits are Sample data. Two bits are an "End-of-Sample" flag and a parity bit. The remaing 6 bits are

not used. Thus four FIFO entries are combined into one 32 bit memory word. This transfer occurs regardless of enables or whether there is room in memory. However, there must be data in the FIFO.

External Sample Interface

The External Sample Interface provides the logic needed to extract two MIB FIFO bytes, combine them into a single 16-bit value and send it over an external cable to an S16D interface [EDT91], a commercial SBus I/O interface board, installed on another machine. The S16D board plugs into an SBus slot of the external data collection computer. Using the S16D interface option on the MIB allows experimenters to perform "on-the-fly" analysis of measurement Samples and also store more Samples than the MIB local memory. The average Sample collection rate is slower via the S16D option than the MIB local memory.

MIB local Memory

The 16 Mbyte MIB memory is configured as four banks of 1M x 32 bits. Four entries are extracted from the FIFO and combined into a 32 bit word and then written into the local memory via a pipeline holding register. Although a FIFO entry is 16 bits, only 8 bits are Sample data. The MIB local memory requires 24 VME address bits to access any 32-bit word, 2 bits for bank select and 20 bits for word select, and 2 bits for byte level addressing. Since these are word accesses aligned on word boundaries, the byte level address is always 00. The MIB local memory may be accessed via the VMEbus at any time, since memory arbitration will interleave VME access with Sample storage. VME memory write is provided for testing the memory.

Dynamic random-access memory (DRAM) is used for the local memory because it is economical and the low power consumption reduces heating as a problem. The memory is made up of 32 1M x 4bit DRAM chips. The chief disadvantages of DRAM are typically slower access than fast static RAM, and the need for periodic refresh. The 1M x 4 DRAM chips have 1024 refresh addresses, each of which must be refreshed at least once every 16 milliseconds. A commercial DRAM controller chip transparently provides the refresh accesses.

A 24-bit counter serves as the memory address pointer for Sample storage; the VME address is used for processor access. In principle, this counter may be read or written by the processor at any time. However, since a write to the counter while it is storing MultiKron Samples could cause the stored Samples to be scrambled, a safety interlock has been programmed into the controlling PAL which causes a VME bus timeout error if this occurs. If there is a need to write to the counter during the course of an experiment, the user should disable Sampling, wait for any Samples enroute to be safely written, write the new count, then re-enable Sampling.

Before Sampling begins, the user should initialize the MIB memory address pointer. The initialization code distributed with the Experimenter's Toolkit provides for this initialization. The user can read the memory address pointer during the experiment to determine how much of the memory space has been written. The memory address pointer, points to the next available memory location.

In the simple buffer mode, Sample writing is halted when the memory is full. If new Samples continue to be generated, the MIB FIFO will eventually fill and stop accepting data from the MultiKron. The MultiKron will then fill up its small internal FIFO, and either stop generating new Samples or cause a VME bus timeout error, depending on how the MultiKron is configured [MIN92]. A MIB option (DROP, see Table 2) will discard any new Samples in the MIB FIFO once the local memory is full. Alternatively, the MultiKron option to discard Samples when its internal FIFO is full could also be used.

In the circular buffer mode, when the memory is full, Sample writing continues from the beginning of memory by wrapping the memory address pointer around to zero, overwriting the oldest Samples and thus retaining the most recent Samples generated. The MIB "memory full" flag in the MIB Status register indicates whether a wraparound has occurred.

REFERENCES

[MIN92] Mink, A., and Carpenter, R. J., "Operating Principles of MultiKron Performance Instrumentation for MIMD Computers," National Institute of Standards and Technology, NISTIR 4737, Mar. 1992.

[EDT91] Engineering Design Team, Inc., "S16D High Speed 16-bit I/O Interface for the SUN SPARCstation--User's Guide," 1100 NW Compton Dr, Beaverton, OR 97006, July 1991.

TABLE 1. MultiKron Interface Board Address Map

Byte addresses in Hex, relative to installed base address

ADDRESS	Description
	READ/WRITE
0,000,000 - 0,FFF,FFC	MIB Local Memory
1,000,000 - 1,000,1FC	MultiKron
	WRITE Only
1,000,400	MIB Control register
1,000,404	MIB Counter Input register
1,000,408	N/A
1,000,40C	N/A
1,000,410	Sample address pointer
1,000,414	16 bit High-Order MultiKron Input Data register
1,000,418	"FPULSE" - Do one "manual" MultiKron Network transfer to FIFO (use for testing)
1,000,41C	RESET MIB and MultiKron
	READ Only
1,000,500	MIB Status register
1,000,504	MIB FIFO TEST register
1,000,508	N/A
1,000,50C	N/A
1,000,510	Sample address pointer
1,000,514	32 bit High-Order MultiKron Output Data register
1,000,518	Board Version Number (03 Hex)

TABLE 2. MIB CONTROL Register (Write Only)

at relative address: 1,000,400 (Hex); Recommended DEFAULT value = D50C01 (Hex)

Bits	Name	Description
0-7	ICPU[7..0]	CPU ID to MultiKron (multiplexed with XCPU[7..0] via EXT_CPU)
8	*MANPUL	Used for testing--operationally set to 0 "manually" read the next entry out of the MIB FIFO to the VME
9	*MANSW	Used for testing--operationally set to 0 "manually" move the next four entries out of the MIB FIFO and into the local MIB memory (use with LOCAL = 1, MEMW = 0)
10	*MEMW	Used for testing--operationally set to 1 1 = enable sample storage to local MIB memory
11	DROP	1 = discard samples if local MIB memory is full
12	EXT_RSC	Select the source of the MultiKron resource counters' external inputs 1 = use MIB external inputs XRC[15..0] 0 = use IRC[15..0] from the MIB Counter Input register
13	EXT_CPU	Select the source of the MultiKron CPU ID inputs 1 = use MIB external inputs XCPU[7..0] 0 = use ICPU[7..0] from the MIB Control register
14-15	-	N/A
16-17	WAIT[1..0]	Number of MultiKron Wait States (use = 01)
18	*NOTESTB	Used for testing--operationally set to 1 0 = places MultiKron into TEST mode
19	*TEST2	Used for testing--operationally set to 0 1 = enables MultiKron internal TEST2 mode with output data on TST[7..0] of the MIB Status register Note--Select inputs are LOW-active in TEST2, so X[15..0] should be HIGH before entering TEST2 mode
20	OUTEN	1 = enable MultiKron outputs (if Low ALL outputs are disabled)
21	*SPM	Used for testing--operationally set to 0 Controls MultiKron network data transfer to MIB FIFO 1 = single pulse mode--a write to MIB address 1,000,018 causes a single transfer 0 = normal mode--transfers to MIB FIFO are automatic
22	LOCAL	1 = MultiKron samples are stored in local MIB memory (MEMW=1), 0 = MultiKron samples are sent to the output network
23	NOWRAP	1 = MIB memory configure as a simple buffer (use with DROP enabled to discard samples) 0 = MIB memory configure as a circular buffer (use with DROP disabled)

*used for testing only

TABLE 3. MIB COUNTER INPUT Register (Write Only)

at relative address: 1,000,404 (Hex)

Bits	Name	Description
0-15	IRC[15..0]	Alternative for MultiKron Resource Counters' external input if no actual external signals exist.

TABLE 4. MIB STATUS Register (Read Only)

at relative address: 1,000,500 (Hex)

Bits	Name	Description
0-7	TST[7..0]	MultiKron test output data when in TEST2 mode
8	-	N/A
9	EFB	0 = MIB FIFO is empty (poll this bit when the CPU reads Samples from the MIB local memory)
10	FFB	0 = MIB FIFO is full
11	NETRDY	Normally matches FFB from MIB FIFO, allows MultiKron Samples to be written to the MIB FIFO
12-15	WSB[3..0]	While assembling 4 bytes of MultiKron sample from MIB FIFO which byte is next (0 = MSB)
16-18	-	N/A
19	SMWREQ	1 = MultiKron Sample transfer to local MIB memory in progress
20	-	N/A
21	MEMFULL	1 = MultiKron Samples have completely filled local MIB memory (subsequent samples discarded or blocked, depending on DROP)
22-23	-	N/A

TABLE 5. MIB FIFO TEST Register (Read Only)

at relative address: 1,000,504 (Hex)

Bits	Name	Description
0-15	FQ[15..0]	Read output of MIB FIFO, following enabling of MANPUL bit in MIB Control Register when in local mode

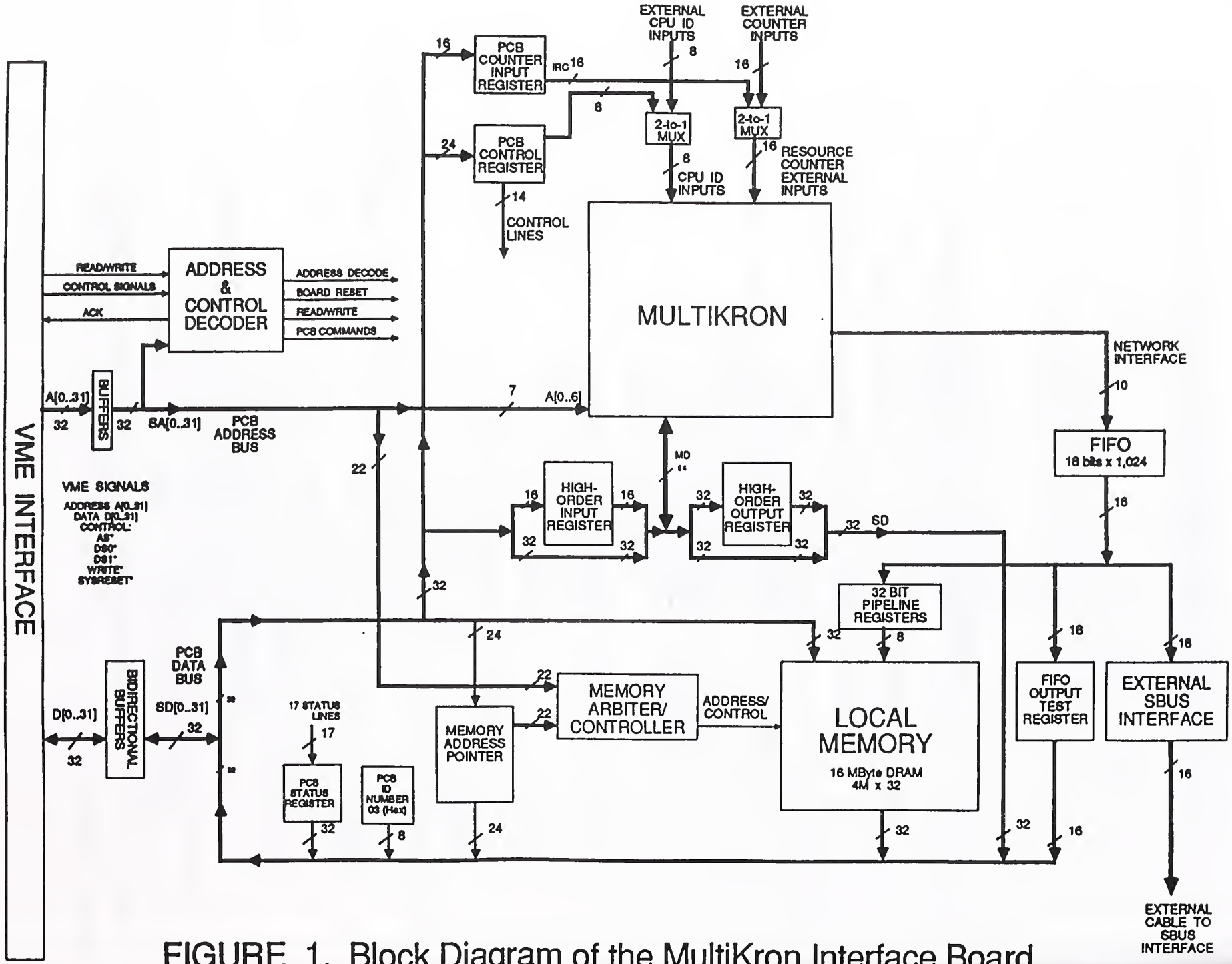

FIGURE 1. Block Diagram of the MultiKron Interface Board.

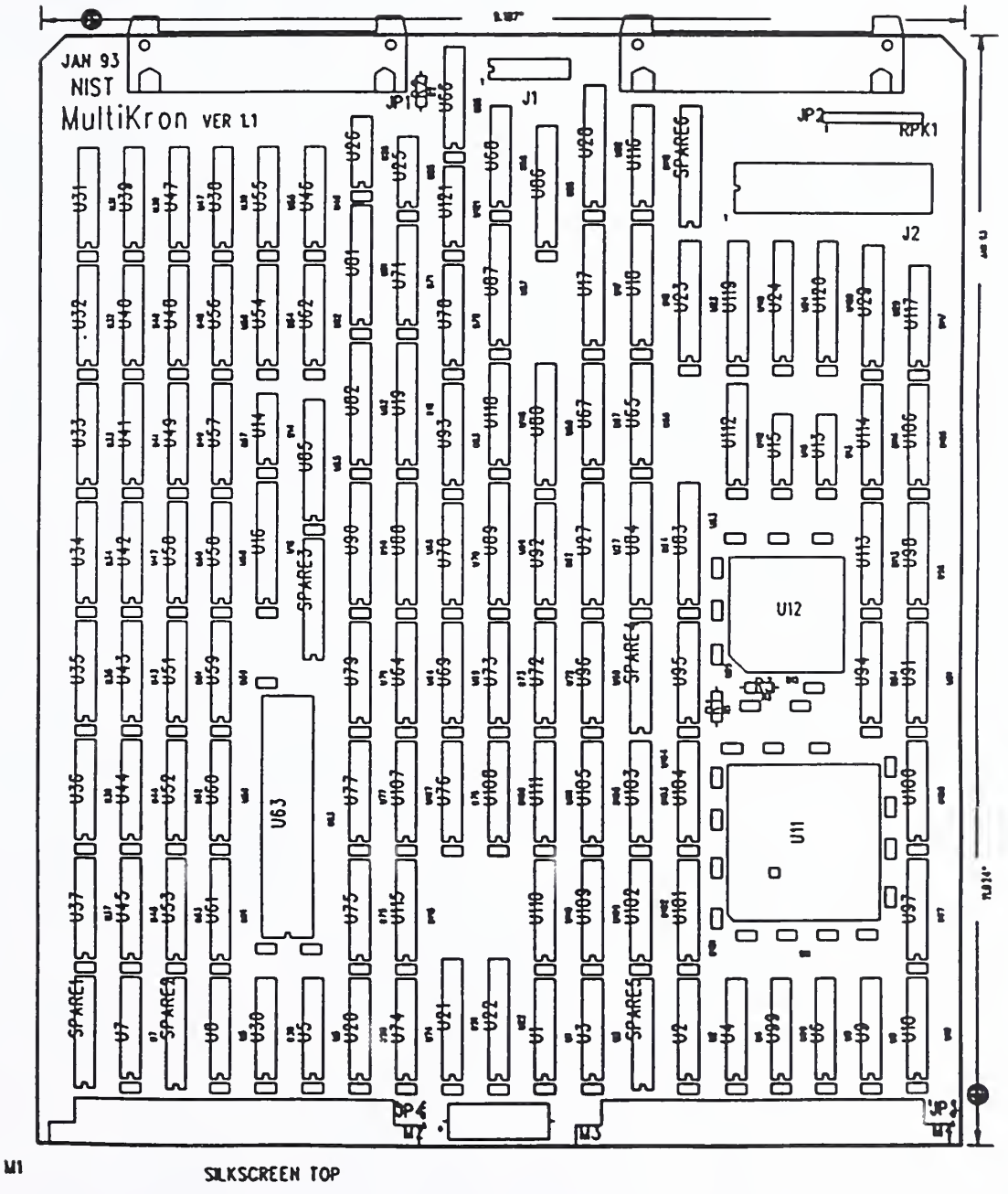

FIGURE 2. Layout of MultiKron Interface Board.